UNITED STATES PATENT AND TRADEMARK OFFICE

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BEFORE THE PATENT TRIAL AND APPEAL BOARD

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SK HYNIX INC. and SK HYNIX AMERICA INC.,
Petitioners,

v.

NETLIST, INC.
Patent Owner.

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Case No. IPR2020-01044
U.S. Patent No. 9,858,218

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# DECLARATION OF ROBERT J. MURPHY

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I, Robert J. Murphy, make this declaration in connection with the proceeding identified above.

## I. INTRODUCTION

1. I have been retained by counsel for Netlist, Inc. ("the Patent Owner") as a technical expert in connection with the proceeding identified above. I submit this declaration in support of Patent Owner's Response to the Petition for *Inter Partes* Review of United States Patent No. 9,858,218 ("the '218 Patent"). I have been retained to provide a technical opinion concerning the '218 Patent, and certain prior art references cited in the above-captioned *Inter Partes* Review proceeding, which are discussed in further detail below.

## II. EXPERT QUALIFICATIONS

2. I have over forty-four years of experience in the semiconductor industry, and have experience in the design of high speed, high complexity semiconductor products, including Full Custom Microprocessors, E2CMOS and BiCMOS PALs, CMOS and NMOS SRAMs (Static Random Access Memory), CCDs, DRAMs (Conventional and Pseudo-Static), and RAD Hard SOS CMOS.

3. I earned a Bachelor of Science Degree in Electrical Engineering in 1974 from Drexel University, in Philadelphia, Pennsylvania. I earned a Master of Science Degree in Electrical Engineering in 1976 from the University of California, Los Angeles.

4. Since January, 2021 I have been employed as the VP of Engineering for IC Manage a company that makes software tools to assist in the design of Integrated Circuits.

5. Before that, since 1998, I have been self-employed in my own consulting business known as Firenza, LLC, which is an outsource engineering design company that assists in the design and implementation of semiconductor devices. Additionally, I perform expert witness work as available. For example, I was an expert witness or consultant for Netlist in the related matters of *In the Matter of Certain Memory Modules and Components Thereof, and Products Containing Same,* Inv. No. 337-TA-1023 (USITC filed September 1, 2016), *In the Matter of Certain Memory Modules and Components Thereof, and Products Containing Same,* Inv. No. 337-TA-1089 (USITC filed October 31, 2017) and *Inter Partes* Reviews of related U.S. Patent No. 8,489,837 ("the '837 Patent"), Case No. IPR2017-00548, and U.S. Patent No. 9,535,623 ("the '623 Patent), Case No. IPR2017-00303.

6. Before founding Firenza, LLC, I was Director of Engineering at Silicon Graphics, Inc. ("SGI") in Mountain View, California. I was employed with SGI from June 1992 through April 1998. I was involved in the hiring, management and direction of circuit engineers in processor and floating point chip designs. I also assisted in the design of phase locked loops ("PLL").

7. Prior to SGI, I worked with Weitek Corporation in Sunnyvale, California, from February 1989 to June 1992, achieving the position of Director of Engineering in 1990. While at Weitek, I was charged with, among other things, the responsibility for designing circuitry to implement high performance memory, output drivers, and electrostatic discharge (ESD) devices. Examples include a 40 MHz SPARC combined IU/FPU product and a floating point coprocessor compatible with the Intel i486.

8. Before Weitek, I was employed by National Semiconductor Corporation in Santa Clara, California from October 1985 through February 1989. I achieved the position of design manager and chief technical contributor for their E2CMOS PAL group. Significant design projects included the world's first BiCMOS PAL, and improved Ti-W fuse blowing circuitry. Prior to my employment with National Semiconductor, I worked with RCA in Sommerville, New Jersey from April 1982 to October 1983. There, I led an inter-divisional program to develop 2 micron CMOS technology, and also helped design a 64K SRAM (Static Random Access Memory).

9. Prior to RCA, I was an SRAM design manager with National Semiconductor in Santa Clara, California and West Jordan, Utah from February 1978 to April 1982. I directed the design of a 4T cell 4K SRAM product, and was promoted to Section Head when my first design went into production on the first

mask set. I was later promoted to Design Manager. My first design at National was a Pseudo-Static DRAM. Before National Semiconductor I worked for Hughes Aircraft in El Segundo, California from June 1974 to February 1978. This began as a part-time position, wherein I worked as a Test Engineer testing space flight sub-assemblies, and later became an integrated circuit designer, all while obtaining my Master's Degree.

10. My professional background and technical qualifications are stated above and are reflected in my Curriculum Vitae, attached as Appendix A to this Declaration.

11. I have no personal or financial stake or interest in the outcome of the present *inter partes* review.

12. This declaration is based on information known to me as of the date of this declaration, and I reserve the right to modify or expand upon my opinions based on new information and in response to additional discovery, rulings, declarations and testimony. I have not previously testified as an expert witness at trial, hearing, or by deposition during the last four years, other than what is disclosed on my C.V. and in this declaration.

## III. MATERIALS CONSIDERED

13. In forming the opinions set forth in this declaration, I have considered and relied upon my education, knowledge of the relevant field, and my experience. I

have also reviewed and considered the specification of the ’218 Patent and the prosecution history of the ’218 Patent. I understand that SK hynix Inc., SK hynix America Inc., and SK hynix memory solutions Inc. (collectively, “Hynix” or “Petitioner”) have requested *inter partes* review of the ’218 Patent in a Petition dated December 17, 2020. I understand that the December 17 Petition was accompanied by an expert declaration by Dr. Donald Alpert (Ex. 1003, “Alpert Declaration” or “Alpert Decl.”) dated June 8, 2020. I have reviewed both the Petition and the Alpert Declaration.

14. I understand that, in the Petition, Hynix requests the Patent Trial and Appeal Board (“the Board”) to institute an *inter partes* review as to claims 1-24 of the ’218 Patent based on references cited in the Petition. I have reviewed and am familiar with those references, which include:

- U.S. Patent Application Publication No. 2008/0098277 to Hazelzet (“Hazelzet”);
- JEDEC Committee Letter Ballot, Committee: JC-40.4, Committee Item Number: 142.35 (“JEDEC”);
- U.S. Patent No. 8,139,430 to Buchmann et al. (“Buchmann”);
- U.S. Patent No. 8,359,521 to Kim et al. (“Kim”);

## IV. DEFINITIONS AND STANDARDS

15. I have been informed and understand that claims are construed from the perspective of a person of ordinary skill in the art ("POSITA") at the time of the claimed invention. I understand that, in this proceeding, the claims should be given their ordinary and accustomed meaning as understood by one of ordinary skill in the art in view of the patent and its file history.

16. With respect to anticipation under 35 U.S.C. § 102, I have been informed that a single reference must describe the claimed invention with sufficient precision and detail to establish that the subject matter existed in the prior art. I understand that a vague or ambiguous teaching that neither discloses nor enables the claimed invention cannot anticipate the invention. I understand that a limitation may be deemed inherently disclosed in a prior-art reference, but only if it is necessarily present in the prior-art reference, as opposed to being merely probable or possible.

17. I have also been informed and understand that the subject matter of a patent claim is obvious under 35 U.S.C. § 103 if the differences between the subject matter of the claim and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a POSITA. I have also been informed that the framework for determining obviousness involves considering the following factors: (i) the scope and content of the prior art; (ii) the

differences between the prior art and the claimed subject matter; (iii) the level of ordinary skill in the art; and (iv) any objective evidence of non-obviousness. I understand that the claimed subject matter would have been obvious to a POSITA if, for example, it results from the combination of known elements according to known methods to yield predictable results, the simple substitution of one known element for another to obtain predictable results, use of a known technique to improve similar devices in the same way or applying a known technique to a known device ready for improvement to yield predictable results. I have also been informed that the analysis of obviousness may include recourse to logic, judgment, and common sense available to the person of ordinary skill in the art that does not necessarily require explication in any reference.

18. I understand that 35 U.S.C. § 112 imposes a "written description" requirement on patentees. I understand the "written description" requirement is met if a person of ordinary skill in the art would have understood the inventor to have been in possession of the claimed invention at the time of filing, even if every nuance of the claims is not explicitly described in the specification.

## V. LEVEL OF ORDINARY SKILL IN THE ART

19. I understand that U.S. patent law interprets patents and prior art from the point of view of a hypothetical person of ordinary skill in the art ("POSITA").

20. The field of the ’218 Patent includes memory module initialization and training sequencing. Professionals in these fields will generally be electrical engineers, computer engineers, or computer scientists.

21. I understand that the Patent Owner has previously proposed that a person of ordinary skill in the art for a related proceeding would have a Bachelor’s degree in electrical engineering, computer engineering, or in a related field and at least one year of work experience relating to memory systems, and would be familiar with the design of memory devices and modules.

22. In my review of the ’218 Patent, from my education, from my knowledge of the relevant field, and my experience, and for the same reasons stated above, I agree with the Patent Owner’s proposal for the level ordinary skill in the art. I meet these criteria under both the Petitioner’s proposed level of skill and the Patent Owner’s proposed level of skill. I consider myself to be a person with at least ordinary skill in the art pertaining to the ’218 Patent. In addition, I was a person of ordinary skill in the art at the time of invention of the ’218 Patent. I reserve the right to challenge Dr. Alpert’s definition of a person of ordinary skill in the art in this proceeding.

23. I see that Dr. Alpert disputes the effective filing date of the ’218 Patent. (Ex. 1003, Alpert Decl., ¶ 43). The effective filing date of the ’218 Patent is

June 12, 2009, and I will support that conclusion in a later section of this declaration.

## VI. CLAIM CONSTRUCTION

24. I understand for that Hynix has provided some constructions of certain claim terms. For the purposes of this declaration, I do not see the need to offer any claim constructions or respond to Hynix's claim constructions. I reserve the right to offer claim constructions and address Hynix's claim constructions in this proceeding.

## VII. RELEVANT INFORMATION CONCERNING THE '218 PATENT

### A. The Correct Priority Date of the '218 Patent is June 12, 2009

25. I have been asked to opine on the priority date of the '218 Patent. I understand that Petitioners and their expert argue that the '218 Patent is not entitled to its priority date of June 12, 2009 because they claim certain claim elements are not disclosed in the Provisional Application. (Pet. at 4-9; Ex. 1003 at ¶¶ 43-51). I disagree. A review of the Provisional Application shows that there is written description for all of the disputed claim elements.

#### 1. The '218 Patent Claims Reciting That the First Edge Connections Are not Active Are Supported By the Priority Application

26. In my opinion, the Petition incorrectly asserts that the claim element "train[ing] with one or more training sequences while the first edge connections

are not active," is not sufficiently disclosed in the Provisional Application. (Pet. at 4-7).

***a. The priority application provides written description support for this claim***

27. The Priority Application discloses that that the MCH is idle while then-current LRDIMMs complete their tasks (e.g., training). (Ex. 1008 at 22) ("Although the notifying method is an advantageous handshaking method between the MCH and the memory subsystem controller, the LR-DIMM proposal requires the MCH to insert a waiting period. The shortcoming of the current the LR-DIMM proposal is that, instead of adopting the notification, the proposal requires the MCH to be in standby (idle, or wait) while the memory subsystem controller completes its task.").

28. Among its other disclosures, the Priority Application discloses the use of a notification signal to allow the MCH to execute independent commands instead of idling while the memory module performs training. (Ex. 1008 at 22) ("In the notifying method, the memory subsystem controller sends a signal to the MCH when it completes the required or requested operation. This method allows the MCH to execute independent command while it is waiting for a notification signaling for the memory subsystem controller.").

29. A POSITA would understand that allowing the MCH to execute independent commands means allowing the MCH to perform other tasks unrelated to the memory module undergoing training. (Ex. 1008 at 23) ("In certain embodiments in which more than one memory subsystem is connected to the MCH, each controller that associates with each memory subsystem drives the notifying signal pin to the high impedance state from the low impedance state when it completes the required operation. Thus, it provides the condition that the MCH can only pull the notifying signal high when all memory subsystem controllers are done with the required operation. This method allows the MCH to work with a non-homogenous memory subsystem, such as mixing of DIMMs with different DIMM density, ranks, DRAM density, speed, DRAM configuration, etc.").

30. The Priority Application further discloses that, when the memory module is undergoing training, the Error-Out pin is pulled Low, and when the memory module is in normal operation, the Error-Out pin is pulled High. (Ex. 1008 at 23 and Fig. 3 (stating that the error-out pin is "Low during MB training" and "High during normal operation unless parity error occurs")). Therefore, the memory module undergoing training is not accessed for normal read or write operation. (Ex. 1008 at 23).

31. Before the MCH receives a notification signal from a memory subsystem performing training operations, it can perform independent operations that are unrelated to the memory subsystem. When the MCH is performing these independent operations, it is ***not*** performing operations with the memory module that is performing training. *Id.* The priority application further discloses that "the notification of completion of the required or requested task from the memory subsystem controller would generate an interrupt to the system ***during the initialization period*** as error occurrence generates an interrupt to the system ***during the normal operation****"* (emphasis added). Thus, the priority application draws a clear boundary between initialization and normal operation.

32. The passages above provide the "necessary information" to a POSITA that the '595 patent claims reciting that the priority application provides written description support for the '595 claims reciting that a memory controller not access the module for memory read and write operations in the second mode.

33. The Petition corroborates this. (Pet. at 6 ("Moreover, it was known before the 2009 provisional filing date that ***some training*** included sending data over the data edge connections, while ***other training did not***."); *id.* ("It was known, however, that such buffers employed memory read and write operations instituted by the memory controller that transferred data over the edge connections with the data pins ("*first edge connections*") during ***some*** training modes.")). Setting aside

the fact that Petitioners and Dr. Alpert cite no evidence for their speculation, the statement actually proves Patent Owner's point. The Petition confirms that a POSITA would have clearly known that some training may have involved active data pins, while other types of training clearly would not. *Id.*

34. Thus, in my opinion, the Provisional Application reasonably conveys to a POSITA that the first edge connections include one or more pins that are inactive during training. Having been disclosed, it is proper to claim.

#### 2. The Provisional Application Supports the '218 Patent Claims Reciting Performance of One or More Memory Read or Write Operations Not Associated With the One or More Training Sequences

35. In my opinion the Petition incorrectly asserts that "configured to perform one or more memory read or write operations not associated with the one or more training sequences," as recited in each claim 1 of the '218 patent, is not sufficiently disclosed in the Provisional Application. (Pet. at 7-8).

##### *a. The priority application provides written description support for this claim*

36. In my opinion, the priority application explicitly discloses two modes of operation: training and normal. (Ex. 1008 at Fig 3. and pp. 22-23). The priority application then explains that memory modules performing MB training can output a low signal during MB training and that a high signal can indicate that ***training is***

***done***. (Ex. 1008 at Fig. 3). This unambiguously conveys to a POSITA that when training is ***done***, the module will be in normal operation without training.

37. Further, the priority application starts with the sentence: "Certain embodiments described herein provide a method of providing a feedback path from a memory subsystem to the MCH (Memory Controller Hub, e.g., system memory controller) ***during initialization***" (Ex. 1008 at 22), and then goes on to state that, "[i]n general, there is no method of handshaking between the MCH and a memory subsystem ***during initialization***…" (Ex. 1008 at 22) (*emphasis added*). The priority application is clear that the method of providing a feedback path in certain embodiments is performed "during initialization." A POSITA undoubtedly recognizes that when the memory subsystem is being initialized, it is ***not*** ready for memory operation, and thus is ***not*** accessed by the MCH for read or write operations.

38. The priority application also discloses that "the notification of completion of the required or requested task from the memory subsystem controller would generate an interrupt to the system ***during the initialization period*** as error occurrence generates an interrupt to the system ***during the normal operation****"* (Ex. 1008 at 24) (emphasis added). Thus, the priority application draws a clear boundary between initialization and normal operation.

39. In view of these disclosures, a POSITA would clearly understand that, when a memory module is performing training, it is ***not*** accessed by the MCH for read or write operations. This, alone, provides written description support, because a POSITA would understand that the priority application discloses the performance of normal read or write operations that are not associated with training.

#### *b. Petitioners and Petitioners' expert corroborate that written description support exists for this claim*

40. Petitioners and their expert, Dr. Alpert, corroborate that all the parts of that claim element would have been known to a POSITA when reading the Provisional Application. Petitioners' only argument is that training ***could*** occur during normal operation. (Pet. at 7 ("In fact, as Dr. Alpert explains, a Skilled Artisan would understand training ***could*** occur during normal operation.")) (emphasis added). Petitioners' expert, Dr. Alpert, testified similarly. Ex. 2026 at 31:10-32:4 (explaining that it is not the case that training can never be done in normal operation). Setting aside the fact that Petitioners' argument is ***not*** disclosed in the priority application and they cite no evidence to substantiate their speculation, it actually proves Patent Owner's point. Through their statements, Petitioners and their expert tacitly concede that a POSITA would understand that training typically does not occur during normal operation—it just is not the case that training can never occur during normal operation. *Id.* This serves as an explicit

message to a POSITA that the Provisional Application discloses normal read or write operations that are not associated with training.

### 3. The Provisional Application Supports the '218 Patent Claims Reciting "One or More" Training "Sequences"

41. In my opinion, the Petition incorrectly asserts that "one or more" training "sequences," as recited in each independent claim of the '218 patent, is not sufficiently disclosed in the Provisional Application. (Pet. at 8-9). Petitioners' and Dr. Alpert's argument as to why "one or more training sequences" is not disclosed is that the provisional application "only discloses 'MB Training.'" (Pet. at 8-9). In my opinion, Petitioners' and Dr. Alpert's, argument fails.

42. To start, Petitioners' expert, Dr. Alpert, admitted that a POSITA would understand that the provisional application discloses "multiple different types of training." (Ex. 2026 at 33:17-20). And, I agree, that alone, confirms that a POSITA would understand that the provision application discloses "one or more training sequences."

43. Additionally and separately, Dr. Alpert explains that the Provisional Application discloses "MB training" in the context of "then current LRDIMMs under development / standardization, DDR3 LRDIMM," which a POSITA would understand refers to "training of interfaces to/from and/or operations of a Memory Buffer." (Ex. 1003, ¶46). The Petition includes nearly identical admissions. (*See*

Pet. at 6.) In that same context, the Provisional Application also discloses initialization sequences when describing that newly developed LR-DIMMs memory modules require "the MCH to hand over ***one or more parts of the initialization operation sequences*** to the memory subsystem controller" as an issue to be addressed by the invention. (Ex. 1008 at 22 (emphasis added)).

44. Here, in my opinion, the Provisional Application reasonably conveys operation sequences (e.g., sequences of operations) that would occur during the initialization of a memory subsystem (e.g., "initialization operation sequences"). MB training is exactly that—a sequence of training operations that could occur during the overall initialization period. It is explicitly disclosed by the Provisional Application. Petitioners' expert went a step further and stated that, in addition to MB training, a POSITA would understand that the provisional application discloses "multiple different types of training." (Ex. 2026 at 33:17-20).

45. Even in the context of just MB training, one or more training sequences are disclosed. This is because the Provisional Application explains that memory modules performing MB training has its notifying signal pin at a low impedance state during MB training and can drive its notifying signal pin to a high impedence state to indicate that training is done. (Ex. 1008 at 22 and Fig. 3 (stating that the error-out pin is "low during MB training")).

46. The Provisional Application explicitly states that the low impedance state can be asserted for different sections of the overall initialization step. (Ex. 1008 at 23) ("Figure 3 shows the operation of the notifying signal in accordance with an example embodiment. The output of ***the notifying signal is low*** impedance while the memory subsystem controller executing ***each section of the initialization step***, thus the notifying signal is pulled low by the memory subsystem controller. ***As the memory controller completes each step, it drives the notifying signal pin to the high impedance state***.") (emphasis added). Collectively, multiple training operations are performed, and multiple notifying signals in relation to training operations are disclosed. This clearly discloses "one or more" training sequences. Therefore, the Provisional Application sufficiently discloses, and the patent owner properly claims, one or more training sequences.

### B. General Overview of the '218 Patent

47. The '218 patent has a priority date of June 12, 2009, and relates generally to the operation of memory modules. (Ex. 1001). Specifically, the '218 patent discloses a memory module that can function in two different modes communicating with a host system. (Ex. 1001, Abstract).

48. As described in the '218 patent, memory modules operate in two distinct modes of operation. (Ex. 1001, 1:42-52, 1:63-2:8, 2:9-14, 4:24-28, 5:61-64, 7:58-65, 9:20-24, 11:47-51, 12:13-17, 12:44-48). The first mode of operation

mode in which the memory module executes a training sequence, during which the memory module may transmit to the memory controller a notification signal associated with the training sequence, but during which the memory module is not accessed by the host for normal memory read or write operations. (Ex. 1001, 1:45-49, 2:17-24, 4:24-31, 5:61-6:10, 6:15-30, 7:3-18, 9:20-27, 11:46-54, 11:55-63). The second mode of operation is a normal operational mode, in which the memory module performs standard read-write, pre-charge, refresh, and similar other standard operations, during which the memory devices are generally accessible by the host system. (Ex. 1001, 1:49-58, 2:2-6, 6:41-48, 12:4-8).

49. The memory module includes a notification circuit which outputs a notification signal associated with the training sequences to the host system. (Ex. 1001, 1:45-49, 1:66-2:2, 2:20-24, 4:31-37, 7:2-14).

## VIII. OVERVIEW OF THE REFERENCES

### A. Hazelzet

50. U.S. Patent App. Pub. No. 2008/0098277 to Hazelzet ("Hazelzet") is U.S. Patent Publication that was filed on October 23, 2006. Hazelzet discloses a memory module including error correction code (ECC) logic "to identify and correct single bit errors on the command or address bus." (Ex. 1014 at [0008]). The invention disclosed in Hazelzet further includes an error reporting mode during which the system can interrogate the module regarding its error status. (Ex.

1014 at [0009]). The invention implements these features in a register "having error correction code (ECC), parity checking, a multi-byte fault reporting register, read via an independent bus, and real time error lines for both correctable errors and uncorrectable error conditions." (Ex. 1014 at [0016]). Thus, Hazelzet's invention discloses a hybrid device utilizing error detection, error correction, and parity. It does not discuss or mention training.

**B. Buchmann**

51. U.S. Patent No. 8,139,430 to Buchmann ("Buchmann") discloses a power-on initialization test for a cascade interconnect system. Buchmann discloses a memory buffer that includes a bus interface to links in a high-speed channel for communicating with a memory controller via a direct connection or via a cascade interconnection and another memory buffer. (Ex. 1016 at 1:39-43). The interface is operable in a static bit communication (SBC) mode and a high-speed mode. (Ex. 1016 at 1:43-44). The memory buffer includes logic for executing a power-on and initialization training sequence initiated by the memory controller. (Ex. 1016 at 1:44-48). The sequence includes initializing the links to the high-speed channel. (Ex. 1016 at 1:48-50).

**C. JEDEC**

52. The JEDEC reference which Petitioners rely on (Ex. 1015) is not prior art to the '218 Patent because it post-dates the priority date of the '218 Patent. *See*,

Sections VII.A.1 - 3, *supra*. The '218 Patent claims priority to Provisional Application No. 61/186,799 (Ex. 1008 at 12) (the "Provisional Application") which has a filing date of June 12, 2009. (Ex. 1001, Cover). Nonetheless, JEDEC discloses Write Leveling and Read Enable Training. (Ex. 1015 at 4). JEDEC states that the MB performs 'Write Leveling' to the DRAMs to ensure successful writes, and 'Read Enable Training' to ensure it can capture read data from the DRAMs correctly, as part of the DRAM interface training. (Ex. 1015 at 8).

## IX. ANALYSIS OF CITED REFERENCES

### A. Grounds 1-3 Fail for Numerous Reasons

53. I understand Petitioners rely on two combinations to challenge all independent claims in the '218 patent: (1) Hazelzet with JEDEC ("Ground 1") and (2) Hazelzet with Buchmann ("Ground 2").[1] I understand the Board instituted *inter partes* review on the following grounds:

| Ground | References | Basis | Challenged Claims |
|---|---|---|---|
| 1 | *Hazelzet and JEDEC* | 35 U.S. C. § 103 | 1 – 24 |
| 2 | *Hazelzet and Buchmann* | 35 U.S. C. § 103 | 1 – 24 |
| 3 | *Hazelzet, JEDEC or Buchmann, and Kim* | 35 U.S. C. § 103 | 3 – 7, 12 – 14, 20, 22, and 23 |

[1] Petitioners' Ground 3 ("Claims 3-7, 12-14, 20, 22, and 23 are obvious over the combinations analyzed above, and Kim") (Pet. at 66-71) only challenges dependent claims of the '595 patent. For the same reasons that Petitioners' Grounds 1 and 2 fail, Petitioners' Ground 3 also fail.

54. In Ground 1, Petitioners allege that Hazelzet could be combined with JEDEC. (Pet. at 33-36). More specifically, Petitioners allege that the combination of Hazelzet and JEDEC "include a '*first mode*' in which training is carried out." (Pet. at 47). Petitioners rely on JEDEC's Write Leveling and Read Enable Training function to satisfy the "training sequences" limitation of Claim 1. (Pet. at 48). Petitioners allege that JEDEC's ERROUT# signal "represent[s] '*information related to the one or more training sequences*" and could be transmitted via an open drain output. (Pet. at 53-54).

55. In Ground 2, Petitioners assert that Hazelzet could be combined with Buchmann. (Pet. at 33-36). Specifically, Petitioners allege that the combination of Hazelzet and Buchman "include a '*second mode*' in which training is carried out." (Pet. at 47). Petitioners rely on Buchmann's TS0 and TS3 function to satisfy the "training sequences" limitation of Claim 1. (Pet. at 48). Petitioners allege that Buchmann's TS0_done, TS3_ack, or TS3_done signals "represent '*information related to the one or more training sequences*" and could be transmitted via an open drain output. (Pet. at 50-52).

56. All Grounds need to demonstrate that a POSITA would find it obvious (1) to add the kind of alleged training in JEDEC or Buchmann to Hazelzet (2) in an entirely new mode that is separate from Hazelzet's normal mode of operation and (3) utilize a single output to communicate parity errors and

information related to training. As explained below, Ground 1 fails because JEDEC is not prior art. Further, all Grounds fail because there is (1) no motivation to add the type of training in JEDEC or Buchmann to Hazelzet, (2) no motivation to combine Hazelzet with Buchmann or JEDEC in a way that Hazelzet is reconstructed to have a training mode separate from its ECC mode of operation, and (3) no motivation to combine Hazelzet with Buchmann or JEDEC such that Hazelzet is reconstructed to output signals related to training sequences over its UE line while in a training mode, and, separately, output parity errors via its open drain line during a normal mode of operation.

#### 1. Ground 1 Fails Because Petitioners Have Failed to Demonstrate that JEDEC is Prior Art

57. Ground 1 fails because JEDEC is not prior art. *See* Section XXX, *supra*. The provisional application provides written description support for every portion of the ’218 patent claims. *Id.*

#### 2. Grounds 1-3 Fail Because There is No Motivation to Add Buchmann’s or JEDEC’s Alleged Training to Hazelzet

##### *a. Problem and Solution Taught in Hazelzet*

58. The Petition identifies an alleged problem with Hazelzet related to errors in data caused by unreliable or noisy communications between a host system and a memory module. (Pet. at 26). This is not an accurate characterization of Hazelzet after reading its entire disclosure. In reality, a POSITA would understand

that Hazelzet focused on providing a cost-sensitive solution for optimizing performance and reliability. (Ex. 1014 at [0001]-[0006]). Unlike Petitioners' and Dr. Alpert's characterization, Hazelzet did not focus myopically on a system's reliability to the detriment of its performance or cost considerations. Instead, Hazelzet sought a solution that would strike a balance, for low end and midrange systems ("reduced function" systems having an "adequate level of asset-protection"), between performance, reliability, and cost. *Id*. Hazelzet identified this, and a POSITA would understand, as being a problem overlooked by the industry. *Id*.

59. The Hazelzet reference contemplated numerous, different solutions to this problem including: "memory mirroring, symbol slicing and extensive forms of fault rejection and redundancy" as well as "error detection and/or correction methods such as CRC (Cyclic Redundancy Code), EDC (Error Detection and Correction), parity or other encoding/decoding methods suited for this purpose" and" "further reliability enhancements [that] may include operation re-try (to overcome intermittent faults such as those associated with the transfer of information), the use of one or more alternate or replacement communication paths to replace failing paths and/or lines, complement-re- complement techniques" and "the use of bus termination, on busses as simple as point-to-point links or as complex as multi-drop structures," which "is becoming more common consistent

with increased performance demands." (Ex. 1014 at [0005], [0127], [0128]). Ultimately, based on performance, cost, and reliability considerations, Hazelzet chose to implement a hybrid solution focused on error code correction ("ECC") functionality that allows a memory module system to perform normal operations in conjunction with parity. (Ex. 1014 at [0016]). Hazelzet relied on parity to enhance a system's performance and ECC to enhance its reliability. (Ex. 200X (Alpert Deposition) at 65:13-19). Hazelzet makes no mention of training—even in its contemplated alternative solutions to the problem it identified (i.e., the appropriate balance of performance and reliability for low end memory systems). (Ex. 1014 at [0005], [0127], [0128]). Notwithstanding, Petitioners and Dr. Alpert allege that a POSITA would be motivated to add training—specifically, the alleged training disclosed in Buchmann and JEDEC—to Hazelzet. (Pet. at 33-39), but as a POSITA I disagree.

60. A POSITA would not be motivated to add Buchmann's or JEDEC's alleged training to Hazelzet. As a POSITA would understand, Buchmann's and JEDEC's alleged training, in contrast to Hazelzet's chosen solution of ECC, are fundamentally different solutions to distinct problems in memory modules. As I explain in further detail below, ECC uses an algorithm to correct errors in received data packets after the data has been transmitted. Buchmann's alleged training seeks to synchronize the timing of memory module communication to ensure error-free

transmission of data packets via a high-speed link before the data is sent, while JEDEC's alleged training is meant to solve the timing issues related to the memory buffers in LR-DIMM, which are not present in Hazelzet. Put simply, ECC corrects data errors once they have occurred, and, in contrast, Buchmann's or JEDEC's alleged training is used to prevent timing errors from occurring before they do.

***b. General Overview of ECC***

61. A system implementing ECC leverages redundancies encoded in data packets to detect errors in transmitted data, and to apply a correcting algorithm to the corrupted data. Redundancy is used primarily for correcting "hard" errors in memory circuits to improve production yield. (Ex. 2030 at 764). With error correction it is possible to detect and correct errors occurring either in manufacturing or in the field to "improve the reliability of the memory device in the system" as well as the yield. (Ex. 2030 at 765). Detecting and correcting errors can be used to give improvement in long term in-system yield. (Ex. 2030 at 765).

62. Generally, error correction involves two simple steps: first, an error must be detected, and, second, the error must be corrected. (Ex. 2030 at 765). The simplest method of error correction is a simple duplication of every bit in the array. (Ex. 2030 at 765). The drawback to this is that the chip size is increased. Different techniques can be deployed which take less area on the chip, though. (Ex. 2030 at 765). Hamming codes are frequently used for this purpose. (Ex. 2030 at 765).

With Hamming codes, error correction can be performed on many different bit field sizes with the assistance of additional parity bits in the array. (Ex. 2030 at 765). There is a trade-off in that small bit fields allow fast error detection but require a large number of extra parity bits in the memory matrix. (Ex. 2030 at 766). Large bit fields permit use of a smaller amount of extra matrix for the parity cells but error detection is slower. (Ex. 2030 at 766).

63. With single error correction, a memory word with one bad bit can be corrected to recover the original information, whereas two bad bits can be detected, but not corrected. (Ex. 2030 at 766). Error correction is useful in system not only to correct soft errors due to noise or alpha particle hits, but also for hard error correction. (Ex. 2030 at 766). A soft error can be corrected by reprogramming the bit. (Ex. 2030 at 766). A hard error is a "stuck at" failure. Since only one error in a word can be corrected, a system failure with error correction present occurs only if two errors occur in the same word. (Ex. 2030 at 766). This occurrence can be lessened by clearing the soft errors more frequently and by regularly replacing parts with hard errors. (Ex. 2030 at 766). For these reasons, ECC is an effective way to reduce and eliminate soft and hard errors in memory systems in order to improve the reliability of data being communicated.

### *c. General Overview of Training*

64. Timing uncertainty is a challenge—separate from the existence of soft and hard errors in memory systems which are resolved via ECC—related to data capture and processing in memory systems. (Ex. 2029 at 195). This would exist in Buchmann's high speed link or JEDEC's memory buffers. It is related to data capture and processing, which is a different problem than Hazelzet attempted to resolve. In operation, a clock path that runs between the clock pads and capture latches may include a clock receiver, timing adjust circuits, and a clock distribution network (or clock tree). (Ex. 2029 at 195). Data, command, and address paths, on the other hand, may be much shorter and only include input buffers. (Ex. 2029 at 195). With different electrical lengths, the input paths are no longer source synchronous internally. (Ex. 2029 at 195). Furthermore, process, voltage and temperature (PVT) variations introduce excessive jitter, and even post-production trimming may not be sufficient as the timing margin shrinks. (Ex. 2029 at 195). Aligning the clock with data, command and address helps to ensure synchronous communication. One way to retain the clock and data relationship is by matching the routing all the way from the pads to the capture points. (Ex. 2029 at 195). On-chip, closed-loop synchronization or input path "de-skewing" is another approach. (Ex. 2029 at 195). For instance, data training, either in relation to a host memory

controller or conducted inside the DRAM itself, can improve the capture timing or ensure reliable data capture over PVT variations. (Ex. 2029 at 195).

65. Based on various design choices that a POSITA would consider, synchronization circuitry can be implemented using digital or analog, open or closed loop methodologies or any combination thereof. (Ex. 2029 at 252). The two most common synchronization circuits used are the delay-locked loop (DLL) and the phase-locked loop (PLL). (Ex. 2029 at 252). The DLL is widely used in memory interfaces for its simplicity and good jitter performance. (Ex. 2029 at 252). An alternative approach is the PLL, which is usually found in communication systems and microprocessors for clock data recovery and frequency synthesis. (Ex. 2029 at 252).

***d. General Differences Between ECC and Training***

66. Training is a solution to a different problem than that addressed by ECC. Training seeks to pre-emptively ensure reliable performance of a memory module. From the perspective of the memory controller, each component on a memory module is a slightly different distance away, and each component takes a slightly different amount of time to perform an operation. Conventional memory modules include predetermined constants for timing that balance these concerns by erring on the side of allowing more time, and thus result in inefficiency.

67. ECC cannot, and does not, seek to optimize the timing of signals between memory controller and components on the memory module. ECC is used to correct errors in data packets by including redundant information in each data packet. Upon receipt of the data packets, an algorithm compares all the data to determine whether there are any errors, and if so, to use the redundant information to correct the errors.

68. At a high level, the shipment of a package from a shipping company to a recipient is a useful analogy to highlight the differences between ECC and training. Training is used to determine when a package should be sent and received to ensure that the intended recipient is available to receive it. If it is sent too early or late, the intended recipient will not be home to receive it. Training makes sure that the shipping company sends the package at a time when the recipient is home. ECC, on the other hand, seeks to ensure that the right content is sent in the package, and, if not, resending the correct content. This is done without regard for when the package is sent. ECC ensures that, if a basketball is intended to be shipped, a basketball is ultimately shipped. If, instead, a football is shipped, ECC will correct the mistake and resend a package that includes a basketball.

### *e. There is No Motivation to Add Buchmann's or JEDEC's Alleged Training to Hazelzet for Multiple Reasons*

69. All of Petitioners' Grounds require Buchmann's or JEDEC's alleged training to be added to Hazelzet. (Pet. at 4). Petitioners allege that a POSITA "would have been motivated to add training to Hazelzet because it was known that training improved memory module reliability." (Pet. at 38). That is the only reason Petitioners give for why a POSITA would specifically—and to the exclusion of other choices—add Buchmann's or JEDEC's alleged training to Hazelzet. This single, conclusory statement fails to establish, with any particularity, why a POSITA would have specifically chosen Buchmann's or JEDEC's alleged training—as opposed to any other technique to improve memory module reliability—to add to Hazelzet, without hindsight teachings from the '218 patent.

### *f. Petitioners' Motivation to Combine is Conclusory and Logically Inconsistent*

70. Petitioners and Dr. Alpert do not explain why a POSITA would be motivated to add training to Hazelzet beyond the generic, conclusory statement that all the references relate to "reliability." (Pet. at 37-38). I understand this fails to satisfy a motivation to combine the references. Petitioners do not even attempt to analyze why a POSITA would be motivated to add training—to the exclusion of any other technique—to Hazelzet in order to "improve overall system reliability."

71. A POSITA would understand that Hazelzet, itself, presents a different memory module from that of Buchmann or JEDEC, and aims to solve a different problem. Specifically, Hazelzet uses ECC to improve system reliability. This demonstrates that a POSITA would not be motivated to add training, because there is no teaching or suggestion of any other problems to be solved using training besides the alleged problem of "system reliability" which has already been resolved by ECC. In fact, different solutions to the same problem, like Hazelzet's choice to use ECC instead of training, is further evidence of non-obviousness. This does not demonstrate obviousness or a motivation to add training to Hazelzet, let alone the specific type of training alleged to be disclosed in Buchmann or JEDEC. In fact, Hazelzet's choice to use ECC to solve the only problem it presents, is further indicia of non-obviousness.

72. There are numerous options available to improve the "reliability" of a memory system—many of which are identified in Hazelzet (Ex. 1014 at [0005], [0127] and [0128]) and do not include training—Petitioners state that training, alone, would be the obvious choice. As a POSITA I disagree and such a conclusory, unsupported statement does not demonstrate why a POSITA would have combined the elements from specific references in the way that the claimed invention does.

73. In my opinion, the conclusory testimony of Petitioners' expert does not provide an articulated motivation to add Buchmann's or JEDEC's alleged training to Hazelzet either. (Ex. 1003 at ¶¶ 161-163).

#### *g. Petitioners' Motivation to Combine is the Result of Impermissible Hindsight*

74. I believe Petitioners' unsupported contention to add training to Hazelzet is the result of improper hindsight.

75. Petitioners' expert, Dr. Alpert, has already alleged that Hazelzet's ECC mode is training. (Ex. 2031 at 92:23-93:5). If Hazelzet already has training, why would a POSITA be motivated to add training? The rhetorical answer is: a POSITA would not.

76. However, now Dr. Alpert states that Hazelzet does ***not*** have training. (Ex. 2026 at 52:17-22; 53:13-18). In similar contradictory fashion, Petitioners and their expert previously said that training would be obvious to add to Hazelzet's ECC (normal) mode, but now say it would be obvious to add a whole new training mode of operation in Hazelzet that is separate from its ECC (normal) mode. *See* Section IX.A.3, *infra*. Put another way, depending on the claims that Petitioners and their expert are challenging, they interpret and map references differently. This is backwards. What Hazelzet discloses has to be the same no matter what. Likewise, how a POSITA would be motivated to combine it with other references

does not change depending on the claims being challenged. Hazelzet either discloses training or does not. Both cannot be true. And it would either be obvious to add training to Hazelzet's ECC mode or not. Again, both cannot be true.

77. I believe the only explanation for Petitioners' dramatic shift in positions is that they are using the claims as a guide to reconstruct a system based on cherry-picked passages of disparate references. From what I understand, this is textbook impermissible hindsight. Petitioners' arguments are built on a foundation of impermissible hindsight. For this reason alone, all Grounds fail.

#### *h. Petitioners' Motivation to Combine is Based on What a POSITA Could Have Done; Not what a POSITA Would Have Done*

78. As previously stated, Petitioners allege that "a Skilled Artisan would have been motivated to add training to Hazelzet because it was known that training improved memory module reliability." (Pet. at 37-38). In my opinion this statement provides no reason for why a POSITA would be motivated to add Buchmann's or JEDEC's alleged training to Hazelzet. It simply states that training can improve memory module reliability. This is tantamount to saying that a POSITA would add Buchmann's or JEDEC's alleged training to Hazelzet because they could add training to Hazelzet. However, a POSITA would understand that Hazelzet identifies numerous, different improvements that a POSITA could implement to improve the "reliability" of its specific memory module including:

"memory mirroring, symbol slicing and extensive forms of fault rejection and redundancy" as well as "error detection and/or correction methods such as CRC (Cyclic Redundancy Code), EDC (Error Detection and Correction), parity or other encoding/decoding methods suited for this purpose" and" "further reliability enhancements [that] may include operation re-try (to overcome intermittent faults such as those associated with the transfer of information), the use of one or more alternate or replacement communication paths to replace failing paths and/or lines, complement-re- complement techniques" and "the use of bus termination, on busses as simple as point-to-point links or as complex as multi-drop structures," which "is becoming more common consistent with increased performance demands." (Ex. 1014 at [0005], [0127], [0128]). But from what I understand, what a POSITA could have done does not satisfy the legal requirement of demonstrating, with evidence, what a POSITA would have done.

#### *i. Hazelzet, Buchmann and JEDEC Disclose Teachings that Diverge from One Another*

79. Petitioners ignore the fact that the teachings of Hazelzet diverge from Buchmann's and JEDEC's alleged training. As explained earlier, ECC and training are different solutions to a different problem. *See* Sections IX.A.2.a - d, *supra*. Moreover, Hazelzet identifies numerous, different improvements that a POSITA could implement to improve "reliability" of its system—none of which include

training. (Ex. 1014 at [0005], [0127], [0128]). I understand that the Federal Circuit confirms that a reference may be said to teach away when a person of ordinary skill, upon reading the reference, would be discouraged from following the path set out in the reference, or would be led in a direction divergent from the path that was taken by the applicant. Unlike the '218 patent, which chose training as a method to improve system reliability, Hazelzet chose ECC after contemplating numerous other techniques—none of which involved training. Accordingly, Hazelzet's teaching would lead a POSITA on a path that diverges from the one taken by the '218 patent.

### 3. There is No Motivation to Create a Separate Training Mode in Hazelzet

80. All of Petitioners' Grounds require Buchmann's or JEDEC's alleged training to be added to Hazelzet as a new mode that is distinct from Hazelzet's normal mode of operation. (Pet. at 4, 38-39). Specifically, Petitioners argue, in a section titled "Motivation to Add Training as a Mode Separate from Normal Operations," that a POSITA "would have been motivated to combine the[] references by adding training in a mode separate from normal operation" in Hazelzet. (Pet. at 38-39). However, Petitioners previously argued, and the Board agreed, that a POSITA would add training to Hazelzet's ECC mode of operation,

which is a normal mode of operation. This is the exact opposite of what Petitioners currently argue.

81. Specifically, Petitioners previously took the position that a POSITA would have found it obvious to add Buchmann's training to Hazelzet.

> One skilled in the art would have found it obvious to implement the notification techniques of Hazelzet in the "training" schemes of Buchmann that make use of the "SBC mode" (i.e., error correcting mode). (Ex. 1017, 8:24-9:17; Ex1003 at ¶¶165, 171).

(Ex. 2015 at 62, IPR2018-00303 Petition). Petitioners' expert explained that a POSITA would find it obvious to add training into Hazelzet's ECC mode of operation (i.e., a normal mode of operation):

> Because the "SBC mode" is a mode of operation where "error correcting code" is provided, Ex. 1017 (Buchmann) at 14:25-28, one skilled in the art would have found it obvious to combine the "training" schemes (e.g., "TS3: upstream lane training and repair") described in Buchmann with the notification scheme of Hazelzet in the "ECC mode" (i.e., "second mode," as claimed).

(Ex. 2017 at ¶171, Dr. Alpert's IPR2018-00303 Declaration). Petitioners now appear to say that Hazelzet's ECC mode is, in fact, a normal mode of operation. (Pet. at 70 (stating that Hazelzet has "parity and ECC normal operating modes"))

82. I understand the Board agreed with Petitioners' prior position that the ECC mode of Hazelzet was a "second mode." (Ex. 2016 at 20 (finding Hazelzet's ECC mode to be a "second mode") and 12 (finding that Buchmann's training mode would be implemented in Hazelzet's ECC mode), IPR2018-00303 FWD). The

Board further credited the opinion of Petitioners' expert as being "consistent with the prior art disclosures." (*Id.* at 13 (citing Ex. 1003 at ¶¶121-150, 158-186)). Accordingly, Petitioners and their expert successfully argued that a POSITA would find it obvious to add training to Hazelzet's ***normal*** (i.e., ECC mode) mode of operation.

83. Now, Petitioners and their expert attempt to argue that it would be obvious to add training as a separate mode of operation, outside Hazelzet's normal mode of operation. (Pet. at 38-39). But, if a POSITA would have been motivated to add training into Hazelzet's normal mode of operation (i.e., ECC mode), they could not now be motivated to do the exact opposite by adding training to Hazelzet as a separate mode from the normal mode of operation. A POSITA would understand that the two options are incongruent to one another. Choosing one makes it non-obvious to choose the other. And, it would not be obvious to add Buchmann's or JEDEC's alleged training to Hazelzet in an entirely new mode.

84. Setting aside the logical inconsistency with Petitioners' present argument that is fundamentally inconsistent with their prior view of the world, which alone is fatal to the Grounds in the petition, Petitioners gloss over the discordant reconstruction of Hazelzet that would be required to add an entirely new mode of operation to that system. Indeed, Petitioners provide no evidence or explanation as to why the addition of an entirely new mode of operation would be

obvious and straightforward. (Pet. at 38-39). The opposite is true. Adding an entirely new mode of operation would require substantial reconstruction and redesign of Hazlezet, and doing so is not obvious, nor would there be a reasonable likelihood of success in doing so.

85. For example, below is a list of all the things a POSITA would need to contemplate when adding a new mode of operation to a memory module:

- How the "new" mode would interact with all the other existing modes so that there would be no unwanted interactions.
- How commands to enter this "new" mode would be received and decoded and what they would control.
- What exact state the memory module would be in after the command to enter was decoded.
- What state each of the memory devices would be in while in the "new" mode, including the control of all input/output pins such that no signal contentions would occur.
- All actions that the memory module would be permitted to perform while in the "new" mode, ensuring that those actions would be permissible to the components on the module (*e.g.*, DRAMs, Memory Buffer, Serial Detect, etc.)
- All interactions with the Host Controller while in the "new" mode, including preventing unwanted interactions with the other Memory Modules in the system.
- How to achieve proper signaling (Timing and Signal Levels) between the Memory Module and the Host Controller.

- How to know when to exit from the "new" mode, including how to exit such that the Memory Module and Host Controller are appropriately set up for any of their next potential operations.

- What power might be consumed during the "new" mode and implementation of potential power mitigation strategies.

86. Petitioners and Dr. Alpert fail to address any of these issues that any POSITA would understand would be necessary to consider when adding a new mode of operation to a memory module. And these are just considerations one would need to contemplate when adding a new mode to a memory module. For Hazelzet, which discloses a memory device, a similar list of considerations would need to be considered:

- How the "new" mode would interact with all the other existing modes so that there would be no unwanted interactions.

- How commands to enter this "new" mode would be received and decoded and what they would control.

- What exact state the memory device would be in after the command to enter was decoded.

- What state each of the memory devices would be in while in the "new" mode, including the control of all input/output pins such that no signal contentions would occur.

- All actions that the memory device would be permitted to perform while in the "new" mode, ensuring that those actions would be permissible to the components on the module (*e.g.*, DRAMs, Memory Buffer, Serial Detect, etc.)

- What signal actions are permissible between the Memory Device and the Memory Buffer while in the "new" mode.

- All interactions with the Memory Buffer while in the "new" mode, including preventing unwanted interactions with the other Memory Devices on the Memory Module.

- How to achieve proper signaling (Timing and Signal Levels) between the Memory Device and the Memory Buffer.

- How to know when to exit from the "new" mode, including how to exit such that the Memory Device and the Memory Buffer are appropriately set up for any of their next potential operations.

- What power might be consumed during the "new" mode and implementation of potential power mitigation strategies.

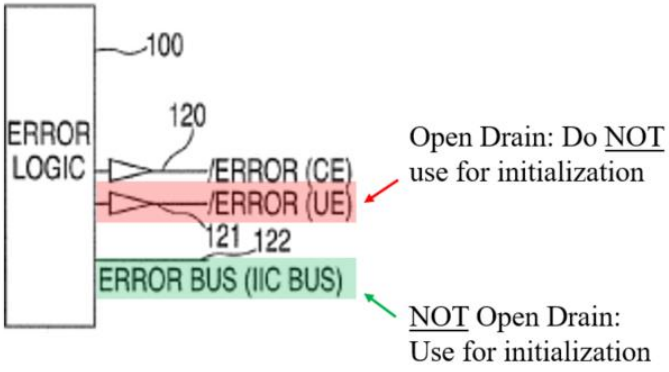
87. Dr. Alpert appears to concede this point, noting that adding a new mode of operation to a memory module like Hazelzet would include fundamental and complex redesigns to the entire system, which would have to be tested "extensively." (Ex. 2026 at 70:3-76:10). Despite acknowledging these issues, Petitioners and Dr. Alpert fail to address any of them when discussing how they would add training to Hazelzet, and instead suggest the combinations would be "straight-forward." I disagree. For the reasons above, a POSITA would recognize that Petitioners' proposed combinations would not have a reasonable likelihood of success.

#### 4. There is No Motivation to Use Hazelzet's Open Drain Signaling for Training Notifications

88. All of Petitioners' Grounds require Buchmann's or JEDEC's alleged training to (1) be added to Hazelzet (2) as a new mode that is distinct from Hazelzet's normal mode of operation *and* (3) to utilize Hazelzet's UE line. (Pet. at 4, 39-41). Petitioners allege "it would have been further obvious to communicate training status in the new mode using the same open drain output used in other modes." (Pet. at 39). However, Petitioners provide no articulated reason why a POSITA would have been motivated to do so. (Pet. at 39-41). Instead, Petitioners make a number of generic statements related to a POSITA's ability to utilize an open drain output for multiple purposes. *Id*. This amounts to a contention that a POSITA ***could*** have, not ***would*** have, used an open drain for multiple purposes. I understand that it is legally insufficient for Petitioner to simply allege that a POSITA could use an open drain for multiple reasons. A POSITA would have understood that they could just as easily have reused a different pin than Hazelzet's open drain. Why would a POSITA have been motivated to use the open drain signal—as opposed to other pins—in Hazelzet? Petitioners did not even attempt to answer the question. For good reason, Petitioners cannot.

89. Hazelzet discourages use of its UE (open drain) pin during initialization. Instead, Hazelzet discloses initialization that utilizes a bus that is

distinct from the UE. Specifically, Hazelzet suggests that a POSITA would use "a distinct bus, such as a presence detect bus [], an IIC bus [] and/or the SMBUS, which has been widely utilized and documented in computer systems using such memory modules." (Ex. 1014 at [0124]). Accordingly, Hazelzet prefers use of its IIC bus instead of its UE pin.




(Ex. 1014 at Figure 4B) (annotated).

90. A POSITA would understand that Hazelzet prefers "the use of a separate bus" because it "offers the advantage of providing an independent means for both initialization and uses other than initialization…including changes to the subsystem operational characteristics on-the-fly and for the reporting of and response to operational subsystem information such as utilization, temperature data, failure information or other purposes." (Ex. 1014 at [0125]). In other words, Hazelzet prefers to reuse its IIC bus (not UE) for different functions—including initialization—while in its normal mode of operation. Using the IIC bus allows Hazelzet to perform initialization "on-the-fly." (Ex. 1014 at [0125]).

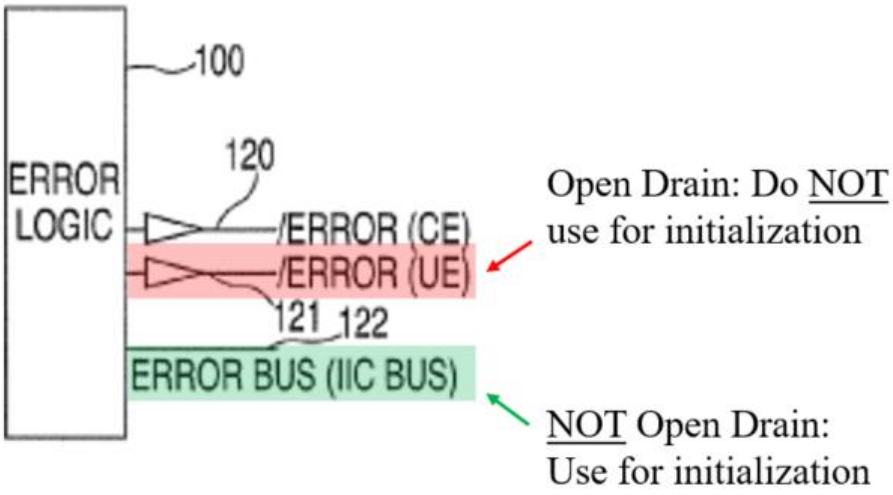
91. Not only do Petitioners fail to muster an argument as to why a POSITA would be motivated to use Hazelzet's UE line for training outputs, such an argument would be contrary to the teachings of Hazelzet because Hazelzet discloses utilizing the IIC bus during initialization for numerous perceived benefits and advantages. (Ex. 1014 at [0124]-[0125]). Accordingly, a POSITA would not be motivated to use Hazelzet's UE to communicate training status as Petitioners suggest in conclusory fashion. A POSITA would be motivated to reuse Hazelzet's IIC bus in order to improve performance, efficiency, and reliability.

### 5. Claims 1-24 are not obvious over Hazelzet in view of JEDEC for Additional Reasons

92. As a preliminary matter, as I have already discussed, I do not believe JEDEC is prior art to the '218 patent. *See* Section VII.A.1 - 3, *supra*. Further, for the reasons detailed above, a POSITA would understand that there is no motivation to (1) add JEDEC's training to Hazelzet, (2) add JEDEC's training as a separate mode to Hazelzet, or (3) use Hazelzet's open drain signaling for JEDEC's alleged training notifications. *See* Sections IX.A.1 - 4, *supra*. In addition to these reasons, the '218 claims are not obvious over Hazelzet in view of JEDEC for two separate reasons.

93. First, Petitioners allege that a POSITA would use Hazelzet's UE line to output JEDEC's alleged training notifications. (Pet. at 35-36). However, a

POSITA would understand that Hazelzet teaches away from doing this. Specifically, Hazelzet prefers to perform initialization via a separate, distinct bus, like "an IIC bus (such as defined in published JEDEC standards such as the 168 Pin DIMM family in publication 21-C revision 7R8). (Ex. 1014 at [0124]). Even if it were obvious to add JEDEC's training to Hazelzet—and it is not—Hazelzet specifically teaches that a JEDEC-standard IIC bus should be used. Hazelzet also includes an IIC bus that is different than its UE line.




(Ex. 1014 at Figure 4B) (annotated). Because Hazelzet, itself, explicitly discloses the desire to use a JEDEC-standard IIC bus for initialization, a POSITA would not be motivated to implement JEDEC's alleged training via Hazelzet's UE line. Hazelzet has a good reason for utilizing the IIC bus:

> The use of a separate bus, such as described in the embodiment above, also offers the advantage of providing an independent means for both initialization and uses other than initialization, such as described in U.S. Pat. No. 6,381,685 to Dell et al., of common assignment

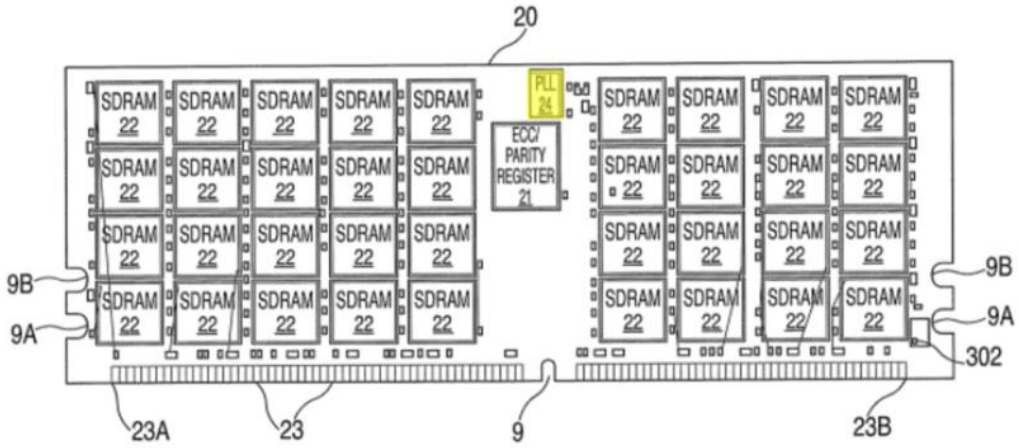
> herewith, including changes to the subsystem operational characteristics on-the-fly and for the reporting of and response to operational subsystem information such as utilization, temperature data, failure information or other purposes.
>
> (Ex. 1014 at [0125]).

There is no reason to use Hazelzet's UE line.

94. Second, Hazelzet's memory module does not have memory buffers, which would cause timing issues and which hides the memory devices from the memory bus, a problem JEDEC's alleged training aims to address. Thus, a POSITA would not be motivated to add JEDEC's training to Hazelzet in the first place, let alone trying to perform JEDEC's training in Hazelzet's ECC/Parity register, which is where Hazelzet's UE line resides. Hazelzet at Figure 4A and 4B. Instead, a POSITA would understand that a PLL or DLL component was the most obvious choice to perform training.

> Based on various design choices that a POSITA would consider, synchronization circuitry can be implemented using digital or analog, open or closed loop methodologies or any combination thereof. The two most common synchronization circuits used are the delay-locked loop (DLL) and the phase-locked loop (PLL). The DLL is widely used in memory interfaces for its simplicity and good jitter performance. An alternative approach is the PLL, which is usually found in communication systems and microprocessors for clock data recovery and frequency synthesis.
>
> (Ex. 200X at 252).

Since Hazelzet includes a DLL, that component would be the logical component to perform training, not the ECC/Parity register.




FRONT SIDE OF DIMM - 72 PLANAR

FIG. 3A

(Ex. 1014 at Figure 3A) (annotated). For at least these reasons, a POSITA would not be motivated to implement JEDEC's training on Hazelzet's UE line.

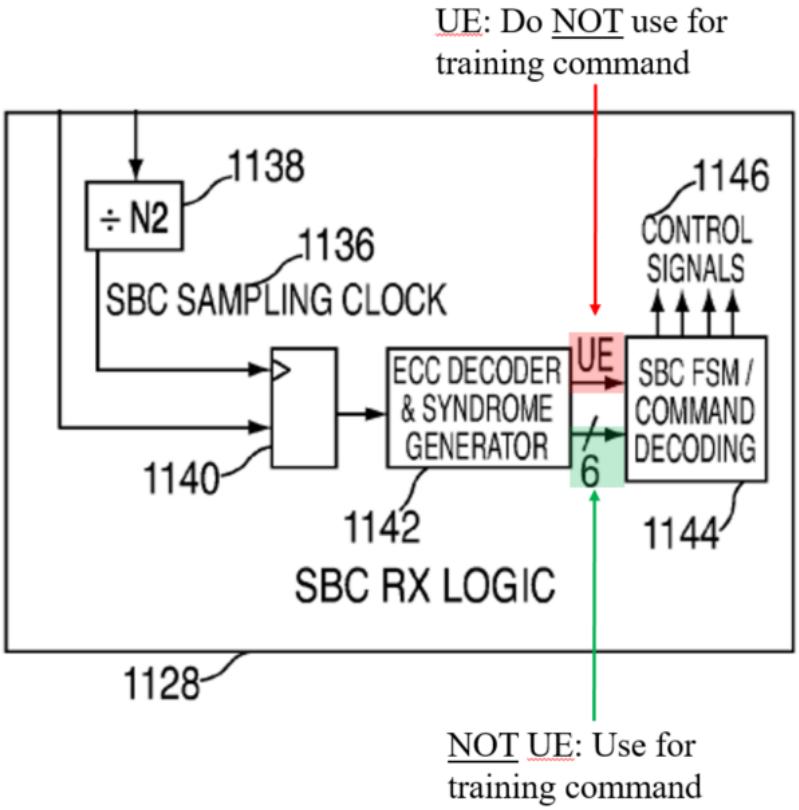
### 6. Claims 1-24 are not obvious over Hazelzet in view of Buchmann for Additional Reasons

95. For the reasons detailed previously, there is no motivation to (1) add Buchmann's training to Hazelzet, (2) add Buchmann's training as a separate mode to Hazelzet, or (3) use Hazelzet's open drain signaling for Buchmann's alleged training notifications. *See* Sections IX.A.1 - 4, *supra*. In addition to these reasons, a POSITA would understand that the '218 claims are not obvious over Hazelzet in view of Buchmann for two separate reasons. More specifically, Petitioners allege

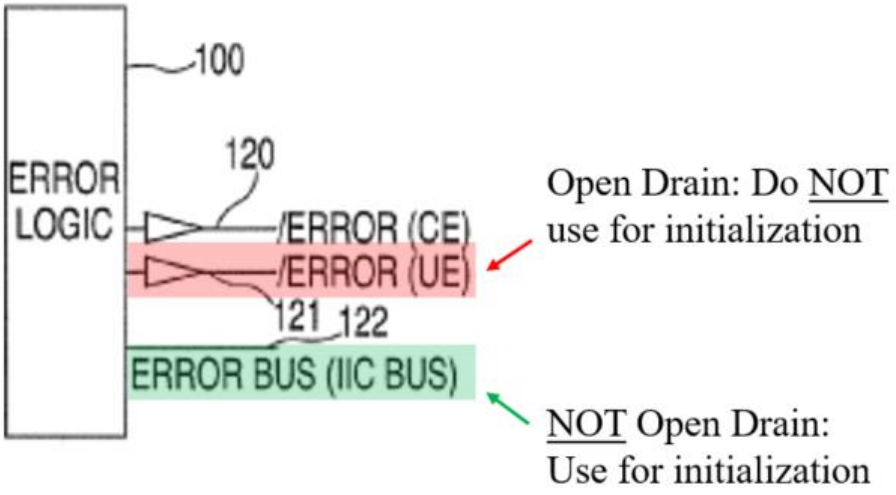
that it would be obvious to output Buchmann's TS commands via Hazelzet's UE line. (Pet. at 35-36). It would not be obvious to a POSITA for two reasons.

96. First, Petitioners rely on Buchmann's TS3 commands as being incorporated into Hazelzet. However, Petitioners' expert previously stated that Buchmann's TS3 commands "wouldn't necessarily be a very appropriate command" for Hazelzet. (Ex. 2031 at 121:6-15). Petitioners make no attempt to explain why TS3 commands would be a good fit now, and make no attempt to explain why Buchmann's TS0 commands—or any other TS command for that matter—are actually appropriate for inclusion in Hazelzet. This contention is conclusory.

97. Second, Petitioners allege that Buchmann's TS commands (specifically, TS0_done, TS3_ack, and TS3_done) would be obvious to output via Hazelzet's UE line in order to satisfy the claimed "associated with the one or more training sequences." (Pet. at 53). However, Buchmann includes the same UE line as Hazelzet and does not send its TS commands over it. Instead, Buchmann sends its TS commands via separate bus (annotated in green below).




(Ex. 1016 at Figure 11) (annotated). Indeed, Buchmann confirms that its TS commands are output via a different pin than its UE, and Petitioners' expert agrees that Buchmann's UE line does not communicate Buchmann's commands. (Ex. 2031 at 106:20-107:11; 108:6-14; 124:17-19). Similarly, Hazelzet teaches the use of an IIC bus—not UE—for initialization.




(Ex. 1014 at Figure 4B) (annotated).

98. Accordingly, both Buchmann and Hazelzet disclose teachings that diverge from the ’218 claims. The modification and combination proposed by the Petition do not make the ’218 claims obvious; they actually teach away from the ’218 claims.

Executed on March 11, 2021

By: Robert J. Murphy

# APPENDIX A

**Robert J. Murphy**
**72 Fairview Plaza**
**Los Gatos, California 95030**
**(408) 396-6098**
**murf@firenza-llc.com**

**Abstract:** More than 47 Years of experience in management,design, hands-on development & debug of: High speed, high complexity, high density and high volume commercial semiconductor products including Full Custom Microprocessors, $E^2$CMOS and BiCMOS PALs, CMOS and NMOS SRAMs, CCDs and RAD Hard SOS CMOS.

**Vice President of Engineering** — **IC Manage, INC.**
**1/21 – PRESENT** — **Campbell, CA.**

Responsible for all software engineering including development, applications engineering, testing and documentation for Integrated Circuit Revision Control & Cloud Computing Software.

**Founder & Owner** — **Firenza, LLC**
**4/98 – PRESENT** — **Los Gatos, CA.**

Founded company to respond to the growing needs of the semiconductor industry to license quality high performance building blocks for Semi-Custom and ASIC designs. Developed business plan, cultivated customers and managed the efforts of Design Professionals to deliver world class building blocks in 0.25u 0.18u, 0.13u, 65nM & 14nM processes. Provided circuit design reviews on 65 nM Major Microprocessor. Designed EFUSE circuit for another 65 nM Microprocessor. Debugged and provided layout based solutions for 65 nM process latch-up issue. Designed 28nM & 14nM SRAM circuits. Developed custom 10Ghz SRAMs IP Blocks for custom processor in 14nM process.

Performed Expert Witness work on the following cases:

NeoMagic Corporation v. Trident Microsystems, Inc.
D. Del., C.A. No. 98-699-RRM, Client: Trident, Year: 1999

Rambus, Inc. v. Infineon Technologies AG,
Infineon Technologies North America Corp.,
And
Infineon Technologies Holding North America, Inc.
Eastern D. Virginia, C.A. No. 3:00cv524, Client: Rambus, Year: 2001

Micron v, Rambus, Inc.
D. Del., C.A. No. 00-792-(RRM), Client: Rambus Year: 2001

Hynix Semiconductor Inc. et al. v. Rambus, Inc.
Northern D. Calif., Case No. CV 00-20905 RMW
Client: Rambus, Year: 2005

Rambus, Inc. v. Hynix Semiconductor Inc. et al.
Northern D. Calif., Case Nos. C-05-00334, C-05-02298,
C-06-00244, C-00-20905 RMW, Client: Rambus Year: 2007

Toshiba v. Hynix
International Trade Commission, Investigation No. 337-TA-592
Client: Toshiba Year: 2007

UniRAM Technology, Inc. v. MONOLITHIC SYSTEM TECHNOLOGY, TAIWAN SEMICONDUCTOR MANUFACTURING COMPANY, LTD, & TSMC NORTH AMERICA
Northern D. Calif., Case No. CV-04-01268-VRW
Client: UniRAM Year: 2008

Perego, et al. v. Drehmel, et al.
U.S.P.T.O., Patent Interference No. 105,467 (Bd. Pat, App.& Int.)
Client: Rambus Year: 2007

Reexamination proceedings involving various U.S. Patents in the Farmwald / Horowitz Family derived from Application No. 07/510,898
Client: Rambus Year: 2011

Reexamination proceedings involving U.S. Patents #'s 7,210,016; 7,177,998, Client: Rambus, Year: 2009

Reexamination proceedings involving U.S. Patents #'s 7,287,119; 7,330,952; 7,330,953; 7,360,050; Client: Rambus, Year: 2010

Reexamination proceedings involving U.S. Patents #'s 7,287,109; 6,591,353; 6,470,405; Client: Rambus, Year: 2009

*In The Matter Of: CERTAIN MLC FLASH MEMORY DEVICES AND PRODUCTS CONTAINING SAME,* International Trade Commission, Investigation No. 337-TA-683, Client: BTG, Year: 2009

e.Digital Corporation v. Toshiba America Information Systems Inc.
Southern D. California, Case No, '13CV2909 BEN BGS, Client: Toshiba, Year: 2013, Matter: Flash Memory File System in a Handheld Record *and Playback Device*

*In The Matter Of: CERTAIN STATIC RANDOM ACCESS MEMORIES AND PRODUCTS CONTAINING SAME,* International Trade Commission, Investigation No. 337-TA-792,Client: GSI Year: 2013

*In The Matter Of: CERTAIN WIRELESS COMMUNICATIONS EQUIPMENT AND ARTICLES THEREIN,* International Trade Commission,
Investigation No. 337-TA-866, Client: Ericcson Year: 2013,
Matter: Wireless Communication Equipment & Power Supplies

Solid State Storage Solutions, Inc. v. STEC, INC., OCZ TECHNOLOGY, INC., CORSAIR MEMORY, TEXAS MEMORY SYSTEMS, INC., PNY TECHNOLOGIES, INC., PATRIOT MEMORY LLC, FUSION-IO, INC., OTHER WORLD COMPUTING, INC., and MUSKIN, INC. Eastern D. Texas, Case No. 2:11-cv-00391-JRG-RSP, Client: Solid State Year: 2012

GSI Technology, Inc. v. UNITED MEMORIES INC. and INTEGRATED SILICON SOLUTION, INC., Northern D. Calif., Case No. 13-cv-1081-PSG Client: GSI Year: 2015, Matter: Static RAM Memory Devices & Features

GSI Technology, Inc. v. CYPRESS SEMICONDUCTOR CORP. Northern D. Calif., Case No. 5:11-cv-03613-EJD Client: GSI, Year: 2015, Matter: Static RAM Memory Devices & Features

CYPRESS SEMICONDUCTOR CORP. v. GSI Technology, Inc. Northern D. Calif., Case Nos. 3:13-cv-02013-JST (JCS), 4:13-cv-03757-JST (JCS), Client: GSI, Year: 2015, Matter: Static RAM Memory Devices & Features

Petition for *Inter Partes* Review involving U.S. Patents nos. 6,292,403 (Case IPR2014-00121) and 6,069,839 (Case IPR2014-00202), Client: GSI, Year: 2015, Matter: Static RAM Memory Devices & Features

Petition for *Inter Partes* Review involving U.S. Patent no. 6,058,045 (Case IPR2014-00113), Client: Toshiba, Year: 2015, Matter: DRAM Memory & Features for Display Operations

Petition for *Inter Partes* Review involving U.S. Patent no. 5,687,132 (Case IPR2014-00317), Client: Toshiba, Year: 2015, Matter: DRAM Memory & Features for Display Operations

*In The Matter Of: CERTAIN INTEGRATED CIRCUITS AND PRODUCTS CONTAINING THE SAME, U.S. ITC Inv. No. 337-TA-920, Client: Freescale, Year: 2014, Matter: C*ircuitry for timing operations within memory circuits and to bond pad structures and layouts used on integrated circuits.

Freescale Semiconductor, Inc. v. MediaTek Inc., et al., Northern D. of California, Case No. 5:14cv02185BLF, Client: Freescale, Year: 2014, Matter: Circuitry for timing operations within memory circuits and to bond pad structures and layouts used on integrated circuits.

Petition for *Inter Partes* Review involving U.S. Patent no. 5,500,819 (Case IPR2014-00418), Client: Toshiba, Year: 2015, Matter: DRAM Memory & Features for Display Operations

Intellectual Ventures I LCC et al. v. Toshiba Corporation et al. D, Del., C.A. No. 13-453-SLR-SRF, Client: Toshiba, Year: 2017, Matter: DRAM Memory & Features for Display Operations

*In The Matter Of: CERTAIN MEMORY MODULES AND COMPONENTS THEREOF, AND PRODUCTS CONTAINING SAME, U.S. ITC Inv. No. 337-TA-1023,* Client: Netlist, Year: 2017, Matter: Features of DRAM Memory Modules

Petition for *Inter Partes* Review involving U.S. Patent no. 8,489,837 (Case IPR2017-00548), Client: Netlist, Year: 2017, Matter: Features of DRAM Memory Modules

*In The Matter Of: CERTAIN MEMORY MODULES AND COMPONENTS THEREOF, U.S. ITC Inv. No. 337-TA-1089,* Client: Netlist, Year: 2018, Matter: Features of DRAM Memory Modules

Petition for *Inter Partes* Review involving U.S. Patent no. 9,535,623 (Case IPR2018-00303), Client: Netlist, Year: 2018, Matter: Features of DRAM Memory Modules

PHENIX LONGHORN, LLC v. WISTRON CORP. et al.
Eastern D. Texas, Case No. 2:17-cv-000711-RWS, Client: Phenix, Year: 2018, Matter: Gamma Reference Generator for Monitors & Televisions

Petition for *Inter Partes* Review involving U.S. Patent no. 7,233,305 (Case IPR2018-01255), Client: Phenix, Year: 2018, Matter: Gamma Reference Generator for Monitors & Televisions

PHENIX LONGHORN, LLC v. TEXAS INSTRUMANTS INC.
Eastern D. Texas, Case No. 2:18-cv-00020-RWS, Client: Phenix, Year: 2018, Matter: Gamma Reference Generator for Monitors & Televisions

Petition for *Inter Partes* Review involving U.S. Patent no. 6,651,134 (Case IPR2020-01492), Client: Qualcomm, Year: 2020, Matter: DRAM Memory Device with Fixed Burst Length

**Director of Engineering** **Silicon Graphics Inc.**
**6/92 – 4/98** **Mountain View, CA.**

*Beast Program*: Hired, managed and directed circuit designers on this 500 MHz design. Responsible for the scheduling and design reviews for all custom circuit design on the chip. Supported CAD tool development with test structures, test cases and debug.

*T5 (R10000) Program*: Assisted in the final completion of this processor. Took my team of people down to the project in it's late stages and managed 10% of the Units (3) on the chip. Was a key member of the schedule review team.

*TFP (R8000) Program:* Managed the design and implementation of the Floating Point Chip for SGI's POWER CHALLENGE systems. Directed the re-design of a large Tag Ram done for SGI by Toshiba. Managed a group of Toshiba's engineers in the US and interacted with their counterparts in Japan to debug and repair the design. The repaired design was fully functional with speeds of 110 MHz.

The redesign was accomplished while holding 16 lots of silicon in the fab. All of the lots were saved and parts delivered to SGI on time.

Major accomplishments included:

* Hired over 20 people.
* Managed a total team of 30 people.
* Developed extensive relationships with our Japanese Partners.
* Hired contractors as needed for specific expertise

* Directed the development and implementation of world class PLL designs onto the whole SGI campus.
* Developed internal circuit design resources via training and assignment selection.

**Director of Engineering** **Weitek Corp.**
**2/89 - 6/92** **Sunnyvale, CA**

Initially hired as a Design Manager with responsibility for putting a single chip into production. One year later, was managing the company's most important product along with others. Developed circuitry which gave the company world-class performance in memory, output drivers, and Electro-Static Discharge (ESD). Promoted to Director (1990). Managed the circuit design, architecture and layout groups. This included budgeting, staffing, and resource allocation for multiple programs, the largest of which was over 400K transistors. Responsible for the technical and administrative management of a staff that included 20 engineers and 5 layout people.

Major accomplishments included:

* Managed the product design and release to production of a 40 MHz SPARC combined IU/FPU product
* Managed the development and release to production of a Floating Point Coprocessor that works with the Intel i486.
* Directed the redesign and release to production of two products, completed by other managers, which were not production worthy.
* Aided Manufacturing in the pre- and post-production release management of our silicon foundries. This included modeling, process issues and production/testing problems.
* Increased the staff by more than 50% in a one year period.
* Delivered multiple projects on time.

**Senior Engineering Manager** **National Semiconductor Corp.**
**10/83 - 2/89** **Santa Clara, CA**

As the design manager and chief technical contributor for the E2CMOS PAL group, was a member of a team of three responsible for the introduction of three second-sourced products. Enlarged the design staff, established methodology and set circuit design criteria for new products under development.

The group's actions enabled the product line to go from zero revenue to greater than $1 million/month in just 12 months. Prior to the start up of the E2CMOS PAL group, designed a Bi-CMOS PAL using lateral Ti-W fuses.

Major accomplishments included:

* Doubled the reliability of the second-sourced devices.
* Participated fully in all aspects of the second-sourcing

licensing agreement.
* Designed the world's first BiCMOS PAL, which was given as a paper at the ISSCC conference in 1986.
* Developed the methodology and theory to improve lateral Ti-W fuse blowing circuitry.

**Program Manager** **RCA**
**4/82 - 10/83** **Sommerville, NJ**

Lead an inter-divisional program to develop 2 micron CMOS technology and a 64K SRAM for the commodity market. Responsible for a team of 15 people who: developed the process, did the modeling, designed the circuits, created the layout, and performed the testing.

Major accomplishments included:

* Created a test chip (4K SRAM) shown to be fully functional, at speed, less than half way thru the program. This test chip was used to flush out the final bugs in the processing.
* Managed the development of three new process features (Poly fuses, Poly Resistors and a 1 mask twin-tub process) that previously did not exist at RCA. Was technically responsible for Poly Resistors and Poly fuses.
* Produced fully functional units at speed on first silicon.(64K SRAM)
* Completed the program within two weeks of an 18 month schedule and under our $1.2 million budget.

**SRAM Design Manager** **National Semiconductor**
**2/78 - 4/82** **West Jordan, Utah**

Hired as a circuit designer into the Santa Clara, Ca memory group to design a Pseudo-Static DRAM memory. Then designed a 4T cell 4K SRAM product. Promoted to Section Head when my first SRAM design went into production on the first mask set, not at the original design size, but on a 10% shrink die which was placed on the wafer across one of the rows.

Later, promoted to SRAM Design Manager and transferred to National's production facility in West Jordan. Supervised a team of six design engineers developing new products and providing production support for SRAM material in the fab.

Major accomplishments included:

* Designed National's first SRAM with a 4T cell using poly resistors.
* Developed a power-on standby circuit for the 2147 (4Kx1 SRAM 55nS) that was eventually copied by Intel.
* Technical Management of the development of the world’s first output short circuit control put into an SRAM.
* Responsible for SRAM products which had a peak production rate of 30 K 4 inch (100 mm) wafers per month
* Lead the team that brought the 2114 (4K SRAM) wafer yield from 50

die/wafer to over 280 die/wafer in 62 days.
* Re-designed the 2114 to get the yield to 375 die / wafer and increased the production run rate to 4 million units per month.

**Circuit Designer** **Hughes Aircraft Co.**
**6/74 - 2/78** **El Segundo, CA**

Won a Hughes Masters Fellowship and worked part-time at Hughes while getting my Masters degree at UCLA. Initially, a Test Engineer testing space flight sub-assemblies, then my first design work was in power supplies. After receiving my MSEE, moved into IC design. Designed custom LSI's using SOS CMOS and a standard cell approach. Team Member designing Hughes 64K CCD Memories and


also solely designed the Analog Buried Channel CCD used for the Liquid Crystal Light Valve.

Major accomplishments included:

* Helped develop the first Liquid Crystal Light Valve at Hughes.
* Designed or tested circuits that are still performing somewhere in space.

**EDUCATION:**

| | | | |
|---|---|---|---|
| BSEE | Drexel University, Philadelphia, PA | June 1974 |
| MSEE | UCLA, Los Angles, CA | June 1976 |

**SIGNIFICANT PUBLICATIONS:** "A Bipolar-CMOS Field Programmable Array" ISSCC Feb 1986; "Liquid-Crystal Electro-Optical Modulators for Optical Processing of Two-Dimensional Data" SPIE Sept. 1977

**SKILL SET:** C, Verilog, Hspice, Dracula, Cadence/Mentor Design Tools