

## APPENDIX B6.

### U.S. Patent No. 4,845,050 (“Kim”) applied to ’336 Patent

As demonstrated in the chart below, claims 1-16 and 65-80 of U.S. Patent No. 8,766,336 are anticipated by Kim, and/or rendered obvious by Kim (in combination with itself, the secondary references identified below, and/or the knowledge of a person of ordinary skill in the art). Kim was published on July 4, 1989, and therefore, Kim qualifies as prior art at least under pre-AIA 35 U.S.C. §§ 102(a) and 102(b).

Claim Number	Claim Language	Exemplary Citations in Kim
1-Pre	1. An electrical junction, comprising	<p>To the extent the preamble is limiting, Kim discloses an electrical junction. For example:</p> <p>Kim discloses metal-semiconductor contacts, which can be used to form electrical junctions.</p> <div style="text-align: center;"> <p style="text-align: center;">FIG. 3C</p> </div> <p>Kim at Fig. 3C; <i>see also</i> Kim at Fig. 2.</p> <p>“Method of Making Mo/TiW or W/TiW Ohmic Contacts to Silicon.” Kim at Title.</p> <p>“Referring now to FIGS. 1 and 2, there is shown a composite body 10 representing a portion of a silicon gate CMOS integrated circuit including contacts made simultaneously to an N+ region, a P+ region and a polycrystalline electrode or line.</p>

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		<p>The composite body 10 includes a substrate 11 of monocrystalline silicon of relatively high resistivity having a pair of active regions 12 and 13 separated by a thick region 14 of silicon dioxide, referred to as field oxide. A region 15 of N-type conductivity and low resistivity is formed in the active region 12 and a region 16 of P-type conductivity and low resistivity is formed in the active region 13.” Kim at 2:54-65.</p> <p>“After suitable cleaning of the surface portions of conductive members 15,17 and 16 of silicon by entirely conventional means such as rinsing in a solution of hot hydrogen peroxide and sulfuric acid followed by a water rinse and a dip in hydrofluoric acid buffered by ammonium fluoride to remove native silicon oxide thereon, the structure of FIG. 3B is placed in sputtering apparatus in which a layer of about 800 Angstroms thick of an alloy consisting of about 10 percent titanium and the remainder tungsten by weight is sputtered over the layer 20 of silicon dioxide and into the apertures 21, 22 and 23 therein to cover the walls of the apertures and also the exposed portions of the conductive members 15, 17 and 16 of silicon semiconductor material.” Kim at 4:11-25.</p> <p>“The first conductor 27 of an alloy of 10% titanium and the remainder tungsten by weight forms a stable low resistance ohmic contact to the silicon conductive members 15, 17 and 16, and also forms a strong bond to the thick layer 20 of silicon dioxide. It is believed that during the sintering step titanium in the conductor 27 at the interface between the conductor 27 and the silicon conductive members 15, 17 and 16 reacts with native silicon dioxide present on the exposed portions of these conductors to form silicon and titanium dioxide, a semiconductor, thereby reducing the interface resistance. Alloys in the range of about 10% to 40% by weight of titanium and the remainder tungsten are particularly suitable for providing low resistance contacts to silicon.” Kim at 4:63-5:4.</p>
1[a]	an interface layer disposed between a contact metal and a group IV semiconductor,	Kim discloses an interface layer disposed between a contact metal and a group IV semiconductor. For example:

Claim Number	Claim Language	Exemplary Citations in Kim
		<p><i>See</i> evidence cited for claim element 62[a] of Appendix A6 (claim chart for Kim applied to '423 Patent), disclosing an interface layer disposed between a conductor (i.e., contact metal) and a silicon-based semiconductor. Silicon is a group IV semiconductor.</p>
1[b]	the semiconductor comprising a source or drain of a transistor,	<p>Kim discloses the semiconductor comprising a source or drain of a transistor. For example:</p> <p>Kim discloses a CMOS circuit with an interface layer disposed between a contact metal and semiconductor with N+ and P+ regions, and a person of ordinary skill in the art would understand that such a configuration could apply to a source or drain region of the transistor.</p> <p>“Referring now to FIGS. 1 and 2, there is shown a composite body 10 representing a portion of a silicon gate CMOS integrated circuit including contacts made simultaneously to an N+ region, a P+ region and a polycrystalline electrode or line. The composite body 10 includes a substrate 11 of monocrystalline silicon of relatively high resistivity having a pair of active regions 12 and 13 separated by a thick region 14 of silicon dioxide, referred to as field oxide. A region 15 of N-type conductivity and low resistivity is formed in the active region 12 and a region 16 of P-type conductivity and low resistivity is formed in the active region 13. A conductive line 17 of polycrystalline silicon which has been heavily doped with N-type activators to provide low resistivity therein is formed over the field oxide region 14.” Kim at 2:54-3:1.</p> <p>“A plurality of conductive members 24, 25 and 26 overlie the insulating members 20 and extend into respective openings 21, 22 and 23 thereof and make low resistance contact to respective conductive members 15, 17 and 16 of silicon of low resistivity. Each of the conductive members 24, 25 and 26 include a first conductor 27 bonded to the layer of silicon dioxide 20 and sintered to a conductive member of silicon of low resistivity and a second conductor 28 bonded to the first conductor 27. The first conductor 27 consists of an alloy of about 10% titanium and the</p>

Claim Number	Claim Language	Exemplary Citations in Kim
		<p>remainder tungsten by weight. The second conductor is constituted of molybdenum.” Kim at 3:6-18.</p> <p>“The conductive members 24, 25 and 26 are formed simultaneously and make low resistance ohmic contact to respective regions 15 and 16, and conductive line 17.” Kim at 3:21-23.</p> <p>“Apertures 21, 22 and 23 are in registry with respective regions 15, 17 and 16 exposing surface portions thereof. After suitable cleaning of the surface portions of conductive members 15, 17 and 16 of silicon by entirely conventional means such as rinsing in a solution of hot hydrogen peroxide and sulfuric acid followed by a water rinse and a dip in hydrofluoric acid buffered by ammonium fluoride to remove native silicon oxide thereon, the structure of FIG. 3B is placed in sputtering apparatus in which a layer of about 800 Angstroms thick of an alloy consisting of about 10 percent titanium and the remainder tungsten by weight is sputtered over the layer 20 of silicon dioxide and into the apertures 21, 22 and 23 therein to cover the walls of the apertures and also the exposed portions of the conductive members 15, 17 and 16 of silicon semiconductor material. Using the same sputtering apparatus without breaking the vacuum therein molybdenum is sputter deposited over the layer of the alloy of titanium and tungsten to a thickness of about 3000 Angstroms.” Kim at 4:11-28.</p> <p>“The first conductor 27 of an alloy of 10% titanium and the remainder tungsten by weight forms a stable low resistance ohmic contact to the silicon conductive members 15, 17 and 16, and also forms a strong bond to the thick layer 20 of silicon dioxide. It is believed that during the sintering step titanium in the conductor 27 at the interface between the conductor 27 and the silicon conductive members 15, 17 and 16 reacts with native silicon dioxide present on the exposed portions of these conductors to form silicon and titanium dioxide, a semiconductor, thereby reducing the interface resistance. Alloys in the range of about 10% to 40%</p>

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		<p>by weight of titanium and the remainder tungsten are particularly suitable for providing low resistance contacts to silicon.” Kim at 4:63-5:4.</p> <p><i>See also</i> Kim at Figs. 1-3.</p> <p>To the extent Kim does not disclose a semiconductor comprising a source or drain of a transistor, this limitation would have been obvious in view of Kim and the knowledge of one of ordinary skill in the art and/or the prior art identified below. A person of ordinary skill in the art at the time of the alleged invention of the ’336 Patent would have understood that the types of metal-semiconductor contacts disclosed in Kim are applicable to, for example, semiconductor source/drain regions in a transistor, and would have found it obvious to apply Kim interface layer configuration to semiconductor source/drain regions in a transistor.</p> <p>Electrical junctions between a metal and a semiconductor, and where the semiconductor is a source or a drain of a transistor device were ubiquitous in the art, and well known to persons of ordinary skill in the art. For example, field effect transistors (“FET”) such as metal-insulator-semiconductor FET (“MISFET”) and metal-oxide-semiconductor FET (“MOSFET”) include source and drain regions formed by doped semiconductors. This is well-known and taught to undergraduate-level students, as disclosed in textbooks such as “Solid State Electronic Devices 4th Edition” by Ben Streetman (“Streetman”). <i>See generally</i> Streetman at Preface; <i>id.</i> at Chapter 8; Fig. 8-19(a) showing n+ doped source/drains in an n-channel MOSFET device, and Fig. 8-19(b) showing p+ doped source/drains in a p-channel MOSFET device. Fig. 8-8 discloses a typical cross-sectional structure of an n-channel MOSFET that is well-known to persons of ordinary skill in the art, where metal (aluminum as shown) is coupled to the source and drain regions of the transistor device to allow interconnection to other transistors in the integrated circuit. (“For example, the surface of a typical integrated circuit is a maze of p and n regions, which must be contacted and interconnected. It is important that such contacts be ohmic, with minimal resistance and no tendency to</p>

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		<p>rectify signals.”) Streetman at 187. As taught in textbooks such as Streetman, this forms a metal-semiconductor junction (contact). <i>Id.</i>, <i>see also id.</i> at chapter 5.7 on metal-semiconductor junctions. A person of ordinary skill would understand that using the FET as intended (where the gate voltage controls the conductivity of the channel between the source and drain terminals) requires some way of coupling the metallic interconnects to the source/drain terminals.</p> <p>As another example, “Principles of CMOS VLSI Design 2nd Edition” by Neil Weste et al. (“Weste”) disclosed in 1993 that “CMOS [Complementary Metal Oxide Silicon] technology has steadily moved to occupy a central position in modern electronic system design ... [and] finds ubiquitous use in the majority of leading edge commercial applications.” Weste at vii. <i>See also id.</i> at Preface, chapter 1 (Introduction to CMOS Circuits) and chapter 2 (MOS Transistor Theory) for basic textbook introductory description of CMOS technology. The building blocks of CMOS integrated circuits are the complementary N-type and P-type MOS transistors (known in the art as nMOS and pMOS). <i>Id.</i> at 5. Fig. 3.2 in Weste shows a cross-sectional view of an nMOS transistor that would have been common knowledge among those of ordinary skill in the art.</p> <div data-bbox="835 987 1837 1295"> <p><b>FIGURE 3.2</b> An nMOS transistor showing the growth of field oxide below the silicon surface</p> </div> <p><i>Id.</i> at Fig. 3.2, showing “source metal” coupled to and forming a junction with n+ doped “source diffusion” region in the semiconductor, and “drain metal” coupled to and forming a junction with n+ doped “drain diffusion” region in the</p>

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		<p>semiconductor. <i>See also id.</i> at 121-122 describing ohmic contacts being formed in the source/drain region; <i>see also id.</i> at Fig. 3.7 and corresponding description of a basic nMOS fabrication process at Chapter 3.2.1; <i>see also id.</i> at Chapter 1.3 describing the structure of nMOS and pMOS transistors shown in Fig. 1.1, including the source and drain regions and connections thereto.</p> <p><i>See also, e.g.:</i></p> <ul style="list-style-type: none"> <li>• U.S. Patent No. 5,292,677 (“Dennison”) (disclosing a semiconductor comprising a source or drain of a transistor);</li> <li>• U.S. Patent No. 6,724,088 (“Jammy”) (disclosing a semiconductor comprising a source or drain of a transistor);</li> </ul> <p>A person of ordinary skill in the art would have found it obvious to apply the interface layer configuration in Kim to semiconductor source/drain regions in a transistor and/or would have been motivated to do so for at least the following exemplary reasons:</p> <ul style="list-style-type: none"> <li>• A person of ordinary skill in the art, in fabricating <i>e.g.</i> MOSFET-based integrated circuit devices, would have needed to couple metal interconnects to the semiconductor source/drain regions in the FET devices to build actual functional circuits, and therefore requires forming metal-semiconductor junctions.</li> <li>• For such exemplary applications, a person of ordinary skill in the art would have been motivated to form an ideal ohmic contact with “minimal resistance.” Streetman at 187. It was well-known in the art that real metal-semiconductor junctions include <i>e.g.</i> surface states that pin the Fermi level and cause real junctions to depart from ideal behavior. <i>Id.</i> at 189. Therefore, it would have been obvious to apply the teachings of Kim that discloses adding an interface layer to depin the Fermi level, thus allowing the choice of metal work function to control the properties of the metal-</li> </ul>

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		<p>semiconductor junction (<i>e.g.</i>, control the Schottky barrier height) to improve on the properties of the ohmic contacts.</p> <ul style="list-style-type: none"> <li>• A person of ordinary skill in the art would have looked to other prior art disclosures relating to metal-semiconductor junctions.</li> <li>• A person of ordinary skill in the art would have understood that the source/drain region in a transistor comprises a semiconductor, and that a metal-semiconductor junction would exist for coupling to the source/drain region. Accordingly, a person of ordinary skill in the art would have understood and been motivated to apply the teachings relating to metal-semiconductor junctions to such junctions in a transistor.</li> <li>• A person of ordinary skill in the art would have understood that the problems generally associated with a metal-semiconductor junction (<i>e.g.</i>, Schottky barrier, contact resistance, etc.) would equally apply to such a junction in the source/drain of the transistor, and would have understood and been motivated to apply solutions to those problems to a metal-semiconductor junction in a transistor.</li> <li>• The above combination of Kim in view of any of the above references would have merely involved a combination of known prior art elements and technologies, according to known methods, to yield predictable results. <i>KSR</i>, 550 U.S. at 416.</li> </ul> <p>A person of ordinary skill in the art would recognize that such a modification to Kim would merely entail:</p> <ul style="list-style-type: none"> <li>• Combining prior art elements according to known methods to yield predictable results (<i>see, e.g.</i>, <i>KSR</i>, 550 U.S. at 416-17), where forming the metal-to-source/drain junction in a transistor would have the predictable characteristics and advantages where the Fermi level is depinned;</li> <li>• Simple substitution of one known element (pinned metal-semiconductor junction) for another (depinned junction) to obtain predictable results (<i>see, e.g.</i>, <i>KSR</i>, 550 U.S. at 416-17);</li> </ul>

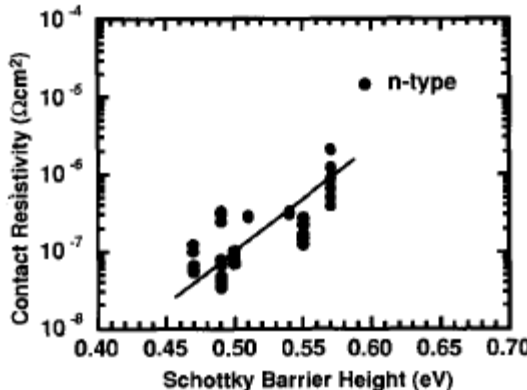


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		<ul style="list-style-type: none"> <li>• Use of known technique to improve similar devices (methods, or products) in the same way, as discussed <i>supra</i> (see, e.g., KSR, 550 U.S. at 416-17);</li> <li>• Applying a known technique to a known device (method, or product) ready for improvement to yield predictable results, as discussed <i>supra</i> (see, e.g., KSR, 550 U.S. at 416-17);</li> <li>• “Obvious to try” – choosing from a finite number of identified, predictable solutions (interface structures that are known to depin the Fermi level and thereby allow independent control of the Schottky barrier based on the metal work function), with a reasonable expectation of success (enhanced ability to control the characteristics of the junction) (see, e.g., KSR, 550 U.S. at 421);</li> <li>• Known work in one field of endeavor may prompt variations of it for use in either the same field or a different one based on design incentives or other market forces if the variations are predictable to one of ordinary skill in the art, such as applying the studies on the underlying physics of metal-semiconductor junctions, and applying the teachings to devices that make use of same (see, e.g., KSR, 550 U.S. at 417);</li> <li>• Some teaching, suggestion, or motivation in the prior art that would have led one of ordinary skill to modify the prior art reference or to combine prior art reference teachings to arrive at the claimed invention, as expressly disclosed in the prior art identified <i>supra</i>.</li> </ul>
1[c]	the interface layer comprising a metal oxide	<p>Kim discloses the interface layer comprising a metal oxide. For example:</p> <p><i>See</i> evidence cited for claim element 62[a] of Appendix A6 (claim chart for Kim applied to '423 Patent), disclosing an interface layer comprising titanium dioxide, which is a metal oxide.</p>
1[d]	and configured to reduce a height of a Schottky barrier between the contact metal and the semiconductor from that which would exist at a contact junction	<p>Kim discloses an interface layer configured to reduce a height of a Schottky barrier between the contact metal and the semiconductor from that which would exist at a contact junction between the contact metal and the semiconductor without the interface layer disposed therebetween. For example:</p>

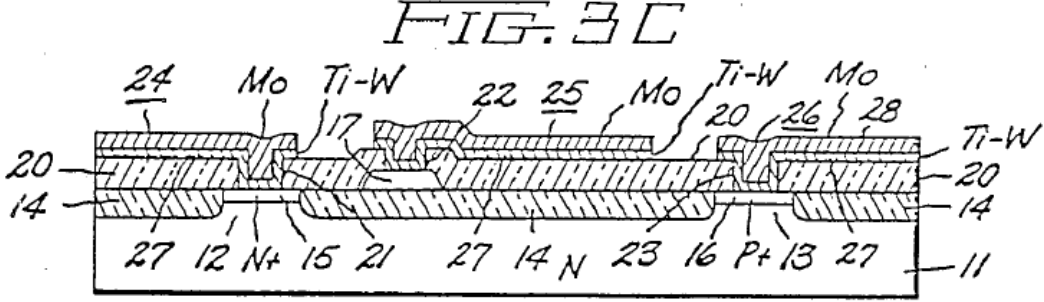
Claim Number	Claim Language	Exemplary Citations in Kim
	<p>between the contact metal and the semiconductor without the interface layer disposed therebetween,</p>	<p>“It is believed that during the sintering step titanium in the conductor 27 at the interface between the conductor 27 and the silicon conductive members 15, 17 and 16 reacts with native silicon dioxide present on the exposed portions of these conductors to form silicon and titanium dioxide, a semiconductor, thereby reducing the interface resistance.” Kim at 4:63-5:1.</p> <p>This limitation would have been obvious in view of Kim and the knowledge of one of ordinary skill in the art and/or the prior art identified below.</p> <p>It would have been obvious to configure the interface layer (that depins the Fermi level) to reduce the height of a Schottky barrier.</p> <p>A person of ordinary skill in the art would understand that electrical junctions between a metal and a semiconductor transistor source/drain were ubiquitous in the art. For example, field effect transistors (“FET”) such as metal-insulator-semiconductor FET (“MISFET”) and metal-oxide-semiconductor FET (“MOSFET”) include source and drain regions formed by doped semiconductors. This is well-known and taught to undergraduate-level students, as disclosed in textbooks such as “Solid State Electronic Devices 4th Edition” by Ben Streetman (“Streetman”). <i>See generally</i> Streetman at Preface; <i>id.</i> at Chapter 8; Fig. 8-19(a) showing n<sup>+</sup> doped source/drains in an n-channel MOSFET device, and Fig. 8-19(b) showing p<sup>+</sup> doped source/drains in a p-channel MOSFET device. Fig. 8-8 discloses a typical cross-sectional structure of an n-channel MOSFET that is well-known to persons of ordinary skill in the art, where metal (aluminum as shown) is coupled to the source and drain regions of the transistor device to allow interconnection to other transistors in the integrated circuit. Furthermore, it was well known in the art that it was desirable for such contacts to be “ohmic” with minimal contact resistance. “For example, the surface of a typical integrated circuit is a maze of p and n regions, which must be contacted and interconnected. It is important that such contacts be ohmic, with minimal resistance and no tendency to rectify signals.” Streetman at 187. Metal-semiconductor junctions are taught at the</p>

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		<p>undergraduate-level, as disclosed in textbooks such as Streetman. <i>Id.</i>, <i>see also id.</i> at chapter 5.7 on metal-semiconductor junctions. Ohmic contacts (in contrast to rectifying Schottky junctions for forming diodes) can be obtained by reducing the height of a Schottky barrier. <i>Id.</i> at chapter 5.7.3 (discussing ohmic contacts); <i>compare to id.</i> at chapter 5.7.2 (discussing rectifying contacts). To the extent Kim does not expressly or inherently disclose that the height of the Schottky barrier is reduced, it would have been obvious to do so in view of the teachings in Kim that discloses an interface layer can depin the Fermi level (thus allow the engineering of the Schottky barrier height by an appropriate choice of metal work function). It would have been obvious to take advantage of this capability to engineer the height of the Schottky barrier at least where an ohmic contact is desired in a practical application, such as where a metal is needed to couple to a source or drain region of a FET device. As discussed <i>supra</i>, the obvious design choice for an ohmic contact would be to reduce the height of the Schottky barrier, in view of Kim and the knowledge of persons of ordinary skill in the art. Moreover, where the presence of the interface layer depins the Fermi level, a person of ordinary skill in the art would understand that the effect on the height of the Schottky barrier for n-doped semiconductor is complementary to the effect for p-doped semiconductor. This is because the sum of the Schottky barrier heights to n-doped semiconductor and p-doped semiconductor is equal to the bandgap. <i>See e.g.</i> E. H. Rhoderick et al., <i>Metal-semiconductor contacts</i> IEE PROC., Vol. 129 Pt. I, No. 1, Feb. 1982 pp. at 1-14 (“Rhoderick”), discussing equation (5) and its derivation in sections 2.1 and 2.2 at 1-2. Accordingly, where the presence of the interface layer causes an increase in the height of the Schottky barrier for <i>e.g.</i> n-doped semiconductor, the height of the Schottky barrier for the same semiconductor (but p-doped) would decrease by the corresponding amount (and vice versa). <i>See also</i> discussion of this claim element in Appendix B7 (claim chart for Bosscher), citing Bosscher at 380. Therefore, where the Fermi level is depinned, the presence of the interface layer would necessarily decrease the height of the Schottky barrier of either n-doped or p-doped semiconductor. Accordingly, to the extent the interface layer disposed between the metal and the semiconductor in Kim increases the height of the</p>

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		<p>Schottky barrier, it would have been obvious to change the doping of the semiconductor to the opposite conductivity type to reduce the height of the Schottky barrier. Alternatively, a person of ordinary skill in the art would understand that the height Schottky barrier can be reduced by appropriate selection of a different metal, if the conductivity type of the semiconductor must be preserved. These are routine design choices that are familiar to those of ordinary skill in the art.</p> <p>Indeed, it was known in the art that a thin oxide layer between a metal-semiconductor junction reduces the Schottky barrier height. <i>See, e.g.</i>, U.S. Patent No. 4,110,488 (“Risko”) at 1:43-50 (“The deposition of the Schottky metal upon an oxide adjacent a silicon substrate has heretofore produced inferior Schottky barriers. An inferior Schottky barrier is a barrier having barrier height substantially below 0.86 eV. Hence, a production of a Schottky barrier on an oxide coated substrate is known to produce a Schottky barrier with a substantially lowered barrier height.”).</p> <p>Further, a person of ordinary skill in the art would have been motivated to configure the interface layer to reduce the height of the Schottky barrier for a metal-to-source/drain contact, as it was known that contact resistance can be further reduced by lowering the height of the Schottky barrier. As Streetman teaches, “it is important that such contacts be ohmic, with minimal resistance...” Streetman at 187. “Study on determining factors of low contact resistivity in transition metal-silicon systems” by S. Zaima et al., Applied Surface Science 870/71 (1993) pp. 624-628 (“Zaima”) studied contact resistivity of different metals to n<sup>+</sup> doped semiconductor with “a thin dielectric layer at the interface” (Zaima at 624) and found that “the contact resistivity for n<sup>+</sup>-Si has a large dependence on the Schottky barrier height.” <i>Id.</i> Zaima teaches that the contact resistance “is ideally governed by the tunneling process of carriers through a Schottky barrier formed at the interface ... [t]herefore, the lower <math>\phi_B</math> [Schottky barrier height] and the higher <math>N_D</math> (doping concentration) result in lower <math>\rho_c</math> [contact resistivity] ...” Zaima at 625,</p>

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		<p>627; <i>see also</i> Fig. 3 showing that decreases in Schottky barrier heights generally leads to lower contact resistivity.</p> <div><table border="1"><caption>Estimated data points from Figure 3</caption><thead><tr><th>Schottky Barrier Height (eV)</th><th>Contact Resistivity (Ωcm²)</th></tr></thead><tbody><tr><td>0.46</td><td>1.5 × 10⁻⁷</td></tr><tr><td>0.47</td><td>1.0 × 10⁻⁷</td></tr><tr><td>0.48</td><td>2.0 × 10⁻⁷</td></tr><tr><td>0.49</td><td>1.2 × 10⁻⁷</td></tr><tr><td>0.50</td><td>3.0 × 10⁻⁷</td></tr><tr><td>0.51</td><td>1.8 × 10⁻⁷</td></tr><tr><td>0.52</td><td>4.0 × 10⁻⁷</td></tr><tr><td>0.53</td><td>2.5 × 10⁻⁷</td></tr><tr><td>0.54</td><td>1.0 × 10⁻⁷</td></tr><tr><td>0.55</td><td>1.5 × 10⁻⁷</td></tr><tr><td>0.56</td><td>3.0 × 10⁻⁷</td></tr><tr><td>0.57</td><td>1.2 × 10⁻⁷</td></tr><tr><td>0.58</td><td>2.0 × 10⁻⁷</td></tr><tr><td>0.59</td><td>4.0 × 10⁻⁷</td></tr><tr><td>0.60</td><td>1.0 × 10⁻⁷</td></tr></tbody></table></div> <p>Fig. 3. Relation between the contact resistivity and the Schottky barrier height for n-type Si.</p> <p>A person of ordinary skill in the art would recognize that such a modification to Kim would merely entail:</p> <ul style="list-style-type: none"><li>Combining prior art elements according to known methods to yield predictable results (<i>see, e.g., KSR</i>, 550 U.S. at 416-17), where depinning the Fermi level is known to overcome the independence of Schottky barrier height from the metal work function, and a lower Schottky barrier height is known to reduce contact resistance;</li><li>Simple substitution of one known element for another to obtain predictable results (<i>see, e.g., KSR</i>, 550 U.S. at 416-17), where substituting a junction where the Fermi level is depinned for one where the Fermi level is pinned allows the designer to choose metal whose workfunction can affect the Schottky barrier height, thereby choosing a material that can lower the</li></ul>	Schottky Barrier Height (eV)	Contact Resistivity (Ωcm²)	0.46	1.5 × 10⁻⁷	0.47	1.0 × 10⁻⁷	0.48	2.0 × 10⁻⁷	0.49	1.2 × 10⁻⁷	0.50	3.0 × 10⁻⁷	0.51	1.8 × 10⁻⁷	0.52	4.0 × 10⁻⁷	0.53	2.5 × 10⁻⁷	0.54	1.0 × 10⁻⁷	0.55	1.5 × 10⁻⁷	0.56	3.0 × 10⁻⁷	0.57	1.2 × 10⁻⁷	0.58	2.0 × 10⁻⁷	0.59	4.0 × 10⁻⁷	0.60	1.0 × 10⁻⁷
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Claim Number	Claim Language	Exemplary Citations in Kim
		<p>Schottky barrier height (compared to a pinned Fermi level where the Schottky barrier height is fixed)</p> <ul style="list-style-type: none"> <li>• Use of known technique to improve similar devices (methods, or products) in the same way (<i>see, e.g., KSR, 550 U.S. at 416-17</i>), where the metal-semiconductor junctions are improved by depinning the Fermi level to allow greater control of e.g. contact resistance, such as by lowering the Schottky barrier height;</li> <li>• Applying a known technique to a known device (method, or product) ready for improvement to yield predictable results, as discussed <i>supra</i> (<i>see, e.g., KSR, 550 U.S. at 416-17</i>);</li> <li>• “Obvious to try” – choosing from a finite number of identified, predictable solutions, with a reasonable expectation of success, as discussed <i>supra</i> (<i>see, e.g., KSR, 550 U.S. at 421</i>);</li> <li>• Known work in one field of endeavor may prompt variations of it for use in either the same field or a different one based on design incentives or other market forces if the variations are predictable to one of ordinary skill in the art, including applications where the contact resistance in a metal-semiconductor junction is an important metric in semiconductor device designs (<i>see, e.g., KSR, 550 U.S. at 417</i>);</li> <li>• Some teaching, suggestion, or motivation in the prior art that would have led one of ordinary skill to modify the prior art reference or to combine prior art reference teachings to arrive at the claimed invention, as expressly disclosed in the prior art identified <i>supra</i></li> </ul>
1[e]	and wherein the electrical junction has a specific contact resistance of less than or equal to approximately 10 $\Omega\text{-}\mu\text{m}^2$ .	<p>Kim discloses an electrical junction that has a specific contact resistance of less than or equal to approximately 10 <math>\Omega\text{-}\mu\text{m}^2</math>. For example:</p> <p>“In contacts made at about 400° C to N+ regions of silicon having a concentration of arsenic atoms of about <math>3 \times 10^{20}</math> atoms per <math>\text{cm}^3</math>, specific contact resistance ranged from 10 to 20 ohm– (micrometer)<sup>2</sup>.” Kim at 5:19-22.</p>

Claim Number	Claim Language	Exemplary Citations in Kim
		<p>“In contacts made at about 650° C to N+ regions of silicon having a concentration of arsenic atoms of about <math>3 \times 10^{20}</math> atoms per <math>\text{cm}^3</math>, specific contact resistance ranged from 8 to 15 ohm– (micrometer)<sup>2</sup>. In contacts made at about 650° C to P+ regions of silicon having a concentration of boron atoms of about <math>7 \times 10^{19}</math> atoms per <math>\text{cm}^3</math>, specific contact resistance ranged from 10 to 20 ohm– (micrometer)<sup>2</sup>.” Kim at 5:27-34.</p>
2	2. The electrical junction of claim 1, wherein the semiconductor comprises an n-type doped source or drain of a transistor.	<p>Kim discloses a semiconductor comprising an n-type doped source or drain of a transistor. For example:</p> <p>Kim discloses n-type semiconductor doping.</p>  <p>Kim at Fig. 3C; <i>see also</i> Kim at Fig. 2.</p> <p>“Referring now to FIGS. 1 and 2, there is shown a composite body 10 representing a portion of a silicon gate CMOS integrated circuit including contacts made simultaneously to an N+ region, a P+ region and a polycrystalline electrode or line. The composite body 10 includes a substrate 11 of monocrystalline silicon of relatively high resistivity having a pair of active regions 12 and 13 separated by a thick region 14 of silicon dioxide, referred to as field oxide. A region 15 of N-type</p>

Claim Number	Claim Language	Exemplary Citations in Kim
		<p>conductivity and low resistivity is formed in the active region 12 and a region 16 of P-type conductivity and low resistivity is formed in the active region 13.” Kim at 2:54-65.</p> <p><i>See also supra</i> claim element 1[b] (disclosures relating to source or drain of transistor).</p>
3	<p>3. The electrical junction of claim 1, wherein the electrical junction has a specific contact resistance of less than or equal to approximately <math>1\ \Omega\text{-}\mu\text{m}^2</math>.</p>	<p>Kim discloses an electrical junction wherein the electrical junction has a specific contact resistance of less than or equal to approximately <math>1\ \Omega\text{-}\mu\text{m}^2</math>. For example:</p> <p>This limitation would have been obvious in view of Kim and the knowledge of one of ordinary skill in the art and/or the prior art identified below.</p> <p>A person of ordinary skill in the art at the time of the alleged invention of the ’336 Patent would have understood that an interface layer between a contact metal and conductor could be used to obtain a contact resistance of less than or equal to approximately <math>1\ \Omega\text{-}\mu\text{m}^2</math>, and would have found it obvious to modify Kim to obtain a contact resistance of less than or equal to approximately <math>1\ \Omega\text{-}\mu\text{m}^2</math>. For example, C.Y. Chang et al., <i>Specific Contact Resistance of Metal-Semiconductor Barriers</i>, 14 SOLID-STATE ELECTRONICS 541 (1971) (“Chang”) discloses that contact resistance of less than or equal to approximately <math>1\ \Omega\text{-}\mu\text{m}^2</math> can be achieved at metal-semiconductor junctions. <i>See, e.g.</i>, Chang at Figs. 3, 4, 5, 7, 8.</p> <p>A person of ordinary skill in the art would have found it obvious and been motivated to obtain a contact resistance less than or equal to approximately <math>1\ \Omega\text{-}\mu\text{m}^2</math> for at least the following exemplary reasons:</p> <ul style="list-style-type: none"> <li>• A person of ordinary skill in the art would have looked to other prior art disclosures relating to metal-semiconductor junctions.</li> <li>• A person of ordinary skill in the art would have understood that contact resistance inherently existed between a metal and semiconductor junction, and that it would have been desirable to reduce contact resistance to provide</li> </ul>



Claim Number	Claim Language	Exemplary Citations in Kim
		<p>a more efficient and improved junction. Accordingly, a person of ordinary skill in the art would have found it obvious and been motivated to design and implement a metal-semiconductor junction with as small a contact resistance as possible, including a junction with a contact resistance that less than <math>1\ \Omega\text{-}\mu\text{m}^2</math>. This motivation is reflected in, for example, the 2001 International Tech Roadmap for Semiconductor – Interconnect at 7 (“2001 Tech Roadmap”), which discloses decreasing contact resistance through the passage of time; as such, a person of ordinary skill in the art would have understood that a goal of continued research into semiconductor process and fabrication technology would have been to decrease contact resistance.</p> <ul style="list-style-type: none"> <li>• Obtaining a contact resistance less than <math>1\ \Omega\text{-}\mu\text{m}^2</math> was already known, and a person of ordinary skill in the art would have a reasonable expectation of success in implementing an interface layer between a metal-semiconductor junction to achieve a contact resistance in this range.</li> <li>• As disclosed in Chang, a person of ordinary skill in the art would have understood that contact resistance could be altered by appropriate doping (among other known variables). <i>See, e.g.</i>, Chang at 544 (“In the tunneling range (<math>&gt; 10^{18}\ \text{cm}^{-3}</math>), however, <math>R_c</math> becomes a strong function of doping.”). And a person of ordinary skill would have the knowledge and ability to adjust doping accordingly to obtain a particular contact resistance, including a contact resistance less than <math>1\ \Omega\text{-}\mu\text{m}^2</math>.</li> <li>• There is no unexpected result associated with the claimed range (“less than or equal to approximately <math>1\ \Omega\text{-}\mu\text{m}^2</math>”), and the prior art discloses values within the claimed range. Given that the claimed range does not provide an unexpected result, and given the similarities of the teachings of Kim and the above identified references, there would have been a reasonable expectation of success in implementing an interface layer in Kim that would achieve a contact resistance of less than or equal to approximately <math>1\ \Omega\text{-}\mu\text{m}^2</math>.</li> <li>• Contact resistance was a known variable, and if “less than or equal to approximately <math>1\ \Omega\text{-}\mu\text{m}^2</math>” is an optimum number for the contact resistance in a metal-semiconductor junction, the claimed range is obvious because</li> </ul>

Claim Number	Claim Language	Exemplary Citations in Kim
		<p>“discovery of an optimum value of a result effective variable in a known process is ordinarily within the skill of the art.” <i>In re Boesch</i>, 617 F.2d 272, 276 (C.C.P.A. 1980); <i>In re Aller</i>, 220 F.2d 454, 456 (C.C.P.A. 1955); <i>see also In re Applied Materials, Inc.</i>, 692 F.3d 1289, 1295 (Fed. Cir. 2012).</p> <ul style="list-style-type: none"> <li>• A person of ordinary skill in the art would have understood that obtaining a contact resistance with a particular value is nothing more than routine optimization yielding predictable results.</li> </ul> <p>A person of ordinary skill in the art would recognize that such a modification to Kim would merely entail:</p> <ul style="list-style-type: none"> <li>• Combining prior art elements according to known methods to yield predictable results (<i>see, e.g., KSR</i>, 550 U.S. at 416-17), such as, for example, using the appropriate doping (among other variables) to obtain a particular contact resistance;</li> <li>• Simple substitution of one known element for another to obtain predictable results (<i>see, e.g., KSR</i>, 550 U.S. at 416-17), for example, by using the appropriate doping (among other variables) to obtain a particular contact resistance;</li> <li>• Use of known technique to improve similar devices (methods, or products) in the same way (<i>see, e.g., KSR</i>, 550 U.S. at 416-17);</li> <li>• Applying a known technique to a known device (method, or product) ready for improvement to yield predictable results, as discussed <i>supra</i> (<i>see, e.g., KSR</i>, 550 U.S. at 416-17);</li> <li>• “Obvious to try” – choosing from a finite number of identified, predictable solutions, with a reasonable expectation of success, as discussed <i>supra</i> (<i>see, e.g., KSR</i>, 550 U.S. at 421);</li> <li>• Known work in one field of endeavor may prompt variations of it for use in either the same field or a different one based on design incentives or other market forces if the variations are predictable to one of ordinary skill in the</li> </ul>

Claim Number	Claim Language	Exemplary Citations in Kim
		<p>art, such as the motivation to use a lower contact resistance, as discussed <i>supra</i> (see, e.g., KSR, 550 U.S. at 417);</p> <ul style="list-style-type: none"> <li>Some teaching, suggestion, or motivation in the prior art that would have led one of ordinary skill to modify the prior art reference or to combine prior art reference teachings to arrive at the claimed invention, as expressly disclosed in the prior art identified <i>supra</i>.</li> </ul>
4	4. The electrical junction of claim 3, wherein the semiconductor comprises an n-type doped source or drain of a transistor.	<p>Kim discloses a semiconductor comprising an n-type doped source or drain of a transistor. For example:</p> <p><i>See supra</i> evidence cited for claim 2.</p>
5-Pre	5. An electrical junction comprising	<p>To the extent the preamble is limiting, Kim discloses an electrical junction. For example:</p> <p><i>See supra</i> evidence cited for claim element 1-Pre.</p>
5[a]	an interface layer disposed between a contact metal and a semiconductor,	<p>Kim discloses an interface layer disposed between a contact metal and a semiconductor. For example:</p> <p><i>See supra</i> evidence cited for claim element 1[a].</p>
5[b]	the semiconductor comprising a source or drain of a transistor,	<p>Kim discloses the semiconductor comprising a source or drain of a transistor. For example:</p> <p><i>See supra</i> evidence cited for claim element 1[b].</p>
5[c]	the interface layer being a metal oxide	<p>Kim discloses the interface layer being a metal oxide. For example:</p> <p><i>See supra</i> evidence cited for claim element 1[c].</p>
5[d]	and sufficiently thick to depin a Fermi level of the semiconductor,	<p>Kim discloses an interface layer sufficiently thick to depin a Fermi level of the semiconductor. For example:</p> <p><i>See</i> evidence cited for claim element 62[b] of Appendix A6 (claim chart for Kim applied to '423 Patent).</p>

Claim Number	Claim Language	Exemplary Citations in Kim
5[e]	yet sufficiently thin to provide the junction with a specific contact resistance of less than or equal to approximately $10\ \Omega\text{-}\mu\text{m}^2$ .	Kim discloses an interface layer sufficiently thin to provide the junction with a specific contact resistance of less than or equal to approximately $10\ \Omega\text{-}\mu\text{m}^2$ .  <i>See supra</i> evidence cited for claim element 1[e].
6	6. The electrical junction of claim 5, wherein the semiconductor comprises an n-type doped source or drain of a transistor.	Kim discloses a semiconductor comprising an n-type doped source or drain of a transistor. For example:  <i>See supra</i> evidence cited for claim 2.
7	7. The electrical junction of claim 5, wherein the electrical junction has a specific contact resistance of less than or equal to approximately $1\ \Omega\text{-}\mu\text{m}^2$ .	Kim discloses an electrical junction wherein the electrical junction has a specific contact resistance of less than or equal to approximately $1\ \Omega\text{-}\mu\text{m}^2$ . For example:  <i>See supra</i> evidence cited for claim 3.
8	8. The electrical junction of claim 7, wherein the semiconductor comprises an n-type doped source or drain of a transistor.	Kim discloses a semiconductor comprising an n-type doped source or drain of a transistor. For example:  <i>See supra</i> evidence cited for claim 2.
9-Pre	9. An electrical junction, comprising	To the extent the preamble is limiting, Kim discloses an electrical junction. For example:  <i>See supra</i> evidence cited for claim element 1-Pre.
9[a]	a conductor;	Kim discloses a conductor. For example:  <i>See</i> evidence cited for claim element 62[a] of Appendix A6 (claim chart for Kim applied to '423 Patent), disclosing a conductor.
9[b]	a semiconductor selected from a list consisting of Si, Ge, C (a crystal structure of which is selected from a list comprising a diamond lattice, a fulleride or a polymer), an alloy of Ge and Si, an	Kim discloses a semiconductor selected from a list consisting of Si, Ge, C (a crystal structure of which is selected from a list comprising a diamond lattice, a fulleride or a polymer), an alloy of Ge and Si, an alloy of Ge and C, an alloy of Si and C, and an alloy of Si, Ge, and C. For example:

Claim Number	Claim Language	Exemplary Citations in Kim
	alloy of Ge and C, an alloy of Si and C, and an alloy of Si, Ge, and C;	<i>See</i> evidence cited for claim element 62[a] of Appendix A6 (claim chart for Kim applied to '423 Patent), disclosing a silicon-based semiconductor.
9[c]	and an interface layer disposed therebetween,	Kim discloses an interface layer disposed therebetween. For example:  <i>See</i> evidence cited for claim element 62[a] of Appendix A6 (claim chart for Kim applied to '423 Patent).
9[d]	the semiconductor comprising a source or drain of a transistor,	Kim discloses a semiconductor comprising a source or drain of a transistor. For example:  <i>See supra</i> evidence cited for claim element 1[b].
9[e]	the interface layer comprising a metal oxide	Kim discloses the interface layer comprising a metal oxide. For example:  <i>See supra</i> evidence cited for claim element 1[c].
9[f]	and being sufficiently thick to approximately equal a penetration depth of metal induced gap states (MIGS) in the semiconductor which would be present the interface layer were absent,	Kim discloses an interface layer being sufficiently thick to approximately equal a penetration depth of metal induced gap states (MIGS) in the semiconductor which would be present the interface layer were absent. For example:  According to Plaintiff's infringement contentions, 5nm (or in the alternative, 3nm) is a thickness sufficient to approximately equal a penetration depth of metal induced gap states (MIGS) in the semiconductor which would be present if the interface layer were absent. Ex. B to Plaintiff's infringement contentions at 50. However, Plaintiff elsewhere contends that the conductor electron wave function distance is 1-3nm, or less. Ex. B to Plaintiff's infringement contentions at 16. Thus, consistent with Plaintiff's infringement theory and apparent claim construction, this limitation is satisfied by a thickness of 5 nm, or 3 nm, or 1-3nm or less. To the extent Kim does not expressly or inherently disclose an interface layer within these ranges, it would have been obvious to choose a thickness that is approximately less than 5 nm.

Claim Number	Claim Language	Exemplary Citations in Kim
		<p><i>See, e.g.</i> discussion of obviousness and cited evidence in limitation of 1[d] of Appendices C1 through C10 (regarding the thickness of the interface layer).</p> <p>This limitation would have been obvious in view of Kim and the knowledge of one of ordinary skill in the art and/or the prior art identified in the Appendices identified <i>supra</i>.</p>
9[g]	yet sufficiently thin to provide the junction with a specific contact resistance of less than or equal to approximately 10 $\Omega\text{-}\mu\text{m}^2$ .	<p>Kim discloses an interface layer sufficiently thin to provide the junction with a specific contact resistance of less than or equal to approximately 10 <math>\Omega\text{-}\mu\text{m}^2</math>. For example:</p> <p><i>See supra</i> evidence cited for claim element 1[e].</p>
10	10. The electrical junction of claim 9, wherein the semiconductor comprises an n-type doped source or drain of a transistor.	<p>Kim discloses a semiconductor comprising an n-type doped source or drain of a transistor. For example:</p> <p><i>See supra</i> evidence cited for claim 2.</p>
11	11. The electrical junction of claim 9, wherein the electrical junction has a specific contact resistance of less than or equal to approximately 1 $\Omega\text{-}\mu\text{m}^2$ .	<p>Kim discloses an electrical junction wherein the electrical junction has a specific contact resistance of less than or equal to approximately 1 <math>\Omega\text{-}\mu\text{m}^2</math>. For example:</p> <p><i>See supra</i> evidence cited for claim 3.</p>
12	12. The electrical junction of claim 11, wherein the semiconductor comprises an n-type doped source or drain of a transistor.	<p>Kim discloses a semiconductor comprising an n-type doped source or drain of a transistor. For example:</p> <p><i>See supra</i> evidence cited for claim 2.</p>
13-Pre	13. An electrical junction, comprising	<p>To the extent the preamble is limiting, Kim discloses an electrical junction. For example:</p> <p><i>See supra</i> evidence cited for claim element 1-Pre.</p>
13[a]	a semiconductor and a conductor separated from the semiconductor	<p>Kim discloses a semiconductor and a conductor separated from the semiconductor by an interface layer comprising a metal oxide. For example:</p>

Claim Number	Claim Language	Exemplary Citations in Kim
	by an interface layer comprising a metal oxide	<p><i>See</i> evidence cited for claim element 62[a] of Appendix A6 (claim chart for Kim applied to '423 Patent), disclosing an interface layer disposed between a conductor and a silicon-based semiconductor.</p> <p><i>See supra</i> evidence cited for claim element 1[c] (disclosures related to interface layer comprising a metal oxide).</p>
13[b]	and having a thickness sufficient to depin a Fermi level of the conductor in a vicinity of the junction	<p>Kim discloses an interface layer having a thickness sufficient to depin a Fermi level of the conductor in a vicinity of the junction. For example:</p> <p><i>See</i> evidence cited for claim element 62[b] of Appendix A6 (claim chart for Kim applied to '423 Patent).</p>
13[c]	yet thin enough to provide the junction with a specific contact resistance of less than or equal to approximately $10\ \Omega\text{-}\mu\text{m}^2$ ,	<p>Kim discloses an interface layer thin enough to provide the junction with a specific contact resistance of less than or equal to approximately <math>10\ \Omega\text{-}\mu\text{m}^2</math>. For example:</p> <p><i>See supra</i> evidence cited for claim element 1[e].</p>
13[d]	wherein the semiconductor comprises a source or drain of a transistor.	<p>Kim discloses a semiconductor comprising a source or drain of a transistor. For example:</p> <p><i>See supra</i> evidence cited for claim element 1[b].</p>
14	14. The electrical junction of claim 13, wherein the semiconductor comprises an n-type doped source or drain of a transistor.	<p>Kim discloses a semiconductor comprising an n-type doped source or drain of a transistor. For example:</p> <p><i>See supra</i> evidence cited for claim 2.</p>
15	15. The electrical junction of claim 13, wherein the electrical junction has a specific contact resistance of less than or equal to approximately $1\ \Omega\text{-}\mu\text{m}^2$ .	<p>Kim discloses an electrical junction wherein the electrical junction has a specific contact resistance of less than or equal to approximately <math>1\ \Omega\text{-}\mu\text{m}^2</math>. For example:</p> <p><i>See supra</i> evidence cited for claim 3.</p>
16	16. The electrical junction of claim 15, wherein the semiconductor	<p>Kim discloses a semiconductor comprising an n-type doped source or drain of a transistor. For example:</p>

Claim Number	Claim Language	Exemplary Citations in Kim
	comprises an n-type doped source or drain of a transistor.	<i>See supra</i> evidence cited for claim 2.
65-Pre	65. An electrical junction comprising	To the extent the preamble is limiting, Kim discloses an electrical junction. For example:  <i>See supra</i> evidence cited for claim element 1-Pre.
65[a]	an interface layer disposed between a contact metal and a group IV semiconductor,	Kim discloses an interface layer disposed between a contact metal and a group IV semiconductor. For example:  <i>See supra</i> evidence cited for claim element 1[a].
65[b]	the interface layer comprising a metal oxide	Kim discloses the interface layer comprising a metal oxide. For example:  <i>See supra</i> evidence cited for claim element 1[c].
65[c]	and configured to reduce a height of a Schottky barrier between the contact metal and the semiconductor from that which would exist at a contact junction between the contact metal and the semiconductor without the interface layer disposed therebetween,	Kim discloses an interface layer configured to reduce a height of a Schottky barrier between the contact metal and the semiconductor from that which would exist at a contact junction between the contact metal and the semiconductor without the interface layer disposed therebetween. For example:  <i>See supra</i> evidence cited for claim element 1[d].
65[d]	and wherein the electrical junction has a specific contact resistance of less than or equal to approximately 1000 $\Omega\text{-}\mu\text{m}^2$ ,	Kim discloses an electrical junction that has a specific contact resistance of less than or equal to approximately 1000 $\Omega\text{-}\mu\text{m}^2$ . For example:  “In contacts made at about 400° C to N+ regions of silicon having a concentration of arsenic atoms of about $3\times 10^{20}$ atoms per $\text{cm}^3$ , specific contact resistance ranged from 10 to 20 ohm– (micrometer) <sup>2</sup> .” Kim at 5:19-22.  “In contacts made at about 650° C to N+ regions of silicon having a concentration of arsenic atoms of about $3\times 10^{20}$ atoms per $\text{cm}^3$ , specific contact resistance ranged



Claim Number	Claim Language	Exemplary Citations in Kim
		<p>from 8 to 15 ohm– (micrometer)<sup>2</sup>. In contacts made at about 650° C to P+ regions of silicon having a concentration of boron atoms of about <math>7 \times 10^{19}</math> atoms per cm<sup>3</sup>, specific contact resistance ranged from 10 to 20 ohm– (micrometer)<sup>2</sup>.” Kim at 5:27-34.</p>
65[e]	<p>wherein the contact metal is a metal or a stack of metals deposited on the interface layer.</p>	<p>Kim discloses a contact metal wherein the contact metal is a metal or a stack of metals deposited on the interface layer. For example:</p> <div data-bbox="835 560 1879 860" data-label="Image"> </div> <p>Kim at Fig. 3C; <i>see also</i> Kim at Fig. 2.</p> <p>“Referring now to FIGS. 1 and 2, there is shown a composite body 10 representing a portion of a silicon gate CMOS integrated circuit including contacts made simultaneously to an N+ region, a P+ region and a polycrystalline electrode or line. The composite body 10 includes a substrate 11 of monocrystalline silicon of relatively high resistivity having a pair of active regions 12 and 13 separated by a thick region 14 of silicon dioxide, referred to as field oxide. A region 15 of N-type conductivity and low resistivity is formed in the active region 12 and a region 16 of P-type conductivity and low resistivity is formed in the active region 13.” Kim at 2:54-65.</p> <p>“After suitable cleaning of the surface portions of conductive members 15,17 and 16 of silicon by entirely conventional means such as rinsing in a solution of hot</p>

Claim Number	Claim Language	Exemplary Citations in Kim
		hydrogen peroxide and sulfuric acid followed by a water rinse and a dip in hydrofluoric acid buffered by ammonium fluoride to remove native silicon oxide thereon, the structure of FIG. 3B is placed in sputtering apparatus in which a layer of about 800 Angstroms thick of an alloy consisting of about 10 percent titanium and the remainder tungsten by weight is sputtered over the layer 20 of silicon dioxide and into the apertures 21, 22 and 23 therein to cover the walls of the apertures and also the exposed portions of the conductive members 15, 17 and 16 of silicon semiconductor material.” Kim at 4:11-25.
66	66. The electrical junction of claim 65, wherein the electrical junction has a specific contact resistance of less than or equal to approximately $100\ \Omega\text{-}\mu\text{m}^2$ .	Kim discloses an electrical junction that has a specific contact resistance of less than or equal to approximately $100\ \Omega\text{-}\mu\text{m}^2$ . For example:  “In contacts made at about $400^\circ\text{C}$ to N+ regions of silicon having a concentration of arsenic atoms of about $3\times 10^{20}$ atoms per $\text{cm}^3$ , specific contact resistance ranged from 10 to 20 ohm– (micrometer) <sup>2</sup> .” Kim at 5:19-22.  “In contacts made at about $650^\circ\text{C}$ to N+ regions of silicon having a concentration of arsenic atoms of about $3\times 10^{20}$ atoms per $\text{cm}^3$ , specific contact resistance ranged from 8 to 15 ohm– (micrometer) <sup>2</sup> . In contacts made at about $650^\circ\text{C}$ to P+ regions of silicon having a concentration of boron atoms of about $7\times 10^{19}$ atoms per $\text{cm}^3$ , specific contact resistance ranged from 10 to 20 ohm– (micrometer) <sup>2</sup> .” Kim at 5:27-34.
67	67. The electrical junction of claim 65, wherein the electrical junction has a specific contact resistance of less than or equal to approximately $10\ \Omega\text{-}\mu\text{m}^2$ .	Kim discloses an electrical junction that has a specific contact resistance of less than or equal to approximately $10\ \Omega\text{-}\mu\text{m}^2$ . For example:  <i>See supra</i> evidence cited for claim element 1[e].
68-Pre	68. An electrical junction comprising	To the extent the preamble is limiting, Kim discloses an electrical junction. For example:  <i>See supra</i> evidence cited for claim element 1-Pre.

Claim Number	Claim Language	Exemplary Citations in Kim
68[a]	an interface layer disposed between a contact metal and a semiconductor,	Kim discloses an interface layer disposed between a contact metal and a semiconductor. For example:  <i>See supra</i> evidence cited for claim element 1[a].
68[b]	the interface layer being a metal oxide and	Kim discloses the interface layer being a metal oxide. For example:  <i>See supra</i> evidence cited for claim element 1[c].
68[c]	sufficiently thick to depin a Fermi level of the semiconductor,	Kim discloses an interface layer sufficiently thick to depin a Fermi level of the semiconductor. For example:  <i>See supra</i> evidence cited for claim element 5[d].
68[d]	yet sufficiently thin to provide the junction with a specific contact resistance of less than or equal to approximately $1000\ \Omega\text{-}\mu\text{m}^2$ ,	Kim discloses an interface layer sufficiently thin to provide the junction with a specific contact resistance of less than or equal to approximately $1000\ \Omega\text{-}\mu\text{m}^2$ . For example:  <i>See supra</i> evidence cited for claim element 65[d].
68[e]	wherein the contact metal is a metal or a stack of metals deposited on the interface layer.	Kim discloses a contact metal wherein the contact metal is a metal or a stack of metals deposited on the interface layer. For example:  <i>See supra</i> evidence cited for claim element 65[e].
69	69. The electrical junction of claim 68, wherein the electrical junction has a specific contact resistance of less than or equal to approximately $100\ \Omega\text{-}\mu\text{m}^2$ .	Kim discloses an electrical junction that has a specific contact resistance of less than or equal to approximately $100\ \Omega\text{-}\mu\text{m}^2$ . For example:  <i>See supra</i> evidence cited for claim 66.
70	70. The electrical junction of claim 68, wherein the electrical junction has a specific contact resistance of less than or equal to approximately $10\ \Omega\text{-}\mu\text{m}^2$ .	Kim discloses an electrical junction that has a specific contact resistance of less than or equal to approximately $10\ \Omega\text{-}\mu\text{m}^2$ . For example:  <i>See supra</i> evidence cited for claim element 1[e].

Claim Number	Claim Language	Exemplary Citations in Kim
71-Pre	71. An electrical junction, comprising	To the extent the preamble is limiting, Kim discloses an electrical junction. For example:  <i>See supra</i> evidence cited for claim element 1-Pre.
71[a]	a conductor;	Kim discloses a conductor. For example:  <i>See supra</i> evidence cited for claim element 9[a].
71[b]	a semiconductor selected from a list consisting of Si, Ge, C (a crystal structure of which is selected from a list comprising a diamond lattice, a fulleride or a polymer), an alloy of Ge and Si, an alloy of Ge and C, an alloy of Si and C, and an alloy of Si, Ge, and C;	Kim discloses a semiconductor selected from a list consisting of Si, Ge, C (a crystal structure of which is selected from a list comprising a diamond lattice, a fulleride or a polymer), an alloy of Ge and Si, an alloy of Ge and C, an alloy of Si and C, and an alloy of Si, Ge, and C. For example:  <i>See supra</i> evidence cited for claim element 9[b].
71[c]	and an interface layer disposed therebetween,	Kim discloses an interface layer disposed therebetween. For example:  <i>See</i> evidence cited for claim element 62[a] of Appendix A6 (claim chart for Kim applied to '423 Patent).
71[d]	the interface layer comprising a metal oxide	Kim discloses the interface layer comprising a metal oxide. For example:  <i>See supra</i> evidence cited for claim element 1[c].
71[e]	and being sufficiently thick to approximately equal a penetration depth of metal induced gap states (MIGS) in the semiconductor which would be present the interface layer were absent,	Kim discloses an interface layer being sufficiently thick to approximately equal a penetration depth of metal induced gap states (MIGS) in the semiconductor which would be present the interface layer were absent. For example:  <i>See supra</i> evidence cited for claim element 9[f].

Claim Number	Claim Language	Exemplary Citations in Kim
71[f]	yet sufficiently thin to provide the junction with a specific contact resistance of less than or equal to approximately $1000\ \Omega\text{-}\mu\text{m}^2$ ,	Kim discloses an interface layer sufficiently thin to provide the junction with a specific contact resistance of less than or equal to approximately $1000\ \Omega\text{-}\mu\text{m}^2$ . For example:  <i>See supra</i> evidence cited for claim element 65[d].
71[g]	wherein the conductor is a metal or a stack of metals deposited on the interface layer.	Kim discloses a conductor wherein the conductor is a metal or a stack of metals deposited on the interface layer. For example:  <i>See supra</i> evidence cited for claim element 65[e].
72	72. The electrical junction of claim 71, wherein the electrical junction has a specific contact resistance of less than or equal to approximately $100\ \Omega\text{-}\mu\text{m}^2$ .	Kim discloses an electrical junction that has a specific contact resistance of less than or equal to approximately $100\ \Omega\text{-}\mu\text{m}^2$ . For example:  <i>See supra</i> evidence cited for claim 66.
73	73. The electrical junction of claim 71, wherein the electrical junction has a specific contact resistance of less than or equal to approximately $10\ \Omega\text{-}\mu\text{m}^2$ .	Kim discloses an electrical junction that has a specific contact resistance of less than or equal to approximately $10\ \Omega\text{-}\mu\text{m}^2$ . For example:  <i>See supra</i> evidence cited for claim element 1[e].
74-Pre	74. An electrical junction, comprising,	To the extent the preamble is limiting, Kim discloses an electrical junction. For example:  <i>See supra</i> evidence cited for claim element 1-Pre.
74[a]	a semiconductor and a conductor separated from the semiconductor by an interface layer comprising a metal oxide	Kim discloses a semiconductor and a conductor separated from the semiconductor by an interface layer comprising a metal oxide. For example:  <i>See supra</i> evidence cited for claim element 13[a].
74[b]	and having a thickness sufficient to depin a Fermi level of the	Kim discloses an interface layer having a thickness sufficient to depin a Fermi level of the conductor in a vicinity of the junction. For example:

Claim Number	Claim Language	Exemplary Citations in Kim
	conductor in a vicinity of the junction	<i>See</i> evidence cited for claim element 62[b] of Appendix A6 (claim chart for Kim applied to '423 Patent).
74[c]	yet thin enough to provide the junction with a specific contact resistance of less than or equal to approximately 1000 $\Omega\text{-}\mu\text{m}^2$ ,	Kim discloses an interface layer yet thin enough to provide the junction with a specific contact resistance of less than or equal to approximately 1000 $\Omega\text{-}\mu\text{m}^2$ . For example:  <i>See supra</i> evidence cited for claim element 65[d].
74[d]	wherein the conductor is a metal or a stack of metals deposited on the interface layer.	Kim discloses a conductor wherein the conductor is a metal or a stack of metals deposited on the interface layer. For example:  <i>See supra</i> evidence cited for claim element 65[e].
75	75. The electrical junction of claim 74, wherein the electrical junction has a specific contact resistance of less than or equal to approximately 100 $\Omega\text{-}\mu\text{m}^2$ .	Kim discloses an electrical junction that has a specific contact resistance of less than or equal to approximately 100 $\Omega\text{-}\mu\text{m}^2$ . For example:  <i>See supra</i> evidence cited for claim 66.
76	76. The electrical junction of claim 75, wherein the electrical junction has a specific contact resistance of less than or equal to approximately 10 $\Omega\text{-}\mu\text{m}^2$ .	Kim discloses an electrical junction that has a specific contact resistance of less than or equal to approximately 10 $\Omega\text{-}\mu\text{m}^2$ . For example:  <i>See supra</i> evidence cited for claim element 1[e].
77-Pre	77. An electrical junction, comprising	To the extent the preamble is limiting, Kim discloses an electrical junction. For example:  <i>See supra</i> evidence cited for claim element 1-Pre.
77[a]	an n-type doped Si semiconductor and a conductor separated from the semiconductor by an interface layer comprising a metal oxide	Kim discloses an n-type doped Si semiconductor and a conductor separated from the semiconductor by an interface layer comprising a metal oxide. For example:  <i>See</i> evidence cited for claim element 62[a] of Appendix A6 (claim chart for Kim applied to '423 Patent), disclosing an interface layer disposed between a conductor and a silicon-based semiconductor.

Claim Number	Claim Language	Exemplary Citations in Kim
		<p><i>See supra</i> evidence cited for claim element 1[c] (disclosures relating to interface layer comprising a metal oxide).</p> <p><i>See supra</i> evidence cited for claim 2 (disclosures relating to n-type doped semiconductor).</p>
77[b]	and having a thickness sufficient to depin a Fermi level of the conductor in a vicinity of the junction	<p>Kim discloses an interface layer having a thickness sufficient to depin a Fermi level of the conductor in a vicinity of the junction. For example:</p> <p><i>See</i> evidence cited for claim element 62[b] of Appendix A6 (claim chart for Kim applied to '423 Patent).</p>
77[c]	yet thin enough to provide the junction with a specific contact resistance of less than or equal to approximately $1000\ \Omega\text{-}\mu\text{m}^2$ .	<p>Kim discloses an interface layer thin enough to provide the junction with a specific contact resistance of less than or equal to approximately <math>1000\ \Omega\text{-}\mu\text{m}^2</math>. For example:</p> <p><i>See supra</i> evidence cited for claim element 65[d].</p>
78	78. The electrical junction of claim 77, wherein the electrical junction has a specific contact resistance of less than or equal to approximately $100\ \Omega\text{-}\mu\text{m}^2$ .	<p>Kim discloses an electrical junction that has a specific contact resistance of less than or equal to approximately <math>100\ \Omega\text{-}\mu\text{m}^2</math>. For example:</p> <p><i>See supra</i> evidence cited for claim 66.</p>
79	79. The electrical junction of claim 77, wherein the electrical junction has a specific contact resistance of less than or equal to approximately $10\ \Omega\text{-}\mu\text{m}^2$ .	<p>Kim discloses an electrical junction that has a specific contact resistance of less than or equal to approximately <math>10\ \Omega\text{-}\mu\text{m}^2</math>. For example:</p> <p><i>See supra</i> evidence cited for claim element 1[e].</p>
80	80. The electrical junction of claim 77, wherein the electrical junction has a specific contact resistance of less than or equal to approximately $1\ \Omega\text{-}\mu\text{m}^2$ .	<p>Kim discloses an electrical junction wherein the electrical junction has a specific contact resistance of less than or equal to approximately <math>1\ \Omega\text{-}\mu\text{m}^2</math>. For example:</p> <p><i>See supra</i> evidence cited for claim 3.</p>

