

Low Noise Capacitive Sensor for Multi-touch Mobile handset's applications

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Abstract—Capacitive touch screen sensor, though it enables multi-touch recognition, has problems rejecting distributed noise such as LCD, RF and EMI interferences coupled to transparent ITO electrodes. This paper presents a capacitive sensor design for multiple channels at the X-Y crossing of ITO patterns on the LCD panel. Capacitance-to-Voltage converter (C-VC) with moving average and time interleaved scheme is proposed to reject noises and achieve high data-rate. Calibration algorithm is used to compensate the delay of each channel due to series RC of ITO pattern. The measured signal-to-noise ratio of the sensor is 24dB at 65Hz scanning frequency for 320 channels. The prototype IC is implemented in a 0.18 CMOS technology, while consuming 13mW from 3.3V and 6mW from 1.8V supply.

I. INTRODUCTION

Over the past years, touch aware sensor has become the most prevalent UI technology in touch-based applications such as mobile handset, portable media player and laptop PC. To realize multi-touch recognition such as zoom in, zoom out and resizing, capacitive sensor based on conductive property of fingers has been widely used. A behavioral model of capacitive sensing is shown in Fig. 1. When a conductive object like a finger approaches to the separated X, Y ITO electrodes, fringing fields between two electrodes are directed to the finger, causing the decrease in capacitance. The exact touch point record can be achieved by detecting the largest capacitance change and then conducting interpolation scheme.

However, touch point detections are frequently contaminated with widely distributed noises such as RF, LCD and EMI interferences. This is mostly induced from fingers coupled to the ITO electrodes. To suppress these noises, several techniques such as Δ - Σ modulator or relaxation oscillator have been used for front-end circuits [1]. The difficulty with these approaches is inherent nonlinearity and their performance is also limited by quite low scanning frequency, which disables multi-touch recognition.

In this paper, a new effective interface is proposed for capacitive touch screen sensor. Multi capacitance-to-voltage converters (C-VC) are operated as time-interleaved scheme to enhance the data rate and reject noises. Moreover, the calibration technique is used to compensate for the aging and RC delay of ITO layers.

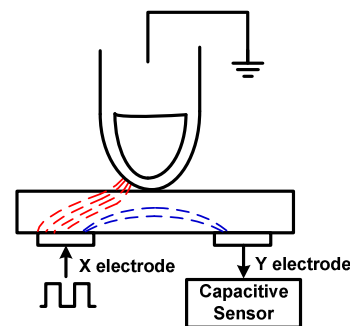


Fig.1 Behavioral model of capacitive sensing

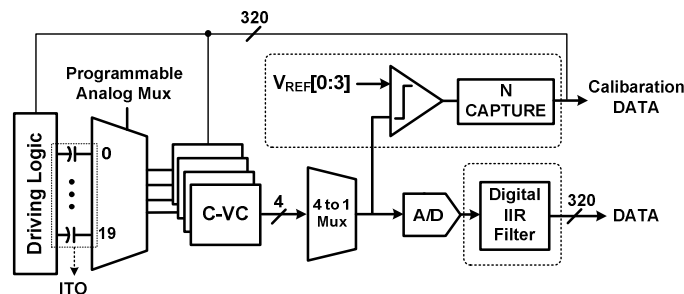


Fig.2 Proposed Time-interleaved architecture of capacitive touch screen sensor

II. PROPOSED ARCHITECTURE

A. Block Diagram

Fig. 2 shows the proposed time interleaved architecture of the sensor interface. It consists of four C-VCs, calibration comparators, programmable Mux and ITO driving logic. First, C-VCs convert the capacitance changes of ITO electrodes into the voltage levels. By conducting several conversion stages for each channel, C-VCs amplify the wanted DC voltage level and reject the interferences coupled to the ITO. The resulting signal level is converted by the SAR-ADC and filtered once again by IIR filter in DSP. Depending on the touch panel size, the number of channels and operating C-VC

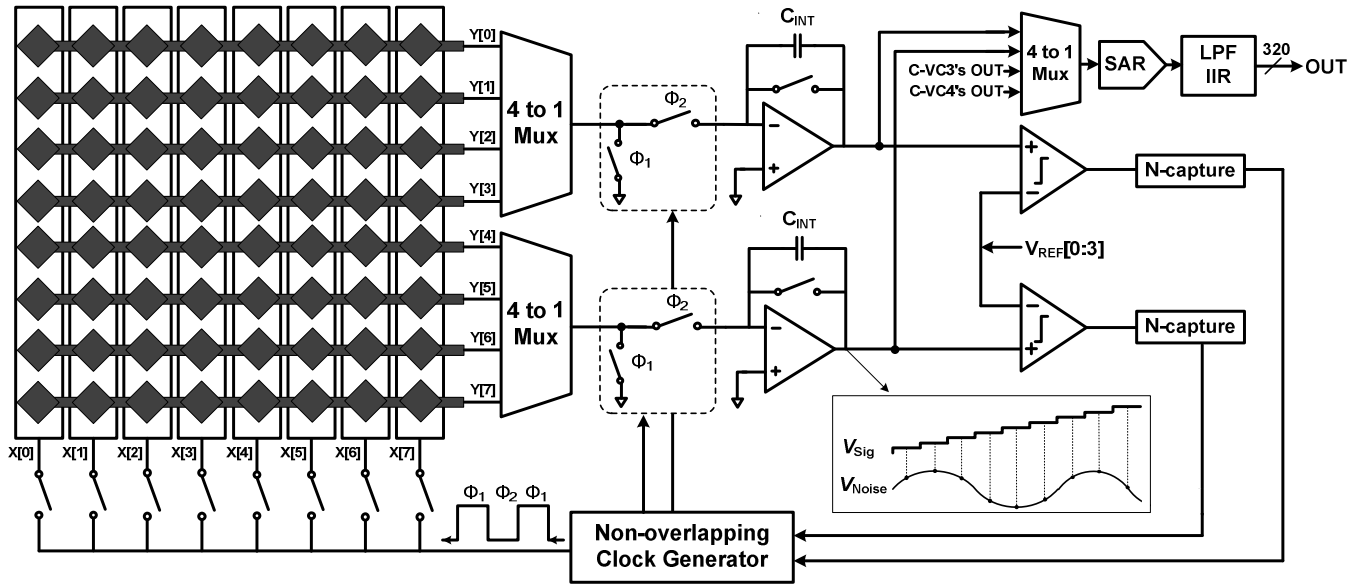


Fig. 3 Time interleaved architecture of the capacitance-to-voltage converters (C-VCs) with calibration technique. All blocks except ITO layers and C_{INT} are implemented on chip.

blocks can be controlled by programmable Mux. The outputs of C-VCs are also connected to the calibration comparators, and compared with controllable V_{ref} to decide the number of conversion times of C-VCs for each channel.

B. Capacitance-to-Voltage Converter

Fig. 3 shows a schematic diagram of the interface and ITO layers. For clarity only half of the fully architecture is shown. The ITO layers consist of two layers: the upper Y layer which is connected to the interface for sensing and the lower X layer for driving. X electrodes [7:0] are sequentially driven by non-overlapping clock generator and switches. To prevent LCD noise emission under driving X layer, X electrodes which are not driven are kept to virtual ground. When Φ_1 turns on, the input DC voltage is integrated to the capacitor configured between X and Y layers. At next Φ_2 clock, the charge on this capacitor is discharged to C_{INT} , generating the signal proportional to the capacitance change.

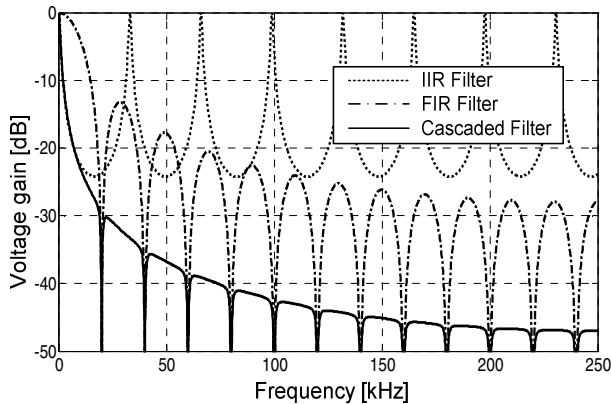


Fig. 4 Cascaded Filter response

With repetition of this conversion stage, DC voltage level increases with stair case waveform and noises coupled to the ITO layers are moving-average filtered [2-3]. The voltage transfer function from the input to the C-VC output is given by

$$H(z) = \left(\frac{1}{C_{INT}} \sum_{i=1}^N z^{-i} \right) C_{ITO} \quad (1)$$

Where $z = e^{j2\pi f/fs}$ and fs is conversion frequency. This defines a FIR low pass with null at fs/N and its multiples. Due to the discrete-time characteristic of C-VCs, interference around $f=fs$, $2fs$, $3fs$, will alias to the DC but also be attenuated by low pass IIR filter in DSP. Fig. 4 shows the cascaded filter response. It achieves 37dB rejection ratio at 50kHz with 25-conversion stages and 1:4 ratio of IIR filter.

Fig. 5 shows time interleaved sequences of C-VC blocks. To reduce the power consumption, only four C-VCs cover the entire Y electrodes [15:0] and C-VC blocks are connected to one ADC through 4-to-1 Mux. C-VC acts as the S/H circuit by itself, requiring no additional S/H circuits for ADC.

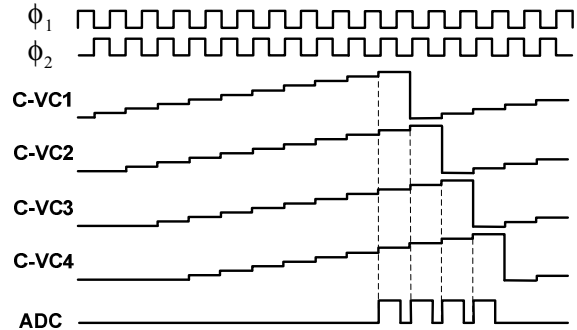


Fig. 5 Sequences of time-interleaved architecture and C-VCs' output waveforms.

By time interleaving the C-VCs, scanning frequency has increased which is 10% higher than parallel operation. Also S/H leakage error due to the standby of C-VC can be reduced. The class-AB op-amp is designed for C-VC circuit that uses fully input dynamic range of ADC [4]. Depending on the touch panel size or C_{INT} , the phase margin and slew rate of op-amp can be digitally controlled by changing the buffer's current driving capability.

C. Calibration circuit

At the channels far from the interface, ITO electrodes are highly resistive and have much parasitic capacitances to adjacent electrodes. This makes fully charge transfer to C_{INT} impossible, causing detection errors. Fig. 6 shows this detection error. For the channel at the crossing of $x[0]$ electrode and $y[0]$ electrode which is farthest from the interface, maximum detection error occurs. This detection error will be worsened as touch panel size increases. The C-VCs output formula considering ITO's series resistors and parasitic capacitors can be approximated by

$$V_{OUT,C-VC} = \left[\frac{V_{DC}}{C_{INT}} (1 - e^{-t/\tau}) \right] C_{ITO,NM} \quad (2)$$

Where $\tau = 1/(NR_x + MR_y)C_{ITO,NM}$ and N is the X-driving electrode number and M is the Y-sensing electrode number respectively. Fig. 3 shows the calibration comparators. For all channels of X-Y crossing of ITO electrodes, voltage levels are balanced by changing the number of conversion times and detected by comparator which has negative input connected to reference voltage. Then this number applies to the driving switch and C-VC blocks as soon as sensing procedure is initiated.

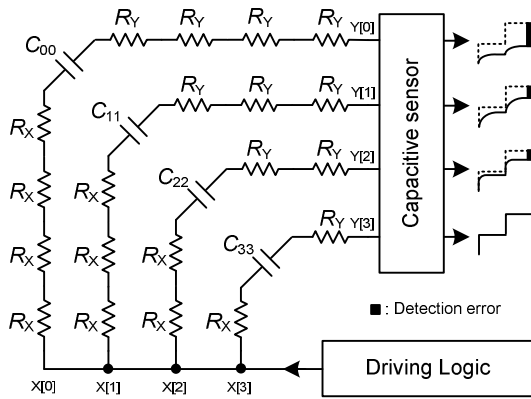


Fig. 6 Equivalent RC lumped model of ITO layers

D. Non-overlapping clock generator

Fig.7 shows the non-overlapping clock generator. For correct operation of C-VCs and driving switch logic, non-overlapping

clock must be generated. By delaying the falling time of the inverter and cascading the inverter arrays at next stage, the duty has been controlled. 1.8V to 3.3V level shifters are integrated to operate 3.3V analog circuits. Non-overlapping time must be minimized to prevent floating internal node which is exposed to external interferences.

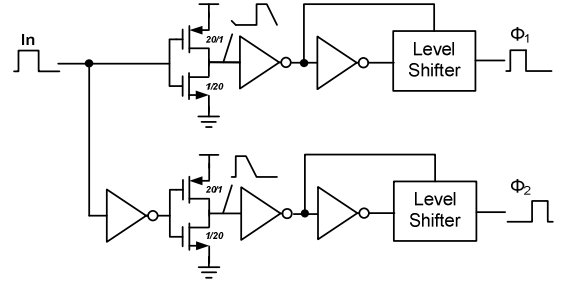


Fig. 7 Non-overlapping clock generator

III. MEASUREMENT RESULTS

The capacitive sensor is fabricated in a standard 0.18-um CMOS process. A measurement board is shown in Fig. 8. The total chip size occupies $2 \times 2 \text{ mm}^2$ and measurement was made using 7 inches ITO layers with 320 channels (20 by 16). The static performance is characterized through signal-to-noise ratio (SNR) and scanning frequency. The SNR of the touch screen sensor is defined as [5]:

$$\text{SNR(dB)} = 20 \log \frac{\text{STouch}}{\text{NTouch}_{\text{RMS100}}} \quad (3)$$

$$\text{STouch} = \text{Signal}_{\text{Touch,AVG100}} - \text{Signal}_{\text{Untouch,AVG100}} \quad (4)$$

$$\text{NTouch}_{\text{RMS100}} = \sqrt{\frac{\sum_{n=0}^{n=99} (\text{Signal}[n] - \text{Signal}_{\text{Touch}})^2}{100}} \quad (5)$$

Where AVG100 means the simple numeric average of 100 data points and RMS 100 means the root-mean-square of 100 data points, using $\text{Signal}_{\text{Touch}}$ as a baseline. The measured SNR versus number of conversion stages is shown in Fig. 9. As the number of conversion times or filter coefficients increases twice, SNR increases about 6dB. Fig. 10 shows the measured scanning frequency for 320 channels. 65 data points for coordinate detection are updated every one second (65Hz) with 200 kHz clock frequency and 22-filter coefficients.

Fig. 11 shows the measured calibration data from 10-bit ADC. Before calibration the maximum variation of ADC output is about 300. After calibration, the variation is within 50 levels which is less than 5% of ADC's full range.

Table 1 summarizes the measured parameters. This shows the possibility of this architecture for a practical touch based applications.



Fig. 8 Measurement board of sensor chip and ITO layer

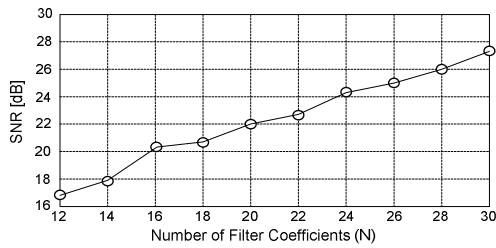


Fig. 9 Measured signal-to-noise ratio versus number of filter coefficients

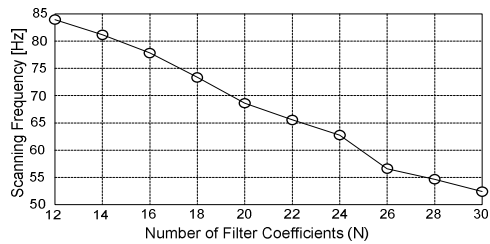


Fig. 10 Measured scanning frequency versus number of filter coefficients

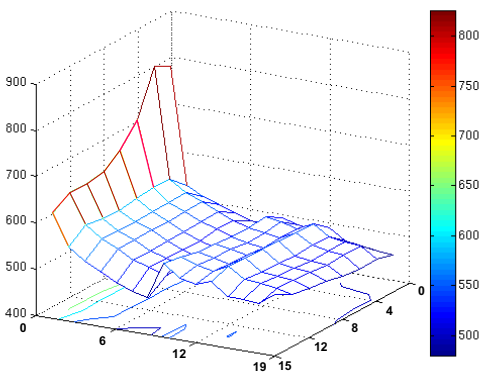


Fig. 11(a) Raw data points for 20(x) by 16(y) ITO layers'

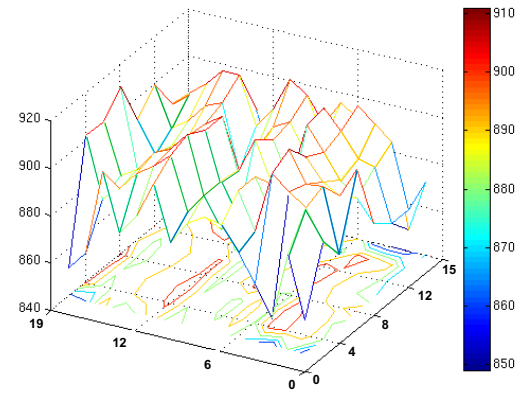


Fig. 11(b) Calibration data points for 20(x) by 16(y) ITO layers'

TABLE I. PERFORMANCE SUMMARY

SNR	24dB
Scan Frequency	65Hz
Technology	180nm CMOS
Channel	320 channels (X:20, Y:16)
Power consumption	Analog :13mW, Digital : 6mW
Active Die Area	4mm²

IV. CONCLUSIONS

This paper demonstrates an effective filtering technique that can attenuate noises induced to the ITO layers with 37dB rejection at 50kHz frequency. Time-interleaved architecture of C-VCs extremely enhances the data rate up to 65Hz scanning frequency, which enables multi-touch recognition. Compatibility with all commercial ITO products is achieved through the calibration technique. Its simplicity and practicality with low power consumption make it suited for touch screen sensor systems which must operate in harsh environment.

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