

**UNITED STATES PATENT AND TRADEMARK OFFICE**  
**BEFORE THE PATENT TRIAL AND APPEAL BOARD**

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**QUALCOMM INCORPORATED**  
**PETITIONER**

**v.**

**MONTEREY RESEARCH LLC**  
**PATENT OWNER**

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***INTER PARTES* REVIEW NO. IPR2021-00121**  
**PATENT 7,977,797**

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**PETITION FOR *INTER PARTES* REVIEW UNDER 35 U.S.C. § 312**

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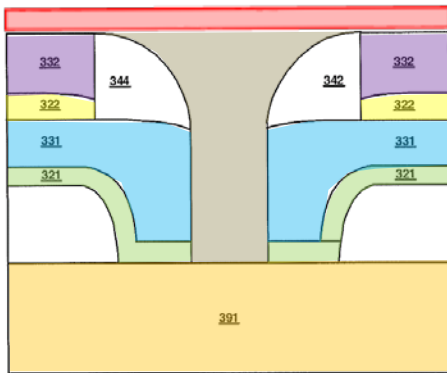
**PETITIONER’S EXHIBIT LIST**

<b>Exhibit</b>	<b>Shorthand</b>	<b>Description</b>
1001	‘797 Patent	U.S. Patent No. 7,977,797
1002	Lee Decl.	Declaration of Dr. Jack Lee
1003	Peng	U.S. Patent No. 7,338,903
1004	Lin	U.S. Patent Publication No. 2004/0124420
1005	Brase	U.S. Patent No. 6,576,550
1006	Chien	U.S. Patent No. 6,365,504
1007	’797 FH	File Wrapper for U.S. Patent No. 7,977,797
1008	’727 FH	File Wrapper for U.S. Patent No. 7,752,727
1009	Chung	U.S. Patent Publication No. 2005/0003656
1010	Chooi	U.S. Patent Publication No. 2001/0055878
1011	Streetman	Streetman & Banerjee, Solid State Electronic Devices (5th ed.) (1999), Chapters 6 and 9
1012	Monterey Complaint	<i>Monterey Research, LLC v. Qualcomm Incorporated, et. al</i> , No. 19-cv-2083, D.I. 1 (D. Del. Nov. 1, 2019)
1013	Chien ’610	U.S. Patent App. No. 2002/0142610
1014	Fu	U.S. Patent No. 6,316,348
1015	Penner	PCT App. No. WO 01/24244
1016	Shields	U.S. Patent No. 6,441,418
1017	Chen	U.S. Patent No. 6,570,257
1018	Chu	U.S. Patent Publication No. 2004/0192058
1019	Bowman	Basic Integrated Circuit Technology Reference Manual (1993)
1020	Bjorkman	U.S. Patent No. 6,669,858
1021	’727 Patent	U.S. Patent No. 7,572,727
1022	Natori	Natori et al., “Thickness dependence of the effective dielectric constant in a thin film capacitor,” Applied Physics Letters Vol. 73(5), 632 (1998).

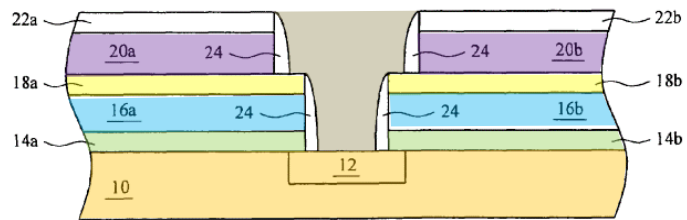
<b>Exhibit</b>	<b>Shorthand</b>	<b>Description</b>
1023		OMITTED
1024		OMITTED
1025	Hall-Ells Decl.	Declaration of Dr. Sylvia Hall-Ellis
1026	Bowman2	Cost Effective IC Manufacturing (1998-1999)
1027	Donovan	“Contamination-Free Manufacturing for Semiconductors and Other Precision Products,” Robert P. Donovan, ed. (2001)

## I. INTRODUCTION

The '797 Patent uses a “multiple etch stop insulation layer” having a particular [green/blue/yellow/purple] arrangement of layers and a [tan] contact region shaped such that “a larger portion of the multiple etch stop insulation layer is removed close to the [red] metal layer and a smaller portion is removed closer to the [orange] substrate.” EX1001, 2:48-56. Peng discloses the claimed layers and contact shape.

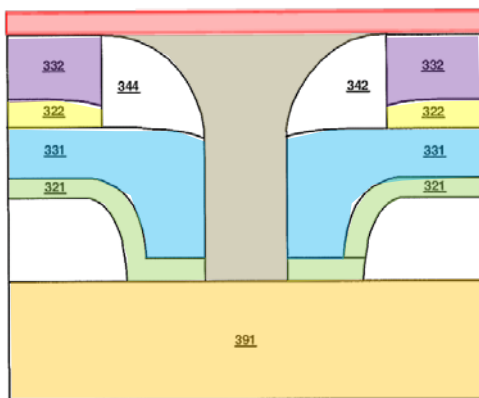


EX1001 ('797 Pat.), FIG. 3E<sup>1</sup>

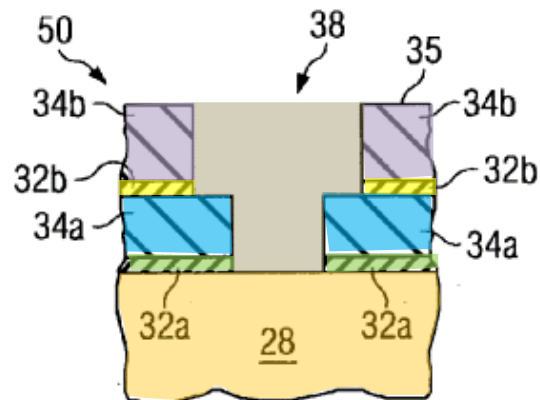


EX1003 (Peng), FIG. 2

Lin also discloses the claimed layers and contact shape.



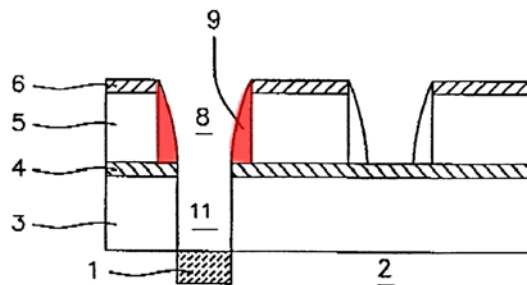
EX1001 ('797 Pat.), FIG. 3E



EX1004 (Lin), FIG. 12

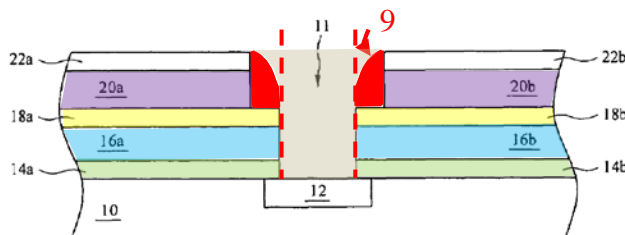
<sup>1</sup> All colorized figures annotated.

The '797 Patent also uses spacers to “control” the “substrate coupling area width” at the bottom of the contact area. EX1001, 4:39-45. But the use of spacers as an etch mask to define a relatively smaller bottom for a contact region was also known. As shown in FIG. 2f below, Chien discloses using “spacers 9 as an etching mask” to define a smaller bottom contact opening in dual damascene processes—in which a smaller contact opening is defined beneath a larger trench, as in Peng and Lin. EX1006, 4:56-5:2 (explaining use of spacers as a mask “solve[s] problems of misalignment ... and aid[s] the process control”).

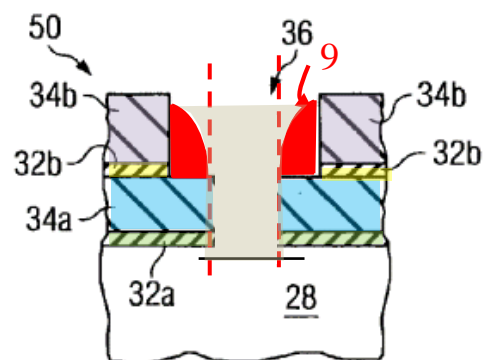


**EX1006 (Chien), FIG. 2f**

It was obvious to use Chien’s [red] spacers in Peng’s and Lin’s similar dual damascene designs, and doing so meets every limitation of the challenged claims.



**EX1003 (Peng), FIG. 2  
(modified per Chien)**



**EX1004 (Lin), FIG. 10  
(modified per Chien)**

## II. MANDATORY NOTICES

### A. Real Party in Interest (37 C.F.R. § 42.8(b)(1))

The real parties-in-interest are Qualcomm Incorporated (NASDAQ: QCOM), Qualcomm Technologies, Inc., and Qualcomm CDMA Technologies Asia-Pacific Pte Ltd.

### B. Related Matters (37 C.F.R. § 42.8(b)(2))

(1) *Monterey Research, LLC v. Qualcomm Inc., et al*, Civil Action No. 1-19-cv-02083 (Del. 2019), which involves the '797 Patent.

### C. Lead and Back-Up Counsel (37 C.F.R. § 42.8(b)(3))

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Petitioner consents to electronic service.



### III. GROUNDS FOR STANDING

Pursuant to 37 C.F.R. § 42.104(a), Petitioner certifies that the '797 Patent is available for *inter partes* review, and that Petitioner is not barred or estopped from requesting an *inter partes* review on the grounds identified in this Petition.

### IV. STATEMENT OF PRECISE RELIEF REQUESTED FOR EACH CLAIM CHALLENGED

#### A. Claims for Which Review Is Requested (§42.104(b)(1))

Petitioner requests review and cancellation of Claims 1-12 and 14-15 based on the following Grounds.

#### B. Statutory Grounds of Challenge (§42.104(b)(2))<sup>2</sup>

All claims are invalid under §103(a) over these combinations of prior art:

Ground	Claims	Prior Art Combination
1	1-8	Peng (EX1003), Brase (EX1005)
2	1-8, 11-12	Peng, Brase, Chien (EX1006)
3	1-7, 11	Lin (EX1004), Chien
4	10	Peng, Brase, Chen (EX1017)
5	10, 14	Peng, Brase, Chien, Chen
6	10, 14	Lin, Chien, Chen

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<sup>2</sup> All Grounds are supported by a POSITA's general knowledge. *Koninklijke Philips N.V. v. Google LLC*, 948 F.3d 1330, 1337-38 (Fed. Cir. 2020).

Filed August 2, 2004 and entitled to priority of its April 24, 2004 provisional (EX1002, ¶74), Peng is prior art under §102(e).

Issued June 10, 2003, Brase is prior art under §102(b).

Issued April 2, 2002, Chien is prior art under §102(b).

Filed December 31, 2002, Lin is prior art under §102(a) and (e) as of its July 1, 2004 publication.

Issued May 27, 2003, Chen is prior art under §102(b).

## **V. THE GROUNDS IN THIS PETITION ARE NOT CUMULATIVE**

The proposed Grounds are not cumulative over the prosecution history of the '797 Patent or its parent, U.S. Patent No. 7,572,727 (the '727 Patent, EX1021).

First, none of Peng, Lin, Brase, or Chen were before the Examiner. *See generally* EX1001, cover; EX1008; EX1007.

Second, Chien was considered, but is applied here: (1) differently than the Examiner applied it, but (2) in a way that is consistent with the Examiner's unchallenged statements of Chien's disclosure. Specifically, during prosecution of the parent '727 Patent, the Examiner rejected Claim 15 as anticipated by Chien, as disclosing both: (1) a series of etch stop and dielectric layers, and (2) "nitride spacers (9) ... used as an etching mask to etch a via hole (11)." EX1008, 187/269. Applicants did not dispute the Chien disclosed the latter. *Id.*, 173-174/269. Instead, Applicants amended the claim to add details regarding the arrangement of etch stop

and dielectric layers, and argued that Chien did not disclose those added limitations.

*Id.* The Examiner withdrew the rejection on that basis, but never withdrew his assertions regarding Chien's spacers. *Id.*, 156-160/269.

This Petition does not rely on Chien for any element that Applicants asserted was missing from Chien. Rather, the proposed grounds rely on Peng and Lin as disclosing the claimed layer structure, and apply Chien's spacers as a known and desirable way to form the smaller bottom via. In Grounds 2-3, a POSITA would have *started* with Peng or Lin and adopted Chien's undisputed dual damascene formation disclosure, including using spacers to define a via hole for the explicit benefits Chien discloses. These grounds are unlike any invalidity theory asserted in prosecution.

To the extent PO may argue that the Examiner chose not to assert a rejection using Chien in this way, the Examiner erred because, as discussed below, the grounds present a straightforward modification based on explicit motivation.

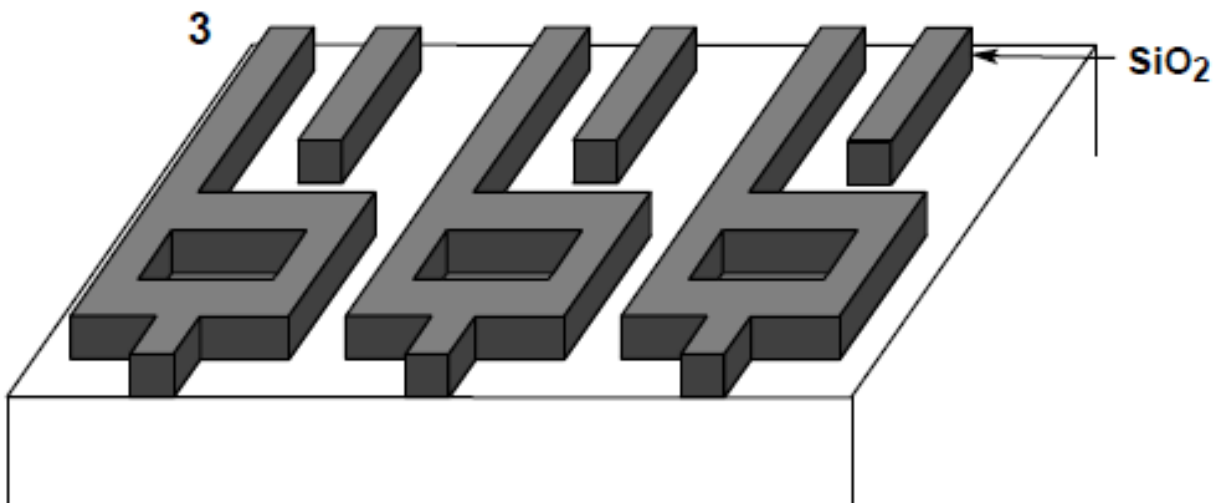
## VI. FIELD OF TECHNOLOGY

### A. Integrated Circuits and Transistor Fabrication

As of the ECPD, known integrated circuits included millions of transistors and other active devices formed in rows on and above a substrate along with vertical and horizontal conductive structures to connect the active devices. EX1002, ¶19.

At a high level, fabrication of integrated circuits alternately repeats (a) depositing a layer of material; and (b) etching away portions of the deposited layer—both to shape the deposited materials and to form voids for subsequent deposition of additional materials. *Id.*, ¶19.

An example of a [dark gray] layer etched to form structures is shown below.

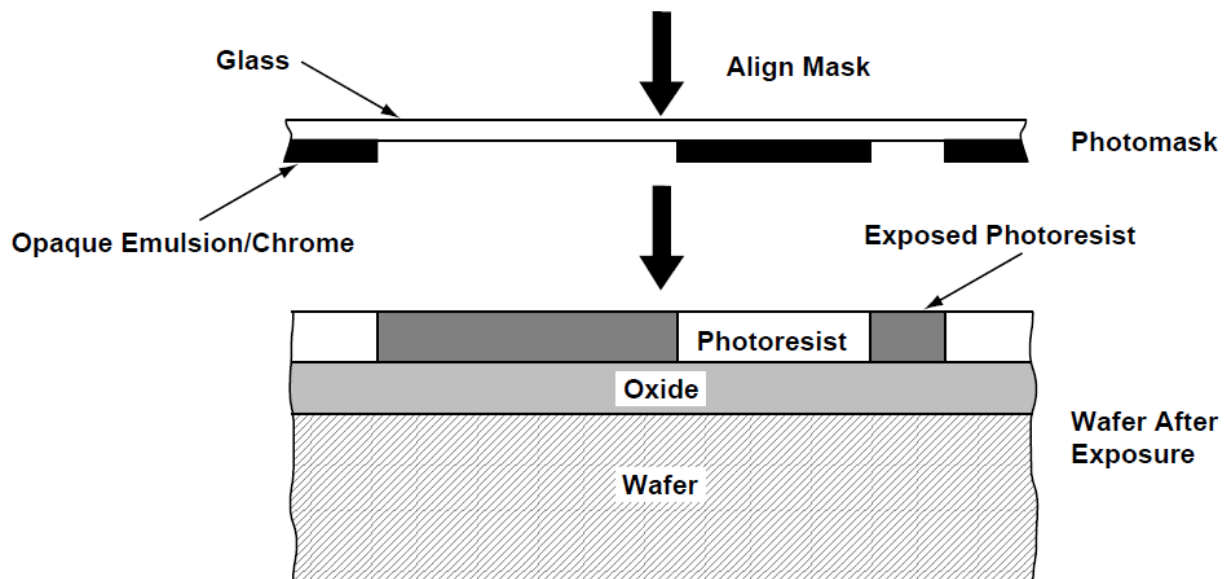


EX1019, 18/112.

## B. Etching Techniques

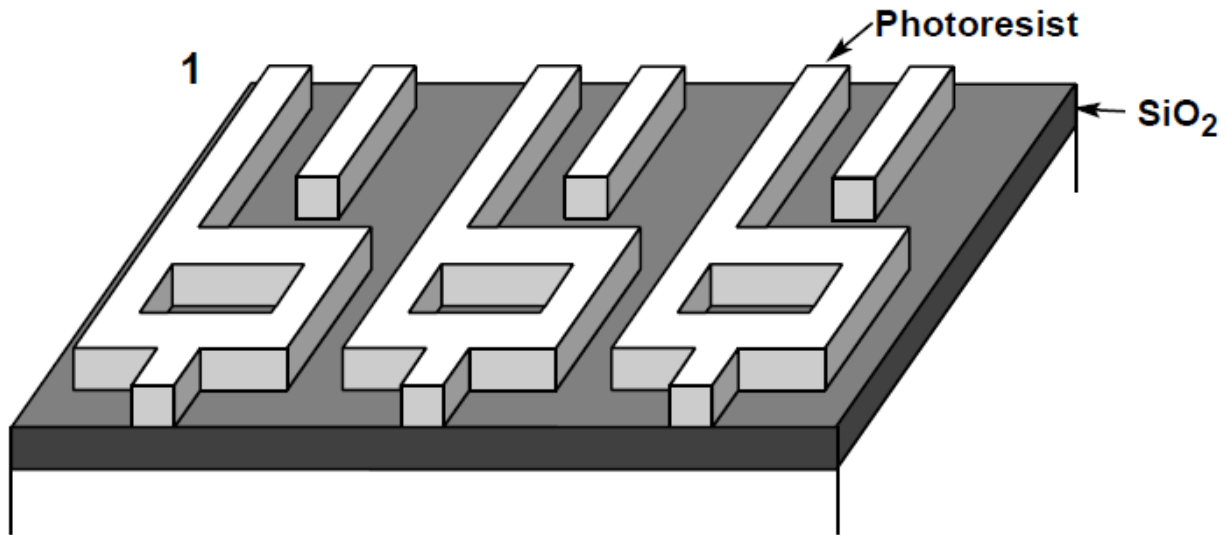
**Photolithography.** In photolithography, a common method used to etch layers in semiconductors (e.g., integrated circuits), a photoresist layer is deposited on another layer (e.g., oxide) that is to be etched; and the photoresist layer is then selectively exposed to light by shining the light through a patterned “mask” as shown below. EX1002, ¶21. Some parts of the mask transmit light while others block light.

*Id.*



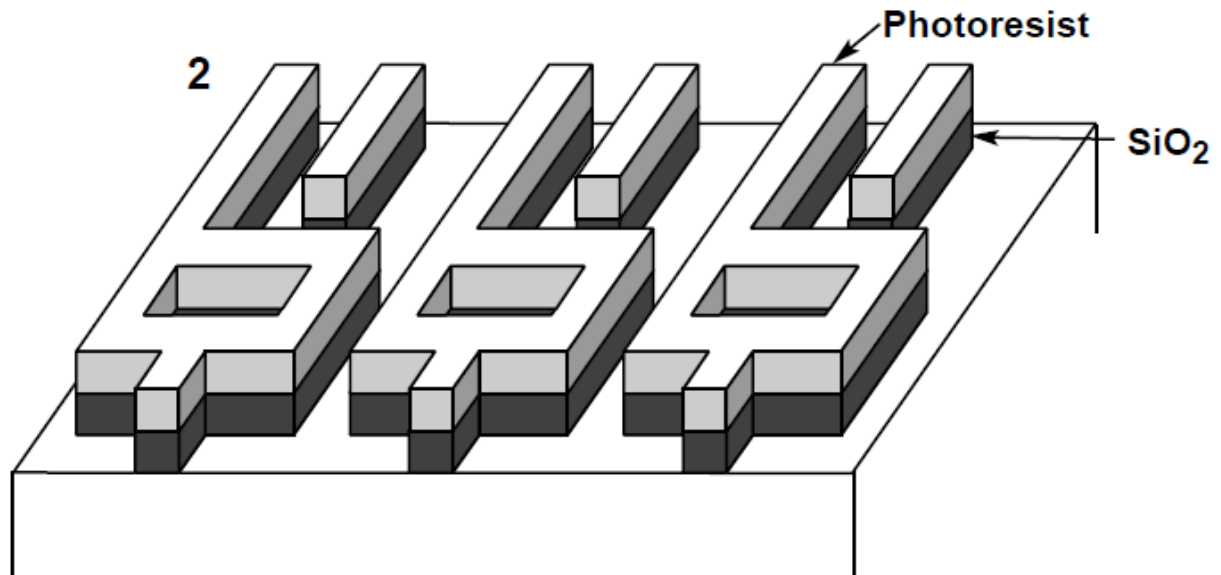
EX1019, 17/112.

The portions of the photoresist layer exposed to light are chemically modified to be removable, while the remaining portions of the photoresist layer retain their integrity (or vice versa). EX1002, ¶22. Removing the removable parts of the photoresist layer thus results in patterns like those shown below. *Id.*



EX1019, 18/112 (annotations in original). The remaining parts of the photoresist layer form a patterned protective barrier over the layer to be etched, here the  $\text{SiO}_2$  layer. EX1002, ¶23.

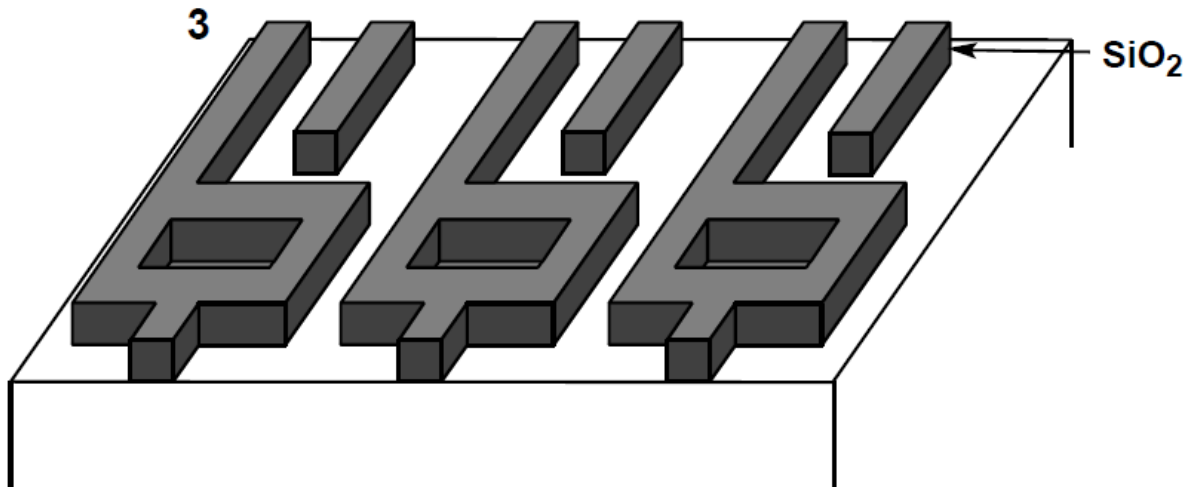
An etchant, chosen to be effective in etching  $\text{SiO}_2$ , is then applied, with the photoresist layer protecting portions of the layer such that unprotected parts are removed to leave the desired pattern. *Id.*



EX1019, 18/112 (annotations in original).

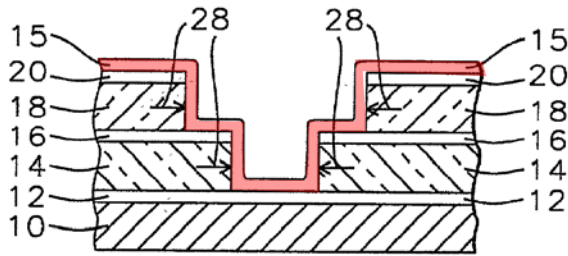
The remaining photoresist is then removed, leaving the etched layer(s).

EX1002, ¶24.

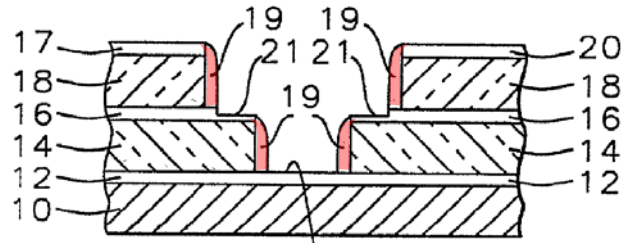


EX1019, 18/112 (annotations in original).

**Anisotropic Etching.** As shown below, it was well known to form vertical spacers *without* photolithography. EX1002, ¶¶32, 34-35. Chooi FIGs. 5 and 6 illustrate forming spacers from a [red] “layer (15) conformally lin[ing] all exposed surfaces of the trench and via formation” using “an anisotropic etch,” (which targets material in one direction over another), to remove the horizontal portions of the conformal coating without photolithography [and] thereby“ form[ing] a [red] spacer layer (19) from” layer 15. EX1010, ¶¶48-49.



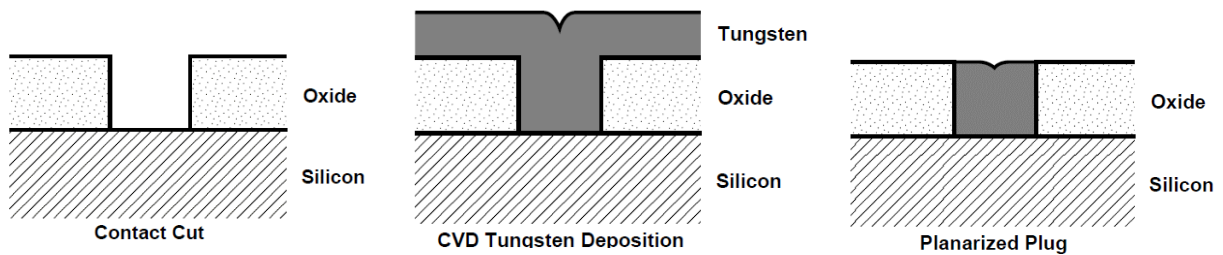
EX1010, FIG. 5



EX1010, FIG. 6

### C. Contact Holes and Dual Damascene Structures

As noted above, it was well-known to use etching to form voids for subsequent deposition of materials. EX1002, ¶36. One such void or space was known as a contact hole or “via.” *Id.* Contact holes or vias were formed through one or more insulating layers, and subsequently filled with conductive material to define a “plug” that extends vertically to interconnect conductive structures above and below the plug. *Id.* Below, the three cross-sections (from left to right) illustrate etching a via, filling the via with conductive material, and removing excess conductive material to form a plug.

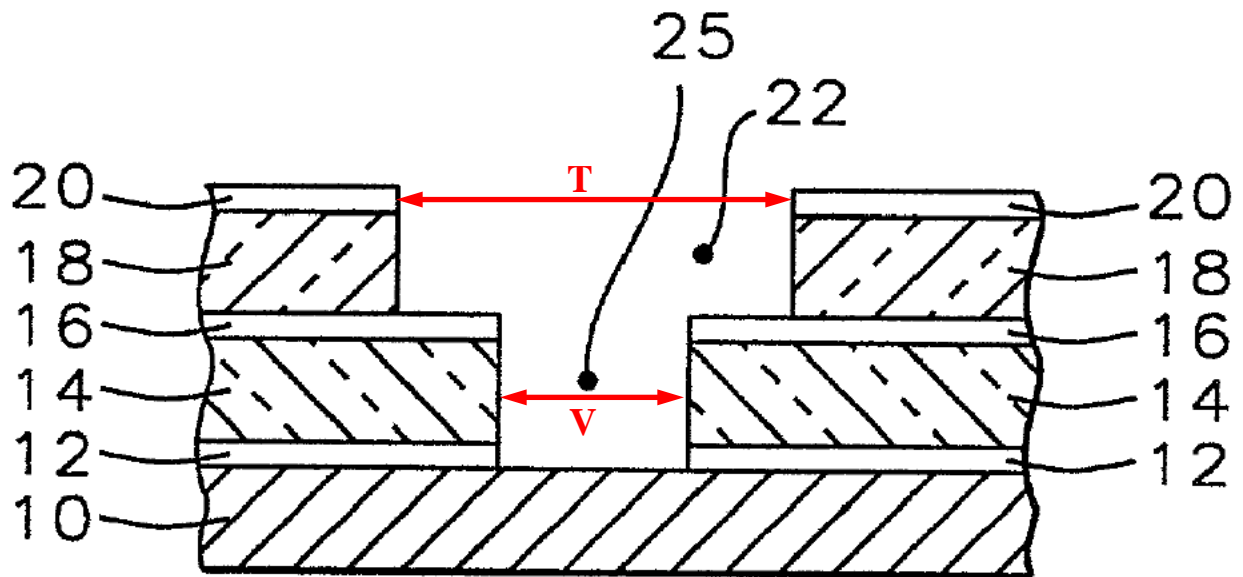


EX1019, 75/112; EX1002, ¶36. Once the plug is formed, a conductive layer can be deposited on the oxide layer, with the conductive layer in contact with the plug, and then patterned to form horizontal interconnects. EX1002, ¶36.



Rather than forming an opening only for a contact plug, and then depositing a conductive layer for horizontal interconnects on top of an insulating (*e.g.*, oxide) layer, it was also well known to form a “dual damascene” structure that included a single void (in the insulating layer) having **both** (a) a vertical via/contact hole and (b) trenches for horizontal interconnects. *Id.*, ¶37.

An exemplary dual damascene structure having a “trench (22) and via (25)” is shown below. *Id.* In this configuration, the trench 22 is elongated with a width “T” in the plane of the page, and a length that extends into the page; whereas the via 25 is a vertical passage with width “V” in the plane of the page.

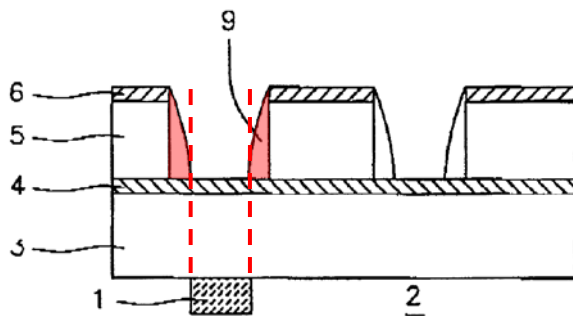


EX1010, FIG. 4 (annotated), ¶[0047].

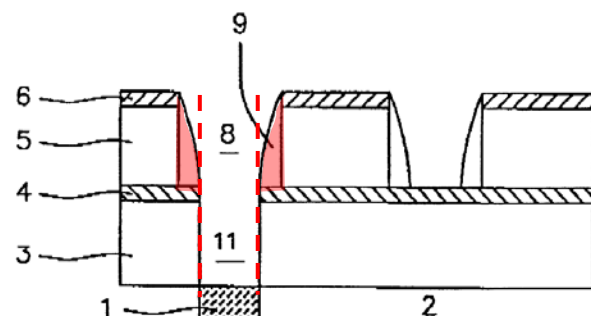
There were multiple known ways to form dual damascene structures, utilizing various combinations of etch stop layers, dielectric layers, and conventional

photolithography. EX1010, ¶[0047] (listing “several methods known in the art”); EX1002, ¶38.

For example, it was known to define the area in which to etch the lower “via” of a dual damascene opening using spacers (created using deposition of a conformal layer and anisotropic etching as discussed above). EX1002, ¶40 (citing EX1006, 4:25-5:2). For example, Chien discloses using [red] spacers 9 “as an etching mask” to form “via hole 11.” *Id.*



**EX1006, FIG. 2d**



**EX1006, FIG. 2f**

As shown above:

- first, the trench (8) is etched in the top layer (5);
- next, [red] spacers (9) are added in the trench (8) to define the smaller area in which to etch the via; and
- last, via (11) is etched.

This use of spacers was known to “solve problems of misalignment in forming small via holes” that occur when attempting to perfectly align separate photomasks for trench and via openings, and such spacers thereby “aid the process control.” EX1002, ¶41 (citing EX1006, 4:66-5:2).

Dual damascene was used for interconnections at all levels of a device, both upward from transistors in the substrate and between layers of interconnects as shown, for example, in Brase.

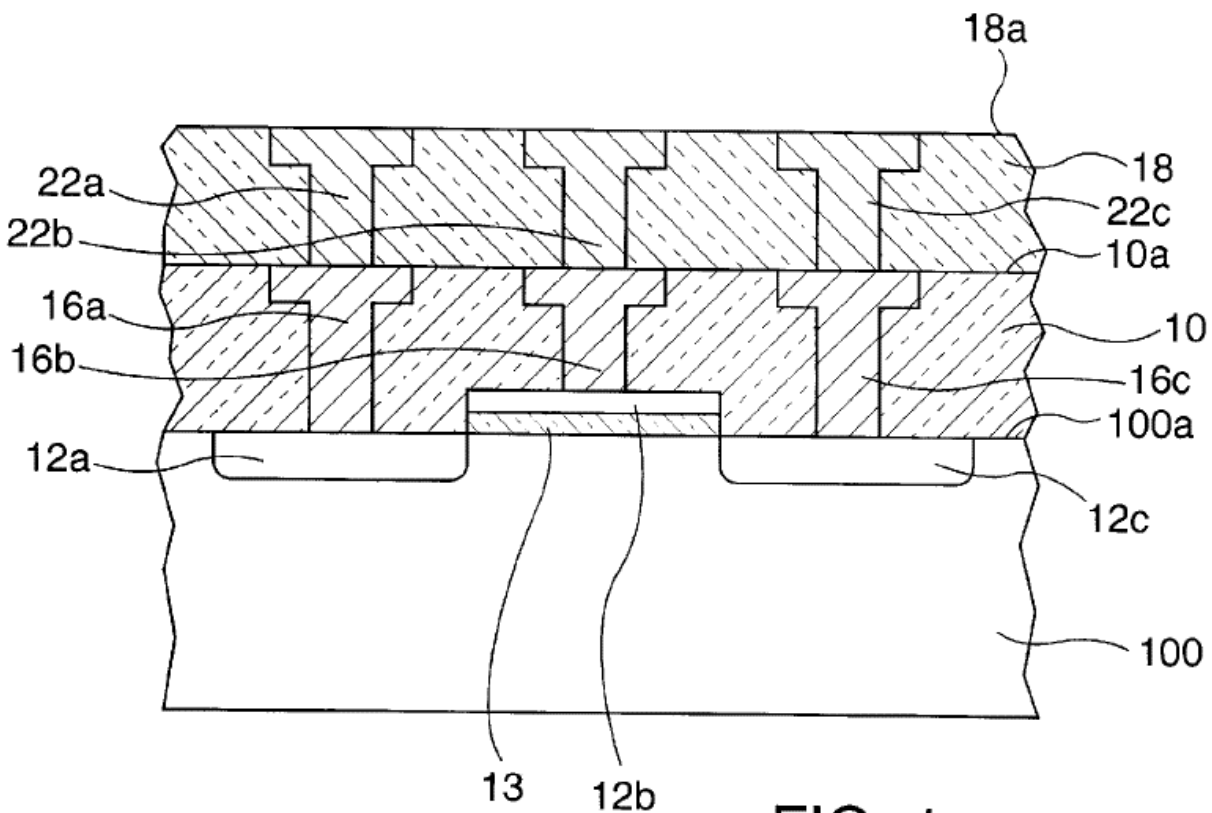
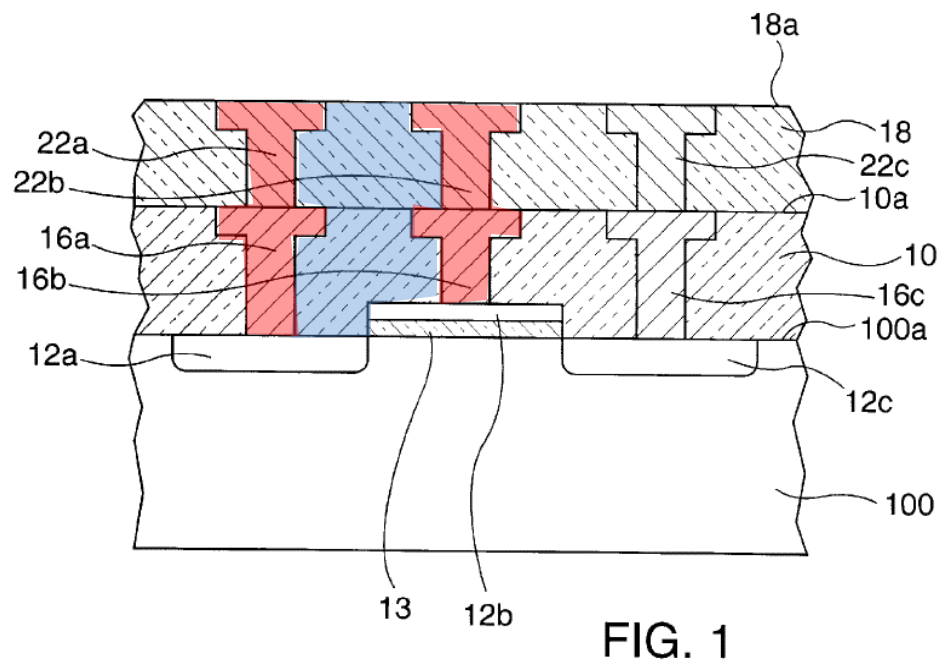


FIG. 1

EX1005, FIG. 1.

Each of the contact holes is formed in dielectric materials that insulate one contact from another contact and isolate electrical current to the conductive material in the plugs. Referring to Brase's FIG. 1 again, [blue] dielectric material between contacts 16a and 16b insulates [red] contacts 16a and 16b by preventing electrical current flow from contact 16a to 16b through the layers 10 and 18. EX1002, ¶¶39, 42 (citing EX1019, 74/112).



EX1005, FIG. 1.

## VII. LEVEL OF ORDINARY SKILL IN THE ART

A POSITA as of the '797 Patent's ECPD of September 2, 2004,<sup>3</sup> would have had at least a master's degree in electrical engineering, materials science, physics, or a related degree, and at least 3-5 years of experience in semiconductor devices and fabrication technologies. EX1002, ¶49. Additional experience may substitute for an advanced degree, for example, a bachelor's degree with at least 5-6 years of experience. *Id.* The prior art and the '797 Patent also evidence this level of ordinary skill. *See Chore-Time Equip., Inc. v. Cumberland Corp.*, 713 F.2d 774, 779 (Fed. Cir. 1983); *Okajima v. Bourdeau*, 261 F.3d 1350, 1355 (Fed. Cir. 2001).

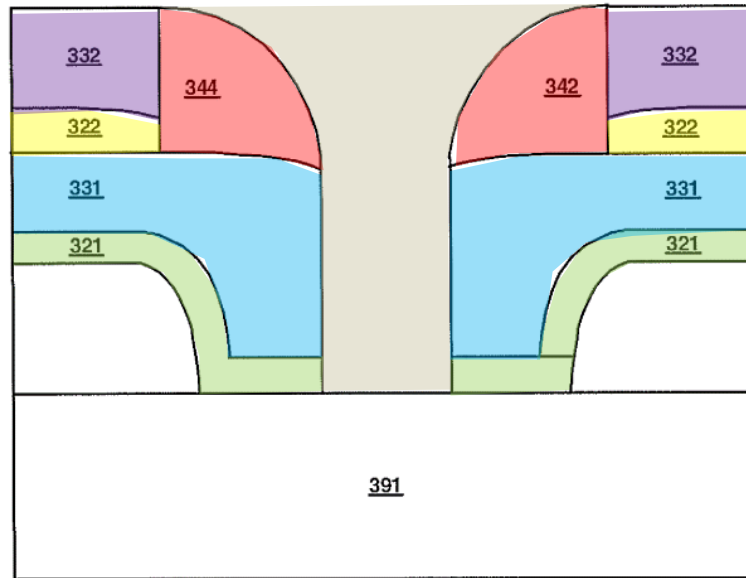
## VIII. OVERVIEW OF THE '797 PATENT

### A. '797 Patent Disclosure

The '797 Patent discloses structures and processes for forming a “contact region” extending from a substrate in an integrated circuit. EX1001, Abstract. This [tan] contact region is formed within a “multiple etch stop insulation layer” having [green] etch stop layer 321, [blue] sub interlevel dielectric layer 331, [yellow] etch stop layer 322, [purple] sub interlevel dielectric layer 332. EX1001, FIG. 3E, 4:50-5:51. The '797 Patent also discloses [red] sub spacer regions 342 and 344.

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<sup>3</sup> All statements in this Petition about the knowledge and skills of, and what would have been obvious to, a POSITA are offered from this perspective as of this date.



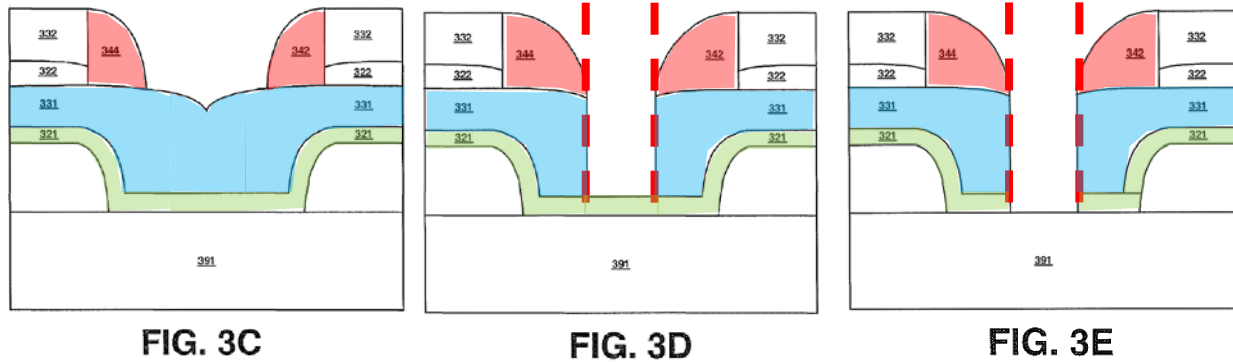
*Id.*, FIG. 3E. The '797 Patent asserts this design “facilitate[s] formation of contacts” that have “relatively small substrate connections.” *Id.*, 2:39-44. In particular, “a larger portion of the multiple etch stop insulation layer is removed close to the metal layer and a smaller portion is removed closer to the substrate.” *Id.*, 2:51-56.

The '797 Patent states that “the substrate coupling area width can be controlled by spacer width 142 and 144.” *Id.*, 4:42-44<sup>4</sup>; *see also id.*, 5:21-27. To achieve a contact bottom, [blue] “sub interlevel dielectric layer 331 is etched” as shown in FIG. 3D, and [green] “etch stop layer 321 is removed” as shown in FIG. 3E. *Id.*, 5:40-47. As can be seen in the annotations of FIGs. 3C-3E below, the etched portions are consistent with use of [red] sub spacer regions 342 and 344 as an etching

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<sup>4</sup> All emphasis added unless otherwise indicated.

mask—*i.e.*, [red] sub spacer regions define the area that is etched to form the via in [blue] layer 331.



*Id.*, FIGs. 3C-3E.

## B. Prosecution History

The '797 Patent is a divisional of U.S. Patent No. 7,572,727 (the '727 Patent, EX1019), and the challenged claims recite integrated circuits with features that closely track those of the method claims in the parent '727 Patent. As such, the prosecution of the parent '727 Patent is relevant to the challenged claims.

### 1. Parent '727 Patent

After a restriction requirement, the elected ones of the original claims recited contact formation process steps of forming layers of a multiple etch stop region and, in dependent claims, either (a) “forming a sub spacer region such that a substrate coupling area of said contact region is smaller than a metal layer coupling area of said contact region” or (b) “a non-lithography spacer formation process to achieve a sub-100 micro-meter contact bottom dimension.” EX1008, 197-201/269.

In a first substantive action, the Examiner rejected certain claims as anticipated by Chien and others as obvious over Shields in view of U.S. Patent No. 5,912,188 (“Gardner”). EX1008, 185-191/269. In doing so, the Examiner identified each of Chien and Shields as disclosing spacers formed on sides of an opening and using those spacers as a mask for subsequently etching a via. EX1008, 187/269 (“Nitride spacers (9)...”), 188-189/269 (“Nitride spacers (20)...”).

In response, Applicants did not contest that Chien and Shields each discloses the claimed “sub spacer” elements defining a reduced coupling/etching area. Applicants instead amended the claims to add additional details of the arrangement and properties of the dielectric and etch stop layers. *Id.*, 165-179/269.

In response to the amendments, the Examiner withdrew some rejections, but maintained the obviousness rejection of all claims over Shields in view of Gardner. *Id.*, 156-160/269. The Examiner asserted that Shields disclosed that “[n]itride spacers (20) are formed on the sides of the second oxide layer (18),” and that the “contact hole (27) is narrower at the bottom ... than at the top ... due to the formation of the spacers.” *Id.*, 157/269.

Applicants introduced several additional rounds of amendments to add additional details of the arrangement and properties of the dielectric and etch stop layers, arguing that those new details distinguished Shields in view of Gardner. *Id.*,



144-151/269, 116-124/269, 76-85/269. In these subsequent rounds of amendments, Applicants never contested Shield's disclosure of the sub spacer formation elements.

After three rounds of submissions, the Examiner allowed two of the three independent claims. *Id.*, 53-58/269. The Examiner issued a new rejection of independent application Claim 15 as anticipated by Chung, but noted that dependent application claim 20 would be allowable if written in independent form. *Id.* In response, Applicants added amended application claim 15 to include application claim 20's limitation of "a non-lithography spacer formation process is also utilized to achieve a contact bottom," and the Examiner then allowed the remaining claims. *Id.*, 44/269, 33-35/269.

## **2. Challenged '797 Patent**

Applicants filed the application for the '797 Patent as a divisional that included apparatus claims roughly mirroring certain allowed method claims of the '727 Patent. EX1007, 111/137, 127-130/137. The Examiner rejected a number of claims as indefinite under Section 112, Second Paragraph, and rejected Claim 11 over Chung. *Id.*, 67-71/137. The Examiner distinguished claim 11 from its parallel (allowed) method claim in the parent '727 Patent by asserting that claim 11's language related to the spacer formation process "do not necessarily impart structural characteristics," and therefore did not need to be mapped. *Id.*, 67-71/137. Applicants responded by amending Claim 11 and arguing that the amendments made

the spacer recitations “a structural difference.” EX1007, 49-56/137. The Examiner accepted the argument and allowed the claims. *Id.*, 40-42/137.

Of note, despite identifying Chung as disclosing the recited arrangement of etch stop and dielectric layers, and identifying Shields and Chien as disclosing the recited use of spacers, the Examiner never asserted modifying Chung (or any other reference with the recited arrangement of etch stop and dielectric layers) to include Chien’s spacers. This Petition demonstrates why such a combination, never asserted by the Examiner, renders the claims obvious.

**C. Claim Construction (37 C.F.R. § 42.104(b)(3))**

Petitioner interprets the claims of the ’797 Patent according to the *Phillips* claim construction standard. 83 Fed. Reg. 51340, 51340-44 (Oct. 11, 2018); *Phillips v. AWH Corp.*, 415 F.3d 1303 (Fed. Cir. 2005).

**1. “etch stop layer”**

A POSITA at the ECPD would have understood that the ’797 Patent uses the term “etch stop layer” consistent with its ordinary meaning in semiconductor fabrication, to mean *a layer that has a significantly slower etching rate than a neighboring layer for at least one etchant*. EX1002, ¶¶64-65. That is, the etch stop layer has a higher etch selectivity than another layer targeted for etching. *Id.*, ¶¶64 (citing EX1015, 2/15 (“Etch selectivity is defined as the ratio of the etch rates between a first material that is to be etched with respect to a second material.”)).

Because the etchant etches the etch stop layer at a significantly lower rate than the neighboring layer, the etch stop layer substantially stops the etching process from continuing past the targeted layer. EX1002, ¶64. For example, a POSITA would have recognized that silicon nitride and silicon oxynitride were well known for use as etch stop layers. *Id.* (citing EX1013, ¶[0012] (“[T]he stop layer is silicon nitride and the dielectric to silicon nitride etch rate selectivity is at least 10”), ¶[0011] (“[T]he dielectric layer comprises a doped or undoped silicon dioxide ....”); EX1014, Abstract (“The present invention provides an anti-reflective Si-Rich Silicon oxynitride (SiON) etch barrier layer ....”), 2:15-16 (using a “special silicon oxide etch that has a high selectivity to Si-Rich SiON and SiN)).

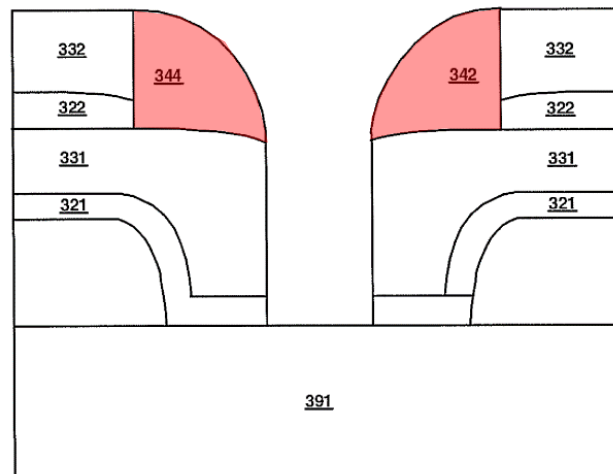
**2. “a non-lithography spacer formation process”**

A POSITA at the ECPD would have understood “a non-lithography spacer formation process,” recited in independent Claim 11, to mean *a process of forming spacers without a lithographically-formed photoresist layer*. EX1002, ¶66. For example, the ’797 Patent describes that:

In one exemplary implementation, the multiple etch stop insulation layers creates etching processes with ***non-lithographic*** spacer formation using multiple steps so that smaller contact holes (e.g., 0.06  $\mu\text{m}$  to 0.13  $\mu\text{m}$ ) can be created close to the substrate coupling area and larger contact top (e.g., 0.16  $\mu\text{m}$  to 0.18  $\mu\text{m}$ ) can be created closer to a metal layer coupling area.

EX1001, 5:21-27. In particular, “[i]n step 223 sub spacer regions 342 and 344 are formed,” and “FIG. 3C is an illustration of one embodiment of a wafer after a portion of etch stop layer 322 is removed in step 222 and sub spacer regions 342 and 344 are formed in step 223.” *Id.*, 5:36-40. The ’797 Patent does not offer any detail on *how* these spacers are formed—confirming that such spacers and their formation were already well-known to a POSITA. *See, e.g., id.*, 6:28-30. However, by way of example, the spacer formation process through deposition of a conformal layer and anisotropic etching described in Section VI.B above, is non-lithographic because it does not involve lithography. EX1002, ¶66.

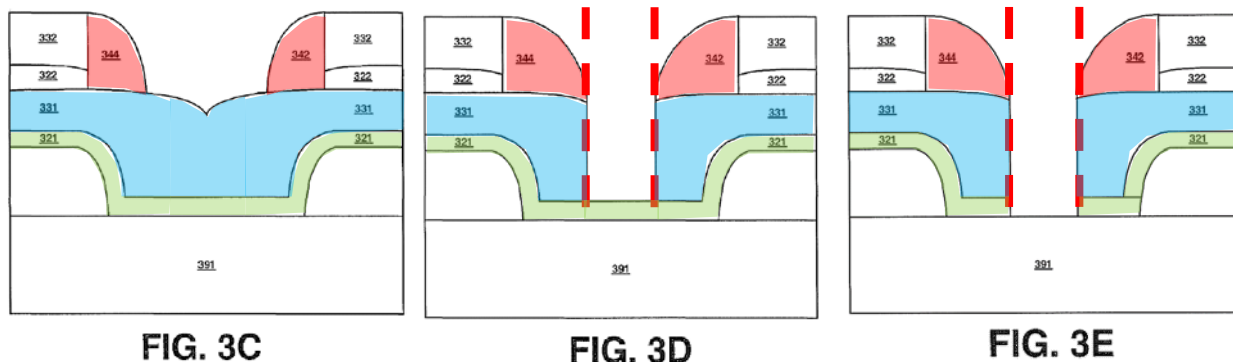
While the ’797 Patent does not include details of the actual formation process, spacers formed by anisotropic etching as described in §VI.B were known to have a curved top portion, consistent with [red] spacers 142 and 144 shown in FIG. 3E. EX1002, ¶66.



EX1001, FIG. 3E; *see also* EX1006, FIG. 2d-2f, 4:25-59 (“spacers 9”).

3. “a spacer region such that a substrate coupling area of said contact region is smaller than a metal layer coupling area of said contact region”

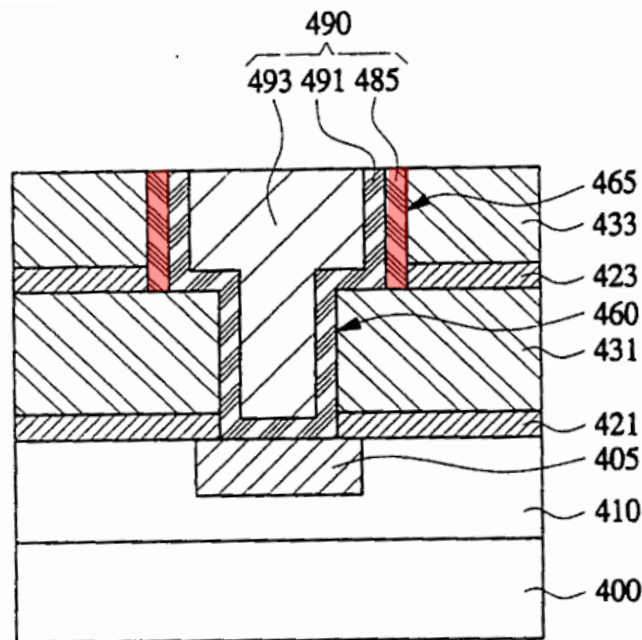
**Petitioner’s Construction:** A POSITA as of the ECPD would have understood that “a spacer region *such that* a substrate coupling area of said contact region is smaller than a metal layer coupling area of said contact region” means the “spacer region” *controls, at least in part*, the size of the a substrate coupling area of said contact region to be smaller than a metal layer coupling area of said contact region. EX1002, 68. This construction is consistent with the ’797 Patent’s preferred embodiment, in which “the substrate coupling area width can be controlled by spacer width 142 and 144.” EX1001, 4:42-44, FIG. 1B; EX1002, ¶68. As shown in FIGs. 3C-3E, the location of the [red dotted line] edges of [red] spacers 342 and 344 *controls* the width of the substrate coupling area by serving as an etch mask for etching of [blue] sub interlevel dielectric layer 331 and [green] etch stop layer 321.



EX1001, FIGs. 3C-3E; EX1002, ¶68.

**PO Litigation Construction:** In its Complaint against Petitioner, PO appears to apply a broader construction of this claim phrase. *See* EX1012, ¶¶134.h, 149.a. Specifically, PO appears to interpret “a spacer region *such that* a substrate coupling area of said contact region is smaller than a metal layer coupling area of said contact region” to require only that (1) the “spacer region” exist in the integrated circuit and (2) with the spacer region present, “a substrate coupling area of said contact region is smaller than a metal layer coupling area of said contact region.”

This PO Litigation Construction interprets “such that” as merely requiring that the recited dimensions be true in a device including the recited spacer region. It is unclear how the PO Litigation Construction can be reconciled with the file history. During prosecution of the ’797 Patent, the Examiner rejected application Claim 11, asserting that Chung disclosed the recited etch stop and insulating layers, as well as that [red] etching buffer layers 485 of Chung were “spacer[s].” EX1007, 69/137.



EX1009, FIG. 4; EX1002, ¶70. Applicants did not dispute this mapping, but instead amended the step of forming the sub-spacer regions to further recite “such that a substrate coupling area of said contact region is smaller than a metal layer coupling area of said contact region.” EX1007, 53/137. The Examiner then allowed the claim, listing the recited etch stop and insulating layers along with the “such that” phrase in the reasons for allowance. *Id.*, 41/137.

As can be seen in Chung’s FIG. 4, the substrate coupling area (at the bottom of 493) is smaller than a metal layer coupling area (at the top of 493). Thus, this amendment could not have supported an allowance of the claims under the PO Litigation Construction. EX1002, ¶71. Nevertheless, in view of PO’s apparent

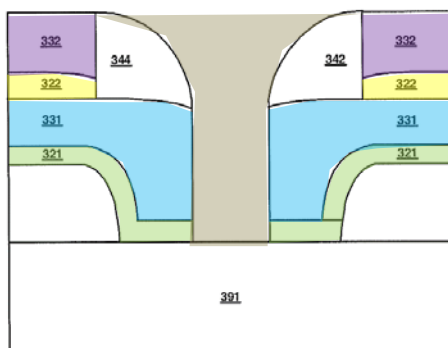
attempt to broaden the claims, this Petition also includes proposed grounds that apply this broader PO Litigation Construction.

## IX. SPECIFIC EXPLANATION OF GROUNDS

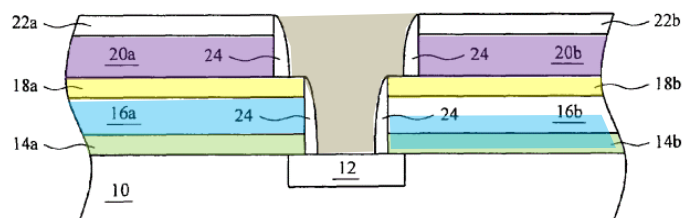
### A. Ground 1 – Peng-Brase Renders Obvious Claims 1-8

#### 1. Peng

Peng discloses a “dual damascene” process for use in “methods for fabricating microelectronic products,” which typically “include[] a semiconductor substrate.” EX1003, 1:11-12, 3:47-49, 3:57-61. Peng uses the same layers in the same sequence as the ’797 Patent’s claimed “multiple etch stop insulation layer.” Specifically, Peng includes a [green] “pair of patterned first barrier layers 14a and 14b” (the claimed first etch stop layer), a [blue] “pair of patterned first dielectric layers 16a and 16b” (the claimed first sub interlevel dielectric layer), a [yellow] “pair of patterned etch stop layers 18a and 18b” (the claimed second etch stop layer), and a [purple] “pair of patterned second dielectric layers 20a and 20b” (the claimed second sub interlevel dielectric layer) all formed on substrate 10. EX1003, 4:16-23.



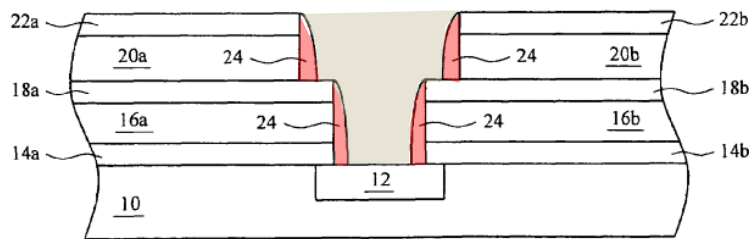
EX1001, FIG. 3E



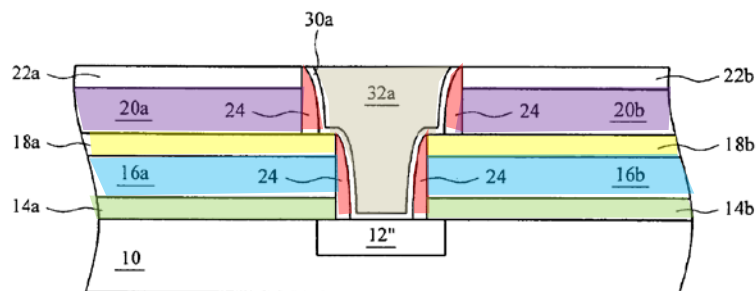
EX1003, FIG. 2



Peng discloses embodiments with and without [red] “optional sidewall protecting layers 24 upon sidewall surfaces within the [tan] dual damascene aperture 11.”



EX1003, 4:41-43, FIG. 2. In either case, [tan] “patterned second copper containing conductor layer 32a” fills dual damascene aperture 11. EX1003, 6:45-51; EX1002, ¶73.

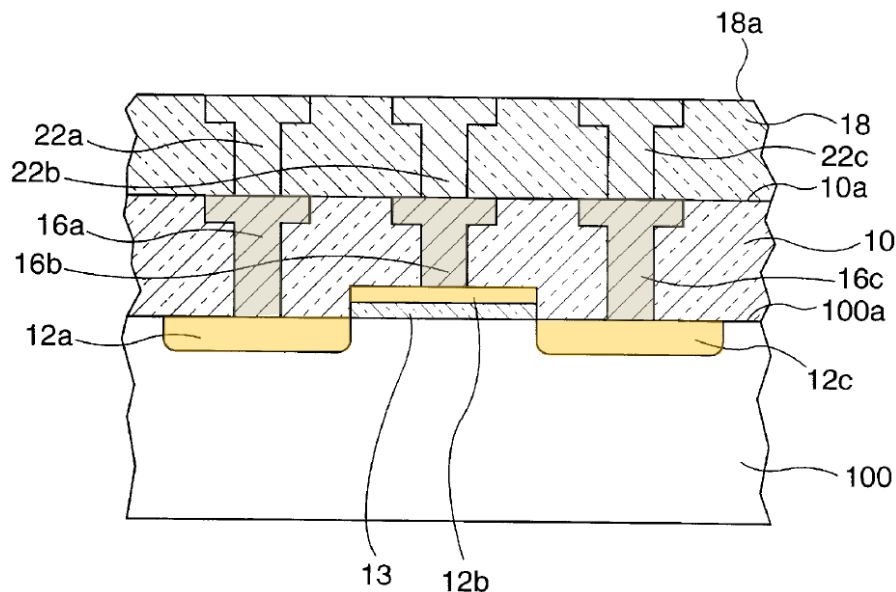


EX1003, FIG. 6.

## 2. *Brase*

Brase, like Peng, discloses a “dual Damascene process” within “integrated circuit devices.” EX1005, 1:7-12. Brase discloses additional details regarding how dual damascene structures fit within integrated circuit devices, consistent with a POSITA’s general knowledge. EX1002, ¶75. Specifically, Brase discloses a substrate having active devices with [orange] source, drain, and gate regions with

contacts accessing those regions to provide an electrical connection to metal interconnect layers above. EX1005, FIG. 1. As shown below, Brase discloses a “portion of a silicon wafer 100” with a “field effect transistor” having [orange] “diffused regions 12a and 12c, the drain and source regions, respectively, and a [orange] gate region 12b which is over a dielectric gate layer 13.”



*Id.*, 4:46-53, FIG. 1; EX1002, ¶75. Brase further discloses openings through “insulating (dielectric) layer 10” “to expose the diffusion regions 12a and 12c and the gate region 12b” in the form of a [tan] dual damascene via/trench structure filled with “metal 16a, 16b, and 16c.” EX1005, 4:46-65. Finally, Brase discloses that the top of “metal 16a, 16b, and 16c” are used “to provide metal to metal contact” with additional metal layers above. *Id.*, 4:67-5:3.

### 3. *Motivation to Combine*

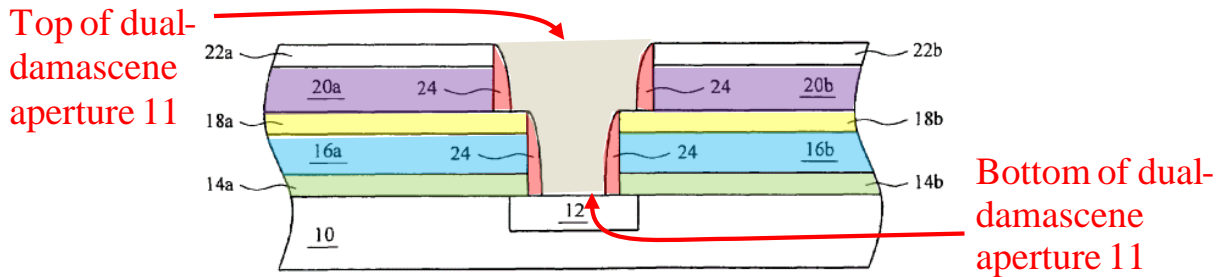
To implement a complete integrated circuit featuring Peng's dual damascene structure, a POSITA would have been motivated to utilize Brase's disclosure of well-known integrated circuit structures surrounding a dual damascene contact. EX1002, ¶76. That is, a POSITA would have been motivated to include surrounding circuitry beyond the specific disclosure of Peng because a POSITA would have understood that doing so was necessary to implement a complete device. *Id.* This is consistent with Peng's explicit description that "substrate 10 *may be employed within* a microelectronic product selected from the group including but not limited to *integrated circuit products.*" EX1003, 3:57-61; *see also id.*, 1:54-57; EX1002, ¶76. Accordingly, a POSITA would have been motivated to utilize Brase's disclosure of well-known integrated circuit structures surrounding a dual damascene contact. EX1002, ¶76.

Because each of Peng and Brase disclose use of dual damascene contacts for interconnections within an integrated circuit (*see* §§IX.A.1, IX.A.2), a POSITA would have understood Brase's disclosure to be compatible with Peng. EX1002, ¶77. Such use would not present any technical challenges because the contact formation described in Peng is agnostic of the contents of the substrate to which the contact is formed and coupled. *Id.* Further, all of the manufacturing steps for

forming Peng's damascene aperture 11 operate only on layers on the substrate, and are not materially affected by the contents of the substrate. *Id.*

#### **4. *Modification of Peng in view of Brase***

Peng-Brase would include the well-known integrated circuit structures described by Brase, in combination with Peng's dual-damascene structure. EX1002, ¶78. Utilizing Brase's disclosure of well-known integrated circuit structures to implement Peng's dual-damascene structure does not require changes to Peng's disclosure of damascene aperture 11 and surrounding layers. *Id.* Rather, the implementation relies on Brase to complete the structures above and below. *Id.* First, it was within the general knowledge of a POSITA, as demonstrated by Brase, that a substrate such as Peng's substrate 10 would include elements of active devices such as Brase's "field effect transistor" having "diffused regions 12a and 12c, the drain and source regions, respectively, and a gate region 12b which is over a dielectric gate layer 13." EX1005, 4:50-53; EX1002, ¶78. A POSITA would have understood that the bottom of Peng's damascene aperture 11 would contact a region of that substrate requiring interconnection, *i.e.*, one of diffused regions 12a and 12c. EX1002, ¶78, EX1003, FIG. 2, EX1005, FIG. 1. Indeed, a POSITA would have understood that exposing each such region to enable interconnections was necessary for the devices to function. EX1002, ¶78.



EX1003, FIG. 2; EX1005, 4:50-55, 4:67-5:3.

Second, turning to the top of damascene aperture 11, it was within the general knowledge of a POSITA, as explained and illustrated by Brase, that the top of damascene aperture 11 is available “to provide metal to metal contact” with metal interconnect layers above. EX1002, ¶79; EX1005, 4:67-5:3.

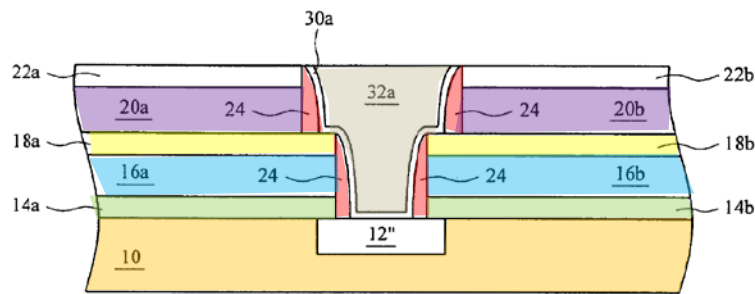
### 5. *Element-by-element Analysis*

#### **Limitation 1[p]: “An integrated circuit comprising”**

Peng modified by Brase discloses this limitation. Peng discloses “fabricating a microelectronic product” on a substrate, in which the “microelectronic product selected from the group including but not limited to *integrated circuit products*.” EX1003, 1:54-55; 3:57-61; 7:8-67; FIG. 6; EX1002, ¶80.

#### **Limitation 1[a]: “a substrate for providing an electrical well for said integrated circuit”**

As discussed in Section IX.A.4, above, Peng-Brase includes an [orange] substrate having “diffused regions 12a and 12c, the drain and source regions, respectively.” EX1005, 4:50-55.



EX1003, FIG. 6; EX1005, 4:50-55; EX1002, ¶81.

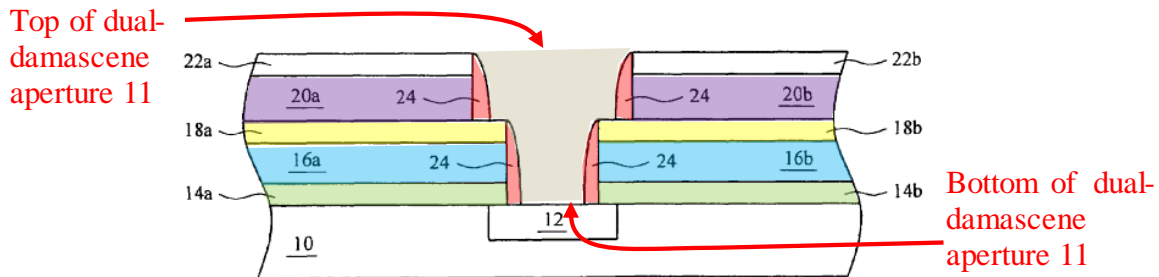
A POSITA would have understood that diffused regions 12a and 12c are necessarily “electrical wells” provided in a substrate. EX1002, ¶82. Specifically, a diffused region in a semiconductor device is doped with a p-type or n-type material to create an electrical well of charge carriers that move to produce the electrical current through the device. *Id.*, (citing EX1011,<sup>5</sup> 34/170).

**Limitation 1[b]: “a contact region coupled to said substrate, said contact region provides an electrical path to and from said substrate”**

As discussed in Section IX.A.4, Peng’s [tan] “damascene aperture 11” (the claimed contact region) exposes a region of the substrate requiring interconnection, including any one of diffused region 12a (drain) or 12c (source). EX1003, FIG. 2; EX1005, 4:50-55, 4:67-5:3; EX1002, ¶83.

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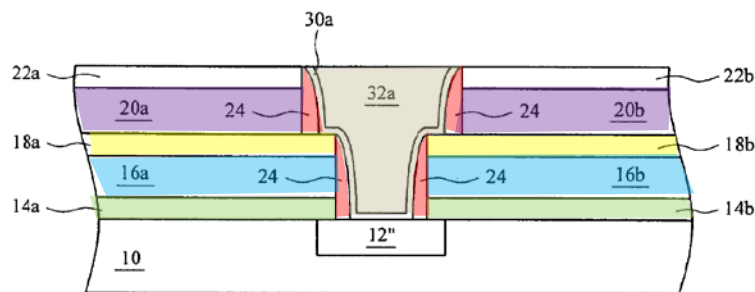
<sup>5</sup> EX1011 (Streetman) is authentic and was publicly available no later than June 9, 1999. EX1002, ¶18; EX1025, ¶¶46-53.



EX1003, FIG. 2; EX1002, ¶83.

[Tan] damascene aperture 11 is coupled to the substrate to expose one of diffused region 12a (drain) or 12c (source), each of which is within substrate 10. EX1003, 3:40-42 (“A patterned copper containing conductor layer 12 is formed *within the substrate 10*.”); *id.*, FIG 2; EX1002, ¶84.

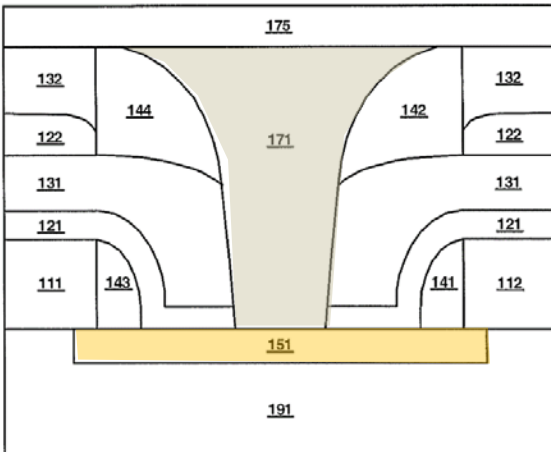
Damascene aperture 11 is filled with “patterned second copper containing conductor layer 32a” and “patterned barrier layer 30a” (which is a “conductor barrier layer”), establishing an electrical path to and from the substrate.



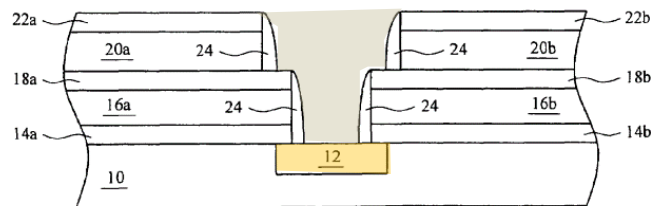
EX1003, FIG. 6, 6:37-54; EX1002, ¶85.

This understanding of Peng-Brase is what the '797 Patent describes—*i.e.*, for FIG. 1B, “[c]ontact region 171 is coupled to substrate 191.” EX1001, 3:67-4:16. As

can be seen in FIG. 1B, contact region 171 is in contact with [orange] source/drain region 151 within substrate 191.



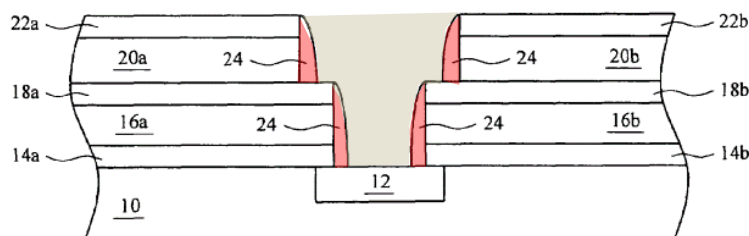
EX1001, FIG. 1B



EX1003, FIG. 2

**Limitation 1[c]: “a spacer region such that a substrate coupling area of said contact region is smaller than a metal layer coupling area of said contact region”**

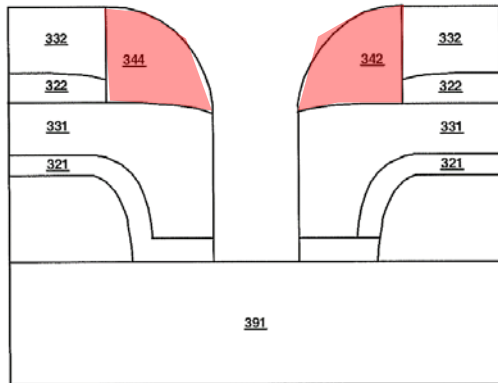
Peng-Brase discloses this limitation under the **PO Litigation Construction** of this term. *See* §VIII.C.3, above. Peng discloses [red] “sidewall protecting layers 24” (the claimed spacer regions) “upon sidewall surfaces within the dual damascene aperture 11.”



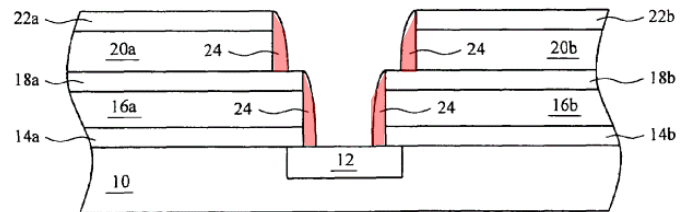
EX1003, 4:40-52; FIG. 2; EX1002, ¶86-87.



Sidewall protecting layers 24 closely resemble '797 Patent's spacers 342 and 342. EX1002, ¶225.

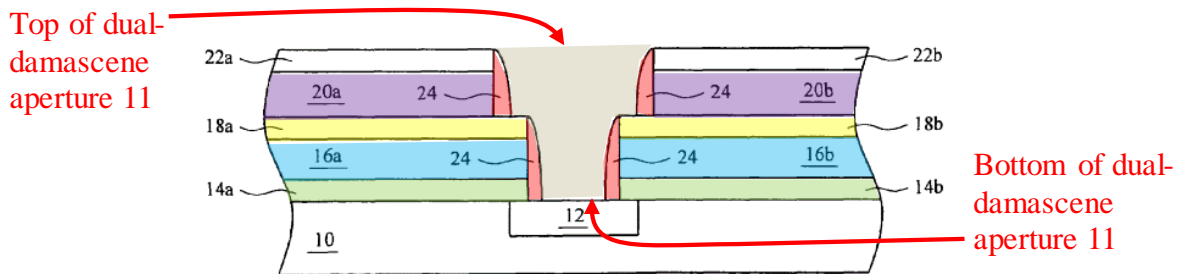


**EX1001, FIG. 3E**



**EX1003, FIG. 2**

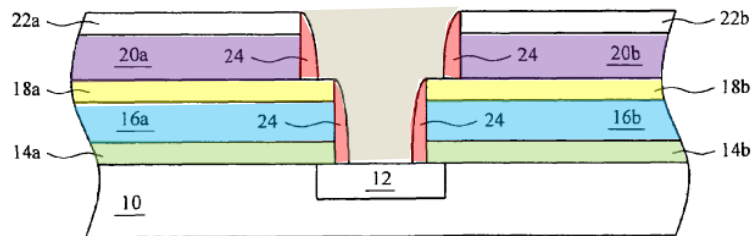
Peng also discloses that, with sidewall protecting layers 24 in place, the opening at the bottom of damascene aperture 11 (the claimed substrate coupling area of the contact region) is smaller than the opening at the bottom of damascene aperture 11 (the claimed metal layer coupling area of the contact region).



EX1003, FIG. 2; EX1002, ¶88. The larger width of the trench region as compared to the via region of the dual damascene aperture is a fundamental feature of dual damascene designs. EX1002, ¶88.

**Limitation 1[d]: “a multiple etch stop insulation layer coupled to said contact region, wherein said multiple etch stop insulation layer provides electrical insulation between other regions of said integrated circuit and isolates guidance of electrical current flow in said contact region”**

Peng-Brase would include Peng’s stack of insulating layers (the claimed multiple etch stop insulation layer) formed on substrate 10 including a [green] “pair of patterned first barrier layers 14a and 14b,” a [blue] “pair of patterned first dielectric layers 16a and 16b,” a [yellow] “pair of patterned etch stop layers 18a and 18b,” and a [purple] “pair of patterned second dielectric layers 20a and 20b.”



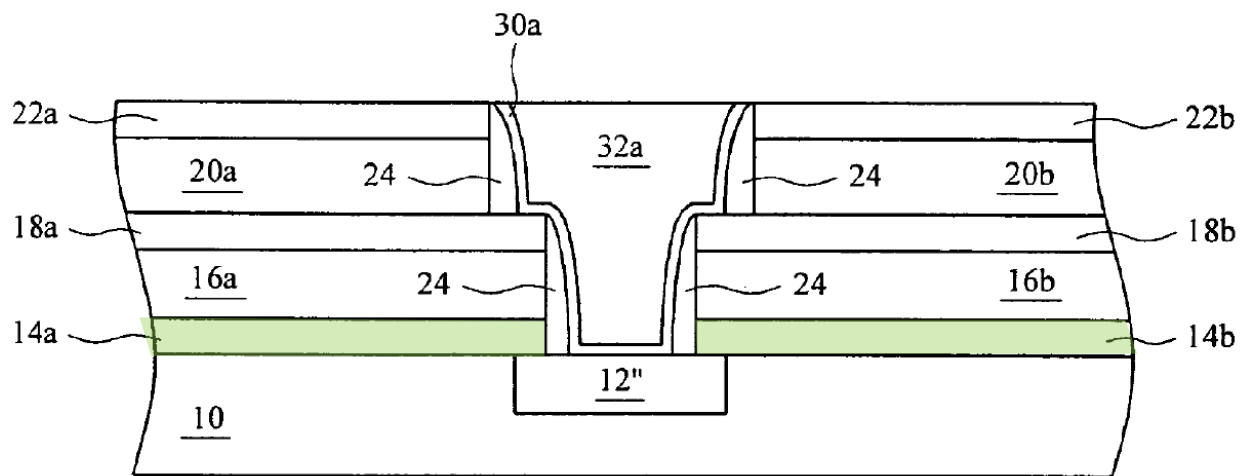
EX1003, 4:24-33, FIG. 2; EX1002, ¶89.

These layers are coupled to [tan] damascene aperture 11 (the claimed contact region) both (a) directly via the portions [yellow] of etch stop layers 18a/18b between the upper and [red] lower spacers 24 on either side of aperture 11, and (b) indirectly through [red] sidewall protecting layers 24. EX1003, FIG. 2; EX1002, ¶90. These layers provide electrical insulation between other regions of said integrated circuit and isolates guidance of electrical current flow in said contact region because each of the layers is a dielectric layer. EX1003, 4:16-23; EX1002,

¶90. Specifically, Peng discloses layers 16a, 16b, 20a, and 20b are “any of several dielectric materials” and layers 14a, 14b, 18a, and 18b are “higher dielectric constant dielectric materials.” EX1003, 4:1-20. A POSITA would have understood that each of these dielectric materials is an insulating material. EX1002, ¶90.

**Limitation 1[d1]: “wherein said multiple etch stop insulation layer includes: a first etch stop layer directly on said substrate in said contact region”**

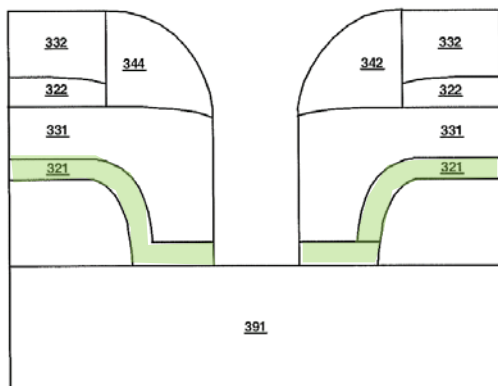
Peng-Brase would include Peng’s [green] “barrier layers” 14a and 14b. EX1003, 4:16-23; EX1002, ¶91.



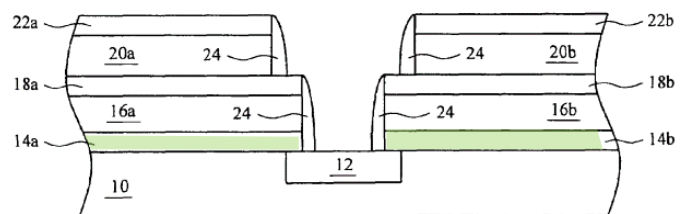
A POSITA would have understood Peng uses the term “barrier layer” interchangeably with “etch stop layer.” EX1002, ¶92. Peng separately refers to another “barrier dielectric layer,” layer 22, as a “*stop* layer” (which a POSITA would have understood to refer to an *etch* stop layer). EX1003, 3:53-54; 4:34; EX1002, ¶92.

A POSITA would further understand Peng's description of the chemistry and location of that the barrier layers 14a and 14b refer to an "etch stop layer." EX1002, ¶93. Peng's barrier layers 14a and 14b are "higher dielectric constant [] materials," whereas neighboring layers 16a and 16b are "comparatively lower dielectric constant dielectric material." EX1003, 4:16-23; EX1002, ¶93. A POSITA would have understood that such higher dielectric constant materials have a lower etch rate for certain etchants compared to neighboring low dielectric material. EX1002, ¶93 (citing EX1020, 2:30-34).

Finally, barrier layers 14a and 14b are directly on the substrate. EX1003, FIG. 2; EX1002, ¶94. Further, barrier layers 14a and 14b are "on said substrate in said contact region" to the same degree as the '797 Patent, which illustrates etch stop layer 321 patterned around the contact region.



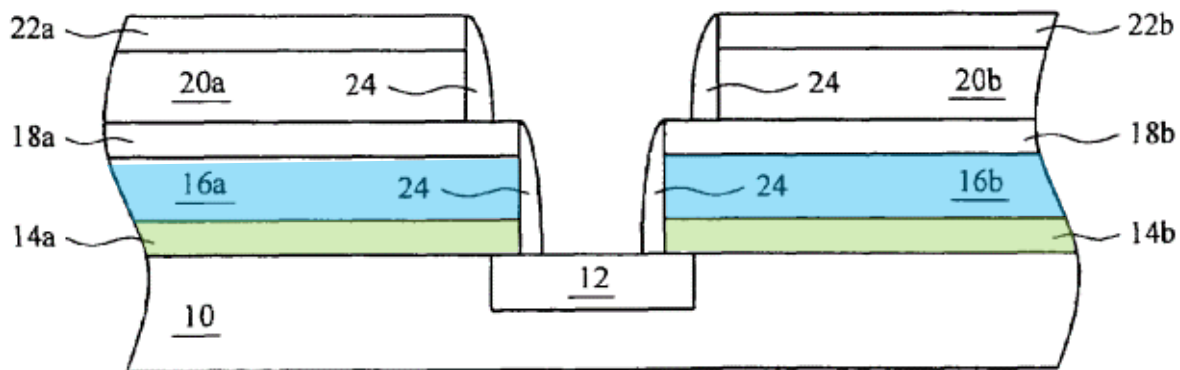
**EX1001, FIG. 3E**



**EX1003, FIG. 2**

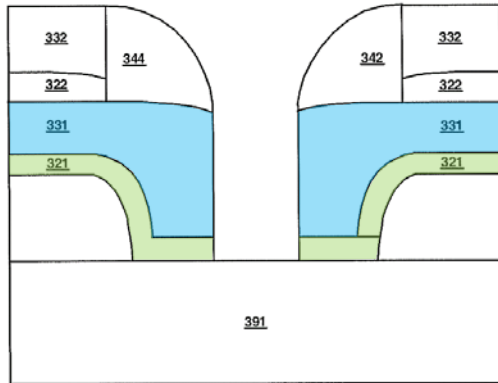
**Limitation 1[d2]: “a first sub interlevel dielectric layer over said first etch stop layer”**

Peng discloses [blue] “dielectric layers 16a and 16b” (the claimed first sub interlevel dielectric layer) over the [green] barrier layers 14a and 14b (the claimed first etch stop layer).

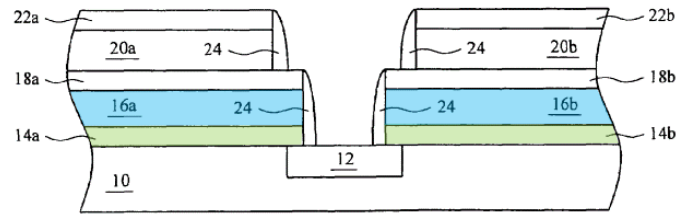


EX1003, FIG. 2, 4:16-23; EX1002, ¶95.

Dielectric layers 16a and 16b match the '797 Patent's [blue] sub interlevel dielectric layer 331. EX1002, ¶96.



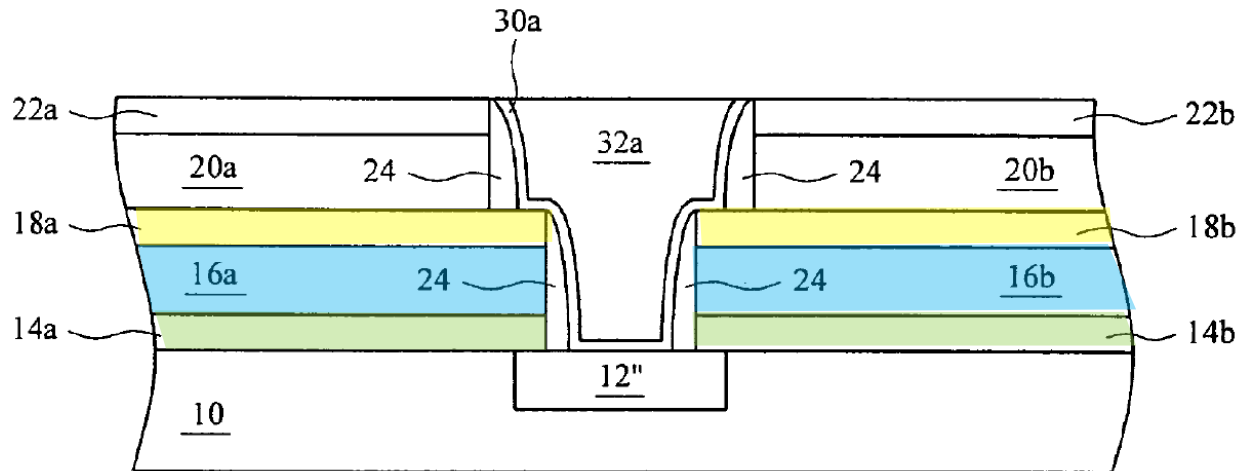
**EX1001, FIG. 3E**



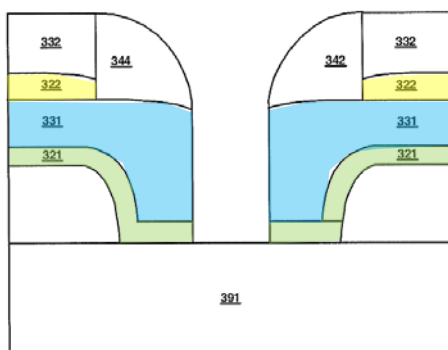
**EX1003, FIG. 2**

**Limitation 1[d3]: “a second etch stop layer over said first sub interlevel dielectric layer, wherein said second etch stop layer has similar selectivity characteristics as said first etch stop layer and wherein said first sub interlevel dielectric layer is between said first etch stop layer and said second etch stop layer”**

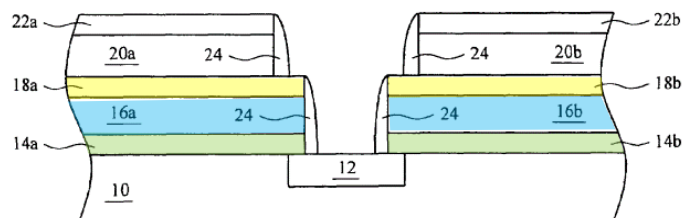
Peng discloses [yellow] “etch stop layers 18a and 18b” (the claimed second etch stop layer) over [blue] dielectric layers 16a and 16b (the claimed first sub interlevel dielectric layer).



EX1003, FIG. 2, 4:16-23; EX1002, ¶97. Further, as shown, [blue] dielectric layers 16a and 16b (the claimed first sub interlevel dielectric layer) are between the first [green] barrier layers 14a and 14b (the claimed first etch stop layer) and [yellow] etch stop layers 18a and 18b. *Id.* Again, the arrangement of these layers matches the '797 Patent.



**EX1001, FIG. 3E**



**EX1003 (Peng), FIG. 2**

Peng describes that “[e]ach of the ... first barrier layers 14a and 14b [and] etch stop layers 18a and 18b ... is typically formed of higher dielectric constant

dielectric materials.” EX1003, 4:16-23; EX1002, ¶98. A POSITA would have understood this passage describing the materials for both layers collectively as disclosing or, at a minimum, suggesting using the same materials for both layers. EX1002, ¶98. By selecting the same material for the two layers, the layers will necessarily have identical etch selectivities. *Id.*, ¶¶99-100.

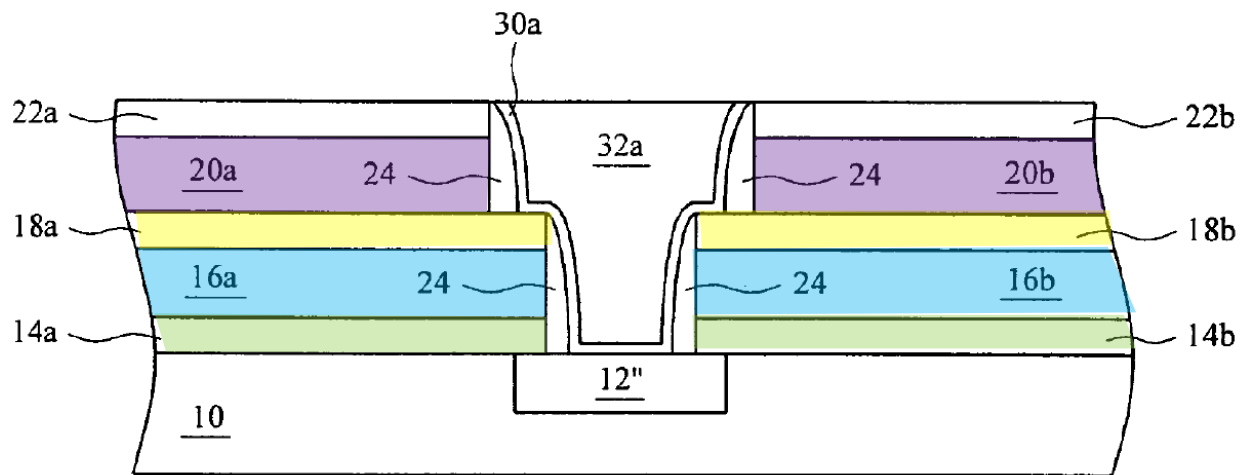
Further, a POSITA would have understood that the most straightforward implementation these two etch stop layers having similar properties is to use the same material. EX1002, ¶99. A POSTIA would have been motivated to choose the same materials for these layers because reducing the number of different materials in the structure reduces complexity during manufacturing. *Id.* An increase in the number of materials increases the number of different etchants, source materials, and recipes required to manufacture the integrated circuit, which increases the cost and decreases the yield. *Id.*

Finally, even if layers 14 and 18 were formed with different materials, but both higher dielectric constant dielectric materials, a POSITA would expect such materials would have similar properties, including similar selectivity characteristics. *Id.*, ¶101.

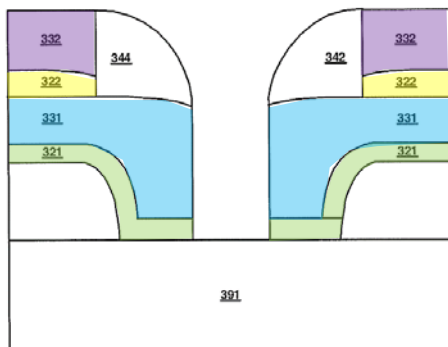


**Limitation 1[d4]: “a second sub interlevel dielectric layer over said second etch stop layer”**

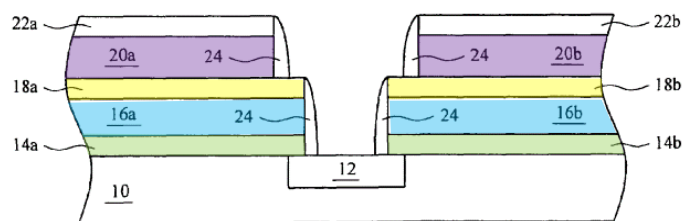
Peng modified by Brase discloses this limitation. Peng discloses [purple] dielectric layers 20a and 20b (the claimed second sub interlevel dielectric layer) over [yellow] etch stop layers 18a and 18b (the claimed second etch stop layer).



EX1003, FIG. 2, 3:50-54; EX1002, ¶102. Again, the arrangement of these layers matches the '797 Patent.



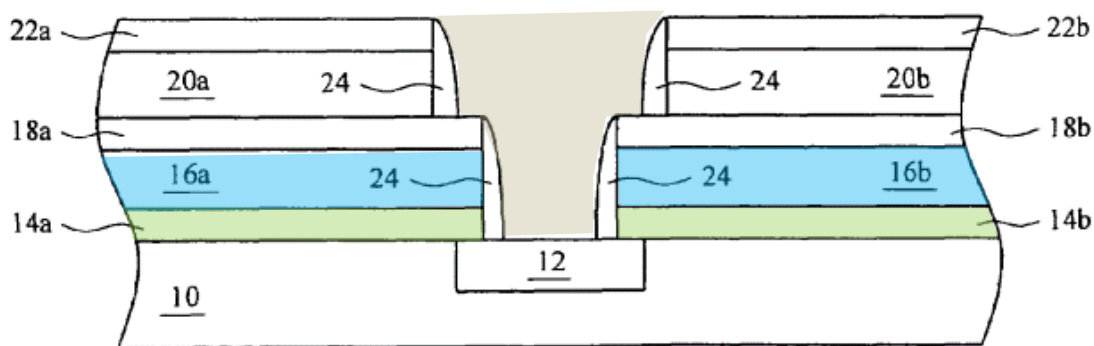
**EX1001, FIG. 3E**



**EX1003 (Peng), FIG. 2**

**Limitation 2: “An integrated circuit of claim 1 wherein said first etch stop layer protects removal of a substrate material by an etch process.”**

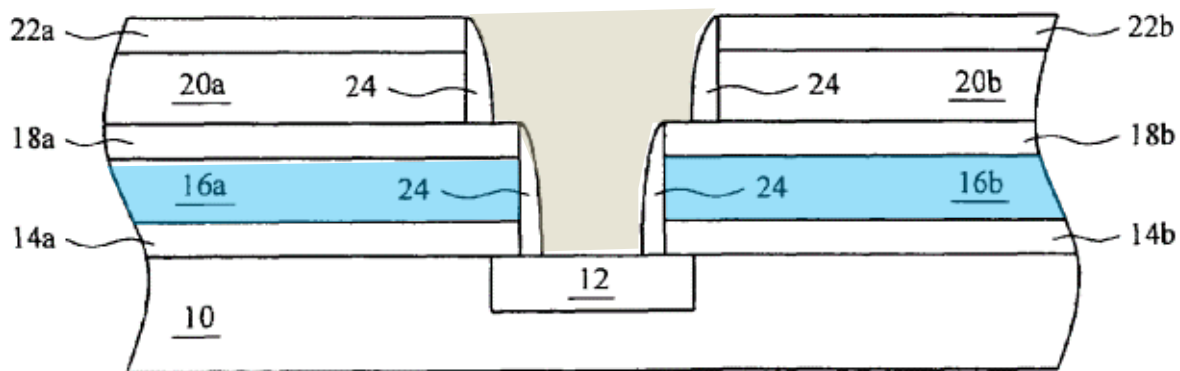
[Green] barrier layers 14a and 14b (the claimed first etch stop layer) protects removal of a substrate by an etch process based on their position and function. Peng refers to [green] layers 14a and 14b and [blue] layers 16a and 16b as “patterned” layers, which a POSITA would have understood refers to etching of those layers to form the contact opening. EX1003, 3:43-47; EX1002, ¶103.



EX1003, FIG. 2, 4:24-33; EX1002, ¶103. As explained for Limitation 1[d1], barrier layers 14a and 14b are an etch stop layer and have a significantly lower etching rate than a neighboring layer, the dielectric layers 16a and 16b. By serving as an etch stop layer arranged between layers 16a and 10, a POSITA would have understood that barrier layers 14a and 14b protect removal of a substrate material during etching of dielectric layers 16a and 16b. EX1002, ¶103. The barrier layers 14a and 14b are later removed using a different etchant to allow contact to the substrate 10 through the [tan] contact opening. EX1002, ¶103; EX1004, FIG. 12, ¶[0033].

**Limitation 3: “An integrated circuit of claim 1 wherein said first sub interlevel dielectric layer insulates said contact region.”**

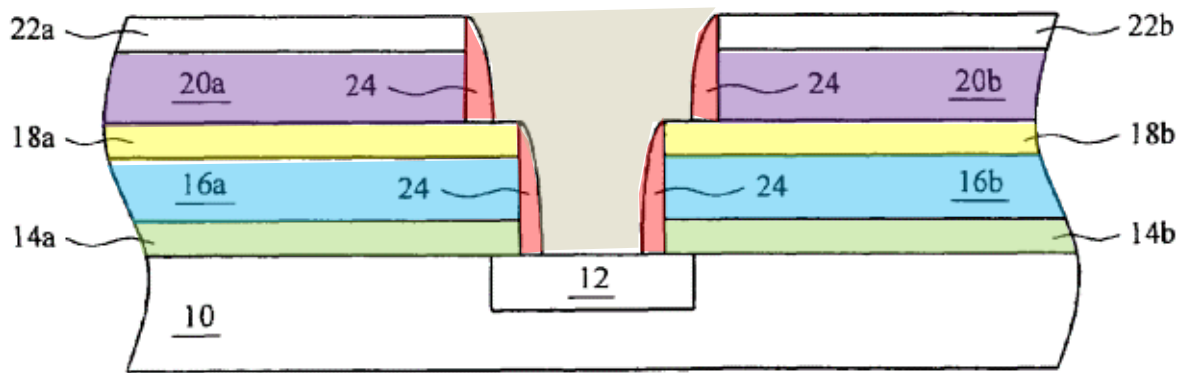
Brase’s first sub interlevel dielectric layers—[blue] dielectric layers 16a and 16b —are “formed of a ... dielectric material,” which a POSITA would have understood is an insulating material. EX1003, 4:20-23; EX1002, ¶104. [Blue] dielectric layers 16a and 16b surround, and thus insulate, the [tan] contact region, in addition to the insulation provided by spacers 24. The isolation of the contact region from other portions of the integrated circuit is a function of the total thickness of materials, and the dielectric layers 16a and 16b contribute to that thickness. *See* §VI.C; EX1002, ¶104.



EX1003, FIG. 2; EX1002, ¶104.

**Limitation 4: “An integrated circuit of claim 1 wherein said second etch stop layer protects lower layers during an etching process.”**

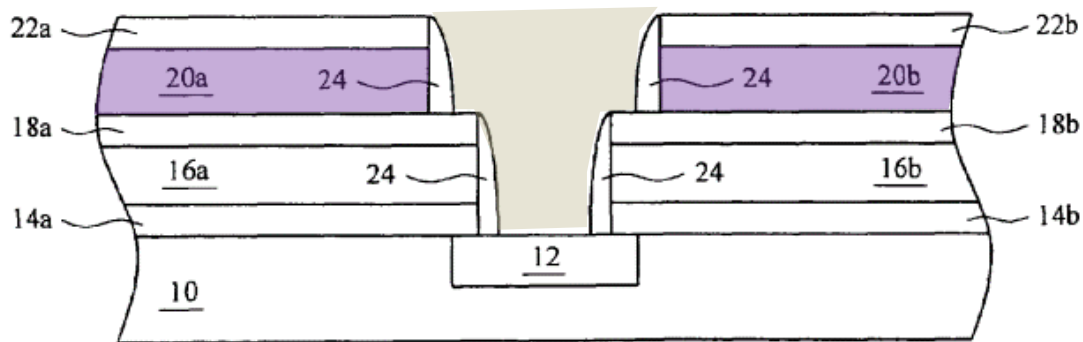
Peng’s second etch stop layer—[yellow] “etch stop layers 18a and 18b”—protects [blue/green] lower layers during an etch process based on their position and function. EX1002, ¶105. A POSITA would have understood based on Peng’s use of the term “etch stop” and description of layer chemistry that [yellow] etch stop layers 18a and 18b serve as an etch stop, having a significantly lower etching rate (than [purple] dielectric layers 20a/20b) for an etchant used to etch [purple] dielectric layers 20a and 20b. EX1003, 4:16-23; EX1002, ¶105. By serving as an etch stop, [yellow] etch stop layers 18a and 18b protects layers below. EX1002, ¶105.



EX1003, FIG. 2.

**Limitation 5: “An integrated circuit of claim 1 wherein said second sub interlevel dielectric layer insulates said contact region.”**

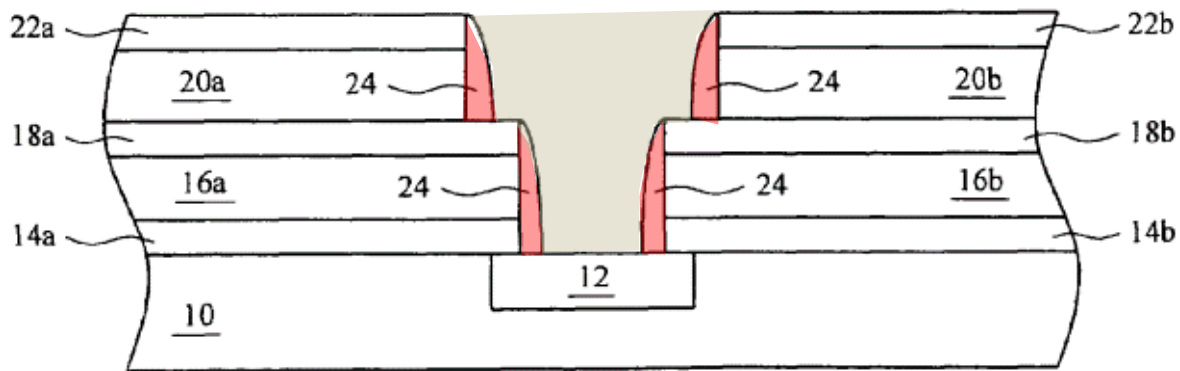
Peng modified by Brase discloses this limitation. [Purple] dielectric layers 20a and 20b (the claimed second sub interlevel dielectric layer) are “formed of a ... dielectric material,” which a POSITA would have understood is an insulating material. EX1003, 4:20-23; EX1002, ¶106. [Purple] dielectric layers 20a and 20b surround, and thus insulate, the [tan] contact region as described above in Limitation 3 for the dielectric layers 16a and 16b.



EX1003, FIG. 2; EX1002, ¶106.

**Limitation 6: “An integrated circuit of claim 1 wherein said spacer region insulates said contact region.”**

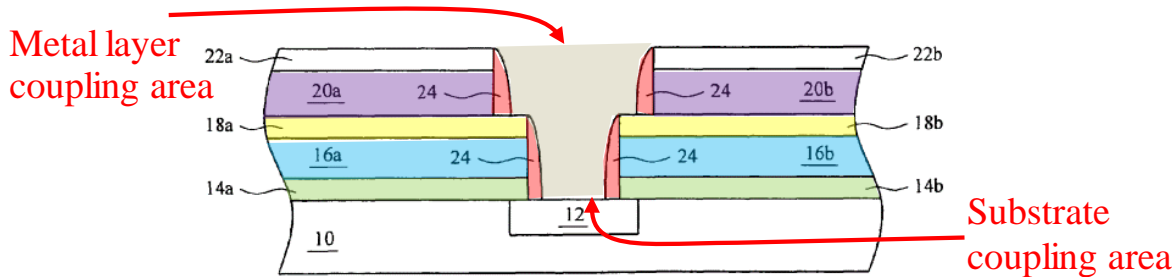
Peng’s spacer region—[red] sidewall protecting spacers 24—are “formed of a ... dielectric material,” which a POSITA would have understood to be an insulating material. EX1003, 4:43-50; EX1002, ¶107. [Red] sidewall protecting layers 24 surround the [tan] contact region, and thus insulate it, as described above in Limitation 3 for the dielectric layers 16a and 16b.



EX1003, FIG. 2; EX1002, ¶107.

**Limitation 7: “An integrated circuit of claim 1 wherein said substrate coupling area of said contact region permits multiple active regions to be arranged relatively close to one another while a metal layer coupling area of said contact region is larger than said substrate coupling area of said contact region to provide better process window with desired critical dimension (CD).”**

Peng-Brase includes this limitation. The '797 Patent does not describe this claim limitation as a separate structural or functional element, but rather as a benefit flowing from the relative sizes of the top and bottom coupling areas of the contact region already recited in Limitation 1[c]. EX1001, 4:39-49. Thus, this element is met based on the shape of damascene aperture 11 demonstrated for Limitation 1[c] and shown below.



EX1003, FIG. 2; EX1002, ¶108.

First, as discussed in Section VI.A above, integrated circuits include rows of repeated gate and source/drain regions making up transistors. Minimizing the width between successive gates maximizes density. EX1002, ¶109. Each of the gates includes an accompanying source/drain region. *Id.* (citing EX1004, FIG. 17). Those source/drain regions are located between successive gates. *Id.* Contacts are formed to those source/drain regions to electrically couple the transistors. *Id.*; EX1005, FIG. 6. One limiting factor to the ability to reduce width between successive gates is the space needed for contact to the source/drain regions that are located around each of the gates. EX1002, ¶109; EX1019, 73/112. The contact to the source/drain regions is through the damascene aperture 11 as described in §IX.A.4. EX1002, ¶78. Thus, a POSITA would have understood that the relatively small substrate coupling area of damascene aperture 11 permits multiple active regions—*i.e.*, gate regions of adjacent transistors—to be arranged relatively close to one another (as compared to designs with larger substrate coupling areas that would require gate regions to be placed farther apart). EX1002, ¶109; *compare to* EX1001, 4:45-47.

Second, as described in Section IX.A.4 above, the top of damascene aperture 11 is available “to provide metal to metal contact” with metal interconnect layers above. EX1002, ¶79; EX1005, 4:67-5:3. A POSITA would have understood that the larger coupling area at the top of damascene aperture 11 is easier to align with the contacting metal above, resulting in a higher likelihood that the contact to the substrate that is formed has a contact area greater than a minimum desired contact area, referred to as a critical dimension, for conducting electrical signals. EX1002, ¶110; EX1008, 233/269; *compare to* EX1001, 4:47-49.

**Limitation 8: “An integrated circuit of claim 1 wherein said first etch stop layer is in a range of about 300 to 800 Å thick, said first sub interlevel dielectric layer is in a range of about 1,000 to 2,000 Å thick, said second etch stop layer is in a range of about 300 to 800 Å thick and said second sub interlevel dielectric layer is in a range of about 10K Å±1K Å thick.”**

Peng’s first etch stop layer—barrier layers 14a and 14b—has a thickness of 200-500Å, which overlaps the claimed range of 300-800Å. EX1003, 4:24-35. Peng’s first sub interlevel dielectric layer—dielectric layers 16a and 16b—has a thickness of 1000-4000Å, which overlaps the claimed range of 1000-2000Å. EX1003, 4:24-35. And Peng’s second etch stop layer—etch stop layers 18a and 18b—has a thickness of 200-500Å, which overlaps the claimed range of 300-800Å. EX1003, 4:24-35; EX1002, ¶111. This disclosure of overlapping ranges



“establishes a *prima facie* case of obviousness.” *Genentech, Inc. v. Hospira, Inc.*, 946 F.3d 1333, 1341 (Fed. Cir. 2020).

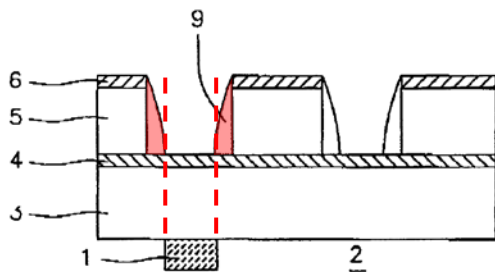
Peng discloses dielectric layers 20a and 20b (the claimed second sub interlevel dielectric layer) having a thickness of 1000-4000Å. EX1003, 4:31-33. A POSITA would have understood that a dielectric layer of this range would have the same properties as a dielectric layer in the claimed range of 9000-11000Å. EX1002, ¶¶112-14 (citing EX1022, at 3/4 (“Notice that the thickness dependence is almost negligible for samples with  $K \leq 10$ .”)). Specifically, a POSITA would have understood the thickness of dielectric layers 20a and 20b was chosen to provide insulation from the layers above. *Id.*, ¶¶113-14. Having chosen the disclosed range to be thick enough to provide the desired insulation, it follows that a thicker layer in the claimed range would continue to provide the desired insulation. *Id.* Accordingly, “a prima facie case of obviousness exists” because “the claimed range and the prior art range do not overlap but *are close enough such that one skilled in the art would have expected them to have the same properties.*” *In re Peterson*, 315 F.3d 1325, 1329 (Fed. Cir. 2003).

**B. Ground 2 – Peng-Chien-Brase Renders Obvious Claims 1-8 & 11-12**

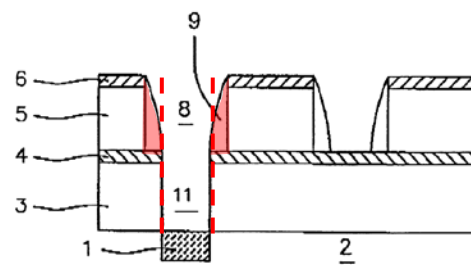
**1. Chien**

Chien, like Peng, discloses a “dual damascene method for interconnecting metal conductive lines and via plugs in integrated circuits.” EX1006, 1:5-11. Chien,

however, uses spacers to define an area to be etched in its lower dielectric layer, in the same manner as the '797 Patent. As shown below in FIGs. 2d and 2f, Chien discloses using [red] “second conductive line spacers 9”<sup>6</sup> that “provide an easier controlled alignment.” *Id.*, 4:34-35. Chien discloses, first, “depositing a protective layer” of “conformal silicon nitride;” and, second, “forming [red] second conductive line spacers 9” from the layer by “removing the protective layer” from horizontal surfaces (*i.e.*, anisotropically etching). *Id.*, 4:25-39, FIG. 2d; EX1002, ¶¶115-116.



**EX1006, FIG. 2d**



**EX1006, FIG. 2f**

Then, Chien discloses “utilizing ... [red] second conductive line spacers 9 as an etching mask” to form “via hole 11” within the damascene aperture. EX1006, 4:57-62, FIG. 2f; EX1002, ¶116.

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<sup>6</sup> The modifier “second conductive line” before spacers refers to the fact that the spacers are formed in the opening that eventually is filled with conductive material to form “second conductive line 12.” EX1006, 5:3-6; EX1002, ¶115, n1.

## 2. *Motivation to Combine*

A POSITA would have been motivated to use the dual damascene formation process of Chien in forming the via (smaller, lower portion) of Peng's damascene aperture 11 to obtain the advantages of using spacers as an etching mask to define a contact bottom explicitly described by Chien (and other references), including to overcome challenges with conventional lithography. EX1002, ¶117.

Chien explains that “alignment is a *frequently encountered problem which is needed to be solved in the dual damascene method*,” and the use of spacers 9 solves that problem. EX1006, 4:33-37. In particular, “second conductive line spacers 9 will ensure the via hole to be positioned at the center” and thereby “misalignment can be reduced and thus the process window can be extended and the manufacturing processes can be controlled.” *Id.*, 4:39-44.

Chien further explains that the use of spacers 9 “can produce small-sized via[s] in a less strict process condition,” which was becoming more important as “the integration density of semiconductor devices increases.” EX1006, 2:25-29, 1:15-29; EX1002, ¶119. Chien further explains that: “The introduction of the conductive line spacers not only provides better alignment between the conductive lines and vias but also provide better control of a small via and provides better coverage effects in depositing and filling metal between the conductive line openings and via holes.” EX1006, 3:4-9.

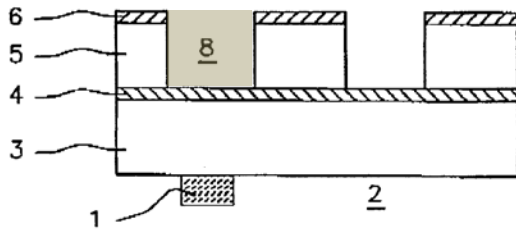
Other references proposing similar solutions to Chien identified similar problems, and explained how the use of spacers as an etching mask overcame that problem. For example, Shields discloses a dual damascene process using “spacers 20” to determine the width of the hole “mak[ing] electrical contact with a source or drain region in the substrate.” EX1016, 4:66-5:6. Like Chien, Shields describes multiple benefits for this process, including “reduc[ing] contact size while avoiding manufacturing difficulties associated with small contacts” and “produc[ing] narrow dual width contacts which provide charge gain reduction.” *Id.*, 5:21-27.

A POSITA would have been motivated to further combine the Peng-Chien combined damascene structure with Brase for the same reasons explained in Section IX.A.3 above for Peng-Brase.

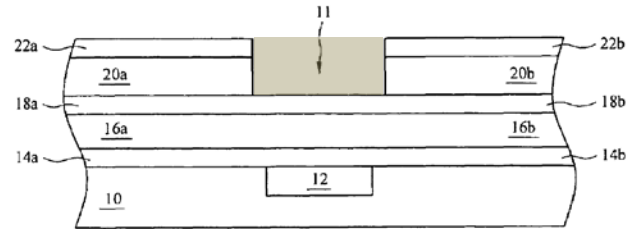
### **3. *Modification of Peng in view of Chien and Brase***

A POSITA would have modified Peng by utilizing the dual damascene formation process of Chien in to form Peng’s dual-damascene aperture 11. EX1002, ¶122.

Chien discloses first using “photolithographic processes” to “form a second line opening 8,” which is the [tan] trench opening. EX1006, 4:10-24, FIGs. 2b-2c. Applying this disclosure to Peng entails using “photolithographic processes” to etch a portion of planarized stop layer 22 and dielectric layer 20 to form the [tan] trench opening of damascene aperture. EX1003, 4:16-23, FIG. 1, EX1002, ¶123.

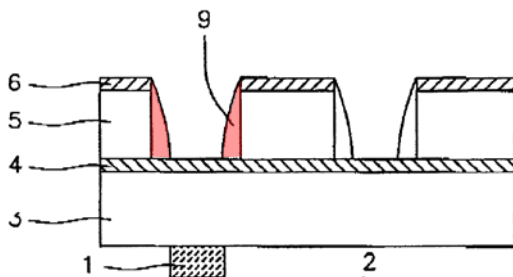


**EX1006, FIG. 2c**

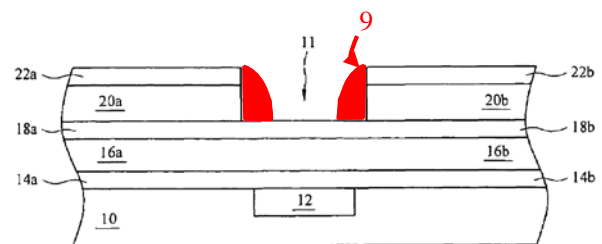


**EX1003, FIG. 1**  
(modified to show lower layers intact)

As shown below, Chien discloses next forming [red] “second conductive line spacers 9” on the sidewalls of the trench opening by “depositing a layer of conformal silicon nitride” and then etching to remove the horizontal portions. EX1006, 4:25-44, FIG. 2d; EX1002, ¶124. Applying this disclosure to Peng entails forming [red] silicon nitride spacers on the sidewalls of planarized stop layer 22 and dielectric layer 20. EX1003, 4:16-23, FIG. 1, EX1002, ¶124. This spacer formation process is fully compatible with Peng as it matches the formation of “optional sidewall protecting layers 24” Peng already discloses (this optional step would be omitted when implementing Chien’s formation process). EX1003, 4:44-47, EX1002, ¶124.

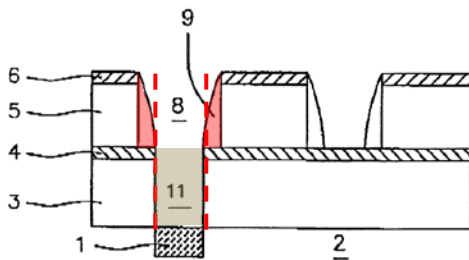


**EX1006, FIG. 2d**

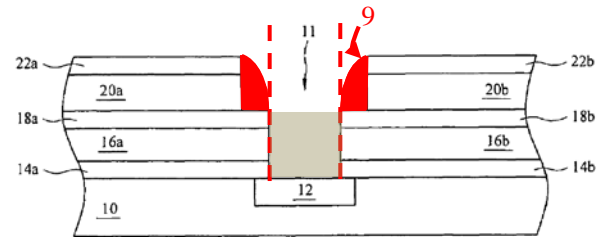


**EX1003, FIG. 1**  
(modified per Chien, and to show  
lower layers intact)

Finally, Chien forms a [tan] “via hole 11” to the substrate by etching the remaining layers, “utilizing ... the [red] second conductive line spacers 9 as an etching mask” as indicated below by the dotted red lines. EX1006, 4:57-5:2; EX1002, ¶125. Applying this disclosure to Peng entails etching etch stop layer 18, dielectric layer 16, and barrier layer 14 to form a via hole to the substrate. EX1003, 4:16-23, FIG. 1, EX1002, ¶125.

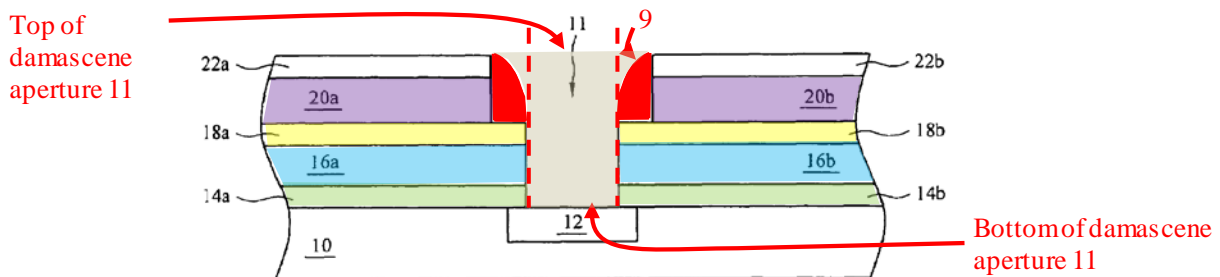


**EX1006, FIG. 2f**



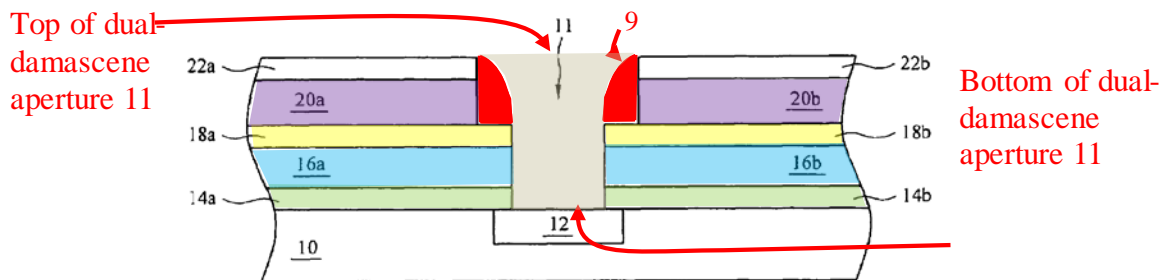
**EX1003, FIG. 1  
(modified per Chien)**

Because Chien, like Peng, discloses a dual damascene aperture, the modification leaves [tan] damascene aperture 11 consistent with Peng’s disclosures, along with spacers on the sidewalls of the trench.



EX1003, FIG. 1; EX1002, ¶126. The opening at the top of damascene aperture 11 remains wider than the opening at the bottom of damascene aperture 11 based on the curve of [red] spacers 9. EX1002, ¶126. This is consistent with Chien, which describes an exemplary “width of the second conductive line opening 8” (the top of the damascene opening) as  $0.2\text{ }\mu\text{m}$  with a corresponding “size of the via hole 11” (the bottom of the damascene opening) as  $0.18\text{ }\mu\text{m}$ . EX1006, 5:31-36.

Finally, implementation of Peng using Chien’s formation further utilizing Brase’s disclosure of well-known integrated circuit structures method leaves damascene aperture 11 and surrounding layers unchanged and relies on the general knowledge of a POSITA, as reflected in Brase, to complete the structures above and below. See §IX.A.4; EX1002, ¶127.



EX1003, FIG. 1; EX1005, 4:50-55, 4:67-5:3; EX1002, ¶127.

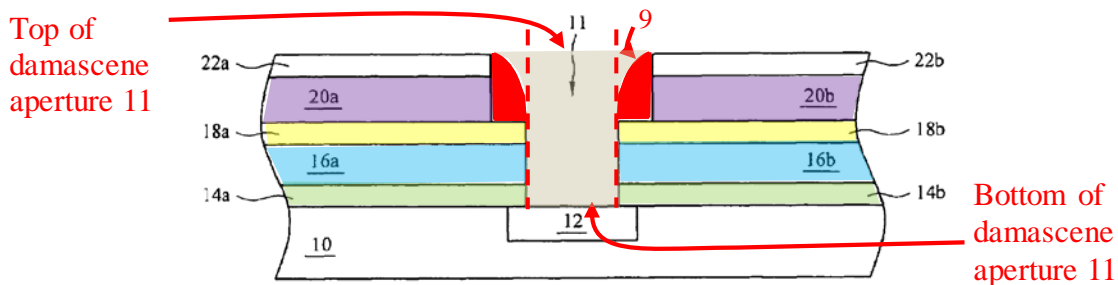
#### 4. *Element-by-element Analysis*

##### **Limitations 1[p], 1[a], 1[b], 1[d1], 1[d2], 1[d3], 1[d4], 2-5, 7, and 8**

Peng-Chien-Brase discloses these limitations for the same reasons described for Peng-Brase in Ground 1. *See* §IX.A above.

##### **Limitation 1[c]<sup>7</sup>**

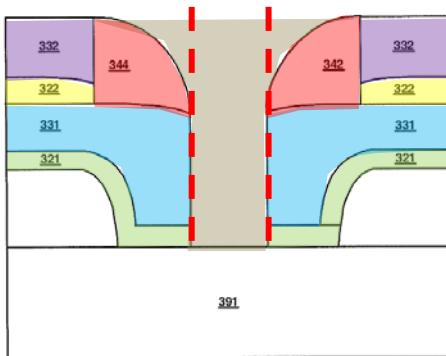
Peng-Chien-Brase discloses this limitation under each of **Petitioner's Construction** and the **PO Litigation Construction**. *See* §VIII.C.3, above. The dual-damascene structure of Peng-Chien includes [red] spacers 9 (the claimed spacer region) on the sidewalls of the trench opening of dual damascene aperture 11:



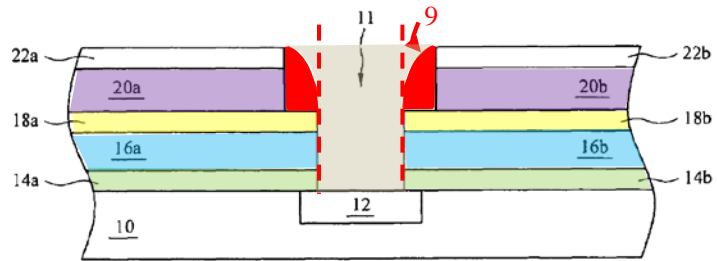
EX1003, FIG. 1; §IX.B.3; EX1002, ¶129. This arrangement matches the '797 Patent.

<sup>7</sup> *See* §IX.A.5 for the text of claim limitations also addressed in Ground 1.





EX1001, FIG. 3E



EX1003 (Peng), FIG. 1

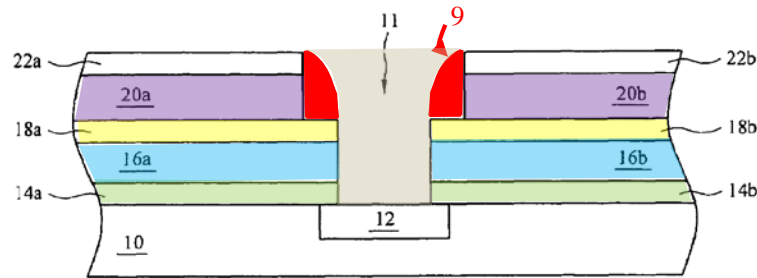
As indicated above by dashed red lines, the opening at the bottom of damascene aperture 11 (the claimed substrate coupling area of said contact region) is smaller than the opening at the top of damascene aperture 11 (the claimed metal layer coupling area of said contact region), meeting **the PO Litigation Construction**. EX1002, ¶130.

Further, as discussed in Section IX.B.3, [red] spacers 9 **control** the width of the opening at the bottom of damascene aperture 11 by “utilizing ... [red] spacers 9 as an etching mask,” meeting **Petitioner’s Construction**. EX1006, 4:57-5:2; *see also id.*, Abstract (stating “spacers” “provide better **control** of a small via”); EX1002, ¶131.

### Limitation 1[d]

Peng-Chien-Brase meet this limitation via the same layers identified in Peng-Chien in Ground 1. *See* §IX.A above. The mapping differs from Ground 1 only in that the multiple etch stop insulation layer is coupled to [tan] dual damascene

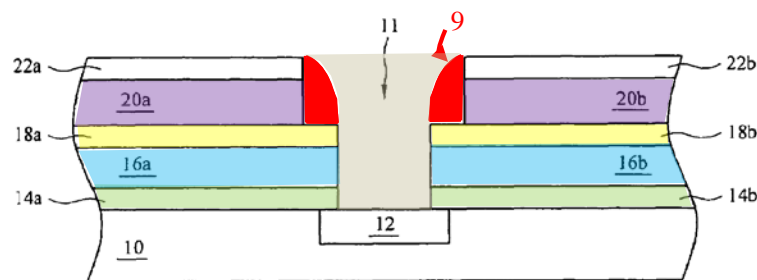
aperture 11 (a) directly by way of all of etch stop layers 18a/18b, dielectric layers 16a/16b, and etch stop layers 14a/14b; and (b) indirectly through [red] spacers 9. See also Ground 1, Limitation 1[d].



EX1003, FIG. 1; EX1002, ¶132.

**Limitation 6:**

Peng-Chien-Brase includes Chien's spacers 9 formed of "silicon nitride." EX1006, 4:25-44; §IX.B.3; EX1002, ¶133. Silicon nitride is an insulating material. EX1002, ¶133. [Red] spacers 9 abut damascene aperture 11, thereby insulating the contact region. *Id.*



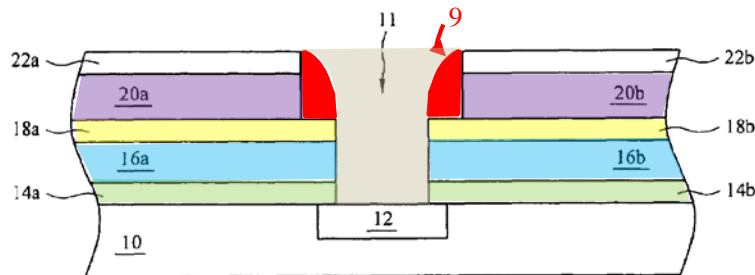
EX1003, FIG. 1.

**Limitation 11[p]: "An integrated circuit"**

See §IX.A, Limitation 1[p].

**Limitation 11[a1]: “a multiple etch stop insulation layer comprising a first etch stop layer and a second etch stop layer wherein said first etch stop layer and said second etch stop layers have similar selectivity characteristics”**

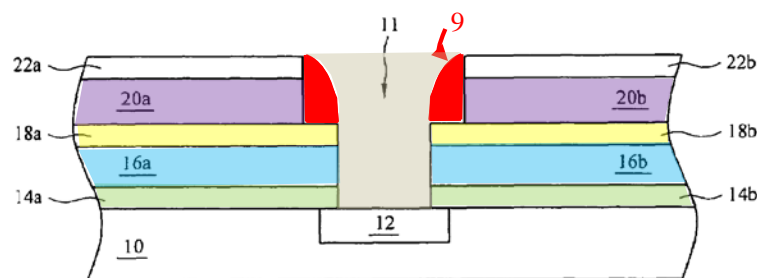
As discussed for Limitation 1[d] in Section IX.A (Ground 1), a [green] “pair of patterned first barrier layers 14a and 14b,” a [blue] “pair of patterned first dielectric layers 16a and 16b,” a [yellow] “pair of patterned etch stop layers 18a and 18b,” and a [purple] “pair of patterned second dielectric layers 20a and 20b” together comprise the claimed multiple etch stop insulation layer. EX1003, 4:24-33, FIG. 2; EX1002, ¶135. As discussed for Limitations 1[d1] and 1[d3] in Section IX.A, [green] “barrier layers 14a and 14b” and [yellow] “etch stop layers 18a and 18b” are the claimed first and second etch stop layers, respectively, and have similar (*i.e.*, the same) etch selectivity. EX1003, FIG. 2, 4:16-23; EX1002, ¶135.



EX1003, FIG. 1.

**Limitation 11[a2]: “said first etch stop layer formed in an area directly next to a substrate corresponding to a contact region and under a first sub interlevel dielectric layer and said second etch stop layer formed under a second interlevel dielectric layer, wherein said first sub interlevel dielectric layer is between said first etch stop layer and said second etch stop layer”**

Peng-Chien-Brase includes Peng’s layers, including [green] “barrier layers 14a and 14b” (the claimed first etch stop layer) directly next to substrate 10 that corresponds to damascene aperture 11 (the claimed contact region). EX1003, FIG. 1; EX1002, ¶136. Peng’s [green] “barrier layers 14a and 14b” are under [blue] “dielectric layers 16a and 16b,” which is the claimed first sub interlevel dielectric layer as explained for Limitation 1[d2] in Section IX.A. *Id.* Peng’s [yellow] “etch stop layers 18a and 18b” (the claimed second etch stop layer) is under [purple] “second dielectric layers 20a and 20b,” which is the claimed second sub interlevel dielectric layer as explained for Limitation 1[d4] in Section IX.A. *Id.* Finally, Peng discloses [blue] “dielectric layers 16a and 16b” are between [green] “barrier layers 14a and 14b” and [yellow] “etch stop layers 18a and 18b.” *Id.*



EX1003, FIG. 1.

**Limitation 11[a3]: “wherein said multiple etch stop insulation layer is formed utilizing a lithography process”**

Peng-Chien-Brase would include forming Peng’s dual-damascene aperture 11 via Chien’s process. *See* §IX.B.3. Chien discloses forming a trench portion of the dual damascene aperture using “photolithographic processes” to remove a portion of the top etch stop layer and insulating layer, corresponding to dielectric layer 20 in Peng, which is part of the multiple etch stop insulation layer. EX1006, 4:10-24, FIGS. 2b-2c; EX1003, 4:16-23, FIG. 1, EX1002, ¶137.

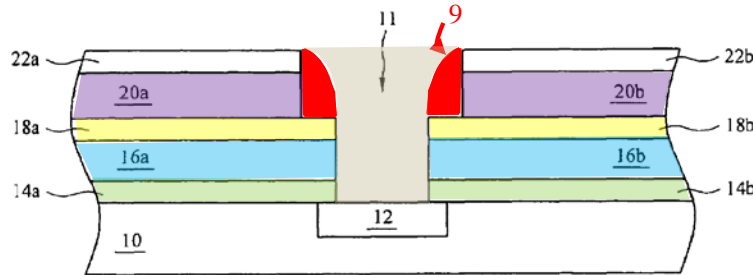
**Limitation 11[b1]: “a contact region in said multiple etch stop insulation layer”**

*See* §IX.A, Limitation 1[b].

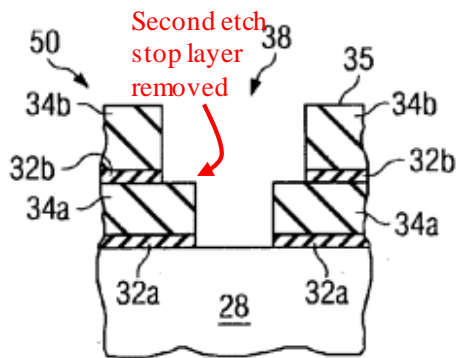
**Limitation 11[b2]: “wherein creating of said contact region includes forming sub-spacer regions in removed portions of said second sub interlevel dielectric layer and said second etch stop layer”**

Peng-Chien-Brase renders obvious this limitation. As discussed in §IX.B.3, forming Peng’s dual damascene aperture using Chien’s process includes forming [red] spacers 9 (the claimed sub-spacer regions) in removed layers that define a trench opening. EX1006, 4:10-24, FIGS. 2b-2c; EX1003, 4:16-23, FIG. 1, EX1002, ¶139. In Peng, the trench opening is formed by removing portions of dielectric layer

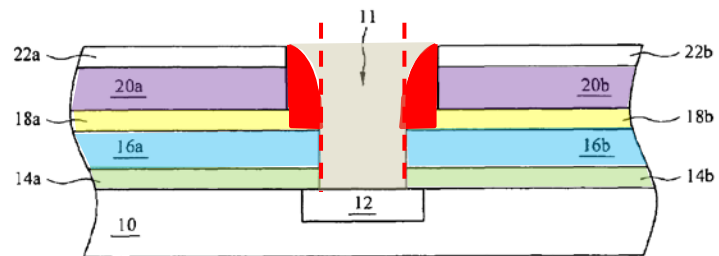
20 (the claimed second dielectric layer), but not etch stop layer 18 (the claimed second etch stop layer).



EX1003, 4:16-23, FIG. 1; EX1002, ¶139. However, it was also known to form a trench opening in a dual damascene aperture through the etch stop layer between two dielectric layers. EX1002, ¶¶140-41 (citing EX1004, FIG. 12, ¶[0033]).



**EX1004, FIG. 12**



**EX1003, FIG. 1  
(modified per Lin)**

It would have been an obvious design choice to form the trench opening in Peng, and subsequently spacers 9 by also removing a portion of etch stop layer 18. *Id.*, ¶141; EX1004, FIG. 12, ¶[0033]. A POSITA would have understood that because

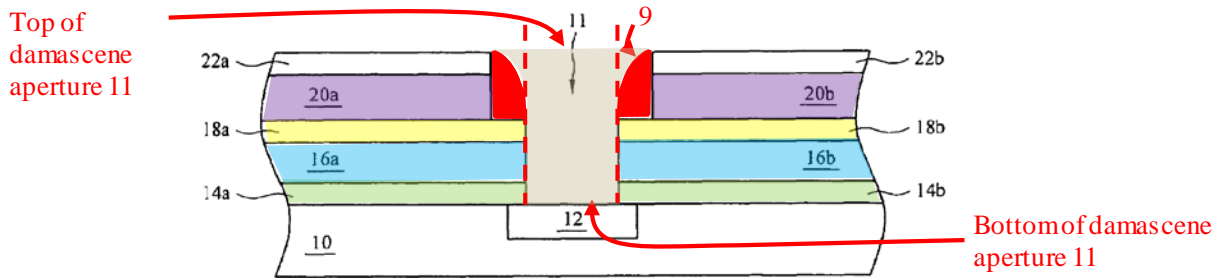
spacers 9 serve as a mask for etching the via opening, etch stop layer 18 is not needed for etching the via hole. EX1002, ¶142; *see also* EX1004, ¶[0033].

**Limitation 11[b3]: “wherein a non-lithography spacer formation process is also utilized to achieve a contact bottom such that a substrate coupling area of said contact region is smaller than a metal layer coupling area of said contact region”**

Peng-Chien-Brase would include forming Peng’s dual-damascene aperture 11 via Chien’s process. *See* §IX.B.3. Chien discloses forming [red] “second conductive line spacers 9” on the sidewalls of the trench opening by “depositing a layer of conformal silicon nitride” and then etching to remove the horizontal portions. EX1006, 4:25-44, FIG. 2d; EX1002, ¶143. A POSITA would have understood that forming spacers from a conformal layer uses a non-lithographic formation process using anisotropic etch, as Peng explicitly describes. EX1002, ¶143; EX1003, 4:43-46 (describing “deposition and anisotropic etch method as is otherwise generally conventional” for forming sidewalls).

As discussed in Section IX.B.3, the fabrication process “utiliz[es]” [red] spacers 9 “as an etching mask” to etch to the substrate as indicated below by the dotted lines, thereby achieving a contact bottom. EX1006, 4:57-5:2; *see also id.*, Abstract (stating “spacers” “provide better *control* of a small via”); EX1002, ¶144. As can be seen below, the opening at the bottom of damascene aperture 11 (the

claimed substrate coupling area of said contact region) is smaller than the opening at the bottom of damascene aperture 11 (the claimed metal layer coupling area of said contact region).



EX1003, FIG. 1; EX1002, ¶144.

**Limitation 12:** “wherein said first etch stop layer is in a range of about 300 to 800 Å thick, said first sub interlevel dielectric layer is in a range of about 1,000 to 2,000 Å thick, said second etch stop layer is in a range of about 300 to 800 Å thick and said second sub interlevel dielectric layer is in a range of about 10K Å±1K Å thick”

See §IX.A, Limitation 8.

### C. Ground 3 – Lin-Chien Renders Obvious Claims 1-7 & 11

Ground 3 presents an additional mapping based on Lin, which has a substantially earlier priority date, and would not be subject to the same antedating challenges as Peng. Ground 3 is also not cumulative of Ground 2 because Lin provides additional disclosure of multiple elements that would overcome any

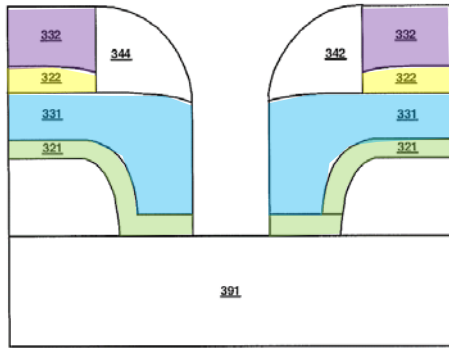


challenge to Peng. For example, for Limitation 1[d1] in Grounds 1 and 2, the Petition explains that a POSITA would understand that Peng's "barrier layer" 14 functions as etch stops and therefore is the claimed "first etch stop layer." To the extent Patent Owner challenges this understanding, in Ground 3 the Petition maps the claimed "first etch stop layer" to Lin's "*etch stop layer 32a*." As another example, for Limitation 11[b2] in Ground 2, the Petition explains that it was obvious to modify Peng to remove a portion of etch stop layer 18 (the claimed second etch stop layer) as part of the trench opening. To the extent Patent Owner challenges this assertion, Lin explicitly discloses forming an upper trench opening by removing portions of dielectric layer 34b (the claimed second dielectric layer) *and etch stop layer 32b* (the claimed second etch stop layer).

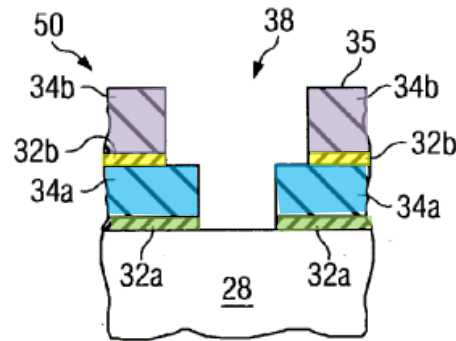
### ***1. Lin***

Lin discloses a "dual damascene procedure for forming a contact opening" for use in "manufacturing a semiconductor device." EX1004, ¶¶[0003], [0022], [0033]. Lin uses the same layers in the same sequence as the '797 Patent's claimed "multiple etch stop insulation layer," including (1) a [green] "first SiC etch stop layer 32a" (the claimed first etch stop layer), (2) a [blue] "first low-k dielectric layer 34a" (the claimed first sub interlevel dielectric layer), (3) a [yellow] "second SiC etch stop layer 32b" (the claimed second etch stop layer), and (4) a [purple] "second low-k dielectric layer 34b" (the claimed second sub interlevel dielectric layer) surrounding

“contact opening 38” exposing a portion of “underlying layer 28.” Compare EX1004, ¶[0033], FIG. 12 with EX1001, FIG. 3E; EX1002, ¶146.



**EX1001, FIG. 3E**



**EX1004, FIG. 12**

Lin further discloses “underlying layer 28 may be ... a substrate having highly doped regions (source, drain)” or “a substrate layer having electrical components formed therein (e.g., transistors, capacitors, resistors, diodes, etc.). EX1004, ¶[0027]. A POSITA would have understood that opening 38 in such a structure exposes the source/drain region. EX1002, ¶147. Further, while shown in FIG. 12 as an opening, Lin discloses that “[t]he trenches and contact vias can then be filled with a conducting material, preferably copper.” *Id.*, ¶¶[0046]-[0047]. And, “more than one layer of metallization may be included” such that the top of contact opening 38 couples to a higher layer of metallization. *Id.*, ¶[0048].

## **2. Motivation to Combine**

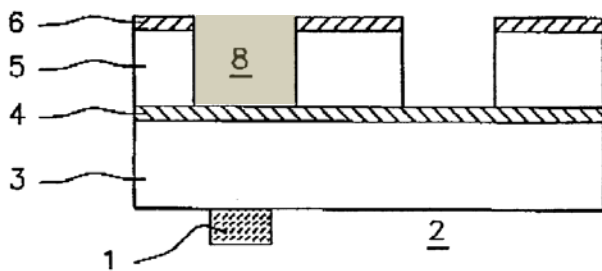
A POSITA would have been motivated to utilize the dual damascene formation process of Chien in forming Lin’s contact opening 38 for the same reasons

as described for utilizing Chien to form Peng's aperture 11, as discussed in §IX.B.2 above. EX1002, ¶¶117-21, 148.

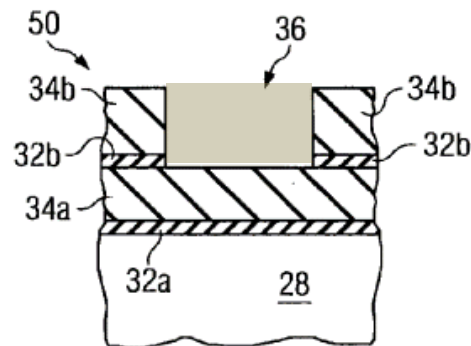
### 3. *Modification of Lin in view of Chien*

A POSITA would utilize Chien's dual-damascene formation process to form Lin's opening 38. EX1002, ¶148.

Chien discloses first using "photolithographic processes" to "form a second line opening 8," which is the [tan] trench opening. EX1006, 4:10-24, FIGs. 2b-2c. Applying this disclosure to Lin entails using "photolithographic processes" to etch a portion second low-k dielectric layer 34b and etch stop layer 32b to form the [tan] trench opening "first opening 36." EX1004, ¶[0033], FIG. 10; EX1002, ¶149.



**EX1006, FIG. 2c**

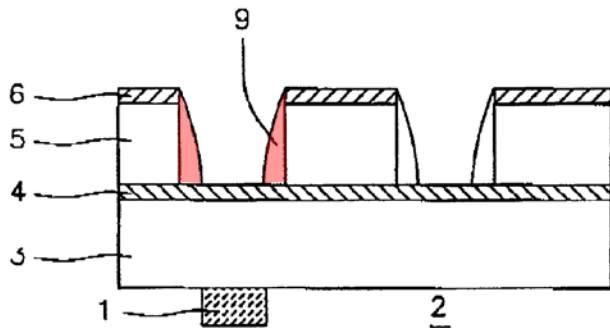


**EX1004, FIG. 10**

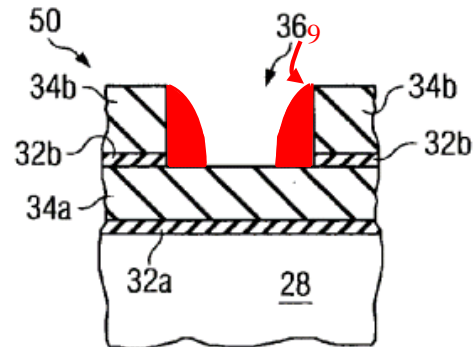
Chien discloses next forming [red] "second conductive line spacers 9" on the sidewalls of the trench opening by "depositing a layer of conformal silicon nitride" and then etching to remove the horizontal portions. EX1006, 4:25-44, FIG. 2d; EX1002, ¶150. Applying this disclosure to Lin entails forming [red] silicon nitride

spacers on the sidewalls of second low-k dielectric layer 34b and etch stop layer 32b.

EX1004, FIG. 10, EX1002, ¶150.

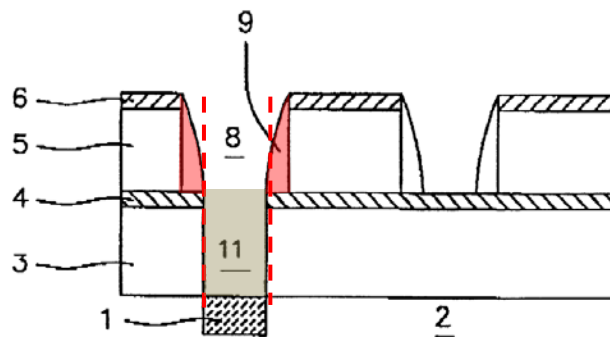


**EX1006, FIG. 2d**

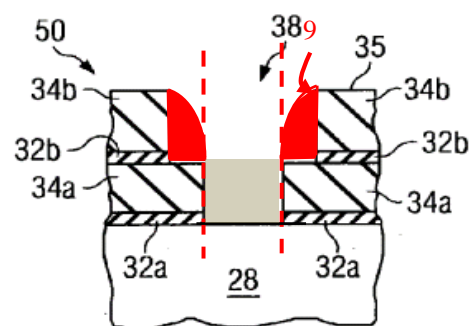


**EX1004, FIG. 10  
(modified per Chien)**

Chien discloses finally forming a [tan] “via hole 11” to the substrate by etching the remaining layers by “utilizing” “the [red] second conductive line spacers 9 as an etching mask” as indicated by the dotted red lines. EX1006, 4:57-5:2; EX1002, ¶151. Applying this disclosure to Lin entails etching first low-k dielectric layer 34a and etch stop layer 32a to form a [tan] via hole to the substrate in contact opening 38. EX1004, FIG. 12, EX1002, ¶151.



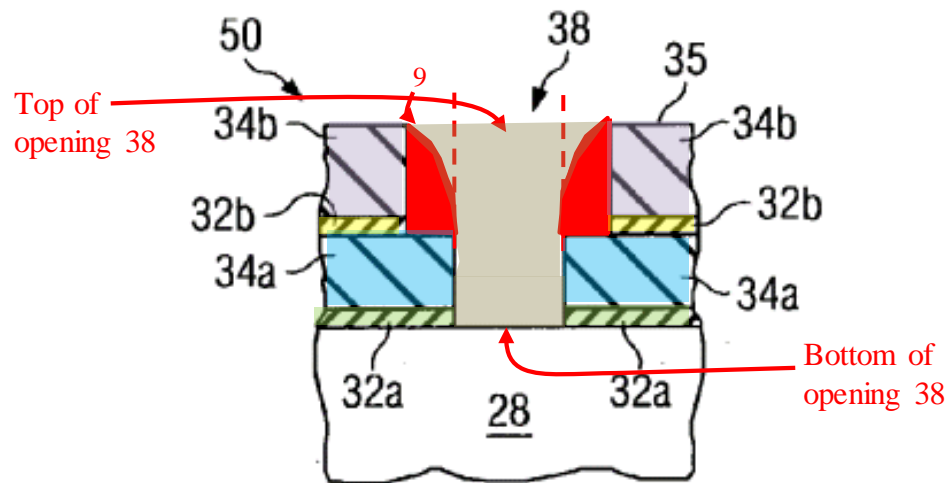
**EX1006, FIG. 2f**



**EX1004 (Lin), FIG. 12**

(modified per Chien)

Because Chien, like Lin, discloses a dual damascene aperture, the modification leaves [tan] contact opening 38 consistent with Lin's disclosures, along with spacers on the sidewalls of the trench.



EX1004, FIG. 12; EX1002, ¶152. The opening at the top of contact opening 38 remains wider than the opening at the bottom of contact opening 38 based on the curve of [red] spacers 9. EX1002, ¶152. This is consistent with Chien, which describes an exemplary “width of the second conductive line opening 8” (the top of the damascene opening) as 0.2  $\mu\text{m}$  with a corresponding “size of the via hole 11” (the bottom of the damascene opening) as 0.18  $\mu\text{m}$ . EX1006, 5:31-36.

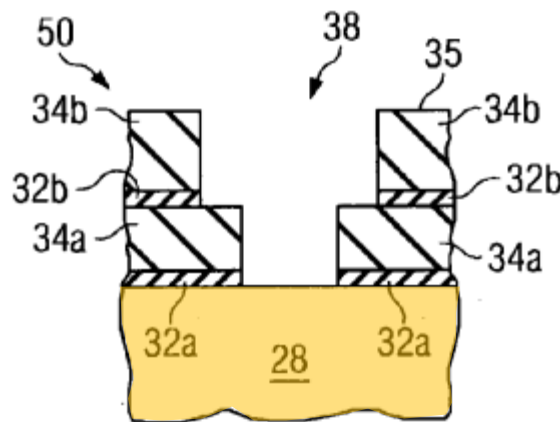
#### 4. *Element-by-element Analysis*

##### **Limitation 1[p]<sup>8</sup>**

Lin modified by Chien discloses this limitation. Lin describes that dual damascene processes “are useful in small sized semiconductor technologies” such as “*an integrated circuit* that includes transistors 64 and 66.” EX1004, ¶[0038].

##### **Limitation 1[a]:**

Lin describes a “dual damascene procedure for forming a contact opening” 38 to “an underlying layer 28.” EX1004, ¶[0033]. The [orange] underlying layer may be “a substrate having highly doped regions (source, drain).” EX1004, ¶[0027].



EX1004, FIG. 12, ¶[0027].

A POSITA would have understood that such highly doped regions, such as a source or drain, are “electrical wells” provided in a substrate. EX1002, ¶155 (citing

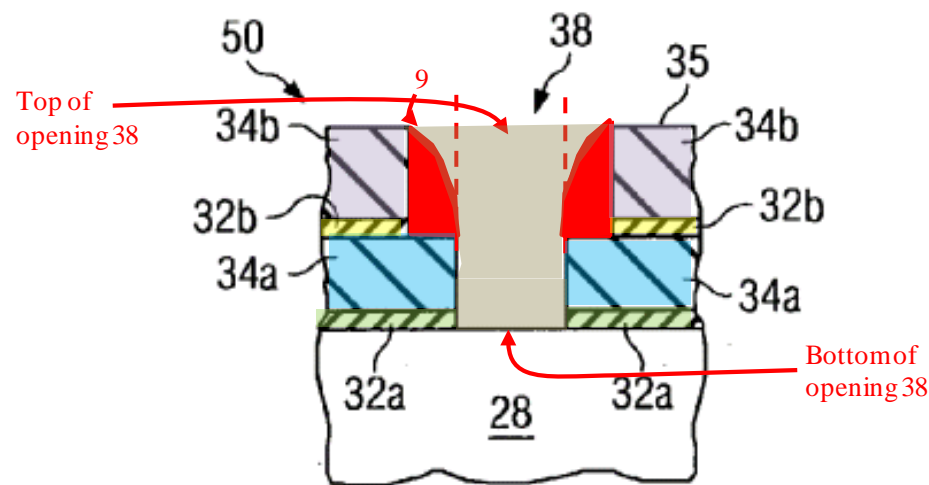
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<sup>8</sup> See §IX.A.5 for the text of claim limitations also addressed in Ground 1.

EX1011, 34/170). A doped region in a semiconductor device is a portion of the substrate with additional p-type or n-type material to create an electrical well of charge carriers that move to produce the electrical current through the device. *Id.* (citing EX1011, 108/170).

### **Limitation 1[b]**

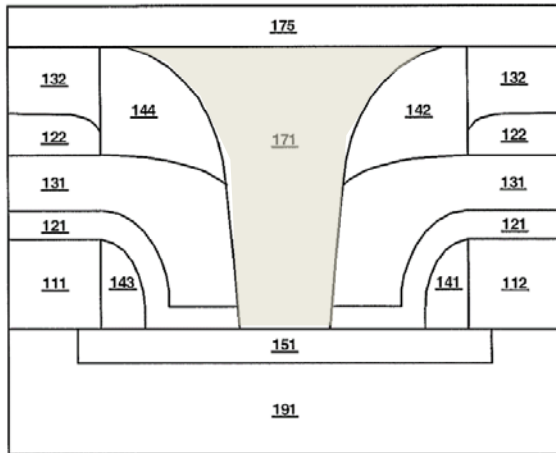
Lin modified by Chien discloses this limitation. Lin's [tan] "opening 38" (the claimed contact region) exposes a region of the underlying layer 28, which may be a substrate with source and drain regions or n-wells. EX1004, ¶¶[0027]; [0033]; [0037].



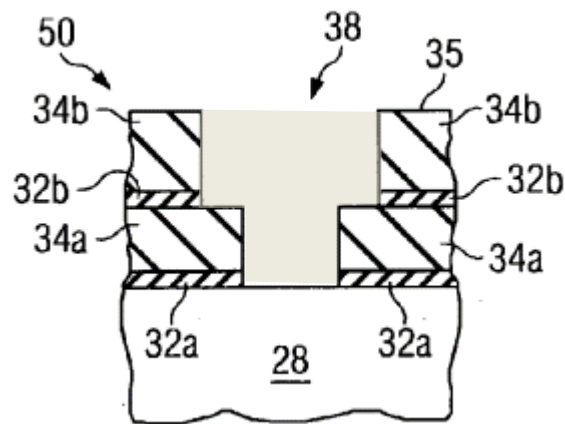
EX1004, FIG. 12; EX1002, ¶156.

[Tan] opening 38 is coupled to the substrate because it exposes the underlying layer 28, which is the substrate. EX1004, ¶¶[0027], [0033], FIG 12; EX1002, ¶157. This mapping matches the '797 Patent, which states, in describing FIG. 1B,

“[c]ontact region 171 is coupled to substrate 191.” EX1001, 3:66-4:16. As can be seen in FIG. 1B below, contact region 171 is in contact with source/drain region 151 within substrate 191.



**EX1001, FIG. 1B**



**EX1004, FIG. 12**

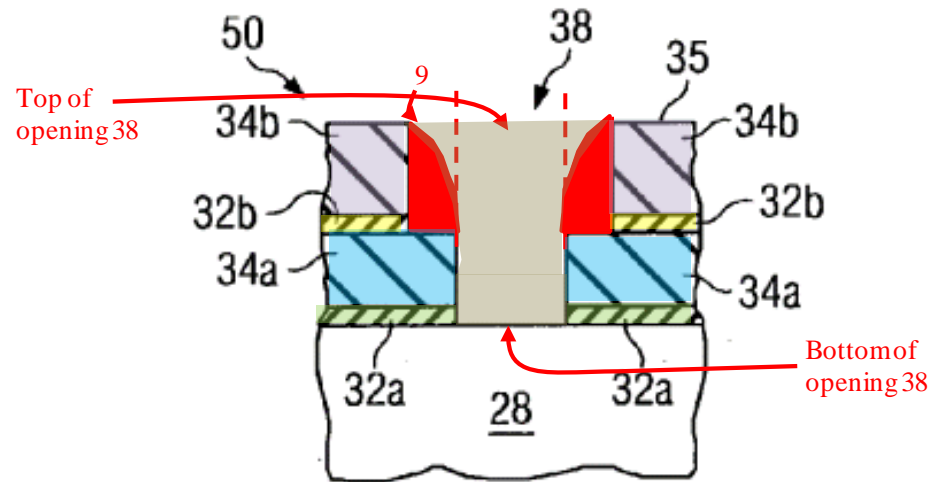
Finally, opening 38 is filled with “conducting material (e.g., 94a)” and “polished back so that a top surface 95a of the conducting material 94a is substantially planar with the top surface 35a of the dielectric layer 34a,” establishing an electrical path to and from the substrate. EX1004, ¶[0047]; FIG. 17; EX1002, ¶158.

### **Limitation 1[c]**

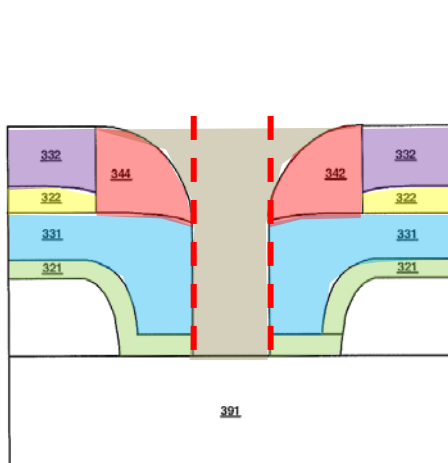
Lin modified by Chien discloses this limitation under either of **Petitioner’s Construction** or the **PO Litigation Construction**. See §VIII.C.3. Lin-Chien



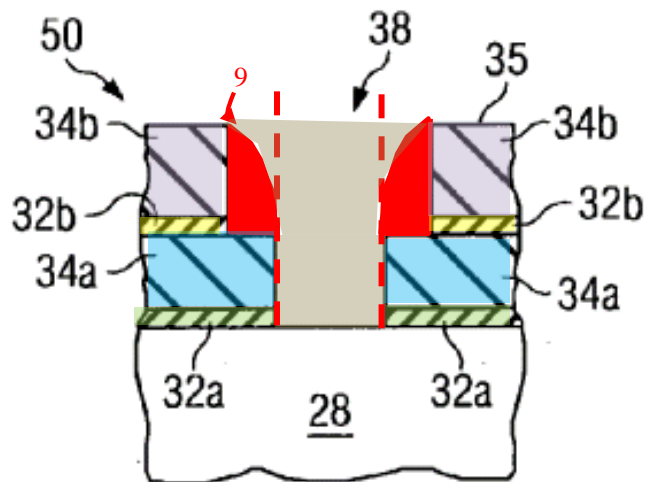
includes [red] spacers 9 on the sidewalls of the trench opening of opening 38 as explained in Section IX.C.3.



EX1004, FIG. 12; EX1002, ¶159.. This arrangement matches the '797 Patent.



**EX1001, FIG. 3E**



**EX1004, FIG. 12**

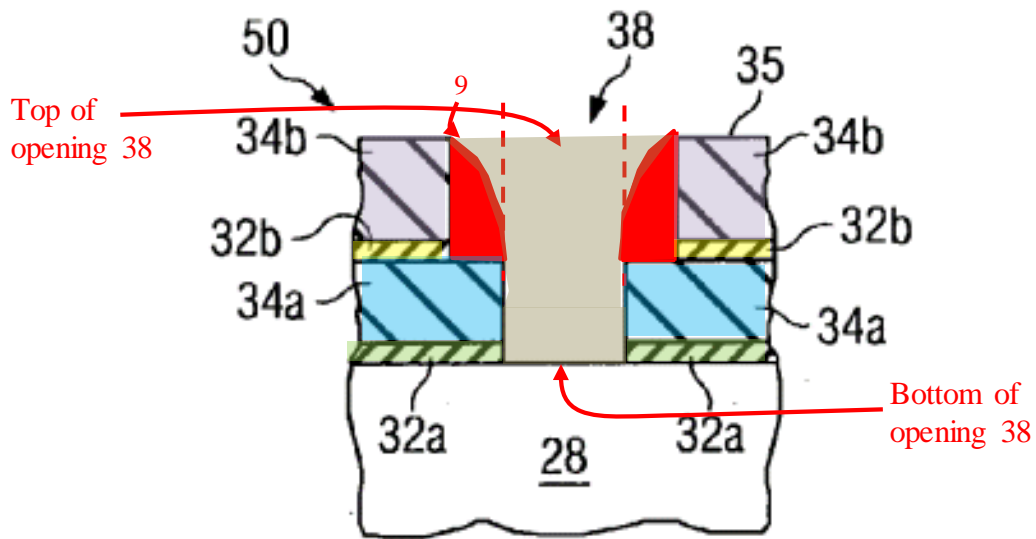
As indicated by the dashed red lines, the area at the bottom of opening 38 (the claimed substrate coupling area of said contact region) is smaller than the area at the top of opening 38 (the claimed metal layer coupling area of said contact region),

meeting the **PO Litigation Construction**. EX1004, FIG. 12; EX1006, FIG. 2f; EX1002, ¶160.

Further, as discussed in §IX.C.3, [red] spacers 9 *control* the bottom of opening 38 by “utilizing” “the [red] second conductive line spacers 9 as an etching mask,” meeting **Petitioner’s Construction**. EX1006, 4:57-5:2; *see also id.*, Abstract (stating “spacers” “provide better *control* of a small via”); EX1002, ¶161.

### **Limitation 1[d]**

Lin discloses a stack of insulating layers formed on underlying layer 28 (a substrate) including (1) a [green] “first SiC etch stop layer 32a” (the claimed first etch stop layer), (2) a [blue] “first low-k dielectric layer 34a” (the claimed first sub interlevel dielectric layer), (3) a [yellow] “second SiC etch stop layer 32b” (the claimed second etch stop layer), and (4) a [purple] “second low-k dielectric layer 34b” (the claimed second sub interlevel dielectric layer). EX1004, ¶[0033].

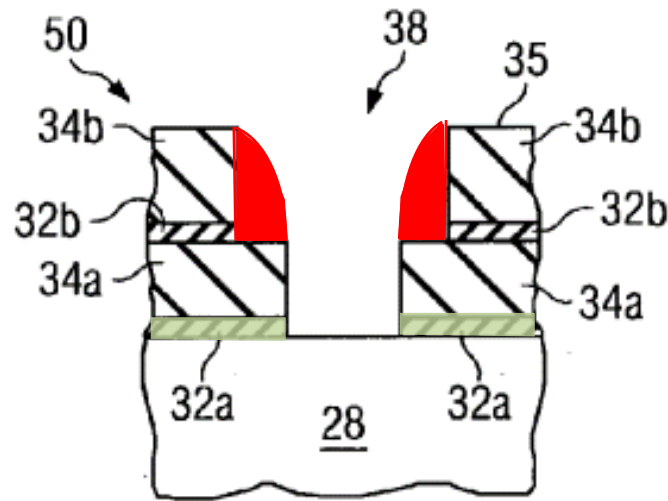


EX1004, FIG. 12; EX1002, ¶162.

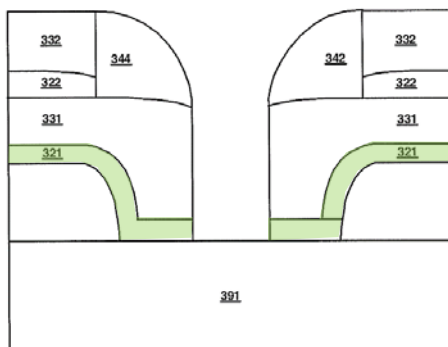
These layers are coupled to a [tan] opening 38 (the claimed contact region) (a) directly by way of dielectric layer 34a and etch stop layer 32a, and (b) indirectly through [red] spacers 9. EX1004, FIG. 12; EX1002, ¶163. These layers provide electrical insulation between other regions of said integrated circuit and isolates guidance of electrical current flow in said contact region because each of the layers is a dielectric layer. EX1004, ¶[0033]; EX1002, ¶163. Specifically, Lin discloses that layers 32a and 32b are SiC, and layers 34a and 34b are “any of a variety of dielectric materials.” EX1004, ¶¶[0033], [0026]. A POSITA would have understood that dielectric materials and SiC are insulating materials. EX1002, ¶163.

**Limitation 1[d1]**

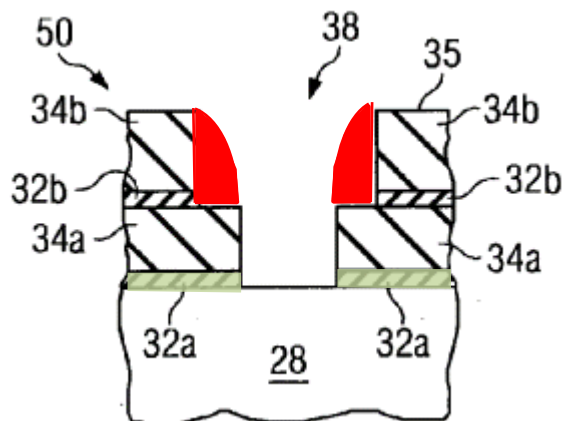
Lin describes [green] “first SiC etch stop layer 32a.”



EX1004, ¶[0033], FIG. 12; EX1002, ¶164. Etch stop layer 32a is directly on the substrate. EX1004, ¶[0033], FIG. 12; EX1002, ¶165. Further, etch stop layer 32a is “on said substrate in said contact region” to the same degree as the ’797 Patent, which illustrates etch stop layer 321 patterned around the contact region.



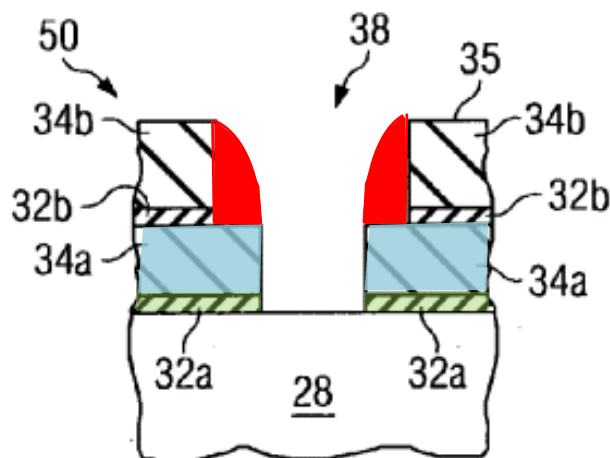
**EX1001, FIG. 3E**



**EX1004, FIG. 12**

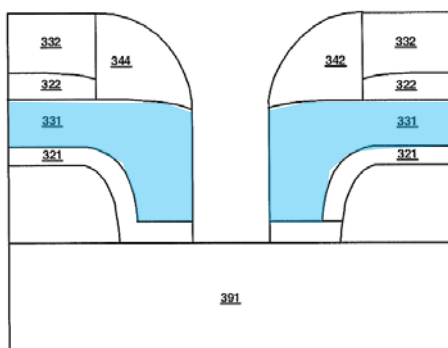
### Limitation 1[d2]

Lin discloses a [blue] “first low-k dielectric layer 34a” (the claimed first sub interlevel dielectric layer) over the [green] etch stop layer 32a (the claimed first etch stop layer).

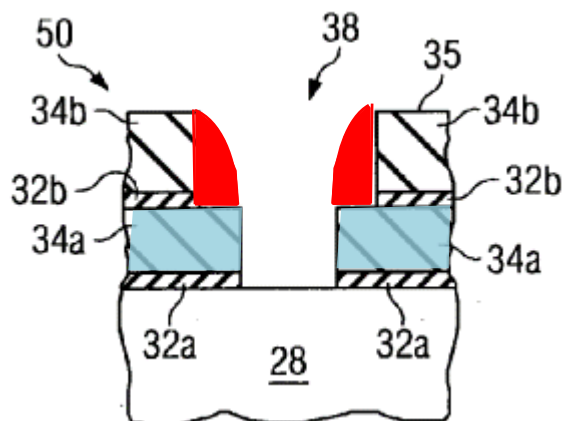


EX1004, FIG. 12; EX1002, ¶166.

Dielectric layer 34a matches the '797 Patent's [blue] sub interlevel dielectric layer 331. EX1002, ¶167.



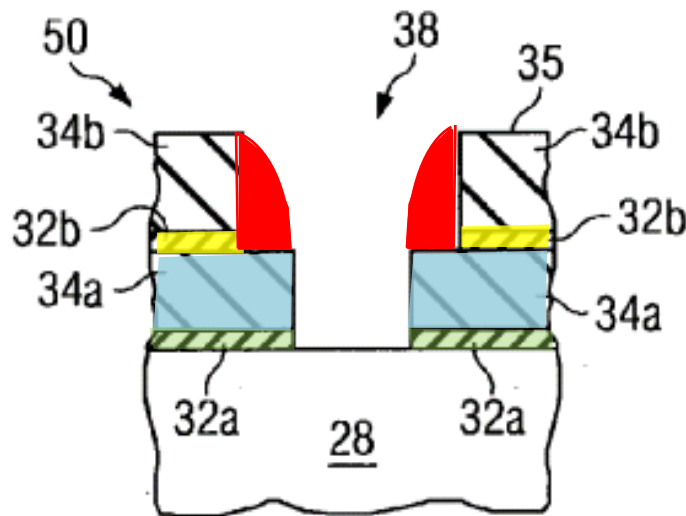
**EX1001, FIG. 3E**



**EX1004 (Peng), FIG. 12**

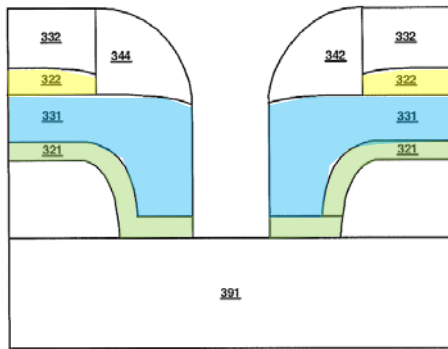
**Limitation 1[d3]**

Lin discloses [yellow] “second SiC etch stop layer 32b” over [blue] dielectric layer 34a (the claimed first sub interlevel dielectric layer). .

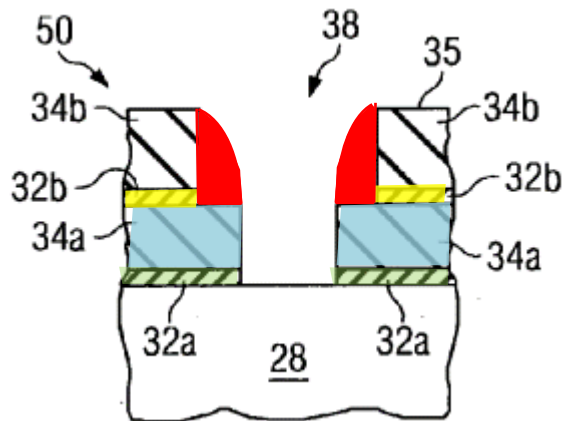


EX1004, ¶[0033], FIG. 12; EX1002, ¶168. Lin describes that the etch stop layer 32a and 32b are both SiC materials. *Id.* By selecting the same material for the two layers, the layers will necessarily have identical etch selectivities. EX1002, ¶168.

Further, [blue] dielectric layer 34a (the claimed first sub interlevel dielectric layer) is between the first [green] etch stop layer 32a and [yellow] etch stop layer 32b. EX1004, FIG. 12; EX1002, ¶169. Again, the arrangement of these layers matches the '797 Patent.



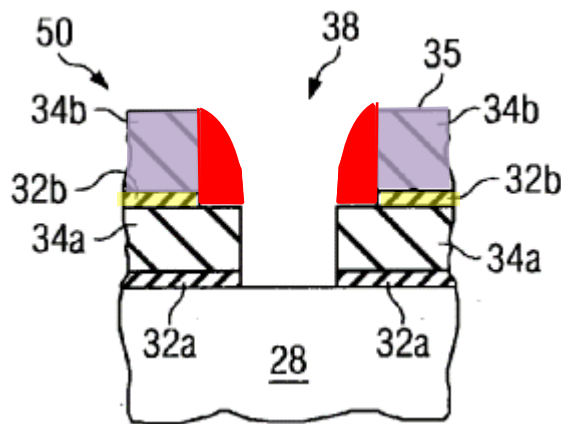
EX1001, FIG. 3E



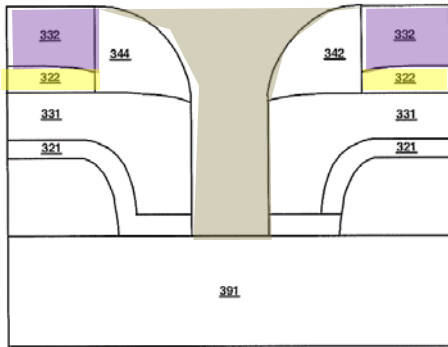
EX1004, FIG. 12

### Limitation 1[d4]

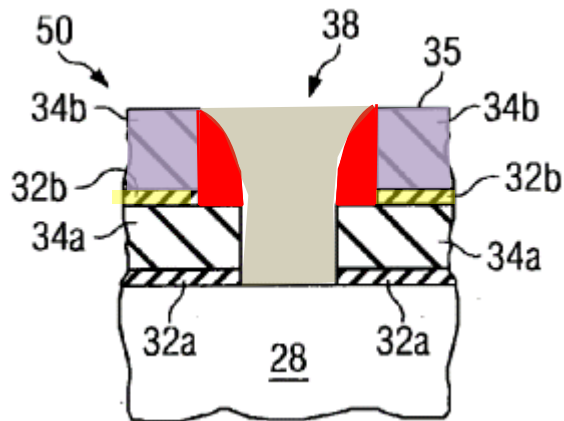
Lin discloses [purple] “second low-k dielectric layer 34b” (the claimed second sub interlevel dielectric layer) over [yellow] etch stop layer 32b (the claimed second etch stop layer). EX1004, ¶[0033]; EX1002, ¶170.



EX1004, FIG. 12; EX1002, ¶170. Again, the arrangement of these layers matches the '797 Patent.



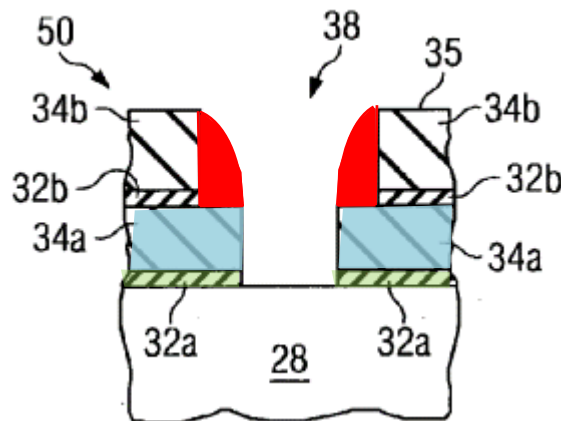
**EX1001, FIG. 3E**



**EX1004 (Lin), FIG. 12**

## Limitation 2

Lin modified by Chien discloses this limitation. [Green] etch stop layer 32a protects removal of a substrate by an etch process based on its position and function.



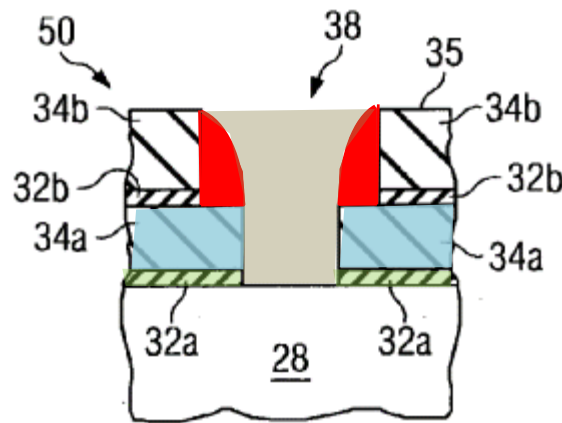
EX1004, FIG. 12; EX1002, ¶171. Lin discloses etching the dielectric layer “using an etch chemistry that is selective against etching SiC”—the material layer 32a—such that layer 32a “acts as an etch stop layer.” EX1004, ¶[0028]. By serving as an etch stop layer arranged between layer 34a and underlying layer 28 (the substrate),



a POSITA would have understood that etch stop layer 32a protects against removal of a substrate material during etching of the dielectric layer 34a. EX1002, ¶171.

### **Limitation 3**

As discussed for Limitation 1[d1], [blue] dielectric layer 34a (the claimed first sub interlevel dielectric layer) is an insulating material that surrounds, and thus insulates, the [tan] contact region.

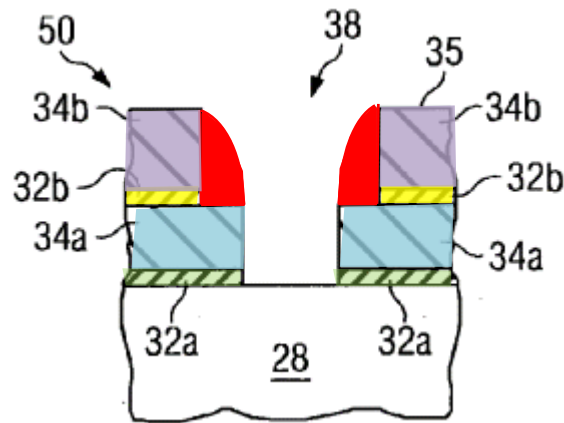


EX1004, FIG. 12; EX1002, ¶172.

### **Limitation 4**

Lin modified by Chien discloses this limitation. [Yellow] etch stop layer 32b (the claimed second etch stop layer) protects [blue/green] lower layers during an etch process based on its position and function. EX1002, ¶173. Lin discloses etching the dielectric layer “using an etch chemistry that is selective against etching SiC” used for [yellow] etch stop layer 32b such that it “acts as an etch stop layer.” EX1004,

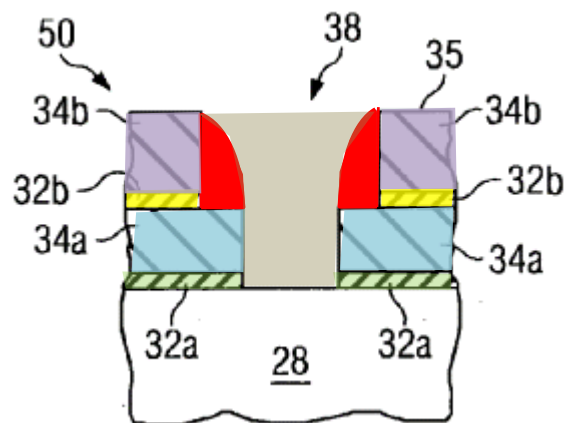
¶¶[0028], [0033]; EX1002, ¶173. By serving as an etch stop, [yellow] etch stop layer 32b protects layers below.



EX1004, FIG. 12; EX1002, ¶173.

### Limitation 5

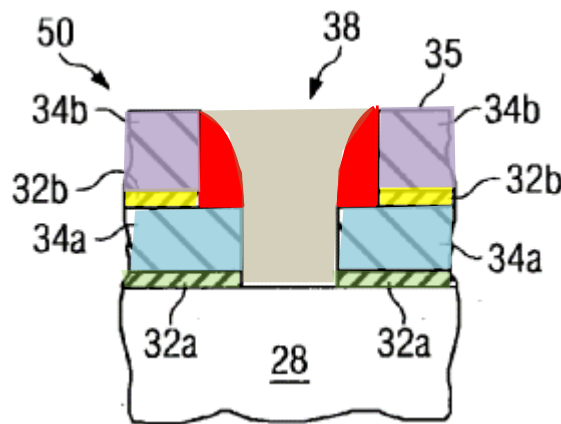
As discussed for Limitation 1[d1], [purple] dielectric layer 34b (the claimed second sub interlevel dielectric layer) is an insulating material that surrounds, and thus insulates, the [tan] contact region. EX1004, ¶[0033], FIG. 12; EX1002, ¶174.



EX1004, FIG. 12; EX1002, ¶174.

### Limitation 6

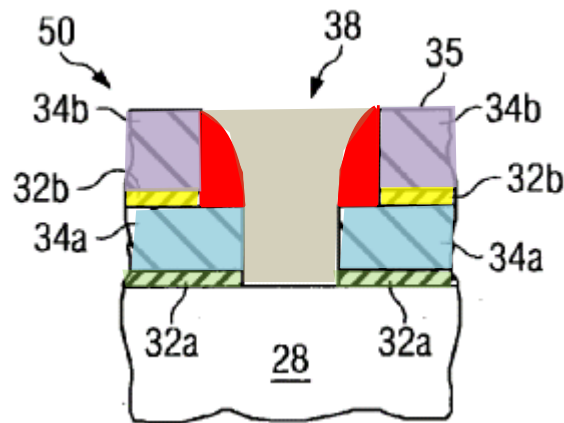
Lin modified by Chien discloses this limitation. Chien discloses that [red] spacers 9 are made of silicon nitride, which a POSITA would have understood is an insulating material. EX1006, 4:25-39; EX1002, ¶175. [Red] spacers 9 surround the [tan] contact region, and thus insulate it.



EX1004, FIG. 12; EX1002, ¶175.

### Limitation 7

Lin-Chien renders obvious this limitation. The '797 Patent does not describe this claim limitation as a separate structural or functional element, but rather as a benefit flowing from the relative sizes of the top and bottom coupling areas of the contact region already recited in Limitation 1[c]. EX1001, 4:39-49. Thus, this element is met based on the shape of opening 38 demonstrated for Limitation 1[c] and shown below.



EX1004, FIG. 12; EX1002, ¶176.

First, as discussed in Section VI.A, integrated circuits include rows of repeated gate and source/drain regions making up transistors. Minimizing the width between successive gates maximizes density. EX1002, ¶177. Each of the gates includes an accompanying source/drain region. *Id.*; EX1004, FIG. 17. Those source/drain regions are located between successive gates. EX1002, ¶177. Contacts are formed to those source/drain regions to electrically couple the transistors. EX1002, ¶177; EX1005, FIG. 6. One contributing factor to the ability to reduce width between successive gates is the space needed for contact to the source/drain regions that are located around each of the gates. EX1002, ¶177; EX1019, 73/112. The contact to the source/drain regions is through the damascene aperture 11 as described in §IX.A.4. EX1002, ¶78. Thus, a POSITA would have understood that the relatively small substrate coupling area of opening 38 permits multiple active regions, specifically gate regions of consecutive transistors, to be arranged relatively

close to one another (as compared to designs with larger substrate coupling areas that would require gate regions to be placed farther apart). EX1002, ¶177; *compare to* EX1001, 4:45-47.

Second, as described in Section IX.C.1, the top of opening 38 couples to a higher layer of metallization. EX1002, ¶178; EX1004, ¶¶[0046]-[0048]. A POSITA would have understood that the larger coupling area the top of opening 38 is fully aligned with the contacting metal above, resulting in a higher likelihood that the contact to the substrate that is formed has a contact area greater than a minimum desired contact area, referred to as a critical dimension, for conducting electrical signals. EX1002, ¶178; EX1008, 233/269; *compare to* EX1001, 4:47-49.

**Limitation 11[p]**<sup>9</sup>

See Limitation 1[p].

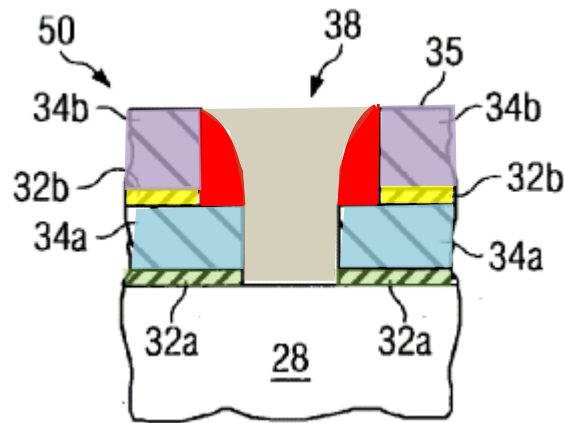
**Limitation 11[a1]**

As discussed for Limitation 1[d], [green] etch stop layer 32a, [blue] dielectric layer 34a, [yellow] etch stop layer 32b, and [purple] dielectric layer 34b comprise the claimed multiple etch stop insulation layer. EX1004, ¶[0033], FIG. 12; EX1002, ¶180. As discussed for Limitations 1[d1] and 1[d3], [green] etch stop layer 32a and

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<sup>9</sup> See §IX.B.4 for the text of claim limitations also addressed in Ground 2.

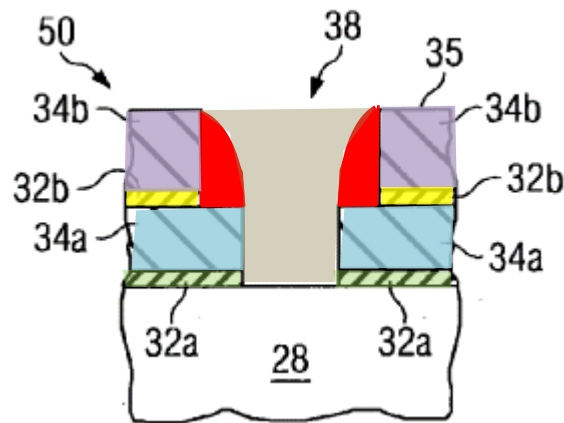
[yellow] etch stop layer 32b are the claimed first and second etch stop layers, respectively, and have similar (*i.e.*, the same) etch selectivity.



EX1004, FIG. 12, ¶[0033]; EX1002, ¶180.

#### **Limitation 11[a2]**

Lin discloses [green] etch stop layer 32a (the claimed first etch stop layer) directly next to underlying layer 28 (a substrate) corresponding to opening 38 (the claimed contact region). EX1004, ¶[0033], FIG. 12; EX1002, ¶181. Lin discloses [green] etch stop layer 32a is under [blue] dielectric layer 34a, which is the claimed first sub interlevel dielectric layer as explained for Limitation 1[d2]. *Id.* Lin further discloses [yellow] etch stop layer 32b (the claimed second etch stop layer) is under [purple] dielectric layer 34b, which is the claimed second sub interlevel dielectric layer as explained for Limitation 1[d4]. *Id.* Finally, Lin discloses [blue] dielectric layer 34b is between [green] etch stop layer 32a and [yellow] etch stop layer 32b. *Id.*



EX1004, FIG. 12.

**Limitation 11[a3]**

Lin-Chien utilizes Chien's formation process. *See* §IX.C.3 above. Chien discloses forming the trench portion of the dual damascene aperture using "photolithographic processes" to remove a portion of the top etch stop layer and insulating layer, corresponding to dielectric layer 20 in Peng, which is part of the multiple etch stop insulation layer. EX1006, 4:10-24, FIGS. 2b-2c; EX1004, ¶[0033], FIG. 12; EX1002, ¶¶182.

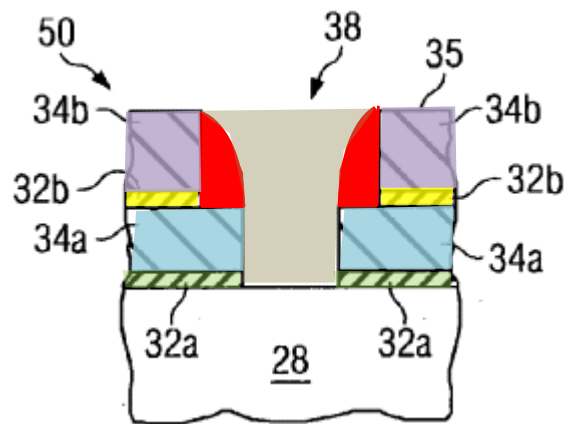
**Limitation 11[b1]**

See Limitation 1[b].

**Limitation 11[b2]**

As discussed in §IX.C.3, forming Lin's dual damascene aperture using Chien's process includes forming [red] spacers 9 (the claimed sub-spacer regions) in removed layers forming a trench opening. EX1006, 4:10-24, FIGS. 2b-2c;

EX1004, ¶[0033], FIG. 12; EX1002, ¶¶184. In Lin, the upper trench opening is formed by removing portions of dielectric layer 34b (the claimed second dielectric layer) and etch stop layer 32b (the claimed second etch stop layer).



EX1004, FIG. 12; EX1002, ¶184.

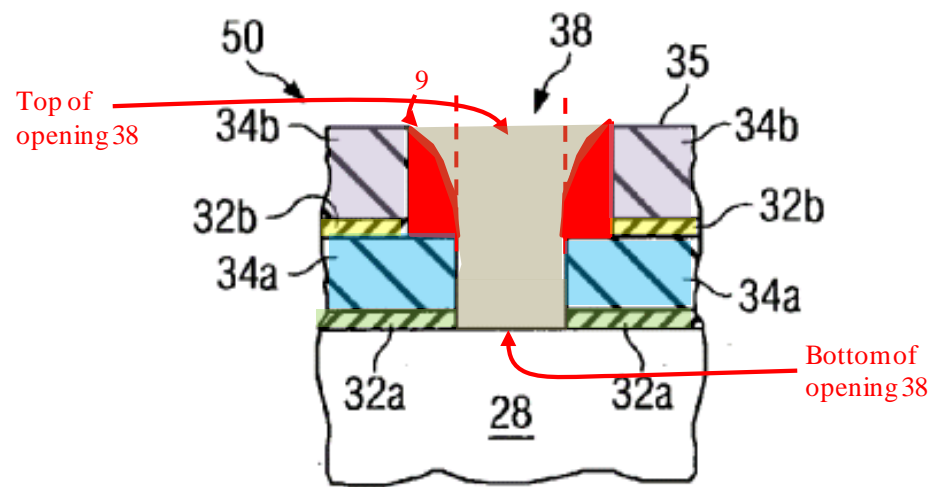
### **Limitation 11[b3]**

As discussed in Section IX.C.3, Chien discloses forming [red] “second conductive line spacers 9” on the sidewalls of the trench opening by “depositing a layer of conformal silicon nitride” and then etching to remove the horizontal portions. EX1006, 4:25-44, FIG. 2d; EX1002, ¶185. A POSITA would have understood that forming spacers from a conformal layer is a non-lithographic formation process using anisotropic etch, as Chien describes. EX1002, ¶185; EX1006, 4:25-44.

As discussed in Section IX.C.3, the fabrication process “utiliz[es]” [red] spacers 9 “as an etching mask” to etch to the substrate as indicated by the dotted



lines, thereby achieving a contact bottom. EX1006, 4:57-5:2; *see also id.*, Abstract (stating “spacers” “provide better *control* of a small via”); EX1002, ¶186. As illustrated below, the bottom of opening 38 (the claimed substrate coupling area of said contact region) is smaller than the top of opening 38 (the claimed metal layer coupling area of said contact region).



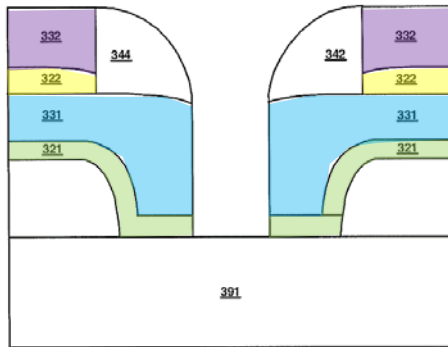
EX1004, FIG. 12; EX1002, ¶186.

#### D. Grounds 4-6

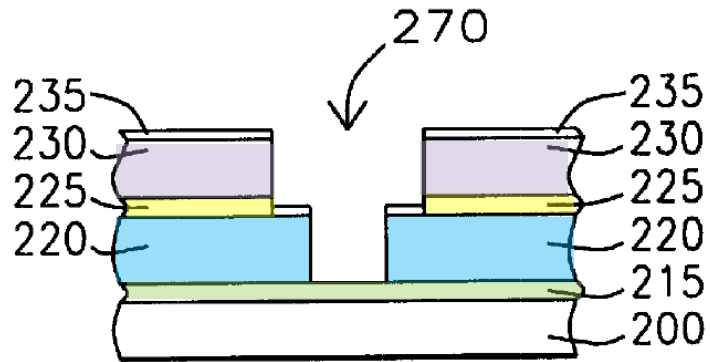
##### 1. *Chen*

Chen, like Peng and Lin, discloses a “dual damascene” structure for a “damascene interconnect.” EX1017, Abstract, FIG. 2e; EX1002, ¶187. Chen’s dual-damascene structure is also similar to that of the ’797 patent, including “semiconductor substrate (200),” [green] silicon nitride “layer (215),” [blue]

“[intermetal dielectric] layer (220),” [yellow] “etch stop layer (225),” and [purple] “second [intermetal dielectric] layer (230).” EX1017, 4:55-5:49; EX1002, ¶187.

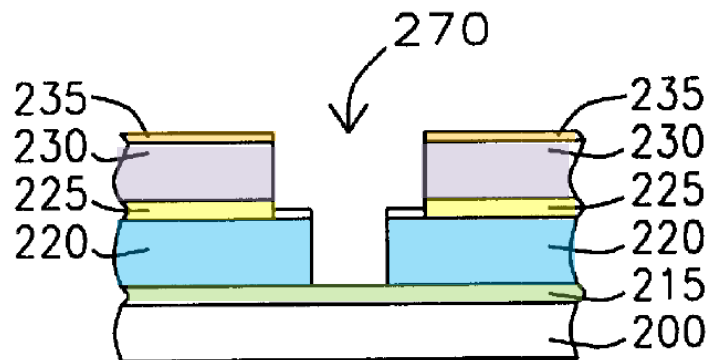


EX1001, FIG. 3E



EX1017, FIG. 2e

Chen additionally describes that “[i]t is preferred that a[] [gold] antireflective coating (ARC) [235] is also formed over the [purple] second IMD layer [230].” EX1017, 5:49-51. “This is because, [gold] ARC layer (235) ... serves to control the dimensional integrity (CD control, as is known in the art) during a subsequent etch step.” *Id.*, 5:51-54.



EX1017, Fig. 2e.

## **2. *Motivation to Combine***

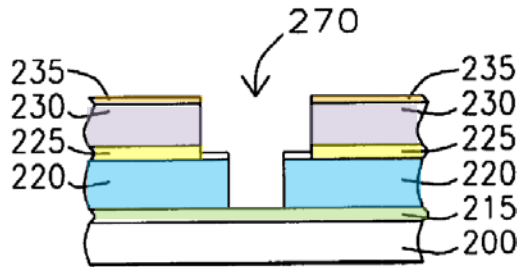
A POSITA would have been motivated to include Chen's ARC layer 235 in the dual damascene structures of Peng and Lin to obtain the benefit of "control[ing] the dimensional integrity (CD control, as is known in the art) during a subsequent etch step." EX1017, 5:51-54; EX1002, ¶189. A POSITA would have understood that an ARC layer achieves this benefit by "reduc[ing] undesired light reflections from an underlying IMD layer ... during a photolithographic patterning process." EX1002, ¶189 (citing EX1018, ¶[0020]). A POSITA would have understood Chen's disclosure to be compatible with the structures formed in Grounds 1-3, each of which involves using a photolithographic process to etch a dielectric layer. §§IX.A.1, IX.B.3, IX.C.3; EX1002, ¶189.

## **3. *Modification of Peng in view of Chen***

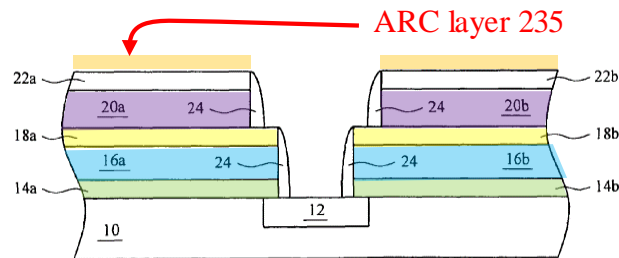
A POSITA would have modified each of Peng-Brase and Peng-Chien-Brase by including the ARC layer of Chen. EX1002, ¶190.

Applying Chen's disclosure of forming "an antireflective coating (ARC)" "over the [purple] second IMD layer" to Peng entails forming ARC layer 235 on top of [purple] second dielectric layers 20a and 20b either in addition or as an alternative to stop layers 22a and 22b. EX1017, 5:46-51; EX1003, 4:33-35; EX1002, ¶191. A POSITA would have understood that ARC layers can also function as an etch stop layer or may be paired with an etch stop layer. EX1002, ¶191 (citing EX1018,

¶[0020] (“a single layer of silicon oxynitride (e.g., SiON), functioning as both an etch stop and a [dielectric anti-reflectance coating] layer”)).



**EX1006, FIG. 2c**

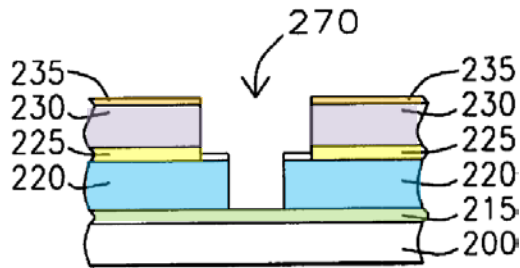


**EX1003, FIG. 2  
(modified per Chen)**

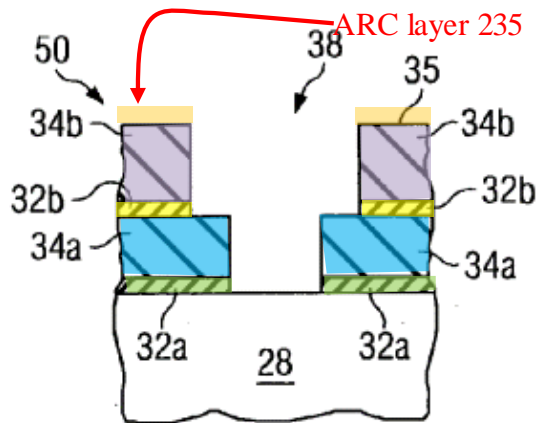
The ARC layer improves the dimensional integrity of the etch through layers 22b and 20b, and would not affect formation of Peng’s spacer regions 24 as described in Grounds 1 and 2. EX1002, ¶192.

#### **4. *Modification of Lin and Chien in view of Chen***

Applying Chen’s disclosure of forming “an antireflective coating (ARC)” “over the [purple] second IMD layer” to Lin entails forming ARC layer 235 on top of [purple] dielectric layer 34b. EX1017, 5:46-51; EX1003, 4:33-35; EX1002, ¶194.



**EX1006, FIG. 2c**



**EX1004, FIG. 12  
(modified per Chen)**

The ARC layer 235 would improve the dimensional integrity of the etch through layer 34b, and would not affect formation of Lin's opening 38 as described in Ground 3. EX1002, ¶195.

### **5. *Element-by-element analysis***

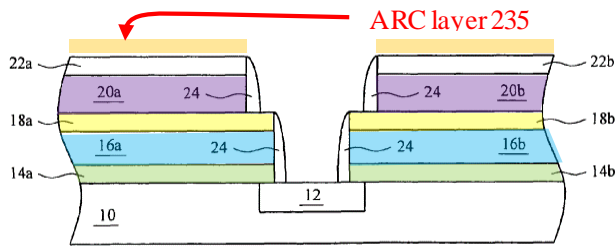
**Limitation 10: “An integrated circuit of claim 1 further comprising depositing an anti reflective coating layer.”**

Ground 4: *See* §IX.A.5 (Claim 1).

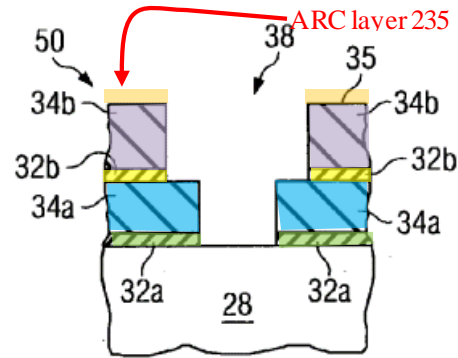
Ground 5: *See* §IX.B.4 (Claim 1).

Ground 6: *See* §IX.C.4 (Claim 1).

Grounds 4-6: As discussed in §§IX.D.3-IX.D.4, it was obvious to modify the structures of each of Grounds 1, 2, and 3 to include [gold] ARC layer 235, meeting this limitation in Grounds 4, 5, and 6, respectively. EX1002, ¶196.



**EX1003, FIG. 2**  
(modified per Chen)



**EX1004, FIG. 12**  
(modified per Chen)

**Limitation 14: “An integrated circuit of claim 11 further comprising depositing an anti reflective coating layer.”**

Ground 5: *See* §IX.B.4 (Claim 11).

Ground 6: *See* §IX.C.4 (Claim 11).

Grounds 5-6: As discussed in §§IX.D.3-IX.D.4, it was obvious to modify the structures of each of Grounds 2 and 3 to include [gold] ARC layer 235, meeting this limitation in Grounds 5 and 6, respectively. EX1002, ¶196.

## **X. CONCLUSION**

For the above reasons, the challenged claims are invalid under §103(a).

Dated: October 26, 2020

Respectfully submitted,

/Eagle H. Robinson/  
Eagle H. Robinson

*Lead Counsel for Petitioner*

**CERTIFICATE OF WORD COUNT**

Pursuant to 37 C.F.R. § 42.24(a)(i), the undersigned certifies that this Paper—exclusive of the table of contents, mandatory notices under § 42.8, certificate of service, and this certificate of word count—includes 13,829 words.

/Eagle H. Robinson/  
Eagle H. Robinson (Reg. No. 61,361)

## **CERTIFICATE OF SERVICE**

Pursuant to 37 C.F.R. § 42.6(e) and 37 C.F.R. § 42.105(a), the undersigned certifies that on October 26, 2020, a complete copy of this Petition for *Inter Partes* Review, Petitioner's power of attorney, and all exhibits were served on Patent Owner at the correspondence addresses of record listed below by FedEx®:

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Attn: Legal - Bldg. 6.1  
SAN JOSE CA 95134

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