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Alexandria, Virginia 22313-1450 www.uspto.gov

APPLICATION NO.	APPLICATION NO. ISSUE DATE		ATTORNEY DOCKET NO.	CONFIRMATION NO.	
10/953,291	05/22/2007	7221173	BACHMAN 3-11-16-173	2052	

47386

7590

05/02/2007

RYAN, MASON & LEWIS, LLP 1300 POST ROAD SUITE 205 FAIRFIELD, CT 06824

ISSUE NOTIFICATION

The projected patent number and issue date are specified above.

Determination of Patent Term Adjustment under 35 U.S.C. 154 (b)

(application filed on or after May 29, 2000)

The Patent Term Adjustment is 0 day(s). Any patent to issue from the above-identified application will include an indication of the adjustment on the front page.

If a Continued Prosecution Application (CPA) was filed in the above-identified application, the filing date that determines Patent Term Adjustment is the filing date of the most recent CPA.

Applicant will be able to obtain more detailed information by accessing the Patent Application Information Retrieval (PAIR) WEB site (http://pair.uspto.gov).

Any questions regarding the Patent Term Extension or Adjustment determination should be directed to the Office of Patent Legal Administration at (571)-272-7702. Questions relating to issue and publication fee payments should be directed to the Customer Service Center of the Office of Patent Publication at (571)-272-4200.

APPLICANT(s) (Please see PAIR WEB site http://pair.uspto.gov for additional applicants):

Mark Adam Bachman, Sinking Spring, PA; Daniel Patrick Chesire, Winter Garden, FL; Taeho Kook, Orlando, FL; Sailesh M. Merchant, Macungie, PA;

IR103 (Rev. 11/05) Microchip et al. Ex. 1002-1

PART B - FEE(S) TRANSMITTAL

Complete and send this form, together with applicable fee(s), to: Mail Mail Stop ISSUE FEE
Commissioner for Patents
P.O. Box 1450 Alexandria, Virginia 22313-1450 or Fax (571)-273-2885

						213-2003			
INSTRUCTIONS: This appropriate. All further indicated unless correct maintenance fee notifical	form should be used correspondence includied below or directed of tions.	for transmitting ng the Patent, ac herwise in Block	the ISS lvance of 1, by	UE FEE and PUBLIC orders and notification (a) specifying a new co	CATION of main orrespon	FEE (if requitenance fees with dence address;	ired). I vill be and/or	Blocks I through 5 sh mailed to the current r (b) indicating a sepa	ould be completed when correspondence address a rate "FEE ADDRESS" for the contract of the con
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47386 RYAN, MASC 1300 POST ROA SUITE 205				Cer	tificate	of Mailing or Transi			
FAIRFIELD, CT	`06824			ĺ		Kare	n V	ertz	(Depositor's name
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APPLICATION NO.	FILING DATE			FIRST NAMED INVENT	TOR		ATTO	RNEY DOCKET NO.	CONFIRMATION NO.
10/953,291	09/29/2004			Mark Adam Bachma	an		BACH	MAN 3-11-16-173	2052
TITLE OF INVENTION BUMPING PROCESS	: METHOD AND STE	RUCTURES FO	R TEST	ING A SEMICONDU	CTOR V	WAFER PRIO	r to	PERFORMING A FL	IP CHIP
APPLN. TYPE	SMALL ENTITY	ISSUE FEE D	UE	PUBLICATION FEE D	UE PRI	EV. PAID ISSUE	FEE	TOTAL FEE(S) DUE	DATE DUE
nonprovisional	NO	\$1400		\$300		\$0 .		\$1700	04/24/2007
EXAMI	NER	ART UNI	······································	CLASS-SUBCLASS					
NGUYEN,	TUNG X	2829		324-754000					
"Fee Address" indi	nce address or indication ondence address (or Cha /122) attached. cation (or "Fee Address 2 or more recent) attach	nge of Correspor	dence	(1) the names of up to 3 registered patent attorneys or agents OR, alternatively, (2) the name of a single firm (having as a member a registered attorney or agent) and the names of up to					
3. ASSIGNEE NAME AN PLEASE NOTE: Unle recordation as set forth (A) NAME OF ASSIG	ess an assignee is ident in 37 CFR 3.11. Comp			· ·	ne patent. an assig				cument has been filed fo
Agere S	ystems, In	C.		Allent	town	ı, Penn	syl	vania	
Please check the appropria	ate assignee category or	categories (will a	ot be p	rinted on the patent):	☐ Indi	vidual KK Co	rporatio	on or other private grou	p entity Governmen
4a. The following fee(s) a XX Issue Fee Publication Fee (No	41	b. Payment of Fee(s): (F A check is enclose Payment by credit The Director is her overpayment, to Do	d. card. Fo	orm PTO-2038	is attac	ched.	ciency, or credit any extra copy of this form).		
5. Change in Entity State	,	•	***********						
• •	SMALL ENTITY statu			• •	_	-		TTY status. See 37 CF	1007 1 7
NOTE: The Issue Fee and interest as shown by the re	cords of the United Sta	pres) will not be see Parent and Tra	accepte idemark	d from anyone other that Office.	an the ap	plicant; a regis	tered a	ttorney or agent; or the	assignee or other party in
Authorized Signature	grant !	Jan	√		1	Date Ap	ril	17, 2007	
Typed or printed name	Charles V	W. Gaine	es_		1	Registration No	o	36,804	
This collection of informa an application. Confidenti submitting the completed	tion is required by 37 C ality is governed by 35 application form to the	FR 1.311. The in U.S.C. 122 and 3 USPTO. Time v	formation 7 CFR Vill vary	on is required to obtain of 1.14. This collection is depending upon the in	or retain estimate dividual	a benefit by the ed to take 12 m case. Any cor	e publi inutes nments	c which is to file (and to complete, including on the amount of time	by the USPTO to process gathering, preparing, and you require to complete

this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, Virginia 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, Virginia 22313-1450.

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Electronic Patent Application Fee Transmittal							
Application Number:	10	953291					
Filing Date:	29	-Sep-2004					
Title of Invention:	METHOD AND STRUCTURES FOR TESTING A SEMICONDUCTOR WAFER PRIOR TO PERFORMING A FLIP CHIP BUMPING PROCES						
First Named Inventor/Applicant Name: Mark Adam Bachman							
Filer:	Charles W. Gaines/Karen Vertz						
Attorney Docket Number:	ney Docket Number: BACHMAN 3-11-16-173						
Filed as Large Entity							
Utility Filing Fees							
Description		Fee Code	Quantity	Amount	Sub-Total in USD(\$)		
Basic Filing:							
Pages:							
Claims:							
Miscellaneous-Filing:							
Petition:							
Patent-Appeals-and-Interference:							
Post-Allowance-and-Post-Issuance:							
Utility Appl issue fee		1501	1	1400	1400		
Publ. Fee- early, voluntary, or normal		1504	1	300	300		

Description	Fee Code	Fee Code Quantity		Sub-Total in USD(\$)
Extension-of-Time:				
Miscellaneous:				
) (\$)	1700		

Electronic Acl	knowledgement Receipt
EFS ID:	1688425
Application Number:	10953291
International Application Number:	
Confirmation Number:	2052
Title of Invention:	METHOD AND STRUCTURES FOR TESTING A SEMICONDUCTOR WAFER PRIOR TO PERFORMING A FLIP CHIP BUMPING PROCESS
First Named Inventor/Applicant Name:	Mark Adam Bachman
Customer Number:	47386
Filer:	Charles W. Gaines/Karen Vertz
Filer Authorized By:	Charles W. Gaines
Attorney Docket Number:	BACHMAN 3-11-16-173
Receipt Date:	17-APR-2007
Filing Date:	29-SEP-2004
Time Stamp:	10:59:22
Application Type:	Utility

Payment information:

Submitted with Payment	yes
Payment was successfully received in RAM	\$1700
RAM confirmation Number	1642
Deposit Account	082395

The Director of the USPTO is hereby authorized to charge indicated fees and credit any overpayment as follows: Charge any Additional Fees required under 37 C.F.R. Section 1.16 and 1.17

File Listing:

Document Number	Document Description	File Name	File Size(Bytes)	Multi Part /.zip	Pages (if appl.)
1	Issue Fee Payment (PTO-85B)	Issue_Publication_Fees.pdf	154612	no	1
Warnings:					
Information:					
2	Fee Worksheet (PTO-06)	fee-info.pdf	8357	no	2
Warnings:					
Information:					
		Total Files Size (in bytes):	1	62969	

This Acknowledgement Receipt evidences receipt on the noted date by the USPTO of the indicated documents, characterized by the applicant, and including page counts, where applicable. It serves as evidence of receipt similar to a Post Card, as described in MPEP 503.

New Applications Under 35 U.S.C. 111

If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application.

National Stage of an International Application under 35 U.S.C. 371

If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.

New International Application Filed with the USPTO as a Receiving Office

If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.





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NOTICE OF ALLOWANCE AND FEE(S) DUE

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01/24/2007

RYAN, MASON & LEWIS, LLP 1300 POST ROAD SUITE 205 FAIRFIELD, CT 06824

EXAMINER						
NGUYEN, TUNG X						
ART UNIT	PAPER NUMBER					

2829 DATE MAILED: 01/24/2007

ſ	APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
Ī	10/953.291	09/29/2004	Mark Adam Bachman	BACHMAN 3-11-16-173	2052

TITLE OF INVENTION: METHOD AND STRUCTURES FOR TESTING A SEMICONDUCTOR WAFER PRIOR TO PERFORMING A FLIP CHIP

BUMPING PROCESS

APPLN. TYPE	SMALL ENTITY	ISSUE FEE DUE	PUBLICATION FEE DUE	PREV. PAID ISSUE FEE	TOTAL FEE(S) DUE	DATE DUE
nonprovisional	NO	\$1400	\$300	\$0	\$1700	04/24/2007

THE APPLICATION IDENTIFIED ABOVE HAS BEEN EXAMINED AND IS ALLOWED FOR ISSUANCE AS A PATENT. PROSECUTION ON THE MERITS IS CLOSED. THIS NOTICE OF ALLOWANCE IS NOT A GRANT OF PATENT RIGHTS. THIS APPLICATION IS SUBJECT TO WITHDRAWAL FROM ISSUE AT THE INITIATIVE OF THE OFFICE OR UPON PETITION BY THE APPLICANT. SEE 37 CFR 1.313 AND MPEP 1308.

THE ISSUE FEE AND PUBLICATION FEE (IF REQUIRED) MUST BE PAID WITHIN THREE MONTHS FROM THE MAILING DATE OF THIS NOTICE OR THIS APPLICATION SHALL BE REGARDED AS ABANDONED. THIS STATUTORY PERIOD CANNOT BE EXTENDED. SEE 35 U.S.C. 151. THE ISSUE FEE DUE INDICATED ABOVE DOES NOT REFLECT A CREDIT FOR ANY PREVIOUSLY PAID ISSUE FEE IN THIS APPLICATION. IF AN ISSUE FEE HAS PREVIOUSLY BEEN PAID IN THIS APPLICATION (AS SHOWN ABOVE), THE RETURN OF PART B OF THIS FORM WILL BE CONSIDERED A REQUEST TO REAPPLY THE PREVIOUSLY PAID ISSUE FEE TOWARD THE ISSUE FEE NOW DUE.

HOW TO REPLY TO THIS NOTICE:

I. Review the SMALL ENTITY status shown above.

If the SMALL ENTITY is shown as YES, verify your current SMALL ENTITY status:

- A. If the status is the same, pay the TOTAL FEE(S) DUE shown above.
- B. If the status above is to be removed, check box 5b on Part B Fee(s) Transmittal and pay the PUBLICATION FEE (if required) and twice the amount of the ISSUE FEE shown above, or

If the SMALL ENTITY is shown as NO:

- A. Pay TOTAL FEE(S) DUE shown above, or
- B. If applicant claimed SMALL ENTITY status before, or is now claiming SMALL ENTITY status, check box 5a on Part B Fee(s) Transmittal and pay the PUBLICATION FEE (if required) and 1/2 the ISSUE FEE shown above.

II. PART B - FEE(S) TRANSMITTAL, or its equivalent, must be completed and returned to the United States Patent and Trademark Office (USPTO) with your ISSUE FEE and PUBLICATION FEE (if required). If you are charging the fee(s) to your deposit account, section "4b" of Part B - Fee(s) Transmittal should be completed and an extra copy of the form should be submitted. If an equivalent of Part B is filed, a request to reapply a previously paid issue fee must be clearly made, and delays in processing may occur due to the difficulty in recognizing the paper as an equivalent of Part B.

III. All communications regarding this application must give the application number. Please direct all communications prior to issuance to Mail Stop ISSUE FEE unless advised to the contrary.

IMPORTANT REMINDER: Utility patents issuing on applications filed on or after Dec. 12, 1980 may require payment of maintenance fees. It is patentee's responsibility to ensure timely payment of maintenance fees when due.

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appropriate. All further indicated unless corrected anitenance fee notificated to the control of	correspondence includired below or directed oth tions.	or training the linerwise	Patent, advance or in Block I, by (a					correspondence address as rate "FEE ADDRESS" for
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47386	7590 01/24	/2007			Corr	rificate	of Mailing or Transn	nission
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FAIRFIELD, CT	1 06824							(Depositor's name)
								(Signature)
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APPLICATION NO.	FILING DATE			FIRST NAMED INVENTOR		ATTO	RNEY DOCKET NO.	CONFIRMATION NO.
10/953,291	09/29/2004		<u> </u>	Mark Adam Bachman		BACH	MAN 3-11-16-173	2052
TITLE OF INVENTION BUMPING PROCESS	N: METHOD AND STE	RUCTL	IRES FOR TESTI	ING A SEMICONDUCTO	OR WAFER PRIO	R TO	PERFORMING A FL	IP CHIP
APPLN. TYPE	SMALL ENTITY	IS	SUE FEE DUE	PUBLICATION FEE DUE	PREV. PAID ISSUI	E FEE	TOTAL FEE(S) DUE	DATE DUE
nonprovisional	NO		\$1400	\$300	\$0		\$1700	04/24/2007
EXAM	INER		ART UNIT	CLASS-SUBCLASS				
NGUYEN	, TUNG X		2829	324-754000				
☐ "Fee Address" ind	ondence address (or Cha B/122) attached. lication (or "Fee Address 20 or more recent) attach	Correspondence	2. For printing on the patent front page, list (1) the names of up to 3 registered patent attorneys or agents OR, alternatively, (2) the name of a single firm (having as a member a registered attorney or agent) and the names of up to 2 registered patent attorneys or agents. If no name is listed, no name will be printed.					
3. ASSIGNEE NAME A PLEASE NOTE: Un recordation as set fort (A) NAME OF ASSI	less an assignee is ident th in 37 CFR 3.11. Com	A TO E	E PRINTED ON all of this form is NO	THE PATENT (print or type data will appear on the part a substitute for filing and (B) RESIDENCE: (CITY	atent. If an assign assignment.			ocument has been filed for
Please check the appropr	iate assignee category or	r catego	ories (will not be pr	rinted on the patent):	Individual Co	orporati	on or other private gro	oup entity Government
	are submitted: No small entity discount # of Copies	ed)	b. Payment of Fee(s): (Plea A check is enclosed. Payment by credit car The Director is hereby overpayment, to Depo	d. Form PTO-2038	is atta	ched.	shown above) ficiency, or credit any n extra copy of this form).	
5. Change in Entity Sta	-			<u> </u>			TITT!	SD 1 277 (22)
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NOTE: The Issue Fee an interest as shown by the	records of the United St	iuired) ates Pat	will not be accepte ent and Trademark	of from anyone other than to Office.	ne applicant, a regi	stered a	attorney or agent, or th	e assignee of other party in
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submitting the completed application form to the USFIO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, Virginia 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, Virginia 22313-1450.

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APPLICATION NO. FILING DATE		FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.		
10/953,291	09/29/2004	Mark Adam Bachman	BACHMAN 3-11-16-173 2052			
47386 7	590 01/24/2007		EXAM	INER		
RYAN, MASON	N & LEWIS, LLP	NGUYEN, TUNG X				
1300 POST ROAL	-		ART UNIT	PAPER NUMBER		
SUITE 205 FAIRFIELD, CT	06824		2829 DATE MAILED: 01/24/200	7		

Determination of Patent Term Adjustment under 35 U.S.C. 154 (b)

(application filed on or after May 29, 2000)

The Patent Term Adjustment to date is 0 day(s). If the issue fee is paid on the date that is three months after the mailing date of this notice and the patent issues on the Tuesday before the date that is 28 weeks (six and a half months) after the mailing date of this notice, the Patent Term Adjustment will be 0 day(s).

If a Continued Prosecution Application (CPA) was filed in the above-identified application, the filing date that determines Patent Term Adjustment is the filing date of the most recent CPA.

Applicant will be able to obtain more detailed information by accessing the Patent Application Information Retrieval (PAIR) WEB site (http://pair.uspto.gov).

Any questions regarding the Patent Term Extension or Adjustment determination should be directed to the Office of Patent Legal Administration at (571)-272-7702. Questions relating to issue and publication fee payments should be directed to the Customer Service Center of the Office of Patent Publication at 1-(888)-786-0101 or (571)-272-4200.

	Application No.	Applicant(s)						
	•							
Notice of Allowability	10/953,291 Examiner	BACHMAN ET AL.						
nodes of Anomability	Examiner	Art Onit						
	Tung X. Nguyen	2829						
The MAILING DATE of this communication appe All claims being allowable, PROSECUTION ON THE MERITS IS herewith (or previously mailed), a Notice of Allowance (PTOL-85) NOTICE OF ALLOWABILITY IS NOT A GRANT OF PATENT RIC of the Office or upon petition by the applicant. See 37 CFR 1.313	(OR REMAINS) CLOSED in this apport of the communication of the communication of the communication is subject to the communication in the communication is subject to the	olication. If not included will be mailed in due course. THIS						
1. 🖂 This communication is responsive to the amendment filed of	<u>on 11/9/06</u> .							
2. The allowed claim(s) is/are <u>1-10</u> .								
3. Acknowledgment is made of a claim for foreign priority un a) All b) Some* c) None of the:								
 Certified copies of the priority documents have Certified copies of the priority documents have 								
Copies of the certified copies of the priority documents have	· · · · · · · · · · · · · · · · · · ·							
International Bureau (PCT Rule 17.2(a)).	differits have been received in this	national stage application from the						
* Certified copies not received:		•						
Applicant has THREE MONTHS FROM THE "MAILING DATE" of this communication to file a reply complying with the requirements noted below. Failure to timely comply will result in ABANDONMENT of this application. THIS THREE-MONTH PERIOD IS NOT EXTENDABLE.								
4. A SUBSTITUTE OATH OR DECLARATION must be submit INFORMAL PATENT APPLICATION (PTO-152) which give								
5. CORRECTED DRAWINGS (as "replacement sheets") mus	t be submitted.							
(a) ☐ including changes required by the Notice of Draftspers	on's Patent Drawing Review (PTO-	948) attached						
1) 🗌 hereto or 2) 🔲 to Paper No./Mail Date								
(b) ☐ including changes required by the attached Examiner's Paper No./Mail Date	s Amendment / Comment or in the C	Office action of						
Identifying indicia such as the application number (see 37 CFR 1 each sheet. Replacement sheet(s) should be labeled as such in the								
6. DEPOSIT OF and/or INFORMATION about the deposit attached Examiner's comment regarding REQUIREMENT I								
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 Notice of References Cited (PTO-892) Notice of Draftperson's Patent Drawing Review (PTO-948) 	 5. ☐ Notice of Informal F 6. ☐ Interview Summary 	•						
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4. Examiner's Comment Regarding Requirement for Deposit of Biological Material		ent of Reasons for Allowance						
•	9. Other	•						
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Art Unit: 2829

REASONS FOR ALLOWANCE

1. Claims 1-10 are allowed.

Applicant's arguments have been fully considered and deemed persuasive, see "Remark" on papers 5-6, filed 11/09/06, with respect to claim(s) 1-10. The claims are allowed by the following reasons:

As to claims 1, 9, the prior art of record does not teach an interface assembly for a semiconductor wafer particularly defined by characteristic of the test pad integrally constructed with the bonding pad that form an integral conductive structure such that separate interconnect testing lines from the test pad to the bonding pad are not present in the integral structure. The absented interconnect lines from the test pad to bonding pad of the claimed system gives the benefit of reduced or avoided propagation delays in test signal passing therethrough [see paragraph 14 on page 4 in specification].

As to claim 10, the prior art of record does not teach an interface assembly for a semiconductor wafer particularly defined by characteristic of the first metal redistribution layer connecting to the bonding and test pad, and being co-planar with one another, the first metal redistribution layer is electrically connected by way of a via to a second redistribution layer being disposed in a different plane than the first redistribution layer.

These features in combination with the other elements of the claim are neither disclosed nor suggested by the prior art of record.

The other claims depend from the claim 1. They are allowed for the same reasons.

Any comments considered necessary by applicant must be submitted no later than the payment of the issue fee and, to avoid processing delays, should preferably accompany the issue fee. Such submissions should be clearly labeled "Comments on Statement of Reasons for Allowance."

Conclusion

2. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Tung X. Nguyen whose telephone number is (571) 272-1967. The examiner can normally be reached on 8:30am-5:00pm M-F.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Ha T. Nguyen can be reached on (571) 272-1678. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

TN 1/19/07

HA TRAN NGUYEN
SUPERVISORY PATENT EYAMINED



Application/Control No. 10/953,291	Applicant(s)/Patent under Reexamination BACHMAN ET AL.
Examiner	Art Unit
Tung X. Nguyen	2829

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UNITED STATES DEPARTMENT OF COMMERCE United States Patent and Trademark Office Address COMMISSIONER FOR PATENTS RO. Box 1930 Afranafia, Viginis 22313-1450 www.mptp.gpr

Rib Data Sheet

CONFIRMATION NO. 2052

SERIAL NUMBI 10/953,291	ER	FILING DATE 09/29/2004 RULE	С	CLASS 324	GROI	UP AR1 2829	T UNIT	D	ATTORNEY OCKET NO. hman 3-11-16- 173
APPLICANTS		,			·				
Mark Adam	n Bachr	man, Sinking Spring,	PA;						
Daniel Patrick Chesire, Winter Garden, FL; Taeho Kook, Orlando, FL;Sailesh M. Merchant, Macungie, PA;									
CONTINUING DATA									
FOREIGN APPLICATIONS									
IF REQUIRED, FO ** 11/15/2004	OREIG	IN FILING LICENSE	GRANTE	:D					
Foreign Priority claimed 35 USC 119 (a-d) cond met Verified and Acknowledged	ditions	yes no no Met after	ter 	STATE OR COUNTRY PA	DRA	ETS WING	TOT. CLAII		INDEPENDENT CLAIMS
ADDRESS 29391	ANGE A	WOLTER MORA & M. AVENUE	AIRE, P.						19/07
TITLE Method and struc	ctures f	or testing a semicond	luctor wa	ifer prior to per	rforming	j a flip (chip bum	iping f	process
	No	Authority has been gi to charge/cr for following	redit DEP	aper 'OSIT ACCOU	INT		16 Fees (g) essing Ext. of

Search Notes

Application/Control No.	Applicant(s)/Patent under Reexamination	
10/953,291	BACHMAN ET AL.	
Examiner	Art Unit	

Tung X. Nguyen

	SEAR	CHED			
Class	Subclass	Date	Examiner		
324	754 ·	6/17/2005	TN		
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	760				
	765				
	158.1				
	72.5				
	73.1				
438	18	6/17/2005	TN		
	132				
	FOR101	1/19/2007	TN		
	FOR142				
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257	48,529	1/19/2007	TN		

INT	INTERFERENCE SEARCHED									
Class	Subclass	Date Examin								
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SEARCH NOTES (INCLUDING SEARCH STRATEGY)								
	DATE	EXMR						
EAST search in all of the database with keywords search; inventors search, and updated search	1/19/2007	TN						
Interference search (see history printed out)	1/19/2007	TN						
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Ref #	Hits	Search Query	DBs	Default Operator	Plurals	Time Stamp
L1	4559	324/754.ccls.	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2007/01/19 19:47
L2	62723	bond\$4 adj2 pad	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2007/01/19 19:47
L3	7059	test\$4 adj2 pad	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2007/01/19 19:48
L4	745	2 with 3	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2007/01/19 19:48
L5	78031	(avoid\$4 or reduc\$4) near5 delay	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2007/01/19 19:49
L6	8	4 and 5	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2007/01/19 19:51
L7	16749	324/754-765,158.1.ccls.	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON .	2007/01/19 19:51
L8	16749	L7	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2007/01/19 19:51
L9	217	4 and 8	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR .	ON	2007/01/19 19:51

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L10	2	5 and 9	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2007/01/19 19:52
L11	2535	257/48,529.ccls.	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2007/01/19 19:52
L12	2535	L11	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2007/01/19 19:52
L13	57	4 and 12	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2007/01/19 19:52
L14	1	5 and 13	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2007/01/19 19:53
L15	1038	438/18,132.ccls.	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2007/01/19 19:53
L16	1038	L15	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON .	2007/01/19 19:53
L17	25	4 and 16	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2007/01/19 19:56
L18		5 and 17	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2007/01/19 19:53
L19	0	4 with "without trace"	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON ·	2007/01/19 19:56

L20	0	4 with "without traces"	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2007/01/19 19:56
L21	0	4 with "without lines"	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2007/01/19 19:57
L22 .	0	4 with without with (line or trace or conductive adj l(ine or trace))	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON .	2007/01/19 20:05
L24	13	("20020135055" "20030116835" "5346861" "5682061" "6361959" "6372627" "6437591" "6600171" "6670634" "6680213" "6687989" "6708399").PN. OR ("6869809").URPN.	US-PGPUB; USPAT; USOCR	OR	ON	2007/01/19 20:04
L25	0	4 with without with (line or trace or conductive adj (line or trace))	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2007/01/19 20:05
L26	4	4 same without with (line or trace or conductive adj (line or trace))	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON .	2007/01/19 20:05
L27 .	39	4 and without with (line or trace or conductive adj (line or trace))	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2007/01/19 20:09
L28	2	(test\$4 near3 wafer and prior near4 (flip adj chip near2 bump\$4)).ti.	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2007/01/19 20:10
L29	2	(test\$4 near3 wafer and prior near4 (flip adj chip near2 bump\$4)).ab.	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2007/01/19 20:10

						
L30	1	(test\$4 near3 wafer and prior near4 (flip adj chip near2 bump\$4)).clm.	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2007/01/19 20:14
L31	1715	257/e21.521.ccls.	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2007/01/19 20:14
L32		4 and 31	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2007/01/19 20:15
L33	7	257/e21.524.ccls.	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2007/01/19 20:16
L34	2	4 and 33	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2007/01/19 20:17
L35	895	438/18,for101,for142,8.ccls.	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2007/01/19 20:18
L36	21	4 and 35	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2007/01/19 20:22
L37	32	(bachman near2 mark).inv.	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2007/01/19 20:23
L38	2	4 and 37	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2007/01/19 20:23
L39	19	(chesire near2 daniel).inv.	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON .	2007/01/19 20:24

L40	24	(kook near2 taeho).inv.	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2007/01/19 20:24
L41	248	(merchant near2 sailesh).inv.	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2007/01/19 20:25
L42	2	4 and 41	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR ,	ON	2007/01/19 20:25
L43	. 1	((first adj3 redistribution and second adj3 redistribution) with different adj2 plane).clm.	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2007/01/19 20:32
S1	0	(Yu adj et adj al).inv.	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2007/01/19 19:46
S2	0	"Us-2004/0173794 A1"	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2005/06/17 10:22
S3	0	·"2004/0173794"	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2005/06/17 10:22
S4	27	"0173794"	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON .	2005/06/17 10:26
S5	0	S4 and Yu	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2005/06/17 10:26
S6	3921	324/754.ccls.	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2005/06/17 10:27

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant:

Mark Adam Bachman, et al.

Serial No.:

10/953,291

Filed:

September 29, 2004

Title:

METHOD AND STRUCTURES FOR TESTING A SEMICONDUCTOR

WAFER PRIOR TO PERFORMING A FLIP CHIP BUMPING PROCESS

Grp./A.U.:

2829

Examiner:

Tung X. Nguyen

Confirmation No.: 2052

Commissioner for Patents P.O. Box 1450 Alexandria, VA 22313-1450 I hereby certify that this correspondence is being electronically filed with United States Patent and trademark Office on:

Karen vertz

(Printed or typed name of person signing the certificate)

(Signature of the person signing the certificate)

Sir:

AMENDMENT UNDER 37 C.F.R. § 1.111

In response to the Examiner's Action mailed July 24, 2006, please amend the aboveidentified application as follows:

IN THE CLAIMS:

1. (Currently Amended) An interface assembly for a semiconductor wafer, said interface assembly comprising:

a flip chip bonding pad including a region for performing a bumping process; and

a test pad integrally constructed with said bonding pad that form an integral conductive structure such that separate interconnect testing lines from said test pad to said bonding pad are not present in said integral structure, said test pad being coplanar relative to said flip chip bonding pad and including a probe region for performing wafer-level testing prior to performing said bumping process.

- 2. (Original) The interface assembly of claim 1 wherein said test pad may be disposed anywhere along a periphery of said bonding pad.
- 3. (Original) The interface assembly of claim 1 wherein said bonding pad comprises a shape selected from the group consisting of a polygonal shape, and a circular shape.
- 4. (Original) The interface assembly of claim 1 wherein said test pad comprises a shape selected from the group consisting of a polygonal shape, and a circular shape.
- 5. (Original) The interface assembly of claim 1 further comprising a first metal redistribution

layer electrically connected to said bonding and test pads, and being co-planar with one another.

- 6. (Original) The interface assembly of claim 5 wherein said first metal redistribution layer is electrically connected by way of a via to a second redistribution layer being disposed in a different plane than the first redistribution layer.
- 7. (Original) The interface assembly of claim 1 wherein the region to be bumped is defined by a first opening in a passivation layer.
- 8. (Original) The interface assembly of claim 7 wherein the probe region is defined by a second opening in said passivation layer, said first and second openings being spaced apart from one another.
- 9. (Currently Amended) A method for testing a semiconductor wafer prior to performing a flip chip bumping process, said method comprising:

providing a flip chip bonding pad having a region for performing said bumping process; integrally constructing a test pad with said bonding pad to form an integral conductive structure such that separate interconnect testing lines from said test pad to said bonding pad are not present in said integral structure; and

disposing said test pad coplanar with said flip chip bonding pad, said test pad including a probe region for performing a wafer test prior to performing said bumping process.

10. (New) An interface assembly for a semiconductor wafer, said interface assembly comprising:
a flip chip bonding pad including a region for performing a bumping process;

a test pad integrally constructed with said bonding pad, said test pad being coplanar relative to said flip chip bonding pad and including a probe region for performing wafer-level testing prior to performing said bumping process; and

a first metal redistribution layer electrically connected to said bonding and test pads, and being co-planar with one another, said first metal redistribution layer is electrically connected by way of a via to a second redistribution layer being disposed in a different plane than the first redistribution layer.

REMARKS/ARGUMENTS

The Applicants have carefully considered this application in connection with the Examiner's Action and respectfully request reconsideration of this application in view of the foregoing amendment and the following remarks.

The Applicants originally submitted Claims 1-9 in the application. The Applicants have amended Claims 1 and 9 and present new Claim 10, which is Claim 6 drafted in independent form. Accordingly, Claims 1-10 are currently pending in the application.

I. Rejection of Claims 1-5, 7-9 under 35 U.S.C. §102

These claims are rejected under 35 U.S.C. §102(e) as anticipated by U.S. Patent No. 6,869,809 to Yu, et al. (Yu). However, as now amended, Yu does not teach and every element of Claims 1 and 9. For example, Yu does not teach that the test pad and bond pad are integrally formed such that separate interconnect testing lines from the test pad to the bonding pad are not present in the integral structure. In fact, Yu specifically teaches to the contrary. In Column 5, lines 11-30, Yu teaches that the test pads 208a are electrically connected to various flip-chip bonding pads 208 through trace lines 209, as shown in FIG. 3A. Given the presence of these lines in Yu, propagation delays in the test signals would be present, which is contrary to a stated purpose of the invention to reduce or avoid such propagation delays in the test signals.

Therefore, Yu does not disclose each and every element of the claimed invention and as such, is not an anticipating reference for Claim1 or 9. Because Claims 2-8 are dependent upon

Claim 1, Yu also cannot be an anticipating reference for these claims. Accordingly, the Applicants

respectfully request the Examiner to withdraw the §102 rejection with respect to Claims 1-9.

As the Examiner has indicated, Claim 6 is deemed allowable over the cited references if

re-written in independent form, including all of the elements of the base claim and any intervening

claims. Applicants have presented re-written Claim 6 as New Claim 10. According to the

Examiner's indication of allowability, New Claim 10 is not anticipated by Yu.

II. Conclusion

In view of the foregoing amendment and remarks, the Applicants now see all of the Claims

currently pending in this application to be in condition for allowance and therefore earnestly solicit a

Notice of Allowance for Claims 1-10.

The Applicants request the Examiner to telephone the undersigned attorney of record at

(972) 480-8800 if such would further or expedite the prosecution of the present application. The

Commissioner is hereby authorized to charge any fees, credits or overpayments to Deposit Account

08-2395.

Respectfully submitted,

Charles W. Gaines

Registration No. 36,804

Dated:

P.O. Box 832′570′

Richardson, Texas 75083

(972) 480-8800

6

Electronic Patent Application Fee Transmittal							
Application Number:	109	953291					
Filing Date:	29-	-Sep-2004					
Title of Invention:	Method and structures for testing a semiconductor wafer prior to performing a flip chip bumping process Mark Adam Bachman						
First Named Inventor/Applicant Name: Mark Adam Bachman							
Filer:	Charles W. Gaines/Karen Vertz						
Attorney Docket Number:	BACHMAN 3-11-16-173						
Filed as Large Entity							
Utility Filing Fees							
Description		Fee Code	Quantity	Amount	Sub-Total in USD(\$)		
Basic Filing:							
Pages:							
Claims:							
Miscellaneous-Filing:							
Petition:							
Patent-Appeals-and-Interference:							
Post-Allowance-and-Post-Issuance:							
Extension-of-Time:							
Extension - 1 month with \$0 paid		1251	1	120 Microchip et a	₁₂₀ al. Ex. 1002-27		

Description	Fee Code	Quantity	Amount	Sub-Total in USD(\$)	
Miscellaneous:					
	Total in USD (\$)				

Electronic Acknowledgement Receipt				
EFS ID:	1303601			
Application Number:	10953291			
International Application Number:				
Confirmation Number:	2052			
Title of Invention:	Method and structures for testing a semiconductor wafer prior to performing a flip chip bumping process			
First Named Inventor/Applicant Name:	Mark Adam Bachman			
Customer Number:	47386			
Filer:	Charles W. Gaines/Karen Vertz			
Filer Authorized By:	Charles W. Gaines			
Attorney Docket Number:	BACHMAN 3-11-16-173			
Receipt Date:	09-NOV-2006			
Filing Date:	29-SEP-2004			
Time Stamp:	15:20:27			
Application Type:	Utility			

Payment information:

Submitted with Payment	yes
Payment was successfully received in RAM	\$120
RAM confirmation Number	116
Deposit Account	082395

The Director of the USPTO is hereby authorized to charge indicated fees and credit any overpayment as follows: Charge any Additional Fees required under 37 C.F.R. Section 1.16 and 1.17

File Listing:

Document Number	Document Description	File Name	File Size(Bytes)	Multi Part /.zip	Pages (if appl.)
1		Amendment1_111.pdf	363566	yes	6
	Multipa	rt Description/PDF files in	.zip description		
	Document De	Start	E	nd	
	Amendment - After No	1		1	
	Claims	2	2 4		
	Applicant Arguments/Remarks Made in an Amendment 5 6				
Warnings:					
Information:					
2	Fee Worksheet (PTO-875)	fee-info.pdf	8208 no		2
Warnings:		1			
Information:					
		Total Files Size (in bytes)	3	71774	

This Acknowledgement Receipt evidences receipt on the noted date by the USPTO of the indicated documents, characterized by the applicant, and including page counts, where applicable. It serves as evidence of receipt similar to a Post Card, as described in MPEP 503.

New Applications Under 35 U.S.C. 111

If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application.

National Stage of an International Application under 35 U.S.C. 371

If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.

P	PATENT APPLICATION FEE DETERMINATION RECORD Substitute for Form PTO-875						Application or Docket Number 10/953,291		Fil	ing Date 29/2004	To be Mailed
	APPLICATION AS FILED – PART I (Column 1) (Column 2)							ENTITY	OR		HER THAN
	FOR	N	JMBER FIL	· · ·	MBER EXTRA		RATE (\$)	FEE (\$)		RATE (\$)	FEE (\$)
	BASIC FEE (37 CFR 1.16(a), (b), or (c))		N/A		N/A		N/A		1	N/A	
	SEARCH FEE (37 CFR 1.16(k), (i), (i)		N/A		N/A		N/A		1	N/A	
	EXAMINATION FE (37 CFR 1.16(o), (p),	Ε	N/A		N/A		N/A		1	N/A	
	ΓAL CLAIMS CFR 1.16(i))		min	us 20 = *		1	x \$ =		OR	x \$ =	
IND	EPENDENT CLAIM CFR 1.16(h))	S	mi	inus 3 = *		1	x \$ =		1	x \$ =	
	APPLICATION SIZE (37 CFR 1.16(s))	shee is \$2 addit	ts of pape 50 (\$125 ional 50 s	ation and drawing er, the applicatio for small entity) sheets or fraction a)(1)(G) and 37	n size fee due for each n thereof. See						
	MULTIPLE DEPEN	IDENT CLAIM PR	ESENT (3	7 CFR 1.16(j))							
* If t	the difference in colu	ımn 1 is less than	zero, ente	r "0" in column 2.			TOTAL			TOTAL	
	APP	(Column 1)	AMEND	DED — PART II (Column 2)	(Column 3)	_	SMAL	L ENTITY	OR		ER THAN ALL ENTITY
AMENDMENT	11/09/2006	CLAIMS REMAINING AFTER AMENDMENT		HIGHEST NUMBER PREVIOUSLY PAID FOR	PRESENT EXTRA		RATE (\$)	ADDITIONAL FEE (\$)		RATE (\$)	ADDITIONAL FEE (\$)
)ME	Total (37 CFR 1.16(i))	* 10	Minus	** 20	= 0		x \$ =		OR	X \$50=	0
	Independent (37 CFR 1.16(h))	* 3	Minus	***3	= 0		x \$ =		OR	X \$200=	0
AMI	Application Si	ze Fee (37 CFR 1	.16(s))								
	FIRST PRESEN	ITATION OF MULTIF	PLE DEPEN	DENT CLAIM (37 CFF	R 1.16(j))				OR		
							TOTAL ADD'L FEE		OR	TOTAL ADD'L FEE	0
		(Column 1)		(Column 2)	(Column 3)					'	
L		CLAIMS REMAINING AFTER AMENDMENT		HIGHEST NUMBER PREVIOUSLY PAID FOR	PRESENT EXTRA		RATE (\$)	ADDITIONAL FEE (\$)		RATE (\$)	ADDITIONAL FEE (\$)
AMENDMENT	Total (37 CFR 1.16(i))	*	Minus	**	=		x \$ =		OR	x \$ =	
DM	Independent (37 CFR 1.16(h))	*	Minus	***	=		x \$ =		OR	x \$ =	
EΝ	Application Si	ze Fee (37 CFR 1	.16(s))								
ΑN	FIRST PRESEN	ITATION OF MULTIF	LE DEPEN	DENT CLAIM (37 CFF	R 1.16(j))				OR		
							TOTAL ADD'L FEE		OR	TOTAL ADD'L FEE	
** If	the entry in column the "Highest Numbe f the "Highest Numb "Highest Number P	er Previously Paid er Previously Paid	For" IN TH	HIS SPACE is less HIS SPACE is less	than 20, enter "20 s than 3, enter "3".		Patsy Z	nstrument Ex immerman priate box in colu		er:	

This collection of information is required by 37 CFR 1.16. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 12 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.

If you need assistance in completing the form, call 1-800-PTO-9199 and select option 2.



UNITED STATES DEPARTMENT OF COMMERCE United States Patent and Trademark Office Address COMMISSIONER FOR PATENTS P.O. BOX 1450 Alexandria, Virginia 22313-1450

APPLICATION NUMBER	FILING OR 371 (c) DATE	FIRST NAMED APPLICANT	ATTY. DOCKET NO./TITLE
10/953,291	09/29/2004	Mark Adam Bachman	Bachman 3-11-16-173

CONFIRMATION NO. 2052

29391 BEUSSE WOLTER SANKS MORA & MAIRE, P. A. 390 NORTH ORANGE AVENUE SUITE 2500 ORLANDO, FL 32801 *OC00000019747323*

Date Mailed: 07/25/2006

NOTICE REGARDING CHANGE OF POWER OF ATTORNEY

This is in response to the Power of Attorney filed 07/17/2006.

• The Power of Attorney to you in this application has been revoked by the assignee who has intervened as provided by 37 CFR 3.71. Future correspondence will be mailed to the new address of record(37 CFR 1.33).

SYED AREEBUDDIN PTOSS (703) 308-9150

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UNITED STATES DEPARTMENT OF COMMERCE United States Patent and Trademark Office Address: COMMISSIONER FOR PATENTS P.O. Box 1450 Alexandria, Vinginia 22313-1450 www.uspto.gov

FILING OR 371 (c) DATE FIRST NAMED APPLICANT ATTY, DOCKET NO./TITLE APPLICATION NUMBER BACHMAN 3-11-16-173 10/953,291 09/29/2004 Mark Adam Bachman

CONFIRMATION NO. 2052

OC000000019747407

47386 RYAN, MASON & LEWIS, LLP 1300 POST ROAD SUITE 205 FAIRFIELD, CT 06824

Date Mailed: 07/25/2006

NOTICE OF ACCEPTANCE OF POWER OF ATTORNEY

This is in response to the Power of Attorney filed 07/17/2006.

The Power of Attorney in this application is accepted. Correspondence in this application will be mailed to the above address as provided by 37 CFR 1.33.

SYED AREEBUDDIN PTOSS (703) 308-9150

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UNITED STATES DEPARTMENT OF COMMERCE United States Patent and Trademark Office Address: COMMISSIONER FOR PATENTS P.O. Box 1450 Alexandria, Virginia 22313-1450 www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.		
10/953,291	09/29/2004	Mark Adam Bachman	Bachman 3-11-16-173	2052		
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BEUSSE W	OLTER SANKS	NGUYEN	NGUYEN, TUNG X			
390 NORTH	ORANGE AVEN	3				
SUITE 2500			ART UNIT	PAPER NUMBER		
ORLANDO	FI 32801		2020			

DATE MAILED: 07/24/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

		Applicat	ion No.					
	Office Action Summany	10/953,2	91		BACHMAN ET AL.			
	Office Action Summary	Examine	r	Art Unit				
		Tung X.		2829				
Period fo	The MAILING DATE of this communic or Reply	cation appears on th	e cover sheet with	the correspondence ad	Idress			
WHIC - Exter after - If NO - Failu Any r	A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION. - Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication. - If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication. - Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).							
Status								
1) 又	Responsive to communication(s) filed	d on <i>08 Mav 2006</i> .						
'-	•	b) This action is	non-final.					
· · ·	Since this application is in condition f	<i>'</i> —		s, prosecution as to the	e merits is			
<i>,</i> —	closed in accordance with the practic	•		·				
Dispositi	on of Claims							
4)⊠	Claim(s) 1-9 is/are pending in the app	plication.						
ŕ	4a) Of the above claim(s) is/ar	e withdrawn from c	onsideration.					
5)	Claim(s) is/are allowed.							
6)⊠	Claim(s) <u>1-5 and 7-9</u> is/are rejected.							
7)🖂	Claim(s) <u>6</u> is/are objected to.							
8)[Claim(s) are subject to restrict	tion and/or election	requirement.					
Applicati	on Papers							
9)	The specification is objected to by the	Examiner.						
10)⊠	The drawing(s) filed on <u>29 September</u>	<u>r 2004</u> is/are: a)⊠	accepted or b)□	objected to by the Exa	miner.			
	Applicant may not request that any object	tion to the drawing(s)	be held in abeyance	e. See 37 CFR 1.85(a).				
	Replacement drawing sheet(s) including							
11)	The oath or declaration is objected to	by the Examiner. N	lote the attached (Office Action or form P	TO-152.			
Priority ι	ınder 35 U.S.C. § 119							
-	Acknowledgment is made of a claim f ☐ All b) ☐ Some * c) ☐ None of:	for foreign priority u	nder 35 U.S.C. § 1	119(a)-(d) or (f).				
	1. Certified copies of the priority of	documents have be	en received.					
	2. Certified copies of the priority of	documents have be	en received in Ap _l	plication No				
	3. Copies of the certified copies of	•		eceived in this National	Stage			
	application from the Internation							
* See the attached detailed Office action for a list of the certified copies not received.								
Attachmen	tic)							
	ι(s) e of References Cited (PTO-892)		4) Interview Su	mmary (PTO-413)	•			
2) Notic	e of Draftsperson's Patent Drawing Review (P		Paper No(s)/	Mail Date	0.450)			

Art Unit: 2829

DETAILED ACTION

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless -

- (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.
- 2. Claims 1-5, 7-9 are rejected under 35 U.S.C. 102(e) as being anticipated by Yu et al. (u.s.p 6,869,809).

As to claims 1, 9 Yu et al. discloses in Figs. 3-5, a device comprising a flip chip bonding pad (208 of figure 4A) including a region for performing a bumping (col. 5, lines 15-18); and a test pad (208a of figure 4A) integrally constructed with the bonding pad (208), the test pad being co-planar relative to the flip chip bonding pad and including a probe region (202 of figure 3B) for performing wafer-level testing prior to performing the bumping process (see the abstract, and col. 5, lines 10-20).

As to claim 2, Yu et al. discloses in figs. 3-5, the test pad (208a of figure 4A) may be disposed anywhere along a periphery of the bonding pad (208 of figure 4A).

As to claim 3, Yu et al. discloses in Figs. 3-5, the bonding pad comprises a shape from the group consisting of a polygonal shape, and circular shape (208 of figure 4A).

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Page 3

As to claim 4, Yu et al. discloses in Figs. 3-5, the test pad (208a of figure 4A) comprises a shape from the group consisting of a polygonal shape, and circular shape (208a).

As to claim 5, Yu et al. discloses in Figs. 3-5, a first metal redistribution layer (202 of figure 3B) electrically connected to the bonding and test pads, and being coplanar with one another (fig. 3B).

As to claim 7, Yu et al. discloses in Figs. 3-5, the region (220 of figure 4C) to be bumped is defined by a first opening in a passivation layer (210 of figure 4C).

As to claim 8, Yu et al. discloses in Figs. 3-5, the probe region (208a figure 4A) is defined by a second opening in the passivation, the first and second openings being spaced apart form one another (fig. 4A).

Allowable Subject Matter

- 3. Claim 6 is objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.
- 4. The following is a statement of reasons for the indication of allowable subject matter:

As to claim 6, the prior art does not teach or suggest the interface assembly wherein the first metal redistribution layer is electrically connected by way of a via to a second redistribution layer being disposed in a different plane than the first redistribution layer.

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Response to Arguments

In view of the Appeal Brief filed on 5/08/06, PROSECUTION IS HEREBY REOPENED.

Conclusion

5. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Tung X. Nguyen whose telephone number is (571) 272-1967. The examiner can normally be reached on 8:30am-5:00pm M-F.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Ha T. Nguyen can be reached on (571) 272-1678. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

TN 7/18/06 JERMELE HOLLINGTON
PRIMARY EXAMINER
AU 2829

777

PTO/SB/08A (05-03)

Approved for use through 07/31/2006. OMB 0651-0031
U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE
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Substitute for form 1449B/PTO		Application Number	10/953,291
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	1 of 1	Attorney Docket Number	Bachman 3-11-16-173 (383)
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			J.S. PATENT DO	CUMENTS	
Examiner Initials	Cite No.1	Document Number Number-Kind Code Strategics	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear
TN	01	US-6,359,342 B1	03-19-2002	Yuan et al.	
TN	02	US 2004/0161865 A1	08-19-2004	Yu et al.	
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		FOREIGN PA	ATENT DOCU	MENTS		 .
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4	Signature			

If you need assistance in completing the form, call 1-800-PTO-9199 (1-800-786-9199) and select option 2.

EXAMINER: Initial if reterence considered, whether or not diabon is in conformance with MPEP 609. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.

'Applicant's unique citation designation number (optional). *Applicant is to place a check mark ners if English Language Translation is attached.

This collection of information is required by 97 CFR 1.98. The Information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 2 hours to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the Individual complete, including gathering, preparing, and submitting the complete this form and/or suggestions for reducing this burden, should be sent to the Chief case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief case. Any comments of the Chief case. Any comments of the case of the case of the chief case.

Notice of References Cited Application/Control No. 10/953,291 Examiner Tung X. Nguyen Applicant(s)/Patent Under Reexamination BACHMAN ET AL. Page 1 of 1

U.S. PATENT DOCUMENTS

*		Document Number Country Code-Number-Kind Code	Date MM-YYYY	Name	Classification
*	Α	US-6,869,809	03-2005	Yu et al.	438/14
	В	US-			
	C	US-			
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FOREIGN PATENT DOCUMENTS

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NON-PATENT DOCUMENTS

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*A copy of this reference is not being furnished with this Office action. (See MPEP § 707.05(a).) Dates in MM-YYYY format are publication dates. Classifications may be US or foreign.

Search Notes

Application/Control No.	Applicant(s)/Patent under Reexamination		
10/953,291	BACHMAN ET AL.		
Examiner	Art Unit		
Tung X Nguyen	2829		

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324	754	6/17/2005		NT 1		
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	760					
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	158.1					
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438	18	6/17/2005		TN		
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257	48	6/17/2005		TN		
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SEARCH NOT (INCLUDING SEARCH)
	DATE	EXMR
Consulted with Vinh Nguyen about field search	6/17/2005	TN
EAST search and keywords search and updated search (see history printed out)	7/18/2006	TN

Index of Claims

App	lica	tion	/Conti	rol No.
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10/953,291

Examiner

Tung X. Nguyen

Reexamination **BACHMAN ET AL.**

Applicant(s)/Patent under

Art Unit

2829

Rejected Allowed

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L1	2533	(flip adj chip) near3 pad	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/07/18 13:26
L2	4342	test adj pad	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/07/18 13:26
L3	74	1 and 2	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/07/18 13:27
L4	36	(perform\$4 near3 bump\$4 adj process)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/07/18 13:27
L5	6	3 and 4	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/07/18 13:27
L6	12	("20020135055" "20030116835" "5346861" "5682061" "6361959" "6372627" "6437591" "6600171" "6670634" "6680213" "6687989" "6708399").PN. OR ("6869809").URPN.	US-PGPUB; USPAT; USOCR	OR	ON	2006/07/18 14:12
L7	4	"6869809"	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/07/18 15:19
L8	0	438/18/132.ccls	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/07/18 15:20
L9	2373	257/48,529.ccls.	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/07/18 15:20

		LASI Searc	,			
L10	2429	324/73.1,72.5.ccls.	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/07/18 15:20
L11	0	438/18,132.ccls	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/07/18 15:20
L12	985	438/18,132.ccls.	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/07/18 15:21
L13	11	1 and 12	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/07/18 15:21
L14	2	3 and 13	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/07/18 15:21
L15	0	10 and 1	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/07/18 15:21
L16	27	9 and 1	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/07/18 15:21
L17	1	4 and 16	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/07/18 15:22
S1	0	(Yu adj et adj al).inv.	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2005/06/17 10:21
S2	0	"Us-2004/0173794 A1"	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2005/06/17 10:22

S3	0	"2004/0173794"	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2005/06/17 10:22
54	27	"0173794"	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2005/06/17 10:26
S5	0	S4 and Yu	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2005/06/17 10:26
S6	3921	324/754.ccls.	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2005/06/17 10:27
S7	0	S6 and pad with bumb\$4 and test\$4	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2005/06/17 10:28
S8	346	S6 and pad with bump\$4 and test\$4	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2005/06/17 10:28
S9	297	S8 and wafer	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2005/06/17 10:53
S10	0	(crip\$4 adj line) with wafer	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2005/06/17 10:55
S11	1	(scrip\$4 adj line) with wafer	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2005/06/17 10:57
S12	1	(scrip\$4 near3 line) with wafer	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2005/06/17 10:57

		EAST Scare	,			
S13	3450	(scri\$4 near3 line) with wafer	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2005/06/17 14:49
S14	43	S13 and S6	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2005/06/17 14:44
S15	2	"20040173794"	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2005/06/17 14:49
S16	14773	324/754-765,158.1.ccls.	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2005/06/17 14:49
S17	123	(scribe near3 line) near3 pad with wafer	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2005/06/17 14:52
S18	9	S16 and S17	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2005/06/17 14:51
S19	10131	fang.inv.	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/07/18 10:45
S20	0	test\$4 adj (electrical adj characteristic with bump)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/07/18 10:46
S21	50	test\$4 with (electrical adj characteristic with bump)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/07/18 10:46
S22	6	S19 and S21	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/07/18 13:25

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REVOCATION OF POWER OF Filing Date 9/29/2004

REVOCATION OF POWER OF ATTORNEY WITH NEW POWER OF ATTORNEY AND

CHANGE OF CORRESPONDENCE ADDRESS

Application Number	10/953,291
Filing Date	9/29/2004
First Named Inventor	Mark Adam Bachman, et al.
Art Unit	2829
Examiner Name	Tung X. Nguyen
Attorney Docket Number	BACHMAN 3-11-16-173

I hereby revoke all previous powers of attorney given in the above-identified application.								
A Power of Attorney is submitted herewith.								
OR I here	171000							
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Please	Please change the correspondence address for the above-identified application to:							
	The address associated with Customer Number: 47396							
OR								
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Name	David L. Smi	ih	THE RESIDENCE OF THE PROPERTY	man fluctum interne		ungeneta estistares	And the second s	naktir an ka-lejuwa minguwan oki 50 denimbah kundulan di 20 denimbah di 20 denimb
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	es of all the lover ulted, see below	ntona or assigness of record	of the entire interest o	ir their rep	resentative(s)	are required. 9	ekilikan ibndu	forms if more than one
D Total								

This collection of Information is required by 97 CFR 1.39. The information is required to obtain or retain a banefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.11 and 1.14. This collection is estimated to take 3 minutes to complete, including getthering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments in the amount of time you require to complete this form end/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Abxandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. 8FND TO: Commissioner for Patents, P.O. Box 1450, Abxandria, VA 22313-1450.

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STATEMENT UNDER 37 CFR 3.73(b)						
Applicant/Patent Owner: Agere Systems Inc.						
Application No./Patent No./Control No.: 10/953,291	Filed/Issue Date: 9/29/2004					
Entitled: METHOD AND STRUCTURES FOR TESTING A SEMICOND BUMPING PROCESS	DUCTOR WAFER PRIOR TO PERFORMING A FLIP CHIP					
	, a					
	(Type of Assignee: corporation, partnership, university, government agency, etc.)					
1. the assignee of the entire right, title, and interest; or						
an assignee of less than the entire right, title and interest (The extent (by percentage) of its ownership interest is						
in the patent application/patent identified above by virtue of either	er:					
A. An assignment from the inventor(s) of the patent application in the United States Patent and Trademark Office at Reel original assignment is attached. OR	on/patent identified above. The assignment was recorded 016176 , Frame 0450 , or a true copy of the					
	ion/patent identified above, to the current assignee as follows:					
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The document was recorded in the United States F Reel, Frame	Patent and Trademark Office at					
3. From:To:						
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Additional documents in the chain of title are listed on a	a supplemental sheet.					
As required by 37 CFR 3.73(b)(1)(i), the documentary evidence of the chain of title from the original owner to the assignee was, or concurrently is being, submitted for recordation pursuant to 37 CFR 3.11. [NOTE: A separate copy (i.e., a true copy of the original assignment document(s)) must be submitted to Assignment Division in accordance with 37 CFR Part 3, to record the assignment in the records of the USPTO. See MPEP 302.08]						
The undersigned (whose tille is subplied below) is authorized to	act on behalf of the assignee. July 17, 2006					
Signature						
Charles W. Gaines	972-480-8800					
Printed or Typed Name	Telephone Number					
Attorney for Applicants Title						

This collection of information is required by 37 CFR 3.73(b). The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.11 and 1.14. This collection is estimated to take 12 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.

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JUNE 23, 2005

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BEUSSE BROWNLEE WOLTER MORA & MARIE, . PA JAMES H. BEUSSE 390 N. ORANGE AVENUE SUITE 2500 ORLANDO, FL 32801



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RECORDATION DATE: 01/27/2005

REEL/FRAME: 016176/0450 NUMBER OF PAGES: 5

BRIEF: ASSIGNMENT OF ASSIGNOR'S INTEREST (SEE DOCUMENT FOR DETAILS).

ASSIGNOR:

BACHMAN, MARK ADAM

DOC DATE: 12/15/2004

ASSIGNOR:

CHESIRE, DANTEL PATRICK

DOC DATE: 11/18/2004

ASSIGNOR:

KOOK, TAEHO

DOC DATE: 12/17/2004

ASSIGNOR:

MERCHANT, SAILESH M.

DOC DATE: 12/17/2004

ASSIGNEE:

AGERE SYSTEMS, INC. 1110 AMERICAN PARKWAY NE ALLENTOWN, PENNSYLVANIA 18109 016176/0450 PAGE 2

SERIAL NUMBER: 10953291

FILING DATE: 09/29/2004

PATENT NUMBER:

ISSUE DATE:

TITLE: METHOD AND STRUCTURES FOR TESTING A SEMICONDUCTOR WAFER PRIOR TO

'PERFORMING A FLIP CHIP BUMPING PROCESS

TONYA LEE, EXAMINER
ASSIGNMENT DIVISION
OFFICE OF PUBLIC RECORDS

01-27-2005
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To the Honorable Commissioner of Patents and Trademarks	s: Please record the attached orig	inal documents or copy there
1. Name of conveying party(ies): Mark Adam Bachman Daniel Patrick Chesire Taeho Kook Sailesh M. Merchant Additional name(s) of conveying party(ies) attached? Yes V No		of receiving party(ies)
3. Nature of conveyance: ✓ Assignment	Street Address: 111	0 American Parkwa
Other Bachman 12-15-2004 Chesire 11-18-2004 Kook 12-17-2004	City: Allentown	State: PA_Zip:_181
Execution Date: Merchant 12-17-2004 4. Application number(s) or patent number(s):	Additional name(s) & addre	ess(es) attached? Yes
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5. Name and address of party to whom correspondence concerning document should be mailed:	tached? Yes No 6. Total number of applica	ations and patents invol
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Additional numbers at 5. Name and address of party to whom correspondence concerning document should be mailed: Name: James H. Beusse Internal Address: Beusse Brownlee Wolter Mora & Maire, P.A Street Address: 390 N. Orange Avenue Suite 2500	tached? Yes No 6. Total number of applica 7. Total fee (37 CFR 3.41 Enclosed Authorized to be of applica 8. Deposit account number	etions and patents involutions\$ 40.00 Charged to deposit accorder:
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Commissioner of Patents & Trademarks, Box Assignments Washington, D.C. 20231

ASSIGNMENT AND AGREEMENT

For value received, We, MARK ADAM BACHMAN of Sinking Spring in the County of Berks and State of Pennsylvania; DANIEL PATRICK CHESIRE of Winter Garden, in the County of Orange and State of Florida; TAEHO KOOK of Orlando, in the County of Orange and State of Florida and SAILESH M. MERCHANT of Macungie in the County of Lehigh and State of Pennsylvania hereby sell, assign and transfer to Agere Systems, Inc., a corporation of the State of Delaware, having an office at 1110 American Parkway NE, Allentown, PA 18109, U.S.A., and its successors, assigns and legal representatives, the entire right, title and interest, for the United States of America, in and to certain inventions related to METHOD AND STRUCTURES FOR TESTING A SEMICONDUCTOR WAFER PRIOR TO PERFORMING A FLIP CHIP BUMPING PROCESS described in an application for Letters Patent of the United States. Application No. 10/953,291, filed September 29, 2004, and all the rights and privileges in said application and under any and all Letters Patent that may be granted in the United States for said inventions; and we also concurrently hereby sell, assign and transfer to Agere Systems, Inc. the entire right, title and interest in and to said inventions for all countries foreign to the United States, including all rights of priority arising from the application aforesaid, and all the rights and privileges under any and all forms of protection, including Letters Patent, that may be granted in said countries foreign to the United States for said inventions.

We authorize Agere Systems, Inc. to make application for such protection in its own name and maintain such protection in any and all countries foreign to the United States, and to invoke and claim for any application for patent or other form of protection for said inventions, without further authorization from us, any and all benefits, including the right of priority provided by any and all treaties, conventions, or agreements.

We hereby consent that a copy of this assignment shall be deemed a full legal and formal equivalent of any document which may be required in any country in proof of the right of Agere Systems, Inc. to apply for patent or other form of protection for said inventions and to claim the aforesaid benefit of the right of priority.

We request that any and all patents for said inventions be issued to Agere Systems, Inc. in the United States and in all countries foreign to the United States, or to such nominees as Agere Systems, Inc. may designate.

We agree that, when requested, we shall, without charge to Agere Systems, Inc. but at its expense, sign all papers, and do all acts which may be

necessary, desirable or convenient other forms of protection.	ent in connectio	n with said applications, patents, or
Date: 14/15/2004		Mark ADAM BACHMAN
United States of America)	
State of Pennsylvania) ss:	
County of)	
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		be the individual described in and moveledged execution of the same. Notary Public Notarial Seal Janet M. Garger, Notary Public Allentown, Lehigh County My Commission Expires Dec. 28, 2004 Member, Pennsylvania Association of Notaries
Date:	PARESIN .	DANIEL PATRICK CHESIRE
United States of America)	DANIEL PATRICK CHESIKE
State of Florida) ss:	
County of Orange)	
came Daniel Patrick Chesire, to	me known to	, 2004, before me personally be the individual described in and nowledged execution of the same.
	,	Notary Public

necessary, desirable or convenie other forms of protection.	nt in connectio	on with said applications, patents, or
Date:		MARK ADAM BACHMAN
United States of America State of Pennsylvania County of)) ss:)	
On this day of came Mark Adam Bachman , to who executed the foregoing instru	me known to iment, and ack	_, 2004, before me personally be the individual described in and knowledged execution of the same.
		Notary Public
Date: 11-18-2004 United States of America State of Florida County of Orange)) ss:)	Daniel PATRICK CHESIRE
On this 12 day of 10 day of 10 came Daniel Patrick Chesire , to who executed the foregoing instru	rember me known to ment, and ack	, 2004, before me personally be the individual described in and nowledged execution of the same. Notary Public
		Many V Carter My Commission DD347715 Expires September 20, 2008

Bachman 3-11-16-173

Date: <u>Dec. 17, 2004</u>	To
	TAEHO KOOK
United States of America) State of Florida Tomusloonia) ss: County of Orange Lehigh)	
On thisday of	, 2004, before me personally he individual described in and who owledged execution of the same.
	Notary Public Notarial Seal Janet M. Garger, Notary Public Allentown, Lehigh County My Commission Expires Dec. 28, 2004 Member, Pennsylvania Association of Notaries
Date: 12 Dec 0 4	SAILESH M. MERCHANT
United States of America) State of Pennsylvania) ss: County of)	
On thisday of	
	Notarial Seal Janet M. Garger, Notary Public Allentown, Lehigh County My Commission Expires Dec 28, 2004 Member, Pennsylvania Association of Notaries

Agere Systems, Inc. 1110 American Parkway NE Allentown, Pennsylvania 18109

Electronic Acknowledgement Receipt					
EFS ID:	1116060				
Application Number:	10953291				
Confirmation Number:	2052				
Title of Invention:	Method and structures for testing a semiconductor wafer prior to performing a flip chip bumping process				
First Named Inventor:	Mark Adam Bachman				
Customer Number:	29391				
Filer:	Charles W. Gaines/Elizabeth Schumacher				
Filer Authorized By:	Charles W. Gaines				
Attorney Docket Number:	Bachman 3-11-16-173				
Receipt Date:	17-JUL-2006				
Filing Date:	29-SEP-2004				
Time Stamp:	17:37:49				
Application Type:	Utility				
International Application Number:					
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File Listing:

Document Number	Document Description	File Name	File Size(Bytes)	Multi Part	Pages
1	Power of Attorney (may include Associate POA)	POA.pdf	152007	no	1

Warnings:								
Information:								
2	Assignee showing of ownership per 37 CFR 3.73(b).	Statement_373b.pdf	464796	no	8			
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If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application.

National Stage of an International Application under 35 U.S.C. 371

If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.

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	FORM	L	Art Unit		Adam Bachman
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	Affidavits/declaration(s)		ange of Correspondence		Status Letter
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Firm Name	Beusse Wolter San	ks Moi	ra & Maire. P.A		
Signature		77			
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Printed name	Enrique J. Mora				
Date	May 3, 2006			Reg. No.	36,875

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Kathy L. Tissue

Typed or printed name

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May 3, 2006

Date

PTO/SB/17 (12-04)

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		2004. iations Act, 2005 (H.R. 4818).		Complete i					
		Application Number	er 10/953,2	91					
FEE TR	LANS	SMITTAL	Filing Date	09/29/20	04				
Fo	r FY 2	005	First Named Inven	tor Mark A	dam Bachman et al.				
			Examiner Name	NGUYE	N, Tung X.				
Applicant claims small			Art Unit	2829					
TOTAL AMOUNT OF PAY	MENT (\$	500.00	Attorney Docket N	o. Bachma	n 3-11-16-173				
METHOD OF PAYMENT (check all that apply)									
Deposit Account	Deposit Accou	Money Order No	Deposit Acco	unt Name:					
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FEE CALCULATION									
1. BASIC FILING, SEA	FILING			EXAMINATION I Small E					
Application Type	Fee (\$)	Fee (\$) Fee (Small Entity S) Fee (\$)	Fee (\$) Fee (\$					
Utility	300	150 500	250	200 100					
Design	200	100 100	50	130 65					
Plant	200	100 300	150	160 80					
Reissue	300	150 500	250	600 300					
Provisional	200	100 0	0	0 0					
2. EXCESS CLAIM FEES Fee Description Each claim over 20 or, for Reissues, each claim over 20 and more than in the original patent Each independent claim over 3 or, for Reissues, each independent claim more than in the original patent Multiple dependent claims Small Entity Fee (\$) Fee (\$) 25 20 100 Multiple dependent claims									
Total Claims - 20 or HP = HP = highest number of total Indep. Claims - 3 or HP =	claims paid fo	x = or, if greater than 20		Multiple Depende Fee (\$)	Fee Paid (\$)				
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4 OTHER FEE(S)					Fees Paid (\$)				

SUBMITTED BY		-
Signature	Registration No. 36,875	Telephone 407-926-7705
Name (Print/Type)	Enrique Mora	Date 5/3/2006

Non-English Specification, \$130 fee (no small entity discount)

Other: Appeal Brief Fees

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\$500.00

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

e: Application of:

Applicants: Mark Adam Bachman et al)

Serial No.: 10/953,291)

Filed: 09/29/2004

Title: Method and Structures for Testing)

A Semiconductor Wafer Prior to Performing a Flip Chip Bumping

Process

Examiner: NGUYEN, Tung X.

Group Art Unit: 2829

Confirmation No.: 2052

Atty. Docket No.: Bachman

3-11-16-173

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APPELLANT'S BRIEF UNDER 37 CFR 41.10

This brief is in furtherance of the Notice of Appeal filed in this application on March 14, 2006.

1. REAL PARTY IN INTEREST - 37 CFR 41.37(c)(1)(i)

The real party in interest in the present Appeal is the assignee of record of the present application, Agere Systems, Inc.

2. RELATED APPEALS AND INTERFERENCES - 37 CFR 41.37(c)(1)(ii)

To the best of our knowledge, there is no other appeal, interference or judicial proceeding that is related to or that will directly affect, or that will be directly affected by, or that will have a bearing on the Board's decision in this Appeal.

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3. STATUS OF CLAIMS - 37 CFR 41.37(c)(1)(iii)

Claims cancelled: none.

Claims withdrawn but not cancelled: none.

Claims pending: 1-9.
Claims allowable: 6.

Claims rejected: 1-5 and 7-9.

Claim rejections appealed: 1-5 and 7-9.

4. STATUS OF AMENDMENTS - 37 CFR 41.37(c)(1)(iv)

There is no amendment filed subsequent to final rejection.

5. SUMMARY OF CLAIMED SUBJECT MATTER- 37 CFR 41.37(c)(1)(v)

The present invention generally relates to structures and techniques for enabling wafer level testing prior to performing a bumping process in a flip chip assembly. FIG. 2 illustrates a conductive test pad 22 integrally constructed with a conductive bonding pad 24. This arrangement provides at least the following advantages: conductive test pad 22 provides a respective probe region 26 where a probe tip may be placed for performing, for example, wafer level testing. The bonding pad 24 includes a bump region 28 that is no longer subject to mechanical contact with the probe tip and resulting surface irregularities. It is envisioned that since the test pad and bonding pad comprise an integral structure that no longer requires interconnect lines, and avoids or substantially reduces propagation delays in test signals passing therethrough, an interface assembly embodying aspects of the present invention should lead to more reliable and accurate test results.

Claim 1

Independent claim 1 is directed to an interface assembly (20) for a semiconductor wafer. The interface assembly comprises a flip chip bonding pad (24) including a region (28) for performing a bumping process. The interface assembly further comprises a test pad (22) integrally constructed with the

bonding pad. The test pad is co-planar relative to the flip chip bonding pad and includes a probe region (26) for performing wafer-level testing prior to performing a bumping process. See paragraph 14 and FIG. 2 of the publication document for the present application.

Claim 9

Independent claim 9 is directed to a method for testing a semiconductor wafer prior to performing a flip chip bumping process. The method comprises providing a flip chip bonding pad (24) having a region (28) for performing the bumping process. The method further comprises integrally constructing a test pad (22) with the bonding pad. The test pad is disposed coplanar with the flip chip bonding pad. The test pad includes a probe region (26) for performing a wafer test prior to performing the bumping process. See paragraph 14 and FIG. 2 of the publication document for the present application.

- 6. GROUNDS OF REJECTION TO BE REVIEWED UPON APPEAL 37 CFR 41.37(c)(1)(vi)
- A) Whether claims 1-5, and 7-9, stand rejected under 35 U.S.C. §102(e) as being anticipated by publication No. US 2003/0094966 (hereinafter Fang).

7. APPENDICES

A copy of the claims 1-5, and 7-9 involved in this appeal is attached as a claims appendix under 37 CFR 41.37(c)(1)(viii). No evidence appendix under 37 CFR 41.37(c)(1)(xi) or related proceedings appendix under 37 CFR 41.37(c)(1)(x) is required.

37 CFR 41.37(c)(1)(vii)

A) Rejection of claims 1-5, and 7-9, under 35 U.S.C. §102(e) as being anticipated by publication No. US 2003/0094966 (hereinafter Fang).

Appellant argues that Fang does not support a *prima facie* case of anticipation for claims 1-5 and 7-9 because Fang fails to teach each of the claimed elements and/or operational relationships. With regard to the rejections applied against claims 1-5 and 7-9, it is appellants' belief that not all of the rejected claims stand or fall together. More specifically, apparatus claims 1-5, 7 and 8, stand together. However, claim 9, directed to a method for testing a semiconductor wafer prior to performing a flip chip bumping process, should be grouped separately from claims 1-5, 7 and 8 for purposes of this appeal.

The test for establishing a *prima facie* case of anticipation under §102 "requires the presence in a single prior art reference of each and every element of the claimed invention, arranged as in the claim." (<u>Lindemann Maschinenfabrik GMbH v. American Hoist and Derrick Co.</u>, 730 F.2d 1452, 221 USPQ 481,485 (Fed. Cir. 1984)). Furthermore, "there must be no difference between the claimed invention and the referenced disclosure, as viewed by a person of ordinary skill in the field of the invention." <u>Scripps Clinic and Research Found. v. Genentech Inc.</u>, 927 F.2d 1565, 18 USPQ2d 1001, 1010 (Fed. Cir. 1991)). Absence from the reference disclosure of any claim element and/or operational interrelationship negates anticipation under §102.

A.1) Arguments Regarding Claim 1

The Examiner relies on Fang to reject claim 1 under 35 U.S.C. §102. Fang is directed to a method for testing electrical characteristics of bumps. (See Abstract of Fang). Accordingly, Fang describes bumps 34 and 35 electrically interconnected by metal traces 32 and 33 respectively. It is respectfully submitted that the Examiner mischaracterizes that Fang discloses in FIG. 3 a flip chip bonding pad 32. In fact, Fang describes that structures 32 and 33 are metal traces for electrically interconnecting three separate bumps 31, 34, and 35. See

page 1 of Fang, lines 5-7 of paragraph 15. A metal trace is distinct from a flip chip bonding pad. As shown in FIG. 4, metal traces 32 and 33 are coated with a passive layer 42 for preventing damage due to moisture or particles. See page 2 of Fang, lines 9-11, excerpt of paragraph 16. Accordingly, the metal traces 32 and 33 are not physically accessible for testing. As noted above, Fang merely uses metal traces 32 and 33 to electrically connect three separate bumps. Applicant understands that one of those separate bumps is used for bump testing. However, it is plainly clear that the test bump 31 is physically separate from the bumps 34 and 35 being tested through the test bump. Fang fails to describe a flip chip bonding pad having a test pad integrally constructed therewith, as set forth in claim 1. Accordingly, it is not believed that there is any description or suggestion in Fang that meets the structural and/or operational relationships set forth in appellant's claim 1. Anticipation under 35 U.S.C. §102 requires that "The identical invention must be shown in as complete detail as contained in the ...claim." (In re Bond, 910 F.2d 831, 15USPQ2d 1566 (Fed. Cir. 1990)). Accordingly, it is submitted that Fang fails to anticipate claim 1.

Moreover, applicant submits that Fang teaches away from the claimed invention being that Fang describes bumps which are electrically interconnected by metal traces (e.g., interconnect lines). This is the antithesis of the claimed structure that comprises a test pad integrally constructed with the bonding pad. For example, since the test pad and bonding pad comprise an integral structure that no longer requires interconnect lines, this avoids or substantially reduces propagation delays in test signals passing therethrough, and this should lead to more reliable and accurate test results. Accordingly, although not raised by the Examiner, it is felt that Fang also fails to render obvious claim 1.

Claims 2-5 and 7 depend from claim 1 and thus incorporate the structural and/or operational relationships set forth in claim 1 plus their own recitations. It is respectfully submitted that Fang also fails to anticipate such claims under the §102 statutory requirements and these rejections should be withdrawn.

A.2) Arguments Regarding Claim 9

With regard to independent claim 9, directed to a method for testing a semiconductor prior to performing a flip chip bumping process. The method in part recites providing a flip chip bonding pad having a region for performing the bumping process. The method further recites integrally constructing a test pad with the bonding pad. As discussed, Fang fails to describe the foregoing structural and/or operational relationships, and consequently, Fang fails to anticipate this claim under the §102 statutory requirements and this rejection should also be withdrawn.

Moreover, applicant submits that Fang teaches away from the claimed invention being that Fang describes bumps which are electrically interconnected by metal traces (e.g., interconnect lines). This is the antithesis of the claimed method that comprises integrally constructing a test pad with the bonding pad. For example, since the test pad and bonding pad comprise an integral structure that no longer requires interconnect lines, this avoids or substantially reduces propagation delays in test signals passing therethrough, and this should lead to more reliable and accurate test results. Accordingly, although not raised by the Examiner, it is felt that Fang also fails to render obvious claim 9.

Respectfully submitted,

Enrique J. Mora, Esquire Registration No. 36.875

Beusse, Wolter, Sanks, Mora & Maire, P.A.

390 North Orange Avenue, Suite 2500

Orlando, Florida 32801 Telephone: (407) 926-7705 Facsimile: (407) 926-7720

CLAIMS APPENDIX 37 CFR 41.37(c)(1)(viii)

- 1. An interface assembly for a semiconductor wafer, said interface assembly comprising:
- a flip chip bonding pad including a region for performing a bumping process; and
- a test pad integrally constructed with said bonding pad, said test pad being co-planar relative to said flip chip bonding pad and including a probe region for performing wafer-level testing prior to performing said bumping process.
- 2. The interface assembly of claim 1 wherein said test pad may be disposed anywhere along a periphery of said bonding pad.
- 3. The interface assembly of claim 1 wherein said bonding pad comprises a shape selected from the group consisting of a polygonal shape, and a circular shape.
- 4. The interface assembly of claim 1 wherein said test pad comprises a shape selected from the group consisting of a polygonal shape, and a circular shape.
- 5. The interface assembly of claim 1 further comprising a first metal redistribution layer electrically connected to said bonding and test pads, and being co-planar with one another.

- 7. The interface assembly of claim 1 wherein the region to be bumped is defined by a first opening in a passivation layer.
- 8. The interface assembly of claim 7 wherein the probe region is defined by a second opening in said passivation layer, said first and second openings being spaced apart from one another.
- 9. A method for testing a semiconductor wafer prior to performing a flip chip bumping process, said method comprising:

providing a flip chip bonding pad having a region for performing said bumping process;

integrally constructing a test pad with said bonding pad; and

disposing said test pad coplanar with said flip chip bonding pad, said test pad including a probe region for performing a wafer test prior to performing said bumping process.

CERTIFICATE OF MAILING

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Kathy L. Tissue J. Lissue

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Docket Number (Optional)

NOTICE OF APPEAL FROM THE EXAMINER TO

THE BOARD OF PATENT APPEALS AND INTERFER	KENCES	Bachman 3-	11-10-173 (383)			
I hereby certify that this correspondence is being deposited with the United States Postal Service with sufficient postage as first class mail in an envelope addressed to "Commissioner for Patents, P.O. Box	In re Applicat Mark Adai	ion of m Bachman				
1450, Alexandria, VA 22313-1450" [37 CFR 1.8(a)] on	Application N 10/953,29		Filed 09/29/2004			
SignatureKathy L. Lissue		and Structures for Testir ng a Flip Chip Bumping	g a Semiconductor Wafer Prior to Process			
Typed or printed Kathy L. Tissue	Art Unit 2829		aminer NGUYEN, Tung X.			
Applicant hereby appeals to the Board of Patent Appeals and Interferen	ces from the last o	decision of the exami	ner.			
The fee for this Notice of Appeal is (37 CFR 41.20(b)(1))	٠	\$	500.00			
Applicant claims small entity status. See 37 CFR 1.27. Therefore, by half, and the resulting fee is:	the fee shown abo	ove is reduced	3			
A check in the amount of the fee is enclosed.			·			
Payment by credit card. Form PTO-2038 is attached.						
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The Director is hereby authorized to charge any fees which may b to Deposit Account No I have enclose	e required, or creded a duplicate copy	dit any overpayment y of this sheet.				
A petition for an extension of time under 37 CFR 1.136(a) (PTO/S	B/22) is enclosed.					
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I am the			1			
applicant/inventor.		$2 \rightarrow 7$				
assignee of record of the entire interest. See 37 CFR 3.71. Statement under 37 CFR 3.73(b) is enclosed. (Form PTO/SB/96)	Enriq	ye√J. Mora	printed name			
attorney or agent of record. Registration number		26-7705				
		Telepho	one number			
attorney or agent acting under 37 CFR 1.34. Registration number if acting under 37 CFR 1.34.	Marc	h 14, 2006				
NOTE: Signatures of all the inventors or assignees of record of the entire interest or their representative(s) are required. Submit multiple forms if more than one signature is required, see below.						
Total of farms are submitted						
*Total of forms are submitted.						

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are required to respond to a collection of information unless it displays a valid OMB control number. Application Number 10/953.291 **TRANSMITTAL** Filing Date 09/29/2004 First Named Inventor **FORM** Mark Adam Bachman Art Unit 2829 **Examiner Name** NGUYEN, Tung X. (to be used for all correspondence after initial filing)

Tota	al Number of	Pages in	This Submission			omey booket Num	Bachm	an 3-1	1-16-1	173 (383)	
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Printed	l name	Enriq	ue J Mora			·					
Date March 14, 2006						Reg. No.	36,8	375	-		
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Typed	or printed r	name	Kathy L.Tiss	sue	T			-	Date	March 14, 2006	

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PETITION	FOR EXTENSION OF TIME UNDER :	Docket Number (Optional)					
(Fees	FY 2005 pursuant to the Consolidated Appropriations Act, 2	Bachman 3-11-16-173 (383)					
Application	Number 10/953,291		Filed 09/29/2004				
For Met	hod and Structures for Testing a Semice	onductor Wafer Prior	to Performing a Flip Cl	nip Bumping Process			
Art Unit 2	2829		Examiner NGUYEN,	Гung X.			
This is a req application.	uest under the provisions of 37 CFR 1.136	(a) to extend the perio	d for filing a reply in the a	bove identified			
The request	ed extension and fee are as follows (check	time period desired ar	nd enter the appropriate f	fee below):			
		<u>Fee</u>	Small Entity Fee	100.00			
~	One month (37 CFR 1.17(a)(1))	\$120	\$60	<u>\$ 120.00</u>			
	Two months (37 CFR 1.17(a)(2))	\$450	\$225	\$			
	Three months (37 CFR 1.17(a)(3))	\$1020	\$510	\$			
	Four months (37 CFR 1.17(a)(4))	\$1590	\$795	\$			
	Five months (37 CFR 1.17(a)(5))	\$2160	\$1080	\$			
Applica	nt claims small entity status. See 37 CFR 1	.27.					
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The Di	rector has already been authorized to o	charge fees in this a	oplication to a Deposit	Account.			
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I am the	applicant/inventor.						
	assignee of record of the entire	interest. See 37 CF	R 3.71.				
	Statement under 37 CFR 3.1	` '	•				
	attorney or agent of record. Reg	gistration Number	36,875	_			
	attorney or agent under 37 CFF	R 1.34. · 37 CFR 1.34					
	March 14, 2006						
	Signature		Dat	te			
Enrig	dé J. Mora		(407) 926-77	05			
	Typed or printed name		Telephone	Number			
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Total	of forms are	submitted.					

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390 N. Orange Avenue, Suite 2500 Orlando, Florida 32801 Telephone (407) 926-7700 Facsimile (407) 926-7720 www.felawfl-com <u>OP COUNSPL</u> JACKSON O. BROWNLER JOSEPH FISCHER

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FROM DATE Enrique J. Mora March 15, 2006

RE :

Serial Number 10/953,291; filed 09/29/2004

Bachman 3-11-16-173 (383)

VIA FACSIMILE ONLY

Attached please find for entry into the above-referenced application:

- 1) Information Disclosure Statement Transmittal (2 pages); and
- 2) IDS Form 1449.

Yours truly,

Reg. #36,875

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Application No. 10/953,291

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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re: Application of:

Mark Adam Bachman

Group Art Unit: 2829

Serial No.:

10/953,291

Examiner: NGUYEN, Tung X.

Filed:

09/29/2004

For:

Method and Structures for Testing a Semiconductor Wafer Prior to Performing a

Flip Chip Bumping Process

INFORMATION DISCLOSURE STATEMENT TRANSMITTAL

1.	Pursuant to 37 CFR 1.97(b)
	(within 3 months of filing or prior to 1st Office Action)

2. Certification Pursuant to 37 CFR 1.97(c) (before Final Office Action or Allowance)

3. Petition, Certification & Petition Fee Payment Pursuant to 37 CFR 1.97(d) (after Final Office Action or Allowance but before issue fee payment)

Commissioner of Patents P.O. Box 1450 Alexandria, VA 22313-1450

Sir:

The following are submitted in the above-identified application in compliance with 37 CFR 1.97 & 1.98:

A list of documents on form PTO-1449 is enclosed herewith.

This paper is submitted in accordance with:

5. 37 CFR 1.97(b): [within 3 months of filing or prior to 1st Office Action]

Application No. 10/953,291

	6.	37 CFR 1.97(c): [before Final office Action or Allowance, whichever is earlier; and				
\boxtimes	7.	The required certification made in item 10 below; or				
	8.	The \$180.00 fee specified in 37 CFR §1.17(p) for submission of this Information Disclosure Statement.				
	9. fee pa	37 CFR §1.97(d): [after Final Office Action or Allowance, but before issue ayment]; and				
		a)	This is a petition for consideration of the subject Information Disclosure Statement. The petition fee (\$180.00) required by 37 CFR 1.17(i)(1) is authorized in item 11 below. (Direct this letter to: "Attention: PETITIONS EXAMINER" and, if applicable, include batch locator information: e.g., "Allowed Files, Batch, Date of Allowance"), and			
		þ)	The required Certification is stated in item 10 below.			
\boxtimes	10.	Certific	cation			
		a)	Each item of information contained in this Statement was cited in a communication from a foreign patent office in a counterpart foreign application not more than three months prior to the filing of this Statement;			
or						
		b) after n CFR 1	No item of information contained in this Statement was cited in a communication from a foreign patent office in a counterpart foreign application or, to the knowledge of the person signing this document making reasonable inquiry, was known to any individual designated in 37.56(c) more than three (3) months prior to the filing of this Statement.			
	11.	Please Disclo	e charge all applicable fees associated with the submittal of this Information sure Statement to Deposit Account No			
			Respectfully submitted,			
			Enrique d. Mora, Esquire Reg No. 38,875 Beusse Wolter, Sanks, Mora & Maire, P.A. 390 North Orange Avenue, Suite 2500 Orlando, FL 32801 Telephone: (407) 926-7705 Facsimile: (407) 926-7720 Email: emora@iplawfl.com			

PTO/SB/08A (05-03)

Approved for use through 07/31/2006. OMB 0651-0031

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Under the Paper work Reduction Act of 1985, no pe			Complete if Known		
Substitute for form 1449B/PTO			Application Number	10/953,291	
INFORMATION DISCLOSURE STATEMENT BY APPLICANT (Use as many sheets as necessary)				09/29/2004	
				Mark Adam Bachman	
			Group Art Unit	2829	
			Examiner Name	NGUYEN, Tung X.	
Sheet 1	of	,	Attorney Docket Number	Bachman 3-11-16-173 (383)	

			I.S. PATENT DO		D Oak was I ass Milhorn
Examiner Initials	Cite No.1	Document Number	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear
	l	Number-Kind Code ^{24 Mount}		V. ==	
	01	US-6,359,342 B1	03-19-2002	Yuan et al.	
	02	US 2004/0161865 A1	08-19-2004	Yu et al.	
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		FOREIGN P	ATENT DOCU	MENTS		
Examiner Initials	Cite No.1	Foreign Patent Document Country Code3-Number3-King Code3(if known)	Publication Data MM-DD-YYYY	Name of Patenties or Applicant of Cred Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear	70
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Signature	Considered
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If you need assistance in completing the form, call 1-800-PTO-9199 (1-800-786-9199) and select option 2.

EXAMINER: Initial if reterence considered, whether or not citation is in conformance with MPEP 609. Draw line through citation if not in conformance

EXAMINER: Initial if reterance considered, whether or not gration is in conformance with MPEP 609. Draw line through criation if not in conformance and not considered. Include copy of this form with next communication to applicant.

Applicant's unique citation designation number (optional). Applicant is to place a check mark ners if English Language Translation is attached.

This collection of information is required by 37 CFR 1.98. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 2 hours to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the Individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief information Officer, U.S. Patent and Trademark Office, U.S. Pepartment of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. FEES OR COMPLETED FORMS TO THIS ADDRESS. SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.



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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO
10/953,291	09/29/2004	Mark Adam Bachman	Bachman 3-11-16-173	2052
29391	29391 7590 02/09/2006		EXAMINER	
BEUSSE BROWNLEE WOLTER MORA & MAIRE, P. A. 390 NORTH ORANGE AVENUE			NGUYEN,	TUNG X
SUITE 2500			ART UNIT	PAPER NUMBER
ORLANDO,	FL 32801	2829		
			DATE MAIL ED: 02/09/2006	4

Please find below and/or attached an Office communication concerning this application or proceeding.

Advisory Action Before the Filing of an Appeal Brief

Application No.	Applicant(s)	
10/953,291	BACHMAN ET AL.	
Examiner	Art Unit	
Tung X. Nguyen	2829	

The MAILING DATE of this communication appears on the cover sheet with the correspondence address
THE REPLY FILED 17 January 2006 FAILS TO PLACE THIS APPLICATION IN CONDITION FOR ALLOWANCE.
1. The reply was filed after a final rejection, but prior to or on the same day as filing a Notice of Appeal. To avoid abandonment of this application, applicant must timely file one of the following replies: (1) an amendment, affidavit, or other evidence, which places the application in condition for allowance; (2) a Notice of Appeal (with appeal fee) in compliance with 37 CFR 41.31; or (3) a Request for Continued Examination (RCE) in compliance with 37 CFR 1.114. The reply must be filed within one of the following time periods:
a) \boxtimes The period for reply expires $\underline{3}$ months from the mailing date of the final rejection.
b) The period for reply expires on: (1) the mailing date of this Advisory Action, or (2) the date set forth in the final rejection, whichever is later. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of the final rejection. Examiner Note: If box 1 is checked, check either box (a) or (b). ONLY CHECK BOX (b) WHEN THE FIRST REPLY WAS FILED WITHIN TWO MONTHS OF THE FINAL REJECTION. See MPEP 706.07(f).
Extensions of time may be obtained under 37 CFR 1.136(a). The date on which the petition under 37 CFR 1.136(a) and the appropriate extension fee have been filed is the date for purposes of determining the period of extension and the corresponding amount of the fee. The appropriate extension fee under 37 CFR 1.17(a) is calculated from: (1) the expiration date of the shortened statutory period for reply originally set in the final Office action; or (2) as set forth in (b) above, if checked. Any reply received by the Office later than three months after the mailing date of the final rejection, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).
NOTICE OF APPEAL 2. The Notice of Appeal was filed on A brief in compliance with 37 CFR 41.37 must be filed within two months of the date of filing the Notice of Appeal (37 CFR 41.37(a)), or any extension thereof (37 CFR 41.37(e)), to avoid dismissal of the appeal. Since a Notice of Appeal has been filed, any reply must be filed within the time period set forth in 37 CFR 41.37(a). AMENDMENTS
3. The proposed amendment(s) filed after a final rejection, but prior to the date of filing a brief, will <u>not</u> be entered because (a) They raise new issues that would require further consideration and/or search (see NOTE below);
 (b) ☐ They raise the issue of new matter (see NOTE below); (c) ☐ They are not deemed to place the application in better form for appeal by materially reducing or simplifying the issues for appeal; and/or
(d) ☐ They present additional claims without canceling a corresponding number of finally rejected claims. NOTE: (See 37 CFR 1.116 and 41.33(a)).
4. The amendments are not in compliance with 37 CFR 1.121. See attached Notice of Non-Compliant Amendment (PTOL-324).
5. Applicant's reply has overcome the following rejection(s):
6. Newly proposed or amended claim(s) would be allowable if submitted in a separate, timely filed amendment canceling the
non-allowable claim(s). 7. For purposes of appeal, the proposed amendment(s): a) will not be entered, or b) will be entered and an explanation of how the new or amended claims would be rejected is provided below or appended. The status of the claim(s) is (or will be) as follows:
Claim(s) allowed: Claim(s) objected to: <u>6</u> . Claim(s) rejected: <u>1-5 and 7-9</u> .
Claim(s) withdrawn from consideration: AFFIDAVIT OR OTHER EVIDENCE
8. The affidavit or other evidence filed after a final action, but before or on the date of filing a Notice of Appeal will <u>not</u> be entered because applicant failed to provide a showing of good and sufficient reasons why the affidavit or other evidence is necessary and was not earlier presented. See 37 CFR 1.116(e).
9. The affidavit or other evidence filed after the date of filing a Notice of Appeal, but prior to the date of filing a brief, will <u>not</u> be entered because the affidavit or other evidence failed to overcome <u>all</u> rejections under appeal and/or appellant fails to provide a showing a good and sufficient reasons why it is necessary and was not earlier presented. See 37 CFR 41.33(d)(1).
10. The affidavit or other evidence is entered. An explanation of the status of the claims after entry is below or attached. REQUEST FOR RECONSIDERATION/OTHER
11. The request for reconsideration has been considered but does NOT place the application in condition for allowance because: See Continuation Sheet.
12. Note the attached Information Disclosure Statement(s). (PTO/SB/08 or PTO-1449) Paper No(s) 13. Other:
<u>.</u>

Continuation of 11. does NOT place the application in condition for allowance because: Applicant's response filed 1/17/06 have been fully considered but they are not persuasive.

In re pages 2-3, Applicant argues that Fang fails to describe a flip chip bonding pad having a test pad integrally constructed therewith. In response, Examiner respectfully disagrees about that. In the wafer manufacture process for conducing the processes, such as exposure, developing and etching; forming the pads, are electrically connected to the other pads on the neighboring chips, on the scribe line (13 of figure 3) located between mutually neighboring chips (36, 37 of figure 3); after the flip-chip bumping processing, the wafer being formed with bumps (31, 34, 35 of figure 3) on all the pads on chips (36, 37 of figure 3) and on the scribe lines (col. 1, lines 1-7). Therefore, Fang disclose to describe a flip chip bonding pad (32 of figure 3) having a test pad at the end of bonding pad (32 of figure 3) for processing the bump (31, 34, 35 of figure 3) to testing the neighboring chips without contacting the bump on the chip.

JERMELE HOLLINGTON PRIMARY EXAMINER

AU2829

02/01/06

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TO

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Commissioner for Patents USPTO

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FAX No.

1-571-273-8300

No of PAGES

5 (including cover sheet)

FROM :

Enrique J. Mora January 17, 2006

DATE :
RE :
ATTY. DOCKET NO:

Serial Number 10/953,291; filed 09/29/2004

Bachman 3-11-16-173

VIA FACSIMILE ONLY

Attached please find for entry into the above-referenced application:

Reply/Response Under CFR 1.116 – responsive to Final Office Action dated 11/14/2005 - (4 pages).

Yours truly,

Certificate of Transmission

I hereby certify that this correspondence is being facsimile transmitted to the United States Patent and Trademark Office, Fax No. 571-273-830()

on January 17, 2006.

Kathy L. Tassue

Bachman 3-11-16-173

Certificate of Facsimile

I hereby certify that this correspondence is being Forwarded to Fax No. 571-273-8300 and addressed to the Commissioner for Patents, MAIL STOP AMENDMENT, Alexandria, VA 22313-1450 on

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JAN 17 2006

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re: Application of:

Mark Adam Bachman et al) Applicants:

10/953,291 Serial No.:

Filed: 09/29/2004

Title: Method and Structures for Testing)

A Semiconductor Wafer Prior to Performing a Flip Chip Bumping

Process

Examiner: NGUYEN, Tung X.

Group Art Unit: 2829

Confirmation No.: 2052

Atty. Docket No.: Bachman

3-11- 16-173

Mail Stop AMENDMENT Commissioner for Patents P.O. Box 1450 Alexandria, VA 22313-1450

REPLY/RESPONSE UNDER CFR 1.116

This Reply is in response to the Final Office Action dated as mailed November 14, 2005 and having a timely two-month response date of January 17, 2006 (given that the January 14, 2006 fell on a Saturday and Monday, January 16, 2006 was a federal holiday).

Please amend the above-identified application as follows:

Remarks/Arguments begin on page 2 of this paper.

Bachman 3-11-16-173

REMARKS/ARGUMENTS

Claims 1-5, and 7-9, stand rejected as being anticipated by publication No. US 2003/0094966 (hereinafter Fang). Applicant appreciates the recognition of allowable subject matter in claim 6, which presently stands objected to. As described in greater detail below, applicant strongly believes that the Office Action misconstrues Fang and requests reconsideration of the rejections and objections.

The Office Action Misconstrues Fang's Disclosure

The Office Action states that Fang discloses in FIG. 3 a flip chip bonding pad 32. In fact, Fang describes that structures 32 and 33 are metal traces for electrically interconnecting three separate bumps 31, 34, and 35. See page 1 of Fang, lines 5-7 of paragraph 15. A metal trace is distinct from a flip chip bonding pad. This distinction would be readily understood in the art. As shown in FIG. 4, metal traces 32 and 33 are coated with a passive layer 42 for preventing damage due to moisture or particles. See page 2 of Fang, lines 9-11, excerpt of paragraph 16. Accordingly, the metal traces 32 and 33 are not physically accessible for testing. As noted above, Fang merely uses metal traces 32 and 33 to electrically connect three separate bumps. Applicant understands that one of those separate bumps is used for bump testing. However, it is plainly clear that the test bump 31 is physically separate from the bumps 34 and 35 being tested through the test bump. Fang fails to describe a flip chip bonding pad having a test pad integrally constructed therewith, as set forth in claim 1. Applicant advantageously avoids the need of metal traces for electrically interconnecting the test pad with the bonding pad.

Bachman 3-11-16-173

The Office Action Disregards Structural and/Operational Relationships Recited in the Claims

Fang describes that the separate bumps 31, 34 and 35 are structures formed after a flip chip bumping process is performed. See Fang page, lines 12-14, excerpt of paragraph 16. This is inapposite to the operational and/or structural relationships recited in claim 1 that specifically recite a flip chip bonding pad and a test pad for performing testing prior to performing the bumping process. This is another notable difference between the claimed invention and Fang that the Office Action simply disregards. It is noted that the improved test structure enabled by applicant's invention could be used after performing the bumping process. In this case, the resulting structure would be a bump with a test pad integrally constructed therewith. That is, a bump (in lieu of the bonding pad) with an integral test pad. The key point being that the resulting post-bumping structure would continue to be entirely different from the structure of Fang, which merely provides three separate bumps. None of the bump structures of Fang includes a bump and a test pad integrally constructed with the bump being tested.

In view of the foregoing remarks, it is respectfully submitted that Fang fails to anticipate or otherwise render obvious claim 1, and applicant kindly requests that this basis of rejection be removed.

Claims 2-5 and 7 depend from claim 1 and thus incorporate the structural and/or operational relationships set forth in claim 1 plus their own recitations. It is respectfully submitted that Fang also fails to anticipate such claims under the §102 statutory requirements and these rejections should be withdrawn.

Claim 9 is directed to a method for testing a semiconductor prior to performing a flip chip bumping process. The method in part recites providing a flip chip bonding pad having a region for performing the bumping process. The method further recites integrally constructing a test pad with the bonding pad. As discussed, Fang fails to describe the foregoing structural and/or operational relationships, and consequently, Fang fails to anticipate this claim under the §102 statutory requirements and this rejection should also be withdrawn.

Bachman 3-11-16-173

It is respectfully submitted that each of the claims pending in this application recites patentable subject matter and it is further submitted that such claims comply with all statutory requirements and thus each of such claims should be allowed.

* * * * * * *

The Examiner is invited to call the undersigned if clarification is needed on any aspects of this Reply/Amendment, or if the Examiner believes a telephonic interview would expedite the prosecution of the subject application to completion.

Respectfully submitted,

Enrique d. More

Registration No. 36,875

Beusse Brownlee Wolter Mora & Maire, P.A.

390 N. Orange Avenue, Suite 2500

Orlando, FL 32801

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United States Patent and Trademark Office



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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/953,291	09/29/2004	Mark Adam Bachman	Bachman 3-11-16-173	2052
29391	7590 11/14/2005		EXAM	INER
	OWNLEE WOLTER MO	NGUYEN, TUNG X		
390 NORTH	ORANGE AVENUE			
SUITE 2500			ART UNIT	PAPER NUMBER
ORLANDO,	ORLANDO, FL 32801			
	•		DATE MAILED: 11/14/200	5

Please find below and/or attached an Office communication concerning this application or proceeding.

>	Application No.	Applicant(s)				
	10/953,291	BACHMAN ET AL.				
Office Action Summary	Examiner	Art Unit				
	Tung X. Nguyen	2829				
The MAILING DATE of this communication app Period for Reply	pears on the cover sheet with the c	orrespondence address				
A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION. - Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication. - If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication. - Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).						
Status						
1) ☐ Responsive to communication(s) filed on 9/06/ 2a) ☐ This action is FINAL. 2b) ☐ This 3) ☐ Since this application is in condition for alloware closed in accordance with the practice under E	action is non-final. nce except for formal matters, pro					
Disposition of Claims						
4) ☐ Claim(s) is/are pending in the application. 4a) Of the above claim(s) is/are withdrawn from consideration. 5) ☐ Claim(s) is/are allowed. 6) ☑ Claim(s) 1-5 and 7-9 is/are rejected. 7) ☑ Claim(s) 6 is/are objected to. 8) ☐ Claim(s) are subject to restriction and/or election requirement.						
Application Papers						
9) ☐ The specification is objected to by the Examine 10) ☑ The drawing(s) filed on 29 September 2004 is/a Applicant may not request that any objection to the Replacement drawing sheet(s) including the correct 11) ☐ The oath or declaration is objected to by the Example 2004.	are: a) \square accepted or b) \square object drawing(s) be held in abeyance. Section is required if the drawing(s) is object.	e 37 CFR 1.85(a). jected to. See 37 CFR 1.121(d).				
Priority under 35 U.S.C. § 119						
 12) Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f). a) All b) Some * c) None of: 1. Certified copies of the priority documents have been received. 2. Certified copies of the priority documents have been received in Application No. 3. Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)). * See the attached detailed Office action for a list of the certified copies not received. 						
Attachment(s)						
 Notice of References Cited (PTO-892) Notice of Draftsperson's Patent Drawing Review (PTO-948) Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date 	4) Interview Summary Paper No(s)/Mail Da 5) Notice of Informal P 6) Other:					

Art Unit: 2829

DETAILED ACTION

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless -

- (a) the invention was known or used by others in this country, or patented or described in a printed publication in this or a foreign country, before the invention thereof by the applicant for a patent.
- 2. Claims 1-5, 7-9 are rejected under 35 U.S.C. 102(b) as being anticipated by Fang (Pub.No. US 2003/0094966).

As to claims 1, 9, Fang discloses in Figs. 3, a device comprising a flip chip bonding pad (32 of figure 3) including a region for performing a bumping (34, 35 of figure 3); and a test pad (31 of figure 3) integrally constructed with the bonding pad (32), the test pad being co-planar relative to the flip chip bonding pad and including a probe region (via 31) for performing wafer-level testing prior to performing the bumping process (see the abstract, and col. 1, lines 15-19 of paragraph 15).

As to claim 2, Fang discloses in figs. 3, the test pad (31) may be disposed anywhere along a periphery of the bonding pad (32).

As to claim 3, Fang discloses in Figs. 3, the bonding pad comprises a shape from the group consisting of a polygonal shape, and circular shape (34).

As to claim 4, Fang discloses in Figs. 3, the test pad (31) comprises a shape from the group consisting of a polygonal shape, and circular shape (31).

Art Unit: 2829

As to claim 5, Fang discloses in Figs. 3, a first metal redistribution layer (32) electrically connected to the bonding and test pads, and being co-planar with one another (fig. 3).

As to claim 7, Fang discloses in Figs. 3, the region to be bumped is defined by a first opening in a passivation layer (34 connecting to 35 for testing).

As to claim 8, Fang discloses in Figs. 3, the probe region (31) is defined by a second opening in the passivation, the first and second openings being spaced apart form one another (fig. 3).

Allowable Subject Matter

- 3. Claim 6 is objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.
- 4. The following is a statement of reasons for the indication of allowable subject matter:

As to claim 6, the prior art does not teach or suggest the interface assembly wherein the first metal redistribution layer is electrically connected by way of a via to a second redistribution layer being disposed in a different plane than the first redistribution layer.

Response to Arguments

5. Applicant's arguments filed 9/6/05 have been fully considered but they are not persuasive.

Application/Control Number: 10/953,291 Page 4

Art Unit: 2829

In re pages 4-6, to applicant argues that Fang patents fail to anticipate claims 1, and 9 under the 102 statutory requirements.

In response, the examiner respectfully disagrees with Applicant about the issue for the following the reasons: As to claims 1, 9, Fang clearly disclose in Figs. 3, a device comprising a flip chip bonding pad (32 of figure 3) including a region for performing a bumping (34, 35 of figure 3); and a test pad (31 of figure 3) integrally constructed with the bonding pad (32); the test pad being co-planar relative to the flip chip bonding pad and including a probe region (via 31) for performing wafer-level testing prior to performing the bumping process (see the abstract, and col. 1, lines 15-19 of paragraph 15).

Conclusion

6. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Tung X. Nguyen whose telephone number is (571) 272-1967. The examiner can normally be reached on 8:30am-5:00pm M-F.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Nestor Ramirez can be reached on (571) 272-2034. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

TN 11/08/05

VINH NGUYEN
PRIMARY EXAMINER

A.u. 2829 11/10/05 Index of Claims

10/953,291

Examiner

Tung X. Nguyen

Applicant(s)/Patent under Reexamination

BACHMAN ET AL.

Art Unit

2829

√	Rejected
H	Allowed

_	(Through numeral) Cancelled
÷	Restricted

N	Non-Elected
	Interference

A	Appeal
0	Objected

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Application/Control No.	Applicant(s)/Patent under Reexamination	
10/953,291	BACHMAN ET AL.	
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S1		(Yu adj et adj al).inv.	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2005/06/17 10:21
S2	0	"Us-2004/0173794 A1"	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2005/06/17 10:22
S3	0	"2004/0173794"	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR .	ON	2005/06/17 10:22
S4	27	"0173794"	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2005/06/17 10:26
S 5	0	S4 and Yu	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2005/06/17 10:26
S6	3921	324/754.ccls.	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2005/06/17 10:27
S7	0	S6 and pad with bumb\$4 and test\$4	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2005/06/17 10:28
S8	346	S6 and pad with bump\$4 and test\$4	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2005/06/17 10:28
S9	297	S8 and wafer	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2005/06/17 10:53
S10	0	(crip\$4 adj line) with wafer	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2005/06/17 10:55

S11	1	(scrip\$4 adj line) with wafer	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2005/06/17 10:57
S12	1	(scrip\$4 near3 line) with wafer	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2005/06/17 10:57
S13	3450	(scri\$4 near3 line) with wafer	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2005/06/17 14:49
S14	43	S13 and S6	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2005/06/17 14:44
S15	2	"20040173794"	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2005/06/17 14:49
S16	14773	324/754-765,158.1.ccls.	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2005/06/17 14:49
S17	123	(scribe near3 line) near3 pad with wafer	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR .	ON	2005/06/17 14:52
S18	9	S16 and S17	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM TDB	OR	ON	2005/06/17 14:51

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1-571-273-8300 7 (including cover sheet)

No of PAGES FROM

Enrique J. Mora

DATE

September 6, 2005

Serial Number 10/953,291

ATTY. DOCKET NO:

Bachman 3-11-16-173 (383)

VIA FACSIMILE ONLY

Attached please find for entry into the above-referenced application:

Reply/Amendment to Office Action Dated 6/29/2005 (6 pages). 1)

Yours truly,

nrjejue d/ Mora Beg. #36,875

Certificate of Transmission

I hereby certify that this correspondence is being facsimile transmitted to the United States Patent and Trademark Office, Fax No. 571-273-8300

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By: Kathy Tissue

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re: Application of:

Applicants: March Adam Bachman

Examiner: NGUYEN, Tung X.

Serial No.: 10/953,291

Group Art Unit: 2829

Filed:

09/29/2004

Confirmation No.: 2052

Title: Method and Structures for Testing)

A Semiconductor Wafer Prior to Performing a Flip Chip Bumping

Process

Atty. Docket No.: Bachman

3-11-16-173

Mail Stop AMENDMENT Commissioner for Patents P.O. Box 1450 Alexandria, VA 22313-1450

REPLY/RESPONSE UNDER CFR 1.111

This Reply is in response to the Office Action dated as mailed June 29, 2005 and having a response due date of September 29, 2005.

Please amend the above-identified application as follows:

Amendments to Claims are reflected in the listing of claims which begins on page 2 of this paper.

Remarks/Arguments begin on page 4 of this paper.

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IN THE CLAIMS:

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WHAT IS CLAIMED IS:

- 1. (Original) An interface assembly for a semiconductor wafer, said interface assembly comprising:
- a flip chip bonding pad including a region for performing a bumping process; and
- a test pad integrally constructed with said bonding pad, said test pad being co-planar relative to said flip chip bonding pad and including a probe region for performing wafer-level testing prior to performing said bumping process.
- 2. (Original) The interface assembly of claim 1 wherein said test pad may be disposed anywhere along a periphery of said bonding pad.
- 3. (Original) The interface assembly of claim 1 wherein said bonding pad comprises a shape selected from the group consisting of a polygonal shape, and a circular shape.
- 4. (Original) The interface assembly of claim 1 wherein said test pad comprises a shape selected from the group consisting of a polygonal shape, and a circular shape.
- (Original) The interface assembly of claim 1 further comprising a first metal redistribution layer electrically connected to said bonding and test pads, and being co-planar with one another.
- 6. (Original) The interface assembly of claim 5 wherein said first metal redistribution layer is electrically connected by way of a via to a second

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redistribution layer being disposed in a different plane than the first redistribution layer.

- (Original) The interface assembly of claim 1 wherein the region to 7. be bumped is defined by a first opening in a passivation layer.
- (Original) The interface assembly of claim 7 wherein the probe 8. region is defined by a second opening in said passivation layer, said first and second openings being spaced apart from one another.
- (Original) A method for testing a semiconductor wafer prior to 9. performing a flip chip bumping process, said method comprising:

providing a flip chip bonding pad having a region for performing said bumping process;

integrally constructing a test pad with said bonding pad; and

disposing said test pad coplanar with said flip chip bonding pad, said test pad including a probe region for performing a wafer test prior to performing said bumping process.

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REMARKS/ARGUMENTS

Applicant is appreciative of the Examiner's efforts in trying to conduct a concise and thorough examination of the present invention.

Claims 1-5, and 7-9, stand rejected as being anticipated by publication No. US 2003/0094966 (hereinafter Fang). Applicant appreciates the recognition of allowable subject matter in claim 6, which presently stands objected to. Reconsideration of the rejections and objections is solicited in view of the foregoing amendment and the following remarks.

Regarding any rejection under §102, it is noted that the test for anticipation is whether all the elements and operational relationships of the rejected claim are found within a single prior art reference. There must not be any differences between the claimed invention and the reference disclosure as viewed by a person of ordinary skill in the art. Absent from the reference disclosure of any claim element and/or operational interrelationship negates anticipation under §102.

Claim 1 is directed to an interface assembly for a semiconductor wafer. The interface assembly comprises a flip chip bonding pad including a region for performing a bumping process. The interface assembly further comprises a test pad integrally constructed with the bonding pad. The test pad is co-planar relative to the flip chip bonding pad and includes a probe region for performing wafer-level testing prior to performing the bumping process.

Fang is directed to a method for testing electrical characteristics of bumps. (See Abstract of Fang). Accordingly, Fang describes bumps 34 and 35 electrically interconnected by metal traces 32 and 33 respectively. See paragraph 15 and FIG. 3 of Fang. The technique of Fang expressly recognizes that bumps are structures formed after a flip chip bumping process is performed. See Fang paragraph 8, line 5. This is wholly inapposite to the operational and/or structural relationships recited in claim 1 that specifically recites a flip chip bonding pad including a region for performing a bumping process (i.e., a precursor structure prior to a bumping process) and a probe region for performing wafer-level testing prior to performing the bumping process.

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Fang is an example of a type of technique for probing a wafer after the bumping process has been performed. As applicant described in the specification section designated "Background of The Invention", this type of technique suffers from various drawbacks that are not applicable to the claimed invention. For example, the type of post-bumping probing technique (typified by Fang) may lead to incremental costs since there is a possibility that the bumping process (that takes valuable time and resources) may have been performed in an already defective wafer that should have been discarded prior to continuing with any such bump fabrication processes. On this basis alone it is felt that Fang fails to anticipate claim 1 under the §102 statutory requirements. Applicant, however, goes on to present below an alternative basis regarding the inability of Fang to anticipate claim 1.

Applicant notes that the bumps in Fang are not integrally constructed with one another. More particularly, such post-bumping structures require separate metal traces in order to be electrically interconnected to one another. By way of comparison, claim 1 recites a test pad integrally constructed with a bonding pad. In view of the integral construction, applicant advantageously avoids the need of metal traces for electrically interconnecting the test pad with the bonding pad. As applicant stated in the section of the specification designated "Background of the Invention", the presence of interconnect lines (as described by Fang) can introduce undesirable propagation delays to test signals.

In view of the foregoing remarks, it is respectfully submitted that Fang fails to anticipate or otherwise render obvious claim 1, and applicant kindly requests that this basis of rejection be removed.

Claims 2-5 and 7 depend from claim 1 and thus incorporate the structural and/or operational relationships set forth in claim 1 plus their own recitations. It is respectfully submitted that Fang also fails to anticipate such claims under the §102 statutory requirements and these rejections should be withdrawn.

Claim 9 is directed to a method for testing a seimconductor prior to performing a flip chip bumping process. Consequently, Fang (directed to post-bump testing) also

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fails to anticipate this claim under the §102 statutory requirement and this rejection should also be withdrawn.

It is respectfully submitted that each of the claims pending in this application recites patentable subject matter and it is further submitted that such claims comply with all statutory requirements and thus each of such claims should be allowed.

* * * * * * *

The Examiner is invited to call the undersigned if clarification is needed on any aspects of this Reply/Amendment, or if the Examiner believes a telephonic interview would expedite the prosecution of the subject application to completion.

Respectfully submitted,

Enrique J. Mora

Registration No. 36,875

Beusse Brownlee Wolter Mora & Maire, P.A.

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Orlando, FL 32801

Telephone: 407-926-7705 Fax: 407-926-7720

PATENT APPLICATION FEE DETERMINATION RECORD 1695329 Effective December 8, 2004 CLAIMS AS FILED - PART I SMALL ENTITY OTHER THAN (Column 1) (Column 2) TYPE [OR SMALL ENTITY TOTAL CLAIMS RATE FEE RATE FEE FOR NUMBER FILED NUMBER-EXTRA BASIC FEE 150.00 BASIC FEE OR 300.00 TOTAL CHARGEABLE CLAIMS ninus 20 X\$ 25= X\$50= OR INDEPENDENT CLAIMS mhus 3 = X100 =X200= MULTIPLE DEPENDENT CLAIM PRESENT OR +180= +360= * If the difference in column 1 is less than zero, enter *0" in column 2 OR TOTAL OR TOTAL CLAIMS A'S AMENDED - PART II OTHER THAN (Column 1) (Column 2) (Column 3) SMALL ENTITY SMALL ENTITY OR. CLAIMS HIGHEST REMAINING ADDI-NUMBER PRESENT ADDI-AFTER AMENDMEN PREVIOUSLY RATE TIONAL **EXTRA** AMENOMENT RATE TIONAL PAID FOR FEE FEE Minus X\$ 25= X\$50= OR Independent Minus FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM X100= X200= OR +180= OR +360= TOTAL TOTAL ADDIT, FEE ADDIT. FEE (Column 1) (Column 2) (Column 3) CLAIMS HIGHEST REMAINING NUMBER ADDI-PRESENT ADDI-AMENDMENT AFTER PREVIOUSLY RATE EXTRA TIONAL AMENDMENT RATE TIONAL PAID FOR FEE FEE Total Minus X\$ 25= X\$50± OR Independent Minuis FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM X100= X200= OR: +180= +360= OR TOTAL OR ADDIT, FEE ADDIT, FEE (Column 1) (Column 2) (Column 3) CLAIMS HIGHEST REMAINING NUMBER PRESENT ADDI-ADDI-AMENDMENT AFTER PREVIOUSLY TIONAL **EXTRA** RATE RATE TIONAL AMENDMENT PAID FOR FEE FEE Total Minus X\$ 25= X\$50=OR Independent Minus X100= FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM X200= OR +180= +360= OR

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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/953,291	09/29/2004	Mark Adam Bachman	Bachman 3-11-16-173	2052
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	OWNLEE WOLTER RANGE AVENUE	NGUYEN	, TUNG X	
SUITE 2500	IG II (GE /I (EI (GE		ART UNIT	PAPER NUMBER
ORLANDO, F	L 32801		2829	·

DATE MAILED: 06/29/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

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	Application No.	Applicant(s)	0
	10/953,291	BACHMAN ET AL	.
Office Action Summary	Examiner	Art Unit	
	Tung X. Nguyen	2829	
The MAILING DATE of this communication a Period for Reply	ppears on the cover sheet	t with the correspondence ad	dress
A SHORTENED STATUTORY PERIOD FOR REF THE MAILING DATE OF THIS COMMUNICATION - Extensions of time may be available under the provisions of 37 CFR after SIX (6) MONTHS from the mailing date of this communication. - If the period for reply specified above is less than thirty (30) days, a r - If NO period for reply is specified above, the maximum statutory perion - Failure to reply within the set or extended period for reply will, by state than the period for reply will be period for reply will, by state than the period for reply will be period for	N. 1.136(a). In no event, however, ma eply within the statutory minimum of od will apply and will expire SIX (6) N ute, cause the application to becom	y a reply be timely filed thirty (30) days will be considered timely MONTHS from the mailing date of this cole BABANDONED (35 U.S.C. § 133).	y. ommunication.
Status			
1) Responsive to communication(s) filed on 29	September 2004.		
· ·	his action is non-final.		
3) Since this application is in condition for allow			e merits is
closed in accordance with the practice unde	r <i>Ex parte Quayle</i> , 1935 (C.D. 11, 453 O.G. 213.	
Disposition of Claims			
4) Claim(s) 1-9 is/are pending in the application	n.		
4a) Of the above claim(s) is/are withd	rawn from consideration.		
5) Claim(s) is/are allowed.			
6)⊠ Claim(s) <u>1-5 and 7-9</u> is/are rejected.			
7) Claim(s) 6 is/are objected to.	d/as aloation requirement		
8) Claim(s) are subject to restriction and	a/or election requirement.		
Application Papers			
9) The specification is objected to by the Exam 10) The drawing(s) filed on 29 September 2004 Applicant may not request that any objection to t Replacement drawing sheet(s) including the corr 11) The oath or declaration is objected to by the	is/are: a)⊠ accepted or he drawing(s) be held in abe rection is required if the draw	eyance. See 37 CFR 1.85(a). ving(s) is objected to. See 37 C	FR 1.121(d).
Priority under 35 U.S.C. § 119			
12) Acknowledgment is made of a claim for foreign a) All b) Some * c) None of: 1. Certified copies of the priority documed 2. Certified copies of the priority documed 3. Copies of the certified copies of the papplication from the International Bures * See the attached detailed Office action for a first service of the papplication from the International Bures * See the attached detailed Office action for a first service of the papplication from the International Bures * See the attached detailed Office action for a first service of the priority documents * See the attached detailed Office action for a first service of the priority documents * See the attached detailed Office action for a first service of the priority documents * See the attached detailed Office action for a first service of the priority documents * See the attached detailed Office action for a first service of the priority documents * See the attached detailed Office action for a first service of the priority documents * See the attached detailed Office action for a first service of the priority documents * See the attached detailed Office action for a first service of the priority documents * See the attached detailed Office action for a first service of the priority documents * See the attached detailed Office action for a first service of the priority documents * See the attached detailed Office action for a first service of the priority documents * See the attached detailed Office action for a first service of the priority documents * See the attached detailed Office action for a first service of the priority documents * See the attached detailed Office action for a first service of the priority documents * See the attached detailed Office action for a first service of the priority documents * See the attached detailed Office action for a first service of the priority documents * See the attached detailed Office action for a first service of the priority documents * See the attached detailed Office action for a first service of the priority	ents have been received. ents have been received i riority documents have be eau (PCT Rule 17.2(a)).	in Application No een received in this National	Stage
Attachment(s) 1) Notice of References Cited (PTO-892) 2) Notice of Draftsperson's Patent Drawing Review (PTO-948) 3) Information Disclosure Statement(s) (PTO-1449 or PTO/SB/Paper No(s)/Mail Date 9/29/04.	Paper	ew Summary (PTO-413) No(s)/Mail Date of Informal Patent Application (PT	O-152)

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DETAILED ACTION

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless -

- (a) the invention was known or used by others in this country, or patented or described in a printed publication in this or a foreign country, before the invention thereof by the applicant for a patent.
- 2. Claims 1-5, 7-9 are rejected under 35 U.S.C. 102(b) as being anticipated by Fang (Pub.No. US 2003/0094966).

As to claims 1, 9, Fang discloses in Figs. 3, a device comprising a flip chip bonding pad (32 of figure 3) including a region for performing a bumping (34, 35 of figure 3); and a test pad (31 of figure 3) integrally constructed with the bonding pad (32), the test pad being co-planar relative to the flip chip bonding pad and including a probe region (via 31) for performing wafer-level testing prior to performing the bumping process (see the abstract, and col. 1, lines 15-19 of paragraph 15).

As to claim 2, Fang discloses in figs. 3, the test pad (31) may be disposed anywhere along a periphery of the bonding pad (32).

As to claim 3, Fang discloses in Figs. 3, the bonding pad comprises a shape from the group consisting of a polygonal shape, and circular shape (34).

As to claim 4, Fang discloses in Figs. 3, the test pad (31) comprises a shape from the group consisting of a polygonal shape, and circular shape (31).

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As to claim 5, Fang discloses in Figs. 3, a first metal redistribution layer (32) electrically connected to the bonding and test pads, and being co-planar with one another (fig. 3).

As to claim 7, Fang discloses in Figs. 3, the region to be bumped is defined by a first opening in a passivation layer (34 connecting to 35 for testing).

As to claim 8, Fang discloses in Figs. 3, the probe region (31) is defined by a second opening in the passivation, the first and second openings being spaced apart form one another (fig. 3).

Allowable Subject Matter

- 3. Claim 6 is objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.
- The following is a statement of reasons for the indication of allowable subject matter:

As to claim 6, the prior art does not teach or suggest the interface assembly wherein the first metal redistribution layer is electrically connected by way of a via to a second redistribution layer being disposed in a different plane than the first redistribution layer.

Conclusion

5. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Tung X. Nguyen whose telephone number is (571) 272-1967. The examiner can normally be reached on 8:30am-5:00pm M-F.

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If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Nestor Ramirez can be reached on (571) 272-2034. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

TN 6/20/05.

VINH NGUYËN PRIMARY EXAMINER

A.4-2829

Microchip et al. Ex. 1002-107

PTO/SB/08A (08-03)

Approved for use through 07/31/2006. OMB 0651-0031

U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE
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Substitute for form 1449B/PTO				Complete if Known			
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				First Named Inventor	Mark Adam Bachman		
			-10/11/1	Art Unit	Not Yet Assigned 2829		
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Sheet	1	of	2	Attorney Docket Number	Bachman 3-11-16-173		

	U.S. PATENT DOCUMENTS						
Examiner Initials	Cite No. ¹	Document Number Number-Kind Code ^{2(i known)}	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear		
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Signature	Mes.	Considered	6/17/05	

EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant. ¹Applicant's unique citation designation number (optional). ²See Kinds Codes of USPTO Patent Documents at www.uspto.gov or MPEP 901.04. ³Enter Office that issued the document, by the two-letter code (WIPO Standard ST.3). ⁴For Japanese patent documents, the indication of the year of the reign of the Emperor must precede the serial number of the patent document. ⁵Kind of document by the appropriate symbols as indicated on the document under WIPO Standard ST.16 if possible. ⁶Applicant is to place a check mark here if English Language Translation is attached.

This collection of information is required by 37 CFR 1.97 and 1.98. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 2 hours to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.

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CLASS

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INFORMATION DISCLOSURE			SURE	Filing Date	Simultaneously Herewith 09 129/2004	
STATEMENT BY APPLICANT		First Named Inventor	Mark Adam Bachman			
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Sheet	2	of	2	Attorney Docket Number	Bachman 3-11-16-173 /	

		NON-PATENT LITERATURE DOCUMENTS	
Examiner Initials	Cite No.1	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.	T²
JW	1	LOIS YONG, TU ANH TRAN, STEPHEN LEE, BILL WILLIAMS and JODY ROSS, "Novel Method of Separating Probe and Wire Bond Regions Without Increasing Die Size," 2003 Electronic Components and Technology Conference, pp. 1323-1329.	
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EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.

Applicant's unique citation designation number (optional). ²Applicant is to place a check mark here if English Language Translation is attached. This collection of information is required by 37 CFR 1.98. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 2 hours to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.

Notice of References Cited Application/Control No. 10/953,291 Examiner Tung X. Nguyen Applicant(s)/Patent Under Reexamination BACHMAN ET AL. Art Unit Page 1 of 1

U.S. PATENT DOCUMENTS

*		Document Number Country Code-Number-Kind Code	Date MM-YYYY	Name	Classification
	Α	US-5,956,567 A	09-1999	Tomita, Yasuhiro	438/18
	В	US-2003/0094966 A1	05-2003	Fang, Jen-Kuang	324/765
	С	US-			
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*A copy of this reference is not being furnished with this Office action. (See MPEP § 707.05(a).)

Dates in MM-YYYYY format are publication dates. Classifications may be US or foreign.

U.S. Patent and Trademark Office PTO-892 (Rev. 01-2001)



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CONFIRMATION NO. 2052

					 	
SERIAL NUMBI 10/953,291	FILING DATE 09/29/2004 RULE	CLASS 324	GROUP ART 2829		ATTORNEY DOCKET NO. achman 3-11-16- 173	
APPLICANTS						
Mark Adam	n Bachman, Sinking Spring,	PA;				
	Daniel Patrick Chesire, Winter Garden, FL; Taeho Kook, Orlando, FL;Sailesh M. Merchant, Macungie, PA;					
** CONTINUING I	* CONTINUING DATA **********************************					
** FOREIGN APP	PLICATIONS	/ ****				
IF REQUIRED, F0 ** 11/15/2004	OREIGN FILING LICENSE	GRANTED				
Foreign Priority claimed 35 USC 119 (a-d) condi met Verified and Acknowledged	litions yes no Met aff	STATE OR COUNTRY PA	SHEETS DRAWING 2	TOTAL (CLAIMS 9	INDEPENDENT CLAIMS 2	
	ADDRESS 29391 BEUSSE BROWNLEE WOLTER MORA & MAIRE, P. A. 390 NORTH ORANGE AVENUE SUITE 2500 ORLANDO , FL					
TITLE Method and struct	tures for testing a semicond	ductor wafer prior to per	forming a flip c	chip bumping	j process	
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324	754	6/17/2005	TN		
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Approved for use through 07/31/2006. OMB 0651-0031
U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE collection of information unless it displays a valid OMB control number no persons are required to respond to a Application Number 10/953,291 **TRANSMITTAL** Filing Date 09/29/2004 First Named Inventor **FORM** Mark Adam Bachman Art Unit 2858

(to be used for all correspondence after initial filing)	Examiner Name	Not Yet Assigned							
Total Number of Pages in This Submission	Attorney Docket Number	Bachman 3-11-16-173							
EN	CLOSUPES (Charle all	that applied							
Fee Transmittal Form Fee Attached Amendment/Reply (w/Attachment) After Final Affidavits/declaration(s) Extension of Time Request Express Abandonment Request Information Disclosure Statement	Drawing(s) Licensing-related Papers Petition Petition to Convert to a Provisional Application Power of Attorney, Revocatio Change of Correspondence A Terminal Disclaimer Request for Refund CD, Number of CD(s) Landscape Table on CD Larks	Status Letter Other Enclosure(s) (please Identify below): 1. Postcard 2. Formalities Letter (Confirmation No. 2052) 3. Signed Declaration and POA (4 pgs.)							
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James H. Beusse January 18, 2005	-	Reg. No. 27,115							
	CERTIFICATE OF TRANSMISSION/MAILING								
sufficient postage as first class mail in an envelope a the date shown below:		O or deposited with the United States Postal Service with Patents, P.O. Box 1450, Alexandria, VA 22313-1450 on							
Signature	Signature Charco A hattoulege								
Typed or printed name Grayce A. Lichte	nberger	Date January 18, 2005							

This collection of information is required by 37 CFR 1.5. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.11 and 1.14. This collection is estimated to 2 hours to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commence, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.

If you need assistance in completing the form, call 1-800-PTO-9199 and select option 2.

PTO/SB/17 (12-04)

Approved for use through 07/31/2006. OMB 0651-0032

U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE

Under the panerwork Reduction Act of 1995 no persons are required to respond to a collection of information unless it displays a valid OMB control number

Fees pursuant to the Consolidated Approp	3/2004.		e if Known						
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TOTAL AMOUNT OF PAYMENT (\$) 130.00	Attorney Docket No	. Bachn	ıan 3-11-16-	173				
METHOD OF PAYMENT (check	all that apply)								
Check Credit Card	Money Order No	one Other (pleas	e identify):						
Deposit Account Deposit Account Number: Deposit Account Name:									
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3. APPLICATION SIZE FEE									
If the specification and drawings	s exceed 100 sheets of p	paper, the application	size fee due	is \$250 (\$125 i	for small entity)				
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4. OTHER FEE(S)									
Non-English Specification, \$130 fee (no small entity discount)									
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This collection of information is required by 37 CFR 1.136. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 30 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.

If you need assistance in completing the form, call 1-800-PTO-9199 and select option 2.



In re Application of:

Applicants: Mark Adam Bachman, et al.

Examiner: Not Yet Assigned

Serial No.: 10/953,291

Art Unit: 2858

Filed:

09/29/2004

Confirmation No.: 2052

For:

Method And Structures For Testing A

Semiconductor Wafer Prior To Performing A Flip Chip Bumping

Process

Mail Stop Missing Parts Commissioner for Patents P.O. Box 1450 Alexandria, VA 22313-1450

RESPONSE TO NOTICE TO FILE MISSING PARTS OF NONPROVISIONAL APPLICATION (FILING DATE GRANTED)

In response to the Notice To File Missing Parts Of Nonprovisional Application, Filing Date Granted, dated as mailed November 17, 2004 and having a period of response to and including January 18, 2004 (given that January 17, 2005 was a National Holiday), enclosed are the following items required for filing in the above-referenced U.S. Patent Application:

- 1. Formalities Letter (Confirmation No. 2052);
- 2. The \$130.00 Surcharge is being paid by enclosed check; and
- 3. Signed Declaration and Power of Attorney (4 pages).

Respectfully submitted,

James H. Beusse

Reg. No. 27,115

∕B∉usse, Brownlee, Wolter, Mora & Maire, P.A.

390 N. Orange Avenue, Suite 2500

Orlando, FL 32801

Phone: (407) 926-7701



CERTIFICATE OF MAILING

I HEREBY CERTIFY that this <u>Response To Notice to File Missing Parts of NonProvisional Application Filing Date Granted</u> is being deposited with the United States Postal Service as first class mail in an envelope addressed to: Mail Stop Missing Parts, Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450 on this 18th day of January, 2005.

Grayce A. Lichtenberger



UNITED STATES DEPARTMENT OF COMMERCE United States Patent and Trademark Office Address: COMMISSIONER FOR PATENTS P.O. Box 1450 Alexandria, Viginia 22313-1450

APPLICATION NUMBER FILING OR 371 (c) DATE FIRST NAMED APPLICANT ATTORNEY DOCKET NUMBER

10/953,291 09/29/2004 Mark Adam Bachman Bachman 3-11-16-173

29391 BEUSSE BROWNLEE WOLTER MORA & MAIRE, P. A. 390 NORTH ORANGE AVENUE SUITE 2500 ORLANDO, FL 32801 CONFIRMATION NO. 2052
FORMALITIES LETTER
OC000000014374716

Date Mailed: 11/17/2004

NOTICE TO FILE MISSING PARTS OF NONPROVISIONAL APPLICATION

FILED UNDER 37 CFR 1.53(b)

Filing Date Granted

Items Required To Avoid Abandonment:

An application number and filing date have been accorded to this application. The item(s) indicated below, however, are missing. Applicant is given **TWO MONTHS** from the date of this Notice within which to file all required items and pay any fees required below to avoid abandonment. Extensions of time may be obtained by filing a petition accompanied by the extension fee under the provisions of 37 CFR 1.136(a).

- The oath or declaration is missing.
 A properly signed oath or declaration in compliance with 37 CFR 1.63, identifying the application by the above Application Number and Filing Date, is required.
- To avoid abandonment, a late filing fee or oath or declaration surcharge as set forth in 37 CFR 1.16(e) of \$130 for a non-small entity, must be submitted with the missing items identified in this letter.

SUMMARY OF FEES DUE:

Total additional fee(s) required for this application is \$130 for a Large Entity

• \$130 Late oath or declaration Surcharge.

Replies should be mailed to:

Mail Stop Missing Parts

Commissioner for Patents

P.O. Box 1450

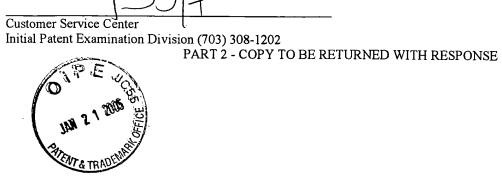
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A copy of this notice <u>MUST</u> be returned with the reply.





IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Declaration and Power of Attorney

As the below named inventors, we hereby declare that:

Our residence, post office address and citizenship are as stated below next to our name.

We believe we are the original, first and sole inventors of the subject matter which is claimed and for which a patent is sought on the invention entitled METHOD AND STRUCTURES FOR TESTING A SEMICONDUCTOR WAFER PRIOR TO PERFORMING A FLIP CHIP BUMPING PROCESS, the specification of which was filed on September 29, 2004, as application Serial No. 10/953,291.

We hereby state that we have reviewed and understand the contents of the above identified specification, including the claims, as amended by an amendment, if any, specifically referred to in this oath or declaration.

We acknowledge the duty to disclose all information known to us which is material to patentability as defined in Title 37, Code of Federal Regulations, 1.56.

We hereby claim foreign priority benefits under Title 35, United States Code, 119 of any foreign application(s) for patent or inventor's certificate listed below and have also identified below any foreign application for patent or inventor's certificate having a filing date before that of the application on which priority is claimed:

None

We hereby claim the benefit under Title 35, United States Code, 120 of any United States application(s) listed below and, insofar as the subject matter of each of the claims of this application is not disclosed in the prior United States application in the manner provided by the first paragraph of Title 35, United States Code, 112, I acknowledge the duty to disclose all information known to me to be material to patentability as defined in Title 37, Code of Federal Regulations, 1.56 which became available between the filing date of the prior application and the national or PCT international filing date of this application:

None

We hereby declare that all statements made herein of our own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code and that such willful false statements may jeopardize the validity of the application or any patent issued thereon.

We hereby appoint the registered practitioners associated with Customer Number **29391** to prosecute said application, to make alterations and amendments therein, to receive the patent, and to transact all business in the Patent and Trademark Office.

Full name of sole inventor (or 1st joint inventor):

MARK ADAM BACHMAN

Inventor's signature Much Adam	Brehman Date 12/15/2004
Residence:	3 Esther Circle Sinking Spring, PA 19608
Citizenship:	USA
Post Office Address:	3 Esther Circle Sinking Spring, PA 19608
,	
Full name of 2nd joint inventor:	PATRICK DANIEL CHESIRE
Inventor's signature	Date
Residence:	2018 Wintermere Pointe Drive Winter Garden, FL 34787
Citizenship:	USA
Post Office Address:	2018 Wintermere Pointe Drive Winter Garden, FL 34787

We hereby appoint the registered practitioners associated with Customer Number **49382** to prosecute said application, to make alterations and amendments therein, to receive the patent, and to transact all business in the Patent and Trademark Office.

Full name of sole inventor (or 1st joint inventor):

MAF	≀K	ΔD	ΔM	RΔ	CH	ΜΔΝ
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Inventor's signature	Date
Residence:	3 Esther Circle Sinking Spring, PA 19608
Citizenship:	USA
Post Office Address:	3 Esther Circle Sinking Spring, PA 19608
Full name of 2nd joint inventor	DANIEL PATRICK CHESIRE
Inventor's and	Q. Chesine Date 12-14-2004
Residence:	2018 Wintermere Pointe Drive Winter Garden, FL 34787
Citizenship:	USA
Post Office Address:	2018 Wintermere Pointe Drive Winter Garden, FL 34787

TAEHO KOOK Full name of 3rd joint inventor:

Inventor's signature

Date Dec. 17, 2004

Residence:

9253 Wickham Way

Orlando, FL 32836

Citizenship:

-KOREA USA T.K.

Post Office Address:

9253 Wickham Way

Orlando, FL 32836

Full name of 3rd joint inventor:

SAILESH M. MERCHANT

Inventor's

signature

Date 12 Dec 04

Residence:

7156 Moonbeam Lane

Macungie, PA 18062

Citizenship:

USA

Post Office Address:

7156 Moonbeam Lane

Macungie, PA 18062

Telephone calls should be made to **JAMES H. BEUSSE** at:

Phone No.: 407-926-7701

Fax No.:

407-926-7720

All written communications are to be addressed to:

JAMES H. BEUSSE, ESQUIRE BEUSSE BROWNLEE WOLTER MORA & MAIRE, P.A. 390 NORTH ORANGE AVENUE, SUITE 2500 ORLANDO, FL 32801



UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE United States Patent and Trademark Office Address COMMISSIONER FOR PATENTS PO. Box 1450 Alexandria, Viginia 22313-1450 www.uspto.gov

APPLICATION NUMBER FILING OR 371 (c) DATE FIRST NAMED APPLICANT ATTORNEY DOCKET NUMBER

10/953,291 09/29/2004

Mark Adam Bachman

Bachman 3-11-16-173

29391
BEUSSE BROWNLEE WOLTER MORA & MAIRE, P. A.
390 NORTH ORANGE AVENUE
SUITE 2500
ORLANDO, FL 32801

CONFIRMATION NO. 2052 FORMALITIES LETTER

OC000000014374716

Date Mailed: 11/17/2004

NOTICE TO FILE MISSING PARTS OF NONPROVISIONAL APPLICATION

FILED UNDER 37 CFR 1.53(b)

Filing Date Granted

Items Required To Avoid Abandonment:

An application number and filing date have been accorded to this application. The item(s) indicated below, however, are missing. Applicant is given **TWO MONTHS** from the date of this Notice within which to file all required items and pay any fees required below to avoid abandonment. Extensions of time may be obtained by filing a petition accompanied by the extension fee under the provisions of 37 CFR 1.136(a).

- The oath or declaration is missing.
 A properly signed oath or declaration in compliance with 37 CFR 1.63, identifying the application by the above Application Number and Filing Date, is required.
- To avoid abandonment, a late filing fee or oath or declaration surcharge as set forth in 37 CFR 1.16(e) of \$130 for a non-small entity, must be submitted with the missing items identified in this letter.

SUMMARY OF FEES DUE:

Total additional fee(s) required for this application is \$130 for a Large Entity

\$130 Late oath or declaration Surcharge.

Replies should be mailed to: Mail Stop Missing Parts

Commissioner for Patents

P.O. Box 1450

Alexandria VA 22313-1450

A copy of this notice <u>MUST</u> be returned with the reply.

Customer Service Center | Unitial Patent Examination Division (703) 308-1202

PART 3 - OFFICE COPY

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UTILITY PATENT APPLICATION **TRANSMITTAL**

(Only for new nonprovisional applications under 37 CFR 1.53(b))

Attorney Docket No.	Bachman 3-11-16-173				
First Inventor	Mark Adam Bachman				
Title	Method And Structures For Testing A Semiconductor Wa Prior To Performing A Flip Chip Bumping Process				
Express Mail Label No.	EO 002 729 826 US	2			

<u> </u>		
APPLICATION ELEMENTS See MPEP chapter 600 concerning utility patent application contents.	ADDRESS TO. P.O. Box 14	oner for Patents () (450 (VA 22313-1450
1. Fee Transmittal Form (e.g., PTO/SB/17) (Submit an original and a duplicate for fee processing) Applicant claims small entity status. See 37 CFR 1.27. 3. Specification [Total Pages 8] (preferred arrangement set forth below) - Descriptive title of the invention - Cross Reference to Related Applications - Statement Regarding Fed sponsored R & D - Reference to sequence listing, a table, or a computer program listing appendix - Background of the Invention - Brief Summary of the Invention - Brief Description of the Drawings (if filed) - Detailed Description - Claim(s) - Abstract of the Disclosure	ii. Paper c. Statements verifying ACCOMPANYING AP	ndix) Sequence Submission Form (CRF) Ince Listing on: D-R (2 copies); or Identity of above copies PLICATION PARTS
4. Drawing(s) (35 U.S.C. 113) [Total Sheets] 5. Oath or Declaration [Total Sheets] a. Newly executed (original or copy) b. Copy from a prior application (37 CFR 1.63(d)) (for continuation/divisional with Box 18 completed) i. DELETION OF INVENTOR(S) Signed statement attached deleting inventor(s) name in the prior application, see 37 CFR 1.63(d)(2) and 1.33(b). 6. Application Data Sheet. See 37 CFR 1.76	or its equivalent. 17. Other:	nt Power of Attorney Iment (if applicable) Copies of IDS Copies of IDS Citations (MPEP 503) emized) Document(s) led) under 35 U.S.C. 122 st attach form PTO/SB/35
specification following the title, or in an Application Data Sheet under 37	7 CFR 1.76: tion-in-part (CIP) of prior application Art Unit: a prior application, from which an oath o or divisional application and is hereby li	n No.:
19. CORRESPONI	DENCE ADDRESS	
Customer Number: 29391	OR Corres	spondence address below
Name		
Address		
City	State	Zip Code
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Name (Print/Type) James H. Beusse	Registration No. (Attorney/Agent)	27,115
Signature		Date Sept 29 2004

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PTO/SB/17 (10-03)

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Effective 10/01/2003. Patent fees are subject to annual revision.

Applicant claims small entity status. See 37 CFR 1.27

TOTAL AMOUNT OF PAYMENT

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Complete if Known					
Application Number	Not Yet Known				
Filing Date	Simultaneously Herewith				
First Named Inventor	Mark Adam Bachman				
Examiner Name	Not Yet Assigned				
Art Unit	Not Yet Assigned				
Attorney Docket No.	Bachman 3-11-16-173				

METHOD OF PAYMENT (check all that apply)			**	FEE	ECALCULATION (continued)	
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The Director is authorized to: (check all that apply)	1053	130	1053		Non-English specification For filing a request for ex parte reexamination	
Charge fee(s) indicated below Credit any overpayments		2,520	1812	_,	· · ·	
Charge any additional fee(s) or any underpayment of fee(s)	1804	920*	1804	920"	Requesting publication of SIR prior to Examiner action	
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to the above-identified deposit account.	4054	440	2254	==	Examiner action	
FEE CALCULATION	1251	110	2251	55 210	Extension for reply within first month Extension for reply within second month	
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Code (\$) Code (\$)		•		740	Extension for reply within fourth month	
1001 770 2001 385 Utility filing fee 770.00		2,010	2255		Extension for reply within fifth month	
1002 340 2002 170 Design filing fee	1401	330	2401		Notice of Appeal	
1003 530 2003 265 Plant filing fee	1402	330	2402		Filing a brief in support of an appeal	
1004 770 2004 385 Reissue filing fee	1403	290	2403		Request for oral hearing	
1005 160 2005 80 Provisional filing fee	1451		1451		Petition to institute a public use proceeding	
SUBTOTAL (1) (\$) 770.00	1452	110	2452	55	Petition to revive - unavoidable	
2. EXTRA CLAIM FEES FOR UTILITY AND REISSUE		1,330	2453	6 65	Petition to revive - unintentional	
Fee from	1501		2501		Utility issue fee (or reissue)	
Extra Claims below Fee Paid Total Claims 9 -20** = 0 X 18.00 = 0.00	1502	480	2502		Design issue fee	
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Claims Z - 3 = 0 X 33:33 0.00	1460	130	1460		Petitions to the Commissioner	
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Code (\$) Code (\$)	8021	40	802°	1 40	Recording each patent assignment per property (times number of properties)	
1202 18 2202 9 Claims in excess of 20 1201 86 2201 43 Independent claims in excess of 3	1809	770	2809	385	Filing a submission after final rejection	
1201 86 2201 43 Independent claims in excess of 3 1203 290 2203 145 Multiple dependent claim, if not paid	1810	770	2810	385	(37 CFR 1.129(a)) For each additional invention to be	
1204 86 2204 43 ** Reissue independent claims	.5.5			- 500	examined (37 CFR 1.129(b))	
over original patent	1801	770	2801	385	Request for Continued Examination (RCE)	
1205 18 2205 9 ** Reissue claims in excess of 20 and over original patent	1802	900	1802	900	Request for expedited examination of a design application	
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SUBTOTAL (2) (\$) 0.00 **or number previously paid, if greater; For Reissues, see above	*Redi	uced by	Basic l	Filing F	ee Paid SUBTOTAL (3) (\$) 0.00)

SUBMITTED BY Registration No. Telephone (407) 926-7715 27,115 Name (Print/Type) September 29, 2004 Signature

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(Complete (if applicable))

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of:

Applicants:

Mark Adam Bachman, et al.

Application No.:

Not Yet Assigned

Filed:

Simultaneously Herewith

For:

Method And Structures For Testing A

Semiconductor Wafer Prior To Performing A Flip Chip Bumping

Process

Commissioner for Patents P.O. Box 1450 Alexandria, VA 22313-1450

Sir:

EXPRESS MAIL # EO 002 729 826 US

Date of Deposit: September 29, 2004

I hereby certify that the attached Utility Patent Application, transmittal forms, Information Disclosure Statement and Drawings were deposited with the United States Postal Service "Express Mail Post Office to Addressee" service under 37 CFR 1.10 on the date indicated above and is addressed to: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.

Respectfully submitted,

Grayce A. Lichtenberger

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METHOD AND STRUCTURES FOR TESTING A SEMICONDUCTOR WAFER PRIOR TO PERFORMING A FLIP CHIP BUMPING PROCESS

FIELD OF THE INVENTION

[001] The present invention is generally related to semiconductor devices, and, more particularly, to structures and techniques for enabling wafer level testing prior to performing a bumping process in a flip chip assembly.

BACKGROUND OF THE INVENTION

[002] By way of background, flip chip microelectronic assembly generally refers to a direct electrical connection of face-down (hence, "flipped") electronic components onto substrates, circuit boards, or carriers, by means of conductive bumps on the chip bond pads. By way of comparison, wire bonding technology generally uses face-up chips with a wire connection to each pad. Flip chip technology has *inter alia* enabled substantial input/output (I/O) connection flexibility. For example, wire bond connections are generally limited to the perimeter of the die, driving die sizes up as the number of connections increase. Flip chip connections, such as area array bumps, can use the entire area of the die, accommodating many more connections on a smaller die.

[003] FIG. 1 is a top view schematic representation of a metal bonding pad 8 (e.g., Al or Cu bonding pad) of a semiconductor device that includes a bump region 10 over the metal bonding pad 8. FIG. 1 is provided for illustrating some of the difficulties encountered in the prior art. The bump region 10 --where a bumping process is to be performed for constructing an electrically conductive bump (e.g., a solder bump) for the flip chip assembly -- may be defined by a passivation opening 12 in a passivation layer that surrounds the bonding pad.

[004] It is known that for a semiconductor device that uses flip chip technology, performing wafer-level testing through the metal bonding pad to verify circuit functionality is generally not desirable prior to performing the bumping process. For example, a test probe tip that may be placed in contact with the bonding pad

may gouge the metal pad surface. The resulting surface irregularities on the bump pad can lead to difficulties in establishing and maintaining strong adhesion for one or more metal layers that may be deposited during the formation of the bump. For example, prior to bump formation, a process referred to as under bump metallization (UBM) allows the fabrication of a barrier metal to prevent interaction of the metal pad with the solder bump. The UBM structure comprises an "adhesion layer" that should adhere well to both the bond pad metal and the surrounding passivation layer in order to provide a strong, low-stress electromechanical connection. Similarly, a "diffusion barrier" layer may be deposited to limit the diffusion of solder into the underlying material.

[005] Known attempts to address the foregoing issues have involved construction of peripheral test pads that are physically separate but electrically connected to the bonding pad by way of interconnect lines. Such structures are commonly referred to as "redistribution layers (RDL)" in the industry. It has been observed that such RDL interconnect lines can introduce undesirable propagation delays to test signals and such delays can lead to lower device speeds. In the case of copper bonding pads, the use of an aluminum-alloy RDL at the uppermost level can lead to additional costs as the fabrication of the aluminum RDL requires additional processing steps of deposition, pattern and etch. Moreover, use of aluminum RDLs may lead to lower device yield as increased processing steps increase the probability of undesirable particles, thus limiting yield.

[006] One approach proposed for wire bond connections, and hence of little practical use for semiconductors involving flip chip connections, is described in IEEE publication titled "Electronic Components and Technology Conference", at page Nos. 1323-1329, May 2003 in paper by Lois Young et al. This approach generally requires stacking at least two physically different metal pads over one another in order to form a probe region that is separate from a wire bond region. More specifically, this proposed approach requires stacking a portion of an enlarged aluminum cap over a copper pad disposed beneath the aluminum cap. A remaining portion of the enlarged aluminum cap (e.g., where the probe region

is located) is disposed over a dielectric material and this arrangement may lead to cracks in the dielectric since the probe can apply a high force over the probe region. Moreover, the specific requirement of an Al "capping pad" over a copper pad is not a mere design choice since performing wire bonding to copper is generally very difficult for a production environment involving wire bond connections. No such considerations are applicable for flip chip connections.

[007] Another known attempt has involved probing wafers after the bumping process is performed. For different considerations, this attempt also fails to provide a fully satisfactory solution. For example, this post-bumping probing technique may lead to incremental costs since there is a possibility that the bumping process (that takes valuable time and resources) may have been performed in an already defective wafer that should have been discarded prior to continuing with any such bump fabrication processes. Moreover, one may not be able to identify mis-processing steps that can occur during the bumping process itself, unless diagnostic partitioning studies are performed on the wafer.

[008] Accordingly, it would be desirable to provide structures and techniques for allowing a semiconductor device or wafer to be tested prior to a bumping process so that wafer level tests can be undertaken without compromising the integrity of the metal bonding pads therein and without introducing delays to signals used for test purposes.

BRIEF DESCRIPTION OF THE DRAWINGS

[009] These and other advantages of the invention will be more apparent from the following description in view of the drawings that show:

[010] FIG. 1 is a top view schematic representation of a prior art metal flip chip bonding pad that has a common region for bumping and probing a semiconductor wafer.

[011] FIG. 2 is a top view of an exemplary flip chip interface assembly embodying aspects of the present invention.

[012] FIGS. 3 and 4 illustrate respective exemplary arrangements for the bonding pad and/or a test pad integrally constructed with the bonding pad.

[013] FIG. 5 illustrates an exemplary embodiment where an interface assembly embodying aspects of the present invention may be used in combination with one or more metal redistribution layers.

DETAILED DESCRIPTION OF THE INVENTION

L

embodying aspects of the present invention. More particularly, FIG. 2 illustrates a conductive test pad 22 integrally constructed with a conductive bonding pad 24. This arrangement provides at least the following advantages: conductive test pad 22 provides a respective probe region 26 where a probe tip may be placed for performing, for example, wafer level testing. The bonding pad 24 includes a bump region 28 that is no longer subject to mechanical contact with the probe tip and resulting surface irregularities. It is envisioned that since the test pad and bonding pad comprise an integral structure that no longer requires interconnect lines and avoids or substantially reduces propagation delays in test signals passing therethrough, an interface assembly embodying aspects of the present invention should lead to more reliable and accurate test results.

[015] FIG. 2 further shows individual passivation openings 30 and 32 for probe region 26 and bump region 28, respectively. It will be understood that the shape of the metal bonding pad 24 is not limited to a polygonal shape being that any other geometrical shape may be used equally effective for the metal bonding pad. For example, FIG. 4 illustrates an exemplary circular shape for a metal bonding pad 44.

[016] Similarly, the shape of test pad 22 is not limited to a square shape since other geometrical shapes, e.g., rectangular, triangular, etc., may work equally effective. Also, the positioning of the test pad 22 relative to the bonding pad 24 is not limited to any specific orientation. For example, FIG. 2 shows an exemplary arrangement where the test pad 22 is positioned at a six o'clock position while FIG. 3 shows another exemplary arrangement where the test pad 22 is positioned at a three o'clock position. Thus, it will be appreciated that the test

pad may be integrally constructed anywhere along the periphery of the bonding pad.

[017] FIG. 5 illustrates an exemplary embodiment where an interface assembly 50 embodying aspects of the present invention may be used in combination with one or more metal redistribution layers, such as metal redistribution layers 52 and 54, for interconnecting the metal bonding pad 24 to, for example, metal runners or interconnect lines, or other pads, either directly or through vias, such as via 56. In one exemplary embodiment, metal redistribution layer 52 may be co-planar with bonding pad 24 and test pad 22, and metal redistribution layer 54, which is electrically connected to metal redistribution layer 52 by way of via 56, may be positioned at a different level relative to bonding pad 24 and test pad 22. It will be appreciated that these redistribution layers 52 and 54 may be used to connect the bonding pad to other areas of the chip, not necessarily to peripheral bond pads, as is practiced in the prior art and described earlier.

[018] While the preferred embodiments of the present invention have been shown and described herein, it will be obvious that such embodiments are provided by way of example only. Numerous variations, changes and substitutions will occur to those of skill in the art without departing from the invention herein. Accordingly, it is intended that the invention be limited only by the spirit and scope of the appended claims.

CLAIMS

WE CLAIM AS OUR INVENTION:

- 1. An interface assembly for a semiconductor wafer, said interface assembly comprising:
- a flip chip bonding pad including a region for performing a bumping process; and
- a test pad integrally constructed with said bonding pad, said test pad being co-planar relative to said flip chip bonding pad and including a probe region for performing wafer-level testing prior to performing said bumping process.
- 2. The interface assembly of claim 1 wherein said test pad may be disposed anywhere along a periphery of said bonding pad.
- 3. The interface assembly of claim 1 wherein said bonding pad comprises a shape selected from the group consisting of a polygonal shape, and a circular shape.
- 4. The interface assembly of claim 1 wherein said test pad comprises a shape selected from the group consisting of a polygonal shape, and a circular shape.
- 5. The interface assembly of claim 1 further comprising a first metal redistribution layer electrically connected to said bonding and test pads, and being co-planar with one another.
- 6. The interface assembly of claim 5 wherein said first metal redistribution layer is electrically connected by way of a via to a second redistribution layer being disposed in a different plane than the first redistribution layer.

- 7. The interface assembly of claim 1 wherein the region to be bumped is defined by a first opening in a passivation layer.
- 8. The interface assembly of claim 7 wherein the probe region is defined by a second opening in said passivation layer, said first and second openings being spaced apart from one another.
- 9. A method for testing a semiconductor wafer prior to performing a flip chip bumping process, said method comprising:

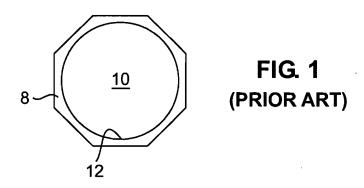
providing a flip chip bonding pad having a region for performing said bumping process;

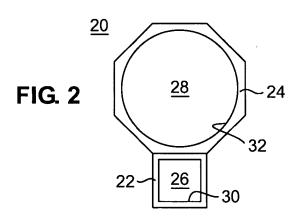
integrally constructing a test pad with said bonding pad; and

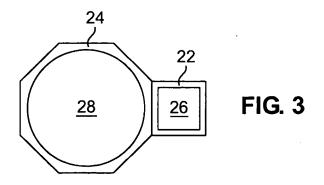
disposing said test pad coplanar with said flip chip bonding pad, said test pad including a probe region for performing a wafer test prior to performing said bumping process.

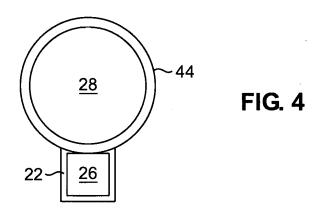
ABSTRACT

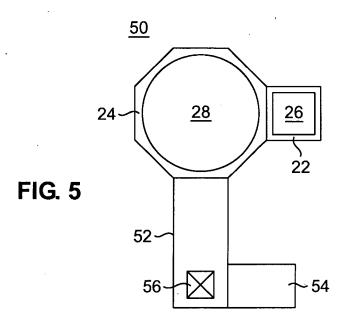
An interface assembly (20) and method for testing a semiconductor wafer prior to performing a flip chip bumping process are provided. The interface assembly includes a flip chip bonding pad (24) having a region (28) for performing the bumping process. A test pad (22) is integrally constructed with the bonding pad and includes a probe region (26) for performing wafer-level testing prior to performing the bumping process. The integral construction of the bonding and testing pads avoids, for example, an introduction of propagation delays to test signals passing therethrough, thereby improving the accuracy and reliability of wafer test results.











PATENT	APPLICATION	SERIAL	NO.	

U.S. DEPARTMENT OF COMMERCE PATENT AND TRADEMARK OFFICE FEE RECORD SHEET

10/04/2004 HALI11 00000001 10953291

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PTO-1556 (5/87)

Application-or-Docket-Number. PATENT APPLICATION FEE DETERMINATION RECORD 10953291 Effective October 1, 2003 CLAIMS AS FILED - PART I OTHER THAN SMALL ENTITY OR SMALL ENTITY TYPE ___ (Column 2) (Column 1) RATE FEE FEE RATE TOTAL CLAIMS OR BASIC FEE 770.00 BASIC FEE 385.00 NUMBER EXTRA NUMBER FILED FOR XS18= XS 9= TOTAL CHARGEABLE CLAIMS OR minus 20= X86= X43= minus 3 = OR INDEPENDENT CLAIMS MULTIPLE DEPENDENT CLAIM PRESENT +290= +145= OR If the difference in column 1 is less than zero, enter "0" in column 2 OR TOTAL 776, TOTAL OTHER THAN CLAIMS AS AMENDED - PART II SMALL ENTITY SMALL ENTITY OR (Column 3) (Column 2) (Column 1) ADDI-HIGHEST ADDI-CLAIMS NUMBER PRESENT TIONAL RATE REMAINING RATE TIONAL **PREVIOUSLY** EXTRA FEE AFTER FEE AMENDMENT PAID FOR **AMENDMENT** X\$18= X\$ 9= OR Minus Total X86= Minus X43= Independent OR FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM +290= +145= OR TOTAL OR ADDIT. FEE ADDIT. FEE (Column 3) (Column 2) (Column 1) ADDI-HIGHEST ADDI-CLAIMS NUMBER PRESENT REMAINING RATE TIONAL RATE TIONAL **PREVIOUSLY EXTRA AFTER** FEE AMENDMENT FEE PAID FOR AMENDMENT X\$18= X\$ 9= OR Minus Total Minus X86= Independent X43=** OR FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM +290= OR +145= TOTAL OR ADDIT. FEE ADDIT. FEE (Column 3) (Column 2) (Column 1) HIGHEST. ADDI-ADDI-CLAIMS NUMBER PRESENT REMAINING TIONAL RATE TIONAL RATE **EXTRA** PREVIOUSLY AFTER ENDMENT FEE FEE PAID FOR AMENDMENT X\$18= X\$ 9= Minus OR **Total** Minus X86= Independent X43= OR FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM +290= OR +145= * If the entry in column 1 is less than the entry in column 2, write "0" in column 3. TOTAL TOTAL OR ™ If the "Highest Number Previously Paid For" IN THIS SPACE is less than 20, enter "20." ADDIT. FEE ***If the "Highest Number Previously Paid For" IN THIS SPACE is less than 3, enter "3." The "Highest Number Previously Paid For" (Total or Independent) is the highest number tound in the appropriate box in column 1. CON.

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Substitute for	form 1449	B/PTO			Complete if Known
		Application Number	Not Yet Assigned		
INFORMATION DISCLOSURE		Filing Date	Simultaneously Herewith		
	STATEMENT BY APPLICANT		First Named Inventor	Mark Adam Bachman	
SIAIL	ALINI C	HAPPL	ICANI	Art Unit	Not Yet Assigned
(Use as	(Use as many sheets as necessary)		Examiner Name	Not Yet Assigned	
Sheet	1	of	2	Attorney Docket Number	Bachman 3-11-16-173

	U.S. PATENT DOCUMENTS										
Examiner Initials	Cite No.1	Document Number Number-Kind Code ^{2(if known)}	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear						
	1	US-2004/0173794 A1	09-09-2004	Yu et al.	, , , , , , , , , , , , , , , , , , , ,						
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Substitute for	form 1449	B/PTO	ICANT First Named Inventor Group Art Unit Not Yet Assigned			
		Application Number	Not Yet Assigned			
INFORM	IATION	DISCLO	OSURE	Filing Date	Simultaneously Herewith	
INFORMATION DISCLOSURE STATEMENT BY APPLICANT (Use as many sheets as necessary) Sheet 2 of 2	First Named Inventor	Mark Adam Bachman				
STATEMENT BY APPLICANT				Group Art Unit	Not Yet Assigned	
(Use as many sheets as necessary)			essary)	Examiner Name	Not Yet Assigned	
Sheet	2	of	2	Attorney Docket Number	Bachman 3-11-16-173	

		NON-PATENT LITERATURE DOCUMENTS	
Examiner Initials	Cite No. ¹	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.	T²
	1	LOIS YONG, TU ANH TRAN, STEPHEN LEE, BILL WILLIAMS and JODY ROSS, "Novel Method of Separating Probe and Wire Bond Regions Without Increasing Die Size," 2003 Electronic Components and Technology Conference, pp. 1323-1329.	
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Examiner	 Date	
Signature	Considered	
Signature	Considered	

EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.

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