IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In the Inter Partes Review of U.S. Patent No. 7,221,173
Trial No.: Not Yet Assigned
Issued: May 22, 2007
Filed: September 29, 2004
Inventors: Bachman et al.
Original Assignee: Agere Systems, Inc.
Title: METHOD AND STRUCTURES FOR TESTING A SEMICONDUCTOR WAFER PRIOR TO PERFORMING A FLIP CHIP BUMPING PROCESS

MAIL STOP PATENT BOARD
Patent Trial and Appeal Board
United States Patent & Trademark Office
P.O. Box 1450
Alexandria, Virginia 22313-1450

DECLARATION OF STANLEY SHANFIELD, Ph.D.

I declare that all statements made herein on my own knowledge are true and that all statements made on information and belief are believed to be true, and further, that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code.

By: 

Dr. Stanley Shanfield

LIST OF MATERIALS CONSIDERED

Exhibit	Description
1001	Bachman et al., U.S. Patent No. 7,221,173 ("the '173 patent")
1002	Prosecution History File Wrapper of the '173 patent
1003	U.S. Patent Publication No. 2003/0094966 ("*Fang*")
1004	U.S. Patent No. 6,869,809 ("*Yu*")
1005	U.S. Patent No. 7,235,412 ("*Mardi*")
1006	U.S. Patent No. 6,765,228 ("*Lin*")
1007	U.S. Patent Publication No. 2003/0173667 ("*Yong*")
1008	Reserved
1009	*Curriculum vitae* of Dr. Stanley Shanfield, Ph.D.
1010	U.S. Patent No. 5,550,480 ("*Nelson*")
1011	U.S. Patent No. 6,744,067 ("*Farnworth*")
1012	U.S. Patent No. 6,597,187 ("*Eldridge*")
1013	Waizman et al., U.S. Patent No. 6,392,301 ("*Waizman*")
1014	Hsu et al., U.S. Patent Application Publication 2005/0037601 ("*Hsu*")

LIST OF APPENDICES

Ex. 1009 *Curriculum vitae* of Stanley Shanfield, Ph.D.

TABLE OF CONTENTS

I. INTRODUCTION

1. My name is Stanley Shanfield, Ph.D.

2. I am making this declaration at the request of Microchip Technology Incorporated and Microsemi Corporation ("Petitioners") in the matter of the *Inter Partes* Review of U.S. Patent No. 7,221,173 ("the '173 patent").

3. I am being compensated for my work in this matter at my standard hourly rate of $385 for consulting services. My compensation in no way depends on the outcome of this proceeding.

4. In preparing this Declaration, I considered all materials cited in the body of this Declaration, which includes but is not limited to the documents identified in the List of Materials Considered. I have relied on information and evidence identified in this declaration, including the '173 patent, its prosecution history, prior art references, the knowledge of a person of ordinary skill in the art ("POSITA"), and other materials listed as appendices to this declaration.

5. This declaration is based on the information currently available to me. To the extent additional information becomes available, I reserve the right to continue my investigation and study, which may include a review of documents and information that may be produced, testimony from depositions not yet taken, and infringement contentions and claim constructions yet to be posed.

II. PROFESSIONAL BACKGROUND

6. I received my B.S. Cum Laude degree in Physics from University of California, Irvine in 1977. I received a Ph.D. in Physics from Massachusetts Institute of Technology in 1981.

7. For more than 38 years I have worked in the semiconductor industry with particular emphasis on semiconductor packaging design, fabrication and production.

8. Early in my career, I became responsible for Raytheon's semiconductor product development line, which produced custom digital and mixed signal silicon devices and ICs for military and commercial electronic systems. I guided the development of automated on-wafer IC test capabilities, including the implementation of post-bump process on-wafer testing. I also established and did development in a prototype packaging, burn-in and test facility. This facility provided a wide variety of ceramic and plastic packaged parts using ICs produced in the development line, including space-qualified packaged devices. In preparation for establishing Raytheon's commercial semiconductor production facilities, I spent time at numerous test and packaging facilities in the US, Japan, Korea, and Indonesia during the early 1990s. In my role as Operations Director at Raytheon Commercial Electronics in the 1990s, I was responsible for the establishment and initial operation of a production IC packaging facility near Seoul, S. Korea. The 24/7 operation

included known-good- (bumped) die measurement, high volume chip and wire bond assembly, and lead frame formation and trimming with injection molded encapsulation of lead frame assemblies. As the Director of Manufacturing & Wafer Fab Technology at AXSUN Technologies, I led the company's electro-optical device manufacturing and created wafer fab, packaging and assembly infrastructure for production of a first-generation product for revenue to multiple customers. At Draper Lab as a division manager in the early 2000s, I established a multi-chip module prototyping facility, and led development work using multi-chip lead frames with a variety of flip chip bumping processes. I invented and led implementation of an ultra-miniature electronics fabrication technology which became a top laboratory priority. Thus, I have hands-on professional expertise with semiconductor packaging design and manufacturing.

III. RELEVANT LEGAL STANDARDS

9. I have been asked to provide my opinion as to whether claims 1-10 of the '173 patent are anticipated by the prior art or would have been obvious to a person of ordinary skill in the art at the time of the invention, in view of the prior art.

10. I am an engineer and scientist by education and profession. The opinions I am expressing in this Declaration involve the application of my engineering knowledge and experience to the evaluation of certain prior art with

respect to the ’173 patent. Aside from my experience in litigation support, my knowledge of patent law is no different than that of any lay person. Therefore, I have requested that the attorneys from Slayden Grubert Beard PLLC, who represent Petitioners, provide me with guidance as to the applicable patent law in this matter. The paragraphs below express my understanding of how I must apply current legal principles related to patentability.

A. Claim Construction

11. It is my understanding that in determining whether a patent claim is anticipated or obvious in view of the prior art in an *inter partes* review (IPR) proceeding, the Patent Trial and Appeal Board (PTAB) gives claims their ordinary and customary meaning, or the meaning that the term would have to a POSITA at the time of the invention. I understand that the claim language, specification, and prosecution history are relevant to determine the meaning of a claim term. I understand that the prosecution history of a patent provides the record of the examination of a patent application before the U.S. Patent and Trademark Office (PTO). The prosecution history provides evidence of how the patent examiner and the inventors understood the patent application and the claims, and can therefore be instructive on how to interpret the claims. My understanding is that extrinsic evidence may also be used in understanding the meaning of a claim term. Extrinsic evidence includes dictionaries, treatises, expert testimony, and prior art. But it is my

understanding that one should first look to the intrinsic evidence in construing claims.

B. Anticipation

12. It is my understanding that a claim is unpatentable under 35 U.S.C. § 102 if each and every element and limitation of the claim is found either expressly or inherently in a single prior art reference. A prior art reference may teach or disclose a claim element either expressly or inherently. In order to disclose an element inherently, a POSITA must recognize from what is expressly disclosed that the inherent element is necessarily present. Additional references may be relied upon in an anticipation challenge to show that a characteristic not disclosed in the reference is inherent in the reference.

C. Obviousness

13. It is my understanding that a claim is unpatentable under 35 U.S.C. § 103 if the claimed subject matter as a whole would have been obvious to a POSITA at the time of the alleged invention. I also understand that an obviousness analysis takes into account the scope and content of the prior art, the differences between the claimed subject matter and the prior art, and the level of ordinary skill in the art at the time of the invention.

14. In determining the scope and content of the prior art, it is my understanding that a reference is considered appropriate prior art if it falls within the

field of the inventor's endeavor. In addition, a reference is prior art if it is reasonably pertinent to the particular problem with which the inventor was involved. A reference is reasonably pertinent if it logically would have commended itself to an inventor's attention in considering his problem. If a reference relates to the same problem as the claimed invention, that supports use of the reference as prior art in an obviousness analysis.

15. To assess the differences between prior art and the claimed subject matter, it is my understanding that 35 U.S.C. § 103 requires that the claimed invention be considered as a whole. I also understand that a finding of obviousness requires more than merely demonstrating that each claim element was known in the prior art. Obviousness requires showing that a POSITA would have been motivated to combine the teachings of the prior art to achieve the claimed invention and would have had a reasonable expectation of success in doing so.

16. It is my understanding that the Supreme Court has recognized several rationales for combining references or modifying a reference to show the obviousness of claimed subject matter. Some of these rationales include: combining prior art elements according to known methods to yield predictable results; simple substitution of one known element for another to obtain predictable results; a predictable use of prior art elements according to their established functions; applying a known technique to a known device (method or product) ready for

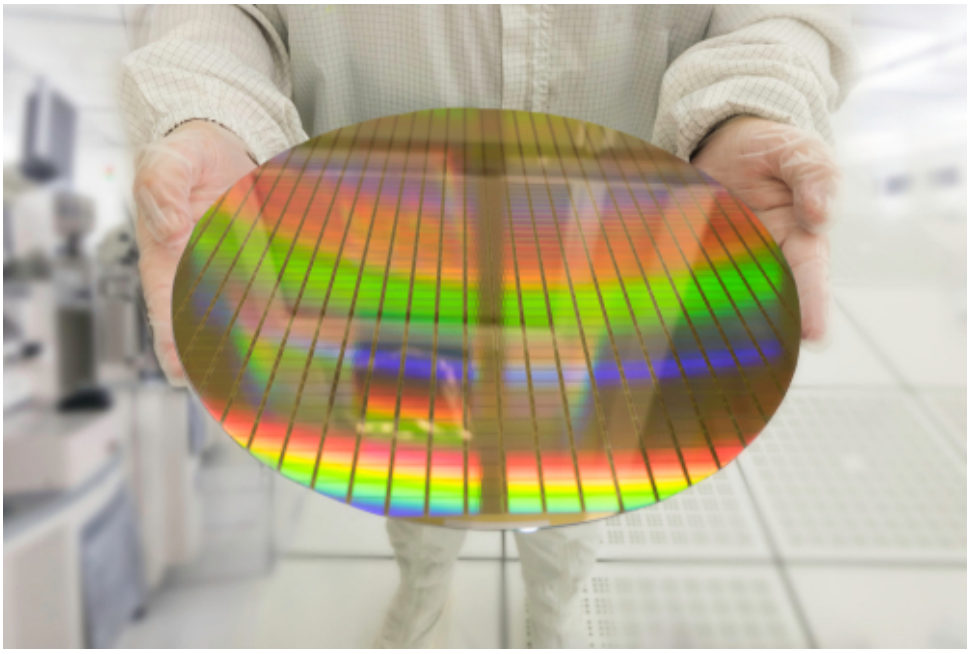
improvement to yield predictable results; choosing from a finite number of identified, predictable solutions, with a reasonable expectation of success; and some teaching, suggestion, or motivation in the prior art that would have led a POSITA to modify the prior art reference or to combine prior art reference teachings to arrive at the claimed invention.

IV. TECHNOLOGY BACKGROUND

17. The technology at issue relates to testing flip chip semiconductor wafers prior to soldering bumps to the wafers. Ex. 1001-1, [54] (Title).

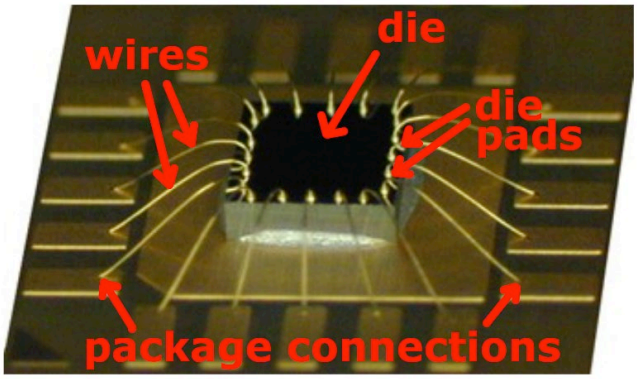
18. Semiconductor devices, such as integrated circuit ("IC") chips, are typically created on a silicon wafer. A silicon wafer is a thin (usually circular) slice of silicon. One wafer can contain tens to hundreds of individual IC chips, also known as "die." The image below shows an example wafer containing a number of ICs (each square is an identical IC):[1]

[1] The images in this Technology Background section were copied from the Internet and accurately illustrate the technology described.

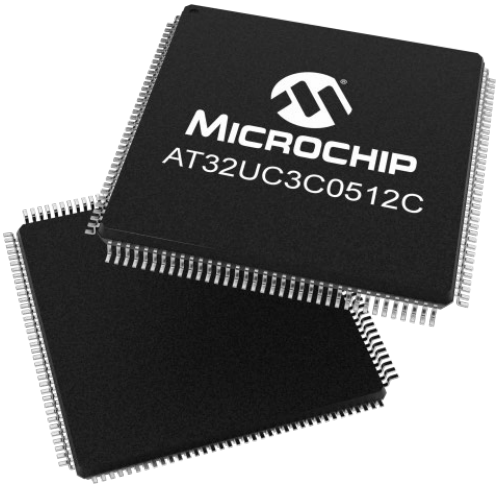


19. Eventually, each die will be cut from the wafer in a process called "dicing." The die will then be put into a "package" so that it can be connected to external circuitry such as a circuit board or another IC or wafer.

20. One method of packaging a die uses a procedure known as "wire bonding." In a wire bonding process, the individual die is patterned with small pads of metal near its edges that serve as the connections to an eventual mechanical package. After the die are cut from the wafer, they are electrically connected to their package terminals via wire bonding. The image below shows metal wires attaching the pads around the perimeter of the die ("die pads") to connections on the package ("package connections"):



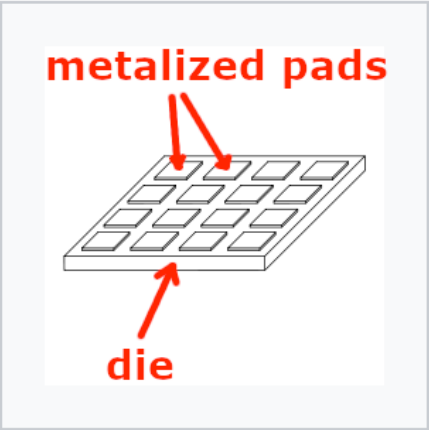
21. The package connections eventually lead to pins on the outside of the package, resulting in a final, packaged product like the one depicted below:



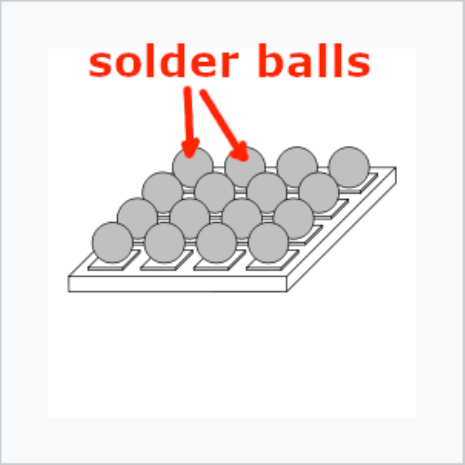
22. "Flip chip" packaging is a packaging technique that was developed in the 1960s. *See* Aviation Week & Space Technology, Sept. 23, 1963, at 96 ("'Flip-Chip' Interconnections—Novel technique for packaging and interconnecting group of semiconductor microcircuit chips, in which 30 to 40 individual circuit function chips are interconnected . . . has been developed by General Electric's Light Military Electronics Dept.…") (available at

https://archive.org/stream/Aviation_Week_1963-09-23#page/n48/mode/1up) (last accessed Aug. 21, 2020)).

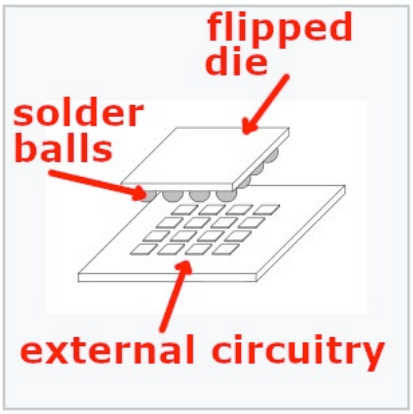
23. For flip chip packaging, the attachment pads—also known as "bond pads"—on the die are metalized to make them more receptive to solder:



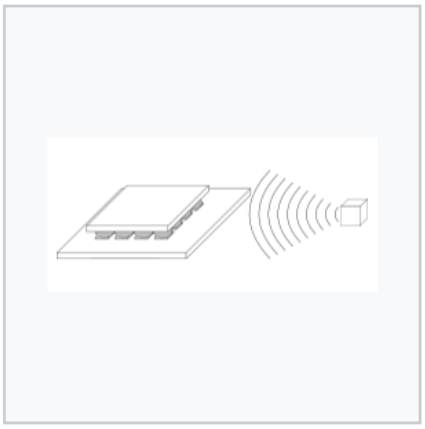
24. Then, a small ball (or "bump") of solder is deposited on each metalized bond pad on the die:



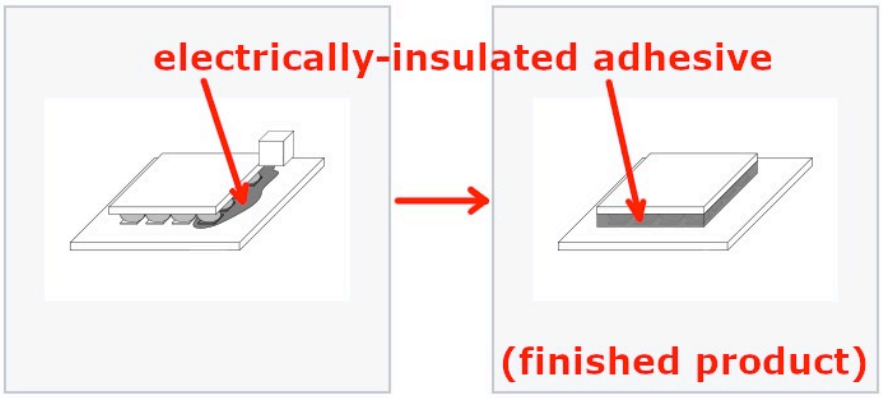
25. The die is flipped and positioned so that the solder balls are facing the connectors on the external circuitry:



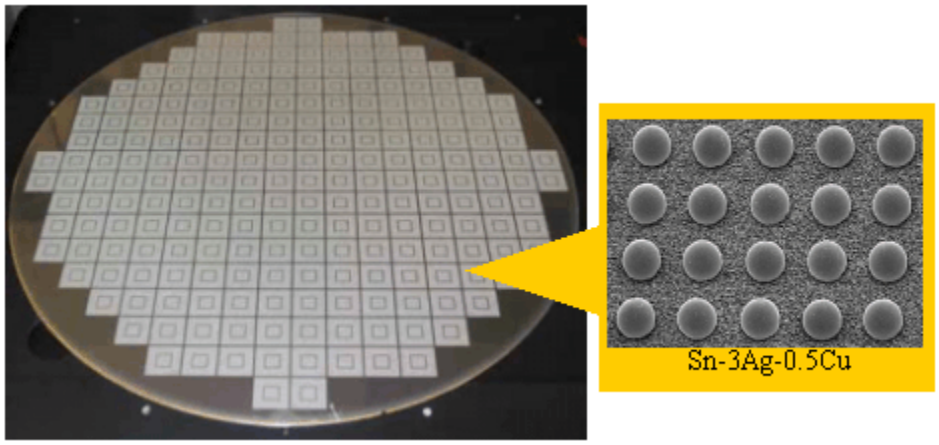
26. The solder balls are then re-melted (typically using hot air):



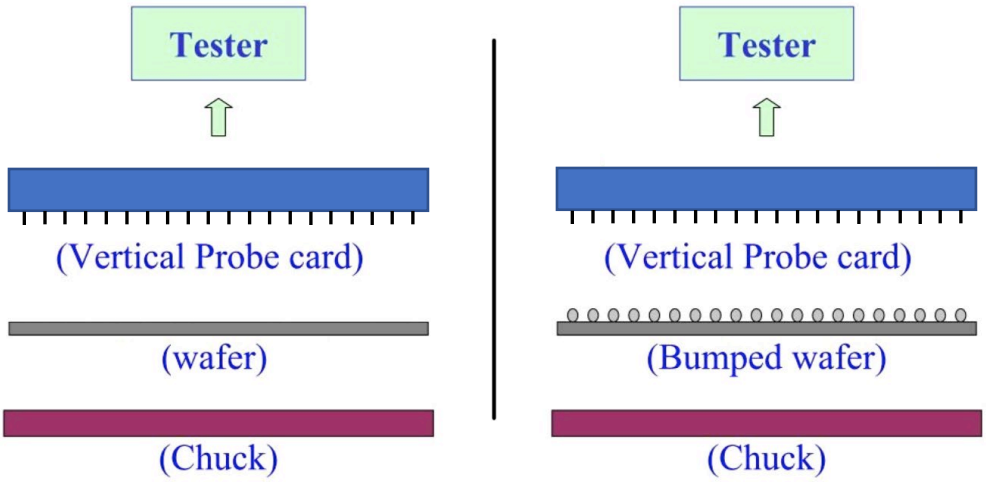
27. The mounted die is "underfilled" using an electrically-insulated adhesive:



28. The above description of flip chip packaging leaves out a number of intermediate steps that involve testing of the die on the wafer. In particular, it is typical that the solder balls/bumps are deposited onto the bond pads on a wafer *before the wafer is diced into individual die*. A wafer with solder balls/bumps is shown below:

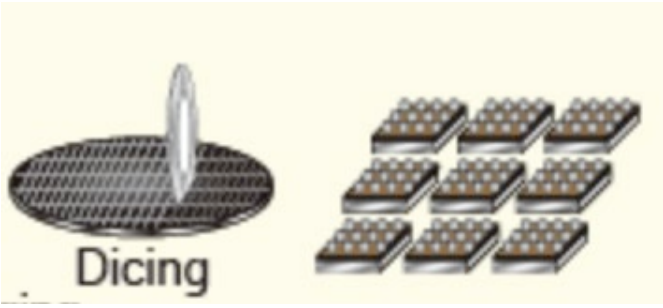


29. At some point before the wafer is diced into individual die/chips, the functionality of the chips are typically tested to make sure the manufacturing process produced functional chips. Testing typically involves "probing" the wafer with a machine known as a tester. The tester is connected to a "probe card" that includes "probes" that sit on top of the wafer during testing. The testing can be done before the wafer is "bumped" (*i.e.*, solder balls deposited) or after, as depicted in the illustrations below. During testing, the probes physically touch either (1) the bond pads on the wafer (without solder balls/bumps) or (2) the solder balls/bumps:



(The "chuck" is a part of the tester that holds the wafer in place during testing.)

30. After the circuitry in each die on the wafer is tested, and the solder balls/bumps deposited, the wafer is diced into individual die, as described above. Unnecessary packaging costs are avoided because die that are found not to be functional during testing are discarded after dicing:



31. Independent of whether wafers incorporate flip chip technology, semiconductor manufacturers are strongly motivated to test die for functionality before any packaging operation. A significant fraction of the cost of manufacturing an integrated circuit is associated with the packaging operation itself, *i.e.* die attachment, wiring bonding, encapsulation, etc. In the very competitive IC

manufacturing environment, testing individual die before packaging is normally an economic necessity.

V. SUMMARY OF THE '173 PATENT

A. The Patent

32. The '173 patent was filed on September 29, 2004 and is titled "Method and Structures for Testing a Semiconductor Wafer Prior to Performing a Flip Chip Bumping Process," and generally describes separate bonding and testing pads. Ex. 1001-1, [22], [54]. "Flip chip" generally refers to a direct electrical connection of face-down (hence, "flipped") electronic components to circuit boards via conductive bumps on the chip bond pads. The '173 patent teaches it was known at the relevant time that a semiconductor device would include a bump region 10 defined by an opening 12 in the passivation layer over a metal bonding pad 8, as shown in Figure 1 and identified as prior art:

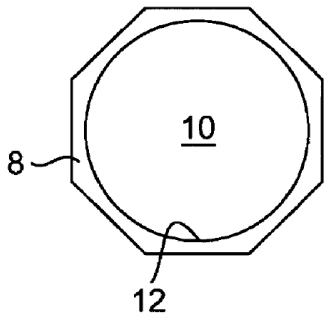
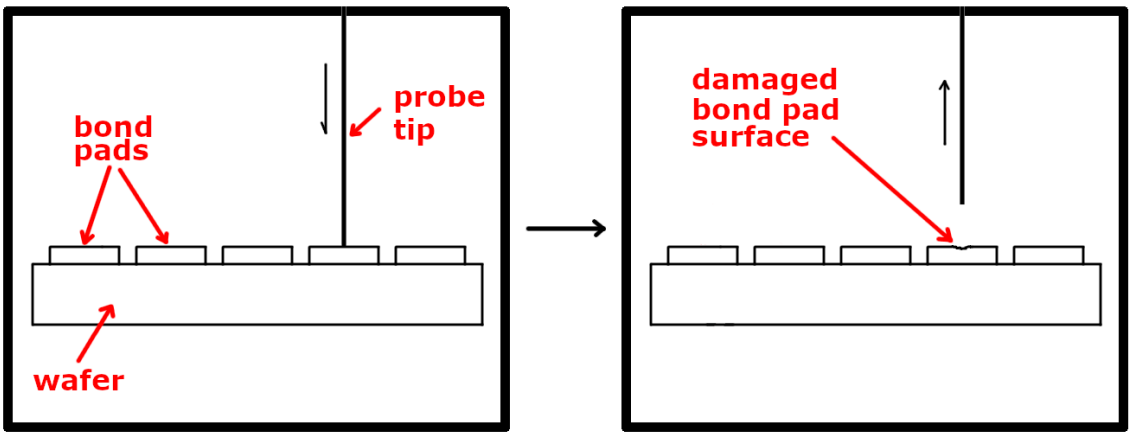


FIG. 1
(PRIOR ART)

Ex. 1001-4, 1:28-37, 2:50-52; Ex. 1001-2, Fig. 1. It was also known to solder an electrically conductive bump to the bump region 10 to create a "flip chip" assembly.

33. The ’173 patent alleges damage to the bump region of the bond pad occurs when a test probe tip contacts the bump region prior to adding the solder bump. Ex. 1001-4, 1:38-56. The test probe tip gouges the bump region and forms irregularities in the surface, which makes it difficult to adhere or solder the electrically conductive bump to the bump region. Ex. 1001-4, 1:38-56. The alleged problem is illustrated in the cross-sectional view below:



34. Admitted prior art attempted to address these problems, including using test pads that are physically separate but electrically connected (by interconnect/trace lines) to the bond pad. Ex. 1001-4, 1:56-60. Because the test pads are physically separate from the bond pads, the probe tip may damage the test pad without consequence.

35. The solder bump is placed on the bond pad, not the damaged test pad. This type of prior art test pad is discussed in U.S. Patent 6,869,809 (“*Yu*”) (Ex. 1004), which was cited during prosecution of the ’173 patent. Ex. 1001-1, [56]. *Yu*’s Figure

3A shows test pads 208a that are physically separate from bond pads 208, connected by interconnect/trace lines 209:

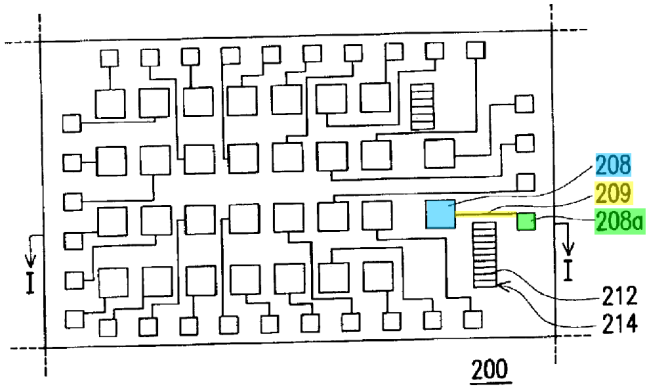


FIG. 3A

Ex. 1004-8, 4:52-55; Ex. 1004-4, Fig. 3A.[2]

36. According to the '173 patent, these interconnect lines between are problematic because (1) they introduce undesirable propagation delays to test signals, and (2) they require "additional processing steps of deposition, pattern and etch." Ex. 1001-4, 1:62-2:4.

37. Another admitted prior art testing method involved probing the wafers after the bumping process is performed. Ex. 1001-4, 2:26-27. "[T]his attempt also fails to provide a fully satisfactory solution. For example, this post-bumping probing technique may lead to incremental costs since there is a possibility that the bumping

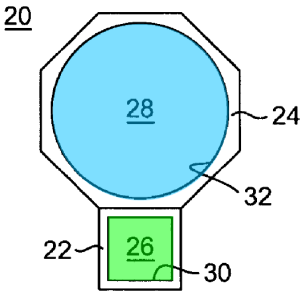
[2] All highlighting, colors, and emphasis added to patent text or figures herein has been added. Any such citations should be understood to include an "(annotated)" and/or "(emphasis added)" parenthetical.

process (that takes valuable time and resources) may have been performed in an already defective wafer….” Ex. 1001-4, 2:27-32.

38. The ’173 patent explains “it would be desirable to provide structures and techniques for allowing a semiconductor device or wafer to be tested prior to a bumping process so that wafer level tests can be undertaken without compromising the integrity of the metal bonding pads therein and without introducing delays to signals used for test purposes.” Ex. 1001-4, 2:38-43.

39. Accordingly, the ’173 patent discloses “a conductive test pad 22 integrally constructed with a conductive bonding pad 24”:

FIG. 2



Ex. 1001-5, 3:1-2, and Fig. 2. The **bump region 28** and the **probe region 26** are exposed through individual openings 32 and 30, respectively, in the passivation layer. The ’173 patent suggests this configuration is advantageous because:

> conductive test pad 22 provides a respective probe region 26 where a probe tip may be placed for performing, for example, wafer level testing. The bonding pad 24 includes a bump region 28 that is no longer subject to mechanical contact with the probe tip and resulting surface irregularities. It is envisioned that since the test pad and bonding pad

> comprise an integral structure that no longer requires interconnect lines and avoids or substantially reduces propagation delays in test signals passing therethrough, an interface assembly embodying aspects of the present invention should lead to more reliable and accurate test results.

Ex. 1001-5, 3:4-14.

B. Prosecution History

40. The application for the '173 patent was filed September 29, 2004. Ex. 1001-1, [22]. The '173 patent issued on May 22, 2007. *Id.*, [45]. During examination of the '173 patent, the Examiner rejected claims 1-6 and 7-9 as anticipated by U.S. Publication No. 2003/0094966 by Fang ("Fang"). Ex. 1002-105 (citing Ex. 1003, Fang). In particular, the rejection was that "Fang discloses in Figs. 3, a device comprising a flip chip bonding pad (32 of figure 3) including a region for performing a bumping (34, 35 of figure 3), and a test pad (31 of figure 3) integrally constructed with the bonding pad (32), the test pad being co-planar relative to the flip chip bonding pad and including a probe region (via 31) for performing wafer-level testing prior to performing the bumping process (see the abstract, and col. 1, lines 15-19 of paragraph 15)." Ex. 1002-105.

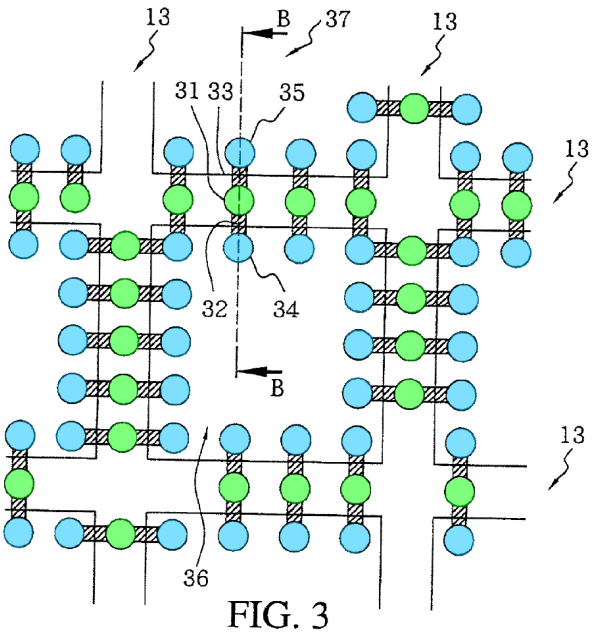


FIG. 3

Ex. 1003-2, Fig. 3. In response, the applicant argued:

> [T]he bumps in Fang are not integrally constructed with one another. More particularly, such post-bumping structures require separate metal traces in order to be electrically interconnected to one another. By way of comparison, claim 1 recites a test pad integrally constructed with a bonding pad.

Ex. 1002-99.

41. The claims were next rejected as anticipated by U.S. Patent No. 6,869,809 ("*Yu*"). Ex. 1002-36 (citing Ex. 1004). In particular, the Examiner found *Yu* discloses the elements of claims 1 and 9.

42. *Yu* et al. discloses in Figs. 3-5, a device comprising a flip chip **bonding pad (208** of figure 4A) including a region for performing a bumping (col. 5, lines 15-18); and a **test pad (208a** of figure 4A) integrally constructed with the **bonding**

pad (208), the test pad being co-planar relative to the flip chip bonding pad and including a probe region (202 of figure 3B) for performing wafer-level testing prior to performing the bumping process (see the abstract, and col. 5, lines 10-20). Ex. 1002-36. In response, the applicant amended the claims to expressly require "a test pad integrally constructed with said bonding pad that form an integral conductive structure such that separate interconnect testing lines from said test pad to said bonding pad are not present in said integral structure." Ex. 1002-22. The applicant argued, "*Yu* teaches that the test pads 208a are electrically connected to various flip-chip bonding pads 208 through trace lines 209, as shown in FIG. 3A." Ex. 1002-25.

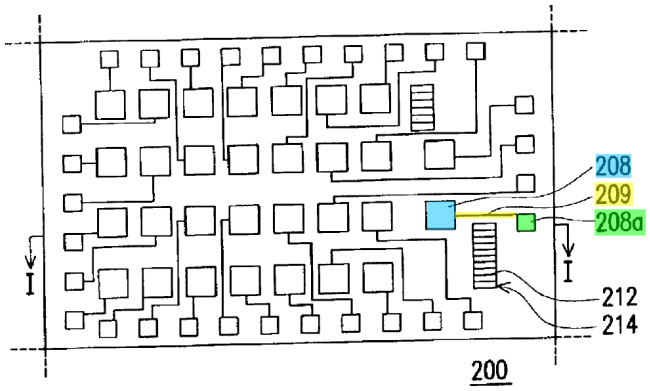


FIG. 3A

Ex. 1004-4, Fig. 3A. The amended claims were then allowed. Ex. 1002-11.

43. I have reviewed the prosecution history of the '173 patent. None of the events or arguments impact my analysis, but I reserve the right to consider those

events and the references cited therein should Patent Owner raise a claim construction argument.

VI. LEVEL OF SKILL IN THE ART

44. In my opinion, a "person of ordinary skill in the art" (POSITA) at the time of the effective filing date of the '173 patent would have possessed at least a bachelor's degree in physics or electrical engineering or a related field as well as at least three (3) years of experience in semiconductor wafer and packaging engineering and development, or alternatively would have an equivalent combination of advanced education and practical experience, such as a master's or a Ph.D. degree and at least one (1) year of experience in semiconductor wafer and packaging engineering and development. This opinion is based on my personal experience in hiring and working directly with wafer test engineers in high volume wafer fab environments. A typical test engineer at the time (2004) was highly knowledgeable in the electrical characteristics of circuitry under test, and had a good grasp of wafer and packaging fabrication processes.

45. It is my understanding that when interpreting the claims of the '173 patent, I must do so based on the perspective of a POSITA at the relevant priority date. For the purpose of this proceeding, I will consider September 29, 2004 (*i.e.*, the filing date) to be the relevant date to ascertain the perspective of one of ordinary skill in the art.

VII. CLAIM CONSTRUCTION

46. It is my understanding that the claims of the ’173 patent should be given their ordinary and customary meaning, and that claim terms should be given the meaning that the terms would have to a POSITA at the time of the invention. This is the meaning I have applied to the claims in my analysis.

VIII. OVERVIEW OF CONCLUSIONS

47. I have reviewed and agree with the analysis in the Petition for *inter partes* review of the ’173 patent. It is my opinion that each and every limitation of each and every challenged claim would have been anticipated and/or obvious to a person of ordinary skill in the art at the time of the alleged invention in view of the prior art cited in the Petition and further explained in this Declaration. Below is a summary of my conclusions:

- It is my opinion that claims 1-10 of the ’173 patent are anticipated or rendered obvious by *Mardi* (U.S. Patent No. 7,235,412).
- It is my opinion that claims 1-7 and 9-10 of the ’173 patent are anticipated or rendered obvious by *Lin* (U.S. Patent No. 6,765,228).
- It is my opinion that claims 5-6 and 10 of the ’173 patent are obvious in view of *Lin* (U.S. Patent No. 6,765,228) and *Yong* (U.S. Patent Publication No. 2003/0173667).

IX. OVERVIEW OF THE PRIOR ART

A. *Mardi*

48. U.S. Patent No. 7,235,412 ("*Mardi*") (Ex. 1005), issued to *Mardi* et al. and titled "Semiconductor Component Having Test Pads and Method and Apparatus for Testing Same," was filed on May 11, 2004. Ex. 1005-1, [22]. I am told *Mardi* qualifies as §102(e) prior art because it was filed before the '173 patent's September 29, 2004 filing date. *Mardi* is directed to testing flip chip semiconductor wafers prior to bump soldering. Ex. 1005-1, [52], [57].

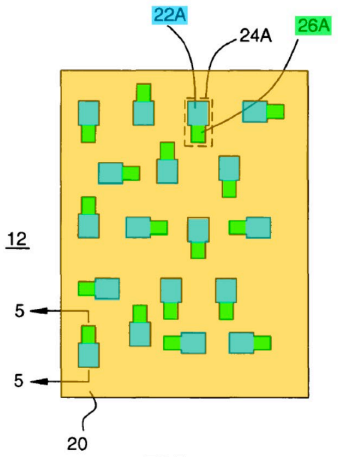


FIG. 4

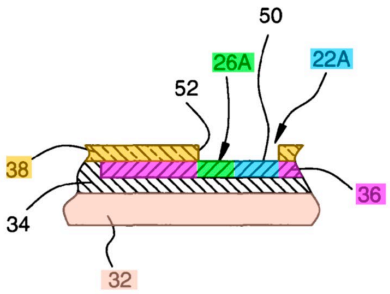


FIG. 5

Ex. 1005-3, Figs. 4-5. *Mardi* discloses **test pads 26A** and **bond pads 22A** are integrated together as "separate regions" of a **top conductor layer 36**. Ex. 1005-8, 5:34-44. A method for testing flip chip semiconductor wafers is also disclosed, wherein the semiconductors are probe tested via the test pads prior to soldering bumps on the bond pads. Ex. 1005-9, 7:24-36; Ex. 1005-4, Fig. 6.

49. *Mardi* discloses at least two exemplary embodiments. The first is depicted in Figures 2-3 and 7-8 ("First *Mardi* Embodiment"):

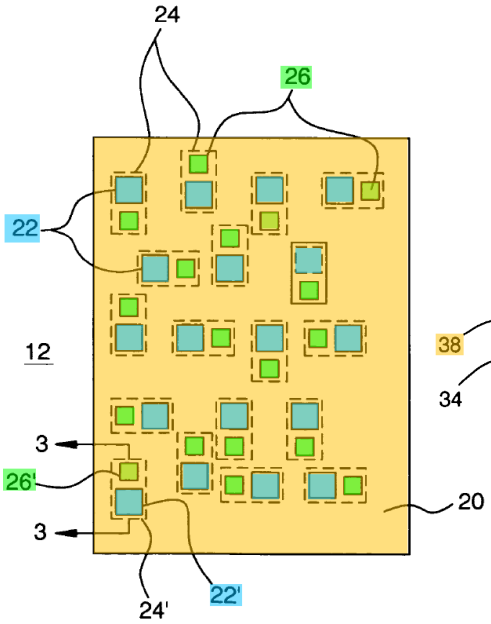


FIG. 2

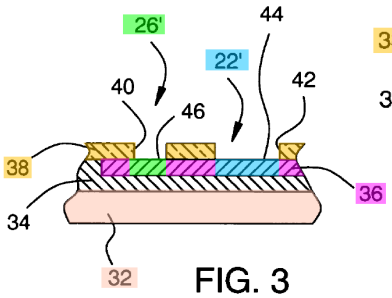


FIG. 3

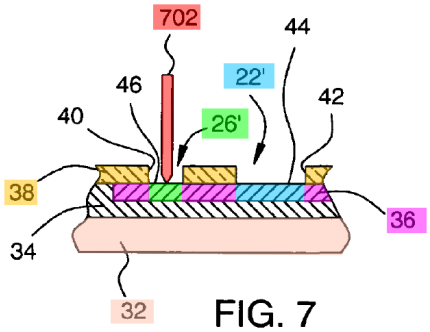


FIG. 7

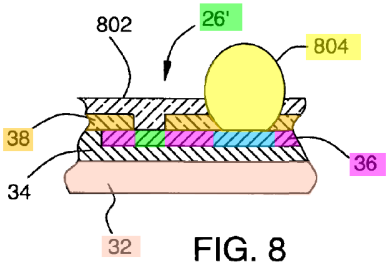


FIG. 8

Ex. 1005-6, 2:53-59; Ex. 1005-7, 3:3-5; Ex. 1005-2, Figs. 2-3; Ex. 1005-5, Figs. 7-8. The second is depicted in Figures 4-5 and 9-10 ("Second *Mardi* Embodiment"):

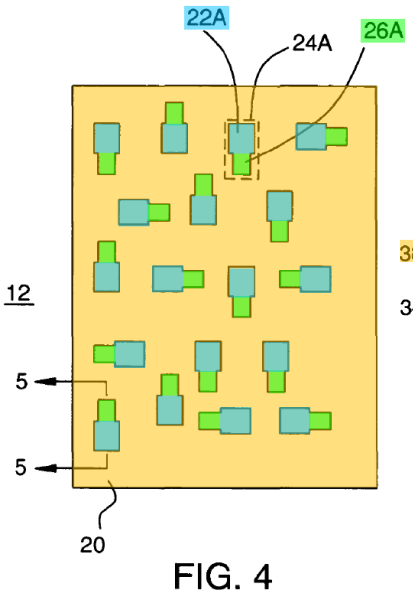


FIG. 4

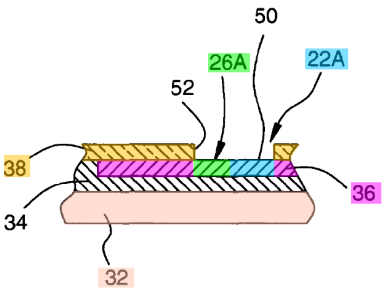


FIG. 5

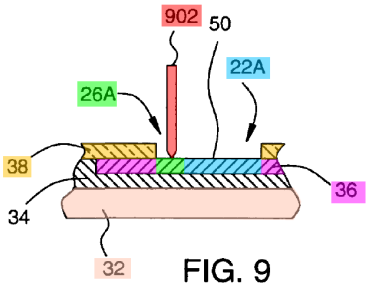


FIG. 9

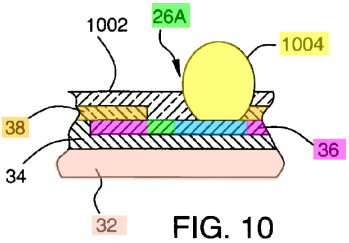


FIG. 10

Ex. 1005-6, 2:6-65; Ex. 1005-7, 3:6-8; Ex. 1005-3, Figs. 4-5; Ex. 1005-5, Figs. 9-10.

50. One difference between the two embodiments is the number of openings in passivation layer 38. In the First *Mardi* Embodiment, there are separate openings for the test pad and bond pad ("opening 40" and "opening 42"), while the Second *Mardi* Embodiment only has one opening for both ("opening 52"):

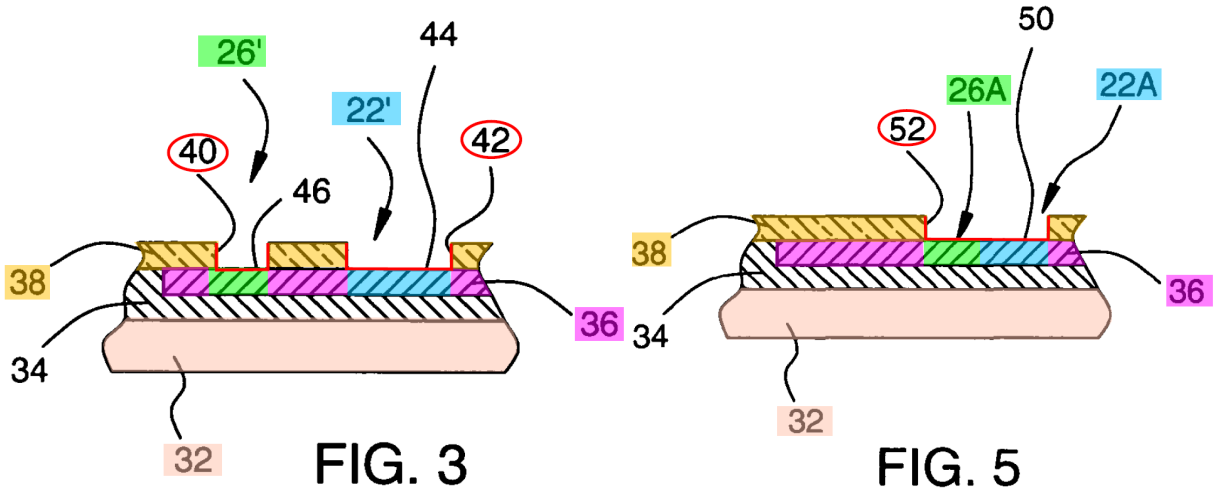


FIG. 3 FIG. 5

Ex. 1005-7, 4:59-62; Ex. 1005-8, 5:34-35; and Ex. 1005-2 to -3, Figs. 3, 5.

B. *Lin*

51. U.S. Patent 6,765,228 ("Lin") (Ex. 1006) issued to *Lin et al*. and is titled "Bonding Pad with Separate Bonding and Probing Areas." *Lin* was filed on October 11, 2002 and issued on July 20, 2004 (Ex. 1006-1, [45]). I have been advised *Lin* qualifies as §102(a) and (e) prior art because it was filed and published before the '173 patent's September 29, 2004 filing date. *Lin* is directed to flip chip

semiconductor wafers having bond pads with separate areas for probe needle contact and wire bonding. Ex. 1006-1, [54], [57].

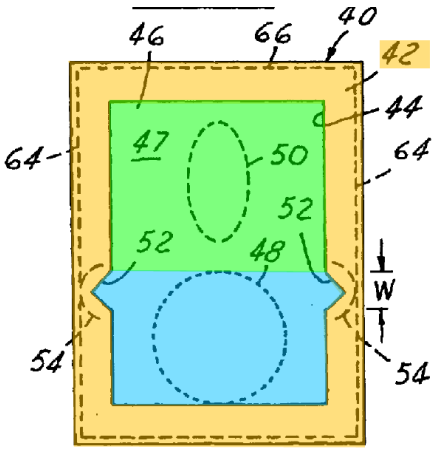


FIG. 5

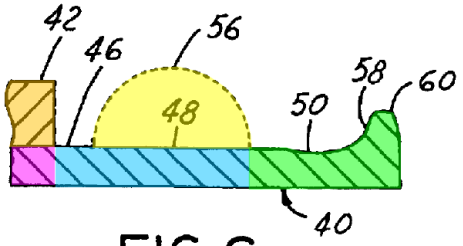


FIG. 6

Ex. 1006-2 to -3, Figs. 5-6. The surface 47 of the bonding pad 46 has a **wire bonding area 48** and a **probe needle contact area 50**. Ex. 1006-5 to -6, 4:56-5:4. Prior to packaging and formation of solder bumps on the respective bonding pads, the chip is subjected to parametric testing which utilizes test structures to assess the electrical characteristics and reliability of the devices on the wafer. Ex. 1006-6, 5:30-45. Probe cards with probe needles are used to interface between the devices on the chip and the test equipment. *Id.* Each probe needle forms a scrub mark and a hump of pad material, which is why separate test regions are provided so the bond region remains unmarked for effective bonding. *Id.*

C. *Yong*

52. U.S. Publication 2003/0173667 ("*Yong*") lists inventors *Yong et al.* and is titled "Semiconductor Device Having a Bond Pad and Method Therefor." Ex.

1007-1, [54], [76]. *Yong* published on September 18, 2003. Ex. 1007-1, [43]. I have been advised *Yong* qualifies as §102(a)-(b), and (e) prior art because it published more than one year prior to the '173 patent's September 29, 2004 filing date. *Yong* relates to probe and wire bond regions of a bond pad. Ex. 1007-1, [54], [57].

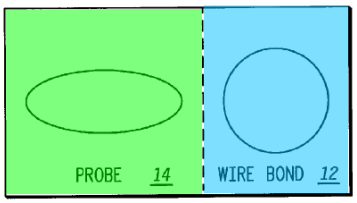


FIG.1

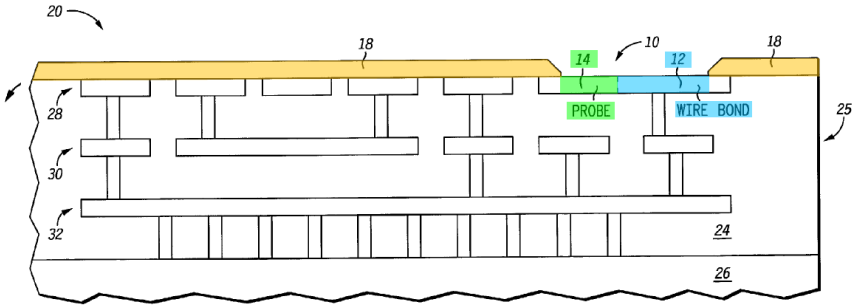


FIG.2

Ex. 1007-2, Figs. 1-2 (excerpted). While the **probe region 14** and **wire bond region 12** are merely separate regions of an integrated bond pad, the separate regions prevent the final metal layer pad from being damaged by probe testing. Ex. 1007-10 to -12, [0013], [0023].

X. GROUND 1: CLAIMS 1-10 ARE ANTICIPATED BY *MARDI*

A. Independent Claim 1

1. Element 1[preamble] — "an interface assembly for a semiconductor wafer"

53. To the extent the preamble is limiting, *Mardi* discloses this element.

54. *Mardi* teaches a semiconductor wafer with bond pads and test pad interfaces ("interface assembly") for testing the semiconductor wafer prior to soldering balls to the bond pads. Ex. 1005-1, [57] ("A semiconductor component

having **test pads** and a method and apparatus for testing the same is described."). The "invention relates to testing a semiconductor component" (Ex. 1005-6, 1:62-63), and "[t]he semiconductor component 11 comprises a substrate 10 … [which] may be a wafer…." Ex. 1005-7, 3:18-23. The **test pad** provides an "interface assembly" whereby a **probe element 902** may be brought into contact with the **test pad 26A** to interface with the semiconductor wafer.

55. In my opinion, the **test pad** provides an "interface assembly" whereby a **probe element 902** may be brought into contact with the **test pad 26A** to interface with the semiconductor wafer.

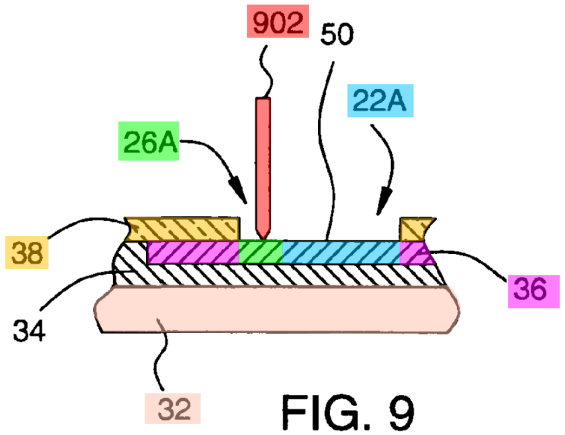


FIG. 9

Ex. 1005-5, Fig. 9. "In this manner, the die or dice of the substrate may be tested or 'burned-in' before further processing (e.g., bumping, packaging, etc.)." Ex. 1005-8, 6:21-23.

2. Element 1[a] — "a flip chip bonding pad including a region for performing a bumping process; and"

56. *Mardi* discloses this element. In *Mardi*, "bond pad 22A" corresponds to the claimed "flip chip bonding pad including a region for performing a bumping process."

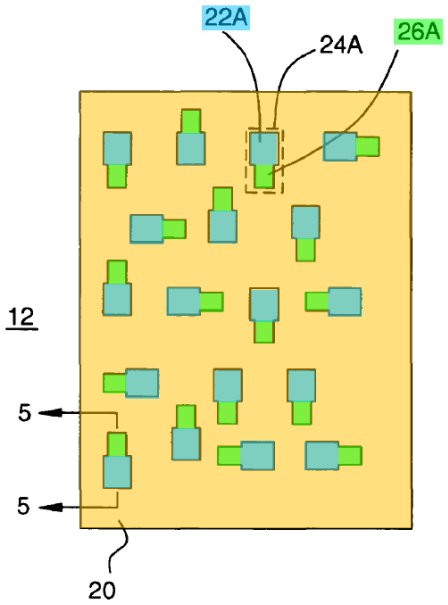


FIG. 4

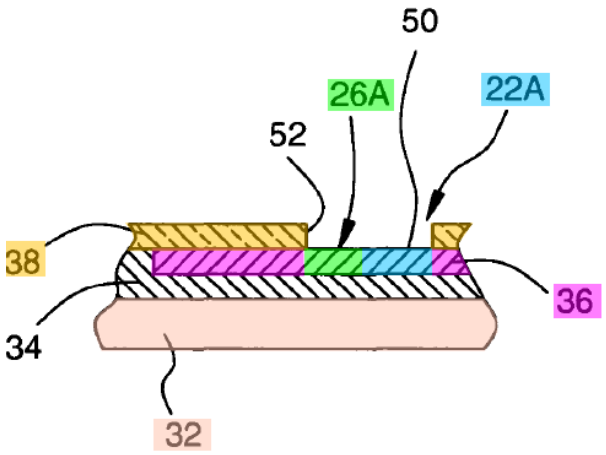


FIG. 5

Ex. 1005-3, Figs. 4-5. The "test/bond pad pair 24A" is a flip chip bonding pad. Ex. 1005-8, 5:5-11 ("bond pads 22 are adapted to support bumped contacts (e.g., solder balls) for providing external electrical connections for the semiconductor die 12. Once the bumped contacts are in place, the semiconductor die 12 may be 'flip chip' mounted (i.e., circuit-side down) to mating electrodes on a supporting substrate, such as a circuit board or lead-frame.")

57. The **bond pad 22A** includes a region for performing a bumping process because "bond pads 22 are adapted to support bumped contacts (e.g., solder balls)

for providing external electrical connections for the semiconductor die 12." Ex. 1005-8, 5:5-11; *see also* Ex. 1005-8, 5:26-33 ("With simultaneous reference to FIGS. 4 and 5, in the present embodiment, the semiconductor die 12 includes a pattern of test/bond pad pairs 24A embedded within the die passivation layer 38. Each of the test/bond pad pairs 24A comprises a die contact portion ('**bond pad 22A**') in electrical communication with a test contact portion ('**test pad 26A**'). FIG. 5 shows a cross-section of one of the test/bond pad pairs 24A.")

3. Element 1[b] — "a test pad integrally constructed with said bonding pad that form an integral conductive structure such that separate interconnect testing lines from said test pad to said bonding pad are not present in said integral structure"

58. *Mardi* discloses this element. The "**test pad 26A**" in *Mardi* corresponds to the claimed "test pad."

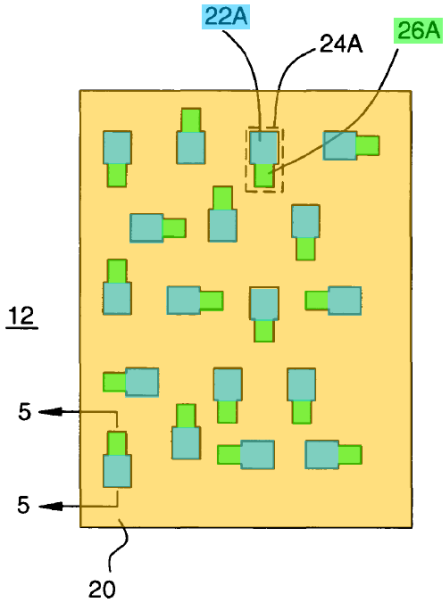


FIG. 4

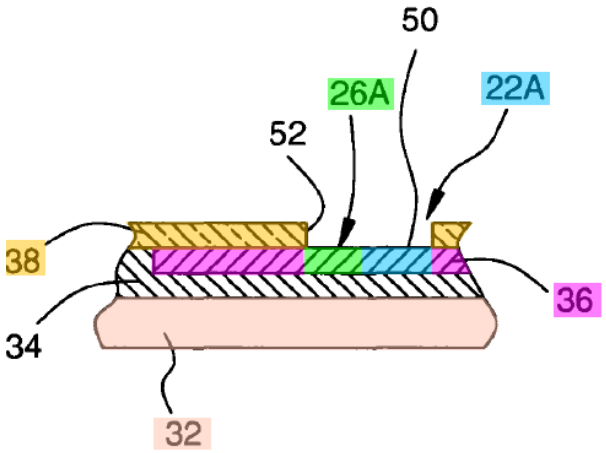


FIG. 5

Ex. 1005-3, Figs. 4-5.

59. Further, the "**bond pad 22A**" and the "**test pad 26A**" are integrally constructed as an integral conductive structure, as claimed. Ex. 1005-8, 5:29-33 ("the semiconductor die 12 includes a pattern of test/bond pad pairs 24A embedded within the die passivation layer 38. Each of the test/bond pad pairs 24A comprises a die contact portion ('**bond pad 22A**') in electrical communication with a test contact portion ('**test pad 26A**'). FIG. 5 shows a cross-section of one of the test/bond pad pairs 24A.")

60. There are no interconnect testing lines between the **test pad 26A** and the **bond pad 22A**. Ex. 1005-8, 5:34-44 ("The top conductor layer 36 electrically couples the **bond pad 22A** with the **test pad 26A**. The **test pad 26A** may be considered as an 'extended test pad' with respect to the **bond pad 22A**.") The integral nature of the test/bond pad pairs 24A is evident from (1) the shape of element 24A in Figure 4, and (2) the fact that the **bond pad 22A** and the **test pad 26A** are merely "separate regions of the section 50 of the top conductor layer 36" (shown in Fig. 5). Ex. 1005-8, 5:39-44; Ex. 1005-3, Fig. 4.

61. Accordingly, it is my opinion that *Mardi* teaches a test pad integrally constructed with the bonding pad with no interconnect testing lines.

4. Element 1[c] — "said test pad being coplanar relative to said flip chip bonding pad and"

62. *Mardi* discloses this element. In *Mardi*, **test pad 26A** is coplanar with the **bond pad 22A** because they are merely "regions" of the same conductor layer.

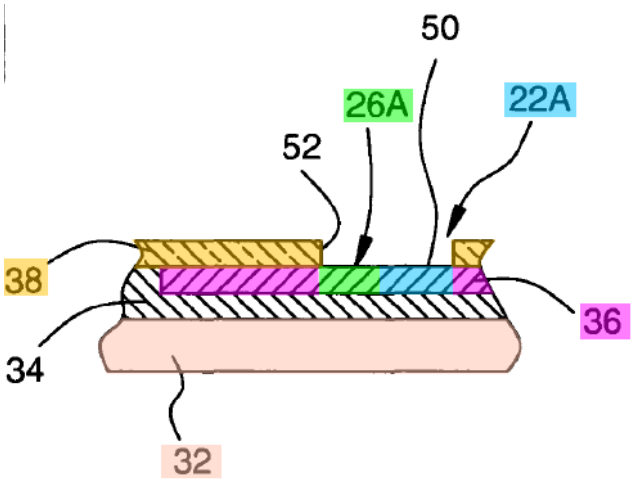


FIG. 5

Ex. 1005-3, Fig. 5; Ex. 1005-8, 5:34-44 ("In the present embodiment, each of the test/bond pad pairs 24A is located in an opening 52 of the passivation layer 38 and comprises a section 50 of the top conductor layer 36. A first portion of the section 50 defines the **bond pad 22A**, and a second portion of the section 50 defines the **test pad 26A**. That is, the **bond pad 22A** and the **test pad 26A** comprise ***separate regions of the section 50 of the top conductor layer 36***.")

5. Element 1[d] — "said test pad . . . including a probe region for performing wafer-level testing prior to performing said bumping process"

63. *Mardi* discloses this element. Figure 9 illustrates that **test pad 26A** is a probe region during wafer-level testing because "a **probe element 902** is in contact

with the portion of the conductor section 50 that defines the **test pad 26A**." Ex. 1005-9, 7:31-32.

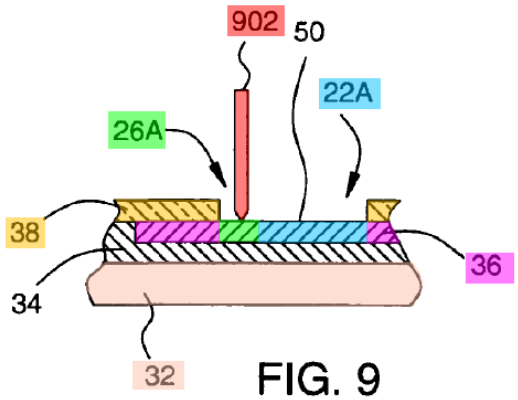


FIG. 9

Ex. 1005-5, Fig. 9. Further, "the **test pad 26A** may be used to test the semiconductor die 12 ***before the semiconductor die 12 is bumped*** [*i.e.* the 'bumping process'] and without contacting the **bond pad 22A**." Ex. 1005-8, 5:54-56.

64. Figure 6 confirms the test pad's probe region is for performing wafer-level testing prior to performing the bumping process:

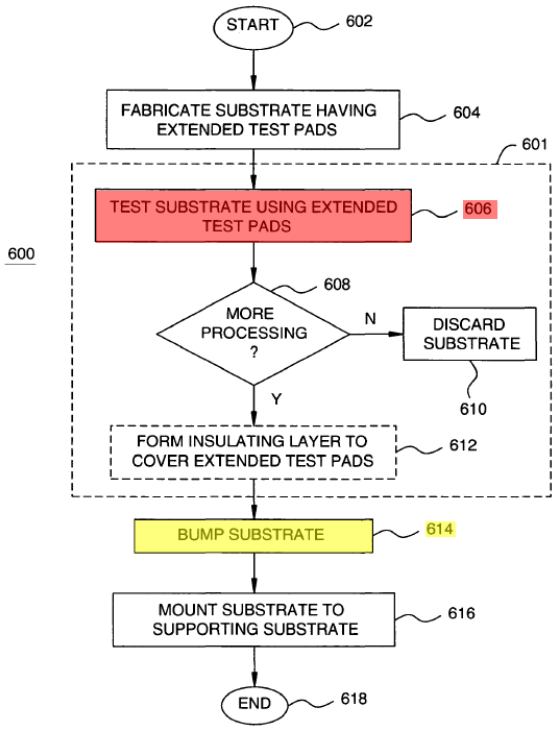


FIG. 6

Ex. 1005-4, Fig. 6. Test pads are fabricated in step 604, the substrate is tested using the probe regions at step 606 ("wafer-level testing"), and the "bumping process" is performed later in step 614. Ex. 1005-9, 7:24-36 ("… FIG. 5 depicts a cross-section of the test/bond pad pair 24A after ***fabrication at step 604***. FIG. 9 depicts a cross-section of the test/bond pad pair 24A during the ***testing at step 606***. Notably, a **probe element 902** is in contact with the portion of the conductor section 50 that defines the **test pad 26A**. The **probe element 902** does not contact the portion of the conductor section 50 that defines the **bond pad 22A**. Thus, damage to the **bond pad 22A** is avoided during the testing at step 606."); Ex. 1005-8, 6:51-55 ("At ***step 614,***

the semiconductor substrate is bumped … using a conventional bumping process.").

65. Figure 10 shows "a bumped contact 1004 formed in electrical communication with the **bump pad 22A**."

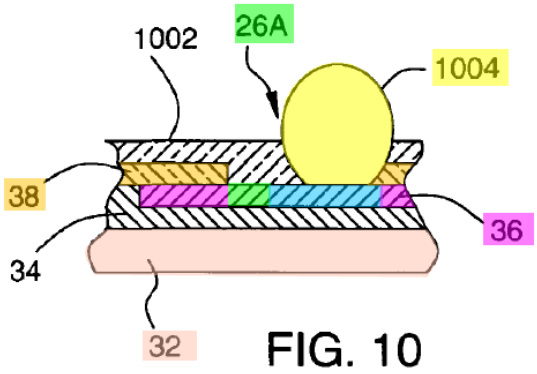


FIG. 10

Ex. 1005-5, Fig. 10. Thus, it is my opinion that *Mardi* teaches the surface of the **test pad 26A** is a probe region for testing the wafer before a **bump** is soldered to the **bond pad 22A**.

6. All Claim 1 Elements: First *Mardi* Embodiment

65.1. The above mapping of claim elements 1[preamble]-[d] is directed at the Second *Mardi* Embodiment found in Figures 4-5 and 9-10. That mapping applies equally to the First *Mardi* Embodiment shown in Figures 2-3 and 7-8 because *Mardi* discloses the following elements are equivalent in the two embodiments:

First *Mardi* Embodiment	**Second *Mardi* Embodiment**
bond pad 22'	bond pad 22A
test pad 26'	test pad 26A
probe element 702	probe element 902
bumped contact 804	bumped contact 1004
passivation layer 38	passivation layer 38

top conductive layer 36	top conductive layer 36
internal conductor portion 34	internal conductor portion 34

Compare Ex. 1005, 3:34-4:5, 7:4-23, Figs. 2-3 & 7-8 (First *Mardi* Embodiment), *with* Ex. 1005, 5:18-44, 7:24-45, Figs. 4-5 & 9-10 (Second *Mardi* Embodiment).

B. Claim 2 — "The interface assembly of claim 1 wherein said test pad may be disposed anywhere along a periphery of said bonding pad."

66. *Mardi* discloses this claim. *Mardi* explains the test pad in the First Mardi Embodiment may be anywhere along the periphery of the bonding pad. Ex. 1005-7, 4:30-33 ("Illustratively, the test pad 26' may be disposed at any point around the perimeter of the bond pad 22'….") Likewise, *Mardi* explains the test pad in the Second Mardi Embodiment may anywhere along the periphery of the bond pad because "[t]he shapes and sizes of the bond pad 22A and the test pad 26A may be selected substantially as described above with respect to FIGS. 2 and 3," *i.e.,* the First Mardi Embodiment. Ex. 1005-8, 5:48-50. Accordingly, it is my opinion that *Mardi* discloses the features of claim 2.

C. Claim 3 — "The interface assembly of claim 1 wherein said bonding pad comprises a shape selected from the group consisting of a polygonal shape, and a circular shape."

67. *Mardi* discloses this claim. *Mardi* expressly describes polygonal and circular shaped bonding pads: "The bond pad 22A and the test pads 26 may be generally square as illustrated in FIG. 2, or may have other shapes known in the art

(e.g., other polygonal or elliptical shapes)." Ex. 1005-7, 4:6-8. Accordingly, it is my opinion that *Mardi* discloses the features of claim 3.

D. Claim 4 — "The interface assembly of claim 1 wherein said test pad comprises a shape selected from the group consisting of a polygonal shape, and a circular shape."

68. *Mardi* discloses this claim. *Mardi* expressly describes polygonal and circular shaped test pads: "The bond pad 22A and the test pads 26 may be generally square as illustrated in FIG. 2, or may have other shapes known in the art (e.g., other polygonal or elliptical shapes)." Ex. 1005-7, 4:6-8. Accordingly, it is my opinion that *Mardi* discloses the features of claim 4.

E. Claim 5 — "The interface assembly of claim 1 further comprising a first metal redistribution layer electrically connected to said bonding and test pads, and being co-planar with one another."

69. *Mardi* discloses this claim. In my opinion, the **top conductor layer 36** of *Mardi* corresponds to the claimed "first metal redistribution layer."

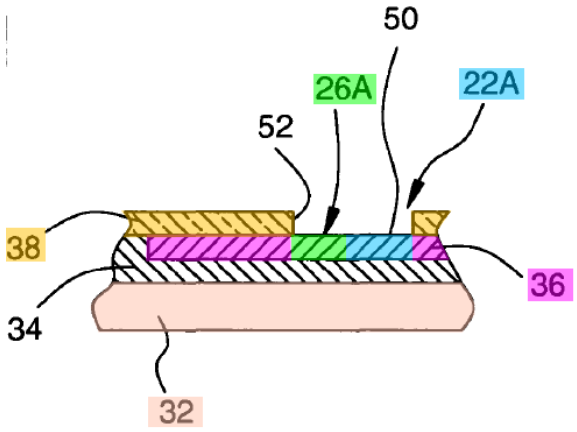


FIG. 5

Ex. 1005-3, Fig. 5. The **test pad 26A** and the **bond pad 22A** are electrically connected to the **top conductor layer 36** because they are a section of that layer. *See* Ex. 1005-8, 5:34-41 ("each of the test/bond pad pairs 24A [*i.e.*, **test pad 26A** and **bond pad 22A]** . . . comprises a section 50 of the **top conductor layer 36"**). As illustrated and described, **top conductor layer 36** is a redistribution layer because it provides electrical communication between the **test pad 26A** and **bond pad 22A** and various semiconductor devices (semiconductor circuits) within the semiconductor. Ex. 1005-7, 4:36-39 (**top conductor layer 36** is "in electrical communication with the various semiconductor devices (semiconductor circuits) within the **semiconductor portion 32**.")

70. As shown in Figure 5, the **top conductor layer 36** extends under the **passivation layer 38** for some distance beyond the **test pad 26A** and **bond pad 22A**, which is typical for a "redistribution layer." The extending "redistribution layer" portion of the **top conductor layer 36** is coplanar with the **test pad 26A** and **bond pad 22A** because all are part of the same "**top conductor layer 36**." Ex. 1005-8, 5:34-36.

71. Further, a conductor layer within the internal conductor portion 34 may also correspond to the "first metal redistribution layer" because "internal conductor portion 34 compris[es] one or more internal conductor layers between the substrate portion 32 and the top conductor layer 36." Ex. 1005-7, 4:39-42. As illustrated in

Figure 5, the uppermost portion of conductor portion 34 is coplanar with the **test pad 26A** and **bond pad 22A**. That portion would be electrically connected to other metal layers using vias: "all of the conductor layers may be separated by respective insulating layers, and may be connected to each other using vias (not shown for simplicity)." Ex. 1005-8, 5:42-45; Ex. 1005-3, Fig. 5.

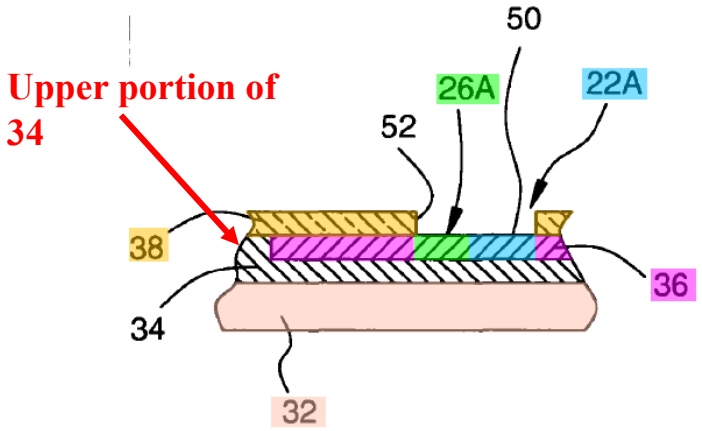


FIG. 5

72. Similarly, all of the test/bond pad pairs 24' (Figure 2) and 24A (Figure 4) are on the same plane because the "the bond pads 22 and the test pads 26 [are] disposed below the level of the die passivation layer 38." Ex. 1005-7, 4:1-5. Thus, other test/bond pad pairs are part of the same "redistribution layer" and are coplanar with the **test pad 26A** and **bond pad 22A**. Accordingly, it is my opinion that *Mardi* discloses the features of claim 5.

F. Claim 6 — "The interface assembly of claim 5 wherein said first metal redistribution layer is electrically connected by way of a via to a second redistribution layer being disposed in a different plane than the first redistribution layer."

73. *Mardi* discloses this claim. *Mardi* expressly discloses vias are used to connect "redistribution layers" at different planes within the semiconductor. As noted above with respect to claim 5, the **top conductor layer 36** and/or the uppermost conductor layer within the internal conductor portion 34 correspond to a "redistribution layer" as claimed. Ex. 1005-8, 4:36-39.

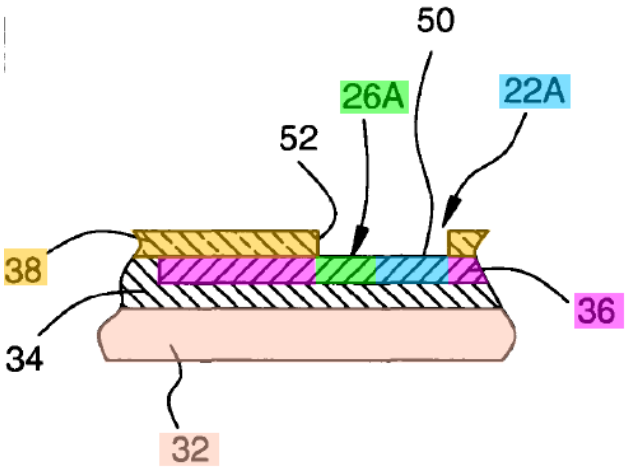


FIG. 5

Ex. 1005-3, Fig. 5.

74. Lower conductor layers in the "internal conductor portion 34" of *Mardi* correspond to the claimed "second redistribution layer" because portion 34 includes "one or more internal conductor layers between the **substrate portion 32** and the **top conductor layer 36**" (Ex. 1005-7, 4:39-42) and it "may be in electrical

communication with the **top conductor layer 36** and the semiconductor devices/circuits within the **semiconductor portion 32**." Ex. 1005-7, 4:45-48.

75. *Mardi* teaches these "redistribution layers" may be connected by vias: "all of the conductor layers may be separated by respective insulating layers, and may be connected to each other using vias (not shown for simplicity)." Ex. 1005-7, 4:42-45. Because *Mardi* discloses there are insulating layers separating all of the conductor layers (including **top conductor layer 36** and any conductor layer(s) inside internal conductor portion 34), *Mardi* expressly discloses the conductor layers are disposed in different planes. Thus, *Mardi* expressly discloses "redistribution layers" at different planes are electrically connected by way of a via. Accordingly, it is my opinion that *Mardi* discloses the features of claim 6.

G. Claim 7 — "The interface assembly of claim 1 wherein the region to be bumped is defined by a first opening in a passivation layer."

76. *Mardi* discloses this claim. In the First *Mardi* Embodiment, the "**opening 42**" is the claimed "first opening":

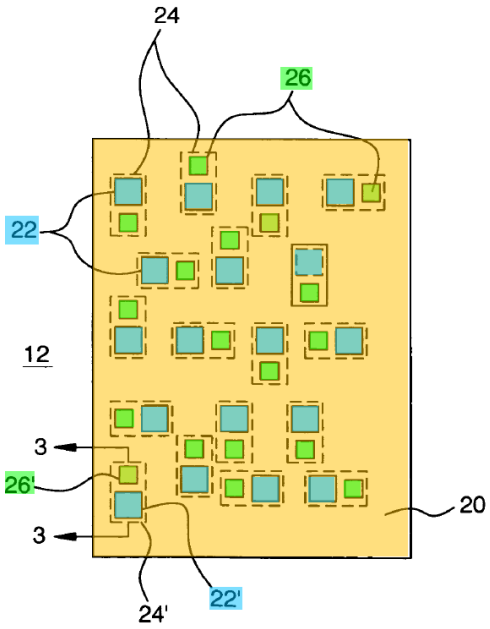


FIG. 2

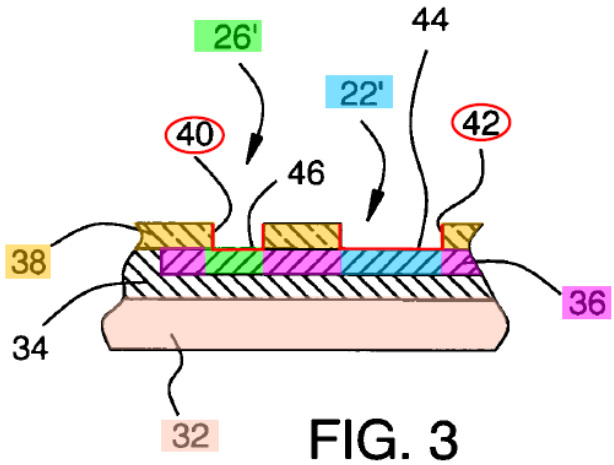


FIG. 3

Ex. 1005-2 to -3, Figs. 2-3. "The **passivation layer 38** is formed over the top conductor layer 36. Each of the **bond pads 22** is located in an **opening 42** of the **passivation layer 38** and comprises a portion 44 of the top conductor layer 36." Ex. 1005-7, 4:58-63.

77. The **bond pad 22** is defined by the **opening 42** in the **passivation layer 38** as claimed because the bond pad is the region to be bumped. Ex. 1005-8, 5:5-7 ("The bond pads 22 are adapted to support bumped contacts (e.g., solder balls) for providing external electrical connections for the semiconductor die 12.")

78. In the Second *Mardi* Embodiment, the "**opening 52**" is the claimed "first opening":

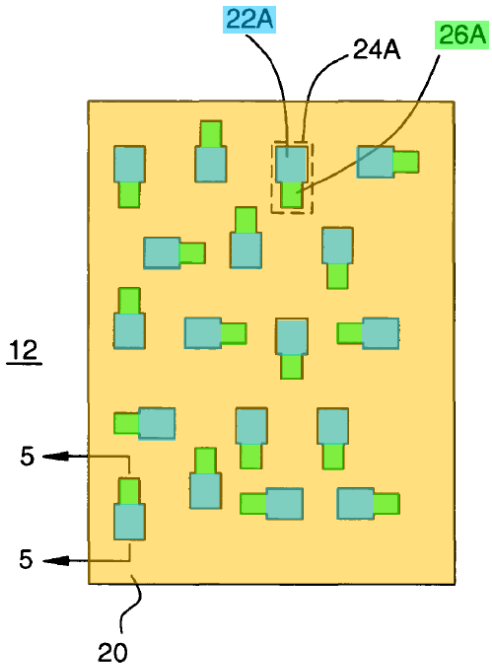


FIG. 4

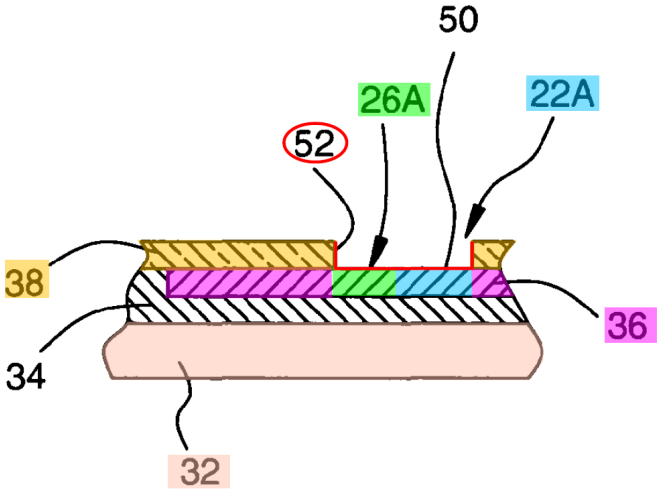


FIG. 5

Ex. 1005-3, Figs. 4-5. "[E]ach of the test/bond pad pairs 24A is located in an **opening 52** of the **passivation layer 38** and comprises a section 50 of the top conductor layer 36. A first portion of the section 50 defines the **bond pad 22A**, and a second portion of the section 50 defines the **test pad 26A**." Ex. 1005-8, 5:34-38.

79. The **bond pad 22A** is defined by the **opening 52** in the passivation layer 38 as claimed because the bond pad is the region to be bumped. Ex. 1005-8, 5:5-7 ("The bond pads 22 are adapted to support bumped contacts (e.g., solder balls) for providing external electrical connections for the semiconductor die 12.")

80. Accordingly, it is my opinion that *Mardi* discloses the features of claim 7.

H. Claim 8 — "The interface assembly of claim 7 wherein the probe region is defined by a second opening in said passivation layer, said first and second openings being spaced apart from one another."

81. *Mardi* discloses this claim. In the First *Mardi* Embodiment, the "**opening 40**" corresponds to the claimed "second opening":

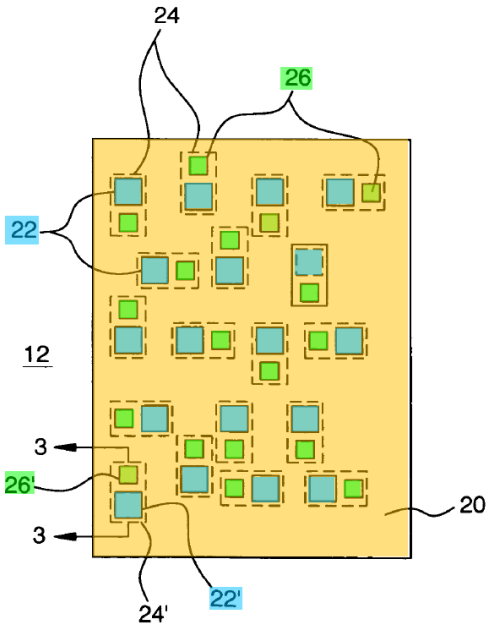


FIG. 2

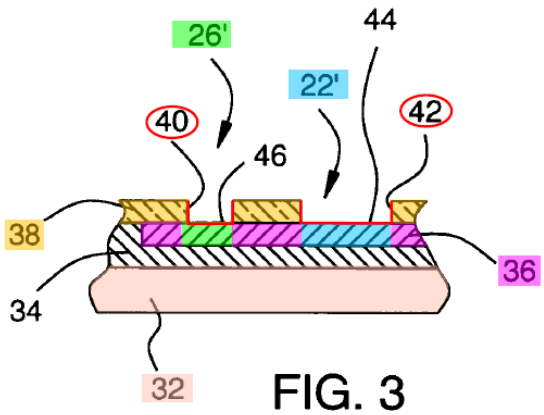


FIG. 3

Ex. 1005-2, Figs. 2-3. "The **passivation layer 38** is formed over the top conductor layer 36. Each of the **bond pads 22** is located in an **opening 42** of the **passivation layer 38** and comprises a portion 44 of the top conductor layer 36. Each of the **test pads 26** is located in an **opening 40** of the **passivation layer 38** and comprises a portion 46 of the top conductor layer 36." Ex. 1005-7, 4:58-63.

82. Thus, in the **passivation layer 38**, the **bond pad 22'** is defined by the **opening 42** and the **test pad 26'** is defined by the **opening 40**, as claimed because

the test pad is used as a probe region. Ex. 1005-9, 7:10-13 ("Notably, a probe element 702 is in contact with the portion 46 of the **top metal layer 36** defining the **test pad 26'**. The probe element 702 does not contact the portion 44 of the **top metal layer 36** defining the **bond pad 22'**.") Accordingly, it is my opinion that *Mardi* discloses the features of claim 8.

I. Independent Claim 9

1. Element 9[preamble] — "method for testing a semiconductor wafer prior to performing a flip chip bumping process"

83. To the extent the preamble is limiting, *Mardi* discloses this element.

84. *Mardi* discloses a method for testing a wafer prior to performing a flip chip bumping process so as not to damage the bond pad: "Fig. 6 is a flow diagram depicting … a process for fabricating an integrated circuit including a semiconductor component testing process …." Ex. 1005-6, 2:66-3:2.

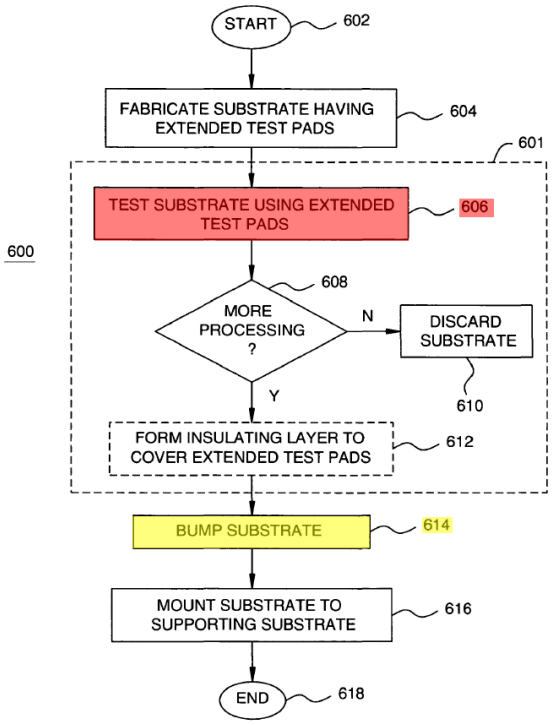


FIG. 6

Ex. 1005-4, Fig. 6. Testing occurs at step 606, and a flip chip bumping process occurs later at step 614. Ex. 1005-9, 7:24-36 ("damage to the bond pad 22A is avoided during the testing at step 606"); Ex. 1005-8, 6:51-55 ("At step 614, the semiconductor substrate is bumped. That is, bumped contacts (e.g., solder balls) are formed on the substrate in electrical communication with the bump pads using a conventional bumping process."); Ex. 1005-9, 7:24-36 ("Notably, a probe element 902 is in contact with the portion of the conductor section 50 that defines the test pad 26A. The probe element 902 does not contact the portion of the conductor section 50 that defines the bond pad 22A. Thus, damage to the bond pad 22A is avoided during the testing at step 606."); Ex. 1005-8, 6:21-23 ("In this manner, the

die or dice of the substrate may be tested or 'burned-in' before further processing (e.g., bumping, packaging, etc.)."). Thus, the Figure 6 flow chart in *Mardi* shows a method where the wafer is tested at step 606 prior to performing a flip chip bumping process at step 614.

2. Element 9[a] — "providing a flip chip bonding pad having a region for performing said bumping process"

85. *Mardi* discloses this element. In particular, *Mardi* discloses "a flip chip bonding pad having a region for performing said bumping process" as shown for element 1[a] above. To the extent the method claim step of "providing" this structural feature requires additional disclosure, *Mardi* discloses "providing" such a structure via fabrication in step 604 of the Figure 6 method: "The semiconductor substrate 10 fabricated at step 604 is then tested in accordance with the test process 601." Ex. 1005-8, 6:10-12.

3. Element 9[b] — "integrally constructing a test pad with said bonding pad to form an integral conductive structure such that separate interconnect testing lines from said test pad to said bonding pad are not present in said integral structure"

86. *Mardi* discloses this element as shown for element 1[b] above. To the extent the method claim step of "integrally constructing" this structural feature requires additional disclosure, *Mardi* discloses "integrally constructing" such a structure via fabrication in step 604 of the Figure 6 method: "The semiconductor

substrate 10 fabricated at step 604 is then tested in accordance with the test process 601." Ex. 1005-8, 6:10-12.

4. Element 9[c] — "disposing said test pad coplanar with said flip chip bonding pad"

87. *Mardi* discloses this element as shown for element 1[c] above. To the extent the method claim step of "disposing" this structural feature requires additional disclosure, *Mardi* discloses "disposing" such a structure via fabrication in step 604 of the Figure 6 method: "The semiconductor substrate 10 fabricated at step 604 is then tested in accordance with the test process 601." Ex. 1005-8, 6:10-12.

5. Element 9[d] — "said test pad including a probe region for performing a wafer test prior to performing said bumping process"

88. *Mardi* discloses this element as shown for element 1[d] above. To the extent the method claim step of "disposing" this structural feature requires additional disclosure, *Mardi* discloses "disposing" such a structure via fabrication in step 604 of the Figure 6 method: "The semiconductor substrate 10 fabricated at step 604 is then tested in accordance with the test process 601." Ex. 1005-8, 6:10-12.

J. Independent Claim 10

1. Element 10[preamble] — "an interface assembly for a semiconductor wafer"

89. *Mardi* teaches this element as shown for element 1[preamble] above.

2. Element 10[a] — "a flip chip bonding pad including a region for performing a bumping process"

90. *Mardi* teaches this element as shown for element 1[a] above.

3. Element 10[b] — "a test pad integrally constructed with said bonding pad"

91. *Mardi* teaches this element as shown for element 1[b] above.

4. Element 10[c] — "said test pad being coplanar relative to said flip chip bonding pad"

92. *Mardi* teaches this element as shown for element 1[c] above.

5. Element 10[d] — "said test pad . . . including a probe region for performing wafer-level testing prior to performing said bumping process"

93. *Mardi* teaches this element as shown for element 1[d] above.

6. Element 10[e] — "a first metal redistribution layer electrically connected to said bonding and test pads, and being co-planar with one another"

94. *Mardi* teaches this element as shown for claim 5 above.

7. Element 10[f] — "said first metal redistribution layer is electrically connected by way of a via to a second redistribution layer being disposed in a different plane than the first redistribution layer"

95. *Mardi* teaches this element as shown for claim 6 above.

XI. GROUND 2: CLAIMS 1-10 ARE OBVIOUS OVER *MARDI* IN VEIW OF A POSITA'S KNOWLEDGE

96. As addressed in Ground 1, *Mardi* fully discloses all elements of claims 1-10. Alternatively, it would have been obvious to a POSITA to modify *Mardi* in view of the POSITA's knowledge to achieve the features of claims 1-10.

A. Independent Claim 1 (and all dependent claims) — "wafer-level testing"

97. As discussed for claim 1, *supra*, with reference to Figures 6 and 9, *Mardi* discloses "performing wafer-level testing prior to performing said bumping process." Ex. 1001-5, 4:6-8. First, Figure 9 illustrates testing with a **probe element 902**.

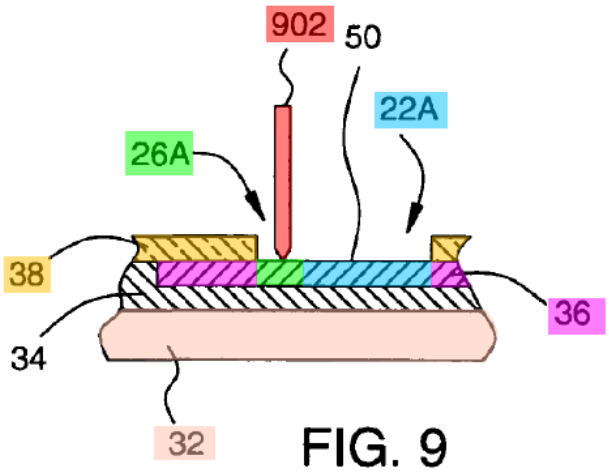


FIG. 9

Ex. 1005-5, Fig. 9. Second, Figure 6 shows testing ***before*** the bumping process. Ex. 1005-8, 5:54-56.

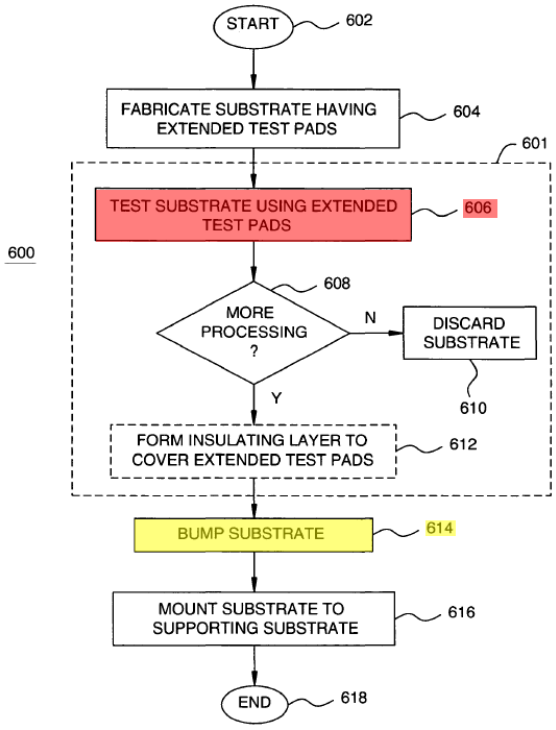


FIG. 6

Ex. 1005-4, Fig. 6.

98. Further, *Mardi* confirms Figures 6 and 9 show "wafer-level testing." In particular, *Mardi* says "the term 'semiconductor component' is meant to encompass a substrate having multiple semiconductor dice" (Ex. 1005-7, 3:30-32), as shown in Figure 1.

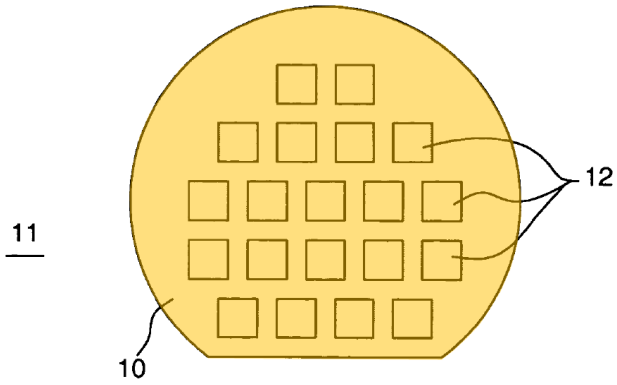


FIG. 1

Ex. 1005-2, Fig. 1.

99. A POSITA understands a "substrate having multiple semiconductor dice" is a wafer. Relative to Figure 6, *Mardi* says "the process 600 is described with respect to a semiconductor component comprising a substrate with a plurality of semiconductor dice," *i.e.*, a wafer. Ex. 1005-8, 5:65-67. *Mardi* teaches process 600 relates to a wafer that is singulated or diced at the mounting step 616. Ex. 1005-9, 7:1-2 ("If the substrate includes multiple dice, the dice are singulated (i.e., diced) before mounting.") Thus, it is my opinion *Mardi* teaches "wafer-level testing."

100. Alternatively, a POSITA would have found it obvious to use *Mardi's* process for "wafer-level testing" because POSITAs knew that wafer-level testing (as opposed to testing one chip at a time) reduces manufacturing costs and manufacturing time. U.S. Patent No. 5,550,480 to *Nelson* et al. was filed in 1994 (over 10 years before the '173 patent), and shows that a POSITA would have knowledge of the benefits of testing semiconductor devices at the wafer level:

> Generally, integrated devices are fabricated in a thin flat substrate material commonly referred to as a semiconductor wafer. After fabrication, the integrated devices in the semiconductor wafer are tested, the semiconductor wafer is separated or divided into individual semiconductor chips or die, and each chip is encapsulated in a package. Since each semiconductor chip typically contains a large number of integrated devices, there is a probability of producing one or more defective integrated devices. Therefore, it is desirable to test the

> integrated devices prior to packaging them to ensure that time, money, and manufacturing capacity are not wasted by packaging defective semiconductor chips. Moreover, testing semiconductor chips in wafer form is easier and more cost efficient than testing a single semiconductor chip that has been separated from the semiconductor wafer. ***In other words, wafer-level testing or probing, i.e., testing semiconductor chips before the semiconductor wafer is separated into individual chips, reduces the manufacturing costs and cycle times associated with manufacturing semiconductor products***.

Ex. 1010-7, 1:13-33.

101. A POSITA would have knowledge of the benefits of testing semiconductor devices at the wafer level. *See* Ex. 1011-1, [57]; Ex. 1011-9, 1:23-49 ("wafer level testing" of wafer comprising flip-chip type semiconductor chips) (2004); Ex. 1012-19, 1:18-27; Ex. 1012-21, 6:42-46 (wafer-level testing of flip chips) (2003); Ex. 1004-1, [57] (same) (2005).

102. It is my opinion all of these references show a POSITA knew wafer-level testing of flip-chips reduces manufacturing costs and cycle times. A POSITA would have used the *Mardi* testing method to test flip-chips at the wafer-level. Thus, "wafer-level testing" as claimed in claim 1 (and claims 2-7 that depend from claim 1) would have been obvious to a POSITA.

a. Claim 5 — "The interface assembly of claim 1 further comprising a first metal redistribution layer electrically connected to said bonding and test pads, and being co-planar with one another."

103. As discussed for claim 5 in Ground 1, *Mardi* expressly discloses claim 5. Alternatively, it would have been obvious to modify *Mardi* to include a first metal redistribution layer electrically connected to said bonding and test pads, and being co-planar with one another. A POSITA knows that **top conductor layer 36** is a metal layer, and this layer can include conductive routing interconnect in addition to the conductive metal that makes up **test pad 26A** and **bond pad 22A**. A POSITA knows this because metal layers are typically fabricated as solid metal layers which are then patterned to remove portions of the metal and leave behind structures such as routing interconnect (*e.g.*, traces) and test/bond pads.

104. This knowledge is evidenced by patent references that predate the '173 patent's September 29, 2004 filing date, such as *Yong* (published September 18, 2003) (Ex. 1007-1); U.S Patent No. 6,392,301 to Waizman (issued May 21, 2002) ("*Waizman*") (Ex. 1013); and U.S. Patent Application Publication 2005/0037601 to Hsu (filed October 27, 2003) ("*Hsu*") (Ex. 1014). For example, as discussed in Ground 5, *infra*, *Yong* discloses pad 10 (which has probe region 14 and wire bond region 12) as part of the upper conductive metal layer 28:

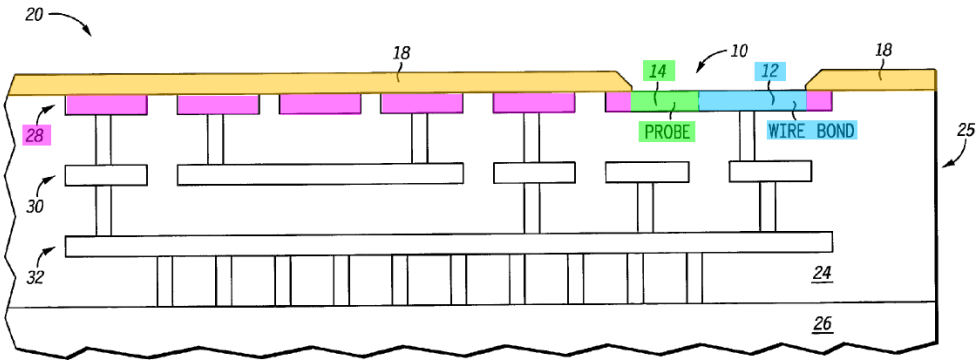


FIG.2

Ex. 1007-2, Fig. 2. Pad 10 is coplanar with, and electrically connected to, other routing interconnect traces that are part of upper conductive layer 28. Ex. 1007-10 to -11, [0013]-[0015].

105. Similarly, *Waizman* discloses metal routing/trace layer 220, which is coplanar with pads 205, 207, 209, and 211 (Ex. 1013-8, 3:1-4:12):

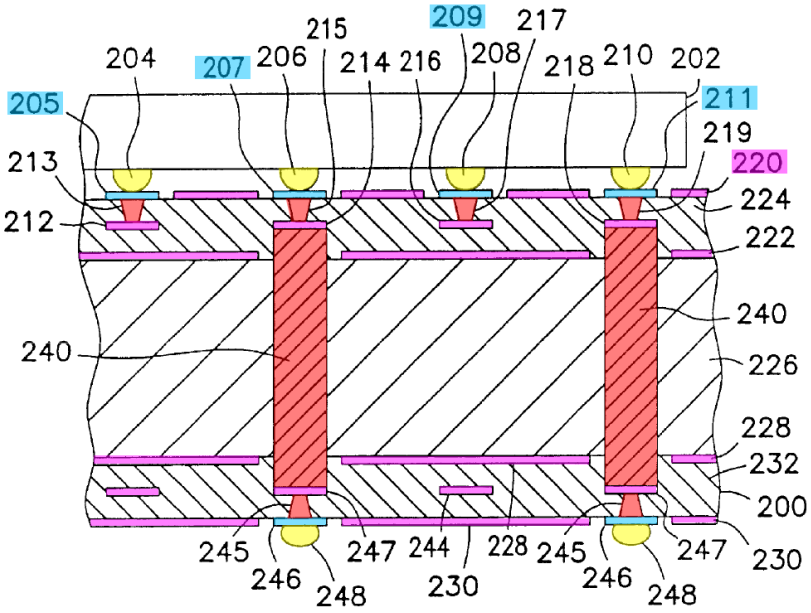


FIG. 2A

Ex. 1013-3, Fig. 2a. And *Hsu* discloses "patterned trace layer 33" which is coplanar with "a plurality of contact pads 330" (Ex. 1014-14, [0046]):

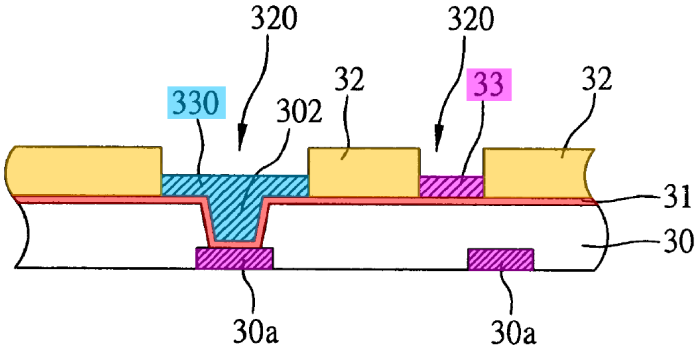


FIG. 3C

Ex. 1014-7, Fig. 3C.

106. *Yong*, *Waizman*, and *Hsu* show that it was common—and a POSITA would have known—to include a redistribution layer for interconnect routing on the same metal layer that is used to form the bond/test pads. A POSITA would know that such interconnect would be electrically connected to one or more bonding/test pads in order to route the signals connected to those pads to "the semiconductor devices/circuits within the semiconductor portion 32" of *Mardi*. Ex. 1005-7, 4:45-48. Thus, it would have been obvious to modify *Mardi* to include a first metal redistribution layer electrically connected to said bonding and test pads, and being co-planar with one another.

B. Claim 6 — "The interface assembly of claim 5 wherein said first metal redistribution layer is electrically connected by way of a via to a second redistribution layer being disposed in a different plane than the first redistribution layer."

107. As discussed for claim 6 in Ground 1, *Mardi* expressly discloses vias are used to connect "redistribution layers" at different planes within the semiconductor. As noted above with respect to claim 5, top conductor layer 36 and/or the uppermost conductor layer within the internal conductor portion 34 correspond to a "first metal redistribution layer" (Ex. 1005-7, 4:36-39; Ex. 1005-3, Fig. 5), and at least one of the conductor layers within the internal conductor portion 34 corresponds to the claimed "second redistribution layer":

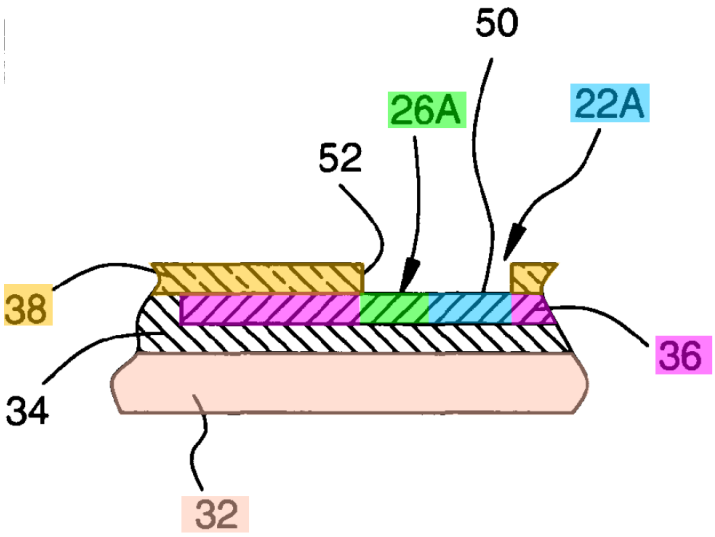


FIG. 5

Ex. 1005-3, Fig. 5; Ex. 1005-7, 4:39-42 ("[I]nternal conductor portion 34 compris[es] one or more internal conductor layers between the substrate portion 32 and the top conductor layer 36.") *Mardi* teaches these "redistribution layers" are

separated by insulating layers and connected by vias: "all of the conductor layers may be separated by respective insulating layers, and may be connected to each other using vias (not shown for simplicity)." Ex. 1005-7, 4:42-45.

108. However, Figure 5 of *Mardi* does not expressly show insulating layers between the redistribution layers and it does not expressly show the vias connecting the redistribution layers. These features are described in the text. Alternatively, these features would be obvious based on a POSITA's knowledge. A POSITA was familiar with both insulation layers and vias. *Id. Mardi* says these features are "not shown for simplicity" (Ex. 1005-7, 4:42-45), and a POSITA would agree it is not necessary for these features to be illustrated.

109. Modified Figure 5 below shows the POSITA's understanding of *Mardi* based on its disclosure that the redistribution layers are separated by an insulating layer and connected by vias:

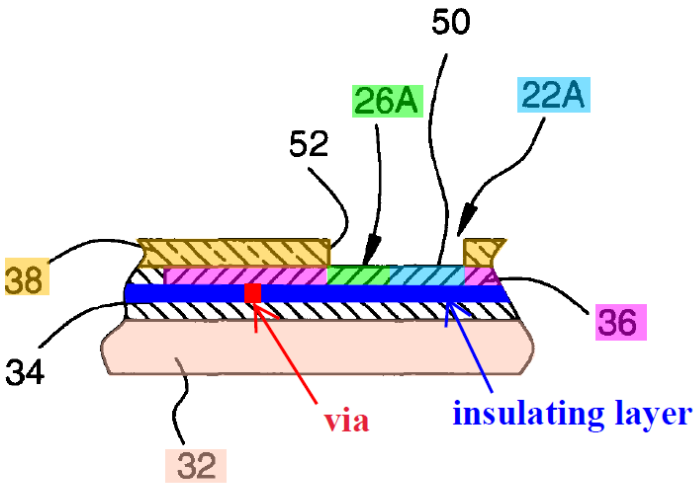


FIG. 5

Ex. 1005-3, Fig. 5 (modified) (showing case where conductor portion 34 has only one internal insulating layer).

110. If not expressly disclosed, the limitations of claim 6 would have been obvious to a POSITA in view of *Mardi* and the POSITA's knowledge.

C. Independent Claim 9 — "wafer test"

111. It is my opinion that *Mardi* teaches "wafer test" as explained above for the "wafer-level testing" of claim 1.

D. Independent Claim 10 — "performing wafer-level testing"

112. It is my opinion that *Mardi* teaches "performing wafer-level testing" as explained above for claim 1.

XII. GROUND 3: CLAIMS 1-4, 7 AND 9 ARE ANTICIPATED BY *LIN*

A. Independent Claim 1

1. Element 1[preamble] — "an interface assembly for a semiconductor wafer"

113. To the extent the preamble is limiting, it is disclosed by *Lin*.

114. *Lin* expressly discloses bonding pad 46 as "an interface assembly for a semiconductor wafer" because it provides an interface for testing the wafer with a probe needle:

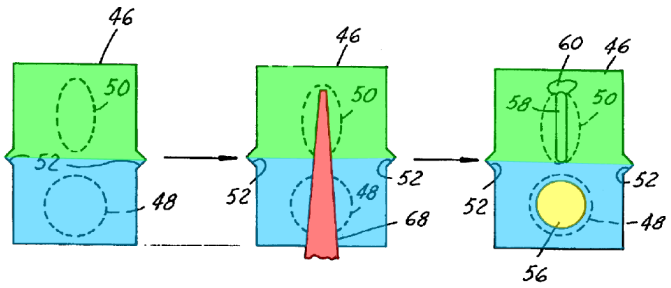


FIG. 8

Ex. 1006-3, Fig. 8. "As shown in FIG. 8, during the parametric testing procedure, the tip of each **probe needle 68** contacts the **probe needle contact area 50** of the corresponding bonding pad 44 [Fig. 6] and forms a scrub mark 58 and a hump 60 of pad material in the bonding pad 46 [Fig. 8]…." Ex. 1006-6, 5:30-35.

115. *Lin* expressly discloses this testing method is for a semiconductor wafer: "a method which enhances wafer sort yield…." Ex. 1006-4, 2:61-62. Accordingly, it is my opinion that *Lin* discloses the features of element 1[preamble].

2. Element 1[a] — "a flip chip bonding pad including a region for performing a bumping process; and"

116. In my opinion, the bottom half of "bonding pad 46" (shaded in blue below and including "wire bonding area 48") corresponds to the claimed "flip chip bonding pad." First, marks 52 in Figure 5 delineate the boundaries between **wire bonding area 48** and the **probe contact area 50** of bonding pad 46:

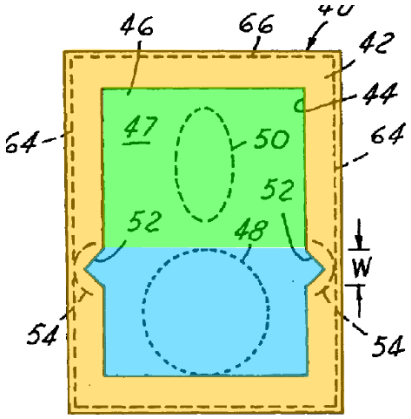


FIG. 5

Ex. 1006-2, Fig. 5; Ex. 1006-6, 5:1-4 ("[M]arks 52 delineate the boundary between wire bonding area 48 and probe contact area 50.")

117. Second, the "bonding pad 46" is for flip chips: "The bonding pad of the present invention is suitable for wire bonding techniques … ***and flip-chip packaging techniques***." Ex. 1006-5, 4:24-26. *Lin* discloses the **wire bonding area 48** is where the solder bump or bond wire contact is formed on bonding pad 46. Ex. 1006-6, 5:40-43 ("Finally, the bonding ball 56 or other electrical contact is formed on the **wire bonding area 48** of the bonding pad 46 for electrical contact with a bonding wire ….")

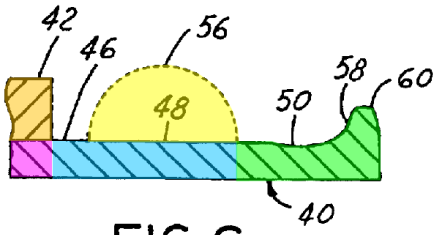


FIG. 6

Ex. 1006-3, Fig. 6. Thus, *Lin* teaches a flip chip bonding pad with a region for performing a bumping process because the **wire bonding area 48** would be bumped with a solder bump when the bonding pad is used with flip-chip packaging techniques. Ex. 1006-5, 3:52-54 ("FIG. 1A is a top view of ... a chip surface prior to bonding of a wire **or solder bump** to the bonding pad"); Ex. 1006-5, 3:1-28 (embodiments of the present invention include "bonding of a **solder bump** or bond wire to the bonding pad"). Accordingly, it is my opinion that *Lin* discloses the features of claim element 1[a].

3. Element 1[b] — "a test pad integrally constructed with said bonding pad that form an integral conductive structure such that separate interconnect testing lines from said test pad to said bonding pad are not present in said integral structure"

118. *Lin* discloses this element. In my opinion, the **probe needle contact area 50** and the **wire bonding area 48** of *Lin* are integrally constructed without interconnect testing lines, as claimed. The upper half of "bonding pad 46" (shaded in green below and including "**probe needle contact area 50**") corresponds to the claimed "test pad" because that is the area where a test probe contacts the pad during testing: "As shown in FIG. 8, during the parametric testing procedure, the tip of each probe needle 68 contacts the **probe needle contact area 50** of the corresponding bonding pad 44 [sic] and forms a scrub mark 58 and a hump 60 of pad material in the bonding pad 46…." Ex. 1006-6, 5:30-35.

119. The "test pad" (**green area**) and the "bonding pad" (**blue area**) are integrally constructed without interconnect testing lines.

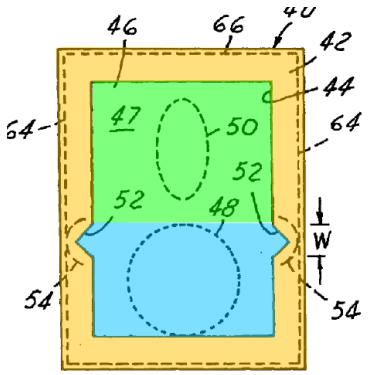


FIG. 5

Ex. 1006-2, Fig. 5. There are no interconnect lines because the two areas are simply different regions of the same bonding pad: "Accordingly, the **wire bonding area 48** and the **probe needle contact area 50** are located in separate, non overlapping areas on the surface 47 of the bonding pad 46." Ex. 1006-5, 4:61-63.

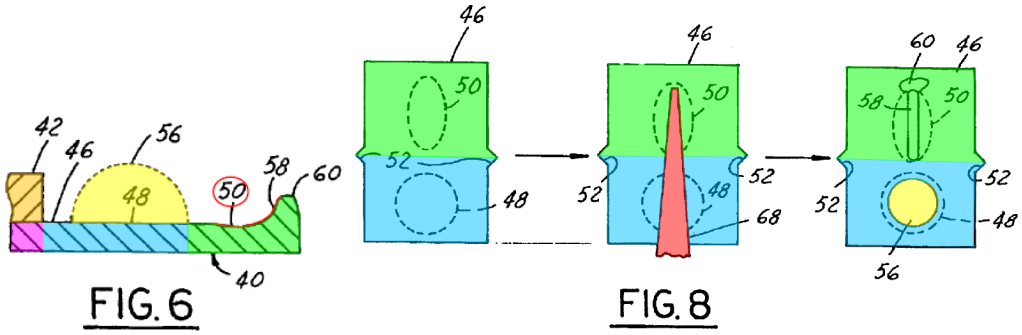
120. Finally, the bonding pad 46, which includes the "test pad" (**green area**) and the "bonding pad" (**blue area**), is a conductive structure: "Each bonding pad 46 may be constructed of aluminum or other suitable electrically-conductive material." Ex. 1006-5, 4:51-53. *Lin* teaches a test pad integrally constructed with the bonding pad with no interconnect testing lines. The claimed "test pad" (upper half of "bonding pad 46" shaded in green) and claimed "bonding pad" (lower half of "bonding pad 46" shaded in blue) are different regions of the same integral conductive structure. Accordingly, it is my opinion that *Lin* discloses the features of claim element 1[b].

4. Element 1[c] — "said test pad being coplanar relative to said flip chip bonding pad"

121. *Lin* discloses this element. The "test pad" (**green area**) and the "bonding pad" (**blue area**) are coplanar because they are simply separate areas of the metal bonding pad 46: "[T]he **wire bonding area 48** and the **probe needle contact area 50** are located in separate, non overlapping areas on the surface 47 of the bonding pad 46." Ex. 1006-5, 4:56-63; Ex. 1006-2, Fig. 5. Accordingly, it is my opinion that *Lin* discloses the features of claim element 1[c].

5. Element 1[d] — "said test pad . . . including a probe region for performing wafer-level testing prior to performing said bumping process"

122. *Lin* discloses this element. In my opinion, the **probe needle contact area 50** corresponds to the "probe region for performing wafer-level testing" because, "during the parametric testing procedure, the tip of each **probe needle 68** contacts the **probe needle contact area 50** of the corresponding bonding pad [46] [Fig. 6] and forms a scrub mark 58 and a hump 60 of pad material in the bonding pad 46 [Fig. 8], as further shown in FIGS. 6 and 8." Ex. 1006-6, 5:31-35.



Ex. 1006-3, Figs. 6 and 8.

123. *Lin* discloses the parametric testing occurs prior to performing a bumping process: "Prior to packaging and formation of the bonding balls 10 on the respective bonding pads 14, the chip 26 is subject to parametric testing…." Ex. 1006-4, 2:25-27.

124. Further, this testing is for a semiconductor wafer: "a method which enhances ***wafer*** sort yield…." Ex. 1006-4, 2:61-62. The wire bonding area 48 is bumped with a solder ball (*i.e.*, a "bumping process") when the bonding pad is used with flip-chip packaging techniques. Ex. 1006-5, 4:24-26 ("[t]he bonding pad of the present invention is suitable for wire bonding techniques, as well as ball grid array (BGA) and flip-chip packaging techniques.") Ex. 1006-5, 3:52-54 ("FIG. 1A is a top view of ... a chip surface prior to bonding of a wire **or solder bump** to the bonding pad.") Ex. 1006-5, 3:1-28 (embodiments of the present invention include "bonding of a **solder bump** or bond wire to the bonding pad.")

125. Accordingly, it is my opinion that *Lin* discloses the features of claim element 1[d].

B. Claim 2 — "The interface assembly of claim 1 wherein said test pad may be disposed anywhere along a periphery of said bonding pad."

126. *Lin* discloses this claim. In my opinion, *Lin* teaches the test pad (**green area**) may be anywhere at the periphery of the bonding pad (**blue area**) because they are merely regions of the same bonding pad 46 separated by marks 52 on two

opposite sides: "[M]arks 52 delineate the boundary between wire bonding area 48 and probe contact area 50." Ex. 1006-6, 5:1-4.

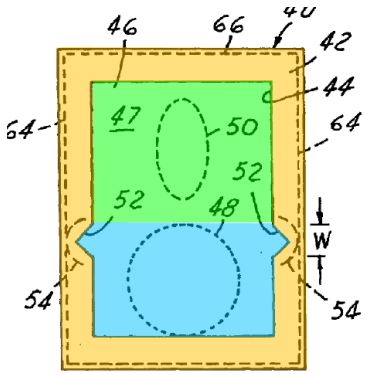


FIG. 5

Ex. 1006-2, Fig. 5.

127. "The bonding pads 46 may be arranged in any desired alternative configuration on the chip 40 consistent with the particular use requirements of the chip 40." Ex. 1006-5, 4:40-43. Thus, *Lin* teaches the test pad (**green area**) may be anywhere along periphery of the bonding pad (**blue area**). *See also*, Ex. 1006-5, 4:56-63 ("As further shown in FIG. 5, a **wire bonding area 48** is located on the surface 47 of each bonding pad 46, adjacent to one of the transverse edges 66 thereof, and a **probe needle contact area 50** is also located on the surface 47 of the bonding pad 46, adjacent to the opposite transverse edge 66 thereof. Accordingly, the **wire bonding area 48** and the **probe needle contact area 50** are located in separate, non overlapping areas on the surface 47 of the bonding pad 46.") Accordingly, it is my opinion that *Lin* discloses the features of claim 2.

C. Claim 3 — "The interface assembly of claim 1 wherein said bonding pad comprises a shape selected from the group consisting of a polygonal shape, and a circular shape."

128. *Lin* discloses this claim. *Lin* teaches a rectangular-shaped ("polygonal") bonding pad.

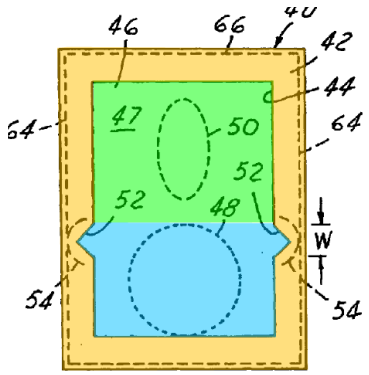


FIG. 5

Ex. 1006-2, Fig. 5. "As shown in FIG. 5, each bonding pad 46 typically has a generally elongated, ***rectangular shape***, having longitudinal edges 64 and transverse edges 66 that may be overlapped by the passivation layer 42." Ex. 1006-5, 4:43-51. Additionally, marks 52 delineate the boundary between wire bonding area 48 and probe contact area 50: "The notch mark or marks 52 serve to clearly indicate the locations of the **wire bonding area 48** and the **probe needle contact area 50** on the bonding pad 46." Ex. 1006-6, 5:1-4. Both the bonding pad (**blue area** including **wire bonding area 48**) and the test pad (**green area** including **probe needle contact area 50**) are rectangular-shaped polygons. Even if the notch marks 52 are considered part of the shape, the pad is polygonal. Accordingly, it is my opinion that *Lin* discloses the features of claim 3.

D. Claim 4 — "The interface assembly of claim 1 wherein said test pad comprises a shape selected from the group consisting of a polygonal shape, and a circular shape."

129. *Lin* discloses this claim. *Lin* teaches the test pad is a rectangular-shaped polygon for the same reasons as explained relative to claim 3 above. Accordingly, it is my opinion that *Lin* discloses the features of claim 4.

E. Claim 7 — "The interface assembly of claim 1 wherein the region to be bumped is defined by a first opening in a passivation layer."

130. *Lin* discloses this claim. In my opinion, the "first opening" is "**pad opening 44**" in *Lin*, which is an opening in **passivation layer 42**: "A rectangular **pad opening 44** extends through the **passivation layer 42** to expose the upper surface of the bonding pad 46." Ex. 1006-5, 4:53-55. As discussed with respect to element 1[a], the **wire bonding area 48** corresponds to the "region to be bumped." As shown in Figure 5, **wire bonding area 48** is defined by the first opening even if it is just a portion of the surface within that opening.

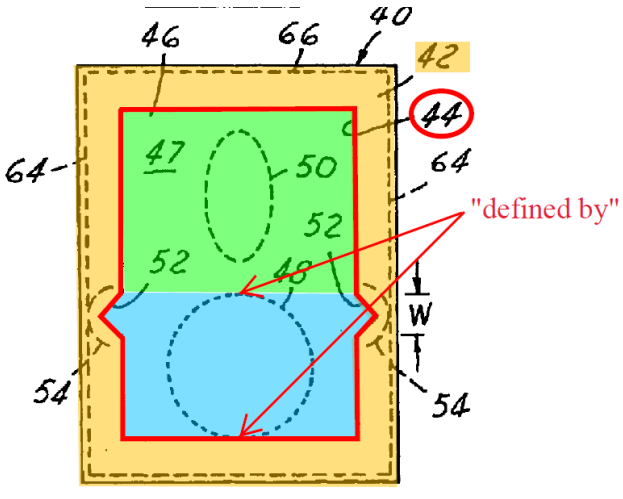


FIG. 5

Ex. 1006-2, Fig. 5. Indeed, notches 52 in the passivation layer further define opening 44 and delineate the boundary between **wire bonding area 48** (the region to be bumped) and **probe needle contact area 50**: "The notch mark or marks 52 serve to clearly indicate the locations of the **wire bonding area 48** and the **probe needle contact area 50** on the bonding pad 46." Ex. 1006-6, 5:1-4. Thus, the **wire bonding area 48** (*e.g.*, the "region to be bumped") is defined by the **pad opening 44**, as claimed. Accordingly, it is my opinion that *Lin* discloses the features of claim 7.

F. Independent Claim 9

1. Element 9[preamble] — "method for testing a semiconductor wafer prior to performing a flip chip bumping process"

131. To the extent the preamble is limiting, it is disclosed by *Lin*.

132. In my opinion, *Lin* expressly teaches wafer testing prior to a flip chip bump bonding process. Ex. 1006-4, 2:61-62 (patent is directed to wafer-level testing: "a method which enhances wafer sort yield…"); Ex. 1006-4, 1:38-65 (describing "flip-chip" technology); Ex. 1006-5, 4:24-26 (bonding pad suitable for "ball grid array (BGA) and flip-chip packaging techniques"); Ex. 1006-4, 1:6-10 ("the present invention relates to a new and improved bonding pad having separate areas for probe needle contact and wire bonding in semiconductor packaging technology."); Ex. 1006-6, 5:30-35, Fig. 8 ("As shown in FIG. 8, during the parametric testing procedure, the tip of each **probe needle 68** contacts the **probe needle contact area**

50 of the corresponding bonding pad 44 and forms a scrub mark 58 and a hump 60 of pad material in the bonding pad 46, as further shown in FIGS. 6 and 8."); Ex. 1006-4, 2:25-2 ("Prior to packaging and formation of the bonding balls 10 on the respective bonding pads 14, the chip 26 is subject to parametric testing….")

2. Element 9[a] — "providing a flip chip bonding pad having a region for performing said bumping process"

133. *Lin* discloses this element. In my opinion, the "bonding pad 46" of *Lin* corresponds to the claimed "flip chip bonding pad." *Lin* discloses "a flip chip bonding pad having a region for performing said bumping process" as shown for element 1[a] above. To the extent the method claim step of "providing" this structural feature requires additional disclosure, *Lin* discloses "providing" such a structure by fabricating it: "[I]n typical application of the present invention, the chip 40, with the bonding pads 46 of the present invention fabricated thereon, as shown in FIG. 7, is initially subjected to conventional parametric testing…." Ex. 1006-6, 5:18-21. Accordingly, it is my opinion that *Lin* discloses the features of claim element 9[a].

3. Element 9[b] — "integrally constructing a test pad with said bonding pad to form an integral conductive structure such that separate interconnect testing lines from said test pad to said bonding pad are not present in said integral structure"

134. *Lin* discloses this element. In my opinion, *Lin* discloses this element as shown for element 1[b] above. To the extent the method claim step of "integrally

constructing" this structural feature requires additional disclosure, *Lin* discloses "integrally constructing" such a structure by fabricating it: "[I]n typical application of the present invention, the chip 40, with the bonding pads 46 of the present invention fabricated thereon, as shown in FIG. 7, is initially subjected to conventional parametric testing…." Ex. 1006-6, 5:18-21. Accordingly, it is my opinion that *Lin* discloses the features of claim element 9[a].

4. Element 9[c] — "disposing said test pad coplanar with said flip chip bonding pad"

135. *Lin* discloses this element. In my opinion, *Lin* discloses this element as shown for element 1[c] above. To the extent the method claim step of "disposing" this structural feature requires additional disclosure, *Lin* discloses "disposing" such a structure by fabricating it: "[I]n typical application of the present invention, the chip 40, with the bonding pads 46 of the present invention fabricated thereon, as shown in FIG. 7, is initially subjected to conventional parametric testing…." Ex. 1006-6, 5:18-21.

5. Element 9[d] — "said test pad including a probe region for performing a wafer test prior to performing said bumping process"

136. *Lin* discloses this element. In my opinion, *Lin* discloses this element as shown for element 1[d] above. To the extent the method claim step of "disposing" this structural feature requires additional disclosure, *Lin* discloses "disposing" such a structure by fabricating it: "[I]n typical application of the present invention, the

chip 40, with the bonding pads 46 of the present invention fabricated thereon, as shown in FIG. 7, is initially subjected to conventional parametric testing…." Ex. 1006-6, 5:18-21. Accordingly, it is my opinion that *Lin* discloses the features of claim element 9[d].

XIII. GROUND 4: CLAIMS 1-7 AND 9-10 ARE OBVIOUS OVER *LIN* IN VEIW OF POSITA'S KNOWLEDGE

137. As addressed in Ground 3, *Lin* fully discloses all elements of claims 1-4, 7, and 9. To the extent it is argued that *Lin* fails to disclose any element, it would have been obvious to a POSITA to modify *Lin* in view of the POSITA's knowledge to achieve the features of claims 1-4, 7, and 9. In addition, it would be obvious to modify *Lin* in view of the POSITA's knowledge to achieve the features of claims 5-6 and 10.

A. Independent Claim 1 (and all dependent claims) — "performing wafer-level testing"

138. As discussed for claim 1, *supra*, with reference to Figures 6 and 8, *Lin* discloses testing prior to the bumping process. First, testing occurs via "multiple **probe needles 68** (one of which is shown in FIG. 8)."

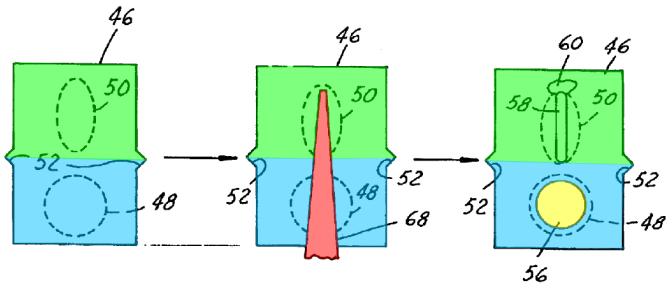


FIG. 8

Ex. 1006-6, 5:28; Ex. 1006-3, Fig. 8. Second, testing occurs prior to performing a bumping process: "**Prior to packaging and formation of the bonding balls** 10 on the respective bonding pads 14, the chip 26 is subjected to parametric testing which utilizes test structures to assess the electrical characteristics and reliability of the devices on the wafer." Ex. 1006-4, 2:25-27.

139. Further, this testing is for a semiconductor wafer: "The chip 40 [FIG. 7] is typically **one of multiple chips** having had integrated circuits (not shown) previously fabricated thereon **on a semiconductor wafer substrate (not shown)**." Ex. 1006-5, 4:29-32 (emphasis added). "Prior to packaging and formation of the bonding balls 10 on the respective bonding pads 14, the chip 26 is subjected to parametric testing which utilizes test structures **to assess the electrical characteristics and reliability of the devices on the wafer**." Ex. 1006-4, 2:25-29 (emphasis added).

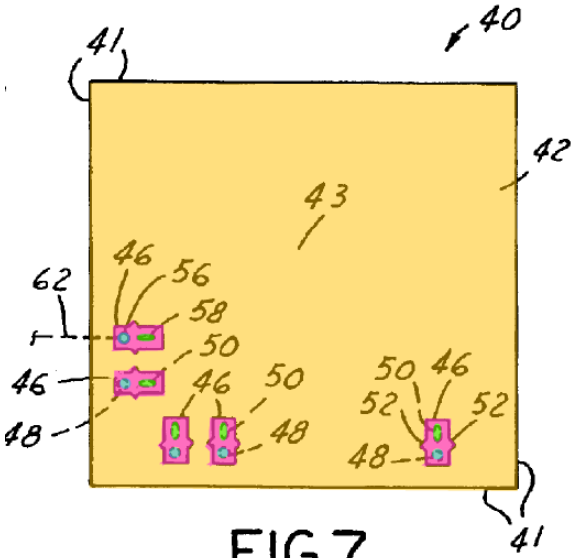


FIG.7

Ex. 1006-3, Fig. 7.

140. A POSITA at the time understood that a semiconductor wafer substrate having multiple chips thereon is a wafer. Further, it is my opinion *Lin* confirms it is performing "wafer-level testing" because the testing "enhances **wafer sort yield**..." Ex. 1006-4, 2:61-62.

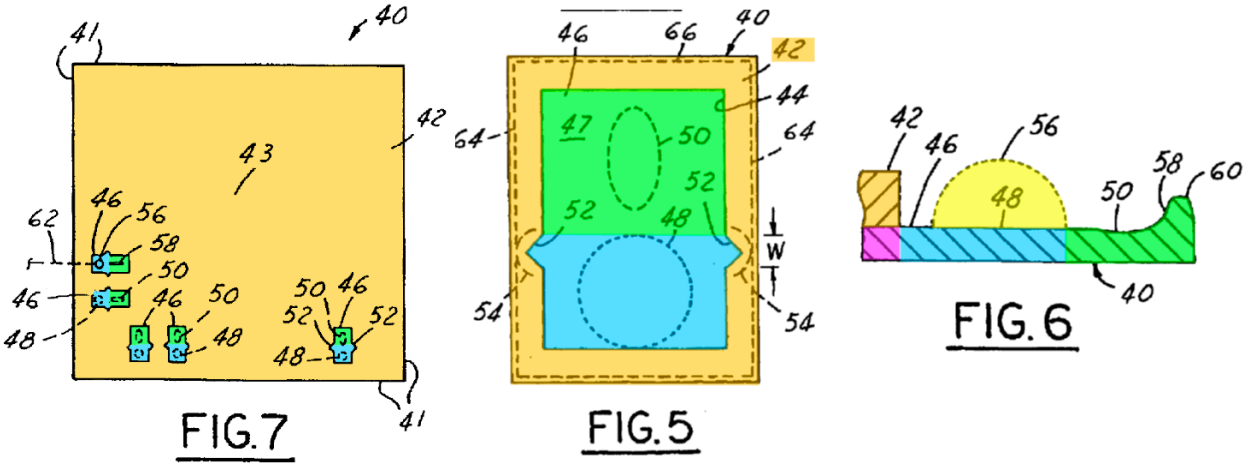
141. Alternatively, a POSITA would have found it obvious to use *Lin's* process for "wafer-level testing" because POSITAs knew that wafer-level testing (as opposed to testing one chip at a time) reduces manufacturing costs and manufacturing time as discussed above for Ground 2 (*see* discussion citing *Nelson*, *Farnworth*, *Eldridge*, and *Yu*).

142. Thus, it is my opinion that "wafer-level testing" as claimed in claim 1 (and claims 2-7 that depend from claim 1) would have been obvious based on *Lin* combined with the POSITA's knowledge.

B. Claim 5 — "The interface assembly of claim 1 further comprising a first metal redistribution layer electrically connected to said bonding and test pads, and being co-planar with one another."

143. *Lin* renders this claim obvious. It is my opinion that the **top conductive layer** in *Lin* corresponds to the "first metal redistribution layer" of claim 5. The **top conductive layer** is immediately under the **passivation layer 42** and comprises: all of the the bonding pads (**blue area** including **wire bonding area 48**), all of the test pads (**green area** including **probe needle contact area 50**), and the remaining

portion of the conductive layer extending under **passivation layer 42** (pink in Figure 6):



Ex. 1006-2 to -3, Figs. 5-7. The **top conductive layer** is formed across the entire surface of the wafer and includes all bond pads 46 as shown in Figure 7. A POSITA understands the **top conductive layer** could include other routing traces under **passivation layer 42** electrically connected to the test/bond pads, as discussed for claim 5 in Ground 2 (discussing knowledge of a POSITA as evidenced by *Yong*, *Waizman*, and *Hsu*). *Lin* explains the bond pad 46 is "embedded in the **passivation layer 42**, in electrical contact with integrated circuits (not shown) formed in the chip 40, typically in conventional fashion." Ex. 1006-5, 4:32-37. This description confirms the **top conductive layer** is "electrically connected to said bonding and test pads," as claimed in claim 5. Further, *Lin* teaches, "[e]ach bonding pad 46 may be constructed of aluminum or other suitable electrically conductive material" (Ex. 1006-5, 4:51-53), which confirms it is "metal," as claimed.

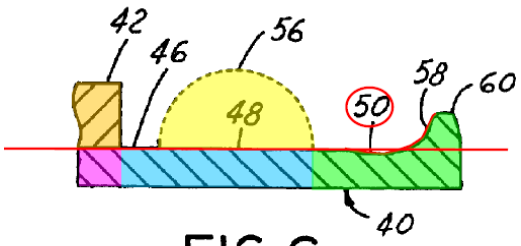
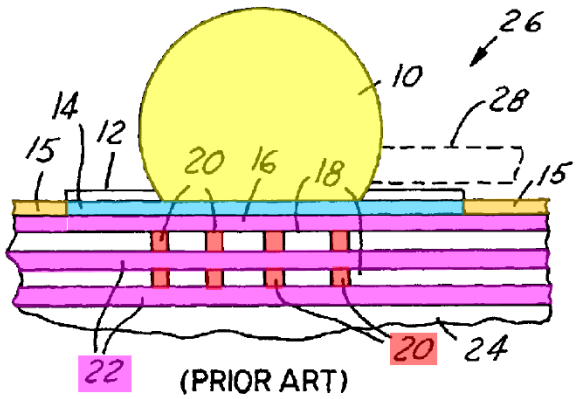


FIG. 6

Because the **top conductive layer** comprises: the bonding pad (**blue area** including **wire bonding area 48**) and the test pad (**green area** including **probe needle contact area 50**), and the remaining portion of the conductive layer under **passivation layer 42** (pink), as illustrated in Figure 6, they are "co-planar with one another" along the plane indicated by the straight red line. Ex. 1006-3, Fig. 6 (modified). To the extent hump 60 is argued to not be co-planar with the rest of the top conductive layer, *Lin* teaches the **probe needle contact area 50** was co-planar prior to scrub mark 58 and hump 60 being formed during a parametric testing procedure.

144. While *Lin* discloses a "prior art" embodiment where the **bonding pad 14** is a separate aluminum plating on top of the first metal redistribution layer, this is not required. It would have been obvious to a POSITA that the aluminum plating could be omitted, and the bumping process performed directly on the first metal redistribution layer.



(PRIOR ART)

FIG. 1

Ex. 1006-2, Fig. 1; Ex. 1006-4, 2:12-14 ("[a]s further shown in FIG. 1, the the **bonding pad 14** is provided in electrical contact with an upper conductive **upper conductive layer 16**.")

145. *Lin* teaches bonding pads 46 of Figures 5-7 "may be constructed of aluminum or other suitable electrically conductive material." Ex. 1006-5, 4:51-53.

146. A POSITA would understand the bonding pad 46 shown in Figures 5-7 may have an aluminum plating over the copper upper conductive layer, or the bonding pad 46 may simply comprise the copper upper conductive layer by itself.

147. Alternatively, it would be obvious to try either of these two identified, well-known solutions (*i.e.*, aluminum or "other suitable" metal), with a reasonable expectation of success. A POSITA understood an aluminum bond pad would typically be used for wire bonding techniques, because either gold or aluminum wire had been found to create reliable thermosonic bonds with aluminum pads. In

particular, using aluminum for both the wire and pad would not be prone to intermetallic formation or corrosion.

148. A POSITA also understood a copper bond pad would be used for solder bump bonding techniques in BGA applications, because copper was used to form a metallic system that minimized interdiffusion, eliminated corrosion, and provided the needed solder wettability, adhesion and electrical conductivity when used with Pb-free solder balls. As the upper conductive layer is typically already copper, a POSITA understood there was no need to form a separate copper pad on top of the copper upper conductive layer. Instead, a POSITA would have used the upper conductive layer itself as the bond pad. *Yong* provides evidence a POSITA knows this, as described for claim 5 in Ground 5 below.

A. Claim 6 — "The interface assembly of claim 5 wherein said first metal redistribution layer is electrically connected by way of a via to a second redistribution layer being disposed in a different plane than the first redistribution layer."

149. *Lin* renders this claim obvious. As noted relative to claim 5 (this Ground 4), the **top conductive layer** in *Lin* corresponds to the "first metal redistribution layer." The **top conductive layer** is immediately under the **passivation layer 42** and comprises: all of the the bonding pads (**blue area** including **wire bonding area 48**), all of the test pads (**green area** including **probe needle contact area 50**), the remaining portion of the conductive layer extending under **passivation layer 42**. The **top conductive layer** also includes other routing traces under **passivation layer**

42, as discussed for claim 5 in Ground 2 (discussing knowledge of a POSITA as evidenced by *Yong*, *Waizman*, and *Hsu*). With reference to the embodiment illustrated in Figures 5-7, *Lin* explains, "multiple bonding pads 46 of the present invention are typically embedded in the **passivation layer 42**, in electrical contact with integrated circuits (not shown) formed in the chip 40, typically in conventional fashion." Ex. 1006-5, 4:34-37, Figs. 5-7. *Lin* further illustrates this "conventional fashion" for electrical contacts and integrated circuits via Figure 1 (prior art). As shown in Figure 1 (prior art), "[t]he **conductive layers 16, 22** are disposed in electrical contact with each other through conductive **vias 20** that extend through the insulative layers 18" (Ex. 1006-4, 2:14-17):

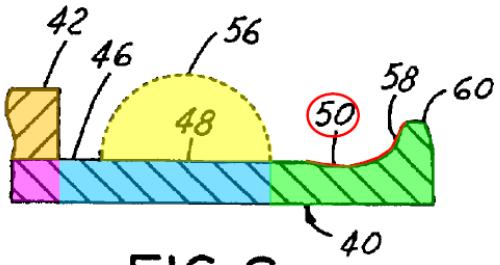
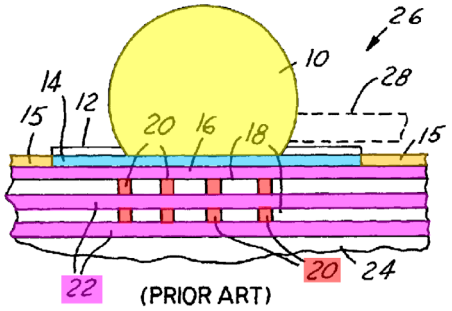
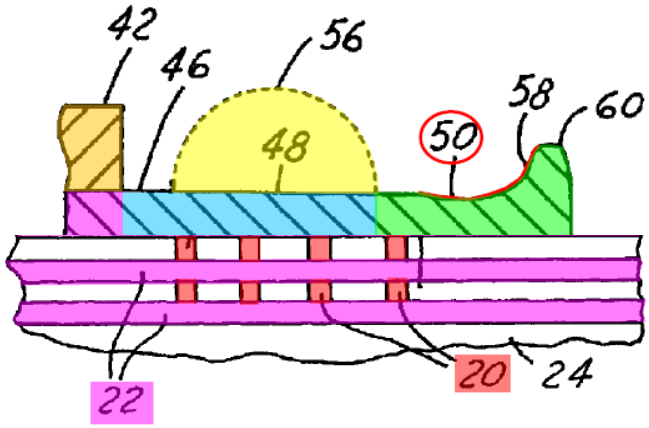


FIG. 6



(PRIOR ART)

FIG. 1



Ex. 1006-2 to -3, Figs. 1 and 6 (modified). With the **conductive layers 22** of Figure 1 shown in Figure 6 (these layers are necessarily present under the pad of Figure 6), the **conductive layers 22** correspond to the "second redistribution layer" and the **vias 20** correspond to the "via," as claimed in claim 6. As shown in Figure 1, *Lin* discloses **top layer 16** is in a different plane than the **conductive layers 22**, such that the **top conductive layer** of Figure 6 is similarly in a different plane, which correspond with the "second redistribution layer being disposed in a different plane than the first redistribution layer," as recited in claim 6.

B. Independent Claim 9 — "wafer test"

150. *Lin* teaches "wafer test" as explained above for the "wafer-level testing" of claim 1. Accordingly, it is my opinion that *Lin* discloses or renders obvious claim 9.

C. Independent Claim 10

1. Element 10[preamble] — "an interface assembly for a semiconductor wafer"

151. *Lin* discloses this element as shown for element 1[preamble] in Ground 3 above.

2. Element 10[a] — "a flip chip bonding pad including a region for performing a bumping process"

152. *Lin* discloses this element as shown for element 1[a] in Ground 3 above.

3. Element 10[b] — "a test pad integrally constructed with said bonding pad"

153. *Lin* discloses this element as shown for element 1[b] in Ground 3 above.

4. Element 10[c] — "said test pad being coplanar relative to said flip chip bonding pad"

154. *Lin* discloses this element as shown for element 1[c] in Ground 3 above.

5. Element 10[d] — "said test pad . . . including a probe region for performing wafer-level testing prior to performing said bumping process"

155. *Lin* discloses this element as shown for element 1[d] in Ground 3 above.

Further, *Lin* teaches "performing wafer-level testing" as explained for claim 1 in this Ground 4.

6. Element 10[e] — "a first metal redistribution layer electrically connected to said bonding and test pads, and being co-planar with one another"

156. *Lin* renders this element obvious as shown for claim 5 in this Ground 4 above.

7. Element 10[f] — "said first metal redistribution layer is electrically connected by way of a via to a second redistribution layer being disposed in a different plane than the first redistribution layer"

157. *Lin* renders this element obvious as shown for claim 6 in this Ground 4 above.

D. Independent Claim 10 — "performing wafer-level testing"

158. *Lin* teaches "performing wafer-level testing" as explained above for claim 1. Accordingly, it is my opinion that *Lin* discloses or renders obvious claim 10.

XIV. GROUND 5: CLAIMS 5-6 AND 10 ARE OBVIOUS IN VIEW OF *LIN* AND *YONG*

A. Independent Claim 1

1. Element 1[preamble]: "an interface assembly for a semiconductor wafer"

159. As noted above in Ground 3, *Lin* discloses the preamble of claim 1. *See* above Ground 3 analysis of *Lin* for claim element 1[preamble].

160. Further, *Yong* expressly teaches testing via a test interface prior to wire bonding. Specifically, *Yong* '6667 discloses "[a] bond pad (1) has a **probe region (14)** and a **wire bond region (12)** that are substantially non-overlapping." Ex. 1007-1, [57].

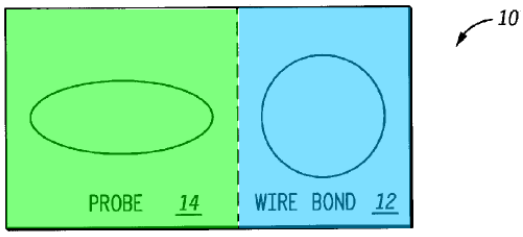


FIG. 1

Ex. 1007-2, Fig. 1. "By separating the **probe region** from the **wire bond region**, the **wire bond region** is not damaged by probe testing, allowing for more reliable wire bonds." Ex. 1007-10, [0011]. "FIG. 1 illustrates a top down view of a bond pad 10

in accordance with the present invention. Bond pad 10 is separated into a **wire bond region 12** and a **probe region 14** as indicated by the dashed line." Ex. 1007-10, [0012]. In my opinion, the bond pad is an interface. Accordingly, it is my opinion that *Yong* discloses claim element 1[preamble].

2. Element 1[a] — "a flip chip bonding pad including a region for performing a bumping process"

161. *Lin* discloses this element as shown in the Ground 3 analysis of *Lin* for element 1[a] above.

162. Similarly, "wire bond 12" of "bond pad 10" in *Yong* corresponds to the "flip chip bonding pad."

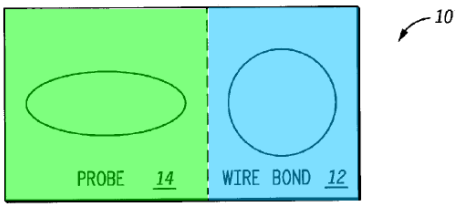


FIG.1

163. *Yong* does not expressly state it can be used with flip chips. In my opinion, a POSITA would have understood the embodiment shown in Figures 1 and 2 would allow for solder balls to be applied to the bond pad for flip chip packaging. For example, "FIG. 2 illustrates a cross-sectional view of a semiconductor device 20 in accordance with the present invention. Semiconductor device 20 has an edge, or perimeter 25, **passivation layer 18**, bond pad 10, interconnect region 24, and active

region, or substrate 26. The bond pad 10 has **wire bond region 12** and **probe region 14** (see FIG. 1) and is positioned relative to perimeter 25." Ex. 1007-10, [0013].

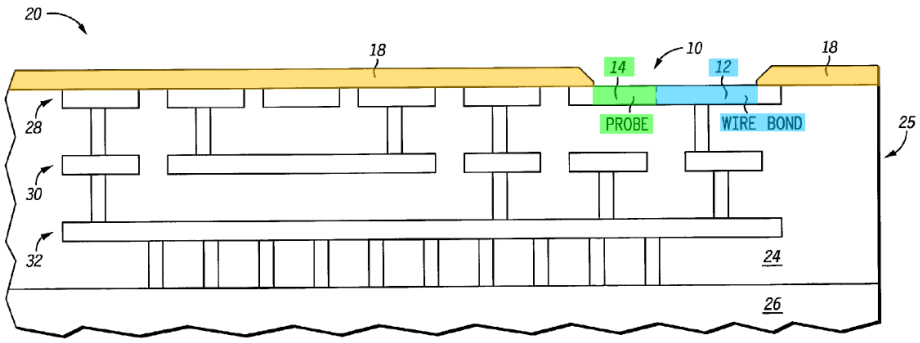


FIG.2

Ex. 1007-2, Fig. 2.

164. Indeed, *Lin* discloses a nearly identical bonding pad having a wire bond region adjacent to the probe region. As discussed in *Lin*, such a configuration "is suitable for wire bonding techniques, as well as ball grid array (BGA) and flip-chip packaging techniques." Ex. 1006-5, 4:24-26.

165. Accordingly, a POSITA would have known that *Yong*'s bond pad could similarly be used for performing a flip chip bumping process. Indeed, this exemplifies (1) the use of a known technique (using bond pads suitable for wire bonding in a flip chip bumping process) to improve similar devices (the similar bond pads in *Lin* and *Yong*) in the same way (performing a flip chip bumping process on the pads); and (2) applying a known technique (bumping process) to a known device (wire bond pads) ready for improvement to yield predictable results.

166. Thus, *Lin* teaches a bonding pad with a region for performing a bumping process. Additionally, a POSITA would have been motivated to improve *Yong*'s bond pad by performing a bumping process on it. Combining *Lin* and *Yong* in this manner is simply the combination of prior art elements according to known methods to yield predictable results. Accordingly, it is my opinion that *Lin* and in view of *Yong* renders claim element 1[a] obvious.

3. Element 1[b] — "a test pad integrally constructed with said bonding pad that form an integral conductive structure such that separate interconnect testing lines from said test pad to said bonding pad are not present in said integral structure"

167. *Lin* discloses this element as shown in the Ground 3 analysis of *Lin* for element 1[b] above.

168. Similarly, it is my opinion that the **probe region 14** and the **wire bond region 12** of *Yong* are integrally constructed without interconnect testing lines, as claimed.

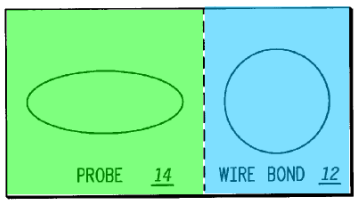


FIG.1

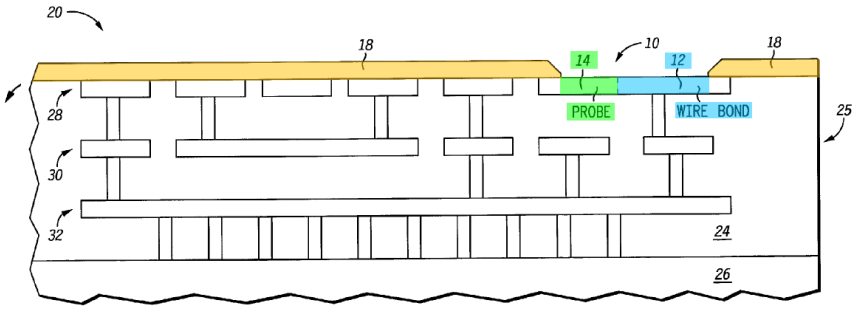


FIG.2

Ex. 1007-2, Figs. 1-2. Indeed, "Bond pad 10 is formed as part of final metal layer 28. After metal layer 28 is formed, passivation layer 18 is deposited over the surface

of the semiconductor device. Openings are provided in **passivation layer 18**, such as shown over bond pad 10, to allow for electrical contacts, such as between semiconductor device 20 to a pin on a package." Ex. 1007-10 to -11, [0014]. In addition, "The bond pad 10 has **wire bond region 12** and **probe region 14** (see FIG. 1) and is positioned relative to perimeter 25." Ex. 1007-10, [0013]. These passages confirm the **probe region 14** and the **wire bond region 12** of *Yong* are integrally constructed without interconnect testing lines.

169. Thus, both *Lin* and *Yong* teach a test pad integrally constructed with the bonding pad with no interconnect testing lines.

4. Element 1[c] — "said test pad being coplanar relative to said flip chip bonding pad and"

170. *Lin* discloses this element as shown in the Ground 3 analysis of *Lin* for element 1[c] above.

171. Similarly, it is my opinion the **probe region 14** and the **wire bond region 12** of *Yong* are coplanar, as claimed. This is shown in Figure 2:

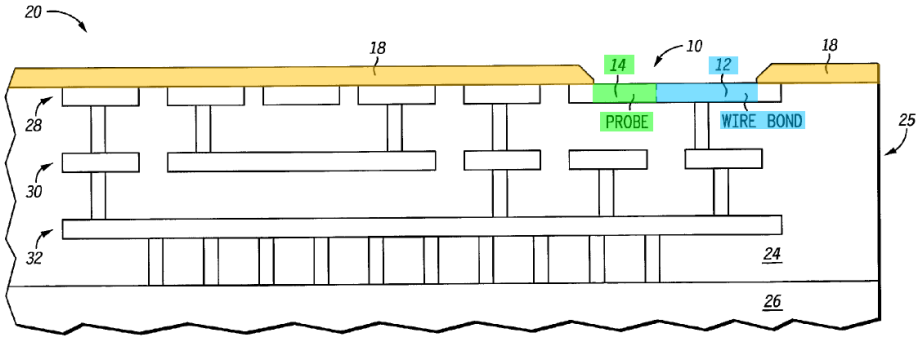


FIG.2

Ex. 1007-2, Fig. 2; Ex. 1007-10, [0013] ("The bond pad 10 has **wire bond region 12** and **probe region 14** (see FIG. 1) and is positioned relative to perimeter 25.")

5. Element 1[d] — "including a probe region for performing wafer-level testing prior to performing said bumping process"

172. *Lin* discloses this element as shown in the Ground 3 analysis of *Lin* for element 1[d] above.

173. Similarly, the oval area in the **probe region 14** of *Yong* corresponds to the claimed "probe region." This is shown in Figure 1:

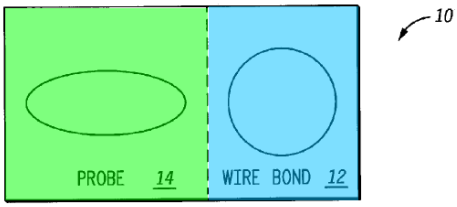


FIG.1

Ex. 1007-2, Fig. 1. *Yong* describes: "Each of the bond pads is separated into **probe regions** and **wire bond regions** as discussed in FIG. 1. The area on each bond pad bounded by an oval is the area designated generally for probe testing and the area on each bond pad bounded by a circle is the area designated generally for wire bonding." Ex. 1007-11 to -12, [0023].

B. Claim 5 — "The interface assembly of claim 1 further comprising a first metal redistribution layer electrically connected to said bonding and test pads, and being co-planar with one another."

174. *Lin* combined with *Yong* renders this claim obvious. In my opinion, the **top conductive layer** of *Lin* corresponds to the "first metal redistribution layer" and

is co-planar along the plane indicated by the straight red line with the bonding pad (**blue area** including **wire bonding area 48**) and the test pad (**green area** including **probe needle contact area 50**) in Figure 6 because they are all parts of the same conductive layer, as discussed relative to claim 5 in Ground 4.

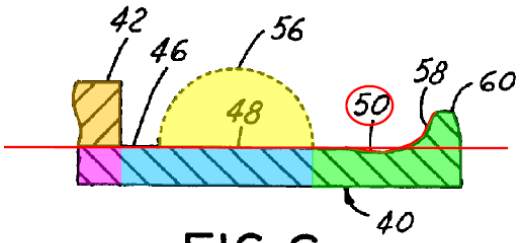


FIG. 6

Ex. 1006-3, Fig. 6 (modified). *Lin* teaches aluminum may be used as the bond pad 46: "Each bonding pad 46 may be constructed of aluminum or other suitable electrically conductive material." Ex. 1006-5, 4:51-53.

175. *Yong* similarly teaches aluminum may be used as a bond pad on top of a copper conductive layer but goes even further to teach the aluminum bond pad may be omitted. *Yong* teaches a redistribution layer coplanar with the test/bonding pads, because it teaches to omit an upper **aluminum layer** so wire can be bonded directly to a **copper top conductive layer**. In particular, *Yong* teaches that **aluminum bond pad 36** may be formed on top of the copper **upper conductive layer 28** to allow for wire bonding to the pad, as shown in Figure 3:

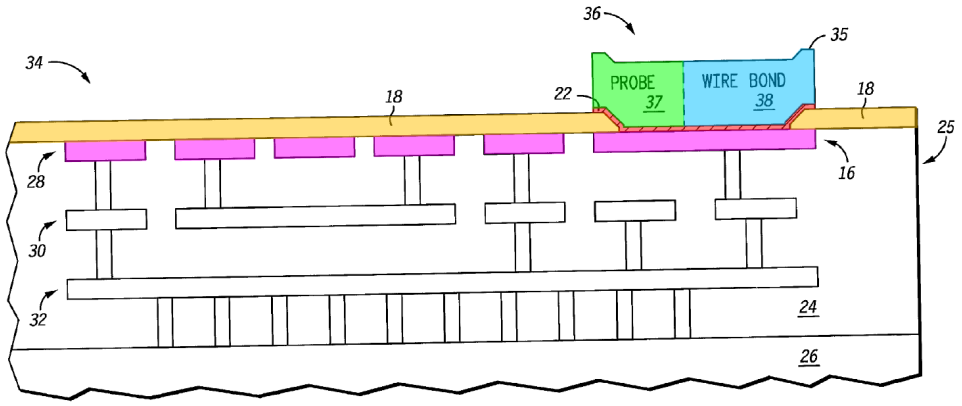


FIG.3

Ex. 1007-3, Fig. 3. "Bond pad 36 includes final metal layer pad 16 and aluminum pad layer 35." Ex. 1007-11, [0016].

176. However, *Yong* teaches aluminum bond pads are not necessary to withstand wire bonding. Instead, aluminum bond pads may be omitted and wire may be bonded directly to the top surface of the copper upper conductive layer 28, which is exposed through an opening in the passivation layer 18, as shown in Fig. 2:

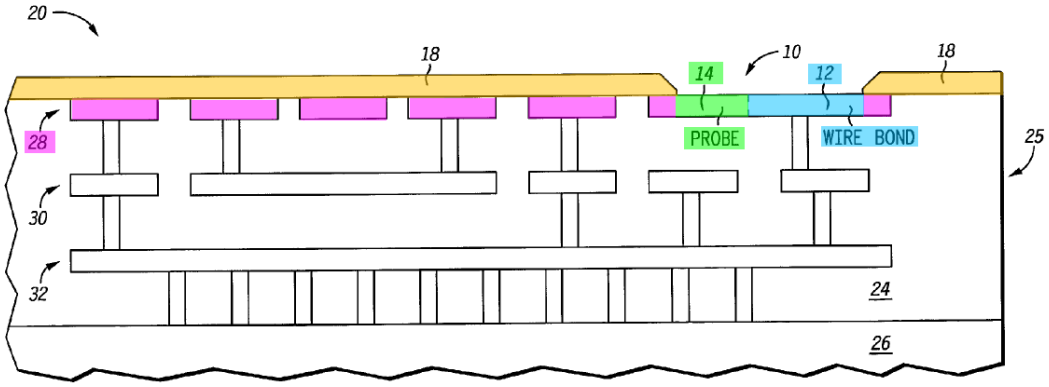
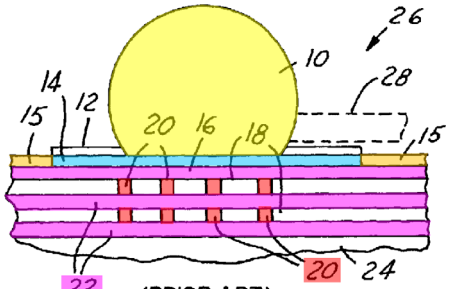


FIG.2

Ex. 1007-2, Fig. 2. *Yong* teaches that no aluminum bond pad layer is needed because "[t]ests have shown that bond pad 10 is strong enough to withstand the impact of a wire bonding tool and can be formed over interconnect layer 24 without damage to

interconnect layer 24 and any underlying circuits of active region 26 as illustrated in FIG. 2." Ex. 1007-11, [0015]. A POSITA understands that if the bond pad 10 is strong enough to withstand the impact of a wire bonding tool, the bond pad 10 would be strong enough to withstand the impact of soldering a solder ball, as discussed above relative to Ground 4, Claim 5. Thus, *Yong* teaches an aluminum bond pad is expressly not needed.

177. A POSITA would have been motivated to remove or omit the **aluminum layer 14** from the Figure 1 prior art embodiment of *Lin* so the bonding ball 10 can be soldered directly to the **copper upper conductive layer 16** similar to the embodiment of Figure 6.



(PRIOR ART)
FIG. 1

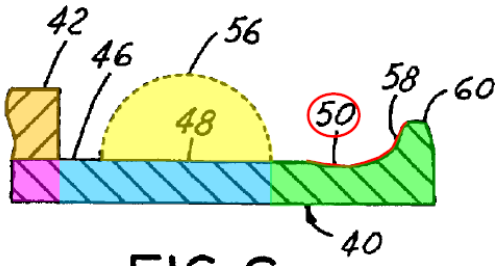


FIG. 6

Compare Ex. 1006-4, 2:4 and 2:21 (Fig. 1 shows "wire bonding ball 10" connects "a bonding wire 28") and Ex. 1006-6, 5:40-41 (Fig. 6 shows "the bonding ball 56 or other electrical contact"). A POSITA would view this modification of the *Lin* prior art embodiment of Figure 1 as the simple substitution of one known element for another (*e.g.*, it was known based on *Yong* to omit an aluminum plating to allow wire

bonding and soldering directly to the copper upper conductive layer) to obtain predictable results.

178. With reference to the prior art embodiment of Figure 1, *Lin* teaches an aluminum **bonding pad 14** may be formed on top of the **copper upper conductive layer 16** to allow for a **wire bonding ball 10** to be bound to the pad. Ex. 1006-5, 4:51-53 ("[e]ach bonding pad 46 may be constructed of aluminum or other suitable electrically-conductive material.")

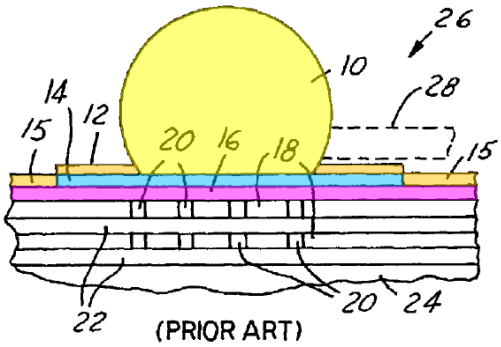
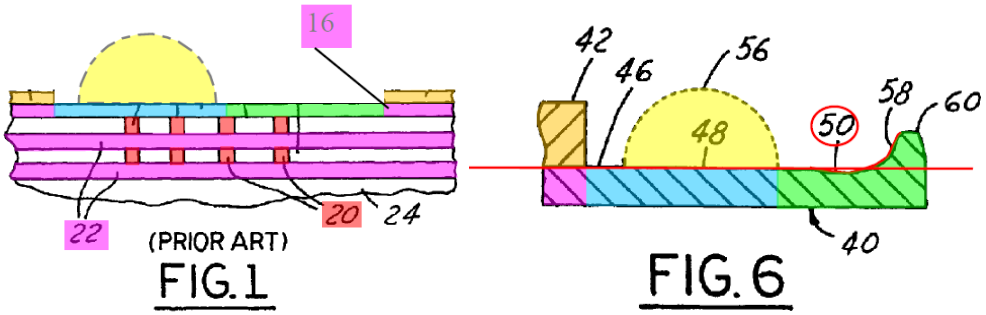


FIG. 1

Ex. 1006-2, Fig. 1.

179. Because *Yong* teaches the **copper upper conductive layer** "is strong enough to withstand the impact of a wire bonding tool," a POSITA would have been motivated to omit the aluminum bonding pad 14 from the *Lin* "prior art" embodiment and solder the **bonding ball 56** directly to the **top surface** of the **copper upper conductive layer 16**, as shown in modified Fig. 1:



Ex. 1006-2, Fig. 1 (modified) and Ex. 1006-3, Fig. 6 (modified). In this configuration, the **probe needle contact area 50** and **wire bonding area 48** are simply regions of, and coplanar with, **upper conductive layer 16**, identical to the embodiment shown in Figure 6.

180. In other words, *Yong*'s teaching that the wire can be bound directly on the upper conductive layer would have led one of ordinary skill to modify the *Lin* "prior art" embodiment to solder a solder bump in a similar manner to achieve a predictable result, *i.e.*, "a first metal redistribution layer electrically connected to said bonding and test pads, and being co-planar with one another." In particular, a POSITA would have known the advantage of coplanarity by omitting the aluminum plating from the redistribution layer would be the elimination of a processing step (aluminum plating), elimination of the contact resistance between two metal layers (aluminum and copper), particularly when the interconnection area is reduced to save area, or when a diffusion barrier is required between layers (like aluminum and copper). The contact resistance can cause unwanted voltage drop in high speed serial connections, and in power supply and ground return lines carrying current during

testing. Thus, a POSITA would have been motivated to omit the aluminum plating from the upper conductive layer of the *Lin* "prior art" embodiment as taught by *Yong*.

181. Accordingly, it is my opinion that *Lin* and in view of *Yong* renders claim 5 obvious.

C. Claim 6 — "The interface assembly of claim 5 wherein said first metal redistribution layer is electrically connected by way of a via to a second redistribution layer being disposed in a different plane than the first redistribution layer."

182. *Lin* combined with *Yong* renders this claim obvious. Beginning with the combinations achieved relative to claim 5, the **top conductive layer** (Fig. 6 modified) and the **upper conductive layer 16** (Fig. 1 modified) of *Lin* correspond to the claimed "first metal redistribution layer." Further, the **underlying conductive layers 22** correspond to the claimed "second redistribution layer," and are layers in different planes electrically connected by way of vias 20.

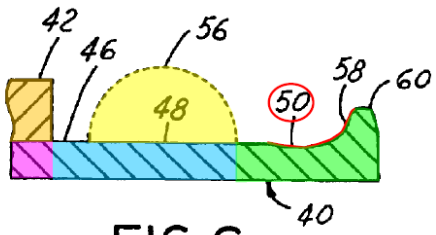


FIG. 6

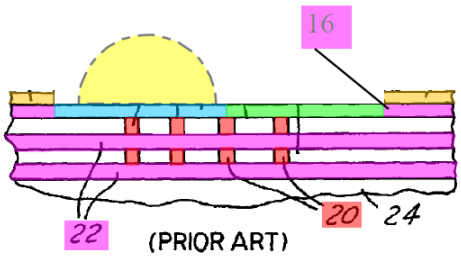


FIG. 1

Ex. 1006-3, Fig. 6 (modified); Ex. 1006-2, Fig. 1 (modified). "[U]pper conductive layer 16 … is separated from an underlying conductive layer 22 by an insulative layer 18. The conductive layers 16, 22 are disposed in electrical contact with each

other through conductive vias 20 that extend through the insulative layers 18." Ex. 1006-4, 2:12-18.

183. Similarly in *Yong*, the **metal layer 28** corresponds to the claimed "first metal redistribution layer," either of **metal layers 30 and 32** correspond to the claimed "second redistribution layer," and the layers in different planes are electrically connected by way of vias. In particular, as shown by the red line, the wire bond pad 12 is connected to the metal layer 28 through vias and lower metal layers 30 and 32.

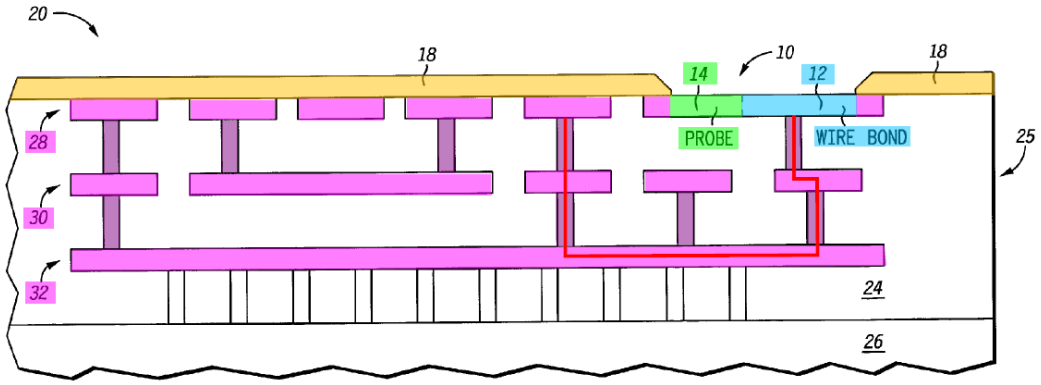


FIG.2

Ex. 1007-2, Fig. 2 (modified). "Interconnect region 24 includes metal layers 28, 30, and 32 for routing power, ground, signal, and other lines between various components of semiconductor device 20. … The metal layers of interconnect region 24 may be interconnected between each other using vias." Ex. 1007-10, [0013].

184. Thus, both *Lin* and *Yong* expressly teach connecting the first redistribution layer to the second redistribution layer by way of vias, where each

redistribution layer is in a different plane. Accordingly, it is my opinion that *Lin* in view of *Yong* renders claim 6 obvious.

D. Independent Claim 10

1. Element 10[preamble]

185. Both *Lin* and *Yong* teach this preamble as shown in the Ground 5 analysis above for claim 1 Preamble. Accordingly, it is my opinion that *Lin* in view of *Yong* renders element 10[preamble] obvious.

2. Element 10[a] — "a flip chip bonding pad including a region for performing a bumping process"

186. Both *Lin* and *Yong* teach this element as shown in the Ground 5 analysis above for claim 1[a]. Accordingly, it is my opinion that *Lin* in view of *Yong* renders element 10[a] obvious.

3. Element 10[b] — "a test pad integrally constructed with said bonding pad"

187. Both *Lin* Patent and *Yong* teach this element as shown in the Ground 5 analysis above for claim 1[b]. Accordingly, it is my opinion that *Lin* in view of *Yong* renders element 10[b] obvious.

4. Element 10[c] — "said test pad being coplanar relative to said flip chip bonding pad"

188. Both *Lin* Patent and *Yong* teach this element as shown in the Ground 5 analysis above for claim 1[c]. Accordingly, it is my opinion that *Lin* in view of *Yong* renders element 10[c] obvious.

5. Element 10[d] — "said test pad . . . including a probe region for performing wafer-level testing prior to performing said bumping process"

189. Both *Lin* Patent and *Yong* teach this element as shown in the Ground 5 analysis above for claim 1[d]. Accordingly, it is my opinion that *Lin* in view of *Yong* renders claim element 10[d] obvious.

6. Element 10[e] — "a first metal redistribution layer electrically connected to said bonding and test pads, and being co-planar with one another"

190. As shown in the Ground 5 analysis above for claim 5, *Lin* teaches claim element 10[e] (claim 5 recites similar limitations). Alternatively as shown in the Ground 5 analysis above for claim 5, *Yong* teaches claim element 10[e]. Thus, it would have been obvious to form in a single layer both the **bonding pad 14** and the **upper conductive layer 16** of *Lin* as taught by *Yong*, as explained above with reference to claim 5 (Ground 5). Accordingly, it is my opinion that *Lin* in view of *Yong* renders claim element 10[e] obvious.

7. Element 10[f] — "said first metal redistribution layer is electrically connected by way of a via to a second redistribution layer being disposed in a different plane than the first redistribution layer"

191. Both *Lin* and *Yong* teach this element as shown in the Ground 5 analysis above for claim 6. Accordingly, it is my opinion that *Lin* in view of *Yong* renders claim element 10[f] obvious.

XV. CONCLUSION

192. For at least the above reasons, it is my opinion: claims 1-10 of the '173 patent are anticipated or rendered obvious by *Mardi*; claims 1-7 and 9-10 of the '173 patent are anticipated or rendered obvious by *Lin*; and claims 5-6 and 10 of the '173 patent are obvious in view of *Lin* and *Yong*.