IN THE UNITED STATES DISTRICT COURT
FOR THE WESTERN DISTRICT OF TEXAS
WACO DIVISION

BELL SEMICONDUCTOR, LLC,	§	
	§	
Plaintiff,	§	
	§	Civil Action No. 6:20-cv-00296-ADA
vs.	§	
	§	JURY TRIAL DEMANDED
MICROCHIP TECHNOLOGY INC.; and	§	
MICROSEMI CORPORATION,	§	
	§	
Defendant.	§	

DEFENDANTS' PRELIMINARY INVALIDITY CONTENTIONS

Pursuant to the Court's November 20, 2020 Scheduling Order (Dkt. 37), Defendants Microchip Technology Incorporated ("Microchip") and Microsemi Corporation ("Microsemi") (collectively "Defendants") serve the following preliminary invalidity contentions to Plaintiff Bell Semiconductor ("Bell Semic"). Defendants are concurrently producing (1) all prior art referenced in these invalidity contentions, (2) technical documents sufficient to show the operation of the accused products, and (3) summary, annual sales information for the accused products for the two years preceding the filing of the Complaint.

I. Introduction

In the absence of a claim construction order from the Court, Defendants base these contentions in part upon the apparent constructions of the asserted claims of U.S. Patent Nos. 8,049,340 ("the '340 patent"), 8,288,269 ("the '269 patent"), 6,743,669 ("the '669 patent"), 7,221,173 ("the '173 patent"), 6,707,132 ("the '132 patent"), 6,624,007 ("the '007 patent")

(collectively "the Asserted Patents") advanced by Bell Semic in its infringement contentions.[1] By identifying exemplary prior art that anticipates and/or renders obvious the asserted claims, Defendants do not admit that the claim limitations are capable of construction, nor do Defendants admit that any claim limitations are supported with an appropriate written description and enabling disclosure in the applicable patent specifications. Nothing herein should be construed as an admission of agreement with Bell Semic's apparent claim constructions or its application of the asserted claims to any of the accused products. Defendants expressly reserve the right to propose alternative constructions to those advocated by Bell Semic and to rebut Bell Semic's actual claim construction and infringement positions.

Bell Semic served its Preliminary Infringement Contentions on October 9, 2020. Defendants reserve the right to amend and supplement these invalidity contentions in response to any amendments to, or revisions of, Bell Semic's infringement contentions or claim construction assertions.

While Defendants contest that any of the claim limitations of the Asserted Patents read on the accused products, to the extent Bell Semic alleges infringement, under Bell Semic's interpretation, it has conceded the invalidity of the Asserted Patents where an accused product predates the Asserted Patents. *See Peters v. Active Mfg. Co.*, 21 F. 319, 321 (C.C.S.D. Ohio 1884), *aff'd*, 129 U.S. 530 (1889) ("That which infringes, if later, would anticipate, if earlier.").

The obviousness combinations provided herein and, in the charts attached as Appendices A–F, are exemplary and are not intended to be exhaustive. Additional obviousness combinations of the references identified in these contentions are possible, and Defendants reserve the right to

[1] U.S. Patent Nos. 6,153,543 and 6,544,907 were also asserted in Bell Semic's Complaint and infringement contentions but have since been dismissed by the Court. Dkt. 33.

use any such combinations in this litigation. In particular, Defendants are currently unaware of the extent, if any, to which Bell Semic will contend the limitations of the claims at issue are not disclosed in the art identified by Defendants as anticipatory or otherwise. To the extent Bell Semic contests any such limitation is not anticipatory or is not present in a reference or combination of references, Defendants reserve the right to identify other references that would have made obvious the addition of the allegedly missing limitation to the disclosed system or method of operation. Similarly, to the extent Bell Semic attempts to swear behind the priority dates asserted in its contentions,[2] Defendants reserve the right to identify other references that anticipate or render obvious the asserted claims.

Defendants' investigation into prior art remains ongoing, including prior art identified in these disclosures, prior art not yet known to Defendants, third-party prior art, and related evidence, documents, and knowledgeable witnesses. Moreover, prior art may become relevant depending upon the invention date Bell Semic alleges for each of the asserted patents, the evidence supporting such allegations, the claim constructions Bell Semic asserts, the claim constructions the Court adopts, Bell Semic's amendment or supplementation of its infringement contentions, and Defendants' further understanding of Bell Semic's infringement contentions. Additional information and evidence about prior art, including documentation and witness testimony, may be presented later. Defendants reserve the right to present this additional information and evidence in support of its invalidity contentions and to amend and supplement these invalidity contentions

[2] Bell Semic asserts that it "expects to establish invention of the subject matter of the asserted claims of the Bachman Patent at least as early as May 10, 2004." *See* Preliminary Infringement Contentions at 9. However, Bell Semic has not identified any documents to support its assertion of an earlier conception date, invention date, and/or diligence from the purported conception date to the September 29,2004 filing date of the '173 Patent.

accordingly in a manner consistent with the Scheduling Order, Federal Rules of Civil Procedure, and the Court's rules.

II. The Asserted Patent Claims

In its Preliminary Infringement Contentions, Bell Semic has asserted that Defendants allegedly infringe the following claims of the Asserted Patents:

Patent	Asserted Claims
8,049,340 (Hall)	1, 3, 4, 6, 12, 13, 16–18
8,288,269 (Hall)	1, 3, 4, 6, 7, 10–14
6,743,669 (Lin)	1–3, 5–7, 9
7,221,173 (Bachman)	9
6,707,132 (Banerjee)	5, 12, 14
6,624,007 (Kobayakawa)	1, 3, 4

Although Bell Semic has not proffered infringement contentions with respect to other unasserted claims of the Asserted Patents, Defendants reserve the right to modify, amend, and/or supplement their invalidity contentions if the Court allows Bell Semic to assert infringement of presently unasserted claims of the Asserted Patents. While Defendants provide the following invalidity contentions for the claims asserted by Bell Semic, Defendants hereby reserve their rights to seek invalidation of all claims in each of the Asserted Patents.

III. Invalidity Contentions

In an effort to focus the issues, Defendants cite representative portions of an identified reference, even where a reference may contain additional support for a particular claim limitation. Persons of ordinary skill in the art generally read an item of prior art as a whole and in the context of other publications and literature. Thus, to understand and interpret any specific statement or disclosure within a prior art reference, such persons would rely on other information within the reference, along with other publications and their general scientific knowledge. Defendants may rely on uncited portions of the prior art references and on other publications (*e.g.*, prior art

references cited on the face of the Asserted Patents and the patents or technical references cited within the body of the Asserted Patents) and expert testimony to provide context, and as aids to understanding and interpreting the portions that are cited. Defendants may rely on expert opinions for additional or different motivations to combine the prior art references. Defendants may also rely on explicit or implicit motivations to combine prior art references disclosed in the references.

Where Defendants cite a particular figure in a prior art reference, the citation should be understood to encompass the caption and description of the figure and any text relating to the figure in addition to the figure itself. Conversely, where a cited portion of text refers to a figure, the citation should be understood to include the figure as well. Additional evidence regarding the features and elements of the prior art reference may be provided by witness testimony, or by additional documents that describe the prior art reference that are discovered through the course of ongoing discovery.

Defendants may rely on any additional prior art and/or motivations to combined prior art references identified in the future by any party in this litigation or in any related litigation, as well as any references discussed or disclosed during third party discovery or in any expert report on the validity of any of the Asserted Patents. Defendants expressly incorporate herein the invalidity contentions served by defendants in related cases filed by Bell Semic (*e.g.*, *Bell Semiconductor, LLC v. NXP Semiconductors, N.V. et al*, 1-20-cv-00611 (W.D. Tex.); *Bell Semiconductor, LLC v. Texas Instruments Incorporated,* 2-20-cv-00048 (E.D. Tex.); *Bell Semiconductor, LLC v. Integrated Device Technology, Inc.*, 1-19-cv-02155 (D. Del.); *Bell Semiconductor, LLC v. Renesas Electronics Corporation et al*, 6-19-cv-02196 (M.D. Fla.)), as they relate to the Asserted Patents; as well as any other invalidity contentions related to the Asserted Patents served on or otherwise provided to Bell Semic, whether past or in the future. Defendants also expressly incorporate herein

the *inter partes* review petitions and accompanying declarations and exhibits related to the Asserted Patents (including, but not limited to the prior art references and motivations to combine those references), including those already filed with the United States Patent and Trademark Office (*e.g.*, IPR2020-01691, IPR2020-01693, IPR2020-01692, IPR2020-01690, IPR2020-01694, IPR2021-00123, IPR2021-00147, IPR2021-00148, IPR2021-00177, IPR2021-00168, IPR2021-00191, IPR2021-00180) and any that may be filed in the future. Defendants reserve the right to modify, amend, and/or supplement their invalidity contentions in response to positions taken by Bell Semic in the above-referenced *inter partes* review proceedings. Defendants may also rely on references identified in the file history of any of the Asserted Patents.

A. U.S. Patent No. 8,049,340

1. Prior Art Patents Under 35 U.S.C. §§ 102(a), (b), (e), (g).

Number	Country	Date of Issue	Date of Application
U.S. Patent No. 6,765,298 (Chin)	United States	Jul. 20, 2004	Dec. 8. 2001
U.S. Patent No. 6,717,255 (Oggioni)	United States	Apr. 6, 2004	Oct. 23, 2001
U.S. Patent No. 6,797,891 (Blair)	United States	Sep. 28, 2004	Mar. 26, 2002
JP 2003-273525 (Inoue)	Japan	Sep. 26, 2003	Mar. 15, 2002
US 6,713,853 (Fazelpour)	United States	Mar. 30, 2004	Jul. 23, 2002
U.S. 7304,863 (Wu)	United States	Dec. 4, 2007	Jun. 9, 2003
U.S. 8,389,870 (Bills)	United States	Mar. 5, 2013	Mar. 9, 2010
U.S. 6,020,562 (Burns et al.)	United States	Feb. 1, 2000	Nov. 11, 1997
U.S. Patent No. 6,392,301 (Waizman et al.)	United States	May 21, 2002	Oct. 25, 1999
U.S. Patent No. 6,797,891 (Blair et al.)	United States	Sep. 28, 2004	Mar. 26, 2002
U.S. Patent No. 6,909,196 (Batra et al.)	United States	Jun. 21, 2005	Jun. 21, 2002

U.S. Patent No. 7,349,223 (Haemer et al.)	United States	Mar. 25, 2008	Jun. 16, 2004
U.S. Patent No. 6,908,340 (Shafer et al.)	United States	Jun. 21, 2005	Sep. 11, 2003

2. Prior Art Publications Under 35 U.S.C. §§ 102(a), (b), (e), (g).

Title	Date of Publication	Author(s)	Publisher
Motorola - MC92600 Quad 1.25 Gbaud Reduced Interface SERDES Reference Manual	Mar. 2003	Unknown	Motorola
MC92600 WarpLink Quad User's Manual	Feb. 2, 2000	Unknown	Motorola
Motorola - MC92602 Quad 1.25 Gbaud Reduced Interface SERDES Reference Manual	Mar. 2003	Unknown	Motorola
MC92602RMAD Errata	Jul. 2003	Unknown	Motorola
High-Speed Digital System Design—A Handbook of Interconnect Theory and Design Practices	2000	Hall et al.	John Wiley & Sons 2000
Status 1998	1998	Burggraaf, P.	Integrated Circuit Engineering Corporation
Semiconductor Packaging: A DoD Dual Use Technology Assessment Final Report	1997	Unknown	Department of Defense
IC Package Designs and IC Signal Performance	2003	Sean Clark	Fairchild Semiconductor
Design techniques for energy efficient and low-power systems	2000	Paul J.M. Havinga	Multimedia Systems, University of Twente
Roadmaps of Packaging Technology	1997	Eric Bogatin	Integrated Circuit Engineering Corporation

Microelectronic Circuits	1991 (3d ed.)	Sedra, Adel et al.	Saunders College Publishing
The Analysis and Design of Linear Circuits	1994	Thomas et al.	Prentice Hall
Parasitic pads	Aug. 17, 2000	Howard Johnson	EDN
A Practical Guide to High-Speed Printed-Circuit-Board Layout	Sep. 2005	John Adrizzoni	Analog Dialogue
Printed Circuit Board Design Techniques for DS40MB200	Oct. 2005	TK Chin	National Semiconductor
Microvias effect on high-frequency signal integrity	Sep. 2002	H Holden	Circuit World (Emerald Insight)
JP2003-273525	Sep. 26, 2003	T Inoue	JPO
Discontinuity impacts and design considerations of high speed differential signals in FC-PBGA packages with high wiring density	2005	N Na et al.	IEEE
PM8358 QuadPHY® 10GX Data Sheet	Nov. 2005	Unknown	PMC-Sierra
Simulation and Measurement of High Speed Serial Link Performance in a Dense, Thin Core Flip Chip Package	May 30, 2006	M. Rolands et al.	IEEE
Microelectronic Circuits	1991	Sedra et al.	Saunders College Publishing
U.S. Patent Pub. 2005/0011676	Jan. 20, 2005	Barr et al.	USPTO
U.S. Patent Pub. 2005/0037601	Feb. 17, 2005	Hsu et al.	USPTO
Single-Chip 4 500-MBd CMOS Transceiver	Dec. 1996	Widmer et al.	IEEE
Final Report for the 10 to 100 Gigabit/Second Networking Laboratory Directed Research and Development Project	Apr. 2001	Witzke et al.	Sandia National Labs.

3. Prior Art Systems Under 35 U.S.C. §§ 102(a), (b), (g).

Defendants identify the systems disclosed in the patents and publications listed above as prior art. Additionally, Defendants identify the following systems, including constituent software, hardware, methods, and processes, as prior art that may anticipate or render obvious the asserted claims of the '340 patent. Each system (1) was known or used in this country before the alleged invention of the claimed subject matter of the '340 patent, (2) was in public use and/or on sale in this country more than one year before the filing date of the application for the '340 patent and/or (3) was invented and not abandoned, suppressed or concealed prior to the alleged invention of the '340 patent.

System or Product	Seller/ Purchaser/ User
MC92600	Motorola
PM63252 RSE-160	PMC-Sierra (now Microchip)
Amazon (F751807) product	Cisco
PPE2CR (F751841) product	Cisco
SantaCruz (F751697) product	Cisco
VTXP48 product	TranSwitch
UltraSPARC III Cheetah+ SME1052	Sun Microsystems

Discovery has not yet started, and Defendants will provide further identification of the above systems and any other systems Defendants learn about through discovery ("the '340 Patent Prior Art Systems"), including constituent software, hardware, methods, and processes, as prior art that may anticipate or render obvious the asserted claims of the '340 patent, as such information becomes available. Defendants reserve the right to amend and supplement these contentions to provide disclosures based on further investigation of and as they acquire additional information about these systems.

4. Invalidity Under 35 U.S.C. § 103.

In addition to certain claims being anticipated, the Asserted Claims are also invalid as obvious over the same teachings identified for anticipation and various combinations of the references as shown in the claim charts accompanying these contentions for at least the reasons set forth in the accompanying claim charts.

In addition, in *KSR International Co. v. Teleflex, Inc.*, the United States Supreme Court held that, among other things, "[t]he combination of familiar elements according to known methods is likely to be obvious when it does no more than yield predictable results." 127 S. Ct. 1727, 1739 (2007); *see also id.* at 1731 ("[A] court must ask whether the improvement is more than the predictable use of prior art elements according to their established functions."). In particular, a patent is obvious where "the content of the prior art, the scope of the patent claim, and the level of ordinary skill in the art are not in material dispute, and the obviousness of the claim is apparent in light of these factors." *Id.* at 1745–46. The Supreme Court further explained that "if a technique has been used to improve one device, and a person of ordinary skill in the art would recognize that it would improve similar devices in the same way, using the technique is obvious unless its actual application is beyond his or her skill." *Id.* at 1731.

The *KSR* Court also recognized that market pressures will motivate a person of ordinary skill to survey known art for solutions to problems. *Id.* at 1732 ("When there is a design need or market pressure to solve a problem and there are a finite number of identified, predictable solutions, a person of ordinary skill in the art has good reason to pursue the known options within his or her technical grasp."). When a person of ordinary skill uses an identified, predictable solution to solve a problem, "it is likely the product not of innovation but of ordinary skill and common sense." *Id.* at 1742. In addition, when "a work is available in one field of endeavor, design incentives and other market forces can prompt variations of it, either in the same field or a different

one." *Id.* at 1740. If a person of ordinary skill can implement a predictable variation, U.S.C. § 103 bars its patentability. *Id.* at 1731. The rationale to combine or modify prior art references is significantly stronger when references seek to solve similar problems, come from the same field, and the solutions to the identified problems in the references correspond well. *In re Inland Steel Co.*, 265 F.3d 1354, 1362 (Fed. Cir. 2001).

Here, to the extent not anticipated, the Asserted Claims represent no more than the result of ordinary implementation of the prior art and no Asserted Claim goes beyond combining familiar elements in known methods to achieve predictable results or does more than choose between clear alternatives known to those of skill in the art. Thus, to the extent that an Asserted Claim is not anticipated, it is nevertheless invalid as obvious.

Though the claim charts (Appendices A1–AX) identify particular exemplary obviousness combinations, Defendants' obviousness defenses are not limited to these combinations. Additional exemplary obviousness combinations on which Defendants rely are provided in the summary table in Section III.A.6 below. The identified prior art references and systems are analogous art and generally directed toward substrate designs. *See Comaper Corp. v. Antec, Inc.*, 596 F.3d 1343, 1350–51 (Fed. Cir. 2010). But more than that, they are complete systems designed in very similar ways to each other, to solve the same problems as the Asserted Patents, namely, to design effective substrates for routing signals to and from integrated circuits and other circuit elements. Because the references are so similar to each other and to the alleged invention of the '340 patent, it would be obvious and routine for an ordinarily skilled artisan to combine any of their elements with one another. One of ordinary skill in the art would have also been motivated to combine the identified prior art references based on the references themselves; the common knowledge of one of ordinary skill in the art; the implied and inherent teachings of the prior art as a whole; and the nature of the

problems allegedly addressed by the ’340 patent and the prior art.

Moreover, one of ordinary skill in the art would have combined familiar elements according to known methods to predictably achieve the claimed invention. *KSR*, 127 S. Ct. at 1740. Likewise, one of ordinary skill in the art, at the time of the alleged invention, would recognize that similar well-known substrate designs could have been improved in similar ways, and would have applied those improvements in the same way to predictably achieve the claimed invention. *Id*. For at least these reasons, it would have been obvious to a person of skill in the art at the time of the alleged invention of the Asserted Claims to combine the various references cited herein to practice the Asserted Claims and there is a motivation in the art to make such a combination.

A person of ordinary skill in the art would have found it obvious to design cutouts in metal layers over signal pads in order to reduce parasitic capacitance between the signal pads and the metal in parallel layers. For example, a person of ordinary skill in the art would have been motivated to combine any of the prior art references with any one of the other references that disclose the use of cutouts to render obvious the asserted claims, including, for example, Chin, Inoue, Fazelpour, Morrison, Holden, and PM6352. Alternatively, a person of ordinary skill in the art would have found it obvious to look to these related references as sources of available design choices that the person of ordinary skill in the art would have found obvious to try and would have understood how to do so. A person of ordinary skill in the art would have a good expectation of success, as many similar designs had been proposed, tested, and used in the industry. Further, design tools at the relevant time would have allowed a person of ordinary skill in the art to design the various cutout sizes and arrangements and perform accurate simulations of how the new design would function. This ability to simulate designs would have increased the expectation of success in implementing the design elements described in the prior art.

The independent claims recite an arrangement of contact pads and associated cutouts within a substrate. The dependent claims recite details a POSITA would have understood as ordinary design choices or common uses.

For example, claims 4 and 16 recite rows of transmit and receive pads/contacts. A POSITA would have understood a common signal type for an integrated circuit package is a transmit or receive signal to allow the integrated circuit to communicate with another circuit. Transmit and receive signals transfer data out of or into an IC thus allowing that IC to communicate with other components in a system. Other components might include, for example, a network adapter for communicating with other systems or a central processing unit requesting or producing data communicated over the network. One specific class of components with rows of transmit and receive pins were SERDES (serializer/deserializer) chips. SERDES chips included at least one set of pins for inputting parallel data (*i.e.*, many simultaneous data bits on multiple "parallel" lines) to be converted to a serial format (*i.e.*, a single stream of data bits serially streaming over one line or a matched pair of differential lines) for transmission by the SERDES and at least one set of pins for outputting parallel data converted from a serial format received by the SERDES. A POSITA would also have understood that contact pads in integrated circuits are arranged in rows, especially in BGA packages. Examples of SERDES references include MC92600, PM6352, and Wu.

In another example, claim 6 requires the second layer to be a routing layer. A POSITA would have understood that metal layers with routing traces are commonly used in integrated circuit packages and the ordering of layers to be an ordinary design choice. Ground and reference layers may distribute power to ICs in the package and they may also be used as shielding to reduce crosstalk, or interference, between signal lines on the same or on other layers, or with other components. Routing traces in metal layers distribute signals between ICs within the package and

connect IC signal pads with package ball pads. This routing becomes increasingly complex as the number of signal lines increases, which is the case with ever larger BGA packages. A POSITA would understand the need to consider using the second metal layer to be a routing layer to maximize routing flexibility within the substrate. Examples of routing layer references include, HighSpeed, PM6352, and Alcoe.

In yet another example, claims 3 and 18 recite cutouts having the same dimensions as the ball pads. A POSITA would have understood the cutouts could be sized smaller than, equal to, or larger than the ball pads to tune the impedance by reducing parasitic capacitance. As explained in the technology background of Defendants' IPR petition, the amount of parasitic capacitance is determined in part by the overlapping area between the ball pads and metal in a parallel metal layer. Thus, cutouts sized smaller than the ball pads will reduce, but not eliminate parasitic capacitance. Cutouts sized identically to the ball pads will nearly eliminate parasitic capacitance, but some so-called "edge capacitance" may remain. A POSITA would also understand that cutouts reduce shielding between layers. Thus, a POSITA would understand that the size of the cutouts represents a design tradeoff and would have been equipped to try different cutout sizes and simulate or test the effects of reduction in parasitic capacitance versus increased interference or crosstalk. Examples of same-size references include Oggioni and PM6352.

In still another example, claim 16 recites conversion of serial data to/from parallel data (*e.g.*, SERDES). A POSITA would have understood a SERDES to commonly include high frequency serial data streams and therefore a POSITA would seek to reduce parasitic capacitance by employing cutouts in metal layers adjacent to substrate contact pads. Serialized data streams operate at many times the rate of their corresponding parallel data streams, since a serialized data stream transports, over a single line (or a differential pair, where each of the lines carries a mirror

image signal of the other), the data on multiple parallel lines, at the same data rate. Examples of SERDES references include MC92600, PM6352, and Wu.

Because these design choices or uses were so common and ordinary, authors of academic and industry publications and those making patent disclosures rarely explained them in detail.

Defendants reserve the right to further specify the motivations to combine the prior art in response to positions that Bell Semic may take later in this case and as discovery, including third party and expert discovery, proceeds. Defendants may rely on any and all portions of the prior art, other documents, and expert testimony to establish that a person of ordinary skill in the art would have been motivated to modify or combine the prior art and his/her knowledge to render the claims invalid as obvious.

5. Invalidity Under 35 U.S.C. § 112.

Defendants assert that claim 16 (and claims 17 and 18, which depend therefrom) of the '340 patent is invalid for failure to meet the requirements of 35 U.S.C. § 112(a). In particular, claim 16 is invalid because the phrase "the electrically conductive layers are operable to convert a serial data stream to or from a parallel data stream" lacks written description. This phrase lacks any corresponding disclosure in the '340 patent to convey that the inventors were in possession of the invention as claimed.

Defendants assert that claim 6 of the '340 patent is invalid for failure to meet the requirements of 35 U.S.C. § 112(b). In particular, claim 6 is invalid because the phrase "the second electrically conductive layer comprises a routing layer electrically connected with the first electrically conductive layer" is indefinite. The phrase, viewed in light of the specification and prosecution history, fails to inform those skilled in the art about the scope of the invention with reasonable certainty.

Defendants assert that claims 1 and 12 (and claims 3, 4, 6, 13, and 16–18, which depend therefrom) of the '340 patent are invalid for failure to meet the requirements of 35 U.S.C. § 112(b). In particular, claims 1 and 12 are invalid because the phrase "substantially no overlap," viewed in light of the specification and prosecution history, fails to inform those skilled in the art about the scope of the invention with reasonable certainty.

6. Summary of '340 Patent Invalidity

The following table summarizes Defendants' invalidity contentions related to the '340 patent, as set forth in this document and Appendices A1–A10.

Invalidity Grounds	Asserted Claims
35 U.S.C. § 112	1, 3, 4, 6, 12, 13, 16–18
35 U.S.C. § 103 – Chin	1, 3, 4, 6, 12, 13, 16–18
35 U.S.C. § 103 – PM6352	1, 3, 4, 6, 12, 13, 16–18
35 U.S.C. § 103 – Inoue	1, 3, 4, 6, 12, 13, 16–18
35 U.S.C. § 103 – Fazelpour	1, 3, 4, 6, 12, 13, 16–18
35 U.S.C. § 103 – Holden	1, 3, 4, 6, 12, 13, 16–18
35 U.S.C. § 103 combination of one or more of {Chin, PM6352, Inoue, Fazelpour, Holden} with one or more of {MC92600, PM6352, Wu}	4, 16–18
35 U.S.C. § 103 combination of one or more of {Chin, PM6352, Inoue, Fazelpour, Holden} with one or more of {HighSpeed, PM6352, Alcoe}	6
35 U.S.C. § 103 combination of one or more of {Chin, PM6352, Inoue, Fazelpour, Holden} with one or more of {Oggioni, PM6352}	3, 18

B. U.S. Patent No. 8,288,269

1. Prior Art Patents Under 35 U.S.C. §§ 102(a), (b), (e), (g).

Number	Country	Date of Issue	Date of Application
U.S. Patent No. 6,765,298 (Chin)	United States	Jul. 20, 2004	Dec. 8. 2001

U.S. Patent No. 6,717,255 (Oggioni)	United States	Apr. 6, 2004	Oct. 23, 2001
U.S. Patent No. 6,797,891 (Blair)	United States	Sep. 28, 2004	Mar. 26, 2002
JP 2003-273525 (Inoue)	Japan	Sep. 26, 2003	Mar. 15, 2002
US 6,713,853 (Fazelpour)	United States	Mar. 30, 2004	Jul. 23, 2002
U.S. 7304,863 (Wu)	United States	Dec. 4, 2007	Jun. 9, 2003
U.S. 8,389,870 (Bills)	United States	Mar. 5, 2013	Mar. 9, 2010
U.S. 6,020,562 (Burns et al.)	United States	Feb. 1, 2000	Nov. 11, 1997
U.S. Patent No. 6,392,301 (Waizman et al.)	United States	May 21, 2002	Oct. 25, 1999
U.S. Patent No. 6,797,891 (Blair et al.)	United States	Sep. 28, 2004	Mar. 26, 2002
U.S. Patent No. 6,909,196 (Batra et al.)	United States	Jun. 21, 2005	Jun. 21, 2002
U.S. Patent No. 7,349,223 (Haemer et al.)	United States	Mar. 25, 2008	Jun. 16, 2004
U.S. Patent No. 6,908,340 (Shafer et al.)	United States	Jun. 21, 2005	Sep. 11, 2003

2. Prior Art Publications Under 35 U.S.C. §§ 102(a), (b), (e), (g).

Title	**Date of Publication**	**Author(s)**	**Publisher**
Motorola - MC92600 Quad 1.25 Gbaud Reduced Interface SERDES Reference Manual	Mar. 2003	Unknown	Motorola
High-Speed Digital System Design—A Handbook of Interconnect Theory and Design Practices	2000	Hall et al.	John Wiley & Sons 2000
MC92600 WarpLink Quad User's Manual	Feb. 2, 2000	Unknown	Motorola
Motorola - MC92602 Quad 1.25 Gbaud Reduced Interface SERDES Reference Manual	Mar. 2003	Unknown	Motorola
MC92602RMAD Errata	Jul. 2003	Unknown	Motorola

Status 1998	1998	Burggraaf, P.	Integrated Circuit Engineering Corporation
Semiconductor Packaging: A DoD Dual Use Technology Assessment Final Report	1997	Unknown	Department of Defense
IC Package Designs and IC Signal Performance	2003	Sean Clark	Fairchild Semiconductor
Design techniques for energy efficient and low-power systems	2000	Paul J.M. Havinga	Multimedia Systems, University of Twente
Roadmaps of Packaging Technology	1997	Eric Bogatin	Integrated Circuit Engineering Corporation
Microelectronic Circuits	1991 (3d ed.)	Sedra, Adel et al.	Saunders College Publishing
The Analysis and Design of Linear Circuits	1994	Thomas et al.	Prentice Hall
Parasitic pads	Aug. 17, 2000	Howard Johnson	EDN
A Practical Guide to High-Speed Printed-Circuit-Board Layout	Sep. 2005	John Adrizzoni	Analog Dialogue
Printed Circuit Board Design Techniques for DS40MB200	Oct. 2005	TK Chin	National Semiconductor
Microvias effect on high-frequency signal integrity	Sep. 2002	H Holden	Circuit World (Emerald Insight)
JP2003-273525	Sep. 26, 2003	T Inoue	JPO
Discontinuity impacts and design considerations of high speed differential signals in FC-PBGA packages with high wiring density	2005	N Na et al.	IEEE
PM8358 QuadPHY® 10GX Data Sheet	Nov. 2005	Unknown	PMC-Sierra
Simulation and Measurement of High Speed Serial Link Performance in a Dense, Thin Core Flip Chip Package	May 30, 2006	M. Rolands et al.	IEEE

Microelectronic Circuits	1991	Sedra et al.	Saunders College Publishing
U.S. Patent Pub. 2005/0011676	Jan. 20, 2005	Barr et al.	USPTO
U.S. Patent Pub. 2005/0037601	Feb. 17, 2005	Hsu et al.	USPTO
Single-Chip 4 500-MBd CMOS Transceiver	Dec. 1996	Widmer et al.	IEEE
Final Report for the 10 to 100 Gigabit/Second Networking Laboratory Directed Research and Development Project	Apr. 2001	Witzke et al.	Sandia National Labs.

3. Prior Art Systems Under 35 U.S.C. §§ 102(a), (b), (g).

Defendants identify the systems disclosed in the patents and publications listed above as prior art. Additionally, Defendants identify the following systems, including constituent software, hardware, methods, and processes, as prior art that may anticipate or render obvious the asserted claims of the ’269 Patent. Each system (1) was known or used in this country before the alleged invention of the claimed subject matter of the ’269 patent, (2) was in public use and/or on sale in this country more than one year before the filing date of the application for the ’269 patent and/or (3) was invented and not abandoned, suppressed or concealed prior to the alleged invention of the ’269 patent.

System or Product	Seller/ Purchaser/ User
MC92600	Motorola
PM63252 RSE-160	PMC-Sierra (now Microchip)
Amazon (F751807) product	Cisco
PPE2CR (F751841) product	Cisco
SantaCruz (F751697) product	Cisco
VTXP48 product	TranSwitch

UltraSPARC III Cheetah+ SME1052	Sun Microsystems

Discovery has not yet started, and Defendants will provide further identification of the above systems and any other systems Defendants learn about through discovery ("the '269 Patent Prior Art Systems"), including constituent software, hardware, methods, and processes, as prior art that may anticipate or render obvious the asserted claims of the '269 patent, as such information becomes available. Defendants anticipate third-party discovery may be necessary to obtain that information. Defendants are still investigating each of these systems and reserve the right to amend and supplement these contentions to provide disclosures based on further discovery and investigation related to these systems as the case progresses.

4. Invalidity Under 35 U.S.C. § 103.

In addition to certain claims being anticipated, the Asserted Claims are also invalid as obvious over the same teachings identified for anticipation and various combinations of the references as shown in the claim charts accompanying these contentions for at least the reasons set forth in the accompanying claim charts.

To the extent not anticipated, the Asserted Claims represent no more than the result of ordinary implementation of the prior art and no Asserted Claim goes beyond combining familiar elements in known methods to achieve predictable results or does more than choose between clear alternatives known to those of skill in the art. Indeed, the '269 patent expressly discloses that most, if not all, of the features claimed in the Asserted Claims were well known to one of ordinary skill in the art.

Though the claim charts (Appendices B1–B10) identify particular exemplary obviousness combinations, Defendants' obviousness defenses are not limited to these combinations. Additional exemplary obviousness combinations on which Defendants rely are provided in the summary table

in Section III.A.6 below. The identified prior art references are analogous art and generally directed toward substrate designs. *See Comaper*, 596 F.3d at1350–51. But more than that, they are complete systems designed in very similar ways to each other, to design effective substrates for routing signals to and from integrated circuits and other circuit elements.

Moreover, one of ordinary skill in the art would have combined familiar elements according to known methods to predictably achieve the claimed invention. *KSR*, 127 S. Ct. at 1740. Likewise, one of ordinary skill in the art, at the time of the alleged invention, would recognize that similar well-known substrate designs could have been improved in similar ways, and would have applied those improvements in the same way to predictably achieve the claimed invention. *Id*. For at least these reasons, it would have been obvious to a person of skill in the art at the time of the alleged invention of the Asserted Claims to combine the various references cited herein to practice the Asserted Claims and there is a motivation in the art to make such a combination.

A person of ordinary skill in the art would have found it obvious to design cutouts in metal layers over signal pads in order to reduce parasitic capacitance between the signal pads and the metal in parallel layers. For example, a person of ordinary skill in the art would have been motivated to combine any of the prior art references with any one of the other references that disclose the use of cutouts to render obvious the asserted claims, including, for example, Chin, Inoue, Fazelpour, Morrison, Holden, and PM6352. Alternatively, a person of ordinary skill in the art would have found it obvious to look to these related references as sources of available design choices that the person of ordinary skill in the art would have found obvious to try and would have understood how to do so. A person of ordinary skill in the art would have a good expectation of success, as many similar designs had been proposed, tested, and used in the industry. Further, design tools at the relevant time would have allowed a person of ordinary skill in the art to design

the various cutout sizes and arrangements and perform accurate simulations of how the new design would function. This ability to simulate designs would have increased the expectation of success in implementing the design elements described in the prior art.

The independent claims recite an arrangement of contact pads and associated cutouts within a substrate. The dependent claims recite details a POSITA would have understood as ordinary design choices or common uses.

For example, claim 14 recites rows of transmit and receive pads/contacts. A POSITA would have understood a common signal type for an integrated circuit package is a transmit or receive signal to allow the integrated circuit to communicate with another circuit. Transmit and receive signals transfer data out of or into an IC thus allowing that IC to communicate with other components in a system. Other components might include, for example, a network adapter for communicating with other systems or a central processing unit requesting or producing data communicated over the network. One specific class of components with rows of transmit and receive pins were SERDES (serializer/deserializer) chips. SERDES chips included at least one set of pins for inputting parallel data (*i.e.*, many simultaneous data bits on multiple "parallel" lines) to be converted to a serial format (*i.e.*, a single stream of data bits serially streaming over one line or a matched pair of differential lines) for transmission by the SERDES and at least one set of pins for outputting parallel data converted from a serial format received by the SERDES. A POSITA would also have understood that contact pads in integrated circuits are arranged in rows, especially in BGA packages. Examples of SERDES references include MC92600, PM6352, and Wu.

In another example, claim 6 requires the second layer to be a routing layer. A POSITA would have understood that metal layers with routing traces are commonly used in integrated circuit packages and the ordering of layers to be an ordinary design choice. Ground and reference

layers may distribute power to ICs in the package and they may also be used as shielding to reduce crosstalk, or interference, between signal lines on the same or on other layers, or with other components. Routing traces in metal layers distribute signals between ICs within the package and connect IC signal pads with package ball pads. This routing becomes increasingly complex as the number of signal lines increases, which is the case with ever larger BGA packages. A POSITA would understand the need to consider using the second metal layer to be a routing layer to maximize routing flexibility within the substrate. Examples of routing layer references include, HighSpeed, PM6352, and Alcoe.

In yet another example, claim 3 recites cutouts having the same dimensions as the ball pads. A POSITA would have understood the cutouts could be sized smaller than, equal to, or larger than the ball pads to tune the impedance by reducing parasitic capacitance. As explained in technology background of Defendants' IPR petition, the amount of parasitic capacitance is determined in part by the overlapping area between the ball pads and metal in a parallel metal layer. Thus, cutouts sized smaller than the ball pads will reduce, but not eliminate parasitic capacitance. Cutouts sized identically to the ball pads will nearly eliminate parasitic capacitance, but some so-called "edge capacitance" may remain. A POSITA would also understand that cutouts reduce shielding between layers. Thus, a POSITA would understand that the size of the cutouts represents a design tradeoff and would have been equipped to try different cutout sizes and simulate or test the effects of reduction in parasitic capacitance versus increased interference or crosstalk. Examples of same-size references include Oggioni and PM6352.

Because these design choices or uses were so common and ordinary, authors of academic and industry publications and those making patent disclosures rarely explained them in detail.

Defendants reserve the right to further specify the motivations to combine the prior art in

response to positions that Bell Semic may take later in this case and as discovery, including third party discovery, proceeds. Defendants may rely on any and all portions of the prior art, other documents, and expert testimony to establish that a person of ordinary skill in the art would have been motivated to modify or combine the prior art and his/her knowledge to render the claims invalid as obvious.

5. Invalidity Under 35 U.S.C. § 112.

Defendants assert that claims 1, 4, 7, and 10 (and claims 3, 6, and 11–14, which depend from claims 1 and 10, respectively) of the '269 patent are invalid for failure to meet the requirements of 35 U.S.C. § 112(a). In particular, claims 1, 4, 7, and 10 are invalid because the phrase "substantially no overlap," viewed in light of the specification and prosecution history, fails to inform those skilled in the art about the scope of the invention with reasonable certainty.

Defendants assert that claims 10 and 11 (and claims 12–14, which depend from claim 10) of the '269 patent are invalid for failure to meet the requirements of 35 U.S.C. § 112(b). In particular, claim 10 recites the phrase "electrically insulating areas," and claim 11 recites "forming a plurality of rows of cutouts … each of the cutouts enclosing one of the electrically insulating areas." These claims are invalid as indefinite because the claims, viewed in light of the specification and prosecution history, fail to inform those skilled in the art as to the scope of the purported invention with reasonable certainty.

6. Summary of '269 Patent Invalidity

The following table summarizes Defendants' invalidity contentions related to the '269 patent, as set forth in this document and Appendices B1–B10.

Invalidity Grounds	Asserted Claims
35 U.S.C. § 112	1, 3, 4, 6, 7, 10–14
35 U.S.C. § 103 – Chin	1, 3, 4, 6, 7, 10–14

35 U.S.C. § 103 – PM6352	1, 3, 4, 6, 7, 10–14
35 U.S.C. § 103 – Inoue	1, 3, 4, 6, 7, 10–14
35 U.S.C. § 103 – Fazelpour	1, 3, 4, 6, 7, 10–14
35 U.S.C. § 103 – Holden	1, 3, 4, 6, 7, 10–14
35 U.S.C. § 103 combination of one or more of {Chin, PM6352, Inoue, Fazelpour, Holden} with one or more of {HighSpeed, PM6352, Alcoe}	12
35 U.S.C. § 103 combination of one or more of {Chin, PM6352, Inoue, Fazelpour, Holden} with one or more of {Oggioni, PM6352}	3

C. U.S. Patent No. 6,743,669

1. Prior Art Patents Under 35 U.S.C. §§ 102(a), (b), (e), (g).

Number	Country	Date of Issue	Date of Application
U.S. Patent No. 6,586,311 (Wu)	United States	Jul. 1, 2003	Apr. 25, 2001
U.S. Patent No. 6,277,683 (Pradeep)	United States	Aug. 21, 2001	Feb. 28, 2000
U.S. Patent No. 6,586,332 (Lee)	United States	Jul. 1, 2003	Oct. 16, 2001
U.S. Patent No. 6,348,389 (Chou)	United States	Feb. 19, 2002	Mar. 11, 1999
U.S. Patent No. 6,620,732 (Schuegraf)	United States	Sep. 16, 2003	Nov. 17, 2000
U.S. Patent No. 6,797,554 (Katayama)	United States	Sep. 28, 2004	Mar. 21, 2002
U.S. Patent No. 6,905,968 (Hseih)	United States	Jun. 14, 2005	Dec. 12, 2001
Korean Patent No. KR100768047B1 (Park)	South Korea	Nov. 30, 2005	Oct. 18, 2007

2. Prior Art Publications Under 35 U.S.C. §§ 102(a), (b), (e), (g).

Title	Date of Publication	Author(s)	Publisher
JP2001144287 (Konishi)	May 25, 2001	Konishi et al.	JPO
JP2001250869 (Fukui)	Sep. 14, 2001	Fukui	JPO
KR20020041581 (Yon)	Jun. 3, 2002	Yon et al.	KPO

US2003/0012925 (Gorrell)	Jan. 16, 2003	Gorell	USPTO

3. Prior Art Systems Under 35 U.S.C. §§ 102(a), (b), (g).

Defendants identify the systems disclosed in the patents listed above as prior art. These systems, including constituent software, hardware, methods, and processes, as prior art that may anticipate or render obvious the asserted claims of the '669 patent. Each system (1) was known or used in this country before the alleged invention of the claimed subject matter of the '669 patent, (2) was in public use and/or on sale in this country more than one year before the filing date of the application for the '669 patent and/or (3) was invented and not abandoned, suppressed or concealed prior to the alleged invention of the '669 patent.

Discovery has not yet started, and Defendants will provide further identification of the above systems and any other systems Defendants learn about through discovery ("the '669 Patent Prior Art Systems"), including constituent software, hardware, methods, and processes, as prior art that may anticipate or render obvious the asserted claims of the '669 patent, as such information becomes available. Defendants anticipate third-party discovery may be necessary to obtain that information. Defendants are still investigating these systems and reserve the right to amend and supplement these contentions to provide disclosures based on further discovery and investigation related to these systems as the case progresses.

4. Invalidity Under 35 U.S.C. § 103.

In addition to the claims being anticipated, the Asserted Claims are also invalid as obvious over the same teachings identified for anticipation and various combinations of the references as shown in the claim charts accompanying these contentions for at least the reasons set forth in the accompanying claim charts.

To the extent not anticipated, the Asserted Claims represent no more than the result of

ordinary implementation of the prior art and no Asserted Claim goes beyond combining familiar elements in known methods to achieve predictable results or does more than choose between clear alternatives known to those of skill in the art.

Though the claim charts (Appendices C1–C5) identify particular exemplary obviousness combinations, Defendants' obviousness defenses are not limited to these combinations. Additional exemplary obviousness combinations on which Defendants rely are provided in the summary table in Section III.E.5 below. The identified prior art references are analogous art and generally directed to forming and utilizing a multi-layer silicide blocking structure for improved protection of areas where silicide is unwanted. *See Comaper*, 596 F.3d at 1350–51. Because the references are so similar to each other and to the alleged invention of the '669 patent, it would have been obvious and routine for an ordinarily skilled artisan to combine any of their elements with one another. One of ordinary skill in the art would have also been motivated to combine the identified prior art references based on the references themselves; the common knowledge of one of ordinary skill in the art; the implied and inherent teachings of the prior art as a whole, and the nature of the problems allegedly addressed by the '669 patent and the prior art.

Moreover, one of ordinary skill in the art would have combined familiar elements according to known methods to predictably achieve the claimed invention. *KSR*, 127 S. Ct. 1727, 1740. Likewise, one of ordinary skill in the art, at the time of the alleged invention, would have recognized that similar well-known silicide techniques and structures could have been improved in similar ways, and would have applied those improvements in the same way to predictably achieve the claimed invention. *Id*. at 1740. For at least these reasons, it would have been obvious to a person of skill in the art at the time of the alleged invention of the Asserted Claims to combine the various references cited herein to practice the Asserted Claims and there is a motivation in the

art to make such a combination.

A person of ordinary skill in the art would have been motivated to try or incorporate the order in which a block mask and oxide film are removed. For example, a person of ordinary skill in the art would have been motivated to combine any reference with any one of the other references that discloses when a block mask is removed including, for example, Pradeep and Aloni. A person of ordinary skill in the art would not have perceived any technical obstacle to the proposed combination and would have a reasonable expectation of success because the proposed combination arranges known elements with each performing the same function it has been known to perform. Moreover, a person of ordinary skill in the art would have relied upon known techniques to make the proposed combination to yield a predictable result. A person of ordinary skill in the art would have found the proposed combinations obvious because the combinations involve a simple substitution of one known limitation for another to obtain a predictable result. A person of ordinary skill in the art would have found the proposed combination obvious to try because the person would have been choosing from a finite number of identified, predictable solutions with a reasonable expectation of success. All references would have been readily accessible to a person of ordinary skill in the art because they are from the same field of endeavor. A person of ordinary skill in the art would have had a strong motivation to combine the references based on the person of ordinary skill in the art's knowledge, design incentives, market forces, common sense and/or the disclosure in the references.

A person of ordinary skill in the art would have been motivated to use the silicide techniques and structures of the identified references with resistors and poly resistors. For example, a person of ordinary skill in the art would have been motivated to combine any reference with any one of the other references that discloses blocking silicide formation on resistors, for example, Lee

and Katayama. A person of ordinary skill in the art would not have perceived any technical obstacle to the proposed combination, and would have had a reasonable expectation of success because the proposed combination arranges known elements with each performing the same function it has been known to perform. A person of ordinary skill in the art would not have perceived any technical obstacle to the proposed combination, and would have had a reasonable expectation of success because the proposed combination arranges known elements with each performing the same function it has been known to perform. For example, a person of ordinary skill in the art would understand the silicide techniques and structures that block silicide formation on integrated circuit elements could be also be used to block silicide formation on passive elements, including resistors and poly resistors, to maintain the resistive properties of those elements. There are only a few types of devices for which selective silicide formation and silicide blocking is beneficial. A person of ordinary skill in the art would have had a reasonable expectation of success in using the silicide formation techniques and structures for passive elements, as such techniques were commonly used. Thus, it would be obvious for a person of ordinary skill in the art to try using silicide blocking techniques on passive elements for which maintaining resistive properties is beneficial.

Defendants reserve the right to further specify the motivations to combine the prior art in response to positions that Bell Semic may take later in this case and as discovery, including third party discovery, proceeds. Defendants may rely on any and all portions of the prior art, other documents, and expert testimony to establish that a person of ordinary skill in the art would have been motivated to modify or combine the prior art and his/her knowledge to render the claims invalid as obvious.

5. Invalidity Under 35 U.S.C. § 112.

Defendants assert that claim 1 (and claims 2, 3, 5–7,9, which depend therefrom) of the '669 patent is invalid for failure to meet the requirements of 35 U.S.C. § 112(b). In particular, claim 1 is invalid because the phrases "selected areas," "semiconductor wafer," "block dielectric layer," "a block mask over the wafer," "divide the mask into masked areas over the selected areas," "unmasked areas left exposed," "the selected areas including at least one resistor," "used as an etch stop layer," "removing said block mask," "exposed portions of the oxide film," "after removing said block mask to expose at least one silicon area" are indefinite. These phrases, viewed in light of the specification and prosecution history, fail to inform those skilled in the art about the scope of the invention with reasonable certainty. These phrases are also not supported by written description in the specification of the '669 patent as required by 35 U.S.C. § 112(a).

Defendants assert that claim 2 of the '669 patent is invalid for failure to meet the requirements of 35 U.S.C. § 112(b). In particular, claim 2 is invalid because the phrase "polysilicon area" is indefinite. This phrase, viewed in light of the specification and prosecution history, fails to inform those skilled in the art about the scope of the invention with reasonable certainty. This phrase is also not supported by written description in the specification of the '669 patent as required by 35 U.S.C. § 112(a).

Defendants assert that claim 3 of the '669 patent is invalid for failure to meet the requirements of 35 U.S.C. § 112(b). In particular, claim 3 is invalid because the phrase "poly resistor" is indefinite. This phrase, viewed in light of the specification and prosecution history, fails to inform those skilled in the art about the scope of the invention with reasonable certainty. This phrase is also not supported by written description in the specification of the '669 patent as required by 35 U.S.C. § 112(a).

Defendants assert that claim 5 of the '669 patent is invalid for failure to meet the requirements of 35 U.S.C. § 112(b). In particular, claim 5 is invalid because the phrase "ranges from about 50 to about 100 Angstroms in thickness" is indefinite. This phrase, viewed in light of the specification and prosecution history, fails to inform those skilled in the art about the scope of the invention with reasonable certainty. This phrase is also not supported by written description in the specification of the '669 patent as required by 35 U.S.C. § 112(a).

Defendants assert that claim 6 of the '669 patent is invalid for failure to meet the requirements of 35 U.S.C. § 112(b). In particular, claim 6 is invalid because the phrase "one of a low temperature oxide film and TEOS oxide" is indefinite. This phrase, viewed in light of the specification and prosecution history, fails to inform those skilled in the art about the scope of the invention with reasonable certainty. This phrase is also not supported by written description in the specification of the '669 patent as required by 35 U.S.C. § 112(a).

Defendants assert that claim 7 of the '669 patent is invalid for failure to meet the requirements of 35 U.S.C. § 112(b). In particular, claim 7 is invalid because the phrase "ranges from about 100 to about 500 Angstroms in thickness" is indefinite. This phrase, viewed in light of the specification and prosecution history, fails to inform those skilled in the art about the scope of the invention with reasonable certainty. This phrase is also not supported by written description in the specification of the '669 patent as required by 35 U.S.C. § 112(a).

Defendants assert that claim 9 of the '669 patent is invalid for failure to meet the requirements of 35 U.S.C. § 112(b). In particular, claim 9 is invalid because the phrase "the forming of a block mask over the selected areas of the semiconductor wafer depositing a photoresist layer" is indefinite. This phrase, viewed in light of the specification and prosecution history, fails to inform those skilled in the art about the scope of the invention with reasonable

certainty. This phrase is also not supported by written description in the specification of the ’669 patent as required by 35 U.S.C. § 112(a).

6. Summary of ’669 Patent Invalidity

The following table summarizes Defendants’ invalidity contentions related to the ’669 patent, as set forth in this document and Appendices C1–C5.

Invalidity Grounds	Asserted Claims
35 U.S.C. § 112	1–3, 5–7, 9
35 U.S.C. § 102 – U.S. Patent No. 6,586,311 (Wu)	1–3, 5–7, 9
35 U.S.C. § 102 – U.S. Patent No. 6,797,554 (Katayama)	1–3, 5–7, 9
35 U.S.C. § 102 – U.S. Patent No. 6,277,683 (Pradeep)	1–3, 5–7, 9
35 U.S.C. § 102 – U.S. Patent No. 6,458,702 (Aloni)	1–3, 5–7, 9
35 U.S.C. § 102 – U.S. Patent No. 6,586,332 (Lee)	1–3, 5–7, 9
35 U.S.C. § 103 – U.S. Patent No. 6,586,311 (Wu) alone or in combination with one or more of: the knowledge of one of ordinary skill in the art; Katayama; Pradeep; Aloni; and Lee.	1–3, 5–7, 9
35 U.S.C. § 103 – U.S. Patent No. 6,797,554 (Katayama) alone or in combination with one or more of: the knowledge of one of ordinary skill in the art; Wu; Pradeep; Aloni; and Lee.	1–3, 5–7, 9
35 U.S.C. § 103 – U.S. Patent No. 6,277,683 (Pradeep) alone or in combination with one or more of: the knowledge of one of ordinary skill in the art; Wu; Katayama; Aloni; and Lee.	1–3, 5–7, 9
35 U.S.C. § 103 – U.S. Patent No. 6,458,702 (Aloni) alone or in combination with one or more of: the knowledge of one of ordinary skill in the art; Wu; Katayama; Pradeep; and Lee.	1–3, 5–7, 9
35 U.S.C. § 103 – U.S. Patent No. 6,586,332 (Lee) alone or in combination with one or more of: the knowledge of one of ordinary skill in the art; Wu; Katayama; Pradeep; and Aloni.	1–3, 5–7, 9

D. U.S. Patent No. 7,221,173

1. Prior Art Patents Under 35 U.S.C. §§ 102(a), (b), (e), (g).

Number	Country	Date of Issue	Date of Application

U.S. Patent No. 6,869,809 (Yu)	United States	Mar. 22, 2005	May 28, 2003
U.S. Patent No. 7,235,412 (Mardi)	United States	Jun. 26, 2007	May 11, 2004
U.S. Patent No. 6,765,228 (Lin)	United States	Jul. 20, 2004	Oct. 11, 2002
U.S. Patent No. 5,550,480 (Nelson)	United States	Aug. 27, 1996	Jul. 5, 1994
U.S. Patent No. 6,744,067 (Farnworth)	United States	Jun. 1, 2004	Jan. 17, 2003
U.S. Patent No. 6,597,187 (Eldridge)	United States	Jul. 22, 2003	Dec. 29, 2000
U.S. Patent No. 6,392,301 (Waizman)	United States	May 21, 2002	Oct. 25, 1999
U.S. Patent No. 6,359,342 (Yuan)	United States	Mar. 19, 2002	Dec. 5, 2000
U.S. Patent No. 5,554,940 (Hubacher)	United States	Sep. 10, 1996	Jul. 5, 1994
U.S. Patent No. 7,394,161 (Kuo)	United States	Jul. 1, 2008	Dec. 8, 2003

2. Prior Art Publications Under 35 U.S.C. §§ 102(a), (b), (e), (g).

Title	**Date of Publication**	**Author(s)**	**Publisher**
U.S. Patent Publication No. 2003/0094966 (Fang)	May 22, 2003	Jen-Kuang Fang	U.S. Patent Office
U.S. Patent Publication No. 2003/0173667 (Yong-667)	Sep. 18, 2003	Yong et al.	U.S. Patent Office
U.S. Patent Application Publication 2005/0037601 (Hsu)	Feb. 17, 2005	Hsu et al.	U.S. Patent Office
U.S. Pat. Pub. No. 2002/0093106 (Krishnamoorthy)	Jul. 18, 2002	Krishnamoorthy et al.	U.S. Patent Office
Novel Method of Separating Probe and Wire Bond Regions Without Increasing Die Size (Yong)	Aug. 2003	Yong	IEEE
JP 2002-329742 A (Narutaki)	Nov. 15, 2002	Kiichi Narutaki et al	Japanese Patent Office

3. Prior Art Systems Under 35 U.S.C. §§ 102(a), (b), (g).

Defendants identify the systems disclosed in the patents and publications listed above as prior art. These systems, including constituent software, hardware, methods, and processes, as prior art that may anticipate or render obvious the asserted claims of the '173 patent. Each system (1) was known or used in this country before the alleged invention of the claimed subject matter of the '173 patent, (2) was in public use and/or on sale in this country more than one year before the filing date of the application for the '173 patent and/or (3) was invented and not abandoned, suppressed or concealed prior to the alleged invention of the '173 patent.

Discovery has not yet started, and Defendants will provide further identification of the above systems and any other systems Defendants learn about through discovery ("the '173 Patent Prior Art Systems"), including constituent software, hardware, methods, and processes, as prior art that may anticipate or render obvious the asserted claims of the '173 patent, as such information becomes available. Defendants anticipate third-party discovery may be necessary to obtain that information. Defendants are still investigating these systems and reserve the right to amend and supplement these contentions to provide disclosures based on further discovery and investigation related to these systems as the case progresses.

4. Invalidity Under 35 U.S.C. § 103.

In addition to certain claims being anticipated, the Asserted Claims are also invalid as obvious over the same teachings identified for anticipation and various combinations of the references as shown in the claim charts accompanying these contentions for at least the reasons set forth in the accompanying claim charts.

To the extent not anticipated, the Asserted Claims represent no more than the result of ordinary implementation of the prior art and no Asserted Claim goes beyond combining familiar elements in known methods to achieve predictable results or does more than choose between clear

alternatives known to those of skill in the art. Indeed, the '173 patent expressly discloses that most, if not all, of the features claimed in the Asserted Claims were well known to one of ordinary skill in the art.

Though the claim charts (Appendices D1–D9) identify particular exemplary obviousness combinations, Defendants' obviousness defenses are not limited to these combinations. Additional exemplary obviousness combinations on which Defendants rely are provided in the summary table in Section III.D.6 below. The identified prior art references are analogous art and generally directed to packaging of semiconductor devices. *See Comaper*, 596 F.3d at 1350–51. Because the references are so similar to each other and to the alleged invention of the '173 patent, it would be obvious and routine for an ordinarily skilled artisan to combine any of their elements with one another. One of ordinary skill in the art would have also been motivated to combine the identified prior art references based on the references themselves; the common knowledge of one of ordinary skill in the art; the implied and inherent teachings of the prior art as a whole; and the nature of the problems allegedly addressed by the '173 patent and the prior art.

Moreover, one of ordinary skill in the art would have combined familiar elements according to known methods to predictably achieve the claimed invention. *KSR*, 127 S. Ct. 1727, 1740. Likewise, one of ordinary skill in the art, at the time of the alleged invention, would recognize that similar well-known packaging of semiconductor devices could have been improved in similar ways, and would have applied those improvements in the same way to predictably achieve the claimed invention. *Id.* at 1740. For at least these reasons, it would have been obvious to a person of skill in the art at the time of the alleged invention of the Asserted Claims to combine the various references cited herein to practice the Asserted Claims and there is a motivation in the art to make such a combination.

A person of ordinary skill in the art would have found it obvious to perform wafer-level testing. For example, a person of ordinary skill in the art would have been motivated to combine any of the prior art references with any one of the other references that disclose a wafer-level test to render them obvious, including, for example, Mardi. Alternatively, a person of ordinary skill in the art would have found it obvious to perform wafer-level testing (as opposed to testing one chip at a time) because it reduces manufacturing costs and manufacturing time. For example, U.S. Patent No. 5,550,480 to Nelson et al. was filed in 1994 (over 10 years before the '173 patent), and shows that a person of ordinary skill in the art would have knowledge of the benefits of testing semiconductor devices at the wafer level. *See also* U.S. Patent No. 6,744,067 at [57], 1:23–49 ("wafer level testing" of wafer comprising flip-chip type semiconductor chips); U.S. Patent No. 6,597,187 at 1:18–27, 6:42–46 (wafer-level testing of flip chips), U.S. Patent No. 6,869,809 at [57]. These references confirm that wafer-level testing was well-known in the art and a person of ordinary skill in the art would have had a reasonable expectation of success of combining these teachings with other prior art references.

A person of ordinary skill in the art would have found it obvious to use an integrally formed bonding pad and test pad. For example, a person of ordinary skill in the art would have been motivated to combine any of the prior art references with one of the other references that disclose an integrally formed bonding pad and test pad without separate interconnecting lines therebetween. First, an integrally formed bonding pad and test pad without separate interconnecting lines therebetween was well-known, as evidenced by other charted references such as Mardi, Lin, Yong, Kuo, and Narutaki. These references are in the same technological field, and have very similar disclosures. Second, person of ordinary skill in the art would have been motivated to form the bonding pad and test pad integrally as taught by these other references to more efficiently produce

the bonding pad and test pad from a single metal layer. Third, a person of ordinary skill in the art would have recognized that an integrally formed bonding pad and test pad was a known substitution for any separately formed bonding and test pads with interconnecting lines therebetween. A person of ordinary skill in the art would have a good expectation of success, as such a successful manner of producing bonding and test pads was well-known as shown by the other charted references.

Defendants reserve the right to further specify the motivations to combine the prior art in response to positions that Bell Semic may take later in this case and as discovery, including third party discovery, proceeds. Defendants may rely on any and all portions of the prior art, other documents, and expert testimony to establish that a person of ordinary skill in the art would have been motivated to modify or combine the prior art and his/her knowledge to render the claims invalid as obvious.

5. Invalidity Under 35 U.S.C. § 112.

Defendants assert that claim 9 of the '173 patent is invalid for failure to meet the requirements of 35 U.S.C. § 112(b). In particular, claim 9 recites the phrases "region" and "probe region" that do not connote sufficiently definite structure and therefore implicate 35 U.S.C. § 112(f). The '173 patent specification and file history also fail to link sufficient structure to these phrases, rendering these terms indefinite.

Defendants assert that claim 9 of the '173 patent is invalid for failure to meet the requirements of 35 U.S.C. § 112(b). In particular, claim 9 is invalid because the phrases "integrally constructing," "integral conductive structure," "separate," "wafer test," and "probe region for performing a wafer test prior to performing said bumping process" are indefinite. These phrases, viewed in light of the specification and prosecution history, fails to inform those skilled in the art about the scope of the invention with reasonable certainty.

6. Summary of '173 Patent Invalidity

The following table summarizes Defendants' invalidity contentions related to the '173 patent, as set forth in this document and Appendices D1–D9.

Invalidity Grounds	Asserted Claims
35 U.S.C. § 112	9
35 U.S.C. § 102 – U.S. Patent No. 6,869,809 (Yu)	9
35 U.S.C. § 102 – U.S. Patent No. 7,235,412 (Mardi)	9
35 U.S.C. § 102 – U.S. Patent No. 6,765,228 (Lin)	9
35 U.S.C. § 102 – U.S. Patent No. 6,359,342 (Yuan)	9
35 U.S.C. § 102 – U.S. Patent No. 5,554,940 (Hubacher)	9
35 U.S.C. § 102 – U.S. Patent No. 7,394,161 (Kuo)	9
35 U.S.C. § 102 – JP 2002-329742 A (Narutaki)	9
35 U.S.C. § 102 – U.S. Patent Publication No. 2003/0173667 (Yong-667)	9
35 U.S.C. § 102 – U.S. Pat. Pub. No. 2002/0093106 (Krishnamoorthy)	9
35 U.S.C. § 103 – U.S. Patent No. 6,869,809 (Yu) alone or in combination with one or more of: the knowledge of one of ordinary skill in the art; Mardi; Lin; Nelson; Farnworth; Eldridge; Waizman; Yuan; Hubacher; Kuo; Fang; Yong-667; Hsu; Krishnamoorthy; Yong; and Narutaki.	9
35 U.S.C. § 103 – U.S. Patent No. 7,235,412 (Mardi) alone or in combination with one or more of: the knowledge of one of ordinary skill in the art; Yu; Lin; Nelson; Farnworth; Eldridge; Waizman; Yuan; Hubacher; Kuo; Fang; Yong-667; Hsu; Krishnamoorthy; Yong; and Narutaki.	9
35 U.S.C. § 103 – U.S. Patent No. 6,765,228 (Lin) alone or in combination with one or more of: the knowledge of one of ordinary skill in the art; Yu; Mardi; Nelson; Farnworth; Eldridge; Waizman; Yuan; Hubacher; Kuo; Fang; Yong-667; Hsu; Krishnamoorthy; Yong; and Narutaki.	9
35 U.S.C. § 103 – U.S. Patent No. 6,359,342 (Yuan) alone or in combination with one or more of: the knowledge of one of ordinary skill in the art; Yu; Mardi; Lin; Nelson; Farnworth;	9

Eldridge; Waizman; Hubacher; Kuo; Fang; Yong-667; Hsu; Krishnamoorthy; Yong; and Narutaki.	
35 U.S.C. § 103 – U.S. Patent No. 5,554,940 (Hubacher) alone or in combination with one or more of: the knowledge of one of ordinary skill in the art; Yu; Mardi; Lin; Nelson; Farnworth; Eldridge; Waizman; Yuan; Kuo; Fang; Yong-667; Hsu; Krishnamoorthy; Yong; and Narutaki.	9
35 U.S.C. § 103 – U.S. Patent No. 7,394,161 (Kuo) alone or in combination with one or more of: the knowledge of one of ordinary skill in the art; Yu; Mardi; Lin; Nelson; Farnworth; Eldridge; Waizman; Yuan; Hubacher; Fang; Yong-667; Hsu; Krishnamoorthy; Yong; and Narutaki.	9
35 U.S.C. § 103 – JP 2002-329742 A (Narutaki) alone or in combination with one or more of: the knowledge of one of ordinary skill in the art; Yu; Mardi; Lin; Nelson; Farnworth; Eldridge; Waizman; Yuan; Hubacher; Kuo; Fang; Yong-667; Hsu; Krishnamoorthy; and Yong.	9
35 U.S.C. § 103 – U.S. Patent Publication No. 2003/0173667 (Yong-667) alone or in combination with one or more of: the knowledge of one of ordinary skill in the art; Yu; Mardi; Lin; Nelson; Farnworth; Eldridge; Waizman; Yuan; Hubacher; Kuo; Fang; Yong-667; Hsu; Krishnamoorthy; Yong; and Narutaki.	9
35 U.S.C. § 103 – U.S. Pat. Pub. No. 2002/0093106 (Krishnamoorthy) alone or in combination with one or more of: the knowledge of one of ordinary skill in the art; Yu; Mardi; Lin; Nelson; Farnworth; Eldridge; Waizman; Yuan; Hubacher; Kuo; Fang; Yong-667; Hsu; Yong; and Narutaki.	9

E. U.S. Patent No. 6,707,132

1. Prior Art Patents Under 35 U.S.C. §§ 102(a), (b), (e), (g).

Number	Country	Date of Issue	Date of Application
U.S. Patent No. 5,498,578 (Steele)	United States	Mar. 12, 1996	May 2, 1994
U.S. Patent No. 6,225,666 (Gadepally)	United States	May 1, 2001	Oct. 29, 1999
U.S. Patent No. 6,559,020 (Salmi)	United States	May 6, 2003	Oct. 20, 1999
U.S. Patent No. 5,633,179 (Kamins)	United States	May 27, 1997	Oct. 11, 1994

U.S. Patent No. 6,784,507 (Wallace)	United States	Aug. 31, 2004	Sep. 27, 2002
U.S. Patent No. 6,861,326 (Gonzalez)	United States	Mar. 1, 2005	Nov. 21, 2001
U.S. Patent No. 6,699,765 (Shideler)	United States	Mar. 2, 2004	Aug. 29, 2002
U.S. Patent No. 6,048,756 (Lee)	United States	Apr. 11, 2000	Jun. 25, 1998
JPH 09-219524 (Hiraoka)	Japan	Jan. 27, 2003	Feb. 9, 2006
U.S. Patent No. 6,800,921 (Coolbaugh)	United States	Oct. 5, 2004	Mar. 1, 2000
U.S. Patent No. 4,885,614 (Furukawa)	United States	Dec. 5, 1989	Jul. 8, 1988
U.S. Patent No. 6,891,209 (Bulsara)	United States	May 10, 2005	Aug. 13, 2002
U.S. Patent No. 5,981,345 (Ryum)	United States	Nov. 9, 1999	Jul. 10, 1997
U.S. Patent No. 6,218,711 (Yu)	United States	Apr. 17, 2001	Feb. 19, 1999
U.S. Patent No. 4,786,828 (Hoffman)	United States	Nov. 22, 1988	May 15, 1987

2. *Prior Art Publications Under 35 U.S.C. §§ 102(a), (b), (e), (g).*

Title	**Date of Publication**	**Author(s)**	**Publisher**
A High Performance Epitaxial I3iGe-Base ECL BiCMOS Technology (Harame 1992)	Dec. 1992	Harame, D.L., et al.	1992 International Technical Digest on Electron Devices Meeting
Si/SiGe Epitaxial-Base Transistors-Part II: Process Integration and Analog Applications (Harame 1995)	March 1995	Harame, D.L., et al.	IEEE Transactions on Electron Devices, Vol. 42, No. 3,
Modular Integration of High-Performance SiGe:C HBTs in a Deep Submicron, Epi-Free CMOS Process (Ehwald)	Dec. 5–8, 1999	Ehwald, K.E., et al.	Technical Digest of the IEEE International Electron Devices Meeting, Washington 1999
Fabrication of a novel strained SiGe:C-channel planar 55nm nMOSFET	2002	Ernst, T., et al.;	2002 Symposium on VLSI Technology Digest of Technical Papers, IEEE

for High-Performance CMOS (Ernst)			
Silicon Processing for the VLSI Era (Wolf)	2000	Wolf, S., et al.	Lattice Press
Microchip Fabrication, A Practical Guide to Semiconductor Processing (Van Zant)	2002 (Fourth Edition)	Peter Van Zant	McGraw-Hill
U.S. Application Publication No. 2002/0117720 (Lee-720)	Aug. 29, 2002	Lee et al.	U.S. Patent Office

3. Prior Art Systems Under 35 U.S.C. §§ 102(a), (b), (g).

Defendants identify the systems disclosed in the patents and publications listed above as prior art. These systems, including constituent software, hardware, methods, and processes, as prior art that may anticipate or render obvious the asserted claims of the '132 patent. Each system (1) was known or used in this country before the alleged invention of the claimed subject matter of the '132 patent, (2) was in public use and/or on sale in this country more than one year before the filing date of the application for the '132 patent and/or (3) was invented and not abandoned, suppressed or concealed prior to the alleged invention of the '132 patent.

Discovery has not yet started, and Defendants will provide further identification of the above systems and any other systems Defendants learn about through discovery ("the '132 Patent Prior Art Systems"), including constituent software, hardware, methods, and processes, as prior art that may anticipate or render obvious the asserted claims of the '132 patent, as such information becomes available. Defendants anticipate third-party discovery may be necessary to obtain that information. Defendants are still investigating these systems and reserve the right to amend and supplement these contentions to provide disclosures based on further discovery and investigation related to these systems as the case progresses.

4. Invalidity Under 35 U.S.C. § 103.

In addition to certain claims being anticipated, the Asserted Claims are also invalid as obvious over the same teachings identified for anticipation and various combinations of the references as shown in the claim charts accompanying these contentions for at least the reasons set forth in the accompanying claim charts.

To the extent not anticipated, the Asserted Claims represent no more than the result of ordinary implementation of the prior art and no Asserted Claim goes beyond combining familiar elements in known methods to achieve predictable results or does more than choose between clear alternatives known to those of skill in the art. Indeed, the '132 patent expressly discloses that most, if not all, of the features claimed in the Asserted Claims were well known to one of ordinary skill in the art.

Though the claim charts (Appendices E1–E17) identify particular exemplary obviousness combinations, Defendants' obviousness defenses are not limited to these combinations. Additional exemplary obviousness combinations on which Defendants rely are provided in the summary table in Section III.E.6 below. The identified prior art references are analogous art and generally directed to electronic semiconductor devices and structures. *See Comaper*, 596 F.3d at 1350–51. But more than that, the majority of these references describe semiconductor devices and structures that include silicon germanium. Because the references are so similar to each other and to the alleged invention of the '132 patent, it would be obvious and routine for an ordinarily skilled artisan to combine any of their elements with one another. One of ordinary skill in the art would have also been motivated to combine the identified prior art references based on the references themselves; the common knowledge of one of ordinary skill in the art; the implied and inherent teachings of the prior art as a whole; and the nature of the problems allegedly addressed by the '132 patent and the prior art.

Moreover, one of ordinary skill in the art would have combined familiar elements according to known methods to predictably achieve the claimed invention. *KSR*, 127 S. Ct. 1727, 1740. Likewise, one of ordinary skill in the art, at the time of the alleged invention, would recognize that similar well-known semiconductor devices and structures could have been improved in similar ways, and would have applied those improvements in the same way to predictably achieve the claimed invention. *Id.* at 1740. For at least these reasons, it would have been obvious to a person of skill in the art at the time of the alleged invention of the Asserted Claims to combine the various references cited herein to practice the Asserted Claims and there is a motivation in the art to make such a combination.

A person of ordinary skill in the art would have been motivated to use a thermal oxide layer. For example, a person of ordinary skill in the art would have been motivated to combine any reference with any one of the other references that discloses thermal oxide to render the use a thermal oxide layer obvious, including, for example, Gadepally, Salmi, Kamins, Wallace, Shideler, Lee, Harame1992, Harame1995, Hiraoka, and Coolbaugh. A person of ordinary skill in the art would not have perceived any technical obstacle to the proposed combination, and would have a reasonable expectation of success because the proposed combination arranges known elements with each performing the same function it has been known to perform. Moreover, a person of ordinary skill in the art would have relied on known techniques to make the proposed combination to yield a predictable result. A person of ordinary skill in the art would have found the proposed combination obvious because the combinations involve a simple substitution of one known limitation for another to obtain a predictable result. A person of ordinary skill in the art would have found the proposed combination obvious to try because the person would have been choosing from a finite number of identified, predictable solutions with a reasonable expectation of success. Both

references would have been readily accessible to a person of ordinary skill in the art because they are from the same field of endeavor. A person of ordinary skill in the art would have a strong motivation to combine the references based on the person of ordinary skill in the art's knowledge, design incentives, market forces, common sense or the disclosure in the references.

A person of ordinary skill in the art would have been motivated use a mask to remove a thermal oxide layer. For example, a person of ordinary skill in the art would understand that removal of a part of a pad oxide would use masking. Such masking is disclosed by several charted references, such as Wallace, Gonzalez, and Coolbaugh. There are only a few ways in which a particular portion of oxide can be removed while leaving some existing portions of the oxide, and masking is the most commonly used technique. A person of ordinary skill in the art would have a reasonable expectation of success in using masking to remove an oxide layer, as such a technique was commonly used. Thus, it would be obvious for a person of ordinary skill in the art to try to remove a pad oxide layer with masking

In another example, a person of ordinary skill in the art would have been motivated to use carbon doping. For example, a person of ordinary skill in the art would have been motivated to combine any reference with any one of the other references that discloses carbon doping to render the asserted claims obvious, including, for example, Ernst, Steele, Shideler, and Van Zant. Ernst discloses integrated circuits with boron doping and Si-Ge channel regions with carbon atoms added. One of ordinary skill in the art would have understood boron is commonly used on portions of transistors such as source, drain, gate, emitter, base, collector, and channels to improve electron mobility and electrical performance, and thus improve the speed of the resulting device. Adding the teachings of Ernst regarding boron dopants, which one of ordinary skill in the art would understand as increasing the speed of the device, and regarding carbon dopants to improve side-

effects of the boron doping such as boron and oxidation enhanced diffusion, would improve devices. The boron and carbon doping disclosed in Ernst were a known technique, and applying this known technique to a device would have had predictable results. One of ordinary skill in the art would have expected the results demonstrated in Ernst to have a similar effect when the doping was applied with a reasonable expectation of success. Steele, Shideler, and Van Zant disclose additional benefits of and motivations for incorporating carbon doping into an SiGe layer, while also confirming that doing so was within the knowledge of a person of ordinary skill in the art. *See* Shideler at 4:19–25 ("The carbon functions to Suppress the out-diffusion of a p-type dopant (Such as boron) that is incorporated in the SiGe layer."); Steele at 1:51–52, 2:20–32, 4:52–55, 6:1–2; Van Zant at 27.

In yet another example, a person of ordinary skill in the art would have been motivated to grow an SiGe layer epitaxially. For example, a person of ordinary skill in the art would have been motivated to combine any reference with any one of the other references that discloses using epitaxial growth to create the SiGe layer. Epitaxial growing the SiGe layer is one of a finite number of identified, predictable solutions for forming the SiGe layer. A person of ordinary skill in the art would understand that forming an SiGe layer through epitaxial growth, such as disclosed in the charted references Wallace, Gonzalez, Shideler, Steele, or Van Zant, could be substituted for another method of the formation of SiGe with a reasonable expectation of success.

Defendants reserve the right to further specify the motivations to combine the prior art in response to positions that Bell Semic may take later in this case and as discovery, including third party discovery, proceeds. Defendants may rely on any and all portions of the prior art, other documents, and expert testimony to establish that a person of ordinary skill in the art would have been motivated to modify or combine the prior art and his/her knowledge to render the claims

invalid as obvious.

5. Invalidity Under 35 U.S.C. § 112.

Defendants assert that claim 5 (and claims 12 and 14, which depend therefrom) of the '132 patent is invalid for failure to meet the requirements of 35 U.S.C. § 112(b). In particular, claim 5 is invalid because the phrases "thermal oxide layer," "depositing Si-Ge on the Silicon substrate," "masking," "silicon substrates," "thermal oxide layer which is disposed on the Silicon substrate," "forming a Si-Ge layer on the exposed portion of the Silicon substrate" are indefinite. These phrases, viewed in light of the specification and prosecution history, fail to inform those skilled in the art about the scope of the invention with reasonable certainty.

Defendants assert that claim 14 of the '132 patent is invalid for failure to meet the requirements of 35 U.S.C. § 112(b). In particular, claim 14 is invalid because the phrase "Si-Ge doped with carbon" is indefinite. The phrase, viewed in light of the specification and prosecution history, fails to inform those skilled in the art about the scope of the invention with reasonable certainty.

Defendants assert that claim 5 (and claims 12 and 14, which depend therefrom) of the '132 patent is invalid for failure to meet the requirements of 35 U.S.C. § 112(a). In particular, claim 5 is invalid because the phrases "further comprising forming a Si-Ge layer on the exposed portion of the Silicon Substrate," "forming a thermal oxide on the Silicon substrate," "thermal oxide layer," "depositing Si-Ge on the Silicon substrate," and "forming a Si—Ge layer on the exposed portion of the Silicon substrate" are not supported by written description in the specification of the '132 patent.

Defendants assert that claim 14 of the '132 patent is invalid for failure to meet the requirements of 35 U.S.C. § 112(a). In particular, claim 14 is invalid because the phrase "Si-Ge doped with carbon" is not supported by written description in the specification of the '132 patent.

6. Summary of '132 Patent Invalidity

The following table summarizes Defendants' invalidity contentions related to the '132 patent, as set forth in this document and Appendices E1–E17.

Invalidity Grounds	Asserted Claims
35 U.S.C. § 112	5, 12, 14
35 U.S.C. § 102 – U.S. Patent No. 5,498,578 (Steele)	5, 12, 14
35 U.S.C. § 102 – U.S. Patent No. 6,225,666 (Gadepally)	5, 12, 14
35 U.S.C. § 102 – U.S. Patent No. 6,559,020 (Salmi)	5, 12, 14
35 U.S.C. § 102 – U.S. Patent No. 5,633,179 (Kamins)	5, 12
35 U.S.C. § 102 – U.S. Patent No. 6,784,507 (Wallace)	5, 12, 14
35 U.S.C. § 102 – U.S. Patent No. 6,861,326 (Gonzalez)	5, 12, 14
35 U.S.C. § 102 – U.S. Patent No. 6,699,765 (Shideler)	5, 12, 14
35 U.S.C. § 102 – U.S. Patent No. 6,048,756 (Lee)	5, 12
35 U.S.C. § 102 – Si/SiGe Epitaxial-Base Transistors-Part II: Process Integration and Analog Applications (Harame 1995)	5, 12
35 U.S.C. § 102 – A High Performance Epitaxial I3iGe-Base ECL BiCMOS Technology (Harame 1992)	5, 12
35 U.S.C. § 102 – U.S. Patent No. 5,981,345 (Ryum)	5, 12, 14
35 U.S.C. § 102 – U.S. Patent No. 6,218,711 (Yu)	5, 12, 14
35 U.S.C. § 102 – U.S. Patent No. 6,800,921 (Coolbaugh)	5, 12
35 U.S.C. § 102 – JPH 09-219524 (Hiraoka)	5, 12, 14
35 U.S.C. § 103 – U.S. Patent No. 5,498,578 (Steele) alone or in combination with one or more of: the knowledge of one of ordinary skill in the art; Gadepally; Salmi; Kamins; Wallace; Gonzalez; Shideler; Lee; Hiraoka; Coolbaugh; Furukawa; Bulsara; Ryum; Yu; Hoffman; Harame 1992; Harame 1995; Ehwald; Ernst; Wolf; Van Zant; and Lee-270.	5, 12, 14
35 U.S.C. § 103 – U.S. Patent No. 6,225,666 (Gadepally) alone or in combination with one or more of: the knowledge of one of ordinary skill in the art; Steele; Salmi; Kamins; Wallace; Gonzalez; Shideler; Lee; Hiraoka; Coolbaugh; Furukawa;	5, 12, 14

Invalidity Grounds	Asserted Claims
Bulsara; Ryum; Yu; Hoffman; Harame 1992; Harame 1995; Ehwald; Ernst; Wolf; Van Zant; and Lee-270.	
35 U.S.C. § 103 – U.S. Patent No. 6,559,020 (Salmi) alone or in combination with one or more of: the knowledge of one of ordinary skill in the art; Steele; Gadepally; Kamins; Wallace; Gonzalez; Shideler; Lee; Hiraoka; Coolbaugh; Furukawa; Bulsara; Ryum; Yu; Hoffman; Harame 1992; Harame 1995; Ehwald; Ernst; Wolf; Van Zant; and Lee-270.	5, 12, 14
35 U.S.C. § 103 – U.S. Patent No. 5,633,179 (Kamins) alone or in combination with one or more of: the knowledge of one of ordinary skill in the art; Steele; Gadepally; Salmi; Wallace; Gonzalez; Shideler; Lee; Hiraoka; Coolbaugh; Furukawa; Bulsara; Ryum; Yu; Hoffman; Harame 1992; Harame 1995; Ehwald; Ernst; Wolf; Van Zant; and Lee-270.	5, 12, 14
35 U.S.C. § 103 – U.S. Patent No. 6,784,507 (Wallace) alone or in combination with one or more of: the knowledge of one of ordinary skill in the art; Steele; Gadepally; Salmi; Kamins; Gonzalez; Shideler; Lee; Hiraoka; Coolbaugh; Furukawa; Bulsara; Ryum; Yu; Hoffman; Harame 1992; Harame 1995; Ehwald; Ernst; Wolf; Van Zant; and Lee-270.	5, 12, 14
35 U.S.C. § 103 – U.S. Patent No. 6,861,326 (Gonzalez) alone or in combination with one or more of: the knowledge of one of ordinary skill in the art; Steele; Gadepally; Salmi; Kamins; Wallace; Shideler; Lee; Hiraoka; Coolbaugh; Furukawa; Bulsara; Ryum; Yu; Hoffman; Harame 1992; Harame 1995; Ehwald; Ernst; Wolf; Van Zant; and Lee-270.	5, 12, 14
35 U.S.C. § 103 – U.S. Patent No. 6,699,765 (Shideler) alone or in combination with one or more of: the knowledge of one of ordinary skill in the art; Steele; Gadepally; Salmi; Kamins; Wallace; Gonzalez; Lee; Hiraoka; Coolbaugh; Furukawa; Bulsara; Ryum; Yu; Hoffman; Harame 1992; Harame 1995; Ehwald; Ernst; Wolf; Van Zant; and Lee-270.	5, 12, 14
35 U.S.C. § 103 – U.S. Patent No. 6,048,756 (Lee) alone or in combination with one or more of: the knowledge of one of ordinary skill in the art; Steele; Gadepally; Salmi; Shideler; Kamins; Wallace; Gonzalez; Hiraoka; Coolbaugh; Furukawa; Bulsara; Ryum; Yu; Hoffman; Harame 1992; Harame 1995; Ehwald; Ernst; Wolf; Van Zant; and Lee-270.	5, 12, 14
35 U.S.C. § 103 – Si/SiGe Epitaxial-Base Transistors-Part II: Process Integration and Analog Applications (Harame 1995) alone or in combination with one or more of: the knowledge of	5, 12, 14

Invalidity Grounds	Asserted Claims
one of ordinary skill in the art; Steele; Gadepally; Salmi; Shideler; Kamins; Wallace; Gonzalez; Lee; Hiraoka; Coolbaugh; Furukawa; Bulsara; Ryum; Yu; Hoffman; Harame 1992; Ehwald; Ernst; Wolf; Van Zant; and Lee-270.	
35 U.S.C. § 103 – A High Performance Epitaxial I3iGe-Base ECL BiCMOS Technology (Harame 1992) alone or in combination with one or more of: the knowledge of one of ordinary skill in the art; Steele; Gadepally; Salmi; Shideler; Kamins; Wallace; Gonzalez; Lee; Hiraoka; Coolbaugh; Furukawa; Bulsara; Ryum; Yu; Hoffman; Harame 1995; Ehwald; Ernst; Wolf; Van Zant; and Lee-270.	5, 12, 14
35 U.S.C. § 103 – U.S. Patent No. 5,981,345 (Ryum) alone or in combination with one or more of: the knowledge of one of ordinary skill in the art; Steele; Gadepally; Salmi; Shideler; Kamins; Wallace; Gonzalez; Lee; Hiraoka; Coolbaugh; Furukawa; Bulsara; Yu; Hoffman; Harame 1992; Harame 1995; Ehwald; Ernst; Wolf; Van Zant; and Lee-270.	5, 12, 14
35 U.S.C. § 103 – U.S. Patent No. 6,218,711 (Yu) alone or in combination with one or more of: the knowledge of one of ordinary skill in the art; Steele; Gadepally; Salmi; Shideler; Kamins; Wallace; Gonzalez; Lee; Hiraoka; Coolbaugh; Furukawa; Bulsara; Ryum; Hoffman; Harame 1992; Harame 1995; Ehwald; Ernst; Wolf; Van Zant; and Lee-270.	5, 12, 14
35 U.S.C. § 103 – U.S. Patent No. 6,800,921 (Coolbaugh) alone or in combination with one or more of: the knowledge of one of ordinary skill in the art; Steele; Gadepally; Salmi; Shideler; Kamins; Wallace; Gonzalez; Lee; Hiraoka; Furukawa; Bulsara; Ryum; Yu; Hoffman; Harame 1992; Harame 1995; Ehwald; Ernst; Wolf; Van Zant; and Lee-270.	5, 12, 14
35 U.S.C. § 103 – JPH 09-219524 (Hiraoka) alone or in combination with one or more of: the knowledge of one of ordinary skill in the art; Steele; Gadepally; Salmi; Shideler; Kamins; Wallace; Gonzalez; Lee; Coolbaugh; Furukawa; Bulsara; Ryum; Yu; Hoffman; Harame 1992; Harame 1995; Ehwald; Ernst; Wolf; Van Zant; and Lee-270.	5, 12, 14

F. U.S. Patent No. 6,624,007

1. Prior Art Patents Under 35 U.S.C. §§ 102(a), (b), (e), (g).

Number	Country	Date of Issue	Date of Application

U.S. Patent No. 6,143,981 (Glenn)	United States	Nov. 7, 2000	Jun. 24, 1998
U.S. Patent No. 6,965,157 (Perez)	United States	Nov. 15, 2005	Dec. 16, 2003
U.S. Patent No. 6,331,451 (Fusaro)	United States	Dec. 18, 2001	Nov. 5, 1999
U.S. Patent No. 5,266,528 (Yamada)	United States	Nov. 30, 1993	Sep. 9, 1992
U.S. Patent No. 6,281,047 (Wu et al.)	United States	Aug. 28, 2001	Nov. 10, 2000
U.S. Patent No. 5,144,709 (Rooney)	United States	Sep. 8, 1992	May 3, 1991
U.S. Patent No. 5,218,229 (Farnworth)	United States	Jun. 8, 1993	Aug. 30, 1991
U.S. Patent No. 5,454,905 (Fogelson)	United States	Oct. 3, 1995	Aug. 9, 1994
U.S. Patent No. 5,696,029 (Alvarez et al.)	United States	Dec. 9, 1997	May 15, 1996
U.S. Patent No. 6,143,981 (Glenn)	United States	Nov. 7, 2000	Jun. 24, 1998
U.S. Patent No. 6,320,251 (Glenn)	United States	Nov. 20, 2001	Jan. 18, 2000
U.S. Patent No. 6,433,277 (Glenn)	United States	Aug. 13, 2002	Jul. 13, 2000
U.S. Patent No. 6,501,156 (Nakanishi et al.)	United States	Dec. 31, 2002	Sep. 8, 2000

2. Prior Art Publications Under 35 U.S.C. §§ 102(a), (b), (e), (g).

Title	**Date of Publication**	**Author(s)**	**Publisher**
Japanese Publication 2001-77263 (Matsuo)	Mar. 23 2001	Matsuo et al.	Japanese Patent Office
Japanese Publication JPH04-305322A (Atobe)	Oct. 28, 1992	Atobe et al.	Japanese Patent Office
Japanese Publication JPH09-102573A (Higuchi)	Apr. 15, 1997	Higuchi et al.	Japanese Patent Office
US 2001/0011772 A1 (Fukasawa et al.)	Aug. 9, 2001	Fukasawa et al.	USPTO
Japanese Publication 2001-298144	Jun. 15, 2005	Fujita et al.	Japanese Patent Office

Japanese Publication JPH3-66153A	Aug. 04, 1989	Omi et al.	Japanese Patent Office
Japanese Publication JPH04-314359A	Apr. 12, 1991	Higuchi	Japanese Patent Office
Japanese Publication PS57155760A	Mar. 23, 1981	Fumihito et al.	Japanese Patent Office
Japanese Publication JPS61-216353A	Mar. 20, 1985	Hideo	Japanese Patent Office
WIPO Publication WO0103186A1	Jan. 11, 2001	Shimanuki	WIPO

3. Prior Art Systems Under 35 U.S.C. §§ 102(a), (b), (g).

Defendants identify the systems disclosed in the patents and publications listed above as prior art. These systems, including constituent software, hardware, methods, and processes, as prior art that may anticipate or render obvious the asserted claims of the ’007 patent. Each system (1) was known or used in this country before the alleged invention of the claimed subject matter of the ’007 patent, (2) was in public use and/or on sale in this country more than one year before the filing date of the application for the ’007 patent and/or (3) was invented and not abandoned, suppressed or concealed prior to the alleged invention of the ’007 patent.

Discovery has not yet started, and Defendants will provide further identification of the above systems and any other systems Defendants learn about through discovery (“the ’007 Patent Prior Art Methods”), including constituent software, hardware, methods, and processes, as prior art that may anticipate or render obvious the asserted claims of the ’007 patent, as such information becomes available. Defendants anticipate third-party discovery may be necessary to obtain that information. Defendants are still investigating these systems and reserve the right to amend and supplement these contentions to provide disclosures based on further discovery and investigation related to these systems as the case progresses.

4. Invalidity Under 35 U.S.C. § 103.

In addition to certain claims being anticipated, the Asserted Claims are also invalid as obvious over the same teachings identified for anticipation and various combinations of the references as shown in the claim charts accompanying these contentions for at least the reasons set forth in the accompanying claim charts.

To the extent not anticipated, the Asserted Claims represent no more than the result of ordinary implementation of the prior art and no Asserted Claim goes beyond combining familiar elements in known methods to achieve predictable results or does more than choose between clear alternatives known to those of skill in the art. Indeed, the '007 patent expressly discloses that most, if not all, of the features claimed in the Asserted Claims were well known to one of ordinary skill in the art.

Though the claim charts (Appendices F1–F8) identify particular exemplary obviousness combinations, Defendants' obviousness defenses are not limited to these combinations. Additional exemplary obviousness combinations on which Defendants rely are provided in the summary table in Section III.F.6 below. The identified prior art references are analogous art and generally directed toward methods for manufacturing semiconductor wafers, leadframes, and packages for integrated semiconductor circuit dies. *See Comaper*, 596 F.3d at 1350–51. But more than that, they are complete systems designed in very similar ways to each other, to cut wafers and leadframe packages with saw blades.

Because the references are so similar to each other and to the alleged invention of the '007 patent, it would be obvious and routine for an ordinarily skilled artisan to combine any of their elements with one another. One of ordinary skill in the art would have also been motivated to combine the identified prior art references based on the references themselves; the common knowledge of one of ordinary skill in the art; the implied and inherent teachings of the prior art as

a whole; and the nature of the problems allegedly addressed by the '007 patent and the prior art.

Moreover, one of ordinary skill in the art would have combined familiar elements according to known methods to predictably achieve the claimed invention. *KSR*, 127 S. Ct. 1727, 1740. Likewise, one of ordinary skill in the art, at the time of the alleged invention, would recognize that similar well-known semiconductor devices and structures could have been improved in similar ways, and would have applied those improvements in the same way to predictably achieve the claimed invention. *Id.* at 1740. For at least these reasons, it would have been obvious to a person of skill in the art at the time of the alleged invention of the Asserted Claims to combine the various references cited herein to practice the Asserted Claims and there is a motivation in the art to make such a combination.

A POSITA would have been motivated to prepare leadframes, semiconductor dies, and resin to make the surface mount packages of the '007 patent. In particular, the cited prior art teaches to make QFN (quad flat no pin) intermediate products or packages, which are surface mount packages. *Matsuo, Glenn,* and *Perez* teach these features. *Matsuo* teaches preparation of an intermediate product. *See Matsuo* at [0041] ("As illustrated in FIG. 1, the lead frame of the present embodiment includes a framework 1 and, inside the framework 1, a rectangular die pad part 2 on which a semiconductor element is mounted…."); *Matsuo* at [0048] ("As illustrated in FIG. 4, the semiconductor element 6 is mounted and bonded with an adhesive such as silver paste on the die pad part 2" of the lead frame.); and *Matsuo* at [0051] ("the lead frame is placed in a die, and a sealing resin 8 consisting of an epoxy resin is injected while the lead part 4 is pressed against the sealing sheet 10 by the die so as to seal the upper surface region of the die pad part 2, the semiconductor element 6, and the lead part 4 and the connection regions of the thin metal wires 7 as the outer periphery of the lead frame."). *Glenn* similarly teaches preparation of an intermediate product.

Glenn at 6:44–65 ("In Step 4 of FIG. 1, the lower second surface of leadframe 20 of FIG. 2 is placed on a flat surface, and a viscous adhesive encapsulating material is applied onto the upward facing upper first surface of leadframe 20. The encapsulating material is applied so that the encapsulating material covers: the integrated circuit die; the bond wires; any exposed peripheral portions of upper first surface 25 of die pad 24 around the die; side surfaces 27 of die pad 24; upper first surface 31 of tabs 30; side surfaces 33 of tabs 33; and part or all of the width of members 22, 22A, 23, and 23A of frame 21."). *Perez* also teaches preparation of an intermediate product. *Perez* at 5:35–40 ("After the die 56 has been attached to the die pad 22 and wire bonded to the leads 16, the leadframe 10 is placed in the cavity of a clam-shell mold (not illustrated), and a molten, insulative plastic, *e.g.*, an epoxy resin, is injected into the cavity to form a protective body 66 over the die, the die pad, and the leads to seal and protect them from the environment."). In fact, all three references teach similar semiconductor surface mount packages, *i.e.*, QFN or quad flat no pin packages. Thus, a POSITA would have been motivated to prepare leadframes, semiconductor dies, and resin to make the surface mount packages of the '007 patent.

A POSITA would have been motivated to "process an electroconductive material" to make a leadframe of the '007 patent. All of the cited prior art references teach processing flat metal electroconductive material to make a leadframe. *See Matsuo* at [0043] ("[T]he lead frame is not a single pattern of the configuration illustrated in FIG. 1, but is rather a plurality of patterns arranged continuously in the horizontal and vertical directions"); *Glenn* 1:64–2:8 ("In one embodiment of an assembly method for a package within the present invention, Step 1 provides a metal lead frame. The leadframe includes a rectangular frame, *e.g.*, a square frame."); *Perez* at 3:62–4:14 ("Fabrication of the leadframe begins with the provision of a thin, polygonal plate 12 of a ductile metal (FIG. 1), which is then patterned to form the nascent leadframe 10 (FIG. 2). In the exemplary

square embodiment illustrated in FIG. 1, the plate 12 is about 0.254 millimeters ("mm") thick, about 4 mm on a side, and made of a copper alloy."); *Atobe* at Abstract ("In a lead frame manufacturing method using stamping, in stamping leads on a lead frame material 10, preliminary stamping of previously forming a slit-shaped preliminary hole 14 connecting tips of inner leads 12 to be formed to each other is performed, and coining is applied to a site of the lead frame material 10 where the tips of the inner leads 12 are to be formed to partially reduce the thickness of the lead frame material 10 and then, the stamping is performed to form the leads."); and *Higuchi* at [0001] ("The present invention relates to a method of manufacturing a lead frame used in a semiconductor device, and in particularly, relates to a method of manufacturing a semiconductor device lead frame provided with a thin flat portion at a tip of an inner lead."). It would have been obvious to a POSITA in view of *Matsuo*, *Glenn*, *Perez*, *Atobe*, and *Higuchi* to process an electroconductive material" to make a leadframe.

A POSITA would have been motivated to cut or dice leadframe packages with two saw blades of different thicknesses via two passes of different depths as suggested by the '007 patent. All of the references teach to cut or dice wafers or leadframe packages. *Matsuo* teaches to cut leadframe packages with two saws of different thicknesses to overcome problems where "resin chipping, cracking, or the like may occur in the portion of the sealing resin adjacent to the lead part due to impact at the time of lead cutting, and the lead part may fall off of the sealing resin portion." *Matsuo* at [0018]. Further, Matsuo teaches two-blade cutting so that "the burrs 12 primarily generated on the side surface sides and the bottom surface side of the lead part 4 are removed, or burr generation itself is prevented." *Matsuo* [0059]. Further, *Glenn* teaches to cut leadframe packages using a conventional wafer saw. *Glenn* at 7:56–8:24 ("Step 6 of FIG. 1 cuts leadframe 20 of FIG. 7 in situ.... To perform Step 6 using a saw, the encapsulated leadframe 20 of

FIG. 7 is inverted and placed on sticky film. Using the exposed portions of leadframe 20 as a guide (see FIG. 2), a ***conventional wafer saw*** is used to saw a completed package from the encapsulated leadframe 20.") *Fukasawa, Wu et al., and Yamada* each teach the use of conventional wafer saws of two different thicknesses to avoid resin chipping and delamination of resin from metal components. *See Fukasawa* at [0023] ("the problem of cracking of a resin layer covering a semiconductor chip or a crack formation at an interface between the resin layer and the semiconductor chip is successfully avoided"); *Wu et al.* at 5:5–13 (first wide cutting blade ensures entire connect bar is cut away and second thin blade cuts all the way through the resin); *and Yamada* at 2:58–62 ("it becomes possible to suppress the occurrence of cracks resulting primarily from the vibration of the diamond blade, to minimize cracks even when they occur.'). *Perez* teaches to cut away the outside portions of the leadframe. *Perez* at 5:46–56 ("The rectangular frame 14 (shown dotted in FIG. 7) of the leadframe 10 is exposed outside of the lateral periphery of the body 66, and is ***subsequently cut away from the body*** and discarded in a finishing operation to leave the outer ends 70 of the locking pads 40 exposed through the side surfaces 72 of the package 68 (see FIG. 8)."). It would have been obvious to a POSITA in view of *Matsuo*, *Glenn*, *Perez*, *Fukasawa, Wu et al., and Yamada* to use two saw blades of different thicknesses to cut lead frame packages via two cut passes at different depths.

Defendants reserve the right to further specify the motivations to combine the prior art in response to positions that Bell Semic may take later in this case and as discovery, including third party discovery, proceeds. Defendants may rely on any and all portions of the prior art, other documents, and expert testimony to establish that a person of ordinary skill in the art would have been motivated to modify or combine the prior art and his/her knowledge to render the claims invalid as obvious.

5. Invalidity Under 35 U.S.C. § 112.

Defendants assert that claim 1 of the ’007 patent is invalid for failure to meet the requirements of 35 U.S.C. § 112(b). In particular, claim 1 is invalid because the phrase “forming a packaging layer to enclose the chip” is indefinite. The phrase, viewed in light of the specification and prosecution history, fails to inform those skilled in the art about the scope of the invention with reasonable certainty.

Defendants assert that claim 4 of the ’007 patent is invalid for failure to meet the requirements of 35 U.S.C. § 112(b). In particular, claim 4 is invalid because the phrase “processing an electroconductive material” is indefinite. The phrase, viewed in light of the specification and prosecution history, fails to inform those skilled in the art about the scope of the invention with reasonable certainty.

6. Summary of ’007 Patent Invalidity

The following table summarizes Defendants’ invalidity contentions related to the ’007 patent, as set forth in this document and Appendices F1–F8.

Invalidity Grounds	Asserted Claims
35 U.S.C. § 112	1, 3, 4
35 U.S.C. § 102 – Japanese Publication 2001-77263 (Matsuo)	1, 3, 4
35 U.S.C. § 103 – 01-77263 (Matsuo) alone or in combination with one or more of: the knowledge of one of ordinary skill in the art; Glenn; Perez; Fusaro; Yamada; Wu et al.; Atobe; Higuchi; and Fukasawa.	1, 3, 4
35 U.S.C. § 103 – U.S. Patent No. 6,143,981 (Glenn) alone or in combination with one or more of: the knowledge of one of ordinary skill in the art; Matsuo; Perez; Fusaro; Yamada; Wu et al.; Atobe; Higuchi; and Fukasawa.	1, 3, 4
35 U.S.C. § 103 – U.S. Patent No. 6,965,157 (Perez) alone or in combination with one or more of: the knowledge of one of ordinary skill in the art; Matsuo; Glenn; Fusaro; Yamada; Wu et al.; Atobe; Higuchi; and Fukasawa.	1, 3, 4

35 U.S.C. § 103 – U.S. Patent No. 6,331,451 (Fusaro) alone or in combination with one or more of: the knowledge of one of ordinary skill in the art; Matsuo; Glenn; Perez; Yamada; Wu et al.; Atobe; Higuchi; and Fukasawa.	1, 3, 4
35 U.S.C. § 103 – U.S. Patent No. 5,266,528 (Yamada) alone or in combination with one or more of: the knowledge of one of ordinary skill in the art; Matsuo; Glenn; Fusaro; Perez; Wu et al.; Atobe; Higuchi; and Fukasawa.	1, 3, 4
35 U.S.C. § 103 – U.S. Patent No. 6,281,047 (Wu et al.) alone or in combination with one or more of: the knowledge of one of ordinary skill in the art; Matsuo; Glenn; Fusaro; Yamada; Perez; Atobe; Higuchi; and Fukasawa.	1, 3, 4
35 U.S.C. § 103 – Japanese Publication JPH04-305322A (Atobe) alone or in combination with one or more of: the knowledge of one of ordinary skill in the art; Matsuo; Glenn; Fusaro; Yamada; Wu et al.; Perez; Higuchi; and Fukasawa.	1, 3, 4
35 U.S.C. § 103 – Japanese Publication JPH09-102573A (Higuchi) alone or in combination with one or more of: the knowledge of one of ordinary skill in the art; Matsuo; Glenn; Fusaro; Yamada; Wu et al.; Atobe; Perez; and Fukasawa.	1, 3, 4
35 U.S.C. § 103 – US 2001/0011772 A1 (Fukasawa) alone or in combination with one or more of: the knowledge of one of ordinary skill in the art; Matsuo; Glenn; Fusaro; Yamada; Wu et al.; Atobe; Higuchi; and Perez.	1, 3, 4

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Respectfully submitted,

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CERTIFICATE OF SERVICE

I hereby certify that on the 4th day of December 2020, I served the foregoing to the following counsel of record:

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