

Filed: March 22, 2021

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

MICROCHIP TECHNOLOGY INCORPORATED; AND
MICROSEMI CORPORATION,

PETITIONERS,

V.

BELL SEMICONDUCTER, LLC,

PATENT OWNER.

IPR2021-00191
U.S. Patent No. 7,221,173

**PATENT OWNER'S PRELIMINARY RESPONSE
UNDER 35 U.S.C. § 313 AND 37 C.F.R. § 42.107**

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I. INTRODUCTION

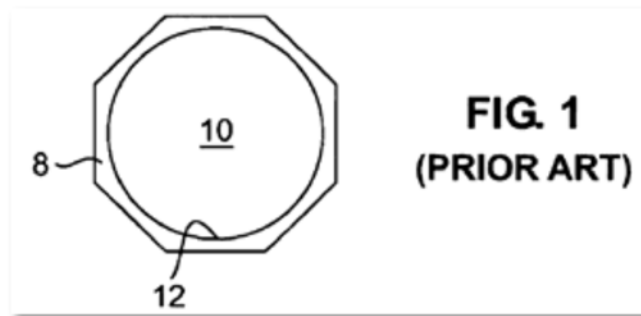
Patent Owner submits this Preliminary Response, which is timely filed on March 22, 2021. The Board should deny institution of the Petition for at least the following reasons. *First, Mardi* (Ex. 1005) is not prior art to the ‘173 Patent because the inventors conceived of the ‘173 Patent before the filing of *Mardi* and were diligent in reducing their invention to practice. Since *Mardi* is not prior art, it cannot be combined with the knowledge of a POSITA as proposed in Ground 2. *Second, Lin* (Ex. 1006) is cumulative of art before the Examiner. *Third, Lin* does not disclose the “wafer-level testing” before bumping limitation found in independent claims 1, 9, and 10. For this same reason, Petitioners’ attempts to combine *Lin* with the knowledge of a POSITA or with *Yong* (Ex. 1007) also fail.

II. BACKGROUND OF THE INVENTION

A. Description of the ‘173 Patent’s Inventions

The ‘173 Patent is directed “to structures and techniques for enabling wafer level testing [of semiconductor devices] prior to performing a bumping process in a flip chip assembly.” (Ex. 1001, 1:8-11.) Specifically, integrated circuits (“ICs”) are fabricated on a semiconductor wafer. Depending on the size of the ICs and the area of the semiconductor wafer, a number of ICs are manufactured simultaneously on each wafer. Before the ICs are cut from the wafer (called “dicing”) and individually packaged, the wafer is tested to ensure the ICs are functional.

Figure 1 represents the prior art and shows “a top view schematic representation of a metal bonding pad 8 (*e.g.*, Al or Cu bonding pad) of a semiconductor device that includes a bump region 10 over the metal bonding pad 8.” (Ex. 1001, 1:28-31.)



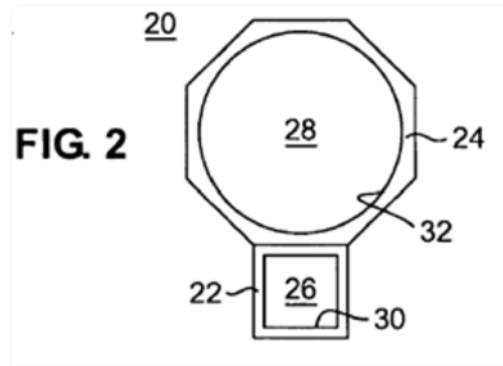
(*Id.*, FIG. 1.)

The ‘173 Patent explains that a “test probe tip that may be placed in contact with the bonding pad may gouge the metal pad surface. The resulting surface irregularities on the bump pad can lead to difficulties in establishing and maintaining strong adhesion for one or more metal layers that may be deposited during the formation of the bump.” (Ex. 1001, 1:41-47.)

To address these issues, as illustrated in Figure 2, the ’173 Patent teaches:

[A] conductive test pad 22 provides a respective probe region 26 where a probe tip may be placed for performing, for example, wafer level testing. The bonding pad 24 includes a bump region 28 that is no longer subject to mechanical contact with the probe tip and resulting surface irregularities. It is envisioned that since the test pad and

bonding pad comprise an integral structure that no longer requires inter connect lines and avoids or Substantially reduces propagation delays in test signals passing therethrough, an interface assembly embodying aspects of the present invention should lead to more reliable and accurate test results.



(Ex. 1001, 3:1-14; Fig. 2.)

In other words, the '173 Patent teaches the creation of a test structure integrally constructed with the bond pad that allows for electrical testing in a separate region from the bump region. The innovative test pad allows electrical testing to be conducted without the probe tips damaging the bump region.

III. LEVEL OF ORDINARY SKILL

For purposes of this Preliminary Response only, Patent Owner does not dispute Petitioners' definition of a POSITA (Pet. 2-3). Should the Board institute (which it should not), Patent Owner reserves the right to further address Petitioners' improper POSITA definition and its impact on the asserted Grounds.

IV. CLAIM CONSTRUCTION

The challenged claims of the '173 Patent are to be construed “using the same claim construction standard that would be used to construe the claim in a civil action under 35 U.S.C. § 282(b).” 37 C.F.R. § 42.100(b) (Nov. 13, 2018). The Petition does not seek construction of any terms of the '173 Patent. (Pet. 15.) Patent Owner reserves the right to provide claim constructions should any trial be instituted.

V. LEGAL STANDARDS

A. Standard For Granting An IPR

The Board may grant a petition for IPR where “the information presented in the petition . . . shows that there is a reasonable likelihood that the petitioner would prevail with respect to at least 1 of the claims challenged in the petition.” 35 U.S.C. § 314(a); 37 C.F.R. § 42.108(c). The Petitioners bear the burden of showing that the statutory threshold is met. Office Patent Trial Practice Guide, 77 Fed. Reg. 48,756 (Aug. 14, 2012). A petition must provide “[a] full statement of the reasons for the relief requested, including a detailed explanation of the significance of the evidence including material facts, and the governing law, rules, and precedent.” 37 C.F.R. § 42.22(a)(2).

B. Obviousness Standard

“A patent may not be obtained . . . if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a

whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains.” 35 U.S.C. § 103(a). The obviousness analysis requires several threshold inquiries.

1. Claims cannot be found obvious if an element is absent.

If a single element of the claim is absent from the prior art, the claim cannot be considered obvious. *In re Rijckaert*, 9 F.3d 1531, 1534 (Fed. Cir. 1993) (reversing obviousness rejection where prior art did not teach or suggest all claim limitations); *Garmin Int’l, Inc. v. Patent of Cuozzo Speed Techs. LLC*, IPR2012-00001, Paper 15, at 15 (PTAB Jan. 9, 2013) (refusing to institute IPR under § 103 where the prior art did not disclose all claim limitations).

2. The *Graham* Factors

Obviousness is resolved based on factual determinations including (1) the scope and content of the prior art, (2) any differences between the claimed subject matter and the prior art, and (3) the level of ordinary skill in the art. *Graham v. John Deere Co.*, 383 U.S. 1, 17-18 (1966).

3. A Petition Must Provide Articulated Reasoning with Rational Underpinnings to Combine or Modify References.

The conclusion of obviousness based on a combination of references must be supported with an explicit analysis of a reason to combine those references. *KSR Int’l Co. v. Teleflex Inc.*, 550 U.S. 398, 418 (2007). Such reasons must be more than “mere conclusory statements; instead, there must be some articulated

reasoning with some rational underpinning to support the legal conclusion of obviousness.” *In re Kahn*, 441 F.3d 977, 988 (Fed. Cir. 2006).

VI. GROUND 1: *MARDI* IS NOT PRIOR ART

A. Legal Standards

A patent owner may antedate a reference by proving earlier conception and reasonable diligence in reducing to practice. *Perfect Surgical Techniques, Inc. v. Olympus Am., Inc.*, 841 F.3d 1004, 1007 (Fed. Cir. 2016). “Conception must be proved by corroborating evidence which shows that the inventor disclosed to others his ‘completed thought expressed in such clear terms as to enable those skilled in the art’ to make the invention.” *Coleman v. Dines*, 754 F.2d 353, 359 (Fed. Cir. 1985) (citing *Field v. Knowles*, 183 F.2d 593, 601 (1950)).

“Reasonable diligence must be shown throughout the entire critical period, which begins just prior to the competing reference’s effective date and ends on the date of the invention’s reduction to practice.” *Perfect Surgical*, 841 F.3d at 1007. An inventor’s testimony of reasonable diligence throughout the critical period “must be corroborated by evidence.” *Id.* We apply a “rule of reason” to evaluate such corroborating evidence. *Id.* at 1008.

Importantly, diligence need not be perfectly continuous—only *reasonably* continuous. *Id.* at 1009. “[P]eriods of inactivity within the critical period do not automatically vanquish a patent owner’s claim of reasonable diligence.” *Id.* “[T]he

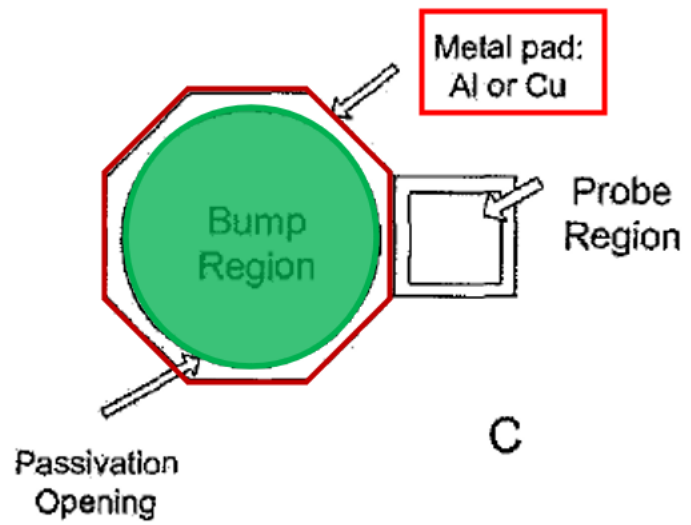
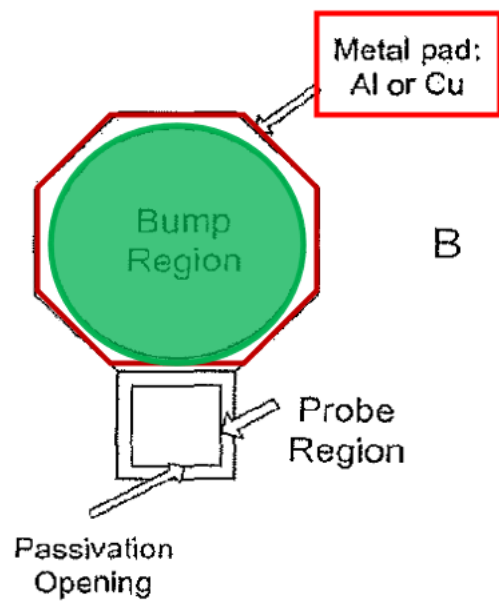
point of the diligence analysis is not to scour the patent owner’s corroborating evidence in search of intervals of time where the patent owner has failed to substantiate some sort of activity.” *Id.* Rather, the adequacy of the reduction to practice is determined by whether, “in light of the evidence as a whole, ‘the invention was not abandoned or unreasonably delayed.’” *Id.* (quoting *Brown v. Barbacid*, 436 F.3d 1376, 1379 (Fed. Cir. 2006)). “Whether a patent antedates a reference is a question of law based on subsidiary findings of fact,” and “[t]he issue of reasonable diligence ‘turns on the factual record, and we review Board determinations as to diligence for support by substantial evidence in the record.’” *Id.* at 1008 (quoting *In re Steed*, 802 F.3d 1311, 1317 (Fed. Cir. 2015)).

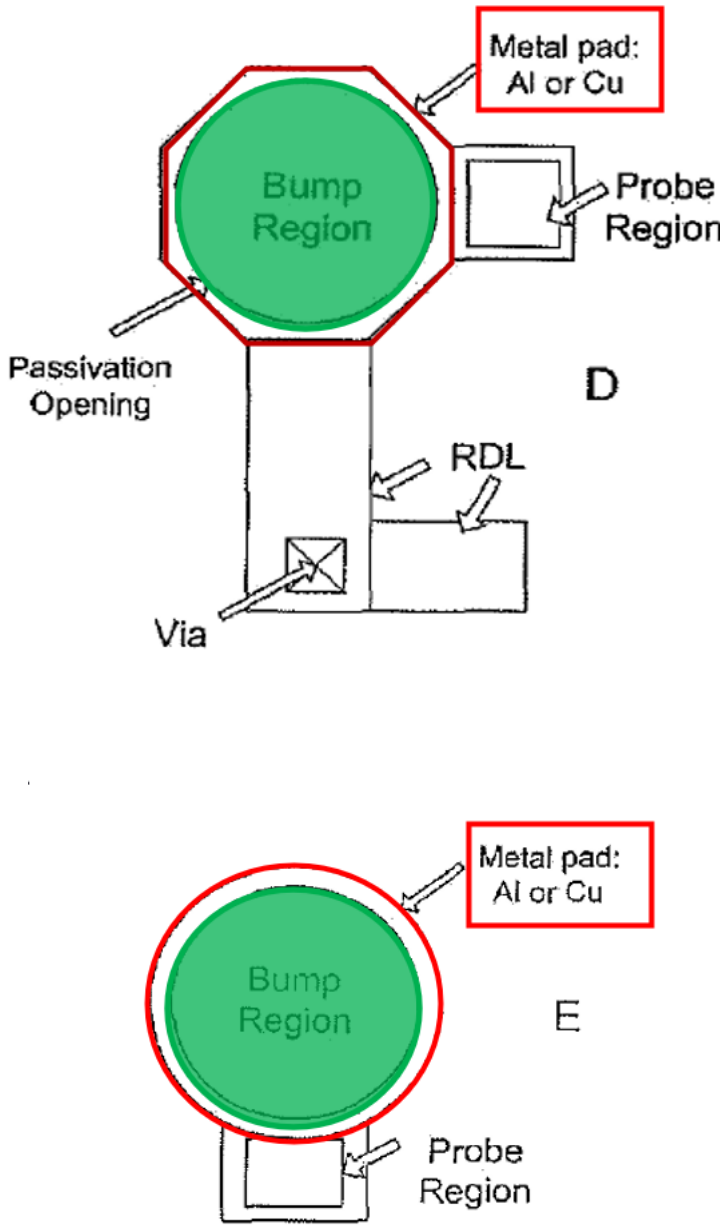
B. The Inventors Conceived of the ’173 Patent Inventions Prior to the Filing of *Mardi*

Mardi was filed on May 11, 2004, and issued on June 26, 2007. (Ex. 1005, Cover.) Petitioners argue that *Mardi* is prior art under 35 U.S.C. § 102(e). (Pet., 15.) However, an Agere Systems Invention Submission form (“Invention Submission”), the same entity that the ’173 was assigned to, shows that the inventors conceived of the invention before *Mardi*’s filing. (*Compare* Ex. 2001 with Ex. 1001, Cover.) The inventors listed in the Invention Submission match the inventors listed on the ’173 Patent. (*Id.*) The Invention Submission is stamped as being received on May 10, 2004, which predates the *Mardi* reference’s filing date. (*Compare* 2001 with Ex. 1005.)

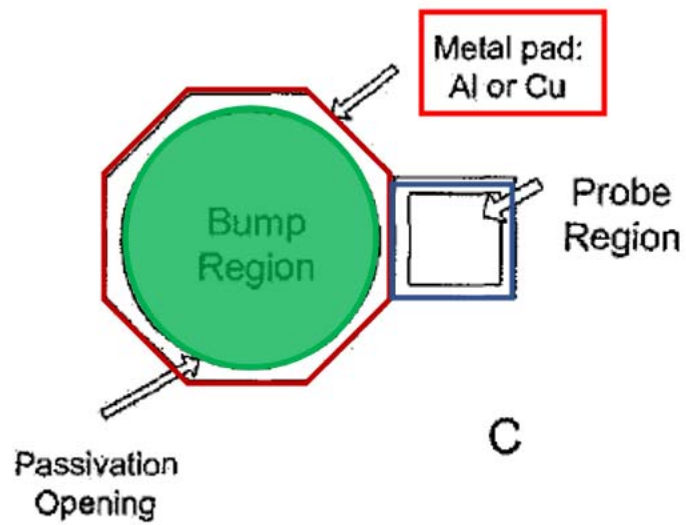
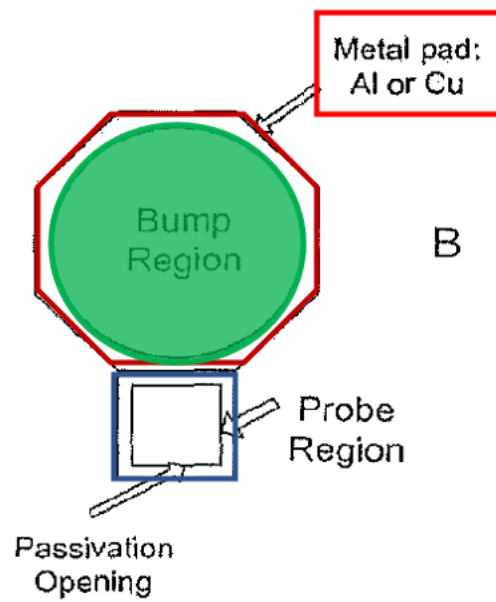
The following chart discusses the disclosure of the Invention Submission on an element-by-element basis. The first column includes the '173 claim language. The second column contains quotations from the Invention Submission, as well as a description showing a one-to-one correspondence between the claim language and Invention Submission disclosure:

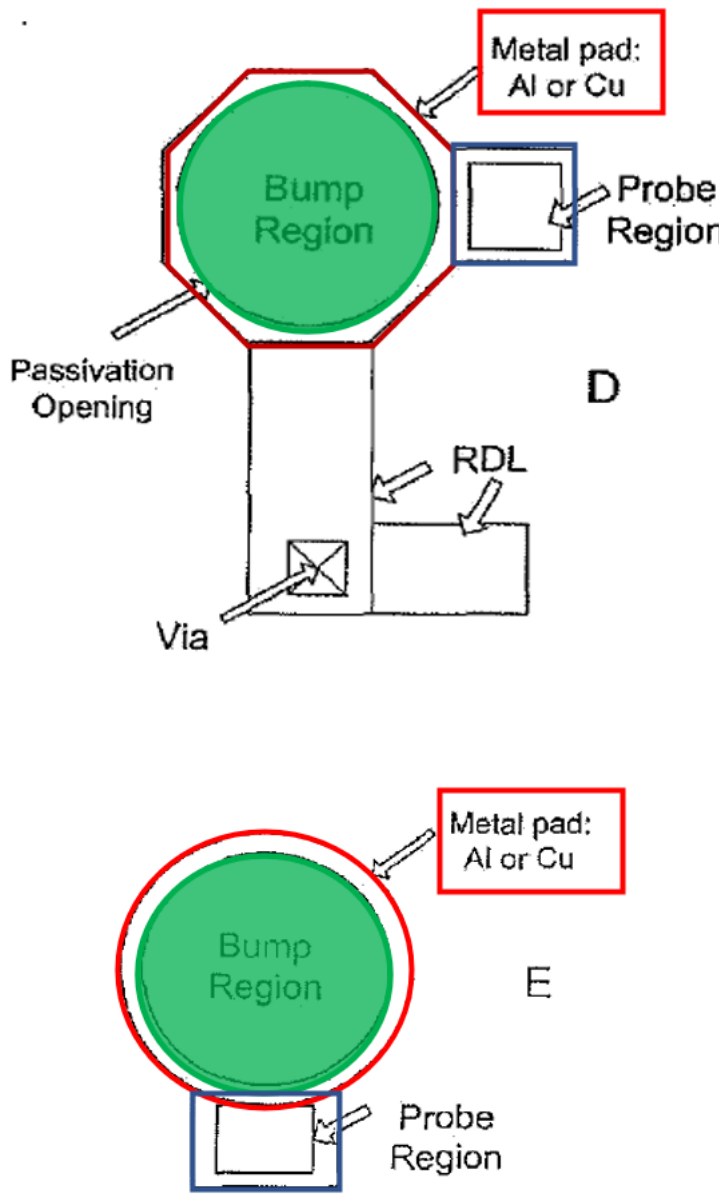
'173 Claim	Invention Submission Disclosure (Ex. 2001)
[1a] An interface assembly for a semiconductor wafer, said interface assembly comprising: a flip chip bonding pad including a region for performing a bumping process;	<p>The Invention Submission describes and provides images, in figures B-E, of a bonding pad that includes a “Bump Region.”</p> <p>The Invention Submission provides:</p> <p><i>“For devices made with flip chip technology, testing on Al or Cu pads prior to bumping to test the chip is not allowed because probe marks gouge the pad surface, making the deposition of under bump metallization (UBM) difficult and subsequent bumping processes unreliable. Thus what is needed in the art is a method of allowing chips to be probed prior to bumping so that wafer level tests can be undertaken.”</i></p> <p>The Invention Submission further describes a preferred embodiment of the invention:</p> <p><i>“Fig. B shows a preferred embodiment of the present invention: a schematic diagram of a metal pad with a square (shown) or rectangular (not shown) probe region, integral with a separate octagonal (shown) bump region. Separate passivation openings for the respective probe and bump regions are also shown.”</i></p> <p>Further, as noted above, the Invention Submission provides multiple examples of metal bond pads (annotated in red) with a “Bump Region” (annotated in green) for performing a bumping process:</p>



	 <p>Diagram D shows a cross-sectional view of a device. A green circular region labeled "Bump Region" is positioned on top of a substrate. A red octagonal outline surrounds the bump region, with a label "Metal pad: Al or Cu" pointing to it. To the right of the bump region is a square opening labeled "Probe Region". On the left side, a "Passivation Opening" is indicated. Below the bump region, a "Via" is shown with a cross-hatch pattern, and "RDL" (Redistribution Layer) is labeled on the right side.</p> <p>Diagram E shows a top-down view of the device. A green circular region labeled "Bump Region" is surrounded by a red circular outline, with a label "Metal pad: Al or Cu" pointing to it. Below the bump region is a square opening labeled "Probe Region".</p>
<p>[1b] and a test pad integrally constructed with said bonding pad that form an integral conductive structure such that separate interconnect</p>	<p>The Invention Submission shows a test pad in multiple orientations connected to the metal bond pad. As shown in Figures B-E, the test pad is an extension of the bond and, therefore, is an integral structure. Furthermore, as seen in the images, there are no interconnect testing lines between the bond pad and the test pad.</p>

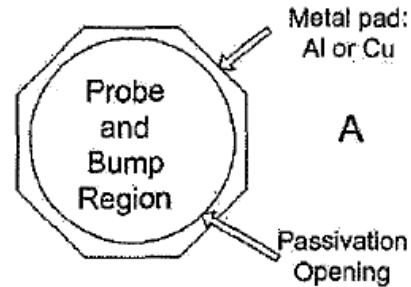
<p>testing lines from said test pad to said bonding pad are not present in said integral structure,</p>	<p>The Invention Submission states:</p> <p><i>“Fig. B shows a preferred embodiment of the present invention: a schematic diagram of a metal pad with a square (shown) or rectangular (not shown) probe region, integral with a separate octagonal (shown) bump region. Separate passivation openings for the respective probe and bump regions are also shown.”</i></p> <p>The Invention Submission notes that one prior art attempt to solve problems with the prior art approaches involved <i>“peripheral probe pads that are connected to the bump pad or probe after bumping.”</i> The inventors noted that <i>“interconnects have to be made from the probe pad to the bump pad, leading to interconnect delays, and/or loss of yield from extra material regions that are susceptible to defects.”</i> As can be seen in Figures B-E, there are no interconnect testing lines in the solution conceived of by the inventors.</p> <p>Figures B-E show the bond pad (annotated in red) containing a bump region (annotated in green) along with an integrally constructed test pad (annotated in blue) without the use of separate interconnect test lines between the bond pad and the test pad:</p>
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	 <p>Diagram D is a cross-sectional view of a metal pad. It features a green circular "Bump Region" and a blue square "Probe Region" adjacent to it. A "Passivation Opening" is shown on the left side of the bump region. Below the bump region, a "Via" is indicated. To the right of the bump region, an "RDL" (Redistribution Layer) is shown. A label "Metal pad: Al or Cu" points to the top right corner of the pad. The letter "D" is located to the right of the diagram.</p> <p>Diagram E is a top-down view of the same metal pad. It shows the green circular "Bump Region" and the blue square "Probe Region" within a red outline representing the metal pad. A label "Metal pad: Al or Cu" points to the top right corner of the pad. The letter "E" is located to the right of the diagram.</p>
<p>[1c] said test pad being coplanar relative to said flip chip bonding pad and including a probe region for performing wafer-level testing</p>	<p>The Invention Submission describes that openings are made in a passivation layer for the bump region and also in the test pad for the probe region: “Fig. B shows a preferred embodiment of the present invention: a schematic diagram of a metal pad with a square (shown) or rectangular (not shown) probe region, integral with a separate octagonal (shown) bump region. Separate passivation openings for the respective probe and bump</p>

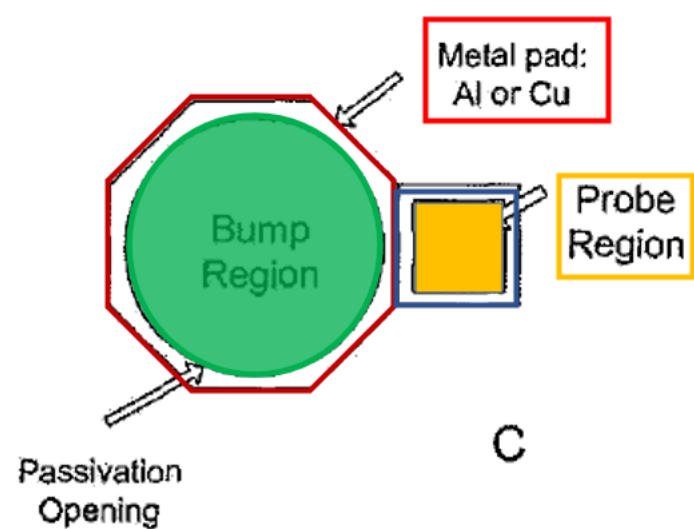
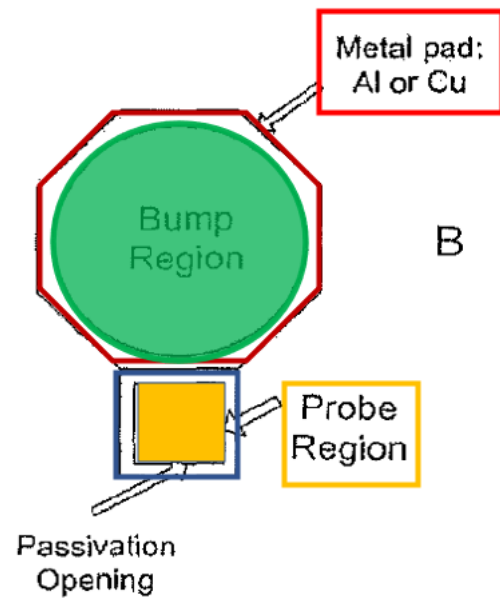
prior to performing said bumping process

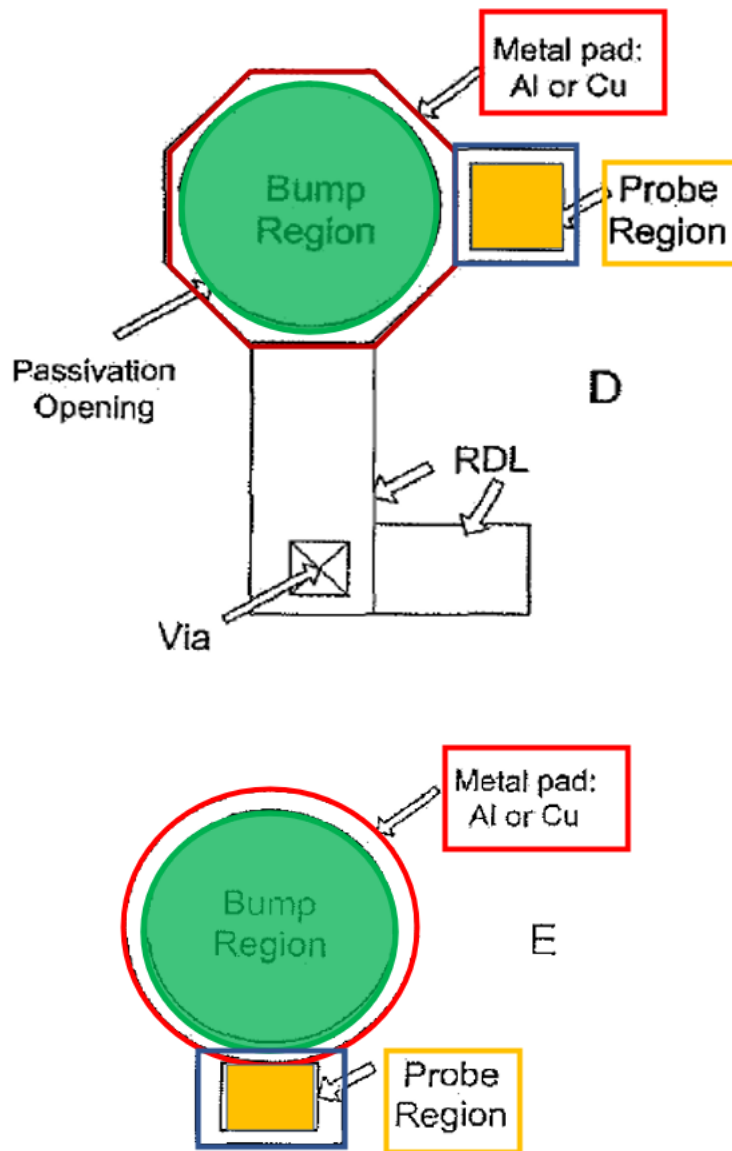
regions are also shown.” The separate openings in the passivation layer demonstrate that the test pad and the bonding pad are coplanar. Further, an object the invention is to allow a wafer to be probed. The Invention Submission notes that in the prior art the probe region and bump region overlapped, meaning they were one in the same as shown in Figure A:



The disclosed invention removed the overlap and created separate, non-overlapping regions. However, the new bump and probe regions disclosed remain in the same plane.

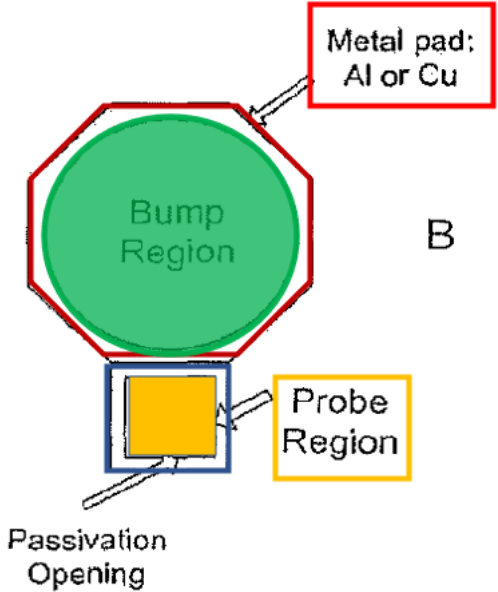
As shown in Figures B-E there is a probe region (annotated in orange) within the test pad (annotated in blue):

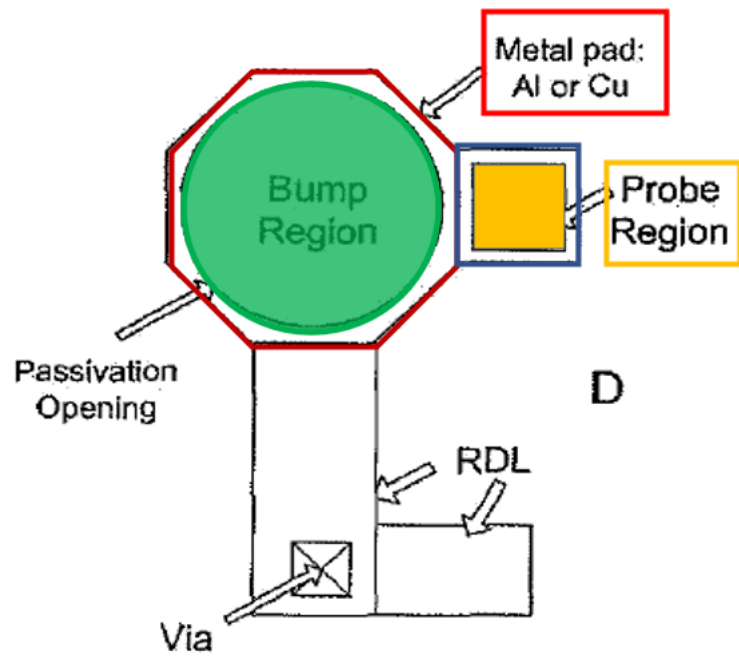
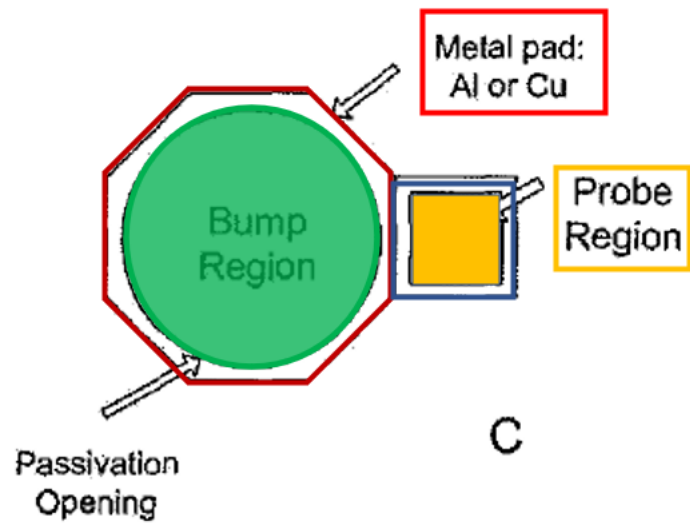


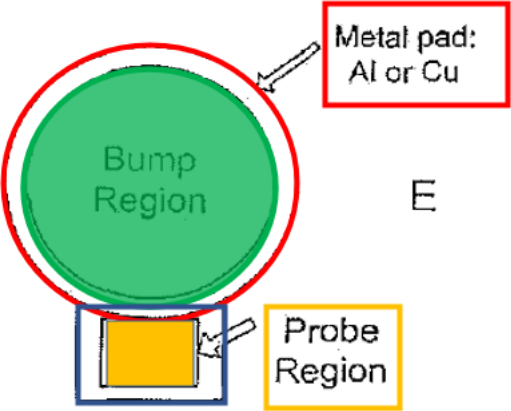
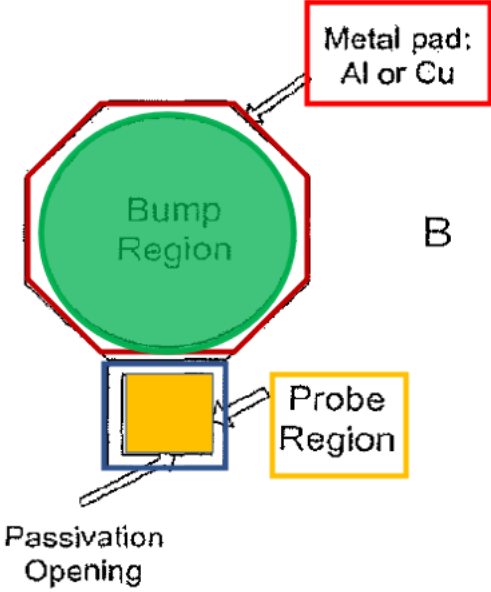


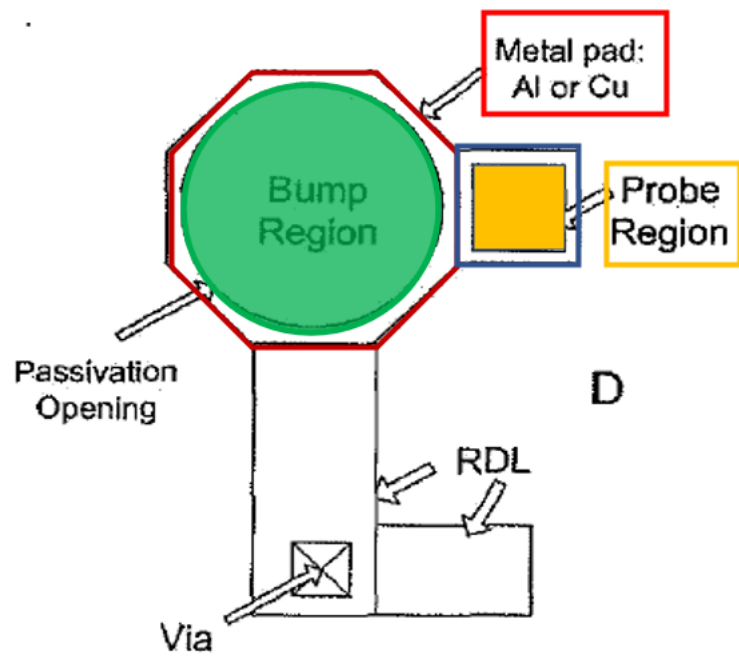
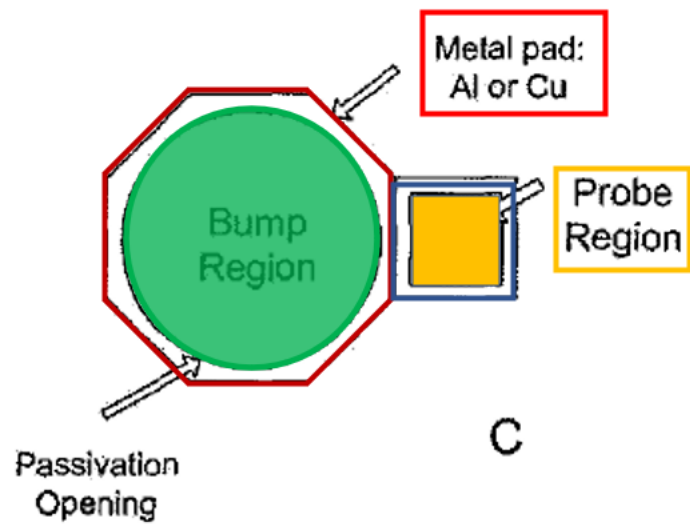
The Invention Submission provides that the disclosed structure allows for wafer-level testing a wafer prior to bumping:

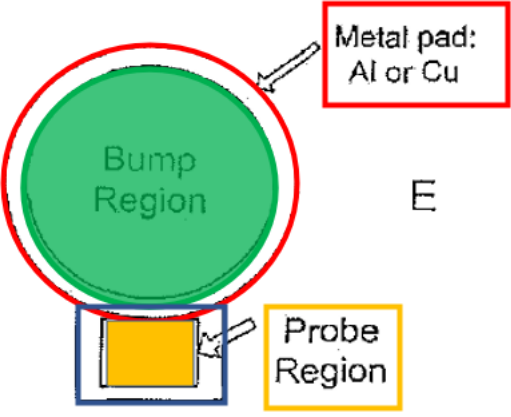
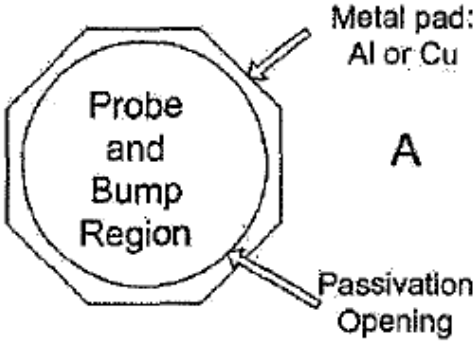
“For devices made with flip chip technology, testing on Al or Cu pads prior to bumping to test the chip is not allowed because probe marks gouge the pad surface, making the deposition of under bump metallization (UBM) difficult and subsequent bumping processes

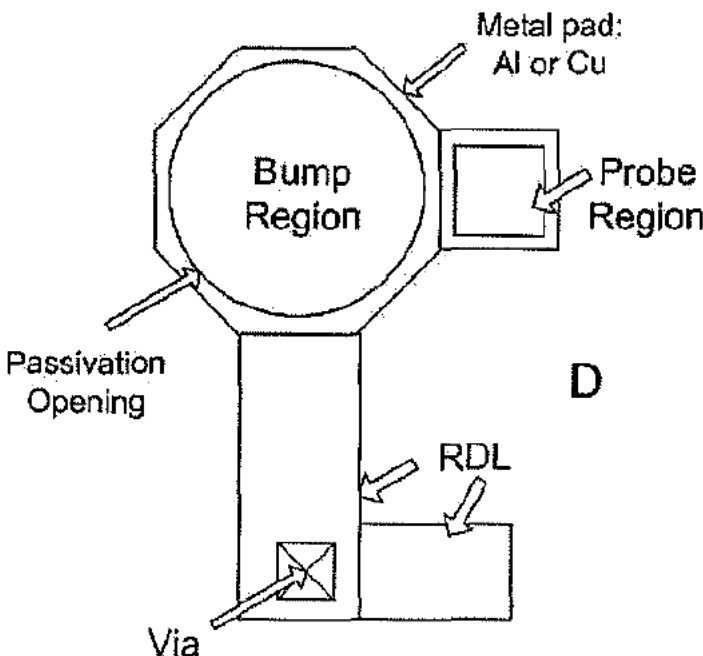
	<p><i>unreliable. Thus what is needed in the art is a method of allowing chips to be probed <u>prior to bumping</u> so that wafer level tests can be undertaken.”</i></p> <p><i>“The use of separate regions for bump formation and probing for testing wafers prior to bumping is easier and reliable.”</i></p>
<p>[2] The interface assembly of claim 1 wherein said test pad may be disposed anywhere along a periphery of said bonding pad.</p>	<p>The Invention Submission provides that the probe region, which is contained within the test pad, can be on any side of the bond pad: <i>“The probe region can be configured on any side of the octagon, such as shown in Fig. C.</i></p> <p>As shown in Figures B-E, the test pad can be placed at various orientations along the edge of the bond pad:</p>  <p>The diagram illustrates a chip interface assembly. It features a central green circular area labeled 'Bump Region'. This region is enclosed within a red octagonal boundary. A label 'Metal pad: Al or Cu' with an arrow points to the red octagonal boundary. Below the bump region, there is a yellow square area labeled 'Probe Region'. A label 'Passivation Opening' with an arrow points to the bottom edge of the yellow square. The entire assembly is labeled with a large 'B' to its right.</p>

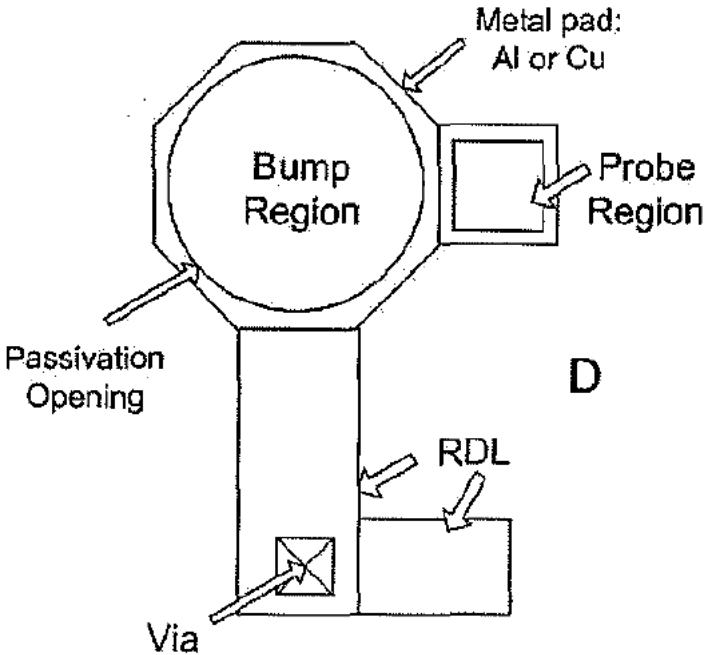
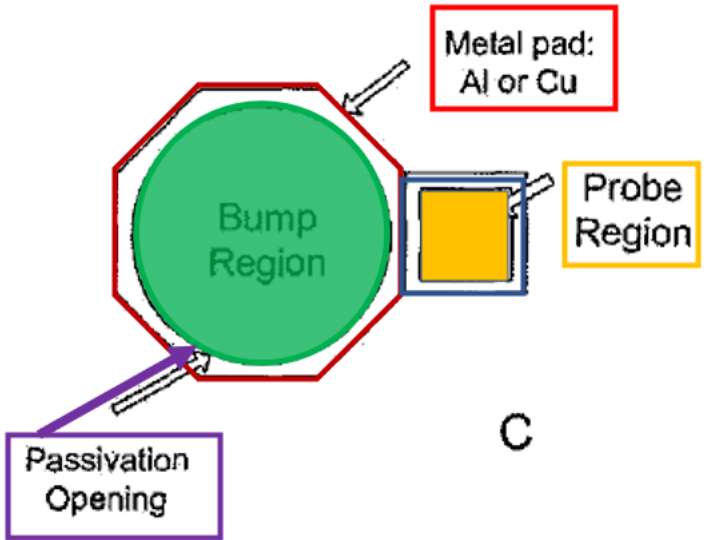


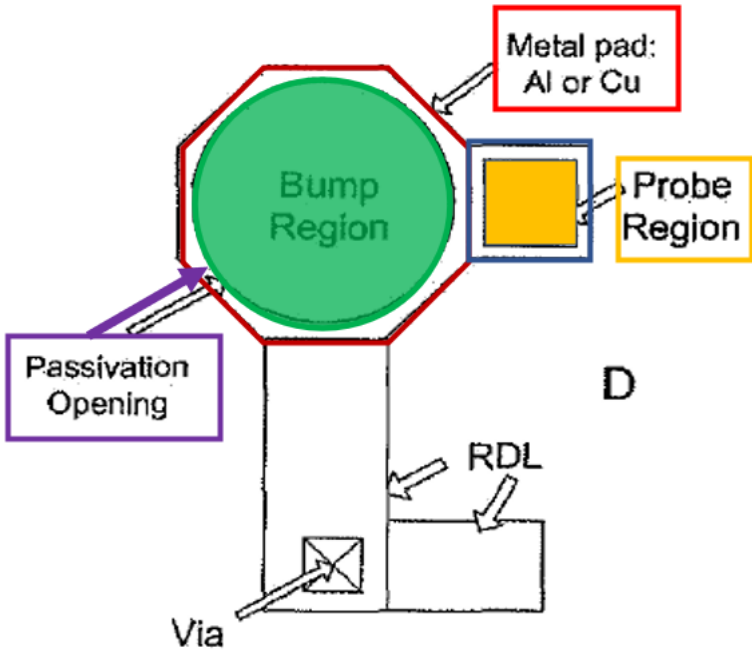
	
<p>[3] The interface assembly of claim 1 wherein said bonding pad comprises a shape selected from the group consisting of a polygonal shape, and a circular shape.</p>	<p>The Invention Submission form shows that the bond pad can have a variety of shapes. Specifically, the Invention Submission states: “While octagonal pads have been shown, a circular pad with a circular passivation opening, such as illustrated in Fig. E, is also conceived.”</p> <p>Further, Figures B-D show the bond pad as an octagon (i.e., a polygon), whereas Figure E shows the bond pad as a circle.</p> 

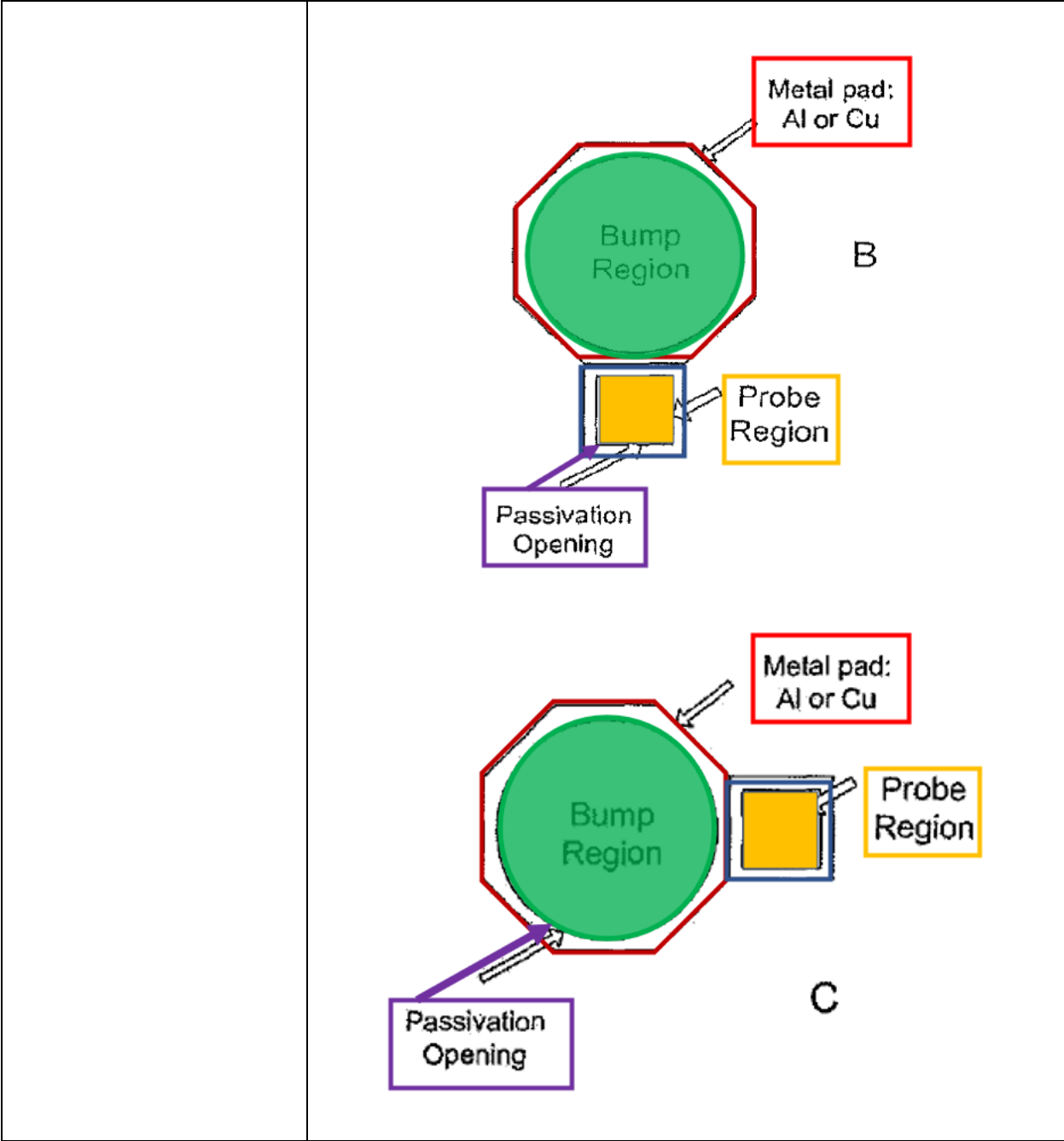


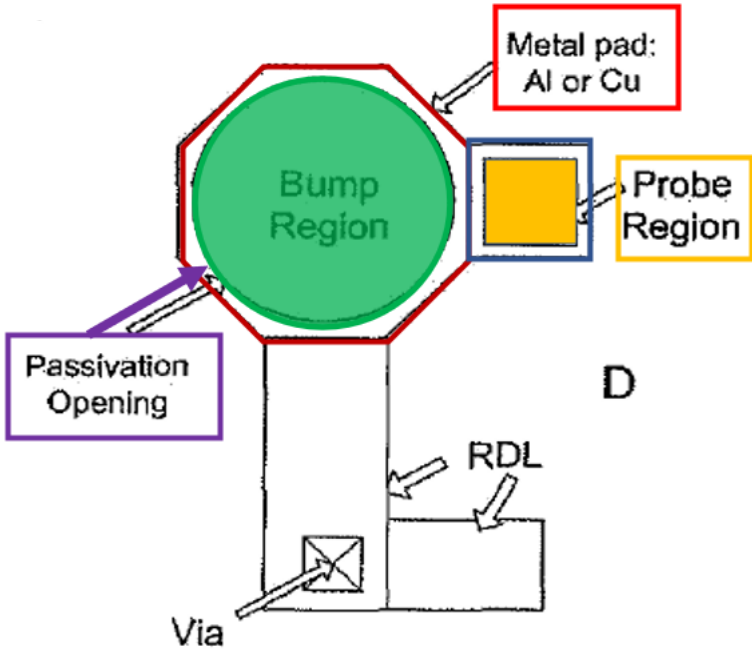
	
<p>[4] The interface assembly of claim 1 wherein said test pad comprises a shape selected from the group consisting of a polygonal shape, and a circular shape.</p>	<p>Figure A in the Invention Submission shows that probe regions can be circular:</p>  <p>As shown in Figures B-E, the test pads are disclosed as mimicking the probe regions' shapes. Therefore, since circular probe regions are disclosed, corresponding circular test pads were also contemplated.</p>
<p>[5] The interface assembly of claim 1 further comprising a first metal redistribution layer electrically connected to said bonding and test pads, and being</p>	<p>The Invention Submission provides that “<i>Metal redistribution layers (RDL) are shown in Fig. D to connect the bump region to other metal runners or interconnect, to other pads, either directly or through vias (for example, one is shown in the illustration).</i>” When the RDLs connect the bump region to other pads, this occurs in the same plane as demonstrated by the</p>

<p>coplanar with one another.</p>	<p>Invention Submission's use of "directly," which is shown below:</p> 
<p>[6] The interface assembly of claim 5 wherein said first metal redistribution layer is electrically connected by way of a via to a second redistribution layer being disposed in a different plane than the first redistribution layer.</p>	<p>The Invention Submission provides that “<i>Metal redistribution layers (RDL) are shown in Fig. D to connect the bump region to other metal runners or interconnect, to other pads, either directly or through vias (for example, one is shown in the illustration).</i>” When the RDLs connect the bump region to other pads “through vias,” this occurs in a different plane because the vias are electrical connections between layers in that go through the plane of one or more adjacent layers. D specifically demonstrate the use of vias to connect to other RDLs in different planes:</p>

	
<p>[7] The interface assembly of claim 1 wherein the region to be bumped is defined by a first opening in a passivation layer.</p>	<p>The Invention Submission discloses that an opening in a passivation layer defines the bump region within in the bond pad. Specifically, Figures C and D depict circular opening in the passivation layer (annotated in purple):</p> 

	
<p>[8] The interface assembly of claim 7 wherein the probe region is defined by a second opening in said passivation layer, said first and second openings are spaced apart.</p>	<p>The Invention Submission demonstrates that the bump region in the bond pad and the probe region in the test pad can be defined by openings in the passivation layer. Further, these openings in the passivation layer are separate, and there is space between the two distinct openings (<i>i.e.</i>, the bump and test probe regions are not comprised a single opening in the passivation layer). This is seen by looking at Figures B-D. The bumping region (annotated in green) is separate from the probe region (annotated in orange).</p>



	 <p>The diagram illustrates a cross-sectional view of a semiconductor wafer structure. A central green circular area is labeled 'Bump Region'. To its right is a yellow square labeled 'Probe Region'. Above the bump region is a red-outlined octagonal area labeled 'Metal pad: Al or Cu'. To the left of the bump region is a purple-outlined rectangular area labeled 'Passivation Opening'. Below the bump region is a white rectangular area labeled 'RDL' (Redistribution Layer). At the bottom left, a small square with an 'X' inside is labeled 'Via'. A large letter 'D' is positioned to the right of the bump region.</p>
<p>[9(a)] A method for testing a semiconductor wafer prior to performing a flip chip bumping process, said method comprising:</p>	<p>For the same reason described above in connection with Claim 1, the Invention Submission discloses testing a semiconductor wafer prior to bumping:</p> <p><i>“For devices made with flip chip technology, testing on Al or Cu pads prior to bumping to test the chip is not allowed because probe marks gouge the pad surface, making the deposition of under bump metallization (UBM) difficult and subsequent bumping processes unreliable. Thus what is needed in the art is a method of allowing chips to be probed prior to bumping so that wafer level tests can be undertaken.”</i></p> <p><i>“The use of separate regions for bump formation and probing for testing wafers prior to bumping is easier and reliable.”</i></p>
<p>[9(b)] providing a flip chip bonding pad having a region for</p>	<p>The Invention Submission provides:</p> <p><i>“For devices made with flip chip technology, testing on Al or Cu pads prior to bumping to test the chip is not</i></p>

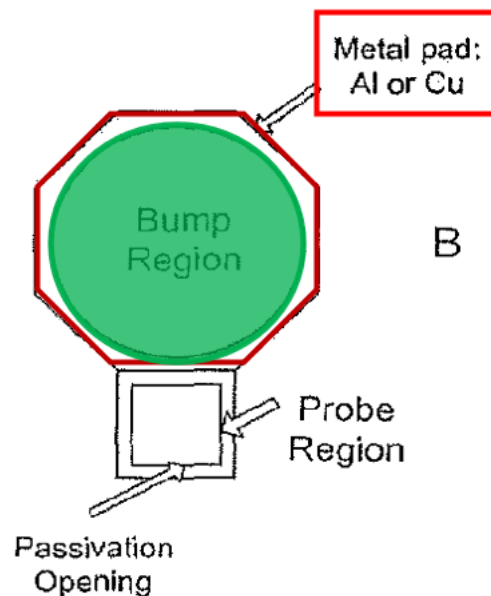
performing said bumping process

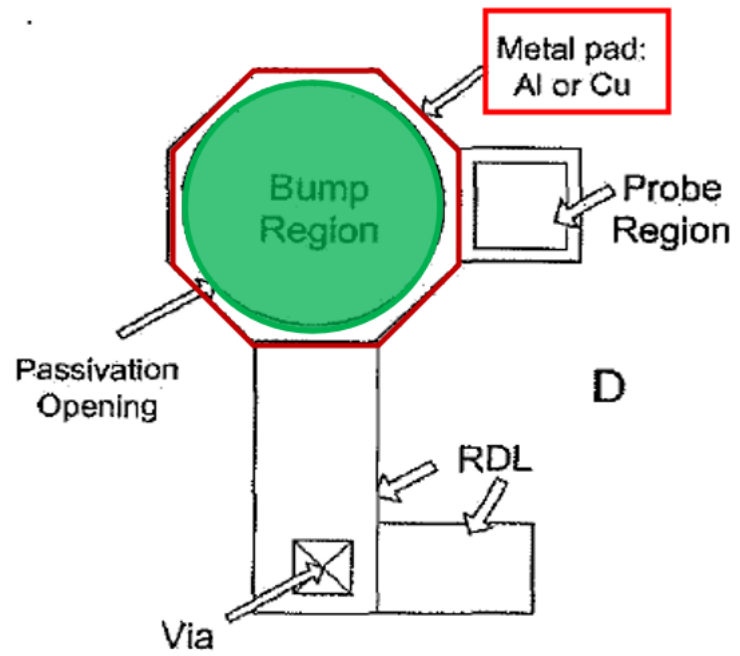
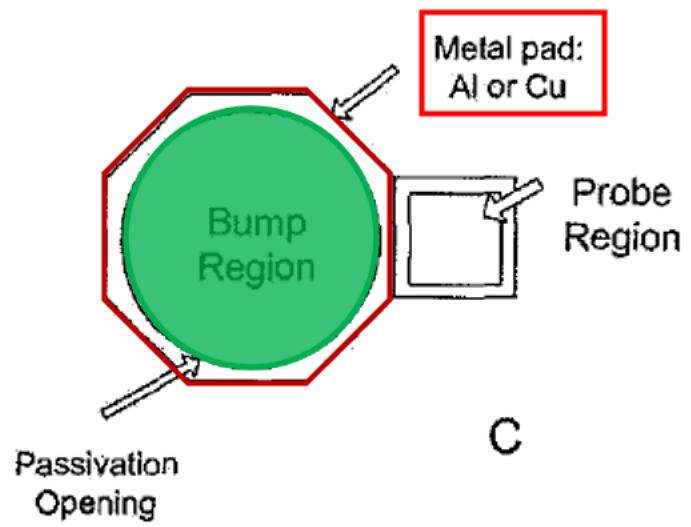
allowed because probe marks gouge the pad surface, making the deposition of under bump metallization (UBM) difficult and subsequent bumping processes unreliable. Thus what is needed in the art is a method of allowing chips to be probed prior to bumping so that wafer level tests can be undertaken.”

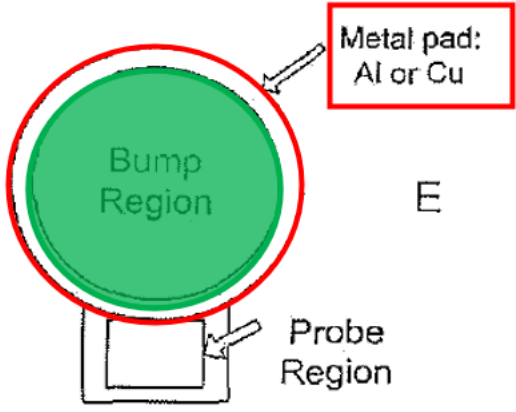
The Invention Submission further describes a preferred embodiment of the invention:

*“Fig. B shows a preferred embodiment of the present invention: **a schematic diagram of a metal pad** with a square (shown) or rectangular (not shown) probe region, **integral with a separate octagonal (shown) bump region**. Separate passivation openings for the respective probe and bump regions are also shown.”*

Further, the Invention Submission provides multiple examples of metal bond pads (annotated in red) with a “Bump Region” (annotated in green) for performing a bumping process:

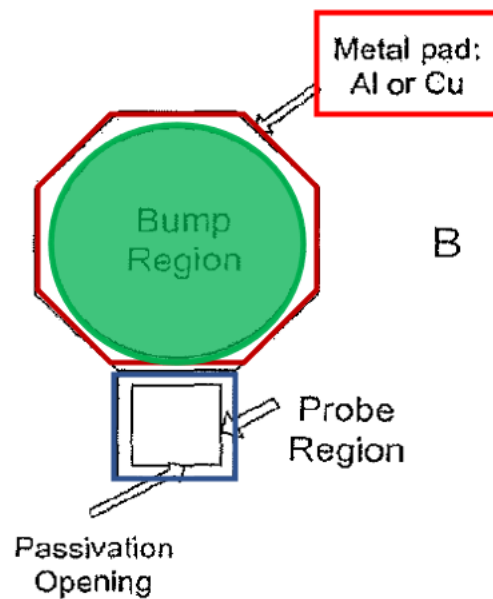


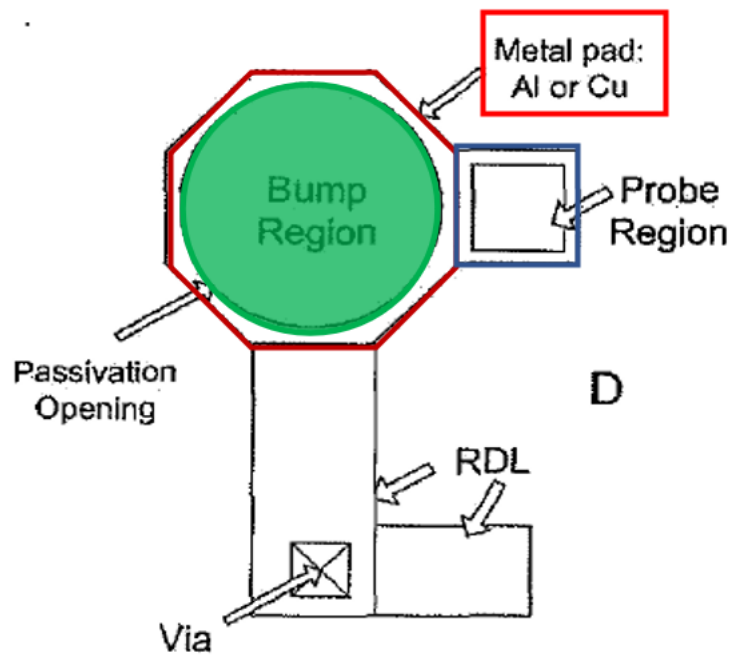
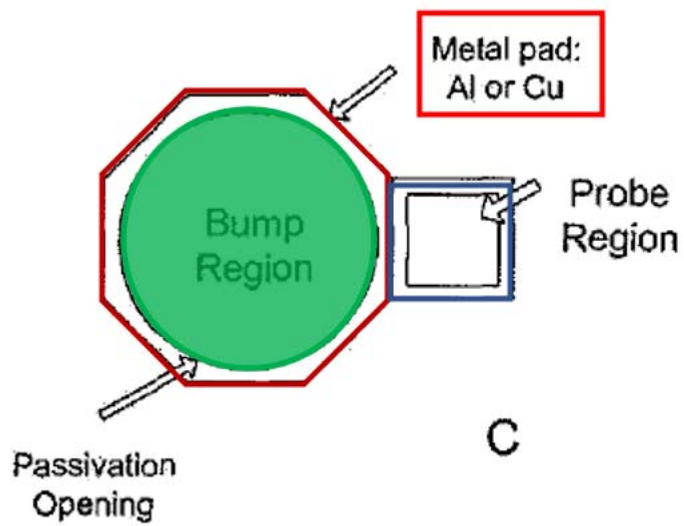


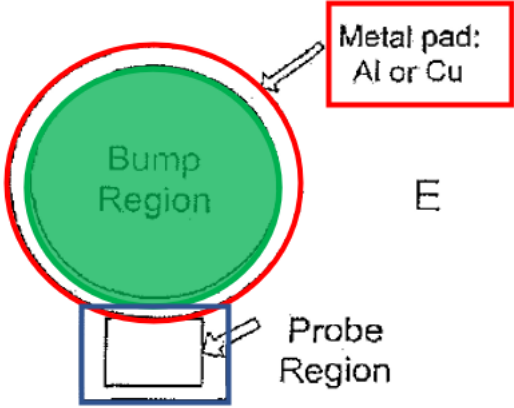
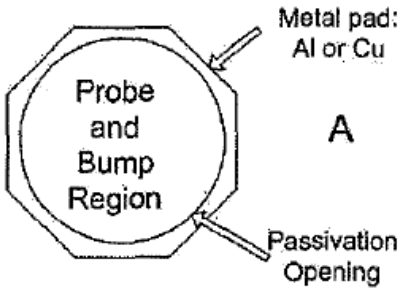
	
<p>[9(c)] integrally constructing a test pad with said bonding pad to form an integral conductive structure such that separate interconnect testing lines from said test pad to said bonding pad are not present in said integral structure;</p>	<p>The Invention Submission shows a test pad in multiple orientations connected to the metal bond pad. As shown in Figures B-E, the test pad is an extension of the bond and, therefore, is an integral structure. Furthermore, as seen in the images, there are no interconnect testing lines between the bond pad and the test pad.</p> <p>The Invention Submission states:</p> <p><i>“Fig. B shows a preferred embodiment of the present invention: a schematic diagram of a metal pad with a square (shown) or rectangular (not shown) probe region, integral with a separate octagonal (shown) bump region. Separate passivation openings for the respective probe and bump regions are also shown.”</i></p> <p>The Invention Submission notes that one prior art attempt to solve problems with the prior art approaches involved “<i>peripheral probe pads that are connected to the bump pad or probe after bumping.</i>” The inventors noted that “<i>interconnects have to be made from the probe pad to the bump pad, leading to interconnect delays, and/or loss of yield from extra material regions that are susceptible to defects.</i>” As can be seen in Figures B-E,</p>

there are no interconnect testing lines in the solution conceived of by the inventors.

Figures B-E show the bond pad (annotated in red) containing a bump region (annotated in green) along with an integrally constructed test pad (annotated in blue) without the use of separate interconnect test lines between the bond pad and the test pad:

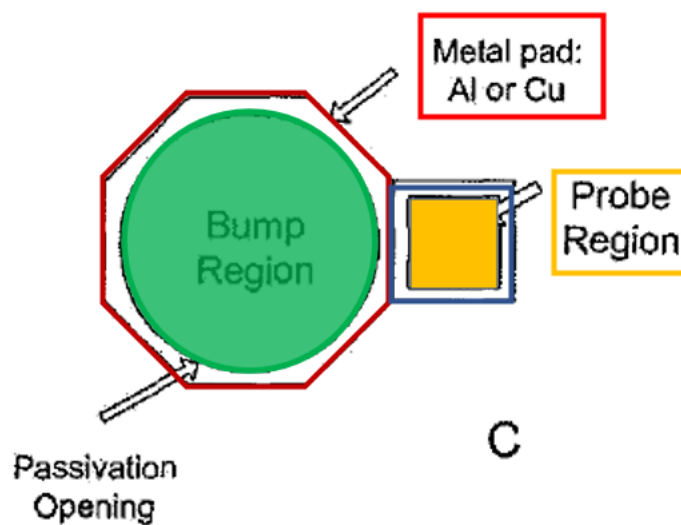
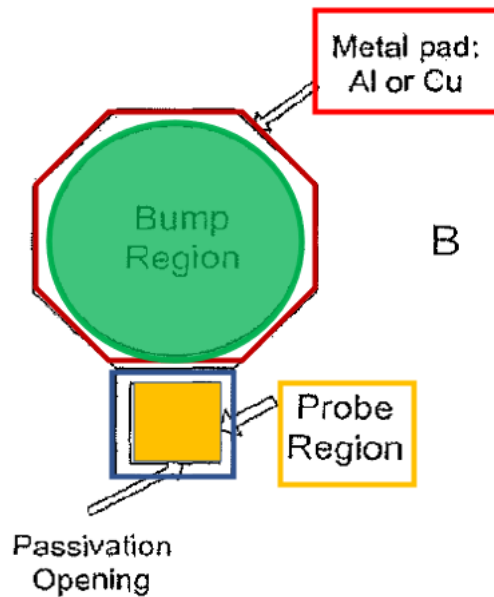


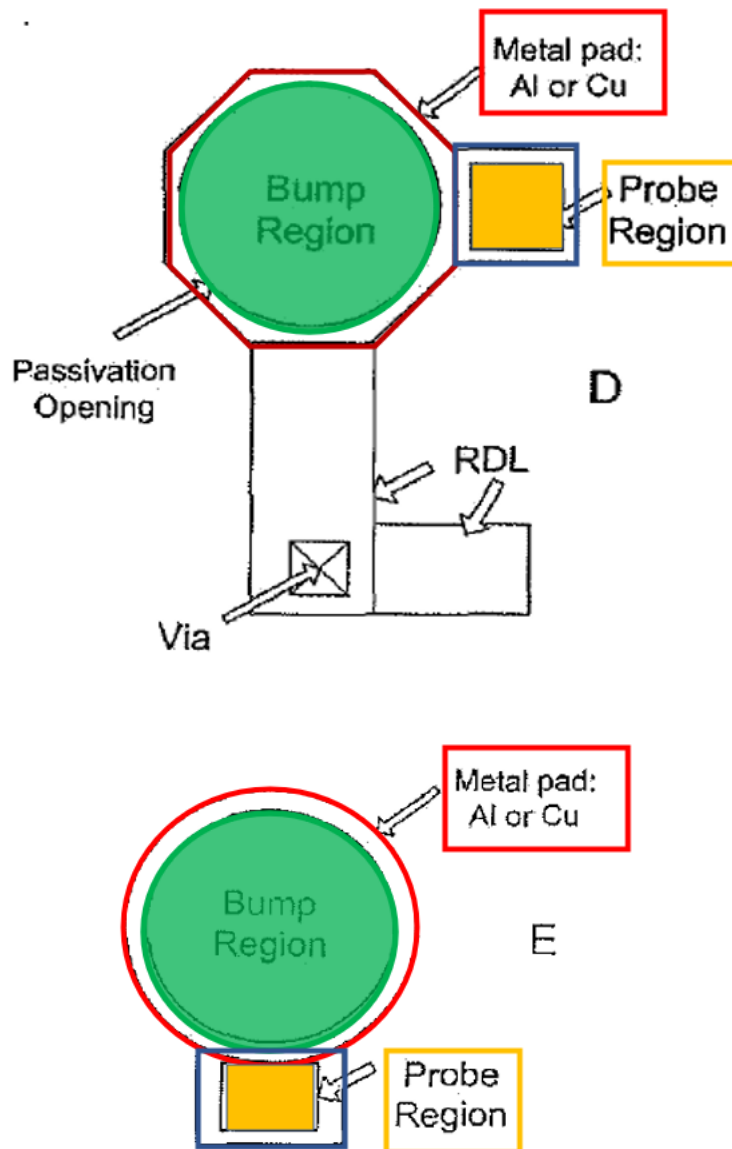


	 <p>The diagram shows a green circular area labeled "Bump Region" inside a larger red circular outline. Below the bump region is a blue rectangular outline labeled "Probe Region". A label "Metal pad: Al or Cu" with an arrow points to the red outline. The letter "E" is to the right of the bump region.</p>
<p>[9(d)] and disposing said test pad coplanar with said flip chip bonding pad, said test pad including a probe region for performing a wafer test prior to performing said bumping process.</p>	<p>The Invention Submission describes that openings are made in a passivation layer for the bump region and also in the test pad for the probe region: “Fig. B shows a preferred embodiment of the present invention: a schematic diagram of a metal pad with a square (shown) or rectangular (not shown) probe region, integral with a separate octagonal (shown) bump region. Separate passivation openings for the respective probe and bump regions are also shown.” The separate openings in the passivation layer demonstrate that the test pad and the bonding pad are coplanar. Further, an object the invention is to allow a wafer to be probed. The Invention Submission notes that in the prior art the probe region and bump region overlapped, meaning they were one in the same as shown in Figure A:</p>  <p>The diagram shows an octagonal shape labeled "Probe and Bump Region" inside a larger octagonal outline. A label "Metal pad: Al or Cu" with an arrow points to the outer octagonal outline. A label "Passivation Opening" with an arrow points to a small gap in the outer octagonal outline. The letter "A" is to the right of the octagonal shape.</p>

The disclosed invention removed the overlap and created separate, non-overlapping regions. However, the new bump and probe regions disclosed remain in the same plane.

As shown in Figures B-E there is a probe region (annotated in orange) within the test pad (annotated in blue):





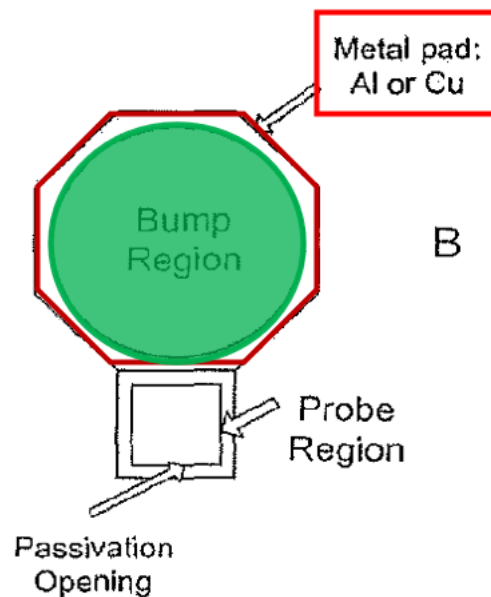
The Invention Submission provides that the disclosed structure allows for wafer-level testing a wafer before bumping:

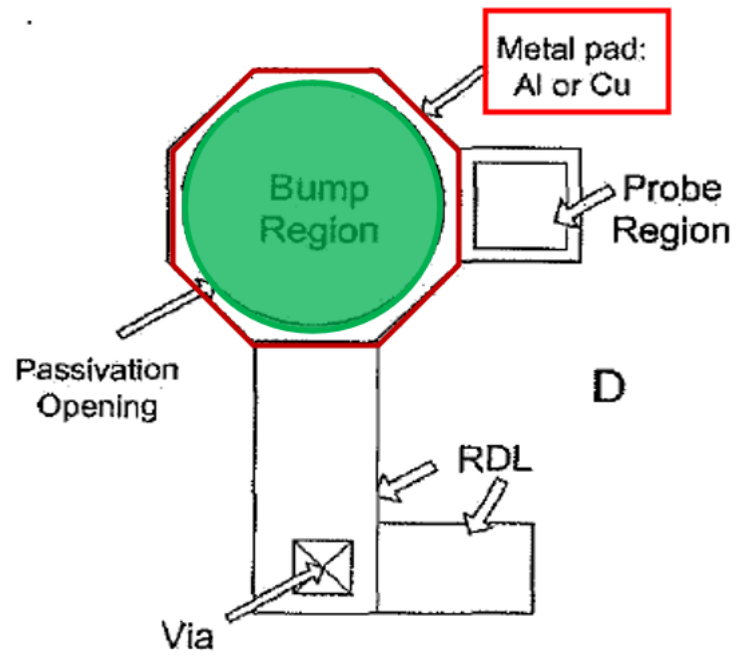
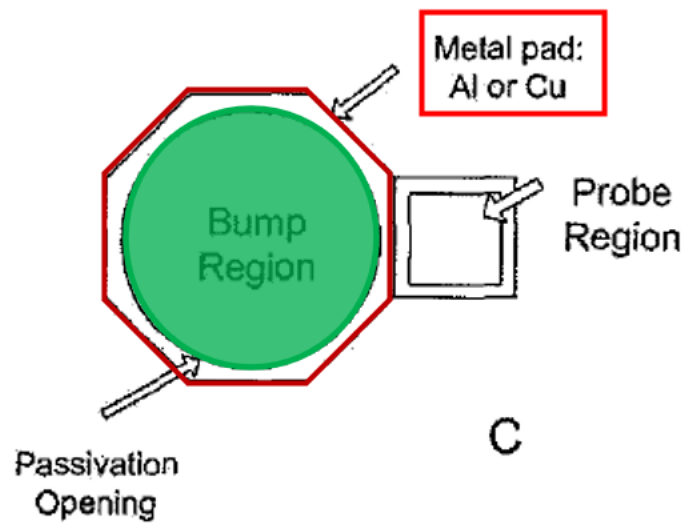
“For devices made with flip chip technology, testing on Al or Cu pads prior to bumping to test the chip is not allowed because probe marks gouge the pad surface, making the deposition of under bump metallization (UBM) difficult and subsequent bumping processes

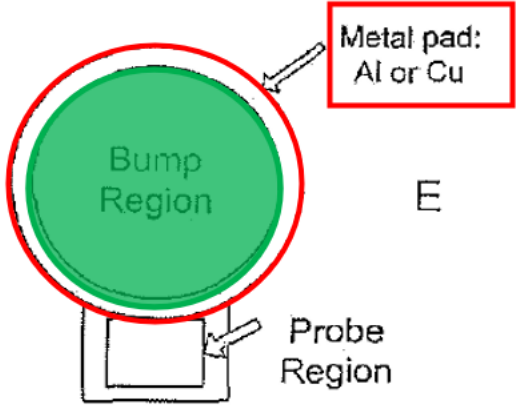
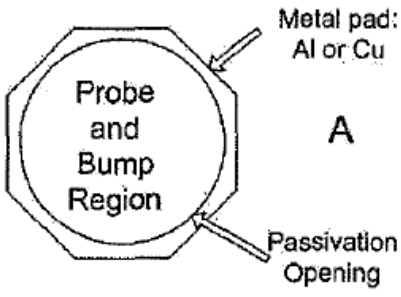
	<p><i>unreliable. Thus what is needed in the art is a method of allowing chips to be probed <u>prior to bumping</u> so that wafer level tests can be undertaken.</i></p> <p><i>“The use of separate regions for bump formation and probing for testing wafers prior to bumping is easier and reliable.”</i></p>
<p>[10a] An interface assembly for a semiconductor wafer, said interface assembly comprising: a flip chip bonding pad including a region for performing a bumping process;</p>	<p>For the same reason described above in connection with Claim 1, the Invention Submission discloses testing a semiconductor wafer prior to bumping:</p> <p><i>“For devices made with flip chip technology, testing on Al or Cu pads prior to bumping to test the chip is not allowed because probe marks gouge the pad surface, making the deposition of under bump metallization (UBM) difficult and subsequent bumping processes unreliable. Thus what is needed in the art is a method of allowing chips to be probed <u>prior to bumping</u> so that wafer level tests can be undertaken.”</i></p> <p><i>“The use of separate regions for bump formation and probing for testing wafers prior to bumping is easier and reliable.”</i></p> <p>The Invention Submission provides:</p> <p><i>“For devices made with flip chip technology, testing on Al or Cu pads prior to bumping to test the chip is not allowed because probe marks gouge the pad surface, making the deposition of under bump metallization (UBM) difficult and subsequent bumping processes unreliable. Thus what is needed in the art is a method of allowing chips to be probed prior to bumping so that wafer level tests can be undertaken.”</i></p> <p>The Invention Submission further describes a preferred embodiment of the invention:</p>

“Fig. B shows a preferred embodiment of the present invention: a schematic diagram of a metal pad with a square (shown) or rectangular (not shown) probe region, integral with a separate octagonal (shown) bump region. Separate passivation openings for the respective probe and bump regions are also shown.”

Further, the Invention Submission provides multiple examples of metal bond pads (annotated in red) with a “Bump Region” (annotated in green) for performing a bumping process:

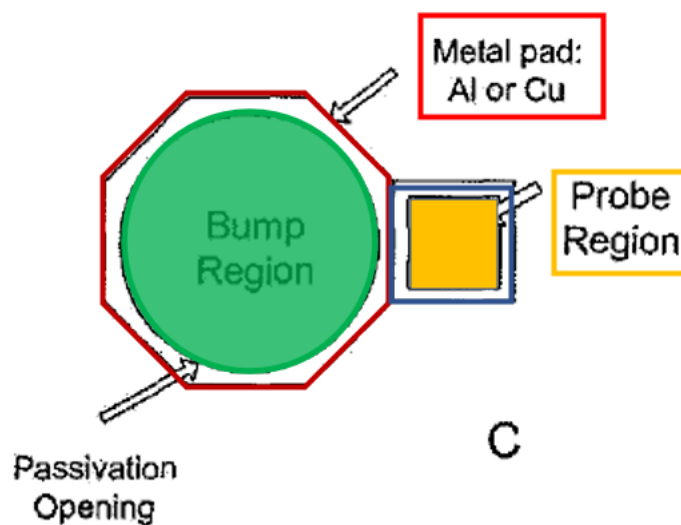
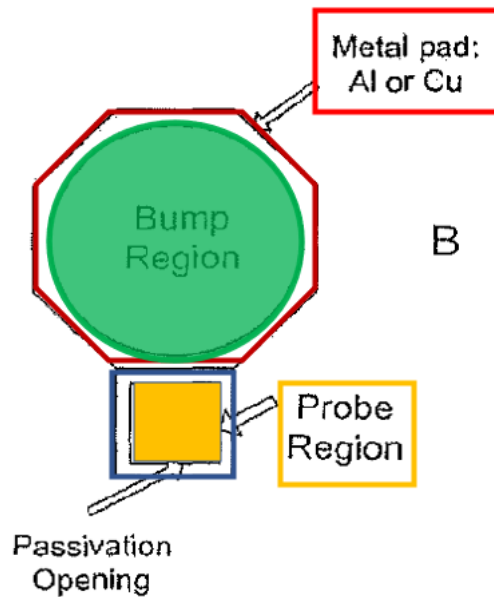


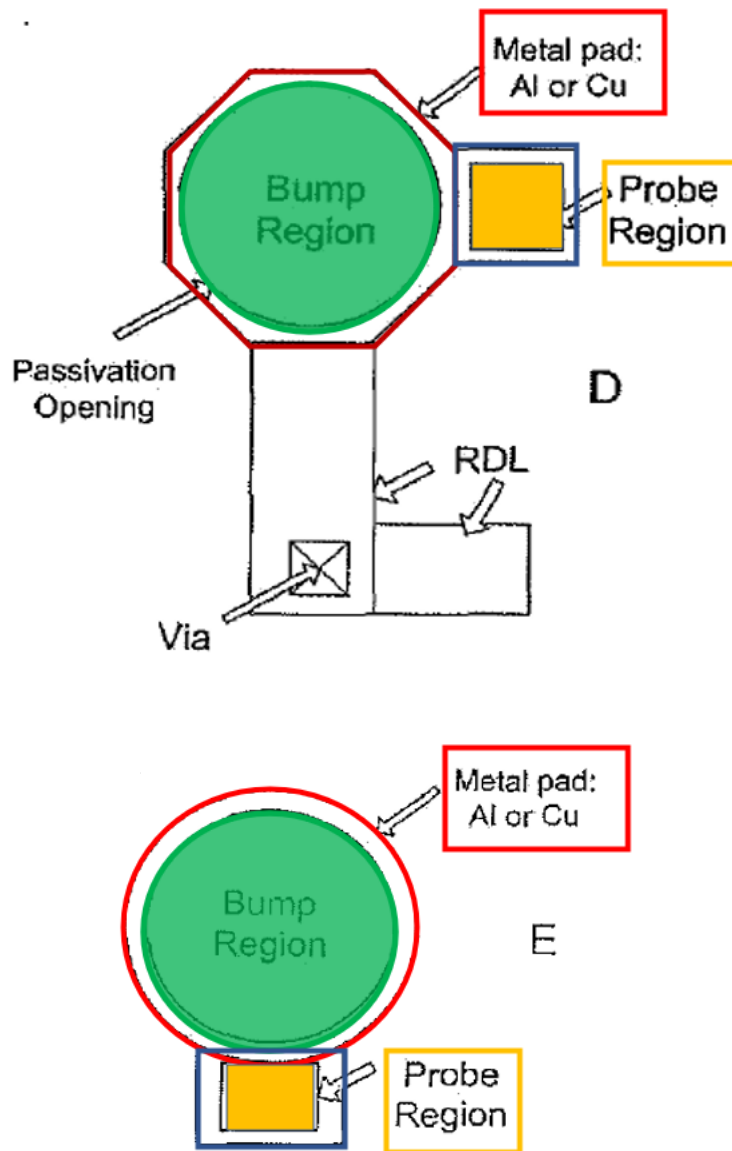


	 <p>The diagram shows a circular metal pad. Inside the pad, there is a green circular area labeled "Bump Region". Surrounding the bump region is a white ring. To the right of the bump region, there is a square area labeled "Probe Region". An arrow points from the text "Metal pad: Al or Cu" to the outer edge of the metal pad. The letter "E" is located to the right of the bump region.</p>
<p>[10b] a test pad integrally constructed with said bonding pad, said test pad being coplanar relative to said flip chip bonding pad and including a probe region for performing wafer-level testing prior to performing said bumping process;</p>	<p>The Invention Submission describes that openings are made in a passivation layer for the bump region and also in the test pad for the probe region: “<i>Fig. B shows a preferred embodiment of the present invention: a schematic diagram of a metal pad with a square (shown) or rectangular (not shown) probe region, integral with a separate octagonal (shown) bump region. Separate passivation openings for the respective probe and bump regions are also shown.</i>” The separate openings in the passivation layer demonstrate that the test pad and the bonding pad are coplanar. Further, an object the invention is to allow a wafer to be probed. The Invention Submission notes that in the prior art the probe region and bump region overlapped, meaning they were one in the same as shown in Figure A:</p>  <p>The diagram shows a circular metal pad. Inside the pad, there is a square area labeled "Probe and Bump Region". An arrow points from the text "Metal pad: Al or Cu" to the outer edge of the metal pad. Another arrow points from the text "Passivation Opening" to a small opening in the metal pad. The letter "A" is located to the right of the probe and bump region.</p>

The disclosed invention removed the overlap and created separate, non-overlapping regions. However, the new bump and probe regions disclosed remain in the same plane.

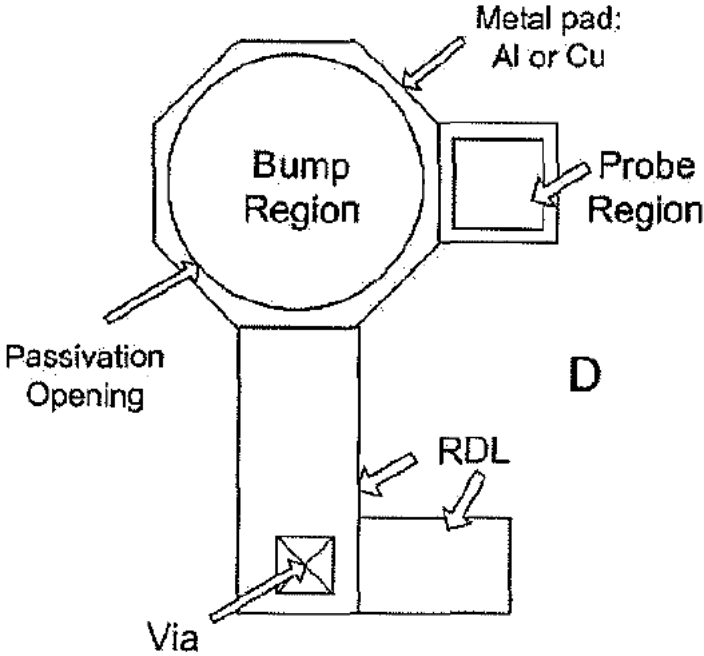
As shown in Figures B-E there is a probe region (annotated in orange) within the test pad (annotated in blue):





The Invention Submission provides that the disclosed structure allows for wafer-level testing a wafer prior to bumping:

“For devices made with flip chip technology, testing on Al or Cu pads prior to bumping to test the chip is not allowed because probe marks gouge the pad surface, making the deposition of under bump metallization (UBM) difficult and subsequent bumping processes

	<p><i>unreliable. Thus what is needed in the art is a method of allowing chips to be probed <u>prior to bumping</u> so that wafer level tests can be undertaken.”</i></p> <p><i>“The use of separate regions for bump formation and probing for testing wafers prior to bumping is easier and reliable.”</i></p>
<p>[10c] and a first metal redistribution layer electrically connected to said bonding and test pads, and being coplanar with one another, said first metal redistribution layer is electrically connected by way of a via to a second redistribution layer being disposed in a different plane than the first redistribution layer.</p>	<p>The Invention Submission provides that “Metal redistribution layers (RDL) are shown in Fig. D to connect the bump region to other metal runners or interconnect, to other pads, either directly or through vias (for example, one is shown in the illustration).” When the RDLs connect the bump region to other pads “through vias,” this occurs in a different plane because the vias are electrical connections between layers in that go through the plane of one or more adjacent layers. Figure D specifically demonstrate the use of vias to connect to other RDLs in different planes:</p> 

C. The Inventors Exercised Reasonable Diligence in Reducing the Invention to Practice

As noted above, the Invention Submission was stamped received by the Agere Patent Committee on May 10, 2004, and the '173 Patent was filed approximately four months later on September 29, 2004. Further, the patent application was originally assigned to Agere Systems, Inc. (Ex. 1001, Cover.)

Mr. Kouros Azimi served as the Chairman of the Agere Patent Committee from February 2004 to 2013. (Ex. 2004, ¶7.) Engineers at Agere would submit ideas for inventions stemming from their work on an invention submission form. (Ex. 2004, ¶8.) The invention submission forms were submitted either via email or in hard copy to the Agere Patent Committee. (*Id.*) Upon receipt by the patent staff, the invention submission form was stamped and (1) assigned a sequential submission number, (2) dated with the date received by the Agere patent committee, and (3) assigned to an in-house Agere attorney. (Ex. 2004, ¶9.)

The Agere Patent Committee met monthly, usually the second Wednesday of the month, to review invention submissions received from Agere engineers. (Ex. 2004, ¶10.) Generally, all invention submissions were compiled into a binder and distributed to committee members before each meeting. (Ex. 2004, ¶11.) The cutoff date to compile invention submission forms was generally one week before the actual meeting. (*Id.*)

If approved by the patent committee, an invention submission would be transmitted to Agere's outside prosecution counsel to prepare a draft application. (Ex. 2004, ¶12.) The transmission to outside prosecution counsel generally occurred within 1-2 weeks after approval by the patent committee. (Id.) Agere generally approved and referred dozens of submissions from each monthly patent review meeting to outside prosecution counsel to become patent applications. (Ex. 2004, ¶13.)

Once assigned, prosecution counsel would review the submission materials. (Ex. 2004, ¶14.) Depending on the materials provided by Agere, prosecution counsel would begin the drafting process (if they had sufficient information), or prosecution counsel might set up a meeting with the relevant engineers/inventor(s) to better understand a claimed invention before beginning the drafting process. (Id.) The drafting process was iterative, with drafts and comments exchanged between outside prosecution counsel on the one hand and in-house counsel and the engineer/inventors(s) on the other hand. (Ex. 2004, ¶15.) Once a patent application was complete, the managing in-house Agere attorney would make one final review of the application before it was filed with the Patent Office. (Ex. 2004, ¶16.) While times could vary depending on the complexity of the invention, on average, it took three months to complete the drafting process and convert an invention submission package into to final patent application. (Id.)

Agere designed and manufactured integrated circuits and was a global leader in semiconductors and software solutions for storage, mobility, and networking markets. (Ex. 2004, ¶¶3-6.) As part of its business, Agere had a licensing program, which provided a significant business and economic incentive to promptly file and protect all intellectual property and inventions developed at the company. (Ex. 2004, ¶6.)

Based on Mr. Azimi's testimony concerning the operation of the Agere Patent Committee, the Invention Submission (Ex. 2001) form was submitted to the committee on Monday, May 10, 2004. (*See also* Ex. 2004, ¶17 (acknowledging that Ex. 2001 is consistent with the form used by Agere in 2004). Given the cutoff for preparing invention disclosure forms, the Invention Submission at issue was discussed at the June 2004 Patent Committee meeting – June 9, 2004. The Invention Submission form would have been approved at the June 2004 meeting and then sent to outside prosecution counsel within 1-2 weeks, meaning outside counsel received relevant materials in late June 2004. (Ex. 2004, ¶18.) Over the next few months, draft applications would be prepared and discussed among outside prosecution counsel (Hitt Gaines), the inventors, and Mr. Fred M. Romano, the responsible in-house counsel at Agere. (Ex. 2004, ¶17.)

Further, Dr. Merchant, one of the co-inventors of the '173 Patent, has similar recollections of the workings of the Agere Patent Committee. (Ex. 2005; ¶¶3-12.)

To the best of Dr. Merchant's recollection, he and his co-inventors conceived of the ideas disclosed in the Invention Submission before May 10, 2004. (Ex. 2005; ¶7.) However, Dr. Merchant also states that the May 10, 2004 date on the invention submission is the date the document was received by the Agere Patent Committee. (Ex. 2005; ¶¶10.) Further, Dr. Merchant recollection aligns with the general operation and timeline described by Mr. Azimi. (Ex. 2005; ¶¶11-12.) Further, Dr. Merchant, while not having specific documents or recollection concerning the draft of the '173 application (because he is a named inventor on over 135 U.S. patents) states that his practice has been, and continues to be, to review all draft applications, and work interactively with prosecution counsel, before an application is filed. (Ex. 2005; ¶¶13.)

Given the testimony of Dr. Merchant and Mr. Azimi, Patent Owner has established reasonable diligence. Agere had a business incentive to file patent applications to protect its intellectual property promptly. The application was filed three months after the Agere Patent Committee approved it. This amount of time is reasonable and expected for an application to be drafted, reviewed, and revised before submission.

The Board has found that corroborating evidence such as that submitted here to be sufficient to establish reasonable diligence. *See LG Electronics, Inc. et al. v. Wi-Lan Inc. et al.*, IPR2018-00704, Paper 4 at 11 (PTAB Sept. 5, 2018) (denying

institution where inventor’s testimony of diligence was corroborated by testimony from the “co-lead of NextWave’s patent program”); *Cf Arctic Cat Inc. v. GEP Power Prod., Inc.*, 919 F.3d 1320, 1332 (Fed. Cir. 2019) (finding no lack of diligence and stating “Lack of diligence cannot be inferred from putting the invention into someone else’s hands for needed testing and awaiting test results for a short period commensurate with the testing need, at least where oversight was diligent. That course of action, as a way of reducing an invention to practice, does not give rise to an inference of unreasonable delay or abandonment of the invention.”).

VII. GROUND 2: *MARDI* CANNOT BE COMBINED WITH THE KNOWLEDGE OF A POSITA

Petitioners seek to combine *Mardi* with the knowledge of a POSITA for a very limited set of limitations or purported knowledge under 35 U.S.C. § 103. (Pet., 2.) Specifically:

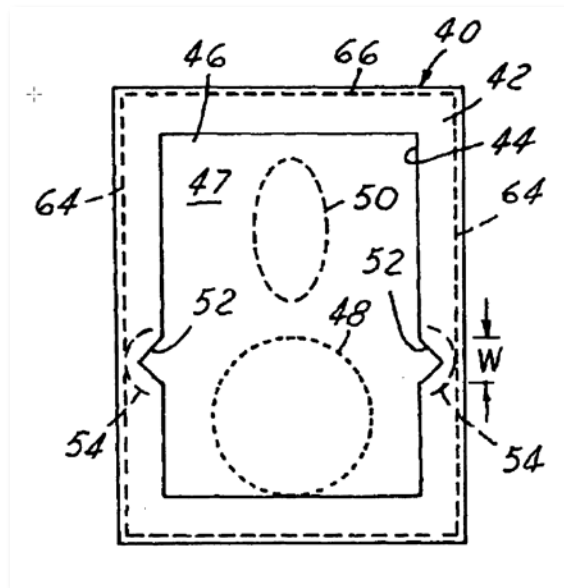
- Claim 1: the “wafer level testing” limitation (Pet., 42-44);
- Dependent Claim 5 (Pet., 44);
- Dependent Claim 6: that vias can connect redistribution layers (Pet., 48);
- Claim 9: “wafer test” (Pet., 49); and
- Claim 10: “performing wafer level testing” (Pet., 49).

Petitioners do not argue that all claim limitations are disclosed by a POSITA or within the purported knowledge of a POSITA. For the vast majority of the limitations, Petitioners rely solely on the disclosure in *Mardi*. More importantly, as shown above, *Mardi* is not prior art because the Invention Submission predates the *Mardi* reference. Thus, to the extent Petitioners purport to combine *Mardi* with the knowledge of POSITA under 35 U.S.C. § 103, such an argument is legally unsustainable because *Mardi* is not a § 102 reference and does not predate the inventors' conception of the disclosed invention. *See* 35 U.S.C. § 103(a) (2012) (“A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the **prior art** are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains.”) (emphasis added); *Lightwave Techs., Inc. v. Corning Glass Works*, No. 86 CIV. 759 (KC), 1991 WL 4737, at *5 (S.D.N.Y. Jan. 18, 1991) (“For similar reasons, the fibers were not admissible on the question of obviousness under 35 U.S.C. § 103. Specifically, because the fibers were not prior art under Section 102, they could not be considered under Section 103.” (citing 2 D. Chisum, *Patents* § 5.02[3] (1990))); *Orthman Mfg., Inc. v. Chromalloy Am. Corp.*, 512 F. Supp. 1284, 1293 (C.D. Ill. 1981) (“Section 102 defines what is and what is not prior art, for the purpose of applying the

obviousness test of 35 U.S.C. § 103.”); *Application of Faust*, 378 F.2d 966, 969 (C.C.P.A. 1967) (“The Faust reference, as a matter of present law, is not ‘prior art.’ Accordingly, no inquiry under section 103 may be made.”)

VIII. GROUND 3: PETITIONERS FAIL TO DEMONSTRATE *LIN* ANTICIPATES

Lin teaches a “bond pad” having a “generally elongated, rectangular configuration with a wire bonding area at one end and a probe needle contact area at the other end of the pad.” (Ex. 1006, Abstract; *see also id.* at 4:17-20.) Further, *Lin*’s Figure 5 “is a top down view of a bonding pad of the present invention, illustrating separate wire binding and probe needle areas on the chip” (Ex. 1006, 3:65-67, Fig. 5):



The concept of elongated bonding pads with separate regions was known when filing the '173 Patent. Indeed, the inventors specifically discuss a paper by

Yong, et al. (the “*Yong Paper*”) (Ex. 2006), which discusses elongated bond pads with separate regions, in the ’173 specification:

One approach proposed for wire bond connections, and hence of little practical use for semiconductors involving flip chip connections, is described in IEEE publication titled “Electronic Components and Technology Conference”, at page Nos. 1323–1329, May 2003 in paper by Lois [sic] Young et al. This approach generally requires stacking at least two physically different metal pads over one another in order to form a probe region that is separate from a wire bond region. More specifically, this proposed approach requires stacking a portion of an enlarged aluminum cap over a copper pad disposed beneath the aluminum cap. A remaining portion of the enlarged aluminum cap (e.g., where the probe region is located) is disposed over a dielectric material and this arrangement may lead to cracks in the dielectric since the probe can apply a high force over the probe region. Moreover, the specific requirement of an Al “capping pad” over a copper pad is not a mere design choice since performing wire bonding to copper is generally very difficult for a production environment involving wire bond connections. No Such considerations are applicable for flip chip connections.

(Ex. 1001, 2:5-25; *see also* Ex. 1002, 144 (evidencing examiner consideration of *Yong Paper*).)

The *Yong Paper* discloses the same elongated bond pad with separate probe and wire bond pad regions that Petitioners rely on in *Lin*:

To overcome the difficulty of wire bonding onto readily oxidized copper bond pads, capping copper bond pads with aluminum has been the industry standard remetalization for wire bonding of a copper technology. In terms of wafer level testing and packaging, the resulting fine pitch geometry has created challenges for both cantilever probe and wire bond processes. Pad damage due to probe marks has been shown to cause “non-sticks” and “lifted bonds” at wire bonding. The wire bond yield loss due to pad damage is aggravated for fine pitch since increasingly smaller bonded ball diameters are formed on top of the same damage area caused by the probe mark. Wire Bond parameter optimization can minimize wire bond yield loss but cannot eliminate the problem. One logical solution is to lengthen the bond pad to create separate regions for probing and wire bonding. However, this method can result in a larger die size.

(Ex. 2006, 1). The *Yong Paper*’s Figures 2 and 4 confirm the overlapping and cumulative disclosure with *Lin*:

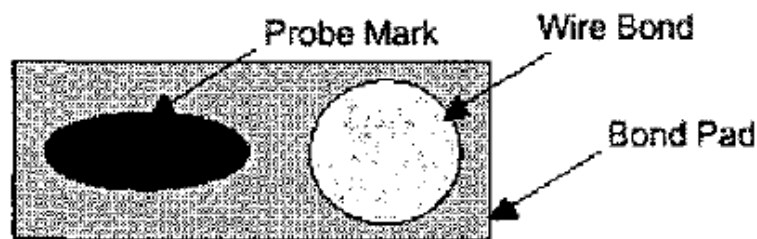


Figure 2: Bond Pad with Separate Probe and Wire Bond Regions

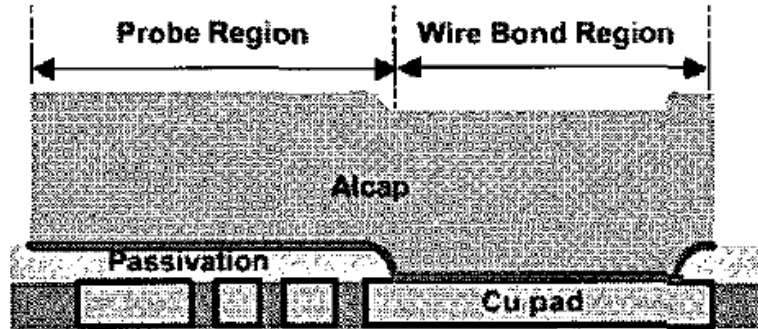


Figure 4: Cross-section of New Bond Pad with Separate Probe and Wire Bond Regions without Increasing Die Size

A. The Board Should Deny Institution Under 325(d) Because the Examiner Considered the Similar Prior Art and Arguments

IPR institution is discretionary. *See SAS Inst. v. Iancu*, 138 S. Ct. 1348, 1356 (2018). “In determining whether to institute or order a proceeding..., the Director may take into account whether, and reject the petition or request because, the same or substantially the same prior art or arguments previously were presented to the Office.” 35 U.S.C. § 325(d).

The Board weighs several non-exclusive factors when determining whether to deny institution, including the following:

- a) the similarities and material differences between the asserted art and the prior art involved during examination;
- b) the cumulative nature of the asserted art and the prior art evaluated during examination;
- c) the extent to which the asserted art was evaluated during examination, including whether the prior art was the basis for rejection;

- d) the extent of the overlap between the arguments made during examination and the manner in which Petitioner relies on the prior art;
- e) whether Petitioner has pointed out sufficiently how the Examiner erred in its evaluation of the asserted prior art; and
- f) the extent to which additional evidence and facts presented in the Petition warrant reconsideration of the prior art or arguments.

Becton, Dickinson & Co. v. B. Braun Melsungen AG, IPR2017-01586, Paper 8 at 17 (PTAB Dec. 15, 2017). “If, after review of factors (a), (b), and (d), it is determined that the same or substantially the same art or arguments previously were presented to the Office, then factors (c), (e), and (f) relate to whether the petitioner has demonstrated a material error by the Office.” *Advanced Bionics, LLC v. MED-EL Elektromedizinische Geräte GmbH*, IPR2019-01469, Paper 6, at 10 (Feb. 13, 2020) (precedential). Importantly, “Section 325(d) is phrased in the disjunctive (‘or’), not the conjunctive (‘and’), when it refers to ‘whether...the same or substantially the same prior art *or* arguments previously were presented to the Office.’ 35 U.S.C. § 325(d). Section 325(d) does not require previous presentation of the same art *and* arguments.” *Edge Endo, LLC v. Michael Scianamblo*, IPR2018-01320, Paper 15 at 12 (PTAB Jan. 14, 2019) (emphasis in original).

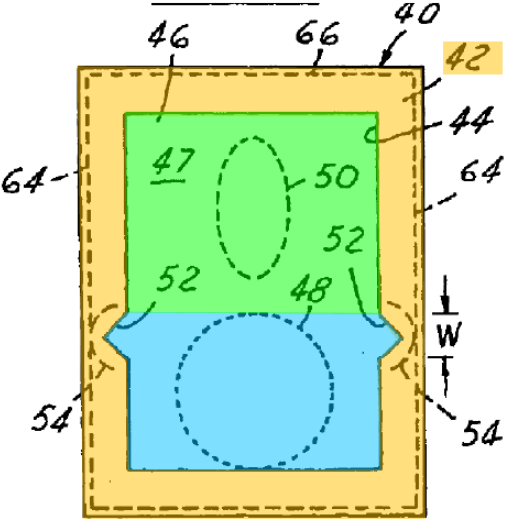
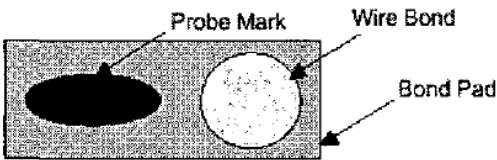
1. Factors (a), (b), & (d) – Similar Art and Arguments Used in the Petition were Previously Presented to the Office

Here, factors (a), (b), and (d) weigh in favor of denial because the same *Yong Paper* was of record during prosecution and is explicitly discussed in the ‘173 specification. Since *Lin* is duplicative of what is disclosed in the *Yong Paper*,

it is cumulative of the arguments and art before the Patent Office. Thus, the arguments presented in the Petition are largely the same as the arguments that were already considered—and rejected— by Patent Office.

a. The Examiner Considered Similar Art

The Board should exercise its discretion and decline to institute on Grounds 3-5 because the disclosure Petitioners rely on in *Lin* overlap with the *Yong Paper*. As shown on the chart below, the elements of *Lin* relied on by Petitioners are disclosed in the *Yong Paper*.

<i>Lin</i>	<i>Yong Paper</i>
<p>Relied on by Petitioners:</p>  <p>FIG. 5</p> <p>(Pet., 50, 52, 54.)</p>	<p>The <i>Yong Paper</i> contains a figure disclosing the same information relied on by Petitioners:</p>  <p>Figure 2: Bond Pad with Separate Probe and Wire Bond Regions</p>
1[a] According to Petitioners:	The <i>Yong Paper</i> discloses a bond pad with two separate regions:

“The bottom half of “bonding pad 46...corresponds to the claimed “flip chip bonding pad.” First, marks 52 in Figure 5 delineate the boundaries between **wire bonding area 48** and the **probe contact area 50** of bonding pad 46 (Pet. 52.)

“One logical solution is to lengthen the bond pad to create separate regions for probing and wire bonding” (Ex. 2007, 1.)

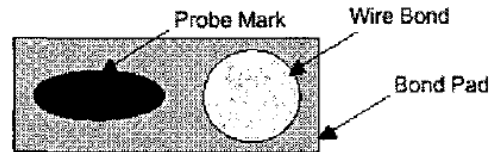


Figure 2: Bond Pad with Separate Probe and Wire Bond Regions

“The solution to eliminate issues due to the interaction between the probe mark and the wire bond is to create separate regions on the bond pad for probing and wire bonding. With separate regions, the probe process can be optimized to maintain the lowest contact resistance with the bond pad without limiting the probe mark size to facilitate good wire bonding.” (Ex. 2007, 2.)

1[b] According to Petitioners:

“The ‘test pad’ (**green area**) and the ‘bonding pad’ (**blue area**) are integrally constructed without interconnect testing lines.” (Pet., 55.)

The *Yong Paper* discloses a bond pad with separate probe and wire bond regions that are integrally constructed without interconnect test lines, as argued by Petitioners.

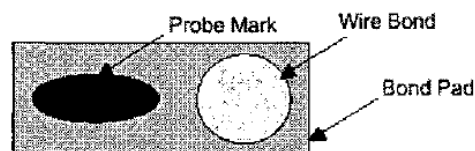


Figure 2: Bond Pad with Separate Probe and Wire Bond Regions

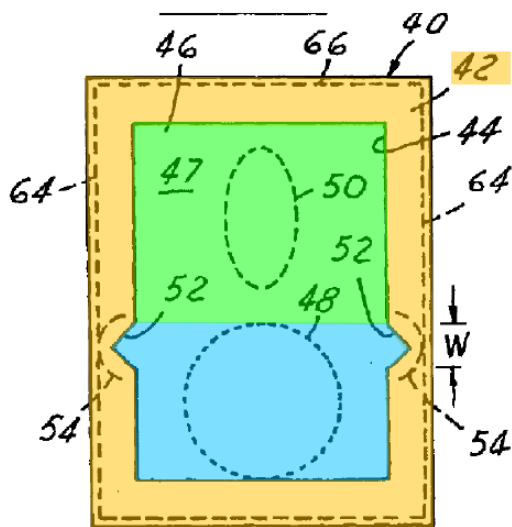


FIG. 5

1[c] According to Petitioners:

“The ‘test pad’ (**green area**) and the ‘bonding pad’” (**blue area**) are coplanar because they are simply separate areas of the metal bonding pad 46: ‘[T]he **wire bonding area 48** and the **probe needle contact area 50** are located in separate, non overlapping areas on the surface 47 of the bonding pad 46.’” (Pet., 55.)

The *Yong Paper* shows the probe and wire bond regions are separate areas of the metal bond pad, as argued by Petitioners.

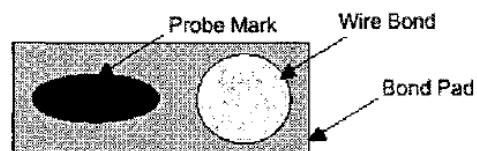


Figure 2: Bond Pad with Separate Probe and Wire Bond Regions

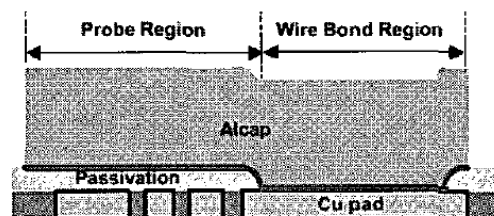


Figure 4: Cross-section of New Bond Pad with Separate Probe and Wire Bond Regions without Increasing Die Size

1[d] According to Petitioners:

“during the parametric testing procedure, the tip of each **probe**

The *Yong Paper* discloses testing using probe tips that contact the bonding pad, as argued by Petitioners:

<p>needle 68 contacts the probe needle contact area 50 of the corresponding bonding pad [46] [Fig. 6] and forms a scrub mark 58 and a hump 60 of pad material in the bonding pad 46 [Fig. 8], as further shown in FIGS. 6 and 8.” (Pet. 55.)</p>	<p>“Cantilever probe technology has long been the most widely used and cost effective method of conducting wafer level Testing”</p> <p>“One of the primary issues is the interaction between the probe mark and the wire bond. The probe mark is the indentation left on the bond pad due to contact between the cantilever needle and the bond pad....For closely spaced and small bond pads, it has become increasingly difficult to control the size, location, and consistency of the probe mark. This creates significant damage on the bond pad, which results in difficulty of forming a bond during wire bonding. The resulting failure modes are ‘non-stick’ during wire bonding, and ‘lifted bond’ resulting in ‘low ball shear strength’ during the ball shear test.”</p> <p>(Ex. 2007, 1.)</p>
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Because there is extensive overlap between *Lin* and the *Yong Paper* before the Examiner, Petitioners’ reliance on *Lin* is cumulative, and institution should be denied.

b. The Examiner Considered Art Cumulative of *the Yong Paper*

The Board should exercise its discretion and decline to institute on Grounds 3-5 because they rely on *Lin*, which is cumulative of the *Yong Paper*. As described above, the portions of *Lin* relied on by Petitioners, and Petitioners’ attendant

arguments, are cumulative of what is disclosed in the *Yong Paper*, which was considered during the original examination. Because the Petition relies on *Lin* for the same teachings before the Examiner, via the *Yong Paper*, the Board should deny institution.

2. Factors (c), (e), and (f) – Petitioners Have Not Persuasively Shown that the Office Committed Material Error When Allowing the Claims

Under the second part of the *Becton, Dickinson* framework, factor (c) “informs . . . petitioner’s showing under factors (e) and (f), which focus on the petitioner’s evidence of previous Office error regardless of the context in which the same or substantially the same art or arguments were previously presented.”

Advanced Bionics, at 10.

Here, the Petition not only fails to point out how the Examiner erred, but it also fails even to acknowledge the Examiner’s evaluation of cumulative prior art. Indeed, the Petition does not even address 325(d) as it relates to cumulative art. Accordingly, factors (c), (e), and (f) favor denial.

B. Lin Does Not Disclose Key Limitations

Independent claim 1 requires: “said test pad being coplanar relative to said flip chip bonding pad and including a probe region for performing wafer-level testing prior to performing said bumping process.” (Ex. 1001, 4:5-8.)

The requirement that the prior art elements themselves be “arranged as in the claim” means that claims cannot be “treated ... as mere catalogs of separate parts, in disregard of the part-to-part relationships set forth in the claims and that give the claims their meaning.” *Lindemann Maschinenfabrik GMBH v. Am. Hoist & Derrick Co.*, 730 F.2d 1452, 1459 (Fed. Cir. 1984). “[U]nless a reference discloses within the four corners of the document not only all of the limitations claimed but also all of the limitations *arranged or combined in the same way as recited in the claim*, it cannot be said to prove prior invention of the thing claimed and, thus, cannot anticipate under 35 U.S.C. § 102.” *Net MoneyIN, Inc. v. VeriSign, Inc.*, 545 F.3d 1359, 1371 (Fed. Cir. 2008) (emphasis added).

For the “wafer-level testing prior to performing said bumping process” requirement, the Petition points to *Lin* at Col. 5:31-35 (Pet., 55), which states:

As shown in FIG. 8, during the parametric testing procedure, the tip of each probe needle 68 contacts the probe needle contact area 50 of the corresponding bonding pad 44 and forms a scrub mark 58 and a hump 60 of pad material in the bonding pad 46, as further shown in FIGS. 6 and 8.

Nothing in this section of the *Lin* specification discusses wafer-level testing.

The Petition then points to *Lin* at Col. 2:25-27, which states: “Prior to packaging and formation of the bonding balls 10 on the respective bonding pads

14, **the chip 26** is Subjected to parametric testing...” (emphasis added). (Pet. 55-56.) Once again, there is no reference in the Petition to “wafer level testing.” Rather, the Petition appears to make an argument about individual chip testing. Further, *Lin* repeatedly refers to testing a “chip,” **not** a wafer, and only discloses “a chip” in its figures. (See Ex. 1006, Fig. 5-8, 4:15-17 “for contact of a probe needle during chip testing and bonding of bond wires to the chip,” 5:18-45 (discussing testing “the chip.”)).

Petitioners also improperly conflate the “parametric testing” in *Lin* with the “wafer-level testing” discussed in the ‘173 Patent. Specifically, *Lin* states that a chip “is subjected to parametric testing which **utilizes test structures** to assess the electrical characteristics and reliability of the devices on the wafer.” (Ex. 1006, 2:27-30 (emphasis added).) A key point in that passage is the use of separate “test structures” to test the chip, not the elongated bond pads with two regions described in *Lin*. It is the bond pads that are used for wafer-level testing in the ‘173 Patent. The “test structures” used for *Lin*’s Parametric testing are different. Specifically, parametric testing involves data pertaining to the semiconductor fabrication process and utilizes test structures in the scribe lines. It is not testing chip functionality through the bond pads, which is taught in the ‘173 Patent. (See Ex. 2007, [0012] (“to collect parametric data pertaining to the wafer fabrication process. As part of this process, metal probe tips of a probe tester are placed in

contact with the test structures located in the scribe grid 118 and the corresponding test structure circuitry is stimulated via the metal probe tips.”); Ex. 2008, 2-3(“The purpose of **parametric test** is to determine the characteristics of a semiconductor manufacturing process...It is important to understand that parametric test is almost never performed on final products. Instead, it is performed on **special structures** that are designed to yield information about the process itself. In production test the parametric test structures are sometimes located in the scribe lanes or “streets” of the wafer to minimize the wafer area taken up by these devices.”) (emphasis added).) Thus, Petitioners failed to establish that *Lin*’s “parametric testing is the same “wafer-level testing” taught in independent claims 1, 9, and 10 of the ’173 Patent. At best, *Lin*’s “parametric” testing is ambiguous and cannot support institution. See *Boston Scientific Neuromodulation Corp. v. Nervo Corp.*, IPR2015-01203, Paper 10, at 13 (PTAB Nov. 30, 2015) (denying institution and citing “*In re Hughes*, 345 F.2d 184 (CCPA 1965) (an ambiguous reference cannot serve as an anticipation)”); *In re Brink*, 419 F.2d 914, 917 (CCPA 1970) (“[I]f a reference is ambiguous and can be interpreted so that it may or may not constitute an anticipation of an appellant’s claims, an anticipation rejection under 35 U.S.C. § 102 based upon the ambiguous reference is improper.”)

Next, it is worth noting that the Petition improperly combines different sections of *Lin* to cobble together its argument. See, e.g., *Reactive Surfaces Ltd.*,

LLP, v. Toyota Motor Corp., IPR2018-01194, Paper 11 at 23 (PTAB Dec. 10, 2018) (denying institution in part where “Petitioner points to disparate disclosures in Schneider to cobble together teachings concerning the various limitations of the challenged claims.”) Specifically, the section from *Lin* Col. 5:31-35 is excerpted from the section entitled “Description of the Preferred Embodiments,” while the rest comes from a description of Figure 2, which *Lin* expressly labels “Prior Art.” (Ex. 1001, Fig. 2.) In other words, Petitioners violate the Federal Circuit’s long-standing precedent that, to establish anticipation, the challenger must show that all of the elements are disclosed and arranged in the same order. Such is not the case with *Lin*.

Further, Petitioners cite a portion of *Lin* at 2:61-62, which states: “Another object of the present invention is to provide a method which enhances wafer sort yield and productivity by relaxing probe mark Specifications in the testing of chips.” While Petitioners bolden the word “Wafer” in the Petition, this section states nothing about “wafer-level testing” and, therefore, does not advance Petitioners’ argument.

Finally, claim 9 contains a similar limitation, specifically: “test pad including a probe region for performing a wafer test prior to performing said bumping process.” Petitioners cite back to and rely on the same evidence from

claim 1[d]. (Pet., 62.) Petitioners’ arguments fail for the same reasons described above.

Since *Lin* does not disclose the “wafer-level test” element of independent claims 1 and 9, dependent claims 2-8 are also not anticipated by *Lin*.

IX. GROUND 4: *LIN* CANNOT BE COMBINED WITH KNOWLEDGE OF A POSITA

As discussed above, *Lin* does not disclose “wafer-level testing” as recited by Claim 1 of the ’173 Patent. To address this shortcoming, Petitioners rely on the alleged knowledge of a POSITA. Petitioners’ argument fails for several reasons.

First, Petitioners do not attempt to show that the wafer-level testing referred to in the “discussion citing Nelson, Farnsworth, Eldridge, and Yu” (Pet., 74) is the same wafer level testing in *Lin*, much less the “wafer-level testing” performed “prior to performing said bumping process” that is claimed in the ’173 patent. (*See* Ex. 1001 at Claims 1, 9, and 10.)

Second, this argument is flawed because it relies on the prior patent claims as a roadmap. In other words, the Petition seeks to merely establish that certain elements may have been known in the art. However, established precedent is clear that a more is needed because “[a] patent composed of several elements is not proved obvious merely by demonstrating that each of its elements was, independently, known in the prior art.” *Man Wah Holdings Ltd. v. Raffel Systems, LLC*, IPR2019-00616, Paper No. 7 at 22 (PTAB Aug. 21, 2019) (*citing KSR*, 550

U.S. at 418); *Orexo AB v. Actavis Elizabeth LLC*, 903 F.3d 1265, 1273 (Fed. Cir. 2018) (“The question is not whether the various references separately taught components of the [challenged claims], but whether the prior art suggested the selection and combination achieved by the [challenged claims’] inventors.”); *Personal Web Techs., LLC v. Apple, Inc.*, 848 F.3d 987, 993–94 (Fed. Cir. 2017) (“that reasoning seems to say no more than that a skilled artisan, once presented with the two references, would have understood that they could be combined. And that is not enough: it does not imply a motivation to pick out those two references and combine them to arrive at the claimed invention.”).

Further, all obviousness challenges in IPRs “*must* address the Graham factors.” *Eizo Corp. v. Barco N.V.*, IPR2014-00358, Paper 11, at 29-30 (PTAB July 23, 2014). For example, the Board faulted the petitioner in *Eizo* for failing to identify the differences between the claimed subject matter and the prior art. *Id.* In particular, the Board found insufficient the petitioner’s “conclusory assertion” that “[t]o the extent [the first reference] may not explicitly teach” the limitation, the second reference “explicitly teaches this limitation.” *Id.* at 30. Other Board decisions have reached the same result. *See, e.g., Moses Lake Indus., Inc. v. Enthone, Inc.*, IPR2014-00243, Paper 6, at 18 (PTAB June 18, 2014); *Moses Lake Indus., Inc. v. Enthone, Inc.*, IPR2014-00246, Paper 6, at 17 (PTAB June 18,

2014); *eBay, Inc. v. Paid, Inc.*, No. CBM2014-00125, Paper 15, at 21 (PTAB Sept. 30, 2014).

Moreover, an obviousness inquiry “is based on factual inquiries including the differences between the claimed invention and the prior art.” *Travelocity.Com v. Cronos Tech.*, CBM2014-00082, Paper 10, at 20 (PTAB Sept. 15, 2014). Thus, identifying the differences between the claimed invention and the prior art is critically important, and the Board has cautioned that a petitioner who fails to state the differences between the claimed invention and the prior art risks having their obviousness grounds denied institution. *Liberty Mutual Ins. Co. v. Progressive Casualty Ins. Co.*, CBM 2012-00003, Paper 7, at 2-3 (PTAB Oct. 25, 2012).

In *Travelocity*, the Board declined institution on obviousness grounds because the petitioner failed to specifically identify the differences between the recited invention and the prior art. *Travelocity*, CBM2014-00082, Paper 10, at 20. The Board stated “[w]ithout having identified specifically the differences between the recited invention and the prior art, Petitioner has failed to make a meaningful obviousness analysis under 35 U.S.C. § 103(a), and, thus, has failed to establish that it is more likely than not that” the independent claims are unpatentable on obviousness grounds. *Id.*

Here, Petitioners similarly fail to identify any differences between the relied upon prior art references and the claimed invention. The Petition also fails to

acknowledge the importance of the *Graham* factors, or even *mention Graham at all*. Absent such discussions and critical analysis, Petitioners have failed to “make a meaningful obviousness analysis” under 35 U.S.C. § 103(a). Institution should be declined for this reason alone. *See Personal Web*, 848 F.3d at 993-94 (“that reasoning seems to say no more than that a skilled artisan, once presented with the two references, would have understood that they could be combined. And that is not enough: it does not imply a motivation to pick out those two references and combine them to arrive at the claimed invention.”).

The Petitioners and their expert merely assert, in conclusory fashion, that some unspecified form of wafer-level testing provides generalized reductions in manufacturing costs (Pet., 64.) without any attempt to provide the analytical underpinning required by Federal Circuit precedent. The Federal Circuit has rejected such generic rationales. *See TQ Delta, LLC v. CISCO Sys., Inc.*, 942 F.3d 1352, 1360 (Fed. Cir. 2019):

The challenger’s expert further testified that:

The motivation to combine would be because you wanted to build something better. You wanted a system that was more efficient, cheaper, or you wanted a system that had more features, makes it more attractive to your customers, because by combining these two things you could do something new that hadn’t been able to do before.

... We rejected this testimony because it “fail[ed] to explain why a person of ordinary skill in the art would have combined elements from specific references *in the way the claimed invention does.*” *Id.* (first citing *KSR*, 550 U.S. at 418, 127 S.Ct. 1727; then citing *Innogenetics*, 512 F.3d at 1373). We explained that “[k]nowledge of a problem and motivation to solve it are entirely different from motivation to combine particular references.” *Id.* (quoting *Innogenetics*, 512 F.3d at 1373).

Thus, the Petitioners’ argument amounts to nothing more than impermissible hindsight bias. *KSR*, 550 U.S. at 421 (“A factfinder should be aware, of course, of the distortion caused by hindsight bias and must be cautious of arguments reliant upon *ex post* reasoning.”). Thus, the Petition fails to make a threshold showing of a *prima facie* case of obviousness based on the knowledge of a POSITA and *Lin*.

X. GROUND 5: *LIN* WITH *YONG*

The Petition only relies on the combination of *Lin* and *Yong* for dependent claims 5-6. (see Pet., 73-80.) However, as it pertains to claim 1, the Petition is clear that only *Lin* is relied on for Ground 1: “As noted above in Ground 3, *Lin* [allegedly] discloses every element of claim 1.” (Pet. 73.) For the same reasons discussed above in connection with Ground 3, *Lin* does not disclose the claimed “wafer level testing” element.

As an initial matter, *Lin* should not be combined with *Yong* for all of the reasons set forth in Section VIII. Further, Petitioners attempt to improperly incorporate a significant portion of its expert declaration by reference: “*Yong* [allegedly] discloses every element of claim 1. Ex. 1008, ¶¶159-173.”) (Pet., 73.) Importantly, there are no arguments *in the Petition* regarding how *Yong* allegedly teaches any elements of claim 1.

The Petition’s incorporation by reference tactics are inappropriate, and the Board has consistently held that reference to other documents for substantive arguments and evidence not detailed in the Petition violates the Board’s rule against incorporation by reference: “Arguments must not be incorporated by reference from one document into another document.” 37 C.F.R § 42.6(a)(3). The Board has invoked this rule repeatedly over time as the basis to deny institution, and Petitioners have been specifically chastised for not adhering to the Board’s rules. *See Delphi Technologies, Inc. v. Microchip Technologies Inc.*, IPR2017-00970, Paper 12 at 20-21 (PTAB Sept. 13, 2017) (stating that having to refer to an expert declaration to understand the arguments in a petition is improper and provides sufficient reason on its own to deny institution); *see also e.g., Fidelity National Information Services, Inc. v. Datatrans Corp.*, IPR2014-00489, Paper 9 at 9 (PTAB Aug. 13, 2014) (“Under our rules, the petition must contain a ‘full statement of the reasons for the relief requested, including a detailed explanation of

the significance of the evidence’ 37 C.F.R. § 42.22(a)(2). We, therefore, decline to consider information presented in a supporting declaration, but not discussed sufficiently in a petition”); *Cisco Sys., Inc. v. C-Cation Techs., LLC*, IPR2014-00454, Paper 12 at 7-10 (PTAB Aug. 29, 2014) (Informative) (noting that “[o]ne purpose of the prohibition against incorporation by reference is to eliminate abuses” of the page limits established for the parties’ substantive papers, and that citing “large portions of another document, without sufficient explanation of those portions, amounts to incorporation by reference”); *2Wire, Inc. v. TQ Delta LLC*, IPR2015-00239, Paper 18 at 10 (PTAB May 29, 2015) (denying institution and stating “Dr. Jacobsen’s analysis is not reflected in the Petition itself, and cannot be incorporated in the Petition by reference... Consequently, we do not consider information presented in the Declaration but not discussed sufficiently in the Petition.”); *Apple Inc. v. ContentGuard Holdings, Inc.*, IPR2015-00451, Paper 9 at 10 (PTAB July 13, 2015) (denying institution and stating “[T]he Petition generally does not stand on its own, and its arguments often are incomprehensible without reviewing broad portions of the Dr. Sherman Declaration, the length of which exceeds the relevant discussion in the Petition by multitudes. The Petition’s practice of . . . using the Declaration to vastly expand its thin analysis and reasoning violates our rules in two respects...”); *Whole Space Industries Ltd., v. Zipshade Industrial (B.V.I.) Corp.*, IPR2015-00488, Paper 14 at 13 (PTAB July 24,

2015) (“Arguments and information that are not presented and developed in the Petition, and instead are incorporated by reference to the Judkins Declaration, are not entitled to consideration.”); *Microsoft Corp. v. Bradium Technologies LLC*, IPR2015-01435, Paper 15 at 29 (Dec. 23, 2015) (denying institution and stating “we will not consider arguments that are not made in the Petition, but are instead incorporated by reference to the cited paragraphs and claims charts of Dr. Michalson’s Declaration.”); *Facebook, Inc. et al. v. Uniloc USA, Inc. et al.*, IPR2017-01524, Paper 7 at 29 (PTAB Dec. 4, 2017) (denying institution and stating “[w]e need not consider assertions and information that are not presented and developed in the Petition, and instead are incorporated by reference to Dr. Lavian’s Declaration.”); *SK Hynix Inc., et al. v. Netlist, Inc.*, IPR2017-00649, Paper 9 at 7 (PTAB Dec. 4, 2017) (“Petitioner in this proceeding is limited to the arguments it makes in the Petition in this IPR not arguments made in another Petition or interpretations of those arguments (made in another Petition) in the Decision to Institute in another IPR.”).

The rules require a detailed discussion of the arguments and evidence upon which it relies *in the petition*. See, e.g., *DeSilva v. DiLeonardi*, 181 F.3d 865, 866–67 (Fed. Cir. 1999) (“A brief must make all arguments accessible to the judges, rather than ask them to play archeologist with the record.”); *A.C. Dispensing Equip. Inc. v. Prince Castle LLC*, IPR2014-00511, Paper 16 at 5–6 (PTAB Sep. 10,

2014) (“Petitioner should not expect the Board to search the record and piece together the evidence necessary to support Petitioner’s arguments.”).

Since Petitioners do not provide any analysis of *Yong* in the petition, none can be considered.

Finally, Petitioners assert that the purported combination of *Lin* and *Yong* allegedly teach all of the limitations of claim 10 of the ’173 Patent. (Pet., 81-82). However, for the “wafer-level testing prior to a bumping process” limitation, the Petition only relies on *Lin*. (Pet., 81 at Element 10[d].) *Lin* does not teach this limitation for the same reasons discussed above in connection with Ground 3.

XI. THE BOARD SHOULD DECLINE INSTITUTION BECAUSE THE PETITIONERS FAILED TO ADDRESS THE *GRAHAM* FACTORS OR STATE THE DIFFERENCES BETWEEN THE CLAIMED INVENTION AND ANY OF THE PRIOR ART FOR GROUNDS 2, 4 AND 5.

Petitioners argue that the challenged claims are obvious based on several combined references and the alleged general knowledge of a POSITA (Grounds 2 and 4) and the alleged combination of *Lin* and *Yong* (Ground 5). Significantly, all obviousness challenges in IPRs “*must* address the Graham factors.” *Eizo Corp. v. Barco N.V.*, IPR2014-00358, Paper 11, at 29-30 (PTAB July 23, 2014). For example, the Board faulted the petitioner in *Eizo* for failing to identify the differences between the claimed subject matter and the prior art. *Id.* In particular, the Board found insufficient the petitioner’s “conclusory assertion” that “[t]o the

extent [the first reference] may not explicitly teach” the limitation, the second reference “explicitly teaches this limitation.” *Id.* at 30. Other Board decisions have reached the same result. *See, e.g., Moses Lake Indus., Inc. v. Enthone, Inc.*, IPR2014-00243, Paper 6, at 18 (PTAB June 18, 2014); *Moses Lake Indus., Inc. v. Enthone, Inc.*, IPR2014-00246, Paper 6, at 17 (PTAB June 18, 2014); *eBay, Inc. v. Paid, Inc.*, No. CBM2014-00125, Paper 15, at 21 (PTAB Sept. 30, 2014).

Moreover, an obviousness inquiry “is based on factual inquiries including the differences between the claimed invention and the prior art.” *Travelocity.Com v. Cronos Tech.*, CBM2014-00082, Paper 10, at 20 (PTAB Sept. 15, 2014). Thus, identifying the differences between the claimed invention and the prior art is critically important, and the Board has cautioned that a petitioner who fails to state the differences between the claimed invention and the prior art risks having their obviousness grounds denied institution. *Liberty Mutual Ins. Co. v. Progressive Casualty Ins. Co.*, CBM 2012-00003, Paper 7, at 2-3 (PTAB Oct. 25, 2012).

In *Travelocity*, the Board declined institution on obviousness grounds because the petitioner failed to specifically identify the differences between the recited invention and the prior art. *Travelocity*, CBM2014-00082, Paper 10, at 20. The Board stated “[w]ithout having identified specifically the differences between the recited invention and the prior art, Petitioner has failed to make a meaningful obviousness analysis under 35 U.S.C. § 103(a), and, thus, has failed to establish

that it is more likely than not that” the independent claims are unpatentable on obviousness grounds. *Id.*

Here, Petitioners similarly fail to identify any differences between the relied upon prior art references and the claimed invention. The Petition also fails to acknowledge the importance of the *Graham* factors, or even *mention Graham at all*. Absent such discussions and critical analysis, Petitioners have failed to “make a meaningful obviousness analysis” under 35 U.S.C. § 103(a). Institution should be declined for this reason alone.

XII. THE *FINTIV* FACTORS SUPPORT DISCRETIONARY DENIAL UNDER § 314(A)

The Board should exercise its discretion to deny the Petition under 35 U.S.C. § 314(a) because each of the *Fintiv* factors weighs heavily in favor of denying institution. The Board’s precedential order in *Apple Inc. v. Fintiv, Inc.*, identifies six relevant factors in determining whether “efficiency, fairness, and the merits support the exercise of authority to deny institution in view of an earlier trial date in the parallel proceeding.” *Apple Inc. v. Fintiv, Inc.*, IPR2020–00019, Paper 11 at 5–6 (PTAB Mar. 20, 2020) (“*Fintiv I*”). These factors relate to “efficiency, fairness, and the merits” and require the Board to take “a holistic view of whether efficiency and integrity of the system are best served by denying or instituting review.” *Id.* at 6. As shown below, these factors strongly favor denying institution.

A. Factor 1: No Current Stay or Pending Stay Request, and a Stay Is Unlikely

In *Fintiv I*, the Board indicated that if a district court had stayed the parallel litigation or if the district court denied a motion for a stay without prejudice “and indicated to the parties that it will consider a renewed motion or reconsider a motion to stay if a PTAB trial is instituted,” then such guidance “if made of record” weighs “against exercising authority to deny institution under *NHK*.” *Fintiv I*, IPR2020-00019, Paper 11 at 6–7. Where “neither party has requested a stay” and “the District Court has not ruled on this issue” the Board declined “to infer, based on actions taken in different cases with different facts, how the District Court would rule should a stay be requested” See *Apple Inc. v. Fintiv, Inc.*, IPR2020–00019, Paper 15 at 12 (PTAB May 13, 2020) (“*Fintiv II*”) (applying the *Fintiv* Factors after supplemental briefing and denying institution under § 314(a)). As a result, the Board considered this factor neutral. *Id.*

Here, Petitioners offer no evidence that Judge Albright would grant a stay if an IPR is instituted. Indeed, the Petition does not even address this factor. (Pet. 82-84.) This factor weighs in favor of the denial of institution.

B. Factor 2: Court’s Trial Date Is Substantially Earlier than the Board’s Projected Statutory Deadline for a Final Written Decision

As *Fintiv I* noted, “[i]f the court’s trial date is earlier than the projected statutory deadline, the Board generally has weighed this fact in favor of exercising authority to deny institution under *NHK*.” *Fintiv I*, IPR2020–00019, Paper 11 at 9.

Here, jury selection for the trial in the district-court action is set to begin on April 25, 2022. (Ex. 2002 at 6.) In contrast, the projected statutory deadline for a final written decision in this proceeding is approximately May 22, 2022—almost a month *after* the trial date. While Petitioners speculate that the trial may be delayed due to the COVID-19 pandemic, there is no evidence to indicate there will be a meaningful delay to the schedule. (Pet. 82-83.) Indeed, Judge Albright recently held a jury trial in *VLSI Tech. LLC v. Intel Corp.*, No. 1:19-cv-00977-ADA (W.D. Tex.) without any issues. In addition, the Board has made clear that it “generally take[s] courts’ trial schedules at face value absent some strong evidence to the contrary.” *Apple Inc. v. Fintiv, Inc.*, IPR2020-00019, Paper 15, at 13 (PTAB. May 13, 2020). Because Petitioners fail to provide any non-speculative evidence regarding the timing of trial, the Board should abide by its general practice and accept the scheduled trial date as it is. This factor, therefore, favors denial of institution.

C. **Factor 3: Significant Investment in the Parallel Proceeding by the Court and the Parties**

The Board considers “the amount and type of work already completed in the parallel litigation by the court and the parties at the time of the institution decision.” *See Fintiv I*, IPR2020-00019, Paper 11 at 9. The Board clarified that this “investment factor is related to the trial date factor, in that more work completed by the parties and court in the parallel proceeding tends to support the arguments that the parallel proceeding is more advanced, a stay may be less likely, and instituting would lead to duplicative costs.” *Id.* at 10. And the Board indicated that while it takes a holistic view in each case, instances where the “court’s trial date is at or around the same time as the projected statutory deadline . . . the decision whether to institute will likely implicate other [*Fintiv*] factors . . . such as the resources that have been invested in the parallel proceeding.” *Fintiv I*, IPR2020–00019, Paper 11 at 9.

In this proceeding, the deadline for institution is May 22, 2021. By that time, the parties will have expended significant resources in the district court litigation complying with the district court’s scheduling order. For example, preliminary infringement and invalidity contentions will have been exchanged by the parties, and two *Markman* hearings will have taken place before May 22, 2021. (Ex. 2002 at 1-4.)

The parties’ investment will also continue to increase after the May 22, 2021 deadline, especially because Judge Albright does not have a practice of granting a stay pending instituted IPRs. *Cont’l Intermodal Grp.-Trucking LLC v. Sand Revolution LLC*, No. 7:18-cv-00147-ADA (July 22, 2020) (order denying motion to stay instituted IPR, discussing general preference, and stating “the Court strongly believes in the Seventh Amendment”). For example, because the district court trial date precedes the projected final written decision deadline in this proceeding, the parties and the district court will have invested a significant amount of time and resources *after institution* but before the final written decision deadline in preparation for the trial—including completion of fact and expert discovery, pre-trial motion practices, trial preparation, and trial. Indeed, the Board has found that such “additional investment of time and resources by the District Court and the parties” occurring “after institution but before our final decision” also weighs “strongly in favor of denying institution.” *Bentley Motors Ltd. v. Jaguar Land Rover Ltd.*, IPR2019-01539, Paper 16, at 9-10 (PTAB Oct. 2, 2020).

Thus, the substantial work and investment (by the parties and the district court) occurring before—and after—the institution decision and before the final written decision, weigh strongly in favor of denying institution and avoiding duplication of efforts.

D. Factor 4: There Is Substantial Overlap between Issues Raised in the Petition and in the Parallel Proceeding

As explained in *Fintiv I*, “if the petition includes the same or substantially the same claims, grounds, arguments, and evidence as presented in the parallel proceeding, this fact has favored denial [of institution].” *Fintiv I*, IPR2020-00019, Paper 11 at 12.

All of the invalidity arguments raised in this proceeding are also raised in the district court action. (Ex. 2003 at 32-33.) Petitioners argue that they “stipulate not to pursue in the district court any ground raised or that could have reasonably raised in an IPR” (Pet. 83.) Yet Petitioners also claim that they “reserve the right to revoke or amend the stipulation if the precedent or governing law changes.” *Id.* Importantly, Petitioners have not submitted their alleged stipulation to the district court, nor has the court accepted such a stipulation.

Through their alleged stipulation, Petitioners are seemingly announcing that they alone will decide which references do or do not proceed at trial. Additionally, there is a declaratory judgment of invalidity pending in the district court. The Patent Owner intends to present all of the references relied on in this IPR to the jury to establish that the patent is not invalid and have a definitive resolution with the Petitioners. Thus, the substantial overlap of the references will remain regardless of Petitioners’ alleged stipulation.

Furthermore, the Board should not assume that the district court will grant Petitioners' motion to withdraw certain invalidity defenses. For example, in *Optis Wireless v. Apple*, Apple attempted to file a motion to withdraw certain invalidity defenses that it raised in the district court in order to strengthen its case under the *Fintiv* factors. (See *Optis Wireless Technology, LLC, et al. v Apple, Inc.*, 2:19-CV-00066, Dkt. 453 (E.D. Tex. Aug. 3, 2020).) That motion was summarily denied to discourage infringer's gamesmanship. (See *Optis Wireless Technology, LLC, et al. v Apple, Inc.*, 2:19-CV-00066, Dkt. 457 (E.D. Tex. Aug. 4, 2020).)

Based on evidence before the PTAB, Factor 4 also weighs in favor of denial.

E. Factor 5: Petitioners and the Defendants in the WDTX Litigation Are the Same

This factor favors discretionary denial if the petitioner and the defendant in the parallel proceeding are the same party. See *Fintiv II*, IPR2020-00019, Paper 15 at 15; *Cisco*, IPR2020-00122, Paper 15 at 10. Here the parties are the same. Accordingly, this factor weighs in favor of discretionary denial.

F. Factor 6: Other Circumstances that Impact the Board's Exercise of Discretion, Including the Merits Favor Non-Institution

The factors considered in the exercise of discretion are part of a balanced assessment of all the relevant circumstances in the case, including the merits. See *Fintiv I*, IPR2020-00019, Paper 11, 14. In considering this factor, a full merits analysis is not necessary, but parties may point out "particular 'strengths or

weaknesses” to aid in determining whether the merits tip the scales one way or the other. *See Fintiv II*, IPR2020-00019, Paper 15 at 15. In view of the deficiencies in Petitioners’ arguments identified in this Response, the Board should deny institution on the merits.

Moreover, other facts bearing upon the discretionary denial decision also confirm that institution should be denied. Specifically, Petitioners are pursuing a strategy of the serial use of government resources solely for a tactical advantage—including the IPRs filed by Petitioners and the declaratory judgment of invalidity in the district court that Petitioners intend to continue to pursue regardless of the Board’s decision. Petitioners do not explain how institution of this IPR would prevent duplicative efforts by the courts and the parties in the pending actions.

Petitioners suggest that the technology at issue in the ’173 Patent is “better suited for an IPR than a jury of laypersons.” (Pet. 84.) This argument ignores the fact that an Article III judge will review any decision made by the jury regarding obviousness.

In sum, the Board should exercise discretion to deny institution under the *Fintiv* decision.

XIII. CONCLUSION

For the foregoing reasons, Patent Owner respectfully requests the Board deny Petitioners’ request for *Inter Partes* Review of U.S. Patent No. 7,221,173.

Dated: March 22, 2021

Respectfully Submitted,

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CERTIFICATE OF WORD COUNT

Under the provisions of 37 C.F.R. § 42.24(d), the undersigned hereby certifies that the Microsoft Office word count for the foregoing Patent Owner's Preliminary Response Under 35 U.S.C. § 313 and 37 C.F.R. § 42.107, excluding the table of contents, table of authorities, certificate of word count, and certificate of service, totals 13,023 words, which is less than the 14,000 words allowed under 37 C.F.R. § 42.24(b)(1).

Dated: March 22, 2021

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CERTIFICATE OF SERVICE

Pursuant to 37 C.F.R. § 42.6(e), I certify that I caused to be served on the counsel for Petitioners a true and correct copy of the foregoing Patent Owner's Preliminary Response Under 35 U.S.C. § 313 and 37 C.F.R. § 42.107, by electronic means on March 22, 2021 at the following addresses of record:

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