

6-20-cv-00889-ADA (U.S. Patent No. 6,704,304)

Terms for U.S. Patent No. 6,704,304		Preliminary Construction
1.	“means for determining whether a call should be routed over said PSTN or said core packet network”	<p>Plain and ordinary meaning.</p> <p>Alternatively, if subject to 35 U.S.C. § 112, ¶ 6, then,</p> <p>Function: “determining whether a call should be routed over said PSTN or said core packet network”;</p> <p>Structure: call feature server of “said server system.”</p>

6-20-cv-00891-ADA (U.S. Patent No. 7,406,260)

Terms for U.S. Patent No. 7,406,260		Preliminary Construction
1.	“masking alarms in the OCh paths in transmit direction”	Plain and ordinary meaning
2.	“masking alarms in the OCh paths in receive direction”	Plain and ordinary meaning
3.	“wherein the step of analyzing alarms comprises the steps of”	Plain and ordinary meaning
4.	“determining if each alarm in the list is an OCh alarm or a port level alarm or a card level alarm”	Plain and ordinary meaning
5.	“masking alarms in the downstream OCh path in the transmit direction that are correlated with each alarm in the list”	Plain and ordinary meaning
6.	“wherein for a specific OCh path, OCh alarms can mask OCh alarms, port level alarms can mask port level alarms and OCh alarms and card level alarms can mask port level alarms and OCh alarms”	Plain and ordinary meaning

6-20-cv-00892-ADA (U.S. Patent No. 7,460,658)

Terms for U.S. Patent No. 7,460,658		Preliminary Construction
1.	“detector embodied at the packet data network and adapted to receive indications provided to the packet data network of at which of the first and at least second locations at which the user selects to communicate”	Plain and ordinary meaning
2.	“calling indicia”	Plain and ordinary meaning
3.	“said indexer is accessed pursuant to the routing of the call to ascertain the calling indicia used to route the call to the selected one of the first location and the at least the second location”	Plain and ordinary meaning
4.	“private network portion”	Plain and ordinary meaning
5.	“detecting, at the packet data network, indications provided to the packet data network of at which of the first and at least second locations at which the user selects to communicate”	Plain and ordinary meaning

6-20-cv-00893-ADA (U.S. Patent No. 7,933,211)

None

6-20-cv-00916-ADA (U.S. Patent No. 7,406,074)

None

6-20-cv-00917-ADA (U.S. Patent No. 7,423,962)

Terms for U.S. Patent No. 7,423,962		Preliminary Construction
1.	“load allocation alternative[s]”	directed logical node pair, which indicates the active and standby logical node
2.	“maintenance means for maintaining logical nodes at least in first and second parallel	Subject to 35 U.S.C. § 112, ¶ 6 Function: “maintaining logical nodes at

	physical cluster nodes capable of transmitting data”	least in first and second parallel physical cluster nodes capable of transmitting data”; Structure: processor and memory, Col. 4:56-61, Col. 5:9-29
3.	“said maintenance means are also configured to maintain information on a primary and a secondary cluster node associated with the load allocation alternative”	Plain and ordinary meaning.
4.	“first forming means for forming load allocation alternatives of the logical nodes such that the first logical node of the load allocation alternative resides in the first cluster node and the second logical node resides in the second cluster node”	Subject to 35 U.S.C. § 112, ¶ 6 Function: “forming load allocation alternatives of the logical nodes such that the first logical node of the load allocation alternative resides in the first cluster node and the second logical node resides in the second cluster node” Structure: processor and memory, Col. 4:56-61, Col. 5:30-61.
5.	“execution means for changing, when a cluster node malfunctions, the load allocation of the logical nodes of the load allocation alternatives, the active logical nodes of which reside in the faulty cluster node, by changing the logical nodes from standby to active and the active nodes to standby”	Subject to 35 U.S.C. § 112, ¶ 6 Function: “changing, when a cluster node malfunctions, the load allocation of the logical nodes of the load allocation alternatives, the active logical nodes of which reside in the faulty cluster node, by changing the logical nodes from standby” Structure: processor and memory, Col. 4:56-61, 5:62-6:3
6.	“defining means for defining an individual external routine address for each load allocation alternative, on the basis of which data is transmitted to the network element”	Subject to 35 U.S.C. § 112, ¶ 6 Function: “defining an individual external routine address for each load allocation alternative, on the basis of which data is transmitted to the network element” Structure: processor and memory, Col. 4:56-61, 6:4-6:12

7.	“load allocation means for distributing the traffic in the apparatus on the basis of a specific load allocation plan between the cluster nodes that comprise logical nodes”	<p>Subject to 35 U.S.C. § 112, ¶ 6</p> <p>Function: “distributing the traffic in the apparatus on the basis of a specific load allocation plan between the cluster nodes that comprise logical nodes”</p> <p>Structure: processor and memory, Col. 4:56-61, 6:13-6:18</p>
8.	“changing means for changing load allocation in such a manner that after the switchover of a load allocation alternative, data is transmitted through a physical interface of the backup cluster node to the redundancy unit of the cluster node”	<p>Subject to 35 U.S.C. § 112, ¶ 6</p> <p>Function: “changing load allocation in such a manner that after the switchover of a load allocation alternative, data is transmitted through a physical interface of the backup cluster node to the redundancy unit of the cluster node”</p> <p>Structure: processor and memory, Col. 4:56-61, 11:64-12:15</p>
8.	“switching means for transmitting data by using a routing address defined for the load allocation alternative even after a switchover of the load allocation alternative”	<p>Subject to 35 U.S.C. § 112, ¶ 6</p> <p>Function: “transmitting data by using a routing address defined for the load allocation alternative even after a switchover of the load allocation alternative”</p> <p>Structure: processor and memory, Col. 4:56-61, 10:7-12</p>
9.	“performing means for performing a switchover of a load allocation alternative inside the network element”	<p>Subject to 35 U.S.C. § 112, ¶ 6</p> <p>Function: “performing a switchover of a load allocation alternative inside the network element”</p> <p>Structure: processor and memory, Col. 4:56-61, 10:34-38</p>

Dated: May 4, 2021

Respectfully submitted,

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CERTIFICATE OF SERVICE

A true and correct copy of the foregoing instrument was served or delivered electronically to all counsel of record via email on May 4, 2021.

/s/ Ryan S. Loveless
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