

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

Intel Corporation
Petitioner

v.

ACQIS LLC
Patent Owner

Case IPR2021-01103

PETITION FOR *INTER PARTES* REVIEW OF
U.S. REISSUED PATENT NO. 45,140
CHALLENGING CLAIMS 14-38
UNDER 35 U.S.C. § 312 AND 37 C.F.R. § 42.104

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Declaration of Dr. Bill Lin
U.S. Reissued Patent No. 45,140
Claims 14-38

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I, Bill Lin, declare as follows:

I. Background and Qualifications

1. My name is Bill Lin.
2. I have been retained on behalf of Petitioner Intel Corporation (“Intel” or “Petitioner”) to provide this Declaration concerning the technical subject matter relevant to a petition for *inter partes* review of U.S. Reissued Patent No. 45,140 (“RE140”). I reserve the right to supplement this Declaration in response to additional evidence that may come to light.
3. I am over 18 years of age. I have personal knowledge of the facts stated in this Declaration and am able to testify competently to them if asked to do so.
4. My compensation is not based on the resolution of this matter. My findings are based on my education, experience, and background in the fields discussed below.
5. I have no financial interest in Intel, nor do I have any financial interest in the RE140.
6. I am a Professor of Electrical and Computer Engineering at the University of California, San Diego (UCSD). I have over 30 years of experience in research and development in the areas of computer networking and computer design. I regularly teach a senior-level design course on the design of advanced processors,

and I have taught graduate courses and advanced special topics in computer architecture and computer networks.

7. At UCSD, I am a Principal Investigator in the UCSD Center for Networked Systems (CNS). CNS brings together researchers to work on a range of challenges in the design of future networked systems. My contribution to CNS has been expertise in the design of computer architecture solutions for packet processing, computer networking, and network measurements. I am also a Principal Investigator in the UCSD Center for Wireless Communications (CWC). CWC brings together researchers to work on a range of challenges in the design of future wireless communications systems. My contribution to CWC has been expertise in the design of computer architecture solutions for wireless networking and mobile computing.

8. I have also testified as an expert witness and consultant in patent and intellectual property litigations as well as *inter partes* reviews.

9. I received a Bachelor of Science in Electrical Engineering and Computer Sciences from University of California, Berkeley in May 1985; a Master's of Science in Electrical Engineering and Computer Sciences from the University of California, Berkeley in May 1988; and a Ph.D. in Electrical Engineering and Computer Sciences from the University of California, Berkeley in May 1991.

10. I am a named inventor on five patents in the fields of computer networking and computer design, and I have published over 190 journal articles and conference papers in top-tier venues and publications.

11. I have also served or am currently serving as Associate Editor or Guest Editor for 3 ACM or IEEE journals, as General Chair on 4 ACM or IEEE conferences, on the Organizing or Steering Committees for 6 ACM or IEEE conferences, and on the Technical Program Committees of over 45 ACM or IEEE conferences.

12. My Curriculum Vitae, which appears as Appendix A in my declaration, contains further details on my education, experience, publications, and other qualifications to render this opinion as expert.

II. Materials Relied On In Forming My Opinion

13. I have reviewed all of the following exhibits listed in the following Table of Exhibits.

Exhibit No.	Description
1001	U.S. Reissued Patent No. 45,140 (“RE140”)
1003	U.S. Patent No. 6,345,330 (“Chu330”)
1004	U.S. Patent Publication No. 2003/0135771 (“Cupps”)
1005	U.S. Patent No. 6,216,185 (“Chu185”)
1006	File history of RE140 (“RE140 FH”)
1007	U.S. Patent No. 6,643,777 (“Chu777”)
1008	U.S. Reissued Patent No. 42,984 (“RE984”)
1009	File history of RE984 (“RE984 FH”)

Exhibit No.	Description
1010	U.S. Patent Application No. 60/083,886 (“’886 Provisional”)
1011	File history of Chu330 (“Chu330 FH”)
1012	August 12, 2011 Amendment from File History of Control No. 90/010,816 (Reexamination of Chu185)
1013	U.S. Reissued Patent No. 41,092 (“RE092”)
1014	U.S. Reissued Patent No. 43,602 (“RE602”)
1015	U.S. Reissued Patent No. 44,468 (“RE468”)
1016	U.S. Reissued Patent No. 44,654 (“RE654”)
1017	U.S. Patent No. 6,621,760 (“Ahmad”)
1019	RE140 with highlights of substantively identical portions from Chu330, Chu185, ’886 Provisional, and Chu777
1020	File history of U.S. Reissued Patent No. 43,602 (“RE602 FH”)
1021	File history of U.S. Reissued Patent No. 44,468 (“RE468 FH”)
1022	<i>ACQIS LLC v. EMC Corp.</i> , Civil Action No. 1:14-cv-13560, No. 185 (D. Mass. Jan. 20, 2017) (EMC Corporation’s Opening Claim Construction Brief)

III. Understanding of the Governing Law

14. I understand that a patent claim is invalid if it is obvious in view of the prior art. I further understand that invalidity of a claim requires that the claim be obvious from the perspective of a person of ordinary skill in the relevant art at the time the invention was made.

A. Person of Ordinary Skill in the Art (“POSITA”)

15. I have been informed and understand that, in the context of an invalidity analysis, a person having ordinary skill in the art (“POSITA”) is a hypothetical person who looks to prior art at the time of the invention. I further understand that the factors that may be considered in determining the level of ordinary skill include:

(1) the problems encountered in the art; (2) the prior art solutions to the problems encountered in the art; (3) the rapidity of innovations; (4) the sophistication of the technology; and (5) the education level of active workers in the field. I understand that these factors need not all be taken into account for the analysis and that one or more of these factors may control.

B. Claim Construction

16. I have been informed that claim construction is a matter of law and that the final claim construction will ultimately be determined by the Board. For purposes of my analysis in this proceeding and with respect to the prior art, I have been informed that claims subject to *inter partes* reviews are currently reviewed under “the *Phillips* standard.”

17. I have been informed that under the *Phillips* standard, claim terms are given their plain and ordinary meaning as understood by a POSITA at the time of the invention in light of the claim language and the patent specification.

18. I have been informed that the claims encompass the embodiments described in the specification.

19. I have been informed that a patentee can serve as his or her own lexicographer. As such, if the specification provides a claim term with a specific

definition, I should interpret that claim term in light of the particular definition provided by the patentee.

C. Written Description, Incorporation By Reference, and Priority

20. I have been informed and understand that a patent's specification must contain a written description of the invention that reasonably conveys to a person of ordinary skill in the art that the inventors were in possession of the claims at the time the application was filed. To satisfy the written description requirement, a patent specification must describe the claims in sufficient detail that one of ordinary skill in the art can reasonably conclude that the inventor had possession of the claimed invention.

21. I have been informed and understand that a description that merely renders the claims obvious does not satisfy the written description requirement. Rather, the disclosure must describe the claims with all of its limitations.

22. I have been informed and understand that an applicant can show possession of the claims by describing the claims with all of its limitations using such descriptive means as words, structures, figures, diagrams, and formulas that fully set forth the claimed invention. Moreover, I have been informed and understand that other patents or patent publications incorporated by reference in the

patent must be considered in assessing whether that patent provides adequate written description.

23. I have been informed and understand that when determining whether an issued patent properly incorporated by reference other patents or patent publications, the inquiry is whether one of ordinary skill in the art could identify the information incorporated.

24. I have been informed and understand that for a claim to receive a priority date of an earlier parent patent or patent application, the earlier patent or patent application must provide adequate written description of the claimed subject matter. I understand that for a claim to obtain the benefit of the filing date of an earlier parent patent or patent application, each parent patent in the chain leading back to the earlier parent patent or patent application must provide adequate written description of the claimed subject matter.

25. I have been informed and understand that a patent can incorporate by reference specific disclosures found in a different patent or patent publication if a POSITA would understand with detailed particularity what specific material it incorporates and clearly indicate where that material is found. I have been informed and understand that if a patent properly incorporated by reference specific

disclosures found in a different patent or patent publication, the incorporated by reference material can provide written description support for the claims.

26. I have also been informed and understand that a priority claim is different from incorporation by reference claim. A priority claim claims the benefit of the earlier filing date of an earlier filed patent application. In contrast, incorporation by reference simply incorporates the disclosure of a different patent or patent publication without claiming the benefit of the earlier filing date of an earlier filed patent application.

D. Obviousness

27. I have been informed and understand that a patent claim can be considered to have been obvious to a POSITA as of the patent's priority date.

28. I have been informed and understand that pursuant to 35 U.S.C. § 103(a), "if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains," a patent may not be obtained.

29. This means that, even if all of the requirements of a claim are not found in a single prior art reference, the claim is not patentable if the differences between

the subject matter in the prior art and the subject matter in the claim would have been obvious to a POSITA at the time of the earliest priority date of the patent application.

30. I have been informed and understand that a determination of whether a claim would have been obvious should be based upon several factors, including, among others:

- Determine the level of POSITA;
- Determine the scope and content of the prior art;
- Ascertain what differences, if any, existed between the claims and the prior art; and
- Consider evidence of secondary indicia of non-obviousness, if such evidence is available, including whether a nexus exists between the claims and the evidence offered.

31. I have been informed and understand that the relevant time for considering whether a claim would have been obvious to a POSITA is the time of the earliest priority date afforded to the patent application.

32. I have been informed and understand that the teachings of one or more references may be combined in the same way as disclosed in the claims, if such a combination would have been obvious to a POSITA. I have been informed and understand that there is no rigid rule for finding that the two or more references

would have been combined. But in determining whether a combination based on either a single reference or multiple references would have been obvious, it is appropriate to consider, among other factors:

- whether the teachings of the prior art references disclose known concepts combined in familiar ways, which, when combined, would yield predictable results;
- whether a person of ordinary skill in the art could implement a predictable variation, and would see the benefit of doing so;
- whether the claimed elements represent one of a limited number of known design choices, and would have a reasonable expectation of success by those skilled in the art;
- whether a person of ordinary skill would have recognized a reason to combine known elements in the manner described in the claim;
- whether there is some teaching or suggestion in the prior art to make the modification or combination of elements claimed in the patent; and
- whether the claim applies a known technique that had been used to improve a similar device or method in a similar way.

33. I understand that one of ordinary skill in the art has ordinary creativity and is not an automaton.

34. I understand that in considering obviousness, it is important not to determine obviousness using the benefit of hindsight derived from the patent being considered.

IV. Overview of The Technology

35. In computer architecture, a bus is a communication system for transferring data between components in a computer. Beginning in the 1970s, electrical engineers and computer scientists began to develop standardized bus interfaces to ameliorate the problem of disparate, proprietary connection types. For example, the Industry Standard Architecture (ISA) bus, which dates back to 1981, was created to provide a standardized physical architecture and software interface for input/output (I/O) devices such as storage devices and graphics cards used with IBM PCs.

36. Early computer buses, like the ISA bus, were based on parallel electrical wires with multiple hardware connections. The Peripheral Component Interconnect (PCI) bus, which dates back to the 1992, is another widely used standard parallel bus interface. Later versions of the PCI bus called PCI-X provided higher data rates and wider data paths (e.g., 64-bit parallel vs. 32-bit parallel). Parallel buses like PCI and PCI-X are typically shared bus architectures with bidirectional links where multiple components could be attached.

37. Buses based on point-to-point serial connections are also widely used. Serial buses are widely used for external computer buses to reduce the cabling requirement. Serial buses are also widely used for both internal and external buses to achieve very high data rates with low power using techniques like Low-Voltage Differential Signaling (LVDS).

38. LVDS was introduced in 1994. LVDS works by transmitting information as the difference between the voltages on a pair of wires, where the two wire voltages are compared at the receiver. In a typical implementation, LVDS uses a current-mode driver output from a low current source to drive a differential line that is terminated by a resistor, which generates a low voltage swing across the receiver inputs. The receiver senses the polarity of this voltage to determine the logic level. The low voltage swing and low current source enable data transmission at very high data rates with low power consumption. The differential signaling approach also makes the transmission mechanism robust against electromagnetic noise interference.

V. Overview of RE140

39. As indicated on the cover page of RE140, RE140 was filed on December 17, 2013 and issued on September 16, 2014. It is one of many reissued patents off of U.S. Patent No. 6,643,777 (the “777 Patent”), which was originally

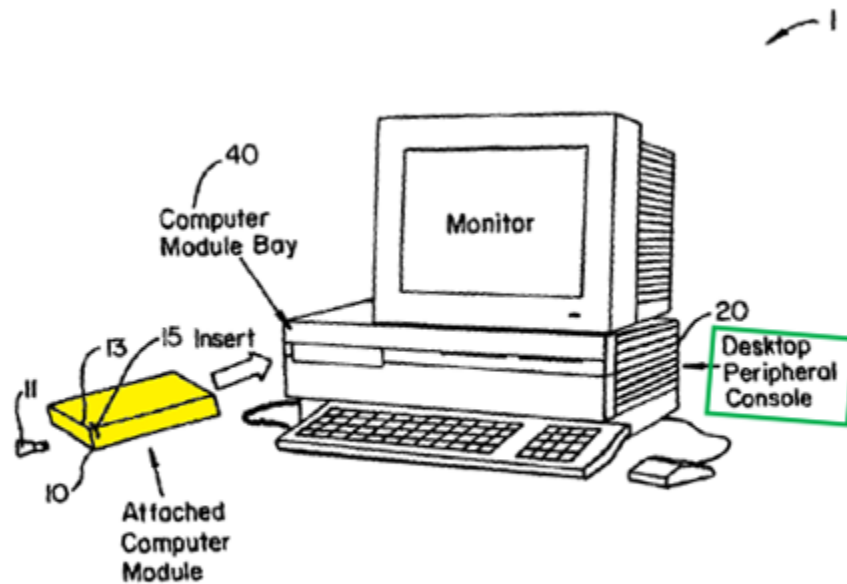
filed on May 14, 1999 and issued on November 4, 2003. Ex. 1001 [RE140] at Cover. As I will discuss in greater detail below, the '777 Patent, however, does not provide full support for the claims.

40. RE140 is directed “to a modular computing environment for desk top computers, ... to other portable or modular computing applications.” Ex. 1001 [RE140] at 1:35-42. Specifically, RE140 notes that “there has been little common ground between ... PCs and laptops in terms of upgrading, ease-of-use, cost, performance, and the like.” Ex. 1001 [RE140] at 2:19-21. RE140 notes that when users use separate portable and desktop computer, “the user has to spend money to buy components and peripherals th[at] are duplicated in at least one of these computers.” Ex. 1001 [RE140] at 2:39-42.

41. Figure 1 of RE140 shows a removable “Attached Computer Module” that is to be attached to a Desktop Peripheral Console.¹ See Ex. 1001 [RE140] at 3:62-64 (“The system also has an attached computer module (i.e., a removable

¹ I have colored Figure 1 by highlighting the Desktop Peripheral Console in green and the Attached Computer Module in yellow. I have added additional coloring and annotations to the figures found in the various exhibits to more clearly explain my opinions throughout my declaration.

module with memory and microprocessor) coupled to the **console**.”). As shown, “the **ACM** inserts into a Computer Module Bay (CMB) within a **peripheral console**.” Ex. 1001 at 3:51-53.



42. Figure 13 of RE140 shows some additional details of the components in the ACM and the peripheral console using schematic block diagrams. Moreover, as shown in Figure 13, “[t]he **ACM 1305** and the **peripheral console 1310** are interfaced through an exchange interface system (XIS) bus 1315” which “includes power bus 1316, **video bus 1317** and **peripheral bus (XPBus) 1318**.” Ex. 1001 [RE140] at 18:46-51.

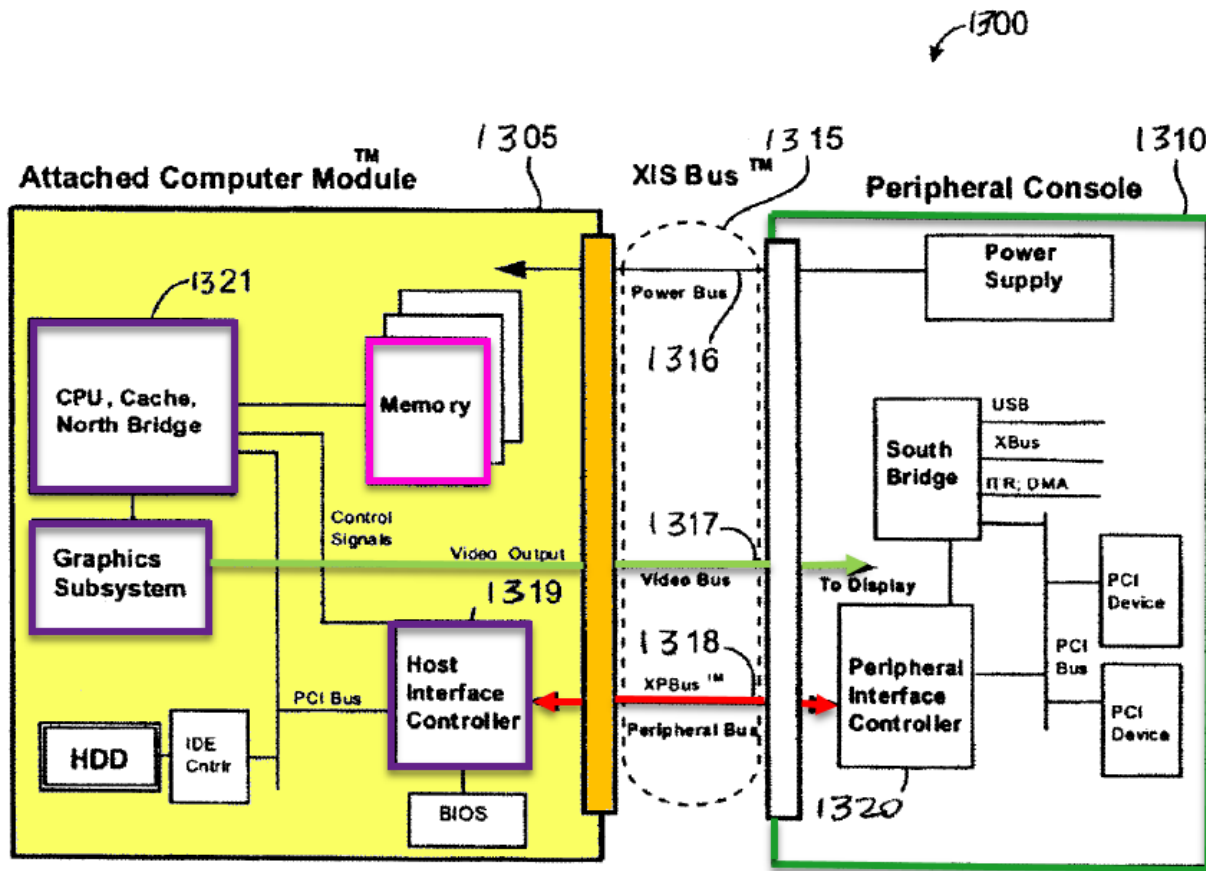
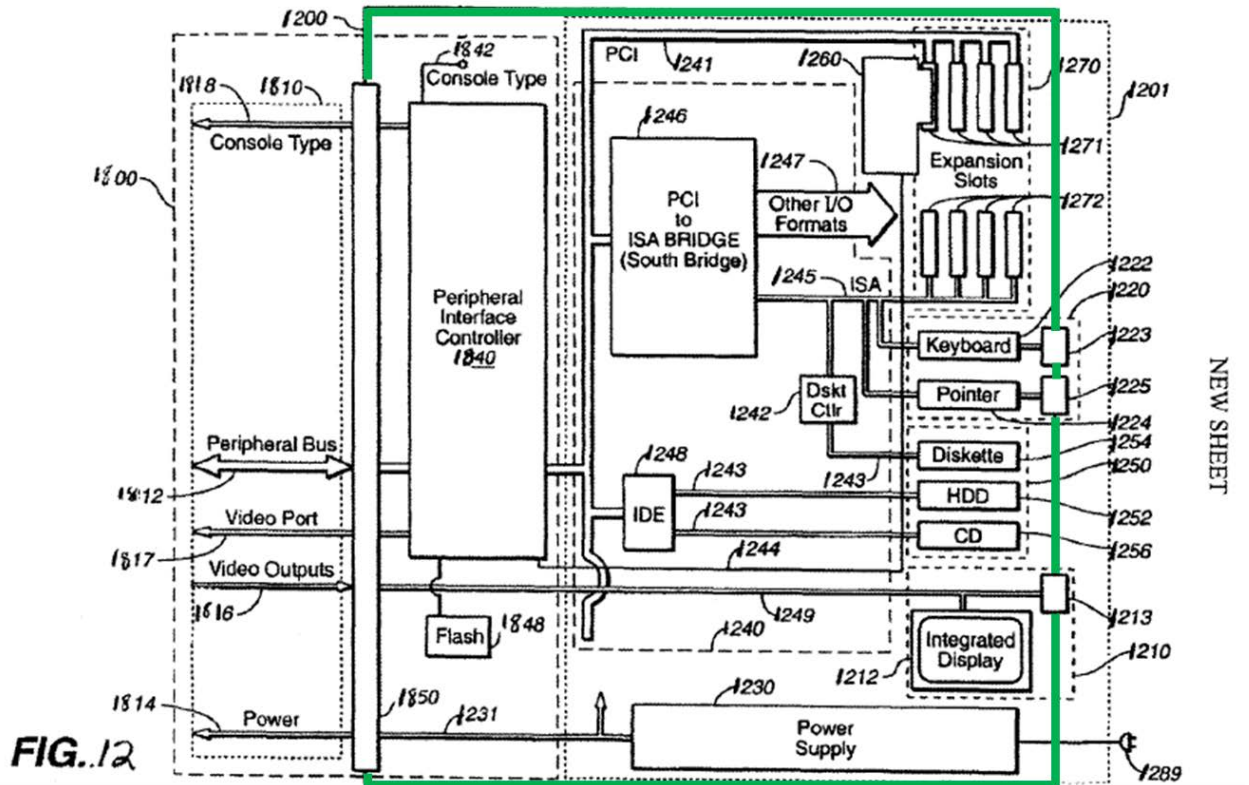


FIG. 13

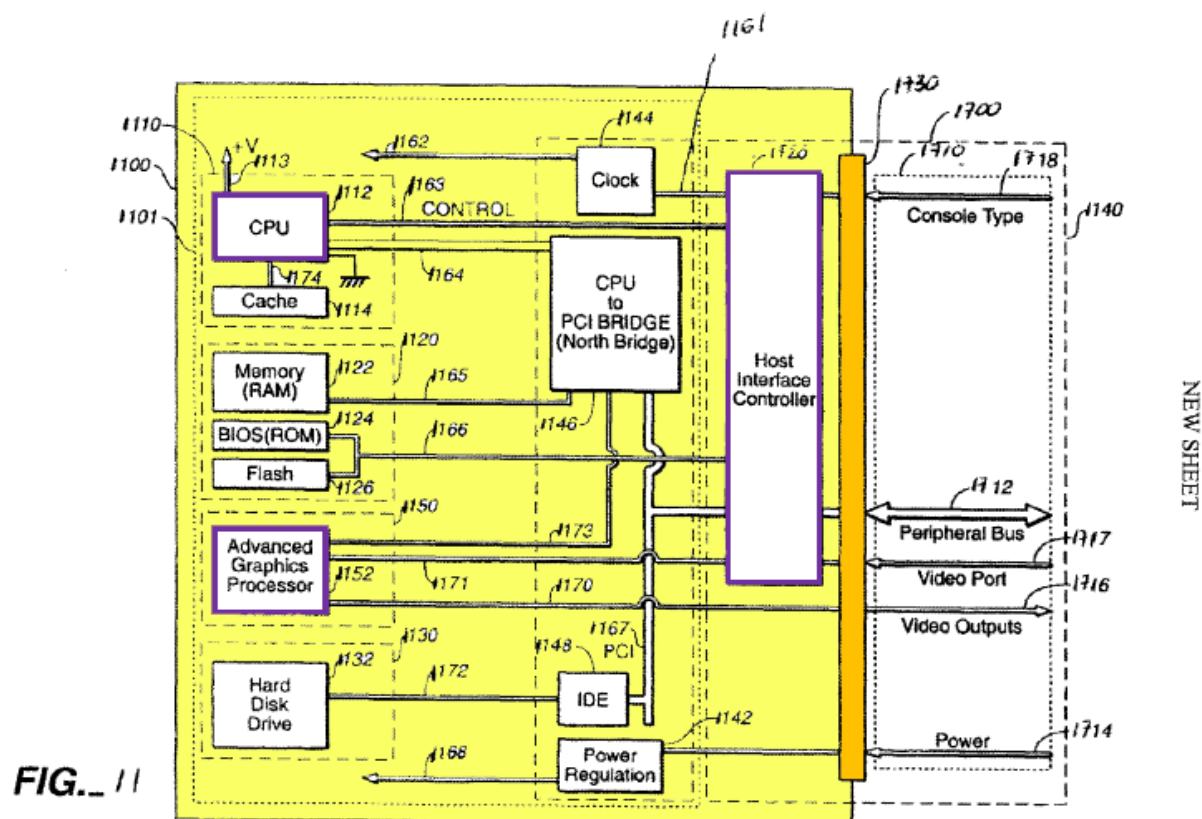
43. Figure 12 below shows some additional details regarding the **peripheral console (PCON)**. As shown, the **PCON** interfaces with the **ACM** using “a Peripheral Interface Controller (PIC) component 1840 [and] a PCON connector component 1950.” Ex. 1001 [RE140] at 16:36-38. Moreover, the Peripheral Interface Control 1840 interfaces with a South Bridge 1246 that connects to various peripherals (*e.g.*, keyboard, pointer). The Peripheral Interface Controller is also

connected to PCI expansion slots 1270 and storage devices, such as hard drive 1252, and CD-ROM drive 1256. See Ex. 1001 [RE140] at 14:62-15:9, 16:23-35, 17:1-30.



44. Figure 11 below shows some additional details of the **ACM**. As shown, the **ACM** includes, among other components, a **central processing unit** (“CPU”), an **advanced graphics processor**, and a **host interface controller**. The **ACM** interfaces with the **PCON** using the “Host Interface Controller (HIC) component 1720 and an **ACM connector component 1730**.” Ex. 1001 [RE140] at 15:44-46.

Moreover, the HIC 1720 is coupled to the North Bridge 1146, which in turn is coupled to the **CPU** and memory.



45. As shown below in Figure 20 of RE140, certain components, such as the **CPU**, the **graphics subsystem** and the **interface controller**, are integrated together in a single chip. See Ex. 1001 [RE140], 19:10-13 (“FIG. 20 shows an attached computer module with single chip 2025 fully integrated: CPU, Cache, Core Logic, Graphics controller and Interface controller.”); see also Ex. 1001 [RE140] at Figure 19 and 19:8-13.

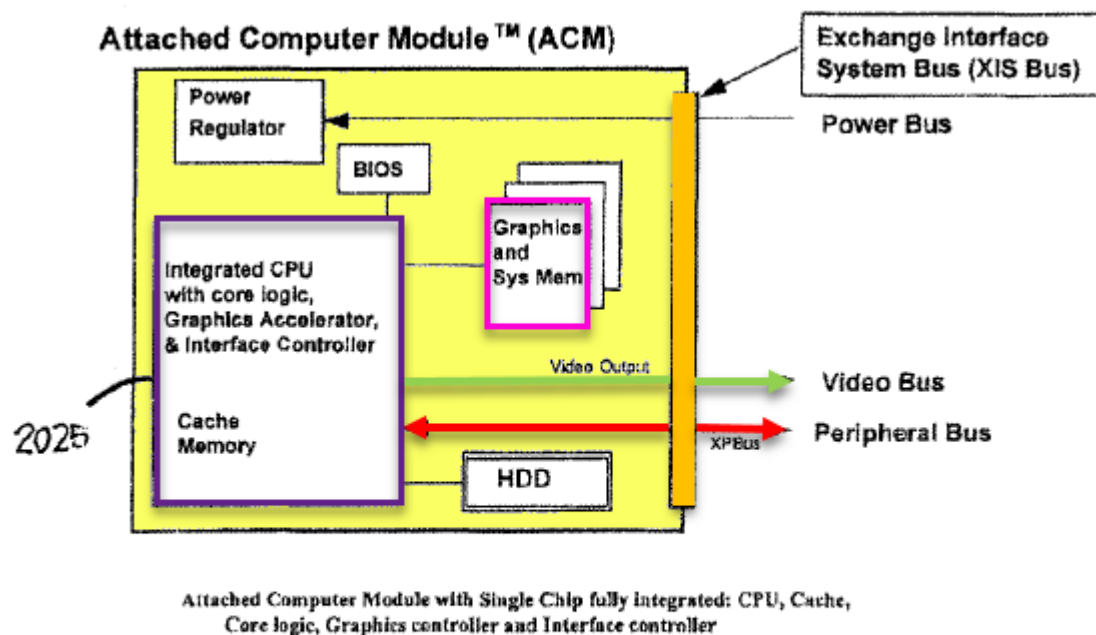


FIG. 20

46. Returning to Figure 13, “[t]he **ACM 1305** and the **peripheral console 1310** are interfaced through an exchange interface system (XIS) bus 1315” which “includes power bus 1316, **video bus 1317** and **peripheral bus (XPBus) 1318**.” Ex. 1001 [RE140] at 18:46-51.

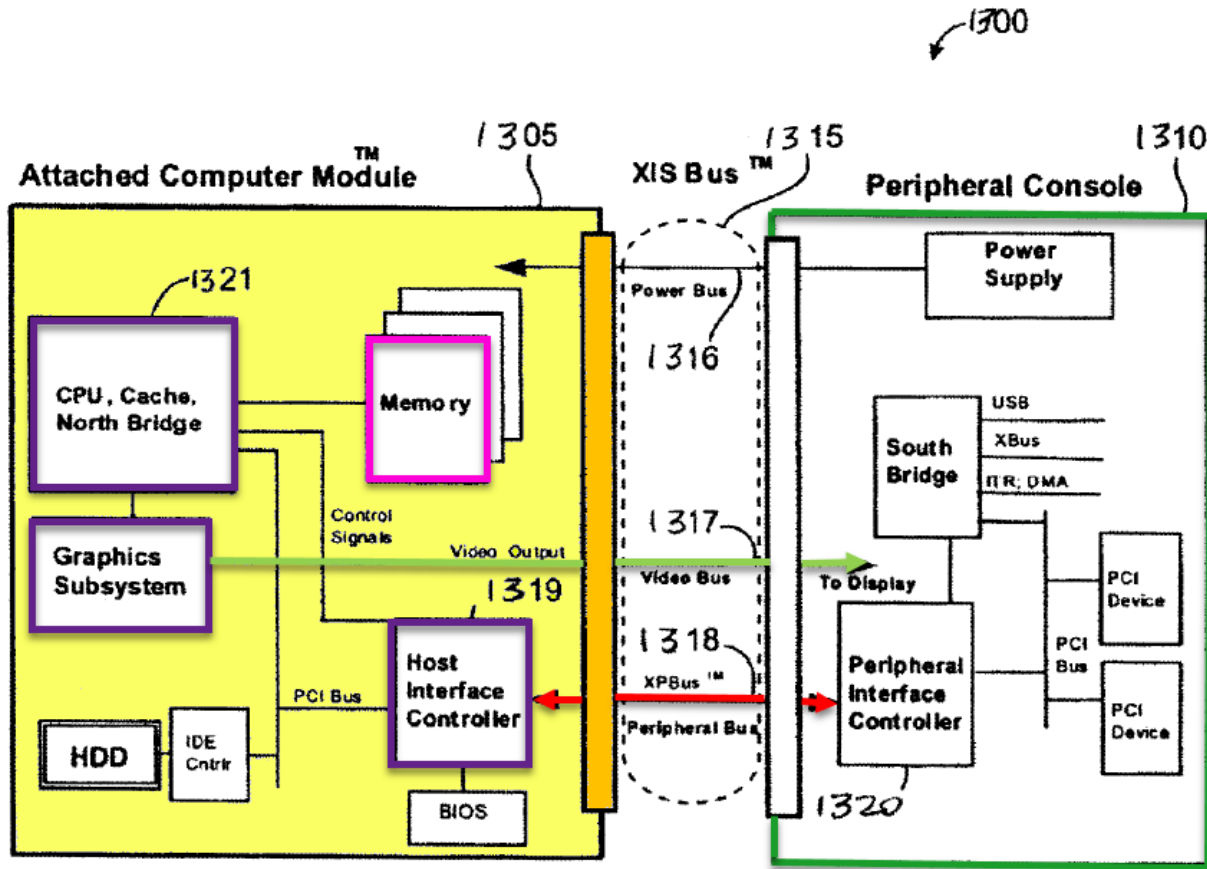


FIG. 13

47. “The power bus 1316 transmits power between **ACM 1305** and **peripheral console 1310**.” Ex. 1001 [RE140] at 18:51-52.

48. “[T]he **video bus 1317** transmits video signals between the **ACM 1305** and the **peripheral console 1310** ... such as Video Electronic Standards Association (VESA) Plug and Display’s Transition Minimized Differential Signaling (TMDS) signals for flat panel display.” Ex. 1001 [RE140] at 18:54-61.

49. Finally, the “**XPBus** 1318 is coupled to host interface controller (HIC) 1319 and to peripheral interface controller (PIC) 1320.” Ex. 1001 [RE140] at 18:62-65; *see also* Ex. 1001 [RE140] at 19:14-51.

50. RE140 provides describes additional details how data—specifically encoded PCI bus transactions—is transmitted across the XPBus by way of Figure 14. As shown, the **HIC** receives from the **host PCI bus** “PCI address/data” (“PCI AD”). The “**first in first out (FIFO) buffers**” queues the PCI AD and **encodes** the PCI AD into a format “more suitable for parallel to serial conversion prior to transmittal on the **XPBus**.” Ex. 1001 [RE140] at 19:29-49. The “**parallel to serial converters 1032**” then serializes the “multiplexed parallel A/D bits” and transmits them “on **data lines PD0 to PD3 of the XPBus**.” Ex. 1001 [RE140] at 19:52-56.

NEW SHEET

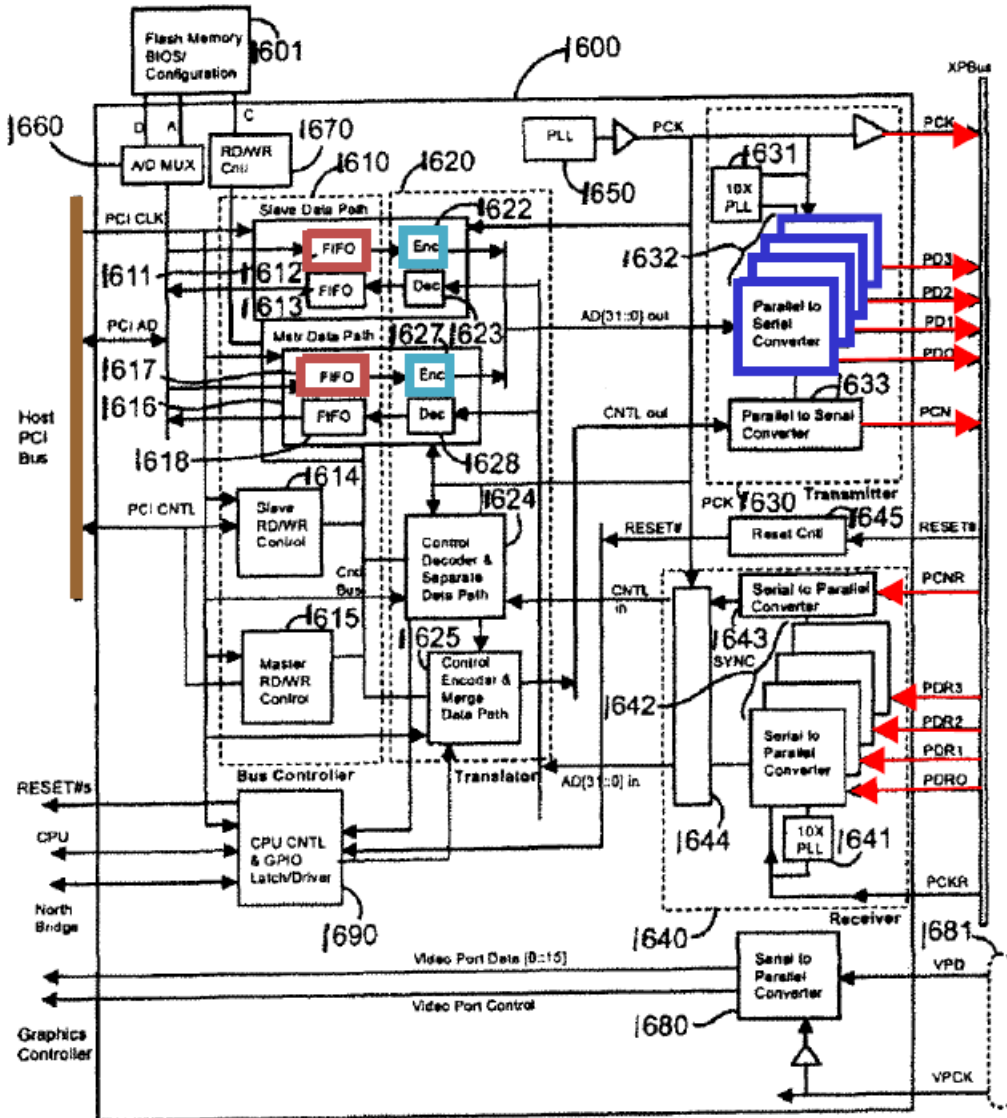


FIG. 14

51. The **HIC** can also receive data from the PIC in the **PCON**, and operates in reverse to what I explained above. See Ex. 1001 [RE140] at 20:18-20, 20:38-42.

52. According to RE140, “[t]he XPBus which includes lines **PCK, PD0 to PD3, PCN, PCKR, PDR0 to PDR3, and PCNR**, has two sets of unidirectional lines transmitting clock signals and bits in opposite directions. The first set of unidirectional lines includes **PCK, PD0 to PD3, and PCN**. The second set of unidirectional lines includes **PCKR, PDR0 to PDR3, and PCNR**. Each of these unidirectional set of lines is a point-to-point bus with a fixed transmitter and receiver....” Ex. 1001 [RE140] at 20:34-42.

53. Figure 16 of RE140 shows the “lines **PCK, PD0 to PD3, and PCN**.” Ex. 1001 [RE140] at 20:14-15. “These lines are *unidirectional LVDS lines* for transmitting clock signals and bits from the HIC to the PIC. The bits on the **PD0 to PD3 and the PCN** lines are sent synchronously within every clock cycle of the **PCK**.”” Ex. 1001 [RE140] at 20:15-18.

NEW SHEET

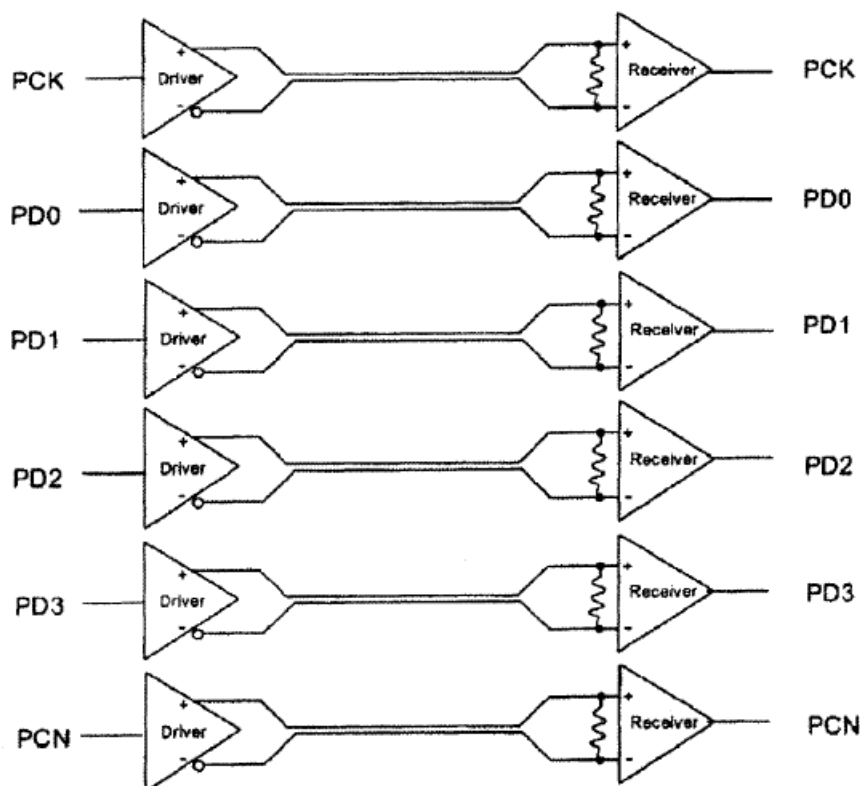


FIG. 16

54. Although not shown in Figure 16, the second “set of lines, namely **PCKR, PDR0 to PDR3, and PCNR**, are used to transmit clock signals and bits from the PIC to HIC. The lines used for transmitting information from the PIC to the HIC have the same structure as those shown in FIG. 16, except that they transmit data in a direction opposite to that in which the lines shown in FIG. 16 transmit data.”” Ex. 1001 [RE140] at 20:18-24.

55. RE140 explains that “[t]he bits sent in the first nibble of each data packet indicate the type of the data packet.” Ex. 1001 [RE140] at 21:25-27. Figure 24 below provides a few examples. For example, if the first nibble of a data packet is **XX00**, that indicates that the data packet is the first segment of PCI AD; if the first nibble of a data packet is **XX10**, that indicates that the data packet is the second segment of PCI AD.

ID bits (P0 P1 P2 P3)	Data Packet Type
XX00	PCI 1st address/data segment
XX10	PCI 2nd address/data segment
0001	Control 1st segment with PCI response
1001	Control 1st segment without PCI response
0101	Control 2nd segment with PCI response
1101	Control 2nd segment without PCI response
0011	Reserved
1011	Reserved
0111	Initialization
1111	NOOP

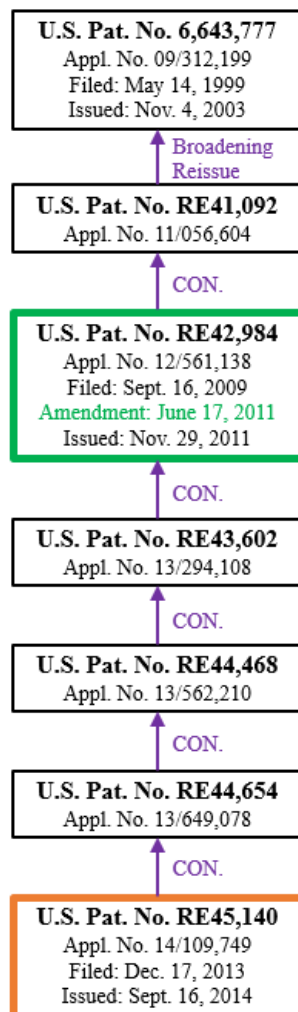
NEW SHEET

FIG. 24

56. If the first nibble is either **0011** or **1011**, it means that the data packet is of the “reserved” type. These “reserved data packet types can be used to support non-PCI bus transactions, e.g., USB transactions.” Ex. 1001 [RE140] at 21:24-25. In other words, RE140 mentions only in passing that USB transactions are supported (without meaningful detail as to **how** it can be supported).

A. Priority Date of RE140

57. The cover page of RE140 includes a “Related U.S. Application Data” section that lists out the relationship between RE140 and its parent patents. I have generated the following block diagram that summarizes these related patents, where I have highlighted the RE140 using an orange outline.



58. I have also highlighted U.S. Reissued Patent No. 42,984 (“RE984”) in green because, as I explain below, it is my opinion that claims 14-38 are only supported by the material that was added to the RE984—not by the materials found in the ’777 patent or U.S. Reissued Patent No. 41,092 (“RE092”).

59. I have reviewed the ’777 patent, (Ex. 1007), U.S. Reissued Patent No. 41,092 (“RE092”) (Ex. 1013), U.S. Reissued Patent No. 42,984 (“RE984 Patent”) (Ex. 1008), U.S. Reissued Patent No. 43,602 (“RE602”) (Ex. 1014), U.S. Reissued Patent No. 44,468 (“RE468”) (Ex. 1015), and U.S. Reissued Patent No. 44,654 (“RE654”) (Ex. 1016).

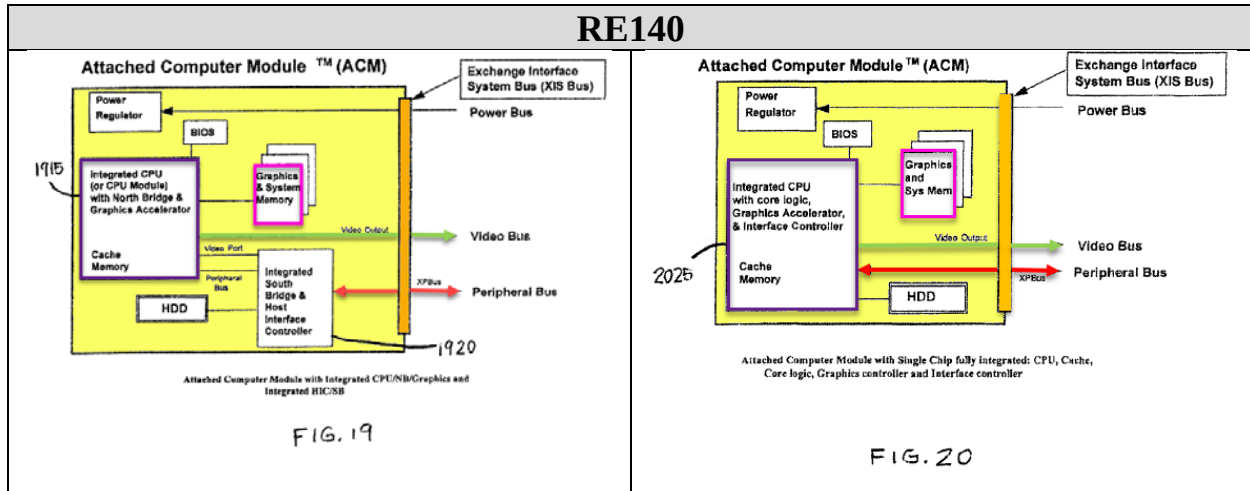
60. In my opinion, none of the ’777 Patent and RE092 provide written description support for claim 14-38 of RE140. They are missing the following limitations, which I have grouped together as “integrated CPU/graphics” limitations and “CPU-LVDS” limitations. The bold, italics emphasis indicate claims that are independent.

Claims	Integrated CPU-graphics Limitations	CPU-LVDS Limitations
14-16	“an integrated Central Processing Unit (CPU) with a graphics controller in a single chip”	Not recited
17		“connecting a second LVDS channel directly to the integrated CPU and graphics controller, the second LVDS channel comprising two unidirectional, serial bit channels that transmit data in opposite directions”
18		Not recited
19-20		“connecting a second LVDS channel directly to the integrated CPU and graphics controller, the second LVDS channel comprising two unidirectional, serial bit channels that transmit data in opposite directions”
21		Not recited
22-25		“connecting a first Low Voltage Differential Signal (LVDS) channel directly to the integrated CPU and graphics controller, wherein the first LVDS channel comprises two unidirectional, serial bit channels that transmit data in opposite directions”
26-29		“connecting a Low Voltage Differential Signal (LVDS) channel directly to the integrated CPU and graphics controller, wherein the LVDS channel comprises two unidirectional, serial bit channels that transmit data in opposite directions”
30-34		
35-38	“an integrated Central Processing Unit (CPU) and graphics controller in a single chip”	“connecting a first Low Voltage Differential Signal (LVDS) channel directly to the integrated CPU and graphics controller, wherein the first LVDS channel comprises two unidirectional, serial bit channels that transmit data in opposite directions”

61. I also summarize below the only figures (and associated descriptions) that support these claims based on the “integrated CPU-graphics” limitations and the “CPU-LVDS” limitations. As shown, except for claims 14-16, 18, and 21, the only possible support for the claims come from Figure 20 and its associated description. Figures 14-16, 18, and 21 arguably find support from Figures 19-20 and its associated description.

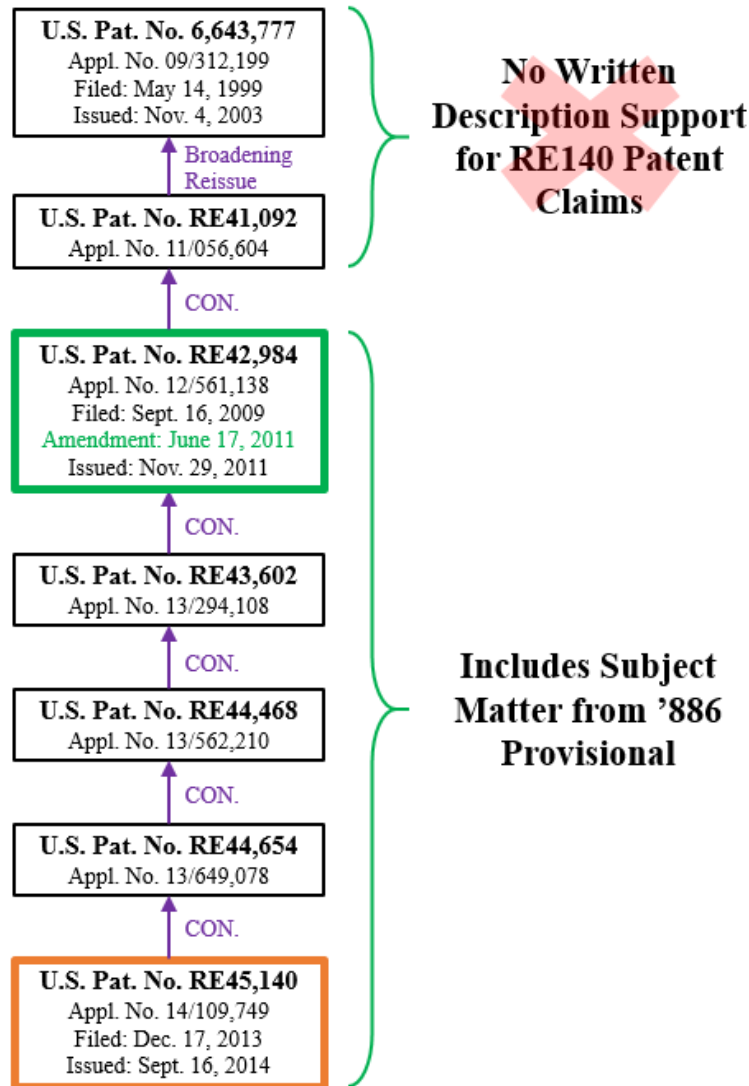
Integrated CPU/graphics	CPU-LVDS	Only Possible Support
14-16		FIGS. 19-20
17	17	FIG. 20
18		FIGS. 19-20
19-20	19-20	FIG. 20
21		FIGS. 19-20
22-25	22-25	FIG. 20
26-29	26-29	FIG. 20
30-34	30-34	FIG. 20
35-38	35-38	FIG. 20

62. I provide below Figures 19 and 20 from RE140. As shown, Figure 19 and 20 include an “Integrated CPU ... & Graphics Accelerator 1915” and an “Integrated CPU with ... Graphics Accelerator... 2025,” respectively. *See, e.g.*, Ex. 1001 [RE140] at 19:8-13 (“FIG. 19 shows an attached computer module with integrated CPU/NB/Graphics 1915 and Integrated HIC/SB 1920. FIG. 20 shows an attached computer module with single chip 2025 fully integrated: CPU, Cache, Core Logic, Graphics controller and Interface controller.”).



63. In Figure 19, the XPSu, which as I explained above are used to transmit data utilizing unidirectional, differential signal pairs in opposite directions, is coupled to the “Integrated CPU ... & Graphics Accelerator 1915” through an “Integrated South Bridge & Host Interface Controller 1920.” In contrast, in Figure 20, the XPSu is directly coupled to the “Integrated CPU with ... Graphics Accelerator... 2025.”

64. Figures 19 and 20 and its associated descriptions first appear in RE984. They do not appear in the '777 Patent or RE092. In other words, RE984 (outlined in green below) is the *first* patent which added in these descriptions and figures in any of parent applications to the RE140 (outlined in orange below).



65. Indeed, Figures 19 and 20 and its associated description were first added to RE984 through an amendment on June 17, 2011—more than two years after the RE984 was first filed. These additions (among other additions) are shown below.

IN THE SPECIFICATION:

Please add the following new paragraphs after the paragraphs previously added at col. 4, line 51:

FIG. 17 is a partial block diagram of a computer system using the interface of the present invention as a bridge between the north and south bridges of the computer system.

FIG. 18 is a partial block diagram of a computer system in which the north and south bridges are integrated with the host and peripheral interface controllers, respectively.

FIG. 19 shows an attached computer module with Integrated CPU/NB/Graphics and Integrated HIC/SB.

FIG. 20 shows an attached computer module with single chip fully integrated: CPU, Cache, Core Logic, Graphics controller and Interface controller.

Please add the following new paragraph after the paragraphs previously added at col. 13, line 33:

In the embodiment shown in FIG. 13, HIC 1319 is coupled to an integrated unit 1321 that includes a CPU, a cache and a north bridge. In another embodiment, such as that shown in FIG. 17, the CPU 1705 and north bridge 1710 are separate rather than integrated units. In yet another embodiment, such as that shown in FIG. 18, the HIC and PIC are integrated with the north and south bridges, respectively, such that integrated HIC and north bridge unit 1805 includes an HIC and a north bridge, while integrated PIC and south bridge unit 1810 includes a PIC and a south bridge. FIG. 19 shows an attached computer module with integrated CPU/NB/Graphics 1915 and Integrated HIC/SB 1920. FIG. 20 shows an attached computer module with single chip 2025 fully integrated: CPU, Cache, Core Logic, Graphics controller and Interface controller.

Ex. 1009 [RE984 FH, Amendment dated June 17, 2011] at 346.

NEW SHEET

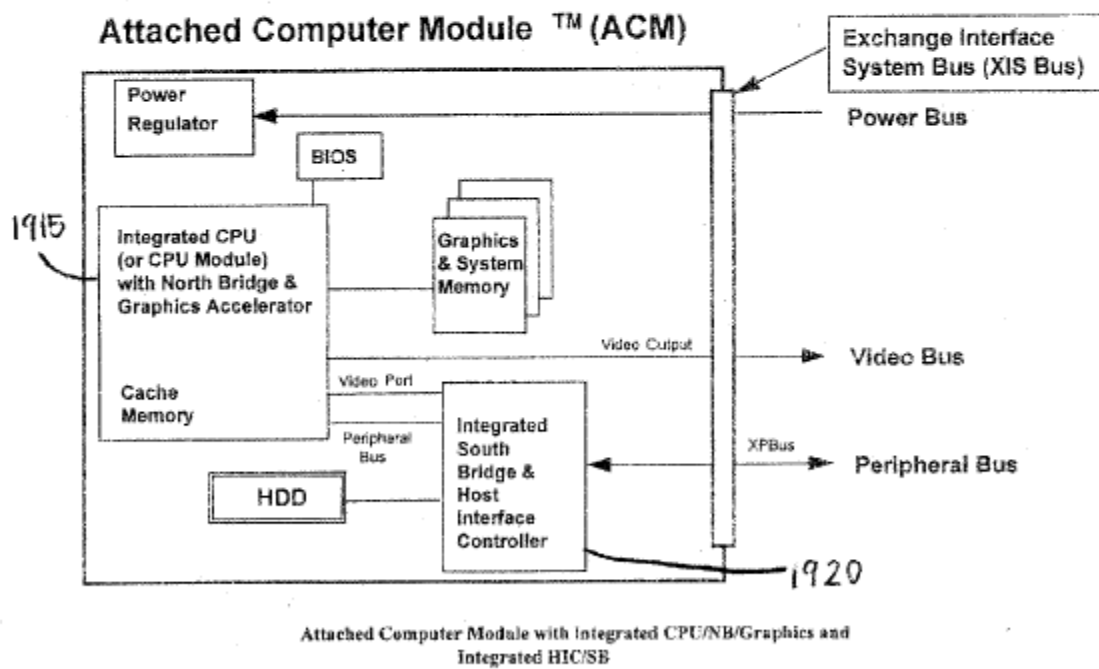


FIG. 19

NEW SHEET

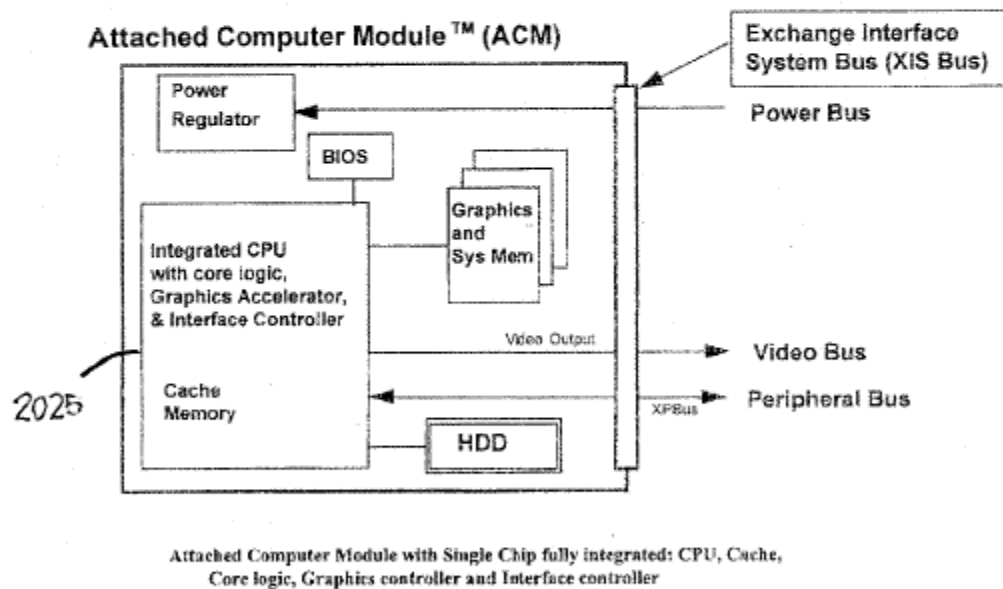


FIG. 20

Ex. 1009 [RE984 FH, Amendment dated June 17, 2011] at 376-377.

66. In making these addition, ACQIS provided the following remarks to the Examiner:

Drawings and Specification

The subject application is a continuation reissue application, for the reissue of original U.S. Patent No. 6,643,777 (the “’777 patent”). At col. 5, lines 9-13, the ‘777 patent incorporated by reference U.S. Application No. 09/149,882, now issued as U.S. Patent No. 6,345,330 (the “’330 patent”), which, in turn, claimed the benefit of and incorporated by reference U.S. Provisional Application No. 60/083,886 (the “’886 provisional application”) (See checked incorporation by reference box in utility patent application transmittal of U.S. Application No. 09/149,882 filed on September 8, 1998). By this paper, the subject application is amended to specifically include certain figures and text from the ‘330 patent, as well as certain figures and text from the ‘886 provisional application. Specifically, the subject application is amended to add new FIG. 17 through FIG. 20, as well as accompanying text. This corresponds to: (a) FIG. 3 and FIG. 4 of the ‘330 patent; (b) the text of the ‘330 patent at col. 3, lines 48-53 and col. 6, lines 26-35; (c) figure 8 and figure 9 of the ‘886 provisional application; and (d) the text of the ‘886 provisional application as originally included in legends of figure 8 and figure 9.] For purposes of consistency, FIG. 3 of the ‘330 patent and its accompanying reference numbers having the format 3xx are re-labeled as FIG. 17 and reference numbers having the format 17xx. Likewise, FIG. 4 of the ‘330 patent and figure 8 and figure 9 of the ‘886 provisional application and their accompanying reference numbers are re-labeled for purposes of consistency. Otherwise, Applicant respectfully submits that the added figures and text correspond to the above-noted figures and text of the ‘330 patent and the ‘886 provisional application, and that no new matter is added.

Ex. 1009 [RE984 FH, Amendment dated June 17, 2011] at 363.

67. Based on my review of the ‘777 Patent, the ‘777 Patent does indeed appear to incorporate by reference Chu330. It states that “[s]ome details of the ACM

can be found in co-pending patent application Ser. Nos. 09/149,882 [Chu330] ... ***and hereby incorporated by reference*** for all purposes,” Ex. 1007 [’777 Patent] at 5:9-13.

68. However, upon review of Chu330, I could not find any discussion indicating that the ’886 Provisional was incorporated by reference into Chu330. The ’886 Provisional is mentioned in Chu330 only as follows: “This application claims any and all benefits as provided by law of U.S. Provisional Application No. 60/083,886, filed May 1, 1998...” Ex. 1003 [Chu330] at 1:7-10. I do not see any statement in Chu330 that “incorporated by reference” the ’886 Provisional.

69. This is contrasted with Chu330’s incorporation by reference of a ***different*** patent—namely Chu185. Regarding Chu185, Chu330 explicitly states: “This application is being filed concurrently with the application of William W.Y. Chu for “Personal Computer Peripheral Console with Attached Computer Module”, filed on Sep. 8, 1998 now U.S. Pat. No. 6,216,185, and ***incorporates the material therein by reference.***” Ex. 1003 [Chu330] at 1:11-15. This is in stark contrast to the language pertaining to the ’886 Provisional which is silent to any specific incorporation by reference language.

70. Page 79 of Chu330's file history (Ex. 1011) shows the "Utility Patent Application Transmittal," which ACQIS referred to in its Amendment dated June 17, 2011 while adding Figures 19 and 20. I have reproduced that page below.

Declaration of Dr. Bill Lin
U.S. Reissued Patent No. 45,140
Claims 14-38

Please type a plus sign (+) inside this box. ☐

PTO/SB/05 (12/97) (modified)
Approved for use through 09/30/00. OMB 0651-0032
Mark Office: U.S. DEPARTMENT OF COMMERCE

**UTILITY
PATENT APPLICATION
TRANSMITTAL**

Only for new nonprovisional applications under 37 CFR 1.53(b))

Attorney Docket No. 38711206-000 Total Pages 106

First Named Inventor or Application Identifier
William W.Y. Chu

Express Mail Label No. EL112731756US

CERTIFICATE OF MAILING BY "EXPRESS MAIL"

Express Mail Label No.: EL112731756US Date of Deposit: September 8, 1998

Whereby certify that this paper or fee is being deposited with the United States Postal Service "Express Mail Post Office to Addressee" service under 37 C.F.R. § 1.10 on the date indicated above and is addressed to: Assistant Commissioner for Patents, Washington, D.C. 20231.

Ararat Kapouytian
Ararat Kapouytian

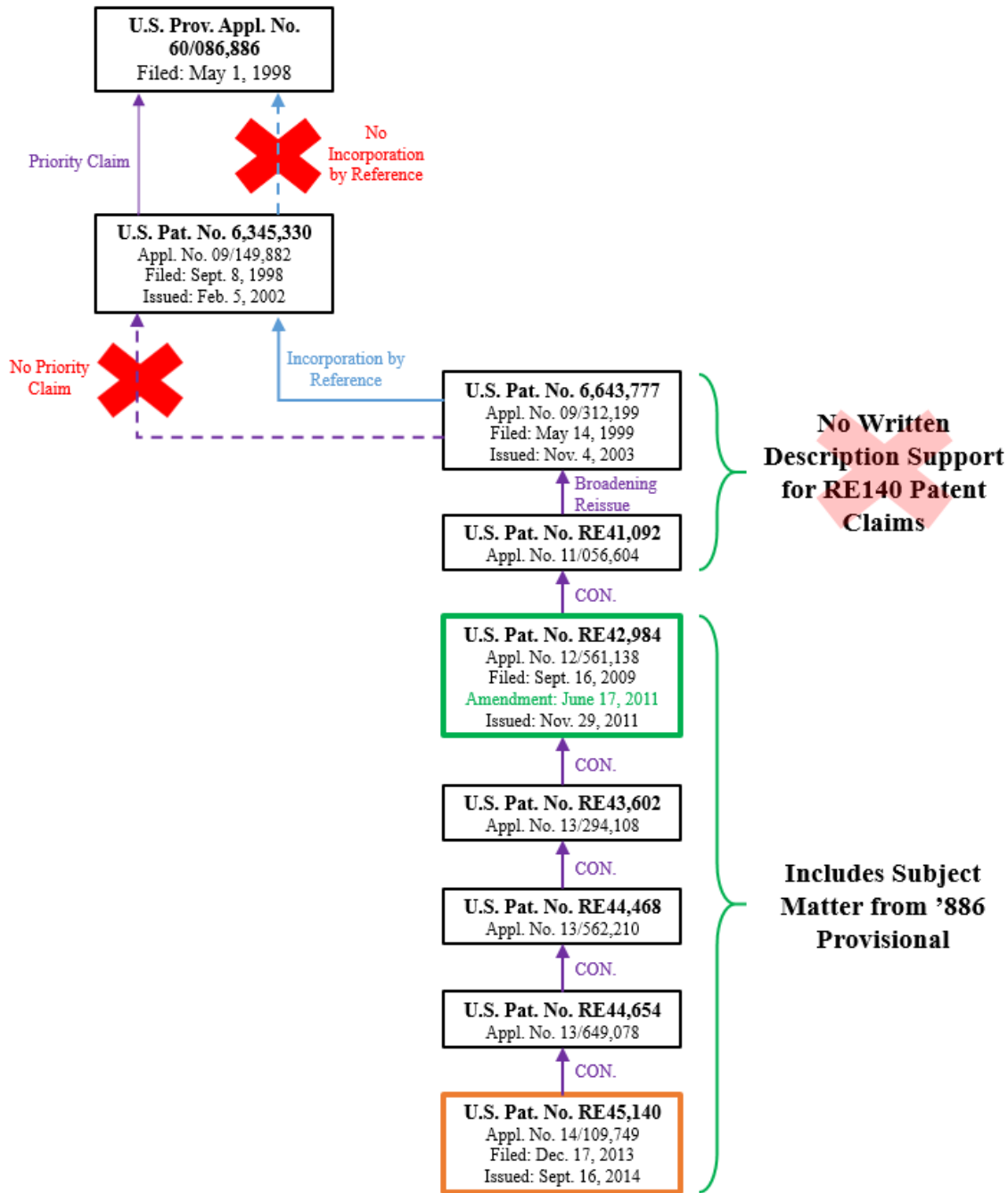
09/08/98

APPLICATION ELEMENTS See MPEP chapter 600 concerning utility patent application contents.		ADDRESS TO: Assistant Commissioner for Patents Box Patent Application Washington, DC 20231	
1. ☒ Fee Transmittal Form (Submit an original, and a duplicate for fee processing)		6. ☐ Microfiche Computer Program (Appendix)	
2. ☒ Specification (Total Pages 45) (preferred arrangement set forth below) - Descriptive title of the Invention - Cross References to Related Applications - Statement Regarding Fed sponsored R & D - Reference to Microfiche Appendix - Background of the Invention - Brief Summary of the Invention - Brief Description of the Drawings (if filed) - Detailed Description - Claim(s) - Abstract of the Disclosure		7. ☐ Nucleotide and/or Amino Acid Sequence Submission (if applicable, all necessary) a. ☐ Computer Readable Copy b. ☐ Paper Copy (identical to computer copy) c. ☐ Statement verifying identity of above copies	
3. ☒ Drawing(s) (35 USC 113) (Total Sheets 57)		ACCOMPANYING APPLICATION PARTS	
☐ Oath or Declaration (Total Pages 1)		8. ☐ Assignment Papers (cover sheet & document(s))	
a. ☐ Newly executed (original or copy)		9. ☐ 37 CFR 3.73(b) Statement (when there is an assignee) ☐ Power of Attorney	
b. ☐ Copy from a prior application (37 CFR 1.63(d) (for continuation/divisional with Box 17 completed) [Note Box 5 below]		10. ☐ English Translation Document (if applicable)	
i. ☐ DELETION OF INVENTOR(S) Signed statement attached deleting inventor(s) named in the prior application, see 37 CFR 1.63(d)(2) and 1.33(b)		11. ☐ Information Disclosure Statement (IDS)/PTO-1449 ☐ Copies of IDS Citations	
5. ☒ Incorporation By Reference (useable if Box 4b is checked) The entire disclosure of the prior application, from which a copy of the oath or declaration is supplied under Box 4b, is considered as being part of the disclosure of the accompanying application and is hereby incorporated by reference therein.		12. ☐ Preliminary Amendment	
		13. ☒ Return Receipt Postcard (MPEP 503) (Should be specifically itemized)	
		14. ☐ Small Entity ☐ Statement filed in prior application, Statement(s) Status still proper and desired	
		15. ☐ Certified Copy of Priority Document(s) (if foreign priority is claimed)	
		16. ☐	
17. If a CONTINUING APPLICATION, check appropriate box and supply the requisite information: ☐ Continuation ☐ Divisional ☐ Continuation-in-part (CIP) of prior application No: _____			

Ex. 1011 [Chu330 FH] at 79.

71. As shown above, there is no mention of the '886 Provisional anywhere on this page. Box 5 labeled "Incorporation By Reference (useable if Box 4b is checked)" is checked, as indicated by the "x." But Box 4b notes that it is "for continuation/divisional with Box 17 completed." There is no mention of the '886 Provisional in either Box 4b or 17. These boxes only mention "Continuation, Divisional, or Continuation-in-part (CIP)." There is simply no reference at all to the '886 Provisional anywhere on the application transmittal form.

72. In other words, Chu330 claims the benefit of the earlier filing date of the '886 Provisional but does not incorporate by reference the '886 Provisional. This is summarized in the schematic below.



73. Accordingly, in my opinion, the earliest priority date afforded to the claims of RE140 should be when Figures 19 and 20 and its associated descriptions

were added to RE984 (*i.e.*, June 17, 2011). All of the prior art that I rely on predate June 17, 2011—including the filing date of RE984, which was September 16, 2009.

B. Summary of the Prosecution History of RE140

74. I have reviewed the file history of RE140. I only saw one office action that rejected all claims of the RE140 based on an obviousness-type double patenting rejection. *See* Ex. 1006 [RE140 FH] at 203. ACQIS overcame this rejection by filing a terminal disclaimer. *See* Ex. 1006 [RE140 FH] at 230-32, 237-38. The claims were then allowed. *See* Ex. 1006 [RE140 FH] at 239-245.

75. There was no discussion or questions from the Examiner whether the material added from the '886 Provisional was new matter or not. Rather, it appears that the Examiner simply accepted the applicant's representation that the '886 Provisional was incorporated by reference into Chu330.

VI. Overview of the Prior Art References

A. Chu330 and Chu185

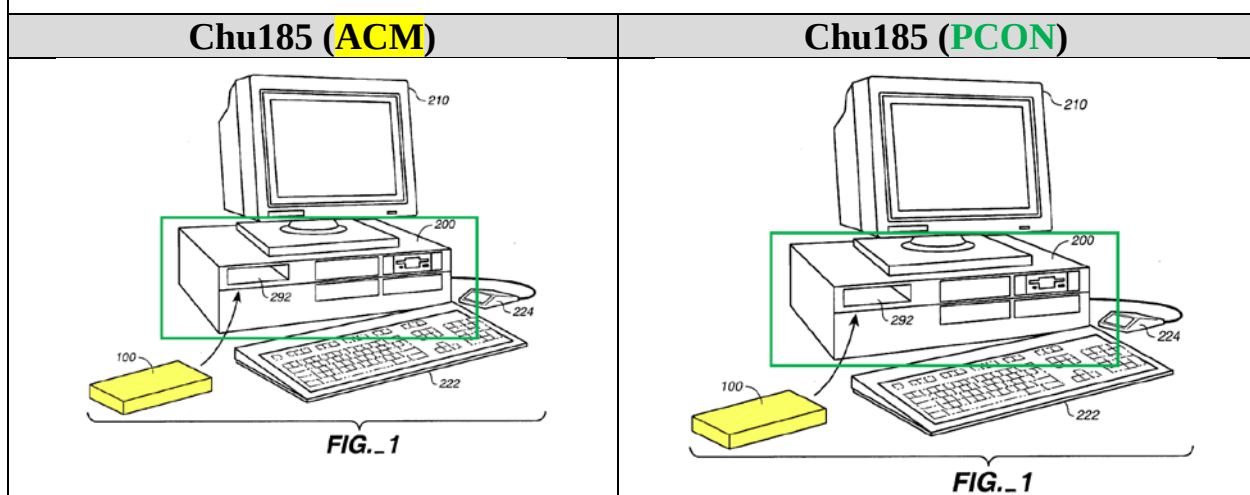
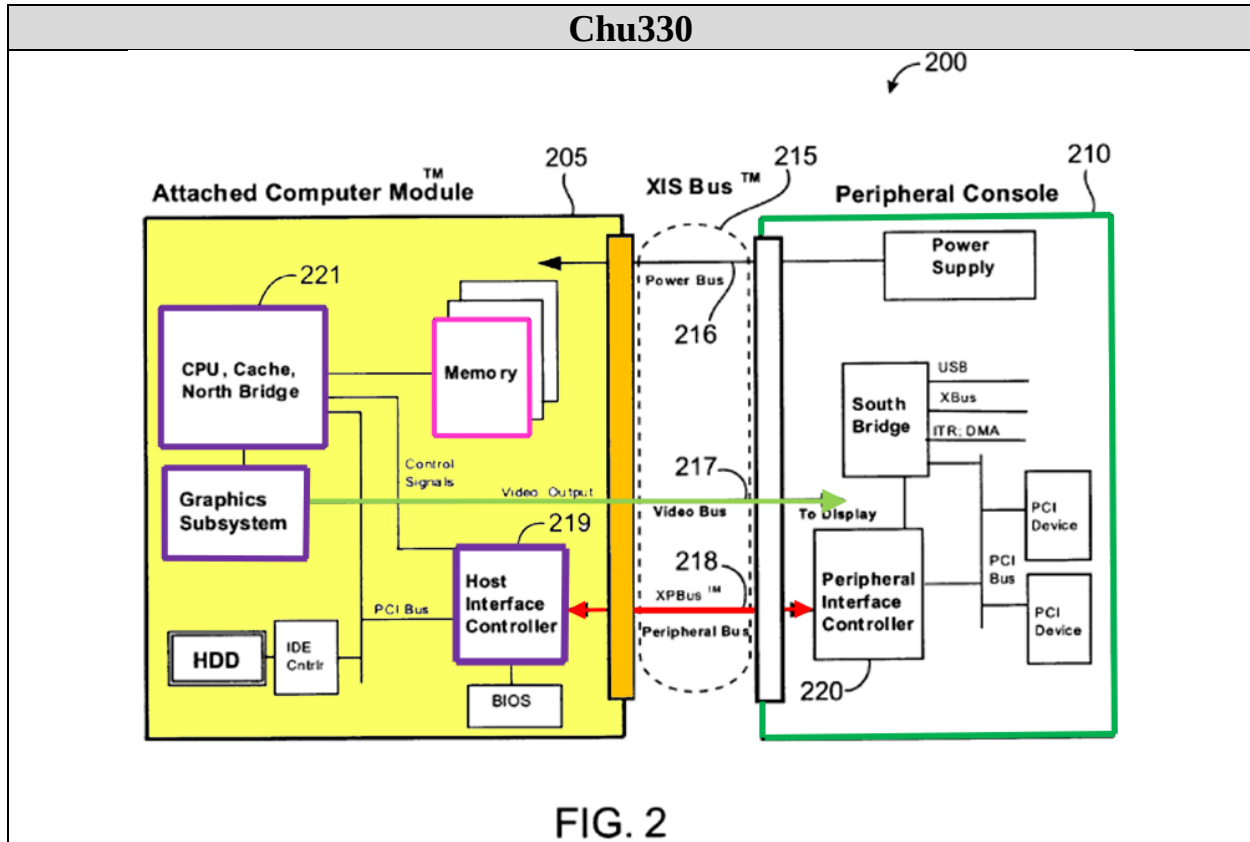
76. Chu330 and Chu185 were both filed on September 8, 1998. Ex. 1003 [Chu330] at Cover; Ex. 1005 [Chu185] at Cover. Chu330 incorporates by reference Chu185 by stating: "***Computer system 200 includes an attached computer module (ACM) 205 and a peripheral console 210***, which are described in greater detail in the application of William W.Y. Chu for 'Personal Computer Peripheral Console

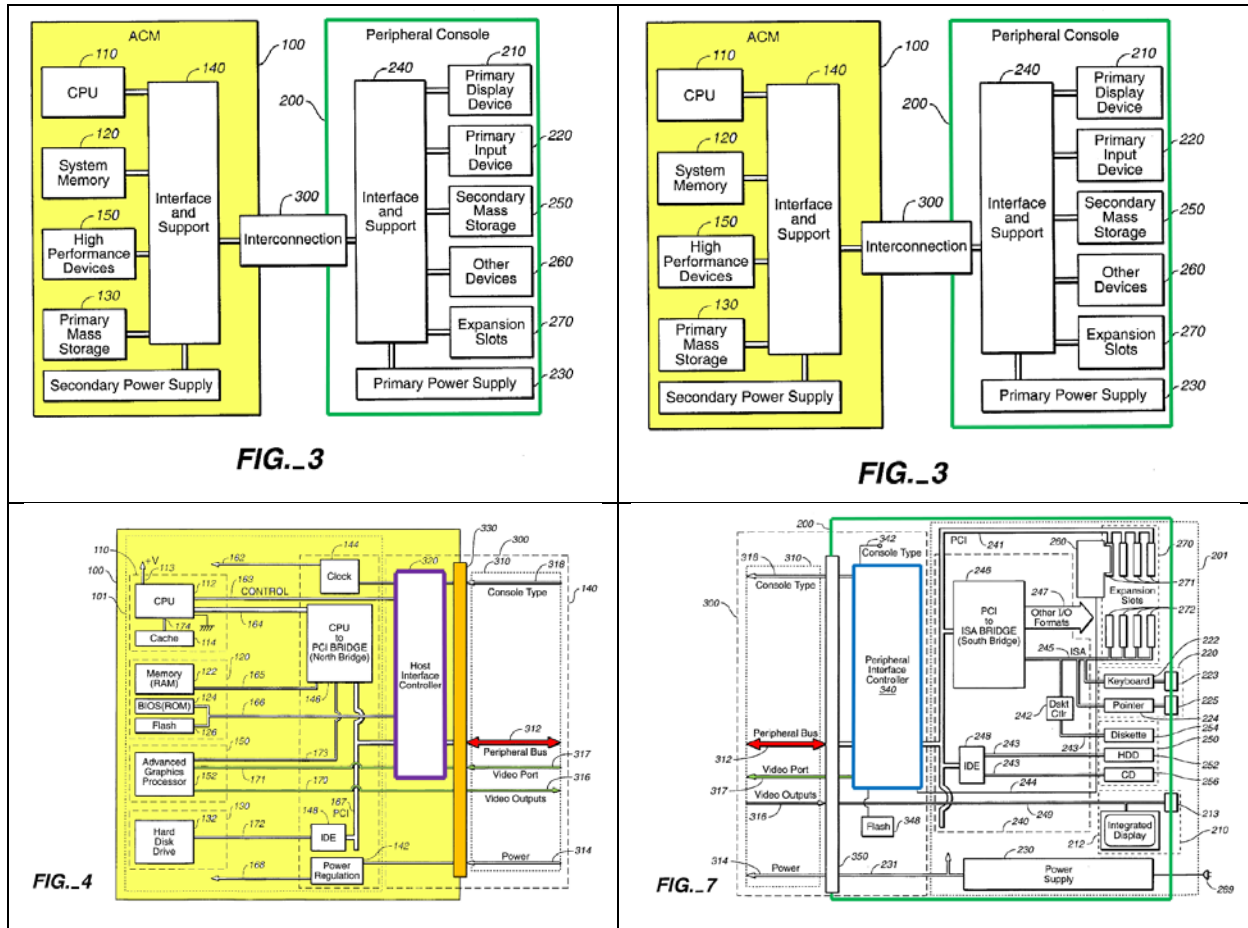
With Attached Computer Module' filed concurrently with the present application on Sep. 8, 1998 and ***incorporated herein by reference.***" Ex. 1003 [Chu330] at 6:1-7. *See also* Ex. 1003 [Chu330] at 1:11-15, 1:54-62.

77. Similarly, Chu185 incorporates by reference Chu330 by stating: "***The preferred ACM-to-PCON Interconnection 300*** is described in detail in a companion U.S. patent application, Ser. No. 09/149,882, entitled 'A Communication Channel and Interface Devices for Bridging Computer Interface Buses,' by the same inventor, filed on the same day herewith, and ***hereby incorporated by reference.***" Ex. 1005 [Chu185] at 5:66-6:4. *See also* Ex. 1005 at 1:11-16.

78. As such, I have been informed and understand that Chu185 should be considered to be part of Chu330.

79. Figure 2 of Chu330, reproduced below, is identical to Figure 13 of RE140, except for small changes in the numbering in the figures. As shown, some high level details of **ACM 205** and **PCON 210** and the interconnection between the two are shown. Figures 1, 3, 4, and 7 of Chu185 likewise show the **ACM 205** and **PCON 210** with varying degrees of detail. *See also* Ex. 1005 [Chu185] at 5:66-6:8.



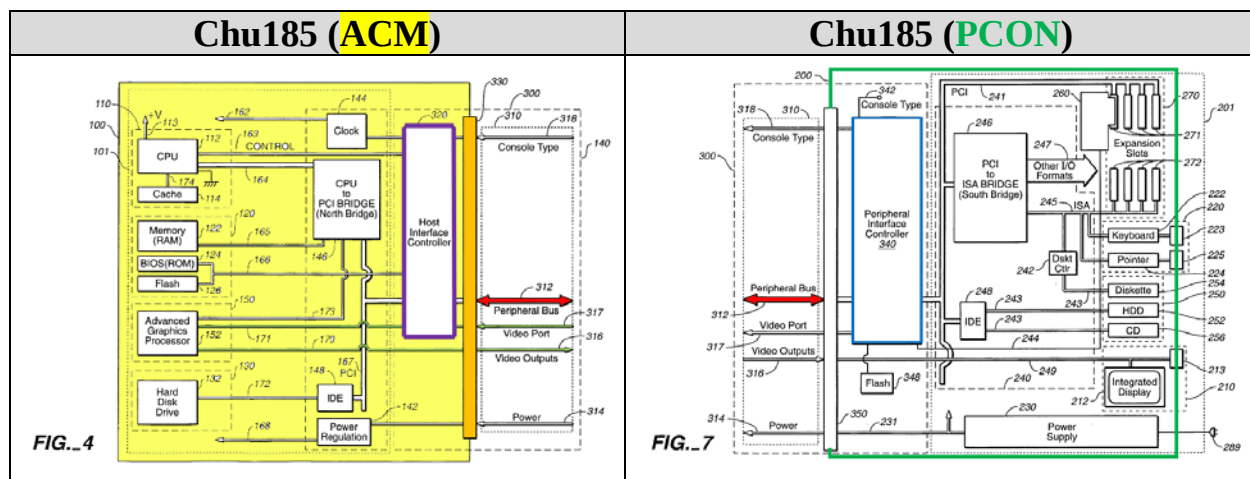


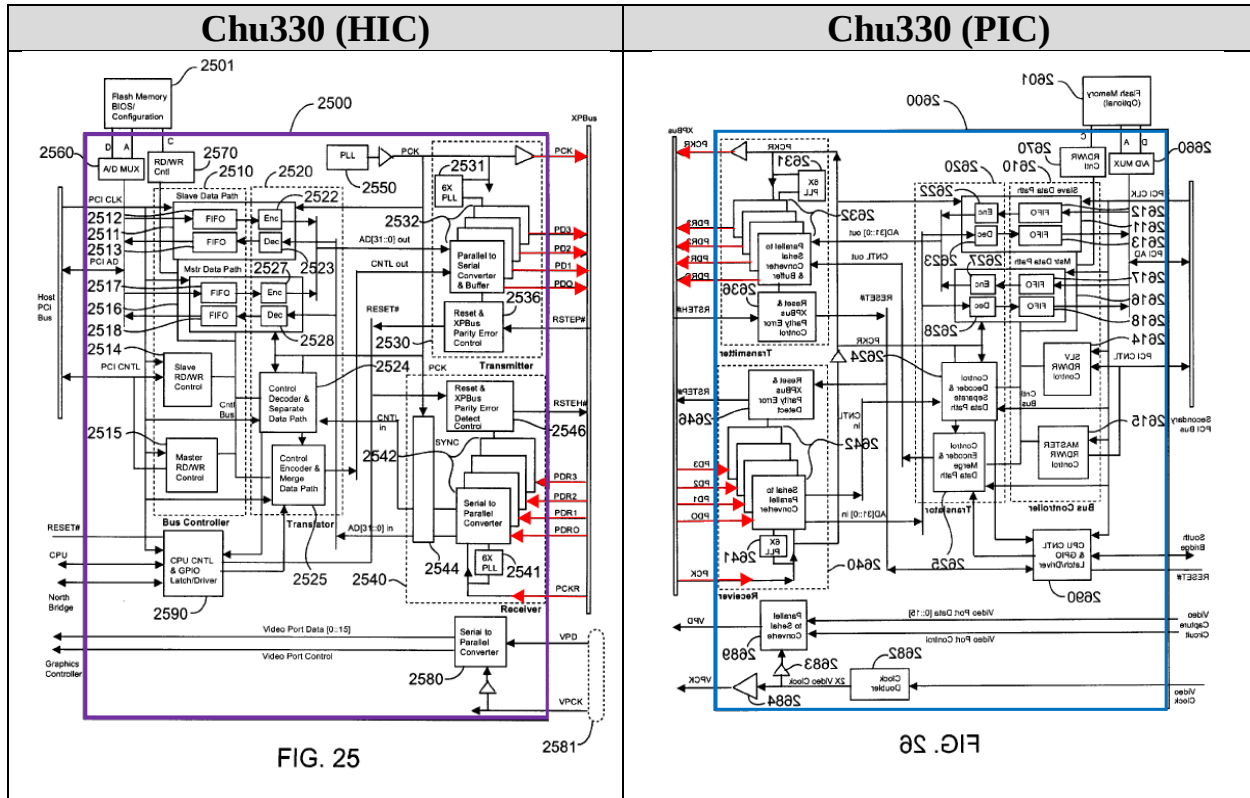
80. Specifically, Figures 4 and 7 of Chu185 (as shown above) show the **Host Interface Controller (HIC) 320** in the **ACM** and the **Peripheral Interface Controller (PIC) 340** in the **PCON** connected together through the “ACM connector component 330.” See Ex. 1005 [Chu185] at 5:57-66.

81. The connection between **ACM** and **PCON** is further detailed in Figure 25 and 26 of Chu330. “FIG. 25 shows a detailed block diagrams of the HIC shown in FIG. 24,” Ex. 1003 [Chu330] at 16:24-25, where “data packet types transmitted

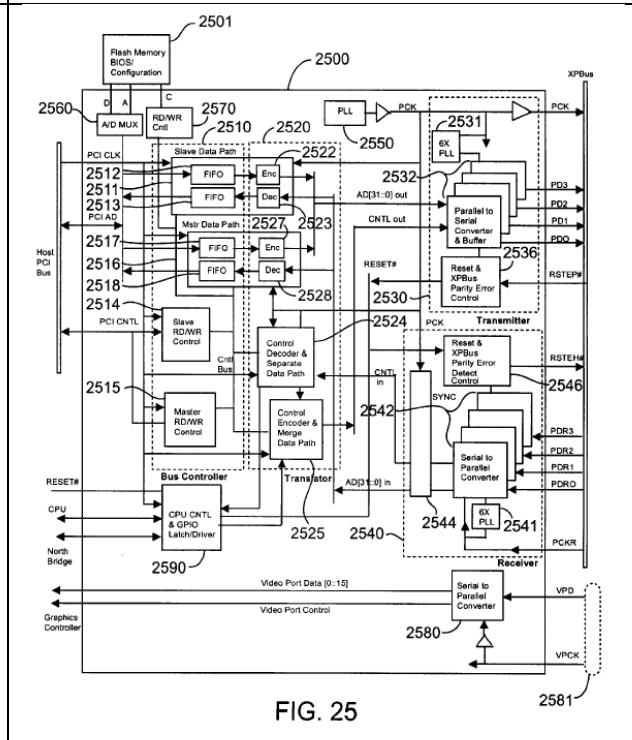
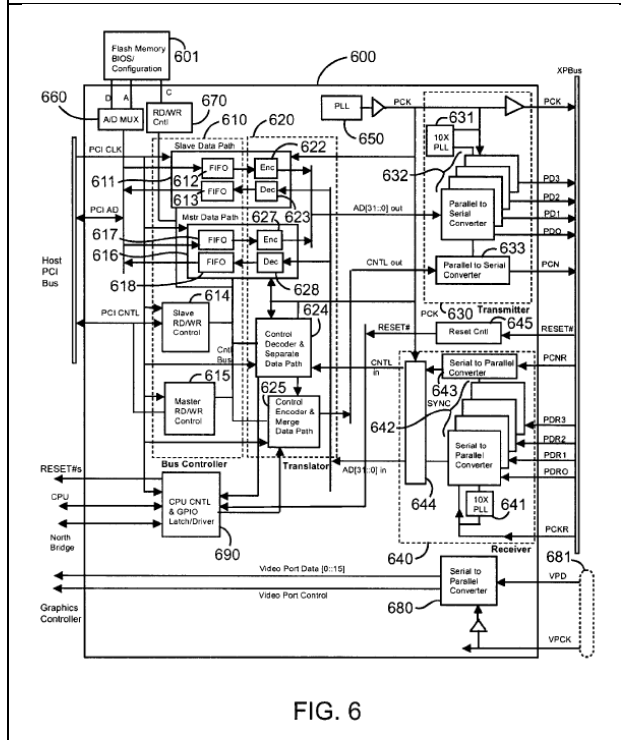
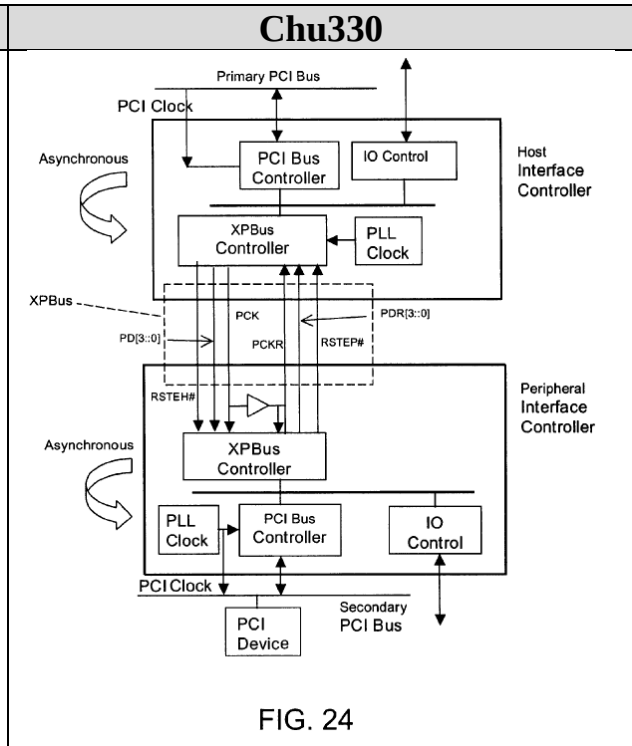
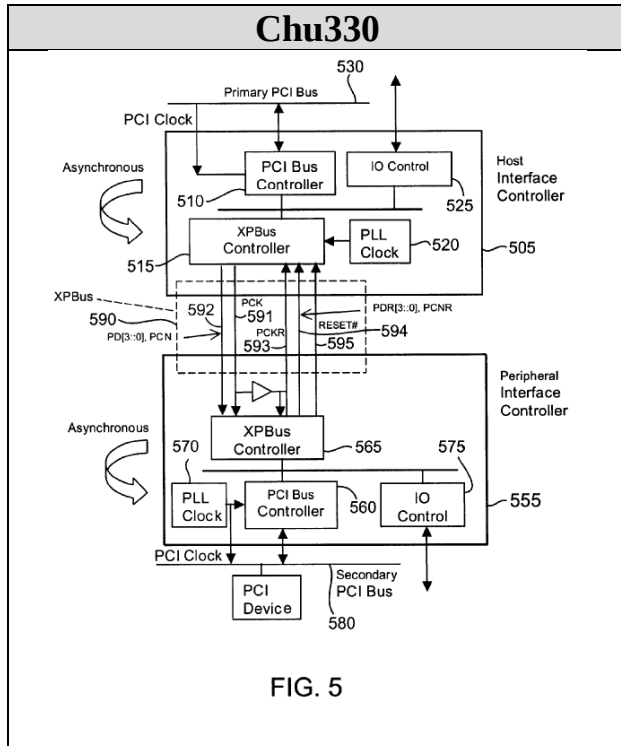
from HIC 2500 to PIC 2600 and from PIC 2600 to HIC 2500, respectively ... on lines PD0 to PD3 and ... on lines PDR0 to PDR3.” Ex. 1003 [Chu330] at 18:11-19.

I have highlighted in red, the additional details regarding the XPBus (Peripheral Bus) below in these figures. As shown, there are numerous **individual data, signal, and clock lines** between the **HIC** and **PIC**. See Ex. 1003 [Chu330] at 16:25-26, 17:8-17.





82. In addition, Figure 24 of Chu330 shows “a block diagram of another embodiment of the HIC and PIC ... and the interface therebetween.” Ex. 1003 [Chu330] at 16:6-8. Moreover, “FIG. 25 shows a detailed block diagrams of the HIC shown in FIG. 24,” Ex. 1003 [Chu330] at 16:24-25, where “data packet types transmitted from HIC 2500 to PIC 2600 and from PIC 2600 to HIC 2500, respectively ... on lines PD0 to PD3 and ... on lines PDR0 to PDR3.” Ex. 1003 [Chu330] at 18:11-19. Figures 24 and 25 are very similar to Figures 5 and 6 of Chu330 in that they both show multiple data lines, such as **PD0** through **PDR3**.



83. Figures 33 and 34 “are tables showing the data packet types transmitted from HIC 2500 to PIC 2600 and from PIC 2600 to HIC 2500, respectively.” Ex. 1003 [Chu330] at 18:11-13. I have highlighted the “reserved” data packets, which can be identified by “[t]he bits sent in the first nibble of each data packet.” Ex. 1003 [Chu330] at 19:22-25. Specifically, “FIG. 35 is a table showing different types of first nibbles and their corresponding data packet types.” Ex. 1003 [Chu330] at 19:22-25. I have highlighted in blue the “reserved” data packets, because those data packets “can be used to support non-PCI bus transactions, e.g., USB transactions.” Ex. 1003 [Chu330] at 19:13-15.

Chu330		RE140	
ID bits (P0 P1 P2 P3)	Data Packet Type	ID bits (P0 P1 P2 P3)	Data Packet Type
X X 0 0	PCI 1st address/data segment	X X 0 0	PCI 1st address/data segment
X X 1 0	PCI 2nd address/data segment	X X 1 0	PCI 2nd address/data segment
0 0 0 1	Control 1st segment with PCI response	0 0 0 1	Control 1st segment with PCI response
1 0 0 1	Control 1st segment without PCI response	1 0 0 1	Control 1st segment without PCI response
0 1 0 1	Control 2nd segment with PCI response	0 1 0 1	Control 2nd segment with PCI response
1 1 0 1	Control 2nd segment without PCI response	1 1 0 1	Control 2nd segment without PCI response
0 0 1 1	Reserved	0 0 1 1	Reserved
1 0 1 1	Reserved	1 0 1 1	Reserved
0 1 1 1	Initialization	0 1 1 1	Initialization
1 1 1 1	NOOP	1 1 1 1	NOOP

FIG. 35

FIG. 24

NEW SHEET

84. In other words, Chu330 teaches that as data flows into the HIC, when the first nibble indicates XX00, a PCI bus transaction is transmitted utilizing the LVDS lines, such as PD0 to PDR3. Then, if the next set of data coming in includes

as the first nibbles 0011, a USB transaction is transmitted utilizing the same set of LVDS lines, such as PD0 to PDR3.

85. In my opinion, these different “embodiments” of Chu330 and Chu185 can be combined by a POSITA for a variety of reasons. First, Chu330 and Chu185 expressly teach a POSITA to make these combinations and modifications. For example, Chu330 and Chu185 both direct a POSITA to find additional details about the **ACM**, **PCON**, and the **ACM**-to-**PCON** Interconnection in each other. Second, even ACQIS appears to think these modifications were possible by explicitly adding only a portion of the embodiment directed to Figure 35 and preparing claims that are based on a combination of these embodiments. Accordingly, in my opinion, a POSITA would have been able to make such a combination or modification with a reasonable expectation of success based on the explicit teachings found in Chu330 and 185.

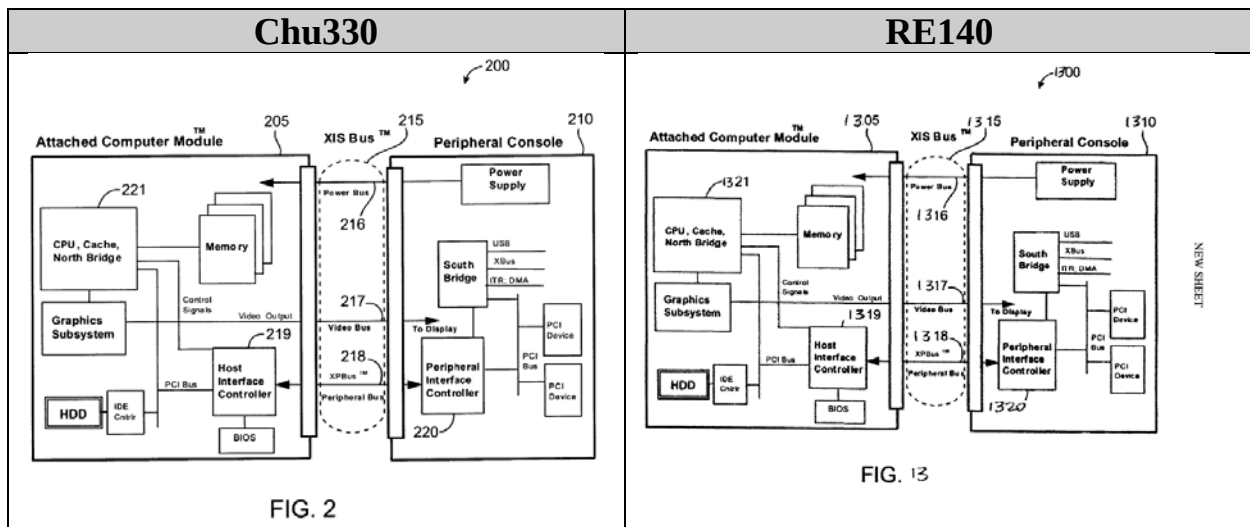
86. A POSITA would have been able to combine the teachings of found in Chu330 and Chu185. First, Chu330 explicitly teaches a POSITA to combine the teachings of Chu185 with Chu330. *See, e.g.*, Ex. 1003 [Chu330] at 1:54-62 (“However, in the context of the computer system of the present invention, which is described in the present inventor’s (William W.Y. Chu’s) application for ‘Personal Computer Peripheral Console With Attached Computer Module’ filed concurrently

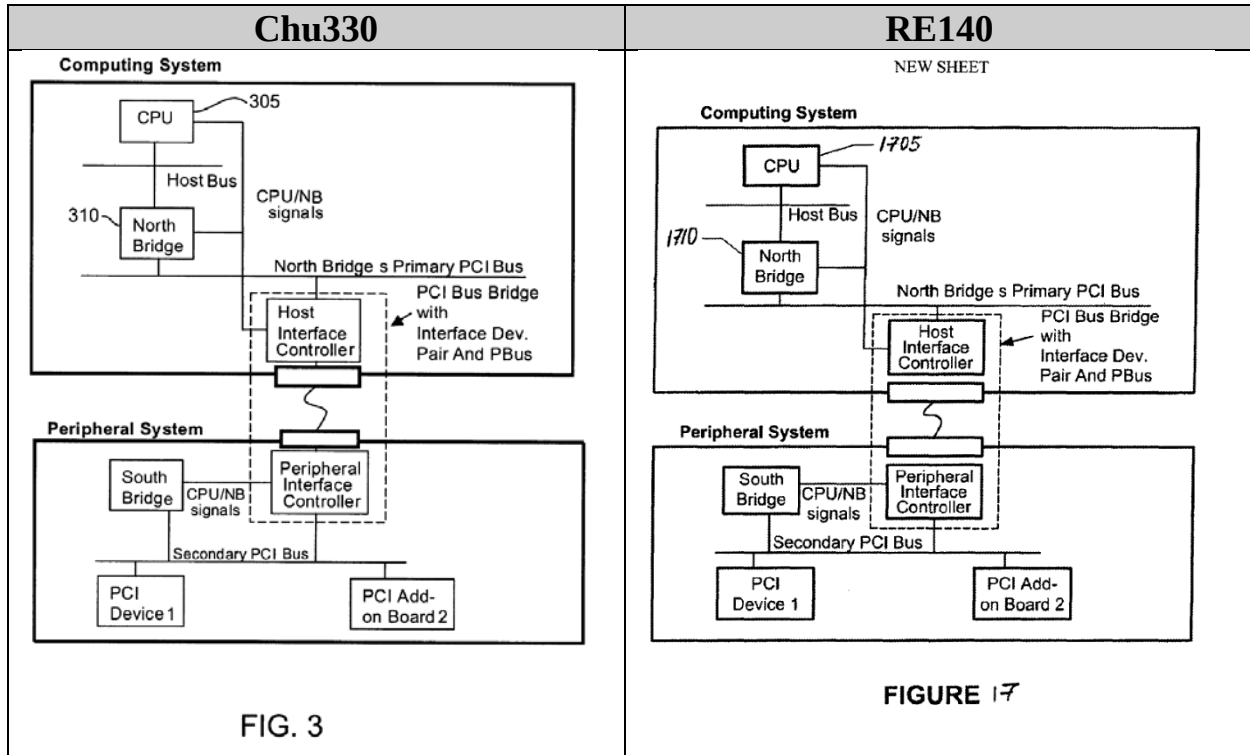
with the present application on Sep. 8, 1998 and incorporated herein by reference, a cable friendly interface is desired for interfacing an attached computer module (ACM) and a peripheral console of the present invention.”); Ex. 1003 [Chu330] at 6:1-7 (“Computer system 200 includes an attached computer module (ACM) 205 and a peripheral console 210, which are described in greater detail in the application of William W.Y. Chu for ‘Personal Computer Peripheral Console with Attached Computer Module’ filed concurrently with the present application on Sep. 8, 1998 and incorporated herein by reference.”).

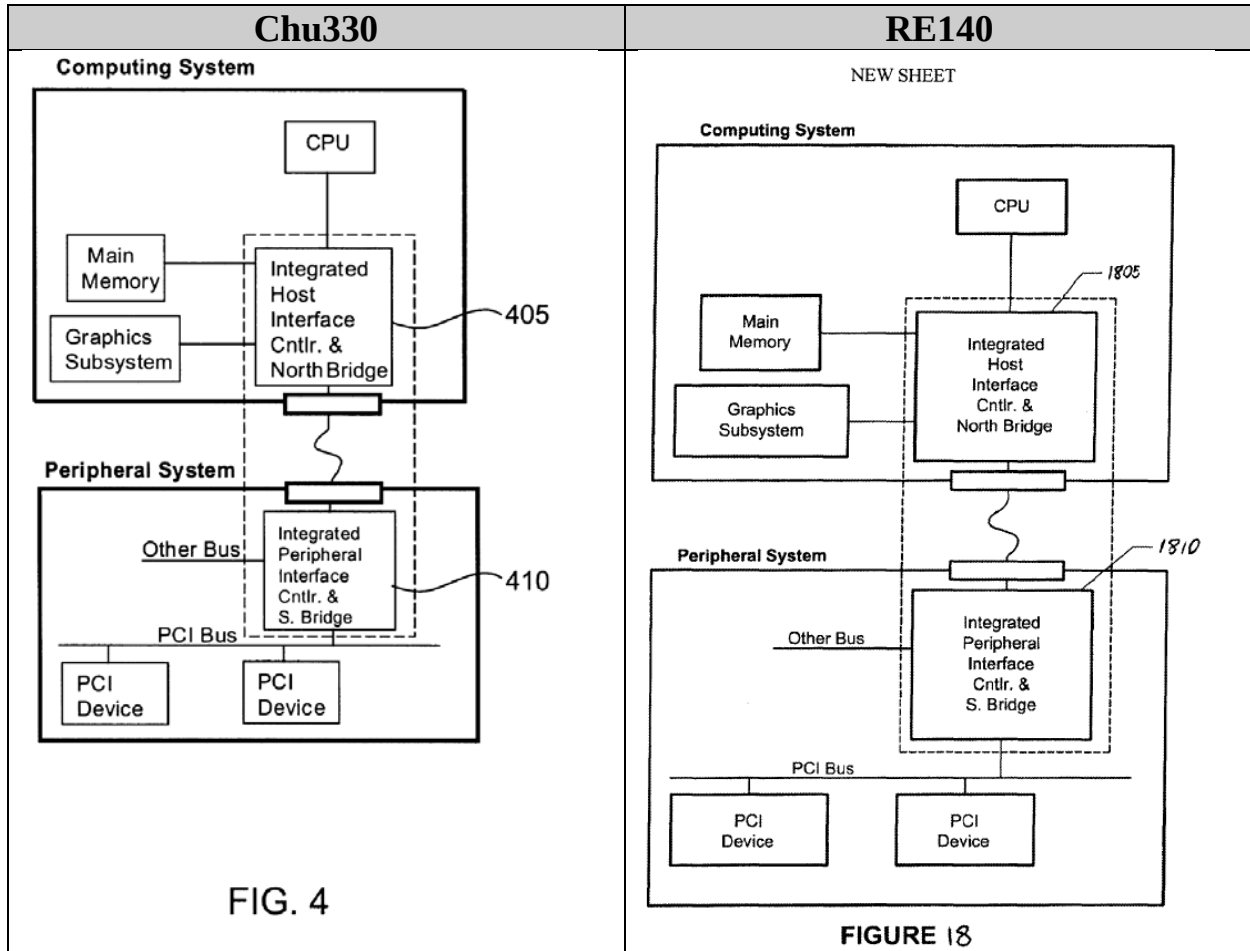
87. Second, Chu185 also explicitly teaches a POSITA to combine the teachings of Chu330 with Chu185. Ex. 1005 [Chu185] at 1:12-17 (“This application is being filed concurrently with the application of William W.Y. Chu for ‘A Communication Channel and Interface Devices for Bridging Computer Interface Buses’, U.S. application No. 09/149,882 filed on Sept. 8, 1998 and incorporates the material therein by reference.”), 5:66-6:4 (“The preferred ACM-to-PCON Interconnection 300 is described in detail in a companion U.S. patent application, Ser. No. 09/149,882, entitled ‘A Communication Channel and Interface Devices for Bridging Computer Interface Buses,’ by the same inventor, filed on the same day herewith, and hereby incorporated by reference.”).

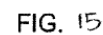
88. Combining the different teachings found in Chu330 and Chu185 would have merely amounted to combining prior art elements according to known methods to yield predictable results with a reasonable expectation of success. In fact, the references all include explicit teaching, suggestion, and/or motivation to combine the different teachings.

89. I reproduce below the figures in RE140 that are identical to those found in Chu330. They are identical figures, except that the numberings have been modified.





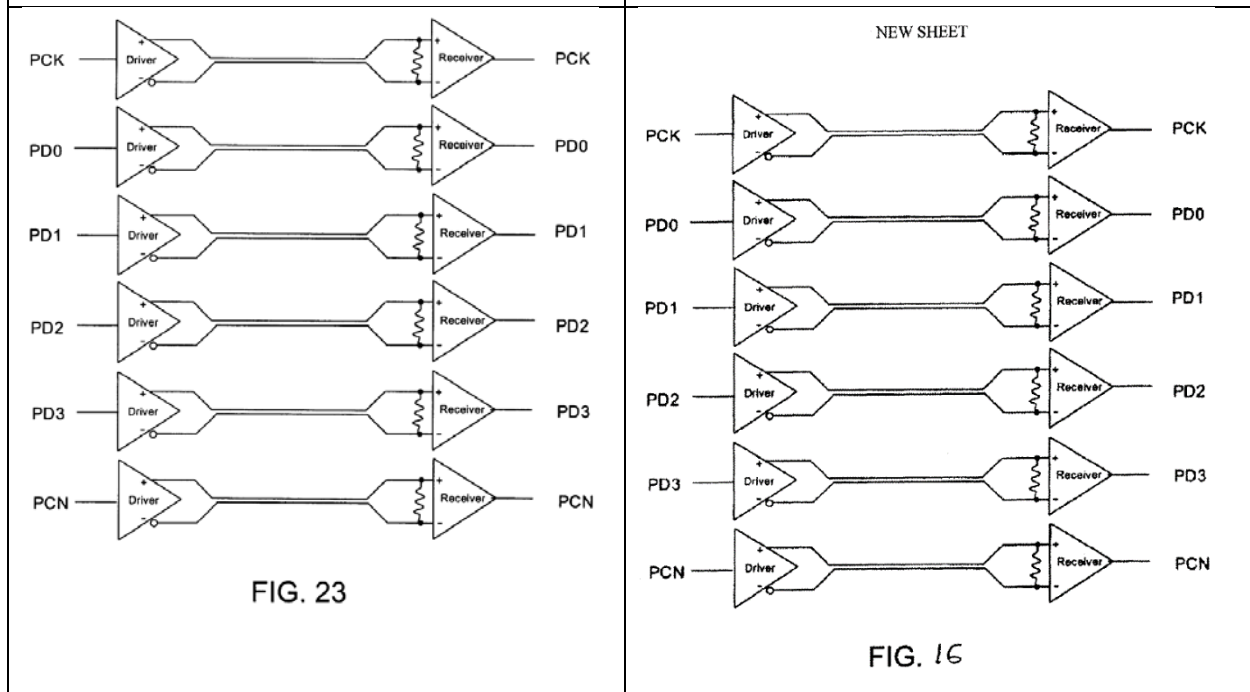




Chu330					RE140				
	Symbol	Signal	Data Rate	Description		Symbol	Signal	Data Rate	Description
1	PD0 RTN			GND	1	PD0 RTN			GND
2	PD0 +	Synch. To PCK	10 x clock rate	Computer to Peripheral LVDS Data 0 +	2	PD0 +	Synch. To PCK	10 x clock rate	Computer to Peripheral LVDS Data 0 +
3	PD0 -			Computer to Peripheral LVDS Data 0 -	3	PD0 -			Computer to Peripheral LVDS Data 0 -
4	PD1 RTN			GND	4	PD1 RTN			GND
5	PD1 +	Synch. To PCK	10 x clock rate	Computer to Peripheral LVDS Data 1 +	5	PD1 +	Synch. To PCK	10 x clock rate	Computer to Peripheral LVDS Data 1 +
6	PD1 -			Computer to Peripheral LVDS Data 1 -	6	PD1 -			Computer to Peripheral LVDS Data 1 -
7	PD2 RTN			GND	7	PD2 RTN			GND
8	PD2 +	Synch. To PCK	10 x clock rate	Computer to Peripheral LVDS Data 2 +	8	PD2 +	Synch. To PCK	10 x clock rate	Computer to Peripheral LVDS Data 2 +
9	PD2 -			Computer to Peripheral LVDS Data 2 -	9	PD2 -			Computer to Peripheral LVDS Data 2 -
10	PD3 RTN			GND	10	PD3 RTN			GND
11	PD3 +	Synch. To PCK	10 x clock rate	Computer to Peripheral LVDS Data 3 +	11	PD3 +	Synch. To PCK	10 x clock rate	Computer to Peripheral LVDS Data 3 +
12	PD3 -			Computer to Peripheral LVDS Data 3 -	12	PD3 -			Computer to Peripheral LVDS Data 3 -
13	PCK RTN			GND	13	PCK RTN			GND
14	PCK +	Clock	Clock rate	Computer to Peripheral LVDS Clock +	14	PCK +	Clock	Clock rate	Computer to Peripheral LVDS Clock +
15	PCK -			Computer to Peripheral LVDS Clock -	15	PCK -			Computer to Peripheral LVDS Clock -
16	PCN RTN			GND	16	PCN RTN			GND
17	PCN +	Synch. To PCK	10 x clock rate	Computer to Peripheral LVDS Control +	17	PCN +	Synch. To PCK	10 x clock rate	Computer to Peripheral LVDS Control +
18	PCN -			Computer to Peripheral LVDS Control -	18	PCN -			Computer to Peripheral LVDS Control -
19	PDR0 RTN			GND	19	PDR0 RTN			GND
20	PDR0 +	Synch. To PCKR	10 x clock rate	Peripheral to Computer LVDS Data 0 +	20	PDR0 +	Synch. To PCKR	10 x clock rate	Peripheral to Computer LVDS Data 0 +
21	PDR0 -			Peripheral to Computer LVDS Data 0 -	21	PDR0 -			Peripheral to Computer LVDS Data 0 -
22	PDR1 RTN			GND	22	PDR1 RTN			GND
23	PDR1 +	Synch. To PCKR	10 x clock rate	Peripheral to Computer LVDS Data 1 +	23	PDR1 +	Synch. To PCKR	10 x clock rate	Peripheral to Computer LVDS Data 1 +
24	PDR1 -			Peripheral to Computer LVDS Data 1 -	24	PDR1 -			Peripheral to Computer LVDS Data 1 -
25	PDR2 RTN			GND	25	PDR2 RTN			GND
26	PDR2 +	Synch. To PCKR	10 x clock rate	Peripheral to Computer LVDS Data 2 +	26	PDR2 +	Synch. To PCKR	10 x clock rate	Peripheral to Computer LVDS Data 2 +
27	PDR2 -			Peripheral to Computer LVDS Data 2 -	27	PDR2 -			Peripheral to Computer LVDS Data 2 -
28	PDR3 RTN			GND	28	PDR3 RTN			GND
29	PDR3 +	Synch. To PCKR	10 x clock rate	Peripheral to Computer LVDS Data 3 +	29	PDR3 +	Synch. To PCKR	10 x clock rate	Peripheral to Computer LVDS Data 3 +
30	PDR3 -			Peripheral to Computer LVDS Data 3 -	30	PDR3 -			Peripheral to Computer LVDS Data 3 -
31	PCKR RTN			GND	31	PCKR RTN			GND
32	PCKR +	Reverse Dir. Clock	Clock rate	Peripheral to Computer LVDS Clock +	32	PCKR +	Reverse Dir. Clock	Clock rate	Peripheral to Computer LVDS Clock +
33	PCKR -			Peripheral to Computer LVDS Clock -	33	PCKR -			Peripheral to Computer LVDS Clock -
34	PCNR RTN			GND	34	PCNR RTN			GND
35	PCNR +	Synch. To PCKR	10 x Clock rate	Peripheral to Computer LVDS Control +	35	PCNR +	Synch. To PCKR	10 x Clock rate	Peripheral to Computer LVDS Control +
36	PCNR -			Peripheral to Computer LVDS Control -	36	PCNR -			Peripheral to Computer LVDS Control -
37	RESET#		Asynchronous	Reset	37	RESET#		Asynchronous	Reset

FIG. 20

FIG. 23



Declaration of Dr. Bill Lin
U.S. Reissued Patent No. 45,140
Claims 14-38

Chu330					RE140				
Pin No.	Symbol	Signal	Standard	Description	Pin No.	Symbol	Signal	Standard	Description
P2	PDR0 +	LVDS		Peripheral data reverse 0 +	P2	PDR0 +	LVDS		Peripheral data reverse 0 +
P3	PDR0 -	LVDS		Peripheral data reverse 0 -	P3	PDR0 -	LVDS		Peripheral data reverse 0 -
P5	PDR1 +	LVDS		Peripheral data reverse 1 +	P5	PDR1 +	LVDS		Peripheral data reverse 1 +
P6	PDR1 -	LVDS		Peripheral data reverse 1 -	P6	PDR1 -	LVDS		Peripheral data reverse 1 -
P8	PDR2 +	LVDS		Peripheral data reverse 2 +	P8	PDR2 +	LVDS		Peripheral data reverse 2 +
P9	PDR2 -	LVDS		Peripheral data reverse 2 -	P9	PDR2 -	LVDS		Peripheral data reverse 2 -
P11	PCKR +	LVDS		Peripheral clock reverse +	P11	PCKR +	LVDS		Peripheral clock reverse +
P12	PCKR -	LVDS		Peripheral clock reverse -	P12	PCKR -	LVDS		Peripheral clock reverse -
P15	PDR3 +	LVDS		Peripheral data reverse 3 +	P15	PDR3 +	LVDS		Peripheral data reverse 3 +
P16	PDR3 -	LVDS		Peripheral data reverse 3 -	P16	PDR3 -	LVDS		Peripheral data reverse 3 -
P18	PCNR +	LVDS		Peripheral control reverse +	P18	PCNR +	LVDS		Peripheral control reverse +
P19	PCNR -	LVDS		Peripheral control reverse -	P19	PCNR -	LVDS		Peripheral control reverse -
P24	PD0 +	LVDS		Peripheral data 0 +	P24	PD0 +	LVDS		Peripheral data 0 +
P25	PD0 -	LVDS		Peripheral data 0 -	P25	PD0 -	LVDS		Peripheral data 0 -
P27	PD1 +	LVDS		Peripheral data 1 +	P27	PD1 +	LVDS		Peripheral data 1 +
P28	PD1 -	LVDS		Peripheral data 1 -	P28	PD1 -	LVDS		Peripheral data 1 -
P30	PD2 +	LVDS		Peripheral data 2 +	P30	PD2 +	LVDS		Peripheral data 2 +
P31	PD2 -	LVDS		Peripheral data 2 -	P31	PD2 -	LVDS		Peripheral data 2 -
P33	PCK +	LVDS		Peripheral clock +	P33	PCK +	LVDS		Peripheral clock +
P34	PCK -	LVDS		Peripheral clock -	P34	PCK -	LVDS		Peripheral clock -
P37	PD3 +	LVDS		Peripheral data 3 +	P37	PD3 +	LVDS		Peripheral data 3 +
P38	PD3 -	LVDS		Peripheral data 3 -	P38	PD3 -	LVDS		Peripheral data 3 -
P40	PCN +	LVDS		Peripheral control +	P40	PCN +	LVDS		Peripheral control +
P41	PCN -	LVDS		Peripheral control -	P41	PCN -	LVDS		Peripheral control -
P13	Config 0	Static	3.3v or GND	Configuration bit 0	P13	Config 0	Static	3.3v or GND	Configuration bit 0
P35	Config 1	Static	3.3v or GND	Configuration bit 1	P35	Config 1	Static	3.3v or GND	Configuration bit 1
P1,P4,P7,P10, P14,P17,P23,P26, P29,P32,P36,P39	GND		GND	Ground	P1,P4,P7,P10, P14,P17,P23,P26, P29,P32,P36,P39	GND		GND	Ground

FIG. 18

Pin No.	Symbol	Signal	Standard	Description	Pin No.	Symbol	Signal	Standard	Description
V2	Red Video	Analog		Video	V2	Red Video	Analog		Video
V4	Green Video	Analog		Video	V4	Green Video	Analog		Video
V6	Blue Video	Analog		Video	V6	Blue Video	Analog		Video
V8	HSYNC			Horizontal Sync	V8	HSYNC			Horizontal Sync
V9	VSNC			Vertical Sync	V9	VSNC			Vertical Sync
V11	DDC2 SCL		VESA DDC std 2	DDC Clock	V11	DDC2 SCL		VESA DDC std 2	DDC Clock
V12	DDC2 SDA		VESA DDC std 2	DDC Data	V12	DDC2 SDA		VESA DDC std 2	DDC Data
V14	TV-CV/CNTL 0			TV Composite Video	V14	TV-CV/CNTL 0			TV Composite Video
V15	SV Y/CNTL 1		Super Video	SV Luminance or Control 1	V15	SV Y/CNTL 1		Super Video	SV Luminance or Control 1
V16	SV C/CNTL 2		Super Video	SV Chrominance or Control 2	V16	SV C/CNTL 2		Super Video	SV Chrominance or Control 2
V24	D0 +	TMDS	VESA P & D	Data 0 +	V24	D0 +	TMDS	VESA P & D	Data 0 +
V25	D0 -	TMDS	VESA P & D	Data 0 -	V25	D0 -	TMDS	VESA P & D	Data 0 -
V27	CLK +	TMDS	VESA P & D	Clock +	V27	CLK +	TMDS	VESA P & D	Clock +
V28	CLK -	TMDS	VESA P & D	Clock -	V28	CLK -	TMDS	VESA P & D	Clock -
V30	D1 +	TMDS	VESA P & D	Data 1 +	V30	D1 +	TMDS	VESA P & D	Data 1 +
V31	D1 -	TMDS	VESA P & D	Data 1 -	V31	D1 -	TMDS	VESA P & D	Data 1 -
V33	D2 +	TMDS	VESA P & D	Data 2 +	V33	D2 +	TMDS	VESA P & D	Data 2 +
V34	D2 -	TMDS	VESA P & D	Data 2 -	V34	D2 -	TMDS	VESA P & D	Data 2 -
V37	VPCK +	LVDS		Video Port Pixel Clock +	V37	VPCK +	LVDS		Video Port Pixel Clock +
V38	VPCK -	LVDS		Video Port Pixel Clock -	V38	VPCK -	LVDS		Video Port Pixel Clock -
V40	VPD +	LVDS		Video Port Pixel Data +	V40	VPD +	LVDS		Video Port Pixel Data +
V41	VPD -	LVDS		Video Port Pixel Data -	V41	VPD -	LVDS		Video Port Pixel Data -
V13	Config 2		3.3v or GND	Configuration bit 2	V13	Config 2		3.3v or GND	Configuration bit 2
V35	Config 3		3.3v or GND	Configuration bit 3	V35	Config 3		3.3v or GND	Configuration bit 3
V1,V3,V5,V7, V10,V23,V26, V29,V32,V36, V39,V42,V43, V44	GND		GND	Ground	V1,V3,V5,V7, V10,V23,V26, V29,V32,V36, V39,V42,V43, V44	GND		GND	Ground

FIG. 19

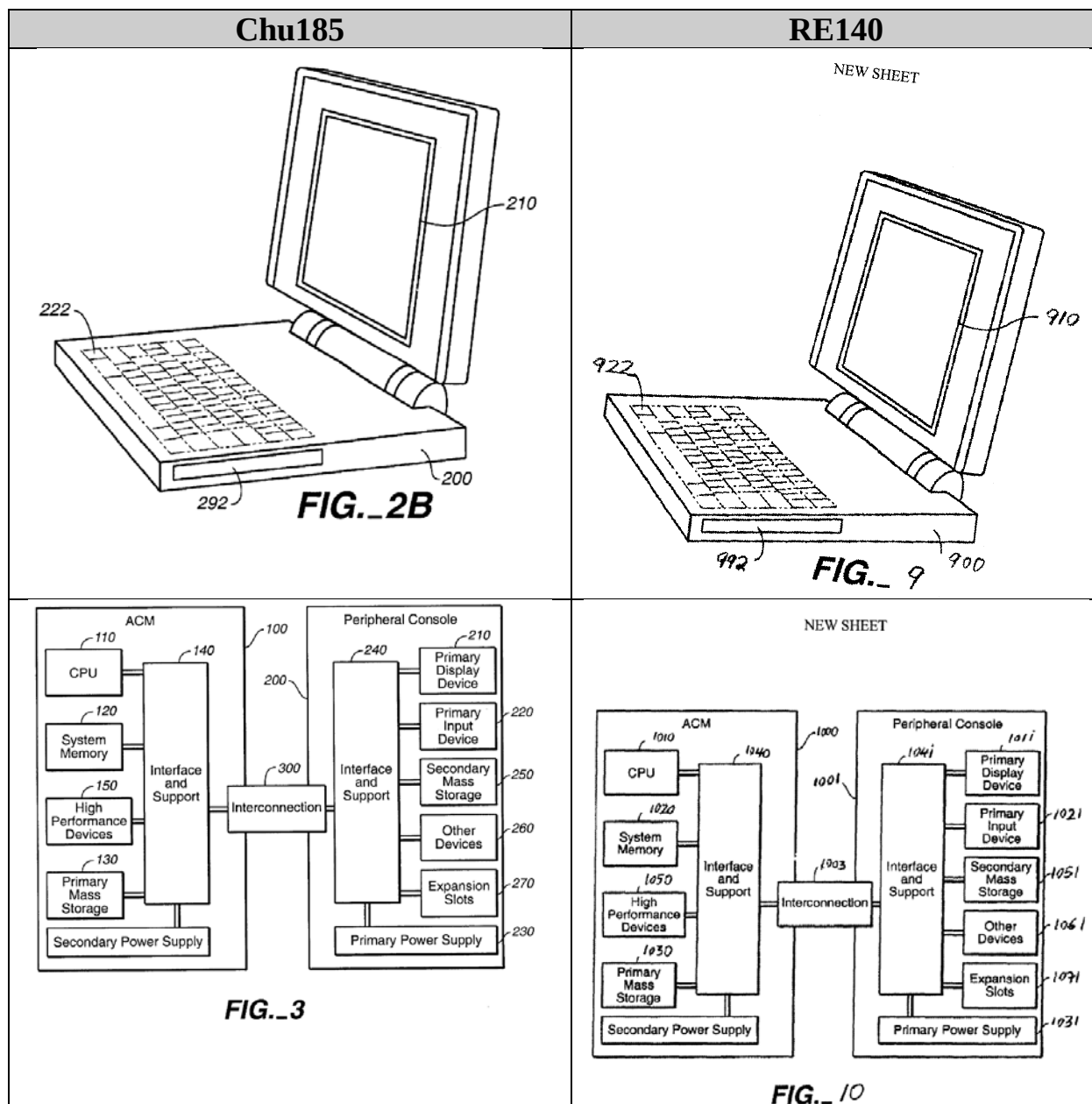
ID bits (P0 P1 P2 P3)	Data Packet Type	ID bits (P0 P1 P2 P3)	Data Packet Type
X X 0 0	PCI 1st address/data segment	X X 0 0	PCI 1st address/data segment
X X 1 0	PCI 2nd address/data segment	X X 1 0	PCI 2nd address/data segment
0 0 0 1	Control 1st segment with PCI response	0 0 0 1	Control 1st segment with PCI response
1 0 0 1	Control 1st segment without PCI response	1 0 0 1	Control 1st segment without PCI response
0 1 0 1	Control 2nd segment with PCI response	0 1 0 1	Control 2nd segment with PCI response
1 1 0 1	Control 2nd segment without PCI response	1 1 0 1	Control 2nd segment without PCI response
0 0 1 1	Reserved	0 0 1 1	Reserved
1 0 1 1	Reserved	1 0 1 1	Reserved
0 1 1 1	Initialization	0 1 1 1	Initialization
1 1 1 1	NOOP	1 1 1 1	NOOP

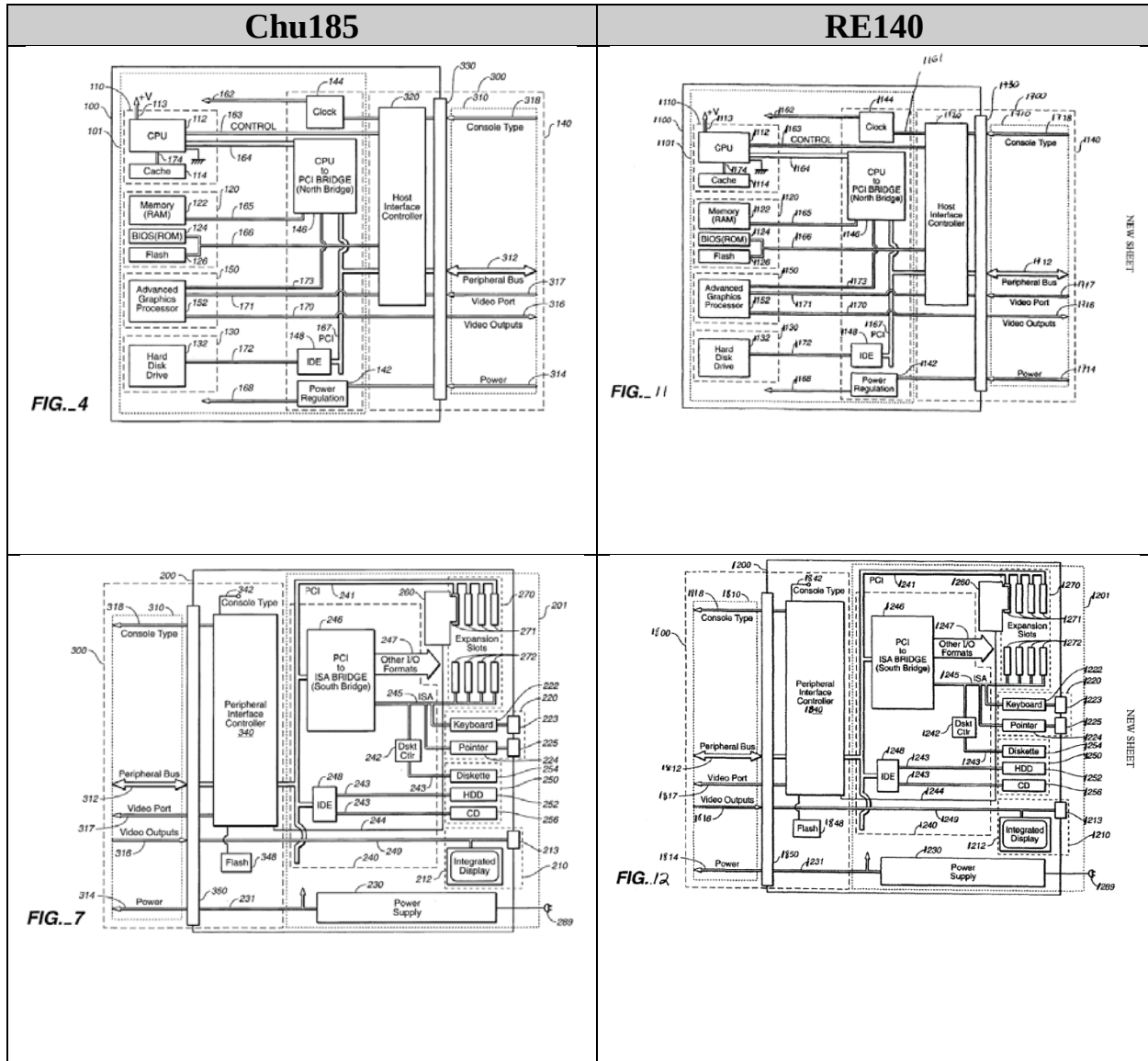
FIG. 35

ID bits (P0 P1 P2 P3)	Data Packet Type	ID bits (P0 P1 P2 P3)	Data Packet Type
X X 0 0	PCI 1st address/data segment	X X 0 0	PCI 1st address/data segment
X X 1 0	PCI 2nd address/data segment	X X 1 0	PCI 2nd address/data segment
0 0 0 1	Control 1st segment with PCI response	0 0 0 1	Control 1st segment with PCI response
1 0 0 1	Control 1st segment without PCI response	1 0 0 1	Control 1st segment without PCI response
0 1 0 1	Control 2nd segment with PCI response	0 1 0 1	Control 2nd segment with PCI response
1 1 0 1	Control 2nd segment without PCI response	1 1 0 1	Control 2nd segment without PCI response
0 0 1 1	Reserved	0 0 1 1	Reserved
1 0 1 1	Reserved	1 0 1 1	Reserved
0 1 1 1	Initialization	0 1 1 1	Initialization
1 1 1 1	NOOP	1 1 1 1	NOOP

FIG. 24

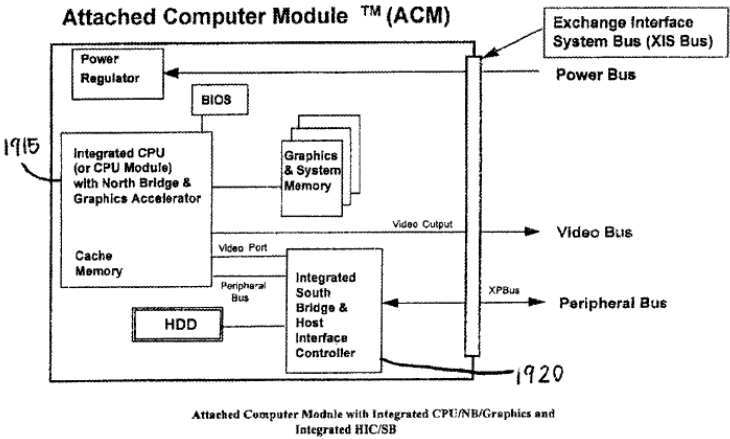
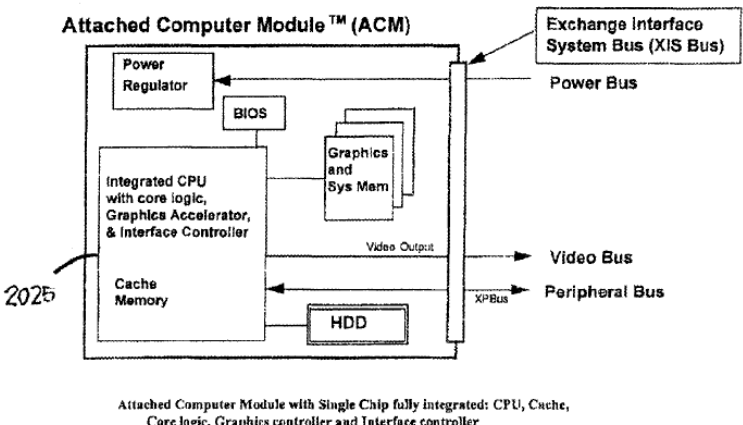
90. I also reproduce below the figures in RE140 that are identical to those found in Chu185. Again, they are identical figures, except that the numberings have been modified.





91. Moreover, RE140 includes Figures 19 and 20, as shown below. Yet, Figures 19 and 20 of RE140 are not included in Chu330 or Chu185. And while the '886 Provisional includes similar figures to Figures 19 and 20 found in RE140, neither Chu330 nor Chu185 incorporates by reference the '886 Provisional. See Ex. 1003 [Chu330] at 1:7-10; Ex. 1005 [Chu185] at 1:7-10. For that reason, while

Chu330 and Chu185 include largely identical disclosure as that of RE140 (as demonstrated above), Chu330 and Chu185 do not include Figures 19 and 20 of RE140. Figures 19 and 20 of RE140 provide the only purported support for the “integrated CPU/graphics” and “CPU-LVDS” limitations.

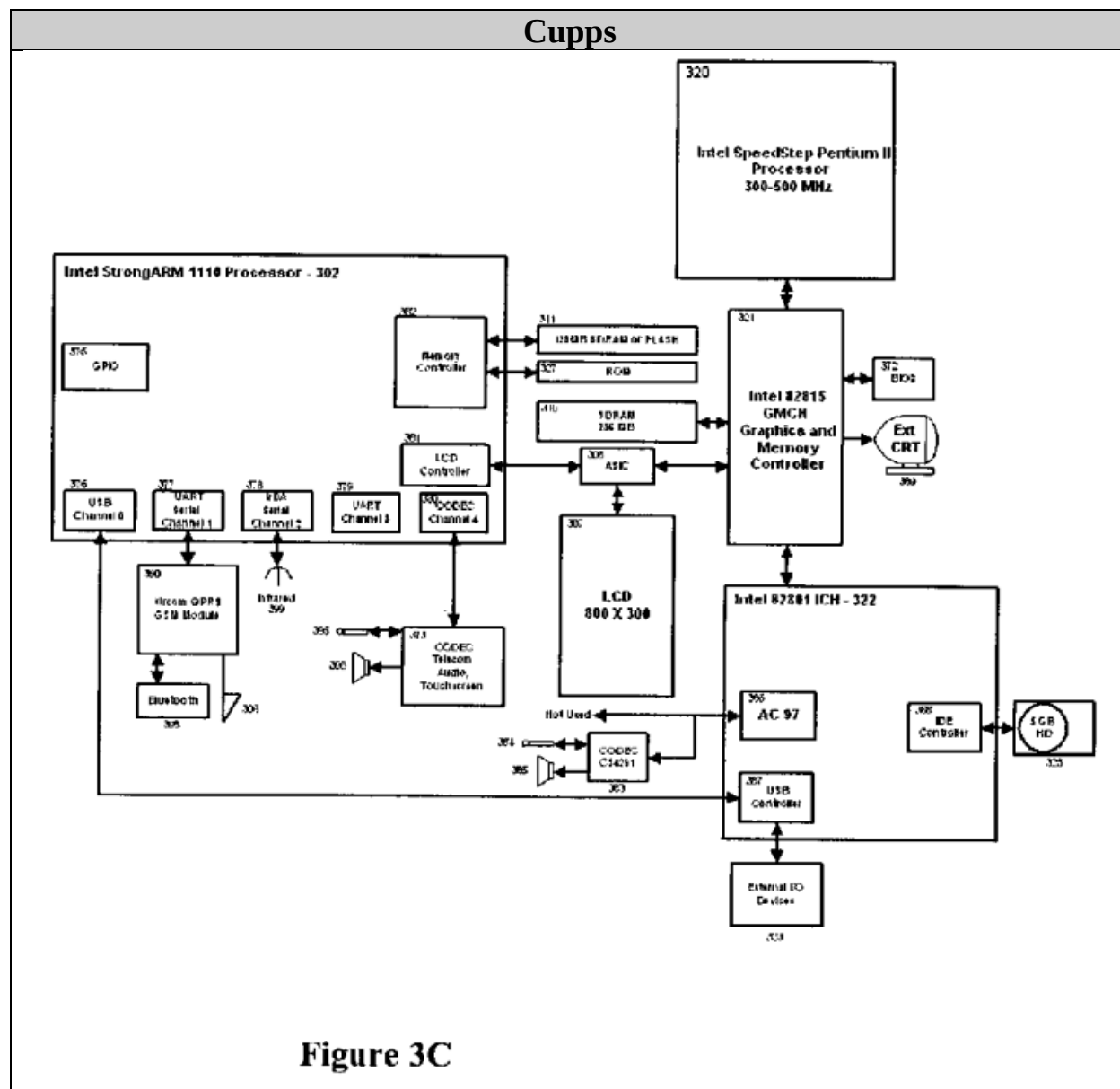
Chu330	RE140
Does not exist	 FIG. 19 The diagram shows an Attached Computer Module (ACM) with the following components and connections: Power Regulator and BIOS are connected to the Power Bus. Integrated CPU (or CPU Module) with North Bridge & Graphics Accelerator (labeled 1915) is connected to Cache Memory and Graphics & System Memory. Cache Memory is connected to the Integrated CPU and Integrated South Bridge & Host Interface Controller (labeled 1920). Graphics & System Memory is connected to the Integrated CPU and Integrated South Bridge & Host Interface Controller. Video Output is connected to the Integrated CPU and Video Bus. Video Port is connected to the Integrated CPU and Integrated South Bridge & Host Interface Controller. Peripheral Bus is connected to the Integrated South Bridge & Host Interface Controller and XPBus. HDD is connected to the Integrated South Bridge & Host Interface Controller. - The ACM is connected to an Exchange Interface System Bus (XIS Bus) via the Power Bus, Video Bus, and Peripheral Bus. Attached Computer Module with Integrated CPU/NB/Graphics and Integrated HIC/SB
Does not exist	 FIG. 20 The diagram shows an Attached Computer Module (ACM) with the following components and connections: Power Regulator and BIOS are connected to the Power Bus. Integrated CPU with core logic, Graphics Accelerator, & Interface Controller (labeled 2025) is connected to Cache Memory and Graphics and Sys Mem. Cache Memory is connected to the Integrated CPU and HDD. Graphics and Sys Mem is connected to the Integrated CPU. Video Output is connected to the Integrated CPU and Video Bus. Peripheral Bus is connected to the Integrated CPU and XPBus. HDD is connected to the Integrated CPU. - The ACM is connected to an Exchange Interface System Bus (XIS Bus) via the Power Bus, Video Bus, and Peripheral Bus. Attached Computer Module with Single Chip fully integrated: CPU, Cache, Core logic, Graphics controller and Interface controller

B. Cupps

92. Cupps was filed in February 28, 2003 and published on July 17, 2003. Each of these dates precede June 17, 2011 (the date Figures 19 and 20 were added to RE984) and September 16, 2009 (the filing date of RE984).

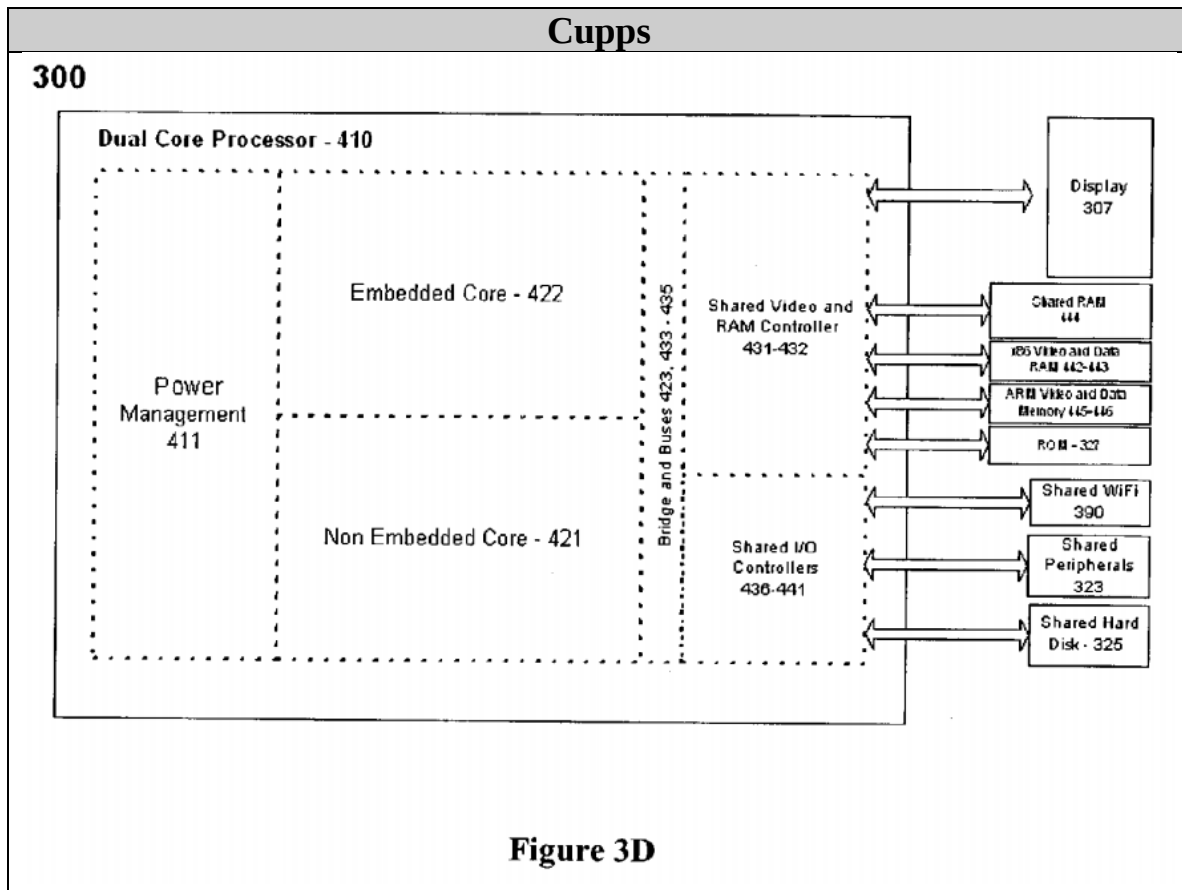
93. Cupps explains that “[c]omputers ... have taken a variety of flavors, including portable computers, which can be carried from place to place with relative convenience.” Ex. 1004 [Cupps] at [0003]. For example, two different processors can be “combined in a [single] handheld housing,” Ex. 1004 [Cupps] at [0013] or “integrated into a single integrated circuit processor.” Ex. 1004 [Cupps] at [0015].

94. Figure 3C of Cupps is an example showing two different processors that were combined in a single handheld housing. As shown, embedded processor 302 (Intel StrongARM 1110 Processor) and non-embedded processor 320 (Intel SpeedStep Pentium II Processor) are combined in a single housing. *See, e.g.*, Ex. 1004 [Cupps] at [0061] and [0215]. What is also included as part of this single handheld housing is an Intel 82815 “graphics and memory controller” that is coupled to the non-embedded processor 320. *See* Ex. 1004 [Cupps] at [0076].



95. Figure 3D of Cupps is an example where different components are “integrated into a single integrated circuit processor.” Ex. 1004 [Cupps] at [0015]. For example, a “Dual Core Processor 410 combine[s] the functionality of embedded

and non-embedded processors with controllers as shown in FIG. 3C onto one integrated circuit.” Ex. 1004 [Cupps] at [0163].



96. Cupps teaches that combining these functionalities into a single integrated circuit can lead to various improvements, such as improved power efficiency, improved performance, smaller physical footprint, and sharing of various peripherals. See Ex. 1004 [Cupps] at [0069].

VII. Level of Ordinary Skill in the Art

97. Based on my experience in the relevant art and the factors listed above in paragraph 15 [Person of Ordinary Skill in the Art], a POSITA in the field of RE140 as of its priority date would have had at least a Bachelor of Science or equivalent degree in Computer Science or Electrical Engineering and two years of graduate work, work experience, or the equivalent in computer systems, interfaces, and architecture. Further, additional education could make up for less practical experience, and vice versa.

98. I met and/or exceeded these requirements for one of ordinary skill in the art as of September 16, 2009 (the filing date of RE984)—as well as June 17, 2011 (the date Figures 19 and 20 were added to RE984).

VIII. Claim Construction

99. I have reviewed the claims, specification, and file history of RE140 and did not find any explicit definition for any particular claim terms.

100. I have been informed and understand that RE140 and patents that are related to RE140 (U.S. Patent Nos. 8,977,797, 9,529,768, and 9,703,750 and U.S. Reissued Patent Nos. 44,654) are currently subject to *inter partes* review challenges (IPR2021-00604, -00605, -00606, -00607, -00608, -00666, -00667, -00668, -00669, and -00670). I understand that the Petitioner in those petitions has proposed

construction of the claim term “peripheral bridge”. That claim term does not appear in RE140.

101. I have also been informed and understand that ACQIS LLC has asserted a number of patents that are similar to the RE140 against numerous entities.

102. I understand that certain claim terms that also appear in RE140 have been construed by the courts in those cases. Counsel has provided me with the following summary of the claim terms that appear in RE140 that have been previously construed.

Claim Term	Adopted/Agree Construction
“console”	a chassis that connects several components of the computer system
“serial bit channel”	a path on which units of information are transferred serially from one component to another
“LVDS”	a signal represented by the difference in voltage between two lines, where the difference in voltage is low
“differential signal channel”	a channel for carrying a signal, the signal being represented by the difference in voltage between two lines
“Peripheral Component Interconnect (PCI) bus”	industry standard computer bus known as Peripheral Component Interconnect Local Bus
“Peripheral Component Interconnect (PCI) bus transaction”	information/transaction, in accordance with the PCI standard, for communication with an interconnected peripheral component

	OR PCI industry standard bus transaction OR a transaction, in accordance with the industry standard PCI Local Bus Specification, for communication with an interconnected peripheral component
“encoded ... Peripheral Component Interconnect (PCI) bus transaction”	code representing a PCI bus transaction
“encoded ... serial bit stream of Peripheral Component (PCI) bus transaction” ²	a PCI bus transaction that has been serialized from a parallel form

103. Because Chu330 and Chu185 provide nearly the identical disclosure as RE140 for these claim terms, these claim terms are taught by Chu330 and Chu185.

104. I have also analyzed the remaining claim terms in claims 14-38 of RE140 and believe that the ordinary and customary meaning of the terms should be applied, and I have done so in the analysis that follows.

² I understand that other related claim terms that discuss PCI bus transaction that have been serialized, or transmitted in serial form, or transmitted over serial bit channels were similarly construed.

IX. Specific Grounds for Challenge

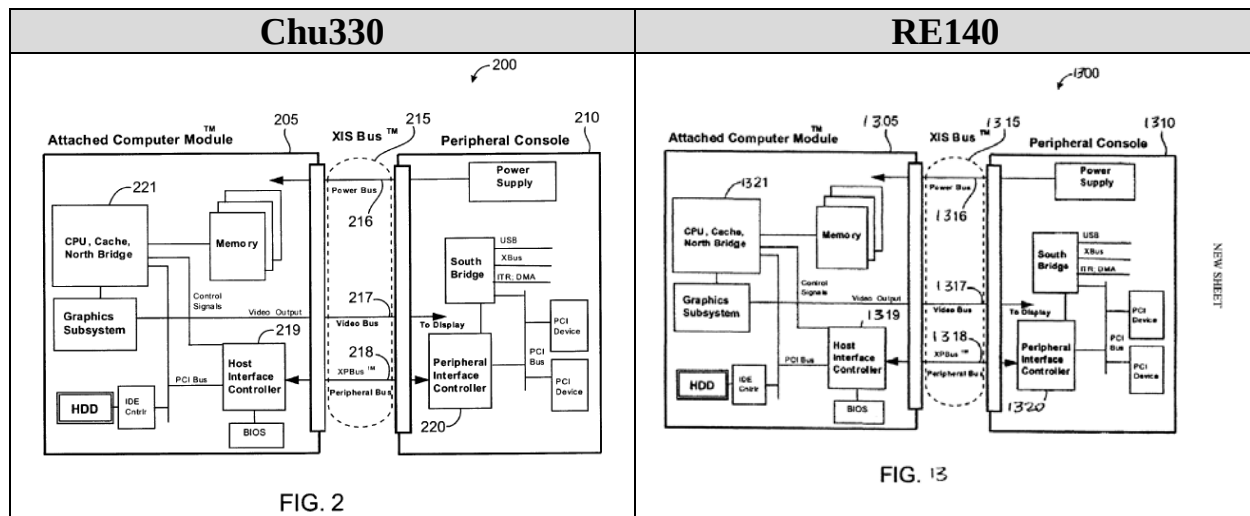
A. Ground I: Chu330 in combination with Cupps Render Obvious Claims 14-38

1. Claim 14

105. As explained in greater detail below, Chu330 in combination with Cupps renders obvious claim 14.

i. [14pre] A method of improving performance of a computer, comprising:

106. Chu330 teaches a “computer,” for example, in Figure 2 of Chu330.



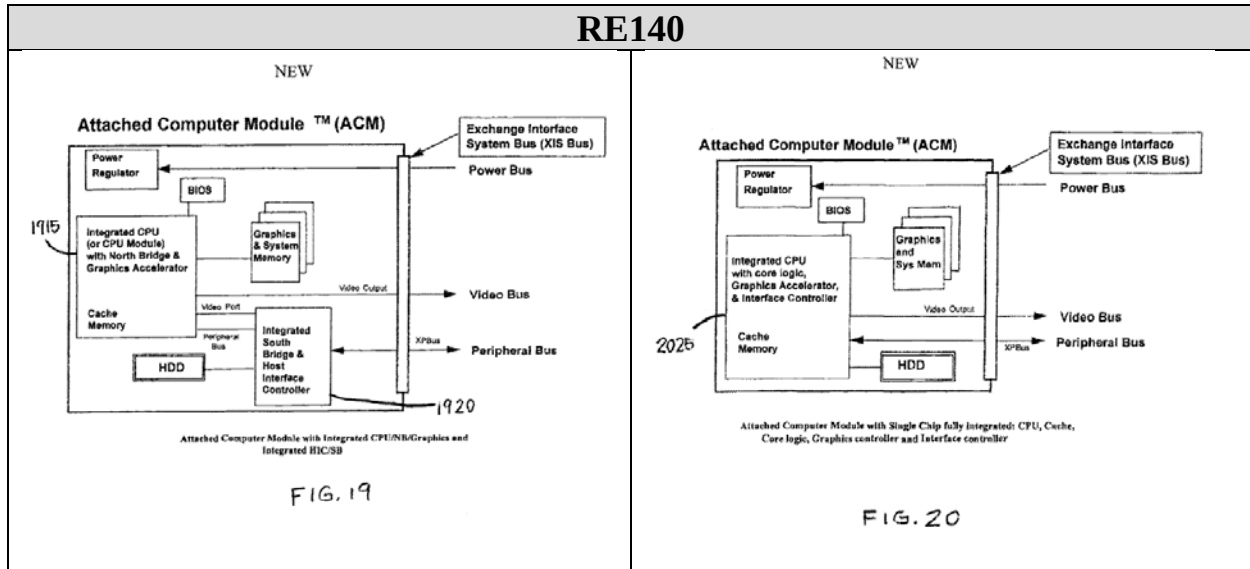
107. “FIG. 2 is a block diagram of one embodiment of a computer system 200 using the interface of the present invention. Computer system 200 includes an attached **computer** module (ACM) 205 and a peripheral console 210...” Ex. 1003 [Chu330] at 5:66-6:2; see also 3:45-47, 6:26-35.

108. Specifically, the attached **computer** module (ACM) 205 in Figure 2 teaches the computer recited in the preamble.

109. Additionally, Chu330 teaches a method of improving the performance of the computer. For example, Chu330 teaches improving computer performance by relying on an “LVDS channel [that is] more cable friendly, faster, consumes less power, and generates less noise, including electromagnetic interferences (EMI), than a PCI channel.” Ex. 1003 [Chu330] at 2:10-15. Additionally, Chu185 explains additional improvements to the computer in that “[t]he core computing power may also include high performance devices 150 such as advanced graphic processor chips that greatly increase overall system performance and which, because of their speed, need to be located close to the CPU.” Ex. 1005 [Chu185] at 4:50-54; *see also* Ex-1004 [0069] (describing “increased performance” as an improvement that results from integration).

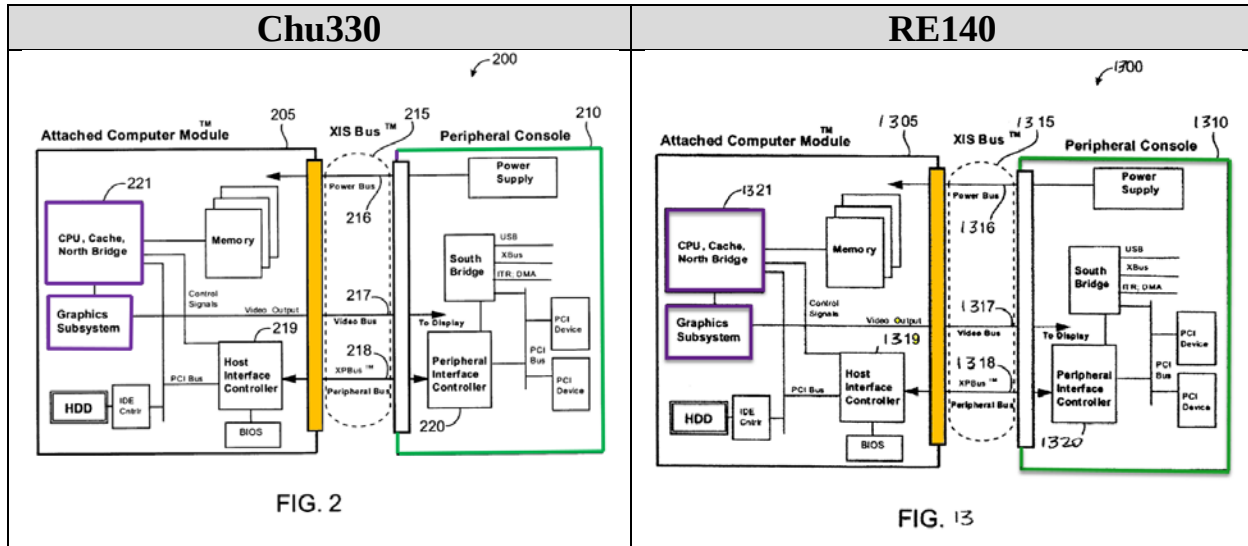
ii. [14a] obtaining an integrated Central Processing Unit (CPU) with a graphics controller in a single chip;

110. At the outset, in my opinion, Figures 19-20 of RE140 are the only disclosure in RE140 that provides support for this limitation. Figures 19 and 20 show the “Integrated CPU with ... Graphics Accelerator” 1915 and “Integrated CPU ... [with] Graphics Accelerator” 2025.

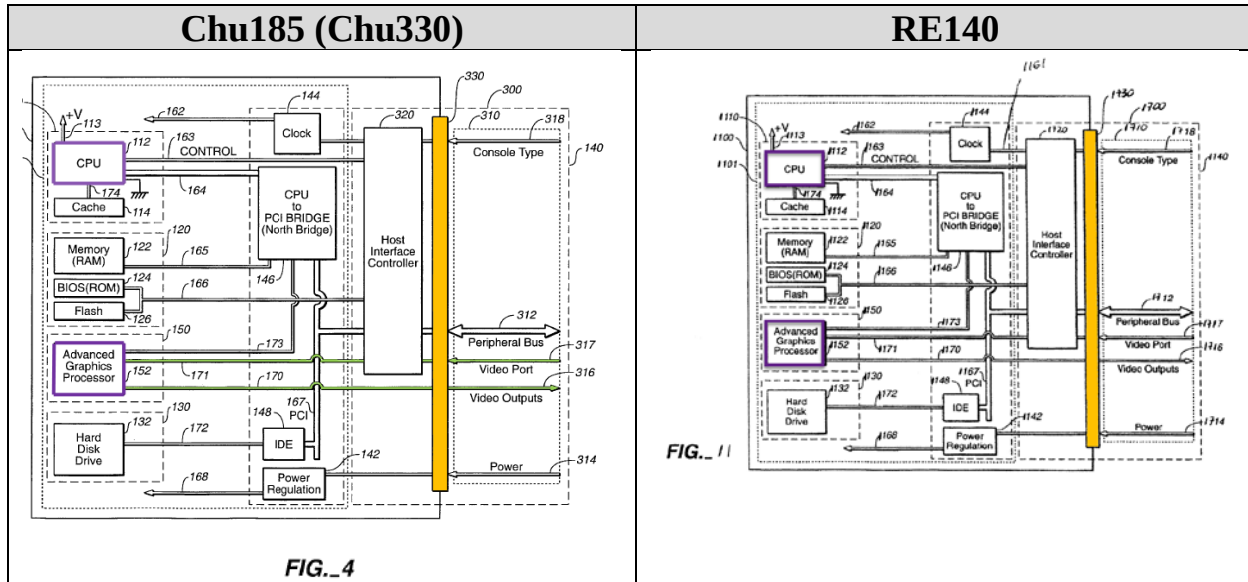


111. Chu330 in combination with Cupps renders this limitation obvious in the same manner.

112. Chu330 shows a “CPU,” a “graphics subsystem,” and a “host interface controller (HIC)” in the ACM of Figure 2. See Ex. 1003 [Chu330] at 5:66-6:35. Additionally, Chu330 also refers to the “graphics subsystem” depicted in Figure 2 as a “graphics controller.” See Ex. 1003 [Chu330] at claims 2, 3, 6; 10:6, Figures 6 and 25. As shown, the XPBus is coupled to the CPU via the HIC. This is also the case in Figure 13 of RE140.



113. Chu185 also shows an “**Advanced Graphics Processor (AGP) 152**” as a “**graphics subsystem**” in Figure 4. Chu330 teaches that the “**Advanced Graphics Processor (AGP) 152**” can be “**Model 740 Graphics Device from Intel Corporation.**” Additionally, as is seen in U.S. Patent No. 6,621,760 (“’760 Patent”), **graphics accelerators** and **graphics processors** may also be referred to as “**graphics controllers.**” Ex. 1017 [’760 Patent] at 1:16-21 (“Currently, **graphics controllers/accelerators** such as the **Intel 740** support A typical **graphics controller** such as the **Intel 740**....”).



114. Obtaining an integrated “CPU,” a “graphics subsystem,” and a “host interface controller (HIC)” in a single chip, where the XPBus is directly coupled to the integrated CPU, would have been obvious by the priority date of RE140.

115. As one example, Cupps teaches that it was well-known to integrate such components together and the benefits of doing so. I reproduce below Figure 3C of Cupps (where I overlaid the text corresponding to a few components because the original text was not clear). I highlight in Figure 3C the **Intel Speedstep Pentium Processor 320**, **Intel 82815 Graphics and Memory Controller Hub (GMCH) 321**, and **Intel 82801 integrated controller hub (ICH) device 322**. Ex. 1004 [Cupps] at [0086] (“Operating with processor 320 are memory and graphics controller 321, such as Intel 82815 graphics memory controller hub (GMCH)

116. Figure 3D of Cupps discloses an “integrated circuit 410 utilizing two processor cores” that “**combine[s]** the functionality of embedded and non-embedded **processors with controllers** as shown in FIG. 3C.” Ex. 1004 [Cupps] at [0163]. Specifically, in Figure 3D, device 300 with a single die (Dual Core Processor 410) having **core 421, shared video and RAM controller 431-432, and shared I/O controllers 436-441** is shown. Ex. 1004 [Cupps] at [0068] (“The Dual Core Processor 410 combines the functionality of embedded and non-embedded processors with controllers onto one integrated circuit”), [0163] (“an integrated circuit 410 utilizing two processor cores 421 and 422 and controllers 431, 432, 436-441 could be used, as shown in FIGS. 3D and 3E. The purpose of the Dual Core Processor 410 is to combine the functionality of embedded and non-embedded processors with controllers as shown in FIG. 3C onto one integrated circuit as shown in FIGS. 3D and 3E.”). In other words, the functionalities associated with the **processor 320, GMCH 321, and ICH 322** are integrated together onto a single die in Figure 3D.

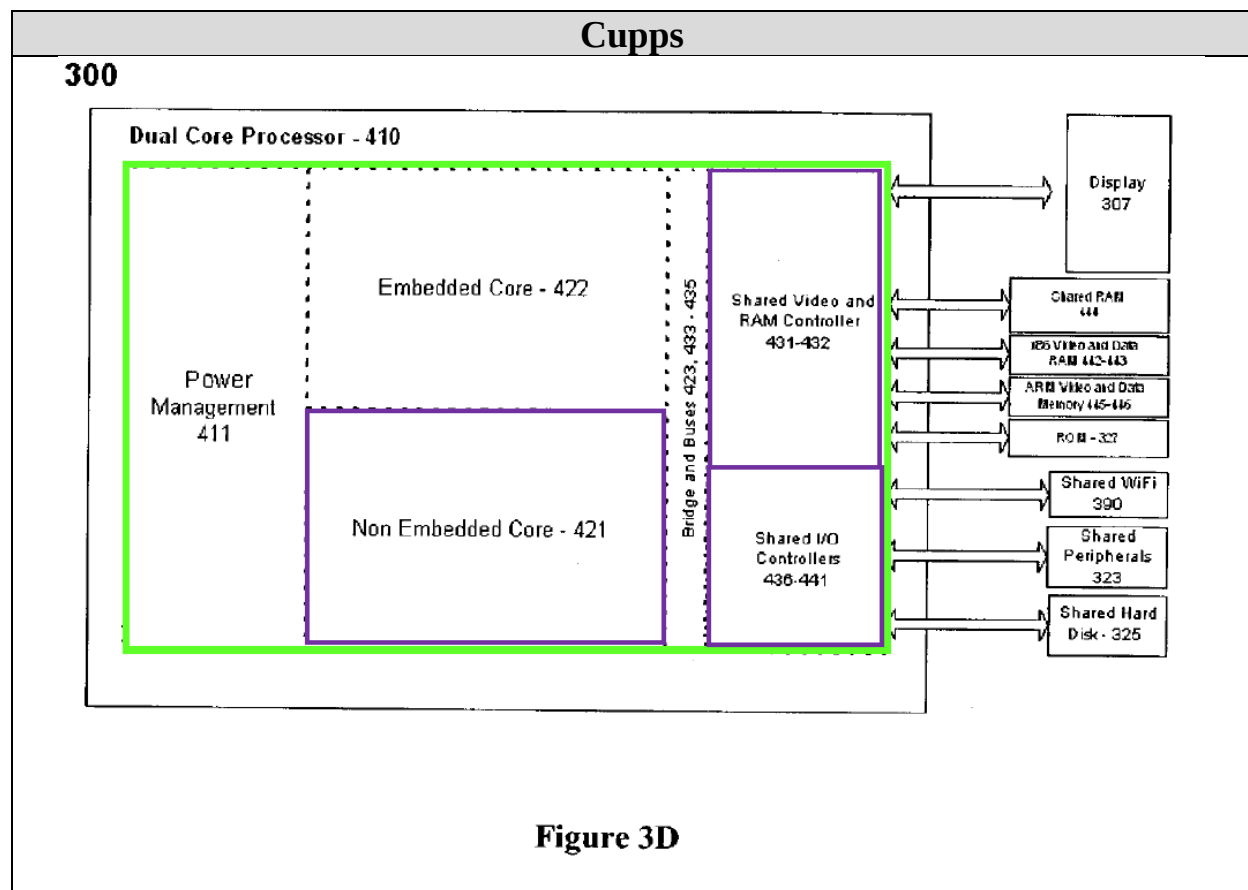
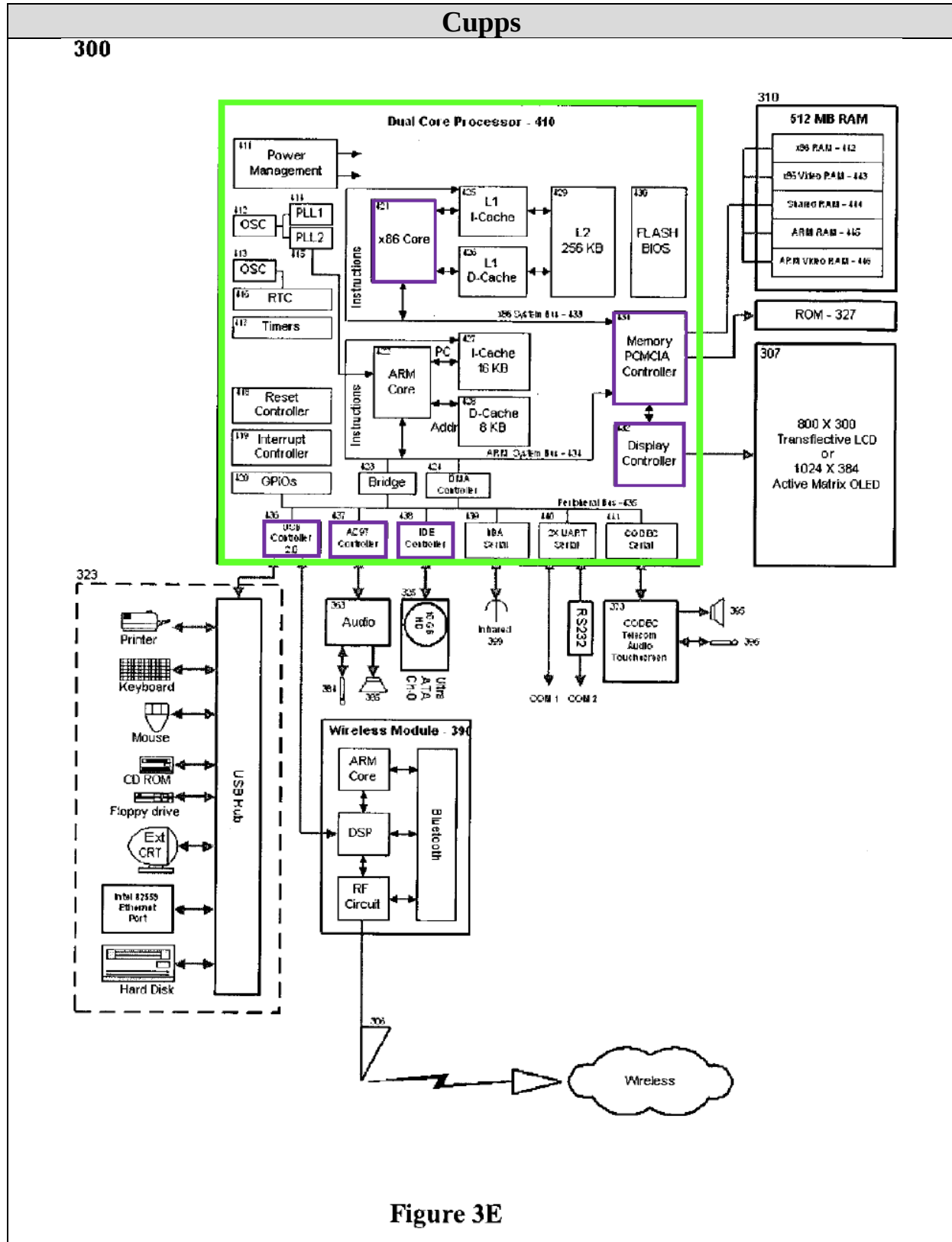
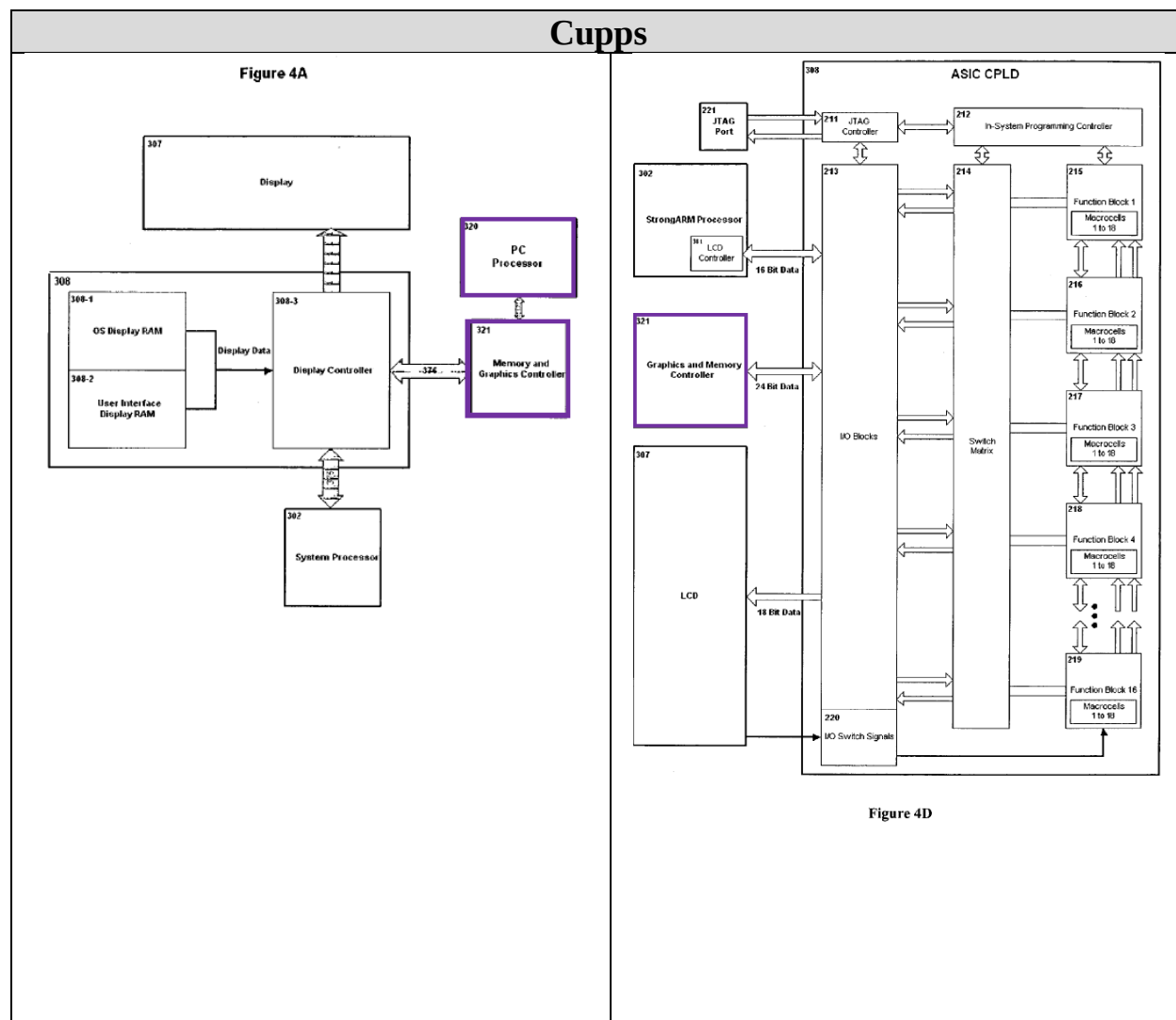


Figure 3D

117. Figure 3E shows another example of the device 300 with the dual core processor 410, where **x86 (non-embedded) core 421** and the **memory PCMCIA and display controllers 431 and 432** (along with other controllers, such as **USB controller 436, AC97 controller 437, IDE controller 438**, etc.) are integrated together onto **a single die**. See Ex. 1004 [Cupps] at [0068].



118. Cupps explains that the device 300 runs with a display controller “Pentium III processor [that] is driven by its ancillary **82815 Graphics Memory and Controller Hub (GMCH) chip.**” Ex. 1004 [Cupps] at [0108]. In other words, although the GMCH 321 is not explicitly shown in Figures 3D and 3E, Cupps makes clear that this functionality is included. This is further supported by Figures 4A and 4D, which shows the processor 320 displaying data on LCD 307 utilizing both the graphics controller 321 and the display controller 308. *See* Ex. 1004 [Cupps] at [0109]-[0110], [0114] (“The **Graphics Memory Controller, FIG. 4D, 321 and FIG. 3C, 321**, then sends the output display data in a 24 bit format, and is passed through the ASIC I/O ... At this point, the user is now seeing a representation of a PC desktop, FIG. 4E, on the LCD, FIG. 3C, 307, and FIG. 4D, 307.”), [0164] (“The logic ... referenced in FIGS. 3C and 4D, would become part the integrated circuit for the **display and memory controller 431 and 432** of the **Dual Core Processor 410.**”).



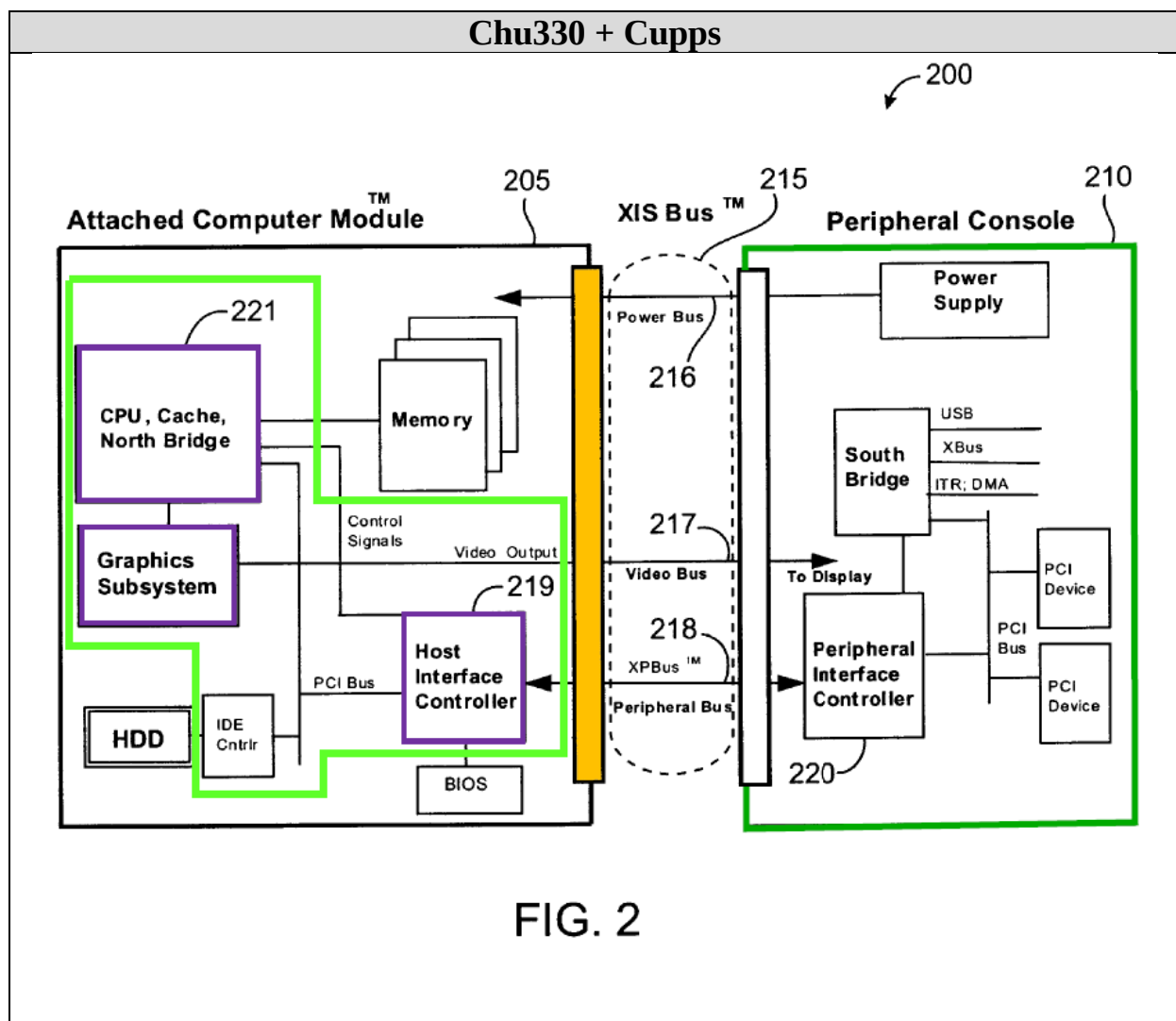
119. Cupps teaches the benefits of integrating these different functionalities into a single device, citing such benefits as improved power efficiency, improved performance, and smaller size. See Ex.1004 [Cupps] at [0015] (“Since they are commonly integrated in one processor integrated circuit, they share some components and reduce the overall device chip count... thereby improving the efficiency and power conservation of the device.”), [0069] (“The benefits of this

embodiment include (a) no power management redundancy; (b) no controller redundancy; (c) the processor cores share memory; (d) improved thermal management; (e) improved power efficiency; (f) increased performance; (g) smaller physical footprint; (h) sharing the display; (i) sharing peripherals; and (j) sharing the hard disk. Other benefits may be apparent to those skilled in the art. One of the reasons for these benefits are that many of the components normally found as redundant functionality in FIGS. 3B and 3C of the Novel Personal Electronic Device **300**, now are shown as an integrated circuit **410** in FIGS. 3D and 3E.”).

120. These types of benefits are exactly the type of benefits that Chu330 was considering as well. *See* Ex. 1003 [Chu330] at 2:10-15 (“It is desirable to use a low voltage differential signal (LVDS) channel in the computer system of the present invention because an LVDS channel is more cable friendly, faster, consumes less power.”).

121. The combination is simply integrating Chu330’s **CPU, graphics subsystem**, and **HIC in a single chip** just like Cupps taught to achieve the well-recognized benefits. The combination merely integrates Chu330’s **CPU, graphics subsystem**, and **HIC in a single chip** in the manner taught by Cupps to achieve the expected benefits of lower power consumption and less redundancy. A

POSITA would have had a reasonable expectation of success in achieving the modification.

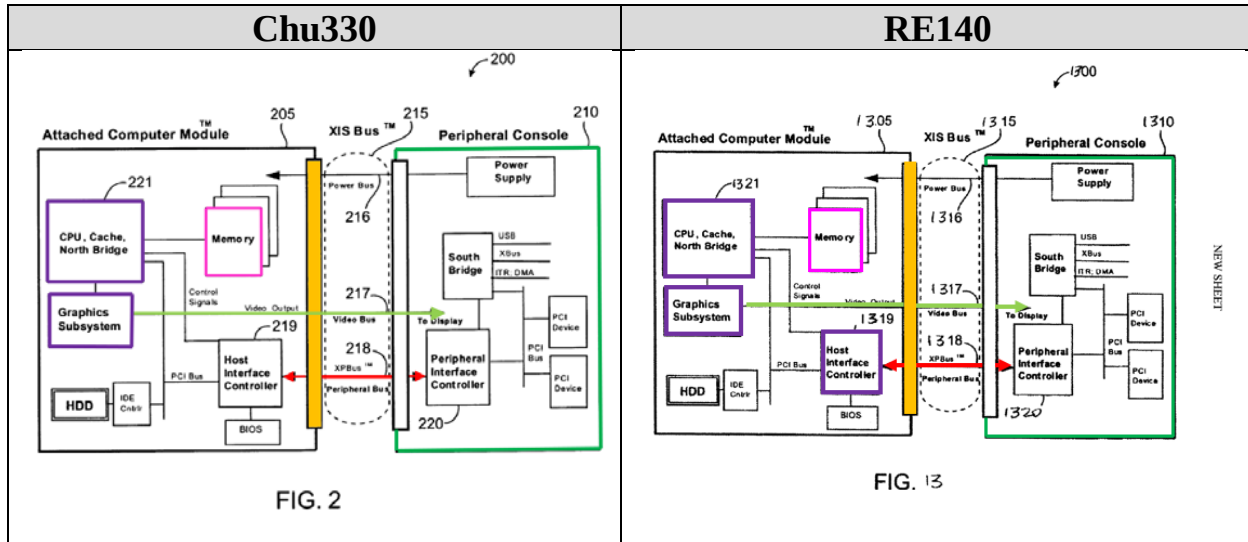


122. It simply uses known techniques to improve explicitly taught by the references in basically the same way that Cupps describes. Chu330's CPU 221 functions just like Cupps' processor 320/421, Chu330's graphic subsystem

functions just like Cupp's graphics controller 321/431-432, and Chu330's host interface controller 219 functions just like Cupps' I/O controller 322/436-441. Integrating these components in the manner taught by Cupps would have been obvious to a POSITA, with the expectation that the benefits discussed by Cupps would have been recognized.

iii. [14b] connecting a **Differential Signal channel** directly to the **integrated CPU and graphics controller** to output **video data**;

123. Figure 2 of Chu330 shows a video bus 217 that indicates a video is output from the **graphics subsystem** over to a "display." In my opinion, Chu330 treats **graphics controller** similarly to a **graphics subsystem** because Chu330 claims sending "a **video display signal** from the **graphics controller** to a display." Ex. 1003 [Chu330] at claims 2, 3 ("video display signal from the graphics controller to a display"), 6, 10:6, Figures 6 and 25.



124. Chu330 further teaches that “the video bus 217 transmits ... **digital video signals** (such as ... **Transition Minimized Differential Signaling (TMDS) signals** for flat panel displays).” Ex. 1003 [Chu330] at 6:15-22. The **TMDS signals** are transmitted over differential signal channels. For example, Figures 28 and 30 show a differential pair of physical lines (i.e., **D0+** and **D0-**) which sends TMDS signals. Ex. 1003 [Chu330] at 17:42-67, Figures 28 and 30; *see also* Ex. 1003 [Chu330] at 13:38-14:1, 15:57-67 (“The term line, when not directly preceded by the terms physical or conductive, is herein used interchangeably with a signal or bit channel which may consist of one or more physical lines for transmitting a signal.”), Figure 17 and 19 (including pins E15-E16). Additionally, **D0+** and **D0-** present Data 0 + and Data 0 -, and for that reason correspond to video data being sent on these line. Ex. 1003 [Chu330], Figure 30.

Chu330

ACM s CMI BUS Connector Plug PIN Position (88 pin):

E14	GND	GND	E1	P23	GND	GND	P1
E15	P&D D0 +	TPA+ /VPD+	E2	P24	PD0 +	PDR0 +	P2
E16	P&D D0 -	TPA- /VPD-	E3	P25	PD0 -	PDR0 -	P3
E17	GND	GND	E4	P26	GND	GND	P4
E18	P&D CLK +	TPB+ /VPCK+	E5	P27	PD1 +	PDR1 +	P5
E19	P&D CLK -	TPB- /VPCK-	E6	P28	PD1 -	PDR1 -	P6
E20	GND	1394 Detect	E7	P29	GND	GND	P7
E21	P&D D1 +	Reserved	E8	P30	PD2 +	PDR2 +	P8
E22	P&D D1 -	Reserved	E9	P31	PD2 -	PDR2 -	P9
E23	GND	Reserved	E10	P32	GND	GND	P10
E24	P&D D2 +	Reserved	E11	P33	PCK +	PCKR +	P11
E25	P&D D2 -	Reserved	E12	P34	PCK -	PCKR -	P12
E26	DFP Detect	Config 2	E13	P35	Config 1	Config 0	P13

V10	GND	V33	V1	P36	GND	GND	P14
V11	GND	V33	V2	P37	PD3 +	PDR3 +	P15
V12	GND	V33	V3	P38	PD3 -	PDR3 -	P16
V13	V33	V33	V4	P39	RSTEP#	RSTEP#	P17
V14	V33	V33	V5	P40	GREEN VIDEO	RED VIDEO	P18
V15	V33	V33	V6	P41	GND	GND	P19
V16	V5	V12	V7	P42	HSYNC	BLUE VIDEO	P20
V17	V5	V12	V8	P43	VSING	GND	P21
V18	V5	V12	V9	P44	DDC2: SCL	DDC2: SDA	P22

FIG. 28

RE140

Not disclosed

Pin No.	Symbol	Signal	Standard	Description
E2	VPD+/TPA+		LVDS or 1394	Video capture port data or 1394
E3	VPD-/TPA-		LVDS or 1394	Video capture port data or 1394
E5	VPCK+/TPA+		LVDS or 1394	Video capture port data or 1394
E6	VPCK-/TPA-		LVDS or 1394	Video capture port data or 1394
E15	D0 +	TMDS	VESA P & D	Data 0 +
E16	D0 -	TMDS	VESA P & D	Data 0 -
E18	CLK +	TMDS	VESA P & D	Clock +
E19	CLK -	TMDS	VESA P & D	Clock -
E21	D1 +	TMDS	VESA P & D	Data 1 +
E22	D1 -	TMDS	VESA P & D	Data 1 -
E24	D2 +	TMDS	VESA P & D	Data 2 +
E25	D2 -	TMDS	VESA P & D	Data 2 -
E13	Config 2			Configuration bit 2
E26	Config 3			Configuration bit 3
E1, E4, E14, E17, E20, E23	GND		GND	Ground

E7	Reserved			Reserved
E8	Reserved			Reserved
E9	Reserved			Reserved
E10	TV-CV/Reserved		NTSC	TV Composite Video or reserved
E11	SV Y/Reserved		Super Video	SV Luminance or reserved
E12	SV C/Reserved		Super Video	SV Chrominance or reserved

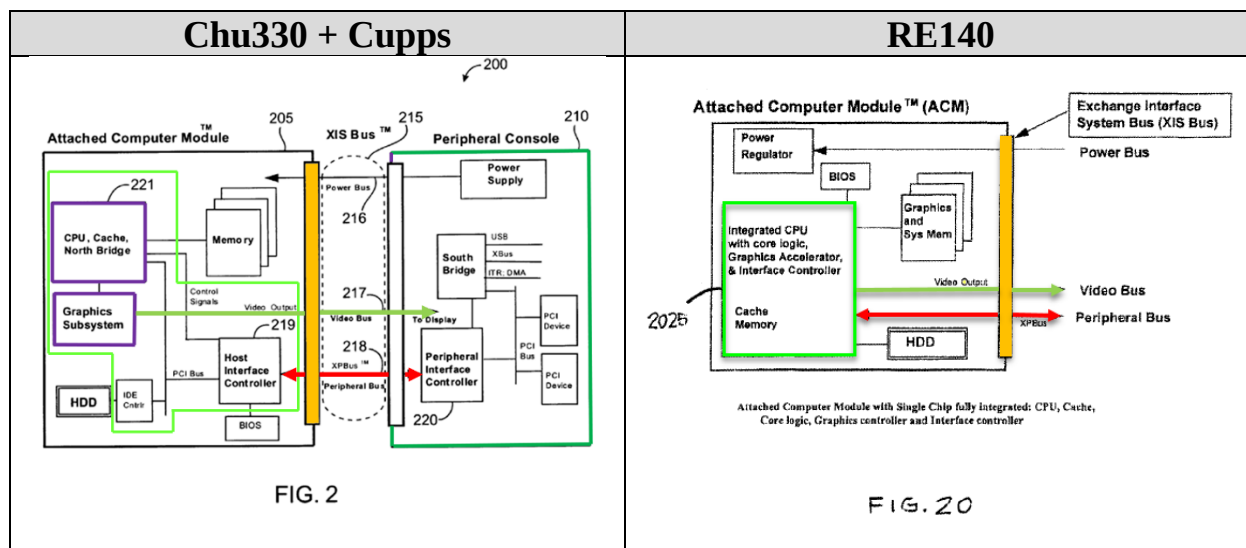
FIG. 30

Pin No.	Symbol	Signal	Standard	Description
V2	Red Video	Analog		Video
V4	Green Video	Analog		Video
V6	Blue Video	Analog		Video
V8	HSYNC			Horizontal Sync
V9	VSING			Vertical Sync
V11	DDC2: SCL		VESA DDC std 2	DDC Clock
V12	DDC2: SDA		VESA DDC std 2	DDC Data
V14	TV-CV/CNTL 0			TV Composite Video
V15	SV Y/CNTL 1		Super Video	SV Luminance or Control 1
V16	SV C/CNTL 2		Super Video	SV Chrominance or Control 2
V24	D0 +	TMDS	VESA P & D	Data 0 +
V25	D0 -	TMDS	VESA P & D	Data 0 -
V27	CLK +	TMDS	VESA P & D	Clock +
V28	CLK -	TMDS	VESA P & D	Clock -
V30	D1 +	TMDS	VESA P & D	Data 1 +
V31	D1 -	TMDS	VESA P & D	Data 1 -
V33	D2 +	TMDS	VESA P & D	Data 2 +
V34	D2 -	TMDS	VESA P & D	Data 2 -
V37	VPCK +	LVDS		Video Port Pixel Clock +
V38	VPCK -	LVDS		Video Port Pixel Clock -
V40	VPD +	LVDS		Video Port Pixel Data +
V41	VPD -	LVDS		Video Port Pixel Data -
V13	Config 2		3.3v or GND	Configuration bit 2
V35	Config 3		3.3v or GND	Configuration bit 3
V1, V3, V5, V7, V10, V23, V26, V29, V32, V36, V39, V42, V43, V44	GND		GND	Ground

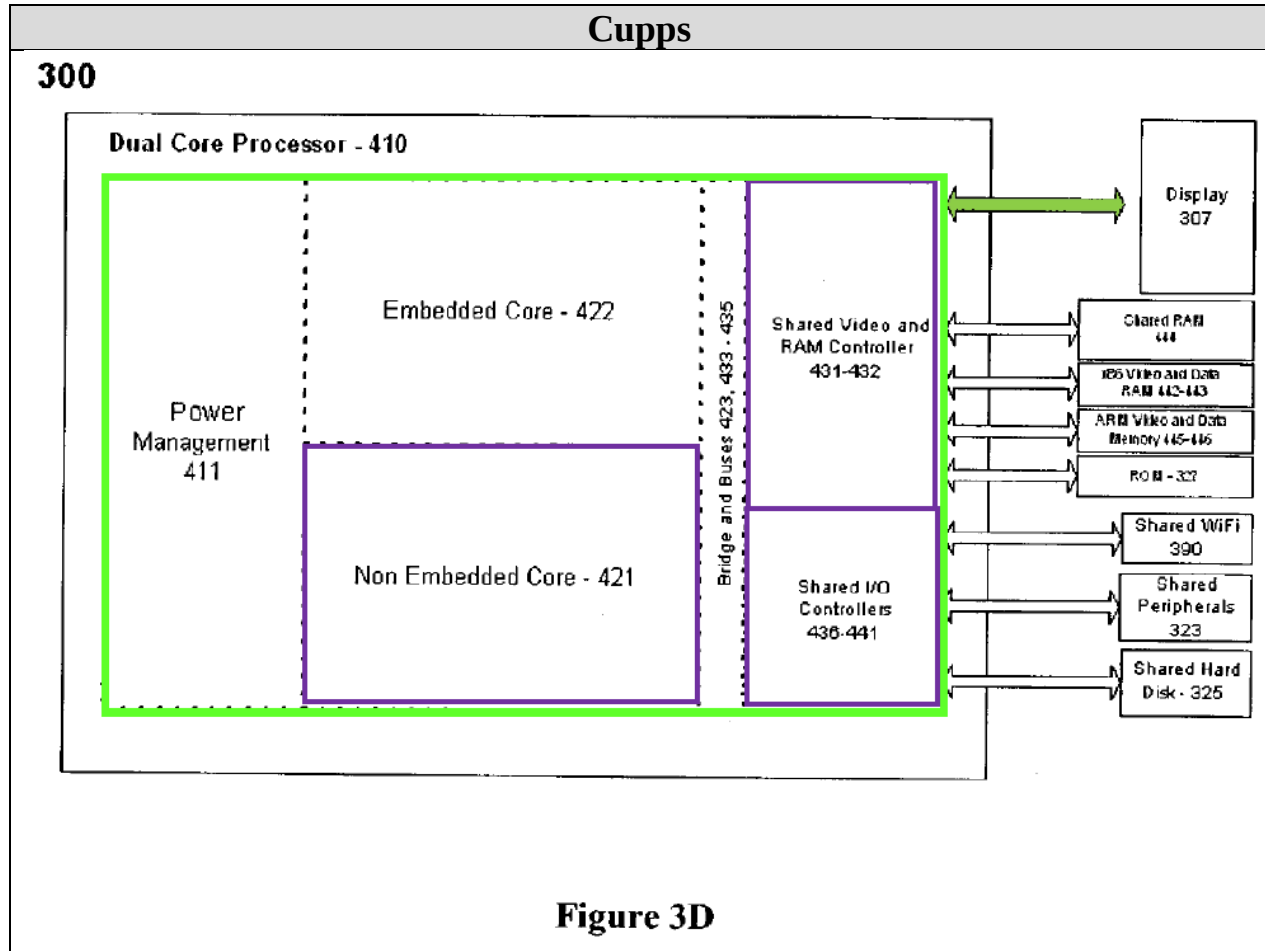
FIG. 22

(Corresponding to Figure 19 of Chu330)

125. Therefore, for the similar reasons as I explained in [limitation 14a], Chu330 in combination with Cupps renders obvious “an **integrated Central Processing Unit (CPU) with a graphics controller in a single chip**” and the **integrated CPU and graphics controller** is also directly connected to the **differential signal channel** to output **video data**.



126. This is similarly taught in Cupps, as shown in Figure 3D below. As shown, the integrated Dual Core Processor 410 outputs video display signals to a display 307.

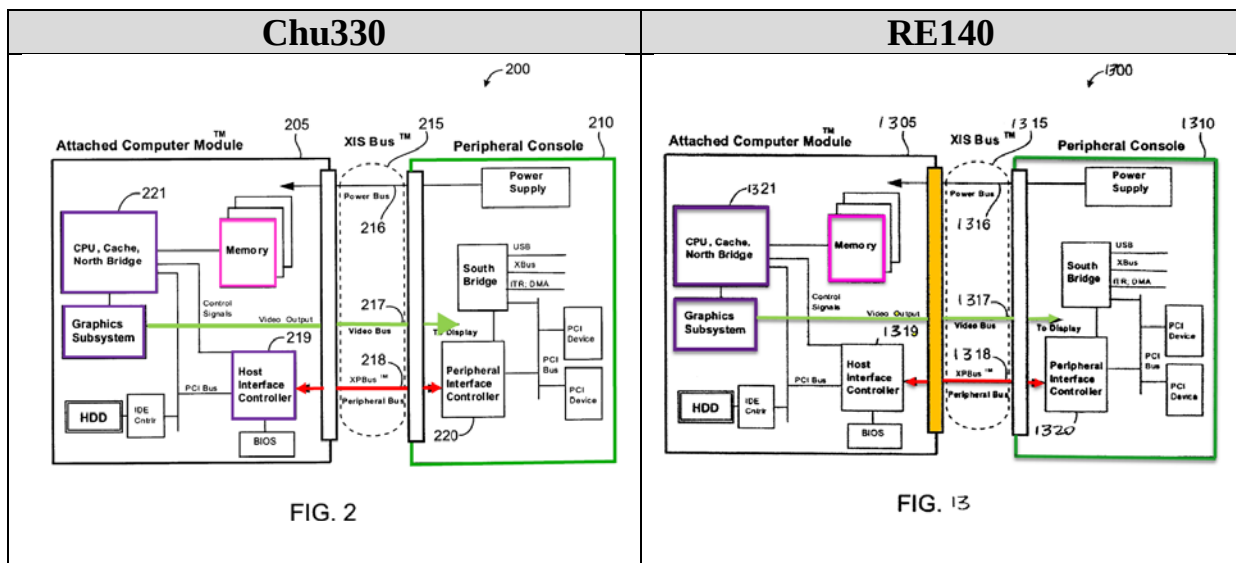


- iv. [14c] conveying Transition Minimized Differential Signaling (TDMS) [sic] signals through the **Differential Signal channel**;

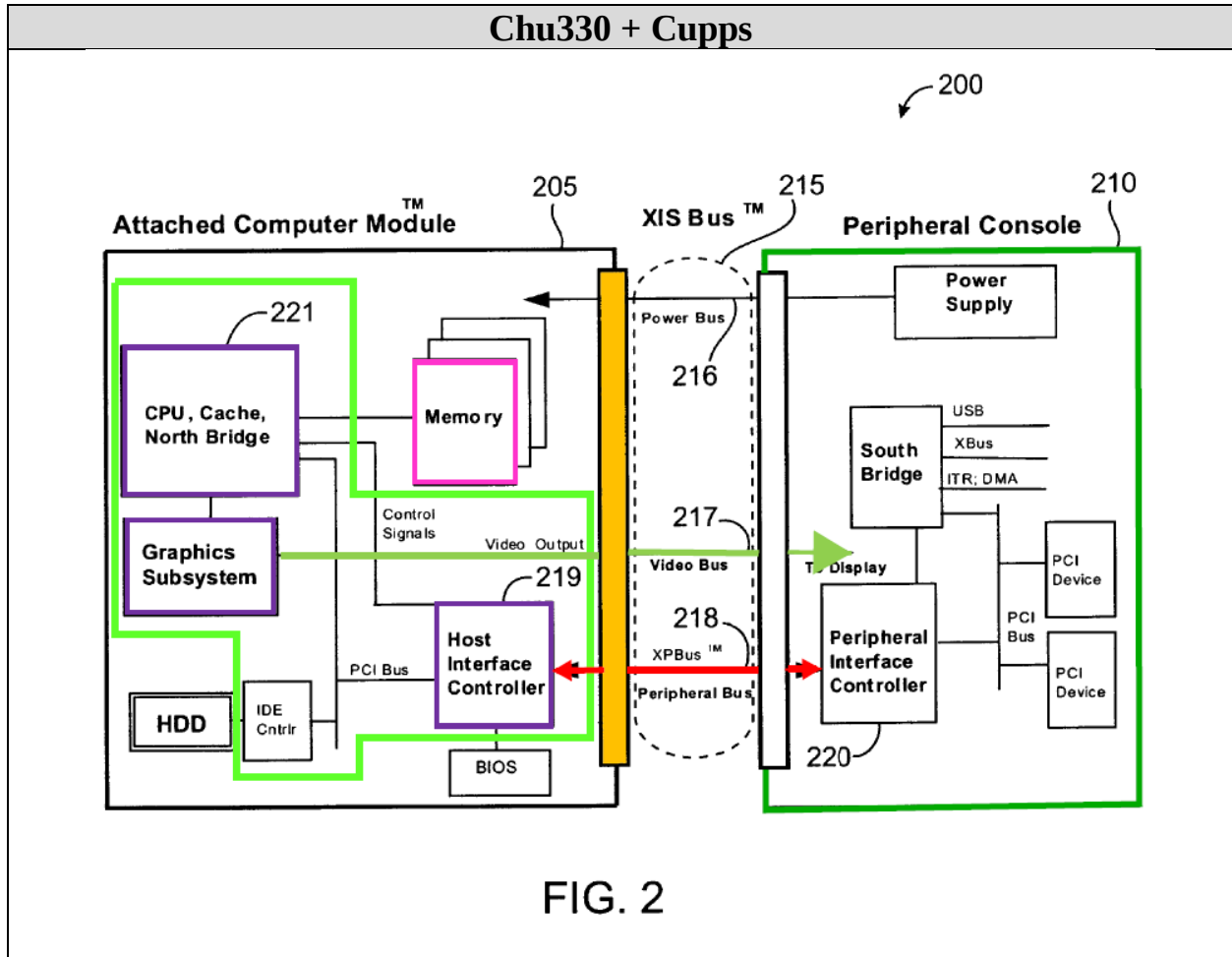
127. I explained above in [limitation 14b] how Chu330 teaches this limitation.

v. [14d] connecting **memory** directly to the **integrated CPU and graphics controller**,

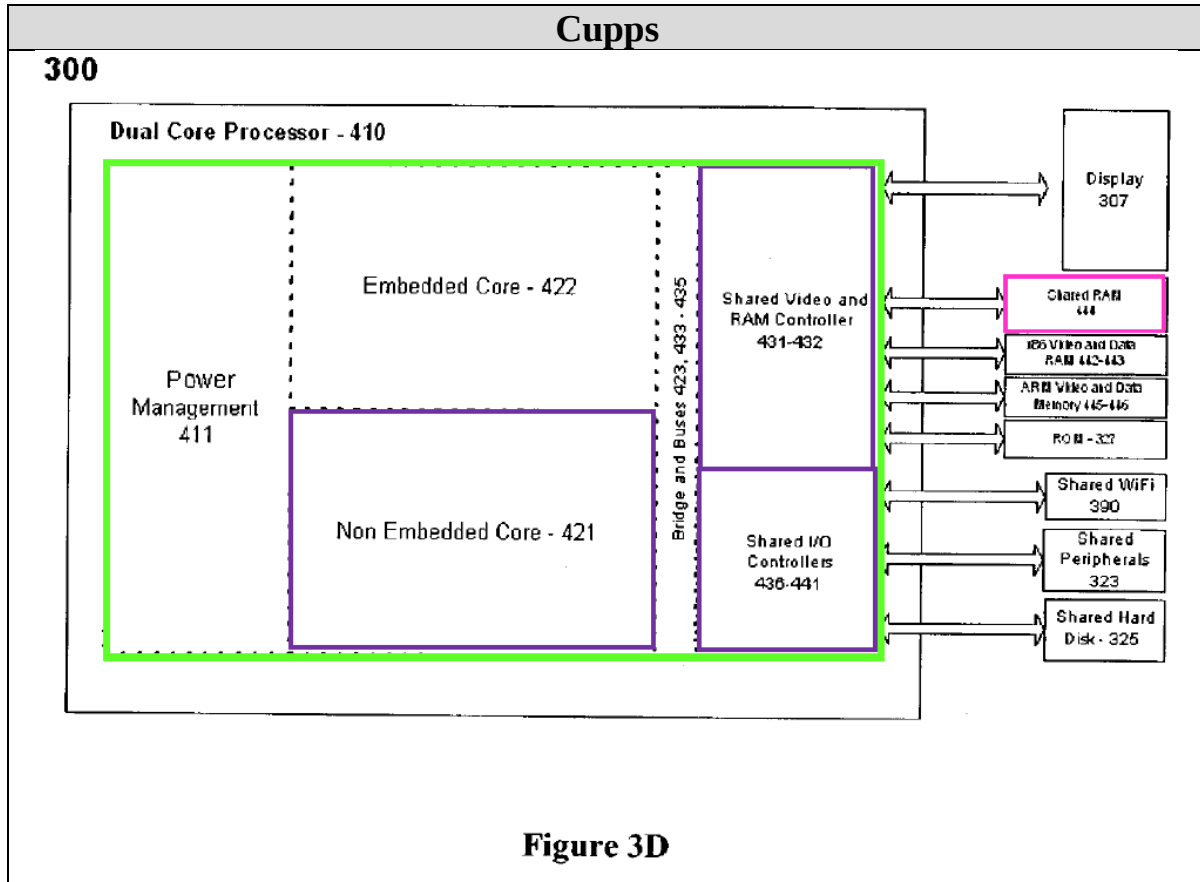
128. Chu330 in Figure 2 shows a **memory** directly connected to a “**CPU**, Cache, North Bridge” (which includes the **CPU**). Ex. 1003 [Chu330] at Figure 2, Claim 1 (teaching “including a **central processing unit** and a **main memory**”).



129. The integration of Chu330’s CPU and graphics subsystem, as discussed above with limitation [14a], then also naturally leads to the **memory** being directly connected to the **integrated CPU and graphics controller**.



130. This is actually shown in both Figures 3D and 3E of Cupps. As shown, the memory (e.g., RAM 310, 444)—which Cupps says “may serve as the main memory”—is directly coupled to the **processor 410** as shown in Figures 3D and 3E. See, e.g., Ex-1004, [0076] (“SDRAM 310 may serve as the main **memory** for devices 302 and 320 for use by computer programs running on their respective operating systems.”), [0081], [0084], [0173]. As such, Chu330 as modified by the teachings of Cupps renders obvious this limitation.



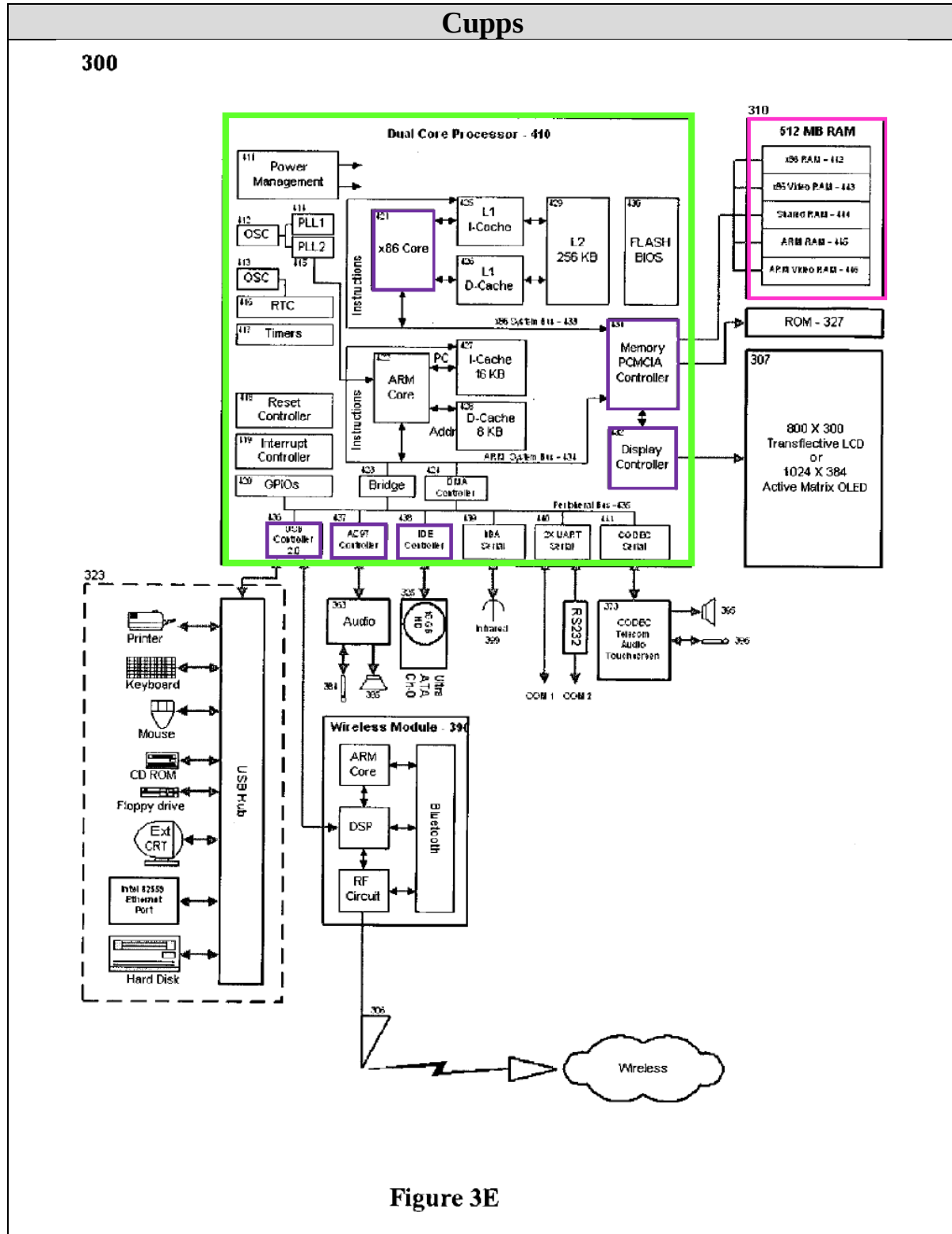
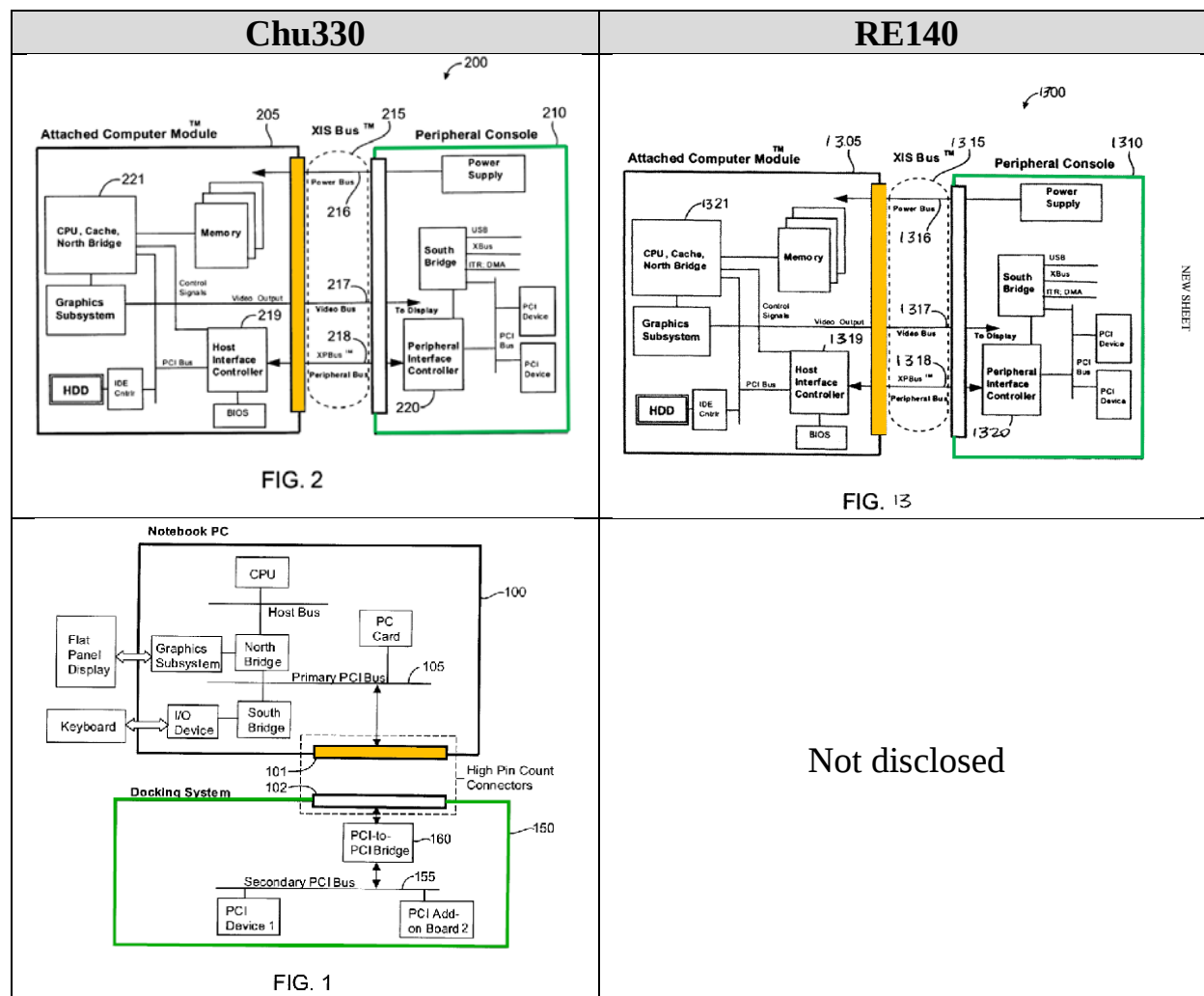


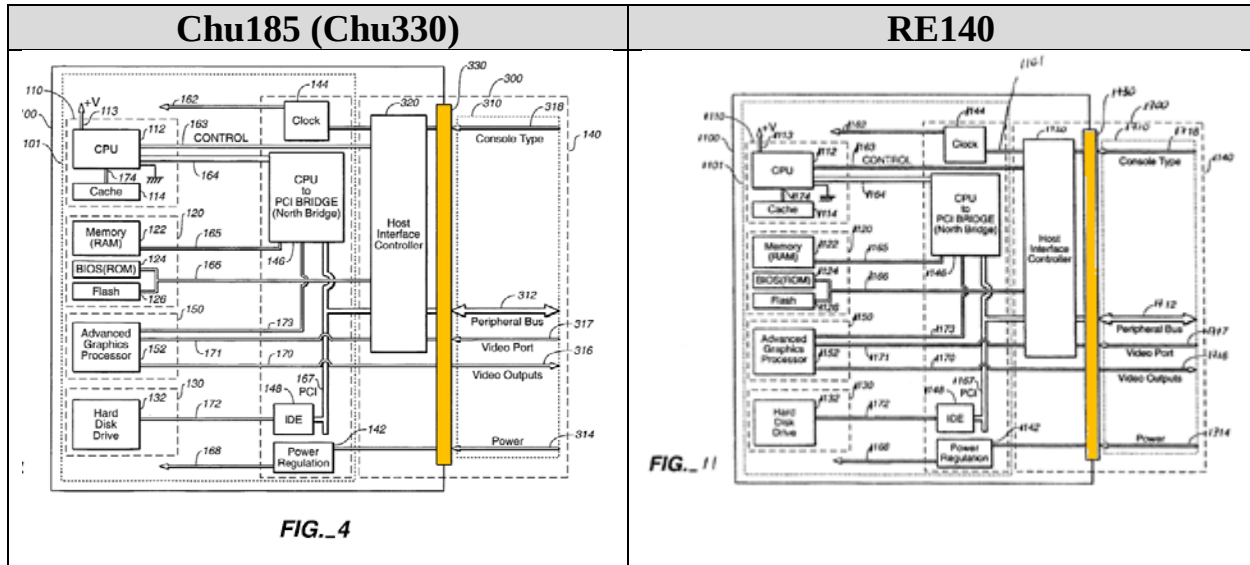
Figure 3E

vi. [14e] providing a **connector** for the computer for connection to a **console**, and,

131. In my opinion, although not explicitly labeled as such, a POSITA would have understood the **rectangular box** shown in Figure 2 of Chu330 as a **connector**. See Ex. 1003 [Chu330] at 6:7-25. Figure 1 also shows a rectangular box labeled as “high pin count connectors 101 and 102” that connects the Notebook PC with the Docking System See Ex. 1003 [Chu330] at 1:24-31. The **rectangular box** in Figure 2 provide the similar connection between the **ACM 205** and **peripheral console 210**.



132. Additionally, Chu185 in Figure 4 also shows an “**ACM connector component 330**” between an ACM and **PCON**. Ex. 1005 [Chu185] at 5:57-59; *see also* Ex. 1005 [Chu185] at 4:33-37, 5:49-52.



133. Moreover, Chu330 has numerous figures that correspond to various pins of a connector. There are specifically 88 pins that provide connections for data and video. Specifically, the pins corresponding to data are preceded by a “P” and the pins corresponding to video are preceded by a “V.” See Ex. 1003 [Chu330] at 4:12-26, 4:45-60, 6:15-22, 6:36-51, 12:58-14:4, 17:34-67, Figures 28-31. I have reproduced some exemplary Figures 28-31 showing these various pin assignments.

Chu330

ACM s CMI BUS Connector Plug PIN Position (88 pin):

E14	GND	GND	E1		P23	GND	GND	P1
E15	P&D D0 +	TPA+ /VPD+	E2		P24	PD0 +	PDR0 +	P2
E16	P&D D0 -	TPA- /VPD-	E3		P25	PD0 -	PDR0 -	P3
E17	GND	GND	E4		P26	GND	GND	P4
E18	P&D CLK +	TPB+ /VPCK+	E5		P27	PD1 +	PDR1 +	P5
E19	P&D CLK -	TPB- /VPCK-	E6		P28	PD1 -	PDR1 -	P6
E20	GND	1394 Detect	E7		P29	GND	GND	P7
E21	P&D D1 +	Reserved	E8		P30	PD2 +	PDR2 +	P8
E22	P&D D1 -	Reserved	E9		P31	PD2 -	PDR2 -	P9
E23	GND	Reserved	E10		P32	GND	GND	P10
E24	P&D D2 +	Reserved	E11		P33	PCK +	PCKR +	P11
E25	P&D D2 -	Reserved	E12		P34	PCK -	PCKR -	P12
E26	DFP Detect	Config 2	E13		P35	Config 1	Config 0	P13
V10	GND	V33	V1		P36	GND	GND	P14
V11	GND	V33	V2		P37	PD3 +	PDR3 +	P15
V12	GND	V33	V3		P38	PD3 -	PDR3 -	P16
V13	V33	V33	V4		P39	RSTEH#	RSTEP#	P17
V14	V33	V33	V5		P40	GREEN VIDEO	RED VIDEO	P18
V15	V33	V33	V6		P41	GND	GND	P19
V16	V5	V12	V7		P42	HSYNC	BLUE VIDEO	P20
V17	V5	V12	V8		P43	VSYN	GND	P21
V18	V5	V12	V9		P44	DDC2: SCL	DDC2: SDA	P22

FIG. 28

Pin No.	Symbol	Signal	Standard	Description
P2	PDR0 +	LVDS		Peripheral data reverse 0 +
P3	PDR0 -	LVDS		Peripheral data reverse 0 -
P5	PDR1 +	LVDS		Peripheral data reverse 1 +
P6	PDR1 -	LVDS		Peripheral data reverse 1 -
P8	PDR2 +	LVDS		Peripheral data reverse 2 +
P9	PDR2 -	LVDS		Peripheral data reverse 2 -
P11	PCKR +	LVDS		Peripheral clock reverse +
P12	PCKR -	LVDS		Peripheral clock reverse -
P15	PDR3 +	LVDS		Peripheral data reverse 3 +
P16	PDR3 -	LVDS		Peripheral data reverse 3 -
P24	PD0 +	LVDS		Peripheral data 0 +
P25	PD0 -	LVDS		Peripheral data 0 -
P27	PD1 +	LVDS		Peripheral data 1 +
P28	PD1 -	LVDS		Peripheral data 1 -
P30	PD2 +	LVDS		Peripheral data 2 +
P31	PD2 -	LVDS		Peripheral data 2 -
P33	PCK +	LVDS		Peripheral clock +
P34	PCK -	LVDS		Peripheral clock -
P37	PD3 +	LVDS		Peripheral data 3 +
P38	PD3 -	LVDS		Peripheral data 3 -
P13	Config 0	Static	3.3v or GND	Configuration bit 0
P35	Config 1	Static	3.3v or GND	Configuration bit 1
P17	RESTEP#	TTL	3.3v	Reset and Parity Error from console to ACM
P39	RESTEH#	TTL	3.3v	Reset and Parity Error from ACM to console
P18	Red Video	Analog		Video
P40	Green Video	Analog		Video
P20	Blue Video	Analog		Video
P42	HSYNC	TTL		Horizontal Sync
P43	VSYSN	TTL		Vertical Sync
P44	DDC2 SCL	TTL	VESA DDC std 2	DDC Clock
P22	DDC2 SDA	TTL	VESA DDC std 2	DDC Data
P1,P4,P7,P10, P14,P19,P21, P23,P26,P29, P32,P36,P41	GND		GND	Ground

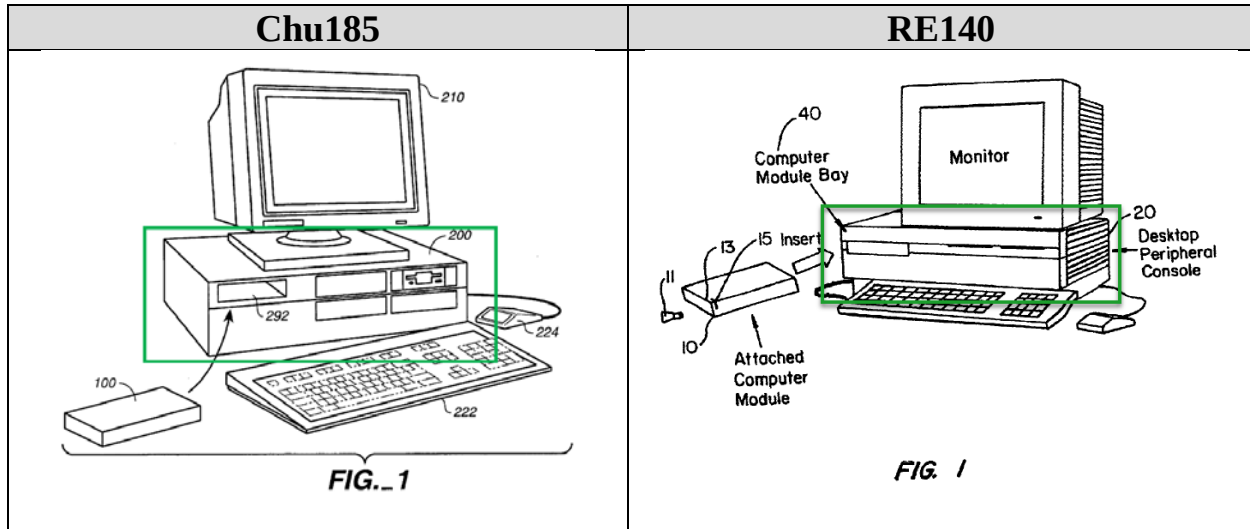
FIG. 29

Pin No.	Symbol	Signal	Standard	Description
E2	VPD+/TPA+		LVDS or 1394	Video capture port data or 1394
E3	VPD-/TPA-		LVDS or 1394	Video capture port data or 1394
E5	VPCK+/TPA+		LVDS or 1394	Video capture port data or 1394
E6	VPCK-/TPA-		LVDS or 1394	Video capture port data or 1394
E15	D0 +	TMDS	VESA P & D	Data 0 +
E16	D0 -	TMDS	VESA P & D	Data 0 -
E18	CLK +	TMDS	VESA P & D	Clock +
E19	CLK -	TMDS	VESA P & D	Clock -
E21	D1 +	TMDS	VESA P & D	Data 1 +
E22	D1 -	TMDS	VESA P & D	Data 1 -
E24	D2 +	TMDS	VESA P & D	Data 2 +
E25	D2 -	TMDS	VESA P & D	Data 2 -
E13	Config 2			Configuration bit 2
E26	Config 3			Configuration bit 3
E1, E4, E14, E17,E20,E23	GND		GND	Ground

E7	Reserved			Reserved
E8	Reserved			Reserved
E9	Reserved			Reserved
E10	TV-CV/reserved		NTSC	TV Composite Video or reserved
E11	SV Y/reserved		Super Video	SV Luminance or reserved
E12	SV C/reserved		Super Video	SV Chrominance or reserved

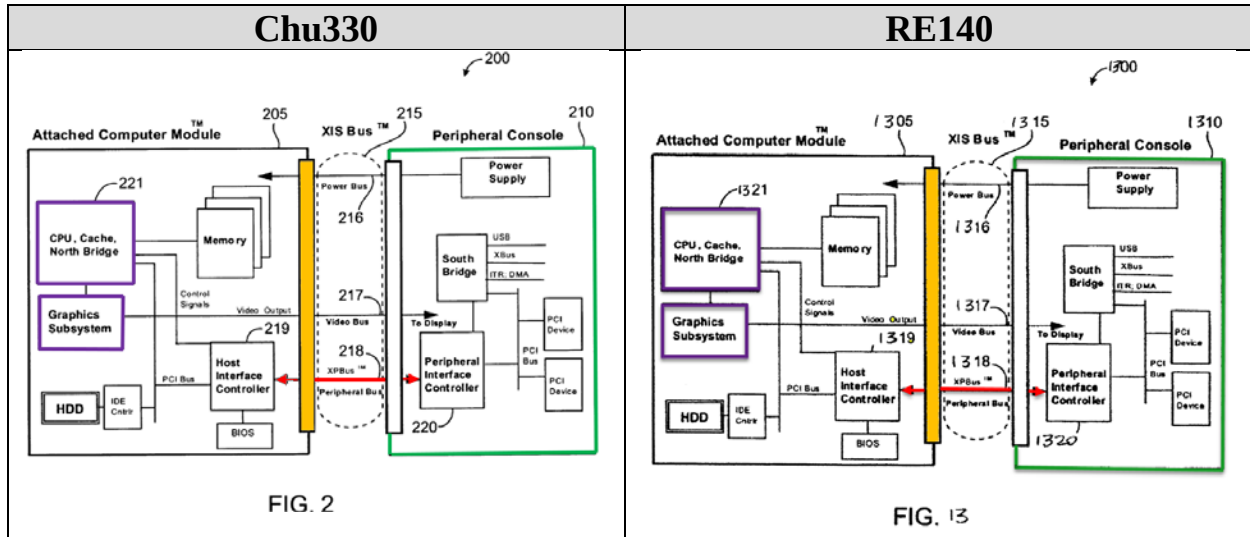
FIG. 30

134. Additionally, Chu185 in Figure 1 shows an additional example of a **PCON**. Ex. 1005, Figure 1. Chu185 teaches that “FIG. 1 depicts an exemplary desktop **peripheral console [PCON]** and attached computing module [ACM]. ... The **PCON** also provides connections for a display monitor, a keyboard, and a mouse.” Ex. 1005, 3:46-51; *see also* Ex. 1005, 4:1-2, 4:47-48 (showing an ACM 100). In Figure 2 Chu185 shows the **PCON** as “a chassis that connects several components of the computer system.” Ex. 1005, 4:33-36.



- vii. [14f] providing a **first Low Voltage Differential Signal (LVDS) channel** to couple to the **connector**, the first LVDS channel comprising two unidirectional, serial bit channels that transmit data in opposite directions.

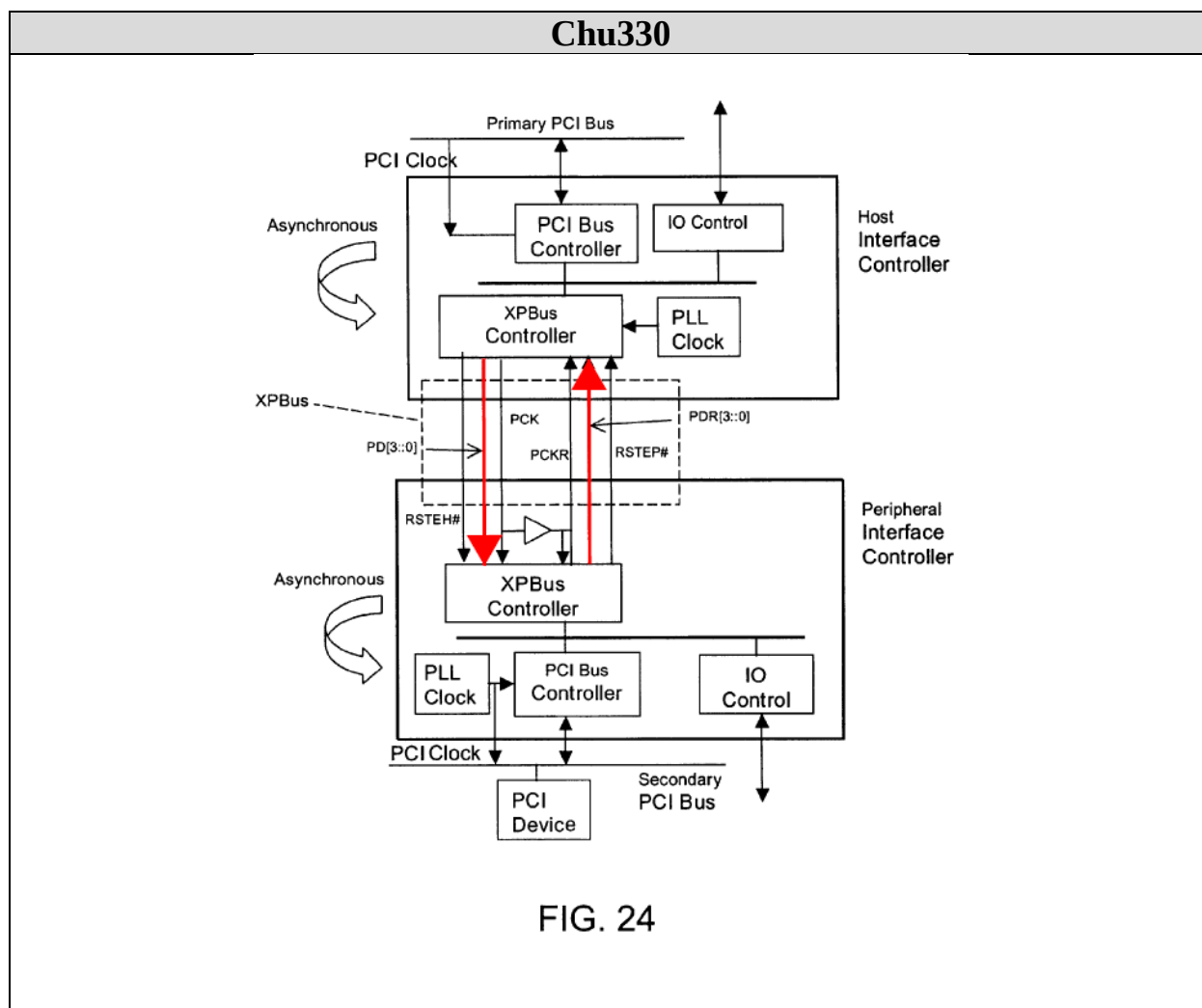
135. Chu330 teaches the claimed “**LVDS channel**.” As shown below in Figure 2, the XIS bus (which includes the XPBus) couples together the ACM 205 and the **PCON 21**, which is coupled to the **connector**. See Ex. 1003 [Chu330] at 6:7-11. “The **PCON** also provides connections for a display monitor, a keyboard, and a mouse.” Ex. 1005 [Chu185] at 3:46-52. The XPBus “is also referred to as an interface channel” and “allows using **LVDS channels**.” Ex. 1003 [Chu330] at 6:7-11 and 2:36-38. Additionally, as seen in Figure 2 below, the XPBus, which includes **LVDS channels**, is coupled to the **connector**. Ex. 1003 [Chu330] at Figure 2.



136. Chu330 also explains that the XPSBus “includes two sets of unidirectional serial bit channels which transmit data in opposite directions such that one set of bit channels transmits serial bits from the HIC to the PIC while the other set transmits serial bits from the PIC to the HIC.” Ex. 1003 [Chu330] at 3:18-23. Similarly, claims 1, 9, and 12 of Chu330 teach that the “differential communication channel [between the ACM and PCON] comprises **an LVDS channel,**” and the “differential signal channel comprises at least two pairs of differential signal lines.” Ex-1003, claims 1, 9, and 12.

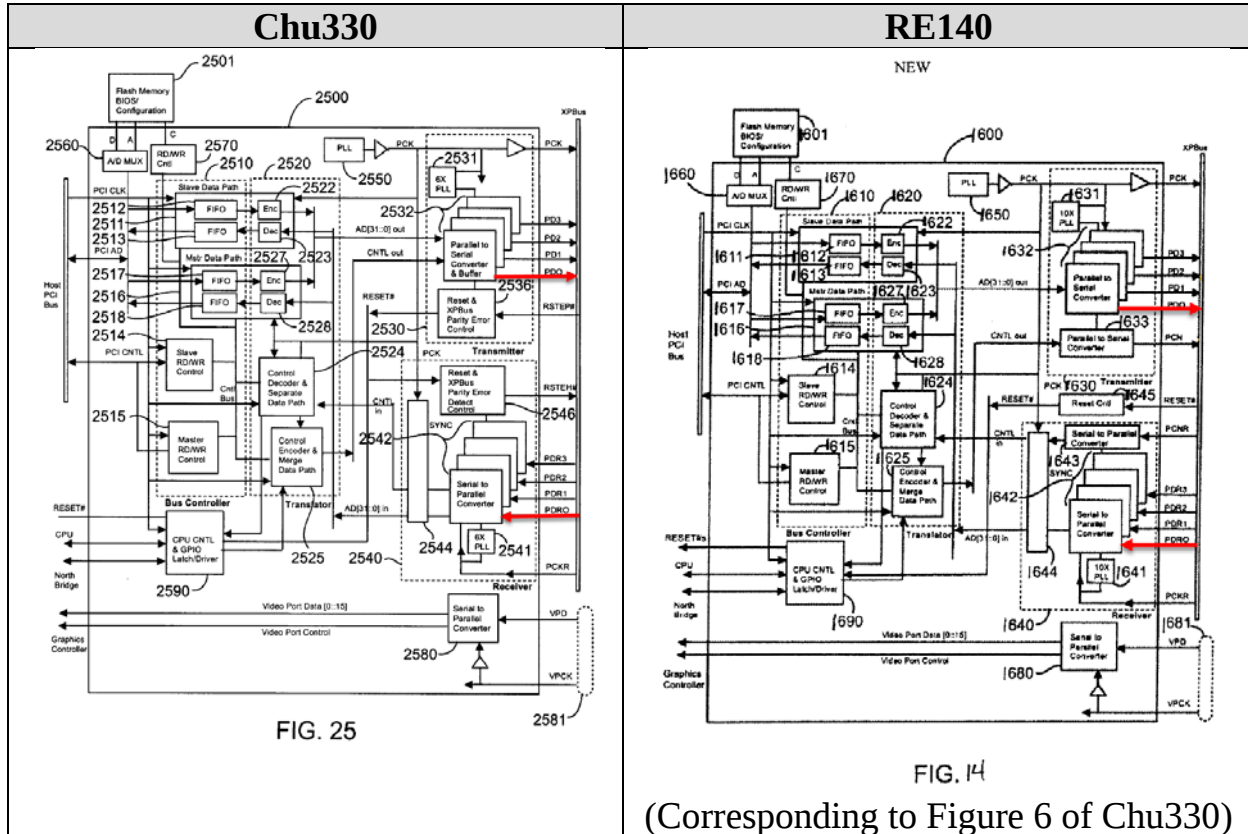
137. As shown in Figure 24 of Chu330, the XPSBus includes PCK line 591 and PD[0::3] lines 592, PCKR line 593, and PDR[0::3] lines 594. See Ex. 1003 [Chu330] at 16:6-8, 6:36-51. A similar set of lines is also shown in Figure 5 of

Chu330. See Ex. 1003 [Chu330] at Figure 5, 6:36-51 (“PCK ... PD[0::3] and PCN lines ... PCKR ... PDR[0::3] and PCNR lines”).



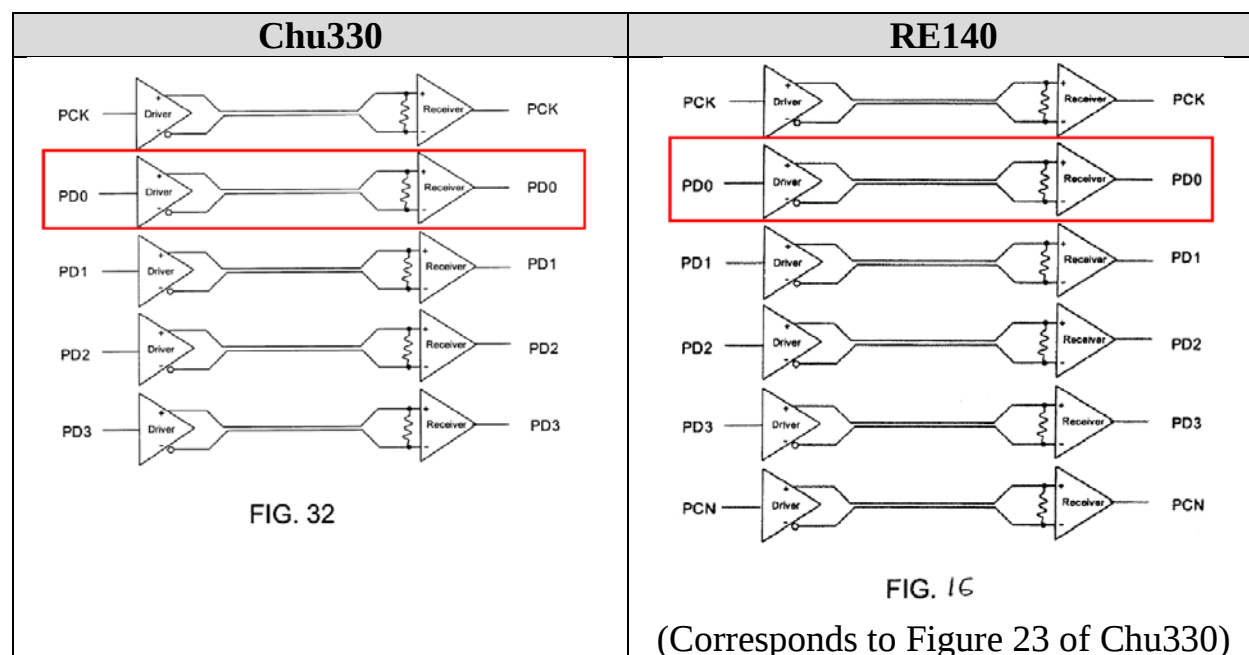
138. Figure 25 of Chu330 shows some additional details within the HIC. See Ex. 1003 [Chu330] at 7:29-30, 16:24-17:13 (“As mentioned above, the remaining elements in HIC 2500 are identical to those in HIC 600 and reference to the

description of elements in HIC 600 may be made to understand the function of the corresponding elements in HIC 2500.”). As shown, the **first LVDS channel** includes data lines, such as **PD0 and PDR0**.



139. Chu330 further shows in Figure 32 that **PD0** is a “unidirectional LVDS line[.]” Ex. 1003 [Chu330] at 18:1-3, 15:11-15. **PDR0** has the same structure as those shown in Figure 32, except that it transmits data in a direction opposite to that in which the lines shown in Figure 32 transmit data. See Ex. 1003 [Chu330] at 18:1-10; see also Ex. 1003 [Chu330] at Figure 23, 15:10-16:5, Figure

23 (also including LVDS lines PCN and PCNR). The “pair of physical lines ... together transmit a signal” and the difference in voltage between them is low. Ex. 1003 [Chu330] at 2:15-17, 15:57-67.



140. Additionally, the **first LVDS channel**, including data lines, such as **PD0 and PDR0**, is taught by Chu330 to include “at least two pairs of differential signal lines.” Ex. 1003 [Chu330] at claims 9 and 12; *see also* Ex. 1003 [Chu330] at 15:10-22, 15:63-67, 18:1-10. Chu330 further teaches that the “[t]he XPBus which includes lines PCK, **PD0** to PD3, ... **PDR0** to PDR3, ... has two sets of unidirectional lines transmitting clock signals and bits in opposite directions.” Ex. 1003 [Chu330], 15:31-34. Chu330 also teaches that “[t]he first set of unidirectional

lines includes PCK, **PD0** to PD3 [and] [t]he second set of unidirectional lines includes PCKR, **PDR0** to PDR3.” Ex. 1003 [Chu330], 15:34-36; *see also* Ex. 1003 [Chu330] at 15:10-16:5, 16:25-26, 17:8-13. Chu330 presents **PD0** as **PD0** as “data lines” being used to send data. Ex. 1003 [Chu330] at 9:16-22; *see also* Ex. 1003 [Chu330] at 8:61-67, 16:25-26, 17:8-13, 18:1-10, Figure 32.

141. Chu330 also teaches that the data lines **PD0** as **PD0** are **serial bit channels**. *See* Ex. 1003 [Chu330] at Figures 2, 5, and 25, Abstract, 2:60-61, 6:7-11, 15:51-16:5; Figs. 2, 5, 24-25, 32. Particularly, Chu330 explains that the “interface channel includes two sets of unidirectional **serial bit channels**.” Ex. 1003 [Chu330] at 3:18-25.

2. Claim 15

- i. [15] The method of claim 14 further comprises conveying Universal Serial Bus (USB) protocol information over the **first LVDS channel**.

142. As I explain above with regard to [limitation 14f], Chu330 teaches an XPBus which conveys data over a **first LVDS channel**.

143. Additionally, the **first LVDS channel** conveys USB protocol information. Particularly, Chu330 states that “[t]he bits sent in the first nibble of each packet indicate the type of data in that packet. FIG. 35 is a table showing different types of first nibbles and their corresponding data packet types.” Ex. 1003

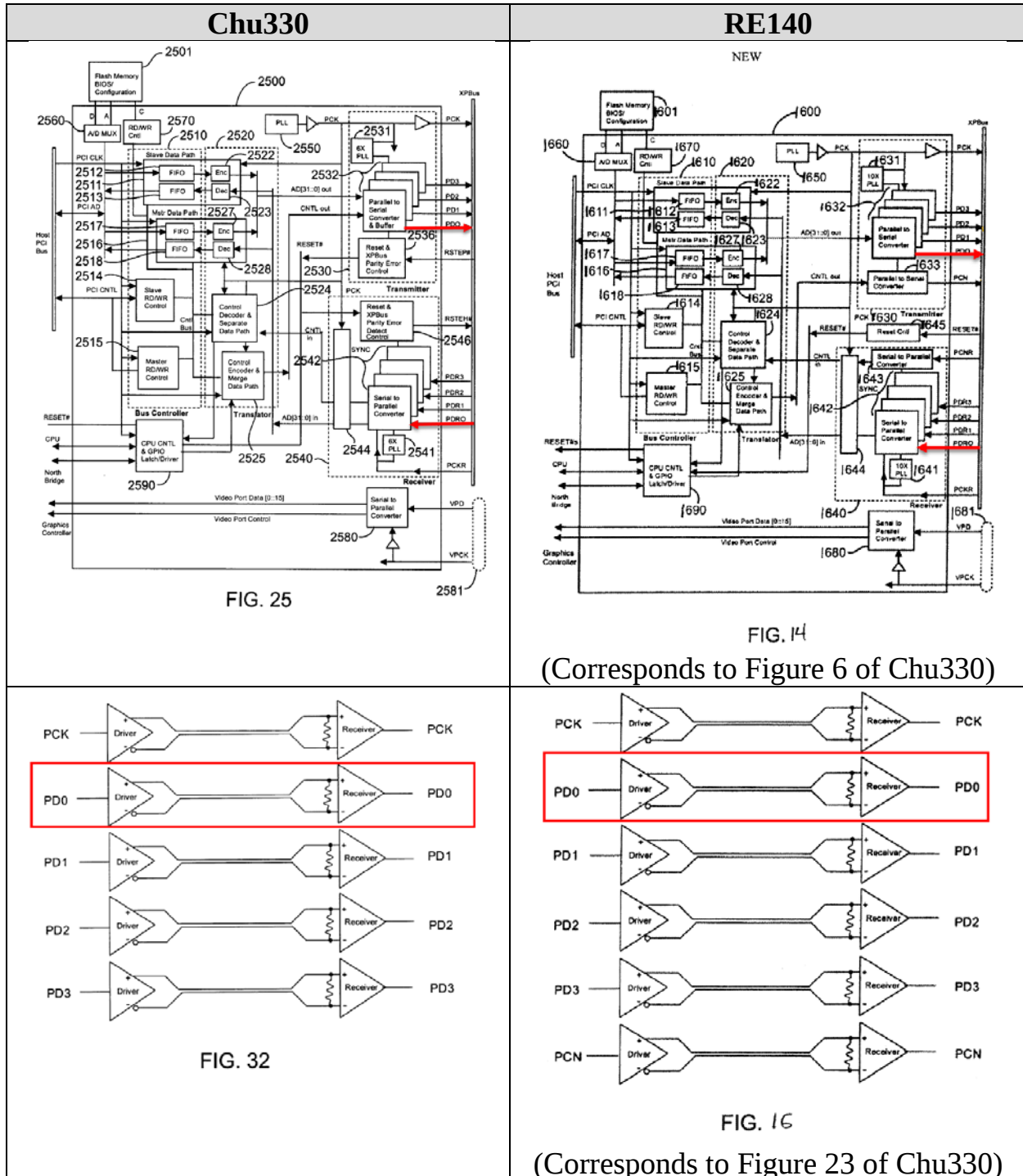
[Chu330] at 19:22-25, Figures 33-35. As I have highlighted below, the “reserved data packet types can be used to support non-PCI bus transactions, *e.g.*, USB transactions.” Ex. 1003 [Chu330] at 19:13-15; *see also* Ex. 1003 [Chu330] at 19:5, 19:22-25.

Chu330	RE140																																												
<table> <tr> <th>ID bits (P0 P1 P2 P3)</th><th>Data Packet Type</th></tr> <tr> <td>X X 0 0</td><td>PCI 1st address/data segment</td></tr> <tr> <td>X X 1 0</td><td>PCI 2nd address/data segment</td></tr> <tr> <td>0 0 0 1</td><td>Control 1st segment with PCI response</td></tr> <tr> <td>1 0 0 1</td><td>Control 1st segment without PCI response</td></tr> <tr> <td>0 1 0 1</td><td>Control 2nd segment with PCI response</td></tr> <tr> <td>1 1 0 1</td><td>Control 2nd segment without PCI response</td></tr> <tr> <td>0 0 1 1</td><td>Reserved</td></tr> <tr> <td>1 0 1 1</td><td>Reserved</td></tr> <tr> <td>0 1 1 1</td><td>Initialization</td></tr> <tr> <td>1 1 1 1</td><td>NOOP</td></tr> </table> FIG. 35	ID bits (P0 P1 P2 P3)	Data Packet Type	X X 0 0	PCI 1st address/data segment	X X 1 0	PCI 2nd address/data segment	0 0 0 1	Control 1st segment with PCI response	1 0 0 1	Control 1st segment without PCI response	0 1 0 1	Control 2nd segment with PCI response	1 1 0 1	Control 2nd segment without PCI response	0 0 1 1	Reserved	1 0 1 1	Reserved	0 1 1 1	Initialization	1 1 1 1	NOOP	<table> <tr> <th>ID bits (P0 P1 P2 P3)</th><th>Data Packet Type</th></tr> <tr> <td>X X 0 0</td><td>PCI 1st address/data segment</td></tr> <tr> <td>X X 1 0</td><td>PCI 2nd address/data segment</td></tr> <tr> <td>0 0 0 1</td><td>Control 1st segment with PCI response</td></tr> <tr> <td>1 0 0 1</td><td>Control 1st segment without PCI response</td></tr> <tr> <td>0 1 0 1</td><td>Control 2nd segment with PCI response</td></tr> <tr> <td>1 1 0 1</td><td>Control 2nd segment without PCI response</td></tr> <tr> <td>0 0 1 1</td><td>Reserved</td></tr> <tr> <td>1 0 1 1</td><td>Reserved</td></tr> <tr> <td>0 1 1 1</td><td>Initialization</td></tr> <tr> <td>1 1 1 1</td><td>NOOP</td></tr> </table> FIG. 24	ID bits (P0 P1 P2 P3)	Data Packet Type	X X 0 0	PCI 1st address/data segment	X X 1 0	PCI 2nd address/data segment	0 0 0 1	Control 1st segment with PCI response	1 0 0 1	Control 1st segment without PCI response	0 1 0 1	Control 2nd segment with PCI response	1 1 0 1	Control 2nd segment without PCI response	0 0 1 1	Reserved	1 0 1 1	Reserved	0 1 1 1	Initialization	1 1 1 1	NOOP
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3. Claim 16

- i. [16] The method of claim 14 further comprises conveying encoded address and data bits of a Peripheral Component Interconnect (PCI) bus transaction in serial form over the **first LVDS channel**.

144. As I explain above with regard to [limitation 14f] and as shown in Figures 25 and 32 of Chu330 below, Chu330 teaches an XPBus which conveys data over the **first LVDS channel**. See Ex. 1003 [Chu330] at 2:36-38.



145. Further, Chu330 teaches, on the differential signal channel, communicating “an encoded bit stream comprising PCI bus transactions data bits, system control signal data bits, and peripheral console configuration information data bits, ... separated within the encoded bit stream.” Ex. 1003 [Chu330] at claim 1. Chu330 teaches that “PCI and ISA peripheral busses are industry standards, well known and understood in the art.” Ex. 1003 [Chu330] at 14:59-61.

146. As shown above in Figure 2 of Chu330, the encoded bit stream of PCI bus transactions are sent from the ACM to the PCI Devices in the PCON. *See* Ex. 1003 [Chu330] at claim 1 (“a differential signal channel between the computer module and the peripheral console, the differential signal channel configured to communicate an encoded bit stream comprising PCI bus transactions”). More specifically, the ACM has a first PCI bus and the PCON has a second PCI bus. *See* Ex. 1003 [Chu330] at 14 (“the computer module further comprises a first PCI bus”), claim 15 (“the peripheral console comprises a second PCI bus”). Moreover, the PCI Devices are connected to the second PCI bus. *See* Ex. 1003 [Chu330] at claim 15 (“the peripheral console comprises a second PCI bus in electrical communication with the differential signal channel through a second interface controller ... to bridge the first PCI bus to the second PCI bus.”). The PCI busses are based on industry standard and so that PCI bus transactions are also in accordance with the industry

standard PCI Local Bus Specification. PCI bus transactions are in accordance with industry standard PCI Local Bus Specification. *See* Ex. 1005 [Chu185] at 14:59-61 (“PCI and ISA peripheral busses are industry standards, well known and understood in the art.”).

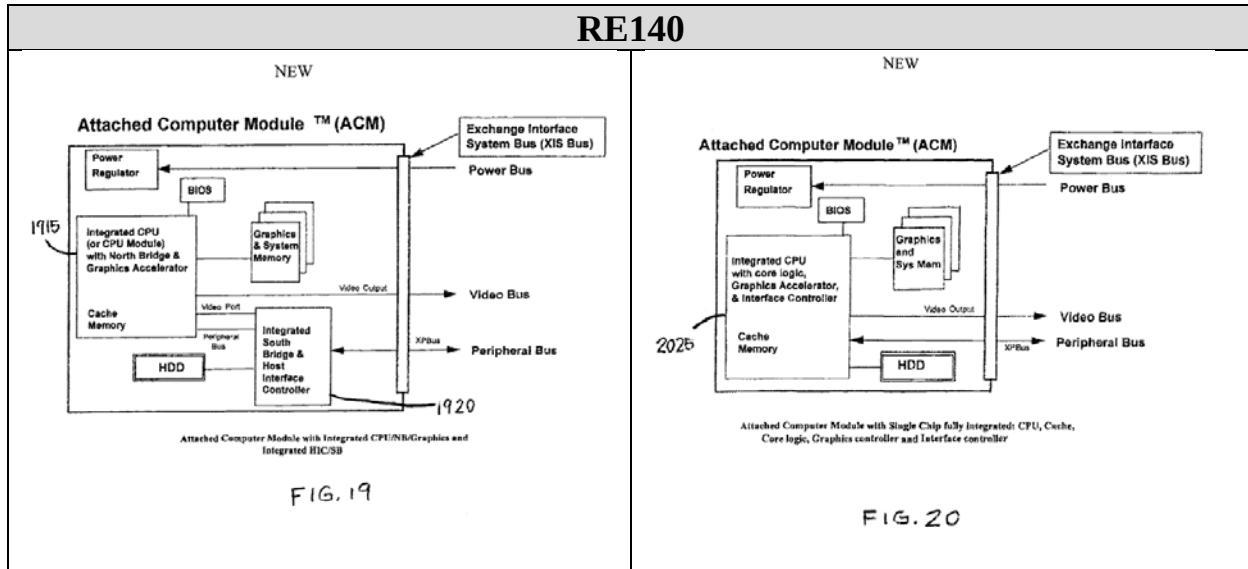
147. The PCI bus transaction bits are also serialized from a parallel form such that bits flow serially over the **first LVDS channel**. For example, Chu330 teaches encoding “PCI address/data (AD) ... bits to a form more suitable for parallel to serial conversion prior to transmittal on the XPBus.” Ex. 1003 [Chu330] at 7:59-64. Specifically, the “multiplexed parallel A/D bits and some control bits ... are serialized ... into ... bit packets ... then output on data lines PD0 to PD3 of the XPBus.” Ex. 1003 [Chu330] at 8:61-65. *See also* Ex. 1003 [Chu330] at 7:64-66, 9:16-27, 14:5-26 (“The bits transmitted on lines PD0 to PD3 represent 32 PCI AD[31:0] signals.”), Fig. 21. Additionally, Chu330 teaches using lines PCN and PCNR for conveying serialized encoded bit packets. *See* Ex. 1003 [Chu330] at 8:29-34, 8:38-47, 8:65-67, 9:27-30; *see also* Ex. 1003 [Chu330] at 16:8-11, 16:35-36. This is mirrored for address and data information from the data lines PDR0 to PDR3. *See* Ex. 1003 [Chu330] at 7:64-66, 9:16-27, 16:25-26, 17:8-13. In other words, Chu330 teaches a flow of bits transferred serially between the HIC and PIC of Figures 2 and 24. Ex. 1003 [Chu330] at 3:18-23, Fig. 5.

148. In that way, the **first LVDS channel** conveys encoded address and data bits of a PCI bus transactions in serial form from the ACM (including the HIC) to the PCON (including the PIC). See Ex. 1003 [Chu330] at Abstract, 2:60-61, 3:18-25, 6:7-11; *see also* Ex. 1003 [Chu330] at 15:51-16:5, Fig 5.

4. Claim 17

- i. [17] The method of claim 14 further comprises of connecting a **second LVDS channel** directly to the **integrated CPU and graphics controller**, the **second LVDS channel** comprising two unidirectional, serial bit channels that transmit data in opposite directions.

149. At the outset, in my opinion, Figure 20 of RE140 is the only disclosure in RE140 that provides support for this limitation. Figure 20 shows the XPBus, which contains the LVDS channel that has two unidirectional, differential signal pairs to transmit data in opposite directions, is directly coupled to the “Integrated CPU with ... Graphics Accelerator... 2025.” In contrast, Figure 19 (as on example) shows the XPBus to be coupled to the “Integrated CPU ... & Graphics Accelerator 1915” through an “Integrated South Bridge & Host Interface Controller 1920.”



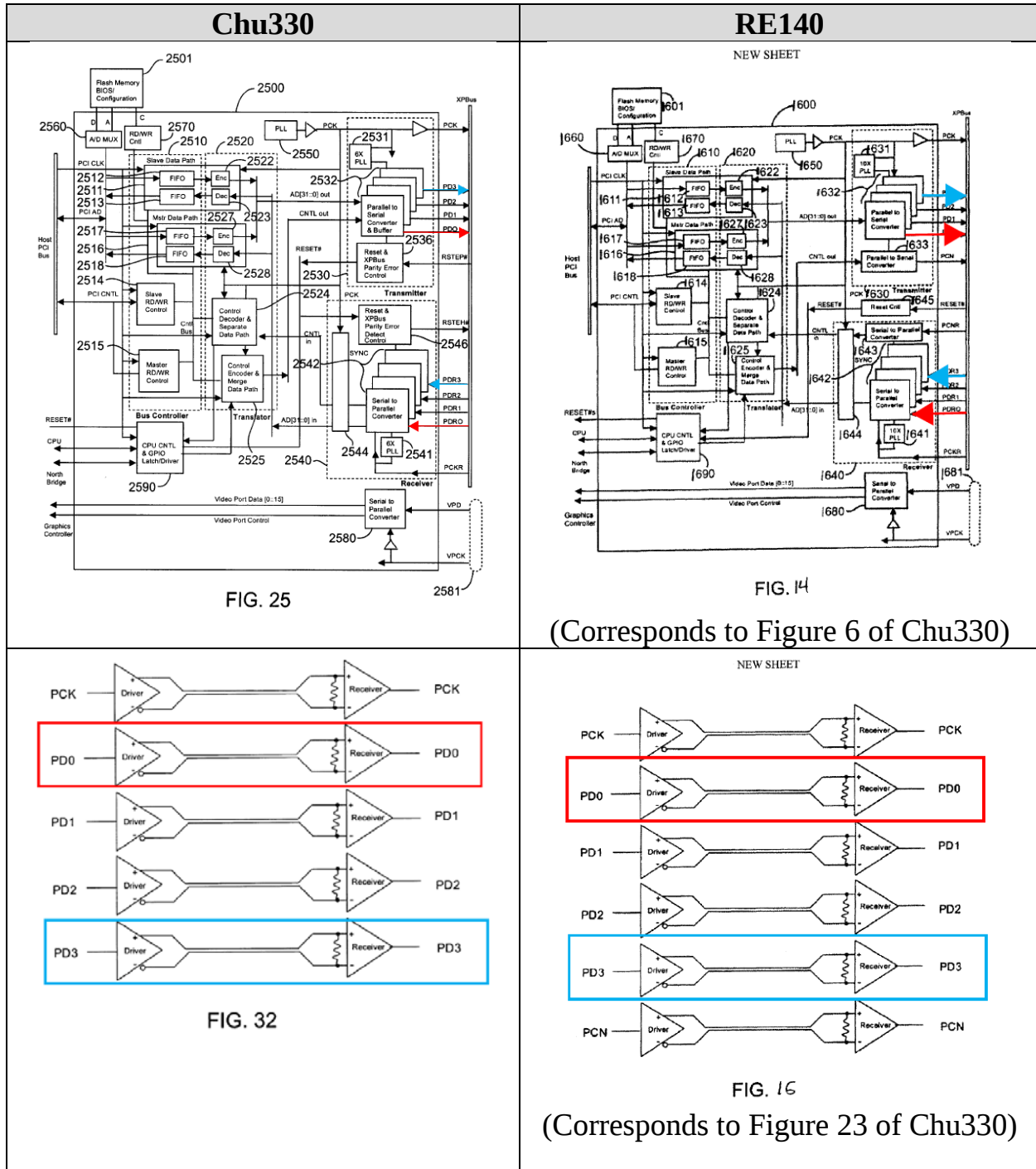
150. I explained above in [limitation 14f] how Chu330 teaches the claimed **first LVDS channel**. Chu330 also teaches the claimed “**second LVDS channel**.” My analysis of the **first LVDS channel** is equally applicable to a **second LVDS channel**.

151. To reiterate, as I explained above in [limitation 14f], Chu330 teaches that the XPBus “allows using **LVDS channels**.” Ex. 1003 [Chu330] at 6:7-11 and 2:36-38. Chu330 also explains that the XPBus “includes two sets of unidirectional serial bit channels which transmit data in opposite directions such that one set of bit channels transmits serial bits from the HIC to the PIC while the other set transmits serial bits from the PIC to the HIC.” Ex. 1003 [Chu330] at 3:18-23. Similarly, claims 1, 9, and 12 of Chu330 teach that the “differential communication channel [between the ACM and PCON] comprises **an LVDS**

channel,” and the “differential signal channel comprises at least two pairs of differential signal lines.” Ex-1003, claims 1, 9, and 12.

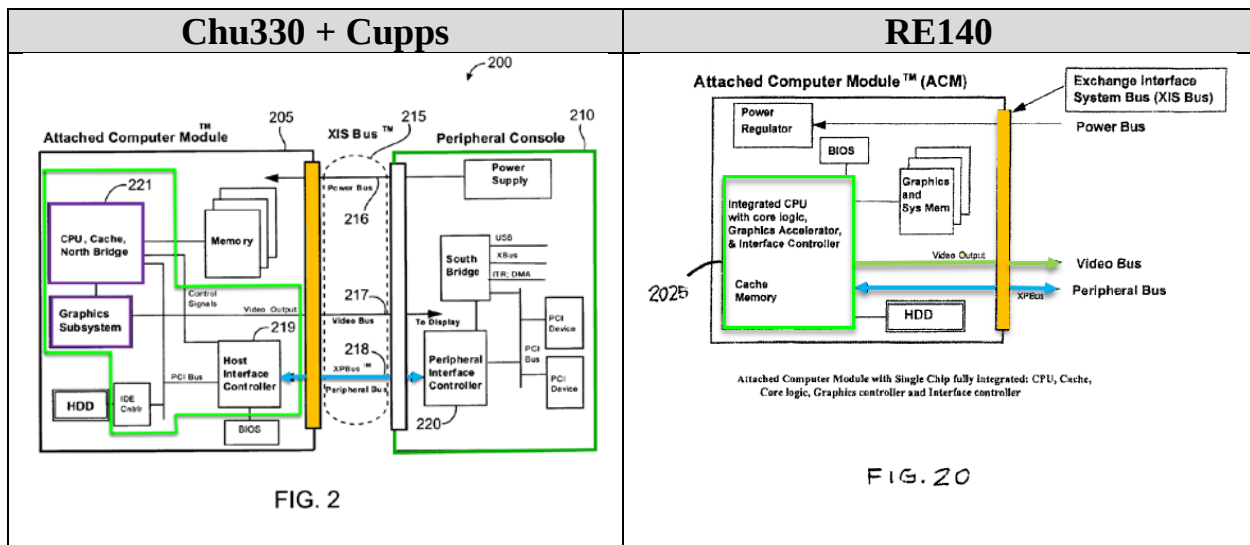
152. As shown in Figure 5 of Chu330, the XPBus includes PCK line 591 and PD[0::3] lines 592, PCKR line 593, and PDR[0::3] lines 594. *See* Ex. 1003 [Chu330] at 6:47-51. Similar set of lines are also shown in Figure 25 of Chu330. Figure 25 of Chu330 shows some additional details within the HIC. *See* Ex. 1003 [Chu330] at 16:24-17:13 (“As mentioned above, the remaining elements in HIC 2500 are identical to those in HIC 600 and reference to the description of elements in HIC 600 may be made to understand the function of the corresponding elements in HIC 2500.”); *see also* 7:29-30, As shown, the **second LVDS channel** includes data lines, such as **PD3 and PDR3**.

153. Chu330 further shows in Figure 32 that **PD3** is a “unidirectional LVDS line[.]” Ex. 1003 [Chu330] at 18:1-3; *see also* Ex. 1003 [Chu330] at 15:11-15. **PDR3** has “the same structure as those shown in FIG. 33, except that they transmit data in the opposite direction than of those shown in FIG. 32.” Ex. 1003 [Chu330] at 18:3-10; *see also* Ex. 1003 [Chu330] at 15:15-21, 15:31-36, Figure 23. The “pair of physical lines ... together transmit a signal” and the difference in voltage between them is low. Ex. 1003 [Chu330] at 2:15-17, 15:57-67.

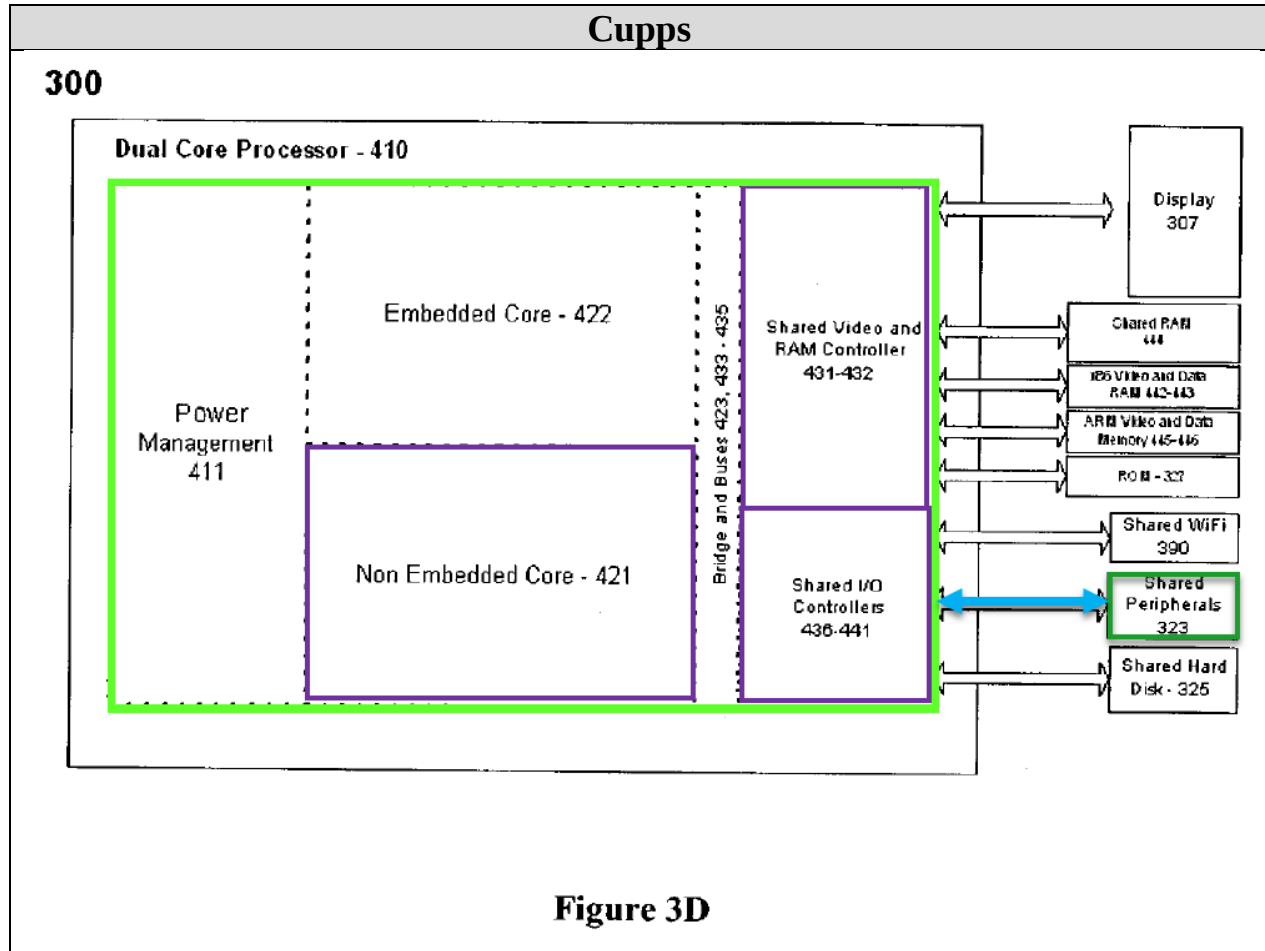


154. Additionally, Chu330 in combination with Cupps renders obvious the **second LVDS channel** being directly connected to the **integrated CPU and**

graphics controller. Particularly, I explained with [limitation 14a] that Chu330 in combination with Cupps teaches integrating **integrated** the **CPU and graphics controller** in **a single chip**, where the XPBus is thereby also directly connected to the **integrated** the **CPU and graphics controller**. As explained above, the XPBus includes the **first LVDS channel** and **second LVDS channel**. In that way, the XPBus, including the **first LVDS channel** and **second LVDS channel**, is directly connected to the **integrated** the **CPU and graphics controller**. This is akin to is shown in RE140 Figure 20 (as shown below).



155. As an example, Cupps depicts **shared peripherals 323 directly connected** to the **integrated chip 410** in Figure 3D.



5. Claim 18

- i. [18pre] A method of improving performance of a computer, comprising:

156. I explained above in [preamble 14pre] how Chu330 teaches this preamble.

- ii. [18a] obtaining an **integrated Central Processing Unit (CPU) with a graphics controller in a single chip,**

157. I explained above in [limitation 14a] how Chu330 teaches this limitation.

- iii. [18b] connecting a **Differential Signal channel directly to the integrated CPU and graphics controller to output video data,**

158. I explained above in [limitations 14b] how Chu330 in combination with Cupps render obvious this limitation.

- iv. [18c] providing a **connector for the computer for connection to a console;**

159. I explained above in [limitations 14e] how Chu330 teaches this limitation.

- v. [18d] providing a first **Low Voltage Differential Signal (LVDS) channel** to couple to the **connector**, the first LVDS channel comprising two unidirectional, serial bit channels that transmit data in opposite directions; and

160. I explained above in [limitation 14f] how Chu330 teaches this limitation.

- vi. [18e] conveying Universal Serial Bus (USB) protocol information through the **first LVDS channel**.

161. I explained above in [limitation 15] how Chu330 teaches this limitation.

6. Claim 19

- i. [19] The method of claim 18 further comprising connecting a **second LVDS channel** directly to the **integrated CPU and graphics controller**, the **second LVDS channel** comprising two unidirectional, serial bit channels that transmit data in opposite directions.

162. I explained above in [claim 17] how Chu330 in combination with Cupps render obvious this limitation.

7. Claim 20

- i. [20] The method of claim 19 further comprising conveying Universal Serial Bus (USB) protocol information over the **second LVDS channel**.

163. I explained above in [claim 15] how Chu330 teaches this limitation. Specifically, the **second LVDS channel** can include data lines **PD3** and **PDR3**. And, just like the **first LVDS channel** can convey USB protocol information, the **second LVDS channel** can convey USB protocol information for the same reasons.

8. Claim 21

- i. [21] The method of claim 18 further comprising conveying Transition Minimized Differential Signaling (TDMS) signals through the **Differential Signal channel**.

164. I explained above in [limitations 14b and 14c] how Chu330 teaches this limitation.

9. Claim 22

- i. [22pre] A method of improving performance of a computer, comprising:

165. I explained above in [preamble 14pre] how Chu330 teaches this preamble.

- ii. [22a] obtaining an **integrated Central Processing Unit (CPU) with a graphics controller in a single chip**;

166. I explained above in [limitation 14a] how Chu330 in combination with Cupps renders obvious this limitation.

- iii. [22b] connecting a **first Low Voltage Differential Signal (LVDS) channel** directly to the **integrated CPU and graphics controller**, wherein the **first LVDS channel** comprises two unidirectional, serial bit channels that transmit data in opposite directions,

167. As I explained above in [limitation 14f], Chu330 teaches the **first LVDS channel** which comprises two unidirectional, serial bit channels that

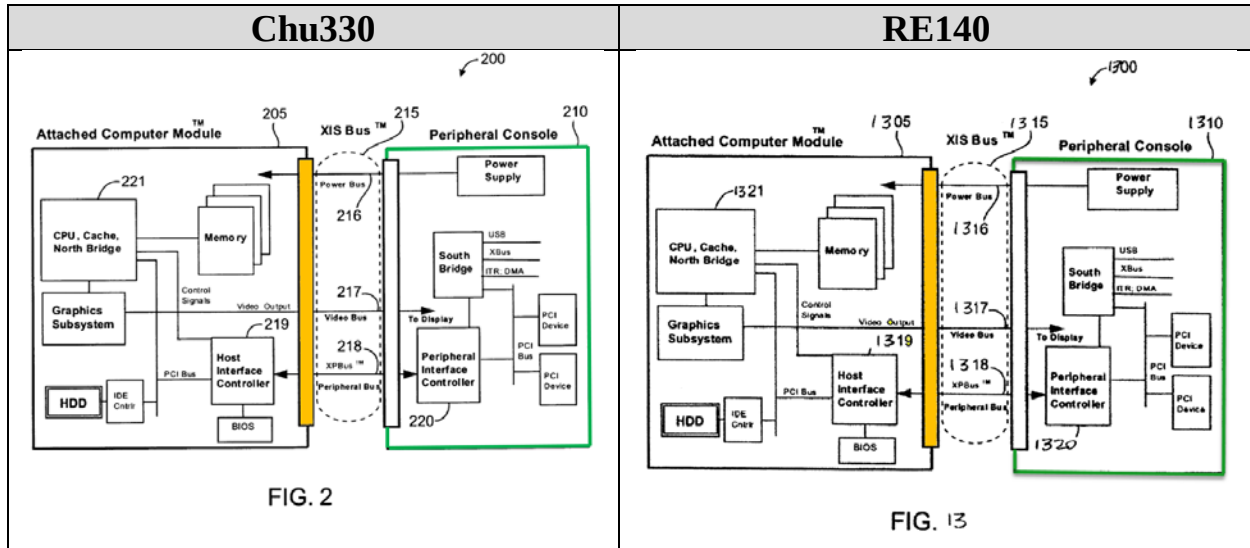
transmit data in opposite directions. I additionally explained above in [claim 17] how Chu330 in combination with Cupps renders obvious the direct connection of the **second LVDS channel** to the **integrated CPU and graphics controller**. The first LVDS channel is directly connected to the to the **integrated CPU and graphics controller** for the same reasons as those provided for the **second LVDS channel** with [claim 17]. For those reasons, Chu330 in combination with Cupps renders obvious this limitation.

iv. [22c] conveying Universal Serial Bus (USB) protocol information through the first LVDS channel;

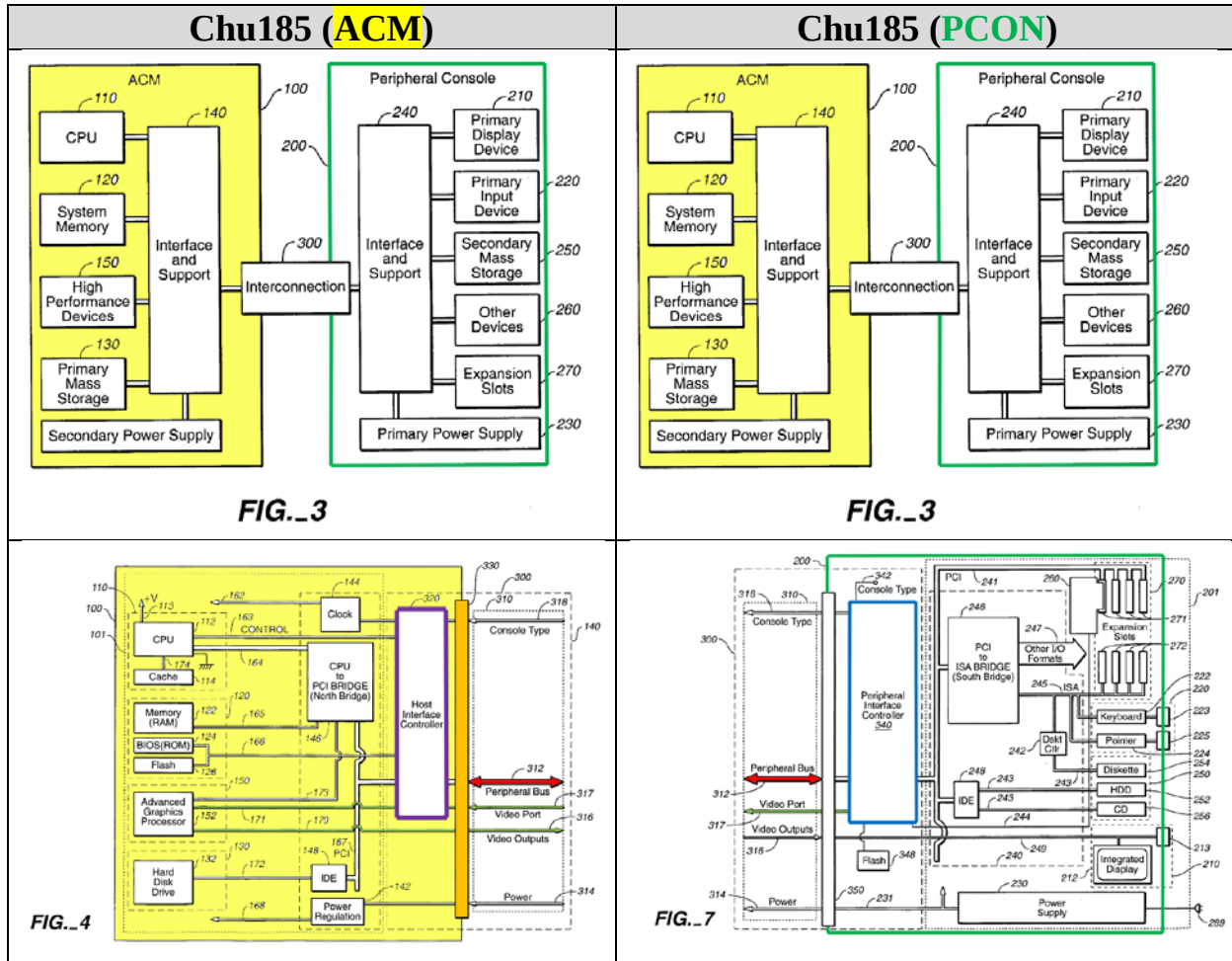
168. I explained above in [claim 15 and limitation 18e] how Chu330 teaches this limitation.

v. [22d] providing a connector for the computer for connection to an external peripheral; and

169. I explained above in [limitation 14e] how Chu330 teaches a **connector** for the computer for connection to a **console**.



170. In Figures 3, 4, and 7, Chu185 (which Chu330 incorporates by reference) also shows an interconnection 300 between an ACM (computer) and **PCON** to “convey ... operational signals between the ACM and **PCON**.” Ex. 1005 [Chu185] at 4:33-36; *see also* Ex. 1005 [Chu185] at 3:55-59 (explaining that the “ACM ... is inserted into the opening of the computer bay ... to interact with the peripheral devices housed in the **PCON**.”). The interconnection 300 connects the ACM to components within the **PCON**—including peripherals. *See* Ex. 1005 [Chu185] at 4:40-44, 5:30-32, 13:9-13, 13:17-21; *see also* Ex. 1005 [Chu185] at 5:59-6:4, 13:1-39. In that way, the **connector** connects to the ACM. Ex-1005, 5:57-6:4.



vi. [22e] providing a **second LVDS channel** to couple to the **connector**, the **second LVDS channel** comprising two unidirectional, serial bit channels that transmit data in opposite directions.

171. I explained above in [limitations 14f and 17] how Chu330 teaches this limitation. The same reasoning applied to show the **first LVDS channel** also applies to show a **second LVDS channel**.

10. Claim 23

- i. [23] The method of claim 22 further comprising conveying Universal Serial Bus (USB) protocol information over the **second LVDS channel**.

172. I explained above in [claims 15 and 20] how Chu330 teaches this limitation.

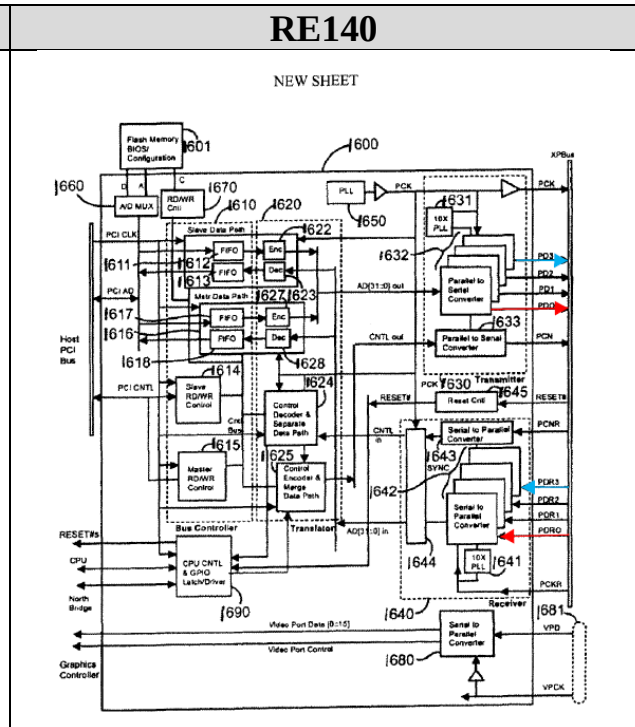
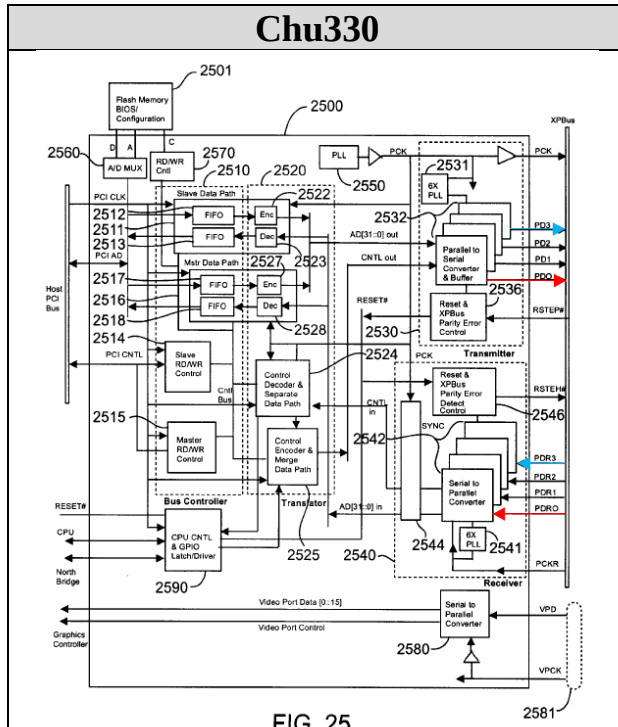
11. Claim 24

- i. [24] The method of claim 22 further comprising conveying encoded address and data bits of a Peripheral Component Interconnect (PCI) bus transaction in serial form over the **second LVDS channel**.

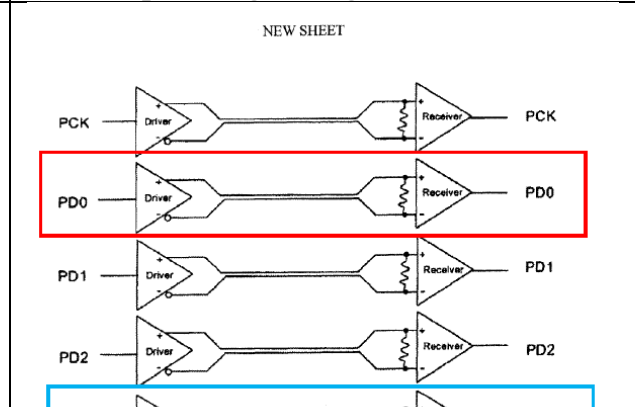
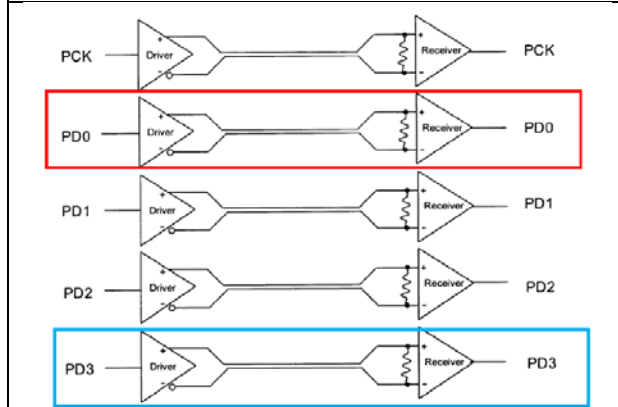
173. I explained above in [claim 16] how Chu330 teaches this limitation. The same reasoning for the **first LVDS channel** conveying PCI bus transactions applies to the **second LVDS channel** conveying PCI bus transactions.

174. To be clear, I have colored below Chu330's Figures 25 and 32 with two different colors the conceptually illustrate two different types of data packet transmission are occurring, but they are not occurring simultaneously. **PD0** and **PDR0**, colored red, indicate encoded USB transactions over the **first LVDS channel**, but all of the data lines from PD0 through PDR3 are utilized for that USB transaction. See Ex. 1003 [Chu330] at 18:13-19. **PD3** and **PDR3**, colored blue, indicate PCI bus transactions, but that PCI bus transaction is conveyed at a

different time over **the second LVDS channel**, and all of the data lines PD0 through PDR3 are utilized for that PCI bus transaction.



(Corresponding to Figure 6 of Chu330)

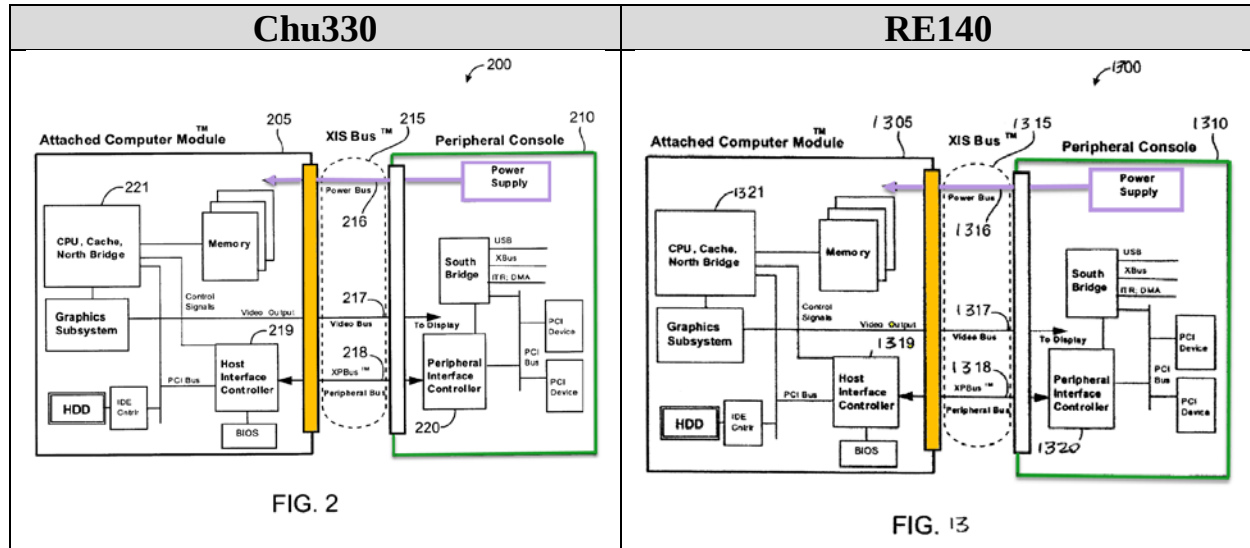


(Corresponding to Figure 23 of Chu330)

12. Claim 25

- i. [25] The method of claim 22 further comprising receiving power from the **connector** upon connection to an **external peripheral power supply**.

175. I explained above in [limitation 14e] how, as shown in Figure 2, Chu330 teaches a **connector** that connects a computer (ACM 205) and console (**peripheral console (PCON) 210**). Ex. 1003 [Chu330] at Figure 2. Chu330 in Figure 2 also shows a “**power supply**” that is located within the **peripheral console**. Ex. 1003 [Chu330] at Figure 2. Chu330 explains that the “**power bus 216** transmits power between ACM 205 and **peripheral console 210**.” Ex. 1003 [Chu330] at 5:12-13; *see also* Ex. 1003 [Chu330] at claim 1. As seen in Figure 2, this transmission of power occurs from the **connector**. Ex. 1003 [Chu330] at Figure 2. More specifically, Chu330 describes the connector as including pins for power related signals. *See* Ex. 1003 [Chu330] at 13:27-31 (explaining that the **connector** “may include pins for transmitting video and/or **power** related signals in addition to the PCI related signals, in which case, the cable would have conductive lines for the video bus and/or **power bus**.”). Additionally, Chu330 in Figure 28 shows pins V9-V18 (GND), V33 (3.3 volts), V5 (5.0 volts), and V12 (12 volts). Ex. 1003 [Chu330] at Figure 28; *see also* Ex. 1003 [Chu330] at 3:34-37, 3:55-59, 13:38-62, 17:42-67, Figures 17-19, and Figures 27 and 29-30.



13. Claim 26

i. [26pre] A method of improving performance of a computer, comprising:

176. I explained above in [preamble 14pre] how Chu330 teaches this preamble.

ii. [26a] obtaining an **integrated Central Processing Unit (CPU) with a graphics controller in a single chip**,

177. I explained above in [limitation 14a] how Chu330 in combination with Cupps renders obvious this limitation.

- iii. [26b] connecting a **Low Voltage Differential Signal (LVDS)** channel directly to the **integrated CPU and graphics controller**, wherein the **LVDS channel** comprises two unidirectional, serial bit channels that transmit data in opposite directions,

178. I explained above in [limitation 14f and claim 17] how Chu330 in combination with Cupps renders obvious this limitation.

- iv. [26c] conveying Universal Serial Bus (USB) protocol information through the **LVDS channel**;

179. I explained above in [claim 15] how Chu330 teaches this limitation.

- v. [26d] connecting a **Differential Signal channel** directly to the **integrated CPU and graphics controller** to output **video data**, and

180. I explained above in [claim 14b] how Chu330 teaches this limitation.

- vi. [26e] connecting **memory** directly to the **integrated CPU and graphics controller**.

181. I explained above in [claim 14d] how Chu330 in combination with Cupps renders obvious this limitation.

14. Claim 27

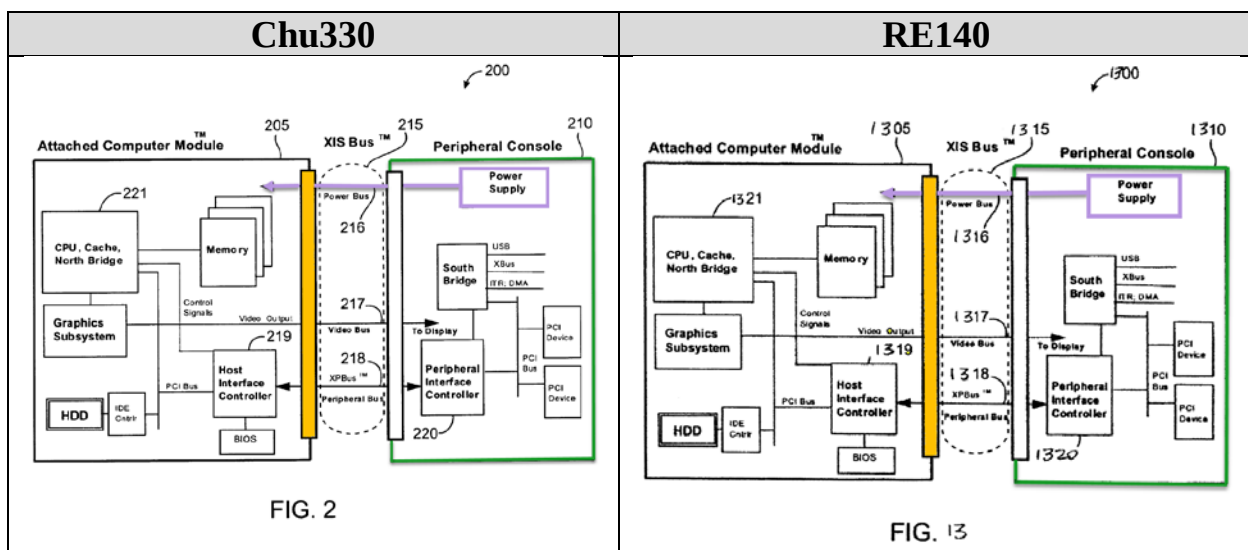
- i. [27] The method of claim 26 further comprising conveying Transition Minimized Differential Signaling (TDMS) signals through the **Differential Signal channel**.

182. I explained above in [limitations 14b and 14c] how Chu330 teaches this limitation.

15. Claim 28

- i. [28] The method of claim 26 further comprising providing a **connector** for the computer for connection to a **console** with a **power supply**.

183. I explained above in [limitation 14e and claim 25] how Chu330 teaches this limitation. As explained previously and as shown in Figure 2 of Chu330 below, the **power supply** is in the **console**.



16. Claim 29

- i. [29a] The method of claim 26 further comprising providing a connector for the computer for connection to a console, and**

184. I explained above in [preamble 14e] how Chu330 teaches this preamble.

- ii. [29b] coupling Universal Serial Bus (USB) protocol information from the LVDS channel to the console.**

185. I explained above in [limitations 14e and 14f, claim 15, and limitation 18e] how Chu330 in combination with Cupps renders obvious this limitation.

17. Claim 30

- i. [30pre] A method of improving performance of a computer, comprising:**

186. I explained above in [preamble 14pre] how Chu330 teaches this preamble.

- ii. [30a] obtaining an integrated Central Processing Unit (CPU) with a graphics controller in a single chip,**

187. I explained above in [limitation 14a] how Chu330 in combination with Cupps renders obvious this limitation.

- iii. [30b] connecting a **Low Voltage Differential Signal (LVDS) channel** directly to the **integrated CPU and graphics controller**, wherein the **LVDS channel** comprises two unidirectional, serial bit channels that transmit data in opposite directions,

188. I explained above in [limitation 14f, claim 17, and limitation 22b] how Chu330 in combination with Cupps renders obvious this limitation. My analysis regarding the **first LVDS channel** and **second LVDS channel** also applies to an **LVDS channel**.

- iv. [30c] conveying serially encoded address and data of a **Peripheral Component Interconnect (PCI) bus transaction through the LVDS channel**;

189. I explained above in [claim 16] how Chu330 teaches this limitation.

- v. [30d] connecting a **Differential Signal channel** directly to the **integrated CPU and graphics controller** to output **video data**, and

190. I explained above in [claim 14b] how Chu330 in combination with Cupps renders obvious this limitation.

- vi. [30e] connecting **memory** directly to the **integrated CPU and graphics controller**.

191. I explained above in [claim 14d] how Chu330 in combination with Cupps renders obvious this limitation.

18. Claim 31

- i. [31a] The method of claim 30 further comprising providing a connector for the computer for connection to a console, and**

192. I explained above in [14e] how Chu330 teaches this limitation.

- ii. [31b] providing a second LVDS channel that couples to the connector, the second LVDS channel comprising two unidirectional, serial bit channels that transmit data in opposite directions.**

193. I explained above in [limitation 14f, claim 17, and limitation 22e] how Chu330 teaches this limitation. My analysis regarding the first LVDS channel also applies to a second LVDS channel.

19. Claim 32

- i. [32] The method of claim 31 further comprising conveying serially encoded address and data of a Peripheral Component Interconnect (PCI) bus transaction to the console through the second LVDS channel and the connector.**

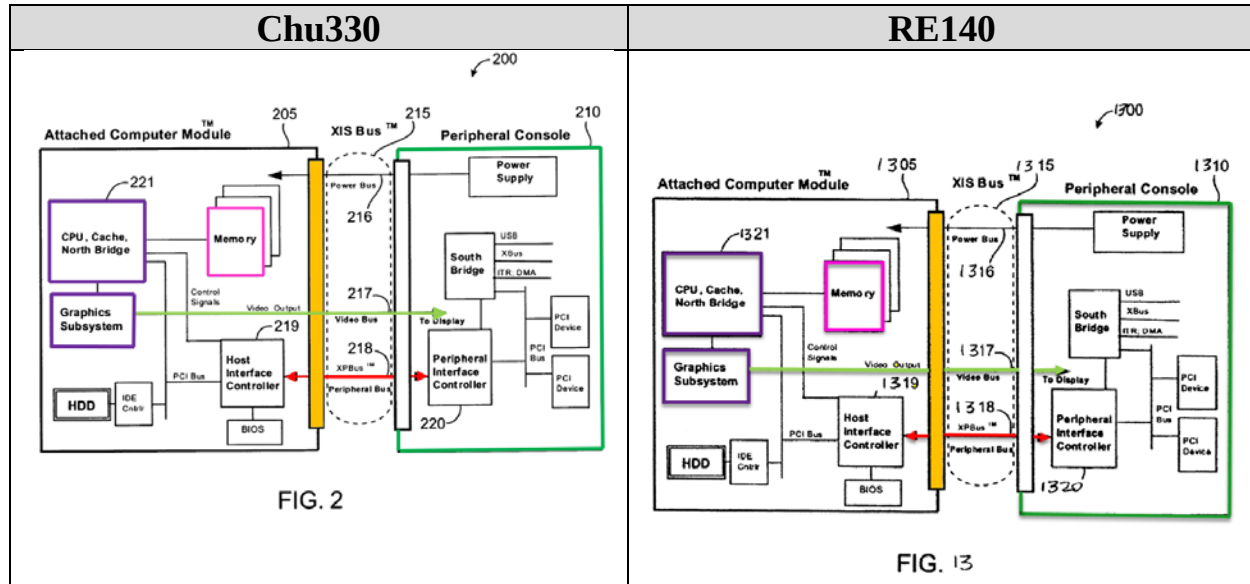
194. I explained above in [limitations 16 and 24] how Chu330 teaches conveying serially encoded address and data of a Peripheral Component Interconnect (PCI) bus transaction through the second LVDS channel. I further explained above [limitations 14e, 14f, and 17] how Chu330 teaches that the second

LVDS channel—as part of the XPBus—conveys data to the **console** through the **connector**. This is further shown in Chu330's Figure 2.

20. Claim 33

- i. **[33] The method of claim 32 further comprising conveying video data to the console through the connector.**

195. I explained above in [limitation 14b and 14c] how, with regard to Figure 2, Chu330 teaches a **video bus** that outputs **video data** on a **differential signal channel**. See Ex. 1003 [Chu330], Figure 2. Chu330 in Figure 2 also shows that the **video bus** outputs **video data** through the **connector** before reaching the **console**. See Ex. 1003 [Chu330], Figure 2. Specifically, Chu330 explains that “[t]he ACM 205 and the **peripheral console 210** are interfaced through an exchange interface system (XIS) bus 215 [and that the] XIS bus 215 includes, power bus 216, **video bus 217** and peripheral bus (XPBus) 218, which also herein referenced to as an interface channel.” Ex. 1003 [Chu330], 6:7-11.



21. Claim 34

- i. [34] The method of claim 31 further comprising conveying Universal Serial Bus (USB) protocol information to the console through the second LVDS channel and the connector.

196. I explained above in [limitations 15 and 20] how Chu330 teaches conveying USB protocol information through the second LVDS channel. I further explained above [limitations 14e and 17] how Chu330 teaches that the second LVDS channel—as part of the XDBus—conveys data to the console through the connector. This is further shown in Chu330's Figure 2.

22. **Claim 35**

- i. **[35pre] A method of improving performance of a computer, comprising:**

197. I explained above in [preamble 14pre] how Chu330 teaches this preamble.

- ii. **[35a] obtaining an integrated Central Processing Unit (CPU) with a graphics controller in a single chip,**

198. I explained above in [limitation 14a] how Chu330 in combination with Cupps renders obvious this limitation.

- iii. **[35b] connecting a first Low Voltage Differential Signal (LVDS) channel directly to the integrated CPU and graphics controller, wherein the first LVDS channel comprises two unidirectional, serial bit channels that transmit data in opposite directions,**

199. I explained above in [limitations 14f, claim 17, and limitation 22b] how Chu330 in combination with Cupps renders obvious this limitation.

- iv. **[35c] connecting a Differential Signal channel directly to the integrated CPU and graphics controller to output video data;**

200. I explained above in [limitation 14b] how Chu330 in combination with Cupps renders obvious this limitation.

- v. [35d] providing a **connector** for the computer for connection to an **external peripheral**; and

201. I explained above in [limitations 14e and 22d] how Chu330 teaches this limitation.

- vi. [35e] providing a **second LVDS channel** to couple to the **connector**, the **second LVDS channel** comprising two unidirectional, serial bit channels that transmit data in opposite directions.

202. I explained above in [limitation 14f, claim 17, and limitation 22e] how Chu330 teaches this limitation.

23. Claim 36

- i. [36] The method of claim 35 further comprising conveying Universal Serial Bus (USB) protocol information to the **external peripheral** through the **second LVDS channel** and the **connector**.

203. I explained above in [limitations 14e and 14f; claims 15, 17, and 20; limitation 22d; and claim 34] how Chu330 teaches this limitation.

204. Specifically, I explained above in [limitations 15 and 20] how Chu330 teaches conveying USB protocol information through the **second LVDS channel**. I further explained above [limitations 14e, 17, and 22d] how Chu330 teaches that the **second LVDS channel**—as part of the XPBus—conveys data to the **external peripheral** through the **connector**. This is further shown in Chu330's Figure 2.

24. Claim 37

- i. **[37] The method of claim 35 further comprising conveying Universal Serial Bus (USB) protocol information through the first LVDS channel.**

205. I explained above in [claim 15] how Chu330 teaches this limitation.

25. Claim 38

- i. **[38] The method of claim 35 further comprising conveying Transition Minimized Differential Signaling (TDMS) signals through the Differential Signal channel.**

206. I explained above in [limitations 14b and 14c] how Chu330 teaches this limitation.

X. Conclusion

207. In my opinion, claims 14-38 of the RE140 are obvious in light of the prior art references.

XI. Availability for Cross-Examination

208. In signing this declaration, I recognize that the declaration will be filed as evidence in a proceeding before the Patent Trial and Appeal Board of the United States Patent and Trademark Office. I also recognize that I may be subject to cross-examination in the proceeding and that cross-examination will take place

within the United States. If cross-examination is required of me, I will appear for cross-examination within the United States during the time allotted for cross-examination.

XII. Right to Supplement

209. I reserve the right to supplement my conclusions and analysis in the future to respond to any arguments that the Patent Owner may raise and to take into account new information as it becomes available to me.

XIII. Jurat

210. I declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code.

Dated: June 24, 2021



Bill Lin

APPENDIX A

BILL LIN
Curriculum Vitae
Tel: 858.531.2441
Email: billmbox@gmail.com

EDUCATION

- **Ph.D.**, Electrical Engineering and Computer Sciences
University of California, Berkeley, May 1991
- **Masters of Science**, Electrical Engineering and Computer Sciences
University of California, Berkeley, May 1988
- **Bachelor of Science**, Electrical Engineering and Computer Sciences
University of California, Berkeley, May 1985

PROFESSIONAL EXPERIENCE

- | | |
|------------------|---|
| 1/1997 – present | University of California, San Diego
Department Chair, Electrical and Computer Engineering
Professor, Electrical and Computer Engineering |
| 2/1992 – 12/1996 | IMEC, Leuven, Belgium
Group Head, Systems Control and Communications Group |

AREAS OF EXPERTISE

- All aspects of computer architecture and computer network problems, including the design of heterogeneous multicore processors, systems-on-chips, data networks, wireless communications and mobile computing systems, and multimedia and graphics systems.

PROFESSIONAL ACTIVITIES

- Served or serving as Editor on 3 ACM or IEEE journals, as General Chair on 4 ACM or IEEE conferences, on the Organizing or Steering Committees for 6 ACM or IEEE conferences, and on the Technical Program Committees of 45 ACM or IEEE conferences.

SELECTED PROFESSIONAL ACTIVITIES

- Associate Editor, ACM Transactions on Design Automation and Electronics Systems (TODAES), 2010-2015
- Editorial Board, International Journal of Embedded Systems, 2003-present
- General Chair, ACM/IEEE Symposium on Networks-on-Chips (NOCS), 2009
- General Chair, ACM/IEEE Symposium on Architectures for Networking and Communications Systems (ANCS), 2010
- Chair of Steering Committee, ACM/IEEE Symposium on Architectures for Networking and Communications Systems (ANCS), 2012-present
- Guest Editor, IEEE Transactions on Network and Service Management (TNSM), 2012-2013
- General Co-Chair, ACM SIGMETRICS, 2015
- General Chair, ACM/IEEE International Symposium on Quality-of-Service (IWQoS), 2011
- Steering Committee, ACM/IEEE International Symposium on Quality-of-Service (IWQoS), 2011-present

PUBLICATIONS

- Published over 190 journal articles and conference papers in top-tier venues and publications.

PATENTS

- Mitigating Low-Rate Denial-of-Service Attacks in Packet-Switched Networks. United States Patent 8,443,444. Issued in May 14, 2013.
- Systems and Methods for Proactive Surge Protection. United States Patent 7,860,004. Issued in December 28, 2010.
- Method and Apparatus for Scan Block Caching. United States Patent 7,672,005. Issued in March 2, 2010.
- Design Environment and a Design Method for Hardware/Software Co-Design. United States Patent 5,870,588. Issued in February 9, 1999.
- System and Method for Generating a Hazard-Free Asynchronous Circuit. United States Patent 5,748,487. Issued in May 5, 1998.

EXPERT WITNESS HISTORY (BILL LIN)

I have served as an expert witness on 29 matters (most matters involved multiple patents in suit), of which I wrote expert reports or declarations for 18 matters, analyzed source code in 13 cases, was deposed 19 times, and testified at trial 3 times. The specific matters and services provided are as follows:

1. Vizio, Inc. v. LG Electronics, Inc. and LG Electronics USA Inc., Civil Action No. 09-cv-1481-BEL
 - Expert witness on behalf of Vizio, Inc.
 - Law firm: Jones Day.
 - Services provided: Provided expert report, analyzed source code.
 - Technologies: Digital TV.
2. Vizio Inc. v. LG Electronics, Inc. and LG Electronics USA Inc., In the Matter of CERTAIN FLAT PANEL DIGITAL TELEVISIONS AND COMPONENTS THEREOF, U.S. International Trade Commission Inv. No. 337-TA-733
 - Expert witness on behalf of Vizio, Inc.
 - Law firm: Jones Day.
 - Services provided: Provided expert report, analyzed source code.
 - Technologies: Digital TV.
3. Vizio Inc. v. Coby Electronics Corp., Curtis International Ltd., E&S International Enterprises, Inc., MStar Semiconductor, Inc., ON Corp US, Inc., Renesas Electronics Corporation, Japan, Renesas Electronics America, Inc., Sceptre, Inc., and Westinghouse Digital, LLC, In the Matter of CERTAIN DIGITAL TELEVISIONS AND COMPONENTS THEREOF, U.S. International Trade Commission Inv. No. 337-TA-789
 - Expert witness on behalf of Vizio, Inc.
 - Law firm: Jones Day.
 - Services provided: Provided expert reports, was deposed, analyzed source code.
 - Technologies: Digital TV.
4. Linex Technologies Inc. v. Hewlett-Packard Company, Apple Inc., Aruba Networks, Inc., Meru Networks, and Ruckus Wireless, In the Matter of CERTAIN WIRELESS COMMUNICATION DEVICES AND SYSTEMS, COMPONENTS THEREOF, AND PRODUCTS CONTAINING SAME, U.S. International Trade Commission Inv. No. 337-TA-775
 - Expert witness on behalf of Hewlett-Packard Company, Apple Inc., Aruba Networks, Inc., Meru Networks, and Ruckus Wireless
 - Law firms: Covington & Burling, K&L Gates, Morrison & Foerster, Lewis Roca & Rothgerber.
 - Services provided: Provided expert reports, was deposed, analyzed source code.
 - Technologies: WiFi networks.
5. MOSAID Technologies, Inc. v. Dell, Inc., Qualcomm Atheros, Inc., et al., Case No. 2:11-cv-00179-TJW
 - Expert witness on behalf of Qualcomm Atheros, Inc.
 - Law Firm: McDermott Will & Emory.
 - Services provided: Provided expert analysis.
 - Technologies: WiFi networks.
6. Hitachi Consumer Electronics Co. Ltd., et al. v. Top Victory Electronics (Taiwan) Co. Ltd., et al., Civil Action No. 2:10-cv-260-JRG.
 - Expert witness on behalf of Vizio, Inc.
 - Law Firm: Akin Gump Strauss Hauer & Feld
 - Services provided: Provided expert reports, analyzed source code.
 - Technologies: Digital TV.

7. United States International Trade Commission (USITC) Investigation Number: 337-TA-853 and Technology Properties Limited, LLC v. Kyocera Corporation and Kyocera Communications, Inc. in the Northern District of California, Case No. 3:12-cv-03860-JSC
 - Expert witness on behalf of Kyocera Corporation and Kyocera Communications.
 - Law firm: Morrison & Foerster.
 - Services provided: Provided expert analysis.
 - Technologies: Cell phones, microprocessors.
8. Netgear, Inc. v. Ruckus Wireless, Inc., Case No. 1:10-cv-00999-SLR / D. Del.
 - Expert witness on behalf of Ruckus Wireless, Inc.
 - Law firms: Lewis Roca & Rothgerber, Orrick.
 - Services provided: Provided expert report, analyzed source code, was deposed, and testified at trial.
 - Technologies: WiFi networks.
9. Sonics, Inc. v. Arteris, Inc., Case No. 11 CV-05311 SBA, and Arteris S.A.S. v. Sonics, Inc., Case No. C 12-00434 (WHA)
 - Expert witness on behalf of Arteris, Inc. and Arteris S.A.S.
 - Law firm: DLA Piper.
 - Services provided: Retained as an expert.
 - Technologies: Systems-on-Chips (SoCs).
10. Linx Technologies Inc. v. Hewlett-Packard Company, Apple Inc., Aruba Networks, Inc., Meru Networks, and Ruckus Wireless, U.S. District Court, Northern District of California, C 13-00159 CW
 - Expert witness on behalf of Hewlett-Packard Company, Apple Inc., Aruba Networks, Inc., Meru Networks, and Ruckus Wireless
 - Law firms: Covington & Burling, Milbank, K&L Gates, Morrison & Foerster, Lewis Roca & Rothgerber.
 - Services provided: Provided expert reports, analyzed source code.
 - Technologies: WiFi networks.
11. Frontier Communications Corp. v. Google, C.A. No. 10-545 (D. Del)
 - Expert witness on behalf of Frontier Communications Corp.
 - Law firm: Steese, Evans & Frankel
 - Services provided: Provided source code analysis.
 - Technologies: Voice over IP.
12. U.S. Ethernet Innovations LLC v. Acer, Inc. et al., Case No. 10-cv-3724 (N.D. Cal.)
 - Expert witness on behalf of Qualcomm Atheros, Inc., Sigma Designs, Inc., and AT&T Services, Inc.
 - Law firms: Reed Smith LLP, Pillsbury Winthrop Shaw Pittman LLP, and Vinson & Elkins LLP.
 - Services provided: Provided expert reports, was deposed, analyzed source code.
 - Technologies: Intelligent network interfaces, data center networks.
13. Inter Partes Review of U.S. Patents.
 - Expert witness on behalf of Netgear, Inc. and Belkin International, Inc.
 - Law firm: Reed Smith LLP.
 - Services provided: Provided declaration for IPR petition.
 - Technologies: Wireless networks.
14. Inter Partes Review of U.S. Patents.
 - Expert witness on behalf of Arista Networks.
 - Law firm: Fish & Richardson.
 - Services provided: Provided declarations for IPR petitions, deposed 3 times.
 - Technologies: Network routers, data center networks.

15. Invalidity Expert Witness.
 - Expert witness on behalf of Intel Corp.
 - Law firm: Wilmer Cutler Pickering Hale and Dorr LLP.
 - Services provided: Provided expert analysis.
 - Technologies: WiFi networks, bluetooth networks.
16. Parthenon Unified Memory Architecture LLC v. HTC Corporation et al., Case No. 2:14-CV-690-JRG-RSP (E. D. Texas).
 - Expert witness on behalf of HTC Corporation and HTC America, Inc.
 - Law firm: Sidley Austin LLP.
 - Services provided: Retained as an expert.
 - Technologies: Memory architectures.
17. System Architecture Information Technology dba SAI Technology, Inc. v. Qualcomm Inc.
 - Expert witness on behalf of Qualcomm Inc.
 - Law firm: McDermott Will & Emory.
 - Services provided: Retained as an expert, provided reports, analyzed source code, was deposed, and testified at trial.
 - Technologies: WiFi networks.
18. Inter Partes Review of U.S. Patents.
 - Expert witness on behalf of Sandvine Corp.
 - Law firm: Erise IP.
 - Services provided: Provided declarations.
 - Technologies: Network monitoring and measurements.
19. Inter Partes Review of U.S. Patents.
 - Expert witness on behalf of Intel Corp., Cavium Inc., and Dell Inc.
 - Law firms: Weil, Gotshal & Manges LLP, Duane Morris LLP, Alston & Bird LLP.
 - Services provided: Provided declarations for IPR petitions, deposed 3 times.
 - Technologies: Intelligent network interfaces, data center networks, memory management.
20. Expert Witness.
 - Law firm: Covington & Burling.
 - Services provided: Retained as an expert.
 - Technologies: WiFi networks.
21. Qualcomm Inc. v. Apple Inc., Inv. No. 337-TA-1065 (ITC)
 - Expert witness on behalf of Apple Inc. and Intel Corp.
 - Law firm: Wilmer Cutler Pickering Hale and Dorr LLP.
 - Services provided: Provided expert reports/declarations, analyzed source code, was deposed.
 - Technologies: Mobile systems, application and modem processors, inter-processor communications, embedded software, processor and bus power management, memory management.
22. Qualcomm Inc. v. Apple Inc., Civ. Action No. 3:17-cv-01375-JAH-MDD (S.D. Cal.)
 - Expert witness on behalf of Apple Inc. and Intel Corp.
 - Law firm: Wilmer Cutler Pickering Hale and Dorr LLP.
 - Services provided: Provided expert reports/declarations, analyzed source code, deposed 2 times, and testified at trial.
 - Technologies: Mobile systems, application and modem processors, inter-processor communications, embedded software, processor and bus power management, memory management.

23. Inter Partes Review of U.S. Patents.
- Expert witness on behalf of Panasonic Avionics Corp.
 - Law firm: Haynes and Boone LLP.
 - Services provided: Provided declarations for IPR petitions.
 - Technologies: Network security.
24. Inter Partes Review of U.S. Patents.
- Expert witness on behalf of Intel Corp.
 - Law firm: Wilmer Cutler Pickering Hale and Dorr LLP.
 - Services provided: Provided declarations for IPR petitions, deposed 4 times.
 - Technologies: Mobile systems, application and modem processors, inter-processor communications, embedded software, power management, memory management.
25. Expert Witness.
- Law firm: Wilmer Cutler Pickering Hale and Dorr LLP.
 - Services provided: Retained as an expert.
 - Technologies: Inter-processor communications and security.
26. Bell Northern Research LLC v. Coolpad Technologies, Inc. et al., Civil Action No. 3:18-cv-01783-CAB-BLM (S.D. Cal.)
- Expert witness on behalf of Coolpad Technologies, Inc. and Yulong Computer Communications
 - Law firm: Perkins Coie LLP.
 - Services provided: Provided expert reports, analyzed source code, deposed.
 - Technologies: Processors, wireless communications, power management.
27. Inter Partes Review of U.S. Patents.
- Expert witness on behalf of Google LLC.
 - Law firm: Paul Hastings LLP.
 - Services provided: Provided declarations for IPR petitions.
 - Technologies: Computer networks, wireless communications.
28. Expert Witness.
- Law firm: Morgan, Lewis & Bockius LLP.
 - Services provided: Retained as an expert.
 - Technologies: Networking and communications.
29. Expert Witness.
- Law firm: Desmarais LLP.
 - Services provided: Retained as an expert.
 - Technologies: Computer systems.