IN THE SPECIFICATION:

Please replace the paragraph previously added at col. 1, line 6 with the following paragraph:

Notice: More than one reissue application has been filed for the reissue of U.S. Patent No. 6,643,777. The reissue applications are U.S. Application Nos. 11/056,604 (a parent reissue application), 11/545,056 (which is a continuation reissue of the parent reissue application), and 12/561,138 (the present application, which is a continuation reissue of the parent reissue application).

This application is a continuation reissue of U.S. Application No. 11/056,604, which is a reissue of U.S. Patent No. 6,643,777, which are incorporated herein by reference.

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Intel Corporation v. ACQIS LLC Intel Corp.'s Exhibit 1009 Vol 2 of 2 Ex. 1009, Page 252

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IN THE CLAIMS:

1-13. (Cancelled)

14. (Amended) <u>A system for information transaction, the system comprising:</u> <u>a console comprising</u>

a low voltage differential signal channel comprising two sets of unidirectional, multiple serial bit channels to transmit data in opposite directions,

an interface controller coupled to the low voltage differential signal channel to communicate an encoded serial bit stream of Peripheral Component Interconnect bus transaction.

a power supply, and

a hard disk drive housed in the console; and

a computer module coupled to the console, the computer module comprising

a central processing unit,

a mass storage device coupled to the central processing unit, and

a security mechanism to provide access protection for the computer module,

wherein the computer module is configured to receive power from the power supply.

15. (Previously Presented) <u>The system of claim 14</u>, wherein the computer module further comprises a computing environment for a user.

16. (Previously Presented) <u>The system of claim 14</u>, wherein the computer module is coupled to the console through serial bit stream data paths employing low voltage differential signaling.

17. (Amended) <u>A system for information transaction, the system comprising:</u> a console comprising

an integrated Liquid Crystal Display and

a low voltage differential signal channel comprising two sets of unidirectional, multiple serial bit channels to communicate an encoded serial bit stream of Peripheral Component Interconnect bus transaction in opposite directions; and

a computer module coupled to the console in a "plug and play" operation, the computer module comprising

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a central processing unit,

a mass storage device coupled to the central processing unit, and

an interface controller to communicate a differential signaling serial bit stream with the console.

18. (Previously Presented) <u>The system of claim 17, wherein the computer module further</u> comprises a computing environment for a user.

19. (Previously Presented) <u>The system of claim 17</u>, wherein the computer module further comprises a hardware dependent security code to perform security identification matching.

20. (Amended) <u>A system for information transaction, the system comprising:</u> a console comprising

a power supply,

<u>a first low voltage differential signal channel comprising two sets of</u> unidirectional, serial bit channels to transmit data in opposite directions, and

a removable media drive housed in the console; and

a computer module coupled to the console, the computer module comprising

a central processing unit,

a mass storage device coupled to the central processing unit,

<u>a second low voltage differential signal channel comprising two sets of</u> unidirectional, serial bit channels to transmit data in opposite directions, and

an interface controller coupled to the console through the second low voltage differential signal channel,

wherein the computer module is configured to receive power from the power supply.

21. (Amended) <u>The system of claim 20</u>, wherein the first low voltage differential signal channel and the second low voltage differential signal channel are configured to transmit data in 10-bit packets.

22. (Previously Presented) <u>The system of claim 20</u>, wherein the computer module further comprises a computing environment for a user.

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23. (Amended) <u>The system of claim 20, wherein the first low voltage differential signal</u> channel is coupled to the second low voltage differential signal channel upon coupling of the computer module to the console.

24. (Amended) <u>A system to connect a computer module to a network, the system comprising:</u> a console comprising

a power supply,

<u>a low voltage differential signal channel comprising two sets of unidirectional,</u> <u>multiple serial bit channels to communicate an encoded serial bit stream of Peripheral</u> Component Interconnect bus transaction in opposite directions, and

an Ethernet controller to provide access to a network; and

a computer module coupled to the console and powered by the power supply, the computer module comprising

a central processing unit,

a mass storage device coupled to the central processing unit, and

a connection software code,

wherein, upon coupling to the console, the computer module is configured to establish a connection to the network using the connection software code.

25. (Previously Presented) <u>The system of claim 24</u>, wherein the computer module is coupled to the console in a "plug and play" operation.

26. (Previously Presented) <u>The system of claim 24, wherein the computer module further</u> comprises a computing environment for a user.

27. (Previously Presented) <u>An information transaction system comprising:</u> <u>a console comprising</u>

an integrated keyboard,

an integrated Liquid Crystal Display,

a low voltage differential signal channel comprising two sets of unidirectional, serial bit channels to transmit data in opposite directions, and

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an interface controller coupled to the low voltage differential signal channel to communicate an encoded serial bit stream of Peripheral Component Interconnect bus transaction; and

a computer module coupled to the console in a "plug and play" operation, the computer module comprising

a central processing unit and

a mass storage device comprising a flash memory.

28. (Previously Presented) <u>The system of claim 27</u>, wherein the central processing unit comprises an integrated circuit chip to operate on a varying clock frequency to vary a power consumption of the integrated circuit chip while in operation.

29. (Previously Presented) <u>The system of claim 27</u>, wherein the computer module further comprises a computing environment for a user.

30. (Previously Presented) <u>The system of claim 27</u>, wherein the interface controller is a first interface controller, and the computer module further comprises a second interface controller coupled to the low voltage differential signal channel to communicate a serial bit stream to the console.

31. (Amended) <u>A system for information transaction, the system comprising:</u> <u>a console comprising</u>

an integrated keyboard,

an integrated Liquid Crystal Display, and

<u>a first low voltage differential signal channel comprising two sets of</u> unidirectional, serial bit channels to transmit data in opposite directions; and

a computer module coupled to the console, the computer module comprising

a central processing unit,

a mass storage device comprising a flash memory,

a second low voltage differential signal channel comprising two sets of unidirectional, serial bit channels to transmit data in opposite directions, and

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an interface controller coupled to the console through the second low voltage differential signal channel,

wherein the first low voltage differential signal channel is coupled to the second low voltage differential signal channel upon coupling of the computer module to the console.

32. (Previously Presented) <u>The system of claim 31</u>, wherein the computer module further comprises a security program to specify a security identification.

33. (Previously Presented) <u>The system of claim 31</u>, wherein the computer module further comprises a computing environment for a user.

34. (Amended) <u>An information transaction system comprising:</u>

a console comprising

<u>a power supply,</u>

<u>a first low voltage differential signal channel comprising two sets of</u> <u>unidirectional, serial bit channels to transmit data in opposite directions, and</u>

a removable media drive housed in the console; and

a computer module coupled to the console, the computer module comprising

a central processing unit,

a flash memory comprising a security identification to provide access protection for the computer module,

a second low voltage differential signal channel comprising two sets of unidirectional, serial bit channels to transmit data in opposite directions, and

an interface controller coupled to the console through the second low voltage differential signal channel,

wherein the computer module is configured to receive power from the power supply.

35. (Previously Presented) <u>The system of claim 34</u>, wherein the computer module further comprises a computing environment for a user.

36. (Amended) The system of claim 34, wherein the first low voltage differential signal channel is coupled to the second low voltage differential signal channel upon coupling of the computer module to the console.

37. (Amended) <u>A method to connect a computer module to a network, the method</u> comprising:

providing a computer module, the computer module comprising (a) a central processing unit and (b) a storage device comprising a connection program;

inserting the computer module into a computer console in a "plug and play" operation, the computer console comprising (a) a low voltage differential signal channel comprising two sets of unidirectional, multiple serial bit channels to communicate an encoded serial bit stream of Peripheral Component Interconnect bus transaction in opposite directions and (b) a networking device to provide access to an external network;

receiving connection information from the computer console to the computer module; and

using the connection program, establishing a connection between the computer module and the external network.

38. (Previously Presented) <u>The method of claim 37, further comprising coupling the</u> computer module to the low voltage differential signal channel.

39. (Previously Presented) <u>The method of claim 37</u>, wherein establishing the connection between the computer module and the external network comprises communicating with the external network through Ethernet.

40. (Amended) <u>A computer system comprising:</u>

a console comprising

a power supply and

<u>a first low voltage differential signal channel comprising two sets of</u> <u>unidirectional, serial bit channels to transmit data in opposite directions; and</u>

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a computer module coupled to the console, the computer module comprising

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a central processing unit to operate on a varying clock frequency to vary a power consumption of the central processing unit while in operation,

a mass storage unit coupled to the central processing unit,

<u>a second low voltage differential signal channel comprising two sets of</u> unidirectional, serial bit channels to transmit data in opposite directions, and

an interface controller coupled to the console through the second low voltage differential signal channel,

wherein the computer module is configured to receive power from the power supply.

41. (Previously Presented) <u>The computer system of claim 40</u>, wherein the computer module further comprises a computing environment for a user.

42. (Amended) <u>The computer system of claim 40</u>, wherein the first low voltage differential signal channel is coupled to the second low voltage differential signal channel upon coupling of the computer module to the console for data communication.

43. (Previously Presented) <u>The computer system of claim 40</u>, wherein the computer module is configured for insertion into the console as a "plug and play" operation.

44. (Amended) <u>A system to connect a computer module to a network, the system comprising:</u> a console comprising

a power supply and

a connection to a network; and

a computer module coupled to the console in a "plug and play" operation, the computer module comprising

a processing unit,

<u>a low voltage differential signal channel comprising two sets of unidirectional,</u> multiple serial bit channels to transmit data in opposite directions,

an interface controller coupled to the low voltage differential signal channel to communicate an encoded serial bit stream of Peripheral Component Interconnect bus transaction, and

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a mass storage device comprising a connection program,

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wherein the computer module is configured to receive power from the power supply, and the connection program is configured to establish communication with the network through the console.

45. (Previously Presented) <u>The system of claim 44, wherein the processing unit comprises an</u> integrated circuit chip to operate on a varying clock frequency to vary a power consumption of the integrated circuit chip while in operation.

46. (Previously Presented) <u>The system of claim 44</u>, wherein the connection to the network comprises an Ethernet connection.

47. (Previously Presented) <u>The system of claim 44</u>, wherein the computer module further comprises a computing environment for a user.

48. (Amended) <u>A computer system comprising:</u>

a console comprising a power supply; and

a computer module coupled to the console, the computer module comprising

a central processing unit,

a low voltage differential signal channel comprising two sets of unidirectional, multiple serial bit channels to transmit data in opposite directions,

an interface controller coupled to the low voltage differential signal channel to communicate an encoded serial bit stream of Peripheral Component Interconnect bus transaction, and

a mass storage device coupled to the central processing unit,

wherein the computer module is configured to receive power from the power supply, and the computer module is configured to communicate, through Ethernet, to a local area network upon coupling of the computer module to the console.

49. (Previously Presented) <u>The computer system of claim 48, wherein the computer module</u> is configured for insertion into the console as a "plug and play" operation.

50. (Previously Presented) <u>The computer system of claim 48</u>, wherein the mass storage device is a first mass storage device, and the console further comprises a second mass storage device coupled to the computer module and configured to receive power from the power supply.

51. (Previously Presented) <u>The computer system of claim 48</u>, wherein the central processing unit is configured to operate on a varying clock frequency to vary a power consumption of the central processing unit while in operation.

52. (Amended) <u>A computer system comprising:</u>

a console comprising a power supply; and

a computer module coupled to the console, the computer module comprising

a central processing unit to operate on a varying clock frequency to vary a power consumption of the central processing unit while in operation.

a low voltage differential signal channel comprising two sets of unidirectional, multiple serial bit channels to transmit data in opposite directions,

an interface controller coupled to the low voltage differential signal channel to communicate an encoded serial bit stream of Peripheral Component Interconnect bus transaction, and

a graphics controller coupled to the central processing unit,

wherein the computer module is configured to receive power from the power supply.

53. (Previously Presented) <u>The computer system of claim 52</u>, wherein the computer module further comprises a core computing environment for a user.

54. (Previously Presented) <u>The computer system of claim 52</u>, wherein the computer module is configured for insertion into the console as a "plug and play" operation.

55. (Amended) <u>A computer system for secured information transaction, the computer system</u> comprising:

a console to connect to a network;

a keyboard coupled to the console; and

a computer module coupled to the console, the computer module comprising

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a central processing unit,

<u>a low voltage differential signal channel comprising two sets of unidirectional,</u> <u>multiple serial bit channels to transmit data in opposite directions,</u>

an interface controller coupled to the low voltage differential signal channel to communicate an encoded serial bit stream of Peripheral Component Interconnect bus transaction, and

a mass storage unit storing a security program and a first user identification data,

wherein the security program is configured to receive a second user identification data via the keyboard, perform a comparison of the first user identification data and the second user identification data, and permit access to the computer module based on the comparison.

56. (Previously Presented) <u>The computer system of claim 55</u>, wherein the security program is further configured to identify a predetermined security status and control a level of access privilege to the computer module.

57. (Previously Presented) <u>The computer system of claim 55</u>, wherein the central processing unit is configured to operate on a varying clock frequency to vary a power consumption of the central processing unit while in operation.

58. (Amended) <u>An information system comprising</u>:

a console comprising

a power supply and

<u>a first low voltage differential signal channel comprising two sets of</u> unidirectional, serial bit channels to transmit data in opposite directions; and

a computer module coupled to the console, the computer module comprising

a central processing unit,

a mass storage device coupled to the central processing unit,

a graphics controller coupled to the central processing unit,

<u>a second low voltage differential signal channel comprising two sets of</u> unidirectional, serial bit channels to transmit data in opposite directions, and

an interface controller coupled to the console through the second low voltage differential signal channel,

wherein the computer module is configured to receive power from the power supply.

59. (Amended) <u>The information system of claim 58, wherein the first low voltage differential</u> <u>signal channel is coupled to the second low voltage differential signal channel for data</u> communication upon coupling of the computer module to the console.

60. (Previously Presented) <u>The information system of claim 58</u>, wherein the computer module is configured for insertion into the console as a "plug and play" operation.

REMARKS

Status of Claims and Support for Claim Changes

Claims 14-60 are pending in the subject reissue application. Claims 1-13 were previously cancelled. In accordance with this paper, Applicant is submitting the following amendments:

- Claim 14 is amended to specify two sets of unidirectional, "multiple" serial bit channels, which has support in the incorporated U.S. Patent No. 6,345,330 (the "330 patent") at FIG. 6, FIG. 11, FIG. 23, and col. 15, line 11 to col. 16, line 5.
- Claim 17 is amended to specify a low voltage differential signal channel "comprising two sets of unidirectional, multiple serial bit channels" to communicate an encoded serial bit stream of Peripheral Component Interconnect bus transaction "in opposite directions," and to delete reference to "via the low voltage differential signal channel," which has support in the incorporated '330 patent at FIG. 6, FIG. 11, FIG. 23, and col. 15, line 11 to col. 16, line 5.
- Claim 20 and its dependent claims 21 and 23 are amended to specify a first "low voltage" differential signal channel and a second "low voltage" differential signal channel, which has support in the incorporated '330 patent at FIG. 23, col. 2, lines 29-51, and col. 15, line 11 to col. 16, line 5.
- Claim 24 is amended to specify a low voltage differential signal channel "comprising two sets of unidirectional, multiple serial bit channels" to communicate an encoded serial bit stream of Peripheral Component Interconnect bus transaction "in opposite directions," which has support in the incorporated '330 patent at FIG. 6, FIG. 11, FIG. 23, and col. 15, line 11 to col. 16, line 5.
- Claim 31 is amended to specify a first "low voltage" differential signal channel and a second "low voltage" differential signal channel, which has support in the incorporated '330 patent at FIG. 23, col. 2, lines 29-51, and col. 15, line 11 to col. 16, line 5.
- Claim 34 and its dependent claim 36 are amended to specify a first "low voltage" differential signal channel and a second "low voltage" differential signal channel, which has support in the incorporated '330 patent at FIG. 23, col. 2, lines 29-51, and col. 15, line 11 to col. 16, line 5.

- Claim 37 is amended to specify a low voltage differential signal channel "comprising two sets of unidirectional, multiple serial bit channels" to communicate an encoded serial bit stream of Peripheral Component Interconnect bus transaction "in opposite directions" and "receiving" connection information (instead of "providing" connection information), which has support in the original U.S. Patent No. 6,643,777 (the "777 patent") at claim 11, as well as in the incorporated '330 patent at FIG. 6, FIG. 11, FIG. 23, and col. 15, line 11 to col. 16, line 5.
- Claim 40 and its dependent claim 42 are amended to specify a first "low voltage" differential signal channel and a second "low voltage" differential signal channel, which has support in the incorporated '330 patent at FIG. 23, col. 2, lines 29-51, and col. 15, line 11 to col. 16, line 5.
- Claims 44, 48, 52, and 55 are amended to specify two sets of unidirectional, "multiple" serial bit channels, which has support in the incorporated '330 patent at FIG. 6, FIG. 11, FIG. 23, and col. 15, line 11 to col. 16, line 5.
- Claim 58 and its dependent claim 59 are amended to specify a first "low voltage" differential signal channel and a second "low voltage" differential signal channel, which has support in the incorporated '330 patent at FIG. 23, col. 2, lines 29-51, and col. 15, line 11 to col. 16, line 5.

The foregoing amendments are made for the purposes of clarification and to expedite the prosecution of the subject reissue application. In accordance with 37 C.F.R. §1.173 and M.P.E.P. §1453 setting forth the manner of making amendments in reissue applications, the entire text of each pending claim is underlined to reflect additions relative to the original patent.

Claim Rejections

The Examiner has rejected claims 14-60 under 35 U.S.C. §251 as being broadened in a reissue application filed after two years from the grant of the original patent. Applicant respectfully traverses the rejections for at least the following reasons.

The subject reissue application is a continuation reissue of a parent reissue application no. 11/056,604 (the "604 reissue application"), for the reissue of the original '777 patent that was granted on November 4, 2003. Although the subject continuation reissue application was filed after the two year period from the grant of the original '777 patent, the parent '604 reissue application was filed within the two year period, namely on February 10, 2005.

The M.P.E.P. explicitly permits broadened claims to be presented in a continuation reissue application after the two year period, if an intent to broaden was indicated in a parent reissue application within the two year period. Specifically, the M.P.E.P. explains:

[A] broadened claim can be presented after two years from the grant of the original patent in a broadening reissue application which was filed within two years from the grant. Where *any* intent to broaden is >unequivocally< indicated in the reissue application within the two years from the patent grant, a broadened claim can subsequently be presented in the reissue after the two year period.... Thus, a broadened claim may be presented in a reissue application after the two years, even though the broadened claim presented after the two years is *different* than the broadened claim presented within the two years. *Finally, if intent to broaden is indicated in a parent reissue application within the two years, a broadened claim can be presented in a continuing (continuation or divisional) reissue application after the two year period*.

[M.P.E.P. §1412.03(IV) (emphasis added)]. The above-quoted passage from the M.P.E.P. does not distinguish between whether broadened claims are later presented in a first reissue application or in a continuation reissue application. In either scenario, if "any" intent to broaden is indicated within the two year period, broadened claims can be later presented, even if "different" than broadened claims presented within the two year period. Here, an intent to broaden was unequivocally indicated in the parent '604 reissue application at the time of filing and within the two year period, through a Reissue Declaration by the inventor and through the presentation of broadened claims in a Preliminary Amendment. [See, e.g., Reissue Declaration of the parent '604 reissue application executed on February 9, 2005 ("Elimination of the term 'predetermined' broadens the scope of the invention, as recited at least in new claim 14.")] Because an intent to broaden was indicated within the two year period, broadened claims in the subject continuation reissue application are permitted by the M.P.E.P., even if "different" than broadened claims in the parent '604 reissue application within the two year period.

The Board of Patent Appeals and Interferences ("BPAI") has recently articulated more stringent criteria for presentation of broadened claims in a continuation reissue application after the two year period. [See Decision on Appeal for reissue application no. 11/503,541 decided on April 26, 2010] Specifically, the BPAI noted that broadening is not permitted in a continuation reissue application after the two year period, if such later broadening is "unrelated" to, or would have been "unforeseeable" in view of, a broadening aspect identified within the two year period. [See Decision at pp. 14-29] Applicant does not concede as to the criteria articulated by the BPAI, given its apparent inconsistency with the above-quoted passage from the M.P.E.P., and

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given that the decision of the BPAI is currently on appeal before the Court of Appeals for the Federal Circuit. Nonetheless, even under the criteria articulated by the BPAI, broadening is permitted in the subject continuation reissue application, since the current broadening is related to, and would have been foreseeable in view of, broadening aspects identified in the parent '604 reissue application within the two year period.

Independent claims 14, 17, 20, 24, 27, 31, 34, 40, 44, 48, 52, 55, and 58 of the subject continuation reissue application are system claims, which are broadened in at least certain aspects relative to system claim 8 of the original '777 patent. Specifically, the system claims of the subject continuation reissue application do not explicitly specify a "peripheral" controller housed in a console. This same broadening aspect was indicated in the parent '604 reissue application within the two year period, through the presentation of broadened claims at the time of filing. For example, and like the system claims of the subject continuation reissue application, claim 16 (reproduced below) presented in the Preliminary Amendment of the parent '604 reissue application also does not explicitly specify a "peripheral" controller:

16. A system for secured information transactions, the system comprising:

a console comprising a network communication controller housed in the console; a user identification input device coupled to the console, the user identification input device being provided for user identification data; and

an attached computer module coupled to the console, the attached computer module comprising a mass storage unit, an interface controller coupled to the console, and a security memory device stored with the user identification data, wherein all data from the computer module passes through the interface controller to reach any device in the console.

Also, the system claims of the subject continuation reissue application do not explicitly specify an "user identification input device." Again, this same broadening aspect was indicated in the parent '604 reissue application within the two year period, through the presentation of broadened claims at the time of filing. For example, and like the system claims of the subject continuation reissue application, claim 37 (reproduced below) presented in the Preliminary Amendment of the parent '604 reissue application also does not explicitly specify an "user identification input device":

<u>37.</u> A system for information transactions, the system comprising: <u>a computer console comprising a network communication controller housed in the</u> <u>console; and</u>

an attached computer module coupled to the console, the attached computer module comprising a central processing unit, a graphics subsystem, and an interface controller coupled to the console, wherein all computer module data passes through the console.

In addition, the system claims of the subject continuation reissue application do not explicitly specify a "security memory device." Once again, this same broadening aspect was indicated in the parent '604 reissue application within the two year period, through the presentation of broadened claims at the time of filing. For example, and like the system claims of the subject continuation reissue application, claim 37 (reproduced above) of the parent '604 reissue application also does not explicitly specify a "security memory device."

Independent claim 37 of the subject continuation reissue application is a method claim, which is broadened in at least a certain aspect relative to method claim 11 of the original '777 patent. Specifically, claim 37 of the subject continuation reissue application does not explicitly specify "configuring the connection program to adapt to the connection information." This same broadening aspect was indicated in the parent '604 reissue application within the two year period, through the presentation of broadened claims at the time of filing. For example, and like claim 37 of the subject continuation reissue application, claim 87 (reproduced below) presented in the Preliminary Amendment of the parent '604 reissue application also does not explicitly specify such a "configuring" operation:

87. A method for operating an attached computer module, the method comprising:

providing an attached computer module, the module comprising a security program, a user password, a first interface controller coupled to an interface connector;

coupling the computer module to a computer console, the computer console comprising a second interface controller compatible to the first interface controller, and a LAN communication controller coupled to an external network;

establishing communication between the two interface controllers;

receiving the user password from the console;

activating the security program to match the user password; and establishing the console access to certain data files in the computer module.

Accordingly, each of the above-identified broadening aspects of the subject continuation reissue application is related to, and would have been foreseeable in view of, broadened claims presented in the parent '604 reissue application within the two year period from the grant of the original '777 patent.

Conclusion

In view of the foregoing, Applicant respectfully submits that no further impediments exist to the allowance of the subject application and, therefore, requests an indication of allowability. However, the Examiner is requested to call the undersigned if any questions or comments arise.

The Director is hereby authorized to charge any appropriate fees under 37 C.F.R. §§1.16, 1.17, and 1.21 that may be required by this paper, and to credit any overpayment, to Deposit Account No. 50-1283.

Date: January 31, 2011 Customer No. 58249 Cooley LLP 777 6th Street NW, Suite 1100 Washington, DC 20001 Tel: (650) 843-5852 Fax: (202) 842-7899 Respectfully submitted, Cooley LLP

By:

Cliff Z. Liu Reg. No. 50,834

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PATENT

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of:	William W.Y. Chu	Confirmation No.:	1717
Serial No.:	12/561,138	Group Art Unit:	2435
Filed:	September 16, 2009	Examiner:	Song, Hosuk

For: DATA SECURITY METHOD AND DEVICE FOR COMPUTER MODULES

Express Mail Label Number: EV 602682060 US Date of Deposit: January 31, 2011

I hereby certify that this paper or fee is being deposited with the United States Postal Service "Express Mail Post Office to Addressee" service under 37 CFR 1.10 on the date indicated above and is addressed to the Director of Patents, PO Box 1450, Alexandria, VA 22318-1450

Date: January 31, 2011

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INFORMATION DISCLOSURE STATEMENT UNDER 37 C.F.R. §1.97(c)

In accordance with the duty of disclosure set forth in 37 C.F.R. §1.56, Applicant(s) hereby submits the following information in conformance with 37 C.F.R. §§1.97 and 1.98.

Pursuant to 37 C.F.R. §1.98, a copy of each non-US patent document cited in the attached Form PTO/SB/08 is enclosed in electronic form on a compact disc (CD).

No copies of the publications listed on the attached Form PTO/SB/08 are being provided pursuant to 37 C.F.R. §1.98(d) because the publications were previously cited by or submitted to the Office in prior Application Serial No. _____ to which the above-identified application claims priority under 35 U.S.C. §120.

No copies of any U.S. patents or U.S. patent application publications listed on the attached Form PTO/SB/08 are being provided pursuant to 37 C.F.R. §1.98.

Publications listed on the attached Form PTO/SB/08 were cited in a foreign search or examination report corresponding to _____ application serial no. _____ and mailed on

Enclosed is a copy of a non-English publication(s) _____. Pursuant to §609 of the M.P.E.P., Applicant submits the attached foreign search or examination report, which cites such non-English language publication(s).

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		ation _	copy of a non-English publication(s) English language (copy enclosed) claims priority from this non-English
			n explanation of non-English publication(s) for which an ation is not available.
			n English translation of non-English publication(s) cited in orm PTO/SB/08.
	Enclos	ed is a c	copy of pending patent Application Serial No.
			closure Statement is filed after the period specified in 37 C.F.R. § g of any of the following:
	\boxtimes	a final	action under 37 C.F.R. §1.113;
•	\boxtimes	a notic	e of allowance under 37 C.F.R. §1.311; or
	\boxtimes	an actio	on that otherwise closes prosecution in this application.
In acco	ordance	with 37	C.F.R. §1.97(c) also enclosed is:
	\boxtimes	Fee un	der 37 C.F.R. §1.17(p) in the amount of \$180.00; or
		Statem	ent as specified in 37 C.F.R. §1.97(e):
. .	·		Each item of information contained in the Information Disclosure Statement cited herein was first cited in a communication from a foreign patent office in a counterpart foreign application not more than three months prior to the filing date of the Information Disclosure Statement; <u>or</u>
			No item of information contained in the Information Disclosure

No item of information contained in the Information Disclosure Statement submitted herewith was cited in a communication from a foreign patent office in a counterpart foreign application, and, to the knowledge of the undersigned, having made a reasonable inquiry, no item of information contained in the Information Disclosure Statement was known to any individual designated in 37 C.F.R. §1.56(c) more than three months prior to the filing date of the Information Disclosure Statement. It is respectfully requested that the Examiner consider the above-noted information and return an initialed copy of the attached Form PTO/SB/08 to the undersigned.

Date: January 31, 2011

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Customer No. 58249 COOLEY LLP 777 6th Street NW, Suite 1100 Washington, DC 20001

Tel: (650) 843-5852 Fax: (202) 842-7899 Respectfully submitted, COOLEY LLP

By: Cliff Z. Liu

Reg. No. 50,834

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Sheet	1		of	23

Complete if Known					
Application Number 12/561,138					
Filing Date	September 16, 2009				
First Named Inventor	William W.Y. Chu				
Art Unit	2435				
Examiner Name	Song, Hosuk				
Attorney Docket Number ACQI-006/03US 310578-2053					

		•	U.S. PATENT D	OCUMENTS	
Examiner Initials*	Cite No.1	Document Number Number-Kind Code ^{2 (if known)}	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear
	A105	4,141,068	02-20-1979	Mager et al.	
	A024	4,228,496	10-14-1980	Katzman et al.	
	A001	4,453,215	06-05-1984	Reid	· · ·
	A104	4,670,837	06-02-1987	Sheets	
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	AO003	5,103,446	04-07-1992	Fischer	
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•	A039	5,436,902	07-25-1995	McNamara et al.	
	AO005	5,519,843	05-21-1996	Moran et al.	
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Examiner	Date Considered	
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INFORMATION DISCLOSURE STATEMENT BY APPLICANT

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of 23

Sheet 2

Co	September 16, 2009 William W.Y. Chu 2435 Song, Hosuk
Application Number	12/561,138
Filing Date	September 16, 2009
First Named Inventor	William W.Y. Chu
Art Unit	2435
Examiner Name	Song, Hosuk
Attorney Docket Number	ACQI-006/03US 310578-2053

			U. S. PATENT D	OCUMENTS	
Examiner Initials*	Cite No.1	Document Number Number-Kind Code ^{2 (if known)}	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear
	A050	5,708,840	01-13-1998	Kikinis et al.	
	A052	5,724,591	03-03-1998	Hara et al.	
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	AO008	5,751,711	05-12-1998	Sakaue	
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	AM001	6,088,620	07-11-2000	Ninomiya et al.	
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(Examiner Signature	· · · · · · · · · · · · · · · · · · ·	Date Considered	

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INFORMATION DISCLOSURE STATEMENT BY APPLICANT

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of

Sheet 3

Complete if Known				
Application Number	12/561,138			
Filing Date	September 16, 2009			
First Named Inventor	William W.Y. Chu			
Art Unit	2435			
Examiner Name	Song, Hosuk			
Attorney Docket Number	ACQI-006/03US 310578-2053			

		·	U. S. PATENT D	OCUMENTS	
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Examiner Signature		Date Considered	
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INFORMATION DISCLOSURE STATEMENT BY APPLICANT (Use as many sheets as necessary)

	mplete if Known
Application Number	12/561,138
Filing Date	September 16, 2009
First Named Inventor	William W.Y. Chu
Art Unit	2435
Examiner Name	Song, Hosuk
Attorney Docket Number	ACQI-006/03US 310578-2053

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of

Sheet 4

	U. S. PATENT DOCUMENTS				
Examiner Initials*	Cite No. ¹	Document Number Number-Kind Code ^{2 (if known)}	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear
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,	AJ001	2010/0174844 A1	07-08-2010	Chu	

		FOREIGN PA	TENT DOCUM	ENTS		
Examiner Initials*	Cite No. ¹	Foreign Patent Document Country Code ³ "Number ⁴ "Kind Code ⁵ (<i>if known</i>)		Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear	۲۴
	B001	JP 6-289956	10-18-1994	Hitachi, Ltd.		
	B002	JP 7-64672	03-10-1995	Toshiba Corp.		
	B005	JP 7-84675	03-31-1995	Hitachi, Ltd.		
	B006	WO 97/005618	02-13-1997	Memory Corporation PLC		

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STATEMENT BY APPLICANT (Use as many sheets as necessary)	of 23	Attorney Docket Number	ACQI-006/03US 310578-2053			

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of 23

Sheet 6

		NON PATENT LITERATURE DOCUMENTS	
Examiner Initials*	Cite No. ^{1.}	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.	T
	C015	Cubix Corporation, Density Series Plug-In Servers, Plug-In Computers for Managed Server Farms, September 15, 1998, 2 pages.	
	C016	Cubix Corporation, Cubix Pentium II Plug-In Computers for Density Series Systems, September 15, 1998, 1 page.	
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	C018	Compaq Computer Corporation, White Paper, "Order and Configuration Guide for Compaq ProLiant Cluster Series F Model 100," September 1998, pages 1-8.	
	C019	Compaq Computer Corporation, QuickSpecs, Compaq ProLiant Cluster Series F Model 100, (undated), pages 8- 36 to 8-37.	
	C020	Compaq Computer Corporation, Compaq Performance Brief, ProLiant 1600 ServerBench Performance Summary, August 1998, pages 1-7.	
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Examiner Signature	Date Considered	

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Sheet

INFORMATION DISCLOSURE STATEMENT BY APPLICANT

~		mplete if Known
	Application Number	12/561,138
	Filing Date	September 16, 2009
	First Named Inventor	William W.Y. Chu
	Art Unit	2435
	Examiner Name	Song, Hosuk
	Attorney Docket Number	ACQI-006/03US 310578-2053

(Use as many sheets as necessary)

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of

		NON PATENT LITERATURE DOCUMENTS		
Examiner Initials*				
	C029	JL ChatCom, Inc Highly Adaptable Intranet and Web Servers, "ChatCom, Inc. Announces Highly Adaptable Intranet and Web Servers," September 3, 1996 [retrieved on December 2, 2009], JL ChatCom, Inc., ChatterBox Communications and Server Solutions [online], Retrieved from the Internet: <url: http://web.archive.org/web/19970104221941/www.jlchatcom.com/chat4int.htm>, 2 pages.</url: 		
	C030	JL ChatCom, Inc., "ChatPower Plus," 1996 [retrieved on December 2, 2009], JL ChatCom, Inc., ChatterBox Communications and Server Solutions [online], Retrieved from the Internet: <url: http://web.archive.org/web/19970104222122/www.jlchatcom.com/chatplus.htm>, 3 pages.</url: 		
	C031	JL ChatCom, Inc., "ChatterBox ChatPower Plus," (undated) [retrieved on December 2, 2009], JL ChatCom, Inc., ChatterBox Communications and Server Solutions [online], Retrieved from the Internet: <url: http://web.archive.org/web/19970104222556/www.jlchatcom.com/cpp1.gif>, 1 page.</url: 		
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	C047	Wolfpack or Microsoft Cluster Services on STAR System, (undated), 3 pages.	L	
	C051	Network Engines, Inc., Network Engines ClusterDirector User's Manual, June 1998, 32 pages.		
	C052	Eversys Corporation, System 8000 Consolidated Network Server Product Brief, (undated), 2 pages.		
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	C054	Eversys Corporation, System 8000 Consolidated Server Presentation, (undated), 23 pages.	L	
	C055	Eversys Corporation, System 8000 Consolidated Network Server, Pentium II Processor Module User's Guide for Module version P2D-BXT, January 1998, 49 pages.		
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INFORMATION DISCLOSURE STATEMENT BY APPLICANT

4	Complete if Known			
Application Number 12/561,138		12/561,138		
Filing Date First Named Inventor		September 16, 2009		
		William W.Y. Chu		
	Art Unit	2435		
	Examiner Name	Song, Hosuk		
	Attorney Docket Number	ACQI-006/03US 310578-2053		

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Sheet 8

		NON PATENT LITERATURE DOCUMENTS	
Examiner Initials*	Cite No. ¹	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.	Т
	C057	Eversys Corporation, WebView 8000 version 1.1 User's Guide, Web-Based Management Software fo the EVERSYS System 8000 Consolidated Server, Revision A-November 1998, Revision B-December 1998, 56 pages.	
	C058	Eversys Corporation, S8000 Single Module Body Assemby, October 9, 1998, 9 pages.	
	C059	Eversys CAPserver Product Brief [online], (undated), [retrieved on November 16, 2009], Retrieved from the Internet: <url: 19961104093115="" capbrief.htm="" http:="" web="" web.archive.org="" www.eversys.com="">, 10 pages.</url:>	
	C060	Eversys CAPcard 9500/sa Product Brief [online], (undated), [retrieved on November 16, 2009], Retrieved from the Internet: <url: 19961104093144="" cc95sa_brief.htm="" http:="" web="" web.archive.org="" www.eversys.com="">, 3 pages.</url:>	
	C061	Evergreen Systems, Inc., "CAPserver, The Communication/Application server for local area networks," Product Guide, (undated), 18 pages.	
	C062	PHILLIPS, J., "9800 Disk Card Design Specification," May 26, 1998, White Cross Systems Limited, pages 1-44.	T
	C063	PHILLIPS, J., "9800 Disk Card Layout Specification," April 6, 1998, White Cross Systems Limited, pages 1-22.	
	C064	FEAKES, L., "Disk Connector Card Functional Requirement Specification," January 14, 1998, White Cross Systems Limited, pages 1-4.	
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	C075	SMITH, B., Processor Backplane Functional Requirement Specification, July 31, 1997, White Cross Systems Limited, pages 1- 11.	
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Complete if Known				
Application Number	12/561,138			
Filing Date	September 16, 2009			
First Named Inventor	William W.Y. Chu			
Art Unit	2435			
Examiner Name	Song, Hosuk			
Attorney Docket Number	ACQI-006/03US 310578-2053			

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_		Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the	Г
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	C079	PHILLIPS, J., "9800 Processor Card Layout Specification," September 29, 1997, White Cross Systems Limited, pages 1-13.	
	C080	MIASTKOWSKI, S. (Editor), "A Whale of a System," BYTE, August 1991, 4 pages, Vol. 16, No. 8.	
	C081	Advanced Micro Devices, Inc., "AMD-K6-III Processor Data Sheet," 21918B/0, October 1999, 326 pages.	1
	C082	Black Box Corporation, "Black Box Serve Switch Duo," Black Box Network Services Manual, July 1998, 52 pages.	
	C083	Cisco Systems, Inc., "Cisco AS5800 Universal Access Server Dial Shelf Controller Card Installation and Replacement," Doc. No. 78-4653-02, 1997, 28 pages.	
	C084	Digital Equipment Corporation, "DIGITAL AlphaServer 4000 and 4100 systems," [Brochure], 1998, 4 pages.	
	C089	EVERSYS, "CAPserver Product Brief" [online], [retrieved on 11-16-2009], Retrieved from the Internet: <url: http://web.archieve.org/web/19961104093115/www.eversys.com/CAPbrief.htm>, 10 pages.</url: 	
	C090	EVERSYS, "CAPcard 9500/sa Product Brief," [online], [retrieved on 11-16-2009], Retrieved from the Internet: <url: 19961104093144="" cc95sa_brief.htm="" http:="" web="" web.archieve.org="" www.eversys.com="">, 3 pages.</url:>	
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	C094	GROW, R. et al., "Gigabit Media Independent Interface Proposal," November 11, 1996, IEEE 802.3Z, Vancouver, 22 pages.	'
	C099	Intel, "Pentium® II Processor at 350 MHz, 400 MHz, and 450 MHz, Datasheet," Order Number 243657-003, August 1998, 83 pages.	
	C100	ELLIS, S., "IRIS FailSafe™ Administrator's Guide," Document Number 007-3109-003, April 6, 1997, 212 pages.	1
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	C103	Novell, Inc., "Novell's NetWare 4.1 Momentum Continues - NetWare 4 Now World's Best-Selling Network Operating System," [online], March 21, 1996, [retrieved on November 16, 2009]. Retrieved from the Internet: <url: 03="" 1996="" archive="" http:="" news="" pr96056.html="" press="" www.novell.com="">, 2 pages.</url:>	
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	C110	Sun Microsystems Computer Company, "Sun™ Enterprise™ 250 Server Owner's Guide," June 1998, Part No. 805-5160-10, Revision A, 324 pages.	
	C111	Sun Microsystems, Inc., "UltraSPARC™ -II CPU Module, Datasheet 400 MHz CPU, 2.0 MP E-Cache," July 1999, 28 pages.	'

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			First Named Inventor	William W.Y. Chu	
	STATEMENT BY APPL		Art Unit	2435	
	(Use as many sheets as necessa	vry)	Examiner Name	Song, Hosuk	
Shoot	10	23	Attorney Docket Number	ACQI-006/03US 310578-2053	

NON PATENT LITERATURE DOCUMENTS Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the Examiner T² Cite No.1 item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue Initials* number(s), publisher, city and/or country where published. C112 Sun Microsystems, Inc., White Paper, "Netra™ ft 1800," April 1999, Revision 09, 50 pages. C113 Compag Computer Corporation, et al., "Universal Serial Bus Specification," September 23, 1998, Revision 1.1, 327 pages. Compag Computer Corporation, et al., "Universal Serial Bus Specification," April 27, 2000, Revision 2.0, 650 C114 pages. Silicon Graphics International, "Additional Information for: IRIS FailSafe Administrator's Guide (IRIX 6.4)," C115 [online], Document Number: 007-3109-003, Published April 6, 1997, [retrieved on November 5, 2009], Retrieved from the Internet: <URL: http://techpubs.sgi.com/library/tpl/cgibin/summary.cgi?coll=0640&db=bks&docnumber=...>, 2 pages. Origin and Onyx Theory of Operations Manual, Document Number 007-3439-002, 1997, Silicon Graphics, Inc., C116 124 pages. C117 QuantumNet, Inc., QuantumNet 6000 Sharing Modules [online], 1996 [retrieved on November 16, 2009], Retrieved from the Internet: <URL: http://web.archive.org/web/19971011194326/www.quantumnet.com/dsq60xx.htm>, 3 pages. JL ChatCom, Inc., "ChatTwin," [retrieved on December 2, 2009], JL ChatCom, Inc., ChatterBox Communications C118 and Server Solutions [online], Retrieved from the Internet: <URL: http://web.archive.org/web/19970104222644/www.ilchatcom.com/chattwin.htm>, 2 pages. EVERSYS, "Welcome to EverSys" [online], [retrieved on 11-16-2009], Retrieved from the Internet: <URL: C119 http://web.archieve.org/web/19961104092834/www.eversys.com/index2.htm>, 1 page. EVERSYS, "Products" [online], [retrieved on 11-16-2009], Retrieved from the Internet: <URL: C120 http://web.archieve.org/web/19961104093103/www.eversys.com/prodinfo.htm>, 2 pages. "Microsoft Press Computer Dictionary, Third Edition," Microsoft Press, 1997, pages 199 and 332, Kim Fryer ed. C121 Excerpt from "Microsoft Computer Dictionary, 5th Edition", Microsoft Press, 2002, pages 96 and 547 C122 Excerpt from IEEE 100: The Authoritative Dictionary of IEEE Standards Terms (7th Ed., 2000), pages 78, 79 and C123 128 ANDERSON, C.R. et al., "IEEE 1355 HS-Links: Present Status and Future Prospects," [online], 1998, [retrieved C124 on 08-11-2010], Retrieved from the Internet: <URL: http://www94.web.cern.ch/HIS/dshs/publications/wotug21/hslink/pdf/hslinkpaper.pdf>, 14 pages. MAMAKOS, L. et al., "Request for Comments 2516 - A method for Transmitting PPP Over Ethernet (PPPoE)," C125 [online], 1999, [retrieved on 08-18-2010], Retrieved from the Internet: <URL: http://ttols.ietf.org/html/rfc2516>, 35 pages.

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Sheet 11

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	C126	HAAS, S., "The IEEE 1355 Standard: Developments, Performance and Application in High Energy Physics," Thesis for degree of Doctor of Philosophy, University of Liverpool, December 1998, 138 pages.	
	C127	"IEEE Std 1355-1995 Standard for Heterogeneous InterConnect (HIC)," Open Micro-processor systems Initiative (OMI), [online], October 30, 1998, [retrieved on 08-06-2010], Retrieved from the Internet: <url: http://grouper.ieee.org/groups/1355/index.html>, 6 pages.</url: 	
	C128	GALLES, M., "Spider: A Hide-Speed Network Interconnect," IEEE Micro, 1997, pp. 34-39. (6 pages)	
	C129	Excerpt from "Microsoft Computer Dictionary, 4th Edition", Microsoft Press, 1999, pages 184-85, 241, 432 (7 pages)	Γ
	C130	Excerpt from "Microsoft Computer Dictionary, 4th Edition", Microsoft Press, 1999, pages 40, 241, 432 (6 pages)	Γ
	C131	Excerpt from IEEE 100: The Authoritative Dictionary of IEEE Standards Terms (7th Ed., 2000), pages 181,304 and 771.	ĺ
	C132	"Family of VME Technology Specifications," [online], date unknown, [retrieved on 12-29-2010], Retrieved from the Internet: <url: http:="" specifications.html="" www.vita.com="">, 1 page.</url:>	
	CB051	CUBIX Customer Service Support System, "Click on the Front Panel That Matches Your System," ©2000, Cubix [online], [retrieved on June 22, 2004]. Retrieved from the Internet at <url: 64.173.211.7="" density="" density.htm="" http:="" support="" techinfo="">, 1 page.</url:>	
	CK001	International Search Report for International Patent Application No. PCT/US99/09369, report mailed November 16, 1999, 7 pages.	1
	CK002	International Preliminary Examination Report for International Patent Application No. PCT/US99/09369, report completed July 5, 2000, 4 pages.	
	CK003	IBM Corporation, "Grounding Spring for Peripheral Device and Bezel Bracket," IBM Technical Disclosure Bulletin, November 1, 1993, Vol. 36, No. 11, 2 pages.	
	CL001	DIGITAL SEMICONDUCTOR Product Brief, "21152 PCI-to-PCI Bridge," February 1996, 6 pages.	
	CL002	INTEL CORPORATION Architectural Overview, "Intel 430TX PCISET: 82439TX System Controller (MTXC)," February 1997, 4 pages.	
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	CL004	INTEL CORPORATION Advance Information, "Intel 440LX AGPSET: 82443LX PCI A.G.P. Controller (PAC)," August 1997, 4 pages.	
	CL005	NATIONAL SEMICONDUCTOR, "DS90CR215/DS90CR216 +3.3V Rising Edge Data Strobe LVDS 21-Bil Channel Link-66 MHz, July 1997, 2 pages.	ſ

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INFORMATION DISCLOSURE STATEMENT BY APPLICANT

-	Co	mplete if Known			
	Application Number 12/561,138				
Filing Date		September 16, 2009			
First Named Inventor William W.Y. Chu		William W.Y. Chu			
	Art Unit 2435				
Examiner Name Song, Hosuk		Song, Hosuk			
	Attorney Docket Number	ACQI-006/03US 310578-2053			

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	NON PATENT LITERATURE DOCUMENTS				
Examiner Initials*	nitials* Cite No. Item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.				
	CL006	NATIONAL SEMICONDUCTOR Product Folder, "DS90CR215 Plus-3.3V Rising Edge Data Strobe LVDS 21-Bit Channel and Link - 66 MHz," National Semiconductor Corporation [online], [retrieved on October 30, 1997]. Retrieved from the Internet at <url:< td=""> http://www.national.com/search/search.cgi/design?keywords=DS90CR215>, 2 pages.</url:<>			
	CL007	VIDEO ELECTRONICS Standards Association (VESA), Plug and Display (P&D) Standard, P&D and Digita Transition Minimized Differential Signaling (TMDS) Video Transmission Overview, 1997, Version 1, Revision 0, pp. 13 & 31-34.			
	CN001	LIQUORMAN, M., "Convergent Technologies Had This Idea," December 5, 1997, Jesse Berst's Anchor Desk [online], [retrieved on July 10, 1998]. Retrieved from the Internet at: <url: http://www.zdnet.com/anchordesk/talkback/talkback_56555.html>, 1 page.</url: 			
	CN002	BERST, J., "Hope For The Modular PCs We All Really Want," December 5, 1997, Jesse Berst's Anchor Desk [online], [retrieved on July 10, 1998]. Retrieved from the Internet at: <url: http://www.zdnet.com/anchordesk/story/story_1504.html>, 3 pages.</url: 			
	CN003	BOYD-MERRITT, R., "Upgradable-PC Effort Takes Divergent Paths," EE Times - Headline News [online], [retrieved on July 31, 1998]. Retrieved from the Internet at : <url: http://techweb.cmp.com/eet/news/97/949news/effort.html>, 3 pages.</url: 			
	CN004	FAEGRE, D. S. et al., "CTOS Revealed - Unisys' Best-Kept Secret Is An Operating System Built For Distributed Business Applications," December 1994, Core Technologies, BYTE [online], [retrieved on July 10, 1998]. Retrieved from the Internet at: <url: 9412="" art="" art2.htm="" http:="" sec13="" www.byte.com="">, 6 pages.</url:>			
	CN005	SPANG, K., "Component House: Design Technology for 'PCs in a Snap' - NeoSystems Offers Building Blocks," Computer Reseller News, April 21, 1997, Issue: 732, Section: Channel Assembly, TechWeb [online], [retrieved on July 31, 1998]. Retrieved from the Internet at: <url: http://www.techweb.com/se/directlink.cgi?CRN19970421S0054>, 2 pages.</url: 			
	CN006	"Think Modular," June 10, 1997, PC Magazine [online], [retrieved on July 31, 1998]. Retrieved from the Internet at: <url: 1611="" 60="" homezdnet.com="" http:="" issues="" pcmag="" pcmg0072.htm="" wysiwyg:="">, 1 page.</url:>			
	DA001 Office Action for U.S. Patent No. 6,718,415, mailed October 10, 2002, 7 pages.				
	DA002 Response for U.S. Patent No. 6,718,415, filed November 7, 2002, 9 pages.				
	DA003 Office Action for U.S. Patent No. 6,718,415, mailed January 29, 2003, 7 pages.				
	DA004 Response for U.S. Patent No. 6,718,415, filed March 6, 2003, 8 pages.				
	DA005	Office Action for U.S. Patent No. 6,718,415, mailed June 4, 2003, 8 pages.			
	DA006	Response for U.S. Patent No. 6,718,415, filed September 4, 2003, 10 pages.	L		
	DB001	Amendment Submitted With RCE for U.S. Patent No. 7,099,981, filed March 1, 2006, 23 pages.			

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First Named Inventor	William W.Y. Chu		
Art Unit	2435		
Examiner Name	Song, Hosuk		
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	Co. Application Number Filing Date First Named Inventor Art Unit Examiner Name		

NON PATENT LITERATURE DOCUMENTS				
Examiner Initials* Cite No.1 Include nam item (book,		Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.	T ²	
	DC001	Office Action for U.S. Patent No. 7,363,415, mailed on April 12, 2007, 23 pages.		
	DC002	Response for U.S. Patent No. 7,363,415, filed on April 24, 2007, 25 pages.		
· .	DD001	Office Action for U.S. Patent No. 7,328,297, mailed February 8, 2007, 5 pages.		
	DD002	Response for U.S. Patent No. 7,328,297, filed April 19, 2007, 32 pages.		
	DD003	Office Action for U.S. Patent No. 7,328,297, mailed July 12, 2007, 13 pages.		
	DD004	Response for U.S. Patent No. 7,328,297, filed July 23, 2007, 20 pages.		
	DF001	Office Action for U.S. Patent No. 7,363,416, mailed April 12, 2007, 23 pages.		
	DF002	Response for U.S. Patent No. 7,363,416, filed April 24, 2007, 23 pages.		
	DG001	Office Action for U.S. Patent No. 7,376,779, mailed September 28, 2007, 24 pages.		
	DG002	Response for U.S. Patent No. 7,376,779, filed October 16, 2007, 23 pages.		
	DH001	Office Action for U.S. Patent No. 7,676,624, mailed December 1, 2008, 8 pages.		
	DH002	Response for U.S. Patent No. 7,676,624, filed January 13, 2009, 14 pages.		
	DH003	Supplemental Response for U.S. Patent No. 7,676,624, filed on February 6, 2009, 13 pages.		
	DI001	Office Action for U.S. Patent No. 7,818,487, mailed September 29, 2009, 10 pages.		
	D1002	Response for U.S. Patent No. 7,818,487, filed November 6, 2009, 3 pages.		
DI003 Amendment for U.S. Patent No. 7,818,487, filed May 11, 2010, 15 pages.				
DI004 Amendment Submitted After Notice of Allowance for U.S. Patent No. 7,818,487, filed August 17, 2010, 14				
	DJ001	Office Action for U.S. Publication No. 2010/0174844, mailed October 28, 2010, 11 pages.		
•	DK001	Office Action for U.S. Patent No. 6,216,185, mailed April 12, 2000, 9 pages.		
	DK002	Response for U.S. Patent No. 6,216,185, filed August 3, 2000, 15 pages.		
	DK003	Office Action for U.S. Patent No. 6,216,185, mailed August 25, 2000, 9 pages.		
	DK004	Response for U.S. Patent No. 6,216,185, filed October 24, 2000, 10 pages.		
	DL001	Office Action for U.S. Patent No. 6,345,330, mailed June 15, 2000, 7 pages.		
DL002 Amendment for U.S. Patent No. 6,345,330, filed September 12, 2000, 5 pages.		Amendment for U.S. Patent No. 6,345,330, filed September 12, 2000, 5 pages.		
DL003 Restriction Requirement for U.S. Patent No. 6,345,330, mailed December 19, 2000, 5 pages.				
	DL004	Amendment filed with Continued Prosecution Application for U.S. Patent No. 6,345,330, filed January 17, 2001, 5 pages.		
	DL005	Office Action for U.S. Patent No. 6,345,330, mailed March 23, 2001, 6 pages.		
· · · · ·	DL006 Response to Office Action for U.S. Patent No. 6,345,330, filed July 19, 2001, 5 pages.			
	DM001	Office Action for U.S. Patent Application No. 09/642,628, mailed April 5, 2001, 9 pages.		
	DO001	Office Action for U.S. Application No. 10/963,825, mailed October 27, 2005, 25 pages.		

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Application Number	12/561,138		
Filing Date	September 16, 2009		
First Named Inventor	William W.Y. Chu		
Art Unit	2435		
Examiner Name	Song, Hosuk		
Attorney Docket Number ACQI-006/03US 310578-2053			

		NON PATENT LITERATURE DOCUMENTS		
Examiner Initials* Cite No.1				
	DO002	Response for U.S. Application No. 10/963,825, filed January 9, 2006, 22 pages.		
_	DO003	Office Action for U.S. Application No. 10/963,825, mailed May 31, 2006, 29 pages.		
	DO004	Amendment Submitted with RCE for U.S. Application No. 10/963,825, filed July 27, 2006, 29 pages.		
	DO005	Office Action for U.S. Application No. 10/963,825, mailed October 20, 2006, 28 pages.		
	DO006	Appellants' Brief for U.S. Application No. 10/963,825, filed January 8, 2007, 31 pages.		
	DO007	Revised Appellants' Brief for U.S. Application No. 10/963,825, filed April 20, 2007, 34 pages.		
	DO008	Examiner's Answer for U.S. Application No. 10/963,825, mailed August 8, 2007, 30 pages.		
	DO009	Reply Brief for U.S. Application No. 10/963,825, filed September 4, 2007, 4 pages.	<u> </u>	
	DO010	Decision on Appeal for U.S. Application No. 10/963,825, mailed February 4, 2009, 13 pages.		
	DO011	Amendment Submitted with RCE for U.S. Application No. 10/963,825, filed February 20, 2009, 24 pages.		
	DO012	Office Action for U.S. Application No. 10/963,825, mailed May 14, 2009, 5 pages.		
	DO013 Response for U.S. Application No. 10/963,825, filed May 22, 2009, 2 pages.			
	DO014 Office Action for U.S. Application No. 10/963,825, mailed September 15, 2009, 14 pages.			
	DO015 Response for U.S. Application No. 10/963,825, filed October 1, 2009, 7 pages.			
	DP001	Office Action for RE 41,294, mailed November 16, 2007, 10 pages.		
	DP002 ·	Response for RE 41,294, filed December 20, 2007, 21 pages.		
	DP003	Office Action for RE 41,294, mailed April 15, 2008, 10 pages.		
	DP004	Amendment Submitted with RCE for RE 41,294, filed May 27, 2008, 14 pages.		
	DP005	Supplemental Amendment Submitted with RCE for RE 41,294, filed July 8, 2008, 12 pages.		
	DP006	Office Action for RE 41,294, mailed September 16, 2008, 11 pages.		
	DP007	Response for RE 41,294, filed October 30, 2008, 14 pages.		
	DP008	Supplemental Response for RE 41,294, filed February 20, 2009, 13 pages.		
	DP009	Supplemental Response for RE 41,294, filed August 17, 2009, 3 pages.		
	DP010	Examiner Interview Summary Record, mailed January 15, 2009, 1 page.		
	DQ001	Office Action for RE 41,076, mailed July 13, 2007, 38 pages.		
	DQ002	Response for RE 41,076, filed September 26, 2007, 18 pages.		
	DQ003	Office Action for RE 41,076, mailed October 17, 2007, 55 pages.		
	DQ004 Amendment Submitted with RCE for RE 41,076, filed November 5, 2007, 19 pages.			
	DQ005	Office Action for RE 41,076, mailed February 11, 2008, 62 pages.		
	DQ006	Response for RE 41,076, filed April 7, 2008, 18 pages.		
	DQ007	Office Action for RE 41,076, mailed June 9, 2008, 25 pages.		

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 Application Number
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 Filing Date
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 First Named Inventor
 William W.Y. Chu

 Art Unit
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 Examiner Name
 Song, Hosuk

 Attorney Docket Number
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_{Sheet} 16 _

		NON PATENT LITERATURE DOCUMENTS	
Examiner Initials*	Cite No.1	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.	T ²
	EA005	Request for Ex Parte Reexamination of US Patent No. 6,216,185, Control No. 90/010,816, filed January 8, 2010, Exhibit DD Claim Charts with respect to the Hitachi '675 for Anticipation and Obviousness, 119 pages	T
	EA006	Office Action in Ex Parte Reexamination of US Patent No. 6,216,185, Control No. 90/010,816, mailed July 27, 2010, 103 pages	,
	EA007	Patent Owner's Response to Office Action in Ex Parte Reexamination of US Patent No. 6,216,185, Control No. 90/010,816, filed September 27, 2010, 55 pages	
	EB001	Request for Inter Partes Reexamination of US Patent No. 6,718,415, Control No. 95/001,276, filed December 2, 2009, 44 pages.	,
	EB002	Request for Inter Partes Reexamination of US Patent No. 6,718,415, Control No. 95/001,276, filed December 2, 2009, Exhibit O, Declaration Under 37 CFR 1.132 of Vincent P. Conroy, 11-24-2009, 3 pages.	-
	EB003	Request for Inter Partes Reexamination of US Patent No. 6,718,415, Control No. 95/001,276, Replacement Exhibit AA, Claim Charts with respect to QuantumNet for Anticipation and Obviousness, filed January 5, 2010, 109 pages.	
	EB004	Request for Inter Partes Reexamination of US Patent No. 6,718,415, Control No. 95/001,276, Replacement Exhibit BB, Claim Charts with respect to Chatcom for Anticipation and Obviousness, filed January 5, 2010, 91 pages.	
	EB005	Request for Inter Partes Reexamination of US Patent No. 6,718,415, Control No. 95/001,276, Replacement Exhibit CC, Claim Charts with respect to QuantumNet for Anticipation and Obviousness, filed January 5, 2010, 85 pages.	
	EB006	Request for Inter Partes Reexamination of US Patent No. 6,718,415, Control No. 95/001,276, Replacement Exhibit DD, Claim Charts with respect to the Origin2000 Manual for Obviousness, filed January 5, 2010, 72 pages.	
	EB007	Request for Inter Partes Reexamination of US Patent No. 6,718,415, Control No. 95/001,276, Replacement Exhibit EE, Claim Charts with respect to Gallagher for Anticipation and Obviousness, filed January 5, 2010, 107 pages.	t
	EB008	Office Action in Inter Partes Reexamination of US Patent No. 6,718,415, Control No. 95/001,276, mailed May 26, 2010, 39 pages.	
	EB009	Patent Owner's Response to Office Action in Inter Partes Reexamination of US Patent No. 6,718,415, Control No. 95/001,276, filed July 27, 2010, 41 pages.	
	EB010	Patent Owner's Response to Office Action in Inter Partes Reexamination of US Patent No. 6,718,415, Control No. 95/001,276, Exhibit A, Declaration of William Henry Mangione-Smith under 37 C.F.R. 1.132, filed July 27, 2010, 29 pages.	

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Sheet 17

	· · · · · · · · · · · · · · · · · · ·	NON PATENT LITERATURE DOCUMENTS	—
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	EC001	Request for Inter Partes Reexamination of US Patent No. 7,099,981, Control No. 95/001,310, filed February 9, 2010, 33 pages	
	EC002	Request for Inter Partes Reexamination of US Patent No. 7,099,981, Control No. 95/001,310, filed December 2, 2009, Exhibit O, Declaration Under 37 CFR 1.132 of Vincent P. Conroy, 11-24-2009, 3 pages.	
	EC003	Request for Inter Partes Reexamination of US Patent No. 7,099,981, Control No. 95/001,310, Exhibit AA, Claim Charts with respect to Gallagher for Anticipation and Obviousness, filed February 9, 2010, 164 pages	
	EC004	Request for Inter Partes Reexamination of US Patent No. 7,099,981, Control No. 95/001,310, Exhibit BB, Claim Charts with respect to QuantumNet for Anticipation and Obviousness, filed February 9, 2010, 158 pages	
	EC005	Request for Inter Partes Reexamination of US Patent No. 7,099,981, Control No. 95/001,310, Exhibit CC, Claim Charts with respect to Chatcom for Anticipation and Obviousness, filed February 9, 2010, 167 pages	
	EC006	Request for Inter Partes Reexamination of US Patent No. 7,099,981, Control No. 95/001,310, Exhibit DD, Claim Charts with respect to the Eversys for Obviousness, filed February 9, 2010, 111 pages	
	EC007	Office Action in Inter Partes Reexamination of US Patent No. 7,099,981, Control No. 95/001,310, mailed July 6, 2010, 83 pages	
	EC008	Patent Owner's Response to Office Action in Inter Partes Reexamination of US Patent No. 7,099,981, Control No. 95/001,310, filed September 3, 2010, 52 pages	
	EC009	Patent Owner's Response to Office Action in Inter Partes Reexamination of US Patent No. 7,099,981, Control No. 95/001,310, Exhibit A, Declaration of William Henry Mangione-Smith under 37 C.F.R. 1.132, filed September 3, 2010, 63 pages	
	ED001	Request for Inter Partes Reexamination of US Patent No. 7,146,446, Control No. 95/001,328, filed March 19, 2010, 35 pages.	
	ED002	Request for Inter Partes Reexamination of US Patent No. 7,146,446, Control No. 95/001,328, Exhibit AA (Part 1), Claim Charts with respect to Gallagher for Anticipation and Obviousness, filed March 19, 2010, 186 pages.	
	ED003	Request for Inter Partes Reexamination of US Patent No. 7,146,446, Control No. 95/001,328, Exhibit AA (Part 2), Claim Charts with respect to Gallagher for Anticipation and Obviousness, filed March 19, 2010, 161 pages.	
·.	ED004	Request for Inter Partes Reexamination of US Patent No. 7,146,446, Control No. 95/001,328, Exhibit BB (Part 1), Claim Charts with respect to QuantumNet for Anticipation and Obviousness, filed March 19, 2010, 139 pages.	
	ED005	Request for Inter Partes Reexamination of US Patent No. 7,146,446, Control No. 95/001,328, Exhibit BB (Part 2), Claim Charts with respect to QuantumNet for Anticipation and Obviousness, filed March 19, 2010, 128 pages.	
	ED006	Request for Inter Partes Reexamination of US Patent No. 7,146,446, Control No. 95/001,328, Exhibit CC, Claim Charts with respect to Chatcom for Anticipation and Obviousness, filed March 19, 2010, 68 pages.	

Examiner Signature	Date Considered	

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INFORMATION DISCLOSURE STATEMENT BY APPLICANT

	Complete if Known			
	Application Number	12/561,138		
	Filing Date	September 16, 2009		
First Named Inventor		William W.Y. Chu		
	Art Unit	2435		
	Examiner Name	Song, Hosuk		
	Attorney Docket Number	ACQI-006/03US 310578-2053		

(Use as many sheets as necessary)

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Sheet 18

		NON PATENT LITERATURE DOCUMENTS	
Examiner Initials*	Cite No. ¹	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.	т
	ED007	Office Action in Inter Partes Reexamination of US Patent No. 7,146,446, Control No. 95/001,328, mailed June 24, 2010, 86 pages.	
	ED008	Patent Owner's Response to Office Action in Inter Partes Reexamination of US Patent No. 7,146,446, Control No. 95/001,328, filed August 24, 2010, 45 pages.	
	ED009	Patent Owner's Response to Office Action in Inter Partes Reexamination of US Patent No. 7,146,446, Control No. 95/001,328, Exhibit A, Declaration of William Henry Mangione-Smith under 37 C.F.R. 1.132, filed September 3, 2010, 61 pages.	
	EE001	Request for Inter Partes Reexamination of US Patent No. 7,328,297, Control No. 95/001,336, filed April 19, 2010, 33 pages.	ŀ
	EE002	Request for Inter Partes Reexamination of US Patent No. 7,328,297, Control No. 95/001,336, Exhibit AA, Claim Charts with respect to Gallagher for Obviousness, filed April 19, 2010, 131 pages.	
	EE003	Request for Inter Partes Reexamination of US Patent No. 7,328,297, Control No. 95/001,336, Exhibit BB, Claim Charts with respect to QuantumNet for Obviousness, filed April 19, 2010, 139 pages.	
	EE004	Request for Inter Partes Reexamination of US Patent No. 7,328,297, Control No. 95/001,336, Exhibit CC, Claim Charts with respect to Chatcom for Obviousness, filed April 19, 2010, 114 pages.	
	EE005	Office Action in Inter Partes Reexamination of US Patent No. 7,328,297, Control No. 95/001,336, mailed August 4, 2010, 95 pages.	
	EE006	Patent Owner's Response to Office Action in Inter Partes Reexamination of US Patent No. 7,328,297, Control No. 95/001,336, filed October 4, 2010, 49 pages.	
	EE007	Patent Owner's Response to Office Action in Inter Partes Reexamination of US Patent No. 7,328,297, Control No. 95/001,336, Exhibit A, Declaration of William Henry Mangione-Smith under 37 C.F.R. 1.132, filed October 4, 2010, 61 pages.	
	EF001	Request for Inter Partes Reexamination of US Patent No. 7,363,415, Control No. 95/001,424, filed August 25, 2010, 34 pages.	
	EF002	Request for Inter Partes Reexamination of US Patent No. 7,363,415, Control No. 95/001,424, Exhibit AA, Claim Charts with respect to Gallagher and Other References for Obviousness, filed August 25, 2010, 114 pages.	
	EF003	Request for Inter Partes Reexamination of US Patent No. 7,363,415, Control No. 95/001,424, Exhibit AB, Claim Charts with respect to Gallagher and Other References for Obviousness, filed August 25, 2010, 92 pages.	
	EF004	Request for Inter Partes Reexamination of US Patent No. 7,363,415, Control No. 95/001,424, Exhibit BA, Claim Charts with respect to QuantumNet and Other References for Obviousness, filed August 25, 2010, 121 pages.	
	EF005	Request for Inter Partes Reexamination of US Patent No. 7,363,415, Control No. 95/001,424, Exhibit BB, Claim Charts with respect to QuantumNet and Other References for Obviousness, filed August 25, 2010, 99 pages.	

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	INFORMATION DISCLOSURE STATEMENT BY APPLICANT (Use as many sheets as necessary)		Filing Date	September 16, 2009
			First Named Inventor	William W.Y. Chu
			Art Unit	2435
(Use as many sheets as necessary)		necessary)	Examiner Name	Song, Hosuk
Shee	19	of 23	Attorney Docket Number	ACQI-006/03US 310578-2053

		NON PATENT LITERATURE DOCUMENTS	
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	EF006	Request for Inter Partes Reexamination of US Patent No. 7,363,415, Control No. 95/001,424, Exhibit CA, Claim Charts with respect to Chatcom and Other References for Obviousness, filed August 25, 2010, 91 pages.	1
	EF007	Request for Inter Partes Reexamination of US Patent No. 7,363,415, Control No. 95/001,424, Exhibit CB, Claim Charts with respect to Chatcom and Other References for Obviousness, filed August 25, 2010, 94 pages.	1
	EF008	Office Action in Inter Partes Reexamination of US Patent No. 7,363,415, Control No. 95/001,424, mailed November 1, 2010, 75 pages.	ł .
	EG001	Request for Inter Partes Reexamination of US Patent No. 7,376,779, Control No. 95/001,475, filed October 27, 2010, 35 pages.	
	EG002	Request for Inter Partes Reexamination of US Patent No. 7,376,779, Control No. 95/001,475, Exhibit AA, Claim Charts with respect to Gallagher and Other References for Obviousness, filed October 27, 2010, 128 pages.	1
	EG003	Request for Inter Partes Reexamination of US Patent No. 7,376,779, Control No. 95/001,475, Exhibit AB, Claim Charts with respect to Gallagher and Other References for Obviousness, filed October 27, 2010, 153 pages.	1
	EG004	Request for Inter Partes Reexamination of US Patent No. 7,376,779, Control No. 95/001,475, Exhibit BA, Claim Charts with respect to QuantumNet and Other References for Obviousness, filed October 27, 2010, 108 pages.	1
	EG005	Request for Inter Partes Reexamination of US Patent No. 7,376,779, Control No. 95/001,475, Exhibit BB, Claim Charts with respect to QuantumNet and Other References for Obviousness, filed October 27, 2010, 112 pages.	
	EG006	Request for Inter Partes Reexamination of US Patent No. 7,376,779, Control No. 95/001,475, Exhibit CA, Claim Charts with respect to Chatcom and Other References for Obviousness, filed October 27, 2010, 112 pages.	1 ·
	EG007	Request for Inter Partes Reexamination of US Patent No. 7,376,779, Control No. 95/001,475, Exhibit CB, Claim Charts with respect to Chatcom and Other References for Obviousness, filed October 27, 2010, 118 pages.	1
	EG008	Office Action in Inter Partes Reexamination of US Patent No. 7,376,779, Control No. 95/001,475, mailed December 20, 2010, 105 pages.	-
	EH001	Request for Inter Partes Reexamination of US Patent No. 7,363,416, Control No. 95/001,476, filed October 27, 2010, 37 pages.	
	EH002	Request for Inter Partes Reexamination of US Patent No. 7,363,416, Control No. 95/001,476, Exhibit AA, Claim Charts with respect to Gallagher and Other References for Obviousness, filed October 27, 2010, 70 pages.	1
	EH003	Request for Inter Partes Reexamination of US Patent No. 7,363,416, Control No. 95/001,476, Exhibit AB, Claim Charts with respect to Gallagher and Other References for Obviousness, filed October 27, 2010, 64 pages.	1
	EH004	Request for Inter Partes Reexamination of US Patent No. 7,363,416, Control No. 95/001,476, Exhibit BA, Claim Charts with respect to QuantumNet and Other References for Obviousness, filed October 27, 2010, 64 pages.	1
	EH005	Request for Inter Partes Reexamination of US Patent No. 7,363,416, Control No. 95/001,476, Exhibit BB, Claim Charts with respect to QuantumNet and Other References for Obviousness, filed October 27, 2010, 71 pages.	1

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of

	Complete if Known			
	Application Number	12/561,138		
	Filing Date	September 16, 2009		
	First Named Inventor	William W.Y. Chu		
Art Unit		2435		
	Examiner Name	Song, Hosuk		
	Attorney Docket Number	ACQI-006/03US 310578-2053		

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Sheet 20

		NON PATENT LITERATURE DOCUMENTS	
Examiner Initials*	nitials* Cite No. Item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.		T ²
	EH006	Request for Inter Partes Reexamination of US Patent No. 7,363,416, Control No. 95/001,476, Exhibit CA, Claim Charts with respect to Chatcom and Other References for Obviousness, filed October 27, 2010, 64 pages.	
	EH007	Request for Inter Partes Reexamination of US Patent No. 7,363,416, Control No. 95/001,476, Exhibit CB, Claim Charts with respect to Chatcom and Other References for Obviousness, filed October 27, 2010, 67 pages.	
	EH008	Office Action in Inter Partes Reexamination of US Patent No. 7,363,416, Control No. 95/001,476, mailed December 6, 2010, 63 pages.	
	IC01	"Defendants' Amended Invalidity Contentions," submitted by the Defendants in the U.S. District Court for the Eastern District of Texas, Case No. 6:09-cv-148-LED on March 1, 2010, 18 pages.	
	IC02	"Exhibit A (Asserted Claims)," submitted by the Defendants in the U.S. District Court for the Eastern District of Texas, Case No. 6:09-cv-148-LED on March 1, 2010, 2 pages.	
	IC03	"Exhibit B - Table 1," submitted by the Defendants in the U.S. District Court for the Eastern District of Texas, Case No. 6:09-cv-148-LED on March 1, 2010, 75 pages.	
	IC04	"Exhibit C," submitted by the Defendants in the U.S. District Court for the Eastern District of Texas, Case No. 6:09-cv-148-LED on March 1, 2010, 2 pages.	
	IC05	"Exhibit D," submitted by the Defendants in the U.S. District Court for the Eastern District of Texas, Case No. 6:09-cv-148-LED on March 1, 2010, 106 pages.	
	IC06	"Exhibit E," submitted by the Defendants in the U.S. District Court for the Eastern District of Texas, Case No. 6:09-cv-148-LED on March 1, 2010, 2 pages.	
	IC07	"Invalidity Chart for Base Reference IBM 8260," submitted by the Defendants in the U.S. District Court for the Eastern District of Texas, Case No. 6:09-cv-148-LED on March 1, 2010, 53 pages.	
	IC08	"Invalidity Chart for Base Reference IBM 8265," submitted by the Defendants in the U.S. District Court for the Eastern District of Texas, Case No. 6:09-cv-148-LED on March 1, 2010, 56 pages.	
· .	IC09	"Invalidity Chart for Base Reference U.S. Patent No. 4,453,215 (Reid)," submitted by the Defendants in the U.S. District Court for the Eastern District of Texas, Case No. 6:09-cv-148-LED on March 1, 2010, 56 pages.	
	IC10	"Invalidity Chart for Base Reference Origin2000," submitted by the Defendants in the U.S. District Court for the Eastern District of Texas, Case No. 6:09-cv-148-LED on March 1, 2010, 56 pages.	
	IC11	"Invalidity Chart for Base Reference QuantumNet," submitted by the Defendants in the U.S. District Court for the Eastern District of Texas, Case No. 6:09-cv-148-LED on March 1, 2010, 49 pages.	
	IC12	"Invalidity Chart for Base Reference U.S. Patent No. 6,564,274 (Heath)," submitted by the Defendants in the U.S. District Court for the Eastern District of Texas, Case No. 6:09-cv-148-LED on March 1, 2010, 57 pages.	
<u></u>	IC13	"Invalidity Chart for Base Reference U.S. Patent No. 5,577,205," submitted by the Defendants in the U.S. District Court for the Eastern District of Texas, Case No. 6:09-cv-148-LED on March 1, 2010, 60 pages.	-

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	First Named Inventor	William W.Y. Chu
	Art Unit	2435
	Examiner Name	Song, Hosuk
	Attorney Docket Number	ACQI-006/03US 310578-2053

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Examiner Initials*	Cite No.1	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.	T
	IC14	"Invalidity Chart for Base Reference U.S. Patent No. 5,802,391," submitted by the Defendants in the U.S. District Court for the Eastern District of Texas, Case No. 6:09-cv-148-LED on March 1, 2010, 61 pages.	
	IC15	"Invalidity Chart for Base Reference U.S. Patent No. 6,715,100," submitted by the Defendants in the U.S. District	
	1015		
	IC16	Court for the Eastern District of Texas, Case No. 6:09-cv-148-LED on March 1, 2010, 64 pages.	
	1010	"Invalidity Chart for Base Reference Cubix BC/Density," submitted by the Defendants in the U.S. District Court for	
	1047	the Eastern District of Texas, Case No. 6:09-cv-148-LED on March 1, 2010, 64 pages.	
	IC17	"Invalidity Chart for Base Reference JP6-289956," submitted by the Defendants in the U.S. District Court for the	
		Eastern District of Texas, Case No. 6:09-cv-148-LED on March 1, 2010, 62 pages.	ļ
	IC18	"Invalidity Chart for Base Reference Gallagher 068 and Gallagher 503," submitted by the Defendants in the U.S.	
		District Court for the Eastern District of Texas, Case No. 6:09-cv-148-LED on March 1, 2010, 108 pages.	
	IC19	"Invalidity Chart for Base Reference Compaq ProLiant Cluster," submitted by the Defendants in the U.S. District	
		Court for the Eastern District of Texas, Case No. 6:09-cv-148-LED on March 1, 2010, 81 pages.	L
	IC20	"Invalidity Chart for Base Reference U.S. Patent No. 5,325,517 to Baker et al. (Appendix 1, Exhibit 15),"	
		submitted by the Defendants in the U.S. District Court for the Eastern District of Texas, Case No. 6:09-cv-148-	
		LED on March 1, 2010, 59 pages.	
	IC21	"Invalidity Chart for Japanese Patent Application H7-64672 (Toshiba '672)," submitted by the Defendants in the	
		U.S. District Court for the Eastern District of Texas, Case No. 6:09-cv-148-LED on March 1, 2010, 55 pages.	
	IC22	"Invalidity Chart for Base Reference ChatCom," submitted by the Defendants in the U.S. District Court for the	
		Eastern District of Texas, Case No. 6:09-cv-148-LED on March 1, 2010, 52 pages.	
	IC23	"Invalidity Chart for Base Reference Ziatech Corp. Ketris 9000 System," submitted by the Defendants in the U.S.	
		District Court for the Eastern District of Texas, Case No. 6:09-cv-148-LED on March 1, 2010, 68 pages.	
	IC24	"Invalidity Chart for Base Reference Ziatech STD 32 Star System," submitted by the Defendants in the U.S.	
		District Court for the Eastern District of Texas, Case No. 6:09-cv-148-LED on March 1, 2010, 62 pages.	
	IC25	"Invalidity Chart for Base Reference U.S. Patent No. 7,339,786 (Bottom et al.)," submitted by the Defendants in	1
		the U.S. District Court for the Eastern District of Texas, Case No. 6:09-cv-148-LED on March 1, 2010, 57 pages.	
	IC26	"Invalidity Chart for Base References RLX Patents, U.S. Patent Nos. 6,747,878, 6,411,506, 6,325,636,	┢
		6,757,748, and 6,985,967 (Hipp et al.)," submitted by the Defendants in the U.S. District Court for the Eastern	
		District of Texas, Case No. 6:09-cv-148-LED on March 1, 2010, 58 pages.	
	IC27	"Invalidity Chart for Base Reference Network Engines P6000 Server," submitted by the Defendants in the U.S.	1-
		District Court for the Eastern District of Texas, Case No. 6:09-cv-148-LED on March 1, 2010, 59 pages.	
	IC28	"Invalidity Chart for Base Reference Eversys 8000 System," submitted by the Defendants in the U.S. District	<u> </u>
	1020	Court for the Eastern District of Texas, Case No. 6:09-cv-148-LED on March 1, 2010, 60 pages.	

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	IC29	"Invalidity Chart for Base Reference Eversys CAPserver," submitted by the Defendants in the U.S. District Court	
		for the Eastern District of Texas, Case No. 6:09-cv-148-LED on March 1, 2010, 59 pages.	
IC30 "Invalidity Chart for Base Reference U.S. 5,809,262," submitted by the Defendants in the U.S. District Court f		Į	
		the Eastern District of Texas, Case No. 6:09-cv-148-LED on March 1, 2010, 62 pages.	
IC31 "Invalidity Chart for Base Reference WhiteCross 9800 System," submitted by the Defendants in the U.S. District			
		Court for the Eastern District of Texas, Case No. 6:09-cv-148-LED on March 1, 2010, 62 pages.	
	IC32	"Invalidity Chart for Base Reference U.S. 5,339,408," submitted by the Defendants in the U.S. District Court for	
		the Eastern District of Texas, Case No. 6:09-cv-148-LED on March 1, 2010, 61 pages.	
	IC33	"Invalidity Chart for Base Reference Tyuluman 536," submitted by the Defendants in the U.S. District Court for	
		the Eastern District of Texas, Case No. 6:09-cv-148-LED on March 1, 2010, 76 pages.	
	IC34	"Invalidity Chart for Base Reference Hong 737," submitted by the Defendants in the U.S. District Court for the	
		Eastern District of Texas, Case No. 6:09-cv-148-LED on March 1, 2010, 77 pages.	
IC35 "Invalidity Chart for Base Reference U.S. 5,436,857 (Nelson)," submitted by the Defendants in the U.S. I			
Court for the Eastern District of Texas, Case No. 6:09-cv-148-LED on March 1, 2010, 6 pages.		Court for the Eastern District of Texas, Case No. 6:09-cv-148-LED on March 1, 2010, 6 pages.	
IC36 "Invalidity Chart for Base Reference U.S. 5,999,952 (Jenkins)", submitted by the Defendants in the U.S. Dis		"Invalidity Chart for Base Reference U.S. 5,999,952 (Jenkins)", submitted by the Defendants in the U.S. District	
		Court for the Eastern District of Texas, Case No. 6:09-cv-148-LED on March 1, 2010, 6 pages.	
	IC37	"Invalidity Chart for Base Reference U.S. 5,608,608 (Flint)", submitted by the Defendants in the U.S. District	
		Court for the Eastern District of Texas, Case No. 6:09-cv-148-LED on March 1, 2010, 6 pages.	
	IC38	"Invalidity Chart for Base Reference U.S. 5,978,821 (Freeny)", submitted by the Defendants in the U.S. District	
		Court for the Eastern District of Texas, Case No. 6:09-cv-148-LED on March 1, 2010, 6 pages.	
	IC39	"Invalidity Chart for Base Reference WO 92/18924 (Wallsten)", submitted by the Defendants in the U.S. District	
		Court for the Eastern District of Texas, Case No. 6:09-cv-148-LED on March 1, 2010, 6 pages.	
	IC40	"Invalidity Chart for Base Reference Ergo Moby Brick", submitted by the Defendants in the U.S. District Court for	
		the Eastern District of Texas, Case No. 6:09-cv-148-LED on March 1, 2010, 5 pages.	
	IC41	"Invalidity Chart for Base Reference U.S. Patent No. 5,463,742 (Kobayashi)", submitted by the Defendants in the	
		U.S. District Court for the Eastern District of Texas, Case No. 6:09-cv-148-LED on March 1, 2010, 5 pages.	
	IC42	"Invalidity Chart for Base Reference Japanese Patent Application Publication H6-289953 (Hitachi)", submitted by	
		the Defendants in the U.S. District Court for the Eastern District of Texas, Case No. 6:09-cv-148-LED on March 1	,
		2010, 5 pages.	
	IC43	"Invalidity Chart for Base Reference Japanese Patent Application Publication H7-84675 (Hitachi)", submitted by	
		the Defendants in the U.S. District Court for the Eastern District of Texas, Case No. 6:09-cv-148-LED on March 1	,
		2010, 5 pages.	

Examiner Signature	Date Considered	

*EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant. 'Applicant's unique citation designation number (optional). ²See Kinds Codes of USPTO Patent Documents at <u>www.uspto.gov</u> or MPEP 901.04. ³Enter Office that issued the document, by the two-letter code (WIPO Standard ST.3). ⁴For Japanese patent documents, the indication of the year of the reign of the Emperor must precede the serial number of the patent document. ⁵Kind of document by the appropriate symbols as indicated on the document under WIPO Standard ST. 16 if possible. ⁶Applicant is to place a check mark here if English language Translation is attached.

This collection of information is required by 37 CFR 1.97 and 1.98. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 2 hours to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.

PTO/SB/08a (07-09) Approved for use through 07/31/2012. OMB 0651-0031

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Substitute for form 1449A/PTO

INFORMATION DISCLOSURE STATEMENT BY APPLICANT

Complete if Known		
Application Number	12/561,138	
Filing Date	September 16, 2009	
First Named Inventor	William W.Y. Chu	
Art Unit	2435	
Examiner Name	Song, Hosuk	
Attorney Docket Number	ACQI-006/03US 310578-2053	

(Use as many sheets as necessary)

23

of

Sheet 23

	NON PATENT LITERATURE DOCUMENTS	
Cite No. ¹	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.	T ²
IC44	"Invalidity Chart for Base Reference U.S. Patent No. 5,187,645 (Spalding)", submitted by the Defendants in the U.S. District Court for the Eastern District of Texas, Case No. 6:09-cv-148-LED on March 1, 2010, 6 pages.	
IC45	"Defendants' Notice of Errata Relating to Defendants' P.R. 3-3 Invalidity Contentions," submitted by the Defendants in the U.S. District Court for the Eastern District of Texas, Case No. 6:09-cv-148-LED on March 1, 2010, 14 pages.	
IF01	"Exhibit 5 - Disclosure of Asserted Claims and Infringement Contentions", submitted by the Plaintiff in the U.S. District Court for the Eastern District of Texas, Case No. 6:09-cv-148-LED, 14 pages.	
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	IC44 IC45	Cite No.1 Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published. IC44 "Invalidity Chart for Base Reference U.S. Patent No. 5,187,645 (Spalding)", submitted by the Defendants in the U.S. District Court for the Eastern District of Texas, Case No. 6:09-cv-148-LED on March 1, 2010, 6 pages. IC45 "Defendants' Notice of Errata Relating to Defendants' P.R. 3-3 Invalidity Contentions," submitted by the Defendants in the U.S. District Court for the Eastern District of Texas, Case No. 6:09-cv-148-LED on March 1, 2010, 6 pages. IC45 "Defendants' Notice of Errata Relating to Defendants' P.R. 3-3 Invalidity Contentions," submitted by the Defendants in the U.S. District Court for the Eastern District of Texas, Case No. 6:09-cv-148-LED on March 1, 2010, 14 pages. IF01 "Exhibit 5 - Disclosure of Asserted Claims and Infringement Contentions", submitted by the Plaintiff in the U.S.

Examiner Signature	Date Considerer	

*EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant. ¹Applicant's unique citation designation number (optional). ²See Kinds Codes of USPTO Patent Documents at <u>www.usplo.gov</u> or MPEP 901.04. ³Enter Office that issued the document, by the two-letter code (WIPO Standard ST.3). ⁴For Japanese patent documents, the indication of the year of the reign of the Emperor must precede the serial number of the patent document. ⁵Kind of document by the appropriate symbols as indicated on the document under WIPO Standard ST. 16 if possible. ⁶Applicant is to place a check mark here if English language Translation is attached.

This collection of information is required by 37 CFR 1.97 and 1.98. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 2 hours to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.



ARTIFACT SHEET

Enter artifact number below. Artifact number is application number + artifact type code (see list below) + sequential letter (A, B, C ...). The first artifact folder for an artifact type receives the letter A, the second B, etc.. Examples: 59123456PA, 59123456PB, 59123456ZA, 59123456ZB

12561138SA

Indicate quantity of a single type of artifact received but not scanned. Create individual artifact folder/box and artifact number for each Artifact Type.

1	CD(s) containing: Image: Computer program listing computer program listing Image: Code: P Doc Code: Computer Artifact Type Code: P pages of specification Image: Code: P and/or sequence listing Image: Code: S Doc Code: Artifact Code: S Doc Code: Artifact Image: Code: S
	Stapled Set(s) Color Documents or B/W Photographs Doc Code: Artifact Artifact Type Code: C
	Microfilm(s) Doc Code: Artifact Artifact Type Code: F
	Video tape(s) Doc Code: Artifact Artifact Type Code: V
	Model(s) Doc Code: Artifact Type Code: M
	Bound Document(s) Doc Code: Artifact Artifact Type Code: B
	Confidential Information Disclosure Statement or Other Documents marked Proprietary, Trade Secrets, Subject to Protective Order, Material Submitted under MPEP 724.02, etc. Doc Code: Artifact Artifact Type Code X
	Other, description: Doc Code: Artifact Artifact Type Code: Z

March 8, 2004

		Substitute for		ERMINATIOI TO-875	N RECORD		Docket Number 61,138		ing Date 16/2009	To be Maile
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	SEARCH FEE (37 CFR 1.16(k), (i), (or (m))	N/A		N/A	N/A			N/A	
	EXAMINATION FE (37 CFR 1.16(o), (p),		N/A		N/A	N/A			N/A	
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	EPENDENT CLAIM CFR 1.16(h))			inus 3 = *		X \$ =			X \$ =	
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preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS

ADDRESS. SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450. If you need assistance in completing the form, call 1-800-PTO-9199 and select option 2.



UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE United States Patent and Trademark Office Address: COMMISSIONER FOR PATENTS P.O. Box 1450 Alexandria, Virginia 22313-1450 www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
12/561,138	09/16/2009	William W.Y. Chu	ACQI-006/03US 310578-2053	1717
58249 COOLEY LLP	7590 03/17/201	1	EXAM	IINER
ATTN: Patent	Group		SONG,	HOSUK
Suite 1100 777 - 6th Stree	t. NW		ART UNIT	PAPER NUMBER
WASHINGTO			2435	
			MAIL DATE	DELIVERY MODE
			03/17/2011	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

	Application No.	Applicant(s)
	12/561,138	CHU, WILLIAM W.Y.
Office Action Summary	Examiner	Art Unit
	HOSUK SONG	2435
The MAILING DATE of this communication app Period for Reply	pears on the cover sheet with the	ne correspondence address
 A SHORTENED STATUTORY PERIOD FOR REPLY WHICHEVER IS LONGER, FROM THE MAILING D/ Extensions of time may be available under the provisions of 37 CFR 1.13 after SIX (6) MONTHS from the mailing date of this communication. If NO period for reply is specified above, the maximum statutory period v Failure to reply within the set or extended period for reply will, by statute Any reply received by the Office later than three months after the mailing earned patent term adjustment. See 37 CFR 1.704(b). 	ATE OF THIS COMMUNICAT 36(a). In no event, however, may a reply b will apply and will expire SIX (6) MONTHS I , cause the application to become ABANDO	ION. e timely filed rom the mailing date of this communication. DNED (35 U.S.C. § 133).
Status		
 1) Responsive to communication(s) filed on <u>31 Ja</u> 2a) This action is FINAL. 2b) This 3) Since this application is in condition for alloward closed in accordance with the practice under E 	action is non-final. nce except for formal matters,	
Disposition of Claims		
 4) Claim(s) <u>14-60</u> is/are pending in the application 4a) Of the above claim(s) is/are withdraw 5) Claim(s) is/are allowed. 6) Claim(s) <u>14-60</u> is/are rejected. 7) Claim(s) is/are objected to. 8) Claim(s) are subject to restriction and/or 	wn from consideration.	
Application Papers		
 9) ☐ The specification is objected to by the Examine 10) ☑ The drawing(s) filed on <u>16 September 2009</u> is/a Applicant may not request that any objection to the Replacement drawing sheet(s) including the correct 11) ☐ The oath or declaration is objected to by the Ex 	are: a) \square accepted or b) \square ob drawing(s) be held in abeyance. tion is required if the drawing(s) is	See 37 CFR 1.85(a). objected to. See 37 CFR 1.121(d).
Priority under 35 U.S.C. § 119		
 12) Acknowledgment is made of a claim for foreign a) All b) Some * c) None of: 1. Certified copies of the priority document: 2. Certified copies of the priority document: 3. Copies of the certified copies of the priority application from the International Bureau * See the attached detailed Office action for a list 	s have been received. s have been received in Applic rity documents have been rece u (PCT Rule 17.2(a)).	cation No eived in this National Stage
Attachment(s) 1) Notice of References Cited (PTO-892) 2) Notice of Draftsperson's Patent Drawing Review (PTO-948) 3) Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date <u>1/31/11;12/16/10</u> . U.S. Patent and Trademark Office PTOL-326 (Rev. 08-06)	4) Interview Summ Paper No(s)/Ma 5) Notice of Inform 6) Other: ction Summary	

DETAILED ACTION

Reissue Applications

A supplemental reissue oath is needed as there have been amendments since the filing of the last oath. This solves the problem that a statement is needed that all errors corrected in this reissue arose without deceptive intent. The supplemental reissue oath/declaration must state that every error which was corrected in the reissue application not covered by the prior oath(s)/declaration(s) submitted in the application arose without any deceptive intention on the part of the applicant. A supplemental reissue oath/declaration is needed which states an error which is being relied upon to support the reissue since the error under 35 USC 251 stated in the prior reissue oath/declaration is not being corrected in the reissue application.

Claims 14-60 are rejected as being based upon a defective reissue oath/declaration under 35 U.S.C. 251 as set forth above. See 37 CFR 1.175.

Response to Applicant's Arguments

Applicant's arguments regarding broadening claims in a continuing reissue application according to MPEP 1412.03(IV) is persuasive. However, a supplemental reissue oath is needed as there have been amendments since the filing of the last oath. Claims 14-60 are rejected as being based upon a defective reissue oath/declaration under 35 U.S.C. 251 as set forth above. See 37 CFR 1.175.

Information Disclosure Statement

The information disclosure statement filed 1/31/11 fails to comply with the provisions of 37 CFR 1.97, 1.98 and MPEP 609 because some of the cited document(s) do not have accompanying dates (please see attached 1449 for the specific documents). It has been placed in the application file, but some of the information referred to therein has not been considered as to the merits. Applicant is advised that the date of any re-submission of any item of information contained in this information disclosure statement or the submission of any missing element(s) will be the date of submission for purpose of determining

Application/Control Number: 12/561,138 Art Unit: 2435

compliance with the requirements based on the time of filing the statement, including all certification requirements for statements under 37 CFR 1.97(e). See MPEP 609.05(a).

Conclusion

THIS ACTION IS MADE FINAL. Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

USPTO Contact Information

Any inquiry concerning this communication or earlier communications from the examiner should be directed to HOSUK SONG whose telephone number is 5712723857. The examiner can normally be reached on mon-fri.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, KIM VU can be reached on 5712723859. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Application/Control Number: 12/561,138 Art Unit: 2435

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pairdirect.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/HOSUK SONG/ Primary Examiner, Art Unit 2435

	Index of Claim	S		on/Control No.		Applicant(s)/Pat Reexamination	
			12/561,13 Examiner	38 r		CHU, WILLIAM	W.Y.
			HOSUK			2435	
Г	√ Rejected –	(Through numera	al)	Non-Elected		Appeal	
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Claim	Date	Claim	Date		laim	Date	
Final Original	3/8/11	Final Original 3/8/11		Final	Original		
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Part of Paper No. 20110308



Application/Control No.	Applicant(s)/Patent under Reexamination		
12/561,138	CHU, WILLIAM	W.Y.	
Examiner	Art Unit		
HOSUK SONG	2435		

	SEAR	CHED	
Class	Subclass	Date	Examiner
726	2-9 16-21	3/8/2011	HS
713	182-183	3/8/2011	HS

INTERFERENCE SEARCHED						
Class	Subclass	Date	Examiner			

SEARCH NOTES (INCLUDING SEARCH STRATEGY)					
	DATE	EXMR			
EAST, foreign patent database IBM TDB	3/8/2011	HS			
NPL	3/8/2011	HS			

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Part of Paper No. 20110308

EAST Search History

EAST Search History (Prior Art)

Ref #	Hits	Search Query	DBs	Default Operator	Plurals	Time Stamp
S94	2343	726/2.ccls.	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2011/03/08 13:02
S95	2379	726/3.ccls.	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2011/03/08 13:02
S96	3429	726/4.ccls.	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2011/03/08 13:02
S97	2097	726/5.ccls.	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2011/03/08 13:02
S98	1279	726/6.ccls.	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2011/03/08 13:02
S99	1151	726/7.ccls.	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2011/03/08 13:02
S100	457	726/8.ccls.	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2011/03/08 13:02
S101	1016	726/9.ccls.	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2011/03/08 13:02

S102	463	726/16.ccls.	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2011/03/08 13:02
S103	762	726/17.ccls.	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2011/03/08 13:02
S104	504	726/18.ccls.	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2011/03/08 13:02
S105	752	726/19.ccls.	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2011/03/08 13:02
S106	474	726/20.ccls.	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2011/03/08 13:02
S107	900	726/21.ccls.	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2011/03/08 13:02
S108	2223	713/182.ccls.	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2011/03/08 13:02
S109	889	713/183.ccls.	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2011/03/08 13:02
S110	310	(tamper adj3 resistant or access \$4 or securit\$4) and (low near2 voltage near5 diff \$7 near7 signal\$4)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2011/03/08 13:04

S111	Ο	(tamper adj3 resistant or access \$4 or securit\$4) and (low near2 voltage near5 diff \$7 near7 signal\$4) and unidirect\$4	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2011/03/08 14:14
S112	0	(tamper adj3 resistant or access \$4 or securit\$4) and (low near2 voltage near5 diff \$7 near7 signal\$4) and serial adj3 bit adj5 channel	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2011/03/08 14:58
S113	188	(tamper adj3 resistant or access \$4 or securit\$4) and (low near2 voltage near5 diff \$7 near7 signal\$4) and diff\$7 near3 signal\$4	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2011/03/08 14:59
S114	16	(tamper adj3 resistant or access \$4 or securit\$4) and (low near2 voltage near5 diff \$7 near7 signal\$4) and diff\$7 near3 signal\$4 and PCI	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2011/03/08 15:03
S115	0	(tamper adj3 resistant or access \$4 or securit\$4) and (low near2 voltage near5 diff \$7 near7 signal\$4) and 726/2.ccls.	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2011/03/08 15:04
S116	0	(tamper adj3 resistant or access \$4 or securit\$4) and (low near2 voltage near5 diff \$7 near7 signal\$4) and 726/3.ccls.	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2011/03/08 15:04

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S117	0	(tamper adj3 resistant or access \$4 or securit\$4) and (low near2 voltage near5 diff \$7 near7 signal\$4) and 726/4.ccls.	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2011/03/08 15:04
S118	0	(tamper adj3 resistant or access \$4 or securit\$4) and (low near2 voltage near5 diff \$7 near7 signal\$4) and 726/5.ccls.	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2011/03/08 15:05
S119	0	(tamper adj3 resistant or access \$4 or securit\$4) and (low near2 voltage near5 diff \$7 near7 signal\$4) and 726/6.ccls.	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2011/03/08 15:05
S120	0	(tamper adj3 resistant or access \$4 or securit\$4) and (low near2 voltage near5 diff \$7 near7 signal\$4) and 726/7.ccls.	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2011/03/08 15:05
S121	0	(tamper adj3 resistant or access \$4 or securit\$4) and (low near2 voltage near5 diff \$7 near7 signal\$4) and 726/8.ccls.	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2011/03/08 15:05
S122	0	(tamper adj3 resistant or access \$4 or securit\$4) and (low near2 voltage near5 diff \$7 near7 signal\$4) and 726/9.ccls.	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2011/03/08 15:05
S123	0	(tamper adj3 resistant or access \$4 or securit\$4) and (low near2 voltage near5 diff \$7 near7 signal\$4) and 726/16.ccls.	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2011/03/08 15:06

S124	0	(tamper adj3 resistant or access \$4 or securit\$4) and (low near2 voltage near5 diff \$7 near7 signal\$4) and 726/167ccls.	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2011/03/08 15:06
S125	0	(tamper adj3 resistant or access \$4 or securit\$4) and (low near2 voltage near5 diff \$7 near7 signal\$4) and 726/17ccls.	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2011/03/08 15:06
S126	0	(tamper adj3 resistant or access \$4 or securit\$4) and (low near2 voltage near5 diff \$7 near7 signal\$4) and 726/17.ccls.	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2011/03/08 15:06
S127	0	(tamper adj3 resistant or access \$4 or securit\$4) and (low near2 voltage near5 diff \$7 near7 signal\$4) and 726/18.ccls.	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2011/03/08 15:06
S128	0	(tamper adj3 resistant or access \$4 or securit\$4) and (low near2 voltage near5 diff \$7 near7 signal\$4) and 726/19.ccls.	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2011/03/08 15:06
S129	0	(tamper adj3 resistant or access \$4 or securit\$4) and (low near2 voltage near5 diff \$7 near7 signal\$4) and 726/20.ccls.	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2011/03/08 15:06
S130	0	(tamper adj3 resistant or access \$4 or securit\$4) and (low near2 voltage near5 diff \$7 near7 signal\$4) and 726/21.ccls.	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2011/03/08 15:06

S131	0	\$4 or securit\$4) and (low near2	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2011/03/08 15:08
S132	0	resistant or access \$4 or securit\$4) and (low near2	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2011/03/08 15:08

3/8/2011 9:25:50 PM

Doc code: IDS Doc description: Information Disclosure Statement (IDS) Filed PTO/SB/08a (01-10) Approved for use through 07/31/2012. OMB 0651-0031 U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE

Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it contains a valid OMB control number.

	Application Number		12561138	
	Filing Date		2009-09-16	
INFORMATION DISCLOSURE	First Named Inventor Williar		iam Chu	
STATEMENT BY APPLICANT (Not for submission under 37 CFR 1.99)	Art Unit		2435	
	Examiner Name	Hosul	< Song	
	Attorney Docket Number		ACQI-006/03US 310578-2053	

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INFORMATION DISCLOSURE Filing Date 2009 STATEMENT BY APPLICANT First Named Inventor William Chu (Not for submission under 37 CFR 1.99) Art Unit 2435 Examiner Name Hosuk Song

English language translation is attached.

	Application Number		12561138	
	Filing Date		2009-09-16	
	First Named Inventor Willia		m Chu	
	Art Unit		2435	
	Examiner Name Hosuk Attorney Docket Number		< Song	
			ACQI-006/03US 310578-2053	

	1	PC MAGAZINE, "Think Modular" (06-10-1997)								
	2	LIQUORMAN, "Convergent Technologies Had This Idea" (12/05/1997)								
	3	BERST, "Hope For The Modular PCs We all Really Want" (12/05/1997)								
	4	BOYD-MERRITT, "Upgradable-PC Effort Takes Divergent Paths" (EE Times 1997) http://techweb.cmp/com/eet/news/97/949news/effort.html								
	5	FAEGRE, et al., "Unisys' Best-Kept Secret Is An Operating System Built For Distributed Business Applications." BYTE (12/1994)								
6 SPANG, "Component House: Design Technology For 'PCs in a snap' NeoSystems Offers Building Blocks" [
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Standard S	T.3). ³ F	USPTO Patent Documents at <u>www.USPTO.GOV</u> or MPEP 901.04. ² Enter office that issued the document, by the two-letter or Japanese patent documents, the indication of the year of the reign of the Emperor must precede the serial number of the pay the appropriate symbols as indicated on the document under WIPO Standard ST.16 if possible. ⁵ Applicant is to place a che	atent document.							



Three alternative schemes for secure Virtual Private Network (VPN) deployment over the Universal Mobile Telecommunication System (UMTS) are proposed and analyzed. The proposed schemes enable a mobile node voluntarily establish an IPsec-based secure ...

Keywords: IKE, IPsec, NAT, UMTS, VPN, mobile Internet, privacy, security

6 Mobile communication security controllers an evaluation paper

Keith E. Mayes, Konstantinos Markantonakis

August 2008 Information Security Tech. Report , Volume 13 Issue 3 Publisher: Elsevier Advanced Technology Publications

Bibliometrics: Downloads (6 Weeks): n/a, Downloads (12 Months): n/a, Downloads (Overall): n/a, Citation Count

Cellular communication via a traditional mobile handset is a ubiquitous part of modern life and as device technology and network performance continues to advance, it becomes possible for laptop computers, Persona Digital Assistants [PDAs; Note abbreviations ...

7 Integrating hardware and software information flow analyses Colin.u. Fidge, Diane Corney.



June 2009 LCTES '09: Proceedings of the 2009 ACM SIGPLAN/SIGBED conference on Languages, compilers, at tools for embedded systems

Publisher: ACM ³ <u>Request Permissions</u>

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Security-critical communications devices must be evaluated to the highest possible standards before they can deployed. This process includes tracing potential information flow through the device's electronic circuitry, for each of the device's operating ...

Keywords: communications devices, embedded software, information security evaluation

Also published in:

June 2009 SIGPLAN Notices Volume 44 Issue 7

8 Semantic context aware security policy deployment

Stere Preda, Frédéric Cuppens, Nora Cuppens, Soulahia, Joaquin G. Alfaro, Laurent Toutain, Yehia Eliakaiby March 2009 ASI ACCS '09: Proceedings of the 4th International Symposium on Information, Computer, and Communications Security

Publisher: ACM 👋 <u>Request Permissions</u>

Full text available: 🐯 <u>Fdf</u> (1.54 MB)

Bibliometrics: Downloads (6 Weeks): 8, Downloads (12 Months): 155, Downloads (Overall): 335, Citation Count:

The successful deployment of a security policy is closely related not only to the complexity of the security requirements but also to the capabilities/functionalities of the security devices. The complexity of the security requirements is additionally ...

Keywords: PDP, PEP, access control, network security

9 A secure pervasive environment

<u>Patrick G. McLean</u>

January 2003 ACSW Frontiers '03: Proceedings of the Australasian information security workshop conference on ACSW frontiers 2003 - Volume 21, Volume 21 Publisher: Australian Computer Society, Inc.

Full text available: 🔀 🖽 (240.64 KB)

Bibliometrics: Downloads (6 Weeks): 0, Downloads (12 Months): 50, Downloads (Overall): 1261, Citation Count:

This paper explores the complications encountered when attempting to create a secure pervasive computing environment. The model introduced in this paper is primarily conceptual. The chosen environment is built around a shared space containing a classified ...

 10
 A spontaneous ad hoc network to share WWW access

 Raquel Lacuesta, Jaime Lloret, Miguel Garcia, Lourdes Peñalver

 April 2010
 EURASIP Journal on Wireless Communications and Networking , Volume 2010

 Publisher: Hindawi Publishing Corp.

Full text available: 🔊 Publisher Site , 🕅 PDF (1.09 MB)

Bibliometrics: Downloads (6 Weeks): 0, Downloads (12 Months): 0, Downloads (Overall): 0, Citation Count: 0

In this paper, we propose a secure spontaneous ad-hoc network, based on direct peer-to-peer interaction, to grant a quick, easy, and secure access to the users to surf the Web. The paper shows the description of our proposal, the procedure of the nodes ...

11 An efficient end-to-end security mechanism for iP multimedia subsystem Chi-Yuan Chen, Tin-Yu Wu, Yueh-Min Huang, Han-Chieh Chao

December 2008 Computer Communications , Volume 31 Issue 18

Publisher: Butterworth-Heinemann

Bibliometrics: Downloads (6 Weeks): n/a, Downloads (12 Months): n/a, Downloads (Overall): n/a, Citation Count

With the rapid growth of the Internet and wireless communications, people make extensive use of portable wireless devices to access information such as voice, data and multimedia, any time from any place, enjoying ubiquitous services. IP multimedia subsystem ...

Keywords: End-to-end security, IP multimedia subsystem (IMS), Key exchange

12 You go to elections with the voting system you have: stop-gap miligations for deployed voting systems J. Alax Halderman. Eric Rescords. Hovay, Shacham, David Wagner.

July 2008 EVT'08: Proceedings of the conference on Electronic voting technology Publisher: USENIX Association

Bibliometrics: Downloads (6 Weeks): n/a, Downloads (12 Months): n/a, Downloads (Overall): n/a, Citation Count

In light of the systemic vulnerabilities uncovered by recent reviews of deployed e-voting systems, the surest way to secure the voting process would be to scrap the existing systems and design new ones. Unfortunately, engineering new systems will take ...

- 13 Specifications of a high-level conflict-free firewall policy language for multi-domain networks
- Bin Zhang, Ehab Al-Shaer, Radha Jagadeesan, James Riely, Corin Pitcher
- June 2007 SACMAT '07: Proceedings of the 12th ACM symposium on Access control models and technologies

Publisher: ACM 👋 Request Permissions

Full text available: 🔀 <u>Fdi</u> (370.35 KB)

Bibliometrics: Downloads (6 Weeks): 5, Downloads (12 Months): 81, Downloads (Overall): 570, Citation Count: 7

Multiple firewalls typically cooperate to provide security properties for a network, despite the fact that these firewalls are often spatially distributed and configured in isolation. Without a global view of the network configuration, such a system ...

Keywords: conflicts free, firewall, policy language

14 A study on the available biometric technologies used in order to control security in physical access Ricardo Janes, Augusto F. Brandão, Eduardo M. Dias

June 2010 WSEAS Transactions on Systems and Control, Volume 5 Issue 6 Publisher: World Scientific and Engineering Academy and Society (WSEAS)

Bibliometrics: Downloads (6 Weeks): n/a, Downloads (12 Months): n/a, Downloads (Overall): n/a, Citation Count

The control of the physical access in automated security systems, like banks, ports, airports and military area: is essential to guarantee the financial security of the institutions and to prevent to the possibility of accomplishment of terrorist acts...

Keywords: access control, biometric technology, biometry, security systems, smart buildings

- 15 Towards self-authenticable smart cards
 - Joaquin Torres, Antonio Izquierdo, Jose M. Sierra, Arturo Ribagorda

September 2006 Computer Communications , Volume 29 Issue 15

Publisher: Butterworth-Heinemann

Bibliometrics: Downloads (6 Weeks): n/a, Downloads (12 Months): n/a, Downloads (Overall): n/a, Citation Count

Traditionally, the smart cards have been seen as security devices, but as soon as they could be integrated into distributed and networked environments their vulnerabilities could be attempted and countermeasures against new security threats in an open-access ...

Keywords: Authentication protocol, Non-split supplicant, Smart card security

6	Research of utility prepayment system based on wireless communication
	<u>Pan Tie-Jun, Zheng Lei-na, Zhang Hua-jun, Fang Chen-bin</u>
	January 2009 W SEAS TRANSACTIONS on COMMUNICATIONS, Volume 8 Issue 1

Publisher: World Scientific and Engineering Academy and Society (WSEAS)

Bibliometrics: Downloads (6 Weeks): n/a, Downloads (12 Months): n/a, Downloads (Overall): n/a, Citation Count

This paper seeks to clarify differences and similarities among impressive array of radio access technologies which can be used in utility prepayment, analyzes the requirements of wireless prepayment utility meter system. It present a set of mobile prepayment ...

Keywords: 3G, OTA, RS485, WiMax, meter, mobile payment, zigbee

- 17 Towards network security policy generation for configuration analysis and testing
- Taghrid Samak, Adel El-Atawy, Ehab Ai-Shaer
 Navember 2000, Parts 2 and 100; Parts and Inc.
- November 2009 SafeConfig '09: Proceedings of the 2nd ACM workshop on Assurable and usable security configuration

Publisher: ACM Sequest Permissions

Full text available: 🐯 <u>Pdf</u> (456.93 KB)

Bibliometrics: Downloads (6 Weeks): 1, Downloads (12 Months): 110, Downloads (Overall): 138, Citation Count:

Access-control lists are an essential part in the security framework of any system. Researchers are always in need to have a repository of ready made policies for conducting research and development. Such policies, especially firewall policies which ...

Keywords: policy generation, policy grammar, security policy

18 Mobile payment system for prepayment meter

<u>Pan Tie-Jun, Zheng Lei-Na</u>

November 2006 **ISP'06:** Proceedings of the 5th WSEAS International Conference on Information Security and Privacy

Publisher: World Scientific and Engineering Academy and Society (WSEAS)

Bibliometrics: Downloads (6 Weeks): n/a, Downloads (12 Months): n/a, Downloads (Overall): n/a, Citation Count

We present an approach in which the payment system of PM is enhanced by supporting mobile access without smart card. PM with embedded ESAM providing encrypting ability and protecting private data is connected to t mobile device by adaptable communication ...

Keywords: GPRS, IrDA, MIDP, OTA, SIM, mobile payment

19 Towards Ubiquitous e-Custom Services

Liana Razmerita, Niels Biorn-Andersen November 2007 WI '07: Proceedin

er 2007 WI '07: Proceedings of the IEEE/WIC/ACM International Conference on Web Intelligence

Publisher: IEEE Computer Society

Full text available: 🗒 Pdf (563.80 KB)

Bibliometrics: Downloads (6 Weeks): 4, Downloads (12 Months): 36, Downloads (Overall): 224, Citation Count: 1

In this paper we present an advanced e-custom system pilot designed to address strategic goals for future custom systems. Future custom systems will support simplified paperless trade procedures, prevent potential security threats and counterfeit tax ...

- 20 Proceedings of the 3rd ACM workshop on Assurable and usable security configuration
 - Tony Sager, Gali-Joon Ahn, Krishna Kant, Heather Richter Lipford

October 2010 SafeConfig '10: Proceedings of the 3rd ACM workshop on Assurable and usable security configuration

Publisher: ACM

Bibliometrics: Downloads (6 Weeks): n/a, Downloads (12 Months): n/a, Downloads (Overall): n/a, Citation Count

It is our great pleasure to welcome you to the 3rd ACM Workshop on Assurable & Usable Security Configuratio 2010 (SafeConfig '10) held in conjunction with the 17th ACM Conference on Computer and Communications Security in Chicago, IL. The ...

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Complete if Known						
Application Number	12/561,138					
Filing Date	September 16, 2009					
First Named Inventor	William W.Y. Chu					
Art Unit	2435					
Examiner Name	Song, Hosuk					
Attorney Docket Number	ACQI-006/03US 310578-2053					

			U.S. PATENT D	OCUMENTS	
Examiner Initials*	Cite No. ¹	Document Number Number-Kind Code ^{2 (if known)}	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear
	A105	4,141,068	02-20-1979	Mager et al.	
	A024	4,228,496	10-14-1980	Katzman et al.	
	A001	4,453,215	06-05-1984	Reid	
	A104	4,670,837	06-02-1987	Sheets	
	A025	4,680,674	07-14-1987	Moore	
	A026	4,760,276	07-26-1988	Lethellier	
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	AO003	5,103,446	04-07-1992	Fischer	
	A023	5,187,645	02-16-1993	Spalding et al.	
	AO004	5,191,581	03-02-1993	Woodbury et al.	
	A032	5,282,247	01-25-1994	McLean et al.	
	AK002	5,293,487	03-08-1994	Russo et al.	
	A007	5,325,517	06-28-1994	Baker et al.	
	A015	5,339,408	08-16-1994	Bruckert et al.	
	A037	5,430,607	07-04-1995	Smith	
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•	A039	5,436,902	07-25-1995	McNamara et al.	
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	AO006	5,572,441	11-05-1996	Boie	
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	AR001	5,590,377	12-31-1996	Smith	
	A047	5,673,172	09-30-1997	Hastings et al.	
	A016	5,680,536	10-21-1997	Tyuluman	

Examiner Signature	/Hosuk Song/	Date Considered	03/08/2011

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23

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Sheet 2

Complete if KnownApplication Number12/561,138Filing DateSeptember 16, 2009First Named InventorWilliam W.Y. ChuArt Unit2435Examiner NameSong, HosukAttorney Docket NumberACQI-006/03US 310578-2053

			U. S. PATENT D	OCUMENTS	
Examiner Initials*	Cite No.1	Document Number Number-Kind Code ^{2 (if known)}	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear
	A050	5,708,840	01-13-1998	Kikinis et al.	
	A052	5,724,591	03-03-1998	Hara et al.	
	A053	5,737,194	04-07-1998	Hopkins et al.	· · · · · · · · · · · · · · · · · · ·
	A107	5,737,524	04-07-1998	Cohen et al.	
	AO008	5,751,711	05-12-1998	Sakaue	· · · · · · · · · · · · · · ·
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INFORMATION DISCLOSURE STATEMENT BY APPLICANT

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of

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Co	mplete if Known
Application Number	12/561,138
Filing Date	September 16, 2009
First Named Inventor	William W.Y. Chu
Art Unit	2435
Examiner Name	Song, Hosuk
Attorney Docket Number	ACQI-006/03US 310578-2053

		,	U. S. PATENT D	OCUMENTS	
Examiner	Cite No.1	Document Number	Publication Date	Name of Patentee or	Pages, Columns, Lines, Where
Initials*		Number-Kind Code ^{2 (if known)}	MM-DD-YYYY	Applicant of Cited Document	Relevant Passages or Relevant Figures Appear
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INFORMATION DISCLOSURE STATEMENT BY APPLICANT (Use as many sheets as necessary)

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Complete if Known **Application Number** 12/561,138 Filing Date September 16, 2009 First Named Inventor William W.Y. Chu Art Unit 2435 Examiner Name Song, Hosuk ACQI-006/03US 310578-2053 Attorney Docket Number

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Examiner Initials*	Cite No. ¹	Foreign Patent Document Country Code ³ "Number ⁴ "Kind Code ⁵ (<i>if known</i>)		Name of Patentee or Applicant of Cited Document	Pages, Columns; Lines, Where Relevant Passages or Relevant Figures Appear	۲°
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Examiner Signature	/Hosuk Song/	Date Considered	03/08/2011

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			Application Number	12/561,138	
	INFORMATION DIS		Filing Date	September 16, 2009	
			First Named Inventor	William W.Y. Chu	
	STATEMENT BY A		Art Unit	2435	
	(Use as many sheets as n	ecessary)	Examiner Name	Song, Hosuk	
Shoot	5	of 23	Attorney Docket Number	ACQI-006/03US 310578-2053	

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Examiner Signature	/Hosuk Song/	Date Considered	03/08/2011

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INFORMATION DISCLOSURE STATEMENT BY APPLICANT

2	Complete if Known			
	Application Number	12/561,138		
ĺ	Filing Date	September 16, 2009		
	First Named Inventor	William W.Y. Chu		
	Art Unit	2435		
	Examiner Name	Song, Hosuk		
	Attorney Docket Number	ACQI-006/03US 310578-2053		

(Use as many sheets as necessary)

23

of

Sheet 6

		NON PATENT LITERATURE DOCUMENTS	
Examiner Initials*	Cite No. ^{1.}	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.	T
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INFORMATION DISCLOSURE STATEMENT BY APPLICANT

Complete if Known				
Application Number	12/561,138			
Filing Date	September 16, 2009			
First Named Inventor	William W.Y. Chu			
Art Unit	2435			
Examiner Name	Song, Hosuk			
Attorney Docket Number	ACQI-006/03US 310578-2053			

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of 23

Sheet 8

		Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the	Т
Examiner Initials*	Cite No. ¹	item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.	Т
	C057	Eversys Corporation, WebView 8000 version 1.1 User's Guide, Web-Based Management Software fo the	
		EVERSYS System 8000 Consolidated Server, Revision A-November 1998, Revision B-December 1998, 56 pages.	
	C058	Eversys Corporation, S8000 Single Module Body Assemby, October 9, 1998, 9 pages.	
	C059	Eversys CAPserver Product Brief [online], (undated), [retrieved on November 16, 2009], Retrieved from the Internet: <url: 19961104093115="" capbrief.htm="" http:="" web="" web.archive.org="" www.eversys.com="">, 10 pages.</url:>	
	C060	Eversys CAPcard 9500/sa Product Brief [online], (undated), [retrieved on November 16, 2009], Retrieved from the Internet: <url: 19961104093144="" brief.htm="" cc95sa="" http:="" web="" web.archive.org="" www.eversys.com="">, 3 pages.</url:>	Γ
	C061	Evergreen Systems; Inc., "GAPserver, The Communication/Application server for local area networks," Product Smide; (undated), 18 pages	T
	C062	PHILLIPS, J., "9800 Disk Card Design Specification," May 26, 1998, White Cross Systems Limited, pages 1-44.	T
	C063	PHILLIPS, J., "9800 Disk Card Layout Specification," April 6, 1998, White Cross Systems Limited, pages 1-22.	T
	C064	FEAKES, L., "Disk Connector Card Functional Requirement Specification," January 14, 1998, White Cross Systems Limited, pages 1-4.	Ī
	C065	FEAKES, L., "Disk Connector Card Layout Specification," January 14, 1998, White Cross Systems Limited, pages 1-6.	
	C069	BURROW, M., WhiteCross Data Exploration, "A Technical Overview of the WXDES/9800," March 2, 1999, Revision 2.00, White Cross Systems Limited, pages 1-90.	ſ
	C072	BURROW, M., WhiteCross Data Exploration, "A Technical Overview of the WXDES/9800," April 21, 1999, White Cross Systems Limited, 222 pages.	T
	C073	KHAN, M. F., "Ethernet Switch Card Design Specification," March 8, 2001, White Cross Systems Limited, pages 1-32.	
	C074	KHAN, M. F., "Ethernet Switch Card Layout Specifications," March 8, 2001, pages 1-31.	Γ
	C075	SMITH, B., Processor Backplane Functional Requirement Specification, July 31, 1997, White Cross Systems Limited, pages 1- 11.	
	C076	SMITH, B., "Processor Backplane Design Specification," February 3, 1998, White Cross Systems Limited, pages 1-16.	
	C077	SMITH, B., "Processor Backplane Layout Specification," November 12, 1997, White Cross Systems Limited, pages 1-7.	T
	C078	PHILLIPS, J., "9800 Processor Card Design Specification," February 25, 1998, White Cross Systems Limited, pages 1-41.	T

(Examiner Signature	/Hosuk Song/	Date Considered	03/08/2011

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Filing Date		September 16, 2009			
	First Named Inventor	William W.Y. Chu			
Art Unit		2435			
	Examiner Name	Song, Hosuk			
	Attorney Docket Number	ACQI-006/03US 310578-2053			

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Sheet 9

		NON PATENT LITERATURE DOCUMENTS	
Examiner Initials*	Cite No. ¹	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.	T
	C079	PHILLIPS, J., "9800 Processor Card Layout Specification," September 29, 1997, White Cross Systems Limited, pages 1-13.	
	C080	MIASTKOWSKI, S. (Editor), "A Whate of a System," BYTE, August 1991, 4 pages, Vol. 16, No. 8.	Γ
	C081	Advanced Micro Devices, Inc., "AMD-K6-III Processor Data Sheet," 21918B/0, October 1999, 326 pages.	
	C082	Black Box Corporation, "Black Box Serve Switch Duo," Black Box Network Services Manual, July 1998, 52 pages.	
	C083	Cisco Systems, Inc., "Cisco AS5800 Universal Access Server Dial Shelf Controller Card Installation and Replacement," Doc. No. 78-4653-02, 1997, 28 pages.	
	C084	Digital Equipment Corporation, "DIGITAL AlphaServer 4000 and 4100 systems," [Brochure], 1998, 4 pages.	
	C089	EVERSYS, "CAPserver Product Brief" [online], [retrieved on 11-16-2009], Retrieved from the Internet: <url: http://web.archieve.org/web/19961104093115/www.eversys.com/CAPbrief.htm>, 10 pages.</url: 	
	C090	EVERSYS, "CAPcard 9500/sa Product Brief," [online], [retrieved on 11-16-2009], Retrieved from the Internet: 	
	C091	Evergreen Systems; Inc., "CAPserver, The Communication/Application server for local-area networks," Product Guido; (undeted); 18 pages.	
	C094	GROW, R. et al., "Gigabit Media Independent Interface Proposal," November 11, 1996, IEEE 802.3Z, Vancouver, 22 pages.	'
	C099	Intel, "Pentium® II Processor at 350 MHz, 400 MHz, and 450 MHz, Datasheet," Order Number 243657-003, August 1998, 83 pages.	
	C100	ELLIS, S., "IRIS FailSafe™ Administrator's Guide," Document Number 007-3109-003, April 6, 1997, 212 pages.	
	C102	NEC, "Server HX4500 User's Guide," PN: 456-00005-000, December 1998, 160 pages.	
	C103	Novell, Inc., "Novell's NetWare 4.1 Momentum Continues - NetWare 4 Now World's Best-Selling Network Operating System," [online], March 21, 1996, [retrieved on November 16, 2009]. Retrieved from the Internet: <url: 03="" 1996="" archive="" http:="" news="" pr96056.html="" press="" www.novell.com="">, 2 pages.</url:>	
	C104	Chepter-7: Maintaining the NetWare Server, "Supervising the Network," (undated), pages 514-517.	Γ
	C105	Ghapter 7: Designing a Data Protection Plan, (undated), pages 170-171.	
	C106	Geneepte, Diek Briver and Bisk Buplexing, (undated), pages 82-63.	
	C107	Network Engines, "P6000EXP Fault-tolerant Load-balanced Clustered Server," 1997, 3 pages.	
	C110	Sun Microsystems Computer Company, "Sun™ Enterprise™ 250 Server Owner's Guide," June 1998, Part No. 805-5160-10, Revision A, 324 pages.	
	C111	Sun Microsystems, Inc., "UltraSPARC™ -II CPU Module, Datasheet 400 MHz CPU, 2.0 MP E-Cache," July 1999, 28 pages.	

Examiner Signature	/Hosuk Song/		Date Considered	03/08/2011	

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	Complete if Known				
	Application Number	12/561,138			
	Filing Date	September 16, 2009			
	First Named Inventor	William W.Y. Chu			
	Art Unit	2435			
	Examiner Name	Song, Hosuk			
	Attorney Docket Number	ACQI-006/03US 310578-2053			
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of 23

Sheet 10

Examiner Initials*	er Cite No. ¹ Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.		T ²
	C112	Sun Microsystems, Inc., White Paper, "Netra™ ft 1800," April 1999, Revision 09, 50 pages.	Γ
	C113	Compaq Computer Corporation, et al., "Universal Serial Bus Specification," September 23, 1998, Revision 1.1, 327 pages.	
	C114	Compaq Computer Corporation, et al., "Universal Serial Bus Specification," April 27, 2000, Revision 2.0, 650 pages.	
<u>.</u>	C115	Silicon Graphics International, "Additional Information for: IRIS FailSafe Administrator's Guide (IRIX 6.4)," [online], Document Number: 007-3109-003, Published April 6, 1997, [retrieved on November 5, 2009], Retrieved from the Internet: <url: <u="">http://techpubs.sgi.com/library/tpl/cgi- bin/summary.cgi?coll=0640&db=bks&docnumber=>, 2 pages.</url:>	
	C116	Origin and Onyx Theory of Operations Manual, Document Number 007-3439-002, 1997, Silicon Graphics, Inc., 124 pages.	
·	C117	QuantumNet, Inc., QuantumNet 6000 Sharing Modules [online], 1996 [retrieved on November 16, 2009], Retrieved from the Internet: <url: http://web.archive.org/web/19971011194326/www.quantumnet.com/dsq60xx.htm>, 3 pages.</url: 	
	C118	JL ChatCom, Inc., "ChatTwin," [retrieved on December 2, 2009], JL ChatCom, Inc., ChatterBox Communications and Server Solutions [online], Retrieved from the Internet: <url: http://web.archive.org/web/19970104222644/www.jlchatcom.com/chattwin.htm>, 2 pages.</url: 	
	C119	EVERSYS, "Welcome to EverSys" [online], [retrieved on 11-16-2009], Retrieved from the Internet: <url: http://web.archieve.org/web/19961104092834/www.eversys.com/index2.htm>, 1 page.</url: 	
	C120	EVERSYS, "Products" [online], [retrieved on 11-16-2009], Retrieved from the Internet: <url: http://web.archieve.org/web/19961104093103/www.eversys.com/prodinfo.htm>, 2 pages.</url: 	
	C121	"Microsoft Press Computer Dictionary, Third Edition," Microsoft Press, 1997, pages 199 and 332, Kim Fryer ed.	
	C122 ⁻	Excerpt from "Microsoft Computer Dictionary, 5th Edition", Microsoft Press, 2002, pages 96 and 547	
	C123	Excerpt from IEEE 100: The Authoritative Dictionary of IEEE Standards Terms (7th Ed., 2000), pages 78, 79 and 128	
	C124	ANDERSON, C.R. et al., "IEEE 1355 HS-Links: Present Status and Future Prospects," [online], 1998, [retrieved on 08-11-2010], Retrieved from the Internet: <url: http://www94.web.cern.ch/HIS/dshs/publications/wotug21/hslink/pdf/hslinkpaper.pdf>, 14 pages.</url: 	
	C125	MAMAKOS, L. et al., "Request for Comments 2516 - A method for Transmitting PPP Over Ethernet (PPPoE)," [online], 1999, [retrieved on 08-18-2010], Retrieved from the Internet: <url: html="" http:="" rfc2516="" ttols.ietf.org="">, 35 pages.</url:>	

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First Named Inventor	William W.Y. Chu			
Art Unit	2435			
Examiner Name	Song, Hosuk			
Attorney Docket Number	ACQI-006/03US 310578-2053			

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Sheet 11

Examiner Initials*	Cite No. ¹	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.	Т
	C126	HAAS, S., "The IEEE 1355 Standard: Developments, Performance and Application in High Energy Physics," Thesis for degree of Doctor of Philosophy, University of Liverpool, December 1998, 138 pages.	
	C127	"IEEE Std 1355-1995 Standard for Heterogeneous InterConnect (HIC)," Open Micro-processor systems Initiative (OMI), [online], October 30, 1998, [retrieved on 08-06-2010], Retrieved from the Internet: <url: http://grouper.ieee.org/groups/1355/index.html>, 6 pages.</url: 	
	C128	GALLES, M., "Spider: A Hide-Speed Network Interconnect," IEEE Micro, 1997, pp. 34-39. (6 pages)	
	C129	Excerpt from "Microsoft Computer Dictionary, 4th Edition", Microsoft Press, 1999, pages 184-85, 241, 432 (7 pages)	
	C130	Excerpt from "Microsoft Computer Dictionary, 4th Edition", Microsoft Press; 1999, pages 40, 241, 432 (6 pages)	Γ
	C131	Excerpt from IEEE 100: The Authoritative Dictionary of IEEE Standards Terms (7th Ed., 2000), pages 181,304 and 771.	ſ
C132 "Family of VME Technology Specifications," [online], date unknown, [retrieved on 12-29-2010], Retrie the Internet: <url: http:="" specifications.html="" www.vita.com="">, 1 page.</url:>		"Family of VME Technology Specifications," [online], date unknown, [retrieved on 12-29-2010], Retrieved from the Internet: <url: http:="" specifications.html="" www.vita.com="">, 1 page.</url:>	
	CB051	CUBIX Customer Service Support System, "Click on the Front Panel That Matches Your System," © 2000, Cubix [online], [retrieved on June 22, 2004]. Retrieved from the Internet at <url: 64.173.211.7="" density="" density.htm="" http:="" support="" techinfo="">, 1 page.</url:>	
	CK001	International Search Report for International Patent Application No. PCT/US99/09369, report mailed November 16, 1999, 7 pages.	
	CK002	International Preliminary Examination Report for International Patent Application No. PCT/US99/09369, report completed July 5, 2000, 4 pages.	
	CK003	IBM Corporation, "Grounding Spring for Peripheral Device and Bezel Bracket," IBM Technical Disclosure Bulletin, November 1, 1993, Vol. 36, No. 11, 2 pages.	
	CL001	DIGITAL SEMICONDUCTOR Product Brief, "21152 PCI-to-PCI Bridge," February 1996, 6 pages.	
	CL002	INTEL CORPORATION Architectural Overview, "Intel 430TX PCISET: 82439TX System Controller (MTXC)," February 1997, 4 pages.	
	CL003	INTEL CORPORATION Architectural Overview, "Intel 82371AB PCI-to-ISA/IDE XCEL-ERATOR (PIIX4)," April 1997, 3 pages.	
	CL004	INTEL CORPORATION Advance Information, "Intel 440LX AGPSET: 82443LX PCI A.G.P. Controller (PAC)," August 1997, 4 pages.	
	CL005	NATIONAL SEMICONDUCTOR, "DS90CR215/DS90CR216 +3.3V Rising Edge Data Strobe LVDS 21-Bit Channel Link-66 MHz, July 1997, 2 pages.	

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Sheet 12

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Examiner Initials*	Cite No.1	item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.	T²
	CL006	NATIONAL SEMICONDUCTOR Product Folder, "DS90CR215 Plus-3.3V Rising Edge Data Strobe LVDS 21-Bit Channel and Link - 66 MHz," National Semiconductor Corporation [online], [retrieved on October 30, 1997]. Retrieved from the Internet at <url< td=""> http://www.national.com/search/search.cgi/design?keywords=DS90CR215>, 2 pages.</url<>	
	CL007	VIDEO ELECTRONICS Standards Association (VESA), Plug and Display (P&D) Standard, P&D and Digita Transition Minimized Differential Signaling (TMDS) Video Transmission Overview, 1997, Version 1, Revision 0, pp. 13 & 31-34.	
	CN001	LIQUORMAN, M., "Convergent Technologies Had This Idea," December 5, 1997, Jesse Berst's Anchor Desk [online], [retrieved on July 10, 1998]. Retrieved from the Internet at: <url: http://www.zdnet.com/anchordesk/talkback/talkback_56555.html>, 1 page.</url: 	
	CN002	BERST, J., "Hope For The Modular PCs We All Really Want," December 5, 1997, Jesse Berst's Anchor Desk [online], [retrieved on July 10, 1998]. Retrieved from the Internet at: <url: http://www.zdnet.com/anchordesk/story/story_1504.html>, 3 pages.</url: 	
	CN003	BOYD-MERRITT, R., "Upgradable-PC Effort Takes Divergent Paths," EE Times - Headline News [online], [retrieved on July 31, 1998]. Retrieved from the Internet at : <url: http://techweb.cmp.com/eet/news/97/949news/effort.html>, 3 pages.</url: 	
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	CN005	SPANG, K., "Component House: Design Technology for 'PCs in a Snap' - NeoSystems Offers Building Blocks," Computer Reseller News, April 21, 1997, Issue: 732, Section: Channel Assembly, TechWeb [online], [retrieved on July 31, 1998]. Retrieved from the Internet at: <url: http://www.techweb.com/se/directlink.cgi?CRN19970421S0054>, 2 pages.</url: 	
	CN006	"Think Modular," June 10, 1997, PC Magazine [online], [retrieved on July 31, 1998]. Retrieved from the Internet at: <url: 1611="" 60="" homezdnet.com="" http:="" issues="" pcmag="" pcmg0072.htm="" wysiwyg:="">, 1 page.</url:>	
	DA001	Office Action for U.S. Patent No. 6,718,415, mailed October 10, 2002, 7 pages.	
	DA002	Response for U.S. Patent No. 6,718,415, filed November 7, 2002, 9 pages.	
	DA003	Office Action for U.S. Patent No. 6,718,415, mailed January 29, 2003, 7 pages.	
	DA004	Response for U.S. Patent No. 6,718,415, filed March 6, 2003, 8 pages.	
	DA005	Office Action for U.S. Patent No. 6,718,415, mailed June 4, 2003, 8 pages.	
	DA006	Response for U.S. Patent No. 6,718,415, filed September 4, 2003, 10 pages.	L
	DB001	Amendment Submitted With RCE for U.S. Patent No. 7,099,981, filed March 1, 2006, 23 pages.	

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Substitute for form 1449A/PTO			Complete if Known		
			Application Number	12/561,138	
			Filing Date	September 16, 2009	
INFORMATION DISCLOSURE STATEMENT BY APPLICANT (Use as many sheets as necessary)			First Named Inventor	William W.Y. Chu	
			Art Unit	2435	
			Examiner Name	Song, Hosuk	
Sheet	13	of 23	Attorney Docket Number	ACQI-006/03US 310578-2053	

		NON PATENT LITERATURE DOCUMENTS	
		Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.	T ²
	DC001	Office Action for U.S. Patent No. 7,363,415, mailed on April 12, 2007, 23 pages.	
	DC002	Response for U.S. Patent No. 7,363,415, filed on April 24, 2007, 25 pages.	
· .	DD001	Office Action for U.S. Patent No. 7,328,297, mailed February 8, 2007, 5 pages.	
	DD002	Response for U.S. Patent No. 7,328,297, filed April 19, 2007, 32 pages.	
	DD003	Office Action for U.S. Patent No. 7,328,297, mailed July 12, 2007, 13 pages.	
	DD004	Response for U.S. Patent No. 7,328,297, filed July 23, 2007, 20 pages.	
	DF001	Office Action for U.S. Patent No. 7,363,416, mailed April 12, 2007, 23 pages.	
	DF002	Response for U.S. Patent No. 7,363,416, filed April 24, 2007, 23 pages.	
	DG001	Office Action for U.S. Patent No. 7,376,779, mailed September 28, 2007, 24 pages.	
	DG002	Response for U.S. Patent No. 7,376,779, filed October 16, 2007, 23 pages.	
	DH001	Office Action for U.S. Patent No. 7,676,624, mailed December 1, 2008, 8 pages.	
DH002 Response for U.S. Patent No. 7,676,624, filed January 13, 2009, 14 pages.		Response for U.S. Patent No. 7,676,624, filed January 13, 2009, 14 pages.	
	DH003	Supplemental Response for U.S. Patent No. 7,676,624, filed on February 6, 2009, 13 pages.	
	DI001	Office Action for U.S. Patent No. 7,818,487, mailed September 29, 2009, 10 pages.	
	D1002	Response for U.S. Patent No. 7,818,487, filed November 6, 2009, 3 pages.	
	D1003	Amendment for U.S. Patent No. 7,818,487, filed May 11, 2010, 15 pages.	
	D1004	Amendment Submitted After Notice of Allowance for U.S. Patent No. 7,818,487, filed August 17, 2010, 14 pages.	
	DJ001	Office Action for U.S. Publication No. 2010/0174844, mailed October 28, 2010, 11 pages.	
	DK001	Office Action for U.S. Patent No. 6,216,185, mailed April 12, 2000, 9 pages.	
	DK002	Response for U.S. Patent No. 6,216,185, filed August 3, 2000, 15 pages.	
	DK003	Office Action for U.S. Patent No. 6,216,185, mailed August 25, 2000, 9 pages.	
	DK004	Response for U.S. Patent No. 6,216,185, filed October 24, 2000, 10 pages.	
	DL001	Office Action for U.S. Patent No. 6,345,330, mailed June 15, 2000, 7 pages.	
	DL002	Amendment for U.S. Patent No. 6,345,330, filed September 12, 2000, 5 pages.	
	DL003	Restriction Requirement for U.S. Patent No. 6,345,330, mailed December 19, 2000, 5 pages.	
	DL004	Amendment filed with Continued Prosecution Application for U.S. Patent No. 6,345,330, filed January 17, 2001, 5	
	D1 005	pages.	
	DL005	Office Action for U.S. Patent No. 6,345,330, mailed March 23, 2001, 6 pages.	
	DL006	Response to Office Action for U.S. Patent No. 6,345,330, filed July 19, 2001, 5 pages.	
	DM001	Office Action for U.S. Patent Application No. 09/642,628, mailed April 5, 2001, 9 pages.	
	DO001	Office Action for U.S. Application No. 10/963,825, mailed October 27, 2005, 25 pages.	L

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Sheet

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Co	mplete if Known
Application Number	12/561,138
Filing Date	September 16, 2009
First Named Inventor	William W.Y. Chu
Art Unit	2435
Examiner Name	Song, Hosuk
Attorney Docket Number	ACQI-006/03US 310578-2053

23

Examiner Initials*	Cite No. ¹	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.	T
	DO002	Response for U.S. Application No. 10/963,825, filed January 9, 2006, 22 pages.	
_	DO003	Office Action for U.S. Application No. 10/963,825, mailed May 31, 2006, 29 pages.	
	DO004	Amendment Submitted with RCE for U.S. Application No. 10/963,825, filed July 27, 2006, 29 pages.	
	DO005	Office Action for U.S. Application No. 10/963,825, mailed October 20, 2006, 28 pages.	
	DO006	Appellants' Brief for U.S. Application No. 10/963,825, filed January 8, 2007, 31 pages.	
	DO007	Revised Appellants' Brief for U.S. Application No. 10/963,825, filed April 20, 2007, 34 pages.	
	DO008	Examiner's Answer for U.S. Application No. 10/963,825, mailed August 8, 2007, 30 pages.	
	DO009	Reply Brief for U.S. Application No. 10/963,825, filed September 4, 2007, 4 pages.	
	DO010	Decision on Appeal for U.S. Application No. 10/963,825, mailed February 4, 2009, 13 pages.	
	D0011	Amendment Submitted with RCE for U.S. Application No. 10/963,825, filed February 20, 2009, 24 pages.	
	DO012	Office Action for U.S. Application No. 10/963,825, mailed May 14, 2009, 5 pages.	
	DO013	Response for U.S. Application No. 10/963,825, filed May 22, 2009, 2 pages.	
	DO014	Office Action for U.S. Application No. 10/963,825, mailed September 15, 2009, 14 pages.	
	DO015	Response for U.S. Application No. 10/963,825, filed October 1, 2009, 7 pages.	
	DP001	Office Action for RE 41,294, mailed November 16, 2007, 10 pages.	
	DP002	Response for RE 41,294, filed December 20, 2007, 21 pages.	
	DP003	Office Action for RE 41,294, mailed April 15, 2008, 10 pages.	
	DP004	Amendment Submitted with RCE for RE 41,294, filed May 27, 2008, 14 pages.	
	DP005	Supplemental Amendment Submitted with RCE for RE 41,294, filed July 8, 2008, 12 pages.	
	DP006	Office Action for RE 41,294, mailed September 16, 2008, 11 pages.	
	DP007	Response for RE 41,294, filed October 30, 2008, 14 pages.	
_	DP008	Supplemental Response for RE 41,294, filed February 20, 2009, 13 pages.	
	DP009	Supplemental Response for RE 41,294, filed August 17, 2009, 3 pages.	
	DP010	Examiner Interview Summary Record, mailed January 15, 2009, 1 page.	
	DQ001	Office Action for RE 41,076, mailed July 13, 2007, 38 pages.	
	DQ002	Response for RE 41,076, filed September 26, 2007, 18 pages.	
	DQ003	Office Action for RE 41,076, mailed October 17, 2007, 55 pages.	
	DQ004	Amendment Submitted with RCE for RE 41,076, filed November 5, 2007, 19 pages.	
	DQ005	Office Action for RE 41,076, mailed February 11, 2008, 62 pages.	
	DQ006	Response for RE 41,076, filed April 7, 2008, 18 pages.	
	DQ007	Office Action for RE 41,076, mailed June 9, 2008, 25 pages.	Τ

Examiner Signature	/Hosuk Song/	Date Considered	03/08/2011

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INFORMATION DISCLOSURE STATEMENT BY APPLICANT

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	Application Number	12/561,138
	Filing Date	September 16, 2009
	First Named Inventor	William W.Y. Chu
	Art Unit	2435
	Examiner Name	Song, Hosuk
_	Attorney Docket Number	ACQI-006/03US 310578-2053

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Sheet 15

		NON PATENT LITERATURE DOCUMENTS	
Examiner Initials*	Cite No. ¹	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.	T
	DQ008	Amendment Submitted with RCE for RE 41,076, filed December 8, 2008, 44 pages.	Γ
	DQ009	Office Action for RE 41,076, mailed December 30, 2008, 8 pages.	
	DQ010	Response for RE 41,076, filed January 16, 2009, 14 pages.	Γ
•	DQ011	Amendment Submitted with RCE for RE 41,076, filed August 4, 2009, 2 pages.	Γ
	DQ012	Examiner Interview Summary Record, mailed February 24, 2009, 4 pages.	Γ
	DQ013	Applicant Summary of Interview, filed March 24, 2009, 1 page.	Г
	DQ014	Examiner Interview Summary Record, mailed September 22, 2009, 5 pages.	Γ
	DR001	Office Action for U.S. Application No. 12/322,858, mailed March 4, 2010, 24 pages.	
	DR002	Response for U.S. Application No. 12/322,858, filed June 4, 2010, 15 pages.	1
	DR003	Office Action for U.S. Application No. 12/322,858, mailed June 25, 2010, 22 pages.	ſ
	DR004	Response for U.S. Application No. 12/322,858, filed October 25, 2010, 12 pages.	Γ
	DS001	Office Action for U.S. Application No. 12/577,074, mailed April 13, 2010, 7 pages.	Γ
	DS002	Response for U.S. Application No. 12/577,074, filed July 13, 2010, 3 pages.	Γ
	DS003 ·	Office Action for U.S. Application No. 12/577,074, mailed November 10, 2010, 6 pages.	
	DT001	Office Action for U.S. Application No. 09/312,199, mailed March 26, 2003, 5 pages.	Γ
	DT002	Response for U.S. Application No. 09/312,199, filed June 11, 2003, 5 pages.	
	DU001	Office Action for RE 41,092, mailed September 17, 2008, 8 pages.	
	DU002	Response for RE 41,092, filed October 27, 2008, 27 pages.	
	DU003	Examiner's Amendment for RE 41,092, mailed November 4, 2009, 4 pages.	
	DV001	Office Action for U.S. Application No. 11/545,056, mailed March 12, 2010, 26 pages.	
	DV002	Response for U.S. Application No. 11/545,056, filed June 14, 2010, 18 pages.	
	DW001	Office Action for U.S. Application No. 12/561,138, mailed September 29, 2010, 4 pages.	
	EA001	Request for Ex Parte Reexamination of US Patent No. 6,216,185, Control No. 90/010,816, filed January 8, 2010 39 pages.	
	EA002	Request for Ex Parte Reexamination of US Patent No. 6,216,185, Control No. 90/010,816, filed January 8, 2010 Exhibit AA to Request Claim Charts with respect to the Hitachi '953 for Anticipation and Obviousness, 136 pages	
	EA003	Request for Ex Parte Reexamination of US Patent No. 6,216,185, Control No. 90/010,816, filed January 8, 2010, Exhibit BB Claim Charts with respect to Kobayashi for Anticipation and Obviousness, 128 pages	,
	EA004	Request for Ex Parte Reexamination of US Patent No. 6,216,185, Control No. 90/010,816, filed January 8, 2010 Exhibit CC Claim Charts with respect to Byte for Anticipation and Obviousness, 122 pages	1

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	First Named Inventor	William W.Y. Chu
	Art Unit	2435
	Examiner Name	Song, Hosuk
	Attorney Docket Number	ACQI-006/03US 310578-2053

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Sheet 16

		NON PATENT LITERATURE DOCUMENTS	
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	EA005	Request for Ex Parte Reexamination of US Patent No. 6,216,185, Control No. 90/010,816, filed January 8, 2010, Exhibit DD Claim Charts with respect to the Hitachi '675 for Anticipation and Obviousness, 119 pages	
	EA006	Office Action in Ex Parte Reexamination of US Patent No. 6,216,185, Control No. 90/010,816, mailed July 27, 2010, 103 pages	
	EA007	Patent Owner's Response to Office Action in Ex Parte Reexamination of US Patent No. 6,216,185, Control No. 90/010,816, filed September 27, 2010, 55 pages	
	EB001	Request for Inter Partes Reexamination of US Patent No. 6,718,415, Control No. 95/001,276, filed December 2, 2009, 44 pages.	
	EB002	Request for Inter Partes Reexamination of US Patent No. 6,718,415, Control No. 95/001,276, filed December 2, 2009, Exhibit O, Declaration Under 37 CFR 1.132 of Vincent P. Conroy, 11-24-2009, 3 pages.	
-	EB003	Request for Inter Partes Reexamination of US Patent No. 6,718,415, Control No. 95/001,276, Replacement Exhibit AA, Claim Charts with respect to QuantumNet for Anticipation and Obviousness, filed January 5, 2010, 109 pages.	
	EB004	Request for Inter Partes Reexamination of US Patent No. 6,718,415, Control No. 95/001,276, Replacement Exhibit BB, Claim Charts with respect to Chatcom for Anticipation and Obviousness, filed January 5, 2010, 91 pages.	
	EB005	Request for Inter Partes Reexamination of US Patent No. 6,718,415, Control No. 95/001,276, Replacement Exhibit CC, Claim Charts with respect to QuantumNet for Anticipation and Obviousness, filed January 5, 2010, 85 pages.	
	EB006	Request for Inter Partes Reexamination of US Patent No. 6,718,415, Control No. 95/001,276, Replacement Exhibit DD, Claim Charts with respect to the Origin2000 Manual for Obviousness, filed January 5, 2010, 72 pages.	
	EB007	Request for Inter Partes Reexamination of US Patent No. 6,718,415, Control No. 95/001,276, Replacement Exhibit EE, Claim Charts with respect to Gallagher for Anticipation and Obviousness, filed January 5, 2010, 107 pages.	
	EB008	Office Action in Inter Partes Reexamination of US Patent No. 6,718,415, Control No. 95/001,276, mailed May 26, 2010, 39 pages.	
	EB009	Patent Owner's Response to Office Action in Inter Partes Reexamination of US Patent No. 6,718,415, Control No. 95/001,276, filed July 27, 2010, 41 pages.	
	EB010	Patent Owner's Response to Office Action in Inter Partes Reexamination of US Patent No. 6,718,415, Control No. 95/001,276, Exhibit A, Declaration of William Henry Mangione-Smith under 37 C.F.R. 1.132, filed July 27, 2010, 29 pages.	

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Sheet 17

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	EC001	Request for Inter Partes Reexamination of US Patent No. 7,099,981, Control No. 95/001,310, filed February 9, 2010, 33 pages	
	EC002	Request for Inter Partes Reexamination of US Patent No. 7,099,981, Control No. 95/001,310, filed December 2, 2009, Exhibit O, Declaration Under 37 CFR 1.132 of Vincent P. Conroy, 11-24-2009, 3 pages.	
	EC003	Request for Inter Partes Reexamination of US Patent No. 7,099,981, Control No. 95/001,310, Exhibit AA, Claim Charts with respect to Gallagher for Anticipation and Obviousness, filed February 9, 2010, 164 pages	
	EC004	Request for Inter Partes Reexamination of US Patent No. 7,099,981, Control No. 95/001,310, Exhibit BB, Claim Charts with respect to QuantumNet for Anticipation and Obviousness, filed February 9, 2010, 158 pages	
	EC005	Request for Inter Partes Reexamination of US Patent No. 7,099,981, Control No. 95/001,310, Exhibit CC, Claim Charts with respect to Chatcom for Anticipation and Obviousness, filed February 9, 2010, 167 pages	
	EC006	Request for Inter Partes Reexamination of US Patent No. 7,099,981, Control No. 95/001,310, Exhibit DD, Claim Charts with respect to the Eversys for Obviousness, filed February 9, 2010, 111 pages	
	EC007	Office Action in Inter Partes Reexamination of US Patent No. 7,099,981, Control No. 95/001,310, mailed July 6, 2010, 83 pages	
	EC008	Patent Owner's Response to Office Action in Inter Partes Reexamination of US Patent No. 7,099,981, Control No. 95/001,310, filed September 3, 2010, 52 pages	
	EC009	Patent Owner's Response to Office Action in Inter Partes Reexamination of US Patent No. 7,099,981, Control No. 95/001,310, Exhibit A, Declaration of William Henry Mangione-Smith under 37 C.F.R. 1.132, filed September 3, 2010, 63 pages	
	ED001	Request for Inter Partes Reexamination of US Patent No. 7,146,446, Control No. 95/001,328, filed March 19, 2010, 35 pages.	
•	ED002	Request for Inter Partes Reexamination of US Patent No. 7,146,446, Control No. 95/001,328, Exhibit AA (Part 1), Claim Charts with respect to Gallagher for Anticipation and Obviousness, filed March 19, 2010, 186 pages.	
	ED003	Request for Inter Partes Reexamination of US Patent No. 7,146,446, Control No. 95/001,328, Exhibit AA (Part 2), Claim Charts with respect to Gallagher for Anticipation and Obviousness, filed March 19, 2010, 161 pages.	
· · ·	ED004	Request for Inter Partes Reexamination of US Patent No. 7,146,446, Control No. 95/001,328, Exhibit BB (Part 1), Claim Charts with respect to QuantumNet for Anticipation and Obviousness, filed March 19, 2010, 139 pages.	
`	ED005	Request for Inter Partes Reexamination of US Patent No. 7,146,446, Control No. 95/001,328, Exhibit BB (Part 2), Claim Charts with respect to QuantumNet for Anticipation and Obviousness, filed March 19, 2010, 128 pages.	
	ED006	Request for Inter Partes Reexamination of US Patent No. 7,146,446, Control No. 95/001,328, Exhibit CC, Claim Charts with respect to Chatcom for Anticipation and Obviousness, filed March 19, 2010, 68 pages.	

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INFORMATION DISCLOSURE STATEMENT BY APPLICANT

Co	mplete if Known
Application Number	12/561,138
Filing Date	September 16, 2009
First Named Inventor	William W.Y. Chu
Art Unit	2435
Examiner Name	Song, Hosuk
Attorney Docket Number	ACQI-006/03US 310578-2053

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Sheet 18

	NON PATENT LITERATURE DOCUMENTS			
Examiner Initials*	Cite No. ¹	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.	T ²	
	ED007	Office Action in Inter Partes Reexamination of US Patent No. 7,146,446, Control No. 95/001,328, mailed June 24, 2010, 86 pages.		
	ED008	Patent Owner's Response to Office Action in Inter Partes Reexamination of US Patent No. 7,146,446, Control No. 95/001,328, filed August 24, 2010, 45 pages.		
	ED009	Patent Owner's Response to Office Action in Inter Partes Reexamination of US Patent No. 7,146,446, Control No. 95/001,328, Exhibit A, Declaration of William Henry Mangione-Smith under 37 C.F.R. 1.132, filed September 3, 2010, 61 pages.		
	EE001	Request for Inter Partes Reexamination of US Patent No. 7,328,297, Control No. 95/001,336, filed April 19, 2010, 33 pages.		
	EE002	Request for Inter Partes Reexamination of US Patent No. 7,328,297, Control No. 95/001,336, Exhibit AA, Claim Charts with respect to Gallagher for Obviousness, filed April 19, 2010, 131 pages.		
	EE003	Request for Inter Partes Reexamination of US Patent No. 7,328,297, Control No. 95/001,336, Exhibit BB, Claim Charts with respect to QuantumNet for Obviousness, filed April 19, 2010, 139 pages.		
	EE004	Request for Inter Partes Reexamination of US Patent No. 7,328,297, Control No. 95/001,336, Exhibit CC, Claim Charts with respect to Chatcom for Obviousness, filed April 19, 2010, 114 pages.		
	EE005	Office Action in Inter Partes Reexamination of US Patent No. 7,328,297, Control No. 95/001,336, mailed August 4, 2010, 95 pages.		
	EE006	Patent Owner's Response to Office Action in Inter Partes Reexamination of US Patent No. 7,328,297, Control No. 95/001,336, filed October 4, 2010, 49 pages.		
· · · ·	EE007	Patent Owner's Response to Office Action in Inter Partes Reexamination of US Patent No. 7,328,297, Control No. 95/001,336, Exhibit A, Declaration of William Henry Mangione-Smith under 37 C.F.R. 1.132, filed October 4, 2010, 61 pages.		
	EF001	Request for Inter Partes Reexamination of US Patent No. 7,363,415, Control No. 95/001,424, filed August 25, 2010, 34 pages.		
	EF002	Request for Inter Partes Reexamination of US Patent No. 7,363,415, Control No. 95/001,424, Exhibit AA, Claim Charts with respect to Gallagher and Other References for Obviousness, filed August 25, 2010, 114 pages.		
	EF003	Request for Inter Partes Reexamination of US Patent No. 7,363,415, Control No. 95/001,424, Exhibit AB, Claim Charts with respect to Gallagher and Other References for Obviousness, filed August 25, 2010, 92 pages.		
	EF004	Request for Inter Partes Reexamination of US Patent No. 7,363,415, Control No. 95/001,424, Exhibit BA, Claim Charts with respect to QuantumNet and Other References for Obviousness, filed August 25, 2010, 121 pages.		
	EF005	Request for Inter Partes Reexamination of US Patent No. 7,363,415, Control No. 95/001,424, Exhibit BB, Claim Charts with respect to QuantumNet and Other References for Obviousness, filed August 25, 2010, 99 pages.		

Examiner Signature	/Hosuk Song/	Date Considered	03/08/2011
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	EF006	Request for Inter Partes Reexamination of US Patent No. 7,363,415, Control No. 95/001,424, Exhibit CA, Claim Charts with respect to Chatcom and Other References for Obviousness, filed August 25, 2010, 91 pages.	
	EF007	Request for Inter Partes Reexamination of US Patent No. 7,363,415, Control No. 95/001,424, Exhibit CB, Claim Charts with respect to Chatcom and Other References for Obviousness, filed August 25, 2010, 94 pages.	
	EF008 ·	Office Action in Inter Partes Reexamination of US Patent No. 7,363,415, Control No. 95/001,424, mailed November 1, 2010, 75 pages.	
	EG001	Request for Inter Partes Reexamination of US Patent No. 7,376,779, Control No. 95/001,475, filed October 27, 2010, 35 pages.	
	EG002	Request for Inter Partes Reexamination of US Patent No. 7,376,779, Control No. 95/001,475, Exhibit AA, Claim Charts with respect to Gallagher and Other References for Obviousness, filed October 27, 2010, 128 pages.	
	EG003	Request for Inter Partes Reexamination of US Patent No. 7,376,779, Control No. 95/001,475, Exhibit AB, Claim Charts with respect to Gallagher and Other References for Obviousness, filed October 27, 2010, 153 pages.	
	EG004	Request for Inter Partes Reexamination of US Patent No. 7,376,779, Control No. 95/001,475, Exhibit BA, Claim Charts with respect to QuantumNet and Other References for Obviousness, filed October 27, 2010, 108 pages.	
	EG005	Request for Inter Partes Reexamination of US Patent No. 7,376,779, Control No. 95/001,475, Exhibit BB, Claim Charts with respect to QuantumNet and Other References for Obviousness, filed October 27, 2010, 112 pages.	
	EG006	Request for Inter Partes Reexamination of US Patent No. 7,376,779, Control No. 95/001,475, Exhibit CA, Claim Charts with respect to Chatcom and Other References for Obviousness, filed October 27, 2010, 112 pages.	·
	EG007	Request for Inter Partes Reexamination of US Patent No. 7,376,779, Control No. 95/001,475, Exhibit CB, Claim Charts with respect to Chatcom and Other References for Obviousness, filed October 27, 2010, 118 pages.	
	EG008	Office Action in Inter Partes Reexamination of US Patent No. 7,376,779, Control No. 95/001,475, mailed December 20, 2010, 105 pages.	
	EH001	Request for Inter Partes Reexamination of US Patent No. 7,363,416, Control No. 95/001,476, filed October 27, 2010, 37 pages.	
	EH002	Request for Inter Partes Reexamination of US Patent No. 7,363,416, Control No. 95/001,476, Exhibit AA, Claim Charts with respect to Gallagher and Other References for Obviousness, filed October 27, 2010, 70 pages.	
	EH003	Request for Inter Partes Reexamination of US Patent No. 7,363,416, Control No. 95/001,476, Exhibit AB, Claim Charts with respect to Gallagher and Other References for Obviousness, filed October 27, 2010, 64 pages.	
	EH004	Request for Inter Partes Reexamination of US Patent No. 7,363,416, Control No. 95/001,476, Exhibit BA, Claim Charts with respect to QuantumNet and Other References for Obviousness, filed October 27, 2010, 64 pages.	
	EH005	Request for Inter Partes Reexamination of US Patent No. 7,363,416, Control No. 95/001,476, Exhibit BB, Claim Charts with respect to QuantumNet and Other References for Obviousness, filed October 27, 2010, 71 pages.	

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	Application Number	12/561,138
	Filing Date	September 16, 2009
	First Named Inventor	William W.Y. Chu
	Art Unit	2435
	Examiner Name	Song, Hosuk
	Attorney Docket Number	ACQI-006/03US 310578-2053

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Sheet 20

		NON PATENT LITERATURE DOCUMENTS	
Examiner Initials*	Cite No. ¹	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.	T
_	EH006	Request for Inter Partes Reexamination of US Patent No. 7,363,416, Control No. 95/001,476, Exhibit CA, Claim Charts with respect to Chatcom and Other References for Obviousness, filed October 27, 2010, 64 pages.	
	EH007	Request for Inter Partes Reexamination of US Patent No. 7,363,416, Control No. 95/001,476, Exhibit CB, Claim Charts with respect to Chatcom and Other References for Obviousness, filed October 27, 2010, 67 pages.	
	EH008	Office Action in Inter Partes Reexamination of US Patent No. 7,363,416, Control No. 95/001,476, mailed December 6, 2010, 63 pages.	
	IC01	"Defendants' Amended Invalidity Contentions," submitted by the Defendants in the U.S. District Court for the Eastern District of Texas, Case No. 6:09-cv-148-LED on March 1, 2010, 18 pages.	
	IC02	"Exhibit A (Asserted Claims)," submitted by the Defendants in the U.S. District Court for the Eastern District of Texas, Case No. 6:09-cv-148-LED on March 1, 2010, 2 pages.	
	IC03	"Exhibit B - Table 1," submitted by the Defendants in the U.S. District Court for the Eastern District of Texas, Case No. 6:09-cv-148-LED on March 1, 2010, 75 pages.	
	IC04	"Exhibit C," submitted by the Defendants in the U.S. District Court for the Eastern District of Texas, Case No. 6:09-cv-148-LED on March 1, 2010, 2 pages.	
	IC05	"Exhibit D," submitted by the Defendants in the U.S. District Court for the Eastern District of Texas, Case No. 6:09-cv-148-LED on March 1, 2010, 106 pages.	
	IC06	"Exhibit E," submitted by the Defendants in the U.S. District Court for the Eastern District of Texas, Case No. 6:09-cv-148-LED on March 1, 2010, 2 pages.	
	IC07	"Invalidity Chart for Base Reference IBM 8260," submitted by the Defendants in the U.S. District Court for the Eastern District of Texas, Case No. 6:09-cv-148-LED on March 1, 2010, 53 pages.	
	IC08	"Invalidity Chart for Base Reference IBM 8265," submitted by the Defendants in the U.S. District Court for the Eastern District of Texas, Case No. 6:09-cv-148-LED on March 1, 2010, 56 pages.	
•	1C09	"Invalidity Chart for Base Reference U.S. Patent No. 4,453,215 (Reid)," submitted by the Defendants in the U.S. District Court for the Eastern District of Texas, Case No. 6:09-cv-148-LED on March 1, 2010, 56 pages.	
	IC10	"Invalidity Chart for Base Reference Origin2000," submitted by the Defendants in the U.S. District Court for the Eastern District of Texas, Case No. 6:09-cv-148-LED on March 1, 2010, 56 pages.	
	IC11	"Invalidity Chart for Base Reference QuantumNet," submitted by the Defendants in the U.S. District Court for the Eastern District of Texas, Case No. 6:09-cv-148-LED on March 1, 2010, 49 pages.	
	IC12	"Invalidity Chart for Base Reference U.S. Patent No. 6,564,274 (Heath)," submitted by the Defendants in the U.S. District Court for the Eastern District of Texas, Case No. 6:09-cv-148-LED on March 1, 2010, 57 pages.	
	IC13	"Invalidity Chart for Base Reference U.S. Patent No. 5,577,205," submitted by the Defendants in the U.S. District Court for the Eastern District of Texas, Case No. 6:09-cv-148-LED on March 1, 2010, 60 pages.	

Examiner Signature	/Hosuk Song/	Date Considered	03/08/2011	
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	IC14	"Invalidity Chart for Base Reference U.S. Patent No. 5,802,391," submitted by the Defendants in the U.S. District Court for the Eastern District of Texas, Case No. 6:09-cv-148-LED on March 1, 2010, 61 pages.	
	IC15	"Invalidity Chart for Base Reference U.S. Patent No. 6,715,100," submitted by the Defendants in the U.S. District Court for the Eastern District of Texas, Case No. 6:09-cv-148-LED on March 1, 2010, 64 pages.	
	IC16	"Invalidity Chart for Base Reference Cubix BC/Density," submitted by the Defendants in the U.S. District Court for the Eastern District of Texas, Case No. 6:09-cv-148-LED on March 1, 2010, 64 pages.	
	IC17	"Invalidity Chart for Base Reference JP6-289956," submitted by the Defendants in the U.S. District Court for the Eastern District of Texas, Case No. 6:09-cv-148-LED on March 1, 2010, 62 pages.	
	IC18	"Invalidity Chart for Base Reference Gallagher 068 and Gallagher 503," submitted by the Defendants in the U.S. District Court for the Eastern District of Texas, Case No. 6:09-cv-148-LED on March 1, 2010, 108 pages.	
	IC19	"Invalidity Chart for Base Reference Compaq ProLiant Cluster," submitted by the Defendants in the U.S. District Court for the Eastern District of Texas, Case No. 6:09-cv-148-LED on March 1, 2010, 81 pages.	
	IC20	"Invalidity Chart for Base Reference U.S. Patent No. 5,325,517 to Baker et al. (Appendix 1, Exhibit 15)," submitted by the Defendants in the U.S. District Court for the Eastern District of Texas, Case No. 6:09-cv-148- LED on March 1, 2010, 59 pages.	
	IC21	"Invalidity Chart for Japanese Patent Application H7-64672 (Toshiba '672)," submitted by the Defendants in the U.S. District Court for the Eastern District of Texas, Case No. 6:09-cv-148-LED on March 1, 2010, 55 pages.	
	IC22	"Invalidity Chart for Base Reference ChatCom," submitted by the Defendants in the U.S. District Court for the Eastern District of Texas, Case No. 6:09-cv-148-LED on March 1, 2010, 52 pages.	
	IC23	"Invalidity Chart for Base Reference Ziatech Corp. Ketris 9000 System," submitted by the Defendants in the U.S. District Court for the Eastern District of Texas, Case No. 6:09-cv-148-LED on March 1, 2010, 68 pages.	
	IC24	"Invalidity Chart for Base Reference Ziatech STD 32 Star System," submitted by the Defendants in the U.S. District Court for the Eastern District of Texas, Case No. 6:09-cv-148-LED on March 1, 2010, 62 pages.	
	IC25	"Invalidity Chart for Base Reference U.S. Patent No. 7,339,786 (Bottom et al.)," submitted by the Defendants in the U.S. District Court for the Eastern District of Texas, Case No. 6:09-cv-148-LED on March 1, 2010, 57 pages.	
	IC26	"Invalidity Chart for Base References RLX Patents, U.S. Patent Nos. 6,747,878, 6,411,506, 6,325,636, 6,757,748, and 6,985,967 (Hipp et al.)," submitted by the Defendants in the U.S. District Court for the Eastern District of Texas, Case No. 6:09-cv-148-LED on March 1, 2010, 58 pages.	
	IC27	"Invalidity Chart for Base Reference Network Engines P6000 Server," submitted by the Defendants in the U.S. District Court for the Eastern District of Texas, Case No. 6:09-cv-148-LED on March 1, 2010, 59 pages.	
	IC28	"Invalidity Chart for Base Reference Eversys 8000 System," submitted by the Defendants in the U.S. District Court for the Eastern District of Texas, Case No. 6:09-cv-148-LED on March 1, 2010, 60 pages.	

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	IC29	"Invalidity Chart for Base Reference Eversys CAPserver," submitted by the Defendants in the U.S. District Court	
		for the Eastern District of Texas, Case No. 6:09-cv-148-LED on March 1, 2010, 59 pages.	
	IC30	"Invalidity Chart for Base Reference U.S. 5,809,262," submitted by the Defendants in the U.S. District Court for	
		the Eastern District of Texas, Case No. 6:09-cv-148-LED on March 1, 2010, 62 pages.	<u> </u>
	IC31	"Invalidity Chart for Base Reference WhiteCross 9800 System," submitted by the Defendants in the U.S. District	
		Court for the Eastern District of Texas, Case No. 6:09-cv-148-LED on March 1, 2010, 62 pages.	L
	IC32	"Invalidity Chart for Base Reference U.S. 5,339,408," submitted by the Defendants in the U.S. District Court for	
		the Eastern District of Texas, Case No. 6:09-cv-148-LED on March 1, 2010, 61 pages.	
	IC33	"Invalidity Chart for Base Reference Tyuluman 536," submitted by the Defendants in the U.S. District Court for	
		the Eastern District of Texas, Case No. 6:09-cv-148-LED on March 1, 2010, 76 pages.	_
	IC34	"Invalidity Chart for Base Reference Hong 737," submitted by the Defendants in the U.S. District Court for the	
		Eastern District of Texas, Case No. 6:09-cv-148-LED on March 1, 2010, 77 pages.	ļ
	IC35	"Invalidity Chart for Base Reference U.S. 5,436,857 (Nelson)," submitted by the Defendants in the U.S. District	
		Court for the Eastern District of Texas, Case No. 6:09-cv-148-LED on March 1, 2010, 6 pages.	
	IC36	"Invalidity Chart for Base Reference U.S. 5,999,952 (Jenkins)", submitted by the Defendants in the U.S. District	
Court for the Eastern District of Texas, Case No. 6:09-cv-148-LED on March 1, 2010, 6 pages.			
	IC37	"Invalidity Chart for Base Reference U.S. 5,608,608 (Flint)", submitted by the Defendants in the U.S. District	
		Court for the Eastern District of Texas, Case No. 6:09-cv-148-LED on March 1, 2010, 6 pages.	
	IC38	"Invalidity Chart for Base Reference U.S. 5,978,821 (Freeny)", submitted by the Defendants in the U.S. District	1
		Court for the Eastern District of Texas, Case No. 6:09-cv-148-LED on March 1, 2010, 6 pages.	1
	IC39	"Invalidity Chart for Base Reference WO 92/18924 (Wallsten)", submitted by the Defendants in the U.S. District	
		Court for the Eastern District of Texas, Case No. 6:09-cv-148-LED on March 1, 2010, 6 pages.	
	IC40	"Invalidity Chart for Base Reference Ergo Moby Brick", submitted by the Defendants in the U.S. District Court for	
		the Eastern District of Texas, Case No. 6:09-cv-148-LED on March 1, 2010, 5 pages.	
	IC41	"Invalidity Chart for Base Reference U.S. Patent No. 5,463,742 (Kobayashi)", submitted by the Defendants in the	
		U.S. District Court for the Eastern District of Texas, Case No. 6:09-cv-148-LED on March 1, 2010, 5 pages.	
	IC42	"Invalidity Chart for Base Reference Japanese Patent Application Publication H6-289953 (Hitachi)", submitted by	
		the Defendants in the U.S. District Court for the Eastern District of Texas, Case No. 6:09-cv-148-LED on March 1	,
		2010, 5 pages.	
	IC43	"Invalidity Chart for Base Reference Japanese Patent Application Publication H7-84675 (Hitachi)", submitted by	
		the Defendants in the U.S. District Court for the Eastern District of Texas, Case No. 6:09-cv-148-LED on March 1	,
		2010, 5 pages.	

Examiner Signature	/Hosuk Song/	Date Considered	03/08/2011
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INFORMATION DISCLOSURE STATEMENT BY APPLICANT

Complete if Known					
Application Number	12/561,138				
Filing Date	September 16, 2009				
First Named Inventor	William W.Y. Chu				
Art Unit	2435				
Examiner Name	Song, Hosuk				
Attorney Docket Number	ACQI-006/03US 310578-2053				

(Use as many sheets as necessary)

23

Sheet 23

	NON PATENT LITERATURE DOCUMENTS						
Examiner Initials*	Cite No. ¹	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.	T ²				
	IC44	"Invalidity Chart for Base Reference U.S. Patent No. 5,187,645 (Spalding)", submitted by the Defendants in the U.S. District Court for the Eastern District of Texas, Case No. 6:09-cv-148-LED on March 1, 2010, 6 pages.					
	IC45	"Defendants' Notice of Errata Relating to Defendants' P.R. 3-3 Invalidity Contentions," submitted by the Defendants in the U.S. District Court for the Eastern District of Texas, Case No. 6:09-cv-148-LED on March 1, 2010, 14 pages.					
	IF01	"Exhibit 5 Disclosure of Accorted Claims and Infringement Contentions", cubmitted by the Plaintiff in the U.S. District Court for the Eastern District of Texas, Case No. 6:00 ov 148 LED, 14 pages.					
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Examiner Signature	Date Considered	03/08/2011

*EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant. ¹Applicant's unique citation designation number (optional). ²See Kinds Codes of USPTO Patent Documents at <u>www.uspto.gov</u> or MPEP 901.04. ³Enter Office that issued the document, by the two-letter code (WIPO Standard ST.3). ⁴For Japanese patent documents, the indication of the year of the reign of the Emperor must precede the serial number of the patent document. ⁵Kind of document by the appropriate symbols as indicated on the document under WIPO Standard ST. 16 if possible. ⁶Applicant is to place a check mark here if English language Translation is attached.

This collection of information is required by 37 CFR 1.97 and 1.98. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 2 hours to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.

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 PTO/SB/30EFS (07-09)

 Request for Continued Examination (RCE)
 Approved for use through 07/31/2012. OMB 0651-0031

 U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE

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	REQUEST FOR CONTINUED EXAMINATION(RCE)TRANSMITTAL (Submitted Only via EFS-Web)							
A 11 11	[-	-web)	• •		
Application Number	12561138	Filing Date	2009-09-16	Docket Number (if applicable)	ACQI-006/03US 310578-2053 ₽	Art Unit	2435	
First Named Inventor	William W.Y. Ch	u		Examiner Name	Song, Hosuk			
This is a Request for Continued Examination (RCE) under 37 CFR 1.114 of the above-identified application. Request for Continued Examination (RCE) practice under 37 CFR 1.114 does not apply to any utility or plant application filed prior to June 8, 1995, or to any design application. The Instruction Sheet for this form is located at WWW.USPTO.GOV								
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in which they	were filed unless	applicant in		applicant does not wi	nents enclosed with the RCE will sh to have any previously filed u			
	y submitted. If a fi on even if this box			any amendments file	ed after the final Office action ma	y be cor	isidered as a	
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Aff	idavit(s)/ Declara	tion(s)						
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				requested under 37 der 37 CFR 1.17(i) re	CFR 1.103(c) for a period of mo quired)	nths _		
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🗙 Patent	Practitioner Sign	ature						
Applic	ant Signature							

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	Signature of Registered U.S. Patent Practitioner							
Signature	/Cliff Z. Liu/	Date (YYYY-MM-DD)	2011-06-17					
Name	Cliff Z. Liu	Registration Number	50834					

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- 6. A record in this system of records may be disclosed, as a routine use, to another federal agency for purposes of National Security review (35 U.S.C. 181) and for review pursuant to the Atomic Energy Act (42 U.S.C. 218(c)).
- 7. A record from this system of records may be disclosed, as a routine use, to the Administrator, General Services, or his/her designee, during an inspection of records conducted by GSA as part of that agency's responsibility to recommend improvements in records management practices and programs, under authority of 44 U.S.C. 2904 and 2906. Such disclosure shall be made in accordance with the GSA regulations governing inspection of records for this purpose, and any other relevant (i.e., GSA or Commerce) directive. Such disclosure shall not be used to make determinations about individuals.
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Attorney Docket No. ACQI-006/03US 310578-2053

PATENT

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Re-Issue of U.S.
Patent No. 6,643,777William W.Y. Chu
Confirmation No.:Confirmation No.:1717Serial No.:12/561,138Group Art Unit:2435Filed:September 16, 2009Examiner:Hosuk Song

FOR: DATA SECURITY METHOD AND DEVICE FOR COMPUTER MODULES

Mail Stop: RCE Commissioner for Patents P.O. Box 1450 Alexandria, VA 22313-1450

AMENDMENT/RESPONSE TO FINAL OFFICE ACTION ACCOMPANYING RCE

In response to the Final Office Action mailed March 17, 2011, please amend the subject application as follows:

Amendments to the Drawings begin on page 2 of this paper.

Amendments to the Specification begin on page 3 of this paper.

Amendments to the Claims are reflected in the listing of the claims which begins on page 4 of this paper.

Remarks/Arguments begin on page 20 of this paper.

IN THE DRAWINGS:

Attachment: New Sheets FIG. 17 through FIG. 20

The subject application is amended to specifically include certain figures from U.S. Patent No. 6,345,330 and U.S. Provisional Application No. 60/083,886.

IN THE SPECIFICATION:

Please add the following new paragraphs after the paragraphs previously added at col. 4, line 51:

FIG. 17 is a partial block diagram of a computer system using the interface of the present invention as a bridge between the north and south bridges of the computer system.

FIG. 18 is a partial block diagram of a computer system in which the north and south bridges are integrated with the host and peripheral interface controllers, respectively.

FIG. 19 shows an attached computer module with Integrated CPU/NB/Graphics and Integrated HIC/SB.

FIG. 20 shows an attached computer module with single chip fully integrated: CPU, Cache, Core Logic, Graphics controller and Interface controller.

Please add the following new paragraph after the paragraphs previously added at col. 13, line 33:

In the embodiment shown in FIG. 13, HIC 1319 is coupled to an integrated unit 1321 that includes a CPU, a cache and a north bridge. In another embodiment, such as that shown in FIG. 17, the CPU 1705 and north bridge 1710 are separate rather than integrated units. In yet another embodiment, such as that shown in FIG. 18, the HIC and PIC are integrated with the north and south bridges, respectively, such that integrated HIC and north bridge unit 1805 includes an HIC and a north bridge, while integrated PIC and south bridge unit 1810 includes a PIC and a south bridge. FIG. 19 shows an attached computer module with integrated CPU/NB/Graphics 1915 and Integrated HIC/SB 1920. FIG. 20 shows an attached computer module with single chip 2025 fully integrated: CPU, Cache, Core Logic, Graphics controller and Interface controller.

Atty. Docket No. ACQI-006/03US 310578-2053 Serial No. 12/561,138

IN THE CLAIMS:

1-13. (Cancelled)

14. (Twice Amended) <u>A system for information transaction, the system comprising:</u> <u>a console comprising</u>

<u>a first low voltage differential signal channel comprising two sets of</u> <u>unidirectional, multiple serial bit channels to transmit data in opposite directions,</u>

<u>a first interface controller coupled to the first low voltage differential signal</u> <u>channel to communicate an encoded serial bit stream of Peripheral Component Interconnect</u> ("PCI") bus transaction,

a power supply, and

a hard disk drive housed in the console; and

a computer module coupled to the console, the computer module comprising

a central processing unit,

a peripheral bridge directly coupled to the central processing unit without any intervening PCI bus, the peripheral bridge comprising a second interface controller,

<u>a second differential signal channel extending directly from the second interface</u> <u>controller, the second differential signal channel comprising two sets of unidirectional, serial bit</u> <u>channels to transmit data in opposite directions</u>,

a mass storage device coupled to the central processing unit through the peripheral bridge, and

a security mechanism to provide access protection for the computer module, wherein the computer module is configured to receive power from the power supply.

15. (Previously Presented) <u>The system of claim 14</u>, wherein the computer module further comprises a computing environment for a user.

16. (Previously Presented) <u>The system of claim 14</u>, wherein the computer module is coupled to the console through serial bit stream data paths employing low voltage differential signaling.

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17. (Twice Amended) <u>A system for information transaction, the system comprising:</u>

a console comprising

an integrated Liquid Crystal Display and

<u>a first low voltage differential signal channel comprising two sets of</u> <u>unidirectional, multiple serial bit channels to communicate an encoded serial bit stream of</u> Peripheral <u>Component Interconnect ("PCI") bus transaction in opposite directions; and</u>

a computer module coupled to the console in a "plug and play" operation, the computer module comprising

a central processing unit,

a peripheral bridge directly coupled to the central processing unit without any intervening PCI bus, the peripheral bridge comprising an interface controller that is integrated with the peripheral bridge,

a second differential signal channel extending directly from the interface controller, the second differential signal channel comprising two sets of unidirectional, serial bit channels to transmit data in opposite directions,

a mass storage device coupled to the central processing unit, and

wherein the interface controller is configured to communicate a differential signaling serial bit stream with the console through the second differential signal channel.

18. (Previously Presented) <u>The system of claim 17, wherein the computer module further</u> comprises a computing environment for a user.

19. (Previously Presented) <u>The system of claim 17</u>, wherein the computer module further comprises a hardware dependent security code to perform security identification matching.

20. (Twice Amended) <u>A system for information transaction, the system comprising:</u> <u>a console comprising</u>

<u>a power supply,</u>

<u>a first low voltage differential signal channel comprising two sets of</u> unidirectional, serial bit channels to transmit data in opposite directions, and

a removable media drive housed in the console; and

<u>a computer module coupled to the console, the computer module comprising</u> <u>a central processing unit comprising an interface controller,</u>

a mass storage device coupled to the central processing unit, and

a second low voltage differential signal channel extending directly from the interface controller, the second low voltage differential signal channel comprising two sets of unidirectional, serial bit channels to transmit data in opposite directions, and

wherein the interface controller is coupled to the console through the second low voltage differential signal channel,

wherein the computer module is configured to receive power from the power supply.

21. (Previously Presented) <u>The system of claim 20, wherein the first low voltage differential</u> signal channel and the second low voltage differential signal channel are configured to transmit data in 10-bit packets.

22. (Previously Presented) <u>The system of claim 20, wherein the computer module further</u> comprises a computing environment for a user.

23. (Previously Presented) <u>The system of claim 20, wherein the first low voltage differential</u> signal channel is coupled to the second low voltage differential signal channel upon coupling of the computer module to the console.

24. (Twice Amended) <u>A system to connect a computer module to a network, the system comprising:</u>

a console comprising

a power supply,

<u>a first low voltage differential signal channel comprising two sets of</u> <u>unidirectional, multiple serial bit channels to communicate an encoded serial bit stream of</u> <u>Peripheral Component Interconnect ("PCI") bus transaction in opposite directions, and</u>

an Ethernet controller to provide access to a network; and

a computer module coupled to the console and powered by the power supply, the computer module comprising

a central processing unit comprising an integrated interface controller,

a second low voltage differential signal channel directly coupled to the integrated interface controller, the second low voltage differential signal channel comprising two sets of unidirectional, serial bit channels to transmit data in opposite directions,

a mass storage device coupled to the central processing unit, and

a connection software code,

wherein, upon coupling to the console, the computer module is configured to establish a connection to the network using the connection software code.

25. (Previously Presented) <u>The system of claim 24</u>, wherein the computer module is coupled to the console in a "plug and play" operation.

26. (Previously Presented) <u>The system of claim 24</u>, wherein the computer module further comprises a computing environment for a user.

27. (Amended) <u>An information transaction system comprising:</u>

a console comprising

an integrated keyboard,

an integrated Liquid Crystal Display,

<u>a first low voltage differential signal channel comprising two sets of</u> <u>unidirectional, serial bit channels to transmit data in opposite directions, and</u>

an interface controller coupled to the first low voltage differential signal channel to communicate an encoded serial bit stream of Peripheral Component Interconnect ("PCI") bus transaction; and

a computer module coupled to the console in a "plug and play" operation, the computer module comprising

a central processing unit,

a peripheral bridge coupled to the central processing unit without any intervening PCI bus,

a second low voltage differential signal channel coupled to the peripheral bridge, the second low voltage differential signal channel comprising two sets of unidirectional, serial bit channels to transmit data in opposite directions, and

a mass storage device comprising a flash memory.

28. (Previously Presented) <u>The system of claim 27</u>, wherein the central processing unit comprises an integrated circuit chip to operate on a varying clock frequency to vary a power consumption of the integrated circuit chip while in operation.

29. (Previously Presented) <u>The system of claim 27</u>, wherein the computer module further comprises a computing environment for a user.

30. (Amended) The system of claim 27, wherein the peripheral bridge is directly coupled to the second low voltage differential signal channel to communicate a serial bit stream to the console.

(Twice Amended) <u>A system for information transaction, the system comprising:</u>
 <u>a console comprising</u>

an integrated keyboard,

an integrated Liquid Crystal Display, and

<u>a first low voltage differential signal channel comprising two sets of</u> unidirectional, serial bit channels to transmit data in opposite directions; and

a computer module coupled to the console, the computer module comprising

a central processing unit,

a peripheral bridge directly coupled to the central processing unit without any intervening Peripheral Component Interconnect bus, the peripheral bridge comprising an interface controller,

a mass storage device comprising a flash memory, and

a second low voltage differential signal channel extending directly from the interface controller, the second low voltage differential signal channel comprising two sets of unidirectional, serial bit channels to transmit data in opposite directions,

wherein the interface controller is coupled to the console through the second low voltage differential signal channel,

wherein the first low voltage differential signal channel is coupled to the second low voltage differential signal channel upon coupling of the computer module to the console.

32. (Previously Presented) <u>The system of claim 31, wherein the computer module further</u> comprises a security program to specify a security identification.

33. (Previously Presented) <u>The system of claim 31</u>, wherein the computer module further comprises a computing environment for a user.

34. (Twice Amended) <u>An information transaction system comprising:</u>

a console comprising

<u>a power supply,</u>

<u>a first low voltage differential signal channel comprising two sets of</u> unidirectional, serial bit channels to transmit data in opposite directions, and

a removable media drive housed in the console; and

a computer module coupled to the console, the computer module comprising

an integrated interface controller and central processing unit configured as a single chip,

<u>a flash memory comprising a security identification to provide access protection</u> for the computer module, and

a second low voltage differential signal channel extending directly from the integrated interface controller and central processing unit, the second low voltage differential signal channel comprising two sets of unidirectional, serial bit channels to transmit data in opposite directions,

wherein the integrated interface controller and central processing unit is coupled to the console through the second low voltage differential signal channel,

wherein the computer module is configured to receive power from the power supply.

35. (Previously Presented) <u>The system of claim 34</u>, wherein the computer module further comprises a computing environment for a user.

36. (Previously Presented) <u>The system of claim 34</u>, wherein the first low voltage differential signal channel is coupled to the second low voltage differential signal channel upon coupling of the computer module to the console.

37. (Twice Amended) <u>A method to connect a computer module to a network, the method</u> comprising:

providing a computer module, the computer module comprising (a) a central processing unit and (b) a storage device comprising a connection program;

inserting the computer module into a computer console in a "plug and play" operation, the computer console comprising (a) a low voltage differential signal channel comprising two sets of unidirectional, multiple serial bit channels to communicate an encoded serial bit stream of Peripheral Component Interconnect ("PCI") bus transaction in opposite directions and (b) a networking device to provide access to an external network;

receiving connection information from the computer console to the computer module; and

using the connection program, establishing a connection between the computer module and the external network.

38. (Previously Presented) <u>The method of claim 37, further comprising coupling the</u> <u>computer module to the low voltage differential signal channel.</u>

39. (Previously Presented) <u>The method of claim 37</u>, wherein establishing the connection between the computer module and the external network comprises communicating with the external network through Ethernet.

40. (Twice Amended) <u>A computer system comprising:</u>

a console comprising

a power supply and

<u>a first low voltage differential signal channel comprising two sets of</u> <u>unidirectional, serial bit channels to transmit data in opposite directions; and</u>

a computer module coupled to the console, the computer module comprising

<u>a central processing unit to operate on a varying clock frequency to vary a power</u> <u>consumption of the central processing unit while in operation</u>,

a mass storage unit coupled to the central processing unit,

<u>a second low voltage differential signal channel comprising two sets of</u> <u>unidirectional, serial bit channels to transmit data in opposite directions, and</u>

a peripheral bridge directly coupled to the central processing unit without any intervening Peripheral Component Interconnect bus, the peripheral bridge comprising an interface controller to output a serial bit stream that is conveyed over the second low voltage differential signal channel,

wherein the interface controller is coupled to the console through the second low voltage differential signal channel,

wherein the computer module is configured to receive power from the power supply.

41. (Previously Presented) <u>The computer system of claim 40</u>, wherein the computer module further comprises a computing environment for a user.

42. (Previously Presented) <u>The computer system of claim 40</u>, wherein the first low voltage differential signal channel is coupled to the second low voltage differential signal channel upon coupling of the computer module to the console for data communication.

43. (Previously Presented) <u>The computer system of claim 40</u>, wherein the computer module is configured for insertion into the console as a "plug and play" operation.

44. (Twice Amended) <u>A system to connect a computer module to a network, the system</u> comprising:

a console comprising

a power supply and

a connection to a network; and

a computer module coupled to the console in a "plug and play" operation, the computer module comprising

a processing unit,

<u>a low voltage differential signal channel comprising two sets of unidirectional,</u> <u>multiple serial bit channels to transmit data in opposite directions,</u>

a peripheral bridge comprising an interface controller coupled to the low voltage differential signal channel to communicate an encoded serial bit stream of address and data of Peripheral Component Interconnect ("PCI") bus transaction, the peripheral bridge coupled to the processing unit without any intervening PCI bus, and

a mass storage device comprising a connection program,

wherein the computer module is configured to receive power from the power supply, and the connection program is configured to establish communication with the network through the console.

45. (Previously Presented) <u>The system of claim 44</u>, wherein the processing unit comprises an integrated circuit chip to operate on a varying clock frequency to vary a power consumption of the integrated circuit chip while in operation.

46. (Previously Presented) <u>The system of claim 44</u>, wherein the connection to the network comprises an Ethernet connection.

47. (Previously Presented) <u>The system of claim 44</u>, wherein the computer module further comprises a computing environment for a user.

48. (Twice Amended) <u>A computer system comprising:</u>

 <u>a console comprising a power supply; and</u>
 <u>a computer module coupled to the console, the computer module comprising</u>
 <u>a central processing unit,</u>

<u>a low voltage differential signal channel comprising two sets of unidirectional,</u> <u>multiple serial bit channels to transmit data in opposite directions,</u>

an integrated interface controller and bridge unit coupled to the low voltage differential signal channel to communicate an encoded serial bit stream of address and data of Peripheral Component Interconnect ("PCI") bus transaction, the integrated interface controller and bridge unit directly coupled to the central processing unit without any intervening PCI bus, and

a mass storage device coupled to the central processing unit,

wherein the computer module is configured to receive power from the power supply, and the computer module is configured to communicate, through Ethernet, to a local area network upon coupling of the computer module to the console. 49. (Previously Presented) <u>The computer system of claim 48, wherein the computer module</u> is configured for insertion into the console as a "plug and play" operation.

50. (Previously Presented) <u>The computer system of claim 48, wherein the mass storage</u> device is a first mass storage device, and the console further comprises a second mass storage device coupled to the computer module and configured to receive power from the power supply.

51. (Previously Presented) <u>The computer system of claim 48</u>, wherein the central processing unit is configured to operate on a varying clock frequency to vary a power consumption of the central processing unit while in operation.

52. (Twice Amended) <u>A computer system comprising:</u> <u>a console comprising a power supply; and</u>

a computer module coupled to the console, the computer module comprising

a central processing unit to operate on a varying clock frequency to vary a power consumption of the central processing unit while in operation,

a low voltage differential signal channel comprising two sets of unidirectional, multiple serial bit channels to transmit data in opposite directions,

a peripheral bridge comprising an interface controller coupled to the low voltage differential signal channel to communicate an encoded serial bit stream of Peripheral Component Interconnect ("PCI") bus transaction, the interface controller coupled to the central processing unit without any intervening PCI bus, and

a graphics controller coupled to the central processing unit,

wherein the computer module is configured to receive power from the power supply.

53. (Previously Presented) <u>The computer system of claim 52</u>, wherein the computer module <u>further comprises a core computing environment for a user.</u>

54. (Previously Presented) <u>The computer system of claim 52</u>, wherein the computer module is configured for insertion into the console as a "plug and play" operation.

55. (Twice Amended) <u>A computer system for secured information transaction, the computer system comprising:</u>

a console to connect to a network;

a keyboard coupled to the console; and

a computer module coupled to the console, the computer module comprising

a central processing unit,

<u>a low voltage differential signal channel comprising two sets of unidirectional,</u> <u>multiple serial bit channels to transmit data in opposite directions,</u>

a peripheral bridge comprising an interface controller coupled to the low voltage differential signal channel to communicate an encoded serial bit stream of Peripheral Component Interconnect ("PCI") bus transaction, the interface controller coupled to the central processing unit without any intervening PCI bus, and

a mass storage unit storing a security program and a first user identification data, wherein the security program is configured to receive a second user identification data via the keyboard, perform a comparison of the first user identification data and the second user identification data, and permit access to the computer module based on the comparison.

56. (Previously Presented) <u>The computer system of claim 55</u>, wherein the security program is further configured to identify a predetermined security status and control a level of access privilege to the computer module.

57. (Previously Presented) <u>The computer system of claim 55</u>, wherein the central processing unit is configured to operate on a varying clock frequency to vary a power consumption of the central processing unit while in operation.

58. (Twice Amended) <u>An information system comprising:</u> a console comprising

a power supply and

<u>a first low voltage differential signal channel comprising two sets of</u> <u>unidirectional, serial bit channels to transmit data in opposite directions; and</u>

<u>a computer module coupled to the console, the computer module comprising</u> <u>a central processing unit comprising an integrated interface controller</u>, a mass storage device coupled to the central processing unit,

a graphics controller coupled to the central processing unit, and

a second low voltage differential signal channel extending directly from the central processing unit, the second low voltage differential signal channel comprising two sets of unidirectional, serial bit channels to transmit data in opposite directions,

wherein the interface controller is coupled to the console through the second low voltage differential signal channel,

wherein the computer module is configured to receive power from the power supply.

59. (Previously Presented) <u>The information system of claim 58</u>, wherein the first low voltage differential signal channel is coupled to the second low voltage differential signal channel for data communication upon coupling of the computer module to the console.

60. (Previously Presented) <u>The information system of claim 58</u>, wherein the computer module is configured for insertion into the console as a "plug and play" operation.

61. (New) The system of claim 14, wherein the encoded serial bit stream comprises 10 bit packets.

62. (New) The system of claim 61, wherein the first interface controller is configured to output encoded PCI address and data bits in serial form that are conveyed over the first low voltage differential signal channel.

63. (New) <u>The system of claim 14</u>, wherein the second interface controller is integrated with the peripheral bridge as a single integrated unit.

64. (New) <u>The system of claim 17</u>, wherein the encoded serial bit stream of PCI bus transaction comprises information to permit decoding to create a PCI bus transaction across the first low voltage differential signal channel.

65. (New) <u>The system of claim 17</u>, wherein the mass storage device is coupled to the central processing unit through the peripheral bridge.

66. (New) The system of claim 20, wherein the central processing unit and the interface controller are integrated in a single chip.

67. (New) <u>The system of claim 66</u>, wherein the central processing unit comprises a graphics subsystem integrated in the single chip.

68. (New) The system of claim 24, wherein the encoded serial bit stream comprises encoded PCI address and data bits in serial form that are conveyed over the first low voltage differential signal channel as 10 bit packets.

69. (New) The system of claim 24, wherein the integrated interface controller is configured to output a serial bit stream that is conveyed over the second low voltage differential signal channel as data packets.

70. (New) <u>The system of claim 69</u>, wherein the serial bit stream comprises information of <u>Universal Serial Bus protocol.</u>

71. (New) <u>The system of claim 30</u>, wherein the peripheral bridge is configured to output the serial bit stream that is conveyed over the second low voltage differential signal channel as data <u>packets</u>.

72. (New) <u>The system of claim 71</u>, wherein the serial bit stream comprises information of <u>Universal Serial Bus protocol.</u>

73. (New) The system of claim 31, wherein the interface controller is integrated with the peripheral bridge as a single integrated unit.

74. (New) <u>The system of claim 73</u>, wherein the interface controller is configured to output a serial bit stream that is conveyed over the second low voltage differential signal channel as 10 bit packets.
75. (New) The system of claim 34, wherein the integrated interface controller and central processing unit comprises a graphics subsystem integrated in the single chip.

76. (New) The system of claim 34, wherein the integrated interface controller and central processing unit is configured to output a serial bit stream that is conveyed over the second low voltage differential signal channel as data packets.

77. (New) The system of claim 76, wherein the serial bit stream comprises information of Universal Serial Bus protocol.

78. (New) The method of claim 37, further comprising conveying, over the low voltage differential signal channel, the encoded serial bit stream as 10 bit packets.

79. (New) <u>The method of claim 78, wherein conveying the encoded serial bit stream</u> comprises conveying information to permit decoding to create a PCI bus transaction across the low voltage differential signal channel.

80. (New) The computer system of claim 40, wherein the interface controller is integrated with the peripheral bridge as a single integrated unit.

81. (New) <u>The computer system of claim 80</u>, wherein the serial bit stream is conveyed over the second low voltage differential signal channel as 10 bit packets.

82. (New) <u>The computer system of claim 80, wherein the serial bit stream comprises</u> information of Universal Serial Bus protocol.

83. (New) The system of claim 44, wherein the encoded serial bit stream comprises 10 bit packets.

84. (New) The system of claim 83, wherein the interface controller is configured to output the encoded serial bit stream that is conveyed over the low voltage differential signal channel.

85. (New) <u>The computer system of claim 48</u>, wherein the integrated interface controller and bridge unit is configured as a single integrated unit.

86. (New) <u>The computer system of claim 85</u>, wherein the integrated interface controller and bridge unit is configured to output the encoded serial bit stream as 10 bit packets that are conveyed over the low voltage differential signal channel.

87. (New) <u>The computer system of claim 52</u>, wherein the peripheral bridge is directly coupled to the central processing unit without any intervening PCI bus.

88. (New) <u>The computer system of claim 87, wherein the interface controller is configured to</u> output the encoded serial bit stream as 10 bit packets that are conveyed over the low voltage <u>differential signal channel.</u>

89. (New) <u>The computer system of claim 88, wherein the encoded serial bit stream comprises</u> information to permit decoding to create a PCI bus transaction across the low voltage differential <u>signal channel.</u>

90. (New) <u>The computer system of claim 55</u>, wherein the peripheral bridge is directly coupled to the central processing unit without any intervening PCI bus.

91. (New) <u>The computer system of claim 90</u>, wherein the interface controller is integrated with the peripheral bridge as a single integrated unit.

92. (New) <u>The computer system of claim 91, wherein the encoded serial bit stream comprises</u> encoded PCI address and data bits in serial form.

93. (New) <u>The information system of claim 58</u>, wherein the integrated interface controller is configured to output a serial bit stream that is conveyed over the second low voltage differential signal channel.

94. (New) The information system of claim 93, wherein the serial bit stream is conveyed over the second low voltage differential signal channel as 10 bit packets.

95. (New) <u>The information system of claim 93</u>, wherein the serial bit stream comprises information of Universal Serial Bus protocol.

REMARKS

Drawings and Specification

The subject application is a continuation reissue application, for the reissue of original U.S. Patent No. 6,643,777 (the "777 patent"). At col. 5, lines 9-13, the '777 patent incorporated by reference U.S. Application No. 09/149,882, now issued as U.S. Patent No. 6,345,330 (the "330 patent"), which, in turn, claimed the benefit of and incorporated by reference U.S. Provisional Application No. 60/083,886 (the "886 provisional application") (See checked incorporation by reference box in utility patent application transmittal of U.S. Application No. 09/149,882 filed on September 8, 1998). By this paper, the subject application is amended to specifically include certain figures and text from the '330 patent, as well as certain figures and text from the '886 provisional application. Specifically, the subject application is amended to add new FIG. 17 through FIG. 20, as well as accompanying text. This corresponds to: (a) FIG. 3 and FIG. 4 of the '330 patent; (b) the text of the '330 patent at col. 3, lines 48-53 and col. 6, lines 26-35; (c) figure 8 and figure 9 of the '886 provisional application; and (d) the text of the '886 provisional application as originally included in legends of figure 8 and figure 9. For purposes of consistency, FIG. 3 of the '330 patent and its accompanying reference numbers having the format 3xx are re-labeled as FIG. 17 and reference numbers having the format 17xx. Likewise, FIG. 4 of the '330 patent and figure 8 and figure 9 of the '886 provisional application and their accompanying reference numbers are re-labeled for purposes of consistency. Otherwise, Applicant respectfully submits that the added figures and text correspond to the above-noted figures and text of the '330 patent and the '886 provisional application, and that no new matter is added.

Status of Claims and Support for Claim Changes

Claims 14-60 were pending in the subject application. Claims 1-13 were previously cancelled. In accordance with this paper, Applicant is submitting the following amendments:

• Claim 14 is amended to specify that the console comprises (1) a "first" low voltage differential signal channel and (2) "a first" interface controller coupled to the "first" low voltage differential signal channel to communicate an encoded serial bit stream of Peripheral Component Interconnect "("PCI")" bus transaction, and that the computer module comprises (1) "a peripheral bridge directly coupled to the central

processing unit without any intervening PCI bus, the peripheral bridge comprising a second interface controller," (2) "a second differential signal channel extending directly from the second interface controller, the second differential signal channel comprising two sets of unidirectional, serial bit channels to transmit data in opposite directions," and (3) a mass storage device coupled to the central processing unit "through the peripheral bridge." These amendments have support, for example, in the original '777 patent at col. 10, lines 1-11 and lines 17-30, as well as in the incorporated '330 patent at FIG. 4, FIG. 23, col. 6, lines 30-35, col. 7, line 61 to col. 8, line 4, and col. 15, line 31 to col. 16, line 5.

- Claim 17 is amended to specify that the console comprises a "first" low voltage differential signal channel comprising two sets of unidirectional, multiple serial bit channels to communicate an encoded serial bit stream of Peripheral Component Interconnect "("PCI")" bus transaction in opposite directions, and that the computer module comprises (1) "a peripheral bridge directly coupled to the central processing unit without any intervening PCI bus, the peripheral bridge comprising an interface controller that is integrated with the peripheral bridge," and (2) "a second differential signal channel extending directly from the interface controller, the second differential signal channel comprising two sets of unidirectional, serial bit channels to transmit data in opposite directions," and "wherein the" interface controller "is configured" to communicate a differential signaling serial bit stream with the console "through the second differential signal channel." These amendments have support, for example, in the incorporated '330 patent at FIG. 4, FIG. 23, col. 6, lines 30-35, col. 7, line 61 to col. 8, line 4, and col. 15, line 31 to col. 16, line 5.
- Claim 20 is amended to specify that the computer module comprises (1) a central processing unit "comprising an interface controller," and (2) a second low voltage differential signal channel "extending directly from the interface controller, the second low voltage differential signal channel" comprising two sets of unidirectional, serial bit channels to transmit data in opposite directions, and "wherein the" interface controller "is" coupled to the console through the second low voltage differential signal channel. These amendments have support, for example, in the incorporated '330 patent at col. 15, line 31 to col. 16, line 5, as well as in the incorporated '886 provisional application at figure 9.

- Claim 24 is amended to specify that the console comprises a "first" low voltage differential signal channel comprising two sets of unidirectional, multiple serial bit channels to communicate an encoded serial bit stream of Peripheral Component Interconnect "("PCI")" bus transaction in opposite directions, and that the computer module comprises (1) a central processing unit "comprising an integrated interface controller," and (2) "a second low voltage differential signal channel directly coupled to the integrated interface controller, the second low voltage differential signal channel stot transmit data in opposite directions." These amendments have support, for example, in the incorporated '330 patent at col. 7, line 61 to col. 8, line 4 and col. 15, line 31 to col. 16, line 5, as well as in the incorporated '886 provisional application at figure 9.
- Claim 27 is amended to specify that the console comprises (1) a "first" low voltage differential signal channel comprising two sets of unidirectional, serial bit channels to transmit data in opposite directions, and (2) an interface controller coupled to the "first" low voltage differential signal channel to communicate an encoded serial bit stream of Peripheral Component Interconnect "("PCI")" bus transaction, and that the computer module comprises (1) "a peripheral bridge coupled to the central processing unit without any intervening PCI bus," and (2) "a second low voltage differential signal channel coupled to the peripheral bridge, the second low voltage differential signal channel comprising two sets of unidirectional, serial bit channels to transmit data in opposite directions." These amendments have support, for example, as discussed above for claim 17.
- Claim 30 is amended to specify that the "peripheral bridge" is "directly" coupled to the "second" low voltage differential signal channel to communicate a serial bit stream to the console. These amendments have support, for example, in the incorporated '330 patent at FIG. 4, FIG. 23, col. 6, lines 30-35, and col. 15, line 31 to col. 16, line 5.
- Claim 31 is amended to specify that the computer module comprises (1) "a peripheral bridge directly coupled to the central processing unit without any intervening Peripheral Component Interconnect bus, the peripheral bridge comprising an interface controller," and (2) a second low voltage differential signal channel "extending directly from the interface controller, the second low voltage differential signal

channel" comprising two sets of unidirectional, serial bit channels to transmit data in opposite directions, and "wherein the" interface controller "is" coupled to the console through the second low voltage differential signal channel. These amendments have support, for example, as discussed above for claim 17.

- Claim 34 is amended to specify that the computer module comprises (1) "an integrated interface controller and" central processing unit "configured as a single chip," and (2) a second low voltage differential signal channel "extending directly from the integrated interface controller and central processing unit, the second low voltage differential signal channel" comprising two sets of unidirectional, serial bit channels to transmit data in opposite directions, and "wherein the integrated" interface controller "and central processing unit is" coupled to the console through the second low voltage differential signal channel. These amendments have support, for example, as discussed above for claim 20.
- Claim 37 is amended to specify two sets of unidirectional, multiple serial bit channels to communicate an encoded serial bit stream of Peripheral Component Interconnect "("PCI")" bus transaction in opposite directions. These amendments have support, for example, in the incorporated '330 patent at FIG. 23, col. 7, line 61 to col. 8, line 4, and col. 15, line 31 to col. 16, line 5.
- Claim 40 is amended to specify that the computer module comprises "a peripheral bridge directly coupled to the central processing unit without any intervening Peripheral Component Interconnect bus, the peripheral bridge comprising an interface controller to output a serial bit stream that is conveyed over the second low voltage differential signal channel," and "wherein the interface controller is" coupled to the console through the second low voltage differential signal channel. These amendments have support, for example, as discussed above for claim 17.
- Claim 44 is amended to specify that the computer module comprises "a peripheral bridge comprising" an interface controller coupled to the low voltage differential signal channel to communicate an encoded serial bit stream of "address and data of" Peripheral Component Interconnect "("PCI")" bus transaction, "the peripheral bridge coupled to the processing unit without any intervening PCI bus." These amendments have support, for example, in the incorporated '330 patent at FIG. 4, FIG. 23, col. 6,

lines 30-35, col. 7, line 61 to col. 8, line 4, col. 8, lines 61-67, and col. 15, line 31 to col. 16, line 5.

- Claim 48 is amended to specify that the computer module comprises an "integrated" interface controller "and bridge unit" coupled to the low voltage differential signal channel to communicate an encoded serial bit stream of "address and data of" Peripheral Component Interconnect "("PCI")" bus transaction, "the integrated interface controller and bridge unit directly coupled to the central processing unit without any intervening PCI bus." These amendments have support, for example, as discussed above for claim 44.
- Claim 52 is amended to specify that the computer module comprises "a peripheral bridge comprising" an interface controller coupled to the low voltage differential signal channel to communicate an encoded serial bit stream of Peripheral Component Interconnect "("PCI")" bus transaction, "the interface controller coupled to the central processing unit without any intervening PCI bus." These amendments have support, for example, as discussed above for claim 17.
- Claim 55 is amended to specify that the computer module comprises "a peripheral bridge comprising" an interface controller coupled to the low voltage differential signal channel to communicate an encoded serial bit stream of Peripheral Component Interconnect "("PCI")" bus transaction, "the interface controller coupled to the central processing unit without any intervening PCI bus." These amendments have support, for example, as discussed above for claim 17.
- Claim 58 is amended to specify that the computer module comprises (1) a central processing unit "comprising an integrated interface controller," and (2) a second low voltage differential signal channel "extending directly from the central processing unit, the second low voltage differential signal channel" comprising two sets of unidirectional, serial bit channels to transmit data in opposite directions, and "wherein the" interface controller "is" coupled to the console through the second low voltage differential signal channel. These amendments have support, for example, as discussed above for claim 20.
- New claim 61 is dependent from claim 14, and specifies that "the encoded serial bit stream comprises 10 bit packets." This claim has support, for example, in the incorporated '330 patent at col. 8, lines 61-67.

- New claim 62 is dependent from claim 61, and specifies that "the first interface controller is configured to output encoded PCI address and data bits in serial form that are conveyed over the first low voltage differential signal channel." This claim has support, for example, in the incorporated '330 patent at FIG. 23, col. 7, line 61 to col. 8, line 4, col. 8, lines 61-67, and col. 15, line 31 to col. 16, line 5.
- New claim 63 is dependent from claim 14, and specifies that "the second interface controller is integrated with the peripheral bridge as a single integrated unit." This claim has support, for example, in the incorporated '330 patent at FIG. 4 and col. 6, lines 30-35.
- New claim 64 is dependent from claim 17, and specifies that "the encoded serial bit stream of PCI bus transaction comprises information to permit decoding to create a PCI bus transaction across the first low voltage differential signal channel." This claim has support, for example, in the incorporated '330 patent at col. 7, line 61 to col. 8, line 4 and col. 8, lines 61-67.
- New claim 65 is dependent from claim 17, and specifies that "the mass storage device is coupled to the central processing unit through the peripheral bridge." This claim has support, for example, in the original '777 patent at col. 10, lines 1-11 and lines 17-30, as well as in the incorporated '330 patent at FIG. 4 and col. 6, lines 30-35.
- New claim 66 is dependent from claim 20, and specifies that "the central processing unit and the interface controller are integrated in a single chip." This claim has support, for example, in the incorporated '886 provisional application at figure 9.
- New claim 67 is dependent from claim 66, and specifies that "the central processing unit comprises a graphics subsystem integrated in the single chip." This claim has support, for example, in the incorporated '886 provisional application at figure 9.
- New claim 68 is dependent from claim 24, and specifies that "the encoded serial bit stream comprises encoded PCI address and data bits in serial form that are conveyed over the first low voltage differential signal channel as 10 bit packets." This claim has support, for example, in the incorporated '330 patent at FIG. 23, col. 8, lines 61-67, and col. 15, line 31 to col. 16, line 5.
- New claim 69 is dependent from claim 24, and specifies that "the integrated interface controller is configured to output a serial bit stream that is conveyed over the second

low voltage differential signal channel as data packets." This claim has support, for example, in the incorporated '330 patent at FIG. 4, FIG. 23, col. 6, lines 30-35, col. 8, lines 61-67, and col. 15, line 31 to col. 16, line 5.

- New claim 70 is dependent from claim 69, and specifies that "the serial bit stream comprises information of Universal Serial Bus protocol." This claim has support, for example, in the incorporated '330 patent at col. 16, lines 1-5.
- New claim 71 is dependent from claim 30, and specifies that "the peripheral bridge is configured to output the serial bit stream that is conveyed over the second low voltage differential signal channel as data packets." This claim has support, for example, in the incorporated '330 patent at FIG. 4, FIG. 23, col. 6, lines 30-35, col. 8, lines 61-67, and col. 15, line 31 to col. 16, line 5.
- New claim 72 is dependent from claim 71, and specifies that "the serial bit stream comprises information of Universal Serial Bus protocol." This claim has support, for example, as discussed above for claim 70.
- New claim 73 is dependent from claim 31, and specifies that "the interface controller is integrated with the peripheral bridge as a single integrated unit." This claim has support, for example, as discussed above for claim 63.
- New claim 74 is dependent from claim 73, and specifies that "the interface controller is configured to output a serial bit stream that is conveyed over the second low voltage differential signal channel as 10 bit packets." This claim has support, for example, as discussed above for claim 69.
- New claim 75 is dependent from claim 34, and specifies that "the integrated interface controller and central processing unit comprises a graphics subsystem integrated in the single chip." This claim has support, for example, as discussed above for claim 67.
- New claim 76 is dependent from claim 34, and specifies that "the integrated interface controller and central processing unit is configured to output a serial bit stream that is conveyed over the second low voltage differential signal channel as data packets." This claim has support, for example, in the incorporated '330 patent at FIG. 23, col. col. 8, lines 61-67, and col. 15, line 31 to col. 16, line 5, as well as in the incorporated '886 provisional application at figure 9.

- New claim 77 is dependent from claim 76, and specifies that "the serial bit stream comprises information of Universal Serial Bus protocol." This claim has support, for example, as discussed above for claim 70.
- New claim 78 is dependent from claim 37, and specifies "conveying, over the low voltage differential signal channel, the encoded serial bit stream as 10 bit packets." This claim has support, for example, in the incorporated '330 patent at FIG. 23, col. 8, lines 61-67, and col. 15, line 31 to col. 16, line 5.
- New claim 79 is dependent from claim 78, and specifies "conveying information to permit decoding to create a PCI bus transaction across the low voltage differential signal channel." This claim has support, for example, in the incorporated '330 patent at FIG. 23, col. 7, line 61 to col. 8, line 4, col. 8, lines 61-67, and col. 15, line 31 to col. 16, line 5.
- New claim 80 is dependent from claim 40, and specifies that "the interface controller is integrated with the peripheral bridge as a single integrated unit." This claim has support, for example, as discussed above for claim 63.
- New claim 81 is dependent from claim 80, and specifies that "the serial bit stream is conveyed over the second low voltage differential signal channel as 10 bit packets." This claim has support, for example, as discussed above for claim 61.
- New claim 82 is dependent from claim 80, and specifies that "the serial bit stream comprises information of Universal Serial Bus protocol." This claim has support, for example, as discussed above for claim 70.
- New claim 83 is dependent from claim 44, and specifies that "the encoded serial bit stream comprises 10 bit packets." This claim has support, for example, as discussed above for claim 61.
- New claim 84 is dependent from claim 83, and specifies that "the interface controller is configured to output the encoded serial bit stream that is conveyed over the low voltage differential signal channel." This claim has support, for example, in the incorporated '330 patent at FIG. 23, col. 7, line 61 to col. 8, line 4, col. 8, lines 61-67, and col. 15, line 31 to col. 16, line 5.

- New claim 85 is dependent from claim 48, and specifies that "the integrated interface controller and bridge unit is configured as a single integrated unit." This claim has support, for example, as discussed above for claim 63.
- New claim 86 is dependent from claim 85, and specifies that "the integrated interface controller and bridge unit is configured to output the encoded serial bit stream as 10 bit packets that are conveyed over the low voltage differential signal channel." This claim has support, for example, in the incorporated '330 patent at FIG. 4, FIG. 23, col. 6, lines 30-35, col. 7, line 61 to col. 8, line 4, col. 8, lines 61-67, and col. 15, line 31 to col. 16, line 5.
- New claim 87 is dependent from claim 52, and specifies that "the peripheral bridge is directly coupled to the central processing unit without any intervening PCI bus." This claim has support, for example, in the incorporated '330 patent at FIG. 4 and col. 6, lines 30-35.
- New claim 88 is dependent from claim 87, and specifies that "the interface controller is configured to output the encoded serial bit stream as 10 bit packets that are conveyed over the low voltage differential signal channel." This claim has support, for example, as discussed above for claim 86.
- New claim 89 is dependent from claim 88, and specifies that "the encoded serial bit stream comprises information to permit decoding to create a PCI bus transaction across the low voltage differential signal channel." This claim has support, for example, as discussed above for claim 79.
- New claim 90 is dependent from claim 55, and specifies that "the peripheral bridge is directly coupled to the central processing unit without any intervening PCI bus." This claim has support, for example, as discussed above for claim 87.
- New claim 91 is dependent from claim 90, and specifies that "the interface controller is integrated with the peripheral bridge as a single integrated unit." This claim has support, for example, as discussed above for claim 63.
- New claim 92 is dependent from claim 91, and specifies that "the encoded serial bit stream comprises encoded PCI address and data bits in serial form." This claim has support, for example, in the incorporated '330 patent at col. 7, line 61 to col. 8, line 4 and col. 8, lines 61-67.

- New claim 93 is dependent from claim 58, and specifies that "the integrated interface controller is configured to output a serial bit stream that is conveyed over the second low voltage differential signal channel." This claim has support, for example, as discussed above for claim 69.
- New claim 94 is dependent from claim 93, and specifies that "the serial bit stream is conveyed over the second low voltage differential signal channel as 10 bit packets." This claim has support, for example, as discussed above for claim 61.
- New claim 95 is dependent from claim 93, and specifies that "the serial bit stream comprises information of Universal Serial Bus protocol." This claim has support, for example, as discussed above for claim 70.

Therefore, claims 14-95 are now pending in the subject application. In accordance with 37 C.F.R. §1.173 and M.P.E.P. §1453 setting forth the manner of making amendments in reissue applications, the entire text of each pending claim is underlined to reflect additions relative to the original patent.

Oath/Declaration

Applicant is submitting a supplemental declaration for reissue application in view of the amendments.

Allowable Subject Matter

The Examiner has withdrawn other rejections of previously pending claims 14-60, and the sole remaining issue is a supplemental declaration for reissue application, which is submitted with this paper. As explained above, the amendments submitted by this paper add further specificity to these previously pending claims, and add claims dependent from these previously pending claims. For at least these reasons, claims 14-95 should be allowable.

Conclusion

In view of the foregoing, Applicant respectfully submits that no further impediments exist to the allowance of the subject application and, therefore, requests an indication of allowability. However, the Examiner is requested to call the undersigned if any questions or comments arise. The Director is hereby authorized to charge any appropriate fees under 37 C.F.R. §§1.16, 1.17, and 1.21 that may be required by this paper, and to credit any overpayment, to Deposit Account No. 50-1283.

Date: June 17, 2011 Customer No. 58249 Cooley LLP 777 6th Street NW, Suite 1100 Washington, DC 20001 Tel: (650) 843-5852 Fax: (202) 842-7899 Respectfully submitted, Cooley LLP

By:

Cliff Z. Liu Reg. No. 50,834

Computing System



FIGURE 17



FIGURE 18



Attached Computer Module with Integrated CPU/NB/Graphics and Integrated HIC/SB

FIG. 19



Attached Computer Module with Single Chip fully integrated: CPU, Cache, Core logic, Graphics controller and Interface controller

FIG.20

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	Attorney Docket Nu	mber ACQI-006/03US 310578-2053
SUPPLEMENTAL DECLARATION	First Named Invento	r William W.Y. Chu
FOR REISSUE	C	OMPLETE if known
PATENT APPLICATION	Application Number	12/561,138
TO CORRECT "ERRORS" STATEMENT	Filing Date	September 16, 2009
(37 CFR 1.175)	Art Unit	2435
	Examiner Name	Song, Hosuk

I/We hereby declare that:

Every error in the patent which was corrected in the present reissue application, and which is not covered by the prior oath(s) and/or declaration(s) submitted in this application, arose without any deceptive intention on the part of the applicant.

WARNING:

Petitioner/applicant is cautioned to avoid submitting personal information in documents filed in a patent application that may contribute to identity theft. Personal information such as social security numbers, bank account numbers, or credit card numbers (other than a check or credit card authorization form PTO-2038 submitted for payment purposes) is never required by the USPTO to support a petition or an application. If this type of personal information is included in documents submitted to the USPTO, petitioners/applicants should consider redacting such personal information from the documents before submitting them to the USPTO. Petitioner/applicant is advised that the record of a patent application is available to the public after publication of the application (unless a non-publication request in compliance with 37 CFR 1.213(a) is made in the application) or issuance of a patent. Furthermore, the record from an abandoned application may also be available to the public if the application is referenced in a published application or an issued patent (see 37 CFR 1.14). Checks and credit card authorization forms PTO-2038 submitted for payment purposes are not retained in the application file and therefore are not publicly available.

I/We hereby declare that all statements made herein of my/our own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under 18 U.S.C. 1001 and that such willful false statements may jeopardize the validity of the application or any patent issued thereon.

Name of Sole or First Inventor	petition has been filed for this unsigned	l inventor
Given Name (first and middle [if any])	Family Name or Sumame	•
William W.Y.	сни	
Inventor's to illiam to.	N. Chu	Date 6/16/2011
Name of Second Inventor.	petition has been filed for this unsigned	l inventor
Given Name (first and middle [if any])	Family Name or Surname	
Inventor's Signature		Date

Additional inventors or legal representatives(s) are being named on the _____ supplemental sheets PTO/SB/92A or 02LR attached hereto.

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Electronic Patent Application Fee Transmittal						
Application Number:	12:	561138				
Filing Date:	16-	Sep-2009				
Title of Invention: Data Security Method and Device For Computer Modules					'S	
First Named Inventor/Applicant Name:	First Named Inventor/Applicant Name: William W.Y. Chu					
Filer:	Cliff Z. Liu/Bobbie Jutras					
Attorney Docket Number:	AC	QI-006/03US 31057	8-2053			
Filed as Small Entity						
Utility under 35 USC 111(a) Filing Fees						
Description		Fee Code	Quantity	Amount	Sub-Total in USD(\$)	
Basic Filing:						
Pages:						
Claims:						
Miscellaneous-Filing:						
Petition:						
Patent-Appeals-and-Interference:						
Post-Allowance-and-Post-Issuance:						
Extension-of-Time:						

Description	Fee Code	Quantity	Amount	Sub-Total in USD(\$)
Miscellaneous:				
Request for continued examination	2801	1	405	405
	Total in USD (\$)		405	

Electronic Acl	knowledgement Receipt
EFS ID:	10335835
Application Number:	12561138
International Application Number:	
Confirmation Number:	1717
Title of Invention:	Data Security Method and Device For Computer Modules
First Named Inventor/Applicant Name:	William W.Y. Chu
Customer Number:	58249
Filer:	Cliff Z. Liu/Bobbie Jutras
Filer Authorized By:	Cliff Z. Liu
Attorney Docket Number:	ACQI-006/03US 310578-2053
Receipt Date:	17-JUN-2011
Filing Date:	16-SEP-2009
Time Stamp:	20:23:26
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	yes					
Payment Type	Deposit Account					
Payment was successfully received in RAM	\$405					
RAM confirmation Number	6801 501283					
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Document Number	Ei Document Description		File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)	
1	Request for Continued Examination	ACQI-006-03US_06-17-11_RCE.	697976	no	3	
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National Stage of an International Application under 35 U.S.C. 371

If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.

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	SEARCH FEE (37 CFR 1.16(k), (i), (i), (i), (i), (i), (i), (i), (i		N/A		N/A	11	N/A			N/A	
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2 0 2011 ਛੱ PATENT & TRADEM ORMATION DISCLOSURE ATEMENT BY APPLICANT

21	Complete if Known						
Application Number 12/561,138							
	Filing Date September 16, 2009						
	First Named Inventor	William W.Y. Chu					
	Art Unit	2435					
	Examiner Name	Hosuk Song					
	Attorney Docket Number	ACQI-006/03US 310578-2053					

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16 of

U. S. PATENT DOCUMENTS								
Examiner	Cite No.1	Document Number	Publication Date	Name of Patentee or	Pages, Columns, Lines, Where			
Initials*	-	Number-Kind Code ^{2 (if known)}	MM-DD-YYYY	Applicant of Cited Document	Relevant Passages or Relevant Figures Appear			
		12/322,858	02-05-2009	Chu				
		11/545,056	10-06-2006	Chu				
	A108	5764924	06-09-1998	Hong	<u></u>			
	A109	5317441	05-31-1994	Sidman				

		FOREIGN PA	TENT DOCUM	ENTS		
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	BA002	WO 94/000970	01-06-1994	Oakleigh Systems, Inc.		

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	C095	Part 3: Carrier sense multiple access with collision detertion (CSMA/CD) access method and physical layer specifications, IEEE Standard 802.3z, The Institute of Electrical and Electronics Engineers, Inc., July 1998, 1262 pages.	
	C133	Excerpt from "Microsoft Computer Dictionary, 5th Edition", Microsoft Press, 2002, pages 96, 329, 624 and 625.	
	C135	Intel Corporation, Intel 82559 Fast Ethernet Controller," [retrieved on 03-14-2011], Retrieved from the Internet: <url: 82559.htm="" controllers="" design="" http:="" lan="" network="" products="" www.intel.com="">, 1 page.</url:>	
	C136	GRUENER, J., "Vendors Pack in More Servers," PC Week, Vol. 14, No. 1, March 17, 1997, 2 pages.	<u>)</u>
	C137	GRIGONIS, R., "Fault Resilient PC's," Flatiron Publishing, 1996, 314 pages.	
	C138	Microsoft Press Computer User's Dictionary, pages 82 and 232, Kim Fryer ed., Microsoft Press, 1998, 5 pages.	
	C139	IBM Thinkpad Product Information Guide, IBM PC Company, April 28, 1998, 26 pages.	
	C140	The American Heritage Dictionary, pages 536, 607 and 770, Dell Publishing, 1994, 5 pages.	
	C141	The New IEEE Standard Dictionary of Electrical and Electronics Terms, Fifth Ed., page 1236, The Institute of Electrical and Electronics Engineers, Inc., 1993, 3 pages.	

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INFORMATION DISCLOSURE STATEMENT BY APPLICANT

Complete if Known				
Application Number	12/561,138			
Filing Date	September 16, 2009			
First Named Inventor	William W.Y. Chu			
Art Unit	2435			
Examiner Name	Hosuk Song			
Attorney Docket Number	ACQI-006/03US 310578-2053			

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Sheet 2

		NON PATENT LITERATURE DOCUMENTS		
Examiner Initials*				
	C142	Microsoft Press Computer Dictionary, Third Ed., pages 96, 313, and 355, Kim Fryer ed., Microsoft Press, 1997, 5 pages.		
	C143	IBM Dictionary of Computing, Tenth Ed., pages 139, 439, 480 and 629, George McDaniel ed., McGraw-Hill, Inc., August 1993, 16 pages.		
	C144	IEEE 100: The Authoritative Dictionary of IEEE Standards Terms, Seventh Ed., pages 703, 704, 856 and 1064, The Institute of Electrical and Electronics Engineers, Inc., 2000, 13 pages.		
	C145	Microsoft Press Computer Dictionary, Second Edition, pages 82, 92, 93 and 260, Alice Smith ed., Microsoft Press, 1994, 13 pages.		
	C146	Microsoft Press Computer User's Dictionary, pages 232, 262, and 275, Kim Fryer ed., Microsoft Press, 1998, 12 pages.		
(C147	FEIBEL, W., Encyclopedia of Networking, Third Edition, page 265, The Network Press, 2000, 4 pages.		
	C148	System 8000, Consolidated Network Server, Product Brief, Eversys Corporation, undated, 2 pages.		
	C149	System 8000, Consolidated Server, Presentation, Eversys Corporation, undated, 23 pages.	Γ	
	C150	IEEE Standard for a High Performance Serial Bus, IEEE Std 1394-1995, The Institute of Electrical and Electronics Engineers, Inc., 1996, 392 pages.		
	C151	RLX System 324 Hardware Installation Guide, RLX Technologies, Inc., 2001, 80 pages.		
	C152	RLX System 324 Platform Guide: RLX Linux Web Server, RLX Technologies, Inc., 2001, 73 pages.		
	C153	RLX System 324 Platform Guide - Windows Powered Web Server - ONLINE, undated, 39 pages.		
	C154	RLX System 324 Technical Guide: RLX Control Tower SNMP Implementation, RLX Techologies, 2001, 32 pages.		
	C155	RLX System 324 Technical Guide: RLX Control Tower SNMP Implementation, Supplementary Document, Draft, RLX Techologies, May 26, 2001, 48 pages.		
	C156	RLX System 324 Technical Guide: RLX Control Tower Backup/Restore, Draft, RLX Techologies, May 18, 2001, 8 pages.		
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	C158	"RocketLogix Passive I/O Board Topology," RocketLogix, Inc., Revision 6, May 24, 2000, 1 page.		
	C159	"RocketLogix Switched I/O Board Topology," RocketLogix, Inc., Revision 6, May 24, 2000, 1 page.		

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S	Substitute for form 1449A/PTO		Complete if Known			
				Application Number	12/561,138	
				Filing Date	September 16, 2009	
	INFORMATION DISCLOSURE			First Named Inventor	William W.Y. Chu	
	STATEMENT BY APPLICANT		JANT	Art Unit	2435	
	(Use as many sheets as necessary)			Examiner Name	Hosuk Song	
Sheet	5	of 1	6	Attorney Docket Number	ACQI-006/03US 310578-20	

Sheet

_{of} 16 Attorney Docket Number ACQI-006/03US 310578-2053

		NON PATENT LITERATURE DOCUMENTS	
Examiner Initials*	Cite No. ¹	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.	T ²
	C202	CHARLESWORTH, I., "Technology Audit, Data Exploration Server," Butler Group, September 1999, 8 pages.	
	C203	GROOM, P., "WhiteCross 9800 pre-release configuration details and USA Pricing Information," WhiteCross Systems Limited, November 3, 1998, 4 pages.	
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	C214	"ChatCom, Inc. Announces PentiumPro/200 MHz Server Module, Server Module Offers Scalability and High Availability for File Server Environments," ChatCom, Inc., Press Release, March 24, 1997, 3 pages.	
	C215	"ChatCom Strengthens Sales Management Team, Three New Sales Directors to Address Growing Demand for ChatCom's ChatterBox™," ChatCom, Inc., Press Release, March 18, 1997, 2 pages.	
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of 16

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	Filing Date	September 16, 2009			
	First Named Inventor	med Inventor William W.Y. Chu			
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	Examiner Name	Hosuk Song			
	Attorney Docket Number	ACQI-006/03US 310578-2053			

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	C218	"Astro Sciences Corporation Shareholders Elect Two New Directors, and Vote to Change Corporate Name to ChatCom, Inc.," Astro Sciences Corporation, Press Release, February 12, 1996, 2 pages.	
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	C220	"ChatCom Names James B. Mariner President/CEO," ChatCom, Inc., Press Relase, March 7, 1996, 2 pages.	
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<u></u>	C223	"Telecom Australia to Receive Astro Sciences/J&L 486 Services," Astro Sciences Corporatoin, Press Release, January 4, 1996, 1 page.	
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	C230	"Astro Sciences Corporation Receives Patent For Network Security and Management," Astro Sciences Corporation, News Release, June 6, 1995, 1 pages.	,
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First Named Inventor	William W.Y. Chu	
Art Unit	2435	
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Attorney Docket Number	ACQI-006/03US 310578-2053	

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	C233	"Astro Sciences Corporation Announces Signing of \$4 Million Credit Facility With Deutsche Financial Services," Astro Sciences Corporation, News Release, May 19, 1995, 1 page.	
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	C285	"Network Engines Announces New Clustered Application Servers for Web, Thin-Client and Windows NT Enterprise Environments," Network Engines, Inc., Press Release, October 8, 1997, 3 pages.	
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INFORMATION DISCLOSURE STATEMENT BY APPLICANT

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ſ	Application Number	12/561,138			
	Filing Date	September 16, 2009			
ſ	First Named Inventor	William W.Y. Chu			
ĺ	Art Unit	2435			
ſ	Examiner Name	Hosuk Song			
I	Attorney Docket Number	ACQI-006/03US 310578-2053			

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Sheet 11

		NON PATENT LITERATURE DOCUMENTS	
Examiner Initials* Cite No. ¹		Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.	T ²
	1F02	"Appendix 6A - Disclosure of Asserted Claims and Infringement Contentions," submitted by the Plaintiff in the U.S. District Court for the Eastern District of Texas, Case No. 6:09-cv-148-LED, 14 pages.	
	IF03	"Disclosure of Asserted Claims and Infringement Contentions," submitted by the Plaintiff in the U.S. District Court for the Eastern District of Texas, Case No. 6:09-cv-148-LED, served on September 14, 2009, 5 pages.	
	IF04	"Exhibit 1, Disclosure of Asserted Claims and Infringement Contentions for Defendant Appro International, Inc.," submitted by the Plaintiff in the U.S. District Court for the Eastern District of Texas, Case No. 6:09-cv-148-LED, served on September 14, 2009, 105 pages.	
	IF05	"Exhibit 2, Disclosure of Asserted Claims and Infringement Contentions for Defendant ClearCube Technology, Inc.," submitted by the Plaintiff in the U.S. District Court for the Eastern District of Texas, Case No. 6:09-cv-148-LED, served on September 14, 2009, 163 pages.	
····	IF06	"Exhibit 3, Disclosure of Asserted Claims and Infringement Contentions for Defendant Dell Inc.," submitted by the Plaintiff in the U.S. District Court for the Eastern District of Texas, Case No. 6:09-cv-148-LED, served on September 14, 2009, 184 pages.	
	IF07	"Exhibit 4, Disclosure of Asserted Claims and Infringement Contentions for Defendant Fujitsu America, Inc.," submitted by the Plaintiff in the U.S. District Court for the Eastern District of Texas, Case No. 6:09-cv-148-LED, served on September 14, 2009, 210 pages.	
	IF08	"Exhibit 5, Disclosure of Asserted Claims and Infringement Contentions for Defendant Hewlett-Packard Co.," submitted by the Plaintiff in the U.S. District Court for the Eastern District of Texas, Case No. 6:09-cv-148-LED, served on September 14, 2009, 279 pages.	
-	IF09	"Exhibit 6, Disclosure of Asserted Claims and Infringement Contentions for Defendant IBM Corp.," submitted by the Plaintiff in the U.S. District Court for the Eastern District of Texas, Case No. 6:09-cv-148-LED, served on September 14, 2009, 242 pages.	
	IF10	"Exhibit 7, Disclosure of Asserted Claims and Infringement Contentions for Defendant NEC Corp. of America," submitted by the Plaintiff in the U.S. District Court for the Eastern District of Texas, Case No. 6:09-cv-148-LED, served on September 14, 2009, 166 pages.	
	IF11	"Exhibit 8, Disclosure of Asserted Claims and Infringement Contentions for Defendant Sun Microsystems, Inc.," submitted by the Plaintiff in the U.S. District Court for the Eastern District of Texas, Case No. 6:09-cv-148-LED, served on September 14, 2009, 243 pages.	
	IF12	"Exhibit 9, Disclosure of Asserted Claims and Infringement Contentions for Defendant Super Micro Computer, Inc.," submitted by the Plaintiff in the U.S. District Court for the Eastern District of Texas, Case No. 6:09-cv-148-LED, served on September 14, 2009, 220 pages.	

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	First Named Inventor	William W.Y. Chu
	Art Unit	2435
	Examiner Name	Hosuk Song
	Attorney Docket Number	ACQI-006/03US 310578-2053

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	IF13	"Disclosure of Plaintiff's Reduced List of Asserted Claims," submitted by the Plaintiff in the U.S. District Court for the Eastern District of Texas, Case No. 6:09-00148-LED, served on July 30, 2010, 6 pages.	
	F01	"Memorandum Opinion and Order Construing Claim Terms and Denying Defendants' Motion for Partial Summary Judgment," Issued by the U.S. District Court for the Eastern District of Texas, Case No. 6:09-cv-148-LED on August 2, 2010, 18 pages.	
-	F02	"Memorandum Opinion and Order Construing Claim Terms," Issued by the U.S. District Court for the Eastern District of Texas, Tyler Division, Case No. 6:09-cv-148-LED, Document 602, Feb. 3, 2011, 12 pgs.	
	F03	"Jury Verdict Form," Returned by the Jury in the U.S. District Court for the Eastern District of Texas, Case No. 6:09-cv-148-LED on Februrary 23, 2011, 2 pages.	
	F04	"Final Judgement," Issued by the U.S. District Court for the Eastern District of Texas, Case No. 6:09-cv-148-LED on March 1, 2011, 1 page.	
	G001	"Complaint for Patent Infringement," Acqis v. Appro Int'I, Inc. et al., Case No. 6:09-cv-00148, filed April 2, 2009, 13 pages.	
	G010	"First Amended Complaint for Patent Infringement," Acqis v. Appro Int'l, Inc. et al., Case No. 6:09-cv-00148, filed May 18, 2009, 14 pages.	
	G011	"Defendant Clearcube Technology, Inc.'s Answer, Counterclaims to Acqis LLC's First Amended Complaint for Patent Infringement, and Jury Demand," Case No. 6:08-cv-00148, filed July 2, 2009, 28 pages.	
	G012	"Defendant Nex Computers Technology, Inc.'s Answer to Acqis LLC's First Amended Complaint for Patent Infringement, and Jury Demand," Case No. 6:09-cv-00148-LED, filed July 8, 2009, 16 pages.	
	G013	"Defendant Hitachi Ameirca, LTD.'s, Answer to Acqis LLC's First Amended Complaint for Patent Infringement, and Affirmative Defenses and Counterclaims," Case No. 6:09-cv-00148- LED, filed July 8, 2009, 22 pages.	
	G014	"Defendant International Business Machines Corp.'s Answer to Acqis LLC's First Amended Complaint, Affirmative Defenses, and Counterclaims," Case No. 6:09-cv-148-LED, filed July 8, 2009, 22 pages.	
	G015	"Second Amended Complaint for Patent Infringement," Acqis v. Appro Int'I, Inc. et al., Case No. 6:09-cv-00148, filed July 22, 2009, 49 pages.	T
	G016	"Defendant Appro's Answer, Affirmative Defenses, and Counterclaims to Acqis LLC's Second Amended Complaint for Patent Infringement," Case No. 6:09-cv-148, filed August 5, 2009, 43 pages.	

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Application Number	12/561,138	
Filing Date September 16, 2009		
First Named Inventor	William W.Y. Chu	
Art Unit	2435	
Examiner Name	Hosuk Song	
Attorney Docket Number	ACQI-006/03US 310578-2053	

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Sheet 13

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	G017	"Defendant International Business Machines Corp.'s Answer to Acqis LLC's Second Amended Complaint, Affirmative Defenses, and Counterclaims," Case No. 6:09-cv-148-LED, filed August 10, 2009, 28 pages.	
	G018	"Defendant Super Micro Computer, Inc.'s Answer and Counterclaims to Acqis LLC's Second Amended Complaint for Patent Infringement," Case No. 6:09-cv-148, filed August 10, 2009, 96 pages.	
	G019	"Defendant Sun Microsystems, Inc.'s Answer and Counterclaims to Acqis LLC's Second Amended Complaint for Patent Infringement," Case No. 6:09-cv-148, filed August 10, 2009, 95 pages.	
	G020	"NEC Corporation of America's Answer, Affirmative Defenses, and Counterclaims to Acqis LLC's Second Amended Complaint for Patent Infringement," Case No. 6:09-cv-00148-LED, filed August 10, 2009, 38 pages.	
	G021	"Answer to Plaintiff's Second Amended Complaint and Counterclaims of Defendant Fujitsu Computer Systems Corp., n/k/a/ Fujitsu America, Inc. to Acqis LLC's Second Amended Complaint for Patent Infringement," Case No. 6:09-cv-00148-LED, filed August 10, 2009, 34 pages.	
	G022	"Answer, Affirmative Defenses, and Counterclaims of Defendant Hewlett-Packard Company to Acqis LLC's Second Amended Complaint for Patent Infringement," Case No. 6:09-cv-148- LED, filed August 10, 2009, 40 pages.	
	G023	"Defendant Clearcube Technology, Inc.'s Answer, Counterclaims to Acqis LLC's Second Amended Complaint for Patent Infringement, and Jury Demand," Case No. 6:08-cv-00148, filed August 10, 2009, 39 pages.	
	G024	"Dell's Answer and Counterclaims to Acqis LLC's Second Amended Complaint," Case No. 6:09-cv-00148-LED, filed August 10, 2009, 36 pages.	
	G025	"Defendant Nex Computers Technology, Inc.'s Answer to Acqis LLC's Second Amended Complaint for Patent Infringement, and Jury Demand," Case No. 6:09-cv-00148-LED, filed August 10, 2009, 28 pages.	
<u>, , , , , , , , , , , , , , , , , , , </u>	G026	"Defendant Clearcube Technology, Inc.'s First Amended Answer, Counterclaims to Acqis LLC's Second Amended Complaint for Patent Infringement and Jury Demand," Case No. 6:09-cv-00148, filed August 11, 2009, 39 pages.	
<u> </u>	G027	"Plaintiff Acqis LLC's Answer to Defendant Appro International, Inc.'s Counterclaims," Case No. 6:09-00148-LED, filed August 28, 2009, 16 pages.	
	G028	"Defendant Clearcube Technology, Inc.'s Second Amended Answer Counterclaims to Acqis LLC's Second Amended Complaint for Patent Infringement and Jury Demand," Case No. 6:09-CV-00148, filed August 31, 2009, 45 pages.	

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Art Unit	2435		
Examiner Name	Hosuk Song		
Attorney Docket Number	ACQI-006/03US 310578-2053		

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Sheet 14

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	G029	"Plaintiff Acqis LLC's Answer to Defendant International Business Machines Corp.'s Counterclaims," Case No. 6:09-00148-LED, filed September 2, 2009, 11 pages.	
	G030	"Plaintiff Acqis LLC's Answer to Defendant Super Micro Computer, Inc.'s Counterclaims," Case No. 6:09-00148-LED, filed September 2, 2009, 15 pages.	
	G031	"Plaintiff Acqis LLC's Answer to Defendant Sun Microsystems, Inc.'s Counterclaims," Case No. 6:09-cv-00148-LED, filed September 2, 2009, 14 pages.	
	G032	"Plaintiff Acqis LLC's Answer to Defendant Dell Inc.'s Counterclaims," Case No. 6:09-00148- LED, filed September 2, 2009, 16 pages.	
	G033	"Plaintiff Acqis LLC's Answer to Defendant Fujitsu Computer Systems Corp., N/K/A Fujitsu America, Inc.'s Counterclaims," Case No. 6.09-00148-LED, filed September 16, 2009, 7 pages.	
	G034	"Plaintiff Acqis LLC's Answer to Defendant Hewlett-Packard Company's Counterclaims," Case No. 6:09-00148-LED, filed September 16, 2009, 14 pages.	
-	G035	"Plaintiff Acqis LLC's Answer to Defendant NEC Corporation of America's Counterclaims," Case No. 6:09-00148-LED, filed September 16, 2009, 8 pages.	
	G036	"Defendant Clearcube Technology, Inc.'s Third Amended Answer to Acqis LLC's Second Amended Complaint for Patent Infringement and Jury Demand," Case No. 6:09-cv-00148, filed November 11, 2009, 26 pages.	
	G037	"Defendant Clearcube Technology, Inc.'s Fourth Amended Answer to Acqis LLC's Second Amended Complaint for Patent Infringement and Jury Demand," Case No. 6:09-cv-00148, filed January 8, 2010, 26 pages.	
	G038	"Dell's First Amended Answer and Counterclaims to Plaintiff's Second Amended Complaint," Case No. 6:09-cv-00148-LED, filed April 22, 2010, 38 pages.	
	G039	"Plaintiff Acqis LLC's Answer to Defendant Dell Inc.'s First Amended Counterclaims," Case No. 6:09-00148-LED, filed May 10, 2010, 16 pages.	
	G040	"Affidavit of Timothy P. Cremen in Support of NEC Corporation of America's Opposition to Plaintiff's Motion to Dismiss and Strike," Case No. 6:09-cv-00148-LED, filed October 9, 2009, 4 pages.	,
	G041	"Comparison [by NEC] of Rejected Elements in Office Action and Elements of Exemplary Claims of Acqis's Patents," Case No. 6:09-cv-00148-LED, filed October 9, 2009, 7 pages.	
	G042	"Defendant NEC Corporation of America's Opposition to Plaintiff's Motion to Dismiss and Motion to Strike," Case No. 6:09-cv-00148-LED, filed October 9, 2010, 36 pages.	
	G043	"Motion to Dismiss Counterclaim Pursuant to Rule 12(b)(6) and Motion to Strike Affirmative Defense Pursuant to Rule 12(f)," Case 6:09-00148-LED, filed September 16, 2009, 18 pages.	

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	H01	"Transcript of Videotaped Deposition of William Mangione-Smith," taken by the Defendants in connection with Case No. 6:09-cv-148-LED in the U.S. District Court for the Eastern District of Texas, September 9, 2010, 192 pages.	
	H02	"Defendant Sun Microsystems, Inc.'s Responses and Objections to Plaintiff Acqis LLC's Second Set of Common Interrogatories," Case No. 6:09-cv-00148-LED, filed May 12, 2010, 9 pages.	
	H03	"Plaintiff Acqis LLP's Objections and Responses to Defendants' First Set of Interrogatories," Case No. 6:09-cv-00148-LED, filed August 5, 2010, 21 pages.	
	H04	"Plaintiff Acqis LLP's Objections and Responses to Defendants' Third Set of Interrogatories," Case No. 6:09-cv-00148-LED, filed August 5, 2010, 13 pages.	
	H05	"Plaintiff Acqis LLP's First Supplemental Objections and Responses to Defendants' Third Set of Interrogatories," Case No. 6:09-cv-00148-LED, filed August 5, 2010, 14 pages.	
	H06	"Declaration of Jennifer Chen in Support of Defendants' Motion for Leave to Amend Defendants' Invalidity Contentions," Case No. 6:09-cv-00148-LED, August 5, 2010, 3 pages.	
	H07	Excerpts of Transcript of "Videotaped Deposition of William W.Y. Chu," taken by the Defendants in connection with Case No. 6:09-cv-148-LED in the U.S. District Court for the Eastern District of Texas, June 7, 2010, 20 pages.	
,	H08	"Declaration of Monty McGraw in Support of Defendants' Motion for Leave to Amend Defendants' Invalidity Contentions," Case No. 6:09-cv-00148-LED, August 5, 2010, 3 pages.	
	101	"Plaintiff's Opening Brief Regarding Claim Construction," Case No. 6:09-cv-00148-LED, filed June 1, 2010, 35 pages.	
	102	"Declaration of Carolyn V. Juarez in Support of Plaintiff Acqis LLC's Opening Brief Regarding Claim Construction," Case No. 6:09-cv-00148-LED, filed June 1, 2010, 3 pages.	
	103	"Defendant's Brief in Response to Plaintiff's Opening Brief Regarding Claim Construction," Case No. 6:09-cv-00148-LED, filed June 15, 2010, 40 pages.	
	104	"Proposed Claim Construction Statement," Case No. Case No. 6:09-cv-00148-LED, filed June 15, 2010, 39 pages.	
	105	"Claim Chart for International Business Machines Corp.," Case No. 6:09-cv-00148-LED, filed June 15, 2010, 12 pages.	Ī
	106	"Acqis LLC's Disclosure of Proposed Terms and Claim Elements For Construction Pursuant to Patent Rule 4-1," Case No. 6:09-cv-00148-LED, filed March 5, 2010, 3 pages.	
	107	"Defendant's List of Proposed Terms and Claim Elements for Construction," Case No. 6:09- cv-00148-LED, filed March 5, 2010, 15 pages.	Γ
	108	"Defendant's Amended List of Proposed Terms and Claim Elements for Construction," Case No. 6:09-cv-00148-LED, filed March 31, 2010, 11 pages.	Γ

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Modular Notebook Computer

Field of the Invention

The present invention is in the area of portable computer systems, and is particularly relevant to portable computers known as notebook computers.

Background of the Invention

Notebook computers are popular among computer users who travel and need to take their work along. They are smaller and lighter than laptops, and are therefore more portable. The evolution to smaller and lighter portable computers, however, is not without problems. For one thing, smaller portable computers means less space for battery packs, which usually means shorter useful life between recharges. Another problem related to smaller size is a difficulty in providing versatility. Smaller size naturally means less space to provide a broad choice in peripheral devices and options.

Yet another problem is related to addresses and data byte size. State-of-the-art computers are capable of 32 bit addresses and 32 bit data words. A 32 bit computer, though, typically needs a bus structure with nearly 100 active signals, equating to high pin count and extensive device and component density. Such high density in a small computer creates many other problems, such as problems with heat dissipation. These are a few of the many problems in designing and developing notebook computers.

What is needed is a new design for a notebook computer based on a bus structure allowing 32-bit capability with a minimum pin count, utilizing, for example, multiplexing of address and data on a single 32 bit structure, and utilizing only state-of-the-art technology to minimize power (hence buffer) requirements, which also minimizes heat and equipment complexity and - 4

density problems. Modularity needs to be raised to a new level by making virtually all components modular and "plug-in", including CPUs, power packs, and all of the various known sorts of peripheral devices.

Summary of the Invention

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In an embodiment of the present invention a frame work for a modular computer is provided having a frame and enclosure for supporting and housing other elements and module bays for docking functional modules. The frame and enclosure supports a Notebus for address, power control, and data transmission between module bays, including a compressed bus architecture with data and address words sharing one set of parallel traces, and at least one power trace for transmitting electrical power. The framework also has an electrical power conversion unit for accepting electrical power from outside the framework, converting it to voltage and current levels needed by the module bays, and supplying the converted power to the power trace of the Notebus. In addition, there is a display screen and a keyboard for input and output, and each module bay has a receiving connector for receiving a mating connector on a function module and providing connection to the Notebus. In one embodiment the framework has a central spine housing a portion of the Notebus, and a plurality of module bays arranged to either side of the notebus. In this embodiment each module bay has a receiving connector, guides for guiding a function module into position, a latching device for holding the function module in the module bay with the mating connector engaged in the receiving connector, and an expulsion mechanism for expelling a function module upon initiation

by an operator.

A CPU module is provided according to an embodiment of the invention with a CPU mounted in a case configured 14

to guide into and dock in a module bay of the framework provided. A state translator resides in the CPU module, and is connected to translate between the states of the CPU and the states of the Notebus. In one embodiment the CPU module has on-board RAM for providing quick memory response without bus wait states.

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A modular computer according to the present invention has a framework as described above, plus a CPU function module docked in a module bay and connected to the Notebus. There are power modules provided according to embodiments of the invention for providing power, and more than one such power module may be used to provide extended operating time. There are also function modules provided for such as floppy disks, hard disk drives, LAN communication, additional RAM, modem communication, serial communication, and FAX transmission over phone lines.

The modularity of the present invention is unique in providing modular CPU coupling, which allows a user to upgrade the modular computer to a more powerful CPU, or to a CPU dedicated to, or especially designed for, a particular need. The modularity also allows a user to tailor the computer to provide longer (or shorter) time between recharges.

Brief Description of the Drawings

Fig. 1A is an isometric view of a modular notebook computer framework according to an embodiment of the present invention.

Fig. 1B is a view of the computer framework of Fig. 1A from one side from the vantage of line 1B-1B on Fig. 1A.

Fig. 2 is a sectioned plan view of the computer framework of Fig. 1A taken according to section line 2-2 of Fig. 1B.

Fig. 3 is an isometric illustration showing a

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function module according to the present invention associated with a docking bay of the framework of Fig. 1A.

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Fig. 4 is another view of a function module according to the present invention.
Fig. 5 is a block diagram of a compressed bus and connection to docking bays in a computer framework according to an embodiment of the present invention.
Fig. 6 is a block diagram of a CPU function module according to an embodiment of the present invention.
Fig. 7 is a block diagram of a power supply function module according to an embodiment of the present invention.
Fig. 7 is a block diagram of a power supply function module according to an embodiment of the present invention, with indication of connections to the internal bus structure and power conversion unit of the computer.
Fig. 8 is a block diagram of a floppy disk drive function module used in the invention.
Fig. 9 is a block diagram of a hard disk drive

module used in an embodiment of the invention. Fig. 10 is a block diagram of a "flash card" memory module according to an embodiment of the present invention.

Fig. 11 is a block diagram of a LAN module according to an embodiment of the present invention. Fig. 12 is a block diagram of a modem module according to an embodiment of the present invention. Fig. 13 is a block diagram of a FAX module according to an embodiment of the present invention. Fig. 14 is a block diagram of a data acquisition module according to an embodiment of the present invention.

Description of the Preferred Embodiments

General Description

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Fig. 1A is an isometric drawing of a notebook computer framework 11 according to the invention. Framework 11 comprises a back housing 13, a tilt-up flat panel display 15, shown closed, a keyboard 17, and a plurality of module bays for plugging in function modules. Back housing 13 includes a power unit for converting electrical input on a wide variety of standards to the form required by the computer. For example, there is a port (not shown) for connecting to a standard household outlet, rated at 120 V., 60 Hz, alternating current. The power unit will convert the input to outputs as needed by the computer bus and functional modules. There are also input ports for 6 V. DC, 12 V. DC, 9 V. DC, and others, and the power unit in one embodiment of the present invention is capable of recognizing the input characteristics by sampling, and switching to proper on-board circuitry to utilize the input.

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In the embodiment shown by Fig. 1A four module bays 19, 21, 23, and 25 are shown along one side of the framework. There are four more module bays along the other side of the framework opposite the module bays shown. There could be more or fewer module bays, but eight is convenient and a good balance between the need to stay small and simple, and to also have adequate versatility.

Fig. 1B is an end view of the notebook computer framework of Fig. 1 in the direction of arrows 1B-1B of Fig. 1A. Each of the module bays has a set of guide and positioning rails such as rails 27 and 29 in bay 19. The rails are to position and guide a function module inserted into the module bay. Each rail in a set has a detent such as detent 31 for latching a module when the module is fully inserted in the bay. Each bay also has a connector such as connector 33 in bay 19. The connectors are for coupling to a mating connector on a function module inserted in a bay. It will be apparent to a ϵ_{k}

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person with skill in the art that there are a number of equivalent ways guide rails, detents, and coupling may be accomplished.

Fig. 2 is a plan section view just above the module bays taken along section line 2-2 of Fig. 1B. Bays 19, 21, 23, and 25 are shown on one side of the section view, and bays 35, 37, 39, and 41 along the opposite side. A printed circuit board structure 57 is fastened in a substantially vertical position down the center of frame 59, and connectors 33, 43, 45, 47, 49, 51, 53, and 55 are connected to the printed circuit board structure and present their pin structure outward toward the respective bay areas. In the presently described embodiment the internal connectors are male connectors, but this is not a requirement of the invention.

As also shown in Fig. 1A, each module bay has a pair of opposed rails located vertically at about the midpoint of the height of the module bay. Rails 27 and 29 serve module bay 19, and similar rails are located in each of the other module bays.

Fig. 3 is an isometric view of a function module 61 according to the invention aligned with module bay 25 of framework 11. Module 61 includes guides 63 and 65 on opposite sides for engaging rails 67 and 69 when module 61 is inserted into bay 25. The module has two springloaded detent levers (lever 73 is shown) for engaging detents in guide rails 67 and 69 when the module is fully inserted. Detent 71 is shown in rail 67 in Fig. 3. Each module bay has a compression spring mechanism engaged by a function module as the module nears full insertion, so there is an outward force on the module when the detent levers engage the detents. Mechanism 75 (Fig. 2) is exemplary. To insert a module one aligns the guides in the module with the guide rails and pushes the module into the module bay until the detents engage. Button 79 on front face 77 of the module is for retracting the detent levers of the module, in which case

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the spring mechanism ejects the module, much as is the case with some floppy disk drives.

Fig. 4 is an isometric view of function module 61, showing back face 81 opposite front face 77. The back face includes a recessed female connector receptacle 83 in the preferred embodiment, for mating with male connectors positioned in each pod bay, such as connector 33 in Fig. 1B and Fig. 2. A second detent lever 74 is opposite lever 73 of Fig. 3.

In the embodiment described above, and in many other embodiments, the notebook computer framework of the present invention comprises a frame with module bays and connectors as described above for "plugging in" function modules, power supply units, and other peripheral devices. The framework also comprises display 15, keyboard 17, and an internal bus structure hereinafter termed the Notebus, which is described in additional detail below, in the section titled "Notebus Bus Structure".

The function modules, as represented by module 61 in Fig. 3 and Fig. 4, are provided in a wide variety of different models capable of a wide variety of different functions. For example, framework 11 has no "on-board" CPU, battery power, or system memory. These functions and all other functions are provided by different models of function modules which may be inserted in any one or a combination of the available module bays. Other kinds of function modules that may be inserted include floppy-disk drives, hard-disk drives, "flashcard" memory modules, LAN and modem adapters, Fax modules, specialty modules such as data acquisition modules adapted to specific equipment, and more. The function modules are also described in more detail in the section below titled "Function Modules".

Electronic Architecture

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Fig. 5 is a block diagram showing internal elements of Notebook computer framework 11, connected to show the electronic architecture of the notebook computer according to the invention. Power input and conversion unit 85 is housed in back housing 13 (Fig. 1) and has ports 87 for power inputs. Unit 85 senses the input conditions and selects appropriate circuitry to convert the input to the voltages needed to power the other elements of the system. Output from the conversion unit is to Notebus 89, which comprises paths for power as well as for digital information such as data and addresses. Because there are a wide variety of function modules, as indicated above and described in more detail below, there needs typically to be more than one power line in the Notebus. For example, the notebook computer of the invention comprises hard disk drive modules, and these modules are preferably provided without their own "on board" power source. The motor drive for the hard disk requires a different power (voltage and current) than does a CPU, for example, so there are parallel power lines of differing size and voltage level in the notebus. A typical Notebus will have, for example, a line for 24V DC, another for 12V DC, and yet another for 5V DC, as well as multiple ground lines.

Notebus 89 connects to a video display controller 91 including Video Random Access Memory (VRAM) which both powers and controls display 15, which in the preferred embodiment is a flat panel display driven by analog driver lines on analog bus 93. Notebus 89 also connects to a keyboard controller 95 which powers and controls keyboard 17 over link 97, accepting keystroke input and converting the input to digital data for transmission on Notebus 89. The keyboard controller may be physically mounted in the keyboard or in framework 11. Notebus 89 also connects as illustrated in Fig. 5 to each of the module bays, such as bay 19, through connectors, such as connector 33. When a function . .

module, such as module 61, is inserted into a module bay, the mating connector in the back of the function module mates with the connector from the Notebus, and circuitry inside the function module is then connected to the Notebus.

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Notebus Bus Structure

The Notebus comprises, as stated above, both power and data paths. The digital lines are capable of carrying 32 addresses and conveying data in 32 bit word length. To minimize pin count and routing complexity, addresses and data are multiplexed on a single set of 32 traces in the overall bus structure. One with skill in the art will recognize that this type of bus is what is known in the art as a low-pin-count or compressed bus. In this kind of bus different types of signals, such as address and data signals, share signal paths through multiplexing. For example, the same set of data lines are used to carry both 32-bit addresses and data words of 32-bit length.

In the Notebus of the present invention, some control signals, such as interrupt arbitration signals, may also share the data lines. Typical examples of buses that are exemplary as usable for the Notebus (with the exception of power supply analog lines in the Notebus) are the "S-Bus" implemented by Sun Microsystems, the "Turbochannel" Bus from Digital Equipment Corporation, and buses compatible with the IEEE-488 standard. The Notebus is a high-speed backplane bus for interconnecting processor, memory and peripheral device modules. The Notebus also supplies standard operating and standby power supply voltages and electrical ground to all module bays.

Function Modules

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Fig. 3 and Fig. 4 show, as described above, two different views of a function module according to the present invention. Also as stated above, function modules may have many different functions. There are as many different functions, in fact, as there are possibilities for discrete peripheral devices, plus power and CPU modules. An individual function module is provided for each function, and in each case the function module has a physical size and form compatible with the bays, guide rails, and connectors for "plugging in" to framework 11.

The "face" of a function module, being the exposed face when the module is "plugged in" (see face 77 in Fig. 3) may have elements specific to the type of module. For example, a CPU module may have no indicators or other elements on the front face, while a floppy disc module will typically have an opening for inserting a floppy disk and a "key" or button for releasing and ejecting the floppy disk.

A unique feature of the present invention is that the CPU for the notebook computer is provided as a CPU function module. This provides an ability for a user to tailor the CPU power to the other modules and application for the notebook computer, and an easy upgrade to more powerful CPUs.

Fig. 6 is a diagram of a CPU module 99 plugged into a bay in a notebook computer according to the present invention. In this case (referring to Fig. 2) the module is plugged into bay 19 having connector 33. This is exemplary, as the module could just as well be plugged into any open bay of framework 11. By virtue of being plugged into connector 33 or another module connector, internal elements of the CPU module are connected to Notebus 89.

The internal elements for module 99 comprise CPU 103, a state translator 105, and RAM memory 113. CPU 103 may be any of a wide variety of CPUs (also called in some • 6

11 cases MPUs) available in the art, for example Intel 80386 or 80486 models, MIPS, RISC implementations, and many others. CPU 103 communicates with State Translator 105 over paths 107, and State Translator 105 communicates with connector 33, hence Notebus 89, over bus 109 internal to the module, which is an extension of bus 89 when the module is plugged into bus 89. State translator 105 is a chip or chip set designed to translate commands and requests of the CPU to commands and requests compatible with the Notebus. It was mentioned above that CPU 103 may be one of a wide variety of CPUs, and that Notebus 89 may be any one of a wide variety of compressed buses. It will be apparent to one with skill in the art that there may be an even wider variety of state translators 105 for translating between the CPU and the Notebus. The state translessor is theoretically a different device for each possible combination of CPU and Notebus. RAM memory module 113 comprises conventional RAM chips mounted on a PCB as is known in the art, and connectable to state translator 105 by a plug or connector interface, such as an edge connector. The purpose of having a RAM module "on board" the CPU module is to provide for rapid memory access, which will be much slower if the RAM is made available in a separate module at one of the other module bays. Memory at another module bay is on the Notebus, and will be subject to bus contention and wait states. The plug-in nature of the RAM unit relative to the CPU module allows different amounts of memory to be provided with a CPU module in the notebook computer of the present invention. As described above, Notebus 89 comprises not only the shared data and address lines, but also power and ground connections for the modules plugged into the various bays. Paths 109 and 107 therefore comprise power and ground lines for CPU 103 and Translator 105. If, for example, CPU 103 is an INTEL 80486

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- 12 microprocessor, State Translator 105 will be a translator for accommodating the state machine of the 80486 to the state machine of the Notebus, which may be any one of the buses described above for bus 89, or another compressed bus. There are many equivalent ways a translator may be implemented for the specific case. Given the manufacturers available design information for the CPU and the equivalent information for bus 89, it is within the skill of workers in the art without undue experimentation to implement the translator and the required connections. This is conventional technology. The implementation of the translator on a module with a CPU to plug into a module bay in the notebook computer is unique to the present invention. In the invention, state translators may be implemented in a single chip set or circuitry set to be capable of translating between a number of CPUs and a number of different bus possibilities. One might, for example, design and implement a translator with the necessary circuitry and intelligence to translate between three different CPUs and three different compressed buses. The state translator could be made hardware or software programmable to select one CPU and one bus from the available selections at some convenient time in the manufacturing cycle, or even at the time of selection of modules to make up a notebook computer. As an example of a hardware programmable translator, a translator could be built to have certain traces cut as a near final step in manufacture as a way

traces cut as a near final step in manufacture as a way of selecting the CPU and bus pair. Translators could also be programmable by virtue of on-board EPROM or EEPROM devices. As an example of software programmability, translators could be implemented with microprocessor technology and software programmable. A CPU module could be plugged into a connector on a special programming unit, for example, before installation in a notebook computer according to the present invention, and ۰.

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be sent certain commands to set up on board software to translate between the desired CPU and bus. It will be apparent to one with skill in the art that there are many possible variations in the implementation of the translators.

Fig. 7 shows a power module 111 plugged into a bay in the notebook computer according to an embodiment of the present invention. The purpose of a power module is to provide a source of power for the computer, which includes any modules plugged into the module bays. As is common in notebook computers in the art, there may be a battery, typically rechargeable, in framework 11, and the battery may also be replaceable and rechargeable through power input lines 87. In the case of an on-board battery pack, there is the option of using all module bays for other than power packs.

Preferably framework 11, sans function modules, has no power capability other than power plugged into one of input lines 87, which may be converted to the power characteristics needed by the computer and distributed on the power lines of the Notebus. For portability, power is typically supplied by one (or more) power modules 111 plugged into one or more of the module bays. Module 111 has a battery pack 101 which is connected via lines 117 to (in this case for example) connector 33, and hence to Notebus 89. Because there are several supply lines in the Notebus for supplying power to function modules at different voltage and with different current capability, the power lines in the Notebus for connecting a power module 111 are not the same as the lines for supplying power to a module. There is instead a separate sat of power lines to pins on the module bay connectors, such as connector 33, which connect as input to power input and conversion unit 85, much as do input ports 87. In Fig. 7, lines 119 and 121 connect power module

11 to conversion unit 85, where the power input from the

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power module is sensed and treated as a power source, much as is done for power input lines 87. This power is converted to the needed voltages and current capabilities, and put back out on the power supply output lines to the module bays. In Fig. 7 line 119 is ground, and arrow 123 represents all of the data/address, control, and power output lines to the module bays. Lines represented by arrow 123, plus lines 119 and 121 are Notebus 89. Although not shown in Fig. 7, there are connections for line 119 and for line 121 to each of the module bay connectors.

Power modules such as module 111 may be plugged into a connector on a charging module separate from the notebook computer, using the same connector used for plugging into the Notebus via a module bay of framework 11, and recharged for later use with a modular notebook computer according to the invention. This allows a user to keep spare power modules ready for use, and to recharge modules without connecting the computer itself to a charging unit. Moreover, the provision of power modules allows a user to provide more or less portable time to the notebook computer by using one or more than one power module.

Fig. 8 shows a floppy disk drive (FDD) module 125 plugged into a module bay in a notebook computer according to an embodiment of the present invention. Module 125 comprises a conventional FDD unit 129 for nominal 3.5 inch disks with conventional circuitry mounted in a case 130 to provide a module with guides, latches, and a connector matable with connector 35 to be able to plug into a module bay in the notebook computer of the present invention. The case comprises an opening 131 for inserting and withdrawing a floppy disk, and an eject button 133 for ejecting a floppy disk. A controller 127 communicates with unit 129 over lines 126 and with connector 33 (hence Notebus 89) over lines 128. The unit also derives power from the

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appropriate pins on connector 33, but these pins and lines are not shown. Controller 127 is an ASIC chip or chip set for translating between the notebus and the FDD unit. Given the data storage standards of the FDD unit and the characteristics of bus 89, it is within the scope of workers with ordinary skill in the art to implement controller 127 without undo experimentation. Fig. 9 shows a hard disk drive (HDD) module 135 according to an embodiment of the present invention plugged into bus 89 in a module bay of framework 11. HDD module 135 comprises a conventional HDD unit 139 mounted in a case 137 to be compatible with plugging into a notebook computer according to the present invention. As in the case of the FDD module described above, a controller 141 is provided to translate between Notebus 89 and the HDD unit. Controller 141 communicates with HDD unit 139 over lines 143, and with connector 33 over lines 145. Connector 33 is exemplary of any one of the module connectors in the notebook computer. Given the characteristics of HDD unit 139 and of Notebus 89, it is within the skill of workers in the art to implement controller 141 without undue experimentation. Power line connections are not shown. In implementing controller 141 there are several protocols that may be used. One is the ST506 standard known in the art. Another is the IDE standard known in the art. Yet another is an enhanced IDE, called EIDE, known to the inventors, and the subject of a separate patent application to be filed. In the EIDE protocol, there may be multiple IDE devices daisy-chained and addressed as secondary IDE devices with an additional select number.

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Fig. 10 shows a "flash card" memory module 147 plugged into connector 33 of the notebook computer of the invention. "Flash-cards" are RAM memory cards known in the art pluggable into typically parallel ports o make connection with internal bus structures of a computer. ٠ż

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Module 147 comprises a conventional "flash card" 151 mounted in a case 149 compatible with the module bay of a notebook computer according to the present invention. As in cases described above, a controller 153 is needed to accomplish communication between the memory structure of the "flash card" and bus 89. Controller 153 communicates with "flash card" unit 151 over lines 155 and with connector 33 over lines 157. There may optionally be an opening 159 in case 149 and a connector (not shown) within unit 151 for inserting and withdrawing flash cards, so relatively large collections of data may be plugged in as desired. Alternatively the interface may be the modular interface afforded by the plug-in module 147. Again, given the known characteristics of the flash card and of bus 89, implementation of the controller is a matter within the skill of workers in the art.

Fig. 11 shows a LAN module 161 plugged into connector 33 of a notebook computer according to an embodiment of the present invention. In the embodiment shown in Fig. 11 a conventional LAN card, such as an Ethernet card, is mounted in a case 163 to be compatible with plugging into a module bay of a notebook computer according to an embodiment of the present invention. LAN card 167 communicates with a conventional connector 165 in the face of the case of module 161 that is exposed when the module is plugged into a bay. This is a conventional connector of the sort known in the art for connecting computers on a network.

Within module 161, in a first alternative, conventional LAN card 167 interfaces to a controller 169 communicating over lines 171 and 173, and the controller translates between bus 89 and the conventional LAN card. In a second alternative, a LAN card is provided with the translation built-in, so no separate controller is needed. The first alternative is preferable. Fig. 12 shows a modem module 175 plugged into • 4

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connector 33 in a bay of a notebook computer according to an embodiment of the present invention. Modem module 175 comprises a conventional modem card 181 mounted in a case 177 to be compatible with plugging into a module bay. In this case, and other cases above, where the term "conventional" is used in conjunction with a card or unit, it is meant that the circuitry and function is conventional. The size may be adjusted to be compatible with a module case for plugging into a bay of a notebook computer according to the present invention. Modem card 181 connects over lines 183 to a telephone interface 179, which may comprise more than one "jack" so a hand set may also be connected. Card 181 communicates to Notebus 89 over lines 187 and 189 through controller 185, which translates between the conventional card and the compressed bus. Alternatively, the translation components may he implemented on a single card along with the modem circuitry. Fig. 13 shows a FAX module 191 plugged into connector 33 of a module bay in an embodiment of the present invention. Module 191 comprises a conventional FAX card 199 mounted in a case 193 to be compatible with plugging into a module bay in the present invention. Fax card 199 communicates over lines 197 with a telephone interface 195, which may, as in the case of the modem module described above, have more than a single telephone "jack".

A controller 201 provides an interface for the conventional FAX card between the card and Notebus 89 over lines 203 and 205. Alternatively, the controller may be implemented on the same card as the FAX circuitry. In yet another alternative, the FAX capability and the modem capability described above may be implemented into a single module.

Fig. 14 shows a specialty data acquisition module 207 plugged into connector 33 in a module bay in a notebook computer according to an embodiment of the - 1

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present invention. Module 207 comprises a circuit card 215 mounted in a case 209 to be compatible with plugging into a module bay. Card 215 communicates over lines 213 to an interface 211 which may comprise one or several acquisition leads for connecting to outside equipment. For example, a data module may be provided for following the output of the vertical and horizontal sweep of an oscilloscope, and would have at least two input leads; one for the vertical and one for the horizontal sweep. Card 215 communicates over lines 217 to connector 33, hence Notebus 89. The circuitry on card 215 is designed to digitize the input if the input is analog, and to be compatible with Notebus 89. Given the characteristics of signals to be measured and the characteristics of Notebus 89, implementation of such a card is within the ordinary skill in the art. There are, in addition to the modules described herein, other modules that may be designed and built to extend the utility of the modular notebook computer of the present invention.

It will be evident to one with skill in the art that there are many changes that might be made without departing from spirit and scope of the present invention. Many of these alternatives have been described above. For example, there may be more than the eight module bays described, or fewer. Similarly, there are many ways modules may be built to be pluggable into a framework such as framework 11. There are similarly many different kinds of connectors that might be utilized. There are many kinds of compressed buses that can be used, and many kinds of modules that may be provided, and many other changes that might be made within the spirit and scope of the invention. What is claimed is:

1. A framework for a modular computer comprising: frame and enclosure means for supporting and housing elements of the framework, said frame and enclosure means having module bays for docking functional modules;

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notebus means for address, power, control, and data transmission between module bays, said notebus means including a compressed bus architecture wherein data and address words share one set of parallel traces, and at least one power trace for transmitting electrical power; electrical power conversion means for accepting electrical power from outside said framework, converting said outside electrical power to voltage and current levels needed by said module bays, and supplying said electrical power to said at least one power trace in said notebus means;

display means connected to said notebus means for displaying text and graphical information; and keyboard means connected to said notebus means for a user to input text and commands to said notebus; each said module bay having a receiving connector for receiving a mating connector on a function module and providing connection to said notebus means.

2. A framework as in claim 1 wherein said frame and enclosure means has a central spine housing a portion of said notebus, and a plurality of module bays arranged to each side of said central spine, each of said module bays having guide means for accepting and guiding a module into said module bay, a latching means for holding said module when received with said mating connector engaged in said receiving connector, and expulsion means operable by a user for expelling a module from said module bay.

3. A CPU module for plugging into a module bay of a

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framework for a modular computer, said module bay having a receiving connector with pins connected to individual traces of a bus means within said framework, said CPU module comprising:

a casing for supporting and housing elements of said CPU module;

guide means for engaging guides in said module bay and guiding said CPU module into and out of said module bay when engaging and disengaging;

mating connector means for engaging said receiving connector to connect traces within said module to said bus;

CPU means mounted within said casing of said CPU module;

state translator means connected to said module connector and to said CPU means for translating signals between said bus and said CPU means.

4. A CPU module as in claim 3 further comprising RAM memory means connected to said state translator means, said RAM memory means for providing RAM memory with minimum access time to said CPU means.

5. A modular computer comprising:

frame and enclosure means for supporting and housing elements of the modular computer, said frame and enclosure means having module bays for docking functional modules;

notebus means for address, power, control, and data transmission between module bays, said notebus means including a compressed bus architecture wherein data and address words share one set of parallel traces, at least one power trace for transmitting electrical power to module bays, and connecting to a receiving connector in each of said module bays;

electrical power conversion means for accepting electrical power from outside said framework, converting · i

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said outside electrical power to voltage and current levels needed by said module bays, and supplying said electrical power to said at least one power trace in said notebus means;

display means connected to said notebus means for displaying text and graphical information; keyboard means connected to said notebus means for a user to input text and commands to said notebus; and a CPU module docked in one of said module bays, said CPU module having module connector means engaging said receiving connector, connecting traces within said module to said bus, CPU means mounted within said CPU module, and state translator means connected to said module connector and to said CPU means for translating signals between said bus and said CPU means.

6. A power module for plugging into a module bay of a framework for a modular computer, said module bay having a receiving connector with pins connected to individual traces of a bus means within said framework, said power module comprising:

a casing for supporting and housing elements of said power module;

guide means for engaging guides in said module bay and guiding said power module into and out of said module bay when engaging and disengaging;

module connector means for engaging said receiving connector to connect traces within said power module to said bus means; and

electrical power storage means mounted within said power module for supplying electrical power to said modular computer.

7. An I/O function module for plugging into a module bay of a framework for a modular computer, said module bay having a receiving connector with pins connected to individual traces of a bus means within said framework, . ŝ

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said function module comprising:

a casing for supporting and housing elements of said function module;

guide means for engaging guides in said module bay and guiding said function module into and out of said module bay;

module connector means for engaging said receiving connector to connect traces within said function module to said bus means; and

I/O function means mounted within said function module for performing an I/O function for said modular computer, said I/O function means connected to said bus through said module connector means.

8. An I/O function module as in claim 7 wherein said module is a floppy disk module having a port for inserting and ejecting a floppy disk, said port accessible with said floppy disk module engaged in said module bay, reading and writing means, and a disk controller configured to operate said floppy disk module from said bus means

9. An I/O function module as in claim 7 wherein said module is a hard disk module, having at least one hard disk, reading and writing means, and a disk controller configured to operate said hard disk module from said bus means.

10. An I/O function module as in claim 7 wherein said module is a RAM memory module, having RAM memory connectable to and accessible by said bus means with said RAM memory module plugged into said module bay.

11. An I/O function module as in claim 7 wherein said module is a LAN module for providing communication between said modular computer and other computer systems on a local area network. • 1

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12. An I/O function module as in claim 7 wherein said module is a modem module for providing communication between said modular computer and other computer systems over a telephone connection.

13. An I/O function module as in claim 7 wherein said module is a serial communication module for providing communication between said modular computer and other computer systems over a serial link.

14. An I/O function module as in claim 7 wherein said module is a facsimile module for providing FAX transmission and reception over telephone lines.

15. An I/O module as in claim 7 wherein said module is a specialty module for data acquisition from an instrument, said function module capable of transmitting commands to the instrument over a communication link, receiving data from the instrument, and translating data for transmission on said bus means.

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Fig. 4

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Fig. 5
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Fig. 6



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Fig. 8

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Fig. 10

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Fig. 13

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INTERNATIONAL SEARCH REPORT

International application No. PCT/US93/06146

A. CLASSIFICATION OF SUBJECT MATTER
IPC(5) ::H05K 7/10; G06F 1/16
US CL :361/395
According to International Patent Classification (IPC) or to both national classification and IPC
B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)

U.S. : 361/380, 390, 391, 392, 393, 394, 399, 415; 364/708

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Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)

C. DOC	UMENTS CONSIDERED TO BE RELEVANT		
Category*	Citation of document, with indication, where a	ppropriate, of the relevant passage	Relevant to claim No.
Y	US, A, 4,894,792 (Mitchell et al) See the entire document.	16 January 1990	1-15
Y	US, A, 4,991,058 (Watkins et all the entire document.	05 February 1991, S	See 2
Y	EP, A, 0,387,749 (Skordou et al) the entire document.	19 September 1990, S	See 2
Y	US, A, 4,680,674 (Moore) 14 Jul See the entire document.	y 1987	2-6
X Furth	er documents are listed in the continuation of Box C	. See patent family ann	EX.
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	INTERNATIONAL SEARCH REPORT	International ap PCT/US93/061	
C (Continua	tion). DOCUMENTS CONSIDERED TO BE RELEVANT		
Category*	Citation of document, with indication, where appropriate, of the relev	Relevant to claim No.	
Y	US, A, 4,941,841 (Darden et al) 17 July 1990, See the entire document.	n <u></u>	2-15
Y.	BYTE, June 1983, pages 150-154, 156, 159, 160, 162 Wayne Clingingsmith, "A Machine for All Processors"		1-15
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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

PLEASE DATE STAMP TO SHOW RECEIPT OF THE BELOW:

In re Application of: William W.Y. Chu Appl. No.: 12/561,138 Filed: September 16, 2009 Art Unit: 2435 Confirmation No.: 1717 Examiner: Song, Hosuk

FOR: DATA SECURITY METHOD AND DEVICE FOR COMPUTER MODULES

1. Information Disclosure Statement (IDS), PTO/SB/08 (16 pgs) (foreign reference and literature references attached)

Date Filed: June 20, 2011

Attorney Docket No.: ACQI-006/03US 310578-2053

Atty/Secy: WEB/mlm

Sorney Docket No. ACQI-006/03US 310578-2053

PATENT

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Ap	oplication of:	William W.Y. Chu	Confirmation No.:	1717
Serial N	lo.:	12/561,138	Group Art Unit:	2435
Filed:		September 16, 2009	Examiner:	Song, Hosuk
For:	DATA SECUR	RITY METHOD AND DE	EVICE FOR COMPU	TER MODULES

Mail Stop Amendment Commissioner for Patents P.O. Box 1450 Alexandria, VA 22313-1450

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INFORMATION DISCLOSURE STATEMENT UNDER 37 C.F.R. §1.97(c)

In accordance with the duty of disclosure set forth in 37 C.F.R. §1.56, Applicant(s)

hereby submits the following information in conformance with 37 C.F.R. §§1.97 and 1.98.

- Pursuant to 37 C.F.R. §1.98, a copy of each non-US patent document cited in the attached Form PTO/SB/08 is enclosed.
- No copies of the publications listed on the attached Form PTO/SB/08 are being provided pursuant to 37 C.F.R. §1.98(d) because the publications were previously cited by or submitted to the Office in prior Application Serial No. _____ to which the above-identified application claims priority under 35 U.S.C. §120.
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- Enclosed is an explanation of non-English publication(s) _____ for which an English translation is not available.

Attorney Docket No. ACQI-006/03US 310578-2053 Serial No. 12/561,138 Page 2

- Enclosed is an English translation of non-English publication(s) _____ cited in the attached Form PTO/SB/08.
- Enclosed is a copy of pending patent Application Serial No.

This Information Disclosure Statement is filed within any one of the following time periods:

- [] within three months from the filing date of this national application other than a CPA under 37 C.F.R. § 1.53(d);
- [] within three months from the date of entry of the national stage as set forth in 37 C.F.R. §1.491 in this international application;
- [] before the mailing date of a first office action on the merits; or
- [x] before the mailing of a first office action after the filing of a request for continued examination under 37 C.F.R. § 1.114.

It is respectfully requested that the Examiner consider the above-noted information and return an initialed copy of the attached Form PTO/SB/08 to the undersigned.

Date: June 20, 2011

Customer No. 58249 COOLEY LLP 777 6th Street NW, Suite 1100 Washington, DC 20001

Tel: (650) 843-5852 Fax: (202) 842-7899

1.

Respectfully submitted, COOLEY LLP

By:

William E. Brow, Reg. No. 64209 for Cliff Z. Liu, Reg. No. 50,834



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EXAMINER SONG, HOSUK PAPER NUMBER ART UNIT

2435

DATE MAILED: 08/04/2011

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
12/561,138	09/16/2009	William W.Y. Chu	ACQI-006/03US	1717
TITLE OF INVENTION: D	ATA SECURITY METHOI) AND DEVICE FOR COMPLITER MODULES	310578-2053	

08/04/2011

APPLN. TYPE	SMALL ENTITY	ISSUE FEE DUE	PUBLICATION FEE DUE	PREV. PAID ISSUE FEE	TOTAL FEE(S) DUE	DATE DUE
nonprovisional	YES	\$755	\$0	\$0	\$755	11/04/2011

THE APPLICATION IDENTIFIED ABOVE HAS BEEN EXAMINED AND IS ALLOWED FOR ISSUANCE AS A PATENT. <u>PROSECUTION ON THE MERITS IS CLOSED</u>. THIS NOTICE OF ALLOWANCE IS NOT A GRANT OF PATENT RIGHTS. THIS APPLICATION IS SUBJECT TO WITHDRAWAL FROM ISSUE AT THE INITIATIVE OF THE OFFICE OR UPON PETITION BY THE APPLICANT. SEE 37 CFR 1.313 AND MPEP 1308.

THE ISSUE FEE AND PUBLICATION FEE (IF REQUIRED) MUST BE PAID WITHIN THREE MONTHS FROM THE MAILING DATE OF THIS NOTICE OR THIS APPLICATION SHALL BE REGARDED AS ABANDONED. THIS STATUTORY PERIOD CANNOT BE EXTENDED. SEE 35 U.S.C. 151. THE ISSUE FEE DUE INDICATED ABOVE DOES NOT REFLECT A CREDIT FOR ANY PREVIOUSLY PAID ISSUE FEE IN THIS APPLICATION. IF AN ISSUE FEE HAS PREVIOUSLY BEEN PAID IN THIS APPLICATION (AS SHOWN ABOVE), THE RETURN OF PART B OF THIS FORM WILL BE CONSIDERED A REQUEST TO REAPPLY THE PREVIOUSLY PAID ISSUE FEE TOWARD THE ISSUE FEE NOW DUE.

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I. Review the SMALL ENTITY status shown above.

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A. If the status is the same, pay the TOTAL FEE(S) DUE shown above.	A. Pay TOTAL FEE(S) DUE shown above, or
B. If the status above is to be removed, check box 5b on Part B - Fee(s) Transmittal and pay the PUBLICATION FEE (if required) and twice the amount of the ISSUE FEE shown above, or	B. If applicant claimed SMALL ENTITY status before, or is now claiming SMALL ENTITY status, check box 5a on Part B - Fee(s) Transmittal and pay the PUBLICATION FEE (if required) and 1/2 the ISSUE FEE shown above.

II. PART B - FEE(S) TRANSMITTAL, or its equivalent, must be completed and returned to the United States Patent and Trademark Office (USPTO) with your ISSUE FEE and PUBLICATION FEE (if required). If you are charging the fee(s) to your deposit account, section "4b" of Part B - Fee(s) Transmittal should be completed and an extra copy of the form should be submitted. If an equivalent of Part B is filed, a request to reapply a previously paid issue fee must be clearly made, and delays in processing may occur due to the difficulty in recognizing the paper as an equivalent of Part B.

III. All communications regarding this application must give the application number. Please direct all communications prior to issuance to Mail Stop ISSUE FEE unless advised to the contrary.

IMPORTANT REMINDER: Utility patents issuing on applications filed on or after Dec. 12, 1980 may require payment of maintenance fees. It is patentee's responsibility to ensure timely payment of maintenance fees when due.

PART B - FEE(S) TRANSMITTAL

Complete and send this form, together with applicable fee(s), to: <u>Mail</u> Mail Stop ISSUE FEE Commissioner for Patents P O Box 1450

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or <u>Fax</u> (571)-273-2885

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⁵⁸²⁴⁹ COOLEY LLP ATTN: Patent Gr Suite 1100 777 - 6th Street, 1	NW		ny change of address)		Fee(s paper have	3) Transmittal. Thi rs. Each additional its own certificate Cert	s certif paper of mai paper	icate cannot be used fo , such as an assignmen ling or transmission.	deposited with the United class mail in an envelope above, or being facsimile e indicated below.
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12/561,138 TITLE OF INVENTION:	09/16/2009 DATA SECURITY ME	ETHOD	AND DEVICE F	William W.Y. Ch OR COMPUTER M		ES		CQI-006/03US 310578-2053	1717
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		NT AND TRADEMARK OFFICE	UNITED STATES DEPAR United States Patent and T Address: COMMISSIONER FC P.O. Box 1450 Alexandria, Virginia 223 www.uspto.gov	Frademark Office OR PATENTS
APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
12/561,138	09/16/2009	William W.Y. Chu	ACQI-006/03US 310578-2053	1717
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COOLEY LLP ATTN: Patent Gro	110		SONG, I	HOSUK
Suite 1100	чр		ART UNIT	PAPER NUMBER
777 - 6th Street, N			2435	
WASHINGTON, I	DC 20001		DATE MAILED: 08/04/201	1

Determination of Patent Term Extension or Adjustment under 35 U.S.C. 154 (b)

A reissue patent is for "the unexpired part of the term of the original patent." See 35 U.S.C. 251. Accordingly, the above-identified reissue application is not eligible for Patent Term Extension or Adjustment under 35 U.S.C. 154(b).

Any questions regarding the Patent Term Extension or Adjustment determination should be directed to the Office of Patent Legal Administration at (571)-272-7702. Questions relating to issue and publication fee payments should be directed to the Customer Service Center of the Office of Patent Publication at 1-(888)-786-0101 or (571)-272-4200.

Privacy Act Statement

The Privacy Act of 1974 (P.L. 93-579) requires that you be given certain information in connection with your submission of the attached form related to a patent application or patent. Accordingly, pursuant to the requirements of the Act, please be advised that: (1) the general authority for the collection of this information is 35 U.S.C. 2(b)(2); (2) furnishing of the information solicited is voluntary; and (3) the principal purpose for which the information is used by the U.S. Patent and Trademark Office is to process and/or examine your submission related to a patent application or patent. If you do not furnish the requested information, the U.S. Patent and Trademark Office may not be able to process and/or examine your submission, which may result in termination of proceedings or abandonment of the application or expiration of the patent.

The information provided by you in this form will be subject to the following routine uses:

- 1. The information on this form will be treated confidentially to the extent allowed under the Freedom of Information Act (5 U.S.C. 552) and the Privacy Act (5 U.S.C 552a). Records from this system of records may be disclosed to the Department of Justice to determine whether disclosure of these records is required by the Freedom of Information Act.
- 2. A record from this system of records may be disclosed, as a routine use, in the course of presenting evidence to a court, magistrate, or administrative tribunal, including disclosures to opposing counsel in the course of settlement negotiations.
- 3. A record in this system of records may be disclosed, as a routine use, to a Member of Congress submitting a request involving an individual, to whom the record pertains, when the individual has requested assistance from the Member with respect to the subject matter of the record.
- 4. A record in this system of records may be disclosed, as a routine use, to a contractor of the Agency having need for the information in order to perform a contract. Recipients of information shall be required to comply with the requirements of the Privacy Act of 1974, as amended, pursuant to 5 U.S.C. 552a(m).
- 5. A record related to an International Application filed under the Patent Cooperation Treaty in this system of records may be disclosed, as a routine use, to the International Bureau of the World Intellectual Property Organization, pursuant to the Patent Cooperation Treaty.
- 6. A record in this system of records may be disclosed, as a routine use, to another federal agency for purposes of National Security review (35 U.S.C. 181) and for review pursuant to the Atomic Energy Act (42 U.S.C. 218(c)).
- 7. A record from this system of records may be disclosed, as a routine use, to the Administrator, General Services, or his/her designee, during an inspection of records conducted by GSA as part of that agency's responsibility to recommend improvements in records management practices and programs, under authority of 44 U.S.C. 2904 and 2906. Such disclosure shall be made in accordance with the GSA regulations governing inspection of records for this purpose, and any other relevant (i.e., GSA or Commerce) directive. Such disclosure shall not be used to make determinations about individuals.
- 8. A record from this system of records may be disclosed, as a routine use, to the public after either publication of the application pursuant to 35 U.S.C. 122(b) or issuance of a patent pursuant to 35 U.S.C. 151. Further, a record may be disclosed, subject to the limitations of 37 CFR 1.14, as a routine use, to the public if the record was filed in an application which became abandoned or in which the proceedings were terminated and which application is referenced by either a published application, an application open to public inspection or an issued patent.
- 9. A record from this system of records may be disclosed, as a routine use, to a Federal, State, or local law enforcement agency, if the USPTO becomes aware of a violation or potential violation of law or regulation.

	Application No.	Applicant(s)					
	12/561,138	CHU, WILLIAM W.Y.					
Notice of Allowability	Examiner	Art Unit					
	HOSUK SONG	2435					
The MAILING DATE of this communication appears on the cover sheet with the correspondence address All claims being allowable, PROSECUTION ON THE MERITS IS (OR REMAINS) CLOSED in this application. If not included herewith (or previously mailed), a Notice of Allowance (PTOL-85) or other appropriate communication will be mailed in due course. THIS NOTICE OF ALLOWABILITY IS NOT A GRANT OF PATENT RIGHTS. This application is subject to withdrawal from issue at the initiative of the Office or upon petition by the applicant. See 37 CFR 1.313 and MPEP 1308.							
1. This communication is responsive to <u>RCE filed on 6/17/11</u>	<u>l.</u>						
2. X The allowed claim(s) is/are <u>14-95</u> .							
 3. Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f). a) All b) Some* c) None of the: 1. Certified copies of the priority documents have been received. 2. Certified copies of the priority documents have been received in Application No. 							
3. Copies of the certified copies of the priority do							
International Bureau (PCT Rule 17.2(a)).		.					
* Certified copies not received:							
Applicant has THREE MONTHS FROM THE "MAILING DATE" noted below. Failure to timely comply will result in ABANDON THIS THREE-MONTH PERIOD IS NOT EXTENDABLE.		eply complying with the requirements					
	4. A SUBSTITUTE OATH OR DECLARATION must be submitted. Note the attached EXAMINER'S AMENDMENT or NOTICE OF INFORMAL PATENT APPLICATION (PTO-152) which gives reason(s) why the oath or declaration is deficient.						
5. CORRECTED DRAWINGS (as "replacement sheets") mu	st be submitted.						
(a) including changes required by the Notice of Draftsper	son's Patent Drawing Review(I	PTO-948) attached					
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(b) ☐ including changes required by the attached Examiner Paper No./Mail Date	's Amendment / Comment or in	the Office action of					
Identifying indicia such as the application number (see 37 CFR a each sheet. Replacement sheet(s) should be labeled as such in							
6. DEPOSIT OF and/or INFORMATION about the depo attached Examiner's comment regarding REQUIREMENT							
Attachment(s) 1. Notice of References Cited (PTO-892)	5. Notice of Inform	nal Patent Application					
2. Notice of Draftperson's Patent Drawing Review (PTO-948)	6. 🔲 Interview Sumi	nary (PTO-413),					
3. Information Disclosure Statements (PTO/SB/08),	7. 🗌 Examiner's Am	il Date endment/Comment					
Paper No./Mail Date <u>6/20/11</u> 4. Examiner's Comment Regarding Requirement for Deposit of Biological Material	8. 🛛 Examiner's Sta	tement of Reasons for Allowance					
	9. 🗌 Other						
/HOSUK SONG/ Primary Examiner, Art Unit 2435							
U.S. Patent and Trademark Office PTOL-37 (Rev. 08-06) N	otice of Allowability	Part of Paper No./Mail Date 20110621					

DETAILED ACTION

The following is an examiner's statement of reasons for allowance: The remarks submitted by the Applicant on 6/17/11 have been considered and are persuasive. Claims 14-95 are allowed.

Any comments considered necessary by applicant must be submitted no later than the payment of the issue fee and, to avoid processing delays, should preferably accompany the issue fee. Such submissions should be clearly labeled "Comments on Statement of Reasons for Allowance."

IDS

The information disclosure statement filed 6/20/11 fails to comply with the provisions of 37 CFR 1.97, 1.98 and MPEP § 609 because some of the cited document(s) do not have accompanying dates(please see attached 1449 for the specific documents). It has been placed in the application file, but some of the information referred to therein has not been considered as to the merits. Applicant is advised that the date of any re-submission of any item of information contained in this information disclosure statement or the submission of any missing element(s) will be date of submission for purposes of determining compliance with the requirements based on the time of filing the statement, including all certification requirements for statements under 37 CFR 1.97(e). See MPEP § 609.05(a).

USPTO Contact Information

Any inquiry concerning this communication or earlier communications from the examiner should be directed to HOSUK SONG whose telephone number is (571)272-3857. The examiner can normally be reached on mon-fri.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, KIM VU can be reached on 5712723859. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Application/Control Number: 12/561,138 Art Unit: 2435

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pairdirect.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/HOSUK SONG/ Primary Examiner, Art Unit 2435

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Part of Paper No. 20110621



Application/Control No. 12/561,138	Applicant(s)/Patent under Reexamination CHU, WILLIAM W.Y.
Examiner	Art Unit
HOSUK SONG	2435

	ISSUE CLASSIFICATION													
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2 0 2011 ಪ INFORMATION DISCLOSURE ATEMENT BY APPLICANT

21	Complete if Known							
	Application Number	12/561,138						
	Filing Date	September 16, 2009						
	First Named Inventor	William W.Y. Chu						
	Art Unit	2435						
	Examiner Name	Hosuk Song						
	Attorney Docket Number	ACQI-006/03US 310578-2053						

(Use as many sheets as necessary) 1 116

U.S. PATENT DOCUMENTS Cite No Document Number Pages, Columns, Lines, Where Examiner Publication Date Name of Patentee or Relevant Passages or Relevant Initials* Number-Kind Code2 (if known) MM-DD-YYYY Applicant of Cited Document Figures Appear 12/322.858 02-05-2009 Chu 11/545,056 Chu 10-06-2006 A108 5764924 06-09-1998 Hong A109 5317441 05-31-1994 Sidman

	FOREIGN PATENT DOCUMENTS					
Examiner Initials*	Cite No. ¹	Foreign Patent Document Country Code ³ "Number ⁴ "Kind Code ⁵ (<i>if known</i>)	Publication Date MM-DD- YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear	T
	BA002	WO 94/000970	01-06-1994	Oakleigh Systems, Inc.		

	NON PATENT LITERATURE DOCUMENTS						
Examiner Initials*	Cite No.1	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.	T ²				
	C095	Part 3: Carrier sense multiple access with collision detertion (CSMA/CD) access method and physical layer specifications, IEEE Standard 802.3z, The Institute of Electrical and Electronics Engineers, Inc., July 1998, 1262 pages.					
	C133	Excerpt from "Microsoft Computer Dictionary, 5th Edition", Microsoft Press, 2002, pages 96, 329, 624 and 625.					
	C135	Intel Corporation, Intel 82559 Fast Ethernet Controller," [retrieved on 03-14-2011], Retrieved from the Internet: <url: 82559.htm="" controllers="" design="" http:="" lan="" network="" products="" www.intel.com="">, 1 page.</url:>					
	C136	GRUENER, J., "Vendors Pack in More Servers," PC Week, Vol. 14, No. 1, March 17, 1997, 2 pages.					
- • • · · · ·	C137	GRIGONIS, R., "Fault Resilient PC's," Flatiron Publishing, 1996, 314 pages.					
	C138	Microsoft Press Computer User's Dictionary, pages 82 and 232, Kim Fryer ed., Microsoft Press, 1998, 5 pages.					
	C139	IBM Thinkpad Product Information Guide, IBM PC Company, April 28, 1998, 26 pages.					
	C140	The American Heritage Dictionary, pages 536, 607 and 770, Dell Publishing, 1994, 5 pages.	<u> </u>				
	C141	The New IEEE Standard Dictionary of Electrical and Electronics Terms, Fifth Ed., page 1236, The Institute of Electrical and Electronics Engineers, Inc., 1993, 3 pages.					

Examine Signatur	/Hosuk Song/	Date Considered	06/29/2011
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*EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant. ¹Applicant's unique citation designation number (optional). ²See Kinds Codes of USPTO Patent Documents at <u>www.uspto.gov</u> or MPEP 901.04. ³Enter Office that issued the document, by the two-letter code (WIPO Standard ST.3). ⁴For Japanese patent documents, the indication of the year of the reign of the Emperor must precede the serial number of the patent document. ⁵Kind of document by the appropriate symbols as indicated on the document under WIPO Standard ST. 16 if possible. ⁶Applicant is to place a check mark here if English language Translation is attached.

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INFORMATION DISCLOSURE STATEMENT BY APPLICANT

Complete if Known				
Application Number	12/561,138			
Filing Date	September 16, 2009			
First Named Inventor	William W.Y. Chu			
Art Unit	2435			
Examiner Name	Hosuk Song			
Attorney Docket Number	ACQI-006/03US 310578-2053			

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Sheet 2

		NON PATENT LITERATURE DOCUMENTS	
Initials*		Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.	T ²
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INFORMATION DISCLOSURE STATEMENT BY APPLICANT

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of 16

Complete if Known						
Application Number	12/561,138					
Filing Date	September 16, 2009					
First Named Inventor	William W.Y. Chu					
Art Unit	2435					
Examiner Name	Hosuk Song					
Attorney Docket Number	ACQI-006/03US 310578-2053					

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Art Unit	2435				
Examiner Name	Hosuk Song				
Attorney Docket Number	ACQI-006/03US 310578-2053				

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of

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	NFORMATION DISC		Filing Date	September 16, 2009
			First Named Inventor	William W.Y. Chu
	STATEMENT BY AP		Art Unit	2435
	(Use as many sheets as nec	essary)	Examiner Name	Hosuk Song
Sheet	5	of 16	Attorney Docket Number	ACQI-006/03US 310578-2053

Attorney Docket Number ACQI-006/03US 310578-205

		NON PATENT LITERATURE DOCUMENTS	
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	Application Number	12	
	Filing Date	S	
	First Named Inventor	W	
STATEMENT BY APPLICANT	Art Unit	24	
(Use as many sheets as necessary)	Examiner Name	H	

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Sheet

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First Named Inventor	William W.Y. Chu	
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INFORMATION DISCLOSURE STATEMENT BY APPLICANT

Complete if Known			
Application Number 12/561,138			
Filing Date	September 16, 2009		
First Named Inventor	William W.Y. Chu		
Art Unit	2435		
Examiner Name	Hosuk Song		
Attorney Docket Number	ACQI-006/03US 310578-2053		

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Sheet 8

_	NON PATENT LITERATURE DOCUMENTS				
Examiner Initials* Cite No. ¹ Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title (when appropriate), title (when appropriate), title (when appropriate), ti		T ²			
	C251	"J&L Introduces Twin Pentium for ChatterBox Systems, J&L Information Systems, Press Release, January 29, 1996, 1 page.			
	C252	"ChatterBox/SAS™ - Scaleable Access Server™," J&L Information Systems, Networks Expo - Boston '96, December 22, 1995, 1 page.			
	C253	"J&L Information Systems Announces ChatPower-Plus™ a Revolutionary Redundant Power Supply System," J&L Information Systems, Press Release, June 19, 1995, 2 pages.			
	C254	"J&L Announces ChatAccess/PC™, a PCMCIA Based Remote LAN Node Server," J&L Information Systems, Press Release, June 19, 1995, 2 pages.			
	C256	"J&L Announces Two Patents," J&L Information Systems, Press Release, February 9, 1995, 1 page.			
	C257	"J&L Announces their ChatExpress-P100 Rackmounted Applications Server at Networks Expo. Boston," J&L Information Systems, Press Release, February 13, 1994, 3 pages.			
	C258	"J&L Doubles the Rack-Mounted Communications Server Density with ChatVantage/486™," J&L Information Systems, Press Release, September 11, 1995, 2 pages.			
	C260	"ChatCom, Inc. Announces Results for the June 30 Quarter," ChatCom, Inc., News Release, August 16, 1996, 2 pages.			
	C261	"Introducing the new ChatterBox™ Corporate and Office Seriesthe Power Behind Your Network," ChatCom, Inc., May 31, 1996, 15 pages.			
	C262	"ChatterBox Communications and Server Solutions," ChatCom, Inc., March 7, 1996, 12 pages.			
	C263	"ChatterBox Communications and Server Solutions Products," ChatCom, Inc., April 24, 1996, 7 pages.			
	C264	LAZIK, G., "Remote Access - a Historical Perspective," Network News, Vol. 3, No. 7, NPA The Network Professional Association, July, 1994, 6 pages.			
	C265	LAZIK, G., "Remote Access - Part II, Cost Analysis," Network News," Vol. 3, No. 8, NPA The Network Professional Association, September, 1994, 5 pages.			
	C267	"Plexnet™ Product Overview," Plexcom, Inc., 1992, 8 pages.			
	C268	"Thin Client Servers High-Speed Data Switching Technical Summary," QuantumNet, Inc., August 29, 2010, 28 pages.			
	C269	Facsimile from Procrass to Paunovich attaching "QuantumNet Network Computing Systems," August 30, 2010, 8 pages.			
	6270	"List of Representative Custemers," Network Engines, Inc., undated, 1 page			
	C271	World Wide System Price Guide, Network Engines, Inc., September 26, 1997, 10 pages.			
	C272	P6000 System Price Guide, Network Engines, Inc., February 24, 1998, 9 pages.			

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Application Number	12/561,138		
Filing Date	September 16, 2009		
First Named Inventor	William W.Y. Chu		
Art Unit	2435		
Examiner Name	Hosuk Song		
Attorney Docket Number	ACQI-006/03US 310578-2053		

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_{of} 16

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Sheet

		NON PATENT LITERATURE DOCUMENTS		
Examiner Initials*				
	C273	"Venture financing is fuel for Powerstation's Growth Plans," Mass High Tech Communications, Inc., June 2, 1997, 1 page.		
	C274	GRIGONIS, R., "Life-Saving Computers: Network Engines," Computer Telephony, September, 1997, 1 page.		
	C275	RODGERS, A., "NT Clustering Hardware Readied, Vendor Racks up Windows NT Clustering Options at NetWorld+Interop," Internetweek, October 20, 1997, 1 page.		
	C276	"Network Engines Awarded Best of Show at Networld + Interop 97, New company debuts product and wins," Network Engines, Inc., Press Release, October 14, 1997, 2 pages.		
	C277	Network Engines Website, Network Engines, Inc., [retrieved on 2-27-1998], Retrieved from the Internet: <url: http:="" www.networkengines.com=""></url:> , 12 pages.		
	C278	Network Engines, Inc., Company Overview, August 26, 2010, 21 pages.		
c	@279	Clustered Servers for Network Based Applications," Network Engines, Inc., undeted, 27-		
	C280	Network Engines ClusterDirector Users' Manual, Revision B, Network Engines, Inc., June, 1998, 88 pages.		
	C281	Network Engines ClusterDirector Users' Manual, Network Engines, Inc., January, 1998, 52 pages.		
	C282	MP700 User Guide, Issue 0.0.89, Network Engines, Inc., October 16, 1997, 29 pages.		
	C283	"ClusterDirector™ Product Description, Fault Tolerance for Industry Standard Processors, Operating Systems, and Applications," Network Engines, Inc., 1998, 4 pages.		
	~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~	Maintenance and Service Cuide, Compaq Armada 4100 and 4200 Families of Personal Computere, 100 pages	•	
	C285	"Network Engines Announces New Clustered Application Servers for Web, Thin-Client and Windows NT Enterprise Environments," Network Engines, Inc., Press Release, October 8, 1997, 3 pages.		
····· -	C286	"Network Engines Announces Partnership With Telegration Associates, Inc.," Network Engines, Inc., Press Release, December 10, 1997, 2 pages.		
	C287	"Network Engines Debuts ClusterDirector in Internet/Intranet Load Balanced Environment," Network Engines, Inc., Press Release, January 27, 1998, 3 pages.		
	C288	STALLINGS, W., "Computer Organization and Architecture - Designing for Performance," Sixth Edition, Pearson Education, Inc., 2003, pages 69-89.		
	C289	HILL, Goff (editor), "The Cable and Telecommunications Professional's Reference: Volume 1," Third Edition, Focal Press, 2007, pp. 225-229, 7 pages.		
	C290	Dell, Inc., White Paper, "PCI Express Technology," February 2004, pages 1-11.		

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Application Number 12/561,138			
Filing Date	September 16, 2009		
First Named Inventor	William W.Y. Chu		
Art Unit	2435		
Examiner Name	Hosuk Song		
Attorney Docket Number	ACQI-006/03US 310578-2053		

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Sheet 10

		NON PATENT LITERATURE DOCUMENTS		
Examiner Initials*	Cite No.   item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.			
	C291	ATHAVALE, A., "How to Lower the Cost of PCI Express Adoption by Using FPGAs," EETimes Design [online] April 26, 2006, [retrieved on May 3, 2011]. Retrieved from the Internet at <url: http://www.eetimes.com/General/DisplayPrintViewContent?contentItemID=4014824&gt;, 6 pages.</url: 		
<u>är ge</u>	C292	THOMS, I., "IBM Hit with \$9M Judgment in Server Patent Suit," Law360 [online], [retrieved on May 3, 2011], Retrieved from the Internet at <url: 229575="" articles="" http:="" print?section="ip" www.law360.com="">, 2 pages.</url:>		
	C293	MCKENZIE, L., "Fujitsu Reaches Deal in Acqis Blade Server IP Spat," Law360 [online], [retrieved on June 16, 2010], Retrieved from the Internet at <url: http://ip.law360.com/print_article/175004&gt;, 2 pages.</url: 		
	C294	PCI Local Bus Specification, Rev. 2.1, The PCI Special Interest Group, June 1, 1995, 298 pages.		
	C295	"National Semiconductor Design Guide," LVDS Owner's Manual, Spring 1997, 65 pages.		
	C296	Intel Corporation, "PCI Express* to PCI-X* Bridge Architecture: Where Interface Standards Meet," 2003, 8 pages.		
·	C297	Desai, D.M. et al., "BladeCenter system overview," IBM Journal of Research and Development, Vol. 49, No. 6, November 2005, pp. 809-821, 13 pages.		
	C298	Spring, Tom, "Top of the News - Broadband Users Still Sing the Blues," PC World, June 2011, pp. 42-54, 13 pages.		
*	C299	San Jose Mercury News, "Business & Stocks - Top Stories from The Mercury News," June 28, 2001, [online], [retrieved on June 30, 2001], Retrieved from the Internet at <url: business="" docs="" http:="" premium="" technews28.htm="" www0.mercurycenter.com="">, 5 pages.</url:>		
	C300	"iMod Pad," Wired Magazine, March 2001, 1 page.		
	IC46	"Amended Invalidity Chart For Base Reference Network Engines P6000 Server," submitted by the Defendants in connection with Case No. 6:09-cv-148-LED on June 4, 2010, 64 pages.		
	IC47	Email from Emanuel to Juarez including Invalidity Chart for Base Reference IBM BladeCenter, submitted by the Defendants in connection with Case No. 6:09-cv-148-LED, dated August 20, 2010, 54 pages.		
	IC48	Letter from Martiniak to Byers regarding Proposed Amendment to the Invalidity Contentions based on products from RLX Systems and a description of RLX products, dated July 15, 2010, 2 pages.		
	IC49	Defendant's Invalidty Chart for Base Reference RLX System 324, proposed in connection with Case No. 6:09-cv-148-LED on July 15, 2010, 58 pages.		

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	Filing Date	September 16, 2009		
	First Named Inventor	William W.Y. Chu		
Art Unit		2435		
	Examiner Name	Hosuk Song		
	Attorney Docket Number	ACQI-006/03US 310578-2053		

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	+F-02	"Appendix 6A Diselecture of Accerted Claims and Infringement Contentions," submitted by			
		the Plaintiff in the U.O. District Court for the Eastern District of Texas, Case No. 6:00 ov 140	•		
		1			
	IF03	"Disclosure of Asserted Claims and Infringement Contentions," submitted by the Plaintiff in			
		the U.S. District Court for the Eastern District of Texas, Case No. 6:09-cv-148-LED, served			
		on September 14, 2009, 5 pages.			
	IF04	"Exhibit 1, Disclosure of Asserted Claims and Infringement Contentions for Defendant Appro			
		International, Inc.," submitted by the Plaintiff in the U.S. District Court for the Eastern District			
		of Texas, Case No. 6:09-cv-148-LED, served on September 14, 2009, 105 pages.			
	IF05	"Exhibit 2, Disclosure of Asserted Claims and Infringement Contentions for Defendant			
		ClearCube Technology, Inc.," submitted by the Plaintiff in the U.S. District Court for the			
		Eastern District of Texas, Case No. 6:09-cv-148-LED, served on September 14, 2009, 163	}		
		pages.	ļ		
	IF06	"Exhibit 3, Disclosure of Asserted Claims and Infringement Contentions for Defendant Dell			
		Inc.," submitted by the Plaintiff in the U.S. District Court for the Eastern District of Texas,			
		Case No. 6:09-cv-148-LED, served on September 14, 2009, 184 pages.	ļ		
	IF07	"Exhibit 4, Disclosure of Asserted Claims and Infringement Contentions for Defendant Fujitsu			
		America, Inc.," submitted by the Plaintiff in the U.S. District Court for the Eastern District of			
		Texas, Case No. 6:09-cv-148-LED, served on September 14, 2009, 210 pages.			
	IF08	"Exhibit 5, Disclosure of Asserted Claims and Infringement Contentions for Defendant			
		Hewlett-Packard Co.," submitted by the Plaintiff in the U.S. District Court for the Eastern			
<u></u>		District of Texas, Case No. 6:09-cv-148-LED, served on September 14, 2009, 279 pages.			
	IF09	"Exhibit 6, Disclosure of Asserted Claims and Infringement Contentions for Defendant IBM			
		Corp.," submitted by the Plaintiff in the U.S. District Court for the Eastern District of Texas,			
		Case No. 6:09-cv-148-LED, served on September 14, 2009, 242 pages.			
	IF10	"Exhibit 7, Disclosure of Asserted Claims and Infringement Contentions for Defendant NEC			
		Corp. of America," submitted by the Plaintiff in the U.S. District Court for the Eastern District	I		
		of Texas, Case No. 6:09-cv-148-LED, served on September 14, 2009, 166 pages.			
	IF11	"Exhibit 8, Disclosure of Asserted Claims and Infringement Contentions for Defendant Sun			
	1	Microsystems, Inc.," submitted by the Plaintiff in the U.S. District Court for the Eastern			
		District of Texas, Case No. 6:09-cv-148-LED, served on September 14, 2009, 243 pages.	<u> </u>		
	IF12	"Exhibit 9, Disclosure of Asserted Claims and Infringement Contentions for Defendant Super			
	Micro Computer, Inc.," submitted by the Plaintiff in the U.S. District Court for the Eastern				
		District of Texas, Case No. 6:09-cv-148-LED, served on September 14, 2009, 220 pages.	I		

(	Examiner Signature	/Hosuk Song/	Date Considered	06/29/2011	

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of 16

Sheet 12

		NON PATENT LITERATURE DOCUMENTS	
Examiner Initials*	Cite No.1	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.	T
	IF13	"Disclosure of Plaintiff's Reduced List of Asserted Claims," submitted by the Plaintiff in the U.S. District Court for the Eastern District of Texas, Case No. 6:09-00148-LED, served on July 30, 2010, 6 pages.	
	F01	"Memorandum Opinion and Order Construing Claim Terms and Denying Defendants' Motion for Partial Summary Judgment," Issued by the U.S. District Court for the Eastern District of Texas, Case No. 6:09-cv-148-LED on August 2, 2010, 18 pages.	
	F02	"Memorandum Opinion and Order Construing Claim Terms," Issued by the U.S. District Court for the Eastern District of Texas, Tyler Division, Case No. 6:09-cv-148-LED, Document 602, Feb. 3, 2011, 12 pgs.	
	F03	"Jury Verdict Form," Returned by the Jury in the U.S. District Court for the Eastern District of Texas, Case No. 6:09-cv-148-LED on Februrary 23, 2011, 2 pages.	
	F04	"Final Judgement," Issued by the U.S. District Court for the Eastern District of Texas, Case No. 6:09-cv-148-LED on March 1, 2011, 1 page.	
	G001	"Complaint for Patent Infringement," Acqis v. Appro Int'l, Inc. et al., Case No. 6:09-cv-00148, filed April 2, 2009, 13 pages.	
	G010	"First Amended Complaint for Patent Infringement," Acqis v. Appro Int'l, Inc. et al., Case No. 6:09-cv-00148, filed May 18, 2009, 14 pages.	
	G011	"Defendant Clearcube Technology, Inc.'s Answer, Counterclaims to Acqis LLC's First Amended Complaint for Patent Infringement, and Jury Demand," Case No. 6:08-cv-00148, filed July 2, 2009, 28 pages.	
	G012	"Defendant Nex Computers Technology, Inc.'s Answer to Acqis LLC's First Amended Complaint for Patent Infringement, and Jury Demand," Case No. 6:09-cv-00148-LED, filed July 8, 2009, 16 pages.	
	G013	"Defendant Hitachi Ameirca, LTD.'s, Answer to Acqis LLC's First Amended Complaint for Patent Infringement, and Affirmative Defenses and Counterclaims," Case No. 6:09-cv-00148- LED, filed July 8, 2009, 22 pages.	
	G014	"Defendant International Business Machines Corp.'s Answer to Acqis LLC's First Amended Complaint, Affirmative Defenses, and Counterclaims," Case No. 6:09-cv-148-LED, filed July 8, 2009, 22 pages.	
	G015	"Second Amended Complaint for Patent Infringement," Acqis v. Appro Int'I, Inc. et al., Case No. 6:09-cv-00148, filed July 22, 2009, 49 pages.	
	G016	"Defendant Appro's Answer, Affirmative Defenses, and Counterclaims to Acqis LLC's Second Amended Complaint for Patent Infringement," Case No. 6:09-cv-148, filed August 5, 2009, 43 pages.	

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Art Unit	2435			
Examiner Name         Hosuk Song           Attorney Docket Number         ACQI-006/03US 310578-2053				

NON PATENT LITERATURE DOCUMENTS Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the Examiner Cite No.1 item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue T² Initials* number(s), publisher, city and/or country where published. G017 'Defendant International Business Machines Corp.'s Answer to Acgis LLC's Second Amended Complaint, Affirmative Defenses, and Counterclaims," Case No. 6:09-cv-148-LED, filed August 10, 2009, 28 pages. G018 "Defendant Super Micro Computer, Inc.'s Answer and Counterclaims to Acgis LLC's Second Amended Complaint for Patent Infringement," Case No. 6:09-cv-148, filed August 10, 2009, 96 pages. G019 Defendant Sun Microsystems, Inc.'s Answer and Counterclaims to Acgis LLC's Second Amended Complaint for Patent Infringement," Case No. 6:09-cv-148, filed August 10, 2009, 95 pages. G020 "NEC Corporation of America's Answer, Affirmative Defenses, and Counterclaims to Acqis LLC's Second Amended Complaint for Patent Infringement," Case No. 6:09-cv-00148-LED, filed August 10, 2009, 38 pages. "Answer to Plaintiff's Second Amended Complaint and Counterclaims of Defendant Fujitsu G021 Computer Systems Corp., n/k/a/ Fujitsu America, Inc. to Acqis LLC's Second Amended Complaint for Patent Infringement," Case No. 6:09-cv-00148-LED, filed August 10, 2009, 34 pages. G022 "Answer, Affirmative Defenses, and Counterclaims of Defendant Hewlett-Packard Company to Acqis LLC's Second Amended Complaint for Patent Infringement," Case No. 6:09-cv-148-LED, filed August 10, 2009, 40 pages. "Defendant Clearcube Technology, Inc.'s Answer, Counterclaims to Acqis LLC's Second G023 Amended Complaint for Patent Infringement, and Jury Demand," Case No. 6:08-cv-00148, filed August 10, 2009, 39 pages. "Dell's Answer and Counterclaims to Acgis LLC's Second Amended Complaint," Case No. G024 6:09-cv-00148-LED, filed August 10, 2009, 36 pages. "Defendant Nex Computers Technology, Inc.'s Answer to Acgis LLC's Second Amended G025 Complaint for Patent Infringement, and Jury Demand," Case No. 6:09-cv-00148-LED, filed August 10, 2009, 28 pages. 'Defendant Clearcube Technology, Inc.'s First Amended Answer, Counterclaims to Acgis G026 LLC's Second Amended Complaint for Patent Infringement and Jury Demand," Case No. 6:09-cv-00148, filed August 11, 2009, 39 pages. "Plaintiff Acgis LLC's Answer to Defendant Appro International, Inc.'s Counterclaims," Case G027 No. 6:09-00148-LED, filed August 28, 2009, 16 pages. "Defendant Clearcube Technology, Inc.'s Second Amended Answer Counterclaims to Acqis G028 LLC's Second Amended Complaint for Patent Infringement and Jury Demand," Case No. 6:09-CV-00148, filed August 31, 2009, 45 pages.

Examiner Signature	/Hosuk Song/	Date Considered	06/29/2011

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# INFORMATION DISCLOSURE STATEMENT BY APPLICANT

Complete if Known			
Application Number 12/561,138			
Filing Date	September 16, 2009		
First Named Inventor William W.Y. Chu			
Art Unit 2435			
Examiner Name Hosuk Song			
Attorney Docket Number ACQI-006/03US 310578-2053			

(Use as many sheets as necessary)

of 16

Sheet 14

		NON PATENT LITERATURE DOCUMENTS	
Examiner Initials*	Cite No. ¹	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.	T ²
	G029	"Plaintiff Acqis LLC's Answer to Defendant International Business Machines Corp.'s Counterclaims," Case No. 6:09-00148-LED, filed September 2, 2009, 11 pages.	
	G030	"Plaintiff Acqis LLC's Answer to Defendant Super Micro Computer, Inc.'s Counterclaims," Case No. 6:09-00148-LED, filed September 2, 2009, 15 pages.	
	G031	"Plaintiff Acqis LLC's Answer to Defendant Sun Microsystems, Inc.'s Counterclaims," Case No. 6:09-cv-00148-LED, filed September 2, 2009, 14 pages.	
	G032	"Plaintiff Acqis LLC's Answer to Defendant Dell Inc.'s Counterclaims," Case No. 6:09-00148- LED, filed September 2, 2009, 16 pages.	
12. <u>22. 22. 22. 2</u> . 2	G033	"Plaintiff Acqis LLC's Answer to Defendant Fujitsu Computer Systems Corp., N/K/A Fujitsu America, Inc.'s Counterclaims," Case No. 6:09-00148-LED, filed September 16, 2009, 7 pages.	
	G034	"Plaintiff Acqis LLC's Answer to Defendant Hewlett-Packard Company's Counterclaims," Case No. 6:09-00148-LED, filed September 16, 2009, 14 pages.	
	G035	"Plaintiff Acqis LLC's Answer to Defendant NEC Corporation of America's Counterclaims," Case No. 6:09-00148-LED, filed September 16, 2009, 8 pages.	
	G036	"Defendant Clearcube Technology, Inc.'s Third Amended Answer to Acqis LLC's Second Amended Complaint for Patent Infringement and Jury Demand," Case No. 6:09-cv-00148, filed November 11, 2009, 26 pages.	
	G037	"Defendant Clearcube Technology, Inc.'s Fourth Amended Answer to Acqis LLC's Second Amended Complaint for Patent Infringement and Jury Demand," Case No. 6:09-cv-00148, filed January 8, 2010, 26 pages.	
	G038	"Dell's First Amended Answer and Counterclaims to Plaintiff's Second Amended Complaint," Case No. 6:09-cv-00148-LED, filed April 22, 2010, 38 pages.	
	G039	"Plaintiff Acqis LLC's Answer to Defendant Dell Inc.'s First Amended Counterclaims," Case No. 6:09-00148-LED, filed May 10, 2010, 16 pages.	
	G040	"Affidavit of Timothy P. Cremen in Support of NEC Corporation of America's Opposition to Plaintiff's Motion to Dismiss and Strike," Case No. 6:09-cv-00148-LED, filed October 9, 2009, 4 pages.	,
	G041	"Comparison [by NEC] of Rejected Elements in Office Action and Elements of Exemplary Claims of Acqis's Patents," Case No. 6:09-cv-00148-LED, filed October 9, 2009, 7 pages.	
	G042	"Defendant NEC Corporation of America's Opposition to Plaintiff's Motion to Dismiss and Motion to Strike," Case No. 6:09-cv-00148-LED, filed October 9, 2010, 36 pages.	
	G043	"Motion to Dismiss Counterclaim Pursuant to Rule 12(b)(6) and Motion to Strike Affirmative Defense Pursuant to Rule 12(f)," Case 6:09-00148-LED, filed September 16, 2009, 18 pages.	

Examiner Signature	/Hosuk Song/	Date Considered	06/29/2011

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Substitute for form 1449A/PTO			Complete if Known	
			Application Number	12/561,138
			Filing Date	September 16, 2009
INFORMATION DISCLOSURE STATEMENT BY APPLICANT (Use as many sheets as necessary)			First Named Inventor	William W.Y. Chu
		BY APPLICANT	Art Unit	2435
		eets as necessary)	Examiner Name	Hosuk Song
Shee	_{et} 15	of 16	Attorney Docket Number	ACQI-006/03US 310578-2053
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		NON PATENT LITERATURE DOCUMENTS	· · ·
Examiner Initials*	Cite No. ¹	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.	T ⁱ
	H01	"Transcript of Videotaped Deposition of William Mangione-Smith," taken by the Defendants in connection with Case No. 6:09-cv-148-LED in the U.S. District Court for the Eastern District of Texas, September 9, 2010, 192 pages.	
	H02	"Defendant Sun Microsystems, Inc.'s Responses and Objections to Plaintiff Acqis LLC's Second Set of Common Interrogatories," Case No. 6:09-cv-00148-LED, filed May 12, 2010, 9 pages.	
	H03	"Plaintiff Acqis LLP's Objections and Responses to Defendants' First Set of Interrogatories," Case No. 6:09-cv-00148-LED, filed August 5, 2010, 21 pages.	
	H04	"Plaintiff Acqis LLP's Objections and Responses to Defendants' Third Set of Interrogatories," Case No. 6:09-cv-00148-LED, filed August 5, 2010, 13 pages.	
	H05	"Plaintiff Acqis LLP's First Supplemental Objections and Responses to Defendants' Third Set of Interrogatories," Case No. 6:09-cv-00148-LED, filed August 5, 2010, 14 pages.	
	H06	"Declaration of Jennifer Chen in Support of Defendants' Motion for Leave to Amend Defendants' Invalidity Contentions," Case No. 6:09-cv-00148-LED, August 5, 2010, 3 pages.	
	H07	Excerpts of Transcript of "Videotaped Deposition of William W.Y. Chu," taken by the Defendants in connection with Case No. 6:09-cv-148-LED in the U.S. District Court for the Eastern District of Texas, June 7, 2010, 20 pages.	
	H08	"Declaration of Monty McGraw in Support of Defendants' Motion for Leave to Amend Defendants' Invalidity Contentions," Case No. 6:09-cv-00148-LED, August 5, 2010, 3 pages.	
	101	"Plaintiff's Opening Brief Regarding Claim Construction," Case No. 6:09-cv-00148-LED, filed June 1, 2010, 35 pages.	
	102	"Declaration of Carolyn V. Juarez in Support of Plaintiff Acqis LLC's Opening Brief Regarding Claim Construction," Case No. 6:09-cv-00148-LED, filed June 1, 2010, 3 pages.	
	103	"Defendant's Brief in Response to Plaintiff's Opening Brief Regarding Claim Construction," Case No. 6:09-cv-00148-LED, filed June 15, 2010, 40 pages.	
	104	"Proposed Claim Construction Statement," Case No. Case No. 6:09-cv-00148-LED, filed June 15, 2010, 39 pages.	
	105	"Claim Chart for International Business Machines Corp.," Case No. 6:09-cv-00148-LED, filed June 15, 2010, 12 pages.	
	106	"Acqis LLC's Disclosure of Proposed Terms and Claim Elements For Construction Pursuant to Patent Rule 4-1," Case No. 6:09-cv-00148-LED, filed March 5, 2010, 3 pages.	
	107	"Defendant's List of Proposed Terms and Claim Elements for Construction," Case No. 6:09- cv-00148-LED, filed March 5, 2010, 15 pages.	
	108	"Defendant's Amended List of Proposed Terms and Claim Elements for Construction," Case No. 6:09-cv-00148-LED, filed March 31, 2010, 11 pages.	

Examiner Signature	/Hosuk Song/	Date Considered	06/29/2011

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Substitute for form 1449A/P	TO	Co	mplete if Known
		Application Number	12/561,138
	N DISCLOSURE	Filing Date	September 16, 2009
		First Named Inventor	William W.Y. Chu
STATEMENT	BY APPLICANT	Art Unit	2435
(Use as many	sheets as necessary)	Examiner Name	Hosuk Song
Sheet 16	of 16	Attorney Docket Number	ACQI-006/03US 310578-2053
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	109	"Defendant's Corrected List of Proposed Terms and Claim Elements for Construction," Case No. 6:09-cv-00148-LED, filed April 2, 2010, 9 pages.	
	110	"Acqis, LLC's P.R4-2 Disclosure of Preliminary Claim Constructions and Extrinsic Evidence," Case No. 6:09-cv-00148-LED, filed April 14, 2010, 10 pages.	
	111	"Defendant's P.R4-2 Disclosure of Preliminary Claim Constructions and Extrinsic Evidence," Case No. 6:09-cv-00148-LED, filed April 14, 2010, 16 pages.	
	112	"Joint Claim Construction Statement," Case No. 6:09-cv-00148-LED, filed April 30, 2010, 46 pages.	
	113	"Amended Joint Claim Construction Statement," Case No. 6:09-cv-00148-LED, filed May 5, 2010, 44 pages.	
	114	"Corrected Page 13 of Plaintiff's Opening Brief Concerning Claim Construction (D.I. 261)," Case No. 6:09-cv-00148-LED, filed June 2, 2010, 2 pages.	
	115	"Plaintiff's Reply Brief Regarding Claim Construction," Case No. 6:09-cv-00148-LED, filed June 28, 2010, 14 pages.	

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Examiner Signature	/Hosuk Song/	Date Considered	06/29/2011	
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Application Number	Application/Co	ntrol No.	Applicant(s)/Patent u Reexamination	under
	12561138			
Document Code – REIS.REVFORM		Internal D	ocument – DC	NOT MAIL

Original Patent Number of Patent to be reissued: 6643777	Notice of Reissue Published in O.G. date: 10/20/2010	
This reissue patent is subjected Ter	minal Disclaimer that	
	psecution of the reissue application ne filing of the reissue application	
The maintenance fee status is:		
is up to date ☐ was not required		
Physical surrender of the letter pate	nt:	
<ul> <li>was made</li> <li>was not made, but a statement of loss/inaccessibility was provided by applicant(s)</li> <li>is not required</li> </ul>		
Final SPRE review Tod	Swann 7/26/2011	

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Application/Control No.	Applicant(s)/Patent under Reexamination				
12/561,138	CHU, WILLIAM W.Y.				
Examiner	Art Unit				
HOSUK SONG	2435				

	SEARCHED								
Class	Subclass	Date	Examiner						
726	1-9 16-21	6/21/2011	HS						
726	26-30	6/21/2011	HS						
726	34,36	6/21/2011	HS						
713	713 182-183		HS						
713	192-194	6/21/2011	HS						

INTERFERENCE SEARCHED								
Class	Class Subclass		Examiner					
726 1-9,26-30		6/21/2011	HS					
726	726 34,36		HS					
713	713 192-194		HS					
USP( see pi		6/21/2011	HS					

SEARCH NO (INCLUDING SEARC	DTES H STRATEGY	)
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# EAST Search History

# EAST Search History (Prior Art)

Ref #	Hits	Search Query	DBs	Default Operator	Plurals	Time Stamp
S410	2520	726/1.ccls.	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2011/06/21 12:04
S411	2474	726/2.ccls.	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2011/06/21 12:04
S412	2562	726/3.ccls.	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2011/06/21 12:04
S413	3621	726/4.ccls.	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2011/06/21 12:04
S414	2227	726/5.ccls.	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2011/06/21 12:04
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S419	488	726/16.ccls.	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2011/06/21 12:05
S420	808	726/17.ccls.	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2011/06/21 12:05
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S433	914	713/183.ccls.	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2011/06/21 12:08
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S436	1069	713/194.ccls.	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2011/06/21 12:08
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S438	2820	(tamper adj3 resis \$6 or access\$4 or securit\$5) and (low near2 voltage near7 diff\$9 near8 signal \$4)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2011/06/21 12:11
S439	629	(tamper adj3 resis \$6 or access\$4 or securit\$5) and (low near2 voltage near7 diff\$9 near8 signal \$4) and (PCI)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2011/06/21 12:12
S440	16	(tamper adj3 resis \$6 or access\$4 or securit\$5) and (low near2 voltage near7 diff\$9 near8 signal \$4) and (PCI) and (serial adj3 bit adj5 channel)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2011/06/21 12:13
S441	31	(tamper adj3 resis \$6 or access\$4 or securit\$5) and (low near2 voltage or power) same diff\$9 near8 signal\$4 and (serial adj3 bit adj5 channel)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2011/06/21 12:14
S442	104	(tamper adj3 resis \$6 or access\$4 or securit\$5) and (low near2 voltage or power) and diff\$9 near8 signal\$4 and (serial adj3 bit adj5 channel)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2011/06/21 12:14
5443	105	(tamper adj3 resis \$6 or access\$4 or securit\$5 or crypt\$7 or encrypt\$4 or encipher\$4 or cipher \$4 or hash\$6) and (low near2 voltage or power) and diff \$9 near8 signal\$4 and (serial adj3 bit adj5 channel)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2011/06/21 12:17

S444	17	(tamper adj3 resis \$6 or access\$4 or securit\$5 or crypt\$7 or encrypt\$4 or encipher\$4 or cipher \$4 or hash\$6) and (low near2 voltage or power) and diff \$9 near8 signal\$4 and (serial adj3 bit adj5 channel) and (PCI or peripheral adj3 component adj5 interconnect) and stream\$4	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2011/06/21 12:18
S445	18	(tamper adj3 resis \$6 or access\$4 or securit\$5 or crypt\$7 or encrypt\$4 or encipher\$4 or cipher \$4 or hash\$6) and (voltage or power) and diff\$9 near8 signal\$4 and (serial adj3 bit adj5 channel) and (PCI or peripheral adj3 component adj5 interconnect)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2011/06/21 12:19
S446	178	(tamper adj3 resis \$6 or access\$4 or securit\$5 or crypt\$7 or encrypt\$4 or encipher\$4 or cipher \$4 or hash\$6) and (voltage or power) and diff\$9 near8 signal\$4 and (serial adj3 bit adj5 stream) and (PCI or peripheral adj3 component adj5 interconnect)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2011/06/21 12:20

S447	7	(tamper adj3 resis \$6 or access\$4 or securit\$5 or crypt\$7 or encrypt\$4 or encipher\$4 or cipher \$4 or hash\$6) and (voltage or power) and diff\$9 near8 signal\$4 and (serial adj3 bit adj5 stream) and (PCI or peripheral adj3 component adj5 interconnect) and (unidirect\$4 or single near3 direct \$4 or single adj3 way)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2011/06/21 12:22
S448	178	(tamper adj3 resis \$6 or access\$4 or securit\$5 or crypt\$7 or encrypt\$4 or encipher\$4 or cipher \$4 or hash\$6) and (voltage or power) and diff\$9 near8 signal\$4 and (serial adj3 bit adj5 stream) and (PCI or peripheral adj3 component adj5 interconnect)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2011/06/21 12:23
S449	33	(tamper adj3 resis \$6 or access\$4 or securit\$5 or crypt\$7 or encrypt\$4 or encipher\$4 or cipher \$4 or hash\$6) and (voltage near4 diff \$7) and (serial adj3 bit adj5 stream) and (PCI or peripheral adj3 component adj5 interconnect)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2011/06/21 12:25

<del>S4</del> 50	1139	(tamper adj3 resis \$6 or access\$4 or securit\$5 or crypt\$7 or encrypt\$4 or encipher\$4 or cipher \$4 or hash\$6) and (voltage near4 diff \$7) and (diff\$8 near4 signal\$5) and (PCI or peripheral adj3 component adj5 interconnect)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2011/06/21 12:26
S451	5	(tamper adj3 resis \$6 or access\$4 or securit\$5 or crypt\$7 or encrypt\$4 or encipher\$4 or cipher \$4 or hash\$6) and (voltage near4 diff \$7) and (diff\$8 near4 signal\$5) and (PCI or peripheral adj3 component adj5 interconnect) and (multiple adj3 bit adj5 channel\$4)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2011/06/21 12:30
S452	23	(tamper adj3 resis \$6 or access\$4 or securit\$5) and (low near2 voltage near7 diff\$9 near8 signal \$4) and 713/300. ccls.	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2011/06/21 15:27
<del>S</del> 453	0	(tamper adj3 resis \$6 or access\$4 or securit\$5 or crypt\$7 or encrypt\$4 or encipher\$4 or cipher \$4 or hash\$6) and (low near2 voltage or power) and diff \$9 near8 signal\$4 and (serial adj3 bit adj5 channel) and 726/1.ccls.	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2011/06/21 15:31
<b>S</b> 454	1	(tamper adj3 resis \$6 or access\$4 or securit\$5) and (low near2 voltage near7 diff\$9 near8 signal \$4) and 726/1.ccls.	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2011/06/21 15:33

S455	0	(tamper adj3 resis \$6 or access\$4 or securit\$5) and (low near2 voltage near7 diff\$9 near8 signal \$4) and 726/2.ccls.	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2011/06/21 15:33
S456	2862	(tamper adj3 resis \$6 or access\$4 or securit\$5 or encipher \$4 or cipher\$4 or encrypt\$4 or hash \$4 or signature) and (low near2 voltage near7 diff\$9 near8 signal\$4)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2011/06/21 15:36
S457	98493	(tamper adj3 resis \$6 or access\$4 or securit\$5 or encipher \$4 or cipher\$4 or encrypt\$4 or hash \$4 or signature) and (diff\$9 near8 signal\$4) and (power\$ or voltage) near3 (low or diff \$8)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2011/06/21 15:37
S458	888	(tamper adj3 resis \$6 or access\$4 or securit\$5 or encipher \$4 or cipher\$4 or encrypt\$4 or hash \$4 or signature) and (diff\$9 near8 signal\$4) and (power\$ or voltage) near3 (low or diff \$8) and (serial adj3 bit adj4 stream\$4)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2011/06/21 15:39
S459	0	(tamper adj3 resis \$6 or access\$4 or securit\$5 or encipher \$4 or cipher\$4 or encrypt\$4 or hash \$4 or signature) and (diff\$9 near8 signal\$4) and (power\$ or voltage) near3 (low or diff \$8) and (serial adj3 bit adj4 stream\$4) and 726/1.ccls.	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2011/06/21 15:41

S460	0	securit\$5 or encipher \$4 or cipher\$4 or	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2011/06/21 15:42
S461	0	\$6 or access\$4 or securit\$5 or encipher \$4 or cipher\$4 or	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2011/06/21 15:43
S462	0	securit\$5 or encipher \$4 or cipher\$4 or	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2011/06/21 15:44
S463	0	(tamper adj3 resis \$6 or access\$4 or securit\$5 or encipher \$4 or cipher\$4 or encrypt\$4 or hash \$4 or signature) and (diff\$9 near8 signal\$4) and (power\$ or voltage) near3 (low or diff \$8) and (serial adj3 bit adj4 stream\$4) and 726/5.ccls.	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2011/06/21 15:46

S464	0	(tamper adj3 resis \$6 or access\$4 or securit\$5 or encipher \$4 or cipher\$4 or encrypt\$4 or hash \$4 or signature) and (diff\$9 near8 signal\$4) and (power\$ or voltage) near3 (low or diff \$8) and (serial adj3 bit adj4 stream\$4) and 726/6.ccls.	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2011/06/21 15:47
S465	4	(tamper adj3 resis \$6 or access\$4 or securit\$5 or encipher \$4 or cipher\$4 or encrypt\$4 or hash \$4 or signature) and (diff\$9 near8 signal\$4) and (power\$ or voltage) near3 (low or diff \$8) and 726/6.ccls.	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2011/06/21 15:48
S466	7	(tamper adj3 resis \$6 or access\$4 or securit\$5 or encipher \$4 or cipher\$4 or encrypt\$4 or hash \$4 or signature) and (diff\$9 near8 signal\$4) and (power\$ or voltage) near3 (low or diff \$8) and 726/7.ccls.	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2011/06/21 15:49
S467	0	(tamper adj3 resis \$6 or access\$4 or securit\$5 or encipher \$4 or cipher\$4 or encrypt\$4 or hash \$4 or signature) and (diff\$9 near8 signal\$4) and (power\$ or voltage) near3 (low or diff \$8) and 726/8.ccls.	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2011/06/21 15:50

S468	13	(tamper adj3 resis \$6 or access\$4 or securit\$5 or encipher \$4 or cipher\$4 or encrypt\$4 or hash \$4 or signature) and (diff\$9 near8 signal\$4) and (power\$ or voltage) near3 (low or diff \$8) and 726/9.ccls.	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2011/06/21 15:50
S469	8	(tamper adj3 resis \$6 or access\$4 or securit\$5 or encipher \$4 or cipher\$4 or encrypt\$4 or hash \$4 or signature) and (diff\$9 near8 signal\$4) and (power\$ or voltage) near3 (low or diff \$8) and 726/16. ccls.	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	Non	2011/06/21 15:53
S470	6	(tamper adj3 resis \$6 or access\$4 or securit\$5 or encipher \$4 or cipher\$4 or encrypt\$4 or hash \$4 or signature) and (diff\$9 near8 signal\$4) and (power\$ or voltage) near3 (low or diff \$8) and 726/17. ccls.	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2011/06/21 15:55
S471	11	(tamper adj3 resis \$6 or access\$4 or securit\$5 or encipher \$4 or cipher\$4 or encrypt\$4 or hash \$4 or signature) and (diff\$9 near8 signal\$4) and (power\$ or voltage) near3 (low or diff \$8) and 726/18. ccls.	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2011/06/21 15:56

S472	6	(tamper adj3 resis \$6 or access\$4 or securit\$5 or encipher \$4 or cipher\$4 or encrypt\$4 or hash \$4 or signature) and (diff\$9 near8 signal\$4) and (power\$ or voltage) near3 (low or diff \$8) and 726/19. ccls.	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR		2011/06/21 15:59
S473	8	(tamper adj3 resis \$6 or access\$4 or securit\$5 or encipher \$4 or cipher\$4 or encrypt\$4 or hash \$4 or signature) and (diff\$9 near8 signal\$4) and (power\$ or voltage) near3 (low or diff \$8) and 726/20. ccls.	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2011/06/21 16:23
S474	6	(tamper adj3 resis \$6 or access\$4 or securit\$5 or encipher \$4 or cipher\$4 or encrypt\$4 or hash \$4 or signature) and (diff\$9 near8 signal\$4) and (power\$ or voltage) near3 (low or diff \$8) and 726/21. ccls.	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2011/06/21 16:42
S475	32	(tamper adj3 resis \$6 or access\$4 or securit\$5 or encipher \$4 or cipher\$4 or encrypt\$4 or hash \$4 or signature) and (diff\$9 near8 signal\$4) and (power\$ or voltage) near3 (low or diff \$8) and 726/26. ccls.	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2011/06/21 16:44

S476	10	(tamper adj3 resis \$6 or access\$4 or securit\$5 or encipher \$4 or cipher\$4 or encrypt\$4 or hash \$4 or signature) and (diff\$9 near8 signal\$4) and (power\$ or voltage) near3 (low or diff \$8) and 726/27. ccls.	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2011/06/21 16:46
S477	8	(tamper adj3 resis \$6 or access\$4 or securit\$5 or encipher \$4 or cipher\$4 or encrypt\$4 or hash \$4 or signature) and (diff\$9 near8 signal\$4) and (power\$ or voltage) near3 (low or diff \$8) and 726/28. ccls.	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2011/06/21 16:48
S478	6	(tamper adj3 resis \$6 or access\$4 or securit\$5 or encipher \$4 or cipher\$4 or encrypt\$4 or hash \$4 or signature) and (diff\$9 near8 signal\$4) and (power\$ or voltage) near3 (low or diff \$8) and 726/29. ccls.	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2011/06/21 16:51
S479	10	(tamper adj3 resis \$6 or access\$4 or securit\$5 or encipher \$4 or cipher\$4 or encrypt\$4 or hash \$4 or signature) and (diff\$9 near8 signal\$4) and (power\$ or voltage) near3 (low or diff \$8) and 726/30. ccls.	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2011/06/21 16:52

S480	11	(tamper adj3 resis \$6 or access\$4 or securit\$5 or encipher \$4 or cipher\$4 or encrypt\$4 or hash \$4 or signature) and (diff\$9 near8 signal\$4) and (power\$ or voltage) near3 (low or diff \$8) and 726/36. ccls.	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2011/06/21 17:02
S481	7	(tamper adj3 resis \$6 or access\$4 or securit\$5 or encipher \$4 or cipher\$4 or encrypt\$4 or hash \$4 or signature) and (diff\$9 near8 signal\$4) and (power\$ or voltage) near3 (low or diff \$8) and 713/182. ccls.	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2011/06/21 17:08
S482	4	(tamper adj3 resis \$6 or access\$4 or securit\$5 or encipher \$4 or cipher\$4 or encrypt\$4 or hash \$4 or signature) and (diff\$9 near8 signal\$4) and (power\$ or voltage) near3 (low or diff \$8) and 713/183. ccls.	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2011/06/21 17:10
S483	10	(tamper adj3 resis \$6 or access\$4 or securit\$5 or encipher \$4 or cipher\$4 or encrypt\$4 or hash \$4 or signature) and (diff\$9 near8 signal\$4) and (power\$ or voltage) near3 (low or diff \$8) and 713/192. ccls.	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2011/06/21 17:14

S484	56	(tamper adj3 resis \$6 or access\$4 or securit\$5 or encipher \$4 or cipher\$4 or encrypt\$4 or hash \$4 or signature) and (diff\$9 near8 signal\$4) and (power\$ or voltage) near3 (low or diff \$8) and 713/193. ccls.	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2011/06/21 17:14
S486	9	(low and voltage and bit and channel and power and differential and (module or program or sofware or application or device or apparatus or component or executable adj3 code) and stream\$4 and access\$4).CLM.	US-PGPUB; USPAT	OR	ON	2011/06/21 17:26
S487	0	(low and voltage and bit and channel and power and differential and (module or program or sofware or application or device or apparatus or component or executable adj3 code) and stream\$4 and access\$4 and securit\$4 and protect\$5).CLM.	US-PGPUB; USPAT	OR	ON	2011/06/21 17:27
S488	2	(low and voltage and bit and channel and power and differential and (module or program or sofware or application or device or apparatus or component or executable adj3 code) and stream\$4 and access\$4 and securit\$4).CLM.	US-PGPUB; USPAT	OR	ON	2011/06/21 17:28

S489	2	(low and voltage and bit and channel and power and differential and (module or program or sofware or application or device or apparatus or component or executable adj3 code) and stream\$4 and access\$4 and securit\$4 and console).CLM.	US-PGPUB; USPAT	OR	ON	2011/06/21 17:28
S490	2	(low and voltage and bit and channel and power and differential and (module or program or sofware or application or device or apparatus or component or executable adj3 code) and stream\$4 and access\$4 and securit\$4 and console and storage).CLM.	US-PGPUB; USPAT	OR	ON	2011/06/21 17:29
S491	2	(low and voltage and bit and channel and power and differential and (module or program or sofware or application or device or apparatus or component or executable adj3 code) and stream\$4 and access\$4 and securit\$4 and console and storage and unidirect\$6). CLM.	US-PGPUB; USPAT	OR	ON	2011/06/21 17:29

S492	2	(low and voltage and bit and channel and power and differential and (module or program or sofware or application or device or apparatus or component or executable adj3 code) and stream\$4 and access\$4 and securit\$4 and console and storage and opposite).CLM.	US-PGPUB; USPAT	OR	ON	2011/06/21 17:30
S493	42	(tamper adj3 resis \$6 or access\$4 or securit\$5 or encipher \$4 or cipher\$4 or	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2011/06/21 18:56

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	Keywords: California security breach information act (CSBIA), Gramm-Leach-Bliley act (GLB), PCI data security and an external (PCI DSS), SQL injection, Sarbanes-Oxley act (SOX), database management system (DBMS), electric communications protection act (ECPA), health insurance portability and accountability act (HIPAA), information security (InfoSec), information technology (IT), system-specific policy (SSP), the enterprise information security (EISP), the fair and accurate credit transactions act (FACT Act)
	4 Cryptoanalysis and Improvements of Cross-Realm C2C-PAKE Protocol Ding XlaoFei, Ma ChuanGul
	July 2009 ICIE '09: Proceedings of the 2009 WASE International Conference on Information Enginee - Volume 01 , Volume 01
	Publisher: IEEE Computer Society
	Full text available: 🕷 <u>Publisher Site</u>
	Bibliometrics: Downloads (6 Weeks): n/a, Downloads (12 Months): n/a, Downloads (Overall): n/a, Citation Cour
	Most existing cross-realm client-to-client password authenticated key exchange (C2C-PAKE) protocols can no resist password-compromise impersonation (PCI) attack. This paper gives a method of resisting this attack a proposes an improved cross-realm
	Keywords: cross-realm, C2C-PAKE, PCI attack, forward secrecy, provable security
	5 Skill gaps and careers in IS compliance: implications for IS degree programs in the U.S. Christma N. Outlay, Poemima Krishnan

May 2010 SI GMI S-CPR '10: Proceedings of the 2010 Special Interest Group on Management Information System's 48th annual conference on Computer personnel research on Computer personnel research

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In this paper, we describe the research questions and methodology for a study that will investigate the opportunities and skill gaps for IS workers in the field of IS compliance. IS compliance skills include knowledge U.S. legislation - such as Sarbanes-Oxley ... Keywords: information systems (IS) skills, information systems compliance, information systems curriculum

6 Near-field communication-based secure mobile payment service

## Kiran S. Kadambi, Jun Li, Alan H. Karo

August 2009 I CEC '09: Proceedings of the 11th International Conference on Electronic Commerce
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The loss of customer account information makes headlines all too often. The Payment Card Industry (PCI) Dat Security Standard (DSS) has generated resistance from merchants because of its cost and complexity. Unfortunately, innovating in the Point of ...

Keywords: NFC, SOA, mobile payment, payment authorization

7 PCI Compliance: Understand and Implement Effective PCI Data Security Standard Compliance Tony Bradley, Anton Chuvakin, Anatoly Elberg, Brian J. Koerner

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Identity theft has been steadily rising in recent years, and credit card data is one of the number one targets fc identity theft. With a few pieces of key information. Organized crime has made malware development and computer networking attacks more  $\dots$ 

8 PCI Compliance: Understand and Implement Effective PCI Data Security Standard Compliance, 2nd adition

Anton Chuvakin, Branden R. Williams

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#### Publisher: Syngress Publishing

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Identity theft and other confidential information theft have now topped the charts as the #1 cybercrime. In particular, credit card data is preferred by cybercriminals. Is your payment processing secure and compliant? Now in its second edition, PCI Compliance ...

9 Coprocessor-based hierarchical trust management for software integrity and digital identity protection Lifu Wang, Partha Dascupta

August 2008 Journal of Computer Security, Volume 16 Issue 3 Publisher: IOS Press

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Malware and rootkits are serious security threats. They can be designed to be resistant to anti-virus and secur software and even remain totally undetectable. This paper describes a hierarchical trust management scheme where the root of trust is ...

Keywords: Computer security, digital identity, software integrity

- 10 Proceedings of the 4th symposium on Usable privacy and security
- Lorrie Faith Cranor
  - July 2008 SOUPS '08: Proceedings of the 4th symposium on Usable privacy and security Publisher: ACM

Bibliometrics: Downloads (6 Weeks): n/a, Downloads (12 Months): n/a, Downloads (Overall): n/a, Citation Count

Welcome to the Fourth Symposium On Usable Privacy and Security! This year's program features 12 technical papers, two workshops, 16 posters, 12 posters published in the past year at other conferences, a panel, four discussion sessions, and two invited ...

- 11 Cryptography as an operating system service: A case study
- Angelos D. Keromytis, Jason L. Wright, Theo De Raadt, Matthew Burnside ۲
- February 2006 Transactions on Computer Systems (TOCS) , Volume 24 Issue 1 Publisher: ACM Sequest Permissions

Full text available: The full text available: Full text available (669.12 KB)

Bibliom etrics: Downloads (6 Weeks): 28, Downloads (12 Months): 162, Downloads (Overall): 2869, Citation Cour

Cryptographic transformations are a fundamental building block in many security applications and protocols. T improve performance, several vendors market hardware accelerator cards. However, until now no operating system provided a mechanism that allowed ...

Keywords: Encryption, authentication, cryptographic protocols, digital signatures, hash functions

- 12 Software security: is ok good enough?
- John B. Dickson ۲
  - February 2011 CODASPY '11: Proceedings of the first ACM conference on Data and application security and priva Publisher: ACM

Full text available: RPDF (358.41 KB)

Bibliometrics: Downloads (6 Weeks): 25, Downloads (12 Months): 29, Downloads (Overall): 29, Citation Count: (

Widely publicized breaches regularly occur involving insecure software. This is due to the fact that the vast majority of software in use today was not designed to withstand attacks encountered when deployed on hostil networks such as the Internet.

Keywords: business justification, return on investment, test coverage

#### 13 Using Independent Auditors as Intrusion Detection Systems

December 2002 ICICS '02: Proceedings of the 4th International Conference on Information and Communications Security

### Publisher: Springer-Verlag

Jesus Molina, William A. Arbauch

Bibliometrics: Downloads (6 Weeks): n/a, Downloads (12 Months): n/a, Downloads (Overall): n/a, Citation Count

A basic method in computer security is to perform integrity checks on the file system to detect the installation malicious programs, or the modification of sensitive files. Integrity tools to date rely on the operating system function correctly, ...

- 14 An embedded fingerprint authentication system integrated with a hardware-based truly random number generator
  - Murat Erat, Kenan Danişman, Salih Erçün, Alper Kanak, Mehmet Kayaoglu

August 2007 CAI P'07: Proceedings of the 12th international conference on Computer analysis of images and patterns

#### Publisher: Springer-Verlag

Bibliometrics: Downloads (6 Weeks): n/a, Downloads (12 Months): n/a, Downloads (Overall): n/a, Citation Count

Recent advances in information security requires randomly selected strong keys. Most of these keys are generated by software-based random number generators. However, implementing a Truly Random Number Generator (TRNG) without using a hardware-supported ...

15 Evil maid goes after PGP whole disk encryption

#### Alexander Tereshkin ٨

 $September \ 2010 \ \ SIN \ '10: \ Proceedings \ of the \ 3rd \ international \ conference \ on \ Security \ of \ information \ and \ network$ Publisher: ACM

Full text available: 📆 Pdf (360.71 KB)

Bibliometrics: Downloads (6 Weeks): 10, Downloads (12 Months): 84, Downloads (Overall): 84, Citation Count: (

Full disk encryption systems are widely used to protect the information from unauthorized access. A common application of such systems is laptop hard drive and removable media encryption, because these can be easily lost or stolen. Indeed, if we assume . Keywords: full disk encryption, trusted boot

16 <u>Type safety from the ground up</u> <u>Chris Hawbitzel</u>

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January 2011 TLDI '11: Proceedings of the 7th ACM SIGPLAN workshop on Types in language design and implementation

#### Publisher: ACM

Full text available: 🗒 <u>PDF</u> (335.16 KB)

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Type safety is the most common mechanism for securely running untrusted code from the Internet. When the untrusted code is written in a type-safe language like JavaScript, Java, or C#, the language's type system guarantees that the code cannot damage ... Keywords: operating system, run-time system, type safety, verification

- 17 The national ignition facility: early operational experience with a large Ada control system
- Robert W. Cerey, Paul J. Van Arsdall, John P. Woodruff
  - December 2002 SI GAda '02: Proceedings of the 2002 annual ACM SIGAda international conference on Ada: The engineering of correct and reliable software for real-time & distributed systems using Ada and related technologies
    - Publisher: ACM 👋 Request Permissions

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The National Ignition Facility (NIF) currently under construction at the University of California Lawrence Livern National Laboratory (LLNL) is a 192-beam, 1.8-Megajoule, 500-Terawatt laser being built by the Department  ${\sf c}$  Energy and the National ...

Also published in:

March 2003 SIGAda Ada Letters Volume XXIII Issue 1

18 Information Security Policies Made Easy Version 11, Version 11 edition

Charles Cresson Wood, Dave Lineman

September 2009 Information Security Policies Made Easy Version 11, Version 11 edition
Publisher: Information Shield, Inc.

Bibliometrics: Downloads (6 Weeks): n/a, Downloads (12 Months): n/a, Downloads (Overall): n/a, Citation Count

Information Security Policies Made Easy, Version 11 is the new and updated version of the gold standard information security policy resource used by over 7000 organizations worldwide. Based on the 25 year consult and security experience of Charles ...

19 Iso27000 and Information Security: A Combined Glossary, 2nd edition It Governance Publishing

April 2010 Iso27000 and Information Security: A Combined Glossary, 2nd edition

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Get to grips with key ISO27000 and information security vocabulary with this indispensable, concise pocket guide! Information security is of crucial importance to your business. If you don t know the difference between cookie and a worm, or between ...

20 PCI DSS v1.2: A Practical Guide to Implementation

 Stave Wright

 October 2009
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Publisher: It Governance Ltd

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APPLICATION NO.	FILING DATE	FI	IRST NAMED IN	VENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.	
12/561,138	09/16/2009	·	William W.Y	. Chu	ACQI-006/03US	1717	
TITLE OF INVENTION: I	DATA SECURITY MET	HOD AND DEVI	CE FOR COM	IPUTER MODULES	310578-2053		
APPLN. TYPE	SMALL ENTITY	ISSUE FEE	E	PUBLICATION FEE	TOTAL FEE(S) DUE	DATE DUE	
nonprovisional	NO	\$1740	L	\$0	\$1740	11/04/2011	
EXAM	INER	ART UNIT	r l	CLASS-SUBCLASS	-1		
SONG, I	·	2435	<b>I</b>	726-002000			
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Electronic Patent Application Fee Transmittal								
Application Number:	12	561138						
Filing Date:	16	-Sep-2009						
Title of Invention:	DATA SECURITY METHOD AND DEVICE FOR COMPUTER MODULES							
First Named Inventor/Applicant Name:	William W.Y. Chu							
Filer:	Cliff Z. Liu/Bobbie Jutras							
Attorney Docket Number:	AC	QI-006/03US 31057	8-2053					
Filed as Large Entity								
Utility under 35 USC 111(a) Filing Fees								
Description		Fee Code	Quantity	Amount	Sub-Total in USD(\$)			
Basic Filing:								
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Claims:								
Miscellaneous-Filing:								
Petition:								
Patent-Appeals-and-Interference:								
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Extension-of-Time:								

Description	Fee Code	Quantity	Amount	Sub-Total in USD(\$)
Miscellaneous:				
	Tot	al in USD	(\$)	1740

Electronic Acl	knowledgement Receipt
EFS ID:	11125263
Application Number:	12561138
International Application Number:	
Confirmation Number:	1717
Title of Invention:	DATA SECURITY METHOD AND DEVICE FOR COMPUTER MODULES
First Named Inventor/Applicant Name:	William W.Y. Chu
Customer Number:	58249
Filer:	Cliff Z. Liu/Bobbie Jutras
Filer Authorized By:	Cliff Z. Liu
Attorney Docket Number:	ACQI-006/03US 310578-2053
Receipt Date:	06-OCT-2011
Filing Date:	16-SEP-2009
Time Stamp:	14:33:55
Application Type:	Utility under 35 USC 111(a)

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Document Number	<b>Document Description</b>	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)			
1	Issue Fee Payment (PTO-85B)	ACQI-006-03US_10-06-11_lssu	u 340970 n.		1			
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Warnings:								
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2	Fee Worksheet (SB06)	fee-info.pdf	30709	no	2			
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## **CONFIRMATION NO. 1717**

Bib Data Sheet

<b>SERIAL NUMBER</b> 12/561,138	FILING OR 371(c) DATE 09/16/2009 RULE				2435	ART UNIT D		TTORNEY DCKET NO. QI-006/03US 0578-2053	
APPLICANTS William W.Y. Chu, Los Altos, CA; ** CONTINUING DATA **********************************									
Foreign Priority claimed 35 USC 119 (a-d) condition met Verified and	35 USC 119 (a-d) conditions met Allowance Allowance Initials Acknowledged Examiner's Signature Initials Acknowledged Examiner's Signature Initials Acknowledged Fixed Part Initials Acknowledged State OK SHEELOS ACKNOWLEDGE ACKNOWLED								
58249 TITLE	IETHOD AND DEVICE	FOR COM	IPUTER MOD	OULES					
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## PTO/SB/08A (07-05) Approved for use through 07/31/2006. OMB 0651-0031

Sub	ostitute for form 1449A/PTO		Complete if Known			
540		Application Number	12/561,138			
IN	FORMATION DISCLOSURE	Filing Date	September 16, 2009			
STATEMENT BY APPLICANT		First Named Inventor	William W.Y. Chu			
		Group Art Unit	2115			
	(use as many sheets as necessary)	Examiner Name	Unassigned			
Sheet	3 of 6	Attorney Docket No.	ACQI-006/03US 310578-2053			

	U.S. PATENT DOCUMENTS						
	Examiner Initials*	Cite No. ¹	Document Number Number-Kind Code ² ( <i>if</i> <i>known</i> )	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear	
	minais	102.	US-6,401,124	06-04-2002	Yang et al.		
		102.	US-6,452,789	09-17-2002	Pallotti et al.		
		103.	US-6,452,790	09-17-2002	Chu et al.		
		105.	US-6,453,344	09-17-2002	Ellsworth		
		106.	US-6,496,361	12-17-2003	Kim et al.		
		107.	US-6,549,966	04-15-2003	Dickens et al.		
		108.	US-6,564,274	05-13-2003	Heath et al.		
		109.	US-6,643,777	11-04-2003	Chu		
		110.	US-6,718,415	04-06-2004	Chu		
		111.	US-6,725,317	04-20-2004	Bouchier et al.		
		112.	US-7,099,981	08-29-2006	Chu		
C	12 1	113.	US-7,416,446	12-05-2006	Chu 7,146,446		
Change(s) a	oplied	114.	US-7,328,297	02-05-2008	Chu		
to document		115.	US-7,363,415	04-22-2008	Chu		
	,	116.	US-7,363,416	04-22-2008	Chu		
/D.H.P./		117.	US-7,376,779	05-20-2008	Chu		
9/16/2011		118.	US-2009/0157939	06/18/2009	Chu		
7/ 10/ 2011		119.					
		120.					
		121.					

FOREIGN PATENT DOCUMENTS								
Examiner Initials*	Cite No. ¹	E Cou Numbe	eign Patent Occument intry Code ³ er ⁴ Kind Code ⁵ (if known)	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear	T	
	1.	WO	92/18924	10-29-1992				
	2.	WO	94/00097	01-06-1994				
~~~	3.	WO	95/13640	05-18-1995				
	4.	EP	722138A1	07-17-1996				
	5.	JP	6-289953	10-18-1994				

		OTHER – NON PATENT LITERATURE DOCUMENTS	
Examiner Initials*	Cite No. ¹	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.	T ⁶
	1.	AGERWALA, T. et al., "SP2 System Architecture", IBM Systems Journal, Vol. 34, No. 2 (1995)	
	2.	Bernal, Carlos, product brochure entitled: "PowerSMP Series 4000", (March 1998) << <u>http://www/winnetmag.com/Windows/Article/ArticleID/3095//3095.html</u> , downloaded from web on June 22, 2004, 2 pgs.	
	3.	CRAGLE, Jonathan, "Density System 1100", (May 1999) << <u>http://www.winnetmag.com/Windows/Article/ArtideID/5199/5199.html</u> >>, downloaded from web on June 21, 2004, 3 pgs.	
	4.	FELDMAN, Jonathan, "Rack Steady: The Four Rack-Mounted Servers That Rocked Our Network", << <u>http://www.networkcomputing.com/shared/printArtide.jhtml?article=/910/910r3sidel</u> .htm>> June 23, 2004, 3 pgs.	

ALL REFERENCES CONSIDERED EXCEPT WHERE LINED THROUGH. /H.S./



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APPLICATION NO.	ISSUE DATE	PATENT NO.	ATTORNEY DOCKET NO.	CONFIRMATION NO.
12/561,138	11/29/2011	RE42984	ACQI-006/03US 310578-2053	1717
58249 759 COOLEY LLP ATTN: Patent Grou Suite 1100 777 - 6th Street, NW WASHINGTON, D	ıp N			

ISSUE NOTIFICATION

The projected patent number and issue date are specified above.

Determination of Patent Term Extension or Adjustment under 35 U.S.C. 154 (b)

A reissue patent is for "the unexpired part of the term of the original patent." See 35 U.S.C. 251. Accordingly, the above-identified reissue application is not eligible for Patent Term Extension or Adjustment under 35 U.S.C. 154(b).

Any questions regarding the Patent Term Extension or Adjustment determination should be directed to the Office of Patent Legal Administration at (571)-272-7702. Questions relating to issue and publication fee payments should be directed to the Application Assistance Unit (AAU) of the Office of Data Management (ODM) at (571)-272-4200.

APPLICANT(s) (Please see PAIR WEB site http://pair.uspto.gov for additional applicants):

William W.Y. Chu, Los Altos, CA;