INT OF DRAWINGS
; ORIGINALLY FILED

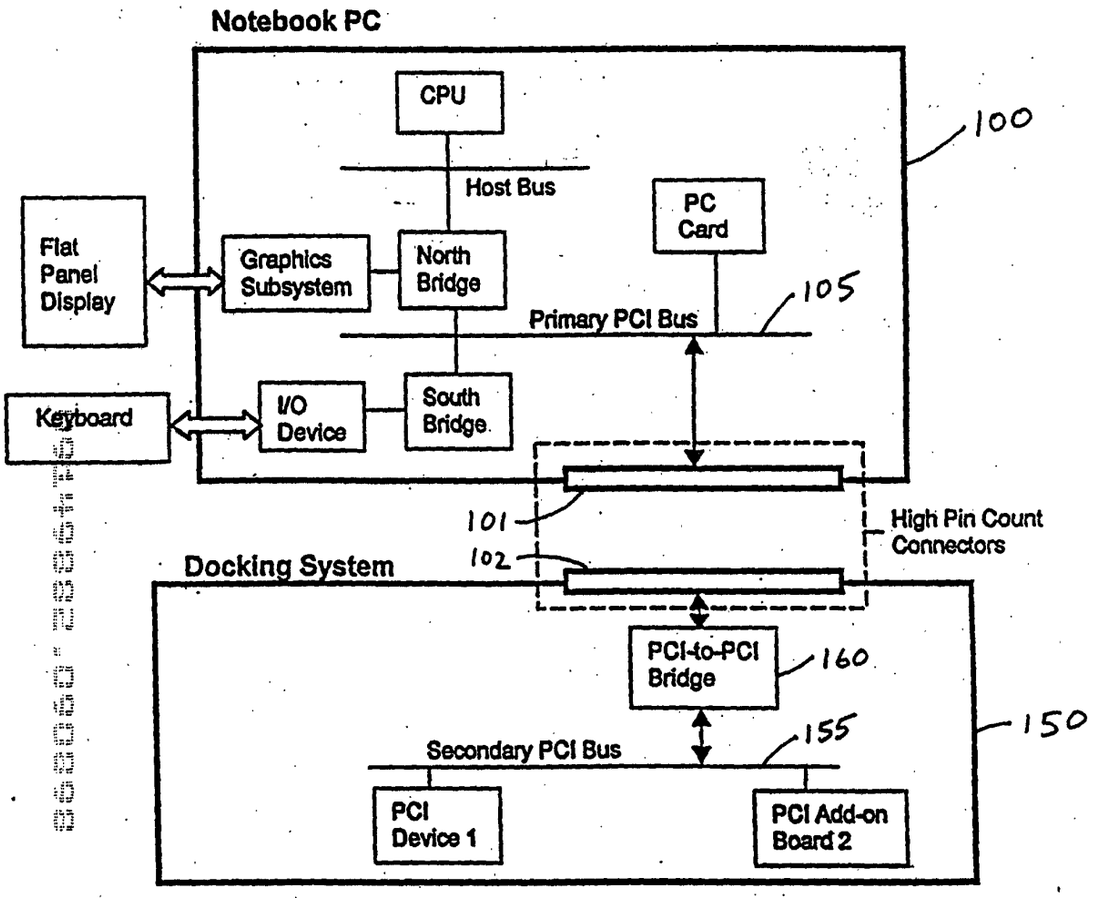


FIGURE 1

Intel Corporation v. ACQIS LLC
Intel Corp.'s Exhibit 1011, Vol 2 of 2
Ex. 1011, Page 185

F OF DRAWINGS
RIGINALLY FILED

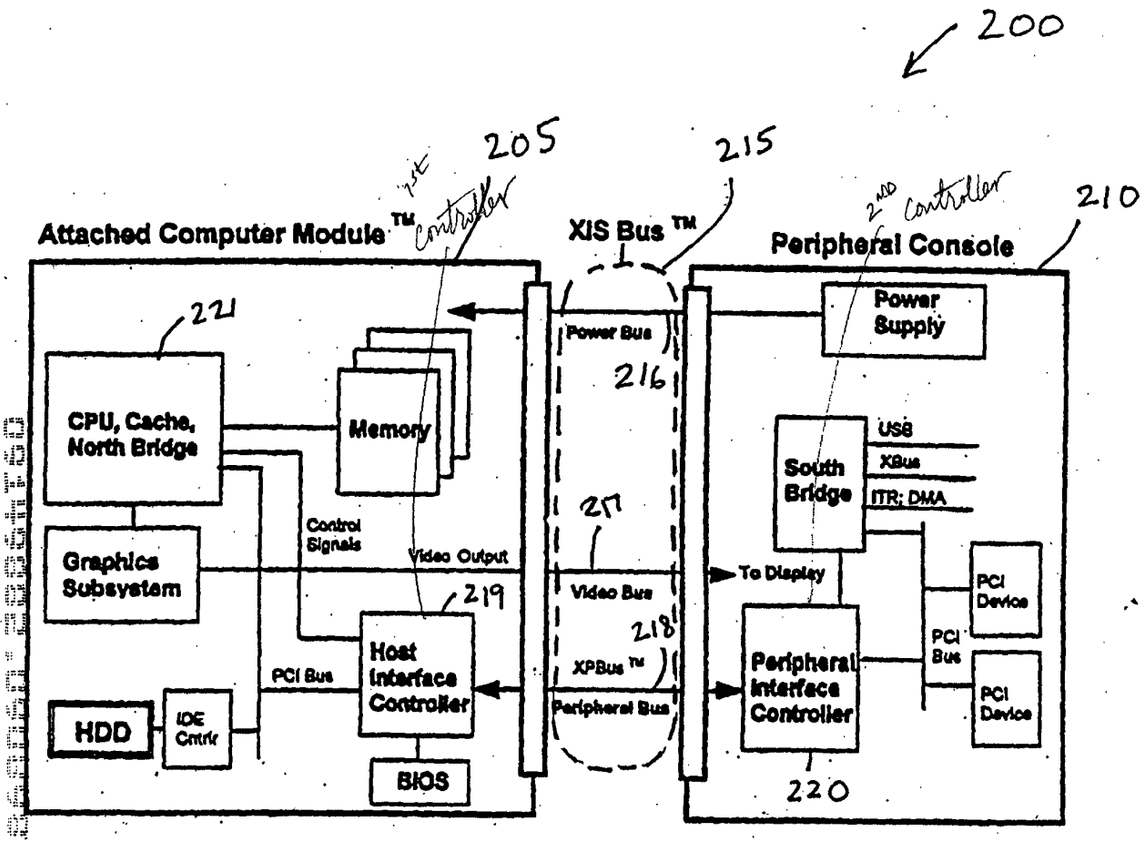


FIGURE 2

INT OF DRAWINGS
S ORIGINALLY FILED

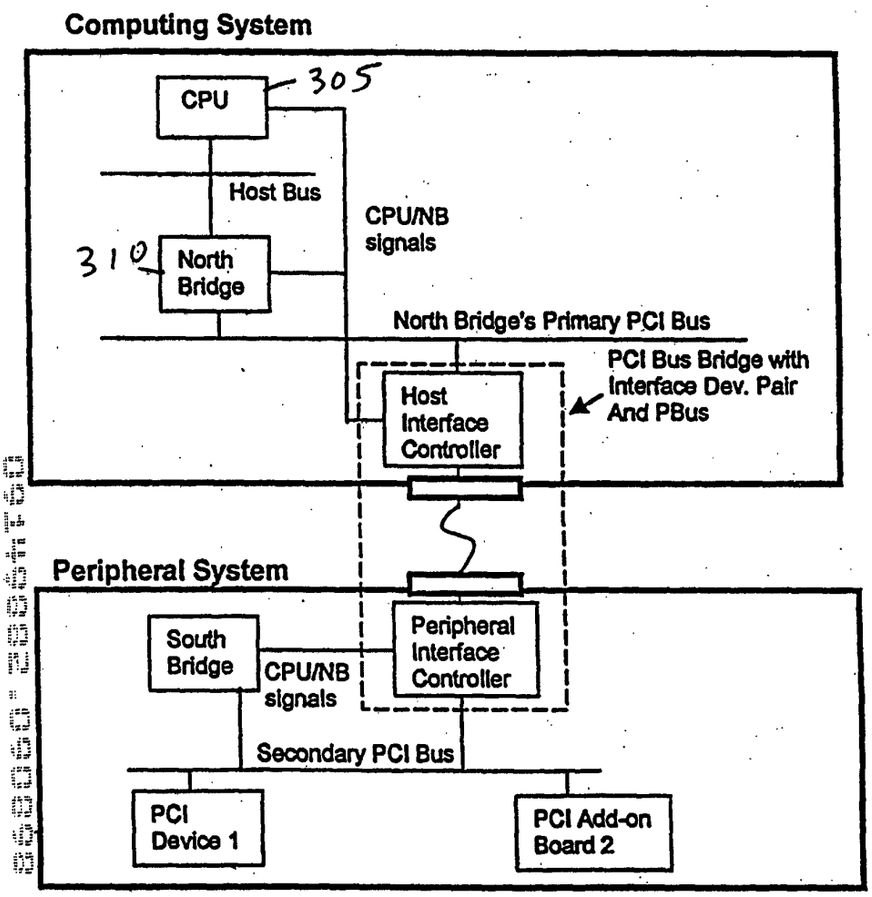


FIGURE 3

T OF DRAWINGS
RIGINALLY FILED

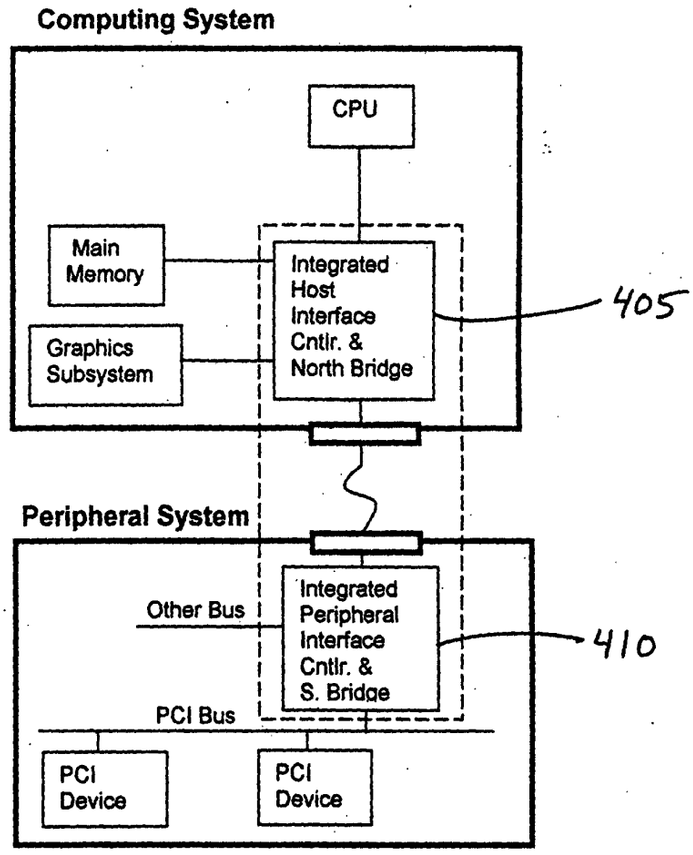


FIGURE 4

UNT OF DRAWINGS
S ORIGINALLY FILED

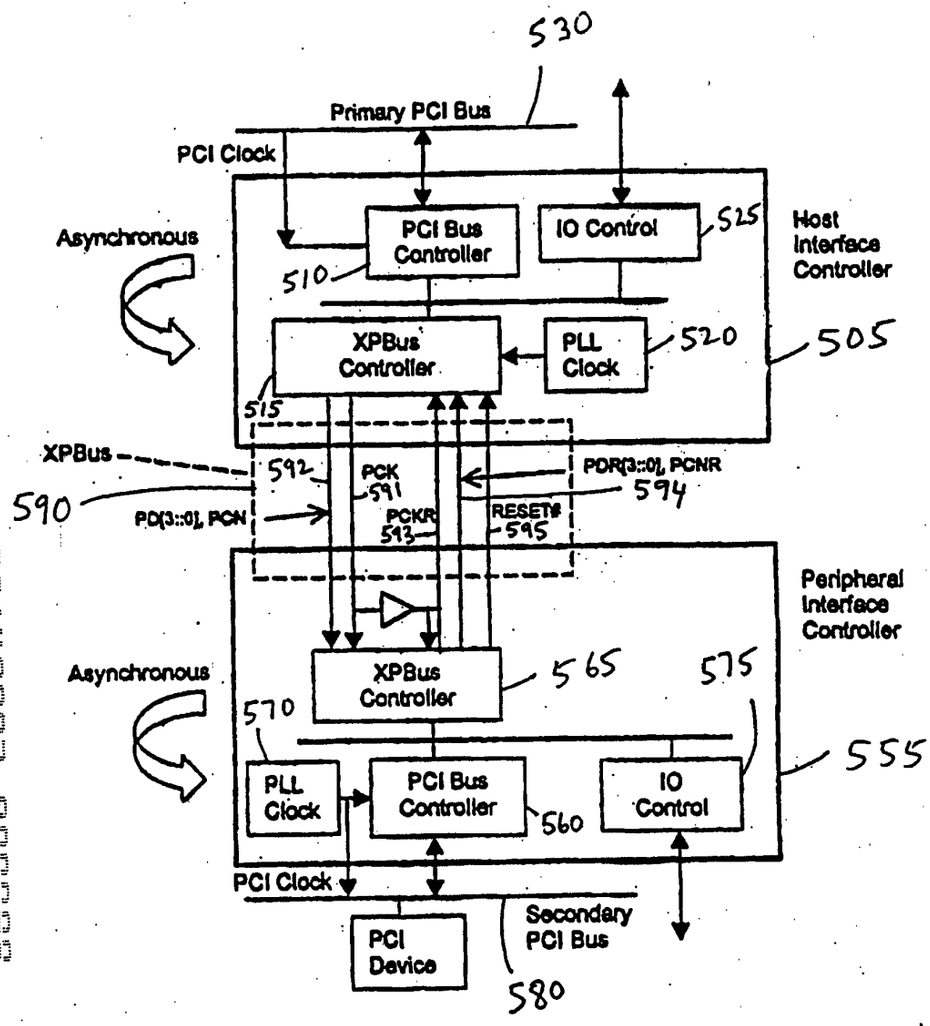


FIGURE 5

RINT OF DRAWINGS
S ORIGINALLY FILED

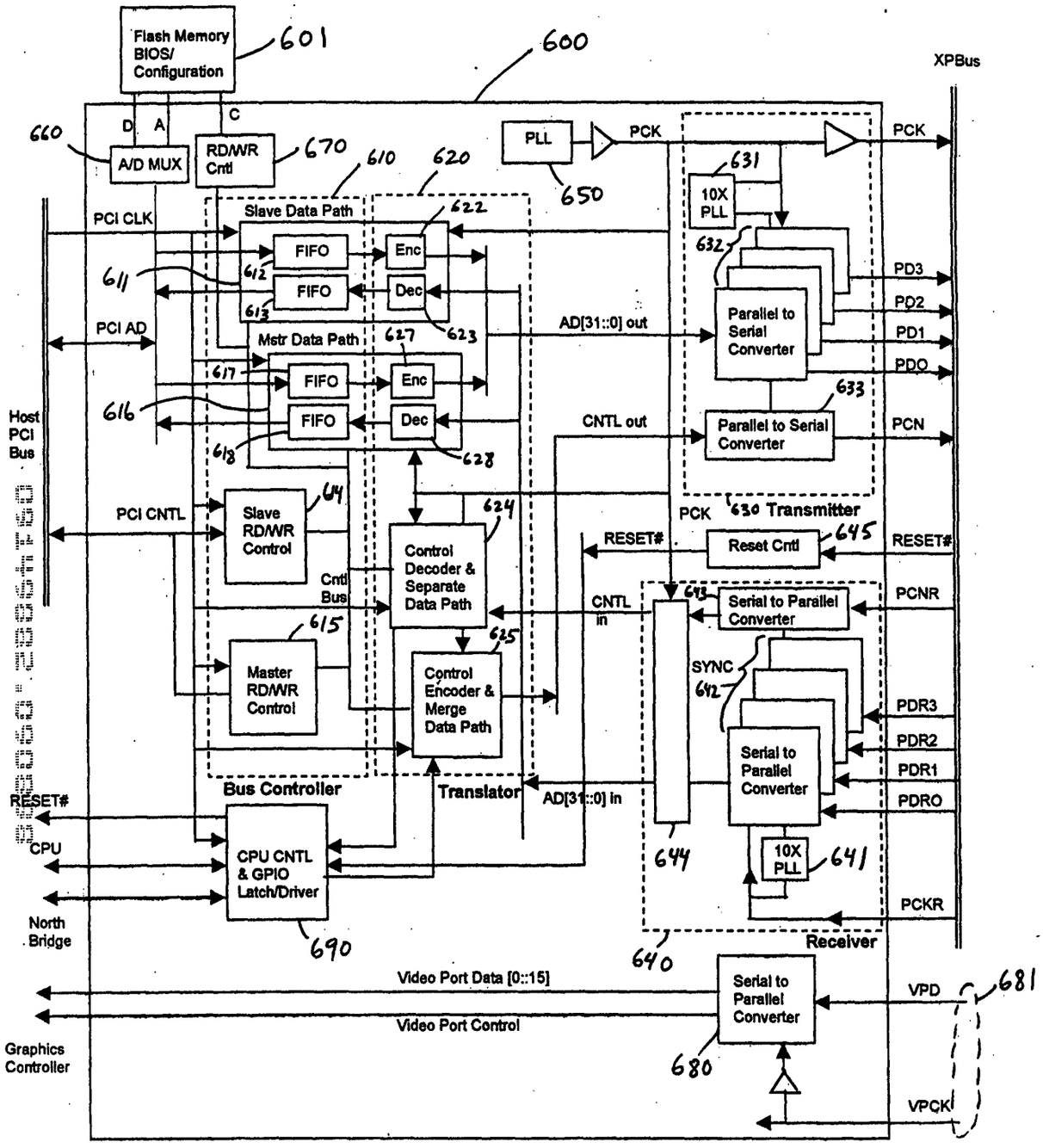


FIGURE 6

INT OF DRAWINGS
S ORIGINALLY FILED

HIC as Target (Default)

Control Signal	HIC to XPBus	XPBus to HIC	Primary PCI Bus	Comment
FRAME #	Encode (BS0)		Transaction Active	
IRDY #	Encode (BS1)		Initiator Ready	
TRDY #	Local		HIC Generates	
DEVSEL #	Local		HIC Accepts Command	Positive decode, medium
STOP #	Local		HIC requests to retry	Posted Read operation
PAR	Encode	Decode	Parity for A/C; D/BE	
IDSEL	Local		Used locally for config. 0	
PERR #	Encode	Decode	Data Parity Error	
SERR #		Decode	Address/System Parity Error	
REQ #		Decode	HIC requests to be master	S. Bus device requests bus
GNT #	Encode		Host grants bus	
RST				Independent signal

FIGURE 7

NT OF DRAWINGS
ORIGINALLY FILED

HIC as Master

Control Signal	HIC to XPBus	XPBus to HIC	Primary PCI Bus	Comment
FRAME #		Decode	Transaction Active	
IRDY #		Decode	Initiator Ready	
TRDY #	Local		Receive from Target	
DEVSEL #	Local		Receive from Target	
STOP #	Local		retry handles locally	
PAR	Encode	Decode	Parity for A/C; D/BE	
IDSEL	Local		Used locally for config. 0	
PERR #	Encode	Decode	Data Parity Error	
SERR #		Decode	Address/System Parity Error	
REQ #		Decode	HIC continue to be Master	PCI device can end REQ#
GNT #	Encode		Arbiter grant bus to HIC	Arbiter can deassert GNT#
RST				Independent signal

FIGURE 8

IT OF DRAWINGS
ORIGINALLY FILED

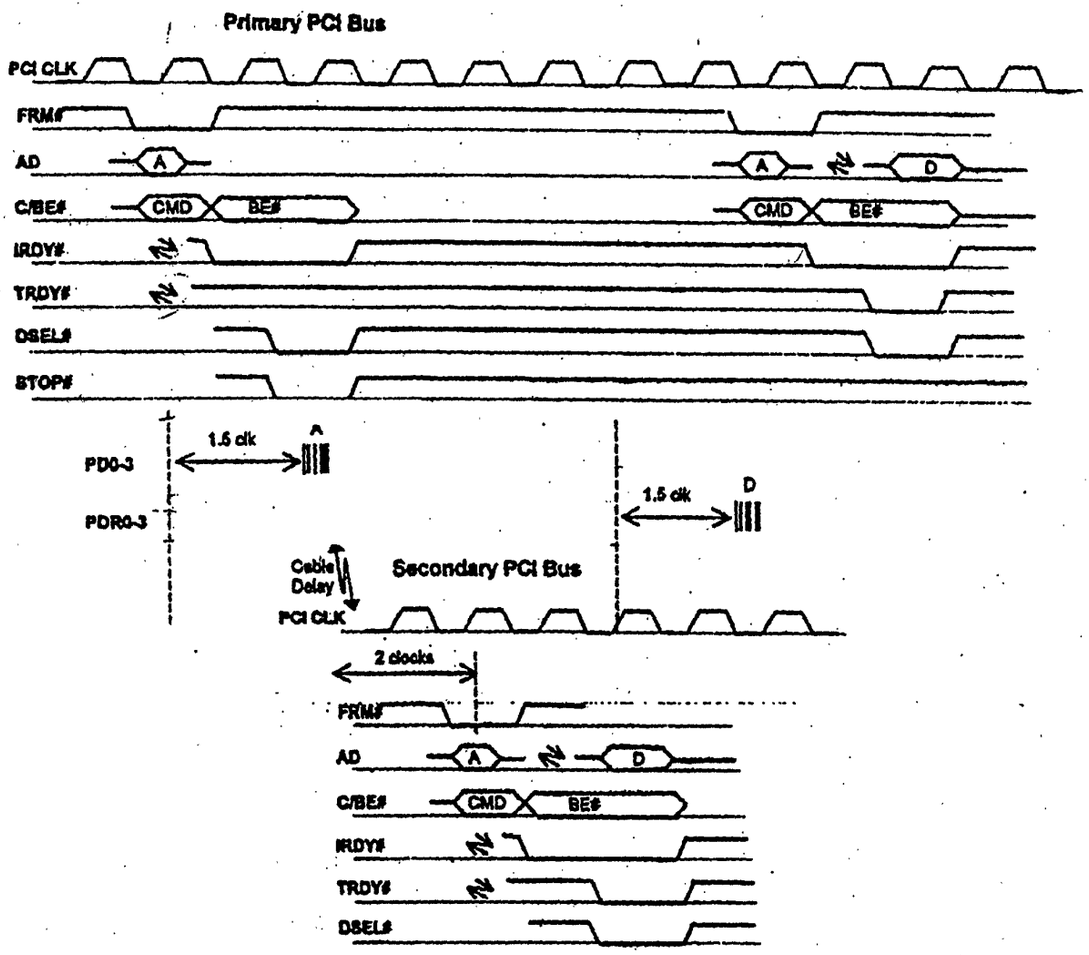


FIGURE 9

NT OF DRAWINGS
ORIGINALLY FILED

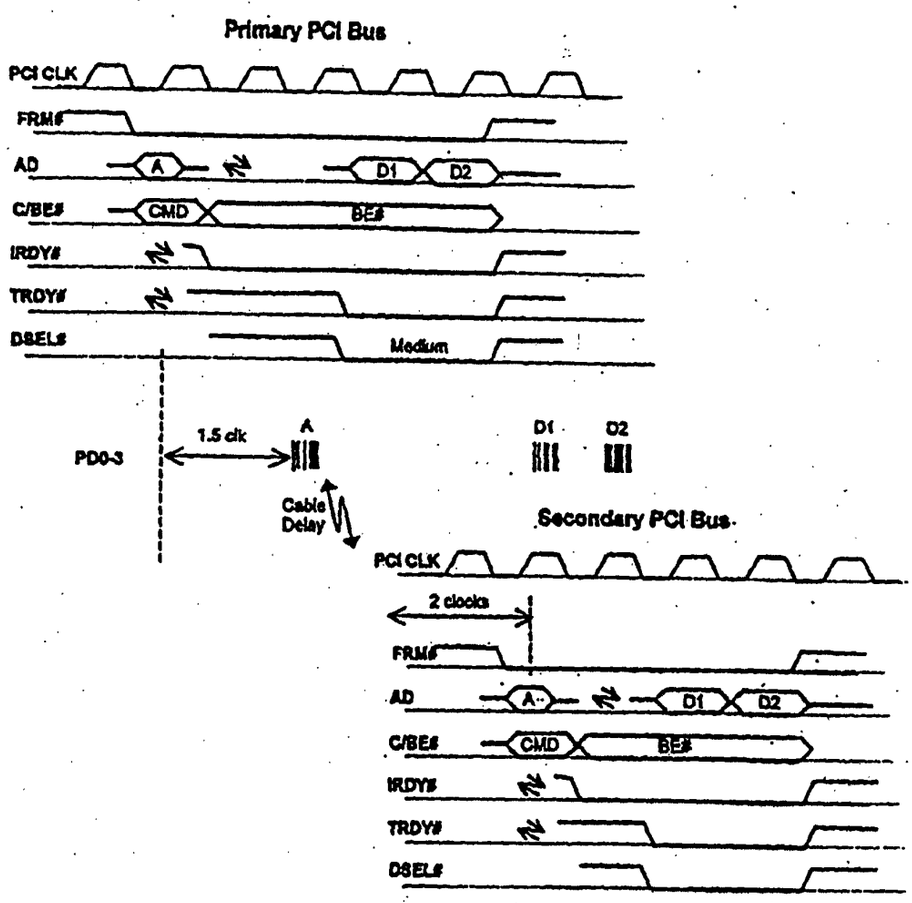


FIGURE 10

INT OF DRAWINGS
; ORIGINALLY FILED

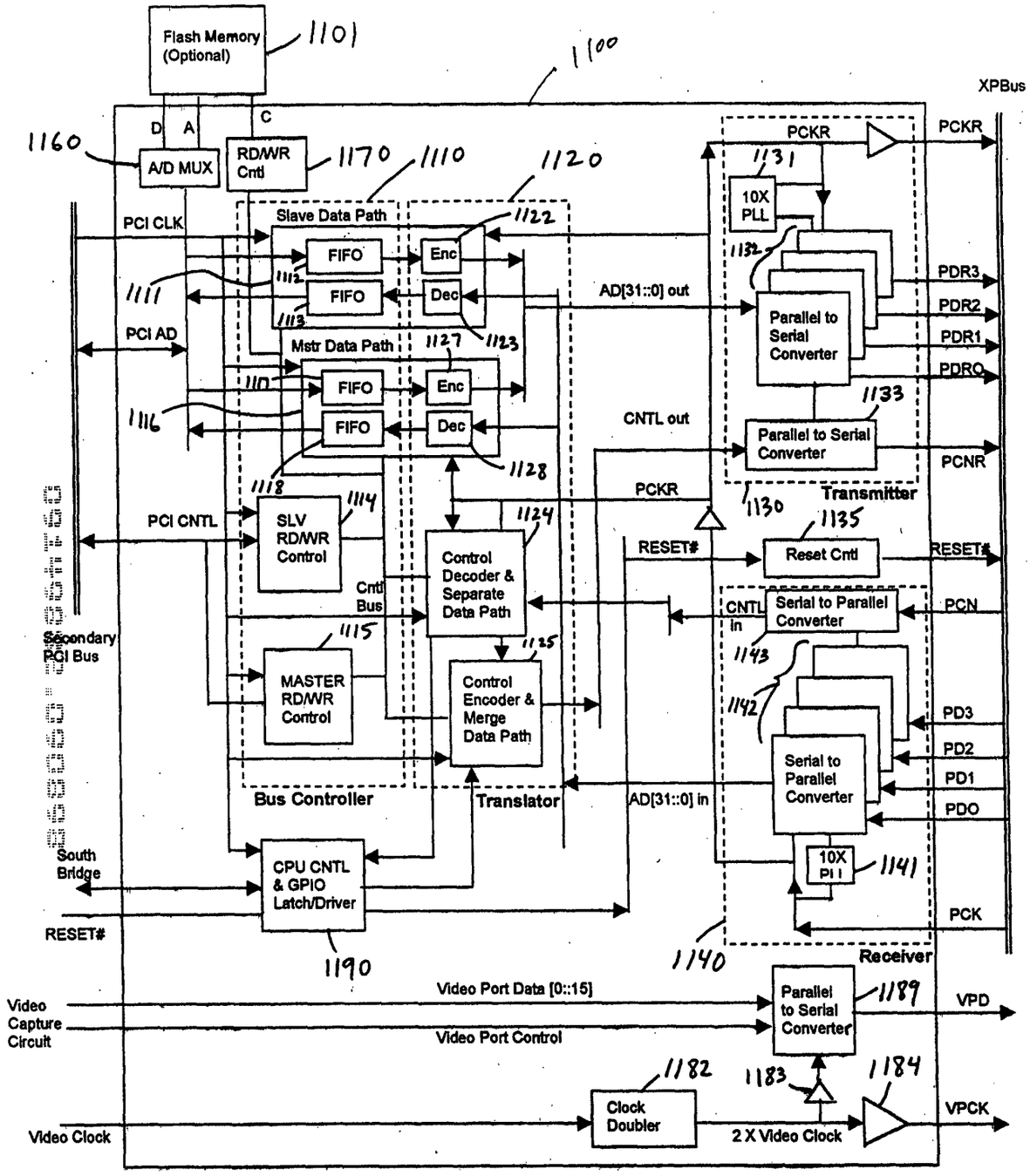


FIGURE 11

RINT OF DRAWINGS
S ORIGINALLY FILED

PIC as Target

Control Signal	PIC to XPBus	XPBus to PIC	Secondary PCI Bus	Comment
FRAME #	Encode (BS0)		Transaction Active	
IRDY #	Encode (BS1)		Initiator Ready	
TRDY #	Local		PIC Generates	
DEVSEL #	Local		PIC Accepts Command	Positive decode, medium
STOP #	Local	Decode	PIC requests to retry	Host can stop trans.
PAR	Encode	Decode	Parity for A/C; D/BE	
IDSEL	Local		Used locally for config. 0	
PERR #	Encode	Decode	Data Parity Error	
SERR #	Encode	Decode	Address/System Parity Error	
REQ #		Decode	PIC requests to be master	P. Bus device requests bus
GNT #	Encode		PIC grants bus to itself	
RST				Independent signal

FIGURE 12

RINT OF DRAWINGS
S ORIGINALLY FILED

PIC as Master (Default)

Control Signal	PIC to XPBus	XPBus to PIC	Secondary PCI Bus	Comment
FRAME #		Decode	Transaction Active	
IRDY #		Decode	Initiator Ready	
TRDY #	Local		Receive from Target	
DEVSEL #	Local		Receive from Target	
STOP #	Local/Encode		Receive from Target	Target can stop trans.
PAR	Encode	Decode	Parity for A/C; D/BE	
IDSEL	Local		Used locally for config. 0	
PERR #	Encode	Decode	Data Parity Error	
SERR #	Encode	Decode	Address/System Parity Error	
REQ #		Decode	PIC request to be Master	
GNT #	Encode		Arbiter grant bus to PIC	
RST				Independent signal

FIGURE 13

INT OF DRAWINGS
; ORIGINALLY FILED

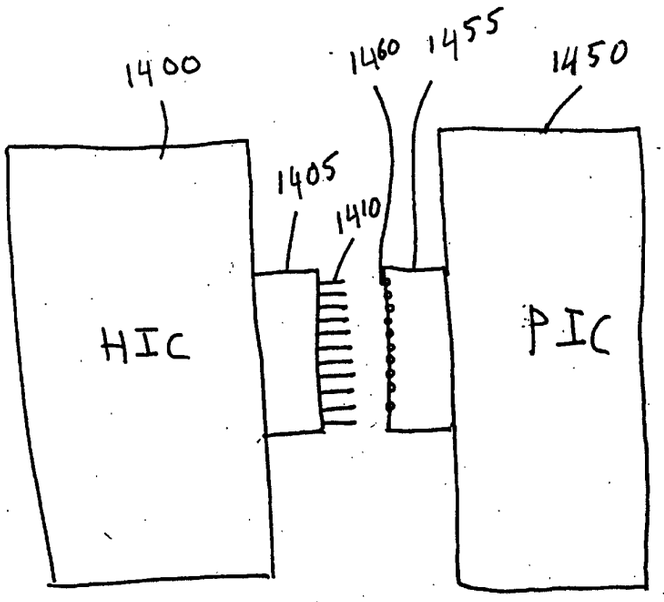


FIGURE 14

INT OF DRAWINGS
S ORIGINALLY FILED

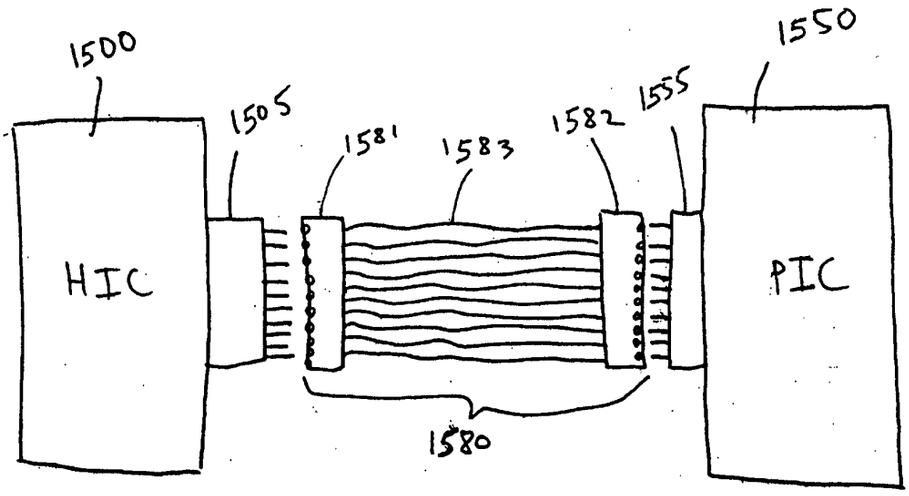


FIGURE 15

05-05-05 : 2:05:04 : 50

NT OF DRAWINGS
ORIGINALLY FILED

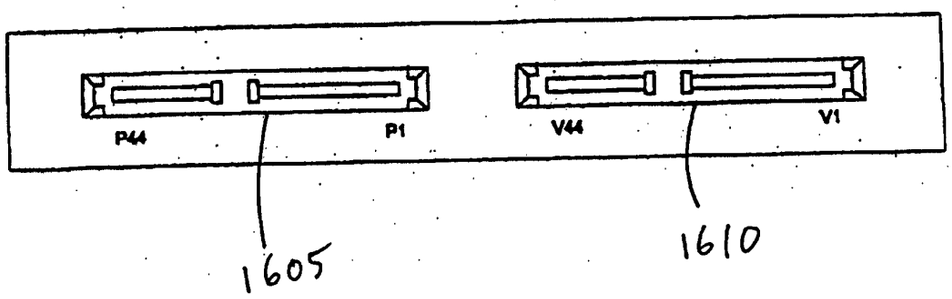


FIGURE 16

IT OF DRAWINGS
ORIGINALLY FILED

ACM's XIS BUS Connector Plug PIN Position (88 pin):

V23	GND	GND	V1		P23	GND	GND	P1
V24	P&D D0 +	RED VIDEO	V2		P24	PD0 +	PDR0 +	P2
V25	P&D D0 -	GND	V3		P25	PD0 -	PDR0 -	P3
V26	GND	GREEN VIDEO	V4		P26	GND	GND	P4
V27	P&D CLK +	GND	V5		P27	PD1 +	PDR1 +	P5
V28	P&D CLK -	BLUE VIDEO	V6		P28	PD1 -	PDR1 -	P6
V29	GND	GND	V7		P29	GND	GND	P7
V30	P&D D1 +	HSYNC	V8		P30	PD2 +	PDR2 +	P8
V31	P&D D1 -	VSYNC	V9		P31	PD2 -	PDR2 -	P9
V32	GND	GND	V10		P32	GND	GND	P10
V33	P&D D2 +	DDC2: SCL	V11		P33	PCK +	PCKR +	P11
V34	P&D D2 -	DDC2: SDA	V12		P34	PCK -	PCKR -	P12
V35	Config 3	Config 2	V13		P35	Config 1	Config 0	P13
V36	GND	TV CV/ CNTL0	V14		P36	GND	GND	P14
V37	VPCK +	SV Y/ CNTL1	V15		P37	PD3 +	PDR3 +	P15
V38	VPCK -	SV C/ CNTL2	V16		P38	PD3 -	PDR3 -	P16
V39	GND	V33	V17		P39	GND	GND	P17
V40	VPD +	V33	V18		P40	PCN +	PCNR +	P18
V41	VPD -	V33	V19		P41	PCN -	PCNR -	P19
V42	GND	V33	V20		P42	Reserved	V5	P20
V43	GND	V33	V21		P43	Reserved	V5	P21
V44	GND	V33	V22		P44	Reserved	V5	P22

FIGURE 17

NT OF DRAWINGS
ORIGINALLY FILED

Pin No.	Symbol	Signal	Standard	Description
P2	PDR0 +	LVDS		Peripheral data reverse 0 +
P3	PDR0 -	LVDS		Peripheral data reverse 0 -
P5	PDR1 +	LVDS		Peripheral data reverse 1 +
P6	PDR1 -	LVDS		Peripheral data reverse 1 -
P8	PDR2 +	LVDS		Peripheral data reverse 2 +
P9	PDR2 -	LVDS		Peripheral data reverse 2 -
P11	PCKR +	LVDS		Peripheral clock reverse +
P12	PCKR -	LVDS		Peripheral clock reverse -
P15	PDR3 +	LVDS		Peripheral data reverse 3 +
P16	PDR3 -	LVDS		Peripheral data reverse 3 -
P18	PCNR +	LVDS		Peripheral control reverse +
P19	PCNR -	LVDS		Peripheral control reverse -
P24	PD0 +	LVDS		Peripheral data 0 +
P25	PD0 -	LVDS		Peripheral data 0 -
P27	PD1 +	LVDS		Peripheral data 1 +
P28	PD1 -	LVDS		Peripheral data 1 -
P30	PD2 +	LVDS		Peripheral data 2 +
P31	PD2 -	LVDS		Peripheral data 2 -
P33	PCK +	LVDS		Peripheral clock +
P34	PCK -	LVDS		Peripheral clock -
P37	PD3 +	LVDS		Peripheral data 3 +
P38	PD3 -	LVDS		Peripheral data 3 -
P40	PCN +	LVDS		Peripheral control +
P41	PCN -	LVDS		Peripheral Control -
P13	Config 0	Static	3.3v or GND	Configuration bit 0
P35	Config 1	Static	3.3v or GND	Configuration bit 1
P1,P4,P7,P10, P14,P17,P23,P26, P29,P32,P36,P39	GND		GND	Ground

FIGURE 18

INT OF DRAWINGS
S ORIGINALLY FILED

Pin No.	Symbol	Signal	Standard	Description
V2	Red Video	Analog		Video
V4	Green Video	Analog		Video
V6	Blue Video	Analog		Video
V8	HSYNC			Horizontal Sync
V9	VSYNC			Vertical Sync
V11	DDC2 SCL		VESA DDC std 2	DDC Clock
V12	DDC2 SDA		VESA DDC std 2	DDC Data
V14	TV-CV/CNTL 0			TV Composite Video
V15	SV Y/CNTL 1		Super Video	SV Luminance or Control 1
V16	SV C/CNTL 2		Super Video	SV Chrominance or Control 2
V24	D0 +	TMDS	VESA P & D	Data 0 +
V25	D0 -	TMDS	VESA P & D	Data 0 -
V27	CLK +	TMDS	VESA P & D	Clock +
V28	CLK -	TMDS	VESA P & D	Clock -
V30	D1 +	TMDS	VESA P & D	Data 1 +
V31	D1 -	TMDS	VESA P & D	Data 1 -
V33	D2 +	TMDS	VESA P & D	Data 2 +
V34	D2 -	TMDS	VESA P & D	Data 2 -
V37	VPCK +	LVDS		Video Port Pixel Clock +
V38	VPCK -	LVDS		Video Port Pixel Clock -
V40	VPD +	LVDS		Video Port Pixel Data +
V41	VPD -	LVDS		Video Port Pixel Data -
V13	Config 2		3.3v or GND	Configuration bit 2
V35	Config 3		3.3v or GND	Configuration bit 3
V1, V3, V5, V7, V10, V23, V26, V29, V32, V36, V39, V42, V43, V44	GND		GND	Ground

FIGURE 19

NT OF DRAWINGS
ORIGINALLY FILED

	Symbol	Signal	Data Rate	Description
1	PD0 RTN			GND
2	PD0 +	Synch. To PCK	10 x clock rate	Computer to Peripheral LVDS Data 0 +
3	PD0 -			Computer to Peripheral LVDS Data 0 -
4	PD1 RTN			GND
5	PD1 +	Synch. To PCK	10 x clock rate	Computer to Peripheral LVDS Data 1 +
6	PD1 -			Computer to Peripheral LVDS Data 1 -
7	PD2 RTN			GND
8	PD2 +	Synch. To PCK	10 x clock rate	Computer to Peripheral LVDS Data 2 +
9	PD2 -			Computer to Peripheral LVDS Data 2 -
10	PD3 RTN			GND
11	PD3 +	Synch. To PCK	10 x clock rate	Computer to Peripheral LVDS Data 3 +
12	PD3 -			Computer to Peripheral LVDS Data 3 -
13	PCK RTN			GND
14	PCK +	Clock	Clock rate	Computer to Peripheral LVDS Clock +
15	PCK -			Computer to Peripheral LVDS Clock -
16	PCN RTN			GND
17	PCN +	Synch. To PCK	10 x clock rate	Computer to Peripheral LVDS Control +
18	PCN -			Computer to Peripheral LVDS Control -
19	PDR0 RTN			GND
20	PDR0 +	Synch. To PCKR	10 x clock rate	Peripheral to Computer LVDS Data 0 +
21	PDR0 -			Peripheral to Computer LVDS Data 0 -
22	PDR1 RTN			GND
23	PDR1 +	Synch. To PCKR	10 x clock rate	Peripheral to Computer LVDS Data 1 +
24	PDR1 -			Peripheral to Computer LVDS Data 1 -
25	PDR2 RTN			GND
26	PDR2 +	Synch. To PCKR	10 x clock rate	Peripheral to Computer LVDS Data 2 +
27	PDR2 -			Peripheral to Computer LVDS Data 2 -
28	PDR3 RTN			GND
29	PDR3 +	Synch. To PCKR	10 x clock rate	Peripheral to Computer LVDS Data 3 +
30	PDR3 -			Peripheral to Computer LVDS Data 3 -
31	PCKR RTN			GND
32	PCKR +	Reverse Dir. Clock	Clock rate	Peripheral to Computer LVDS Clock +
33	PCKR -			Peripheral to Computer LVDS Clock -
34	PCNR RTN			GND
35	PCNR +	Synch. To PCKR	10 x Clock rate	Peripheral to Computer LVDS Control +
36	PCNR -			Peripheral to Computer LVDS Control -
37	RESET#		Asynchronous	Reset

FIGURE 20

INT OF DRAWINGS
S ORIGINALLY FILED

PCK	CK+	CK+	CK+	CK+	CK+	CK-	CK-	CK-	CK-	CK-	CK+	CK+	CK+	CK+	CK+	CK-	CK-	CK-	CK-	CK-
PD0	BS0	CM0#	A00	A01	A02	A03	A04	A05	A06	A07	BS0	BE0#	D00	D01	D02	D03	D04	D05	D06	D07
PD1	BS1	CM1#	A08	A09	A10	A11	A12	A13	A14	A15	BS1	BE1#	D08	D09	D10	D11	D12	D13	D14	D15
PD2	BS2	CM2#	A16	A17	A18	A19	A20	A21	A22	A23	BS2	BE2#	D16	D17	D18	D19	D20	D21	D22	D23
PD3	BS3	CM3#	A24	A25	A26	A27	A28	A29	A30	A31	BS3	BE3#	D24	D25	D26	D27	D28	D29	D30	D31
PCN	CN0	CN1	CN2	CN3	CN4	CN5	CN6	CN7	CN8	CN9	CN0	CN1	CN2	CN3	CN4	CN5	CN6	CN7	CN8	CN9

FIGURE 21

RINT OF DRAWINGS
S ORIGINALLY FILED

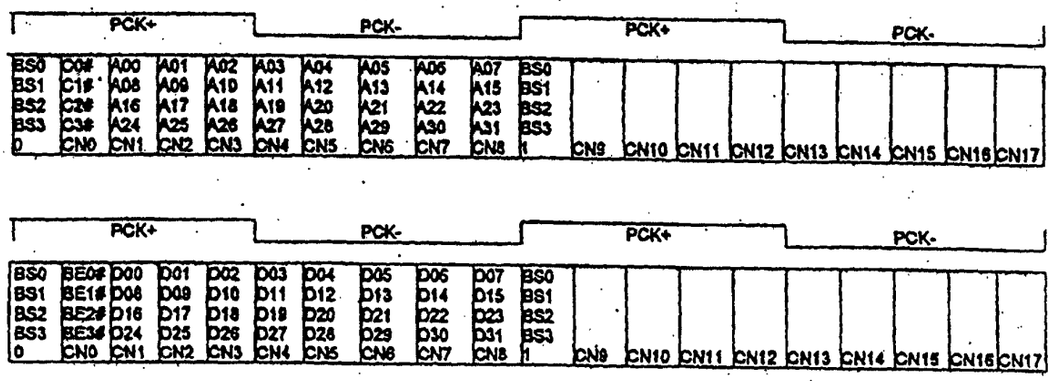


FIGURE 22

UNT OF DRAWINGS
S ORIGINALLY FILED

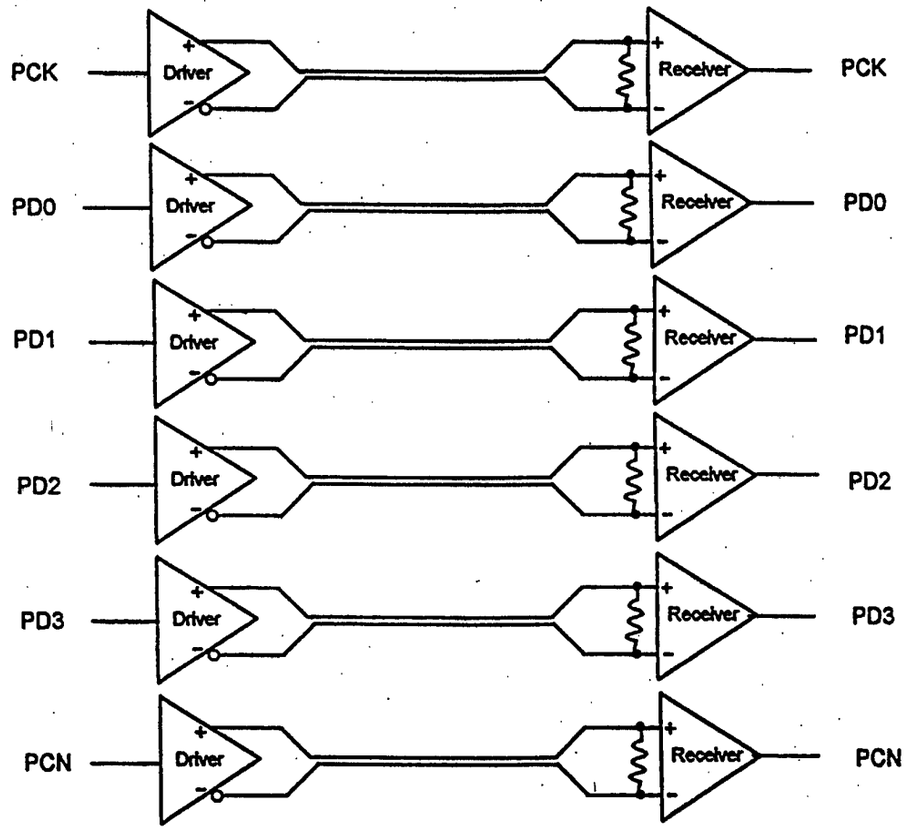


FIGURE 23

INT OF DRAWINGS
ORIGINALLY FILED

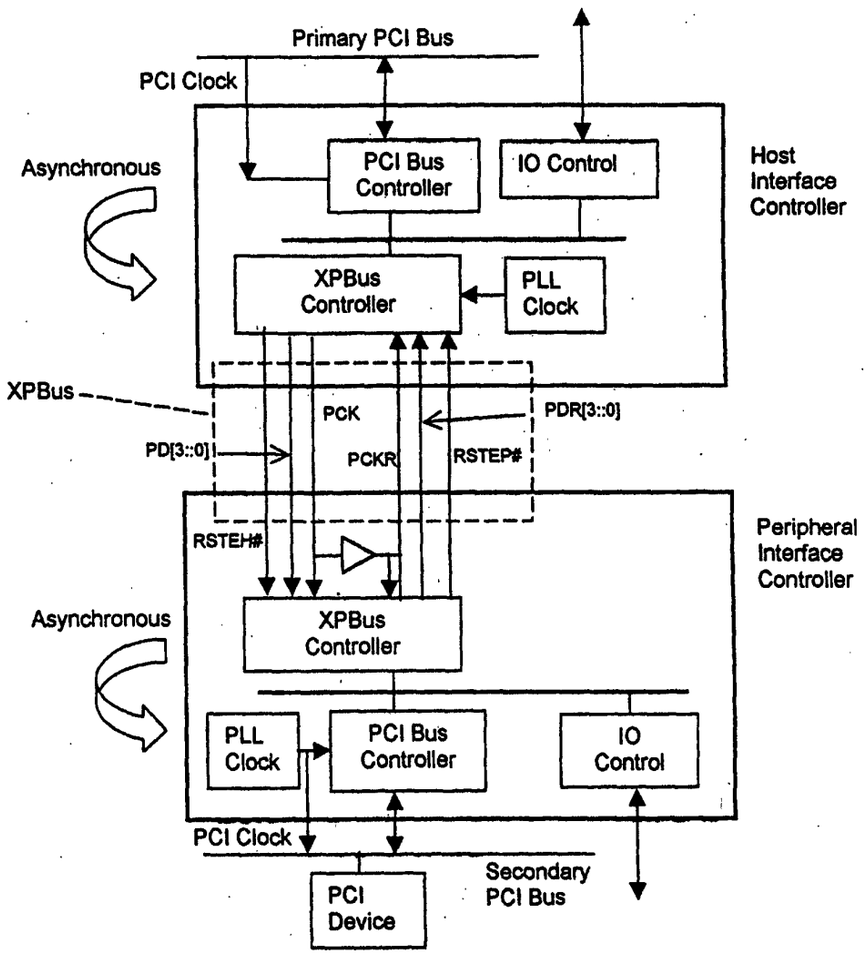


FIGURE 24

INT OF DRAWINGS
S ORIGINALLY FILED

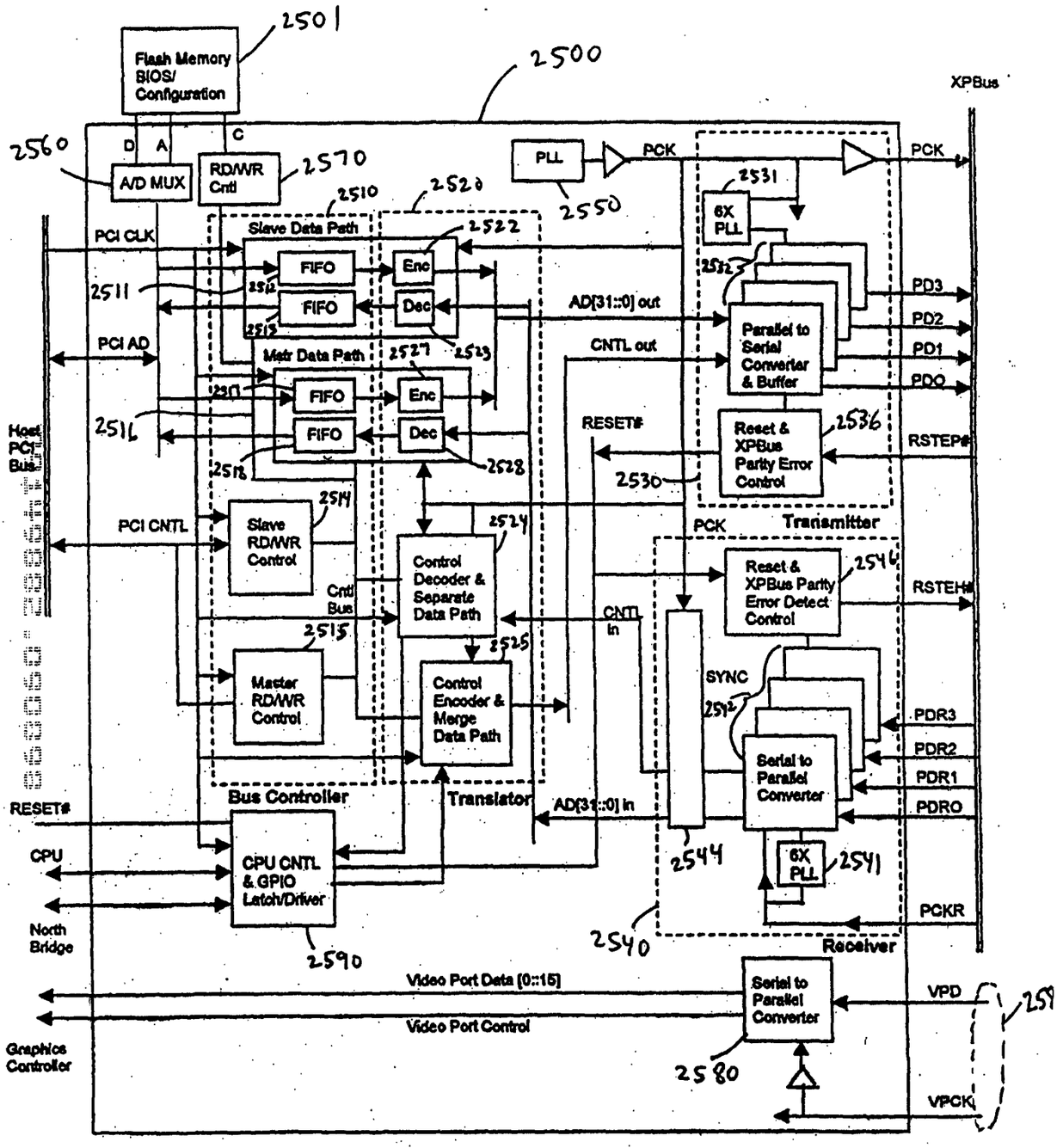


FIGURE 25

PRINT OF DRAWINGS
AS ORIGINALLY FILED

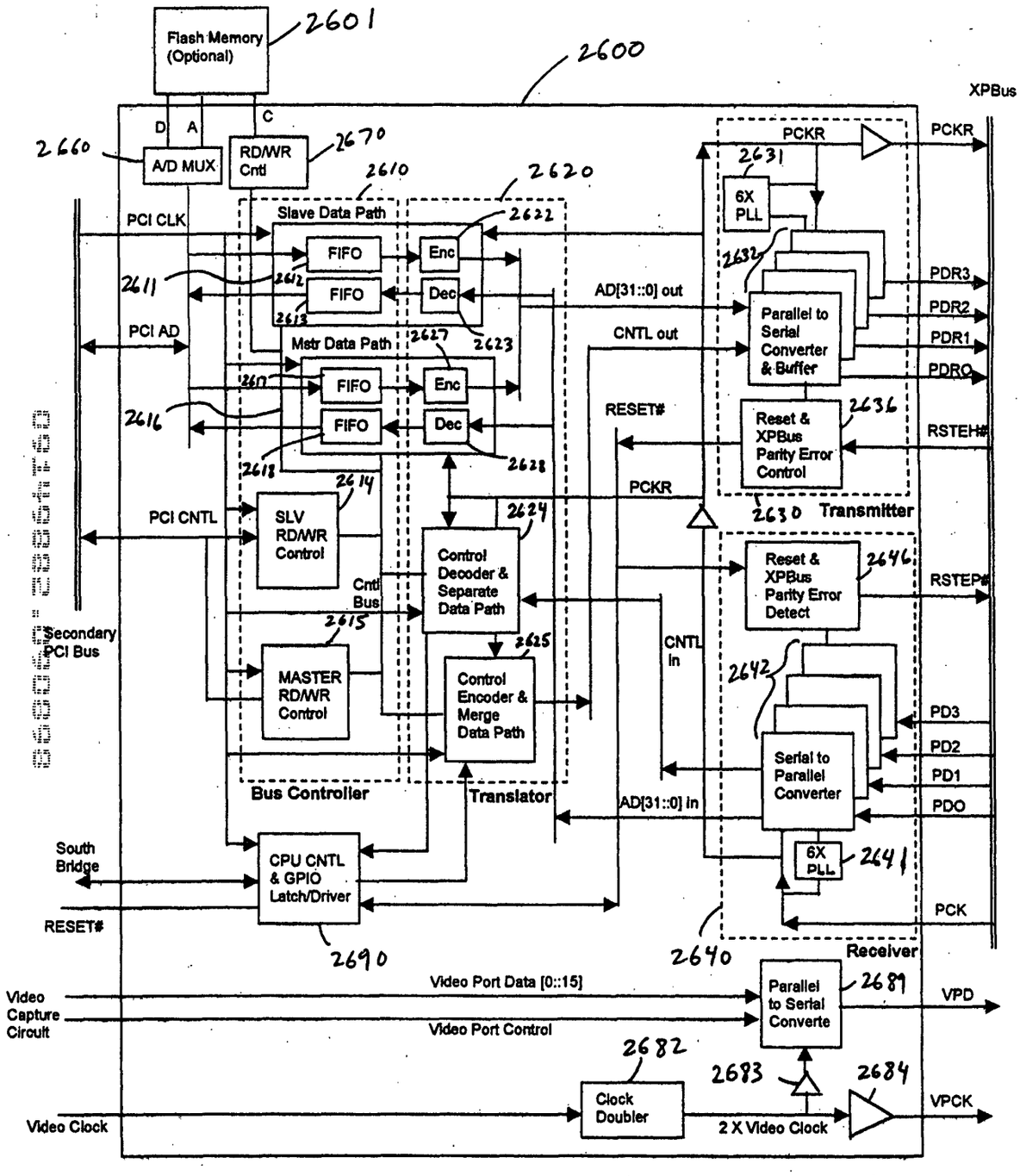


FIGURE 26

OF DRAWINGS
RIGINALLY FILED

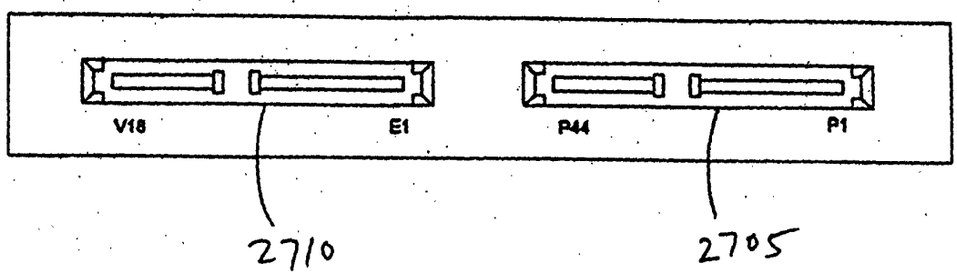


FIGURE 27

PRINT OF DRAWINGS
AS ORIGINALLY FILED

ACM's CMI BUS Connector Plug PIN Position (88 pin):

E14	GND	GND	E1		P23	GND	GND	P1
E15	P&D D0 +	VPD+/TPA+	E2		P24	PD0 +	PDR0 +	P2
E16	P&D D0 -	VPD-/TPA-	E3		P25	PD0 -	PDR0 -	P3
E17	GND	GND	E4		P26	GND	GND	P4
E18	P&D CLK +	VPCK+/TPB+	E5		P27	PD1 +	PDR1 +	P5
E19	P&D CLK -	VPCK-/TPB-	E6		P28	PD1 -	PDR1 -	P6
E20	GND	Reserved	E7		P29	GND	GND	P7
E21	P&D D1 +	Reserved	E8		P30	PD2 +	PDR2 +	P8
E22	P&D D1 -	Reserved	E9		P31	PD2 -	PDR2 -	P9
E23	GND	Reserved	E10		P32	GND	GND	P10
E24	P&D D2 +	Reserved	E11		P33	PCK +	PCKR +	P11
E25	P&D D2 -	Reserved	E12		P34	PCK -	PCKR -	P12
E26	Config 3	Config 2	E13		P35	Config 1	Config 0	P13
V10	GND	V33	V1		P36	GND	GND	P14
V11	GND	V33	V2		P37	PD3 +	PDR3 +	P15
V12	GND	V33	V3		P38	PD3 -	PDR3 -	P16
V13	V33	V33	V4		P39	RSTEH#	RSTEP#	P17
V14	V33	V33	V5		P40	GREEN VIDEO	RED VIDEO	P18
V15	V33	V33	V6		P41	GND	GND	P19
V16	V5	V12	V7		P42	HSYNC	BLUE VIDEO	P20
V17	V5	V12	V8		P43	VSYNC	GND	P21
V18	V5	V12	V9		P44	DDC2: SCL	DDC2: SDA	P22

FIGURE 28

OF DRAWINGS
UGINALLY FILED

Pin No.	Symbol	Signal	Standard	Description
P2	PDR0 +	LVDS		Peripheral data reverse 0 +
P3	PDR0 -	LVDS		Peripheral data reverse 0 -
P5	PDR1 +	LVDS		Peripheral data reverse 1 +
P6	PDR1 -	LVDS		Peripheral data reverse 1 -
P8	PDR2 +	LVDS		Peripheral data reverse 2 +
P9	PDR2 -	LVDS		Peripheral data reverse 2 -
P11	PCKR +	LVDS		Peripheral clock reverse +
P12	PCKR -	LVDS		Peripheral clock reverse -
P15	PDR3 +	LVDS		Peripheral data reverse 3 +
P16	PDR3 -	LVDS		Peripheral data reverse 3 -
P24	PD0 +	LVDS		Peripheral data 0 +
P25	PD0 -	LVDS		Peripheral data 0 -
P27	PD1 +	LVDS		Peripheral data 1 +
P28	PD1 -	LVDS		Peripheral data 1 -
P30	PD2 +	LVDS		Peripheral data 2 +
P31	PD2 -	LVDS		Peripheral data 2 -
P33	PCK +	LVDS		Peripheral clock +
P34	PCK -	LVDS		Peripheral clock -
P37	PD3 +	LVDS		Peripheral data 3 +
P38	PD3 -	LVDS		Peripheral data 3 -
P13	Config 0	Static	3.3v or GND	Configuration bit 0
P35	Config 1	Static	3.3v or GND	Configuration bit 1
P17	RESTEP#	TTL	3.3v	Reset and Parity Error from console to ACM
P39	RESTEH#	TTL	3.3v	Reset and Parity Error from ACM to console
P18	Red Video	Analog		Video
P40	Green Video	Analog		Video
P20	Blue Video	Analog		Video
P42	HSYNC	TTL		Horizontal Sync
P43	VSYNC	TTL		Vertical Sync
P44	DDC2 SCL	TTL	VESA DDC std 2	DDC Clock
P22	DDC2 SDA	TTL	VESA DDC std 2	DDC Data
P1,P4,P7,P10, P14,P19,P21, P23,P26,P29, P32,P36,P41	GND		GND	Ground

FIGURE 29

OF DRAWINGS
RIGINALLY FILED

Pin No.	Symbol	Signal	Standard	Description
E2	VPD+/TPA+		LVDS or 1394	Video capture port data or 1394
E3	VPD-/TPA-		LVDS or 1394	Video capture port data or 1394
E5	VPCK+/TPA+		LVDS or 1394	Video capture port data or 1394
E6	VPCK-/TPA-		LVDS or 1394	Video capture port data or 1394
E15	D0 +	TMDS	VESA P & D	Data 0 +
E16	D0 -	TMDS	VESA P & D	Data 0 -
E18	CLK +	TMDS	VESA P & D	Clock +
E19	CLK -	TMDS	VESA P & D	Clock -
E21	D1 +	TMDS	VESA P & D	Data 1 +
E22	D1 -	TMDS	VESA P & D	Data 1 -
E24	D2 +	TMDS	VESA P & D	Data 2 +
E25	D2 -	TMDS	VESA P & D	Data 2 -
E13	Config 2			Configuration bit 2
E26	Config 3			Configuration bit 3
E1, E4, E14, E17,E20,E23	GND		GND	Ground

E7	Reserved			Reserved
E8	Reserved			Reserved
E9	Reserved			Reserved
E10	TV-CV/reserved		NTSC	TV Composite Video or reserved
E11	SV Y/reserved		Super Video	SV Luminance or reserved
E12	SV C/reserved		Super Video	SV Chrominance or reserved

FIGURE 30

T OF DRAWINGS
RIGINALLY FILED

	Symbol	Signal	Data Rate	Description
1	PD0 RTN			GND
2	PD0 +	Synch. To PCK	6 x clock rate	Computer to Peripheral LVDS Data 0 +
3	PD0 -			Computer to Peripheral LVDS Data 0 -
4	PD1 RTN			GND
5	PD1 +	Synch. To PCK	6 x clock rate	Computer to Peripheral LVDS Data 1 +
6	PD1 -			Computer to Peripheral LVDS Data 1 -
7	PD2 RTN			GND
8	PD2 +	Synch. To PCK	6 x clock rate	Computer to Peripheral LVDS Data 2 +
9	PD2 -			Computer to Peripheral LVDS Data 2 -
10	PD3 RTN			GND
11	PD3 +	Synch. To PCK	6 x clock rate	Computer to Peripheral LVDS Data 3 +
12	PD3 -			Computer to Peripheral LVDS Data 3 -
13	PCK RTN			GND
14	PCK +	Clock	Clock rate	Computer to Peripheral LVDS Clock +
15	PCK -			Computer to Peripheral LVDS Clock -
16	PDR0 RTN			GND
17	PDR0 +	Synch. To PCKR	6 x clock rate	Peripheral to Computer LVDS Data 0 +
18	PDR0 -			Peripheral to Computer LVDS Data 0 -
19	PDR1 RTN			GND
20	PDR1 +	Synch. To PCKR	6 x clock rate	Peripheral to Computer LVDS Data 1 +
21	PDR1 -			Peripheral to Computer LVDS Data 1 -
22	PDR2 RTN			GND
23	PDR2 +	Synch. To PCKR	6 x clock rate	Peripheral to Computer LVDS Data 2 +
24	PDR2 -			Peripheral to Computer LVDS Data 2 -
25	PDR3 RTN			GND
26	PDR3 +	Synch. To PCKR	6 x clock rate	Peripheral to Computer LVDS Data 3 +
27	PDR3 -			Peripheral to Computer LVDS Data 3 -
28	PCKR RTN			GND
29	PCK +	Reverse Dir. Clock	Clock rate	Peripheral to Computer LVDS Clock +
30	PCK -			Peripheral to Computer LVDS Clock -
31	RESTEH#	Host to Peripheral	asynchronous	Reset & Error signal
32	RESTEP#	Peripheral to Host	asynchronous	Reset & Error signal

FIGURE 31

T OF DRAWINGS
RIGINALLY FILED

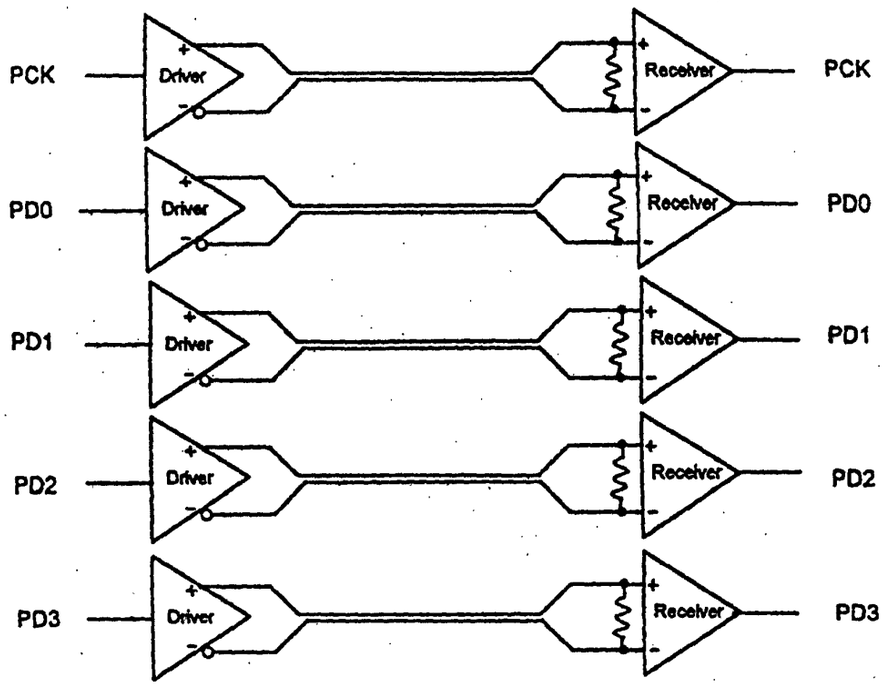


FIGURE 32

OF DRAWINGS
RIGINALLY FILED

Master	Type	HMA1/HMD1	HMA2/HMD2	HMC1	HMC2	Resvd	NOOP
	1st nibble	XX00 (PCI)	XX10 (PCI)	1001 (Control)	1101 (Control)	X011	1111
	2nd nibble	C/BE	Control bits	Control bits	Control bits		
	3rd to 6th	PCI A/D 1st seg.	PCI A/D 2nd seg.	Control 1st seg.	Control 2nd seg.	Other	Void
Target	Type	HTD1	HTD2	HTC1	HTC2	Resrd	NOOP
	1st nibble	XX00	XX10	0001 (Control)	0101 (Control)	X011	1111
	2nd nibble	BE	Control bits	Control bits	Control bits		
	3rd to 6th	PCI D 1st seg.	PCI D 2nd seg.	Control 1st seg.	Control 2nd seg.	Other	Void

FIGURE 33

RINT OF DRAWINGS
S ORIGINALLY FILED

Master	Type	PMA1 / PMD1	PMA2 / PMD2	PMC1	PMC2	Resvd	NOOP
	1st nibble	XX00 (PCI)	XX10 (PCI)	X001(Control)	X101(Control)	X011	1111
	2nd nibble	C/BE	Control bits	Control bits	Control bits		
	3rd to 6th	PCI A/D 1st seg.	PCI A/D 2nd seg.	Control 1st seg.	Control 2nd seg.	Other	Void
Target	Type	PTD1	PTD2	PTC1	PTC2	Resvd	NOOP
	1st nibble	XX00	XX10	X001(Control)	X101 (Control)	X011	1111
	2nd nibble	BE	Control bits	Control bits	Control bits		
	3rd to 6th	PCI D 1st seg.	PCI D 2nd seg.	Control 1st seg.	Control 2nd seg.	Other	Void

FIGURE 34

RINT OF DRAWINGS
AS ORIGINALLY FILED

ID bits (P0 P1 P2 P3)	Data Packet Type
X X 0 0	PCI 1st address/data segment
X X 1 0	PCI 2nd address/data segment
0 0 0 1	Control 1st segment with PCI response
1 0 0 1	Control 1st segment without PCI response
0 1 0 1	Control 2nd segment with PCI response
1 1 0 1	Control 2nd segment without PCI response
0 0 1 1	Reserved
1 0 1 1	Reserved
0 1 1 1	Initialization
1 1 1 1	NOOP

FIGURE 35

RINT OF DRAWINGS
S ORIGINALLY FILED

	PD0	PD1	PD2	PD3
1st control /ID (HMA1 or HMD1)	FRAME#	IRDY#	0: 1st data seg.	0: PCI; Other=1
2nd control	C/BE0#	C/BE1#	C/BE2#	C/BE3#
1st Data Segment	A/D0	A/D8	A/D16	A/D24
1st Data Segment	A/D1	A/D9	A/D17	A/D25
1st Data Segment	A/D2	A/D10	A/D18	A/D26
1st Data Segment	A/D3	A/D11	A/D19	A/D27
3rd control /ID (HMA2 or HMD2)	PAR (PCI)	LOCK#	1: 2nd data seg.	0: PCI; Other=1
4th control	GNT#	reserved	reserved	Cmd PAR (CMI)
2nd Data Segment	A/D4	A/D12	A/D20	A/D28
2nd Data Segment	A/D5	A/D13	A/D21	A/D29
2nd Data Segment	A/D6	A/D14	A/D22	A/D30
2nd Data Segment	A/D7	A/D15	A/D23	A/D31

FIGURE 36

NT OF DRAWINGS
ORIGINALLY FILED

	PD0	PD1	PD2	PD3
1st control /ID (PMA1 or PMD1)	FRAME#	IRDY#	0: 1st data seg.	0: PCI; Other=1
2nd control	C/BE0#	C/BE1#	C/BE2#	C/BE3#
1st Data Segment	A/D0	A/D8	A/D16	A/D24
1st Data Segment	A/D1	A/D9	A/D17	A/D25
1st Data Segment	A/D2	A/D10	A/D18	A/D26
1st Data Segment	A/D3	A/D11	A/D19	A/D27
3rd control /ID (PMA2 or PMD2)	PAR (PCI)	LOCK#	1: 2nd data seg.	0: PCI; Other=1
4th control	GNT#	reserved	reserved	Cntl PAR (CMI)
2nd Data Segment	A/D4	A/D12	A/D20	A/D28
2nd Data Segment	A/D5	A/D13	A/D21	A/D29
2nd Data Segment	A/D6	A/D14	A/D22	A/D30
2nd Data Segment	A/D7	A/D15	A/D23	A/D31

FIGURE 37

RINT OF DRAWINGS
S ORIGINALLY FILED

	PD0	PD1	PD2	PD3
1st control /ID (HTD1 or PTD1)	1	1	0: 1st data seg.	0: PCI; Other=1
2nd control	reserved	reserved	reserved	reserved
1st Data Segment	D0	D8	D16	D24
1st Data Segment	D1	D9	D17	D25
1st Data Segment	D2	D10	D18	D26
1st Data Segment	D3	D11	D19	D27
3rd control /ID (HTD2 or PTD2)	PAR (PCI)	reserved	1: 2nd data seg.	0: PCI; Other=1
4th control	GNT#	reserved	reserved	Cntl PAR (CMI)
2nd Data Segment	D4	D12	D20	D28
2nd Data Segment	D5	D13	D21	D29
2nd Data Segment	D6	D14	D22	D30
2nd Data Segment	D7	D15	D23	D31

FIGURE 38

NT OF DRAWINGS
ORIGINALLY FILED

33Mhz PCI Read transaction:

H > P	HMA1	HMA2	NOOP	NOOP	.....	.....	NOOP	NOOP	HMC1	NOOP
P > H	NOOP	NOOP	PTC1	NOOP	.....:	.....	PTD1	PTD2	NOOP	NOOP

FIGURE 39

T OF DRAWINGS
)RIGINALLY FILED

33 Mhz PCI Write transaction:

H > P	HMA1	HMA2	NOOP	NOOP	HMD1	HMD2	NOOP	NOOP	HMD1	HMD2	NOOP
P > H	NOOP	NOOP	PTC1	NOOP	NOOP	NOOP	PTC2	NOOP	NOOP	NOOP	PTC1

FIGURE 40

NT OF DRAWINGS
ORIGINALLY FILED

Peripheral to Host: PCI Target (on XPBus) Control data packets with PCI response :

	PD0	PD1	PD2	PD3
ID (PTC1)	0: PCI	0: 1st control seg.	0: Control	1: Other
PCI Control Segment	PERR#	SERR#	REQ#	STOP#
CMI Control Segment	CMI PERR#	Buffer Full #	CMI REQ#	CMI GNT#
CPU 1st Control Segment	CPURST	INIT	reserved	reserved
CPU 2nd Control Segment	INTR	NMI	A20M#	IGNNE#
CPU 3rd Control Segment	SMI#	STPCLK#	SLP#	PAR (Cntl Packet)

ID (PTC2)	0: PCI	1: 2nd control seg.	0: Control	1: Other
PCI Control Segment	PERR#	SERR#	REQ#	STOP#
CMI Control Segment	CMI PERR#	Buffer Full #	CMI REQ#	CMI GNT#
NB 1st Control Segment	SUSCLK	SUSSTAT1#	PHOLD#	
GPIO 1st Control Segment	GPIO (0)	GPIO (1)	GPIO (2)	GPIO (3)
GPIO 2nd Control Segment	GPIO (4)	GPIO (5)	reserved	PAR (Cntl Packet)

FIGURE 41

OF DRAWINGS
GINALLY FILED

Peripheral to Host: PCI Target (on XPBus) Control data packets without PCI response :

	PD0	PD1	PD2	PD3
ID (PTC1)	1: No PCI	0: 1st control seg.	0: Control	1: Other
PCI Control Segment	reserved	reserved	reserved	reserved
CMI Control Segment	CMI PERR#	Buffer Full #	CMI REQ#	CMI GNT#
CPU 1st Control Segment	CPURST	INIT	reserved	reserved
CPU 2nd Control Segment	INTR	NMI	A20M#	IGNNE#
CPU 3rd Control Segment	SMI#	STPCLK#	SLP#	PAR (Cntl Packet)

ID (PTC2)	1: No PCI	1: 2nd control seg.	0: Control	1: Other
PCI Control Segment	reserved	reserved	reserved	reserved
CMI Control Segment	CMI PERR#	Buffer Full #	CMI REQ#	CMI GNT#
NB 1st Control Segment	SUSCLK	SUSSTAT1#	PHOLD#	
GPIO 1st Control Segment	GPIO (0)	GPIO (1)	GPIO (2)	GPIO (3)
GPIO 2nd Control Segment	GPIO (4)	GPIO (5)	reserved	PAR (Cntl Packet)

FIGURE 42

INT OF DRAWINGS
ORIGINALLY FILED

Peripheral to Host: PCI Master (on XPBus) Control data packets with PCI response:

	PD0	PD1	PD2	PD3
ID (PMC1)	0: PCI	0: 1st control seg.	0: Control	1: Other
PCI Control Segment	PERR#	SERR#	reserved	reserved
CMI Control Segment	CMI PERR#	Buffer Full #	CMI REQ#	CMI GNT#
CPU 1st Control Segment	CPURST	INIT	reserved	reserved
CPU 2nd Control Segment	INTR	NMI	A20M#	IGNNE#
CPU 3rd Control Segment	SMI#	STPCLK#	SLP#	PAR (Cntl Packet)

ID (PMC2)	0: PCI	1: 2nd control seg.	0: Control	1: Other
PCI Control Segment	PERR#	SERR#	reserved	reserved
CMI Control Segment	CMI PERR#	Buffer Full #	CMI REQ#	CMI GNT#
NB 1st Control Segment	SUSCLK	SUSSTAT1#	PHOLD#	reserved
GPIO 1st Control Segment	GPIO (0)	GPIO (1)	GPIO (2)	GPIO (3)
GPIO 2nd Control Segment	GPIO (4)	GPIO (5)	reserved	PAR (Cntl Packet)

FIGURE 43

INT OF DRAWINGS
; ORIGINALLY FILED

Peripheral to Host: PCI Master (on XPBus) Control data packets without PCI response:

	PD0	PD1	PD2	PD3
ID (PMC1)	1: No PCI	0: 1st control seg.	0: Control	1: Other
PCI Control Segment	reserved	reserved	reserved	reserved
CMI Control Segment	CMI PERR#	Buffer Full #	CMI REQ#	CMI GNT#
CPU 1st Control Segment	CPURST	INIT	reserved	reserved
CPU 2nd Control Segment	INTR	NMI	A20M#	IGNNE#
CPU 3rd Control Segment	SMI#	STPCLK#	SLP#	PAR (Cntl Packet)

ID (PMC2)	1: No PCI	1: 2nd control seg.	0: Control	1: Other
PCI Control Segment	reserved	reserved	reserved	reserved
CMI Control Segment	CMI PERR#	Buffer Full #	CMI REQ#	CMI GNT#
NB 1st Control Segment	SUSCLK	SUSSTAT1#	PHOLD#	reserved
GPIO 1st Control Segment	GPIO (0)	GPIO (1)	GPIO (2)	GPIO (3)
GPIO 2nd Control Segment	GPIO (4)	GPIO (5)	reserved	PAR (Cntl Packet)

FIGURE 44

RINT OF DRAWINGS
S ORIGINALLY FILED

Host to Peripheral: Target Control data packet :

	PD0	PD1	PD2	PD3
ID (HTC1)	0: PCI Target	0: 1st segment	0: Control	1: Other
PCI Control Segment	PERR#	SERR#	REQ#	STOP#
CMI Control Segment	CMI PERR#	Buffer Full #	CMI REQ#	CMI GNT#
CPU 1st Control Segment	FERR#	reserved	reserved	reserved
Reserved				
Reserved				

HTC2 is reserved for future use.

FIGURE 45

NT OF DRAWINGS
ORIGINALLY FILED

Host to Peripheral: Master Control data packet :

	PD0	PD1	PD2	PD3
ID (HMC1)	1: PCI Master	0: 1st segment	0: Control	1: Other
PCI Control Segment	PERR#	SERR#	reserved	reserved
CMI Control Segment	CMI PERR#	Buffer Full #	CMI REQ#	CMI GNT#
CPU 1st Control Segment	FERR#	reserved	reserved	reserved
Reserved				
Reserved				

HMC2 is reserved for future use.

FIGURE 46

RINT OF DRAWINGS
S ORIGINALLY FILED

Host PCI Bus Signal (50 pins)

Name	Type	Pins	Description
AD[31::0]	TS	32	Multiplexed Address/Data. AD is driven to a valid state when GNT# is asserted.
C/BE[3::0]#	TS	4	Multiplexed Command/Byte Enables. For a two-address transaction, 1st address phase carries the command, and the 2nd address phase carries the transaction type. C/BE is driven to a valid state when GNT# is asserted.
FRAME#	STS	1	Indicates beginning and duration of a PCI transaction. When the bus is idle, FRAME# is driven to High for 1 cycle. A pull-up resistor sustains STS signal.
IRDY#	STS	1	Initiator Ready. IRDY# is driven High for 1 cycle if bus is idle, and the state is sustained by a pull-up resistor.
TRDY#	STS	1	Target Ready. When bus is idle, TRDY# is driven High for 1 cycle if bus is idle. An external pull-up resistor sustains STS signal.
DEVSEL#	STS	1	Device Select. DEVSEL# is asserted by target to indicate it is ready to accept the transaction. HIC decodes address of a transaction to decide the need to assert DEVSEL#. As an initiator, HIC waits for 5 cycles to detect assertion of DEVSEL# by the target; otherwise HIC terminates with a master abort. DEVSEL# is driven High for 1 cycle when bus is idle, and the state is sustained by a pull-up resistor.
STOP#	STS	1	Target request to stop transaction. There are 3 cases: STOP#, TRDY# & DEVSEL# asserted: disconnect with data transfer Only STOP# & DEVSEL# asserted: request initiator to retry later Only STOP# asserted: target abort STOP# is driven High for 1 cycle when bus is idle, and the state is sustained by a pull-up resistor.
PAR	TS	1	Even parity for 36 bits of AD & C/BE#. PAR is sent one cycle after address or data is valid. In write transaction, initiator sends PAR one cycle after write data is valid. In read transaction, target sends PAR one cycle after read data is valid.
LOCK#	Input	1	Initiator request lock on target downstream. LOCK# is asserted 1 clock cycle after address phase by an initiator wanting to perform an atomic operation that take more than one transaction to complete. HIC passes the LOCK# request to the secondary PCI bus. HIC does not drive LOCK# or propagate LOCK# upstream.
IDSEL#	Input	1	Chip Select for Type 0 configuration access. During a Type 0 configuration transaction, the initiator asserts IDSEL# during the address phase to select HIC. HIC responds by asserting DEVSEL#.
PERR#	STS	1	Data Parity Error on all transactions except Special Cycle. PERR# is driven one clock cycle after PAR. PERR# is asserted by target during write transactions, and by initiator during read transactions.
SERR#	OD	1	System Error. HIC asserts SERR# under the following conditions: Address parity error, Secondary bus SERR# asserted, Posted write transaction: data parity error on target bus, Posted write transaction discarded, Master abort, Target abort Delayed read or write transaction discarded, and Delayed transaction master timeout.
REQ#	TS	1	Request for bus. If a target retry or disconnect is received in response to initiating a transaction, HIC deasserts REQ# for at least 2 cycles before asserting it again.
GNT#	Input	1	Bus is granted to HIC. HIC can initiate transaction if GNT# is asserted and the bus is idle. When HIC is not requesting bus and GNT# is asserted, HIC must drive AD, C/BE, and PAR to valid logic levels.
CLKRUN#	I/OD	1	Input indicating clock status. HIC can request the central clock resource to start, speed up or maintain the PCI clock. There are 3 clocking states: Clock running, Clock about to stop/slow down, and Clock stopped/slowed.
PCICK	Input	1	PCI Clock. All inputs are sampled on the rising edge of PCICK. Frequency range from 0 to 33Mhz.

FIGURE 47

RINT OF DRAWINGS
AS ORIGINALLY FILED

XPBus Signals

Name	Type	Pins	Description
PCK ±	LVDS Output	2	Peripheral Clock Differential Signal Pair Output to XPBus
PD{3::0] ±	LVDS Output	8	Peripheral Data Differential Signal Pair Output to XPBus
PCN ±	LVDS Output	2	Peripheral Control Differential Signal Pair Output to XPBus
PCKR ±	LVDS Input	2	Peripheral Clock Differential Signal Pair Input from XPBus
PDR{3::0] ±	LVDS Input	8	Peripheral Data Differential Signal Pair Input from XPBus
PCNR ±	LVDS Input	2	Peripheral Control Differential Signal Pair Input from XPBus

FIGURE 48

RINT OF DRAWINGS
AS ORIGINALLY FILED

XIS Bus Video Port Signals

Name	Type	Pins	Description
VPCK ±	LVDS Input	2	Video Port Clock Differential Signal Pair Input; 2 x Video clock rate
PCK ±	LVDS Output	2	Video Port Data Differential Signal Pair Input; 10 bit/clock period

FIGURE 49

INT OF DRAWINGS
S ORIGINALLY FILED

Video Port Signals

Name	Type	Pins	Description
VPD [15::0]	Output	16	Video Port Data Output
VREF	Output	1	Vertical Reference
HREF	Output	1	Horizontal Reference
VCLK	Output	1	Video Pixel Clock
VRDY	Output	1	Video Source Ready

FIGURE 50

INT OF DRAWINGS
S ORIGINALLY FILED

Test Port (JTAG) Signals

Name	Type	Pins	Description
TCK	I	1	Test Clock
TDI	I	1	Test Data In
TDO	O	1	Test Data Out
TMS	I	1	Test Mode Select

FIGURE 52.

INT OF DRAWINGS
S ORIGINALLY FILED

CPU Signals

Name	Type	Pins	Description
CPURST	I/OD	1	CPU Reset and PCI RST#
FERR#	I	1	Numeric Coprocessor Error
IGNNE#	OD	1	Ignore Numeric Exception
INIT	OD	1	Initialization
INTR	OD	1	CPU Interrupt; Pentium: active high; PII active low
A20M#	OD	1	Address 20 Mask; Keyboard Interface
NMI	OD	1	Non-Maskable Interrupt
SMI#	OD	1	System Management Interrupt
STPCLK#	OD	1	Stop Clock
SLP#	OD	1	Sleep

FIGURE 53

INT OF DRAWINGS
ORIGINALLY FILED

North Bridge Signals

Name	Type	Pins	Description
SUSCLK	O	1	Suspend Clock from South Bridge. 32.768Khz for maintenance of DRAM Refresh.
SUSSTAT1#	O	1	Suspend Status Plane 1
PHOLD#	O	1	PCI Hold
PHLDA#	I	1	PCI Hold Acknowledge

FIGURE 54

T OF DRAWINGS
RIGINALLY FILED

GPIO Signals

Name	Type	Pins	Description
GPIO[0]	O	1	CPU_STP# - CPU Clock Stop (optional)
GPIO[1]	O	1	PCI_STP# - PCI Clock Stop (optional)
GPIO[7::2]	I/O	6	General Purpose Input/Output Signals

FIGURE 55

PRINT OF DRAWINGS
AS ORIGINALLY FILED

ERROR/RESET Signals

Name	Type	Pins	Description
RSTEH	O	1	Signal uses for: Reset from Host, Parity error for PIC transmission, & no connect detection
RSTEP	I	1	Signal uses for: Reset from Peripheral, Parity error for HIC transmission, No connect detection

FIGURE 56

PRINT OF DRAWINGS
AS ORIGINALLY FILED

Power/Ground/OSC input Signals

Name	Type	Pins	Description
OSCin	I	1	Oscillator input for LVDS clock
GND (PLL)		1	PLL ground
VCC (PLL)		1	PLL 3.3v
VCC (core)		2	Core/CPU VCC = 3.3v
VCC (LVDS)		2	LVDS VCC = 3.3v
VCC (VP)		1	Video port: all output signals; VCC = 3.3v
VCC (PCI)		2	PCI VCC = 5v tolerant or 3.3v
VCC (Flash)		1	Flash memory VCC = 5v tolerant or 3.3v
GND (core)		2	Core ground
GND (LVDS)		2	LVDS ground
GND (PCI)		2	PCI ground
GND (Flash)		1	Flash memory ground
Reserved		1	Reserved pins

FIGURE 57

09/149882

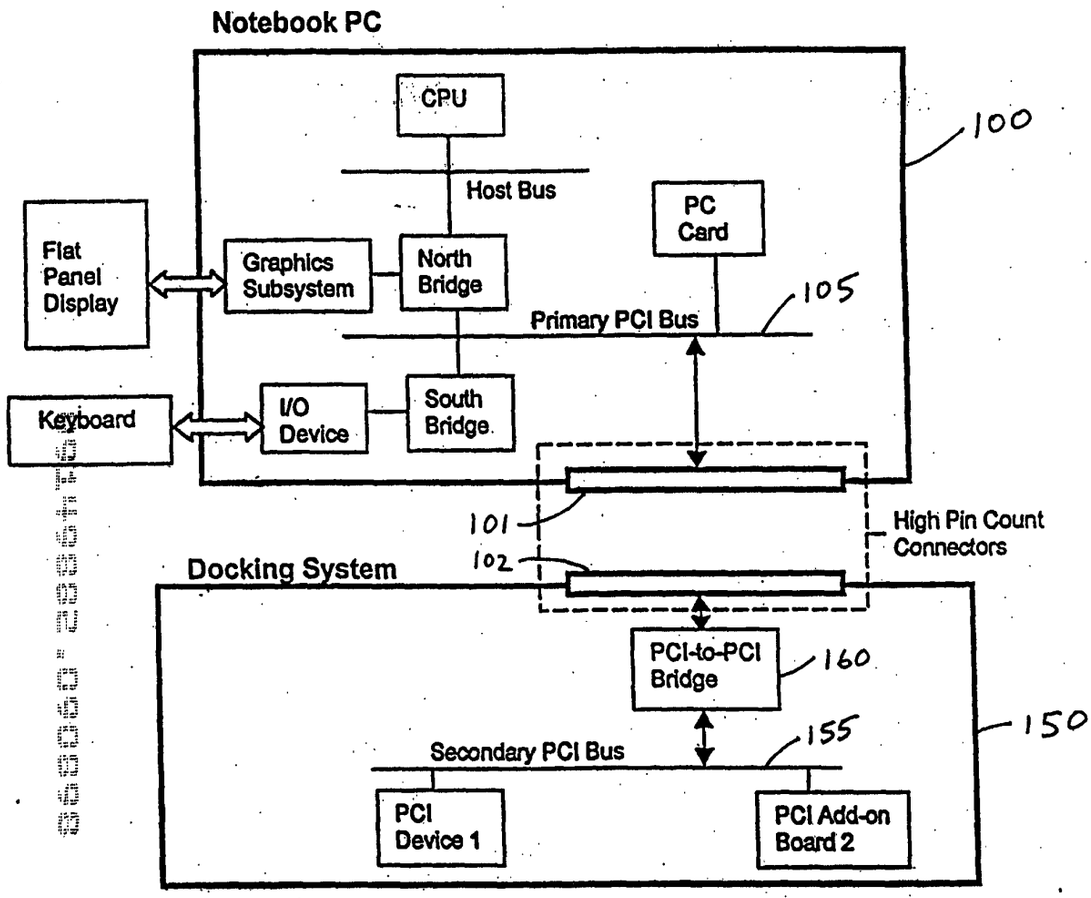


FIGURE 1

57

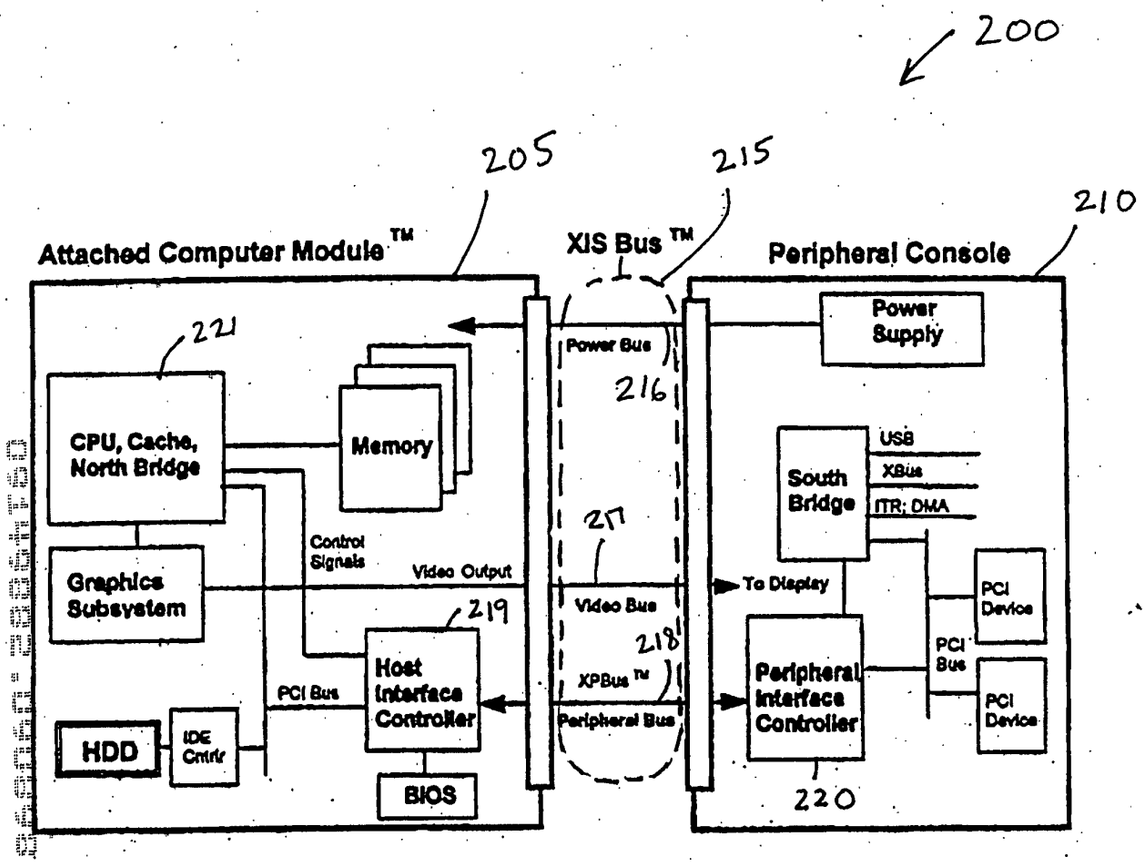

200
205
215
210
Attached Computer Module™
XIS Bus™
Peripheral Console
221
CPU, Cache, North Bridge
Memory
Graphics Subsystem
Control Signals
Video Output
219
Host Interface Controller
PCI Bus
HDD
IDE Cntlr
BIOS
Power Bus
216
217
Video Bus
218
XPBus™
Peripheral Bus
Power Supply
South Bridge
USB
XBus
ITR; DMA
To Display
PCI Device
PCI Bus
PCI Device
Peripheral Interface Controller
220

FIGURE 2

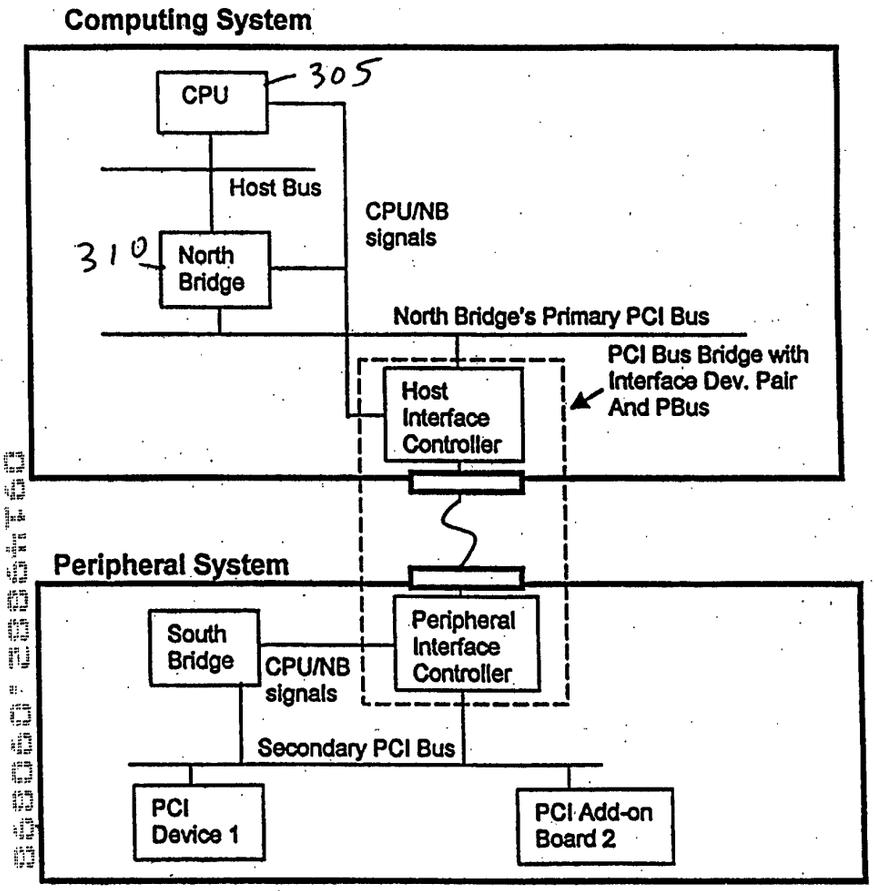

Computing System
CPU
305
Host Bus
CPU/NB signals
310
North Bridge
North Bridge's Primary PCI Bus
PCI Bus Bridge with Interface Dev. Pair And PBus
Host Interface Controller
Peripheral System
South Bridge
CPU/NB signals
Peripheral Interface Controller
Secondary PCI Bus
PCI Device 1
PCI Add-on Board 2

FIGURE 3

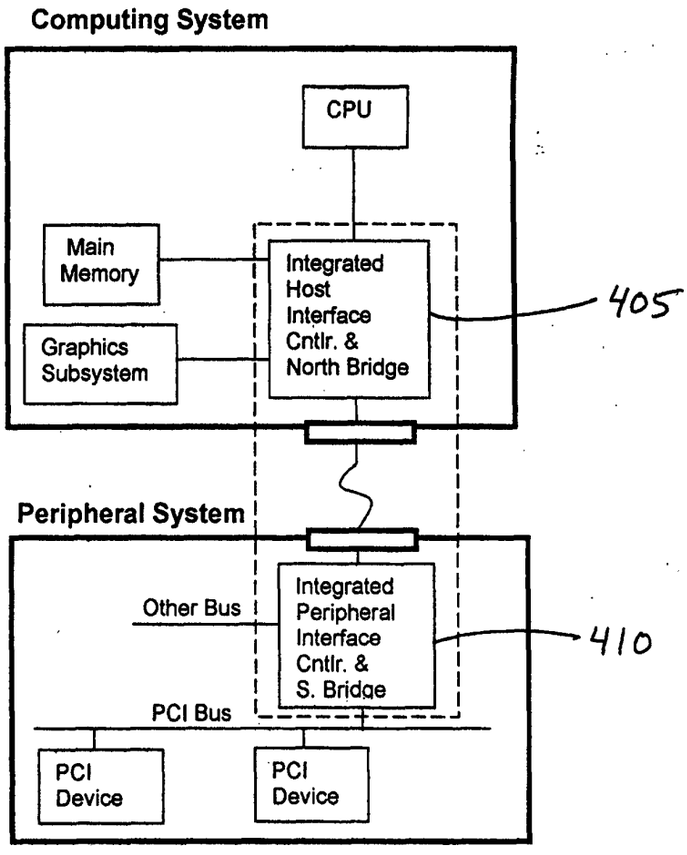

Computing System
CPU
Main Memory
Graphics Subsystem
Integrated Host Interface Cntlr. & North Bridge
405
Peripheral System
Other Bus
Integrated Peripheral Interface Cntlr. & S. Bridge
410
PCI Bus
PCI Device
PCI Device

FIGURE 4

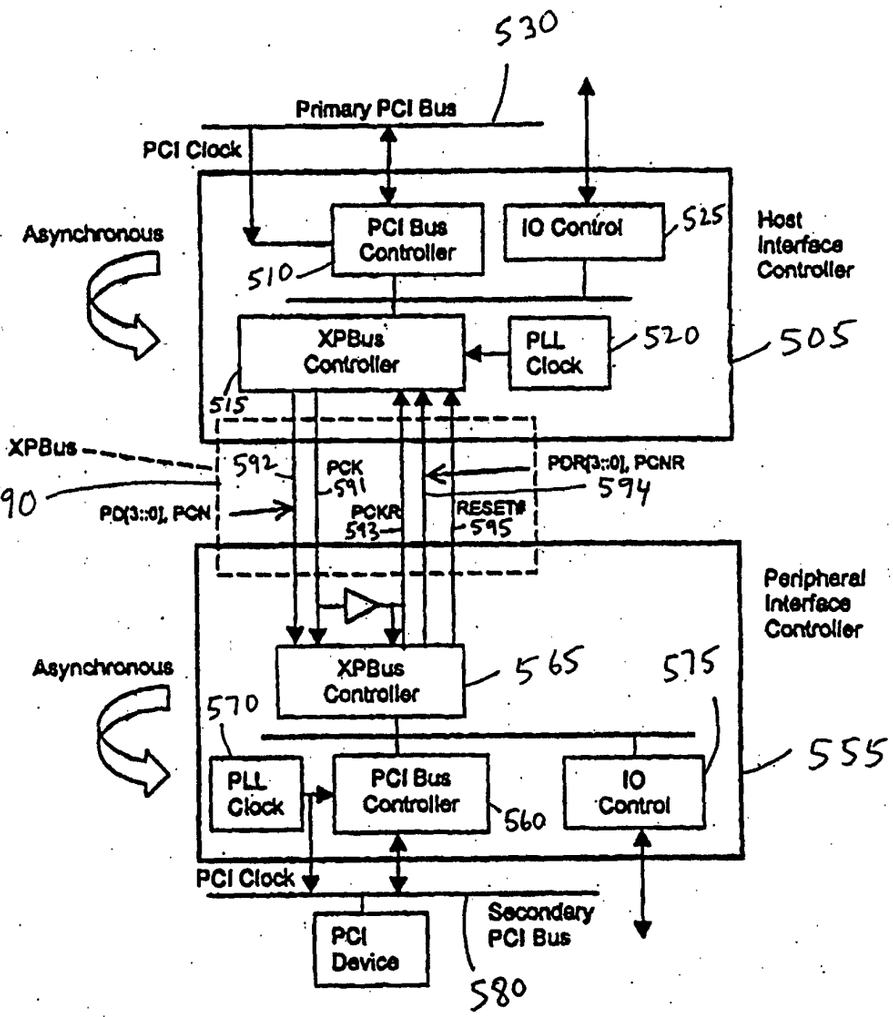

530
Primary PCI Bus
PCI Clock
Asynchronous
PCI Bus Controller
IO Control
525
Host Interface Controller
510
XPBus Controller
PLL Clock
520
505
515
XPBus
592
PCK
591
PDR[3::0], PCNR
594
590
PD[3::0], PCN
PCKR
593
RESET#
595
Peripheral Interface Controller
Asynchronous
XPBus Controller
565
575
570
555
PLL Clock
PCI Bus Controller
560
IO Control
PCI Clock
PCI Device
Secondary PCI Bus
580

FIGURE 5

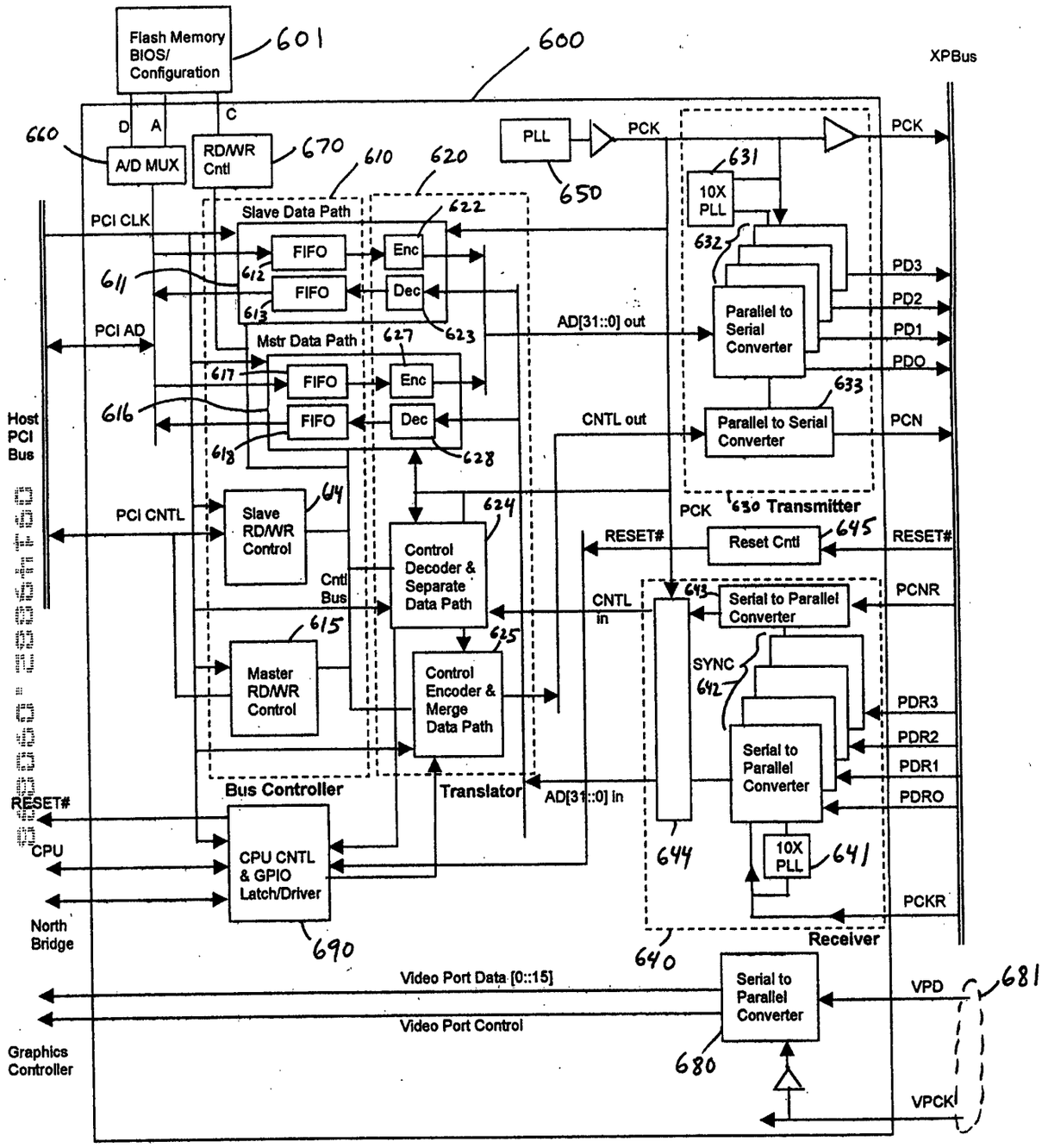

Flash Memory BIOS/ Configuration
601
600
XPBus
D
A
C
660
A/D MUX
RD/WR Cntl
670
610
620
PLL
PCK
650
631
10X PLL
632
PCI CLK
Slave Data Path
622
FIFO
Enc
611
612
FIFO
Dec
613
PD3
PD2
PD1
PDO
PCI AD
Mstr Data Path
627
623
AD[31::0] out
Parallel to Serial Converter
617
FIFO
Enc
616
FIFO
Dec
618
628
633
CNTL out
Parallel to Serial Converter
PCN
Host PCI Bus
PCK
630 Transmitter
PCI CNTL
Slave RD/WR Control
614
624
Control Decoder & Separate Data Path
RESET#
Reset Cntl
645
RESET#
Cntl Bus
CNTL in
643
Serial to Parallel Converter
PCNR
615
SYNC
642
Master RD/WR Control
625
Control Encoder & Merge Data Path
PDR3
PDR2
PDR1
PDRO
Serial to Parallel Converter
Bus Controller
Translator
AD[31::0] in
RESET#
CPU
CPU CNTL & GPIO Latch/Driver
644
10X PLL
641
PCKR
North Bridge
690
640
Receiver
Video Port Data [0::15]
Serial to Parallel Converter
VPD
681
Video Port Control
Graphics Controller
680
VPCK

FIGURE 6

HIC as Target (Default)

Control Signal	HIC to XPBus	XPBus to HIC	Primary PCI Bus	Comment
FRAME #	Encode (BS0)		Transaction Active	
IRDY #	Encode (BS1)		Initiator Ready	
TRDY #	Local		HIC Generates	
DEVSEL #	Local		HIC Accepts Command	Positive decode, medium
STOP #	Local		HIC requests to retry	Posted Read operation
PAR	Encode	Decode	Parity for A/C; D/BE	
IDSEL	Local		Used locally for config. 0	
PERR #	Encode	Decode	Data Parity Error	
SERR #		Decode	Address/System Parity Error	
REQ #		Decode	HIC requests to be master	S. Bus device requests bus
GNT #	Encode		Host grants bus	
RST				Independent signal

FIGURE 7

HIC as Master

Control Signal	HIC to XPBus	XPBus to HIC	Primary PCI Bus	Comment
FRAME #		Decode	Transaction Active	
IRDY #		Decode	Initiator Ready	
TRDY #	Local		Receive from Target	
DEVSEL #	Local		Receive from Target	
STOP #	Local		retry handles locally	
PAR	Encode	Decode	Parity for A/C; D/BE	
IDSEL	Local		Used locally for config. 0	
PERR #	Encode	Decode	Data Parity Error	
SERR #		Decode	Address/System Parity Error	
REQ #		Decode	HIC continue to be Master	PCI device can end REQ#
GNT #	Encode		Arbiter grant bus to HIC	Arbiter can deassert GNT#
RST				Independent signal

FIGURE 8

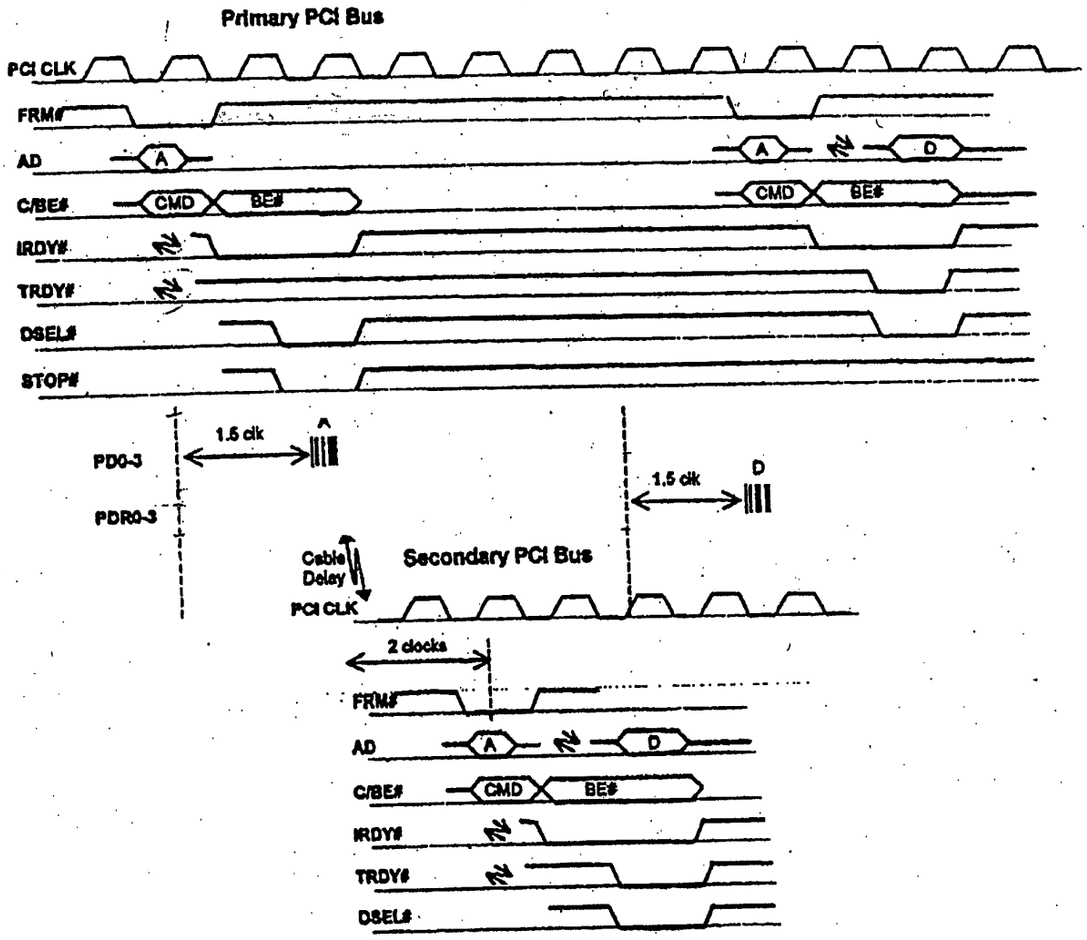

Primary PCI Bus
PCI CLK
FRM#
AD
A
A
D
C/BE#
CMD
BE#
CMD
BE#
IRDY#
TRDY#
DSEL#
STOP#
PD0-3
PDR0-3
1.5 clk
A
1.5 clk
D
Cable Delay
Secondary PCI Bus
PCI CLK
2 clocks
FRM#
AD
A
D
C/BE#
CMD
BE#
IRDY#
TRDY#
DSEL#

FIGURE 9

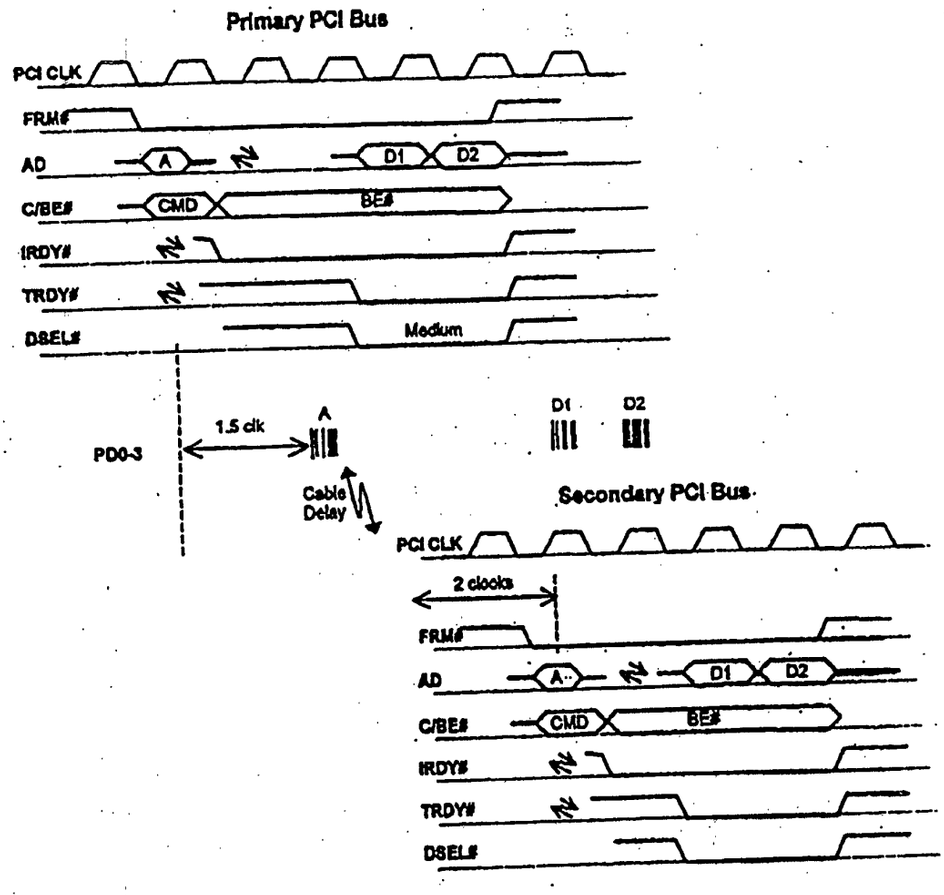

Primary PCI Bus
PCI CLK
FRM#
AD
A
D1
D2
C/BE#
CMD
BE#
IRDY#
TRDY#
DSEL#
Medium
PD0-3
1.5 clk
A
D1
D2
Cable Delay
Secondary PCI Bus
PCI CLK
2 clocks
FRM#
AD
A
D1
D2
C/BE#
CMD
BE#
IRDY#
TRDY#
DSEL#

FIGURE 10

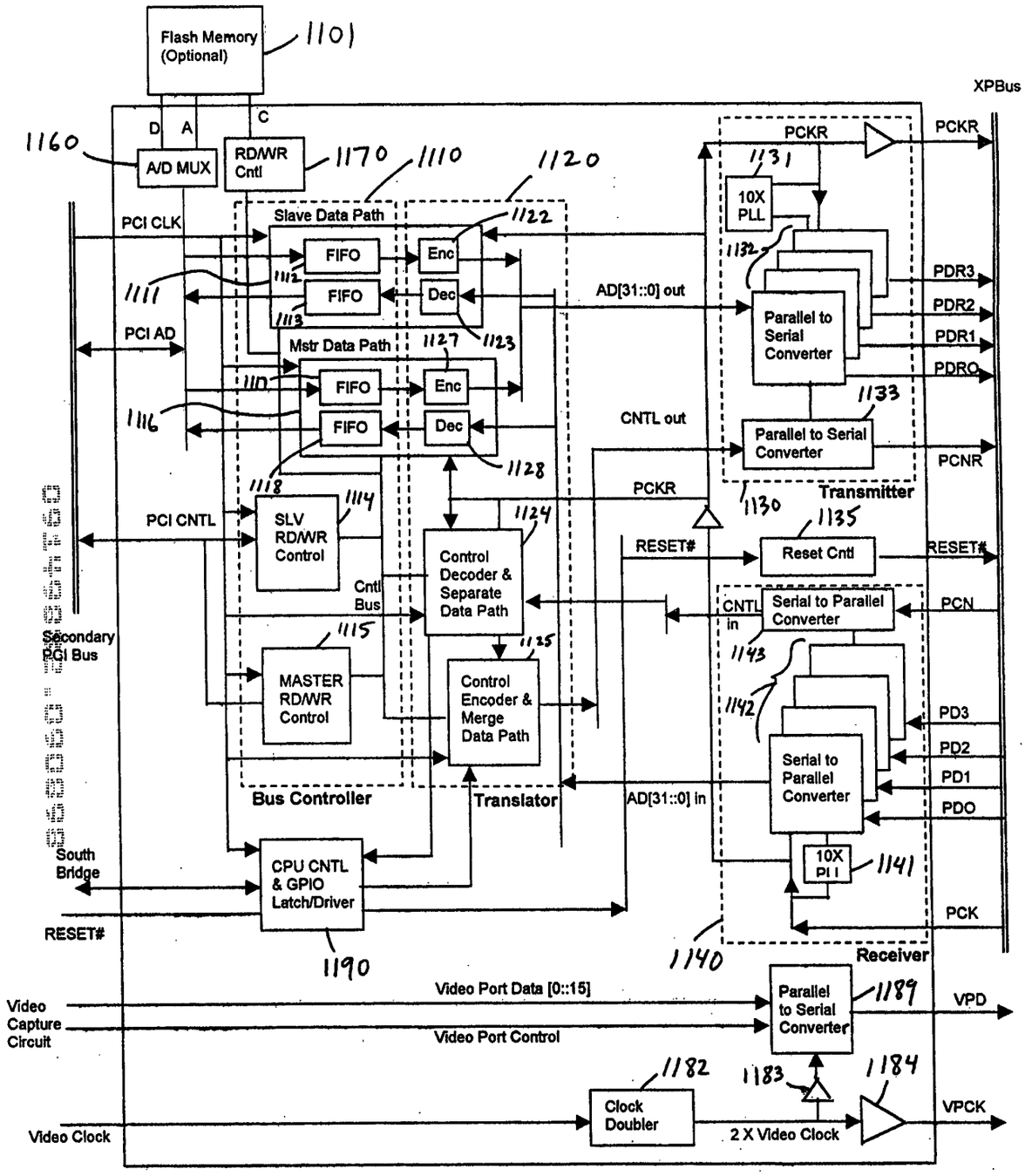

Flash Memory (Optional)
1101
XPBus
D
A
C
1160
A/D MUX
RD/WR Cntl
1170
1110
1120
PCKR
1131
10X PLL
1132
PCI CLK
Slave Data Path
1122
FIFO
Enc
1112
1111
FIFO
Dec
1113
AD[31::0] out
Parallel to Serial Converter
PDR3
PDR2
PDR1
PDR0
PCI AD
Mstr Data Path
1127
1123
1110
FIFO
Enc
1116
FIFO
Dec
1133
CNTL out
Parallel to Serial Converter
PCNR
1128
1118
PCKR
Transmitter
1130
PCI CNTL
SLV RD/WR Control
1114
1124
1135
RESET#
Reset Cntl
RESET#
Control Decoder & Separate Data Path
Cntl Bus
CNTL in
Serial to Parallel Converter
PCN
1115
1143
Secondary PCI Bus
MASTER RD/WR Control
1125
Control Encoder & Merge Data Path
1142
PD3
PD2
PD1
PD0
Serial to Parallel Converter
Bus Controller
Translator
AD[31::0] in
10X PLL
1141
South Bridge
CPU CNTL & GPIO Latch/Driver
PCK
RESET#
1190
1140
Receiver
Video Port Data [0::15]
Parallel to Serial Converter
1189
VPD
Video Capture Circuit
Video Port Control
1182
1183
1184
Clock Doubler
VPCK
Video Clock
2 X Video Clock

FIGURE 11

PIC as Target

Control Signal	PIC to XPBus	XPBus to PIC	Secondary PCI Bus	Comment
FRAME #	Encode (BS0)		Transaction Active	
IRDY #	Encode (BS1)		Initiator Ready	
TRDY #	Local		PIC Generates	
DEVSEL #	Local		PIC Accepts Command	Positive decode, medium
STOP #	Local	Decode	PIC requests to retry	Host can stop trans.
PAR	Encode	Decode	Parity for A/C; D/BE	
IDSEL	Local		Used locally for config. 0	
PERR #	Encode	Decode	Data Parity Error	
SERR #	Encode	Decode	Address/System Parity Error	
REQ #		Decode	PIC requests to be master	P. Bus device requests bus
GNT #	Encode		PIC grants bus to itself	
RST				Independent signal

FIGURE 12

PIC as Master (Default)

Control Signal	PIC to XPBus	XPBus to PIC	Secondary PCI Bus	Comment
FRAME #		Decode	Transaction Active	
IRDY #		Decode	Initiator Ready	
TRDY #	Local		Receive from Target	
DEVSEL #	Local		Receive from Target	
STOP #	Local/Encode		Receive from Target	Target can stop trans.
PAR	Encode	Decode	Parity for A/C; D/BE	
IDSEL	Local		Used locally for config. 0	
PERR #	Encode	Decode	Data Parity Error	
SERR #	Encode	Decode	Address/System Parity Error	
REQ #		Decode	PIC request to be Master	
GNT #	Encode		Arbiter grant bus to PIC	
RST				Independent signal

FIGURE 13

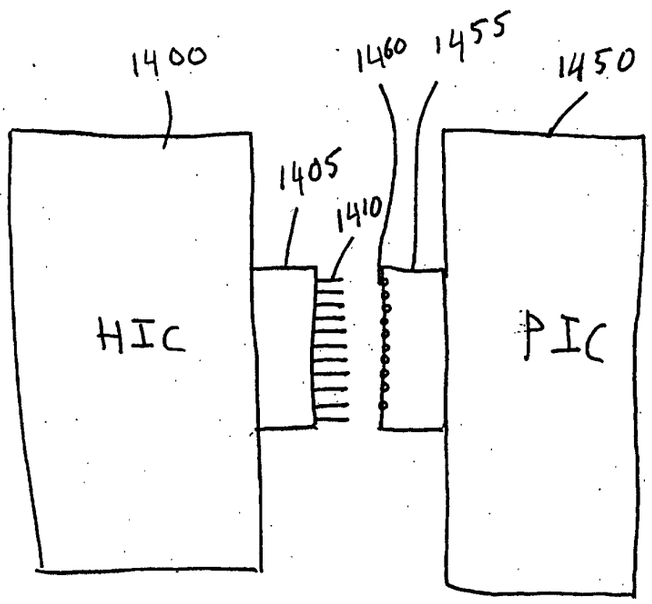


FIGURE 14

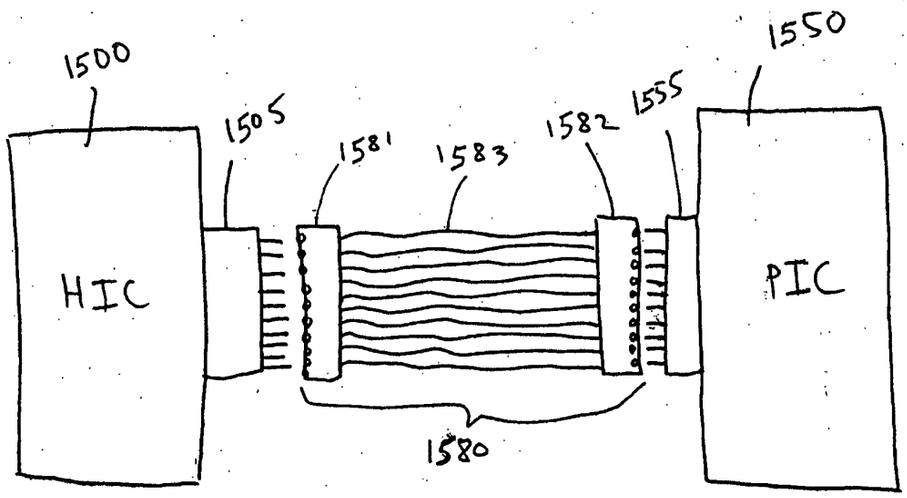


FIGURE 15

SUBSTITUTE SHEET (RULE 26)

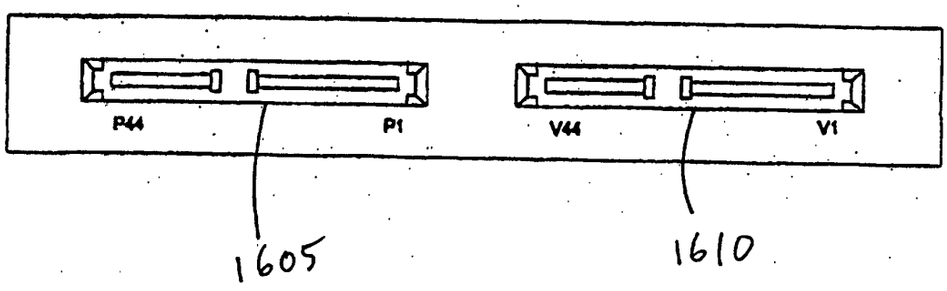


FIGURE 16

ACM's XIS BUS Connector Plug PIN Position (88 pin):

V23	GND	GND	V1		P23	GND	GND	P1
V24	P&D D0 +	RED VIDEO	V2		P24	PD0 +	PDR0 +	P2
V25	P&D D0 -	GND	V3		P25	PD0 -	PDR0 -	P3
V26	GND	GREEN VIDEO	V4		P26	GND	GND	P4
V27	P&D CLK +	GND	V5		P27	PD1 +	PDR1 +	P5
V28	P&D CLK -	BLUE VIDEO	V6		P28	PD1 -	PDR1 -	P6
V29	GND	GND	V7		P29	GND	GND	P7
V30	P&D D1 +	HSYNC	V8		P30	PD2 +	PDR2 +	P8
V31	P&D D1 -	VSYNC	V9		P31	PD2 -	PDR2 -	P9
V32	GND	GND	V10		P32	GND	GND	P10
V33	P&D D2 +	DDC2: SCL	V11		P33	PCK +	PCKR +	P11
V34	P&D D2 -	DDC2: SDA	V12		P34	PCK -	PCKR -	P12
V35	Config 3	Config 2	V13		P35	Config 1	Config 0	P13
V36	GND	TV CV/ CNTL0	V14		P36	GND	GND	P14
V37	VPCK +	SV Y/ CNTL1	V15		P37	PD3 +	PDR3 +	P15
V38	VPCK -	SV C/ CNTL2	V16		P38	PD3 -	PDR3 -	P16
V39	GND	V33	V17		P39	GND	GND	P17
V40	VPD +	V33	V18		P40	PCN +	PCNR +	P18
V41	VPD -	V33	V19		P41	PCN -	PCNR -	P19
V42	GND	V33	V20		P42	Reserved	V5	P20
V43	GND	V33	V21		P43	Reserved	V5	P21
V44	GND	V33	V22		P44	Reserved	V5	P22

FIGURE 17

Pin No.	Symbol	Signal	Standard	Description
P2	PDR0 +	LVDS		Peripheral data reverse 0 +
P3	PDR0 -	LVDS		Peripheral data reverse 0 -
P5	PDR1 +	LVDS		Peripheral data reverse 1 +
P6	PDR1 -	LVDS		Peripheral data reverse 1 -
P8	PDR2 +	LVDS		Peripheral data reverse 2 +
P9	PDR2 -	LVDS		Peripheral data reverse 2 -
P11	PCKR +	LVDS		Peripheral clock reverse +
P12	PCKR -	LVDS		Peripheral clock reverse -
P15	PDR3 +	LVDS		Peripheral data reverse 3 +
P16	PDR3 -	LVDS		Peripheral data reverse 3 -
P18	PCNR +	LVDS		Peripheral control reverse +
P19	PCNR -	LVDS		Peripheral control reverse -
P24	PD0 +	LVDS		Peripheral data 0 +
P25	PD0 -	LVDS		Peripheral data 0 -
P27	PD1 +	LVDS		Peripheral data 1 +
P28	PD1 -	LVDS		Peripheral data 1 -
P30	PD2 +	LVDS		Peripheral data 2 +
P31	PD2 -	LVDS		Peripheral data 2 -
P33	PCK +	LVDS		Peripheral clock +
P34	PCK -	LVDS		Peripheral clock -
P37	PD3 +	LVDS		Peripheral data 3 +
P38	PD3 -	LVDS		Peripheral data 3 -
P40	PCN +	LVDS		Peripheral control +
P41	PCN -	LVDS		Peripheral Control -
P13	Config 0	Static	3.3v or GND	Configuration bit 0
P35	Config 1	Static	3.3v or GND	Configuration bit 1
P1,P4,P7,P10, P14,P17,P23,P26, P29,P32,P36,P39	GND		GND	Ground

FIGURE 18

Pin No.	Symbol	Signal	Standard	Description
V2	Red Video	Analog		Video
V4	Green Video	Analog		Video
V6	Blue Video	Analog		Video
V8	HSYNC			Horizontal Sync
V9	VSYNC			Vertical Sync
V11	DDC2 SCL		VESA DDC std 2	DDC Clock
V12	DDC2 SDA		VESA DDC std 2	DDC Data
V14	TV-CV/CNTL 0			TV Composite Video
V15	SV Y/CNTL 1		Super Video	SV Luminance or Control 1
V16	SV C/CNTL 2		Super Video	SV Chrominance or Control 2
V24	D0 +	TMDS	VESA P & D	Data 0 +
V25	D0 -	TMDS	VESA P & D	Data 0 -
V27	CLK +	TMDS	VESA P & D	Clock +
V28	CLK -	TMDS	VESA P & D	Clock -
V30	D1 +	TMDS	VESA P & D	Data 1 +
V31	D1 -	TMDS	VESA P & D	Data 1 -
V33	D2 +	TMDS	VESA P & D	Data 2 +
V34	D2 -	TMDS	VESA P & D	Data 2 -
V37	VPCK +	LVDS		Video Port Pixel Clock +
V38	VPCK -	LVDS		Video Port Pixel Clock -
V40	VPD +	LVDS		Video Port Pixel Data +
V41	VPD -	LVDS		Video Port Pixel Data -
V13	Config 2		3.3v or GND	Configuration bit 2
V35	Config 3		3.3v or GND	Configuration bit 3
V1, V3, V5, V7, V10, V23, V26, V29, V32, V36, V39, V42, V43, V44	GND		GND	Ground

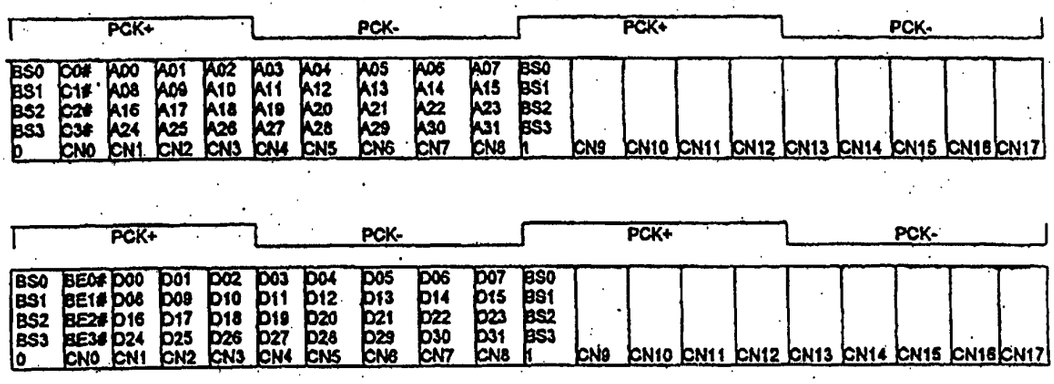
FIGURE 19

	Symbol	Signal	Data Rate	Description
1	PD0 RTN			GND
2	PD0 +	Synch. To PCK	10 x clock rate	Computer to Peripheral LVDS Data 0 +
3	PD0 -			Computer to Peripheral LVDS Data 0 -
4	PD1 RTN			GND
5	PD1 +	Synch. To PCK	10 x clock rate	Computer to Peripheral LVDS Data 1 +
6	PD1 -			Computer to Peripheral LVDS Data 1 -
7	PD2 RTN			GND
8	PD2 +	Synch. To PCK	10 x clock rate	Computer to Peripheral LVDS Data 2 +
9	PD2 -			Computer to Peripheral LVDS Data 2 -
10	PD3 RTN			GND
11	PD3 +	Synch. To PCK	10 x clock rate	Computer to Peripheral LVDS Data 3 +
12	PD3 -			Computer to Peripheral LVDS Data 3 -
13	PCK RTN			GND
14	PCK +	Clock	Clock rate	Computer to Peripheral LVDS Clock +
15	PCK -			Computer to Peripheral LVDS Clock -
16	PCN RTN			GND
17	PCN +	Synch. To PCK	10 x clock rate	Computer to Peripheral LVDS Control +
18	PCN -			Computer to Peripheral LVDS Control -
19	PDR0 RTN			GND
20	PDR0 +	Synch. To PCKR	10 x clock rate	Peripheral to Computer LVDS Data 0 +
21	PDR0 -			Peripheral to Computer LVDS Data 0 -
22	PDR1 RTN			GND
23	PDR1 +	Synch. To PCKR	10 x clock rate	Peripheral to Computer LVDS Data 1 +
24	PDR1 -			Peripheral to Computer LVDS Data 1 -
25	PDR2 RTN			GND
26	PDR2 +	Synch. To PCKR	10 x clock rate	Peripheral to Computer LVDS Data 2 +
27	PDR2 -			Peripheral to Computer LVDS Data 2 -
28	PDR3 RTN			GND
29	PDR3 +	Synch. To PCKR	10 x clock rate	Peripheral to Computer LVDS Data 3 +
30	PDR3 -			Peripheral to Computer LVDS Data 3 -
31	PCKR RTN			GND
32	PCKR +	Reverse Dir. Clock	Clock rate	Peripheral to Computer LVDS Clock +
33	PCKR -			Peripheral to Computer LVDS Clock -
34	PCNR RTN			GND
35	PCNR +	Synch. To PCKR	10 x Clock rate	Peripheral to Computer LVDS Control +
36	PCNR -			Peripheral to Computer LVDS Control -
37	RESET#		Asynchronous	Reset

FIGURE 20

PCK	CK+	CK+	CK+	CK+	CK+	CK-	CK-	CK-	CK-	CK-	CK+	CK+	CK+	CK+	CK+	CK-	CK-	CK-	CK-	CK-
PD0	BS0	CM0#	A00	A01	A02	A03	A04	A05	A06	A07	BS0	BE0#	D00	D01	D02	D03	D04	D05	D06	D07
PD1	BS1	CM1#	A08	A09	A10	A11	A12	A13	A14	A15	BS1	BE1#	D08	D09	D10	D11	D12	D13	D14	D15
PD2	BS2	CM2#	A16	A17	A18	A19	A20	A21	A22	A23	BS2	BE2#	D16	D17	D18	D19	D20	D21	D22	D23
PD3	BS3	CM3#	A24	A25	A26	A27	A28	A29	A30	A31	BS3	BE3#	D24	D25	D26	D27	D28	D29	D30	D31
PCN	CN0	CN1	CN2	CN3	CN4	CN5	CN6	CN7	CN8	CN9	CN0	CN1	CN2	CN3	CN4	CN5	CN6	CN7	CN8	CN9

FIGURE 21



PCK+					PCK-					PCK+									PCK-									
BS0	C0#	A00	A01	A02	A03	A04	A05	A06	A07	BS0																	
BS1	C1#	A08	A09	A10	A11	A12	A13	A14	A15	BS1																	
BS2	C2#	A16	A17	A18	A19	A20	A21	A22	A23	BS2																	
BS3	C3#	A24	A25	A26	A27	A28	A29	A30	A31	BS3																	
0	CN0	CN1	CN2	CN3	CN4	CN5	CN6	CN7	CN8	1	CN9	CN10	CN11	CN12	CN13	CN14	CN15	CN16	CN17								

PCK+					PCK-					PCK+									PCK-									
BS0	BE0#	D00	D01	D02	D03	D04	D05	D06	D07	BS0																	
BS1	BE1#	D08	D09	D10	D11	D12	D13	D14	D15	BS1																	
BS2	BE2#	D16	D17	D18	D19	D20	D21	D22	D23	BS2																	
BS3	BE3#	D24	D25	D26	D27	D28	D29	D30	D31	BS3																	
0	CN0	CN1	CN2	CN3	CN4	CN5	CN6	CN7	CN8	1	CN9	CN10	CN11	CN12	CN13	CN14	CN15	CN16	CN17								

FIGURE 22

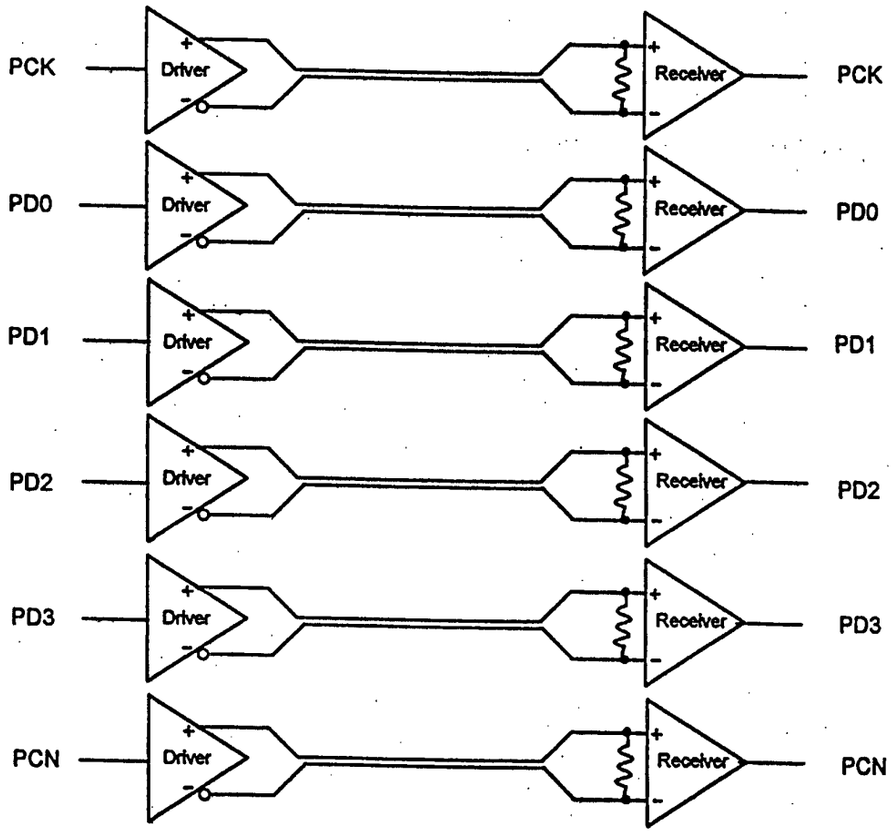

PCK
Driver
Receiver
PCK
PD0
Driver
Receiver
PD0
PD1
Driver
Receiver
PD1
PD2
Driver
Receiver
PD2
PD3
Driver
Receiver
PD3
PCN
Driver
Receiver
PCN

FIGURE 23

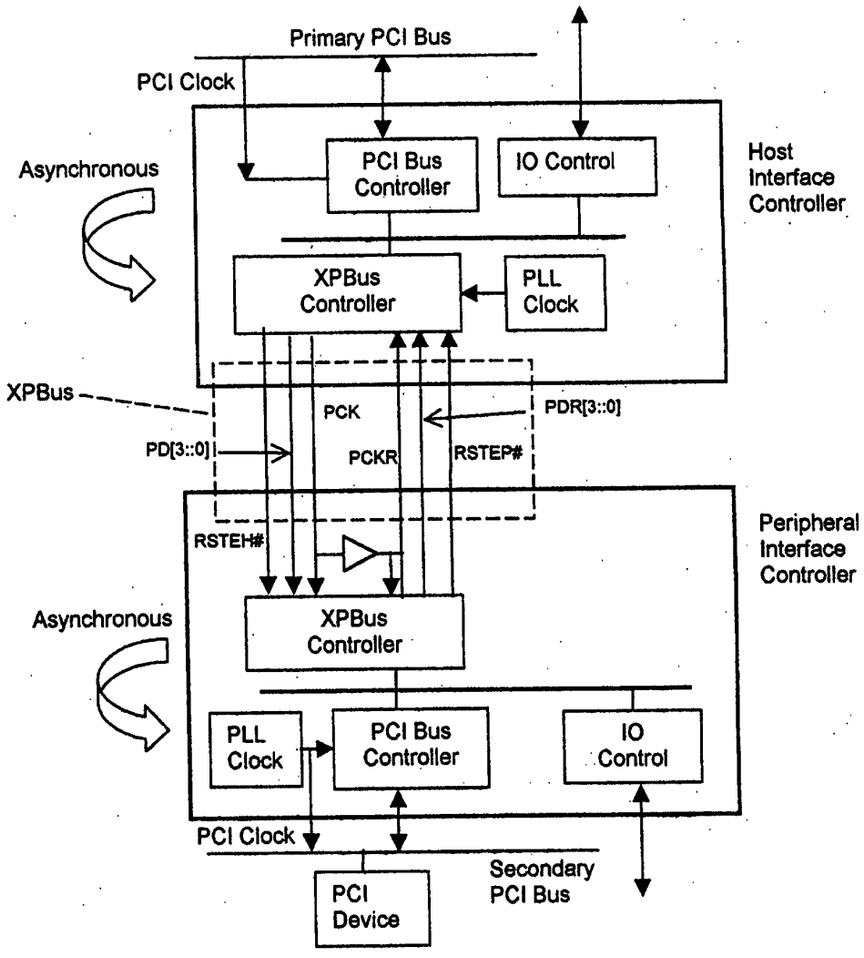

Primary PCI Bus
PCI Clock
Asynchronous
PCI Bus Controller
IO Control
Host Interface Controller
XPBus Controller
PLL Clock
XPBus
PCK
PDR[3::0]
PD[3::0]
PCKR
RSTEP#
RSTEH#
Peripheral Interface Controller
Asynchronous
XPBus Controller
PLL Clock
PCI Bus Controller
IO Control
PCI Clock
Secondary PCI Bus
PCI Device

FIGURE 24

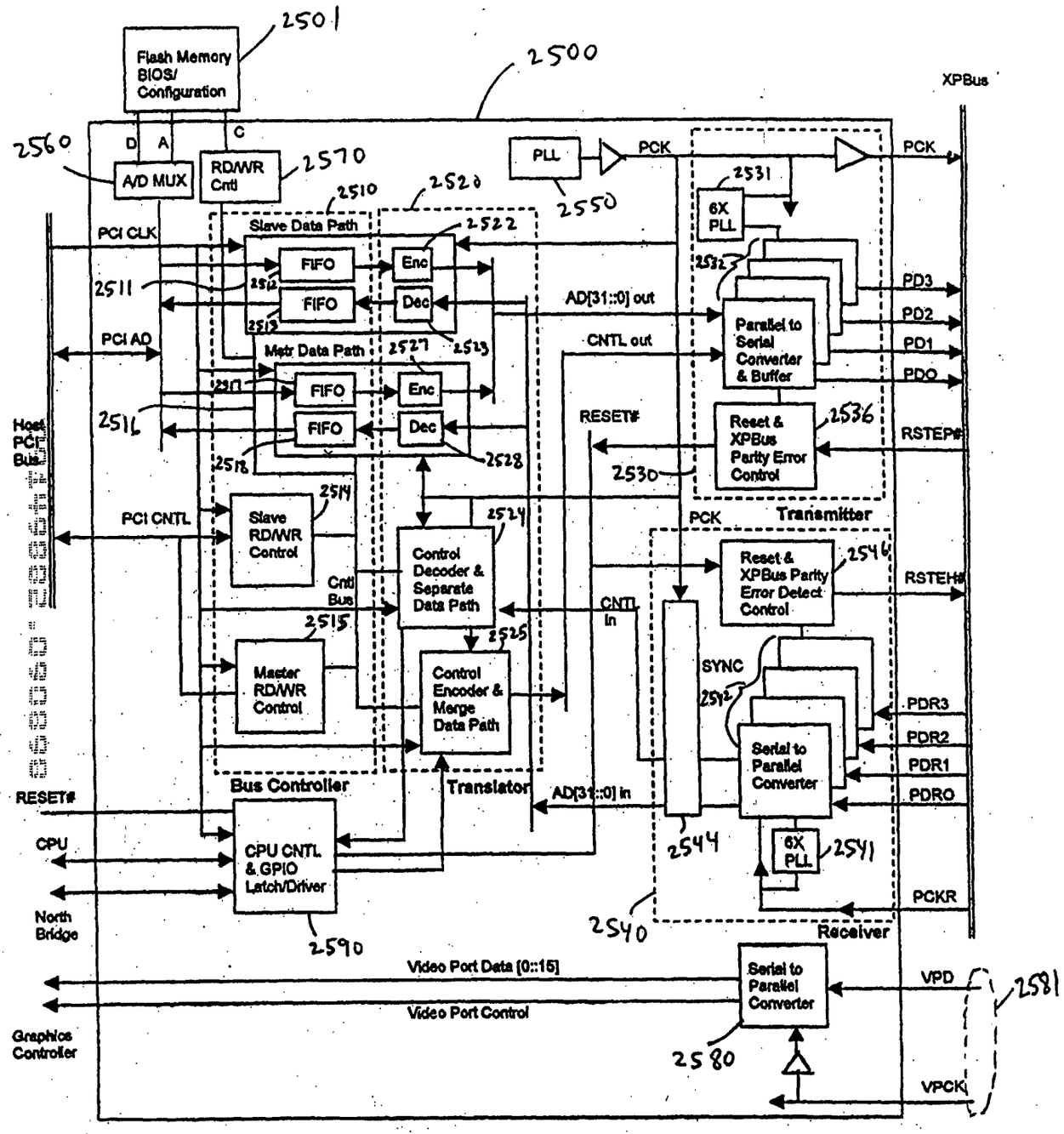

2501
Flash Memory BIOS/ Configuration
2500
XPBus
2560
D
A
C
A/D MUX
RD/WR Cntl
2570
PLL
PCK
2550
2531
6X PLL
2510
2520
Slave Data Path
2522
PCI CLK
FIFO
Enc
2511
2512
FIFO
Dec
AD[31::0] out
PD3
PD2
PD1
PD0
Parallel to Serial Converter & Buffer
PCI AD
Mstr Data Path
2527
2513
CNTL out
2517
FIFO
Enc
2516
FIFO
Dec
RESET#
2536
Reset & XPBus Parity Error Control
RSTEP#
Host PCI Bus
2518
2528
2530
2514
PCI CNTL
Slave RD/WR Control
2524
Control Decoder & Separate Data Path
PCK
Transmitter
2546
Reset & XPBus Parity Error Detect Control
RSTEH#
Cntl Bus
CNTL In
2515
2525
Master RD/WR Control
Control Encoder & Merge Data Path
SYNC
2542
PDR3
PDR2
PDR1
PDR0
Serial to Parallel Converter
Bus Controller
Translator
AD[31::0] In
RESET#
2544
6X PLL
2541
CPU
CPU CNTL & GPIO Latch/Driver
PCKR
North Bridge
2590
2540
Receiver
Video Port Data [0::15]
Serial to Parallel Converter
VPD
2581
Video Port Control
Graphics Controller
2580
VPCK

FIGURE 25

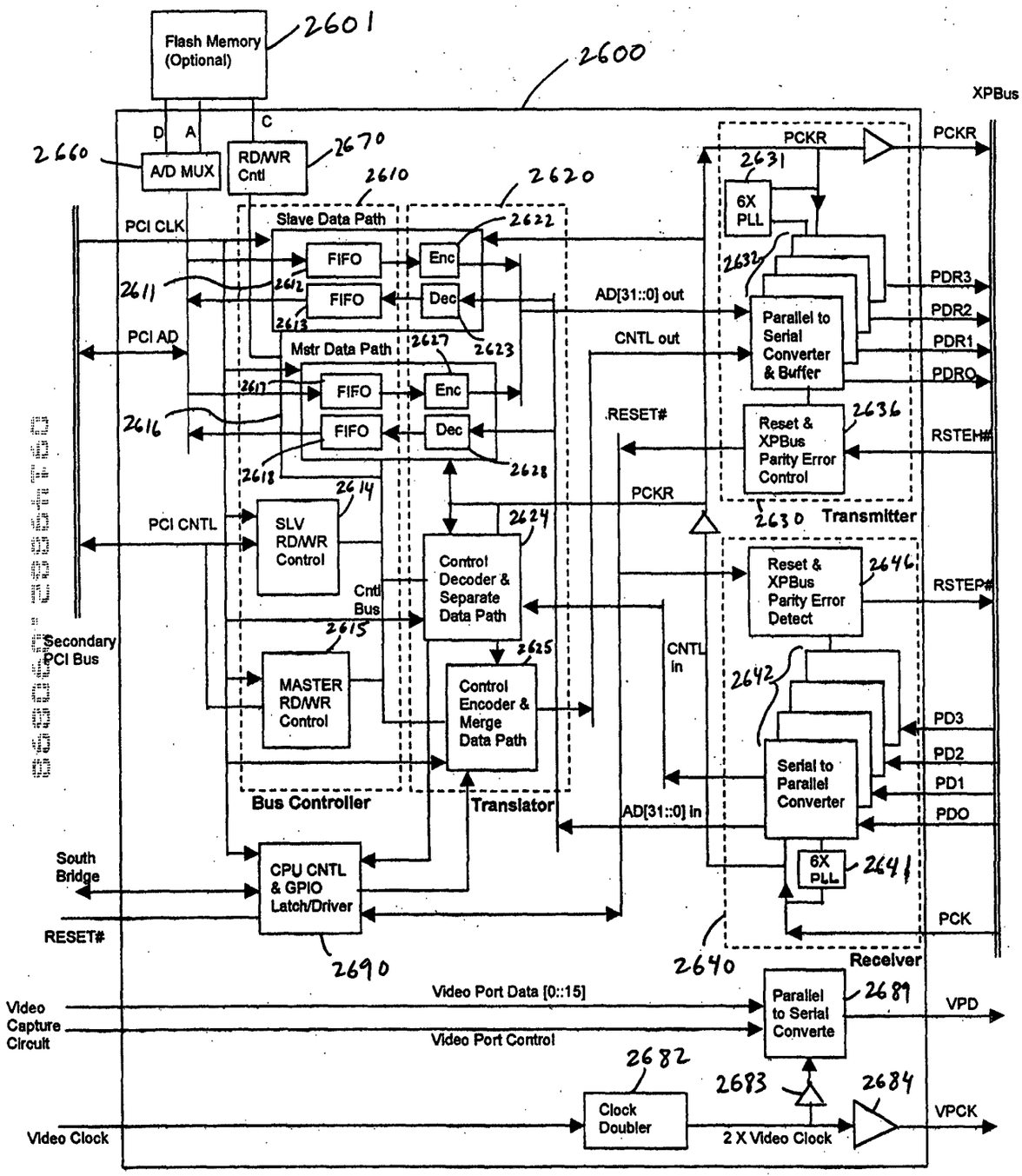

Flash Memory (Optional)
2601
2600
XPBus
D
A
C
2660
A/D MUX
RD/WR Cntl
2670
2610
2620
Slave Data Path
PCI CLK
FIFO
Enc
2622
2611
2612
FIFO
Dec
2613
AD[31::0] out
PCI AD
Mstr Data Path
2627
2623
CNTL out
2617
FIFO
Enc
2616
FIFO
Dec
2618
2628
RESET#
PCKR
PCI CNTL
SLV RD/WR Control
2614
2624
Control Decoder & Separate Data Path
Cntl Bus
Secondary PCI Bus
2615
MASTER RD/WR Control
2625
Control Encoder & Merge Data Path
CNTL in
Bus Controller
Translator
AD[31::0] in
South Bridge
CPU CNTL & GPIO Latch/Driver
RESET#
2690
2640
Receiver
PCKR
2631
6X PLL
2632
Parallel to Serial Converter & Buffer
PDR3
PDR2
PDR1
PDR0
Reset & XPBus Parity Error Control
2636
RSTEH#
2630
Transmitter
Reset & XPBus Parity Error Detect
2646
RSTEP#
2642
PD3
PD2
PD1
PD0
Serial to Parallel Converter
6X PLL
2641
PCK
Video Port Data [0::15]
Video Capture Circuit
Video Port Control
Parallel to Serial Converte
2689
VPD
2682
2683
2684
Clock Doubler
VPCK
Video Clock
2 X Video Clock

FIGURE 26

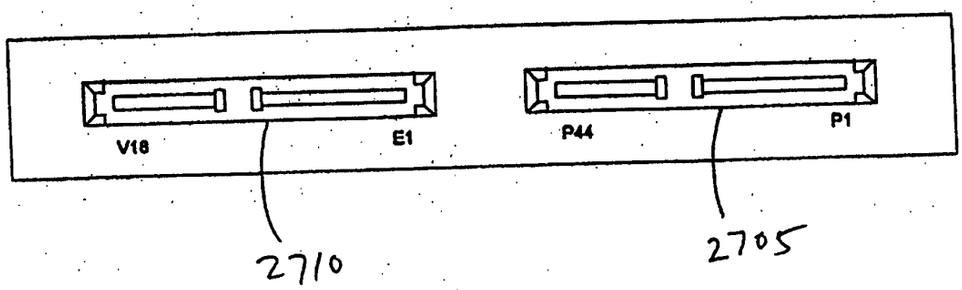


FIGURE 27

ACM's CMI BUS Connector Plug PIN Position (88 pin):

E14	GND	GND	E1	P23	GND	GND	P1
E15	P&D D0 +	VPD+/TPA+	E2	P24	PD0 +	PDR0 +	P2
E16	P&D D0 -	VPD-/TPA-	E3	P25	PD0 -	PDR0 -	P3
E17	GND	GND	E4	P26	GND	GND	P4
E18	P&D CLK +	VPCK+/TPB+	E5	P27	PD1 +	PDR1 +	P5
E19	P&D CLK -	VPCK-/TPB-	E6	P28	PD1 -	PDR1 -	P6
E20	GND	Reserved	E7	P29	GND	GND	P7
E21	P&D D1 +	Reserved	E8	P30	PD2 +	PDR2 +	P8
E22	P&D D1 -	Reserved	E9	P31	PD2 -	PDR2 -	P9
E23	GND	Reserved	E10	P32	GND	GND	P10
E24	P&D D2 +	Reserved	E11	P33	PCK +	PCKR +	P11
E25	P&D D2 -	Reserved	E12	P34	PCK -	PCKR -	P12
E26	Config 3	Config 2	E13	P35	Config 1	Config 0	P13
V10	GND	V33	V1	P36	GND	GND	P14
V11	GND	V33	V2	P37	PD3 +	PDR3 +	P15
V12	GND	V33	V3	P38	PD3 -	PDR3 -	P16
V13	V33	V33	V4	P39	RSTEH#	RSTEP#	P17
V14	V33	V33	V5	P40	GREEN VIDEO	RED VIDEO	P18
V15	V33	V33	V6	P41	GND	GND	P19
V16	V5	V12	V7	P42	HSYNC	BLUE VIDEO	P20
V17	V5	V12	V8	P43	VSYNC	GND	P21
V18	V5	V12	V9	P44	DDC2: SCL	DDC2: SDA	P22

FIGURE 28

Pin No.	Symbol	Signal	Standard	Description
P2	PDR0 +	LVDS		Peripheral data reverse 0 +
P3	PDR0 -	LVDS		Peripheral data reverse 0 -
P5	PDR1 +	LVDS		Peripheral data reverse 1 +
P6	PDR1 -	LVDS		Peripheral data reverse 1 -
P8	PDR2 +	LVDS		Peripheral data reverse 2 +
P9	PDR2 -	LVDS		Peripheral data reverse 2 -
P11	PCKR +	LVDS		Peripheral clock reverse +
P12	PCKR -	LVDS		Peripheral clock reverse -
P15	PDR3 +	LVDS		Peripheral data reverse 3 +
P16	PDR3 -	LVDS		Peripheral data reverse 3 -
P24	PD0 +	LVDS		Peripheral data 0 +
P25	PD0 -	LVDS		Peripheral data 0 -
P27	PD1 +	LVDS		Peripheral data 1 +
P28	PD1 -	LVDS		Peripheral data 1 -
P30	PD2 +	LVDS		Peripheral data 2 +
P31	PD2 -	LVDS		Peripheral data 2 -
P33	PCK +	LVDS		Peripheral clock +
P34	PCK -	LVDS		Peripheral clock -
P37	PD3 +	LVDS		Peripheral data 3 +
P38	PD3 -	LVDS		Peripheral data 3 -
P13	Config 0	Static	3.3v or GND	Configuration bit 0
P35	Config 1	Static	3.3v or GND	Configuration bit 1
P17	RESTEP#	TTL	3.3v	Reset and Parity Error from console to ACM
P39	RESTEH#	TTL	3.3v	Reset and Parity Error from ACM to console
P18	Red Video	Analog		Video
P40	Green Video	Analog		Video
P20	Blue Video	Analog		Video
P42	HSYNC	TTL		Horizontal Sync
P43	VSYNC	TTL		Vertical Sync
P44	DDC2 SCL	TTL	VESA DDC std 2	DDC Clock
P22	DDC2 SDA	TTL	VESA DDC std 2	DDC Data
P1,P4,P7,P10, P14,P19,P21, P23,P26,P29, P32,P36,P41	GND		GND	Ground

FIGURE 29

Pin No.	Symbol	Signal	Standard	Description
E2	VPD+/TPA+		LVDS or 1394	Video capture port data or 1394
E3	VPD-/TPA-		LVDS or 1394	Video capture port data or 1394
E5	VPCK+/TPA+		LVDS or 1394	Video capture port data or 1394
E6	VPCK-/TPA-		LVDS or 1394	Video capture port data or 1394
E15	D0 +	TMDS	VESA P & D	Data 0 +
E16	D0 -	TMDS	VESA P & D	Data 0 -
E18	CLK +	TMDS	VESA P & D	Clock +
E19	CLK -	TMDS	VESA P & D	Clock -
E21	D1 +	TMDS	VESA P & D	Data 1 +
E22	D1 -	TMDS	VESA P & D	Data 1 -
E24	D2 +	TMDS	VESA P & D	Data 2 +
E25	D2 -	TMDS	VESA P & D	Data 2 -
E13	Config 2			Configuration bit 2
E26	Config 3			Configuration bit 3
E1, E4, E14, E17,E20,E23	GND		GND	Ground

E7	Reserved			Reserved
E8	Reserved			Reserved
E9	Reserved			Reserved
E10	TV-CV/reserved		NTSC	TV Composite Video or reserved
E11	SV Y/reserved		Super Video	SV Luminance or reserved
E12	SV C/reserved		Super Video	SV Chrominance or reserved

FIGURE 30

	Symbol	Signal	Data Rate	Description
1	PD0 RTN			GND
2	PD0 +	Synch. To PCK	6 x clock rate	Computer to Peripheral LVDS Data 0 +
3	PD0 -			Computer to Peripheral LVDS Data 0 -
4	PD1 RTN			GND
5	PD1 +	Synch. To PCK	6 x clock rate	Computer to Peripheral LVDS Data 1 +
6	PD1 -			Computer to Peripheral LVDS Data 1 -
7	PD2 RTN			GND
8	PD2 +	Synch. To PCK	6 x clock rate	Computer to Peripheral LVDS Data 2 +
9	PD2 -			Computer to Peripheral LVDS Data 2 -
10	PD3 RTN			GND
11	PD3 +	Synch. To PCK	6 x clock rate	Computer to Peripheral LVDS Data 3 +
12	PD3 -			Computer to Peripheral LVDS Data 3 -
13	PCK RTN			GND
14	PCK +	Clock	Clock rate	Computer to Peripheral LVDS Clock +
15	PCK -			Computer to Peripheral LVDS Clock -
16	PDR0 RTN			GND
17	PDR0 +	Synch. To PCKR	6 x clock rate	Peripheral to Computer LVDS Data 0 +
18	PDR0 -			Peripheral to Computer LVDS Data 0 -
19	PDR1 RTN			GND
20	PDR1 +	Synch. To PCKR	6 x clock rate	Peripheral to Computer LVDS Data 1 +
21	PDR1 -			Peripheral to Computer LVDS Data 1 -
22	PDR2 RTN			GND
23	PDR2 +	Synch. To PCKR	6 x clock rate	Peripheral to Computer LVDS Data 2 +
24	PDR2 -			Peripheral to Computer LVDS Data 2 -
25	PDR3 RTN			GND
26	PDR3 +	Synch. To PCKR	6 x clock rate	Peripheral to Computer LVDS Data 3 +
27	PDR3 -			Peripheral to Computer LVDS Data 3 -
28	PCKR RTN			GND
29	PCK +	Reverse Dir. Clock	Clock rate	Peripheral to Computer LVDS Clock +
30	PCK -			Peripheral to Computer LVDS Clock -
31	RESTEH#	Host to Peripheral	asynchronous	Reset & Error signal
32	RESTEP#	Peripheral to Host	asynchronous	Reset & Error signal

FIGURE 31

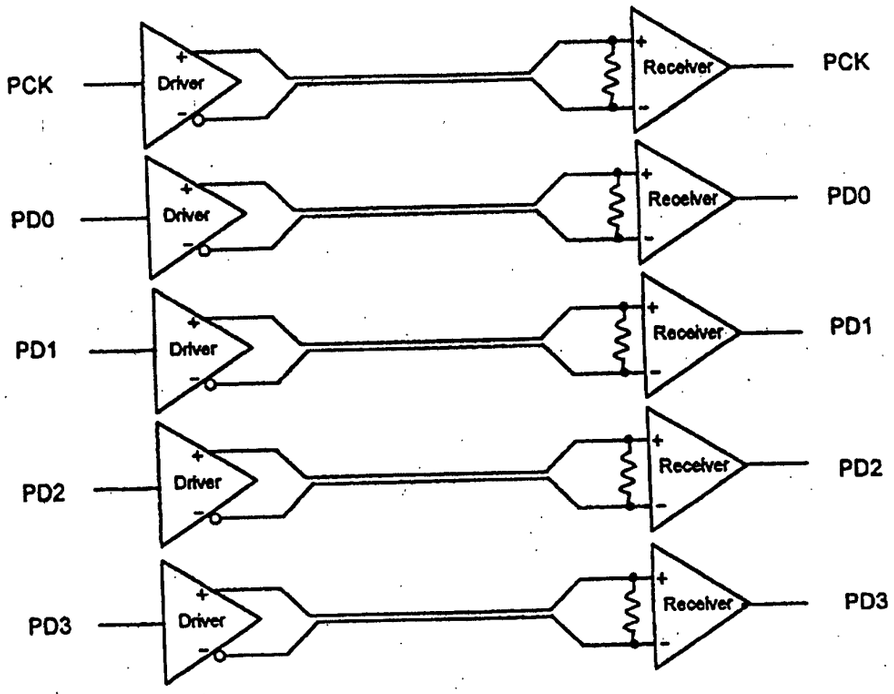

PCK
Driver
Receiver
PCK
PD0
Driver
Receiver
PD0
PD1
Driver
Receiver
PD1
PD2
Driver
Receiver
PD2
PD3
Driver
Receiver
PD3

FIGURE 32

Master	Type	HMA1/HMD1	HMA2/HMD2	HMC1	HMC2	Resvd	NOOP
	1st nibble	XX00 (PCI)	XX10 (PCI)	1001 (Control)	1101 (Control)	X011	1111
	2nd nibble	C/BE	Control bits	Control bits	Control bits		
	3rd to 6th	PCI A/D 1st seg.	PCI A/D 2nd seg.	Control 1st seg.	Control 2nd seg.	Other	Void
Target	Type	HTD1	HTD2	HTC1	HTC2	Resrd	NOOP
	1st nibble	XX00	XX10	0001 (Control)	0101 (Control)	X011	1111
	2nd nibble	BE	Control bits	Control bits	Control bits		
	3rd to 6th	PCI D 1st seg.	PCI D 2nd seg.	Control 1st seg.	Control 2nd seg.	Other	Void

FIGURE 33

Master	Type	PMA1 / PMD1	PMA2 / PMD2	PMC1	PMC2	Resvd	NOOP
	1st nibble	XX00 (PCI)	XX10 (PCI)	X001(Control)	X101(Control)	X011	1111
	2nd nibble	C/BE	Control bits	Control bits	Control bits		
	3rd to 6th	PCI A/D 1st seg.	PCI A/D 2nd seg.	Control 1st seg.	Control 2nd seg.	Other	Void
Target	Type	PTD1	PTD2	PTC1	PTC2	Resvd	NOOP
	1st nibble	XX00	XX10	X001(Control)	X101 (Control)	X011	1111
	2nd nibble	BE	Control bits	Control bits	Control bits		
	3rd to 6th	PCI D 1st seg.	PCI D 2nd seg.	Control 1st seg.	Control 2nd seg.	Other	Void

FIGURE 34

ID bits (P0 P1 P2 P3)	Data Packet Type
X X 0 0	PCI 1st address/data segment
X X 1 0	PCI 2nd address/data segment
0 0 0 1	Control 1st segment with PCI response
1 0 0 1	Control 1st segment without PCI response
0 1 0 1	Control 2nd segment with PCI response
1 1 0 1	Control 2nd segment without PCI response
0 0 1 1	Reserved
1 0 1 1	Reserved
0 1 1 1	Initialization
1 1 1 1	NOOP

FIGURE 35

	PD0	PD1	PD2	PD3
1st control /ID (HMA1 or HMD1)	FRAME#	IRDY#	0: 1st data seg.	0: PCI; Other=1
2nd control	C/BE0#	C/BE1#	C/BE2#	C/BE3#
1st Data Segment	A/D0	A/D8	A/D16	A/D24
1st Data Segment	A/D1	A/D9	A/D17	A/D25
1st Data Segment	A/D2	A/D10	A/D18	A/D26
1st Data Segment	A/D3	A/D11	A/D19	A/D27
3rd control /ID (HMA2 or HMD2)	PAR (PCI)	LOCK#	1: 2nd data seg.	0: PCI; Other=1
4th control	GNT#	reserved	reserved	Cntl PAR (CMI)
2nd Data Segment	A/D4	A/D12	A/D20	A/D28
2nd Data Segment	A/D5	A/D13	A/D21	A/D29
2nd Data Segment	A/D6	A/D14	A/D22	A/D30
2nd Data Segment	A/D7	A/D15	A/D23	A/D31

FIGURE 36

	PD0	PD1	PD2	PD3
1st control /ID (PMA1 or PMD1)	FRAME#	IRDY#	0: 1st data seg.	0: PCI; Other=1
2nd control	C/BE0#	C/BE1#	C/BE2#	C/BE3#
1st Data Segment	A/D0	A/D8	A/D16	A/D24
1st Data Segment	A/D1	A/D9	A/D17	A/D25
1st Data Segment	A/D2	A/D10	A/D18	A/D26
1st Data Segment	A/D3	A/D11	A/D19	A/D27
3rd control /ID (PMA2 or PMD2)	PAR (PCI)	LOCK#	1: 2nd data seg.	0: PCI; Other=1
4th control	GNT#	reserved	reserved	Cntl PAR (CMI)
2nd Data Segment	A/D4	A/D12	A/D20	A/D28
2nd Data Segment	A/D5	A/D13	A/D21	A/D29
2nd Data Segment	A/D6	A/D14	A/D22	A/D30
2nd Data Segment	A/D7	A/D15	A/D23	A/D31

FIGURE 37

	PD0	PD1	PD2	PD3
1st control /ID (HTD1 or PTD1)	1	1	0: 1st data seg.	0: PCI; Other=1
2nd control	reserved	reserved	reserved	reserved
1st Data Segment	D0	D8	D16	D24
1st Data Segment	D1	D9	D17	D25
1st Data Segment	D2	D10	D18	D26
1st Data Segment	D3	D11	D19	D27
3rd control /ID (HTD2 or PTD2)	PAR (PCI)	reserved	1: 2nd data seg.	0: PCI; Other=1
4th control	GNT#	reserved	reserved	Cntl PAR (CMI)
2nd Data Segment	D4	D12	D20	D28
2nd Data Segment	D5	D13	D21	D29
2nd Data Segment	D6	D14	D22	D30
2nd Data Segment	D7	D15	D23	D31

FIGURE 38

33Mhz PCI Read transaction:

H > P	HMA1	HMA2	NOOP	NOOP	.....	.....	NOOP	NOOP	HMC1	NOOP
P > H	NOOP	NOOP	PTC1	NOOP	.....	.....	PTD1	PTD2	NOOP	NOOP

FIGURE 39

33 Mhz PCI Write transaction:

H > P	HMA1	HMA2	NOOP	NOOP	HMD1	HMD2	NOOP	NOOP	HMD1	HMD2	NOOP
P > H	NOOP	NOOP	PTC1	NOOP	NOOP	NOOP	PTC2	NOOP	NOOP	NOOP	PTC1

FIGURE 40

Peripheral to Host: PCI Target (on XPBus) Control data packets with PCI response :

	PD0	PD1	PD2	PD3
ID (PTC1)	0: PCI	0: 1st control seg.	0: Control	1: Other
PCI Control Segment	PERR#	SERR#	REQ#	STOP#
CMI Control Segment	CMI PERR#	Buffer Full #	CMI REQ#	CMI GNT#
CPU 1st Control Segment	CPURST	INIT	reserved	reserved
CPU 2nd Control Segment	INTR	NMI	A20M#	IGNNE#
CPU 3rd Control Segment	SMI#	STPCLK#	SLP#	PAR (Cntl Packet)

ID (PTC2)	0: PCI	1: 2nd control seg.	0: Control	1: Other
PCI Control Segment	PERR#	SERR#	REQ#	STOP#
CMI Control Segment	CMI PERR#	Buffer Full #	CMI REQ#	CMI GNT#
NB 1st Control Segment	SUSCLK	SUSSTAT1#	PHOLD#	
GPIO 1st Control Segment	GPIO (0)	GPIO (1)	GPIO (2)	GPIO (3)
GPIO 2nd Control Segment	GPIO (4)	GPIO (5)	reserved	PAR (Cntl Packet)

FIGURE 41

Peripheral to Host: PCI Target (on XPBus) Control data packets without PCI response :

	PD0	PD1	PD2	PD3
ID (PTC1)	1: No PCI	0: 1st control seg.	0: Control	1: Other
PCI Control Segment	reserved	reserved	reserved	reserved
CMI Control Segment	CMI PERR#	Buffer Full #	CMI REQ#	CMI GNT#
CPU 1st Control Segment	CPURST	INIT	reserved	reserved
CPU 2nd Control Segment	INTR	NMI	A20M#	IGNNE#
CPU 3rd Control Segment	SMI#	STPCLK#	SLP#	PAR (Cntl Packet)

ID (PTC2)	1: No PCI	1: 2nd control seg.	0: Control	1: Other
PCI Control Segment	reserved	reserved	reserved	reserved
CMI Control Segment	CMI PERR#	Buffer Full #	CMI REQ#	CMI GNT#
NB 1st Control Segment	SUSCLK	SUSSTAT1#	PHOLD#	
GPIO 1st Control Segment	GPIO (0)	GPIO (1)	GPIO (2)	GPIO (3)
GPIO 2nd Control Segment	GPIO (4)	GPIO (5)	reserved	PAR (Cntl Packet)

FIGURE 42

Peripheral to Host: PCI Master (on XPBus) Control data packets with PCI response:

	PD0	PD1	PD2	PD3
ID (PMC1)	0: PCI	0: 1st control seg.	0: Control	1: Other
PCI Control Segment	PERR#	SERR#	reserved	reserved
CMI Control Segment	CMI PERR#	Buffer Full #	CMI REQ#	CMI GNT#
CPU 1st Control Segment	CPURST	INIT	reserved	reserved
CPU 2nd Control Segment	INTR	NMI	A20M#	IGNNE#
CPU 3rd Control Segment	SMI#	STPCLK#	SLP#	PAR (Cntl Packet)

ID (PMC2)	0: PCI	1: 2nd control seg.	0: Control	1: Other
PCI Control Segment	PERR#	SERR#	reserved	reserved
CMI Control Segment	CMI PERR#	Buffer Full #	CMI REQ#	CMI GNT#
NB 1st Control Segment	SUSCLK	SUSSTAT1#	PHOLD#	reserved
GPIO 1st Control Segment	GPIO (0)	GPIO (1)	GPIO (2)	GPIO (3)
GPIO 2nd Control Segment	GPIO (4)	GPIO (5)	reserved	PAR (Cntl Packet)

FIGURE 43

Peripheral to Host: PCI Master (on XPBus) Control data packets without PCI response:

	PD0	PD1	PD2	PD3
ID (PMC1)	1: No PCI	0: 1st control seg.	0: Control	1: Other
PCI Control Segment	reserved	reserved	reserved	reserved
CMI Control Segment	CMI PERR#	Buffer Full #	CMI REQ#	CMI GNT#
CPU 1st Control Segment	CPURST	INIT	reserved	reserved
CPU 2nd Control Segment	INTR	NMI	A20M#	IGNNE#
CPU 3rd Control Segment	SMI#	STPCLK#	SLP#	PAR (Cntl Packet)

ID (PMC2)	1: No PCI	1: 2nd control seg.	0: Control	1: Other
PCI Control Segment	reserved	reserved	reserved	reserved
CMI Control Segment	CMI PERR#	Buffer Full #	CMI REQ#	CMI GNT#
NB 1st Control Segment	SUSCLK	SUSSTAT1#	PHOLD#	reserved
GPIO 1st Control Segment	GPIO (0)	GPIO (1)	GPIO (2)	GPIO (3)
GPIO 2nd Control Segment	GPIO (4)	GPIO (5)	reserved	PAR (Cntl Packet)

FIGURE 44

Host to Peripheral: Target Control data packet :

	PD0	PD1	PD2	PD3
ID (HTC1)	0: PCI Target	0: 1st segment	0: Control	1: Other
PCI Control Segment	PERR#	SERR#	REQ#	STOP#
CMI Control Segment	CMI PERR#	Buffer Full #	CMI REQ#	CMI GNT#
CPU 1st Control Segment	FERR#	reserved	reserved	reserved
Reserved				
Reserved				

HTC2 is reserved for future use.

FIGURE 45

Host to Peripheral: Master Control data packet :

	PD0	PD1	PD2	PD3
ID (HMC1)	1: PCI Master	0: 1st segment	0: Control	1: Other
PCI Control Segment	PERR#	SERR#	reserved	reserved
CMI Control Segment	CMI PERR#	Buffer Full #	CMI REQ#	CMI GNT#
CPU 1st Control Segment	FERR#	reserved	reserved	reserved
Reserved				
Reserved				

HMC2 is reserved for future use.

FIGURE 46

Host PCI Bus Signal (50 pins)

Name	Type	Pins	Description
AD[31::0]	TS	32	Multiplexed Address/Data. AD is driven to a valid state when GNT# is asserted.
C/BE[3::0]#	TS	4	Multiplexed Command/Byte Enables. For a two-address transaction, 1st address phase carries the command, and the 2nd address phase carries the transaction type. C/BE is driven to a valid state when GNT# is asserted.
FRAME#	STS	1	Indicates beginning and duration of a PCI transaction. When the bus is idle, FRAME# is driven to High for 1 cycle. A pull-up resistor sustains STS signal.
IRDY#	STS	1	Initiator Ready. IRDY# is driven High for 1 cycle if bus is idle, and the state is sustained by a pull-up resistor.
TRDY#	STS	1	Target Ready. When bus is idle, TRDY# is driven High for 1 cycle if bus is idle. An external pull-up resistor sustains STS signal.
DEVSEL#	STS	1	Device Select. DEVSEL# is asserted by target to indicate it is ready to accept the transaction. HIC decodes address of a transaction to decide the need to assert DEVSEL#. As an initiator, HIC waits for 5 cycles to detect assertion of DEVSEL# by the target; otherwise HIC terminates with a master abort. DEVSEL# is driven High for 1 cycle when bus is idle, and the state is sustained by a pull-up resistor.
STOP#	STS	1	Target request to stop transaction. There are 3 cases: STOP#, TRDY# & DEVSEL# asserted: disconnect with data transfer Only STOP# & DEVSEL# asserted: request initiator to retry later Only STOP# asserted: target abort STOP# is driven High for 1 cycle when bus is idle, and the state is sustained by a pull-up resistor.
PAR	TS	1	Even parity for 36 bits of AD & C/BE#. PAR is sent one cycle after address or data is valid. In write transaction, initiator sends PAR one cycle after write data is valid. In read transaction, target sends PAR one cycle after read data is valid.
LOCK#	Input	1	Initiator request lock on target downstream. LOCK# is asserted 1 clock cycle after address phase by an initiator wanting to perform an atomic operation that take more than one transaction to complete. HIC passes the LOCK# request to the secondary PCI bus. HIC does not drive LOCK# or propagate LOCK# upstream.
IDSEL#	Input	1	Chip Select for Type 0 configuration access. During a Type 0 configuration transaction, the initiator asserts IDSEL# during the address phase to select HIC. HIC responds by asserting DEVSEL#.
PERR#	STS	1	Data Parity Error on all transactions except Special Cycle. PERR# is driven one clock cycle after PAR. PERR# is asserted by target during write transactions, and by initiator during read transactions.
SERR#	OD	1	System Error. HIC asserts SERR# under the following conditions: Address parity error, Secondary bus SERR# asserted, Posted write transaction: data parity error on target bus, Posted write transaction discarded, Master abort, Target abort Delayed read or write transaction discarded, and Delayed transaction master timeout.
REQ#	TS	1	Request for bus. If a target retry or disconnect is received in response to initiating a transaction, HIC deasserts REQ# for at least 2 cycles before asserting it again.
GNT#	Input	1	Bus is granted to HIC. HIC can initiate transaction if GNT# is asserted and the bus is idle. When HIC is not requesting bus and GNT# is asserted, HIC must drive AD, C/BE, and PAR to valid logic levels.
CLKRUN#	I/OD	1	Input indicating clock status. HIC can request the central clock resource to start, speed up or maintain the PCI clock. There are 3 clocking states: Clock running, Clock about to stop/slow down, and Clock stopped/slowed.
PCICK	Input	1	PCI Clock. All inputs are sampled on the rising edge of PCICK. Frequency range from 0 to 33Mhz.

FIGURE 47

XPBus Signals

Name	Type	Pins	Description
PCK ±	LVDS Output	2	Peripheral Clock Differential Signal Pair Output to XPBus
PD{3::0] ±	LVDS Output	8	Peripheral Data Differential Signal Pair Output to XPBus
PCN ±	LVDS Output	2	Peripheral Control Differential Signal Pair Output to XPBus
PCKR ±	LVDS Input	2	Peripheral Clock Differential Signal Pair Input from XPBus
PDR{3::0] ±	LVDS Input	8	Peripheral Data Differential Signal Pair Input from XPBus
PCNR ±	LVDS Input	2	Peripheral Control Differential Signal Pair Input from XPBus

FIGURE 48

XIS Bus Video Port Signals

Name	Type	Pins	Description
VPCK ±	LVDS Input	2	Video Port Clock Differential Signal Pair Input; 2 x Video clock rate
PCK ±	LVDS Output	2	Video Port Data Differential Signal Pair Input; 10 bit/clock period

FIGURE 49

Video Port Signals

Name	Type	Pins	Description
VPD [15::0]	Output	16	Video Port Data Output
VREF	Output	1	Vertical Reference
HREF	Output	1	Horizontal Reference
VCLK	Output	1	Video Pixel Clock
VRDY	Output	1	Video Source Ready

FIGURE 50

Flash Memory Interface Signals

Name	Type	Pins	Description
A[18::0]	Output	19	Address for up to 512K x 8 Memory
DQ[7::0]	I/O	8	Data Input/Output
CE#	O	1	Chip Enable
WE#	O	1	Write Enable
OE#	O	1	Output Enable
WP#	O	1	Write protect

FIGURE 51

Test Port (JTAG) Signals

Name	Type	Pins	Description
TCK	I	1	Test Clock
TDI	I	1	Test Data In
TDO	O	1	Test Data Out
TMS	I	1	Test Mode Select

FIGURE 52

CPU Signals

Name	Type	Pins	Description
CPURST	I/OD	1	CPU Reset and PCI RST#
FERR#	I	1	Numeric Coprocessor Error
IGNNE#	OD	1	Ignore Numeric Exception
INIT	OD	1	Initialization
INTR	OD	1	CPU Interrupt; Pentium: active high; PII active low
A20M#	OD	1	Address 20 Mask; Keyboard Interface
NMI	OD	1	Non-Maskable Interrupt
SMI#	OD	1	System Management Interrupt
STPCLK#	OD	1	Stop Clock
SLP#	OD	1	Sleep

FIGURE 53

North Bridge Signals

Name	Type	Pins	Description
SUSCLK	O	1	Suspend Clock from South Bridge. 32.768Khz for maintenance of DRAM Refresh.
SUSSTAT1#	O	1	Suspend Status Plane 1
PHOLD#	O	1	PCI Hold
PHLDA#	I	1	PCI Hold Acknowledge

FIGURE 54

GPIO Signals

Name	Type	Pins	Description
GPIO[0]	O	1	CPU_STP# - CPU Clock Stop (optional)
GPIO[1]	O	1	PCI_STP# - PCI Clock Stop (optional)
GPIO[7::2]	I/O	6	General Purpose Input/Output Signals

FIGURE 55

ERROR/RESET Signals

Name	Type	Pins	Description
RSTEH	O	1	Signal uses for: Reset from Host, Parity error for PIC transmission, & no connect detection
RSTEP	I	1	Signal uses for: Reset from Peripheral, Parity error for HIC transmission, No connect detection

FIGURE 56

Power/Ground/OSC input Signals

Name	Type	Pins	Description
OSCin	I	1	Oscillator input for LVDS clock
GND (PLL)		1	PLL ground
VCC (PLL)		1	PLL 3.3v
VCC (core)		2	Core/CPU VCC = 3.3v
VCC (LVDS)		2	LVDS VCC = 3.3v
VCC (VP)		1	Video port: all output signals; VCC = 3.3v
VCC (PCI)		2	PCI VCC = 5v tolerant or 3.3v
VCC (Flash)		1	Flash memory VCC = 5v tolerant or 3.3v
GND (core)		2	Core ground
GND (LVDS)		2	LVDS ground
GND (PCI)		2	PCI ground
GND (Flash)		1	Flash memory ground
Reserved		1	Reserved pins

FIGURE 57

Transaction History Date 1998-09-28
Date information retrieved from USPTO Patent Application Information Retrieval (PAIR) system records at www.uspto.gov

BEST COPY

UNITED STATES DEPARTMENT OF COMMERCE
Patent and Trademark Office
Address: COMMISSIONER OF PATENTS AND TRADEMARKS
Washington, D.C. 20231

APPLICATION NUMBER	09 FILING/RECEIPT DATE	FIRST NAMED APPLICANT	ATTORNEY DOCKET NO./TITLE
			38711200030

0262/0928 #2

MORRISON & FOERSTER
425 MARKET STREET
SAN FRANCISCO CA 94105-2482

NOT ASSIGNED

2782

DATE MAILED: 09/28/98

NOTICE TO FILE MISSING PARTS OF APPLICATION
Filing Date Granted

An Application Number and Filing Date have been assigned to this application. The items indicated below, however, are missing. Applicant is given TWO MONTHS FROM THE DATE OF THIS NOTICE within which to file all required items and pay fees required below to avoid abandonment. Extensions of time may be obtained by filing a petition accompanied by the extension fee under the provisions of 37 CFR 1.136(a). **If any of items 1 or 3 through 5 are indicated as missing, the SURCHARGE set forth in 37 CFR 1.16(e) of ☐ $65.00 for a small entity in compliance with 37 CFR 1.27, or ☐ $130.00 for a non-small entity, must also be timely submitted in reply to this NOTICE to avoid abandonment.**

If all required items on this form are filed within the period set above, the total amount owed by applicant as a ☐ small entity (statement filed) ☐ non-small entity is $ 1016.

☐ 1. The statutory basic filing fee is:
- ☐ missing.
- ☐ insufficient.

Applicant must submit $ 790 to complete the basic filing fee and/or file a small entity statement claiming such status (37 CFR 1.27).

☐ 2. Additional claim fees of $_____, including any multiple dependent claim fees, are required.
- $ 492 for 6 independent claims over 3.
- $ 484 for 22 dependent claims over 20.
- $_____ for multiple dependent claim surcharge.

Applicant must either submit the additional claim fees or cancel additional claims for which fees are due.

☐ 3. The oath or declaration:
- ☐ is missing or unexecuted.
- ☐ does not cover the newly submitted items.
- ☐ does not identify the application to which it applies.
- ☐ does not include the city and state or foreign country of applicant's residence.

An oath or declaration in compliance with 37 CFR 1. 63, including residence information and identifying the application by the above Application Number and Filing Date is required.

☐ 4. The signature(s) to the oath or declaration is/are by a person other than inventor or person qualified under 37 CFR 1.42, 1.43 or 1.47.
A properly signed oath or declaration in compliance with 37 CFR 1.63, identifying the application by the above Application Number and Filing Date, is required.

☐ 5. The signature of the following joint inventor(s) is missing from the oath or declaration:

_____

An oath or declaration in compliance with 37 CFR 1.63 listing the names of all inventors and signed by the omitted inventor(s), identifying this application by the above Application Number and Filing Date, is required.

☐ 6. A $50.00 processing fee is required since your check was returned without payment (37 CFR 1.21(m)).
☐ 7. Your filing receipt was mailed in error because your check was returned without payment.
☐ 8. The application does not comply with the Sequence Rules.
See attached "Notice to Comply with Sequence Rules 37 CFR 1.821-1.825."
☐ 9. OTHER: _____

Direct the reply and any questions about this notice to "Attention: Box Missing Parts."

A copy of this notice MUST be returned with the reply.

Customer Service Center
Initial Patent Examination Division (703) 308-1202

PART 3 - OFFICE COPY

FORM PTO-1533 (REV 9-97)

SECTOR # #3

OIPE JC57 OCT 27 1998 PATENT & TRADEMARK OFFICE

PATENT
Docket No. 387112000300

CERTIFICATE OF MAILING BY "FIRST CLASS MAIL"

I hereby certify that this correspondence is being deposited with the United States Postal Service as first class mail in an envelope addressed to: Assistant Commissioner for Patents, Washington, D.C. 20231, on October 23, 1998.

Valerie L. Cohen

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In the application of:

WILLIAM W. Y. CHU

Serial No.: 09/149,882

Filing Date: September 8, 1998

For: A COMMUNICATION CHANNEL AND INTERFACE DEVICES FOR BRIDGING COMPUTER INTERFACE BUSES

Examiner: Not Assigned

Group Art Unit: 2782

TRANSMITTAL LETTER FOR MISSING PARTS OF APPLICATION

Box MISSING PARTS
Assistant Commissioner for Patents
Washington, D.C. 20231

Dear Sir:

In complete response to the Notice to File Missing Parts of Application Under 37 C.F.R. § 1.53(d) dated September 28, 1998, attached please find:

- ☐ A combined Declaration and Power of Attorney signed by the inventor and the surcharge of $130.00 as set forth in 37 C.F.R. § 1.16(e).
- ☒ A declaration signed by the inventor and the surcharge of $130.00 as set forth in 37 C.F.R. § 1.16(e).
- ☒ A Power of Attorney and Prosecution by Assignee Under 37 C.F.R. § 3.71.
- ☒ A Declaration of Small Entity Status.
- ☐ A Petition for Extension of Time.
- ☐ A verified English translation of the application, and the $130.00 fee as set forth in 37 C.F.R. § 1.17(k).

sf-590970

☒ Sole Assignment (copy).

☒ Other: Certificate Under 37 C.F.R. §3.73(b) and Return Receipt Postcard.

The filing fee has been calculated as follows:

FOR	NUMBER FILED	NUMBER EXTRA	RATE	CALCULATIONS
TOTAL CLAIMS	42 - 20 =	22	x $22.00	$484.00
INDEPENDENT CLAIMS	9 - 3 =	6	x $82.00	$492.00
MULTIPLE DEPENDENT CLAIM(S) (if applicable)			+ $270.00	$
			BASIC FEE	$790.00
		TOTAL OF ABOVE CALCULATIONS =		$1,766.00
Reduction by 1/2 for filing by small entity (Note 37 C.F.R. §§ 1.9, 1.27, 1.28). If applicable, verified statement must be attached.				$883.00
SURCHARGE FOR FILING MISSING PARTS				$130.00
			TOTAL =	$1,013.00

☒ A check in the amount of $1,013.00 is attached.

☐ Charge $ to **Deposit Account No. 03-1952**.

The Assistant Commissioner is hereby authorized to charge any additional fees under 37 C.F.R. §§ 1.16 and 1.17 that may be required by this transmittal and associated documents, or to credit any overpayment to **Deposit Account No. 03-1952** referencing Docket No. 387112000300.

Respectfully submitted,

Dated: Oct. 23, 1998

By: Ararat Kapouytian
Ararat Kapouytian
Registration No. 40,044

Morrison & Foerster LLP
425 Market Street
San Francisco, California 94105-2482
Telephone: (415) 268-6147
Facsimile: (415) 268-7522

OIPE JC57
OCT 27 1998
PATENT & TRADEMARK OFFICE

09/149882 #3

PATENT
Docket No. 387112000300

DECLARATION FOR UTILITY PATENT APPLICATION

AS A BELOW-NAMED INVENTOR, I HEREBY DECLARE THAT:

My residence, post office address, and citizenship are as stated below next to my name.

I believe I am the original, first and sole inventor of the subject matter which is claimed and for which a patent is sought on the invention entitled: A COMMUNICATION CHANNEL AND INTERFACE DEVICES FOR BRIDGING COMPUTER INTERFACE BUSES, the specification of which is attached hereto unless the following box is checked:

☒ was filed on September 8, 1998 as United States Application Serial No. 09/149,882 and was amended on * (if applicable).

I HEREBY STATE THAT I HAVE REVIEWED AND UNDERSTAND THE CONTENTS OF THE ABOVE-IDENTIFIED SPECIFICATION, INCLUDING THE CLAIMS, AS AMENDED BY ANY AMENDMENT REFERRED TO ABOVE.

I acknowledge the duty to disclose information which is material to the patentability as defined in 37 C.F.R. § 1.56.

I hereby claim foreign priority benefits under 35 U.S.C. § 119(a)-(d) or § 365(b) of any foreign application(s) for patent or inventor's certificate, or § 365(a) of any PCT International application which designated at least one country other than the United States listed below and have also identified below, by checking the box, any foreign application for patent or inventor's certificate, or PCT International application having a filing date before that of the application on which priority is claimed:

Application No.	Country	Date of Filing (day/month/year)	Priority Claimed?
*			☐Yes ☐No

I hereby claim benefit under 35 U.S.C. § 119(e) of any United States provisional application(s) listed below:

Application Serial No.	Filing Date
60/083,886	May 1, 1998
60/092,706	July 14, 1998

I hereby claim the benefit under 35 U.S.C. § 120 of any United States application(s), or § 365(c) of any PCT International application designating the United States, listed below and, insofar as the subject matter of each of the claims of this application is not disclosed in the prior United States or PCT International application in the manner provided by the first paragraph of 35 U.S.C. § 112, I acknowledge the duty to disclose information which is material to

patentability as defined in 37 C.F.R. § 1.56 which became available between the filing date of the prior application and the national or PCT International filing date of this application.

Application Serial No.	Filing Date	Status
*		☐Patented ☐Pending ☐Abandoned

I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under § 1001 of Title 18 of the United States Code and that such willful false statements may jeopardize the validity of the application or any patent issued thereon.

10/16/98 William W. Y. Chu

Date

Name: William W. Y. Chu
Residence: Los Altos, California
Citizenship: U.S. Citizen
Post Office Address: 1320 Miravalle Avenue, Los Altos, CA 94024

OIPE JC57
OCT 27 1998
PATENT & TRADEMARK OFFICE

PATENT
Docket No. 387112000300

CERTIFICATE OF MAILING BY "FIRST CLASS MAIL"

I hereby certify that this correspondence is being deposited with the United States Postal Service as first class mail in an envelope addressed to: Assistant Commissioner for Patents, Washington, D.C. 20231, on Oct 23, 1998.

Valerie Cohen
Valerie Cohen

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In the application of:

William W. Y. Chu

Serial No.: 09/149,882

Filing Date: September 8, 1998

For: A COMMUNICATION CHANNEL AND INTERFACE DEVICES FOR BRIDGING COMPUTER INTERFACE BUSES

Examiner: Not Assigned

Group Art Unit: 2782

PROSECUTION BY ASSIGNEE AND POWER OF ATTORNEY UNDER 37 C.F.R. § 3.71

Assistant Commissioner for Patents
Washington, D.C. 20231

Dear Sir:

Acqis Technology, Inc., the assignee of the entire right, title and interest in this patent application, under 37 C.F.R. § 3.71 hereby appoints:

Thomas E. Ciotti (Reg No. 21,013)
Gladys H. Monroy (Reg No. 32,430)
E. Thomas Wheelock (Reg No. 28,825)
Shmuel Livnat (Reg No. 33,949)
Antoinette F. Konski (Reg No. 34,202)
David C. Lundmark (Reg No. P-42,815)
Mani Adeli (Reg No. 39,585)
Sean Brennan (Reg No. 39,917)
Robert K. Cerpa (Reg No. 39,933)
Alan W. Cannon (Reg No. 34,977)
Kate H. Murashige (Reg No. 29,959)
Debra A. Shetka (Reg No. 33,309)
Susan K. Lehnhardt (Reg No. 33,943)
Tyler Dylan (Reg No. 37,612)
Harry J. Macey (Reg No. 32,818)
Robert Saltzberg (Reg No. 36,910)
Catherine M. Polizzi (Reg No. 40,130)
J. Michael Schiff (Reg No. 40,253)
Lee K. Tan (Reg No. 39,447)
Madeline I. Johnston (Reg No. 36,174)

sf-584841

Dahna S. Pasternak (Reg No. 41,411)
Frank Wu (Reg No. 41,386)
Barry E. Bretschneider (Reg No. 28,055)
Mark R. Carter (Reg No. 39,131)
E. Victor Donahue (Reg No. 35,492)
Thomas G. Wiseman (Reg No. 35,046)
Ararat Kapouytian (Reg No. 40,044)
Nicholas Buffinger (Reg No. 39,124)
Paula A. Borden (Reg No. 42,344)
Jung-Hua Kuo (Reg No. 41,918)
Raj S. Davé (Reg No. P-42,465)
Richard D. Jordan (Reg No. 33,519)
Stephen C. Durant (Reg No. 31,506)
Hector Gallegos (Reg No. 40,614)
Charles D. Holland (Reg No. 35,196)
Michael Hetherington (Reg No. 32,357)
Thomas D. Mays (Reg No. 34,524)
Wen Liu (Reg No. 32,822)
Cindy S. Kaplan (Reg No. 40,043)
Richard D. Jordan (Reg No. 33,519)
Niki D. Cox (Reg No. 42,446)
William C. Revelos (Reg No. P-42,101)
Sean M. Fitzgerald (Reg No. 42,537)

all of Morrison & Foerster LLP, 425 Market Street, San Francisco, California 94105-2482, telephone (415) 268-7000, to prosecute this application and transact all matters in the United States Patent and Trademark Office connected therewith, said appointment to be to the exclusion of the inventors and their attorneys in accordance with the provisions of 37 C.F.R. § 3.71.

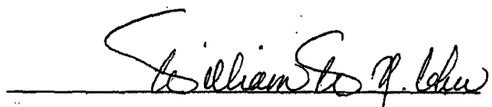
Please direct all written communications relative to this application to:

Ararat Kapouytian
Morrison & Foerster LLP
425 Market Street
San Francisco, California 94105-2482

Please direct all telephone communications to Ararat Kapouytian at (415) 268-6147.

Acqis Technology, Inc.
a California corporation

Dated: Oct. 22nd, 1998



Name: William W. Y. Chu
Title: President and CEO
Address: 1621 West El Camino Real
Mountain View, CA 94040

#4

OIPE JC57 OCT 27 1998 PATENT & TRADEMARK OFFICE

Applicant/Patentee: William W. Y. Chu
Serial No./Patent No.: 09/149,882
Filed on/Issued : September 8, 1998
Client Reference: 387112000300
For: A COMMUNICATION CHANNEL AND INTERFACE DEVICES FOR BRIDGING COMPUTER INTERFACE

VERIFIED STATEMENT CLAIMING SMALL ENTITY STATUS
37 C.F.R. §§ 1.9(f) AND 1.27(c) — SMALL BUSINESS CONCERN

I hereby declare that I am

☐ the owner of the small business concern identified below:
☒ an official of the small business concern empowered to act on behalf of the concern identified below:

NAME OF CONCERN: Acqis Technology, Inc.

ADDRESS OF CONCERN: 1621 West El Camino Real, Mountain View, CA 94040

I hereby declare that the above identified small business concern qualifies as a small business concern as defined in 13 C.F.R. § 121.12, and reproduced in 37 C.F.R. § 1.9(d), for purposes of paying reduced fees to the United States Patent and Trademark Office, in that the number of employees of the concern, including those of its affiliates, does not exceed 500 persons. For purposes of this statement, (1) the number of employees of the business concern is the average over the previous fiscal year of the concern of the persons employed on a full-time, part-time or temporary basis during each of the pay periods of the fiscal year, and (2) concerns are affiliates of each other when either, directly or indirectly, one concern controls or has the power to control the other, or a third party or parties controls or has the power to control both.

I hereby declare that rights under contract or law have been conveyed to and remain with the small business concern identified above with regard to the invention, entitled A COMMUNICATION CHANNEL AND INTERFACE DEVICES FOR BRIDGING COMPUTER INTERFACE BUSES by inventor(s) William W. Y. Chu
described in

☐ the specification filed herewith with title as listed above.
☒ the application identified above.
☐ the patent identified above.

If the rights held by the above identified business concern are not exclusive, each individual, concern or organization having rights in the invention must file separate verified statements averring to their status as small entities, and no rights to the invention are held by any person, other than the inventor, who would not qualify as an independent inventor under 37 C.F.R. § 1.9(c) if that person made the invention, or by any concern which would not qualify as a small business concern under 37 C.F.R. § 1.9(d), or a nonprofit organization under 37 C.F.R. § 1.9(e).

Each person, concern or organization having any rights in the invention is listed below:

☒ no such person, concern, or organization exists.
☐ each such person, concern or organization is listed below.

NAME	ADDRESS	TYPE
		☐ Individual ☐ Small Business Concern ☐ Nonprofit Organization

Separate verified statements are required from each named person, concern or organization having rights to the invention averring to their status as small entities. (37 C.F.R. § 1.27)

I acknowledge the duty to file, in this application or patent, notification or any change in status resulting in loss of entitlement to small entity status prior to paying, or at the time of paying, the earliest of the issue fee or any maintenance fee due after the date on which status as a small entity is no longer appropriate. (37 C.F.R. § 1.28(b))

I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under section 1001 of Title 18 of the United States Code, and that such willful false statements may jeopardize the validity of the application, any patent issuing thereon, or any patent to which this verified statement is directed.

NAME OF PERSON SIGNING: William W. Y. Chu
TITLE OF PERSON IF OTHER THAN OWNER: President and CEO
ADDRESS OF PERSON SIGNING: 1621 West El Camino Real, Mountain View, CA 94040

SIGNATURE: William W. Y. Chu DATE: 10/16/98

PTO/SB/10 (10-92)
sf-584838

Attorney Docket No. 387112000300

ASSIGNMENT
SOLE

COPY

THIS ASSIGNMENT, by William W. Y. Chu (hereinafter referred to as the assignor), residing at 1320 Miravalle Avenue, Los Altos, CA 94024, witnesseth:

WHEREAS, said assignor has invented certain new and useful improvements in A COMMUNICATION CHANNEL AND INTERFACE DEVICES FOR BRIDGING COMPUTER INTERFACE BUSES, set forth in an application for Letters Patent of the United States, having an oath or declaration executed on even date herewith; bearing Serial No. 09/149,882 and filed on September 8, 1998; and

WHEREAS, Acqis Technology, a corporation duly organized under and pursuant to the laws of California and having its principal place of business at 1621 West El Camino Real, Mountain View, CA 94040 (hereinafter referred to as the assignee) is desirous of acquiring the entire right, title and interest in and to said inventions and said application for Letters Patent of the United States, and in and to any Letters Patent or Patents, United States or foreign, to be obtained therefor and thereon:

NOW, THEREFORE, in consideration of One Dollar ($1.00) and other good and sufficient considerations, the receipt of which is hereby acknowledged, said assignor has sold, assigned, transferred and set over, and by these presents does sell, assign, transfer and set over, unto said assignee, its successors, legal representatives and assigns, the entire right, title and interest in and to the above-mentioned inventions, application for Letters Patent, and any and all Letters Patent or Patents in the United States of America and all foreign countries which may be granted therefor and thereon, and in and to any and all divisions, continuations and continuations-in-part of said application, or reissues or extensions of said Letters Patent or Patents, and all rights under the International Convention for the Protection of Industrial Property, the same to he held and enjoyed by said assignee, for its own use and the use of its successors, legal representatives and assigns, to the full end of the term or terms for which Letters Patent or Patents may be granted, as fully and entirely as the same would have been held and enjoyed by the assignor, had this sale and assignment not been made.

AND for the same consideration, said assignor hereby covenants and agrees to and with said assignee its successors, legal representatives and assigns, that, at the time of execution and delivery of these presents, said assignor is the sole and lawful owner of the entire right, title and interest in and to said inventions and the application for Letters Patent above-mentioned, and that the same are unencumbered and that said assignor has good and full right and lawful authority to sell and convey the same in the manner herein set forth.

AND for the same consideration, said assignor hereby covenants and agrees to and with said assignee, its successors, legal representatives and assigns, that said assignor will, whenever counsel of said assignee, or the counsel of its successor, legal representatives and assigns, shall advise that any proceeding in connection with said inventions, or said application for Letters Patent, or any proceeding in connection with Letters Patent for said inventions in any country, including interference proceedings, is lawful and desirable, or that any division, continuation or continuation-in-part of any application for Letters Patent or any reissue or extension of any Letters Patent, to be obtained thereon, is lawful and desirable, sign all papers and documents, take all lawful oaths, and do all acts necessary or required to be done for the procurement, maintenance, enforcement and defense of Letters Patent for said inventions, without charge to said assignee, its successors, legal representatives and assigns, but at the cost and expense of said assignee, its successors, legal representatives and assigns.

AND said assignor hereby requests the Commissioner of Patents to issue said Letters Patent of the United States to said assignee as the assignee of said inventions and the Letters Patent to be issued thereon for the sole use said assignee, its successors, legal representatives and assigns.

10/16/98 — William W. Y. Chu
Date — William W. Y. Chu

sf-584837

OIPE JC57
OCT 27 1998
PATENT & TRADEMARK OFFICE

PTO/SB/96 (10-92)

CERTIFICATE UNDER 37 C.F.R. § 3.73(b)	Docket No. 387112000300

In the application of: William W. Y. Chu
Serial No.: 09/149,882
Filed: September 8, 1998
For: A COMMUNICATION CHANNEL AND INTERFACE DEVICES FOR BRIDGING COMPUTER INTERFACE BUSES

Acqis Technology, Inc., a California corporation, certifies that it is the assignee of the entire right, title and interest in the patent application identified above by virtue of either:

A. ☒ An assignment from the inventor(s) of the patent application identified above. The assignment was recorded in the Patent and Trademark Office at Reel *, Frame *, or **for which a copy thereof is attached.**

OR

B. ☐ A chain of title from the inventor(s) of the patent application identified above, to the current assignee as shown below:

1. From : *
To: *
The document was recorded in the Patent and Trademark Office at Reel *, Frame *, or for which a copy thereof is attached.

2. From : *
To: *
The document was recorded in the Patent and Trademark Office at Reel *, Frame *, or for which a copy thereof is attached.

3. From : *
To: *
The document was recorded in the Patent and Trademark Office at Reel *, Frame *, or for which a copy thereof is attached.

☐ Additional documents in the chain of title are listed on a supplemental sheet.

☒ Copies of assignments or other documents in the chain of title are attached.

The undersigned has reviewed all the documents in the chain of title of the patent application identified above and, to the best of undersigned's knowledge and belief, title is in the assignee identified above.

The undersigned (whose title is supplied below) is empowered to sign this certificate on behalf of the assignee.

I hereby declare that all statements made herein of my own knowledge are true, and that all statements made on information and belief are believed to be true; and further, that these statements are made with the knowledge that willful false statements, and the like so made, are punishable by fine or imprisonment, or both, under Section 1001, Title 18 of the United States Code, and that such willful false statements may jeopardize the validity of the application or any patent issuing thereon.

Dated: Oct. 16, 1998

William W. Y. Chu

Name: William W. Y. Chu
Title: President and CEO

BEST COPY

#3

OIPE JC57 OCT 27 1998 PATENT & TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
Patent and Trademark Office
Address: COMMISSIONER OF PATENTS AND TRADEMARKS
Washington, D.C. 20231

APPLICATION NUMBER	FILING/RECEIPT DATE	FIRST NAMED APPLICANT	ATTORNEY DOCKET NO./TITLE
09/149,882	09/08/1998	CHU	W 39711/2000300

MORRISON & FOERSTER
425 MARKET STREET
SAN FRANCISCO CA 94105-2482

NOT ASSIGNED

2782

DATE MAILED: 09/28/98

NOTICE TO FILE MISSING PARTS OF APPLICATION
Filing Date Granted

An Application Number and Filing Date have been assigned to this application. The items indicated below, however, are missing. Applicant is given TWO MONTHS FROM THE DATE OF THIS NOTICE within which to file all required items and pay fees required below to avoid abandonment. Extensions of time may be obtained by filing a petition accompanied by the extension fee under the provisions of 37 CFR 1.136(a). **If any of items 1 or 3 through 5 are indicated as missing, the SURCHARGE set forth in 37 CFR 1.16(e) of ☐ $65.00 for a small entity in compliance with 37 CFR 1.27, or ☐ $130.00 for a non-small entity, must also be timely submitted in reply to this NOTICE to avoid abandonment.**

If all required items on this form are filed within the period set above, the total amount owed by applicant as a ☐ small entity (statement filed) ☐ non-small entity is $ 1676.

☐ 1. The statutory basic filing fee is:
☑ missing.
☑ insufficient.
Applicant must submit $ 790 to complete the basic filing fee and/or file a small entity statement claiming such status (37 CFR 1.27).

☐ 2. Additional claim fees of $_____, including any multiple dependent claim fees, are required.
$ 492 for 6 independent claims over 3.
$ 484 for 22 dependent claims over 20.
$_____ for multiple dependent claim surcharge.
Applicant must either submit the additional claim fees or cancel additional claims for which fees are due.

11/03/1998 GWASHING 00000036 09149882
01 FC:201 395.00 OP
02 FC:202 246.00 OP
03 FC:203 242.00 OP
04 FC:105 130.00 OP

☐ 3. The oath or declaration
☑ is missing or unexecuted.
☐ does not cover the newly submitted items.
☐ does not identify the application to which it applies.
☐ does not include the city and state or foreign country of applicant's residence.
An oath or declaration in compliance with 37 CFR 1.63, including residence information and identifying the application by the above Application Number and Filing Date is required.

☐ 4. The signature(s) to the oath or declaration is/are by a person other than inventor or person qualified under 37 CFR 1.42, 1.43 or 1.47.
Adjustment date: 12/07/1998 GWASHING
11/03/1998 GWASHING 00000036 09149882
04 FC:105 -130.00 OP
An oath or declaration in compliance with 37 CFR 1.63, identifying the application by the above Application Number and Filing Date, is required.

☐ 5. The signature of the following joint inventor(s) is missing from the oath or declaration:

_____

An oath or declaration in compliance with 37 CFR 1.63 listing the names of all inventors and signed by the omitted inventor(s), identifying this application by the above Application Number and Filing Date, is required.

☐ 6. A $50.00 processing fee is required since your check was returned without payment (37 CFR 1.21(m)).
12/07/1998 GWASHING 00000001 09149882
☐ 7. Your filing receipt was mailed in error because your check was returned without payment.
01 FC:805 65.00 OP

☐ 8. The application does not comply with the Sequence Rules.
See attached "Notice to Comply with Sequence Rules 37 CFR 1.821-1.825."

☑ 9. OTHER: Status of entity

Direct the reply and any questions about this notice to "Attention: Box Missing Parts."

Repln. Ref: 12/07/1998 GWASHING 00141700
DAM:031952 Name/Number:09149882
FC: 704 $65.00 CR

A copy of this notice MUST be returned with the reply.

Customer Service Center
Initial Patent Examination Division (703) 308-1202

PART 2 - COPY TO BE RETURNED WITH RESPONSE

FORM PTO-1533 (REV.9-97)

BEST COPY

UNITED STATES PATENT & TRADEMARK OFFICE
Washington, D.C. 20231

REQUEST FOR PATENT FEE REFUND

1 Date of Request: 11-10-98	2 Serial/Patent # 09/149887

	3 Please refund the following fee(s):	4 PAPER NUMBER	5 DATE FILED	6 AMOUNT
	Filing			$
	Amendment			$
	Extension of Time			$
	Notice of Appeal/Appeal			$
	Petition			$
	Issue			$
	Cert of Correction/Terminal Disc.			$
	Maintenance			$
	Assignment			$
	Other			$

7 TOTAL AMOUNT OF REFUND: $ 65

8 TO BE REFUNDED BY:

- [ ] Treasury Check
- [ ] Credit Deposit A/C #:

9 [0][3]--[1][9][5][2]

10 REASON:

- [X] Overpayment
- [ ] Duplicate Payment
- [ ] No Fee Due (Explanation):

11 REFUND REQUESTED BY:

TYPED/PRINTED NAME: Chanell Farmer TITLE: LIE

SIGNATURE: Chanell Farmer PHONE: 3089583

OFFICE: OIPE

****

THIS SPACE RESERVED FOR FINANCE USE ONLY:

APPROVED: _____ DATE: _____

Instructions for completion of this form appear on the back. After completion, attach white and yellow copies to the official file and mail or hand-carry to:

Office of Finance
Refund Branch
Crystal Park One, Room 802B

FORM PTO 1577
(01/90)

Transaction History Date 1998-12-07
Date information retrieved from USPTO Patent Application Information Retrieval (PAIR) system records at www.uspto.gov

GAU 2782 5
mcla
5.12.99

PATENT
Docket No. 387112000300

CERTIFICATE OF MAILING BY "FIRST CLASS MAIL"

I hereby certify that this correspondence is being deposited with the United States Postal Service as first class mail in an envelope addressed to: Assistant Commissioner for Patents, Washington, D.C. 20231, on December 4, 1998.

Andrea Diaz

RECEIVED
APR 27 1999
Group 2700

OIPE JC51
DEC 07 1998
PATENT & TRADEMARK OFFICE

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In the application of:

William W. Y. Chu

Serial No.: 09/149,882

Filing Date: September 8, 1998

For: A COMMUNICATION CHANNEL AND INTERFACE DEVICES FOR BRIDGING COMPUTER INTERFACE BUSES

Examiner: Not Yet Assigned

Group Art Unit: 2782

RECEIVED
DEC 09 1998
Group 2700

RECEIVED
DEC 15 1998
Group 2700

INFORMATION DISCLOSURE STATEMENT UNDER 37 C.F.R. § 1.97

Assistant Commissioner for Patents
Washington, D.C. 20231

Dear Sir:

Pursuant to 37 C.F.R. § 1.97 and § 1.98, applicants submit for consideration in the above-identified application the documents listed on the attached Form PTO-1449. Copies of the documents are also submitted herewith. The Examiner is requested to make these documents of record:

U.S. Patents

U.S. Patent No. 5,278,509 to Haynes, et al. (01/11/94)

U.S. Patent No. 5,278,730 to Kikinis (01/11/94)

sf-607433

U.S. Patent No. 5,293,497 to Free (03/08/94)

U.S. Patent No. 5,331,509 to Kikinis (07/19/94)

U.S. Patent No. 5,355,391 to Horowitz, et al. (10/11/94)

U.S. Patent No. 5,539,616 to Kikinis (07/23/96)

U.S. Patent No. 5,578,940 to Dillon, et al. (11/26/96)

U.S. Patent No. 5,600,800 to Kikinis, et al. (02/04/97)

U.S. Patent No. 5,606,717 to Farmwald, et al. (02/25/97)

U.S. Patent No. 5,640,302 to Kikinis (06/17/97)

U.S. Patent No. 5,659,773 to Huynh, et al. (08/19/97)

U.S. Patent No. 5,663,661 to Dillon, et al. (09/02/97)

U.S. Patent No. 5,680,126 to Kikinis (10/21/97)

RECEIVED
DEC 1 5 1998
Group 2700

Other References

Digital Semiconductor, 21152 PCI-to-PCI Bridge Product Brief (02/96)

Intel Corporation, Intel 430TX PCISET: 82439TX System Controller (MTXC) Architectural Overview (02/97)

Intel Corporation, Intel 82371AB PCI-to-ISA/IDE XCELERATOR (PIIX4) Architectural Overview (04/97)

Intel Corporation, Intel 440LX AGPSET: 82443LX PCI A.G.P. CONTROLLER (PAC) Advance Information (08/97)

National Semiconductor, DS90CR215/DS90CR216 General Description (07/97)

National Semiconductor, DS90CR215 Product Folder

Video Electronics Standards Association (VESA), Plug and Display(P&D) Standard, P&D and Digital Transition Minimized Differential Signaling (TMDS) Video Transmission Overview, Version 1, Revision 0, pp. 1 & 31-34 (1997)

This Information Disclosure Statement is submitted:

☒ Within three months of the application filing date or before receipt of a first Office Action on the merits; accordingly, no fee or separate requirements are required.

☐ After receipt of a first Office Action on the merits but before a final Office Action or Notice of Allowance.

- ☐ A fee is required. A check in the amount of * is enclosed.
- ☐ A Certification under 37 C.F.R. § 1.97(e) is provided below; accordingly; no fee is believed to be due.

☐ After receipt of a final Office Action or Notice of Allowance, but before payment of the issue fee. Accordingly, a Petition requesting consideration of the Information Disclosure Statement, an authorization to charge our deposit account, and a Certification under 37 C.F.R. § 1.97(e) are provided herein.

Applicants would appreciate the Examiner initialing and returning the Form PTO-1449, indicating that the information has been considered and made of record herein.

This Information Disclosure Statement under 37 C.F.R. § 1.97 is not to be construed as a representation that: (i) a complete search has been made; (ii) additional information material to the examination of this application does not exist; (iii) the information, protocols, results and the like reported by third parties are accurate or enabling; or (iv) the above information constitutes prior art to the subject invention.

In the unlikely event that the transmittal letter is separated from this document and the Patent Office determines that an extension and/or other relief is required, applicant petitions for any required relief including extensions of time and authorizes the Assistant Commissioner to charge the cost of such petitions and/or other fees due in connection with the filing of this

document to **Deposit Account No. 03-1952** referencing 387112000300. However, the Assistant Commissioner is not authorized to charge the cost of the issue fee to the Deposit Account.

Dated: December 4, 1998

Respectfully submitted,

By: Ararat Kapouytian

Ararat Kapouytian
Registration No. 40,044

Morrison & Foerster LLP
425 Market Street
San Francisco, California 94105-2482
Telephone: (415) 268-7000
Facsimile: (415) 268-7522

RECEIVED
DEC 15 1998
Group 2700

#5

PTO/SB/08 (2-92)
Sheet 1 of 2

Form PTO-1449	Docket Number 387112000300	Application Number 09/149,882
INFORMATION DISCLOSURE CITATION IN AN APPLICATION *(Use several sheets if necessary)*	Applicant: William W. Y. Chu	
	Filing Date September 8, 1998	Group Art Unit 2782

RECEIVED
DEC 0 9 1998
Group 2700

OIPE JC51 DEC 0 7 1998 PATENT & TRADEMARK OFFICE

U.S. PATENT DOCUMENTS

Examiner Initials	Ref. No.	Date	Document No.	Name	Class	Subclass	Filing Date If Appropriate
C	1.	01/11/94	5,278,509	Haynes, et al.			
C	2.	01/11/94	5,278,730	Kikinis			
C	3.	03/08/94	5,293,497	Free			
C	4.	07/19/94	5,331,509	Kikinis			
C	5.	10/11/94	5,355,391	Horowitz, et al.			
C	6.	07/23/96	5,539,616	Kikinis			
C	7.	11/26/96	5,578,940	Dillon, et al.			
C	8.	02/04/97	5,600,800	Kikinis, et al.			
C	9.	02/25/97	5,606,717	Farmwald, et al.			
C	10.	06/17/97	5,640,302	Kikinis			
C	11.	08/19/97	5,659,773	Huynh, et al.			
C	12.	09/02/97	5,663,661	Dillon, et al.			
C	13.	10/21/97	5,680,126	Kikinis			

RECEIVED
DEC 15 1998
Group 2700

RECEIVED
APR 27 1999
Group 2700

FOREIGN PATENT DOCUMENTS

Examiner Initials	Ref. No.	Date	Document No.	Country	Class	Subclass	Translation YES	Translation NO
	0.							

OTHER DOCUMENTS *(including author, title, Date, Pertinent Pages, Etc.)*

Examiner Initials	Ref. No.	Title
C	1.	Digital Semiconductor, 21152 PCI-to-PCI Bridge Product Brief (02/96)
C	2.	Intel Corporation, Intel 430TX PCISET: 82439TX System Controller (MTXC) Architectural Overview (02/97)
C	3.	Intel Corporation, Intel 82371AB PCI-to-ISA/IDE XCELERATOR (PIIX4) Architectural Overview (04/97)
C	4.	Intel Corporation, Intel 440LX AGPSET: 82443LX PCI A.G.P. CONTROLLER (PAC) Advance Information (08/97)
C	5.	National Semiconductor, DS90CR215/DS90CR216 General Description (07/97)
C	6.	National Semiconductor, DS90CR215 Product Folder

EXAMINER: (examiner) CM	DATE CONSIDERED: 5-10-00

EXAMINER: Initial if citation considered, whether or not the citation conforms with MPEP 609. Draw a line through the citation if not in conformance and not considered. Include a copy of this form with next communication to applicant.

PTO/SB/ 08 (2-92)
sf-607455

Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE

Form PTO-1449

INFORMATION DISCLOSURE CITATION IN AN APPLICATION

(Use several sheets if necessary)

O I P E
DEC 0 7 1998
PATENT & TRADEMARK OFFICE
JC51

Docket Number 387112000300	Application Number 09/149,882
Applicant: William W. Y. Chu	
Filing Date September 8, 1998	Group Art Unit 2782

RECEIVED
APR 27 1999
Group 2700

OTHER DOCUMENTS *(including author, title, Date, Pertinent Pages, Etc.)*

Examiner Initials	Ref. No.	Title
	7.	Video Electronics Standards Association (VESA), Plug and Display(P&D) Standard, P&D and Digital Transition Minimized Differential Signaling (TMDS) Video Transmission Overview, Version 1, Revision 0, pp. 1 & 31-34 (1997)

RECEIVED
DEC 0 9 1998
Group 2700

RECEIVED
DEC 1 5 1998
Group 2700

EXAMINER:	DATE CONSIDERED: 5-10-00

EXAMINER: Initial if citation considered, whether or not the citation conforms with MPEP 609. Draw a line through the citation if not in conformance and not considered. Include a copy of this form with next communication to applicant.

Other Prior Art

According to the information contained in form PTO-1449 or PTO-892, there are one or more other prior art/non-patent literature documents missing from the original file history record obtained from the United States Patent and Trademark Office. Upon your request we will attempt to obtain these documents from alternative resources. Please note that additional charges will apply for this service.

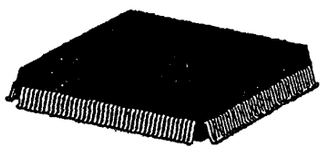
This page is not part of the official USPTO record. It has been determined that content identified on this document is missing from the original file history record.

Digital Semiconductor

21152 PCI-to-PCI Bridge

Product Brief

February 1996



Description

Digital Semiconductor's 21152 is a second-generation PCI-to-PCI bridge and is fully compliant with *PCI Local Bus Specification, Revision 2.1*. The 21152 is pin-to-pin compatible with Digital Semiconductor's 21052, which is fully compliant with *PCI Local Bus Specification, Revision 2.0*. The 21152 provides full support for delayed transactions, which enables the buffering of memory read, I/O, and configuration transactions. The 21152 has separate posted write, read data, and delayed transaction queues with significantly more buffering capability than first-generation bridges. In addition, the 21152 supports buffering of simultaneous multiple posted write and delayed transactions in both directions. Among the features provided by the 21152 are: a programmable 2-level secondary bus arbiter, individual secondary clock software control, and enhanced address decoding. The 21152 has sufficient clock and arbitration pins to support four PCI bus master devices directly on its secondary interface.

The 21152 allows the two PCI buses to operate concurrently. This means that a master and a target on the same PCI bus can communicate while the other PCI bus is busy. This traffic isolation may increase system performance in applications such as multimedia.

Features

- Complies fully with Revision 2.1 of the *PCI Local Bus Specification*
- Implements delayed transactions for all PCI configuration, I/O, and memory read commands—up to three transactions simultaneously in each direction
- Allows 88 bytes of buffering (data and address) for posted memory write commands in each direction—up to five posted write transactions simultaneously in each direction
- Allows 72 bytes of read data buffering in each direction
- Provides concurrent primary and secondary bus operation to isolate traffic
- Provides five secondary clock outputs:
  - Low skew, permitting direct drive of option slots
  - Individual clock control through configuration space
- Provides arbitration support for four secondary bus devices:
  - A programmable 2-level arbiter
  - Hardware disable control, permitting use of an external arbiter
- Provides enhanced address decoding:
  - A 32-bit I/O address range
  - A 32-bit memory-mapped I/O address range
  - A 64-bit prefetchable memory address range
  - ISA-aware mode for legacy support in the first 64KB of I/O address range
  - VGA addressing and VGA palette snooping support
- Supports PCI transaction forwarding for the following commands:
  - All I/O and memory commands
  - Type 1 to Type 1 configuration commands
  - Type 1 to Type 0 configuration commands (downstream only)
  - All Type 1 to special cycle configuration commands
- Includes downstream lock support
- Supports both 5-V and 3.3-V signaling environments

1
Introduction

Digital Semiconductor's 21152 is a second-generation PCI-to-PCI bridge and is fully compliant with *PCI Local Bus Specification, Revision 2.1*. The 21152 is pin-to-pin compatible with Digital Semiconductor's 21052, which is fully compliant with *PCI Local Bus Specification, Revision 2.0*. The 21152 provides full support for delayed transactions, which enables the buffering of memory read, I/O, and configuration transactions. The 21152 has separate posted write, read data, and delayed transaction queues with significantly more buffering capability than first-generation bridges. In addition, the 21152 supports buffering of simultaneous multiple posted write and delayed transactions in both directions. Among the features provided by the 21152 are a programmable 2-level secondary bus arbiter, individual secondary clock software control, and enhanced address decoding. The 21152 has sufficient clock and arbitration pins to support four PCI bus master devices directly on its secondary interface.

The 21152 allows the two PCI buses to operate concurrently. This means that a master and a target on the same PCI bus can communicate while the other PCI bus is busy. This traffic isolation may increase system performance in applications such as multimedia.

1.1 Features

The 21152 has the following features:

- Complies fully with Revision 2.1 of the *PCI Local Bus Specification*
- Complies fully with Revision 1.1 of the *PCI-to-PCI Bridge Architecture Specification*
- Implements delayed transactions for all PCI configuration, I/O, and memory read commands–up to three transactions simultaneously in each direction
- Allows 88 bytes of buffering (data and address) for posted memory write commands in each direction–up to five posted write transactions simultaneously in each direction
- Allows 72 bytes of read data buffering in each direction

Ex. 1011, Page 318

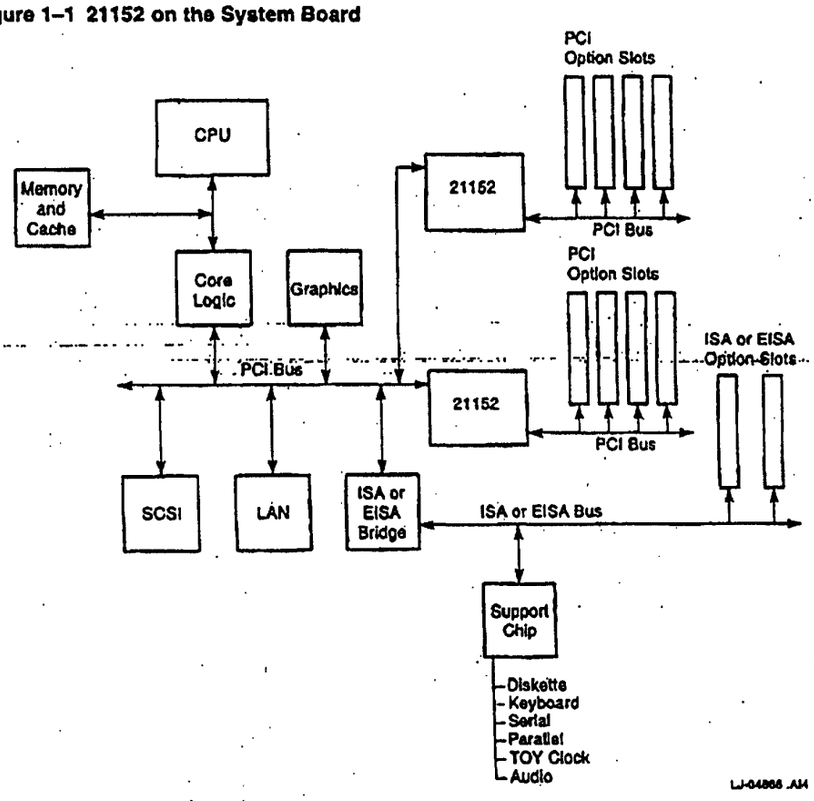
Features

- Provides concurrent primary and secondary bus operation to isolate traffic
- Provides five secondary clock outputs:
  - Low skew, permitting direct drive of option slots
  - Individual clock control through configuration space
- Provides arbitration support for four secondary bus devices:
  - A programmable 2-level arbiter
  - Hardware disable control, permitting use of an external arbiter
- Provides enhanced address decoding:
  - A 32-bit I/O address range
  - A 32-bit memory-mapped I/O address range
  - A 64-bit prefetchable memory address range
  - ISA-aware mode for legacy support in the first 64KB of I/O address range
  - VGA addressing and VGA palette snooping support
- Supports PCI transaction forwarding for the following commands:
  - All I/O and memory commands
  - Type 1 to Type 1 configuration commands
  - Type 1 to Type 0 configuration commands (downstream only)
  - All Type 1 to special cycle configuration commands
- Includes downstream lock support
- Supports both 5-V and 3.3-V signaling environments

The 21152 makes it possible to extend a system's load capability limit beyond that of a single PCI bus by allowing motherboard designers to add more PCI devices, or more PCI option card slots, than a single PCI bus can support. Figure 1–1 illustrates the use of two 21152 PCI-to-PCI bridges on a system board. Each 21152 that is added to the board creates a new PCI bus that provides support for the additional PCI slots or devices.

Ex. 1011, Page 319

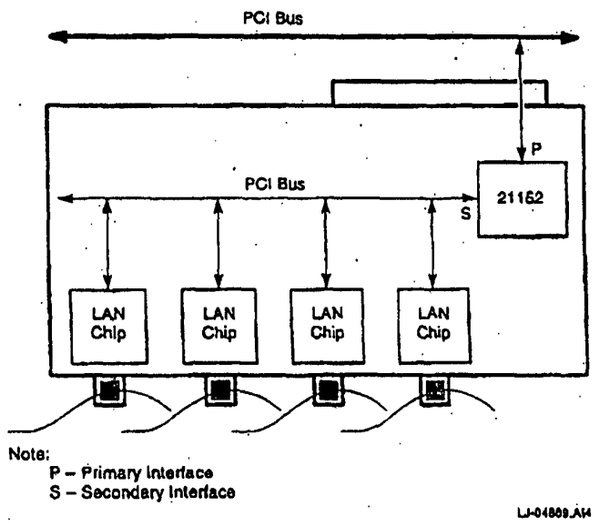
Figure 1–1 21152 on the System Board



Option card designers can use the 21152 to implement multiple-device PCI option cards. Without a PCI-to-PCI bridge, PCI loading rules would limit option cards to one device. The *PCI Local Bus Specification* loading rules limit PCI option cards to a single connection per PCI signal in the option card connector. However, the 21152 overcomes this restriction by providing, on the option card, an independent PCI bus to which up to four devices can be attached.

Figure 1–2 shows how the 21152 enables the design of a multicomponent option card.

Figure 1–2 21152 with Option Cards



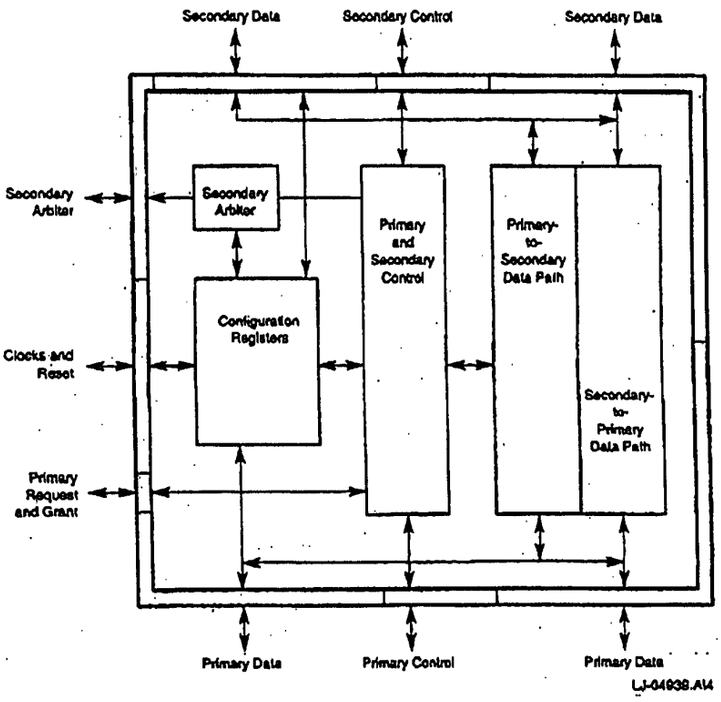
1.2 Architecture

The 21152 internal architecture consists of the following major functions:

- PCI interface control logic for the primary and secondary PCI interfaces
- Data path and data path control logic
- Configuration register and configuration control logic
- Secondary bus arbiter

Figure 1–3 shows the major functional blocks of the 21152.

Figure 1–3 21152 Block Diagram



BEST COPY

PRELIMINARY

INTEL 430TX PCISET: 82439TX SYSTEM CONTROLLER (MTXC)

- Supports Mobile and Desktop
- Supports the Pentium® Processor Family Host Bus at 66 MHz and 60 MHz at 3.3V and 2.5V
- PCI 2.1 Compliant
- Integrated Data Path
- Integrated DRAM Controller
  - 4 Mbytes to 256 MBytes main memory
  - 64-Mbit DRAM/SDRAM Technology Support
  - FPM (Fast Page Mode), EDO and SDRAM DRAM Support
  - 6 RAS Lines Available
  - Integrated Programmable Strength for DRAM Interface
  - CAS-Before-RAS Refresh, Extended Refresh and Self Refresh for EDO
  - CAS-Before-RAS and Self Refresh for SDRAM
- Integrated L2 Cache Controller
  - 64-MB DRAM Cacheability
  - Direct Mapped Organization—Write Back Only
  - Supports 256K and 512K Pipelined Burst SRAM and DRAM Cache SRAM
  - Cache Hit Read/Write Cycle Timings at 3-1-1-1
  - Back-to-Back Read/Write Cycles at 3-1-1-1-1-1-1-1
  - 64K x 32 SRAM also supported
- Fully Synchronous, Minimum Latency 30/33-MHz PCI Bus Interface
  - Five PCI Bus Masters (Including PIIX4)
  - 10 DWord PCI-to-DRAM Read Prefetch Buffer
  - 18 DWord PCI-DRAM Post Buffer
  - Multi-Transaction Timer to Support Multiple Short PCI Transactions
- Power Management Features
  - PCI CLKRUN# Support
  - Dynamic Stop Clock Support
  - Suspend to RAM (STR)
  - Suspend to Disk (STD)
  - Power On Suspend (POS)
  - Internal Clock Control
  - SDRAM and EDO Self Refresh During Suspend
  - ACPI Support
  - Compatible SMRAM (C_SMRAM) and Extended SMRAM (E_SMRAM)
  - SMM Writeback Cacheable in E_SMRAM Mode up to 1 MB
  - 3.3/5V DRAM, 3.3/5V PCI 3.3/5V Tag and 3.3/2.5 SRAM Support
- Test Features
  - NAND Tree Support for all Pins
- Supports the Universal Serial Bus (USB)
- 324-Pin MBGA 430TX PCIset Xcelerated Controller (MTXC) with Integrated Data Paths

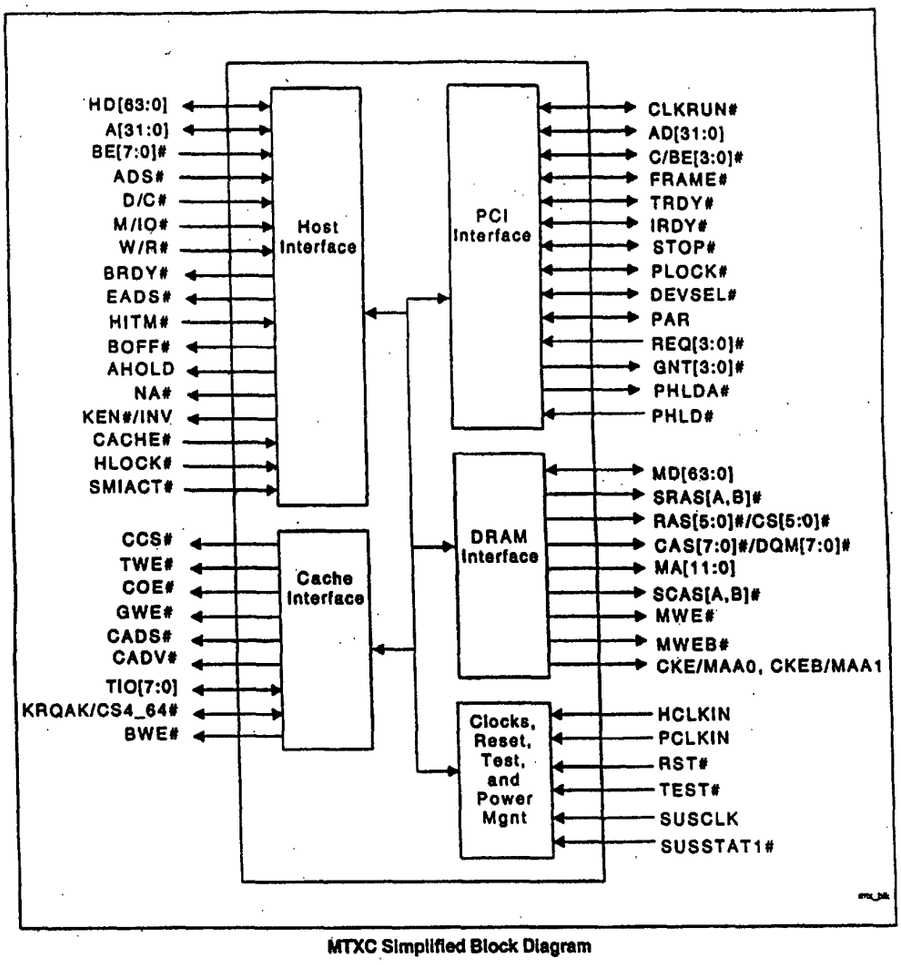
The Intel 430TX PCIset (430TX) consists of the 82439TX System Controller (MTXC) and the 82371AB PCI ISA IDE Xcelerator (PIIX4). The 430TX supports both mobile and desktop architectures. The 430TX forms a Host-to-PCI bridge and provides the second level cache control and a full function 64-bit data path to main memory. The MTXC integrates the cache and main memory DRAM control functions and provides bus control to transfers between the CPU, cache, main memory, and the PCI Bus. The second level (L2) cache controller supports a writeback cache policy for cache sizes of 256 Kbytes and 512 Kbytes. Cacheless designs are also supported. The cache memory can be implemented with pipelined burst SRAMs or DRAM cache SRAMs. An external Tag RAM is used for the address tag and an internal Tag RAM for the cache line status bits. For the MTXC DRAM controller, six rows are supported for up to 256 Mbytes of main memory. The MTXC is highly integrated by including the Data Path into the same BGA chip. Using the snoop ahead feature, the MTXC allows PCI masters to achieve full PCI bandwidth. For increased system performance, the MTXC integrates posted write and read prefetch buffers. The 430TX integrates many Power Management features that enable the system to save power when the system resources become idle.

Information in this document is provided in connection with Intel products. No license, express or implied, by estoppel or otherwise, to any intellectual property rights is granted by this document or by the sale of Intel products. Except as provided in Intel's Terms and Conditions of Sale for such products, Intel assumes no liability whatsoever, and Intel disclaims any express or implied warranty, relating to sale and/or use of Intel products including liability or warranties relating to fitness for a particular purpose, merchantability, or infringement of any patent, copyright or other intellectual property right. Intel products are not intended for use in medical, life saving, or life sustaining applications. Intel reserves the right to make changes to specifications and product descriptions at any time, without notice. The Intel 430TX PCIset may contain design defects or errors known as errata. Current characterized errata are available on request. Third-party brands and names are the property of their respective owners.

© INTEL CORPORATION 1997

February 1997

Order Number: 290559-001



MTXC Simplified Block Diagram

1.0. ARCHITECTURE OVERVIEW

The MTXC host bridge provides a completely integrated solution for the system controller and datapath components in a Pentium processor system. The MTXC Supports all Pentium family processors since P54C, it has 64-bit Host and DRAM Bus Interface, 32-bit PCI Bus Interface, Second level Cache Interface, and it integrates the PCI arbiter.

The MTXC interfaces with the Pentium processor host bus, a dedicated memory data bus, and the PCI bus (see Figure 1).

The MTXC bus interfaces are designed to interface with 2.5V, 3.3V and 5V busses. The MTXC implements 2.5V and 3.3V drivers and 5V tolerant receivers. The MTXC connects directly to the Pentium processor 3.3V or 2.5V host bus, directly to 5V or 3.3V DRAMs, and directly to the 5V or 3.3V PCI bus. The 430TX also interfaces directly to the 3.3V or 5.0V TAGRAM and 3.3V Cache.

The MTXC works with the PCI IDE/ISA Accelerator 4 (PIIX4). The PIIX4 provides the PCI-to-ISA/EIO bridge functions along with other features such as a fast IDE interface (PIO mode 4 and Ultra DMA/33), Plug-n-Play port, APIC interface, PCI 2.1 Compliance, SMBUS interface, and Universal Serial Bus Host Controller functions.

DRAM Interface

The DRAM interface is a 64-bit data path that supports Standard (or Fast) Page Mode (FPM), Extended Data Out (EDO) and Synchronous DRAM (SDRAM) memory. The DRAM controller inside the MTXC is capable of generating 3-1-1-1 for posted writes for any type of DRAM that is used. While read performance is 6-1-1-1 for SDRAM, 5-2-2-2 for EDO, and 6-3-3-3 for FPM.

The DRAM interface supports 4 Mbytes to 256 Mbytes with six RAS lines. The MTXC supports 4-Mbit, 16-Mbit, and 64-Mbit DRAM and SDRAM technology, both symmetrical and asymmetrical. Parity is not supported, and for loading reasons, x32 and x64 SIMMs/DIMMs/SO-DIMMs should be used.

Second Level Cache

The second level cache is direct mapped and supports both 256-Kbyte and 512-Kbyte SRAM configuration using Pipeline Burst SRAM or DRAM Cache SRAM. The Cache performance is 3-1-1-1 for line read/write and 3-1-1-1-1-1-1-1 for back to back reads that are pipelined. Cacheless configuration is also supported.

PCI Interface

The PCI interface is 2.1 compliant and supports up to four PCI bus masters in addition to the PIIX4 bus master requests.

Datapath and Buffers

The MTXC contains three sets of data buffers for optimizing data flow. A five QWord deep DRAM write buffer is provided for CPU-to-DRAM writes, second level cache write backs, and PCI-to-DRAM transfers. This buffer is used to achieve 3-1-1-1 posted writes to DRAM and also provides DWord merging and burst merging for CPU-to-DRAM write cycles. In addition, an extra line of buffering is provided that is combined with the DRAM Write Buffer to supply an 18 DWord deep buffer for PCI to main memory writes. A five DWord buffer is provided for CPU-to-PCI writes to help maximize the bandwidth for graphic writes to the PCI bus. Also, five QWords of prefetch buffering has been added to the PCI-to-DRAM read path that allows up to two lines of data to be prefetched at an x-2-2-2 rate. The MTXC interfaces directly to the Host and DRAM data bus.

Power Management Features

The MTXC implements extensive power management features. The CLKRUN# feature enables controlling of the PCI clock (on/off). The MTXC supports POS, STR, STD, and Soft-off suspend states. SUSCLK and

SUSSTAT1# signals are used for implementing Suspend Logic. The MTXC supports two SMRAM modes; Compatible SMRAM (C_SMRAM) and Extended SMRAM (E_SMRAM). The C_SMRAM is the traditional SMRAM feature implemented in Intel PCIsets. The E_SMRAM is a new feature that supports writeback cacheable SMRAM space up to 1 Mbytes. In order to minimize the idle power, the internal clock in MTXC is turned off (gated off) when there is no activity on the Host and PCI Bus.

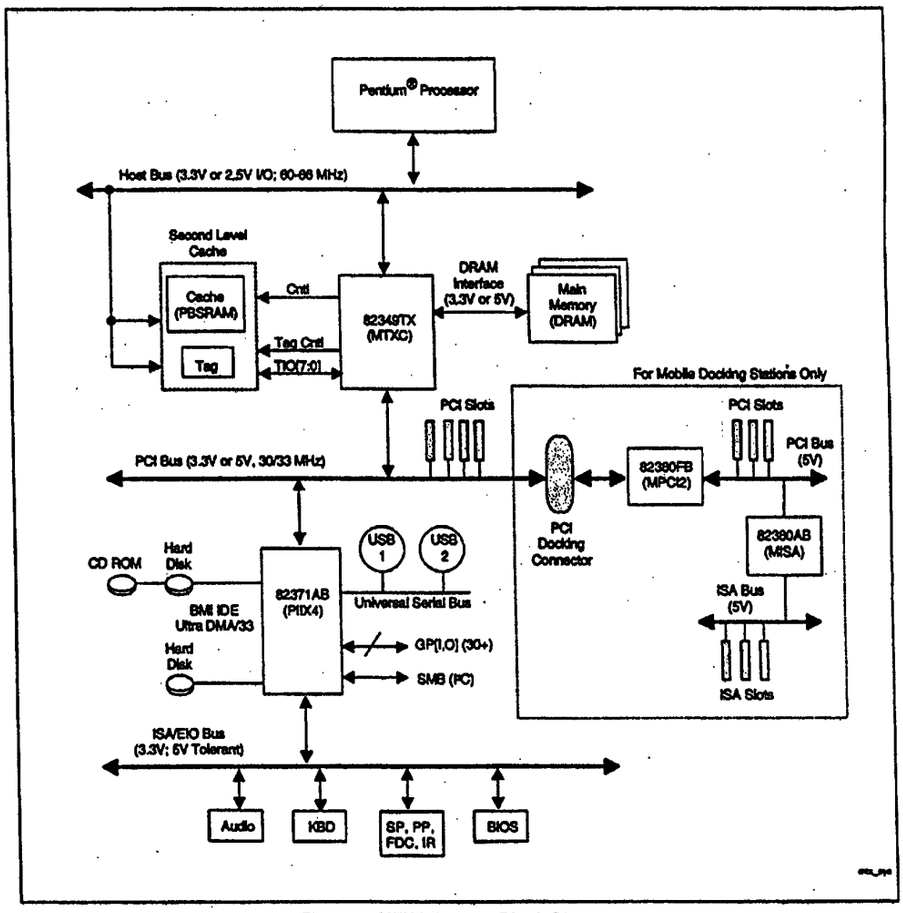


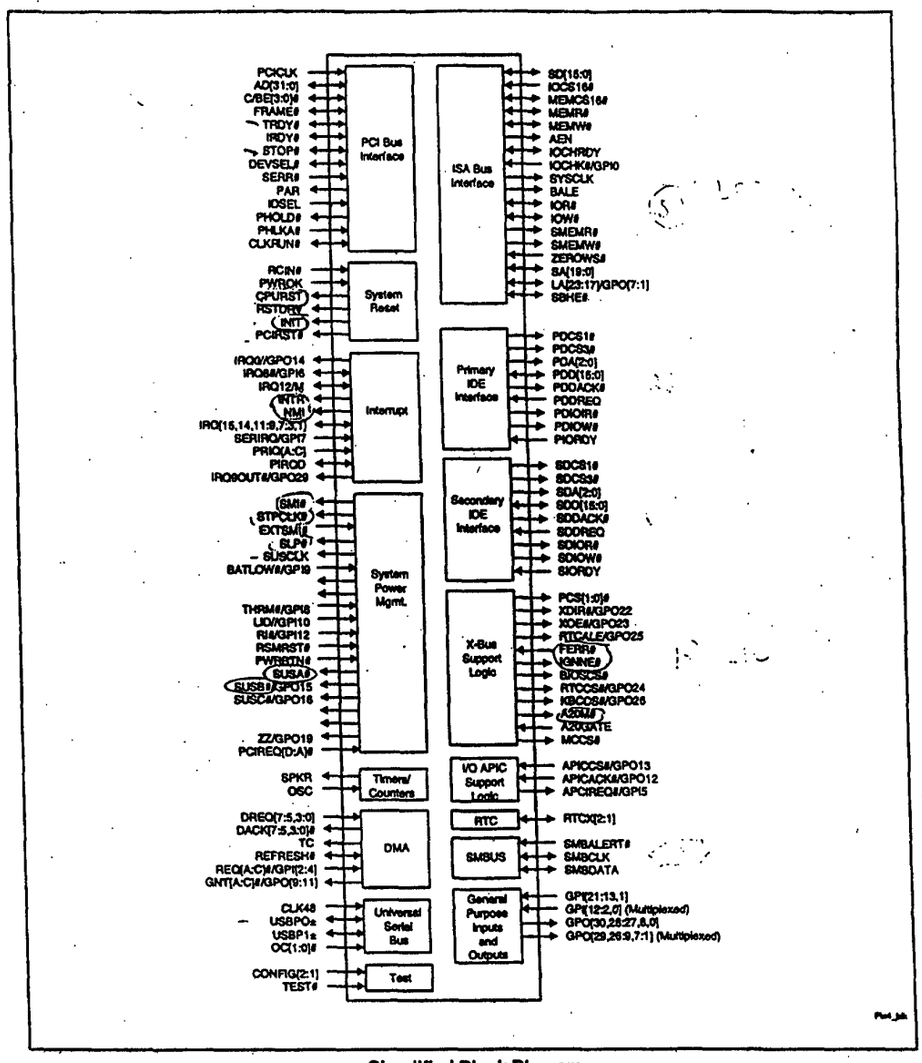
Figure 1. MTXC System Block Diagram

82371AB PCI-TO-ISA / IDE XCELERATOR (PIIX4)

- Supported Kits for both Pentium® and Pentium® II Microprocessors
  - 82430TX ISA Kit
  - 82440LX ISA/DP Kit
- Multifunction PCI to ISA Bridge
  - Supports PCI at 30 MHz and 33 MHz
  - Supports PCI Rev 2.1 Specification
  - Supports Full ISA or Extended I/O (EIO) Bus
  - Supports Full Positive Decode or Subtractive Decode of PCI
  - Supports ISA and EIO at 1/4 of PCI Frequency
- Supports both Mobile and Desktop Deep Green Environments
  - 3.3V Operation with 5V Tolerant Buffers
  - Ultra-low Power for Mobile Environments Support
  - Power-On Suspend, Suspend to RAM, Suspend to Disk, and Soft-OFF System States
  - All Registers Readable and Restorable for Proper Resume from 0.V Suspend
- Power Management Logic
  - Global and Local Device Management
  - Suspend and Resume Logic
  - Supports Thermal Alarm
  - Support for External Microcontroller
  - Full Support for Advanced Configuration and Power Interface (ACPI) Revision 1.0 Specification and OS Directed Power Management
- Integrated IDE Controller
  - Independent Timing of up to 4 Drives
  - PIO Mode 4 and Bus Master IDE Transfers up to 14 Mbytes/sec
  - Supports "Ultra DMA/33" Synchronous DMA Mode Transfers up to 33 Mbytes/sec
  - Integrated 16 x 32-bit Buffer for IDE PCI Burst Transfers
  - Supports Glue-less "Swap-Bay" Option with Full Electrical Isolation
- Enhanced DMA Controller
  - Two 82C37 DMA Controllers
  - Supports PCI DMA with 3 PC/PCI Channels and Distributed DMA Protocols (Simultaneously)
  - Fast Type-F DMA for Reduced PCI Bus Usage
- Interrupt Controller Based on Two 82C59
  - 15 Interrupt Support
  - Independently Programmable for Edge/Level Sensitivity
  - Supports Optional I/O APIC
  - Serial Interrupt Input
- Timers Based on 82C54
  - System Timer, Refresh Request, Speaker Tone Output
- USB
  - Two USB 1.0 Ports for Serial Transfers at 12 or 1.5 Mbit/sec
  - Supports Legacy Keyboard and Mouse Software with USB-based Keyboard and Mouse
  - Supports UHCI Design Guide
- SMBus
  - Host Interface Allows CPU to Communicate Via SMBus
  - Slave Interface Allows External SMBus Master to Control Resume Events
- Real-Time Clock
  - 256-byte Battery-Back CMOS SRAM
  - Includes Date Alarm
  - Two 8-byte Lockout Ranges
- Microsoft Win95* Compliant
- 324 mBGA Package

© INTEL CORPORATION 1997

April 1997 Order Number: 290562-001



Simplified Block Diagram

1.0. ARCHITECTURAL OVERVIEW

PIIX4 is a multi-function PCI device that integrates many system-level functions. Figure 1 shows an example system block diagram using PIIX4.

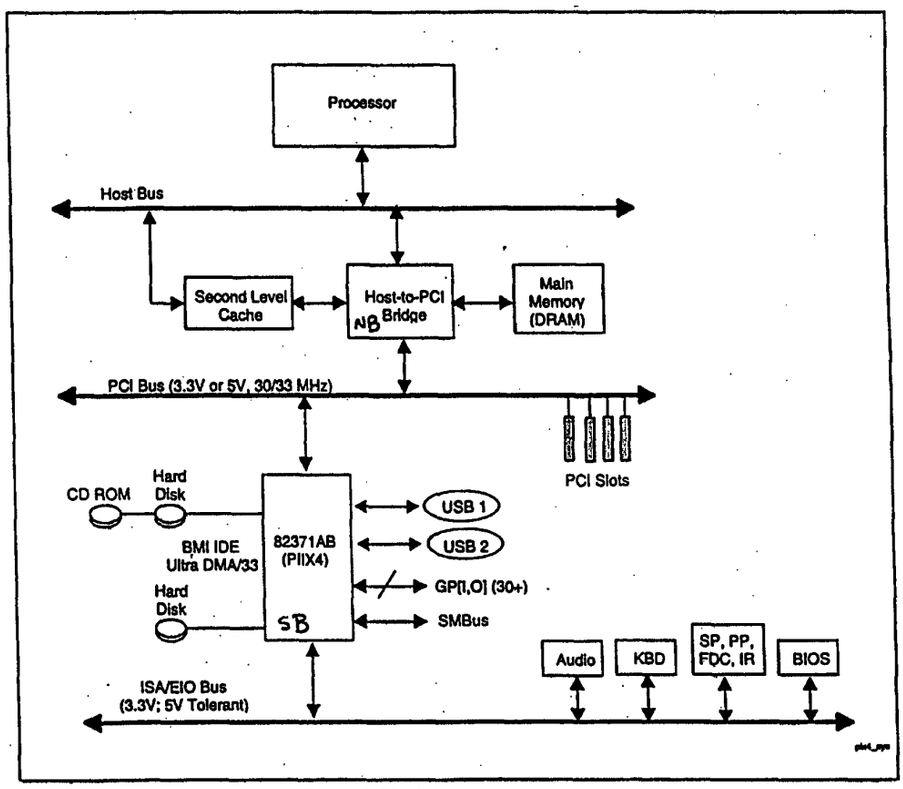


Figure 1. PIIX4 System Block Diagram

PCI to ISA/EIO Bridge

PIIX4 is compatible with the PCI Rev 2.1 specification, as well as the IEEE 996 specification for the ISA (AT) bus. On PCI, PIIX4 operates as a master for various internal modules, such as the USB controller, DMA controller, IDE bus master controller, distributed DMA masters, and on behalf of ISA masters. PIIX4 operates as a slave for its internal registers or for cycles that are passed to the ISA or EIO buses. All internal registers are positively decoded.

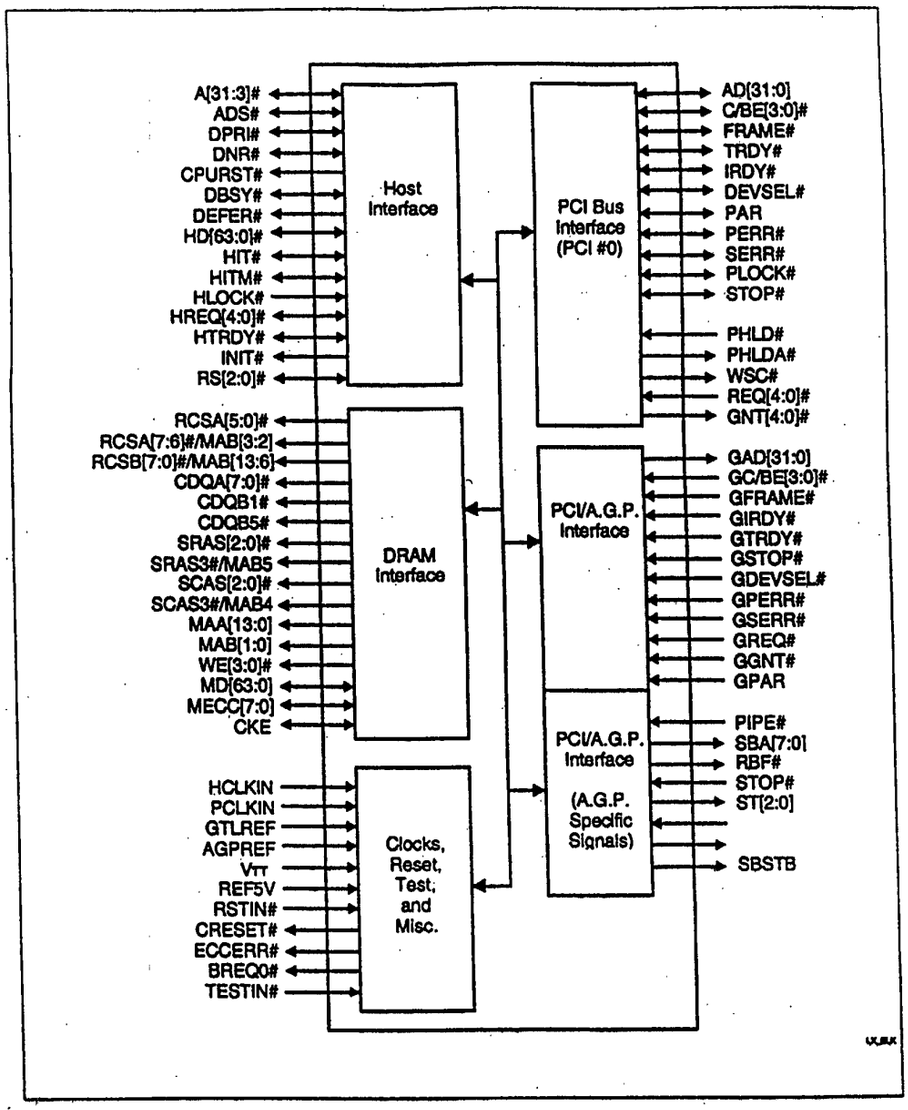
ADVANCE INFORMATION

INTEL 440LX AGPSET: 82443LX PCI A.G.P. CONTROLLER (PAC)

- Supports the Pentium® II processor Bus frequency of 66 MHz
  - Supports 32-Bit Addressing
  - Optimized In-Order and Request Queue
  - Full Symmetric Multi-Processor (SMP) Protocol for Up to Two Processors
  - Dynamic Deferred Transaction Support
  - GTL+ Compliant Host Bus Supports WC Cycles
- Integrated DRAM Controller
  - EDO (Extended Data Out), and Synchronous DRAM Support
  - Supports a Maximum Memory Size of 512 MB With SDRAM, or 1 GB With EDO
  - 64/72-bit Path to Memory
  - Configurable DRAM Interface
  - Support for Auto Detection of Memory Type: (DIMM Serial Presence Detect)
  - 8 RAS Lines Available
  - Support for 4-, 16- and 64-Mbit DRAM devices
  - Support for Symmetrical and Asymmetrical DRAM Addressing
  - Configurable Support for ECC/EC
  - ECC With Single Bit Error Correction and Multiple Bit Error Detection
  - Read-Around-Write Support for Host and PCI DRAM Read Accesses
  - Supports 3.3V DRAMs
- Accelerated Graphics Port Interface
  - A.G.P. Specification Compliant
  - A.G.P. 66/133 MHz 3.3V Devices Supported
  - Synchronous Coupling to the Host Bus Frequency
- PCI Bus Interface
  - PCI Revision 2.1 Interface Compliant
  - Greater Than 100-MBps Data Streaming for PCI-to-DRAM Accesses
  - Integrated Arbiter With Multi-Transaction PCI Arbitration Acceleration Hooks
  - Five PCI Bus Masters are Supported in Addition to the Host and PCI-to-ISA I/O Bridge
  - Delayed Transaction Support
  - PCI Parity Checking and Generation Support
- Data Buffering For Increased Performance
  - Extensive CPU-to-DRAM, PCI-to-DRAM, and A.G.P.-to-DRAM Write Data Buffering
  - CPU-to-A.G.P., PCI-to-A.G.P., and A.G.P.-to-PCI Data Buffering
  - Write Combining Support for CPU-to-PCI Burst Writes
  - Supports Concurrent Host, PCI, and A.G.P. Transactions to Main Memory
- System Management Mode (SMM) Compliant
- 492 Pin BGA Package

The 82443LX (PAC) is the first generation of desktop AGPset designed for the Pentium® II processor. The 82443LX PCI A.G.P. Controller (PAC) integrates a Host-to-PCI bridge, optimized DRAM controller and data path, and an Accelerated Graphics Port (A.G.P.) interface. A.G.P. is a high performance, component level interconnect, targeted at 3D graphics applications and based on a set of performance enhancements to PCI. The I/O subsystem portion of the PAC platform is based on the PIIX4, a highly integrated version of the Intel's PCI-to-ISA bridge family. PAC is developed as the ultimate Pentium II processor platform and is targeted for emerging 3D graphics and multimedia applications. The 440LX AGPset may contain design defects or errors known as errata which may cause the product to deviate from published specifications. Current characterized errata are available on request.

August 1997 Order Number 290564-00


A[31:3]#
ADS#
DPRI#
DNR#
CPURST#
DBSY#
DEFER#
HD[63:0]#
HIT#
HITM#
HLOCK#
HREQ[4:0]#
HTRDY#
INIT#
RS[2:0]#
Host Interface
RCSA[5:0]#
RCSA[7:6]#/MAB[3:2]
RCSB[7:0]#/MAB[13:6]
CDQA[7:0]#
CDQB1#
CDQB5#
SRAS[2:0]#
SRAS3#/MAB5
SCAS[2:0]#
SCAS3#/MAB4
MAA[13:0]
MAB[1:0]
WE[3:0]#
MD[63:0]
MECC[7:0]
CKE
DRAM Interface
HCLKIN
PCLKIN
GTLREF
AGPREF
VTT
REF5V
RSTIN#
CRESET#
ECCERR#
BREQ0#
TESTIN#
Clocks, Reset, Test, and Misc.
PCI Bus Interface (PCI #0)
PCI/A.G.P. Interface
PCI/A.G.P. Interface
(A.G.P. Specific Signals)
AD[31:0]
C/BE[3:0]#
FRAME#
TRDY#
IRDY#
DEVSEL#
PAR
PERR#
SERR#
PLOCK#
STOP#
PHLD#
PHLDA#
WSC#
REQ[4:0]#
GNT[4:0]#
GAD[31:0]
GC/BE[3:0]#
GFRAME#
GIRDY#
GTRDY#
GSTOP#
GDEVSEL#
GPERR#
GSERR#
GREQ#
GGNT#
GPAR
PIPE#
SBA[7:0]
RBF#
STOP#
ST[2:0]
SBSTB

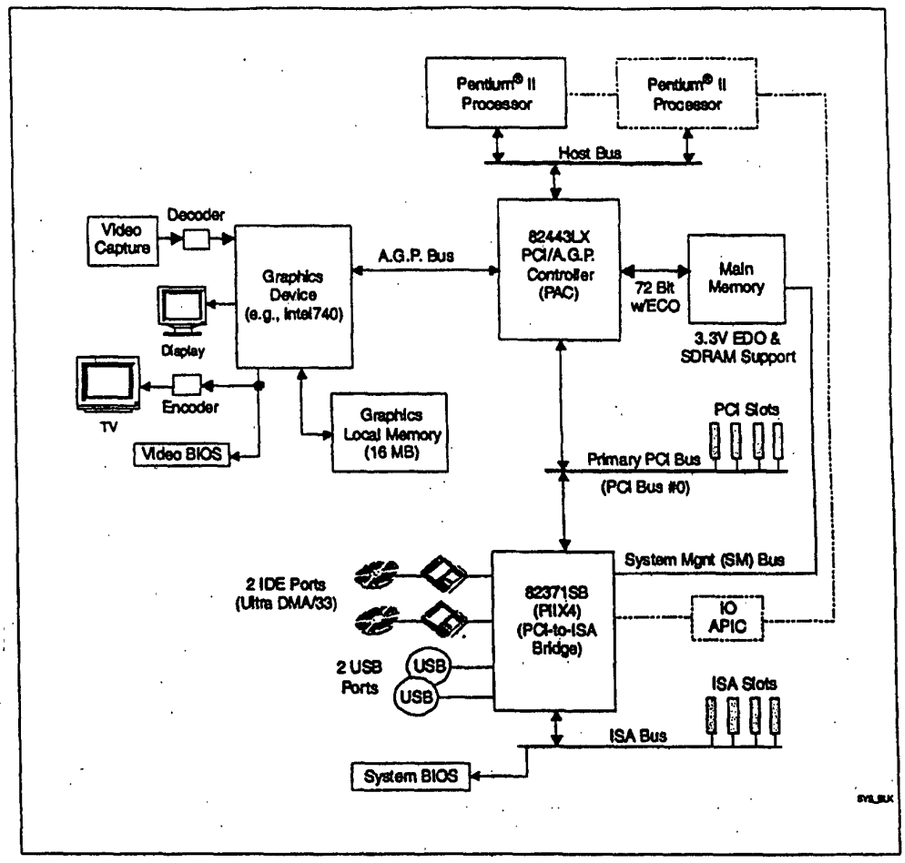
PAC integrates a Host-to-PCI bridge, optimized DRAM controller and data path, and an Accelerated Graphics Port (A.G.P.) interface. The A.G.P. is a high performance, component level interconnect, targeted at 3D graphics applications and based on a set of performance enhancements to PCI. The I/O subsystem portion of the PAC platform is based on the PIIX4, a highly integrated version of the Intel's PCI-to-ISA bridge family. The PAC is developed as the ultimate Pentium II processor platform and is targeted for emerging 3D graphics and multimedia applications. The PAC component includes the following functions and capabilities:

- Support for single and dual Pentium II processor configurations
- 64-bit GTL+ based Host Interface
- 32-bit Host address Support
- 64/72-bit Main Memory Interface with optimized support for SDRAM
- 32-bit PCI Bus Interface with integrated PCI arbiter
- A.G.P. Interface with up to 133-MHz data transfer capability
- Extensive Data Buffering between all interfaces for high throughput and concurrent operations

Figure 1 shows a block diagram of a typical platform based on the 440LX AGPset. The PAC host bus interface supports up to two Pentium II processors at 66 MHz. The physical interface design is based on the GTL+ specification. The PAC provides an optimized 72-bit DRAM interface (64-bit Data plus ECC). This interface supports 3.3V DRAM technologies. The PAC provides the interface to a PCI bus operating at 33 MHz. This interface implementation is compliant with PCI Rev 2.1 Specification. The PAC is the first Intel product that introduces the Accelerated Graphics Port interface. The PAC A.G.P. interface implementation is based on the A.G.P. Specification Rev 1.0. It can support up to 133-MHz data transfer rates.

PAC is designed to support the PIIX4 I/O bridge. PIIX4 is a highly integrated multi-functional component that supports the following functions and capabilities:

- PCI Rev 2.1 compliant PCI-to-ISA Bridge with support for 33-MHz PCI operations
- Deep Green Desktop Power Management Support
- Enhanced DMA controller
- 8259 Compatible Programmable Interrupt Controller
- System Timer functions
- Integrated IDE controller with Ultra DMA/33 support
- USB host interface with support for two USB ports
- System Management Bus (SMB) with support for DIMM Serial Presence Detect
- Support for an external I/O APIC component



The Pentium II processor supports a second level cache size of 256K or 512K. All cache control logic is provided in the Pentium II processor. PAC supports a maximum of 32-bit address or 4-GB memory address space from the processor perspective. PAC provides bus control signals and address paths for transfers between the processor's host bus, PCI bus, Accelerated Graphics Port and main memory. The PAC supports a 4-deep in-order queue (i.e., it provides support for pipelining of up to four outstanding transaction requests on the host bus). Due to the system concurrency requirements, along with support for pipelining of address requests from the host bus, the PAC supports general request queuing for all three interfaces (Host, A.G.P. and PCI).

National Semiconductor

July 1997

DS90CR215/DS90CR216
+3.3V Rising Edge Data Strobe LVDS 21-Bit Channel Link—66 MHz

General Description

The DS90CR215 transmitter converts 21 bits of CMOS/TTL data into three LVDS (Low Voltage Differential Signaling) data streams. A phase-locked transmit clock is transmitted in parallel with the data streams over a fourth LVDS link. Every cycle of the transmit clock 21 bits of input data are sampled and transmitted. The DS90CR216 receiver converts the LVDS data streams back into 21 bits of CMOS/TTL data. At a transmit clock frequency of 66 MHz, 21 bits of TTL data are transmitted at a rate of 462 Mbps per LVDS data channel. Using a 66 MHz clock, the data throughput is 1.386 GBit/s (173 Mbytes/s).

The multiplexing of the data lines provides a substantial cable reduction. Long distance parallel single-ended buses typically require a ground wire per active signal (and have very limited noise rejection capability). Thus, for a 21-bit wide data and one clock, up to 44 conductors are required. With the Channel Link chipset as few as 9 conductors (3 data pairs, 1 clock pair and a minimum of one ground) are needed. This provides a 80% reduction in required cable width, which provides a system cost savings, reduces connector physical size and cost, and reduces shielding requirements due to the cables' smaller form factor.

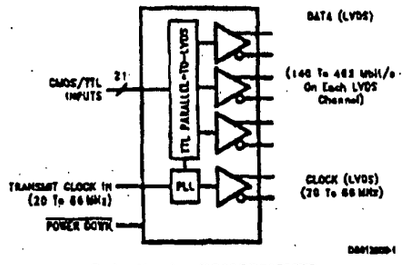
The 21 CMOS/TTL inputs can support a variety of signal combinations. For example, five 4-bit nibbles plus 1 control, or two 9-bit (byte + parity) and 3 control.

Features

- Single +3.3V supply
- Chipset (Tx + Rx) power consumption <250 mW (typ)
- Power-down mode (<0.5 mW total)
- Up to 173 Megabytes/sec bandwidth
- Up to 1.386 Gbps data throughput
- Narrow bus reduces cable size
- 290 mV swing LVDS devices for low EMI
- +1V common mode range (around +1.2V)
- PLL requires no external components
- Low profile 48-lead TSSOP package
- Rising edge data strobe
- Compatible with TIA/EIA-644 LVDS standard
- ESD Rating > 7 kV

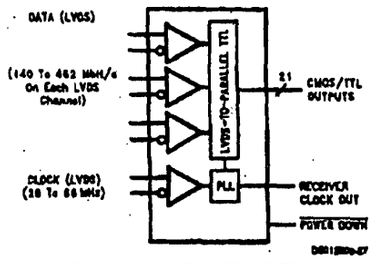
Block Diagrams

DS90CR215



Order Number DS90CR215MTD
See NS Package Number MTD48

DS90CR216

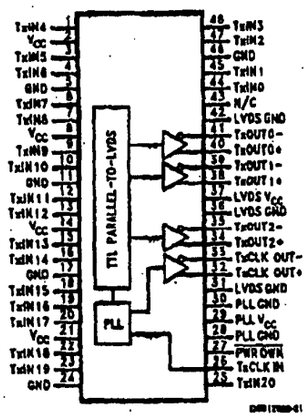


Order Number DS90CR216MTD
See NS Package Number MTD48

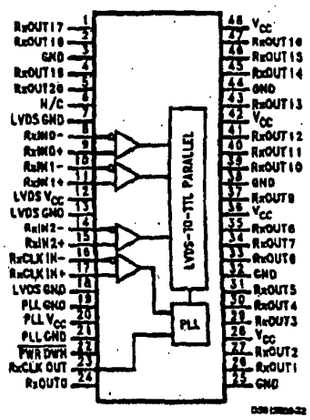
TRI-STATE® is a registered trademark of National Semiconductor Corporation.

© 1997 National Semiconductor Corporation DS012809

Pin Diagrams

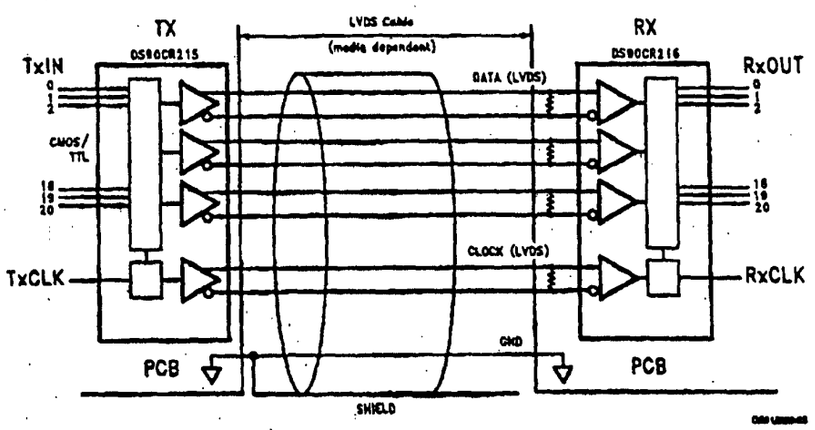


DS90CR215



DS90CR216

Typical Application



National Semiconductor

PRODUCT FOLDER

[Information as of 29-Oct-97]

DS90CR215

Plus-3.3V Rising Edge Data Strobe LVDS 21-Bit Channel and Link - 66 MHz

Generic P/N 90CR215

Contents

General Description
Features
Datasheet
Availability, Models, Samples & Pricing

General Description

The DS90CR215 transmitter converts 21 bits of CMOS/TTL data into three LVDS (Low Voltage Differential Signaling) data streams. A phase-locked transmit clock is transmitted in parallel with the data streams over a fourth LVDS link. Every cycle of the transmit clock 21 bits of input data are sampled and transmitted. The DS90CR216 receiver converts the LVDS data streams back into 21 bits of CMOS/TTL data. At a transmit clock frequency of 66 MHz, 21 bits of TTL data are transmitted at a rate of 462 Mbps per LVDS data channel. Using a 66 MHz clock, the data throughput is 1.386 Gbit/s (173 Mbytes/s).

The multiplexing of the data lines provides a substantial cable reduction. Long distance parallel single-ended buses typically require a ground wire per active signal (and have very limited noise rejection capability). Thus, for a 21-bit wide data and one clock, up to 44 conductors are required. With the Channel Link chipset as few as 9 conductors (3 data pairs, 1 clock pair and a minimum of one ground) are needed. This provides a 80% reduction in required cable width, which provides a system cost savings, reduces connector physical size and cost, and reduces shielding requirements due to the cables' smaller form factor.

The 21 CMOS/TTL inputs can support a variety of signal combinations. For example, five 4-bit nibbles plus 1 control, or two 9-bit (byte + parity) and 3 control.

Features

- Single +3.3V supply
- Chipset (Tx + Rx) power consumption <250 mW (typ)
- Power-down mode (<0.5 mW total)
- Up to 173 Megabytes/sec bandwidth

- Up to 1.386 Gbps data throughput
- Narrow bus reduces cable size
- 290 mV swing LVDS devices for low EMI
- +1V common mode range (around +1.2V)
- PLL requires no external components
- Low profile 48-lead TSSOP package
- Rising edge data strobe
- Compatible with TIA/EIA-644 LVDS standard
- ESD Rating > 7 kV

Datasheet

Receive datasheet via E-mail or download now ; use Adobe Acrobat to view...

DS90CR215/DS90CR216 +3.3V Rising Edge Data Strobe LVDS 21-Bit Channel Link-66 MHz (335 Kbytes; 4-Aug-97)

Availability, Models, Samples & Pricing

Part Number	Grade	Package		Status	Models		Samples & Small Qty Orders	Budgetary Pricing	
		Type	# pins		SPICE	IBIS		Quantity	$US ea
CLINK3V21BT-66	Commercial	evaluation board		Preliminary	N/A	N/A			N/
DS90CR215MTD	Commercial	TSSOP	48	Full production	N/A	N/A	Samples	100-999	$8.650
DS90CR215MTDX	Commercial	TSSOP	48	Full production	N/A	N/A		100-999	$8.700

QUICK SEARCH | PARAMETRIC SEARCH | SYSTEM DIAGRAMS | PRODUCT CATALOG | HOME

Enter Word or Part Number:

Feedback
Use of "Cookies"
Copyright © 1996 National Semiconductor Corporation
National is ISO 9000 certified.
webmaster@webteam.nsc.com
23-Sep-97

1. Introduction

1.1 P&D Overview

The purpose of this standard is to provide a digital interface and, optionally, an analogue interface for video data allowing a wide range of display devices to be attached to a single video port on the host system which may be a personal computer (PC), workstation or other device. This standard only defines the interface at the connector on the host system and provides additional recommendations regarding system implementation.

Monitors using a digital video interface generally have a fixed pixel format, typified by, but not restricted to, a Liquid Crystal Display (LCD) monitor. The objective is to retain data in a digital format thus eliminating the analogue conversion losses that cause screen artifacts. Retaining data in a digital format additionally provides opportunities for reducing system cost and simplifying the display setup.

The digital interface defined in this standard is referred to as Transition Minimised Differential Signaling (TMDS).

Analogue interface monitors are typified by, but not restricted to, CRT (cathode ray tube) based displays.

Prior to the P&D standard, the attachment of digital interface displays to PC's or workstations has required either:

- Conversion of the analogue interface to digital at the display with cost and image quality problems
- Provision of a separate graphics card with a digital interface with cost, space (slot for card), and the issues of a proprietary interface needing to be handled

Key features and benefits of the VESA P&D interface are:

- Single connector for any display device.
- Industry standard, interoperability from multiple suppliers.
- High quality display output.
- Scaleable cost and performance.
- Interoperable solution for analogue and digital monitors.
- Independent software and hardware layers.
- Operating System independent.
- Plug and Play enabled.
- Capable of using existing technology.
- Capable of working over several metres of cable.
- No DC component on interface.
- Low electromagnetic emission.
- Reduced pin count relative to parallel interface (typically 7:1 ratio).

The host receptacle interface defined in this standard is referred to as the P&D-A/D (Plug and Display - Analogue / Digital) in Section 12 which explains the relationships between this and other receptacles in the same family together with the expected monitor plugs.
The P&D-D receptacle shown in Section 12 is a logical extension of this standard for host applications not requiring an analogue option.

©Copyright 1997 Video Electronics Standards Association

5. Electrical Layer Specification: Digital (TMDS) Video Transmission Overview

Note: This section is an overview of the TMDS Interface and includes elements which are not part of the P&D standard.

5.1 Transition Minimised Differential Signaling Interface Overview

The VESA FPDI-2 and P&D Transition Minimised Differential Signaling (TMDS), interface standard is based on PanelLink™ Technology developed by Silicon Image, Inc. of Palo Alto, California. The TMDS interface takes parallel data from the host graphics controller and transmits it serially at high speed to the receiver.

The characteristics of this interface are:

- Uses 3 differential data pairs with timing and control data embedded in data transmission.
- Uses transition controlled binary DC balanced coding for reliable, low-power, and high-speed data transmission.
- Uses low-swing differential voltage.

5.1.1 Introduction

As the data rate from a variety of multimedia sources is increasing at the desktop computing systems interface, a safe and reliable transmission of data at high-speed essential. Video data transmission between computer systems and flat-panel displays (e.g. liquid crystal displays) requires higher speed interconnects for increasing video data. Existing digital interconnect systems for such applications typically employ single ended parallel data streams. The bandwidth requirement increases following the increase in display addressibility or allowing multiple devices to be connected and the parallel interface may give problems with EMI and noisy transmission.

The number of signals required in a parallel interface makes the video transmission difficult and inflexible as signals may interfere each other and thus cables are short. The TMDS interconnect system not only reduces the number of data signals required for high bandwidth data transmission but also minimises the EMI using low swing differential voltage transmission with a new coding scheme for low power operation and simple clocking methods. TMDS technology uses a DC balanced and transition minimised coding scheme for low power operation, and a method of embedding timing and video control signals into the data streams, which further reduces the number of signals required. TMDS technology can be applied to interfacing LCDs and other flat-panel displays that require digital interface for reliable data transmission or remote display application where distance between the display and the host system is relatively long. In the latter case, the transmission media can be fiber optics using serial digital signal.

5.1.2 Logical Architecture

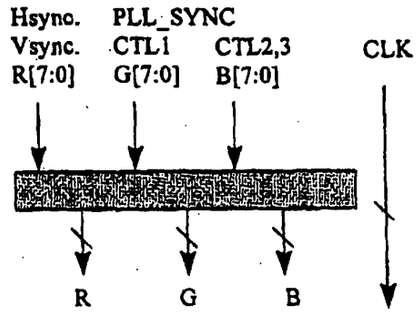


Figure 5-1 : Simplified Block Diagram of a TMDS Interface with Clock + RGB

©Copyright 1997 Video Electronics Standards Association

The high-data rate link system is composed of 3 data lines and an accompanying clock. Signal transmission media can be either a terminated cables such as twin-axial cable or twisted pair with screen return or an optical fiber, in this case a driver and an amplifier for a laser diode and a PIN diode respectively are a signal load and a source for the video link.
The voltage swing on the cable is adjustable[1] with 500mV being the recommended voltage. Since its swing is differential on the pair, the net signal on the pair is required to have a swing twice larger than the single-ended signal. It is required to make the transmitter interface have an externally adjustable current level, in cases when a standard level is not used for maximal current reduction. The implemented interconnect system is required to use low-swing signal on only four terminated lines, so there will be significantly reduced electromagnetic interference (EMI).

For an unconditionally P&D TMDS inter-operable transmitter, the output current level is set at the maximum (12 mA). For limited-domain applications (e.g. notebooks) make the output current level adjustable so that the transmitter can accommodate various kinds of cable and receiver types with minimum power.

The voltage difference between the AVCC and EXT_SWING pin determines the voltage swing of the differential signal pairs. This adjustable low voltage differential swing can be used for various cable lengths. A larger voltage swing would be used for longer cables, and a lower voltage swing should be used for shorter cables. Sometimes larger voltage swings can cause noise on shorter cables due to transmission line effects. It is absolutely necessary to adjust the voltage swing accordingly to the length and type of the cable. The larger the voltage swing, the higher the power consumption.

If the EXT_SWING pin is left unconnected, the internal voltage divider circuit will set the EXT_SWING pin at approximately 2.8V when AVCC is at 3.3V, producing approximately a 500mV swing on the differential signal pairs. The differential voltage level swing for single ended is set by the formula:

$V_{SWING} = 0.5V \times (500\Omega / R_{EXT_SWING})$ where V_{SWING} = Single Ended Differential voltage swing

R_{EXT_SWING} = External Resistor on EXT_SWING pin

Rs (RPOT1)	Vs (Theoretical Calculation)
300Ω	833mV
400Ω	625mV
500Ω	500mV
600Ω	417mV
700Ω	357mV
800Ω	313mV
900Ω	278mV
1KΩ	250mV

Table 5-1 : Theoretical Low Voltage Single Ended Differential Swing Level Relative to R_{EXT_SWING}

[1] The P&D standard requires the voltage swing to be preset.

©Copyright 1997 Video Electronics Standards Association

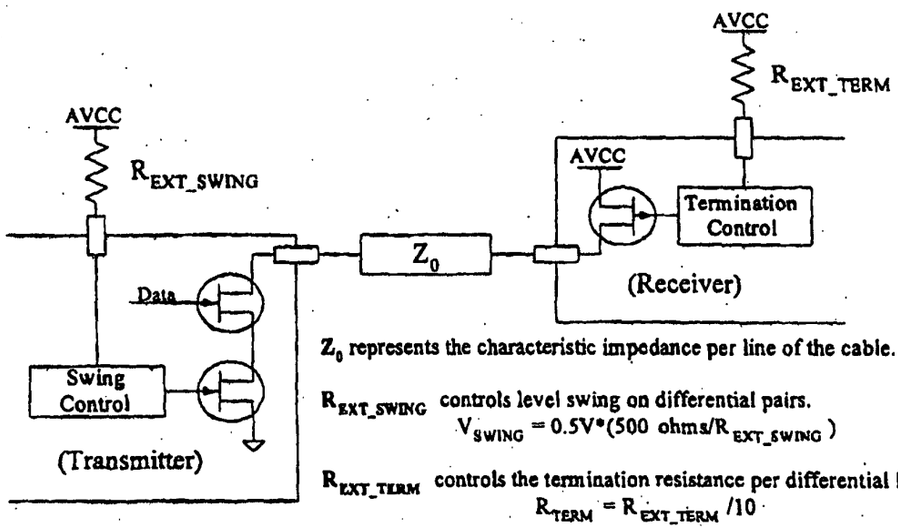


Figure 5-2 : Transition Minimised Differential Voltage Swing Adjust

From the above figure, TMDS technology uses current drive to develop the low voltage differential signal at the receiver side of the transmission line.

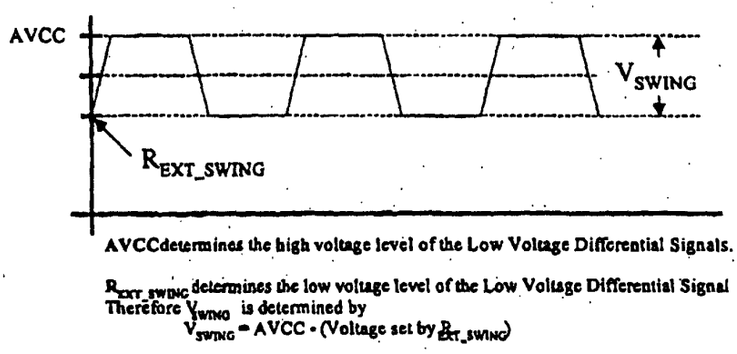
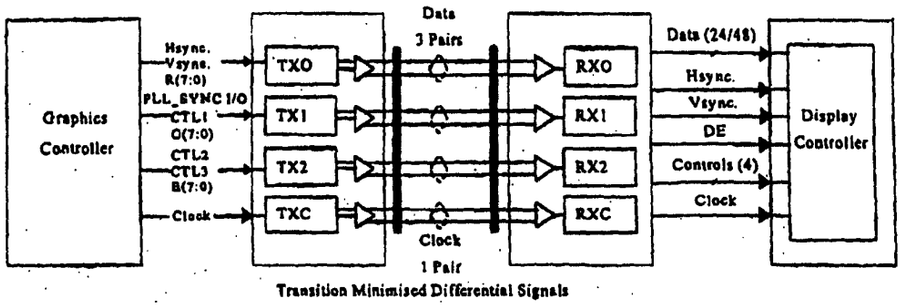


Figure 5-3 : Single Ended Transition Minimised Differential Signal Adjustment

From figure 5.3, the high voltage level of the low voltage differential signals will be set by AVCC, the low voltage is adjustable with the low voltage differential swing control circuit. The low voltage differential voltage swing is adjustable by using a potentiometer (R_{EXT_SWING}).

Video signals are composed of three separate signals, typically RGB, along with two synchronisation signals called Hsync. and Vsync. Instead of having extra lines, those two sync. signals are mixed with the RGB data in the encoder, thereby limiting the number of data pairs to three. The transition-controlled digital encoding will encode 8-bit of data, data enable (DE), and 2-bit of control signals. Control signals are allowed to change only during "blank" time when DE is low/inactive, therefore, the levels of the control signals are constant during active data area when DE is high.

©Copyright 1997 Video Electronics Standards Association



Note: Each pair requires a current return

Figure 5-4 : System Environment Block Diagram Example

The system provides parallel interfaces to both the computer system's display/graphics controller and the display devices, and thus no modification to existing system is required other than adding a TMDS transmitter IC and a TMDS receiver IC.

5.1.3 Summary

TMDS technology implements a high-speed video data transmission system capable of converting parallel video data stream and video display timing and control signals to three high-speed serial differential data pairs at speeds capable of supporting high-resolution displays (e.g. 800x600 color pixels and above addressibilities).

Shown below is a sample of typical monitor requirements for update and refresh rates:

Addressability	Frame Rate (Hz)	Pixel Clock (MHz)	Data Rate (Mbytes/s) Post Palette 12bpp	Data Rate (Mbytes/s) Post Palette 24bpp
Update Rate (Shadow Buffer in Monitor)				
640 x 480	60	25	37.5	75
720 x 400	70	28	42	84
800 x 600	60	40	60	120
1024 x 768	30	23.59	35.38	70.77
1280 x 1024	30	40	60	120
2000 x 2000	30	120	180	360
1280 x 720	30	27.64	41.46	82.92
1920 x 1080	30	62.2	93.3	186.6
CRT Compatible Refresh Rates				
640 x 480	60	25	37.7	75
720 x 400	70	28	42	84
800 x 600	60	40	60	120
1024 x 768	60	65	97.5	195
1280 x 1024	60	112	168	336
1600 x 1200	75	250	375	750
2500 x 2000	75	384	575	1150
1280 x 720	60	77.5	116.25	232.5
1920 x 1080	30(1)	77.5	115.8	231.6

Table 5-2 : Addressability Table

©Copyright 1997 Video Electronics Standards Association

Transaction History Date 1999-03-15
Date information retrieved from USPTO Patent Application Information Retrieval (PAIR) system records at www.uspto.gov

receipt #4

OIPE JC37 MAR 15 1999 PATENT & TRADEMARK OFFICE

PATENT
Docket No. 387112000300

CERTIFICATE OF MAILING BY "FIRST CLASS MAIL"

I hereby certify that this correspondence is being deposited with the United States Postal Service as first class mail in an envelope addressed to: Assistant Commissioner for Patents, Washington, D.C. 20231, on March 11, 1999.

Janet Hollrah

Janet Hollrah

RECEIVED
APR 9 1 1999
Group 2700

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In the application of:

WILLIAM W. Y. CHU

Serial No.: 09/149,882

Filing Date: September 8, 1998

For: A COMMUNICATION CHANNEL AND INTERFACE DEVICES FOR BRIDGING COMPUTER INTERFACE BUSES

Examiner: Not Assigned

Group Art Unit: 2782

RECEIVED
MAR 2 6 1999
Group 2700

TRANSMITTAL

Assistant Commissioner for Patents
Washington, D.C. 20231

Dear Sir:

Transmitted herewith for filing in the above-captioned matter is the following:

- ☒ Request For a Corrected Filing Receipt (two pages);
- ☒ Marked-Up Filing Receipts (copies, two pages); and
- ☒ Return Receipt Postcard.

In the unlikely event that the transmittal letter is separated from this request and the Patent Office determines that a fee is required, applicant petitions for any required relief including extensions of time and authorizes the Assistant Commissioner to charge the cost of such petitions and/or other fees due in connection with the filing of this document to **Deposit**

sf-658136

Account No. 03-1952 referencing Docket No. 387112000300. However, the Assistant Commissioner is not authorized to charge the cost of the issue fee to the Deposit Account.



Respectfully submitted,

Dated: March 11, 1999

By: Ararat Kapouytian

Ararat Kapouytian
Registration No. 40,044

Morrison & Foerster LLP
425 Market Street
San Francisco, California 94105-2482
Telephone: (415) 268-6147
Facsimile: (415) 268-7522

PATENT
Docket No. 387112000300

CERTIFICATE OF MAILING BY "FIRST CLASS MAIL"

I hereby certify that this correspondence is being deposited with the United States Postal Service as first class mail in an envelope addressed to: Assistant Commissioner for Patents, Washington, D.C. 20231, on March 11, 1999

Janet Hollrah

Janet Hollrah

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE



In the application of:

WILLIAM W. Y. CHU

Serial No.: 09/149,882

Filing Date: September 8, 1998

For: A COMMUNICATION CHANNEL AND INTERFACE DEVICES FOR BRIDGING COMPUTER INTERFACE BUSES

Examiner: Not Assigned

Group Art Unit: 2782

RECEIVED
MAR 26 1999
Groun 2700

REQUEST FOR A CORRECTED FILING RECEIPT

Assistant Commissioner for Patents
Washington, D.C. 20231

Dear Sir:

Please furnish the undersigned with a corrected Filing Receipt for the above-identified application. On October 21, 1998, we submitted a Request For a Corrected Filing Receipt, but the revised Filing Receipt that we received did not reflect all of our requested corrections. The corrections needed are as follows: Please delete the title "COMMUNICATION CHANNEL AND INTERFACE DEVICE FOR BRIDGING COMPUTER INTERFACE BUSES" and replace with the title "A COMMUNICATION CHANNEL AND INTERFACE DEVICES FOR BRIDGING COMPUTER INTERFACE BUSES". A copy of the two previous marked-up Filing Receipts are attached.

sf-658120

In the unlikely event that the transmittal letter is separated from this request and the Patent Office determines that a fee is required, applicant petitions for any required relief including extensions of time and authorizes the Assistant Commissioner to charge the cost of such petitions and/or other fees due in connection with the filing of this document to **Deposit Account No. 03-1952** referencing Docket No. 387112000300. However, the Assistant Commissioner is not authorized to charge the cost of the issue fee to the Deposit Account.



Respectfully submitted,

Dated: March 11, 1999 By: Ararat Kapouytian

Ararat Kapouytian
Registration No. 40,044

Morrison & Foerster LLP
425 Market Street
San Francisco, California 94105-2482
Telephone: (415) 268-6147
Facsimile: (415) 268-7522

PTO-103X
(Rev. 8-95)

FILING RECEIPT

RECEIVED
OCT 0 1 1998
MORRISON & FOERSTER

UNITED STATES DEPARTMENT OF COMMERCE
Patent and Trademark Office
ASSISTANT SECRETARY AND COMMISSIONER
OF PATENTS AND TRADEMARKS
Washington, D.C. 20231

APPLICATION NUMBER	FILING DATE	GRP ART UNIT	FIL FEE REC'D	ATTORNEY DOCKET NO.	DRWGS	TOT CL	IND CL
09/149,882	09/08/98	2782	$0.00	387112000300	57	42	9

MORRISON & FOERSTER
425 MARKET STREET
SAN FRANCISCO CA 94105-2482

OIPE JC37 MAR 15 1999 PATENT & TRADEMARK OFFICE

Receipt is acknowledged of this nonprovisional Patent Application. It will be considered in its order and you will be notified as to the results of the examination. Be sure to provide the U.S. APPLICATION NUMBER, FILING DATE, NAME OF APPLICANT, and TITLE OF INVENTION when inquiring about this application. Fees transmitted by check or draft are subject to collection. Please verify the accuracy of the data presented on this receipt. If an error is noted on this Filing Receipt, please write to the Application Processing Division's Customer Correction Branch within 10 days of receipt. Please provide a copy of the Filing Receipt with the changes noted thereon.

Applicant(s)

WILLIAM W. Y. CHU.

CONTINUING DATA AS CLAIMED BY APPLICANT-
PROVISIONAL APPLICATION NO. 60/083,886 05/01/98
PROVISIONAL APPLICATION NO. 60/092,706 07/14/98

INTERFACE
A

FOREIGN FILING LICENSE GRANTED 09/25/98
TITLE
COMMUNICATION CHANNEL AND INTERFACE ~~DEVICE~~ DEVICES FOR BRIDGING COMPUTER ~~INTERFACE~~ BUSES

PRELIMINARY CLASS: 395

(see reverse)

TO-103X
Rev. 8-96)

RECEIVED B

FILING RECEIPT DEC 17 1998

MORRISON & FOERSTER

UNITED STATES DEPARTMENT OF COMMERCE
Patent and Trademark Office
ASSISTANT SECRETARY AND COMMISSIONER
OF PATENTS AND TRADEMARKS
Washington, D.C. 20231

APPLICATION NUMBER	FILING DATE	GRP ART UNIT	FIL FEE REC'D	ATTORNEY DOCKET NO.	DRWGS	TOT CL	IND CL
09/149,882	09/08/98	2782	$948.00	387112000300	57	42	9

ARARAT KAPOUYTIAN
MORRISON AND FOERSTER
425 MARKET STREET
SAN FRANCISCO CA 94105-2482

OIPE JC37 MAR 15 1999 PATENT & TRADEMARK OFFICE

Receipt is acknowledged of this nonprovisional Patent Application. It will be considered in its order and you will be notified as to the results of the examination. Be sure to provide the U.S. APPLICATION NUMBER, FILING DATE, NAME OF APPLICANT, and TITLE OF INVENTION when inquiring about this application. Fees transmitted by check or draft are subject to collection. Please verify the accuracy of the data presented on this receipt. If an error is noted on this Filing Receipt, please write to the Application Processing Division's Customer Correction Branch within 10 days of receipt. Please provide a copy of the Filing Receipt with the changes noted thereon.

Applicant(s)

WILLIAM W. Y. CHU, LOS ALTOS, CA.

CONTINUING DATA AS CLAIMED BY APPLICANT-
PROVISIONAL APPLICATION NO. 60/083,886 05/01/98
PROVISIONAL APPLICATION NO. 60/092,706 07/14/98

FOREIGN FILING LICENSE GRANTED 09/25/98 * SMALL ENTITY *

TITLE

A COMMUNICATION CHANNEL AND INTERFACE ~~DEVICE~~ DEVICES FOR BRIDGING COMPUTER INTERFACE BUSES

PRELIMINARY CLASS: 395

DATA ENTRY BY: FARMER, CHANELL TEAM: 03 DATE: 12/11/98

(see reverse)

OIPE JC89
NOV 15 1999
PATENT & TRADEMARK OFFICE

GTP 2782
#6
RECEIVED
NOV 19 1999
TECH CENTER 2700

PATENT
Docket No. 387112000300

CERTIFICATE OF MAILING BY "FIRST CLASS MAIL"

I hereby certify that this correspondence is being deposited with the United States Postal Service as first class mail in an envelope addressed to: Assistant Commissioner for Patents, Washington, D.C. 20231 on November 10, 1999.

Janet Hollrah

Janet Hollrah

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In the application of:

William W.Y. Chu

Serial No.: 09/149,882

Filing Date: September 8, 1998

For: COMMUNICATION CHANNEL AND INTERFACE DEVICES FOR BRIDGING COMPUTER INTERFACE BUSES

Examiner: Not Yet Assigned

Group Art Unit: 2782

SUPPLEMENTAL INFORMATION DISCLOSURE STATEMENT UNDER 37 C.F.R. § 1.97

Assistant Commissioner for Patents
Washington, D.C. 20231

Dear Sir:

Pursuant to 37 C.F.R. § 1.97 and § 1.98, applicants submit for consideration in the above-identified application the documents listed on the attached Form PTO-1449. The documents listed on the attached PTO-1449 were cited in a communication from a foreign patent office not more than three months prior to the filing of this statement. Copies of the documents are submitted herewith. The Examiner is requested to make these documents of record.

sf-782307

Foreign Documents

European Patent No. EP 0 722 138 A to International Business Machines Corporation

PCT WO 92/18924 A to Boris Wallsten

PCT WO 94/00970 A to Oakleigh Systems, Inc.

PCT WO 95/13640 A to Oakleigh Systems, Inc.

Patent Abstracts of Japan 095(001)(February 28, 1995)(for Japanese publication NO. JP 06 289953 A to Hitachi Ltd.(10/18/94)

This Information Disclosure Statement is submitted:

☒ Within three months of the application filing date or before receipt of a first Office Action on the merits; accordingly, no fee or separate requirements are required.

☐ After receipt of a first Office Action on the merits but before a final Office Action or Notice of Allowance.

- ☐ A fee is required. A check in the amount of * is enclosed.
- ☐ A Certification under 37 C.F.R. § 1.97(e) is provided below; accordingly; no fee is believed to be due.

☐ After receipt of a final Office Action or Notice of Allowance, but before payment of the issue fee. Accordingly, a Petition requesting consideration of the Information Disclosure Statement, an authorization to charge our deposit account, and a Certification under 37 C.F.R. § 1.97(e) are provided herein.

Applicants would appreciate the Examiner initialing and returning the Form PTO-1449, indicating that the information has been considered and made of record herein.

This Supplemental Information Disclosure Statement under 37 C.F.R. § 1.97 is not to be construed as a representation that: (i) a complete search has been made; (ii) additional information material to the examination of this application does not exist; (iii) the information,

protocols, results and the like reported by third parties are accurate or enabling; or (iv) the above information constitutes prior art to the subject invention.

In the unlikely event that the transmittal letter is separated from this document and the Patent Office determines that an extension and/or other relief is required, applicant petitions for any required relief including extensions of time and authorizes the Assistant Commissioner to charge the cost of such petitions and/or other fees due in connection with the filing of this document to **Deposit Account No. 03-1952** referencing 387112000300. However, the Assistant Commissioner is not authorized to charge the cost of the issue fee to the Deposit Account.

Dated: November 10, 1999

Respectfully submitted,

By: Ararat Kapouytian

Ararat Kapouytian
Registration No. 40,044

Morrison & Foerster LLP
425 Market Street
San Francisco, California 94105-2482
Telephone: (415) 268-7000
Facsimile: (415) 268-7522

NOV 15 1999 JC89 PATENT & TRADEMARK OFFICE

#6

PTO/SB/08 (2-92)
Sheet 1 of 1

Form PTO-1449

INFORMATION DISCLOSURE CITATION IN AN APPLICATION

(Use several sheets if necessary)

Docket Number 387112000300	Application Number 09/149,882
Applicant: William W. Y. Chu	
Filing Date September 8, 1998	Group Art Unit 2782

RECEIVED NOV 17 1999 TECHNOLOGY CENTER 2700 MAIL ROOM

U.S. PATENT DOCUMENTS

Examiner Initials	Ref. No.	Date	Document No.	Name	Class	Subclass	Filing Date If Appropriate

FOREIGN PATENT DOCUMENTS

Examiner Initials	Ref. No.	Date	Document No.	Country	Class	Subclass	Translation YES	Translation NO
C	1.	(07/17/96)	0 722 138 A	EP				
✓	2.	(10/29/92)	92 18924 A	WO				
✓	3.	(01/06/94)	94 00970 A	WO				
✓	4.	(05/18/95)	95 13640 A	WO				
✓	5.	(10/18/94)	06 289953 A	JP				

OTHER DOCUMENTS

(including author, title, Date, Pertinent Pages, Etc.)

Examiner Initials	Ref. No.	Title

EXAMINER: (examiner)	DATE CONSIDERED: 5-10-00

EXAMINER: Initial if citation considered, whether or not the citation conforms with MPEP 609. Draw a line through the citation if not in conformance and not considered. Include a copy of this form with next communication to applicant.

Transaction History Date 2000-06-15
Date information retrieved from USPTO Patent Application Information Retrieval (PAIR) system records at www.uspto.gov

BEST COPY

UNITED STATES DEPARTMENT OF COMMERCE
Patent and Trademark Office
Address: COMMISSIONER OF PATENTS AND TRADEMARKS
Washington, D.C. 20231

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.
09/143,[illegible]	07/08/98	[illegible]	[illegible]300

LM02/0615

ARARAT KAPOUYTIAN
MORRISON AND FOERSTER
425 MARKET STREET
SAN FRANCISCO CA 94105-2482

EXAMINER	
[illegible]	

ART UNIT	PAPER NUMBER
2784	7

DATE MAILED: 06/15/00

Please find below and/or attached an Office communication concerning this application or proceeding.

Commissioner of Patents and Trademarks

PTO-90C (Rev. 2/95) 1- File Copy

UNITED STATES DEPARTMENT OF COMMERCE
Patent and Trademark Office
Address: COMMISSIONER OF PATENTS AND TRADEMARKS
Washington, D.C. 20231

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.
09/149,882	09/08/98	CHU	W 38711200300

LM02/0615

ARARAT KAPOUYTIAN
MORRISON AND FOERSTER
425 MARKET STREET
SAN FRANCISCO CA 94105-2482

EXAMINER	
CAO,C	
ART UNIT	**PAPER NUMBER**
2782	7

DATE MAILED: 06/15/00

Please find below and/or attached an Office communication concerning this application or proceeding.

Commissioner of Patents and Trademarks

PTO-90C (Rev. 2/95) 1- File Copy

Office Action Summary

Application No.	Applicant(s)
09/149,882	Chu
Examiner	**Group Art Unit**
Chun Cao	2782

☒ Responsive to communication(s) filed on *Sep 8, 1998*

☐ This action is **FINAL.**

☐ Since this application is in condition for allowance except for formal matters, **prosecution as to the merits is closed** in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11; 453 O.G. 213.

A shortened statutory period for response to this action is set to expire *3* month(s), or thirty days, whichever is longer, from the mailing date of this communication. Failure to respond within the period for response will cause the application to become abandoned. (35 U.S.C. § 133). Extensions of time may be obtained under the provisions of 37 CFR 1.136(a).

Disposition of Claim

☒ Claim(s) *1-42* is/are pending in the applicat

Of the above, claim(s) _____ is/are withdrawn from consideration

☐ Claim(s) _____ is/are allowed.

☒ Claim(s) *1-42* is/are rejected.

☐ Claim(s) _____ is/are objected to.

☐ Claims _____ are subject to restriction or election requirement.

Application Papers

☒ See the attached Notice of Draftsperson's Patent Drawing Review, PTO-948.

☐ The drawing(s) filed on _____ is/are objected to by the Examiner.

☐ The proposed drawing correction, filed on _____ is ☐ approved ☐ disapproved.

☐ The specification is objected to by the Examiner.

☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. § 119

☐ Acknowledgement is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d).

☐ All ☐ Some* ☒ None of the CERTIFIED copies of the priority documents have been

☐ received.

☐ received in Application No. (Series Code/Serial Number) _____.

☐ received in this national stage application from the International Bureau (PCT Rule 17.2(a)).

*Certified copies not received: _____

☐ Acknowledgement is made of a claim for domestic priority under 35 U.S.C. § 119(e).

Attachment(s)

☒ Notice of References Cited, PTO-892

☒ Information Disclosure Statement(s), PTO-1449, Paper No(s). *5 and 6*

☐ Interview Summary, PTO-413

☒ Notice of Draftsperson's Patent Drawing Review, PTO-948

☐ Notice of Informal Patent Application, PTO-152

--- SEE OFFICE ACTION ON THE FOLLOWING PAGES ---

DETAILED ACTION

1. Claims 1- 42 are presented for examination.

Drawings

2. Figure 1 should be designated by a legend such as --Prior Art-- because only that which is old is illustrated. See MPEP § 608.02(g).

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. Claims 1-8, 10-19, 23 and 42 are rejected under 35 U.S.C. 103(a) as being unpatentable over MacLaren, U.S. Patent No. 6,052,513 in view of Todd et al., U.S. Patent No. 4,700,362.

As claims 1 and 4-6, MacLaren discloses a computer system [10, fig. 1], an apparatus for bridging a first computer interface bus [24, fig. 3] and a second computer interface bus [32, fig. 3], each of the first and second computer interface buses having a number of parallel multiplexed address/data bus lines, each of said bus lines operating at a clock speed range having a minimum

and a maximum clock speed [col. 6, lines 57-64; fig. 5; col. 52, lines 26-39], said apparatus comprising:

a first interface controller [26, fig. 3] coupled to the first computer interface bus and a second interface controller [48, fig. 3] coupled to the second interface bus [col. 7, lines 43-45];

a interface channel [104, fig. 3] coupled to the first interface controller, and said interface channel having a clock channel [102, fig.3];

In summary, MacLaren's system manages control signals from the first computer interface bus encoding into multiplex time-multiplexed messages [col. 52, lines 8-20] and decoding multiplex time-multiplexed messages to second computer interface bus [col. 7, line 66-col. 8, line 1]. MacLaren does not teach of encoding control signals to control bits and decoding control bits to control signals.

Todd et al discloses an A-D encoder and a D-A decoder system [abstract]. Todd et al teaches of converting control signals to bit-stream of digital signals [col. 5, lines 16-19], and converting the bit-stream of digital signals to control signals [col. 5, lines 38-40].

It would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the teachings of MacLaren and Todd et al because Todd et al's teachings of encoding control signals and decoding control bits would improve the efficiency and accuracy of MacLaren system by allowing the interface channel to communicate between first and second PCI buses.

As per claim 2, MacLaren's system discloses a first interface controller comprising a host interface controller (HIC) [108, fig. 3], and a second interface controller comprising a peripheral interface controller (PIC)[126, fig. 3].

As per claims 3, MacLaren discloses a interface channel using a low voltage differential signal (LVDS) method [col. 59, lines 2-16]. MacLaren does not explicitly disclose a first translator and a second translator coupling to transmitters and receivers respectively. Inherently, MacLaren discloses translators coupling to transmitters [192, 194, fig. 5] and receivers [196, 198, fig. 5] respectively [col. 52, lines 15-19].

As claims 7 and 12-13, MacLaren discloses a reset line [col. 57, lines 31-33].

As per claim 8, MacLaren teaches a interface channel operating at a high clock speed than the clock speed of the first and second computer interface buses [col. 52, lines 26-39].

As claims 10-11 and 14-15 are written in means plus function and contain the same limitations as claims 1 and 3, therefore the same rejections applied.

As claims 16-19 are written in means plus function and contain the same limitations as claims 1 and 3, therefore the same rejections applied.

As claim 23 is written in means plus function and contain the same limitations as claims 1 and 8, therefore the same rejections applied.

As per claim 42, MacLaren and Todd et al together teach the claimed system. Therefore, MacLaren and Todd et al together teach the claimed method for carrying out the system.

5. Claim 9, 20-22 and 24-41 are rejected under 35 U.S.C. 103(a) as being unpatentable over MacLaren, U.S. Patent No. 6,052,513 and Todd et al., U.S. Patent No. 4,700,362 as applied to claim 1 above, further in view of Dempsey et al., U.S. Patent No. 5,826,048.

MacLaren and Todd et al together do not teach of the interface channel having fewer in number than both the number of bus lines of the first and second computer interface bus. Therefore , providing the interface channel with a reduced number of signal lines. Dempsey et al teaches of converting the PCI transactions into single corresponding MPCI transaction signal by time-division multiplex, [col. 2, lines 60-col. 3, line 5], thereof, reducing number of pins/signals of the interface channel.

It would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the teachings of MacLaren and Todd et al and Dempsey et al because Dempsey et al's teachings of reducing number of pins/signals of the interface channel would reduce the cost of the MacLaren-Todd system.

As claims 20-22 are written in means plus function and contain the same limitations as claims 1 and 9, therefore the same rejections applied.

As claims 24-41 are written in means plus function and contain the same limitations as claims 1 and 9, therefore the same rejections applied.

Any response to this action should be mailed to:

Commissioner of Patents and Trademarks

Washington, D.C. 20231

or faxed to:

(703) 308-9051, (for formal communications intended for entry)

Or:

(703) 306-5404 (for informal or draft communications, please label "PROPOSED" or "DRAFT")

Hand-delivered responses should be brought to Crystal Park II, 2121 Crystal Drive, Arlington. VA., Sixth Floor (Receptionist).

6. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Chun Cao at (703)308-6106. The examiner can normally be reached on Monday-Friday from 7:30 am - 4:00 pm. If attempts to reach the examiner by phone are unsuccessful, the examiner's supervisor Thomas Lee can be reached at (703)305-9717. The fax number for this Art Unit is (703) 308-9051.

Any inquiry of a general nature or relating to the status of this application should be directed to the Group receptionist whose telephone number is (703)305-9600.

Chun Cao

June 5, 2000

THOMAS C. LEE
SUPERVISORY PATENT EXAMINER
GROUP 2700

FORM PTO-892	U.S. DEPARTMENT OF COMMERCE PATENT AND TRADEMARK OFFICE	SERIAL NO.	GROUP ART UNIT	ATTACHMENT TO PAPER NO.	
NOTICE OF REFERENCES CITED		09/149882	2782		7
		APPLICANT(S) Chu			

U.S. PATENT DOCUMENTS

*		DOCUMENT NO.	DATE	NAME	CLASS	SUB-CLASS	FILING DATE
	A	4,700,362	10/1987	Todd et al.	375	249	
	B	4,939,735	7/1990	Fredericks et al.	714	798	
	C	5,826,048	10/1998	Dempsey et al	710	129	
	D	5,848,249	12/1998	Garbus et al	710	128	
	E	5,859,669	1/1999	Prentice	348	469	
	F	5,907,566	5/1999	Benson et al	714	798	
	G	5,960,213	9/1999	Wilson	710	2	
	H	5,968,144	10/1999	Walker et al.	709	100	
	I	5,991,844	11/1999	Khosrowpour	710	129	
	J	6,040,792	3/2000	Watson et al.	341	100	
	K	6,052,513	4/2000	MacLaren	395	294	

FOREIGN PATENT DOCUMENTS

*		DOCUMENT NO.	DATE	COUNTRY	NAME	CLASS	SUB-CLASS
	L						
	M						
	N						
	O						
	P						
	Q						

OTHER REFERENCES (Including Author, Title, Date, Pertinent Pages, Etc.)

	R	
	S	
	T	
	U	

EXAMINER	DATE	
Chun Cao	June 5, 2000	Form892ccs2106b

* A copy of this reference is not being furnished with this office action.
(See Manual of Patent Examining Procedure, section 707.05(a).)

Form PTO 948 (Rev. 8-98) U.S. DEPARTMENT OF COMMERCE - Patent and Trademark Office Application No. 09/149882

NOTICE OF DRAFTSPERSON'S PATENT DRAWING REVIEW

The drawing(s) filed (insert date) 9/8/98 are:

A. ☐ approved by the Draftsperson under 37 CFR 1.84 or 1.152.

B. ☒ objected to by the Draftsperson under 37 CFR 1.84 or 1.152 for the reasons indicated below. The Examiner will require submission of new, corrected drawings when necessary. Corrected drawing must be sumitted according to the instructions on the back of this notice.

1. DRAWINGS. 37 CFR 1.84(a): Acceptable categories of drawings: Black ink. Color.
   - ___ Color drawings are not acceptable until petiton is granted. Fig(s) _____
   - ___ Pencil and non black ink not permitted. Fig(s) _____
2. PHOTOGRAPHS. 37 CFR 1.84 (b)
   - ___ 1 full-tone set is required. Fig(s) _____
   - ___ Photographs not properly mounted (must use brystol board or photographic double-weight paper). Fig(s) _____
   - ___ Poor quality (half-tone). Fig(s) _____
3. TYPE OF PAPER. 37 CFR 1.84(e)
   - ___ Paper not flexible, strong, white, and durable. Fig(s) _____
   - ___ Erasures, alterations, overwritings, interlineations, folds, copy machine marks not accepted. Fig(s) _____
   - ___ Mylar, velum paper is not acceptable (too thin). Fig(s) _____
4. SIZE OF PAPER. 37 CFR 1.84(f): Acceptable sizes:
   - ___ 21.0 cm by 29.7 cm (DIN size A4)
   - ___ 21.6 cm by 27.9 cm (8 1/2 x 11 inches)
   - ___ All drawing sheets not the same size. Sheet(s) _____
   - ___ Drawings sheets not an acceptable size. Fig(s) _____
5. MARGINS. 37 CFR 1.84(g): Acceptable margins:

   Top 2.5 cm Left 2.5cm Right 1.5 cm Bottom 1.0 cm
   SIZE: A4 Size

   Top 2.5 cm Left 2.5 cm Right 1.5 cm Bottom 1.0 cm
   SIZE: 8 1/2 x 11

   Margins not acceptable. Fig(s) 1-3, 5-7, 11, 17-19, 21
   - ___ Top (T) ☒ Left (L) 25, 26, 28, 29, 33, 40, 47-50
   - ___ Right (R) ___ Bottom (B)
6. VIEWS. 37 CFR 1.84(h)

   REMINDER: Specification may require revision to correspond to drawing changes.

   Partial views. 37 CFR 1.84(h)(2)
   - ___ Brackets needed to show figure as one entity. Fig(s) _____
   - ___ Views not labeled separately or properly. Fig(s) _____
   - ___ Enlarged view not labeled separetely or properly. Fig(s) _____
7. SECTIONAL VIEWS. 37 CFR 1.84 (h)(3)
   - ___ Hatching not indicated for sectional portions of an object. Fig(s) _____
   - ___ Sectional designation should be noted with Arabic or Roman numbers. Fig(s) _____
8. ARRANGEMENT OF VIEWS. 37 CFR 1.84(i)
   - ___ Words do not appear on a horizontal, left-to-right fashion when page is either upright or turned so that the top becomes the right side, except for graphs. Fig(s) _____
9. SCALE. 37 CFR 1.84(k)
   - ___ Scale not large enough to show mechanism without crowding when drawing is reduced in size to two-thirds in reproduction. Fig(s) _____
10. CHARACTER OF LINES, NUMBERS, & LETTERS. 37 CFR 1.84(i)
    - ☒ ___ Lines, numbers & letters not uniformly thick and well defined, clean, durable, and black (poor line quality). Fig(s) 1-57
11. SHADING. 37 CFR 1.84(m)
    - ___ Solid black areas pale. Fig(s) _____
    - ___ Solid black shading not permitted. Fig(s) _____
    - ___ Shade lines, pale, rough and blurred. Fig(s) _____
12. NUMBERS, LETTERS, & REFERENCE CHARACTERS. 37 CFR 1.84(p)
    - ___ Numbers and reference characters not plain and legible. Fig(s) _____
    - ___ Figure legends are poor. Fig(s) _____
    - ___ Numbers and reference characters not oriented in the same direction as the view. 37 CFR 1.84(p)(1) Fig(s) _____
    - ___ English alphabet not used. 37 CFR 1.84(p)(2) Figs _____
    - ___ Numbers, letters and reference characters must be at least .32 cm (1/8 inch) in height. 37 CFR 1.84(p)(3) Fig(s) _____
13. LEAD LINES. 37 CFR 1.84(q)
    - Lead lines cross each other. Fig(s) _____
    - Lead lines missing. Fig(s) _____
14. NUMBERING OF SHEETS OF DRAWINGS. 37 CFR 1.84(t)
    - ___ Sheets not numbered consecutively, and in Arabic numerals beginning with number 1. Sheet(s) _____
15. NUMBERING OF VIEWS. 37 CFR 1.84(u)
    - ___ Views not numbered consecutively, and in Arabic numerals, beginning with number 1. Fig(s) _____
16. CORRECTIONS. 37 CFR 1.84(w)
    - ___ Corrections not made from prior PTO-948 dated _____
17. DESIGN DRAWINGS. 37 CFR 1.152
    - ___ Surface shading shown not appropriate. Fig(s) _____
    - ___ Solid black shading not used for color contrast. Fig(s) _____

COMMENTS

REVIEWER AD DATE 1/7/99 TELEPHONE NO. _____

ATTACHMENT TO PAPER NO. 7

GAU2782

OIPE JC135 JUL 19 2000 PATENT & TRADEMARK OFFICE

I hereby certify that this correspondence is being deposited with the United States Postal Service as first class mail in an envelope addressed to:

Assistant Commissioner for Patents
Washington, D.C. 20231

On July 14, 2000

TOWNSEND and TOWNSEND and CREW LLP

By: Deanna Coates

PATENT
Attorney Docket No.: 19152-000200US

RECEIVED
JUL 24 2000
TECH CENTER 2700

#8 /Revocation 7/05

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re application of:	Examiner: Unassigned
William W.Y. Chu	Art Unit: 2782
Application No.: 09/149,882	
Filed: September 8, 1998	
For: COMMUNICATION CHANNEL AND INTERFACE DEVICES FOR BRIDGING COMPUTER INTERFACE BUSES	TRANSMITTAL OF REVOCATION AND SUBSTITUTION OF POWER OF ATTORNEY UNDER 37 CFR §1.36

Assistant Commissioner for Patents
Washington, D.C. 20231

Sir:

Enclosed for filing in the above-identified application is an executed Revocation and Substitution of Power of Attorney Under 37 CFR §1.36 and accompanying Certificate Under 37 CFR §3.73(b) certifying that title is in the assignee.

Respectfully submitted,

Kent J. Tobin
Reg. No. 39,496

TOWNSEND and TOWNSEND and CREW LLP
Two Embarcadero Center, 8th Floor
San Francisco, California 94111-3834
Tel: 650-326-2400
Fax: 650-326-2422
KJT:dmc

PA 3083197 v1

OIPE JC13 JUL 19 2000 PATENT & TRADEMARK OFFICE

I hereby certify that this c... ...dence is being deposited with the United States Postal Service as first class mail in an envelope addressed to:

Assistant Commissioner for Patents
Washington, D.C. 20231

On July 14, 2000

TOWNSEND and TOWNSEND and CREW LLP

By: Deanna Coates

PATENT
Attorney Docket No.: 19152-000200US

RECEIVED
JUL 24 2000
TECH CENTER 2700

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re application of:	Examiner: Unassigned
William W.Y. Chu	Art Unit: 2782
Application No.: 09/149,882	
Filed: September 8, 1998	
For: COMMUNICATION CHANNEL AND INTERFACE DEVICES FOR BRIDGING COMPUTER INTERFACE BUSES	REVOCATION AND SUBSTITUTION OF POWER OF ATTORNEY UNDER 37 CFR §1.36

Assistant Commissioner for Patents
Washington, D.C. 20231

Sir:

Pursuant to 37 CFR § 1.36, Acqis Technology, Inc. revokes all previous powers of attorney and hereby appoints the following to prosecute this application and transact all business in the Patent and Trademark Office connected therewith:

Richart T. Ogawa, Reg. No. 37,692
Kent J. Tobin, Reg. No. 39,496
Stephen Y. Pang, Reg. No. 38,575

Please direct all future correspondence regarding the subject application to:

Richard T. Ogawa
TOWNSEND and TOWNSEND and CREW LLP
Two Embarcadero Center, 8th Floor
San Francisco, CA 94111-3834
Tel 650-326-2400
Fax 650-326-2422

Acqis Technology, Inc.

Date: 7/13/2000

By: William W.Y. Chu
William W.Y. Chu
President and CEO

PA 3082547 v1

OIPE JC
JUL 19 2000
PATENT & TRADEMARK OFFICE

Attorney Docket No. 19152-000200US

RECEIVED
JUL 24 2000
TECH CENTER 2700

CERTIFICATE UNDER 37 C.F.R. § 3.73(b)

Applicant: William W.Y. Chu

Application No.: 09/149,882 Filed: September 8, 1998

For: COMMUNICATION CHANNEL AND INTERFACE DEVICES FOR BRIDGING COMPUTER INTERFACE BUSES

Acqis Technology, Inc., a California corporation
(Name of Assignee) (Type of Assignee, e.g., corporation, partnership, university, government agency, etc.)

certifies that it is assignee of the patent application identified above by virtue of either:

A. ☒ An assignment from the inventor(s) of the patent application identified above. The assignment was recorded in the Patent and Trademark Office at Reel 9557, Frame(s) 0507-0508, or for which a copy thereof is attached.

OR

B. ☐ A chain of title from the inventor(s), of the patent application identified above, to the current assignee as shown below:

1. From: _____ To: _____
The document was recorded in the Patent and Trademark Office at
Reel _____, Frame _____, or for which a copy thereof is attached.

2. From: _____ To: _____
The document was recorded in the Patent and Trademark Office at
Reel _____, Frame _____, or for which a copy thereof is attached.

3. From: _____ To: _____
The document was recorded in the Patent and Trademark Office at
Reel _____, Frame _____, or for which a copy thereof is attached.

☐ Additional documents in the chain of title are listed on a supplemental sheet.

☐ Copies of assignments or other documents in the chain of title are attached.

The undersigned (whose title is supplied below) is empowered to act on behalf of the assignee.

I hereby declare that all statements made herein of my own knowledge are true, and that all statements made on information and belief are believed to be true; and further, that these statements are made with the knowledge that willful false statements, and the like so made, are punishable by fine or imprisonment, or both, under Section 1001, Title 18 of the United States Code, and that such willful false statements may jeopardize the validity of the application or any patent issuing thereon.

Date: 7/13/2000
Name: William W.Y. Chu
Title: President and CEO
Signature: William W. Y. Chu

rev. 4/99
PA 3082533 v1

OC0000000052686621

UNITED STATES DEPARTMENT OF COMMERCE
Patent and Trademark Office
Address: COMMISSIONER OF PATENT AND TRADEMARKS
Washington, D.C. 20231

APPLICATION NUMBER	FILING DATE	FIRST NAMED APPLICANT	ATTY. DOCKET NO./TITLE
09/149,882	09/08/1998	WILLIAM W. Y. CHU	387112000300

RICHARD T. OGAWA
TOWNSEND AND TOWNSEND AND CREW L.L.P
TWO EMBARCADERO CENTER
8 TH FLOOR
SAN FRANCISCO, CA 94111-3834

Date Mailed: 07/25/2000

NOTICE REGARDING POWER OF ATTORNEY

This is in response to the Power of Attorney filed 07/19/2000.

The Power of Attorney in this application is accepted. Correspondence in this application will be mailed to the above address as provided by 37 CFR 1.33.

Customer Service Center
Initial Patent Examination Division (703) 308-1202

OFFICE COPY

OC000000005268591

UNITED STATES DEPARTMENT OF COMMERCE
Patent and Trademark Office
Address: COMMISSIONER OF PATENT AND TRADEMARKS
Washington, D.C. 20231

APPLICATION NUMBER	FILING DATE	FIRST NAMED APPLICANT	ATTY. DOCKET NO./TITLE
09/149,882	09/08/1998	WILLIAM W. Y. CHU	387112000300

ARARAT KAPOUYTIAN
MORRISON AND FOERSTER
425 MARKET STREET
SAN FRANCISCO, CA 941052482

Date Mailed: 07/25/2000

NOTICE REGARDING POWER OF ATTORNEY

This is in response to the Power of Attorney filed 07/19/2000.

The Power of Attorney to you in this application has been revoked by the applicant. Future correspondence will be mailed to the new address of record(37 CFR 1.33).

Customer Service Center
Initial Patent Examination Division (703) 308-1202

OFFICE COPY

GP2722

Amendment

TOWNSEND and TOWNSEND and CREW LLP
Two Embarcadero Center, 8th Floor
San Francisco, California 94111-3834
(415) 576-0200

OIPE JC143 SEP 12 2000 PATENT & TRADEMARK OFFICE

Attorney Docket No. 19152-000200US

#9

In re application of: William W.Y. Chu

Application No.: 09/149,882

Filed: September 8, 1998

Group Art Unit: 2782

For: COMMUNICATION CHANNEL AND INTERFACE DEVICES FOR BRIDGING COMPUTER INTERFACE BUSES

Date: September 07, 2000

I hereby certify that this is being deposited with the United States Postal Service as first class mail in an envelope addressed to:

Assistant Commissioner for Patents
Washington, D.C. 20231

Signed: Ingrid J. Rogers

RECEIVED SEP 20 2000 2700 MAIL ROOM

THE ASSISTANT COMMISSIONER FOR PATENTS
Washington, D.C. 20231

Sir:

Transmitted herewith is an amendment in the above-identified application.

If any extension of time is needed, then this response should be considered a petition therefor.
The filing fee has been calculated as shown below:

	(Col. 1) CLAIMS REMAINING AFTER AMENDMENT		(Col. 2) HIGHEST NO. PREVIOUSLY PAID FOR	(Col. 3) PRESENT EXTRA
TOTAL	*	MINUS	**	=
INDEP.	*	MINUS	***	=
[ ] FIRST PRESENTATION OF MULTIPLE DEP. CLAIM				

SMALL ENTITY RATE	SMALL ENTITY ADDIT. FEE	OR	OTHER THAN SMALL ENTITY RATE	OTHER THAN SMALL ENTITY ADDIT. FEE
x =			x =	
x =			x =	
+ =			+ =	
TOTAL ADDIT. FEE		OR	TOTAL	$-0-

* If the entry in Col. 1 is less than the entry in Col. 2, write "0" in Col. 3.
** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 20, write "20" in this space.
*** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 3, then write "3" in this space. The "Highest Number Previously Paid For" (Total or Independent) is the highest number found from the equivalent box in Col. 1 of a prior amendment or the number of claims originally filed.

[X] No fee is due.

Please charge Deposit Account No. 20-1430 as follows:

[ ] Claims fee $_____
[X] Any additional fees associated with this paper or during the pendency of this application.

2 extra copies of this sheet are enclosed.

TOWNSEND and TOWNSEND and CREW LLP

Kent J. Tobin, Reg. No.: 39,496
Attorneys for Applicant

PA 3095099 v1

A

OIPE JC143 SEP 1 2 2000 PATENT & TRADEMARK OFFICE

I hereby certify that this correspondence is being deposited with the United States Postal Service as first class mail in an envelope addressed to:

Assistant Commissioner for Patents
Washington, D.C. 20231

On 9-7-00

TOWNSEND and TOWNSEND and CREW LLP

By: Ingrid J. Rogus

PATENT
Attorney Docket No.: 19152-000200US

#9
Amdt A
9/21/00
mail

RECEIVED
SEP 20 2000
TC 2700 MAIL ROOM

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re application of:	Examiner: C. Cao
William W.Y. Chu	Art Unit: 2782
Application No.: 09/149,882	Amendment in Response to Office Action Mailed June 15, 2000
Filed: September 8, 1998	
For: COMMUNICATION CHANNEL AND INTERFACE DEVICES FOR BRIDGING COMPUTER INTERFACE BUSES	

Assistant Commissioner for Patents
Washington, D.C. 20231

Sir:

In response to the Office Action mailed June 15, 2000, please amend the above-identified application as follows:

IN THE CLAIMS:

Please add new claims 43-60 as follows:

--43. (New) A modular computer system comprising:

a peripheral console including a power supply and a peripheral component interface;

a computer module including a central processing unit and a main memory;

a power bus between the computer module and the peripheral console, the power bus configured such that the central processing unit receives power only when the computer module is attached to the peripheral console; and

a differential signal channel between the computer module and the peripheral console, the differential signal channel configured to communicate a differential data signal pair between the computer module and the peripheral console.

44. (New) The modular computer system of claim 43 wherein:

the computer module further comprises a graphics controller; and

the peripheral console is configured to receive video capture data from a video source and to communicate the video capture data to the graphics controller.

45. (New) The modular computer system of claim 43 wherein:

the computer module further comprises a graphics controller; and

the computer module is configured to communicate a video display signal from the graphics controller to a display coupled with the peripheral console.

46. (New) The modular computer system of claim 45 further comprising a video bus configured to communicate the video display signal from the computer module to the peripheral console.

47. (New) The modular computer system of claim 46 wherein the video display signal comprises an RGB video signal.

48. (New) The modular computer system of claim 46 wherein the video display signal comprises a digital video signal.

49. (New) The modular computer system of claim 46 wherein the digital video display signal comprises a transition minimized differential signaling (TMDS) signal.

50. (New) The modular computer system of claim 46 wherein the video display signal comprises a television (TV) signal.

6 4
~~51~~. (New) The modular computer system of claim ~~46~~ wherein the video bus is configured to communicate the video capture signal to the graphics controller.

7 1
~~52~~. (New) The modular computer system of claim ~~43~~ wherein the power bus is configured to communicate a power of 3.3V to the computer module.

8 1
~~53~~. (New) The modular computer system of claim ~~43~~ wherein the power bus is configured to communicate a power of 5V to the computer module.

9 1
~~54~~. (New) The modular computer system of claim ~~43~~ wherein the differential signal channel comprises at least two pairs of differential signal lines.

10 9
~~55~~. (New) The modular computer system of claim ~~54~~ wherein a first pair of differential signal lines is configured to communicate a clock signal and a second pair of differential signal lines is configured to communicate a data signal.

11 10
~~56~~. (New) The modular computer system of claim ~~55~~ wherein the first pair of differential signals is configured to communicate the clock signal at a minimum clock speed of 50Mhz.

12 9
~~57~~. (New) The modular computer system of claim ~~54~~ wherein the differential communication channel comprises an LVDS channel.

13 12
~~58~~. (New) The modular computer system of claim ~~57~~ wherein the differential communication channel comprises IEEE 1394 lines.

14 1
~~59~~. (New) The modular computer system of claim ~~43~~ wherein the computer module further comprises a first PCI bus in electrical communication with the differential signal channel through a first interface controller.

15 14
~~60~~. (New) The modular computer system of claim ~~59~~ wherein the peripheral component interface of the peripheral console comprises a second PCI bus in electrical communication

A1 Cont

38

A

with the differential signal channel through a second interface controller, the first interface controller and the second interface controller operating in conjunction to bridge the first PCI bus to the second PCI bus.--

IN THE DRAWINGS:

Please amend Figures 1 and 2 as shown in red in the amended informal drawing submitted herewith.

REMARKS

Claims 43-60 are pending. Claims 1-42 have been canceled.

Previous claims 1-42 have been canceled and replaced with new claims relating to a modular computer system wherein data is exchanged across a differential communication channel between a computer module housing a CPU and memory, and a peripheral console housing a power supply and interfaces to display and input devices. In one embodiment, the computer module further includes a graphics controller, with video capture data communicated across the differential communication from the peripheral console. Support for the new claims is found in general in the specification in Figures 2, 6, and 11, and associated text at pages 9, 11-12, and 18.

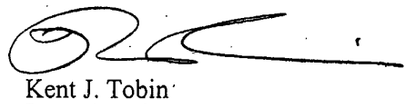
Figure 1 has been amended to include the "Prior Art" legend as requested by the Examiner. Figure 2 has also been amended to indicate the two-way communication of data across video bus 217 of Figure 2. Support for this drawing change is found in Figure 11, which shows the video signals VPD and VPCK being communicated to the computer module from the peripheral console.

CONCLUSION

In view of the foregoing amendments and remarks, Applicant believes all claims now pending in this Application are in condition for allowance. The issuance of a formal Notice of Allowance at an early date is respectfully requested.

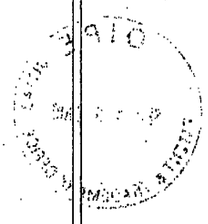
If the Examiner believes a telephone conference would expedite prosecution of this application, please telephone the undersigned at 650-326-2400.

Respectfully submitted,



Kent J. Tobin
Reg. No. 39,496

TOWNSEND and TOWNSEND and CREW LLP
Two Embarcadero Center, 8th Floor
San Francisco, California 94111-3834
Tel: (415) 576-0200
Fax: (415) 576-0300
KJT
PA 3091764 v1



A

BEST COPY

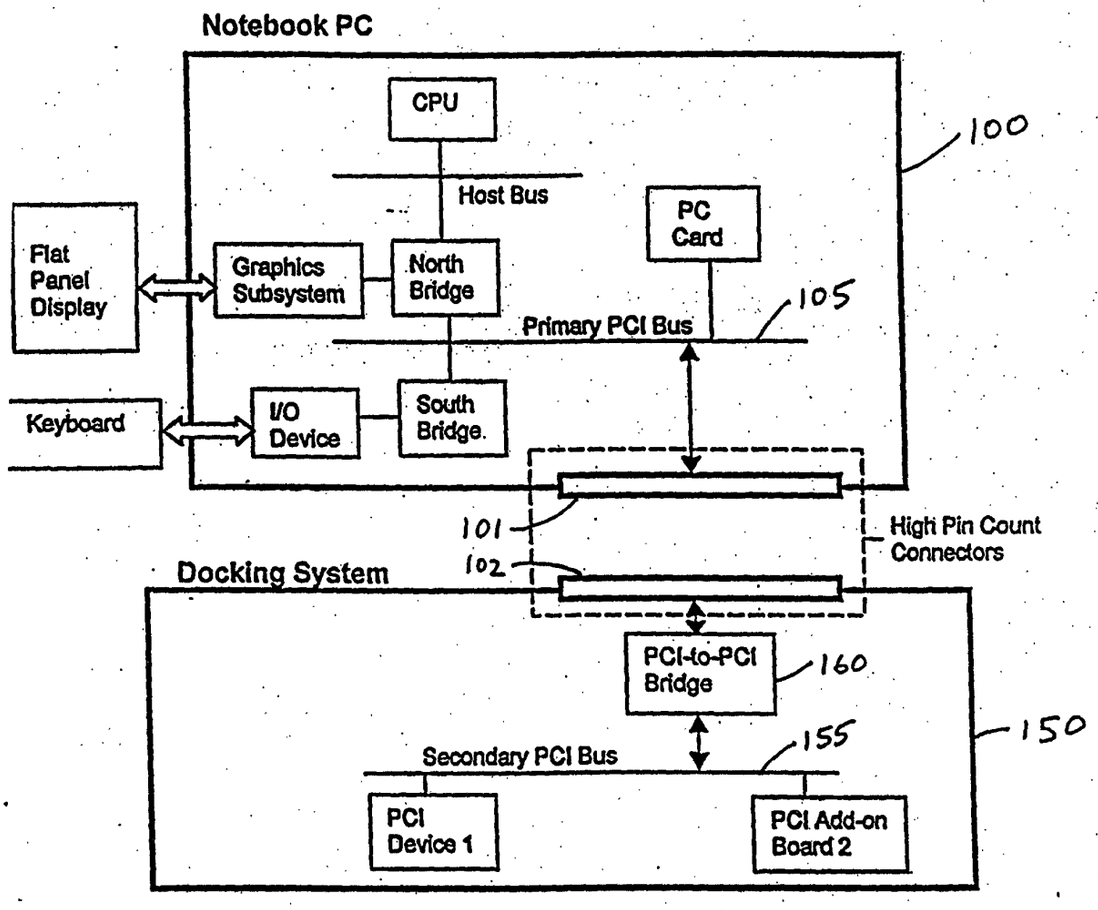


FIGURE 1
(Prior Art)

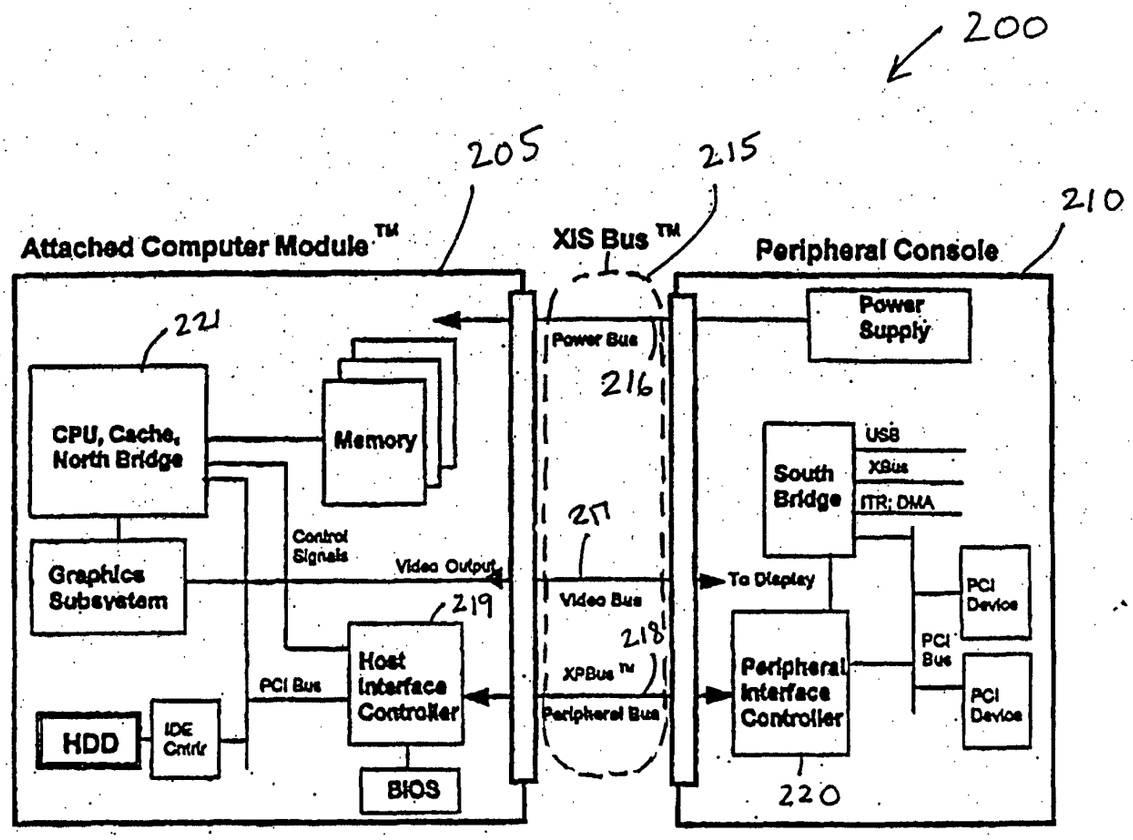

200
205
215
210
Attached Computer Module™
XIS Bus™
Peripheral Console
221
CPU, Cache, North Bridge
Memory
Graphics Subsystem
Control Signals
Video Output
219
Host Interface Controller
PCI Bus
HDD
IDE Cntrlr
BIOS
Power Bus
216
217
Video Bus
218
XPBus™
Peripheral Bus
Power Supply
South Bridge
USB
XBus
ITR; DMA
To Display
PCI Device
PCI Bus
PCI Device
Peripheral Interface Controller
220

FIGURE 2

Transaction History Date 2000-09-25
Date information retrieved from USPTO Patent Application Information Retrieval (PAIR) system records at www.uspto.gov

BEST COPY

I hereby certify that this correspondence is being deposited with the United States Postal Service as first class mail in an envelope addressed to:

Assistant Commissioner for Patents
Washington, D.C. 20231

On 9-22-00

TOWNSEND and TOWNSEND and CREW LLP

By: Ingrid S. Rogers

OIPE
SEP 25 2000
TRADEMARK

PATENT
Attorney Docket No.: 19152-000200US

RECEIVED
SEP 28 2000
TECH CENTER 2700

#10

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re application of:

William W.Y. Chu

Application No.: 09/149,882

Filed: September 8, 1998

For: COMMUNICATION CHANNEL AND INTERFACE DEVICES FOR BRIDGING COMPUTER INTERFACE BUSES

Examiner: C. Cao

Art Unit: 2782

SUPPLEMENTAL INFORMATION DISCLOSURE STATEMENT UNDER 37 CFR §1.97 and §1.98

Assistant Commissioner for Patents
Washington, D.C. 20231

Sir:

The references cited on attached form PTO-1449 are being called to the attention of the Examiner. Copies of the references are enclosed. It is respectfully requested that the cited references be expressly considered during the prosecution of this application, and the references be made of record therein and appear among the "references cited" on any patent to issue therefrom.

As provided for by 37 CFR 1.97(g) and (h), no inference should be made that the information and references cited are prior art merely because they are in this statement and

09/27/2000 WKNGUYEN 00000106 201430 09149882
01 FC:1806 240.00 CH

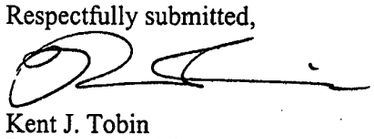
no representation is being made that a search has been conducted or that this statement encompasses all the possible relevant information.

This IDS is being filed after the mailing date of the first Office Action and more than three months after the filing date, but prior to the Notice of Allowance or Final Office Action.

Please deduct $240.00, pursuant to 37 CFR §1.17(p), from the undersigned's Deposit Account No. 20-1430. Please deduct any additional fees from, or credit any overpayment to, the above-noted Deposit Account.

This Petition is submitted in triplicate.

Respectfully submitted,



Kent J. Tobin
Reg. No. 39,496

TOWNSEND and TOWNSEND and CREW LLP
Two Embarcadero Center, 8th Floor
San Francisco, California 94111-3834
Tel: 650-326-2400
Fax: 650-326-2422
KJT:isr

PA 3098235 v1

PTO SEP 25 2000 PATENT & TRADEMARK OFFICE

FORM PTO-1449 (Modified) LIST OF PATENTS AND PUBLICATIONS FOR APPLICANT'S INFORMATION DISCLOSURE STATEMENT (Use several sheets if necessary)	Attorney Docket No.: 19152-000200US	Application No.: 09/149,882
	Applicant: William W.Y. Chu	
	Filing Date: September 8, 1998	Group: 2782

Reference Designation — **U.S. PATENT DOCUMENTS** — Page 1

Examiner Initial	Document No.	Date	Name	Class	Sub-class	Filing Date (If Appropriate)
C 0001	4,890,282	12/26/89	Lambert et al.	370	79	
C 0002	5,463,742	10/31/95	Kobayashi	395	281	
C 0003	5,550,710	08/27/96	Rahamim et al.	361	687	
C 0004	5,721,837	02/24/98	Kikinis et al.	395	281	
C 0005	5,819,050	10/06/98	Boehling et al.	395	284	
0006						
0007						
0008						
0009						
0010						
0011						
0012						

RECEIVED SEP 29 2000 TECH CENTER 2700

FOREIGN PATENT DOCUMENTS

	Document No.	Date	Country	Class	Sub-class	Translation (Yes/No)
0013						
0014						
0015						
0016						
0017						
0018						

OTHER ART (Including Author, Title, Date, Pertinent Pages, Etc.)

0019	
0020	
0021	
0022	
0023	

EXAMINER CAO DATE CONSIDERED 12/11/00

EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609; Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.

2182 2782

PATENT

Attorney Docket No.: 19152-000200US

#12 gw 1-5-01

I hereby certify that this correspondence is being deposited with the United States Postal Service as first class mail in an envelope addressed to:

Assistant Commissioner for Patents
Washington, D.C. 20231

On 10-10-00

TOWNSEND and TOWNSEND and CREW LLP

By: Ingrid S. Rogue

OIPE
OCT 16 2000
PATENT & TRADEMARK OFFICE
JC56

RECEIVED
OCT 20 2000
TECH CENTER 2700

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re application of:

William W.Y. Chu

Application No.: 09/149,882

Filed: September 8, 1998

For: COMMUNICATION CHANNEL AND INTERFACE DEVICES FOR BRIDGING COMPUTER INTERFACE BUSES

Examiner: C. Cao

Art Unit: 2782

SUPPLEMENTAL INFORMATION DISCLOSURE STATEMENT UNDER 37 CFR §1.97 and §1.98

Assistant Commissioner for Patents
Washington, D.C. 20231

Sir:

The references cited on attached form PTO-1449 are being called to the attention of the Examiner. Copies of the references are enclosed. It is respectfully requested that the cited references be expressly considered during the prosecution of this application, and the references be made of record therein and appear among the "references cited" on any patent to issue therefrom.

As provided for by 37 CFR 1.97(g) and (h), no inference should be made that the information and references cited are prior art merely because they are in this statement and

10/10/2000 MBERHE 00000057 201430 09149882
01 FC:126 240.00 CH

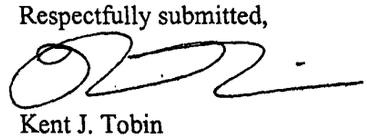
no representation is being made that a search has been conducted or that this statement encompasses all the possible relevant information.

This IDS is being filed after the mailing date of the first Office Action and more than three months after the filing date, but prior to the Notice of Allowance or Final Office Action.

Please deduct $240.00, pursuant to 37 CFR §1.17(p), from the undersigned's Deposit Account No. 20-1430. Please deduct any additional fees from, or credit any overpayment to, the above-noted Deposit Account.

This Petition is submitted in triplicate.

Respectfully submitted,



Kent J. Tobin
Reg. No. 39,496

TOWNSEND and TOWNSEND and CREW LLP
Two Embarcadero Center, 8th Floor
San Francisco, California 94111-3834
Tel: 650-326-2400
Fax: 650-326-2422
KJT:isr

PA 3101959 v1

I hereby certify that this correspondence is being deposited with the United States Postal Service as first class mail in an envelope addressed to:

Assistant Commissioner for Patents
Washington, D.C. 20231

On 10-10-00

TOWNSEND and TOWNSEND and CREW LLP

By: Ingrid T. Rogus

PATENT
Attorney Docket No.: 19152-000200US



IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re application of:

William W.Y. Chu

Application No.: 09/149,882

Filed: September 8, 1998

For: COMMUNICATION CHANNEL AND INTERFACE DEVICES FOR BRIDGING COMPUTER INTERFACE BUSES

Examiner: C. Cao

Art Unit: 2782

SUPPLEMENTAL INFORMATION DISCLOSURE STATEMENT UNDER 37 CFR §1.97 and §1.98

RECEIVED
OCT 20 2000
TECH CENTER 2700

Assistant Commissioner for Patents
Washington, D.C. 20231

Sir:

The references cited on attached form PTO-1449 are being called to the attention of the Examiner. Copies of the references are enclosed. It is respectfully requested that the cited references be expressly considered during the prosecution of this application, and the references be made of record therein and appear among the "references cited" on any patent to issue therefrom.

As provided for by 37 CFR 1.97(g) and (h), no inference should be made that the information and references cited are prior art merely because they are in this statement and

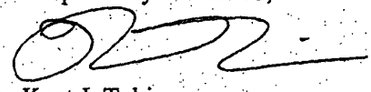
no representation is being made that a search has been conducted or that this statement encompasses all the possible relevant information.

This IDS is being filed after the mailing date of the first Office Action and more than three months after the filing date, but prior to the Notice of Allowance or Final Office Action.

Please deduct $240.00, pursuant to 37 CFR §1.17(p), from the undersigned's Deposit Account No. 20-1430. Please deduct any additional fees from, or credit any overpayment to, the above-noted Deposit Account.

This Petition is submitted in triplicate.

Respectfully submitted,



Kent J. Tobin
Reg. No. 39,496

TOWNSEND and TOWNSEND and CREW LLP
Two Embarcadero Center, 8th Floor
San Francisco, California 94111-3834
Tel: 650-326-2400
Fax: 650-326-2422
KJT:isr

PA 3101959 v1

FORM PTO-1449 (Modified) LIST OF PATENTS AND PUBLICATIONS FOR APPLICANT'S INFORMATION DISCLOSURE STATEMENT (Use several sheets if necessary)	Attorney Docket No.: 19152-000200US Applicant: William W.Y. Chu Filing Date: September 8, 1998	Application No.: 09/149,882 Group: 2782

Reference Designation — **U.S. PATENT DOCUMENTS** — Page 1

Examiner Initial	Document No.	Date	Name	Class	Sub-class	Filing Date (If Appropriate)
C 1	5,948,047	09/07/99	Jenkins et al.	708	141	
C 2	5,999,952	12/07/99	Jenkins et al.	708	100	
C 3	6,029,183	02/22/00	Jenkins et al.	708	100	
4						
5						
6						
7						
8						
9						
10						
11						
12						

RECEIVED
OCT 20 2000
TECH CENTER 2700

OIPE
OCT 16 2000
PATENT & TRADEMARK OFFICE

FOREIGN PATENT DOCUMENTS

	Document No.	Date	Country	Class	Sub-class	Translation (Yes/No)
13						
14						
15						
16						
17						
18						

OTHER ART (Including Author, Title, Date, Pertinent Pages, Etc.)

19	
20	
21	
22	
23	

EXAMINER CAD DATE CONSIDERED 3-14-01

EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609; Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.

Transaction History Date 2000-12-19
Date information retrieved from USPTO Patent Application Information Retrieval (PAIR) system records at www.uspto.gov

BEST COPY

UNITED STATES DEPARTMENT OF COMMERCE
Patent and Trademark Office
Address: COMMISSIONER OF PATENTS AND TRADEMARKS
Washington, D.C. 20231

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.
09/149,882	09/08/98	CHU	W 38711200030C

EXAMINER	
CAO,C	
ART UNIT	**PAPER NUMBER**
2182	11

DATE MAILED: 12/19/00

TM02/1219
RICHARD T. OGAWA
TOWNSEND AND TOWNSEND AND CREW L.L.P
TWO EMBARCADERO CENTER
8 TH FLOOR
SAN FRANCISCO CA 94111-3834

Please find below and/or attached an Office communication concerning this application or proceeding.

Commissioner of Patents and Trademarks

PTO-90C (Rev. 2/95) 1- File Copy
*U.S. GPO: 2000-473-000/44602

Office Action Summary

Application No.	Applicant(s)
09/149,882	Chu
Examiner	**Group Art Unit**
Chun Cao	2182

☒ Responsive to communication(s) filed on *Sep 12, 2000*.

☐ This action is **FINAL.**

☐ Since this application is in condition for allowance except for formal matters, **prosecution as to the merits is closed** in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11; 453 O.G. 213.

A shortened statutory period for response to this action is set to expire *1* month(s), or thirty days, whichever is longer, from the mailing date of this communication. Failure to respond within the period for response will cause the application to become abandoned. (35 U.S.C. § 133). Extensions of time may be obtained under the provisions of 37 CFR 1.136(a).

Disposition of Claims

☒ Claim(s) *43-60* is/are pending in the application.

Of the above, claim(s) *43-60* is/are withdrawn from consideration.

☐ Claim(s) _____ is/are allowed.

☐ Claim(s) _____ is/are rejected.

☐ Claim(s) _____ is/are objected to.

☐ Claims _____ are subject to restriction or election requirement.

Application Papers

☐ See the attached Notice of Draftsperson's Patent Drawing Review, PTO-948.

☐ The drawing(s) filed on _____ is/are objected to by the Examiner.

☐ The proposed drawing correction, filed on _____ is ☐ approved ☐ disapproved.

☐ The specification is objected to by the Examiner.

☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. § 119

☐ Acknowledgement is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d).

☐ All ☐ Some* ☐ None of the CERTIFIED copies of the priority documents have been

☐ received.

☐ received in Application No. (Series Code/Serial Number) _____.

☐ received in this national stage application from the International Bureau (PCT Rule 17.2(a)).

*Certified copies not received: _____.

☐ Acknowledgement is made of a claim for domestic priority under 35 U.S.C. § 119(e).

Attachment(s)

☐ Notice of References Cited, PTO-892

☒ Information Disclosure Statement(s), PTO-1449, Paper No(s). *10*

☐ Interview Summary, PTO-413

☐ Notice of Draftsperson's Patent Drawing Review, PTO-948

☐ Notice of Informal Patent Application, PTO-152

--- SEE OFFICE ACTION ON THE FOLLOWING PAGES ---

DETAILED ACTION

1. Claims 43-60 are presented for examination.

Election/Restriction

2. Newly submitted claims 43-60 directed to an invention that is independent or distinct from the invention originally claimed for the following reasons:

Original claims, drawn to: a first interface controller encodes control signals into control bits; and a second interface controller decodes control bits into control signals, classified in class 710, subclass 69.

Claims 43-60, drawn to: a modular computer system wherin data is exchanged across a differential communication channel between a computer module housing, classified in class 710, subclass 33.

a. These inventions have acquired a separate status in the art as shown by their different classification;

b. The search required for one Group is not required for the other Groups for the reasons above restriction for examination purpose as indicated is proper.

Since applicant has received an action on the merits for the originally presented invention, this invention has been constructively elected by original presentation for prosecution on the merits. Accordingly, claims 43-60 are withdrawn from consideration as being directed to a non-elected invention. See 37 CFR 1.142(b) and MPEP § 821.03.

Conclusion

3. A shortened statutory period for response to this action is set to expire **ONE** month, or **30** days, whichever is longer, from the mailing date of this communication. Failure to respond within the period for response will cause the application to become abandoned. (35 U.S.C. § 133).

Any response to this action should be mailed to:

Commissioner of Patents and Trademarks

Washington, D.C. 20231

or faxed to:

(703) 308-9051, (for formal communications intended for entry)

Or:

(703) 306-5404 (for informal or draft communications, please label "PROPOSED" or "DRAFT")

Hand-delivered responses should be brought to Crystal Park II, 2121 Crystal Drive, Arlington. VA., Sixth Floor (Receptionist).

4. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Chun Cao at (703)308-6106. The examiner can normally be reached on Monday-Friday from 7:30 am - 4:00 pm. If attempts to reach the examiner by phone are

unsuccessful, the examiner's supervisor Thomas Lee can be reached at (703)305-9717. The fax number for this Art Unit is (703) 306-5404.

Any inquiry of a general nature or relating to the status of this application should be directed to the Group receptionist whose telephone number is (703)305-9600.

Chun Cao

Dec. 11, 2000

THOMAS LEE
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2100

01-19-01

CPA $ 2782

CONTINUED PR[illegible] [illegible]CUTION APPLICATION (CPA) REQUEST [illegible]NSMITTAL

Customer No. 20350
TOWNSEND and TOWNSEND and CREW LLP
Two Embarcadero Center, 8th Floor
San Francisco, California 94111-3834
(415) 576-0200

Attorney Docket No. 19152-000200US

#13 Paid 1-26-01

OIPE JC106 JAN 17 2001 PATENT & TRADEMARK OFFICE

ASSISTANT COMMISSIONER FOR PATENTS
BOX CPA
Washington, D.C. 20231

"Express Mail" Label No. EL524033364US
Date of Deposit: 1-17-01

I hereby certify that this is being deposited with the United States Postal Service "Express Mail Post Office to Addressee" service under 37 CFR 1.10 on the date indicated above, addressed to:

Assistant Commissioner for Patents
Box CPA
Washington, D.C. 20231

By: [signature]

RECEIVED JAN 25 2001 Technology Center 2100

Sir:

This is a request under 37 CFR 1.53 (d) for filing a **CPA** of application

No. 09/149,882, filed September 8, 1998, of William W.Y. Chu
for COMMUNICATION CHANNEL AND INTERFACE DEVICES FOR BRIDGING COMPUTER INTERFACE BUSES

Applicant understands that this CPA application automatically ABANDONS the parent application.

[X] An assignment to Acqis Technology, Inc. was filed in the parent application.
[X] Please enter the enclosed preliminary amendment.
[X] Please cancel claim(s) 1-42
[X] Two Sheets Revised informal drawings marked in red.

Claims after Entry of any Amendments, Less any Cancelled Claims

	(Col. 1)	(Col. 2)	SMALL ENTITY			OTHER THAN SMALL ENTITY	
FOR:	NO. FILED	NO. EXTRA	RATE	FEE	OR	RATE	FEE
BASIC FEE				$355.00	OR		$710.00
TOTAL CLAIMS	18 - 20	= *0	x $9.00 =	$0.00	OR	x $18.00 =	
INDEP. CLAIMS	1 - 3	= *0	x $40.00 =	$0.00	OR	x $80.00 =	
[ ] MULTIPLE DEPENDENT CLAIM PRESENTED			+ $135.00 =		OR	+ $270.00 =	
			TOTAL	$355.00	OR	TOTAL	

* If the difference in Col. 1 is less than zero, enter "0" in Col. 2.

Please charge Deposit Account No. 20-1430 as follows:

[X] Filing fee $355.00
[X] Any additional fees associated with this paper or during the pendency of this application.
[ ] The issue fee set in 37 CFR 1.18 at or before mailing of the Notice of Allowance, pursuant to 37 CFR 1.311(b)

[ ] A check for $_____ is enclosed.
2 extra copies of this sheet are enclosed.

01/24/2001 WKORONA 00000009 201430 09149882

01 FC:231 355.00 CH

Respectfully submitted,

TOWNSEND and TOWNSEND and CREW LLP

[signature]

Telephone: (415) 576-0200
Facsimile: (415) 576-0300

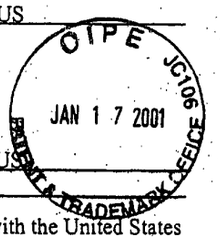
Kent J. Tobin
Reg No.: 39,496
Attorneys for Applicant

PA 3121533 v1

CONTINUED PR[illegible]CUTION APPLICATION (CPA) REQUES[illegible] ANSMITTAL

Customer No. 20350
TOWNSEND and TOWNSEND and CREW LLP
Two Embarcadero Center, 8th Floor
San Francisco, California 94111-3834
(415) 576-0200

Attorney Docket No. 19152-000200US



ASSISTANT COMMISSIONER FOR PATENTS
BOX CPA
Washington, D.C. 20231

"Express Mail" Label No. EL524033364US
Date of Deposit: 1-17-01

I hereby certify that this is being deposited with the United States Postal Service "Express Mail Post Office to Addressee" service under 37 CFR 1.10 on the date indicated above, addressed to:

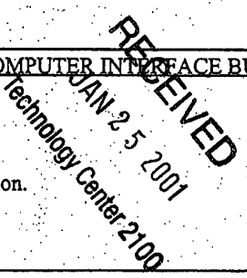
Assistant Commissioner for Patents
Box CPA
Washington, D.C. 20231

By: Anna Caplell

Sir:

This is a request under 37 CFR 1.53 (d) for filing a CPA of application

No. 09/149,882, filed September 8, 1998, of William W.Y. Chu
for COMMUNICATION CHANNEL AND INTERFACE DEVICES FOR BRIDGING COMPUTER INTERFACE BUSES



Applicant understands that this CPA application automatically ABANDONS the parent application.
[X] An assignment to Acqis Technology, Inc. was filed in the parent application.
[X] Please enter the enclosed preliminary amendment.
[X] Please cancel claim(s) 1-42
[X] Two Sheets Revised informal drawings marked in red.

Claims after Entry of any Amendments, Less any Cancelled Claims

FOR:	(Col. 1) NO. FILED		(Col. 2) NO. EXTRA		SMALL ENTITY RATE	SMALL ENTITY FEE		OTHER THAN SMALL ENTITY RATE	OTHER THAN SMALL ENTITY FEE
BASIC FEE						$355.00	OR		$710.00
TOTAL CLAIMS	18	- 20	=	*0	x $9.00 =	$0.00	OR	x $18.00 =	
INDEP. CLAIMS	1	- 3	=	*0	x $40.00 =	$0.00	OR	x $80.00 =	
[ ] MULTIPLE DEPENDENT CLAIM PRESENTED					+ $135.00 =		OR	+ $270.00 =	
					TOTAL	$355.00	OR	TOTAL	

* If the difference in Col. 1 is less than zero, enter "0" in Col. 2.

Please charge Deposit Account No. 20-1430 as follows:

[X] Filing fee $ $355.00
[X] Any additional fees associated with this paper or during the pendency of this application.
[ ] The issue fee set in 37 CFR 1.18 at or before mailing of the Notice of Allowance, pursuant to 37 CFR 1.311(b)

[ ] A check for $_____ is enclosed.
2 extra copies of this sheet are enclosed.

Respectfully submitted,
TOWNSEND and TOWNSEND and CREW LLP

Kent J. Tobin
Reg No.: 39,496
Attorneys for Applicant

Telephone: (415) 576-0200
Facsimile: (415) 576-0300

PA 3121533 v1

I hereby certify that this correspo... ...ace is being deposited with the United States Postal Service as first class mail in an envelope addressed to:

Assistant Commissioner for Patents
Washington, D.C. 20231

On 1-17-01

TOWNSEND and TOWNSEND and CREW LLP

By: Richard T. Rogers

PATENT
Attorney Docket No.: 19152-000200US



IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re application of:

William W.Y. Chu

Application No.: 09/149,882

Filed: September 8, 1998

For: COMMUNICATION CHANNEL AND INTERFACE DEVICES FOR BRIDGING COMPUTER INTERFACE BUSES

Examiner: C. Cao

Art Unit: 2782

Preliminary Amendment

RECEIVED
JAN 25
Technology Center 2100

RECEIVED
JAN 25 2001
Technology Center 2100

Assistant Commissioner for Patents
Washington, D.C. 20231

Sir:

This preliminary amendment accompanies a continued prosecution application (CPA) for the above-referenced application. Please preliminarily amend the above-identified CPA application as follows:

Don't enter same as paper No. 9 w 3-14-01

IN THE DRAWINGS:

Please amend Figures 1 and 2 as shown in red in the amended informal drawing submitted herewith.

IN THE CLAIMS:

Please cancel claims 1-42.

Please add new claims 43-60 as follows:

--43. (New) A modular computer system comprising:

a peripheral console including a power supply and a peripheral component interface;

a computer module including a central processing unit and a main memory;

a power bus between the computer module and the peripheral console, the power bus configured such that the central processing unit receives power only when the computer module is attached to the peripheral console; and

a differential signal channel between the computer module and the peripheral console, the differential signal channel configured to communicate a differential data signal pair between the computer module and the peripheral console.

44. (New) The modular computer system of claim 43 wherein:

the computer module further comprises a graphics controller; and

the peripheral console is configured to receive video capture data from a video source and to communicate the video capture data to the graphics controller.

45. (New) The modular computer system of claim 43 wherein:

the computer module further comprises a graphics controller; and

the computer module is configured to communicate a video display signal from the graphics controller to a display coupled with the peripheral console.

46. (New) The modular computer system of claim 45 further comprising a video bus configured to communicate the video display signal from the computer module to the peripheral console.

47. (New) The modular computer system of claim 46 wherein the video display signal comprises an RGB video signal.

48. (New) The modular computer system of claim 46 wherein the video display signal comprises a digital video signal.

49. (New) The modular computer system of claim 46 wherein the digital video display signal comprises a transition minimized differential signaling (TMDS) signal.

50. (New) The modular computer system of claim 46 wherein the video display signal comprises a television (TV) signal.

51. (New) The modular computer system of claim 46 wherein the video bus is configured to communicate the video capture signal to the graphics controller.

52. (New) The modular computer system of claim 43 wherein the power bus is configured to communicate a power of 3.3V to the computer module.

53. (New) The modular computer system of claim 43 wherein the power bus is configured to communicate a power of 5V to the computer module.

54. (New) The modular computer system of claim 43 wherein the differential signal channel comprises at least two pairs of differential signal lines.

55. (New) The modular computer system of claim 54 wherein a first pair of differential signal lines is configured to communicate a clock signal and a second pair of differential signal lines is configured to communicate a data signal.

56. (New) The modular computer system of claim 55 wherein the first pair of differential signals is configured to communicate the clock signal at a minimum clock speed of 50Mhz.

57. (New) The modular computer system of claim 54 wherein the differential communication channel comprises an LVDS channel.

58. (New) The modular computer system of claim 57 wherein the differential communication channel comprises IEEE 1394 lines.

59. (New) The modular computer system of claim 43 wherein the computer module further comprises a first PCI bus in electrical communication with the differential signal channel through a first interface controller.

60. (New) The modular computer system of claim 59 wherein the peripheral component interface of the peripheral console comprises a second PCI bus in electrical communication with the differential signal channel through a second interface controller, the first interface controller and the second interface controller operating in conjunction to bridge the first PCI bus to the second PCI bus.--

REMARKS

Claims 43-60 are pending. Claims 1-42 have been canceled.

In response to the office action mailed December 19, 2000, Applicant has filed a continued prosecution application (CPA) in order that newly presented claims 43-60 may be examined. Previously pending claims 1-42 are canceled and replaced with new claims relating to a modular computer system wherein data is exchanged across a differential communication channel between a computer module housing a CPU and memory, and a peripheral console housing a power supply and interfaces to display and input devices. In one embodiment, the computer module further includes a graphics controller, with video capture data communicated across the differential communication from the peripheral console. Support for the new claims is found in general in the specification in Figures 2, 6, and 11, and associated text at pages 9, 11-12, and 18.

In the drawings, as requested by the Examiner Figure 1 has been amended to include the "Prior Art" legend. Figure 2 has been amended to indicate the two-way communication of data across video bus 217 of Figure 2. Support for this drawing change to Figure 2 is found in Figure 11, which shows the video signals VPD and VPCK being communicated to the computer module from the peripheral console.

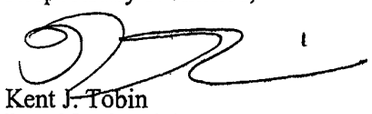
OIPE JC106
JAN 17 2001
PATENT & TRADEMARK OFFICE

CONCLUSION

In view of the foregoing amendments and remarks, Applicant believes all claims now pending in this Application are in condition for allowance. The issuance of a formal Notice of Allowance at an early date is respectfully requested.

If the Examiner believes a telephone conference would expedite prosecution of this application, please telephone the undersigned at 650-326-2400.

Respectfully submitted,



Kent J. Tobin
Reg. No. 39,496

TOWNSEND and TOWNSEND and CREW LLP
Two Embarcadero Center, 8th Floor
San Francisco, California 94111-3834
Tel: (415) 576-0200
Fax: (415) 576-0300
KJT
PA 3118614 v1

BEST COPY

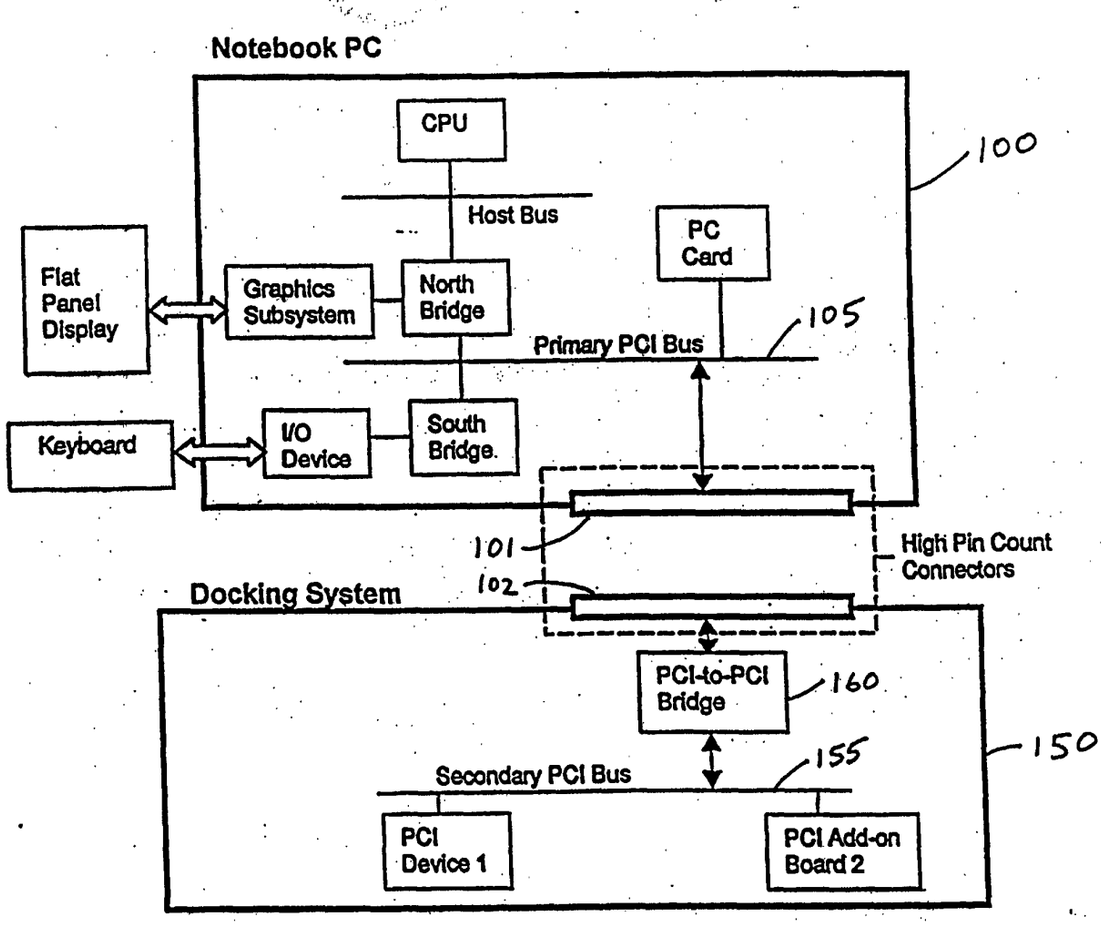


FIGURE 1
(Prior Art)

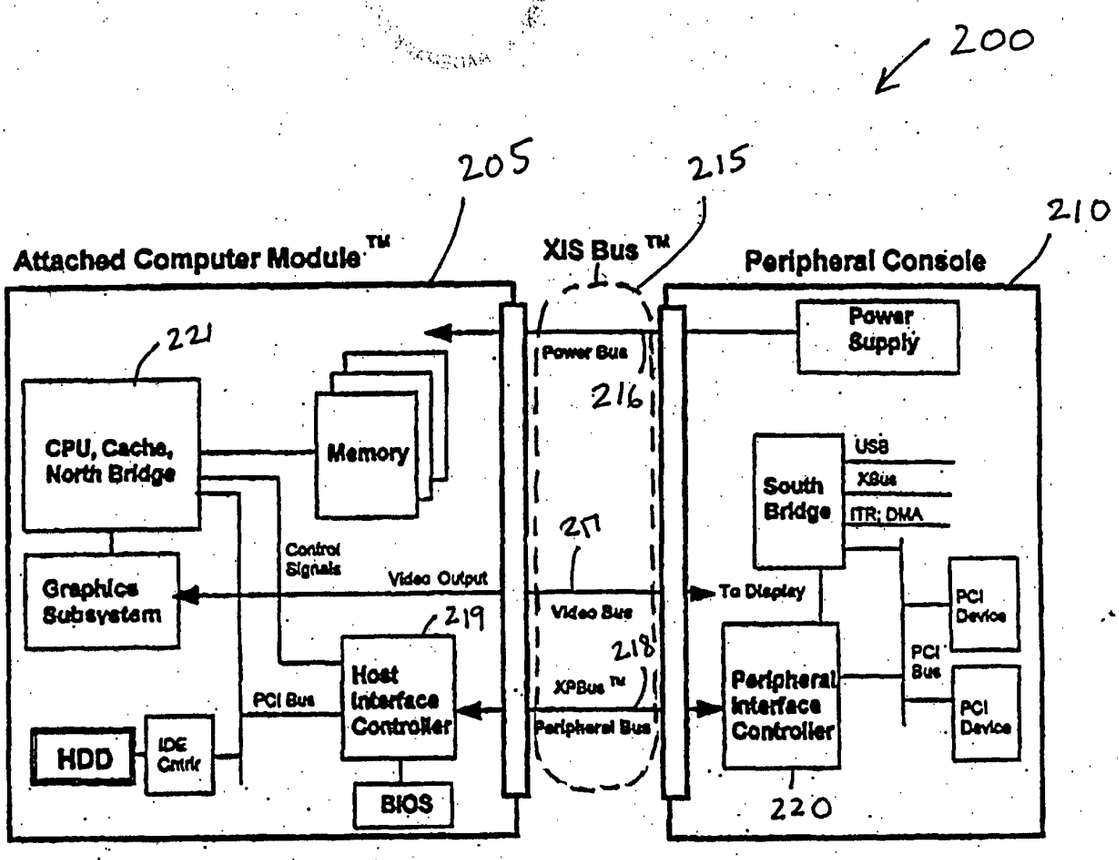

200
205
215
210
Attached Computer Module™
XIS Bus™
Peripheral Console
221
CPU, Cache, North Bridge
Memory
Graphics Subsystem
Control Signals
Video Output
PCI Bus
HDD
IDE Cntrlr
Host Interface Controller
BIOS
219
Power Bus
216
217
Video Bus
218
XPBus™
Peripheral Bus
Power Supply
South Bridge
USB
XBus
ITR; DMA
To Display
PCI Device
PCI Bus
PCI Device
Peripheral Interface Controller
220

FIGURE 2

BEST COPY

UNITED STATES DEPARTMENT OF COMMERCE
Patent and Trademark Office
Address: COMMISSIONER OF PATENTS AND TRADEMARKS
Washington, D.C. 20231

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.
09/149,882	09/08/98	CHU	W 387112000300

TM02/0323

RICHARD T. OGAWA
TOWNSEND AND TOWNSEND AND CREW L.L.P
TWO EMBARCADERO CENTER
8 TH FLOOR
SAN FRANCISCO CA 94111-3834

EXAMINER	
CAO, C	
ART UNIT	PAPER NUMBER
2182	14

DATE MAILED: 03/23/01

Please find below and/or attached an Office communication concerning this application or proceeding.

Commissioner of Patents and Trademarks

PTO-90C (Rev. 2/95)
*U.S. GPO: 2000-473-000/44602

1- File Copy

Office Action Summary

Application No.	Applicant(s)
09/149,882	Chu
Examiner	**Group Art Unit**
Chun Cao	2182

☒ Responsive to communication(s) filed on *Jan 17, 2001*

☐ This action is **FINAL.**

☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11; 453 O.G. 213.

A shortened statutory period for response to this action is set to expire *3* month(s), or thirty days, whichever is longer, from the mailing date of this communication. Failure to respond within the period for response will cause the application to become abandoned. (35 U.S.C. § 133). Extensions of time may be obtained under the provisions of 37 CFR 1.136(a).

Disposition of Claims

☒ Claim(s) *43-60* is/are pending in the application.

Of the above, claim(s) _____ is/are withdrawn from consideration.

☐ Claim(s) _____ is/are allowed.

☒ Claim(s) *43-60* is/are rejected.

☐ Claim(s) _____ is/are objected to.

☐ Claims _____ are subject to restriction or election requirement.

Application Papers

☐ See the attached Notice of Draftsperson's Patent Drawing Review, PTO-948.

☐ The drawing(s) filed on _____ is/are objected to by the Examiner.

☒ The proposed drawing correction, filed on *Jan 17, 2001* is ☒ approved ☐ disapproved.

☐ The specification is objected to by the Examiner.

☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. § 119

☐ Acknowledgement is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d).

☐ All ☐ Some* ☐ None of the CERTIFIED copies of the priority documents have been

☐ received.

☐ received in Application No. (Series Code/Serial Number) _____.

☐ received in this national stage application from the International Bureau (PCT Rule 17.2(a)).

*Certified copies not received: _____

☐ Acknowledgement is made of a claim for domestic priority under 35 U.S.C. § 119(e).

Attachment(s)

☒ Notice of References Cited, PTO-892

☒ Information Disclosure Statement(s), PTO-1449, Paper No(s). *12*

☐ Interview Summary, PTO-413

☐ Notice of Draftsperson's Patent Drawing Review, PTO-948

☐ Notice of Informal Patent Application, PTO-152

--- SEE OFFICE ACTION ON THE FOLLOWING PAGES ---

DETAILED ACTION

1. Claims 43-60 are presented for examination.

Claim Rejections - 35 USC § 102

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless --
>
> (e) the invention was described in a patent granted on an application for patent by another filed in the United States before the invention thereof by the applicant for patent, or on an international application by another who has fulfilled the requirements of paragraphs (1), (2), and (4) of section 371© of this title before the invention thereof by the applicant for patent.

3. Claims 43-46 and 51 are rejected under 35 U.S.C. 102(e) as being anticipated by Jenkins et al. U.S. Patent No. 5,999,952 (hereinafter "Jenkins).

Jenkins is a prior art reference cited by applicant in paper no. 12.

As claim 43, Jenkins discloses a modular computer system [fig. 1] comprising:

a peripheral console [6, fig. 1] including a power supply and a peripheral component interface [col. 9, lines 50-51; col. 10, lines 45-54];

a computer module [1, fig. 3] including a central processing unit [8, fig. 3] and a main memory [12, fig. 3];

a power bus [32, fig. 3] between the computer module and the peripheral console, the power bus configured such that the central processing unit receives power only when the computer module is attached to the peripheral console [col. 10, 40-46];

a differential signal channel between the computer module and the peripheral console, the differential signal channel configured to communicate a differential data signal pair between the computer module and the peripheral console [fig. 3; col. 10, lines 34-37, 46-57].

As claims 44-45, Jenkins further discloses a graphics controller [16, fig. 3], and the peripheral console and the computer module are configured to communicate with the graphics controller [col. 10, lines 30-31].

As claims 46 and 51, Jenkins further discloses a video bus [16, fig. 3;].

Claim Rejections - 35 USC § 103

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> **(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.**

5. Claims 47-50, 52 and 53-60 are rejected under 35 U.S.C. 103(a) as being unpatentable over Jenkins et al. U.S. Patent No. 5,999,952 as applied to claim 43 above further in view of MacLaren, U.S. Patent No. 6,052,513[1].

Office notice is taken that the limitations set forth in claims 47-50 are well known in the art.

---

[1]. MacLaren is a reference cited in prior office action in paper no. 7.

Office notice is taken that the limitations set forth in claims 52-53 are well known in the art. Such as using a power of 3.3V or 5V for computer module. Inherently, Jenkins teaches of using a power of 3.3V or 5V for computer module for the system [col. 10, lines 53-54].

As claims 54-56, Jenkins does not teach that the differential signal channel comprises at least two pairs of differential signal lines.

However, MacLaren teaches that the differential signal channel comprises at least two pairs of differential signal lines [fig. 5; col. 52, lines 7-19, 34-36].

It would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the teachings of MacLaren and Jenkins because MacLaren's teachings of using differential signal lines for data and clock would improve the efficiency and accuracy of Jenkins system by allowing the interface channel to communicate between computer module and peripheral console.

As claim 57, MacLaren discloses an LVDS channel [col. 59, lines 2-16].

Office notice is taken that the limitation set forth in claim 58 is well known in the art. Inherently, MacLaren can able to implement IEEE 1394 for its system [col. 59, lines 2-16].

As claims 59-60, MacLaren discloses a first PCI bus [24, fig. 3] in electrical communication with the differential signal channel through a first interface controller [26, fig. 3], and a second PCI bus [32, fig. 3] in electrical communication with the differential signal channel through a second interface controller [48, fig. 3; col. 6, lines 40-51].

Any response to this action should be mailed to:

Commissioner of Patents and Trademarks

Washington, D.C. 20231

or faxed to:

(703) 308-9051, (for formal communications intended for entry)

Or:

(703) 306-5404 (for informal or draft communications, please label "PROPOSED" or "DRAFT")

Hand-delivered responses should be brought to Crystal Park II, 2121 Crystal Drive, Arlington. VA., Sixth Floor (Receptionist).

5. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Chun Cao at (703)308-6106. The examiner can normally be reached on Monday-Friday from 7:30 am - 4:00 pm. If attempts to reach the examiner by phone are unsuccessful, the examiner's supervisor Thomas Lee can be reached at (703)305-9717. The fax number for this Art Unit is (703) 308-9051.

Any inquiry of a general nature or relating to the status of this application should be directed to the Group receptionist whose telephone number is (703)305-9600.

Chun Cao

Mar 14, 2001

THOMAS LEE
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2100

FORM PTO-892 U.S. DEPARTMENT OF COMMERCE PATENT AND TRADEMARK OFFICE	SERIAL NO. 09/149882	GROUP ART UNIT 2182	ATTACHMENT TO PAPER NO.	15
NOTICE OF REFERENCES CITED	APPLICANT(S) Chu			

U.S. PATENT DOCUMENTS

*		DOCUMENT NO.	DATE	NAME	CLASS	SUB-CLASS	FILING DATE
	A	5,140,172	8/1992	Flach	307	112	
	B	5,264,992	11/1993	Hogdahl et al.	361	681	
	C	6,070,211	5/2000	Neal et al.	710	106	
	D	6,148,243	11/2000	Ishii et al.	700	94	
	E						
	F						
	G						
	H						
	I						
	J						
	K						

FOREIGN PATENT DOCUMENTS

*		DOCUMENT NO.	DATE	COUNTRY	NAME	CLASS	SUB-CLASS
	L						
	M						
	N						
	O						
	P						
	Q						

OTHER REFERENCES (Including Author, Title, Date, Pertinent Pages, Etc.)

	R	
	S	
	T	
	U	

EXAMINER	DATE	
Chun Cao	March 14, 2001	Form892ccs2106b

* A copy of this reference is not being furnished with this office action.
(See Manual of Patent Examining Procedure, section 707.05(a).)

FORM PTO-1449 (Modified)	Attorney Docket No.: 19152-000200US	Application No.: 09/149,882
LIST OF PATENTS AND PUBLICATIONS FOR APPLICANT'S INFORMATION DISCLOSURE STATEMENT (Use several sheets if necessary)	Applicant: William W.Y. Chu	
	Filing Date: September 8, 1998	Group: 2782

Reference Designation — **U.S. PATENT DOCUMENTS** — Page 1

Examiner Initial	Document No.	Date	Name	Class	Sub-class	Filing Date (If Appropriate)
C 1	5,948,047	09/07/99	Jenkins et al.	708	141	
C 2	5,999,952	12/07/99	Jenkins et al.	708	100	
C 3	6,029,183	02/22/00	Jenkins et al.	708	100	
4						
5						
6						
7						
8						
9						
10						
11						
12						

FOREIGN PATENT DOCUMENTS

	Document No.	Date	Country	Class	Sub-class	Translation (Yes/No)
13						
14						
15						
16						
17						
18						

OTHER ART (Including Author, Title, Date, Pertinent Pages, Etc.)

19	
20	
21	
22	
23	

EXAMINER CAO DATE CONSIDERED 3-14-01

EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609; Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.

OCT 16 2000 PATENT & TRADEMARK OFFICE
RECEIVED OCT 20 2000 TECH CENTER 2100

Transaction History Date 2001-07-23
Date information retrieved from USPTO Patent Application Information Retrieval (PAIR) system records at www.uspto.gov

2182 #16

Please type a plus sign (+) inside this box → [+]

PTO/SB/21 (08-00)
Approved for use through 10/31/2002. OMB 0651-0031
U.S. Patent and Trademark Office: U.S. DEPARTMENT OF COMMERCE
Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it displays a valid OMB control number.

OIPE JC764 JUL 23 2001 PATENT & TRADEMARK OFFICE

TRANSMITTAL FORM

(to be used for all correspondence after initial filing)

Application Number	09/149,882
Filing Date	September 8, 1998
First Named Inventor	Chu, William W.Y.
Group Art Unit	2182
Examiner Name	C. Cao
Total Number of Pages in This Submission	
Attorney Docket Number	019152000200

RECEIVED JUL 27 2001 Technology Center 2100

ENCLOSURES *(check all that apply)*

☒ Fee Transmittal Form	☐ Assignment Papers *(for an Application)*	☐ After Allowance Communication to Group
☐ Fee Attached	☐ Drawing(s)	☐ Appeal Communication to Board of Appeals and Interferences
☒ Amendment / Response	☐ Licensing-related Papers	☐ Appeal Communication to Group *(Appeal Notice, Brief, Reply Brief)*
☐ After Final	☐ Petition Routing Slip (PTO/SB/69) and Accompanying Petition	☐ Proprietary Information
☐ Affidavits/declaration(s)	☐ Petition to Convert to a Provisional Application	☐ Status Letter
☒ Extension of Time Request	☐ Power of Attorney, Revocation Change of Correspondence Address	☒ Other Enclosure(s) *(please identify below)*:
☐ Express Abandonment Request	☐ Terminal Disclaimer	1 Reference; Return Postcard
☒ Information Disclosure Statement	☐ Request for Refund	
☐ Certified Copy of Priority Document(s)	☐ CD, Number of CD(s)	
☐ Response to Missing Parts/ Incomplete Application	Remarks	The Commissioner is authorized to charge any additional fees to Deposit Account 20-1430.
☐ Response to Missing Parts under 37 CFR 1.52 or 1.53		

SIGNATURE OF APPLICANT, ATTORNEY, OR AGENT

Firm and Individual name	Townsend and Townsend and Crew LLP Kent J. Tobin Reg No. 39,496
Signature	
Date	7/19/01

CERTIFICATE OF MAILING

I hereby certify that this correspondence is being deposited with the United States Postal Service with sufficient postage as first class mail in an envelope addressed to: Assistant Commissioner for Patents, Washington, D.C. 20231 on this date: 7/19/01

Typed or printed name	Aimee Durham
Signature	Durham
Date	7/19/01

Burden Hour Statement: This form is estimated to take 0.2 hours to complete. Time will vary depending upon the needs of the individual case. Any comments on the amount of time you are required to complete this form should be send to the Chief Information Officer, U.S. Patent and Trademark Office, Washington, DC 20231. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. SEND TO: Assistant Commissioner for Patents, Washington, DC 20231.
PA 3158204 v1

PTO/SB/17 (09-00)

Approved for use through 10/31/2002. OMB 0651-0032

Patent and Trademark Office: U.S. DEPARTMENT OF COMMERCE

Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it displays a valid OMB control number.

FEE TRANSMITTAL for FY 2001

Patent fees are subject to annual revision.

OIPE JC184 JUL 23 2001 PATENT & TRADEMARK OFFICE

RECEIVED JUL 27 2001 Technology Center 2100

TOTAL AMOUNT OF PAYMENT ($) 235

Complete If Known	
Application Number	09/149,882
Filing Date	September 8, 1998
First Named Inventor	Chu, William W.Y.
Examiner Name	C. Cao
Group Art Unit	2182
Attorney Docket No.	019152-000200US

METHOD OF PAYMENT

1. ☒ The Commissioner is hereby authorized to charge indicated fees and credit any over payments to:

Deposit Account Number: 20-1430

Deposit Account Name: Townsend and Townsend and Crew LLP

☒ Charge Any Additional Fee Required Under 37 CFR 1.16 and 1.17

☒ Applicant claims small entity status. See 37 CFR 1.27

2. ☐ Payment Enclosed:

☐ Check ☐ Credit card ☐ Money Order ☐ Other

FEE CALCULATION

1. BASIC FILING FEE

Large Fee Code	Large Entity Fee ($)	Small Fee Code	Small Entity Fee ($)	Fee Description	Fee Paid
101	710	201	355	Utility filing fee	
106	320	206	160	Design filing fee	
107	490	207	245	Plant filing fee	
108	710	208	355	Reissue filing fee	
114	150	214	75	Provisional filing fee	

SUBTOTAL (1) ($)

2. EXTRA CLAIM FEES

			Extra Claims		Fee from below	=	Fee Paid
Total Claims		-20**	=		X	=	
Independent Claims		-3**	=		X	=	
Multiple Dependent					X	=	

Large Fee Code	Large Entity Fee ($)	Small Fee Code	Small Entity Fee ($)	Fee Description
103	18	203	9	Claims in excess of 20
102	80	202	40	Independent claims in excess of 3
104	270	204	135	Multiple dependent claim, if not paid
109	80	209	40	** Reissue independent claims over original patent
110	18	210	9	** Reissue claims in excess of 20 and over original patent

SUBTOTAL (2) ($)

**or number previously paid, if greater; For Reissues, see above

FEE CALCULATION (continued)

3. ADDITIONAL FEES

Large Fee Code	Large Entity Fee ($)	Small Fee Code	Small Entity Fee ($)	Fee Description	Fee Paid
105	130	205	65	Surcharge - late filing fee or oath	
127	50	227	25	Surcharge - late provisional filing fee or cover sheet.	
139	130	139	130	Non-English specification	
147	2,520	147	2,520	For filing a request for reexamination	
112	920*	112	920*	Requesting publication of SIR prior to Examiner action	
113	1,840*	113	1,840*	Requesting publication of SIR after Examiner action	
115	110	215	55	Extension for reply within first month	55
116	390	216	195	Extension for reply within second month	
117	890	217	445	Extension for reply within third month	
118	1,390	218	695	Extension for reply within fourth month	
128	1,890	228	945	Extension for reply within fifth month	
119	310	219	155	Notice of Appeal	
120	310	220	155	Filing a brief in support of an appeal	
121	270	221	135	Request for oral hearing	
138	1,510	138	1,510	Petition to institute a public use proceeding	
140	110	240	55	Petition to revive – unavoidable	
141	1,240	241	620	Petition to revive – unintentional	
142	1,240	242	620	Utility issue fee (or reissue)	
143	440	243	220	Design issue fee	
144	600	244	300	Plant issue fee	
122	130	122	130	Petitions to the Commissioner	
123	50	123	50	Petitions related to provisional applications	
126	180	126	180	Submission of Information Disclosure Stmt	180
581	40	581	40	Recording each patent assignment per property (times number of properties)	
146	710	246	355	Filing a submission after final rejection (37 CFR § 1.129(a))	
149	710	249	355	For each additional invention to be examined (37 CFR § 1.129(b))	
179	710	279	355	Request for Continued Examination (RCE)	
169	900	169	900	Request for expedited examination of a design application	
Other fee (specify)					

The Commissioner is authorized to charge any additional fees to the above noted Deposit Account.

*Reduced by Basic Filing Fee Paid SUBTOTAL (3) ($)235

SUBMITTED BY				Complete (if applicable)	
Name (Print/Type)	Kent J. Tobin	Registration No. (Attorney/Agent)	39,496	Telephone	650-326-2400
Signature				Date	7/19/01

WARNING: Information on this form may become public. Credit card information should not be included on this form. Provide credit card information and authorization on PTO-2038.

Burden Hour Statement: This form is estimated to take 0.2 hours to complete. Time will vary depending upon the needs of the individual case. Any comments on the amount of time you are required to complete this form should be sent to the Chief Information Officer, Patent and Trademark Office, Washington, DC 20231. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. SEND TO: Assistant Commissioner for Patents, Washington, DC 20231. PA 3158205 v1

#16 a/A 7-31-01

I hereby certify that this correspondence is being deposited with the United States Postal Service as first class mail in an envelope addressed to:

Assistant Commissioner for Patents
Washington, D.C. 20231

On July 19 2001

TOWNSEND and TOWNSEND and CREW LLP

By: [signature]

PATENT

Attorney Docket No.: 19152-000200US

OIPE JC184 JUL 23 2001 PATENT & TRADEMARK OFFICE

RECEIVED JUL 27 2001 Technology Center 2100

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re application of:

William W.Y. Chu

Application No.: 09/149,882

Filed: September 8, 1998

For: COMMUNICATION CHANNEL AND INTERFACE DEVICES FOR BRIDGING COMPUTER INTERFACE BUSES

Examiner: C. Cao

Art Unit: 2782

RESPONSE TO OFFICE ACTION OF March 23, 2001

Assistant Commissioner for Patents
Washington, D.C. 20231

Sir:

In response to the Office Action mailed March 23, 2001, please amend the above-referenced application as follows. A petition for a one month extension of time for responding to this office action is submitted herewith.

IN THE CLAIMS:

Please cancel claims 47,48, and 50.

Please amend claims ~~43~~, 44, and 46 as follows:

1 ~~43~~. (Amended) A modular computer system comprising:

a peripheral console including a power supply, a programmable memory containing configuration information, and a peripheral component interface;

a computer module including a central processing unit and a main memory;

40

a power bus between the computer module and the peripheral console, the power bus configured such that the central processing unit receives power only when the computer module is attached to the peripheral console; and

a differential signal channel between the computer module and the peripheral console, the differential signal channel configured to communicate an encoded bit stream comprising PCI bus transaction data bits, system control signal data bits, and peripheral console configuration information data bits, the transaction data bits, system control signal data bits, and peripheral console configuration information data bits separated within the encoded bit stream.

44. (Amended) The modular computer system of claim 43 wherein the computer module further comprises a graphics controller and the peripheral console is configured to receive video capture data from a video source, the modular computer system further comprising a second differential signal channel between the computer module and the peripheral console, the differential channel configured to encode the bit stream to communicate the video capture data to the graphics controller.

46. (Amended) The modular computer system of claim 43 further comprising a video bus configured to communicate mixed encoded RGB analog video display signals, digital video display signals, and television display signals from the computer module to the peripheral console.

REMARKS

Claims 47, 48, and 50 have been canceled. Claims 43, 44, and 46 have been amended. Claims 43-46, 49, and 51-60 are pending.

In the office action mailed March 23, 2001, the Examiner rejected claims 43-46 and 51 as anticipated by U.S. Patent no. 5,999,952 ("the Jenkins patent") under 35 U.S.C. §102. The Examiner also rejected remaining claims 47-50, 52, and 53-60 as obvious under 35 U.S.C. §103, based upon the Jenkins patent in view of U.S. Patent no. 6,052,513 ("the MacLaren patent"). The claims have now been amended to overcome these rejections.

Specifically, pending independent claim 43 has been amended to indicate that the differential signal channel between the computer module and the peripheral console is configured to communicate from a programmable memory an encoded bit stream that includes several different types of information. A first type of encoded information is PCI bus transaction data. A second type of encoded information is system control information. A third type of encoded information is peripheral console configuration information.

Support for this amendment may be found in the specification as originally filed. Specifically, support for the programmable memory of the peripheral console providing configuration signals may be found at page 11, lines 16-20. Support for a differential signal channel communicating an encoded bit stream is found at page 13, lines 2-11 (communicating PCI bus transaction data bits), and page 16, lines 18-26 (communicating system control signal data bits). The communication of peripheral console configuration information data bits is shown in Fig. 35, which lists identification bits "0111' used as an initialization data packet for configuration information. These initialization data package bits are transmitted across the communications structure between the computer module and the peripheral console.

In contrast, while the Jenkins patent devotes considerable discussion to internal configuration of the core unit (See Fig. 3 and col. 10, lines 15-55), the nature of communication between the core and the enclosure is described in only very general terms. (See FIG. 3 and description of "CONNECTOR BUS-CORE 3" and "ENCLOSURE CONNECTOR BUS 4" at col. 10, lines 13-15). Nowhere does the Jenkins patent teach or suggest a communications structure configured to convey encoded bits of the various types recited in claim 43 as amended.

Moreover, the communication structure of the computer system of independent claim 43 is not obvious when the Jenkins patent is considered in light of the MacLaren patent. Specifically, the MacLaren patent describes a PCI-PCI serial link, and does not teach or suggest use in a modular computer system of a communications structure configured to convey encoded bits of the types recited in claim 43.

Finally, dependent claims 44 and 46 describe an additional form of encoded information communicated between the computer module and peripheral console. Specifically, video information such as video capture data or encoded video display data in

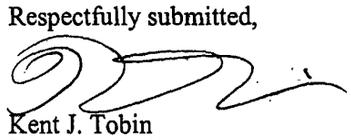
RGB analog or digital video display formats, may also be communicated in accordance with embodiments of computer systems in accordance with the present invention. Neither the Jenkins patent nor the MacLaren patent describe communication structures configured to convey encoded bits of the types recited in claims 44 and 46..

CONCLUSION

In view of the foregoing amendments and remarks, it is believed that all pending claims are now in condition for allowance. The issuance of a formal Notice of Allowance at an early date is respectfully requested.

If the Examiner believes a telephone conference would expedite prosecution of this application, please telephone the undersigned at 650-326-2400.

Respectfully submitted,



Kent J. Tobin
Reg. No. 39,496

TOWNSEND and TOWNSEND and CREW LLP
Two Embarcadero Center, 8th Floor
San Francisco, California 94111-3834
Tel: (415) 576-0200
Fax: (415) 576-0300
KJT
PA 3148802 v1

VERSION WITH MARKINGS TO SHOW CHANGES MADE

In the claims:

43. (Amended) A modular computer system comprising:

a peripheral console including a power supply, a programmable memory containing configuration information, and a peripheral component interface;

a computer module including a central processing unit and a main memory;

a power bus between the computer module and the peripheral console, the power bus configured such that the central processing unit receives power only when the computer module is attached to the peripheral console; and

a differential signal channel between the computer module and the peripheral console, the differential signal channel configured to communicate [a differential data signal pair between the computer module and the peripheral console] an encoded bit stream comprising PCI bus transaction data bits, system control signal data bits, and peripheral console configuration information data bits, the transaction data bits, system control signal data bits, and peripheral console configuration information data bits separated within the encoded bit stream.

44. (Amended) The modular computer system of claim 43 wherein[:] the computer module further comprises a graphics controller[;] and the peripheral console is configured to receive video capture data from a video source, the modular computer system further comprising a second differential signal channel between the computer module and the peripheral console, the differential channel configured to encode the bit stream to communicate the video capture data to the graphics controller.

46. (Amended) The modular computer system of claim [45] 43 further comprising a video bus configured to communicate mixed encoded RGB analog video display signals, digital video display signals, and television display signals [the video display signal] from the computer module to the peripheral console.

PTO/SB/22 (10-00)

Approved for use through 10/31/2002. OMB 0651-0031
U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE

Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it displays a valid OMB control number.

#15
AN 7-31-0.

OIPE JC184 JUL 23 2001 PATENT & TRADEMARK OFFICE

PETITION FOR EXTENSION OF TIME UNDER 37 CFR 1.136(a)

Docket Number (Optional) 019152000200

In re Application of William W.Y. Chu

Application Number 09/149,882 | Filed September 8, 1998

For COMMUNICATION CHANNEL AND INTERFACE DEVICES FOR BRIDGING COMPUTER INTERFACE BUSES

Group Art Unit 2182 | Examiner C. Cao

RECEIVED
JUL 27 2001
Technology Center 2100

This is a request under the provisions of 37 CFR 1.136(a) to extend the period for filing a reply in the above identified application.

The requested extension and appropriate non-small-entity fee are as follows (check time period desired):

- ☒ One month (37 CFR 1.17(a)(1)) $110
- ☐ Two months (37 CFR 1.17(a)(2)) $
- ☐ Three months (37 CFR 1.17(a)(3)) $
- ☐ Four months (37 CFR 1.17(a)(4)) $
- ☐ Five months (37 CFR 1.17(a)(5)) $

☒ Applicant claims small entity status. See 37 CFR 1.27. Therefore, the fee amount shown above is reduced by one-half, and the resulting fee is: $ 55 .

☐ A check in the amount of the fee is enclosed.

☐ Payment by credit card. Form PTO-2038 is attached.

☐ The Commissioner has already been authorized to charge fees in this application to a Deposit Account.

☒ The Commissioner is hereby authorized to charge any fees which may be required, or credit any overpayment, to Deposit Account Number 20-1430.
I have enclosed a duplicate copy of this sheet.

I am the ☐ applicant/inventor.

☐ assignee of record of the entire interest. See 37 CFR 3.71
Statement under 37 CFR 3.73(b) is enclosed. (Form PTO/SB/96).

☒ attorney or agent of record.

☐ attorney or agent under 37 CFR 1.34(a).
Registration number if acting under 37 CFR 1.34(a). _____ .

WARNING: Information on this form may become public. Credit card information should not be included on this form. Provide credit card information and authorization on PTO-2038.

7/19/01
Date

Signature

Kent J. Tobin, Reg. No. 39,496
Typed or printed name

00000003 201430 09149882
55.00 CH

NOTE: Signatures of all the inventors or assignees of record of the entire interest or their representative(s) are required. Submit multiple forms if more than one signature is required; see below*.

☐ *Total of _____ forms are submitted.

Burden Hour Statement: This form is estimated to take 0.1 hours to complete. Time will vary depending upon the needs of the individual case. Any comments on the amount of time you are required to complete this form should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, Washington, DC 20231. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. SEND TO: Assistant Commissioner for Patents, Washington, DC 20231.
PA 3158212 v1

17/2007
7-8-01

PATENT

I hereby certify that this correspondence is being deposited with the United States Postal Service as first class mail in an envelope addressed to:

Assistant Commissioner for Patents
Washington, D.C. 20231

Attorney Docket No.: 019152-000200US

RECEIVED
JUL 27 2001
Technology Center 2100



Date: July 19 2001

TOWNSEND and TOWNSEND and CREW LLP

By: _____



IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re application of:

William W.Y. Chu

Application No.: 09/149,882

Filed: September 8, 1998

For: COMMUNICATION CHANNEL AND INTERFACE DEVICES FOR BRIDGING COMPUTER INTERFACE BUSES

Examiner: C. Cao

Art Unit: 2182

SUPPLEMENTAL INFORMATION DISCLOSURE STATEMENT UNDER 37 CFR §1.97 and §1.98

Assistant Commissioner for Patents
Washington, D.C. 20231

Sir:

The references cited on attached form PTO-1449 are being called to the attention of the Examiner. Copies of the references are enclosed. It is respectfully requested that the cited references be expressly considered during the prosecution of this application, and the references be made of record therein and appear among the "references cited" on any patent to issue therefrom.

As provided for by 37 CFR 1.97(g) and (h), no inference should be made that the information and references cited are prior art merely because they are in this statement and

00000003 203436 09149882
90.00 OP

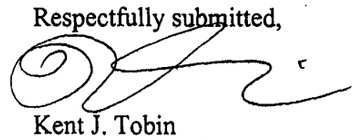
no representation is being made that a search has been conducted or that this statement encompasses all the possible relevant information.

This IDS is being filed after the mailing date of the first Office Action and more than three months after the filing date, but prior to the Notice of Allowance or Final Office Action.

Please deduct $180.00, pursuant to 37 CFR §1.17(p), from the undersigned's Deposit Account No. 20-1430. Please deduct any additional fees from, or credit any overpayment to, the above-noted Deposit Account.

This Petition is submitted in triplicate.

Respectfully submitted,



Kent J. Tobin
Reg. No. 39,496

TOWNSEND and TOWNSEND and CREW LLP
Two Embarcadero Center, 8th Floor
San Francisco, California 94111-3834
Tel: 650-326-2400
Fax: 650-326-2422
KJT:ad

PA 3158208 v1

FORM PTO-1449 (Modified)	Attorney Docket No.: 019152-000200US	Application No.: 09/149,882
LIST OF PATENTS AND PUBLICATIONS FOR APPLICANT'S INFORMATION DISCLOSURE STATEMENT (Use several sheets if necessary)	Applicant: William W.Y. Chu	
	Filing Date: September 8, 1998	Group: 2182

Reference Designation — **U.S. PATENT DOCUMENTS** — Page 1

Examiner Initial	Document No.	Date	Name	Class	Sub-class	Filing Date (If Appropriate)
C AA	6,216,185	04/10/2001	Chu	710	101	09/08/1998
____ AB						
____ AC						
____ AD						
____ AE						
____ AF						
____ AG						
____ AH						
____ AI						
____ AJ						
____ AK						
____ AL						

FOREIGN PATENT DOCUMENTS

	Document No.	Date	Country	Class	Sub-class	Translation (Yes/No)
____ AM						
____ AN						
____ AO						
____ AP						
____ AQ						
____ AR						

OTHER ART (Including Author, Title, Date, Pertinent Pages, Etc.)

____ AS	
____ AT	
____ AU	
____ AV	
____ AW	

EXAMINER C.A. DATE CONSIDERED 5-1-03

EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609; Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.

RECEIVED
JUL 27 2001
Technology Center 2100

BEST COPY

UNITED STATES DEPARTMENT OF COMMERCE
Patent and Trademark Office
Address: COMMISSIONER OF PATENTS AND TRADEMARKS
Washington, D.C. 20231

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.
09/149,882	09/08/98	CHU W	387112000300

TM21/0817
RICHARD T. OGAWA
TOWNSEND AND TOWNSEND AND CREW L.L.P
TWO EMBARCADERO CENTER
8 TH FLOOR
SAN FRANCISCO CA 94111-3834

EXAMINER	
CAO,C	
ART UNIT	PAPER NUMBER
2182	#18

DATE MAILED: 08/17/01

Please find below and/or attached an Office communication concerning this application or proceeding.

Commissioner of Patents and Trademarks

Notice of Allowability

Application No.	Applicant(s)
09/149,882	Chu
Examiner	**Art Unit**
Chun Cao	2182

--The MAILING DATE of this communication appears on the cover sheet with the correspondence address--

All claims being allowable, PROSECUTION ON THE MERITS IS (OR REMAINS) CLOSED in this application. If not included herewith (or previously mailed), a Notice of Allowance and Issue Fee Due or other appropriate communication will be mailed in due course. **THIS NOTICE OF ALLOWABILITY IS NOT A GRANT OF PATENT RIGHTS.** This application is subject to withdrawal from issue at the initiative of the Office or upon petition by the applicant. See 37 CFR 1.313 and MPEP 1308.

1. ☒ This communication is responsive to *communication filed on 7/23/2001*

2. ☒ The allowed claim(s) is/are *43-46, 49, and 51-60*

3. ☐ The drawings filed on _____ are acceptable as formal drawings.

4. ☐ Acknowledgement is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d).

   a) ☐ All b) ☐ Some* c) ☐ None of the:

   1. ☐ Certified copies of the priority documents have been received.
   2. ☐ Certified copies of the priority documents have been received in Application No. _____ .
   3. ☐ Copies of the certified copies of the priority documents have been received in this national stage application from the International Bureau (PCT Rule 17.2(a)).

   *Certified copies not received: _____ .

5. ☐ Acknowledgement is made of a claim for domestic priority under 35 U.S.C. § 119(e).

Applicant has THREE MONTHS FROM THE "MAILING DATE" of this communication to file a reply complying with the requirements noted below. Failure to timely comply will result in ABANDONMENT of this application. **THIS THREE-MONTH PERIOD IS NOT EXTENDABLE FOR SUBMITTING NEW FORMAL DRAWINGS, OR A SUBSTITUTE OATH OR DECLARATION. This three-month period for complying with the REQUIREMENT FOR THE DEPOSIT OF BIOLOGICAL MATERIAL is extendable under 37 CFR 1.136(a).**

6. ☐ Note the attached EXAMINER'S AMENDMENT or NOTICE OF INFORMAL APPLICATION (PTO-152) which gives reason(s) why the oath or declaration is deficient. A SUBSTITUTE OATH OR DECLARATION IS REQUIRED.

7. ☒ Applicant MUST submit NEW FORMAL DRAWINGS

   (a) ☒ including changes required by the Notice of Draftsperson's Patent Drawing Review (PTO-948) attached

   1) ☐ hereto or 2) ☒ to Paper No. 7 .

   (b) ☐ including changes required by the proposed drawing correction filed _____ , which has been approved by the examiner.

   (c) ☐ including changes required by the attached Examiner's Amendment/Comment or in the Office action of Paper No. _____ .

   Identifying indicia such as the application number (see 37 CFR 1.84(c)) should be written on the drawings. The drawings should be filed as a separate paper with a transmittal letter addressed to the Official Draftsperson.

8. ☐ Note the attached Examiner's comment regarding REQUIREMENT FOR THE DEPOSIT OF BIOLOGICAL MATERIAL.

Any reply to this letter should include, in the upper right hand corner, the APPLICATION NUMBER (SERIES CODE/SERIAL NUMBER). If applicant has received a Notice of Allowance and Issue Fee Due, the ISSUE BATCH NUMBER and DATE of the NOTICE OF ALLOWANCE should also be included.

Attachment(s)

1 ☐ Notice of References Cited (PTO-892)
2 ☐ Notice of Informal Patent Application (PTO-152)
3 ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
4 ☐ Interview Summary (PTO-413), Paper No. _____ .
5 ☒ Information Disclosure Statement(s) (PTO-1449), Paper No(s). 17
6 ☐ Examiner's Amendment/Comment
7 ☐ Examiner's Comment Regarding Requirement for Deposit of Biological Material
8 ☐ Examiner's Statement of Reasons for Allowance
9 ☐ Other

THOMAS LEE
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2100

UNITED STATES DEPARTMENT OF COMMERCE
Patent and Trademark Office

NOTICE OF ALLOWANCE AND ISSUE FEE DUE

TM21/0817

RICHARD T. OGAWA
TOWNSEND AND TOWNSEND AND CREW L.L.P
TWO EMBARCADERO CENTER
8 TH FLOOR
SAN FRANCISCO CA 94111-3834

APPLICATION NO.	FILING DATE	TOTAL CLAIMS	EXAMINER AND GROUP ART UNIT	DATE MAILED
09/149,882	09/08/98	015	CAO, C 2182	08/17/01

First Named Applicant: CHU,

35 USC 154(b) term ext. = 0 Days.

TITLE OF INVENTION: COMMUNICATION CHANNEL AND INTERFACE DEVICES FOR BRIDGING COMPUTER INTERFACE BUSES

ATTY'S DOCKET NO.	CLASS-SUBCLASS	BATCH NO.	APPLN. TYPE	SMALL ENTITY	FEE DUE	DATE DUE
0 38711/000300	710-065.000	K76	UTILITY	YES	$620.00	11/19/01

THE APPLICATION IDENTIFIED ABOVE HAS BEEN EXAMINED AND IS ALLOWED FOR ISSUANCE AS A PATENT. PROSECUTION ON THE MERITS IS CLOSED.

THE ISSUE FEE MUST BE PAID WITHIN THREE MONTHS FROM THE MAILING DATE OF THIS NOTICE OR THIS APPLICATION SHALL BE REGARDED AS ABANDONED. THIS STATUTORY PERIOD CANNOT BE EXTENDED.

HOW TO RESPOND TO THIS NOTICE:

I. Review the SMALL ENTITY status shown above.
If the SMALL ENTITY is shown as YES, verify your current SMALL ENTITY status:

A. If the status is changed, pay twice the amount of the FEE DUE shown above and notify the Patent and Trademark Office of the change in status, or
B. If the status is the same, pay the FEE DUE shown above.

If the SMALL ENTITY is shown as NO:

A. Pay FEE DUE shown above, or

B. File verified statement of Small Entity Status before, or with, payment of 1/2 the FEE DUE shown above.

II. Part B-Issue Fee Transmittal should be completed and returned to the Patent and Trademark Office (PTO) with your ISSUE FEE. Even if the ISSUE FEE has already been paid by charge to deposit account, Part B Issue Fee Transmittal should be completed and returned. If you are charging the ISSUE FEE to your deposit account, section "4b" of Part B-Issue Fee Transmittal should be completed and an extra copy of the form should be submitted.

III. All communications regarding this application must give application number and batch number.
Please direct all communications prior to issuance to Box ISSUE FEE unless advised to the contrary.

IMPORTANT REMINDER: Utility patents issuing on applications filed on or after Dec. 12, 1980 may require payment of maintenance fees. It is patentee's responsibility to ensure timely payment of maintenance fees when due.

PATENT AND TRADEMARK OFFICE COPY

PTOL-85 (REV. 10-96) Approved for use through 06/30/99. (0651-0033)

*U.S. GPO: 1999-454-457/24601

#19
J.G. PS

I hereby certify that this correspondence is being deposited with the United States Postal Service as first class mail in an envelope addressed to:Box Issue Fee
Assistant Commissioner for Patents,
Washington, D.C. 20231
on 11-16-01
TOWNSEND and TOWNSEND and CREW LLP
By

PATENT
Attorney Docket No.: 019152-000200

OIPE JC68 DEC 12 2001 PATENT & TRADEMARK OFFICE

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re application of:	
William W.Y. Chu	Examiner: C. Cao
Serial No.: 09/149,882	Art Unit: 2182
Filed: September 8, 1998	Batch No.: K76
For: COMMUNICATION CHANNEL AND INTERFACE DEVICES FOR BRIDGING COMPUTER INTERFACE BUSES	LETTER TO OFFICIAL DRAFTSPERSON

Box Issue Fee
Assistant Commissioner for Patents
Washington, D.C. 20231

Sir:

Pursuant to the Notice of Allowability dated August 17, 2001, applicant submits fifty seven (57) sheets of formal drawings to be made of record in the above-identified case.

Respectfully submitted,

Kent J. Tobin
Reg. No. 39,496

TOWNSEND and TOWNSEND and CREW LLP
Two Embarcadero Center, 8th Floor
San Francisco, California 94111-3834
(415) 576-0200
Fax (415) 576-0300
KJT/ad
PA 154582 v1
PA 3183960 v1

8/17/01

BEST COPY

6345330

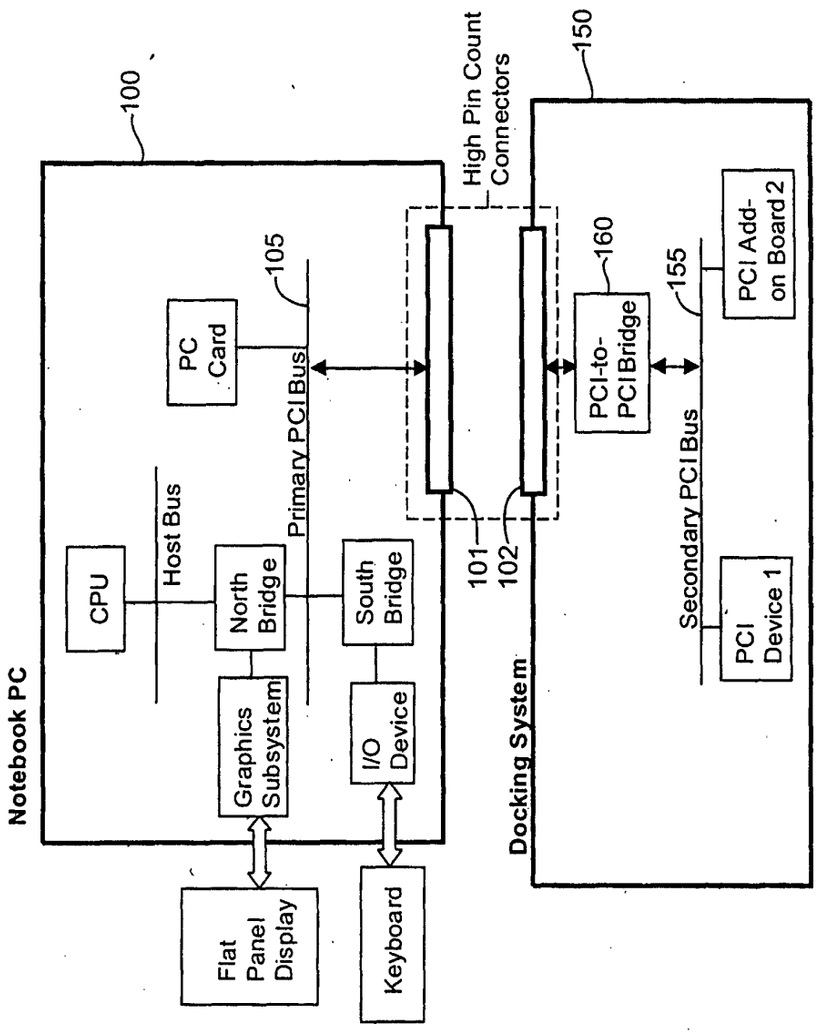


FIG. 1

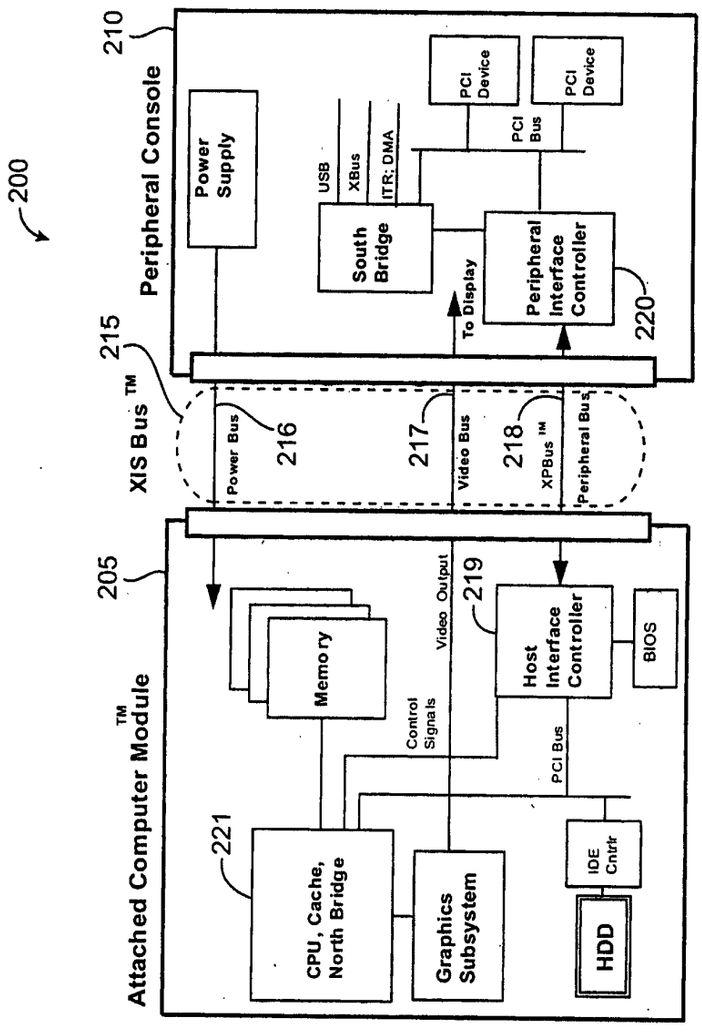

200
210
Peripheral Console
Power Supply
USB
XBus
ITR; DMA
South Bridge
PCI Device
PCI Device
PCI Bus
Peripheral Interface Controller
To Display
220
215
XIS Bus ™
Power Bus
216
217
Video Bus
218
XPBus ™
Peripheral Bus
205
Attached Computer Module ™
Memory
Control Signals
Video Output
219
Host Interface Controller
BIOS
PCI Bus
221
CPU, Cache, North Bridge
Graphics Subsystem
IDE Cntlr
HDD

FIG. 2

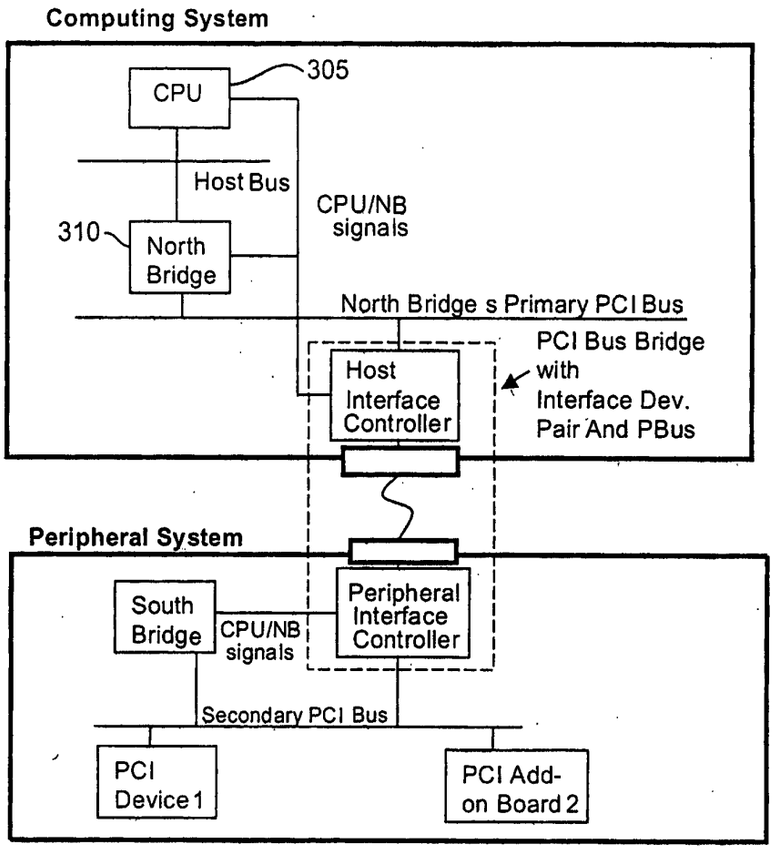

Computing System
CPU
305
Host Bus
CPU/NB signals
310
North Bridge
North Bridge s Primary PCI Bus
PCI Bus Bridge with Interface Dev. Pair And PBus
Host Interface Controller
Peripheral System
South Bridge
CPU/NB signals
Peripheral Interface Controller
Secondary PCI Bus
PCI Device 1
PCI Add-on Board 2

FIG. 3

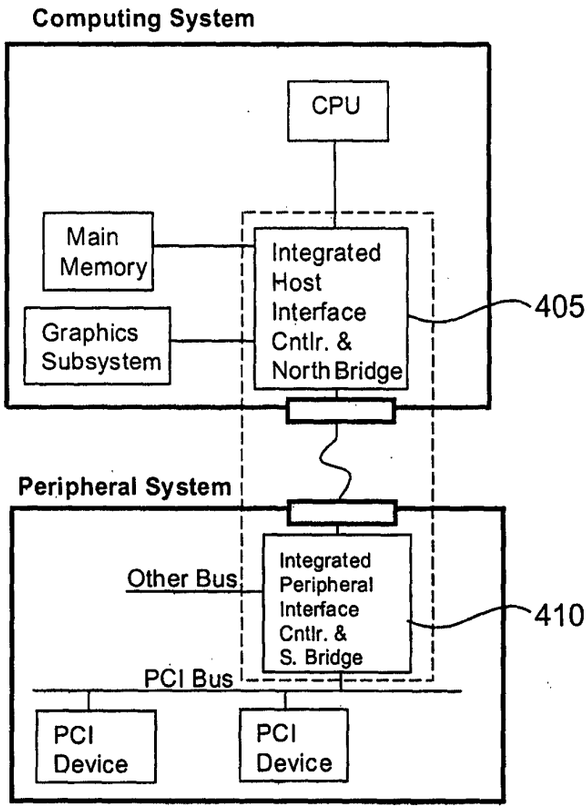

Computing System
CPU
Main Memory
Graphics Subsystem
Integrated Host Interface Cntlr. & North Bridge
405
Peripheral System
Other Bus
Integrated Peripheral Interface Cntlr. & S. Bridge
410
PCI Bus
PCI Device
PCI Device

FIG. 4

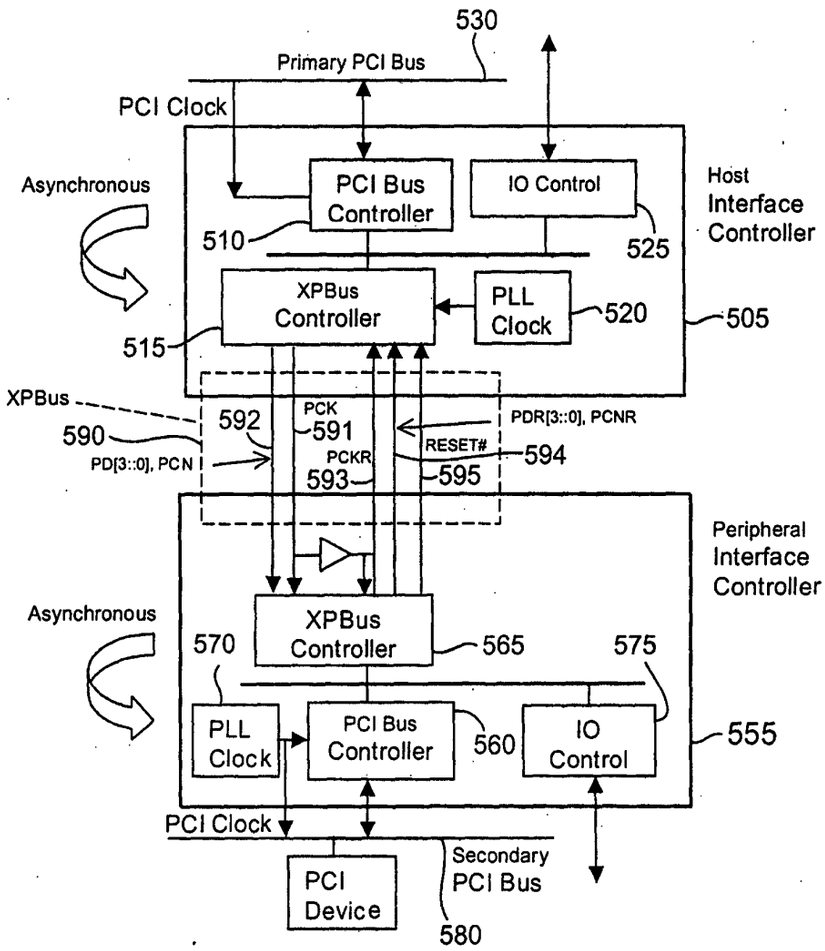

530
Primary PCI Bus
PCI Clock
Asynchronous
PCI Bus Controller
IO Control
Host Interface Controller
510
525
XPBus Controller
PLL Clock
520
505
515
XPBus
590
592
PCK
591
PDR[3::0], PCNR
RESET#
594
PD[3::0], PCN
PCKR
593
595
Peripheral Interface Controller
Asynchronous
XPBus Controller
565
570
575
PLL Clock
PCI Bus Controller
560
IO Control
555
PCI Clock
Secondary PCI Bus
PCI Device
580

FIG. 5

6 / 57

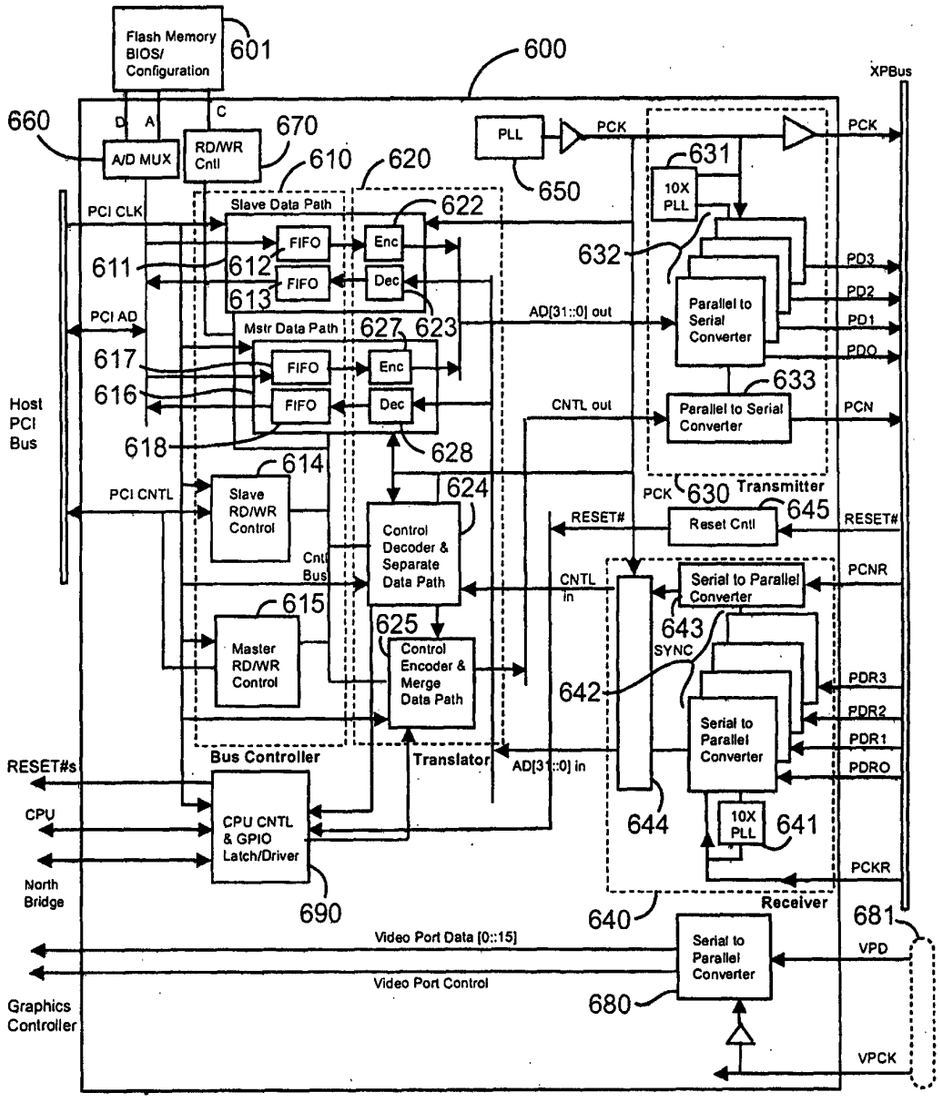

Flash Memory BIOS/ Configuration
601
600
XPBus
660
D
A
C
A/D MUX
RD/WR Cntl
670
610
620
PLL
650
PCK
631
10X PLL
PCI CLK
Slave Data Path
622
FIFO
Enc
611
612
FIFO
Dec
613
632
PD3
PD2
PD1
PD0
PCI AD
Mstr Data Path
627
623
AD[31::0] out
Parallel to Serial Converter
617
FIFO
Enc
616
FIFO
Dec
633
CNTL out
Parallel to Serial Converter
PCN
Host PCI Bus
618
628
614
PCI CNTL
Slave RD/WR Control
624
PCK
630
Transmitter
RESET#
Reset Cntl
645
RESET#
Control Decoder & Separate Data Path
Cntl Bus
CNTL in
Serial to Parallel Converter
PCNR
615
625
643
SYNC
Master RD/WR Control
Control Encoder & Merge Data Path
642
PDR3
PDR2
PDR1
PDRO
Serial to Parallel Converter
RESET#s
Bus Controller
Translator
AD[31::0] in
CPU
CPU CNTL & GPIO Latch/Driver
644
10X PLL
641
PCKR
North Bridge
690
640
Receiver
681
Video Port Data [0::15]
Serial to Parallel Converter
VPD
Video Port Control
680
Graphics Controller
VPCK

FIG. 6

HIC as Target (Default)

Control Signal	HIC to XPBus	XPBus to HIC	Primary PCI Bus	Comment
FRAME #	Encode (BS0)		Transaction Active	
IRDY #	Encode (BS1)		Initiator Ready	
TRDY #	Local		HIC Generates	
DEVSEL #	Local		HIC Accepts Command	Positive decode, medium
STOP #	Local		HIC requests to retry	Posted Read operation
PAR	Encode	Decode	Parity for A/C; D/BE	
IDSEL	Local		Used locally for config. 0	
PERR #	Encode	Decode	Data Parity Error	
SERR #		Decode	Address/System Parity Error	
REQ #		Decode	HIC requests to be master	S. Bus device requests bus
GNT #	Encode		Host grants bus	
RST				Independent signal

FIG. 7

HIC as Master

Control Signal	HIC to XPBus	XPBus to HIC	Primary PCI Bus	Comment
FRAME #		Decode	Transaction Active	
IRDY #		Decode	Initiator Ready	
TRDY #	Local		Receive from Target	
DEVSEL #	Local		Receive from Target	
STOP #	Local		retry handles locally	
PAR	Encode	Decode	Parity for A/C; D/BE	
IDSEL	Local		Used locally for config. 0	
PERR #	Encode	Decode	Data Parity Error	
SERR #		Decode	Address/System Parity Error	
REQ #		Decode	HIC continue to be Master	PCI device can end REQ#
GNT #	Encode		Arbiter grant bus to HIC	Arbiter can deassert GNT#
RST				Independent signal

FIG. 8

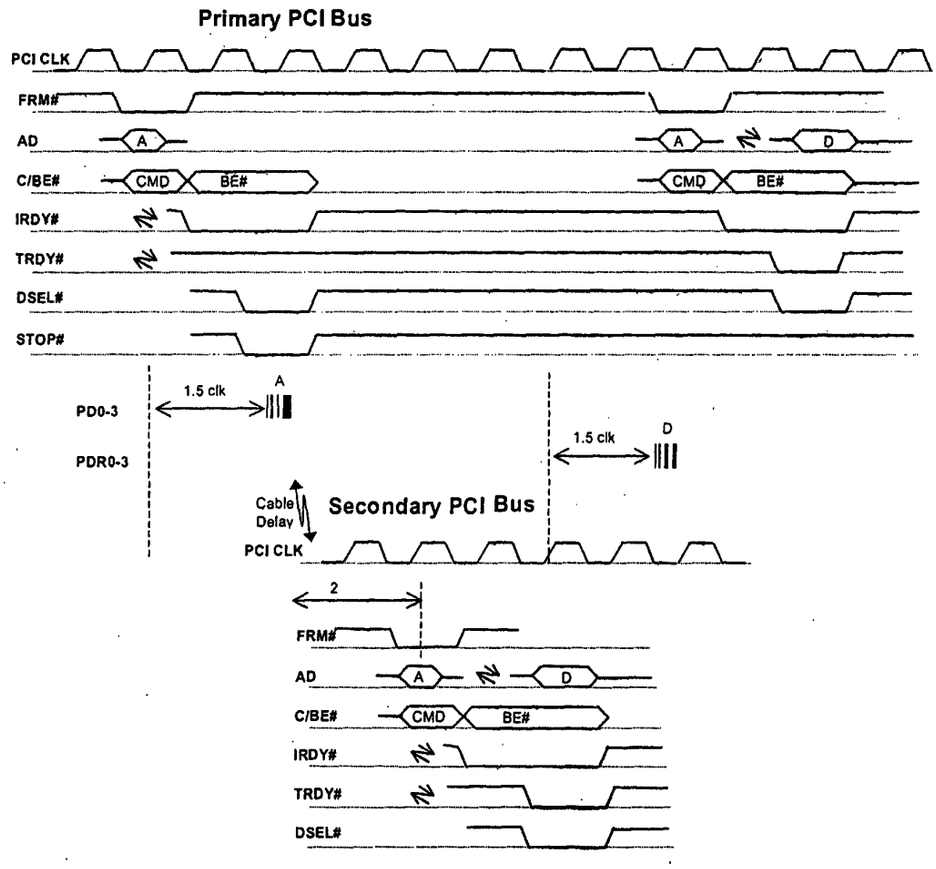

Primary PCI Bus
PCI CLK
FRM#
AD
A
A
D
C/BE#
CMD
BE#
CMD
BE#
IRDY#
TRDY#
DSEL#
STOP#
PD0-3
PDR0-3
1.5 clk
A
1.5 clk
D
Cable Delay
Secondary PCI Bus
PCI CLK
2
FRM#
AD
A
D
C/BE#
CMD
BE#
IRDY#
TRDY#
DSEL#

FIG. 9

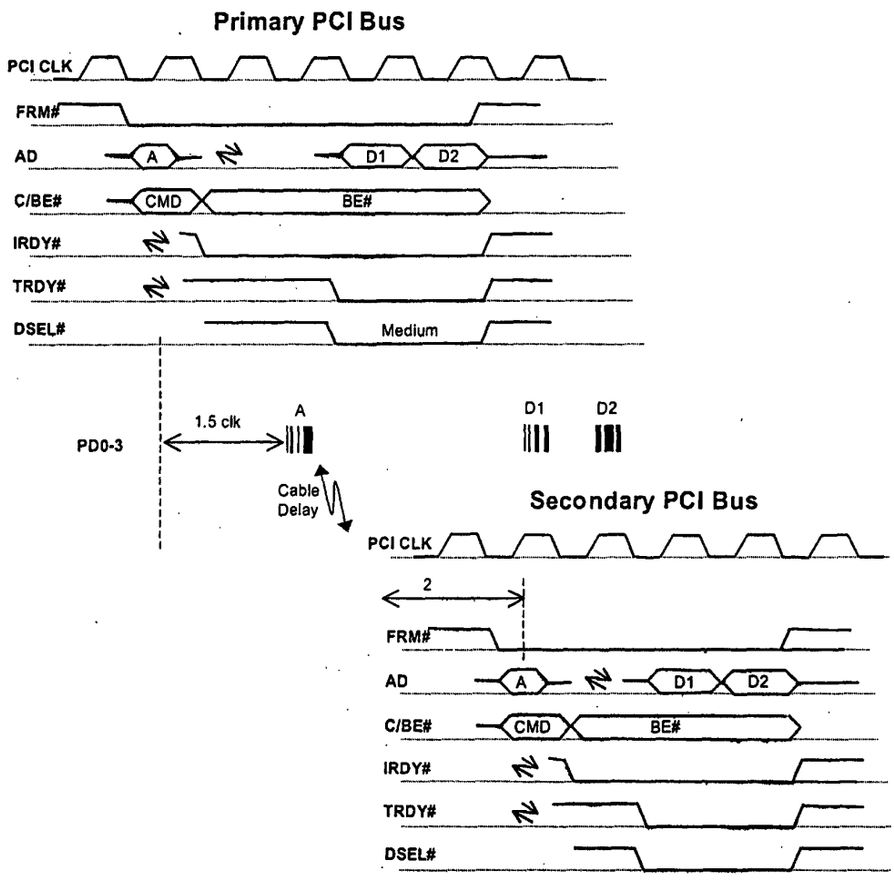

Primary PCI Bus
PCI CLK
FRM#
AD
A
D1
D2
C/BE#
CMD
BE#
IRDY#
TRDY#
DSEL#
Medium
PD0-3
1.5 clk
A
D1
D2
Cable Delay
Secondary PCI Bus
PCI CLK
2
FRM#
AD
A
D1
D2
C/BE#
CMD
BE#
IRDY#
TRDY#
DSEL#

FIG. 10

11 / 57

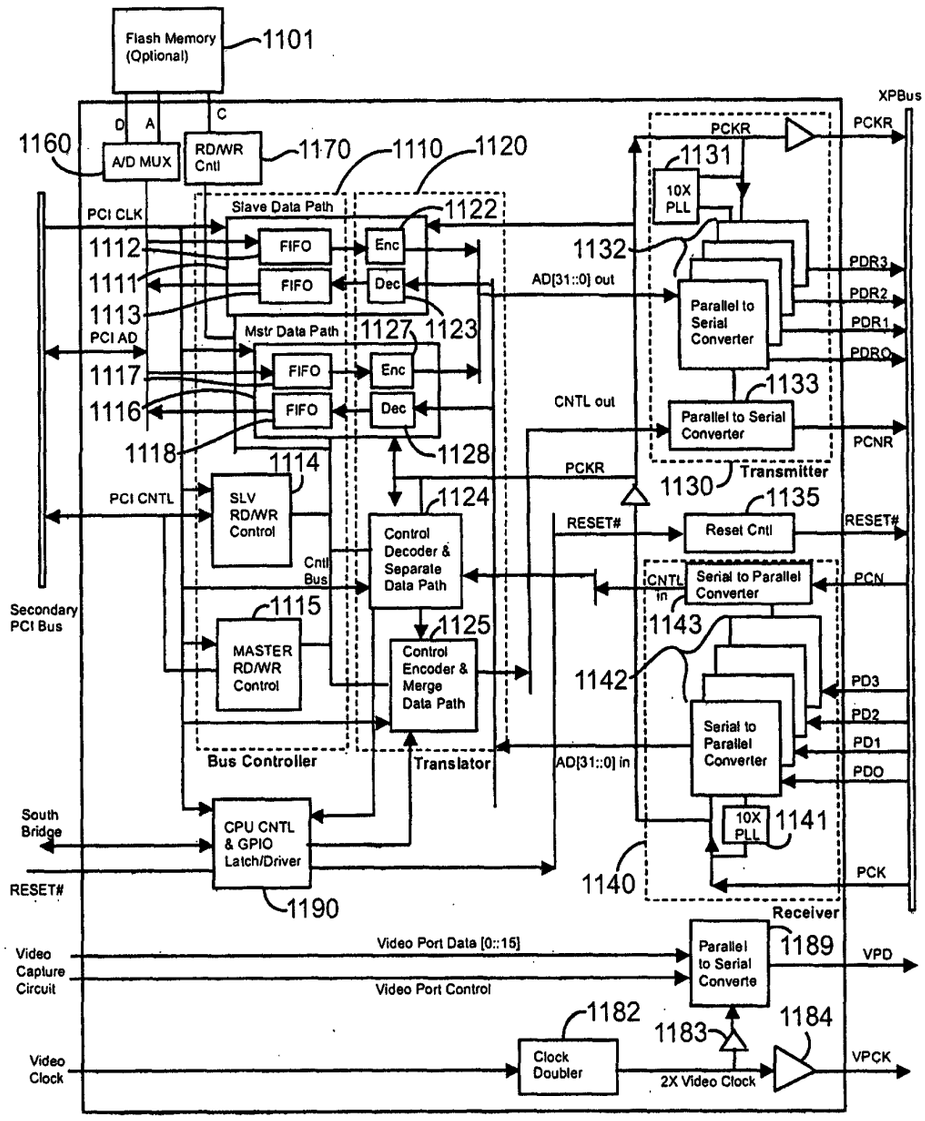

Flash Memory (Optional)
1101
XPBus
D
A
C
1160
A/D MUX
RD/WR Cntl
1170
1110
1120
PCKR
1131
10X PLL
PCI CLK
Slave Data Path
1122
1112
FIFO
Enc
1132
PDR3
1111
FIFO
Dec
AD[31::0] out
Parallel to Serial Converter
PDR2
1113
PDR1
PCI AD
Mstr Data Path
1127
1123
PDR0
1117
FIFO
Enc
1133
1116
FIFO
Dec
CNTL out
Parallel to Serial Converter
1118
1128
PCNR
1114
PCKR
Transmitter
1130
PCI CNTL
SLV RD/WR Control
1124
1135
Control Decoder & Separate Data Path
RESET#
Reset Cntl
RESET#
Cntl Bus
CNTL in
Serial to Parallel Converter
PCN
Secondary PCI Bus
1115
1143
MASTER RD/WR Control
1125
Control Encoder & Merge Data Path
1142
PD3
Serial to Parallel Converter
PD2
PD1
Bus Controller
Translator
AD[31::0] in
PDO
South Bridge
CPU CNTL & GPIO Latch/Driver
10X PLL
1141
RESET#
1190
1140
PCK
Receiver
Video Port Data [0::15]
Parallel to Serial Converte
1189
VPD
Video Capture Circuit
Video Port Control
1182
1183
1184
Video Clock
Clock Doubler
2X Video Clock
VPCK

FIG. 11

PIC as Target

Control Signal	PIC to XPBus	XPBus to PIC	Secondary PCI Bus	Comment
FRAME #	Encode (BS0)		Transaction Active	
IRDY #	Encode (BS1)		Initiator Ready	
TRDY #	Local		PIC Generates	
DEVSEL #	Local		PIC Accepts Command	Positive decode, medium
STOP #	Local	Decode	PIC requests to retry	Host can stop trans.
PAR	Encode	Decode	Parity for A/C; D/BE	
IDSEL	Local		Used locally for config. 0	
PERR #	Encode	Decode	Data Parity Error	
SERR #	Encode	Decode	Address/System Parity Error	
REQ #		Decode	PIC requests to be master	P. Bus device requests bus
GNT #	Encode		PIC grants bus to itself	
RST				Independent signal

FIG. 12

PIC as Master (Default)

Control Signal	PIC to XPBus	XPBus to PIC	Secondary PCI Bus	Comment
FRAME #		Decode	Transaction Active	
IRDY #		Decode	Initiator Ready	
TRDY #	Local		Receive from Target	
DEVSEL #	Local		Receive from Target	
STOP #	Local/Encode		Receive from Target	Target can stop trans.
PAR	Encode	Decode	Parity for A/C; D/BE	
IDSEL	Local		Used locally for config. 0	
PERR #	Encode	Decode	Data Parity Error	
SERR #	Encode	Decode	Address/System Parity Error	
REQ #		Decode	PIC request to be Master	
GNT #	Encode		Arbiter grant bus to PIC	
RST				Independent signal

FIG. 13

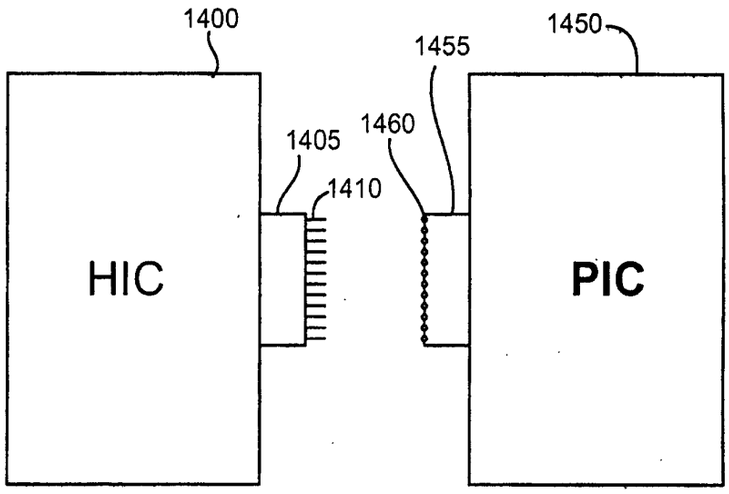


FIG. 14

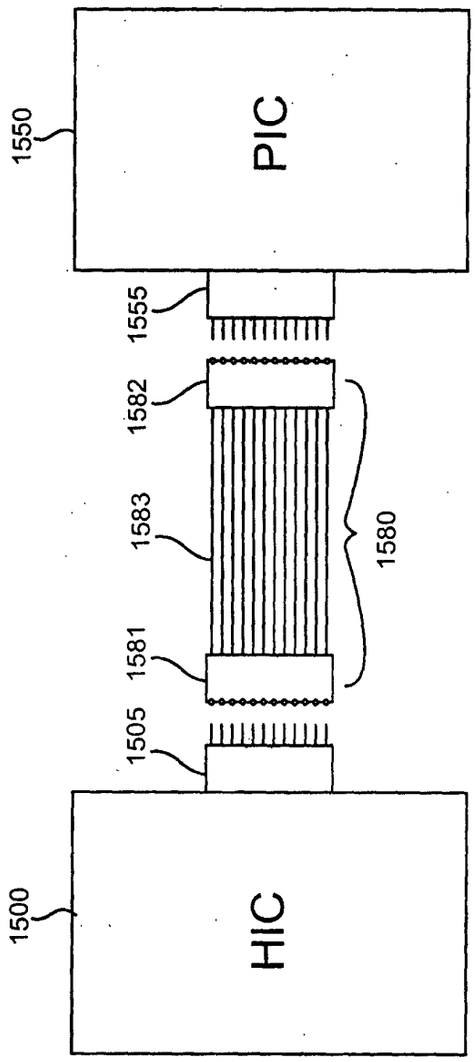


FIG. 15

16 / 57

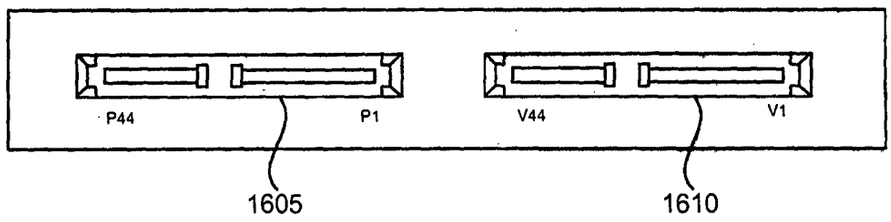


FIG. 16

ACM s XIS BUS Connector Plug PIN Position (88 pin):

V23	GND	V1	P23	GND	GND	P1
V24	P&D D0 +	RED VIDEO	V2	P24	PD0 +	PDR0 +	P2
V25	P&D D0 -	GND	V3	P25	PD0 -	PDR0 -	P3
V26	GND	GREEN VIDEO	V4	P26	GND	GND	P4
V27	P&D CLK +	GND	V5	P27	PD1 +	PDR1 +	P5
V28	P&D CLK -	BLUE VIDEO	V6	P28	PD1 -	PDR1 -	P6
V29	GND	GND	V7	P29	GND	GND	P7
V30	P&D D1 +	HSYNC	V8	P30	PD2 +	PDR2 +	P8
V31	P&D D1 -	VSYNC	V9	P31	PD2 -	PDR2 -	P9
V32	GND	GND	V10	P32	GND	GND	P10
V33	P&D D2 +	DDC2: SCL	V11	P33	PCK +	PCKR +	P11
V34	P&D D2 -	DDC2: SDA	V12	P34	PCK -	PCKR -	P12
V35	Config 3	Config 2	V13	P35	Config 1	Config 0	P13
V36	GND	TV CV/CNTL0	V14	P36	GND	GND	P14
V37	VPCK +	SV Y/CNTL1	V15	P37	PD3 +	PDR3 +	P15
V38	VPCK -	SV C/CNTL2	V16	P38	PD3 -	PDR3 -	P16
V39	GND	V33	V17	P39	GND	GND	P17
V40	VPD +	V33	V18	P40	PCN +	PCNR +	P18
V41	VPD -	V33	V19	P41	PCN -	PCNR -	P19
V42	GND	V33	V20	P42	Reserved	V5	P20
V43	GND	V33	V21	P43	Reserved	V5	P21
V44	GND	V33	V22	P44	Reserved	V5	P22

FIG. 17

Pin No.	Symbol	Signal	Standard	Description
P2	PDR0 +	LVDS		Peripheral data reverse 0 +
P3	PDR0 -	LVDS		Peripheral data reverse 0 -
P5	PDR1 +	LVDS		Peripheral data reverse 1 +
P6	PDR1 -	LVDS		Peripheral data reverse 1 -
P8	PDR2 +	LVDS		Peripheral data reverse 2 +
P9	PDR2 -	LVDS		Peripheral data reverse 2 -
P11	PCKR +	LVDS		Peripheral clock reverse +
P12	PCKR -	LVDS		Peripheral clock reverse -
P15	PDR3 +	LVDS		Peripheral data reverse 3 +
P16	PDR3 -	LVDS		Peripheral data reverse 3 -
P18	PCNR +	LVDS		Peripheral control reverse +
P19	PCNR -	LVDS		Peripheral control reverse -
P24	PD0 +	LVDS		Peripheral data 0 +
P25	PD0 -	LVDS		Peripheral data 0 -
P27	PD1 +	LVDS		Peripheral data 1 +
P28	PD1 -	LVDS		Peripheral data 1 -
P30	PD2 +	LVDS		Peripheral data 2 +
P31	PD2 -	LVDS		Peripheral data 2 -
P33	PCK +	LVDS		Peripheral clock +
P34	PCK -	LVDS		Peripheral clock -
P37	PD3 +	LVDS		Peripheral data 3 +
P38	PD3 -	LVDS		Peripheral data 3 -
P40	PCN +	LVDS		Peripheral control +
P41	PCN -	LVDS		Peripheral Control -
P13	Config 0	Static	3.3v or GND	Configuration bit 0
P35	Config 1	Static	3.3v or GND	Configuration bit 1
P1,P4,P7,P10,				
P14,P17,P23,P26,				
P29,P32,P36,P39	GND		GND	Ground

FIG. 18

Pin No.	Symbol	Signal	Standard	Description
V2	Red Video	Analog		Video
V4	Green Video	Analog		Video
V6	Blue Video	Analog		Video
V8	HSYNC			Horizontal Sync
V9	VSYNC			Vertical Sync
V11	DDC2 SCL		VESA DDC std 2	DDC Clock
V12	DDC2 SDA		VESA DDC std 2	DDC Data
V14	TV-CV/CNTL 0			TV Composite Video
V15	SV Y/CNTL 1		Super Video	SV Luminance or Control 1
V16	SV C/CNTL 2		Super Video	SV Chrominance or Control 2
V24	D0 +	TMDS	VESA P & D	Data 0 +
V25	D0 -	TMDS	VESA P & D	Data 0 -
V27	CLK +	TMDS	VESA P & D	Clock +
V28	CLK -	TMDS	VESA P & D	Clock -
V30	D1 +	TMDS	VESA P & D	Data 1 +
V31	D1 -	TMDS	VESA P & D	Data 1 -
V33	D2 +	TMDS	VESA P & D	Data 2 +
V34	D2 -	TMDS	VESA P & D	Data 2 -
V37	VPCK +	LVDS		Video Port Pixel Clock +
V38	VPCK -	LVDS		Video Port Pixel Clock -
V40	VPD +	LVDS		Video Port Pixel Data +
V41	VPD -	LVDS		Video Port Pixel Data -
V13	Config 2		3.3v or GND	Configuration bit 2
V35	Config 3		3.3v or GND	Configuration bit 3
V1,V3,V5,V7, V10,V23,V26, V29,V32,V36, V39,V42,V43, V44	GND		GND	Ground

FIG. 19

20 / 57

	Symbol	Signal	Data Rate	Description
1	PD0 RTN			GND
2	PD0 +	Synch. To PCK	10 x clock rate	Computer to Peripheral LVDS Data 0 +
3	PD0 -			Computer to Peripheral LVDS Data 0 -
4	PD1 RTN			GND
5	PD1 +	Synch. To PCK	10 x clock rate	Computer to Peripheral LVDS Data 1 +
6	PD1 -			Computer to Peripheral LVDS Data 1 -
7	PD2 RTN			GND
8	PD2 +	Synch. To PCK	10 x clock rate	Computer to Peripheral LVDS Data 2 +
9	PD2 -			Computer to Peripheral LVDS Data 2 -
10	PD3 RTN			GND
11	PD3 +	Synch. To PCK	10 x clock rate	Computer to Peripheral LVDS Data 3 +
12	PD3 -			Computer to Peripheral LVDS Data 3 -
13	PCK RTN			GND
14	PCK +	Clock	Clock rate	Computer to Peripheral LVDS Clock +
15	PCK -			Computer to Peripheral LVDS Clock -
16	PCN RTN			GND
17	PCN +	Synch. To PCK	10 x clock rate	Computer to Peripheral LVDS Control +
18	PCN -			Computer to Peripheral LVDS Control -
19	PDR0 RTN			GND
20	PDR0 +	Synch. To PCKR	10 x clock rate	Peripheral to Computer LVDS Data 0 +
21	PDR0 -			Peripheral to Computer LVDS Data 0 -
22	PDR1 RTN			GND
23	PDR1 +	Synch. To PCKR	10 x clock rate	Peripheral to Computer LVDS Data 1 +
24	PDR1 -			Peripheral to Computer LVDS Data 1 -
25	PDR2 RTN			GND
26	PDR2 +	Synch. To PCKR	10 x clock rate	Peripheral to Computer LVDS Data 2 +
27	PDR2 -			Peripheral to Computer LVDS Data 2 -
28	PDR3 RTN			GND
29	PDR3 +	Synch. To PCKR	10 x clock rate	Peripheral to Computer LVDS Data 3 +
30	PDR3 -			Peripheral to Computer LVDS Data 3 -
31	PCKR RTN			GND
32	PCKR +	Reverse Dir. Clock	Clock rate	Peripheral to Computer LVDS Clock +
33	PCKR -			Peripheral to Computer LVDS Clock -
34	PCNR RTN			GND
35	PCNR +	Synch. To PCKR	10 x Clock rate	Peripheral to Computer LVDS Control +
36	PCNR -			Peripheral to Computer LVDS Control -
37	RESET#		Asynchronous	Reset

FIG. 20

PCK	CK+	CK+	CK+	CK+	CK-	CK-	CK-	CK-	CK+	CK+	CK+	CK+	CK+	CK+	CK-	CK-	CK-	CK-	CK-
PD0	BS0	CM0#	A00	A01	A02	A03	A04	A05	A06	A07	BS0	BE0#	D00	D01	D02	D03	D04	D05	D06	D07
PD1	BS1	CM1#	A08	A09	A10	A11	A12	A13	A14	A15	BS1	BE1#	D08	D09	D10	D11	D12	D13	D14	D15
PD2	BS2	CM2#	A16	A17	A18	A19	A20	A21	A22	A23	BS2	BE2#	D16	D17	D18	D19	D20	D21	D22	D23
PD3	BS3	CM3#	A24	A25	A26	A27	A28	A29	A30	A31	BS3	BE3#	D24	D25	D26	D27	D28	D29	D30	D31
PCN	CN0	CN1	CN2	CN3	CN4	CN5	CN6	CN7	CN8	CN9	CN0	CN1	CN2	CN3	CN4	CN5	CN6	CN7	CN8	CN9

FIG. 21

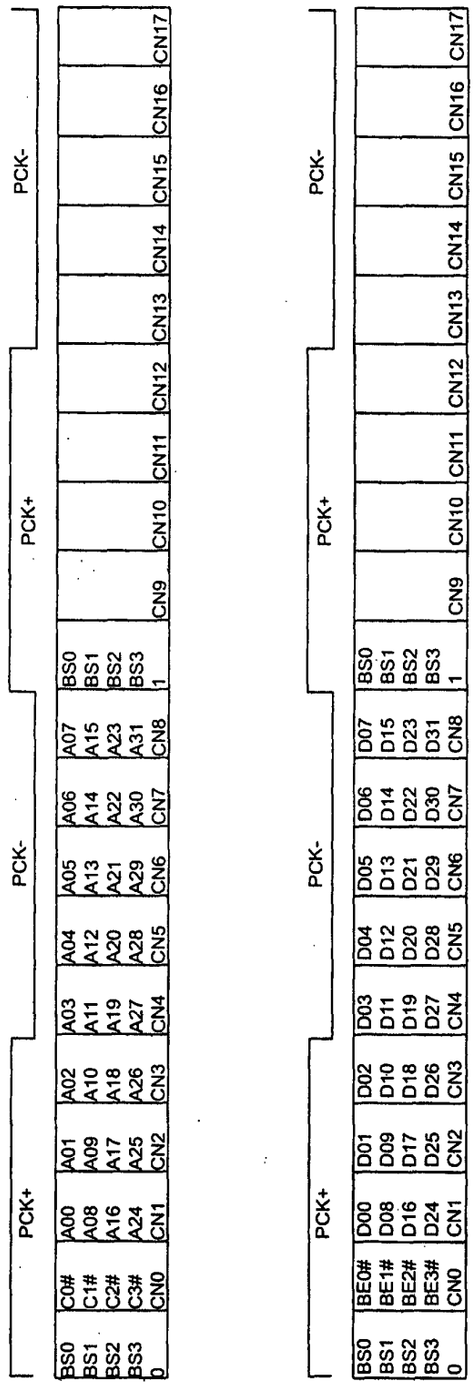

PCK+
PCK-
PCK+
PCK-
BS0 C0# A00 A01 A02 A03 A04 A05 A06 A07 BS0
BS1 C1# A08 A09 A10 A11 A12 A13 A14 A15 BS1
BS2 C2# A16 A17 A18 A19 A20 A21 A22 A23 BS2
BS3 C3# A24 A25 A26 A27 A28 A29 A30 A31 BS3
0 CN0 CN1 CN2 CN3 CN4 CN5 CN6 CN7 CN8 1
CN9 CN10 CN11 CN12 CN13 CN14 CN15 CN16 CN17
PCK+
PCK-
PCK+
PCK-
BS0 BE0# D00 D01 D02 D03 D04 D05 D06 D07 BS0
BS1 BE1# D08 D09 D10 D11 D12 D13 D14 D15 BS1
BS2 BE2# D16 D17 D18 D19 D20 D21 D22 D23 BS2
BS3 BE3# D24 D25 D26 D27 D28 D29 D30 D31 BS3
0 CN0 CN1 CN2 CN3 CN4 CN5 CN6 CN7 CN8 1
CN9 CN10 CN11 CN12 CN13 CN14 CN15 CN16 CN17

FIG. 22

23 / 57

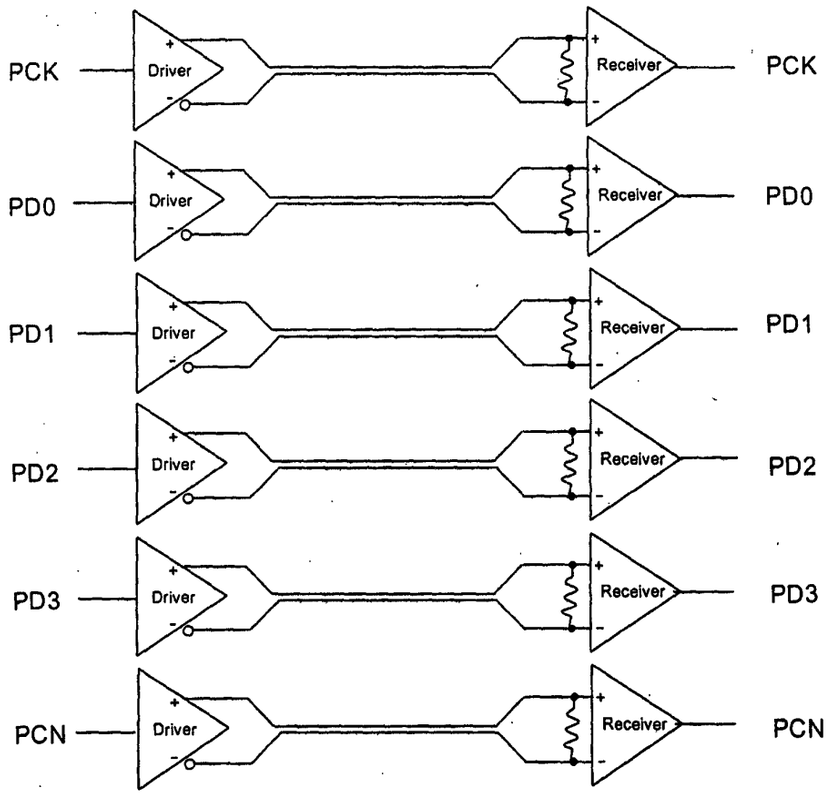

PCK
Driver
Receiver
PCK
PD0
Driver
Receiver
PD0
PD1
Driver
Receiver
PD1
PD2
Driver
Receiver
PD2
PD3
Driver
Receiver
PD3
PCN
Driver
Receiver
PCN

FIG. 23

24 / 57

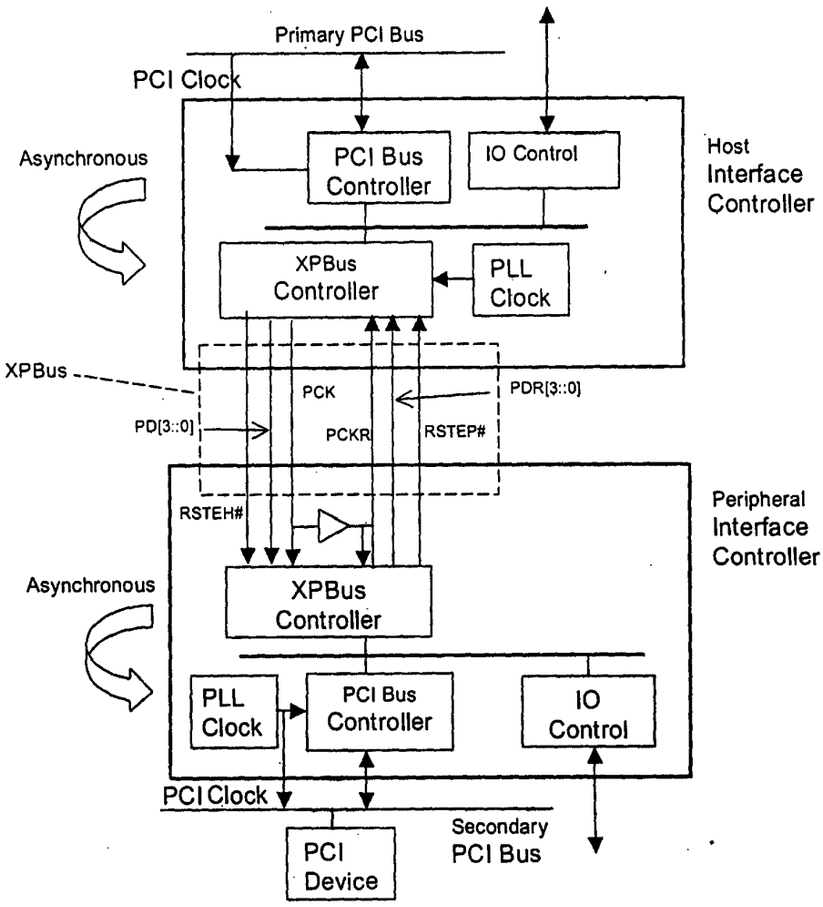

Primary PCI Bus
PCI Clock
Asynchronous
PCI Bus Controller
IO Control
Host Interface Controller
XPBus Controller
PLL Clock
XPBus
PCK
PDR[3::0]
PD[3::0]
PCKR
RSTEP#
RSTEH#
Peripheral Interface Controller
Asynchronous
XPBus Controller
PLL Clock
PCI Bus Controller
IO Control
PCI Clock
Secondary PCI Bus
PCI Device

FIG. 24

25 / 57

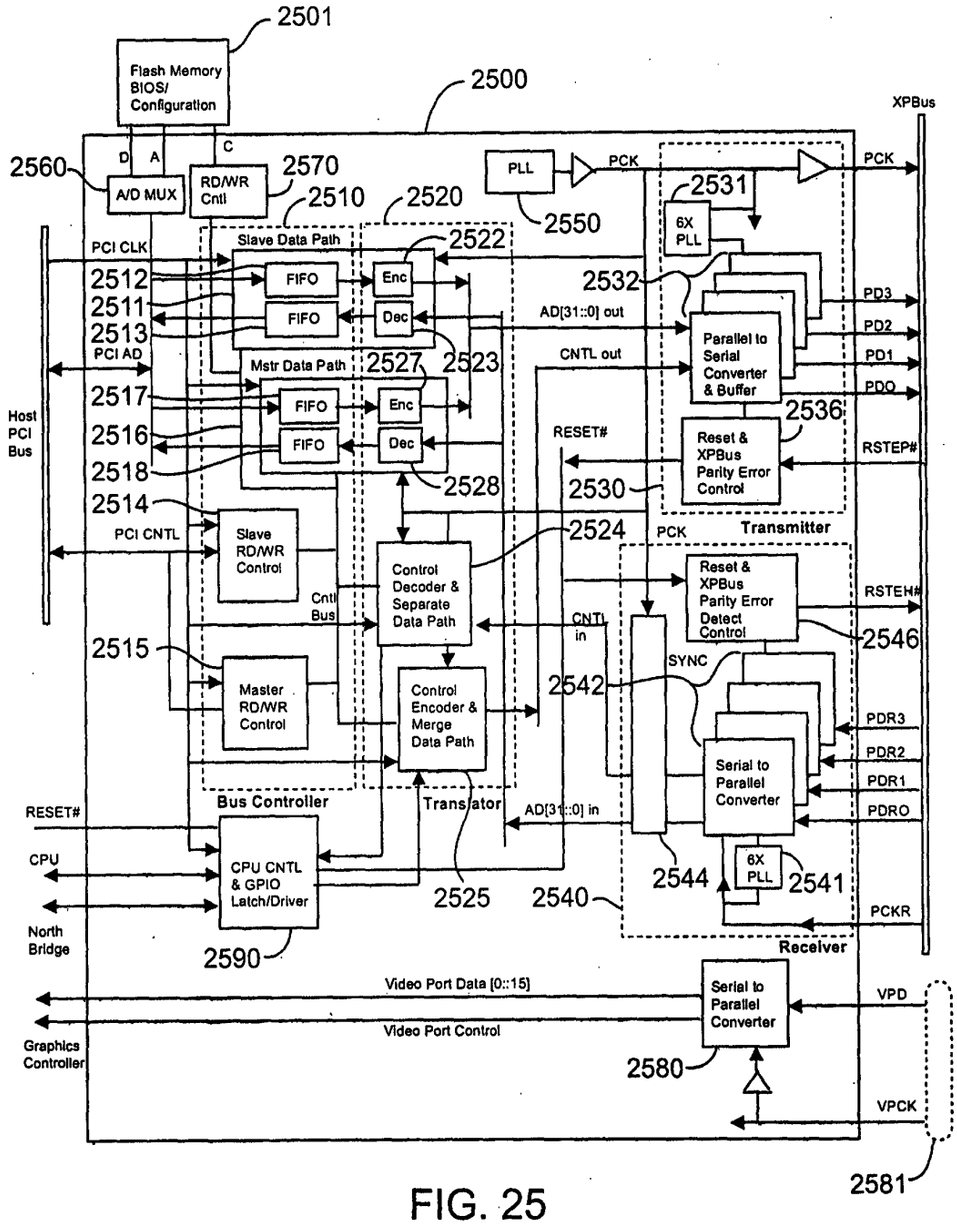

2501
Flash Memory BIOS/ Configuration
2500
XPBus
2560
D
A
C
A/D MUX
RD/WR Cntl
2570
2510
2520
PLL
PCK
2550
2531
6X PLL
PCK
PCI CLK
Slave Data Path
2522
2512
FIFO
Enc
2532
2511
FIFO
Dec
AD[31::0] out
PD3
PD2
2513
PCI AD
Mstr Data Path
2527
2523
CNTL out
Parallel to Serial Converter & Buffer
PD1
PDO
2517
FIFO
Enc
2536
Host PCI Bus
2516
FIFO
Dec
RESET#
Reset & XPBus Parity Error Control
RSTEP#
2518
2528
2530
2514
PCI CNTL
Slave RD/WR Control
2524
PCK
Transmitter
Control Decoder & Separate Data Path
Reset & XPBus Parity Error Detect Control
RSTEH#
Cntl Bus
CNTL in
2546
2515
SYNC
2542
Master RD/WR Control
Control Encoder & Merge Data Path
PDR3
PDR2
Serial to Parallel Converter
PDR1
PDRO
RESET#
Bus Controller
Translator
AD[31::0] in
CPU
CPU CNTL & GPIO Latch/Driver
2544
6X PLL
2541
2525
2540
PCKR
North Bridge
Receiver
2590
Video Port Data [0::15]
Serial to Parallel Converter
VPD
Graphics Controller
Video Port Control
2580
VPCK
2581

FIG. 25

26 / 57

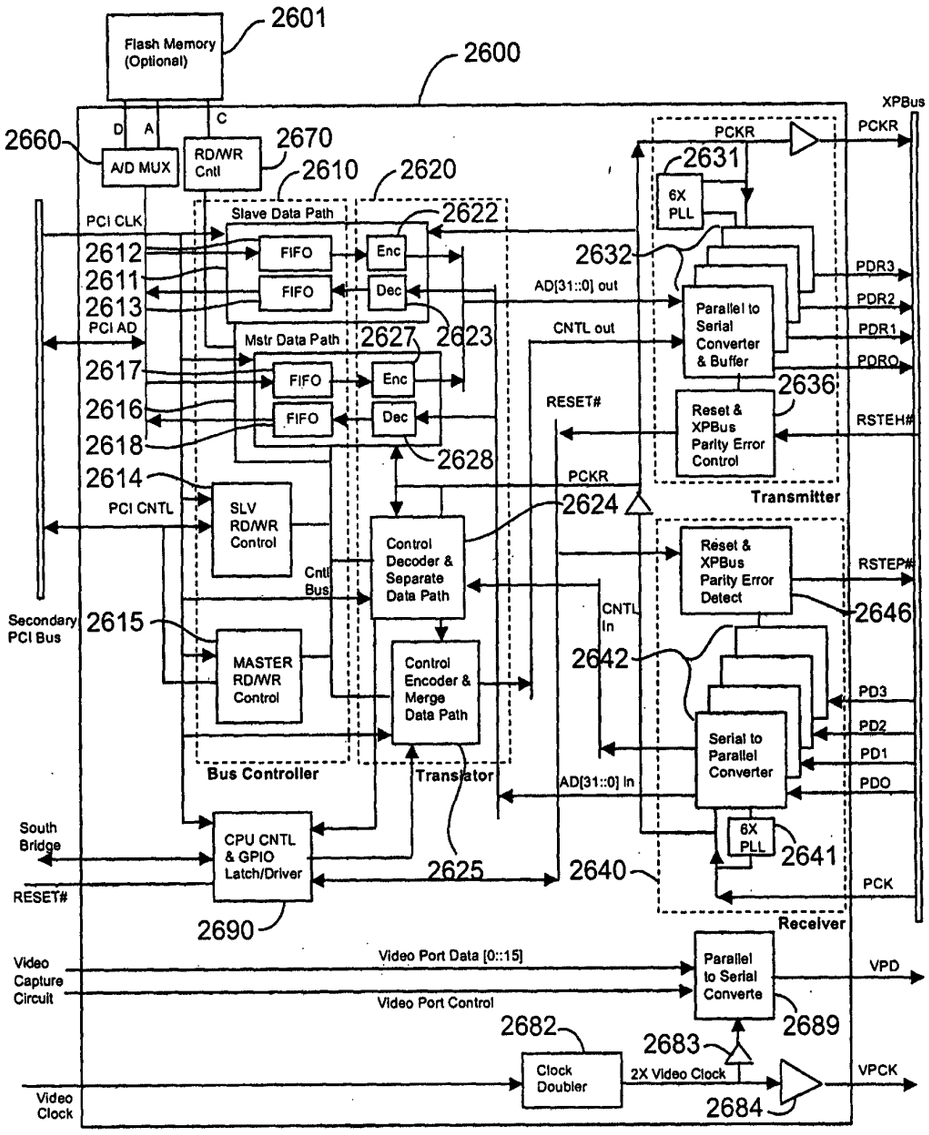

Flash Memory (Optional)
2601
2600
D
A
C
2660
A/D MUX
RD/WR Cntl
2670
2610
2620
PCI CLK
Slave Data Path
2622
2612
2611
2613
PCI AD
FIFO
Enc
Dec
Mstr Data Path
2627
2623
2617
2616
2618
2628
2614
PCI CNTL
SLV RD/WR Control
Control Decoder & Separate Data Path
Cntl Bus
Secondary PCI Bus
2615
MASTER RD/WR Control
Control Encoder & Merge Data Path
Bus Controller
Translator
South Bridge
RESET#
CPU CNTL & GPIO Latch/Driver
2625
2690
XPBus
PCKR
2631
6X PLL
2632
AD[31::0] out
CNTL out
Parallel to Serial Converter & Buffer
PDR3
PDR2
PDR1
PDR0
2636
RESET#
Reset & XPBus Parity Error Control
RSTEH#
Transmitter
2624
Reset & XPBus Parity Error Detect
RSTEP#
2646
CNTL In
2642
PD3
PD2
PD1
PDO
Serial to Parallel Converter
AD[31::0] In
6X PLL
2641
2640
PCK
Receiver
Video Capture Circuit
Video Port Data [0::15]
Video Port Control
Parallel to Serial Converte
VPD
2689
2682
2683
Clock Doubler
2X Video Clock
VPCK
2684
Video Clock

FIG. 26

27 / 57

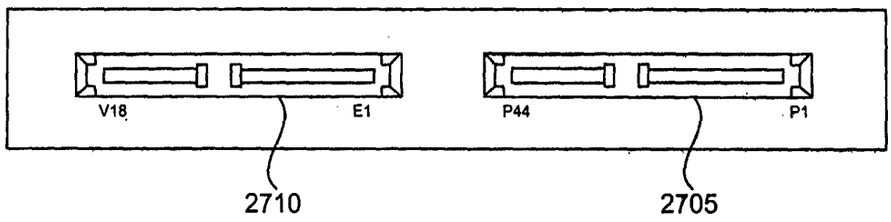


FIG. 27

ACM s CMI BUS Connector Plug PIN Position (88 pin):

E14	GND	GND	E1		P23	GND	GND	P1
E15	P&D D0 +	TPA+ /VPD+	E2		P24	PD0 +	PDR0 +	P2
E16	P&D D0 -	TPA- /VPD-	E3		P25	PD0 -	PDR0 -	P3
E17	GND	GND	E4		P26	GND	GND	P4
E18	P&D CLK +	TPB+ /VPCK+	E5		P27	PD1 +	PDR1 +	P5
E19	P&D CLK -	TPB- /VPCK-	E6		P28	PD1 -	PDR1 -	P6
E20	GND	1394 Detect	E7		P29	GND	GND	P7
E21	P&D D1 +	Reserved	E8		P30	PD2 +	PDR2 +	P8
E22	P&D D1 -	Reserved	E9		P31	PD2 -	PDR2 -	P9
E23	GND	Reserved	E10		P32	GND	GND	P10
E24	P&D D2 +	Reserved	E11		P33	PCK +	PCKR +	P11
E25	P&D D2 -	Reserved	E12		P34	PCK -	PCKR -	P12
E26	DFP Detect	Config 2	E13		P35	Config 1	Config 0	P13
V10	GND	V33	V1		P36	GND	GND	P14
V11	GND	V33	V2		P37	PD3 +	PDR3 +	P15
V12	GND	V33	V3		P38	PD3 -	PDR3 -	P16
V13	V33	V33	V4		P39	RSTEH#	RSTEP#	P17
V14	V33	V33	V5		P40	GREEN VIDEO	RED VIDEO	P18
V15	V33	V33	V6		P41	GND	GND	P19
V16	V5	V12	V7		P42	HSYNC	BLUE VIDEO	P20
V17	V5	V12	V8		P43	VSYNC	GND	P21
V18	V5	V12	V9		P44	DDC2: SCL	DDC2: SDA	P22

FIG. 28

Pin No.	Symbol	Signal	Standard	Description
P2	PDR0 +	LVDS		Peripheral data reverse 0 +
P3	PDR0 -	LVDS		Peripheral data reverse 0 -
P5	PDR1 +	LVDS		Peripheral data reverse 1 +
P6	PDR1 -	LVDS		Peripheral data reverse 1 -
P8	PDR2 +	LVDS		Peripheral data reverse 2 +
P9	PDR2 -	LVDS		Peripheral data reverse 2 -
P11	PCKR +	LVDS		Peripheral clock reverse +
P12	PCKR -	LVDS		Peripheral clock reverse -
P15	PDR3 +	LVDS		Peripheral data reverse 3 +
P16	PDR3 -	LVDS		Peripheral data reverse 3 -
P24	PD0 +	LVDS		Peripheral data 0 +
P25	PD0 -	LVDS		Peripheral data 0 -
P27	PD1 +	LVDS		Peripheral data 1 +
P28	PD1 -	LVDS		Peripheral data 1 -
P30	PD2 +	LVDS		Peripheral data 2 +
P31	PD2 -	LVDS		Peripheral data 2 -
P33	PCK +	LVDS		Peripheral clock +
P34	PCK -	LVDS		Peripheral clock -
P37	PD3 +	LVDS		Peripheral data 3 +
P38	PD3 -	LVDS		Peripheral data 3 -
P13	Config 0	Static	3.3v or GND	Configuration bit 0
P35	Config 1	Static	3.3v or GND	Configuration bit 1
P17	RESTEP#	TTL	3.3v	Reset and Parity Error from console to ACM
P39	RESTEH#	TTL	3.3v	Reset and Parity Error from ACM to console
P18	Red Video	Analog		Video
P40	Green Video	Analog		Video
P20	Blue Video	Analog		Video
P42	HSYNC	TTL		Horizontal Sync
P43	VSYNC	TTL		Vertical Sync
P44	DDC2 SCL	TTL	VESA DDC std 2	DDC Clock
P22	DDC2 SDA	TTL	VESA DDC std 2	DDC Data
P1,P4,P7,P10, P14,P19,P21, P23,P26,P29, P32,P36,P41	GND		GND	Ground

FIG. 29

Pin No.	Symbol	Signal	Standard	Description
E2	VPD+/TPA+		LVDS or 1394	Video capture port data or 1394
E3	VPD-/TPA-		LVDS or 1394	Video capture port data or 1394
E5	VPCK+/TPA+		LVDS or 1394	Video capture port data or 1394
E6	VPCK-/TPA-		LVDS or 1394	Video capture port data or 1394
E15	D0 +	TMDS	VESA P & D	Data 0 +
E16	D0 -	TMDS	VESA P & D	Data 0 -
E18	CLK +	TMDS	VESA P & D	Clock +
E19	CLK -	TMDS	VESA P & D	Clock -
E21	D1 +	TMDS	VESA P & D	Data 1 +
E22	D1 -	TMDS	VESA P & D	Data 1 -
E24	D2 +	TMDS	VESA P & D	Data 2 +
E25	D2 -	TMDS	VESA P & D	Data 2 -
E13	Config 2			Configuration bit 2
E26	Config 3			Configuration bit 3
E1, E4, E14, E17,E20,E23	GND		GND	Ground

E7	Reserved			Reserved
E8	Reserved			Reserved
E9	Reserved			Reserved
E10	TV-CV/reserved		NTSC	TV Composite Video or reserved
E11	SV Y/reserved		Super Video	SV Luminance or reserved
E12	SV C/reserved		Super Video	SV Chrominance or reserved

FIG. 30

	Symbol	Signal	Data Rate	Description
1	PD0 RTN			GND
2	PD0 +	Synch. To PCK	6 x clock rate	Computer to Peripheral LVDS Data 0 +
3	PD0 -			Computer to Peripheral LVDS Data 0 -
4	PD1 RTN			GND
5	PD1 +	Synch. To PCK	6 x clock rate	Computer to Peripheral LVDS Data 1 +
6	PD1 -			Computer to Peripheral LVDS Data 1 -
7	PD2 RTN			GND
8	PD2 +	Synch. To PCK	6 x clock rate	Computer to Peripheral LVDS Data 2 +
9	PD2 -			Computer to Peripheral LVDS Data 2 -
10	PD3 RTN			GND
11	PD3 +	Synch. To PCK	6 x clock rate	Computer to Peripheral LVDS Data 3 +
12	PD3 -			Computer to Peripheral LVDS Data 3 -
13	PCK RTN			GND
14	PCK +	Clock	Clock rate	Computer to Peripheral LVDS Clock +
15	PCK -			Computer to Peripheral LVDS Clock -
16	PDR0 RTN			GND
17	PDR0 +	Synch. To PCKR	6 x clock rate	Peripheral to Computer LVDS Data 0 +
18	PDR0 -			Peripheral to Computer LVDS Data 0 -
19	PDR1 RTN			GND
20	PDR1 +	Synch. To PCKR	6 x clock rate	Peripheral to Computer LVDS Data 1 +
21	PDR1 -			Peripheral to Computer LVDS Data 1 -
22	PDR2 RTN			GND
23	PDR2 +	Synch. To PCKR	6 x clock rate	Peripheral to Computer LVDS Data 2 +
24	PDR2 -			Peripheral to Computer LVDS Data 2 -
25	PDR3 RTN			GND
26	PDR3 +	Synch. To PCKR	6 x clock rate	Peripheral to Computer LVDS Data 3 +
27	PDR3 -			Peripheral to Computer LVDS Data 3 -
28	PCKR RTN			GND
29	PCK +	Reverse Dir. Clock	Clock rate	Peripheral to Computer LVDS Clock +
30	PCK -			Peripheral to Computer LVDS Clock -
31	RESTEH#	Host to Peripheral	asynchronous	Reset & Error signal
32	RESTEP#	Peripheral to Host	asynchronous	Reset & Error signal

FIG. 31

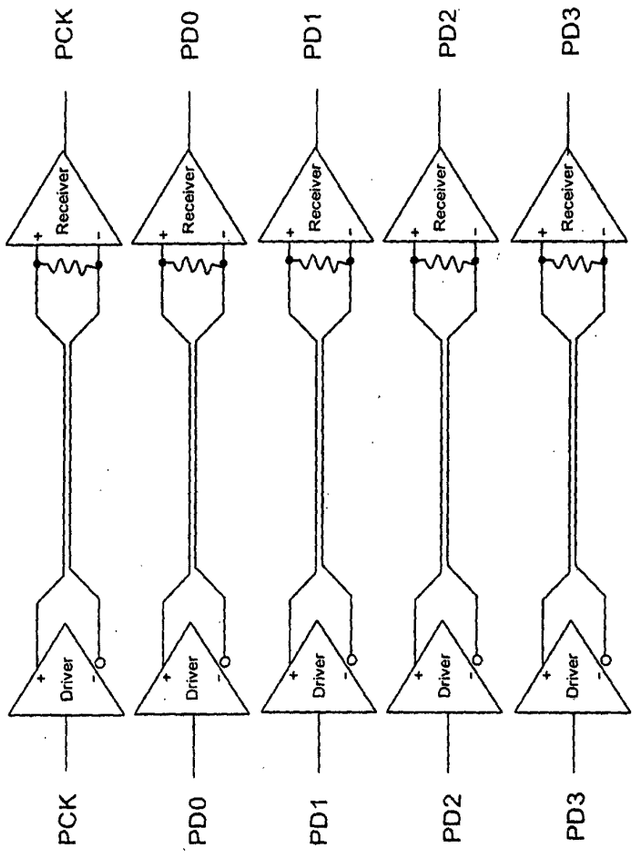


FIG. 32

Master	Type	HMA1/HMD1	HMA2/HMD2	HMC1	HMC2	Resvd	NOOP
	1st nibble	XX00 (PCI)	XX10 (PCI)	1001 (Control)	1101 (Control)	X011	1111
	2nd nibble	C/BE	Control bits	Control bits	Control bits		
	3rd to 6th	PCI A/D 1st seg.	PCI A/D 2nd seg.	Control 1st seg.	Control 2nd seg.	Other	Void
Target	Type	HTD1	HTD2	HTC1	HTC2	Resrd	NOOP
	1st nibble	XX00	XX10	0001 (Control)	0101 (Control)	X011	1111
	2nd nibble	BE	Control bits	Control bits	Control bits		
	3rd to 6th	PCI D 1st seg.	PCI D 2nd seg.	Control 1st seg.	Control 2nd seg.	Other	Void

FIG. 33

Master	Type	PMA1 / PMD1	PMA2 / PMD2	PMC1	PMC2	Resvd	NOOP
	1st nibble	XX00 (PCI)	XX10 (PCI)	X001(Control)	X101(Control)	XX11	1111
	2nd nibble	C/BE	Control bits	Control bits	Control bits		
	3rd to 6th	PCI A/D 1st seg.	PCI A/D 2nd seg.	Control 1st seg.	Control 2nd seg.	Other	Void
Target	Type	PTD1	PTD2	PTC1	PTC2	Resvd	NOOP
	1st nibble	XX00	XX10	X001(Control)	X101 (Control)	XX11	1111
	2nd nibble	BE	Control bits	Control bits	Control bits		
	3rd to 6th	PCI D 1st seg.	PCI D 2nd seg.	Control 1st seg.	Control 2nd seg.	Other	Void

FIG. 34

ID bits (P0 P1 P2 P3)	Data Packet Type
X X 0 0	PCI 1st address/data segment
X X 1 0	PCI 2nd address/data segment
0 0 0 1	Control 1st segment with PCI response
1 0 0 1	Control 1st segment without PCI response
0 1 0 1	Control 2nd segment with PCI response
1 1 0 1	Control 2nd segment without PCI response
0 0 1 1	Reserved
1 0 1 1	Reserved
0 1 1 1	Initialization
1 1 1 1	NOOP

FIG. 35

	PD0	PD1	PD2	PD3
1st control /ID (HMA1 or HMD1)	FRAME#	IRDY#	0: 1st data seg.	0: PCI; Other=1
2nd control	C/BE0#	C/BE1#	C/BE2#	C/BE3#
1st Data Segment	A/D0	A/D8	A/D16	A/D24
1st Data Segment	A/D1	A/D9	A/D17	A/D25
1st Data Segment	A/D2	A/D10	A/D18	A/D26
1st Data Segment	A/D3	A/D11	A/D19	A/D27
3rd control /ID (HMA2 or HMD2)	PAR (PCI)	LOCK#	1: 2nd data seg.	0: PCI; Other=1
4th control	GNT#	reserved	reserved	Cntl PAR (CMI)
2nd Data Segment	A/D4	A/D12	A/D20	A/D28
2nd Data Segment	A/D5	A/D13	A/D21	A/D29
2nd Data Segment	A/D6	A/D14	A/D22	A/D30
2nd Data Segment	A/D7	A/D15	A/D23	A/D31

FIG. 36

37 / 57

	PD0	PD1	PD2	PD3
1st control /ID **(PMA1 or PMD1)**	FRAME#	IRDY#	0: 1st data seg.	0: PCI; Other=1
2nd control	C/BE0#	C/BE1#	C/BE2#	C/BE3#
1st Data Segment	A/D0	A/D8	A/D16	A/D24
1st Data Segment	A/D1	A/D9	A/D17	A/D25
1st Data Segment	A/D2	A/D10	A/D18	A/D26
1st Data Segment	A/D3	A/D11	A/D19	A/D27
3rd control /ID **(PMA2 or PMD2)**	PAR (PCI)	LOCK#	1: 2nd data seg.	0: PCI; Other=1
4th control	GNT#	reserved	reserved	Cntl PAR (CMI)
2nd Data Segment	A/D4	A/D12	A/D20	A/D28
2nd Data Segment	A/D5	A/D13	A/D21	A/D29
2nd Data Segment	A/D6	A/D14	A/D22	A/D30
2nd Data Segment	A/D7	A/D15	A/D23	A/D31

FIG. 37

	PD0	PD1	PD2	PD3
1st control /ID (HTD1 or PTD1)	1	1	0: 1st data seg.	0: PCI; Other=1
2nd control	reserved	reserved	reserved	reserved
1st Data Segment	D0	D8	D16	D24
1st Data Segment	D1	D9	D17	D25
1st Data Segment	D2	D10	D18	D26
1st Data Segment	D3	D11	D19	D27
3rd control /ID (HTD2 or PTD2)	PAR (PCI)	reserved	1: 2nd data seg.	0: PCI; Other=1
4th control	GNT#	reserved	reserved	Cntl PAR (CMI)
2nd Data Segment	D4	D12	D20	D28
2nd Data Segment	D5	D13	D21	D29
2nd Data Segment	D6	D14	D22	D30
2nd Data Segment	D7	D15	D23	D31

FIG. 38

33 Mhz PCI Read transaction:

H > P	HMA1	HMA2	NOOP	NOOP			NOOP	NOOP	HMC1	NOOP
P > H	NOOP	NOOP	PTC1	NOOP			PTD1	PTD2	NOOP	NOOP

FIG. 39

33 Mhz PCI Write transaction:

H > P	HMA1	HMA2	NOOP	NOOP	HMD1	HMD2	NOOP	NOOP	NOOP	HMD1	HMD2	NOOP
P > H	NOOP	NOOP	PTC1	NOOP	NOOP	NOOP	PTC2	NOOP	NOOP	NOOP	NOOP	PTC1

FIG. 40

Peripheral to Host: PCI Target (on XPBus) Control data packets without PCI response :

	PD0	PD1	PD2	PD3
ID (PTC1)	0: PCI	0: 1st control seg.	0: Control	1: Other
PCI Control Segment	PERR#	SERR#	REQ#	STOP#
CMI Control Segment	CMI PERR#	Buffer Full #	CMI REQ#	CMI GNT#
CPU 1st Control Segment	CPURST	INIT	reserved	reserved
CPU 2nd Control Segment	INTR	NMI	A20M#	IGNNE#
CPU 3rd Control Segment	SMI#	STPCLK#	SLP#	PAR (Cntl Packet)

ID (PTC2)	0: PCI	1: 2nd control seg.	0: Control	1: Other
PCI Control Segment	PERR#	SERR#	REQ#	STOP#
CMI Control Segment	CMI PERR#	Buffer Full #	CMI REQ#	CMI GNT#
NB 1st Control Segment	SUSCLK	SUSSTAT1#	PHOLD#	
GPIO 1st Control Segment	GPIO (0)	GPIO (1)	GPIO (2)	GPIO (3)
GPIO 2nd Control Segment	GPIO (4)	GPIO (5)	reserved	PAR (Cntl Packet)

FIG. 41

Peripheral to Host: PCI Target (on XPBus) Control data packets without PCI response :

	PD0	PD1	PD2	PD3
ID (PTC1)	1: No PCI	0: 1st control seg.	0: Control	1: Other
PCI Control Segment	reserved	reserved	reserved	reserved
CMI Control Segment	CMI PERR#	Buffer Full #	CMI REQ#	CMI GNT#
CPU 1st Control Segment	CPURST	INIT	reserved	reserved
CPU 2nd Control Segment	INTR	NMI	A20M#	IGNNE#
CPU 3rd Control Segment	SMI#	STPCLK#	SLP#	PAR (Cntl Packet)

ID (PTC2)	1: No PCI	1: 2nd control seg.	0: Control	1: Other
PCI Control Segment	reserved	reserved	reserved	reserved
CMI Control Segment	CMI PERR#	Buffer Full #	CMI REQ#	CMI GNT#
NB 1st Control Segment	SUSCLK	SUSSTAT1#	PHOLD#	
GPIO 1st Control Segment	GPIO (0)	GPIO (1)	GPIO (2)	GPIO (3)
GPIO 2nd Control Segment	GPIO (4)	GPIO (5)	reserved	PAR (Cntl Packet)

FIG. 42

Peripheral to Host: PCI Master (on XPBus) Control single data packet with PCI response:

	PD0	PD1	PD2	PD3
ID (PMC1)	0: PCI	0: 1st control seg.	0: Control	1: Other
PCI Control Segment	PERR#	SERR#	reserved	reserved
CMI Control Segment	CMI PERR#	Buffer Full #	CMI REQ#	CMI GNT#
CPU 1st Control Segment	CPURST	INIT	reserved	reserved
CPU 2nd Control Segment	INTR	NMI	A20M#	IGNNE#
CPU 3rd Control Segment	SMI#	STPCLK#	SLP#	PAR (Cntl Packet)

ID (PMC2)	0: PCI	1: 2nd control seg.	0: Control	1: Other
PCI Control Segment	PERR#	SERR#	reserved	reserved
CMI Control Segment	CMI PERR#	Buffer Full #	CMI REQ#	CMI GNT#
NB 1st Control Segment	SUSCLK	SUSSTAT1#	PHOLD#	reserved
GPIO 1st Control Segment	GPIO (0)	GPIO (1)	GPIO (2)	GPIO (3)
GPIO 2nd Control Segment	GPIO (4)	GPIO (5)	reserved	PAR (Cntl Packet)

FIG. 43

Peripheral to Host: PCI Master (on XPBus) Control single data packet without PCI response:

	PD0	PD1	PD2	PD3
ID (PMC1)	1: No PCI	0: 1st control seg.	0: Control	1: Other
PCI Control Segment	reserved	reserved	reserved	reserved
CMI Control Segment	CMI PERR#	Buffer Full #	CMI REQ#	CMI GNT#
CPU 1st Control Segment	CPURST	INIT	reserved	reserved
CPU 2nd Control Segment	INTR	NMI	A20M#	IGNNE#
CPU 3rd Control Segment	SMI#	STPCLK#	SLP#	PAR (Cntl Packet)

ID (PMC2)	1: No PCI	1: 2nd control seg.	0: Control	1: Other
PCI Control Segment	reserved	reserved	reserved	reserved
CMI Control Segment	CMI PERR#	Buffer Full #	CMI REQ#	CMI GNT#
NB 1st Control Segment	SUSCLK	SUSSTAT1#	PHOLD#	reserved
GPIO 1st Control Segment	GPIO (0)	GPIO (1)	GPIO (2)	GPIO (3)
GPIO 2nd Control Segment	GPIO (4)	GPIO (5)	reserved	PAR (Cntl Packet)

FIG. 44

Host to Peripheral: Target Control data packet :

	PD0	PD1	PD2	PD3
ID (HTC1)	0: PCI Target	0: 1st segment	0: Control	1: Other
PCI Control Segment	PERR#	SERR#	REQ#	STOP#
CMI Control Segment	CMI PERR#	Buffer Full #	CMI REQ#	CMI GNT#
CPU 1st Control Segment	FERR#	reserved	reserved	reserved
Reserved				
Reserved				

HTC2 is reserved for future use.

FIG. 45

Host to Peripheral: Master Control data packet :

	PD0	PD1	PD2	PD3
ID **(HMC1)**	0: PCI Master	0: 1st segment	0: Control	1: Other
PCI Control Segment	PERR#	SERR#	reserved	reserved
CMI Control Segment	CMI PERR#	Buffer Full #	CMI REQ#	CMI GNT#
CPU 1st Control Segment	FERR#	reserved	reserved	reserved
Reserved				
Reserved				

HMC2 is reserved for future use.

FIG. 46

47 / 57

Name	Type	Pins	Description
AD[31::0]	TS	32	Multiplexed Address/Data. AD is driven to a valid state when GNT# is asserted.
C/BE[3::0]#	TS	4	Multiplexed Command/Byte Enables. For a two-address transaction, 1st address phase carries the command, and the 2nd address phase carries the transaction type. C/BE is driven to a valid state when GNT# is asserted.
FRAME#	STS	1	Indicates beginning and duration of a PCI transaction. When the bus is idle, FRAME# is driven to High for 1 cycle. A pull-up resistor sustains STS signal.
IRDY#	STS	1	Initiator Ready. IRDY# is driven High for 1 cycle if bus is idle, and the state is sustained by a pull-up resistor.
TRDY#	STS	1	Target Ready. When bus is idle, TRDY# is driven High for 1 cycle if bus is idle. An external pull-up resistor sustains STS signal.
DEVSEL#	STS	1	Device Select. DEVSEL# is asserted by target to indicate it is ready to accept the transaction. HIC decodes address of a transaction to decide the need to assert DEVSEL#. As an initiator, HIC waits for 5 cycles to detect assertion of DEVSEL# by the target; otherwise HIC terminates with a master abort. DEVSEL# is driven High for 1 cycle when bus is idle, and the state is sustained by a pull-up resistor.
STOP#	STS	1	Target request to stop transaction. There are 3 cases: STOP#, TRDY# & DEVSEL# asserted: disconnect with data transfer Only STOP# & DEVSEL# asserted: request initiator to retry later Only STOP# asserted: target abort STOP# is driven High for 1 cycle when bus is idle, and the state is sustained by a pull-up resistor.
PAR	TS	1	Even parity for 36 bits of AD & C/BE#. PAR is sent one cycle after address or data is valid. In write transaction, initiator sends PAR one cycle after write data is valid. In read transaction, target sends PAR one cycle after read data is valid.
LOCK#	Input	1	Initiator request lock on target downstream. LOCK# is asserted 1 clock cycle after address phase by an initiator wanting to perform an atomic operation that take more than one transaction to complete. HIC passes the LOCK# request to the secondary PCI bus. HIC does not drive LOCK# or propagate LOCK# upstream.
IDSEL#	Input	1	Chip Select for Type 0 configuration access. During a Type 0 configuration transaction, the initiator asserts IDSEL# during the address phase to select HIC. HIC responds by asserting DEVSEL#.
PERR#	STS	1	Data Parity Error on all transactions except Special Cycle. PERR# is driven one clock cycle after PAR. PERR# is asserted by target during write transactions, and by initiator during read transactions.
SERR#	OD	1	System Error. HIC asserts SERR# under the following conditions: Address parity error, Secondary bus SERR# asserted, Posted write transaction: data parity error on target bus, Posted write transaction discarded, Master abort, Target abort Delayed read or write transaction discarded, and Delayed transaction master timeout.
REQ#	TS	1	Request for bus. If a target retry or disconnect is received in response to initiating a transaction, HIC deasserts REQ# for at least 2 cycles before asserting it again.
GNT#	Input	1	Bus is granted to HIC. HIC can initiate transaction if GNT# is asserted and the bus is idle. When HIC is not requesting bus and GNT# is asserted, HIC must drive AD, C/BE, and PAR to valid logic levels.
CLKRUN#	I/OD	1	Input indicating clock status. HIC can request the central clock resource to start, speed up or maintain the PCI clock. There are 3 clocking states: Clock running, Clock about to stop/slow down, and Clock stopped/slowed.
PCICK	Input	1	PCI Clock. All inputs are sampled on the rising edge of PCICK. Frequency

FIG. 47

XPBus Signals

Name	Type	Pins	Description
PCK +	LVDS Output	2	Peripheral Clock Differential Signal Pair Output to XPBus
PD[3::0] +	LVDS Output	8	Peripheral Data Differential Signal Pair Output to XPBus
PCKR +	LVDS Input	2	Peripheral Clock Differential Signal Pair Input from XPBus
PDR[3::0] +	LVDS Input	8	Peripheral Data Differential Signal Pair Input from XPBus

FIG. 48

XIS Bus Video Port Signals

Name	Type	Pins	Description
VPCK +	LVDS Input	2	Video Port Clock Differential Signal Pair Input; 2 x Video clock rate
PCK +	LVDS Output	2	Video Port Data Differential Signal Pair Input; 10 bit/clock period

FIG. 49

Video Port Signals

Name	Type	Pins	Description
VPD [15::0]	Output	16	Video Port Data Output
VREF	Output	1	Vertical Reference
HREF	Output	1	Horizontal Reference
VCLK	Output	1	Video Pixel Clock
VRDY	Output	1	Video Source Ready

FIG. 50

Flash Memory Interface Signals

Name	Type	Pins	Description
A[18::0]	Output	19	Address for up to 512K x 8 Memory
DQ[7::0]	I/O	8	Data Input/Output
CE#	O	1	Chip Enable
WE#	O	1	Write Enable
OE#	O	1	Output Enable
WP#	O	1	Write protect

FIG. 51

Test Port (JTAG) Signals

Name	Type	Pins	Description
TCK	I	1	Test Clock
TDI	I	1	Test Data In
TDO	O	1	Test Data Out
TMS	I	1	Test Mode Select

FIG. 52

CPU Signal

Name	Type	Pins	Description
CPURST	I/OD	1	CPU Reset and PCI RST#
FERR#	I	1	Numeric Coprocessor Error
IGNNE#	OD	1	Ignore Numeric Exception
INIT	OD	1	Initialization
INTR	OD	1	CPU Interrupt; Pentium: active high; PII active low
A20M#	OD	1	Address 20 Mask; Keyboard Interface
NMI	OD	1	Non-Maskable Interrupt
SMI#	OD	1	System Management Interrupt
STPCLK#	OD	1	Stop Clock
SLP#	OD	1	Sleep

FIG. 53

North Bridge Signals

Name	Type	Pins	Description
SUSCLK	O	1	Suspend Clock from South Bridge. 32.768Khz for maintenance of DRAM Refresh.
SUSSTAT1#	O	1	Suspend Status Plane 1
PHOLD#	O	1	PCI Hold
PHLDA#	I	1	PCI Hold Acknowledge

FIG. 54

55 / 57

GPIO Signals

Name	Type	Pins	Description
GPIO[0]	O	1	CPU_STP# - CPU Clock Stop (optional)
GPIO[1]	O	1	PCI_STP# - PCI Clock Stop (optional)
GPIO[7::2]	I/O	6	General Purpose Input/Output Signals

FIG. 55

ERROR/RESET Signals

Name	Type	Pins	Description
RSTEH	O	1	Signal uses for: Reset from Host, Parity error for PIC transmission, & no connect detection
RSTEP	I	1	Signal uses for: Reset from Peripheral, Parity error for HIC transmission, No connect detection

FIG. 56

57 / 57

Power/Ground/OSC input Signals

Name	Type	Pins	Description
OSCin	I	1	Oscillator input for LVDS clock
GND (PLL)		1	PLL ground
VCC (PLL)		1	PLL 3.3v
VCC (core)		2	Core/CPU VCC = 3.3v
VCC (LVDS)		2	LVDS VCC = 3.3v
VCC (VP)		1	Video port: all output signals; VCC = 3.3v
VCC (PCI)		2	PCI VCC = 5v tolerant or 3.3v
VCC (Flash)		1	Flash memory VCC = 5v tolerant or 3.3v
GND (core)		2	Core ground
GND (LVDS)		2	LVDS ground
GND (PCI)		2	PCI ground
GND (Flash)		1	Flash memory ground
Reserved		5	Reserved pins

FIG. 57

Transaction History Date 2001-12-12
Date information retrieved from USPTO Patent Application Information Retrieval (PAIR) system records at www.uspto.gov

BEST COPY

PART B--ISSUE FEE TRANSMITTAL

Complete and send this form, together with applicable fee(s), to: Box ISSUE FEE
Assistant Commissioner for Patents
Washington, D.C. 20231

MAILING INSTRUCTIONS: This form should be used for transmitting the ISSUE FEE. Blocks 1 through 4 should be completed where appropriate. All further correspondence including the Issue Fee Receipt, the Patent, advance orders and notification of maintenance fees will be mailed to the current correspondence address as indicated unless corrected below or directed otherwise in Block 1, by (a) specifying a new correspondence address; and/or (b) indicating a separate "FEE ADDRESS" for maintenance fee notifications.

CURRENT CORRESPONDENCE ADDRESS (Note: Legibly mark-up with any corrections or use Block 1)

TM21/0817

RICHARD T. OGAWA
TOWNSEND AND TOWNSEND AND CREW L.L.P
TWO EMBARCADERO CENTER
8 TH FLOOR
SAN FRANCISCO CA 94111-3834

Note: The certificate of mailing below can only be used for domestic mailings of the Issue Fee Transmittal. The certificate cannot be used for any other accompanying papers. Each additional paper, such as an assignment or formal drawing, must have its own certificate of mailing.

Certificate of Mailing

I hereby certify that the Issue Fee Transmittal is being deposited with the United States Postal Service with sufficient postage for first class mail in an envelope addressed to the Box Issue Fee address above on the date indicated below.

Aimee Durham (Depositor's name)
(Signature)
11/16/01 (Date)

APPLICATION NO.	FILING DATE	TOTAL CLAIMS	EXAMINER AND GROUP ART UNIT	DATE MAILED
09/149,882	09/08/98	015	CAO, C 2182	08/17/01

First Named Applicant: CHU,

35 USC 154(b) term ext. = 0 Days.

TITLE OF INVENTION: COMMUNICATION CHANNEL AND INTERFACE DEVICES FOR BRIDGING COMPUTER INTERFACE BUSES

ATTY'S DOCKET NO.	CLASS-SUBCLASS	BATCH NO.	APPLN. TYPE	SMALL ENTITY	FEE DUE	DATE DUE
0 387112000300	710-065.000	K76	UTILITY	YES	$620.00	11/19/01

1. Change of correspondence address or indication of "Fee Address" (37 CFR 1.363). Use of PTO form(s) and Customer Number are recommended, but not required.
   - ☐ Change of correspondence address (or Change of Correspondence Address form PTO/SB/122) attached.
   - ☐ "Fee Address" indication (or "Fee Address" Indication form PTO/SB/47) attached.

2. For printing on the patent front page, list (1) the names of up to 3 registered patent attorneys or agents OR, alternatively, (2) the name of a single firm (having as a member a registered attorney or agent) and the names of up to 2 registered patent attorneys or agents. If no name is listed, no name will be printed.
   1 Townsend&Townsend&Crew LLP
   2
   3

3. ASSIGNEE NAME AND RESIDENCE DATA TO BE PRINTED ON THE PATENT (print or type)
   PLEASE NOTE: Unless an assignee is identified below, no assignee data will appear on the patent. Inclusion of assignee data is only appropriate when an assignment has been previously submitted to the PTO or is being submitted under separate cover. Completion of this form is NOT a substitute for filing an assignment.
   (A) NAME OF ASSIGNEE ACQIS TECHNOLOGY, INC.
   (B) RESIDENCE: (CITY & STATE OR COUNTRY) Mountain View, California
   Please check the appropriate assignee category or categories (will not be printed on the patent):
   ☐ individual ☒ corporation or other private group entity, ☐ government

4a. The following fees are enclosed (make check payable to Commissioner of Patents and Trademarks):
   - ☒ Issue Fee
   - ☐ Advance Order - # of Copies

4b. The following fees or deficiency in these fees should be charged to:
   DEPOSIT ACCOUNT NUMBER 20-1430
   (ENCLOSE AN EXTRA COPY OF THIS FORM)
   - ☒ Issue Fee
   - ☒ Advance Order - # of Copies 10

The COMMISSIONER OF PATENTS AND TRADEMARKS IS requested to apply the Issue Fee to the application identified above.

(Authorized Signature) (Date) 11/16/01
Kent J. Tobin, Reg.No.39,496

NOTE: The Issue Fee will not be accepted from anyone other than the applicant; a registered attorney or agent; or the assignee or other party in interest as shown by the records of the Patent and Trademark Office.

Burden Hour Statement: This form is estimated to take 0.2 hours to complete. Time will vary depending on the needs of the individual case. Any comments on the amount of time required to complete this form should be sent to the Chief Information Officer, Patent and Trademark Office, Washington, D.C. 20231. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. SEND FEES AND THIS FORM TO: Box Issue Fee, Assistant Commissioner for Patents, Washington, D.C. 20231.

Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it displays a valid OMB control number.

TRANSMIT THIS FORM WITH FEE

PTOL-85B (REV.10-99) Approved for use through 09/30/99. OMB 0651-0033 Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE

12/17/2001 DYEN22 00000010 201430 09882
01 FC:141 620.00 OP
02 FC:142 40.00 OP

RECEIVED

Atty Docket No. 019152-000200US

PTO FAX NO.: 1-703-746-7238

ATTENTION: Examiner C. Cao
TELEPHONE NO.: 703-746-7240

Official

Group Art Unit 2182

OFFICIAL COMMUNICATION

FOR THE PERSONAL ATTENTION OF

EXAMINER C. Cao

CERTIFICATION OF FACSIMILE TRANSMISSION

I hereby certify that the following document in re Application of William W.Y. Chu, Application No. 09/149,882, filed September 8, 1998 for COMMUNICATION CHANNEL AND INTERFACE DEVICES FOR BRIDGING COMPUTER INTERFACE BUSES is being facsimile transmitted to the Patent and Trademark Office on the date shown below.

Document(s) Attached

1. Transmittal Form (1pg);
2. Fee Transmittal Form (1pg);
3. Copy of Notice of Publication Fee Due (1pg);
4. This Facsmile Transmission Page (1pg).

Number of pages being transmitted, including this page: 4

Dated: December 17, 2001

Aimee Durham

PLEASE CONFIRM RECEIPT OF THIS PAPER BY RETURN FACSIMILE AT (415) 576-0300

TOWNSEND and TOWNSEND and CREW LLP
Two Embarcadero Center, 8th Floor
San Francisco, CA 94111-3834
Telephone: 650-326-2400
Fax: 650-326-2422

PA 3190237 v1

OK to Enter

8/17/01

Received from < 6503262422 > at 12/17/01 11:49:08 AM [Eastern Standard Time]

Please type a plus sign (+) inside this box → [+]

PTO/SB/21 (08-00)
Approved for use through 10/31/2002. OMB 0651-0031
U.S. Patent and Trademark Office: U.S. DEPARTMENT OF COMMERCE

Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it displays a valid OMB control number.

TRANSMITTAL FORM

(to be used for all correspondence after initial filing)

Application Number	09/149,882
Filing Date	September 8, 1998
First Named Inventor	Chu, William W.Y.
Group Art Unit	2182
Examiner Name	C. Cao
Attorney Docket Number	019152-000200US

Total Number of Pages in This Submission

ENCLOSURES *(check all that apply)*

- [x] Fee Transmittal Form
- [ ] Fee Attached
- [ ] Amendment / Response
- [ ] After Final
- [ ] Affidavits/declaration(s)
- [ ] Extension of Time Request
- [ ] Express Abandonment Request
- [ ] Information Disclosure Statement
- [ ] Certified Copy of Priority Document(s)
- [ ] Response to Missing Parts/ Incomplete Application
  - [ ] Response to Missing Parts under 37 CFR 1.52 or 1.53
- [ ] Assignment Papers *(for an Application)*
- [ ] Drawing(s)
- [ ] Licensing-related Papers
- [ ] Petition Routing Slip (PTO/SB/69) and Accompanying Petition
- [ ] Petition to Convert to a Provisional Application
- [ ] Power of Attorney, Revocation Change of Correspondence Address
- [ ] Terminal Disclaimer
- [ ] Request for Refund
- [ ] CD, Number of CD(s)
- [ ] After Allowance Communication to Group
- [ ] Appeal Communication to Board of Appeals and Interferences
- [ ] Appeal Communication to Group *(Appeal Notice, Brief, Reply Brief)*
- [ ] Proprietary Information
- [ ] Status Letter
- [x] Other Enclosure(s) *(please identify below)*:

Copy of Notice of Publication Fee Due.

Remarks The Commissioner is authorized to charge any additional fees to Deposit Account 20-1430.

SIGNATURE OF APPLICANT, ATTORNEY, OR AGENT

Firm and Individual name	Townsend and Townsend and Crew LLP Kent J. Tobin Reg. No. 39,496
Signature	
Date	December 13, 2001

CERTIFICATE OF MAILING

I hereby certify that this correspondence is being facsimile transmitted to the Patent and Trademark Office, Fax No. (703) 746-7238 on December 13, 2001

Typed or printed name	Aimee Durham		
Signature		Date	December 13, 2001

Burden Hour Statement: This form is estimated to take 0.2 hours to complete. Time will vary depending upon the needs of the individual case. Any comments on the amount of time you are required to complete this form should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, Washington, DC 20231. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. SEND TO: Assistant Commissioner for Patents, Washington, DC 20231.

PA 3190234 v1

Received from < 6503262422 > at 12/17/01 11:49:08 AM [Eastern Standard Time]

PTO/SB/17 (09-00)
Approved for use through 10/31/2002. OMB 0651-0032
Patent and Trademark Office: U.S. DEPARTMENT OF COMMERCE
Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it displays a valid OMB control number.

FEE TRANSMITTAL for FY 2001

Patent fees are subject to annual revision.

TOTAL AMOUNT OF PAYMENT ($) 300

Complete if Known	
Application Number	09/149,882
Filing Date	September 8, 1998
First Named Inventor	Chu, William W.Y.
Examiner Name	C. Cao
Group Art Unit	2182
Attorney Docket No.	019152-000200US

METHOD OF PAYMENT

1. ☒ The Commissioner is hereby authorized to charge indicated fees and credit any over payments to:

Deposit Account Number: 20-1430

Deposit Account Name: Townsend and Townsend and Crew LLP

☒ Charge Any Additional Fee Required Under 37 CFR 1.16 and 1.17

☒ Applicant claims small entity status. See 37 CFR 1.27

2. ☐ Payment Enclosed:

☐ Check ☐ Credit card ☐ Money Order ☐ Other

FEE CALCULATION

1. BASIC FILING FEE

Large Fee Code	Large Entity Fee ($)	Small Fee Code	Small Entity Fee ($)	Fee Description	Fee Paid
101	740	201	370	Utility filing fee	
106	330	206	165	Design filing fee	
107	510	207	255	Plant filing fee	
108	740	208	370	Reissue filing fee	
114	160	214	80	Provisional filing fee	

SUBTOTAL (1) ($)

2. EXTRA CLAIM FEES

			Extra Claims		Fee from below		Fee Paid
Total Claims		-20** =		X		=	
Independent Claims		-3** =		X		=	
Multiple Dependent				X		=	

Large Fee Code	Large Entity Fee ($)	Small Fee Code	Small Entity Fee ($)	Fee Description
103	18	203	9	Claims in excess of 20
102	84	202	42	Independent claims in excess of 3
104	280	204	140	Multiple dependent claim, if not paid
109	84	209	42	** Reissue independent claims over original patent
110	18	210	9	** Reissue claims in excess of 20 and over original patent

SUBTOTAL (2) ($)

**or number previously paid, if greater; For Reissues, see above

FEE CALCULATION (continued)

3. ADDITIONAL FEES

Large Fee Code	Large Entity Fee ($)	Small Fee Code	Small Entity Fee ($)	Fee Description	Fee Paid
105	130	205	65	Surcharge - late filing fee or oath	
127	50	227	25	Surcharge - late provisional filing fee or cover sheet.	
139	130	139	130	Non-English specification	
147	2,520	147	2,520	For filing a request for reexamination	
112	920*	112	920*	Requesting publication of SIR prior to Examiner action	
113	1,840*	113	1,840*	Requesting publication of SIR after Examiner action	
115	110	215	55	Extension for reply within first month	
116	400	216	200	Extension for reply within second month	
117	920	217	460	Extension for reply within third month	
118	1,440	218	720	Extension for reply within fourth month	
128	1,960	228	980	Extension for reply within fifth month	
119	320	219	160	Notice of Appeal	
120	320	220	160	Filing a brief in support of an appeal	
121	280	221	140	Request for oral hearing	
138	1,510	138	1,510	Petition to institute a public use proceeding	
140	110	240	55	Petition to revive – unavoidable	
141	1,280	241	640	Petition to revive – unintentional	
142	1,280	242	640	Utility issue fee (or reissue)	
143	480	243	240	Design issue fee	
144	620	244	310	Plant issue fee	
122	130	122	130	Petitions to the Commissioner	
123	50	123	50	Petitions related to provisional applications	
126	180	126	180	Submission of Information Disclosure Stmt	
581	40	581	40	Recording each patent assignment per property (times number of properties)	
146	740	246	370	Filing a submission after final rejection (37 CFR § 1.129(a))	
149	740	249	370	For each additional invention to be examined (37 CFR § 1.129(b))	
179	740	279	370	Request for Continued Examination (RCE)	
169	900	169	900	Request for expedited examination of a design application	
Other fee (specify) Publication Fee					300.

The Commissioner is authorized to charge any additional fees to the above noted Deposit Account.

*Reduced by Basic Filing Fee Paid SUBTOTAL (3) ($)300

SUBMITTED BY				Complete (if applicable)	
Name (Print/Type)	Kent J. Tobin	Registration No. (Attorney/Agent)	39,496	Telephone	650-326-2400
Signature				Date	12/13/01

WARNING: Information on this form may become public. Credit card information should not be included on this form. Provide credit card information and authorization on PTO-2038.

Burden Hour Statement: This form is estimated to take 0.2 hours to complete. Time will vary depending upon the needs of the individual case. Any comments on the amount of time you are required to complete this form should be sent to the Chief Information Officer, Patent and Trademark Office, Washington, DC 20231. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. SEND TO: Assistant Commissioner for Patents, Washington, DC 20231. PA 3190230 v1

Received from < 6503262422 > at 12/17/01 11:49:08 AM [Eastern Standard Time]

KJT 01/152.000200US

UNITED STATES PATENT AND TRADEMARK OFFICE

COMMISSIONER FOR PATENTS
UNITED STATES PATENT AND TRADEMARK OFFICE
WASHINGTON, D.C. 20231
www.uspto.gov

APPLICATION NUMBER	FILING DATE	FIRST NAMED APPLICANT	ATTY. DOCKET NO./TITLE
09/149,882	09/08/1998	WILLIAM W. Y. CHU	387112000300

CONFIRMATION NO. 5616

OC000000005571848

RICHARD T. OGAWA
TOWNSEND AND TOWNSEND AND CREW L.L.P
TWO EMBARCADERO CENTER
8 TH FLOOR
SAN FRANCISCO, CA 94111-3834

Title: COMMUNICATION CHANNEL AND INTERFACE DEVICES FOR BRIDGING COMPUTER INTERFACE BUSES

Response Due 12-21-01 HWC **Date Mailed: 09/21/2001**

NOTICE OF PUBLICATION FEE DUE

The above-identified application was filed (including as a Continued Prosecution Application) on or after November 29, 2000 and a non-publication request in compliance with 37 CFR 1.213 was not included with the application on filing. Since the application has been allowed, a publication fee is due.

The fee due is $300.00. No small entity discount is available. See 37 CFR 1.18(d).

The reply to this notice should be mailed to Box ISSUE FEE, Commissioner for Patents, Washington D.C. 20231.

The publication fee must be submitted within **THREE MONTHS** from the mailing date of this notice or the application may be regarded as abandoned. No extensions of time under 37 CFR 1.136(a) or (b) are available. A reply must be filed to this notice, even if applicant does not anticipate that the application will be published (e.g., because the patent has issued and the projected publication date is more than a month after the issue date of the patent). A proper reply to this notice in such a situation would be a statement that no fee is now due, citing 37 CFR 1.211(e).

If publication of the application does not occur and applicant requests a refund, any publication fee paid will be refunded. See 37 CFR 1.211(e).

For further information about this notice, see the questions and answers posted at: http://www.uspto.gov/web/offices/dcom/olia/aipa/infoexch.htm#CB. Questions relating to this Notice should be directed to the Customer Service Center, Office of Patent Publication at: (703) 308-6789 and 1-888-786-0101.

A copy of this notice should be returned with any reply.

Received from < 6503262422 > at 12/17/01 11:49:08 AM [Eastern Standard Time]

File History Content Report

The following content is missing from the original file history record obtained from the United States Patent and Trademark Office. No additional information is available.

Document Date - 2002-02-05

Document Title - USPTO Grant

This page is not part of the official USPTO record. It has been determined that content identified on this document is missing from the original file history record.

File History Content Report

The following content is missing from the original file history record obtained from the United States Patent and Trademark Office. No additional information is available.

Document Date - 2009-03-26

Document Title

USPTO Communication Re: Change of Address/Power of Attorney

This page is not part of the official USPTO record. It has been determined that content identified on this document is missing from the original file history record.

File History Content Report

The following content is missing from the original file history record obtained from the United States Patent and Trademark Office. No additional information is available.

Document Date - 2009-05-14

Document Title

USPTO Communication Re: Change of Address/Power of Attorney

This page is not part of the official USPTO record. It has been determined that content identified on this document is missing from the original file history record.

File History Content Report

The following content is missing from the original file history record obtained from the United States Patent and Trademark Office. No additional information is available.

Document Date - 2012-10-18

Document Title

USPTO Communication Re: ENTITY STATUS SET TO UNDISCOUNTED (INITIAL DEFAULT SETTING OR STATUS CHANGE)

This page is not part of the official USPTO record. It has been determined that content identified on this document is missing from the original file history record.

BEST COPY

Small entity Status

OP	1	09149882	00000002	102798	120798	205	65.00
OP	4	09149882	00000003	120798	120798	704	65.00-

Case # 09/149882

000S/000S DISPLAYED

ID	TPE	NAME OR ACCOUNT	C-NBR	MLEDTE	CURDTE	F-C	$ AMOUNT
OP	1	09149882	00000054	102798	110398	201	395.00 Pd
OP	1	09149882	00000055	102798	110398	202	246.00 Pd
OP	1	09149882	00000056	102798	110398	203	242.00 Pd
OP	1	09149882	00000057	102798	110398	105	130.00
OP	1	09149882	00000119	102798	110498	581	40.00
OP	1	09149882	00000001	102798	120798	105	130.00-
OP	1	09149882	00000002	102798	120798	205	65.00
OP	4	09149882	00000003	120798	120798	704	65.00-

PATENT APPLICATION FEE DETERMINATION RECORD

Effective October 1, 1997

Application or Docket Number: 09/149882

CLAIMS AS FILED - PART I

	(Column 1) NUMBER FILED	(Column 2) NUMBER EXTRA
BASIC FEE		
TOTAL CLAIMS	42 minus 20 =	* 22
INDEPENDENT CLAIMS	9 minus 3 =	* 6
MULTIPLE DEPENDENT CLAIM PRESENT		

* If the difference in column 1 is less than zero, enter "0" in column 2

SMALL ENTITY TYPE ☐ RATE	FEE	OR	OTHER THAN SMALL ENTITY RATE	FEE
	395.00	OR		790.00
x$11=	242	OR	x$22=	484
x41=	246	OR	x82=	492
+135=		OR	+270=	
TOTAL	883	OR	TOTAL	1766

CLAIMS AS AMENDED - PART II

AMENDMENT A

	(Column 1) CLAIMS REMAINING AFTER AMENDMENT		(Column 2) HIGHEST NUMBER PREVIOUSLY PAID FOR	(Column 3) PRESENT EXTRA
Total	*	Minus	**	=
Independent	*	Minus	***	=
FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM				

SMALL ENTITY RATE	ADDITIONAL FEE	OR	OTHER THAN SMALL ENTITY RATE	ADDITIONAL FEE
x$11=		OR	x$22=	
x41=		OR	x82=	
+135=		OR	+270=	
TOTAL ADDIT. FEE		OR	TOTAL ADDIT. FEE	

AMENDMENT B

	(Column 1) CLAIMS REMAINING AFTER AMENDMENT		(Column 2) HIGHEST NUMBER PREVIOUSLY PAID FOR	(Column 3) PRESENT EXTRA
Total	*	Minus	**	=
Independent	*	Minus	***	=
FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM				

SMALL ENTITY RATE	ADDITIONAL FEE	OR	OTHER THAN SMALL ENTITY RATE	ADDITIONAL FEE
x$11=		OR	x$22=	
x41=		OR	x82=	
+135=		OR	+270=	
TOTAL ADDIT. FEE		OR	TOTAL ADDIT. FEE	

AMENDMENT C

	(Column 1) CLAIMS REMAINING AFTER AMENDMENT		(Column 2) HIGHEST NUMBER PREVIOUSLY PAID FOR	(Column 3) PRESENT EXTRA
Total	*	Minus	**	=
Independent	*	Minus	***	=
FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM				

SMALL ENTITY RATE	ADDITIONAL FEE	OR	OTHER THAN SMALL ENTITY RATE	ADDITIONAL FEE
x$11=		OR	x$22=	
x41=		OR	x82=	
+135=		OR	+270=	
TOTAL ADDIT. FEE		OR	TOTAL ADDIT. FEE	

* If the entry in column 1 is less than the entry in column 2, write "0" in column 3.
** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 20, enter "20."
*** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 3, enter "3."
The "Highest Number Previously Paid For" (Total or Independent) is the highest number found in the appropriate box in column 1.

FORM PTO-875 (Rev. 8/97) *U.S. Government Printing Office: 1997 - 430-571/69194 Patent and Trademark Office, U.S. DEPARTMENT OF COMMERCE

SERIAL NO. 09/149,823

FILING DATE

APPLICANT(S)

MULTIPLE DEPENDENT CLAIM FEE CALCULATION SHEET
(FOR USE WITH FORM PTO-875)

CLAIMS

	AS FILED		AFTER 1st AMENDMENT		AFTER 2nd AMENDMENT	
	IND.	DEP.	IND.	DEP.	IND.	DEP.
1	/					
2		/				
3		/				
4		/				
5		/				
6		/				
7		/				
8		/				
9		/				
10	/					
11		/				
12		/				
13		/				
14		/				
15		/				
16	/					
17		/				
18	/					
19		/				
20	/					
21		/				
22		/				
23	/					
24	/					
25	/	/				
26		/				
27		/				
28		/				
29		/				
30		/				
31		/				
32		/				
33		/				
34		/				
35		/				
36		/				
37		/				
38		/				
39		/				
40		/				
41		/				
42	/					
43						
44						
45						
46						
47						
48						
49						
50						
TOTAL IND.	9					
TOTAL DEP.	33					
TOTAL						

	IND.	DEP.	IND.	DEP.	IND.	DEP.
61						
62						
63						
64						
65						
66						
67						
68						
69						
70						
71						
72						
73						
74						
75						
76						
77						
78						
79						
80						
81						
82						
83						
84						
85						
86						
87						
88						
89						
90						
91						
92						
93						
94						
95						
96						
97						
98						
99						
100						
TOTAL IND.						
TOTAL DEP.						
TOTAL						

Derwent Innovation Patent Export, 2021-01-25 15:55:41 +0000

Search results for: PNS=(US6345330);
Collections searched: DWPI; ARIPO grant; Argentina UM; Argentina app; Armenia grant; Australia UM; Australia app; Australia grant; Austria UM; Austria app; Austria grant; Belarus UM; Belarus grant; Belgium app; Belgium grant; Brazil UM; Brazil app; Brazil grant; Bulgaria UM; Bulgaria app; Bulgaria grant; Canada app; Canada grant; China, Mainland UM; China, Mainland app; China, Mainland grant; Colombia app; Costa Rica UM; Costa Rica app; Croatia UM; Croatia app; Croatia grant; Cuba app; Cuba grant; Czech Republic UM; Czech Republic app; Czech Republic grant; Czechoslovakia grant; Denmark UM; Denmark app; Denmark grant; Estonia UM; Estonia app; Estonia grant; Eurasian (EAPO) grant; Europe (EP) app; Europe (EP) grant; Finland app; Finland grant; France app; France grant; Georgia grant; German Democratic Republic app; German Democratic Republic grant; Germany UM; Germany app; Germany grant; Greece app; Greece grant; Gulf Cooperation Council grant; Hong Kong UM; Hong Kong app; Hong Kong grant; Hungary grant; Iceland grant; India app; India grant; Indonesia UM; Indonesia app; Ireland UM; Ireland app; Ireland grant; Israel grant; Italy grant; Italy grant; Italy grant; Italy grant; Japan UM; Japan app; Japan grant; Korea UM; Korea app; Korea grant; Latvia grant; Lithuania grant; Luxembourgh app; Luxembourgh grant; Malaysia grant; Mexico app; Mexico grant; Moldova UM; Moldova grant; Monaco grant; Mongolia UM; Mongolia grant; Morocco app; Morocco grant; Netherlands app; Netherlands grant; New Zealand grant; Norway app; Norway grant; OAPI grant; PCT (WO) app; Philippines app; Philippines grant; Poland UM; Poland grant; Portugal UM; Portugal app; Portugal grant; Romania UM; Romania app; Romania granted; Russia UM; Russia app; Russia grant; Serbia UM; Serbia app; Serbia grant; Singapore app; Singapore grant; Slovakia UM; Slovakia app; Slovakia grant; Slovenia UM; Slovenia grant; South Africa app; Spain UM; Spain app; Spain grant; Sweden app; Sweden grant; Switzerland app; Switzerland grant; Taiwan UM; Taiwan appl; Taiwan grant; Thailand grant; Tunisia app; Turkey UM; Turkey app; UK app; UK grant; USSR grant; Ukraine UM; Ukraine grant; United States app; United States grant; Uruguay app; Vietnam app; Vietnam grant; Other

Table of Contents

1. US6345330B2 Communication channel and interface devices for bridging computer interface buses

Family 1/1

1 record(s) per family

Record 1/1 US6345330B2 Communication channel and interface devices for bridging computer interface buses

Title: Communication channel and interface devices for bridging computer interface buses
Title - DWPI: Detachable computing module for attachment to peripheral console for forming fully operational personal computer system
Priority Number: US199883886P | US199892706P
Priority Date: 1998-05-01 | 1998-07-14
Application Number: US1998149882A
Application Date: 1998-09-08
Publication Date: 2002-02-05
IPC Class Table:

IPC	Section	Class	Subclass	Class Group	Subgroup
G06F001340	G	G06	G06F	G06F0013	G06F001340

IPC Class Table - DWPI:

IPC - DWPI	Section - DWPI	Class - DWPI	Subclass - DWPI	Class Group - DWPI	Subgroup - DWPI
G06F000116 (IPC 1-7)	G	G06	G06F	G06F0001	G06F000116 (IPC 1-7)
G06F001300 (IPC 1-7)	G	G06	G06F	G06F0013	G06F001300 (IPC 1-7)
G06F001312 (IPC 1-7)	G	G06	G06F	G06F0013	G06F001312 (IPC 1-7)
G06F000300 (IPC 1-7)	G	G06	G06F	G06F0003	G06F000300 (IPC 1-7)
G06F001328 (IPC 1-7)	G	G06	G06F	G06F0013	G06F001328 (IPC 1-7)
G06F001338 (IPC 1-7)	G	G06	G06F	G06F0013	G06F001338 (IPC 1-7)
G06F000116	G	G06	G06F	G06F0001	G06F000116

G06F001340	G	G06	G06F	G06F0013	G06F001340

Assignee/Applicant: Acqis Technology Inc.,Mountain View,CA

JP F Terms:

JP FI Codes:

Assignee - Original: Acqis Technology Inc.

Any CPC Table:

Type	Invention	Additional	Version	Office
Current	**G06F 13/4045**	-	20130101	EP

ECLA: G06F001340D5R

Abstract:

The present invention encompasses an apparatus for bridging a first computer interface bus and a second computer interface bus, where each of the first and second computer interface buses have a number of parallel multiplexed address/data bus lines and operate at a clock speed in a predetermined clock speed range having a minimum clock speed and a maximum clock speed. The apparatus comprises an interface channel having a clock line and a plurality of bit lines for transmitting bits; a first interface controller coupled to the first computer interface bus and to the interface channel to encode first control signals from the first computer interface bus into first control bits to be transmitted on the interface channel and to decode second control bits received from the interface channel into second control signals to be transmitted to the first computer interface bus; and a second interface controller coupled to the interface channel and the second computer interface bus to decode the first control bits from the interface channel into third control signals to be transmitted on the second computer interface bus and to encode fourth control signals from the second computer interface bus into the second control bits to be transmitted on the interface channel.In one embodiment, the first and second interface controllers comprise a host interface controller (HIC) and a peripheral interface controller (PIC), respectively, the first and second computer interface buses comprise a primary PCI and a secondary PCI bus, respectively, and the interface channel comprises an LVDS channel.

Language of Publication: EN

INPADOC Legal Status Table:

Gazette Date	Code	INPADOC Legal Status Impact

2013-07-10	FPAY	+
Description: FEE PAYMENT FEE PAYMENT YEAR 12		
2011-11-01	AS	-
Description: ASSIGNMENT ACQIS LLC, TEXAS ASSIGNMENT OF ASSIGNORS INTEREST; ASSIGNOR:ACQIS TECHNOLOGY, INC.; REEL/FRAME:027154/0398 2011-11-01		
2009-07-31	FPAY	+
Description: FEE PAYMENT FEE PAYMENT YEAR 8		
2005-08-05	FPAY	+
Description: FEE PAYMENT FEE PAYMENT YEAR 4		
2002-01-18	STCF	-
Description: INFORMATION ON STATUS: PATENT GRANT PATENTED CASE		
1998-10-27	AS	-
Description: ASSIGNMENT ACQIS TECHNOLOGY, INC., CALIFORNIA ASSIGNMENT OF ASSIGNORS INTEREST; ASSIGNOR:CHU, WILLIAM W.Y.; REEL/FRAME:009557/0507 1998-10-16		

Post-Issuance (US):

Reassignment (US) Table:

Assignee	Assignor	Date Signed	Reel/Frame	Date
ACQIS LLC,MCKINNEY,TX,US	ACQIS TECHNOLOGY, INC.	2011-11-01	027154/0398	2011-11-01
Conveyance: ASSIGNMENT OF ASSIGNORS INTEREST (SEE DOCUMENT FOR DETAILS).				
Corresponent: COOLEY LLP 777 SIXTH STREET N.W. SUITE 1100 WASHINGTON, DC 20001				
ACQIS TECHNOLOGY INC.,MOUNTAIN VIEW,CA,US	CHU, WILLIAM W.Y.	1998-10-16	009557/0507	1998-10-27
Conveyance: ASSIGNMENT OF ASSIGNORS INTEREST (SEE DOCUMENT FOR DETAILS).				
Corresponent: MORRISON & FOERSTER LLP ARARAT KAPOUYTIAN 425 MARKET STREET SAN FRANCISCO, CA 94105-2482				

Maintenance Status (US):

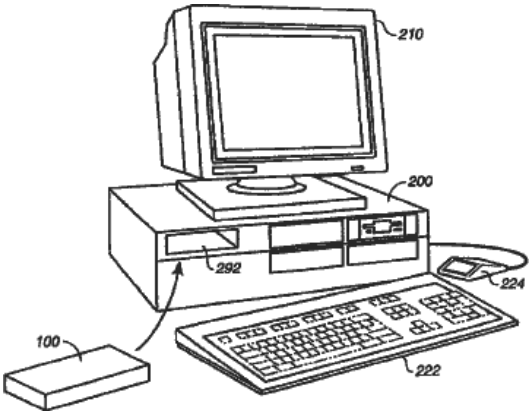
Litigation (US):

Opposition (EP):

License (EP):

EPO Procedural Status:

Front Page Drawing:



Assignee - Current US: ACQIS LLC

Clarivate Analytics
Copyright 2007-2021 CLARIVATE ANALYTICS

COMMUNICATION CHANNEL AND INTERFACE DEVICES FOR BRIDGING COMPUTER INTERFACE BUSES

PATENT #	APPLICATION #	FILING DATE	ISSUE DATE
6345330	09149882	09/08/1998	02/05/2002

Payment Window Status

No maintenance fees are due.

WINDOW	STATUS	FEES
11.5 Year	Closed	Paid

Window	First Day to Pay	Surcharge Starts	Last Day to Pay	Status	Fees
3.5 Year	02/05/2005	08/06/2005	02/06/2006	Closed	Paid
7.5 Year	02/05/2009	08/06/2009	02/05/2010	Closed	Paid
11.5 Year	02/05/2013	08/06/2013	02/05/2014	Closed	Paid

Patent Holder Information

Customer # 204

Entity Status UNDISCOUNTED

Phone Number 3014248890

Address COMPUTER PACKAGES, INC.
414 HUNGERFORD DRIVE
ROCKVILLE, MD 20850
UNITED STATES