

In re Patent of:	William W.Y. CHU	Confirmation No.:	6108
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For:	Ex Parte Reexamination of Patent No. 6,216,185		

Title: PERSONAL COMPUTER PERIPHERAL CONSOLE WITH ATTACHED COMPUTER MODULE

PATENT OWNER'S RESPONSE TO OFFICE ACTION

Remarks/Arguments begin on page 12 of this paper.

IN THE DRAWINGS

Attachment: New Sheets corresponding to FIG. 13 and FIG. 14

IN THE SPECIFICATION

Please add the following new paragraphs immediately after the paragraphs previously added beginning at col. 3, line 40:

FIG. 13 is a partial block diagram of a computer system in which the north and south bridges are integrated with the host and peripheral interface controllers, respectively.

FIG. 14 is a schematic diagram of the signal lines PCK, PD0 to PD3, and PCN.

Please add the following new paragraphs immediately after the paragraphs previously added beginning at col. 17, line 30:

In yet another embodiment, such as that shown in FIG. 13, the HIC and PIC are integrated with the north and south bridges, respectively, such that integrated HIC and north bridge unit 1305 includes an HIC and a north bridge, while integrated PIC and south bridge unit 1310 includes a PIC and a south bridge.

FIG. 14 is a schematic diagram of lines PCK, PD0 to PD3, and PCN. These lines are unidirectional LVDS lines for transmitting clock signals and bits from the HIC to the PIC. The bits on the PD0 to PD3 and the PCN lines are sent synchronously within every clock cycle of the PCK. Another set of lines, namely PCKR, PDR0 to PDR3, and PCNR, are used to transmit clock signals and bits from the PIC to HIC. The lines used for transmitting information from the PIC to the HIC have the same structure as those shown in FIG. 14, except that they transmit data in a direction opposite to that in which the lines shown in FIG. 14 transmit data. In other words they transmit information from the PIC to the HIC. The bits on the PDR0 to PDR3 and the PCNR lines are sent synchronously within every clock cycle of the PCKR. Some of the examples of control information that may be sent in the reverse direction, i.e., on PCNR line, include a request to switch data bus direction because of a pending operation (such as read data available), a control signal change in the target requiring communication in the reverse direction, target busy, and transmission error detected.

The XDBus which includes lines PCK, PD0 to PD3, PCN, PCKR, PDR0 to PDR3, and PCNR, has two sets of unidirectional lines transmitting clock signals and bits in opposite directions. The first set of unidirectional lines includes PCK, PD0 to PD3, and PCN. The second set of unidirectional lines includes PCKR, PDR0 to PDR3, and PCNR. Each of these unidirectional set of lines is a point-to-point bus with a fixed transmitter and receiver, or in other words a fixed master and slave bus. For the first set of unidirectional lines, the HIC is a fixed transmitter/master whereas the PIC is a fixed receiver/slave. For the second set of

unidirectional lines, the PIC is a fixed transmitter/master whereas the HIC is a fixed receiver/slave. The LVDS lines of XPBus, a cable friendly and remote system I/O bus, transmit fixed length data packets within a clock cycle.

The XPBus lines, PD0 to PD3, PCN, PDR0 to PDR3 and PCNR, and the video data and clock lines, VPD and VPCK, are not limited to being LVDS lines, as they may be other forms of bit based lines. For example, in another embodiment, the XPBus lines may be IEEE 1394 lines.

It is to be noted that although each of the lines PCK, PD0 to PD3, PCN, PCKR, PDR0 to PDR3, PCNR, VPCK, and VPD is referred to as a line, in the singular rather than plural, each such line may contain more than one physical line. For example, in the embodiment shown in FIG. 14, each of lines PCK, PD0 to PD3 and PCN includes two physical lines between each driver and its corresponding receiver. The term line, when not directly preceded by the terms physical or conductive, is herein used interchangeably with a signal or bit channel which may consist of one or more physical lines for transmitting a signal. In the case of non-differential signal lines, generally only one physical line is used to transmit one signal. However, in the case of differential signal lines, a pair of physical lines is used to transmit one signal. For example, a bit line or bit channel in an LVDS or IEEE 1394 interface consists of a pair of physical lines which together transmit a signal.

A bit based line (i.e., a bit line) is a line for transmitting serial bits. Bit based lines typically transmit bit packets and use a serial data packet protocol. Examples of bit lines include an LVDS line, an IEEE 1394 line, and a Universal Serial Bus (USB) line.

IN THE CLAIMS

1-48. (Cancelled)

49. (New) A detachable computing module for attachment to a peripheral console for forming a fully operational personal computer system comprising:

an enclosure;

a CPU having a power supply connection point;

memory coupled to said CPU;

mass storage coupled to said CPU; and

interconnection circuitry coupled to said CPU, said interconnection circuitry connectable to a peripheral console, said interconnection circuitry configured to convey a low-voltage differential signaling (LVDS) bit stream;

wherein said power supply connection point of said CPU is uncoupled from any electrical power source having sufficient energy to sustain execution of instructions by said CPU whenever said interconnection circuitry is disconnected from a peripheral console,

wherein said interconnection circuitry comprises a LVDS channel comprising two sets of unidirectional, multiple serial bit channels to transmit data in opposite directions,

wherein said LVDS channel is configured to convey encoded Peripheral Component Interconnect bus transaction data.

50. (New) The apparatus of claim 49 wherein said encoded Peripheral Component Interconnect bus transaction data comprises 10 bit packets.

51-55. (Cancelled)

56. (New) A detachable computing module for attachment to a peripheral console for forming a fully operational personal computer system comprising:

an enclosure;

a CPU;

memory coupled to said CPU;

mass storage coupled to said CPU;

a communication channel coupled to said CPU and configured to convey a low-voltage differential signaling (LVDS) bit stream;

interconnection circuitry coupled to said CPU, said interconnection circuitry connectable to a peripheral console; and

power supply circuitry having a stored energy capacity no greater than the energy required to power said CPU, memory, and mass storage for 30 minutes of operation at the maximum rated speed of the CPU,

wherein said communication channel comprises a first unidirectional, serial bit channel and a second unidirectional, serial bit channel, and said first unidirectional, serial bit channel and said second unidirectional, serial bit channel are configured to transmit data in opposite directions,

wherein said communication channel comprises multiple pairs of unidirectional, serial bit channels to transmit data in opposite directions,

wherein said communication channel is configured to convey an encoded serial bit stream of Peripheral Component Interconnect bus transaction.

57. (New) The apparatus of claim 56 wherein said encoded serial bit stream comprises encoded address and data bits.

58. (New) The apparatus of claim 56 wherein said interconnection circuitry is coupled to said communication channel to encode Peripheral Component Interconnect bus transaction data as said encoded serial bit stream.

59. (New) The apparatus of claim 56 wherein said interconnection circuitry comprises said communication channel to convey said encoded serial bit stream between said computing module and said peripheral console.

60-69. (Cancelled)

70. (New) A personal computer system wherein the core computing power and environment for a computer user can be readily separated and transported from the remaining computer system components comprising:

(a) a detachable computing module including

an enclosure;

a CPU having a power supply connection point;

memory coupled to said CPU;

mass storage coupled to said CPU; and

(b) a peripheral console comprising a power supply; and

(c) interconnection circuitry coupled to said computing module and to said peripheral console for conveying electrical power and signals between said computing module and said peripheral console;

wherein said power supply connection point of said CPU is uncoupled from any electrical power source having sufficient energy to sustain execution of instructions by said CPU whenever said computing module is disconnected from said peripheral console,

wherein said peripheral console further comprises a low-voltage differential signaling (LVDS) channel comprising two sets of unidirectional, multiple serial bit channels to transmit encoded Peripheral Component Interconnect bus transaction data in opposite directions.

71. (New) The apparatus of claim 70 wherein said encoded Peripheral Component Interconnect bus transaction data comprises 10 bit packets.

72-74. (Cancelled)

75. (New) A personal computer system wherein the core computing power and environment for a computer user can be readily separated and transported from the remaining computer system components comprising:

(a) a detachable computing module including

an enclosure,

a CPU,

memory coupled to said CPU,

mass storage coupled to said CPU, and

power supply circuitry having a stored energy capacity no greater than the energy required to power said CPU, memory, and mass storage for 30 minutes of operation at the maximum rated speed of the CPU;

(b) a peripheral console comprising a power supply; and

(c) interconnection circuitry coupled to said computing module and to said peripheral console for conveying electrical power and signals between said computing module and said peripheral console,

wherein said peripheral console further comprises a low-voltage differential signaling (LVDS) channel comprising multiple pairs of unidirectional, serial bit channels to transmit data in opposite directions,

wherein said LVDS channel is configured to communicate an encoded serial bit stream of Peripheral Component Interconnect bus transaction.

76. (New) The apparatus of claim 75 wherein said interconnection circuitry is coupled to said LVDS channel to encode Peripheral Component Interconnect bus transaction data as said encoded serial bit stream.

77-85. (Cancelled)

86. (New) The apparatus of claim 49 further comprising an integrated interface controller and north bridge unit to communicate said encoded Peripheral Component Interconnect bus transaction data, said integrated interface controller and north bridge unit is coupled to said CPU without any intervening Peripheral Component Interconnect bus, and said LVDS channel directly extends from said integrated interface controller and north bridge unit to convey said encoded Peripheral Component Interconnect bus transaction data.

87. (New) The apparatus of claim 86 wherein said memory corresponds to a main memory that is coupled to said CPU through said integrated interface controller and north bridge unit.

88. (New) The apparatus of claim 86 wherein said encoded Peripheral Component Interconnect bus transaction data comprises address and data bits of Peripheral Component Interconnect bus transaction in serial form.

89. (New) The apparatus of claim 88 wherein said integrated interface controller and north bridge unit comprises a north bridge and an interface controller integrated with said north bridge, said interface controller is coupled to said CPU without any intervening Peripheral Component Interconnect bus, and said interface controller is configured to output said address and data bits of Peripheral Component Interconnect bus transaction in serial form that are conveyed over said LVDS channel.

90. (New) The apparatus of claim 89 wherein said LVDS channel comprises a first plurality of unidirectional, differential signal pairs to convey data in a first direction and a second plurality of unidirectional, differential signal pairs to convey data in a second, opposite direction.

91. (New) The apparatus of claim 57 further comprising a peripheral bridge to communicate said encoded address and data bits of Peripheral Component Interconnect bus transaction over said communication channel, and said peripheral bridge is directly coupled to said CPU.

92. (New) The apparatus of claim 91 wherein said peripheral bridge is coupled to said CPU without any intervening Peripheral Component Interconnect bus, and said communication channel directly extends from said peripheral bridge to convey said encoded address and data bits of Peripheral Component Interconnect bus transaction.

93. (New) The apparatus of claim 92 wherein said peripheral bridge comprises a north bridge.

94. (New) The apparatus of claim 93 wherein said peripheral bridge comprises an interface controller integrated with said north bridge, said interface controller is coupled to said CPU without any intervening Peripheral Component Interconnect bus, and said interface controller is configured to output said encoded address and data bits of Peripheral Component Interconnect bus transaction in serial form that are conveyed over said communication channel.

95. (New) The apparatus of claim 92 wherein said memory corresponds to a main memory that is coupled to said CPU through said peripheral bridge.

96. (New) The apparatus of claim 70 wherein said encoded Peripheral Component Interconnect bus transaction data comprises information to permit decoding to create a Peripheral Component Interconnect bus transaction.

97. (New) The apparatus of claim 70 wherein said LVDS channel corresponds to a first LVDS channel, and said detachable computing module comprises:

a second LVDS channel comprising a first unidirectional, serial bit channel to transmit data in a first direction and a second unidirectional, serial bit channel to transmit data in a second, opposite direction; and

a peripheral bridge coupled to said CPU without any intervening Peripheral Component Interconnect bus, said peripheral bridge comprising an integrated interface controller to communicate, over said second LVDS channel, encoded address and data bits of Peripheral Component Interconnect bus transaction in serial form.

98. (New) The apparatus of claim 97 wherein said integrated interface controller is configured to communicate said encoded address and data bits of Peripheral Component Interconnect bus transaction as 10 bit packets.

99. (New) The apparatus of claim 97 wherein said peripheral bridge comprises a north bridge.

100. (New) The apparatus of claim 97 wherein said integrated interface controller is coupled to said CPU without any intervening Peripheral Component Interconnect bus.

101. (New) The apparatus of claim 97 wherein said second LVDS channel directly extends from said integrated interface controller.

102. (New) The apparatus of claim 97 wherein said memory corresponds to a main memory that is coupled to said CPU through said peripheral bridge.

103. (New) The apparatus of claim 75 wherein said LVDS channel corresponds to a first LVDS channel, and said detachable computing module comprises:

an integrated interface controller and bridge unit to output encoded address and data bits of Peripheral Component Interconnect bus transaction in serial form, said integrated interface controller and bridge unit directly coupled to said CPU; and

a second LVDS channel coupled to said integrated interface controller and bridge unit to convey said encoded address and data bits of Peripheral Component Interconnect bus transaction in serial form.

104. (New) The apparatus of claim 103 wherein said second LVDS channel comprises a first plurality of unidirectional, differential signal pairs to convey data in a first direction and a second plurality of unidirectional, differential signal pairs to convey data in a second, opposite direction.

105. (New) The apparatus of claim 103 wherein said integrated interface controller and bridge unit comprises a north bridge and an interface controller integrated with said north bridge.

106. (New) The apparatus of claim 103 wherein said integrated interface controller and bridge unit is coupled to said CPU without any intervening Peripheral Component Interconnect bus.

107. (New) The apparatus of claim 106 wherein said second LVDS channel directly extends from said integrated interface controller and bridge unit.

108. (New) The apparatus of claim 107 wherein said memory corresponds to a main memory that is coupled to said CPU through said integrated interface controller and bridge unit.

109. (New) The apparatus of claim 103 wherein said first LVDS channel is configured to couple to said second LVDS channel.

110. (New) The apparatus of claim 103 wherein said interconnection circuitry comprises a pair of mating connectors.

REMARKS**I. INTRODUCTION:**

Claims 49-50, 56-59, 70-71, and 75-76 of U.S. Patent No. 6,216,185 (the "'185 patent'") were previously subject to reexamination, and currently stand rejected. Patent Owner respectfully traverses the rejections for the reasons set forth below. Claims 49-50, 56-59, 70-71, and 75-76 are unamended by this paper. New claims 86-110 are added by this paper.

For the reasons set forth below, Patent Owner respectfully submits that claims 49-50, 56-59, 70-71, 75-76, and 86-110 should be deemed patentable.

II. DRAWINGS AND SPECIFICATION:

The '185 patent incorporates by reference U.S. Application No. 09/149,882, now issued as U.S. Patent No. 6,345,330 (the "'330 patent'").¹ By this paper, the '185 patent is amended to include additional incorporated material from the '330 patent. Specifically, the '185 patent is amended to add new FIG. 13 and FIG. 14, as well as accompanying text. The added drawings and text correspond to: (a) FIG. 4 and FIG. 23 of the '330 patent; and (b) text of the '330 patent at col. 3, lines 51-53; col. 4, lines 35-36; col. 6, lines 30-35; and col. 15, line 10 to col. 16, line 5. For purposes of consistency, FIG. 4 of the '330 patent and its accompanying reference numbers having the format 4xx (e.g., integrated HIC and north bridge unit 405) are re-labeled as FIG. 13 and reference numbers having the format 13xx (e.g., integrated HIC and north bridge unit 1305). Likewise, FIG. 23 of the '330 patent is re-labeled as FIG. 14. Otherwise, Patent Owner respectfully submits that the added drawings and text correspond to the above-noted drawings and text of the '330 patent, and that no new matter is added.

III. STATUS OF CLAIMS AND SUPPORT FOR CLAIM CHANGES:

In accordance with Patent Owner's response filed on September 27, 2010, original claims 34, 36, 38, 40, and 42 were unamended, original claims 7, 14, and 21 were amended, original claims 1-6, 28-33, 35, 37, 39, and 41 were cancelled, and new claims 43-85 were added. In accordance with Patent Owner's response filed on May 3, 2011 and resubmission of Patent Owner's response filed on June 2, 2011, previously added claims 49, 56, 70, and 75 were amended, previously added claims 50, 57-59, 71, and 76 were unamended, and claims 7-27, 34, 36, 38, 40, 42-48, 51-55, 60-69, 72-74, and 77-85 were cancelled. In accordance with this

¹ See '185 patent at col. 1, lines 11-16 ("This application is being filed concurrently with the application of William W. Y. Chu for 'A Communication Channel and Interface Devices For Bridging Computer Interface Buses', U.S. application No. 09/149,882 filed on Sept. 8, 1998 and incorporates the material therein by reference") and col. 5, line 66 to col. 6, line 4 ("The preferred ACM-to-PCON Interconnection 300 is described in detail in a companion U.S. patent application, Ser. No. 09/149,882, entitled 'A Communication

paper, previously added claims 49-50, 56-59, 70-71, and 75-76 are unamended, and new claims 86-110 are added. Although previously added claims 49-50, 56-59, 70-71, and 75-76 are unamended, these claims are designated as "New" to reflect changes vis-à-vis the '185 patent.

New claim 49 was previously amended to be in independent form in accordance with Patent Owner's response filed on May 3, 2011 and resubmission of Patent Owner's response filed on June 2, 2011. Claim 49 is unamended by this paper.

New dependent claim 50 (dependent from claim 49) was previously added by Patent Owner's response filed on September 27, 2010, and support was set forth therein. Claim 50 is unamended by this paper.

New claim 56 was previously amended to be in independent form in accordance with Patent Owner's response filed on May 3, 2011 and resubmission of Patent Owner's response filed on June 2, 2011. Claim 56 is unamended by this paper.

New dependent claims 57-59 (dependent from claim 56) were previously added by Patent Owner's response filed on September 27, 2010, and support was set forth therein. Claims 57-59 are unamended by this paper.

New claim 70 was previously amended to be in independent form in accordance with Patent Owner's response filed on May 3, 2011 and resubmission of Patent Owner's response filed on June 2, 2011. Claim 70 is unamended by this paper.

New dependent claim 71 (dependent from claim 70) was previously added by Patent Owner's response filed on September 27, 2010, and support was set forth therein. Claim 71 is unamended by this paper.

New claim 75 was previously amended to be in independent form in accordance with Patent Owner's response filed on May 3, 2011 and resubmission of Patent Owner's response filed on June 2, 2011. Claim 75 is unamended by this paper.

New dependent claim 76 (dependent from claim 75) was previously added by Patent Owner's response filed on September 27, 2010, and support was set forth therein. Claim 76 is unamended by this paper.

New dependent claim 86 (dependent from claim 49) specifies "an integrated interface controller and north bridge unit to communicate said encoded Peripheral Component Interconnect bus transaction data, said integrated interface controller and north bridge unit is coupled to said CPU without any intervening Peripheral Component Interconnect bus, and said LVDS channel directly extends from said integrated interface controller and north bridge unit to convey said encoded Peripheral Component Interconnect bus transaction data." Support for this claim can be found, for example, in the '185 patent at FIG. 4; col. 5, line 57 to col. 6, line 13;

and col. 6, lines 31-40, as well as in the incorporated '330 patent at FIG. 4; FIG. 6; FIG. 23; col. 6, lines 30-35; col. 7, line 28 to col. 10, line 18; and col. 15, line 10 to col. 16, line 5.

New dependent claim 87 (dependent from claim 86) specifies that "said memory corresponds to a main memory that is coupled to said CPU through said integrated interface controller and north bridge unit." Support for this claim can be found, for example, in the '185 patent at FIG. 4 and col. 6, lines 31-44, as well as in the incorporated '330 patent at FIG. 4 and col. 6, lines 30-35.

New dependent claim 88 (dependent from claim 86) specifies that "said encoded Peripheral Component Interconnect bus transaction data comprises address and data bits of Peripheral Component Interconnect bus transaction in serial form." Support for this claim can be found, for example, in the '185 patent at col. 5, line 57 to col. 6, line 13, as well as in the incorporated '330 patent at col. 7, line 44 to col. 9, line 43.

New dependent claim 89 (dependent from claim 88) specifies that "said integrated interface controller and north bridge unit comprises a north bridge and an interface controller integrated with said north bridge, said interface controller is coupled to said CPU without any intervening Peripheral Component Interconnect bus, and said interface controller is configured to output said address and data bits of Peripheral Component Interconnect bus transaction in serial form that are conveyed over said LVDS channel." Support for this claim can be found, for example, in the '185 patent at col. 5, line 57 to col. 6, line 13, as well as in the incorporated '330 patent at FIG. 4; FIG. 6; FIG. 23; col. 6, lines 30-35; col. 7, line 44 to col. 9, line 43; and col. 15, line 10 to col. 16, line 5.

New dependent claim 90 (dependent from claim 89) specifies that "said LVDS channel comprises a first plurality of unidirectional, differential signal pairs to convey data in a first direction and a second plurality of unidirectional, differential signal pairs to convey data in a second, opposite direction." Support for this claim can be found, for example, in the '185 patent at col. 5, line 57 to col. 6, line 13, as well as in the incorporated '330 patent at FIG. 23 and col. 15, line 10 to col. 16, line 5.

New dependent claim 91 (dependent from claim 57) specifies "a peripheral bridge to communicate said encoded address and data bits of Peripheral Component Interconnect bus transaction over said communication channel, and said peripheral bridge is directly coupled to said CPU." Support for this claim can be found, for example, in the '185 patent at FIG. 4; col. 5, line 57 to col. 6, line 13; and col. 6, lines 31-40, as well as in the incorporated '330 patent at FIG. 4; FIG. 6; FIG. 23; col. 6, lines 30-35; col. 7, line 28 to col. 10, line 18; and col. 15, line 10 to col. 16, line 5.

New dependent claim 92 (dependent from claim 91) specifies that "said peripheral bridge is coupled to said CPU without any intervening Peripheral Component Interconnect bus, and said communication channel directly extends from said peripheral bridge to convey said encoded address and data bits of Peripheral Component Interconnect bus transaction." Support for this claim can be found, for example, in the '185 patent at FIG. 4; col. 5, line 57 to col. 6, line 13; and col. 6, lines 31-40, as well as in the incorporated '330 patent at FIG. 4; FIG. 6; FIG. 23; col. 6, lines 30-35; col. 7, line 44 to col. 9, line 43; and col. 15, line 10 to col. 16, line 5.

New dependent claim 93 (dependent from claim 92) specifies that "said peripheral bridge comprises a north bridge." Support for this claim can be found, for example, in the '185 patent at FIG. 4; col. 5, line 57 to col. 6, line 13; and col. 6, lines 31-40, as well as in the incorporated '330 patent at FIG. 4 and col. 6, lines 30-35.

New dependent claim 94 (dependent from claim 93) specifies that "said peripheral bridge comprises an interface controller integrated with said north bridge, said interface controller is coupled to said CPU without any intervening Peripheral Component Interconnect bus, and said interface controller is configured to output said encoded address and data bits of Peripheral Component Interconnect bus transaction in serial form that are conveyed over said communication channel." Support for this claim can be found, for example, in the '185 patent at col. 5, line 57 to col. 6, line 13, as well as in the incorporated '330 patent at FIG. 4; FIG. 6; FIG. 23; col. 6, lines 30-35; col. 7, line 44 to col. 9, line 43; and col. 15, line 10 to col. 16, line 5.

New dependent claim 95 (dependent from claim 92) specifies that "said memory corresponds to a main memory that is coupled to said CPU through said peripheral bridge." Support for this claim can be found, for example, in the '185 patent at FIG. 4 and col. 6, lines 31-44, as well as in the incorporated '330 patent at FIG. 4 and col. 6, lines 30-35.

New dependent claim 96 (dependent from claim 70) specifies that "said encoded Peripheral Component Interconnect bus transaction data comprises information to permit decoding to create a Peripheral Component Interconnect bus transaction." Support for this claim can be found, for example, in the '185 patent at col. 5, line 57 to col. 6, line 13, as well as in the incorporated '330 patent at col. 7, line 44 to col. 9, line 43.

New dependent claim 97 (dependent from claim 70) specifies that "said LVDS channel corresponds to a first LVDS channel, and said detachable computing module comprises:" (1) "a second LVDS channel comprising a first unidirectional, serial bit channel to transmit data in a first direction and a second unidirectional, serial bit channel to transmit data in a second, opposite direction;" and (2) "a peripheral bridge coupled to said CPU without any intervening Peripheral Component Interconnect bus, said peripheral bridge comprising an integrated interface controller to communicate, over said second LVDS channel, encoded address and data bits of Peripheral Component Interconnect bus transaction in serial form." Support for this

claim can be found, for example, in the '185 patent at FIG. 4; col. 5, line 57 to col. 6, line 13; and col. 6, lines 31-40, as well as in the incorporated '330 patent at FIG. 4; FIG. 6; FIG. 23; col. 6, lines 30-35; col. 7, line 28 to col. 10, line 18; and col. 15, line 10 to col. 16, line 5.

New dependent claim 98 (dependent from claim 97) specifies that "said integrated interface controller is configured to communicate said encoded address and data bits of Peripheral Component Interconnect bus transaction as 10 bit packets." Support for this claim can be found, for example, in the '185 patent at col. 5, line 57 to col. 6, line 13, as well as in the incorporated '330 patent at col. 8, line 61 to col. 9, line 15 and col. 9, lines 31-43.

New dependent claim 99 (dependent from claim 97) specifies that "said peripheral bridge comprises a north bridge." Support for this claim can be found, for example, in the '185 patent at FIG. 4; col. 5, line 57 to col. 6, line 13; and col. 6, lines 31-40, as well as in the incorporated '330 patent at FIG. 4 and col. 6, lines 30-35.

New dependent claim 100 (dependent from claim 97) specifies that "said integrated interface controller is coupled to said CPU without any intervening Peripheral Component Interconnect bus." Support for this claim can be found, for example, in the '185 patent at FIG. 4; col. 5, line 57 to col. 6, line 13; and col. 6, lines 31-40, as well as in the incorporated '330 patent at FIG. 4 and col. 6, lines 30-35.

New dependent claim 101 (dependent from claim 97) specifies that "said second LVDS channel directly extends from said integrated interface controller." Support for this claim can be found, for example, in the '185 patent at col. 5, line 57 to col. 6, line 13, as well as in the incorporated '330 patent at FIG. 4; FIG. 6; FIG. 23; col. 6, lines 30-35; and col. 15, line 10 to col. 16, line 5.

New dependent claim 102 (dependent from claim 97) specifies that "said memory corresponds to a main memory that is coupled to said CPU through said peripheral bridge." Support for this claim can be found, for example, in the '185 patent at FIG. 4 and col. 6, lines 31-44, as well as in the incorporated '330 patent at FIG. 4 and col. 6, lines 30-35.

New dependent claim 103 (dependent from claim 75) specifies that "said LVDS channel corresponds to a first LVDS channel, and said detachable computing module comprises:" (1) "an integrated interface controller and bridge unit to output encoded address and data bits of Peripheral Component Interconnect bus transaction in serial form, said integrated interface controller and bridge unit directly coupled to said CPU;" and (2) "a second LVDS channel coupled to said integrated interface controller and bridge unit to convey said encoded address and data bits of Peripheral Component Interconnect bus transaction in serial form." Support for this claim can be found, for example, in the '185 patent at FIG. 4; col. 5, line 57 to col. 6, line 13; and col. 6, lines

31-40, as well as in the incorporated '330 patent at FIG. 4; FIG. 6; FIG. 23; col. 6, lines 30-35; col. 7, line 28 to col. 10, line 18; and col. 15, line 10 to col. 16, line 5.

New dependent claim 104 (dependent from claim 103) specifies that "said second LVDS channel comprises a first plurality of unidirectional, differential signal pairs to convey data in a first direction and a second plurality of unidirectional, differential signal pairs to convey data in a second, opposite direction." Support for this claim can be found, for example, in the '185 patent at col. 5, line 57 to col. 6, line 13, as well as in the incorporated '330 patent at FIG. 23 and col. 15, line 10 to col. 16, line 5.

New dependent claim 105 (dependent from claim 103) specifies that "said integrated interface controller and bridge unit comprises a north bridge and an interface controller integrated with said north bridge." Support for this claim can be found, for example, in the '185 patent at FIG. 4; col. 5, line 57 to col. 6, line 13; and col. 6, lines 31-40, as well as in the incorporated '330 patent at FIG. 4 and col. 6, lines 30-35.

New dependent claim 106 (dependent from claim 103) specifies that "said integrated interface controller and bridge unit is coupled to said CPU without any intervening Peripheral Component Interconnect bus." Support for this claim can be found, for example, in the '185 patent at FIG. 4; col. 5, line 57 to col. 6, line 13; and col. 6, lines 31-40, as well as in the incorporated '330 patent at FIG. 4 and col. 6, lines 30-35.

New dependent claim 107 (dependent from claim 106) specifies that "said second LVDS channel directly extends from said integrated interface controller and bridge unit." Support for this claim can be found, for example, in the '185 patent at col. 5, line 57 to col. 6, line 13, as well as in the incorporated '330 patent at FIG. 4; FIG. 6; FIG. 23; col. 6, lines 30-35; and col. 15, line 10 to col. 16, line 5.

New dependent claim 108 (dependent from claim 107) specifies that "said memory corresponds to a main memory that is coupled to said CPU through said integrated interface controller and bridge unit." Support for this claim can be found, for example, in the '185 patent at FIG. 4 and col. 6, lines 31-44, as well as in the incorporated '330 patent at FIG. 4 and col. 6, lines 30-35.

New dependent claim 109 (dependent from claim 103) specifies that "said first LVDS channel is configured to couple to said second LVDS channel." Support for this claim can be found, for example, in the '185 patent at FIG. 3 and col. 5, line 57 to col. 6, line 13, as well as in the incorporated '330 patent at FIG. 2; FIG. 23; col. 6, lines 22-25; and col. 15, line 10 to col. 16, line 5.

New dependent claim 110 (dependent from claim 103) specifies that "said interconnection circuitry comprises a pair of mating connectors." Support for this claim can be found, for example, in the '185 patent at FIG. 6 and col. 12, lines 30-35.

IV. CLAIM REJECTIONS:

Claims 49-50, 56-59, 70-71, and 75-76 stand rejected as allegedly unpatentable over Hitachi '953 (Japanese Patent Application Publication No. H6-289953) in view of Tripathi (U.S. Patent No. 6,161,157) and Hong (U.S. Patent No. 5,764,924). The Examiner effectively concedes that Hitachi '953 fails to disclose claimed features related to a "LVDS" channel (or the conveyance of a "LVDS" bit stream), and relies upon Tripathi as allegedly curing the deficiencies of Hitachi '953.

Patent Owner respectfully requests withdrawal of the rejections, at least because Tripathi fails to qualify as prior art against the '185 patent. The '185 patent issued from U.S. Patent Application No. 09/149,548, which was filed on September 8, 1998 and claims the benefit of U.S. Provisional Application Nos. 60/083,886 and 60/092,706, which were filed on May 1, 1998 and July 14, 1998, respectively.² Tripathi was filed on October 27, 1998 and issued on December 12, 2000. Both the filing date and issuance date of Tripathi are subsequent to the filing dates of May 1, 1998 and July 14, 1998 of the provisional applications to which priority is claimed by the '185 patent, and also subsequent to the filing date of September 8, 1998 of the non-provisional application that issued as the '185 patent. Thus, Tripathi postdates the filing of the '185 patent and fails to qualify as prior art against the '185 patent. In the absence of Tripathi, Patent Owner respectfully submits that the Examiner has failed to establish a *prima facie* case of obviousness of claims 49-50, 56-59, 70-71, and 75-76.³

New claims 86-90 are dependent from claim 49, and should be deemed patentable for at least the reasons applicable for claim 49.

New claims 91-95 are dependent from claim 57, and should be deemed patentable for at least the reasons applicable for claim 57.

New claims 96-102 are dependent from claim 70, and should be deemed patentable for at least the reasons applicable for claim 70.

New claims 103-110 are dependent from claim 75, and should be deemed patentable for at least the reasons applicable for claim 75.

² Like the '185 patent, the incorporated '330 patent was filed on September 8, 1998 and claims the benefit of U.S. Provisional Application Nos. 60/083,886 and 60/092,706, which were filed on May 1, 1998 and July 14, 1998, respectively.

³ See M.P.E.P. (8th Edition, Latest Revision July 2010) §2142 ("The examiner bears the initial burden of factually supporting any *prima facie* conclusion of obviousness. If the examiner does not produce a *prima facie* case, the applicant is under no obligation to submit evidence of nonobviousness.").

V. CONCLUSIONS:

For the reasons set forth in this paper, Patent Owner respectfully submits that claims 49-50, 56-59, 70-71, 75-76, and 86-110 should be deemed patentable.

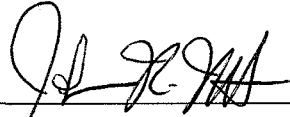
The Director is hereby authorized to charge any appropriate fees under 37 C.F.R. §§1.16, 1.17, 1.20, and 1.21 that may be required by this paper, and to credit any overpayment, to Deposit Account No. 50-1283.

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Customer No. 58249
COOLEY LLP
777 6th Street NW, Suite 1100
Washington, DC 20001
Tel: (703) 456-8000
Fax: (202) 842-7899

Respectfully submitted,
COOLEY LLP

By: _____


John R. Mills
Reg. No. 56,414

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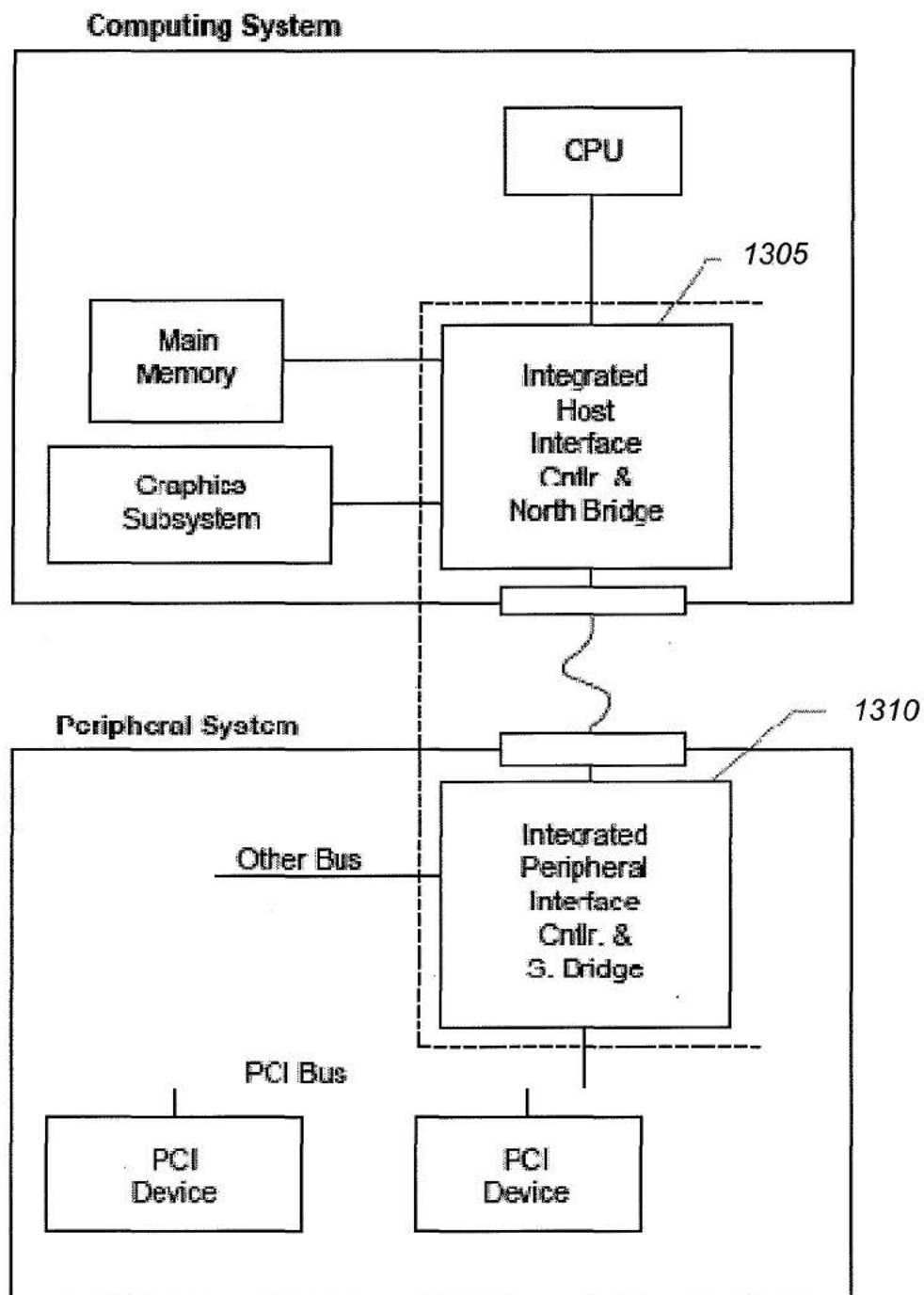


FIG. 13
NEW

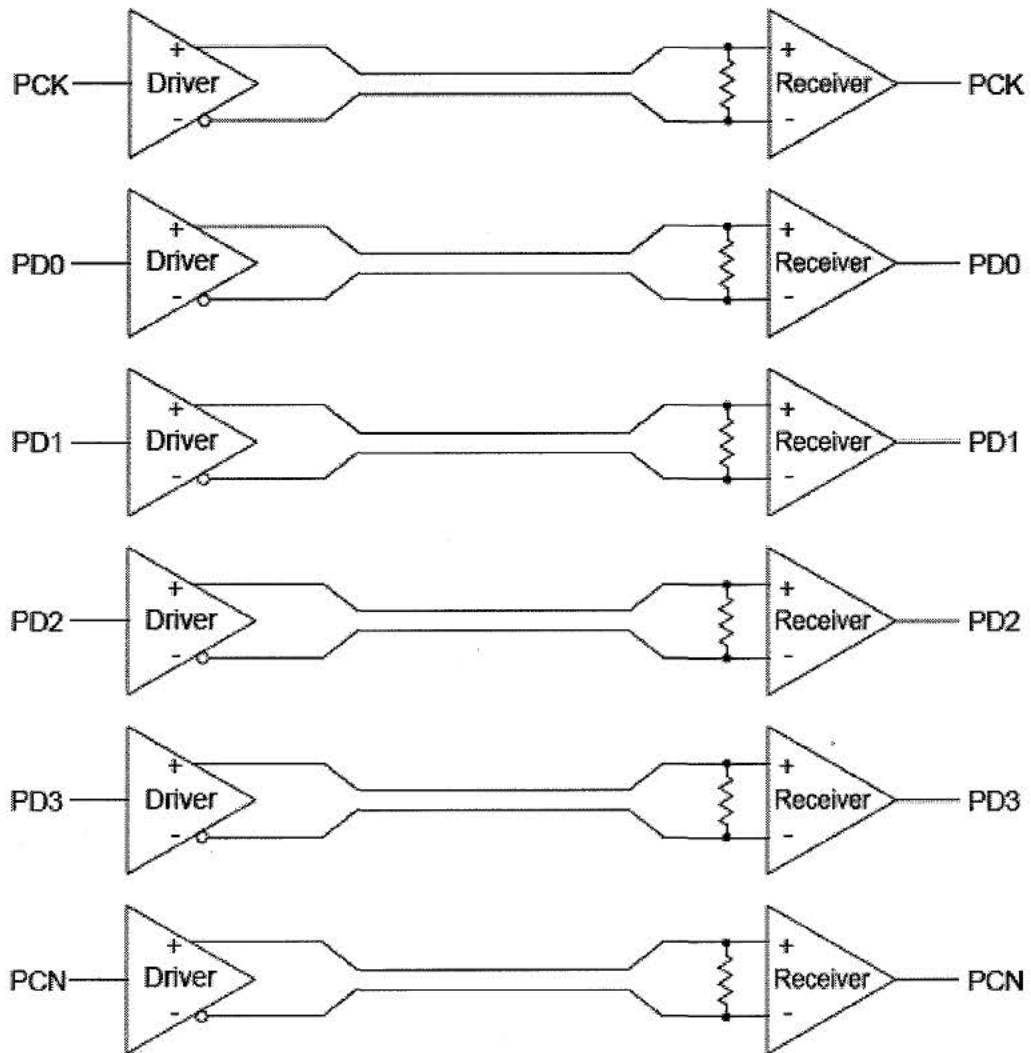


FIG. 14
NEW