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REISSUE PATENT APPLICATION TRANSMITTAL

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	First Named Inventor	William W. Y. Chu
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APPLICATION FOR REISSUE OF:

(Check applicable box)



Utility Patent



Design Patent



Plant Patent

APPLICATION ELEMENTS (37 CFR 1.173)

1. ☐ Fee Transmittal Form (PTO/SB/56)
2. ☐ Applicant claims small entity status. See 37 CFR 1.27.
3. ☒ Specification and Claims in double column copy of patent format (amended, if appropriate)
4. ☒ Drawing(s) (proposed amendments, if appropriate)
5. ☒ Reissue Oath/Declaration (original or copy) (37 C.F.R. 1.175) (PTO/SB/51 or 52)
6. ☒ Power of Attorney
7. ☒ Original U.S. Patent currently assigned? ☒ Yes ☐ No
(If Yes, check applicable box(es))
☒ Written Consent of all Assignees (PTO/SB/53)
☒ 37 C.F.R. 3.73(b) Statement (PTO/SB/96)
8. ☐ CD-ROM or CD-R in duplicate, Computer Program (Appendix) or large table
☐ Landscape Table on CD
9. Nucleotide and/or Amino Acid Sequence Submission (if applicable, items a. - c. are required)
a. ☐ Computer Readable Form (CFR)
b. Specification Sequence Listing on:
i) ☐ CD-ROM (2 copies) or CD-R (2 copies); or
ii) ☐ Paper
c. ☐ Statements verifying identity of above copies

ACCOMPANYING APPLICATION PARTS

10. ☒ Statement of status and support for all changes to the claims. See 37 CFR 1.173.(c).
11. ☐ Foreign Priority Claim (35 U.S.C. 119) (if applicable)
12. ☒ Information Disclosure Statement (IDS) PTO/SB/08 or PTO-1449
☒ Copies of foreign patent documents, publications & other information
13. ☐ English Translation of Reissue Oath/Declaration (if applicable)
14. ☒ Preliminary Amendment
15. ☐ Return Receipt Postcard (MPEP 503) (Should be specifically itemized)
16. Other:

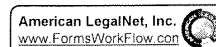
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Chu

(10) **Patent No.:** **US 6,643,777 B1**
(45) **Date of Patent:** **Nov. 4, 2003**

(54) **DATA SECURITY METHOD AND DEVICE
FOR COMPUTER MODULES**

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(22) Filed: **May 14, 1999**

(51) Int. Cl.⁷ **G06F 9/00**

(52) U.S. Cl. **713/200; 713/201; 707/9**

(58) **Field of Search** 713/200, 176,
713/202, 186, 193, 194; 707/9; 361/686,
683; 382/176; 710/303

(56) **References Cited**

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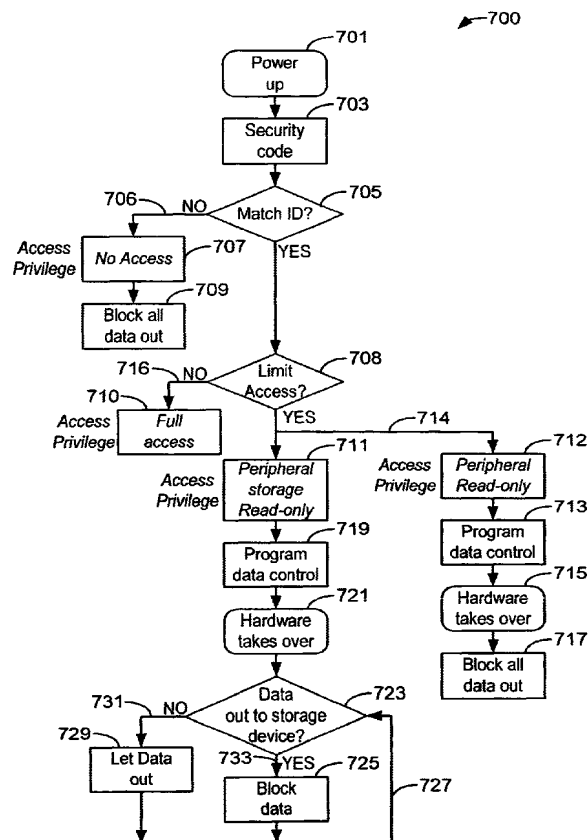
Primary Examiner—Ly V. Hua

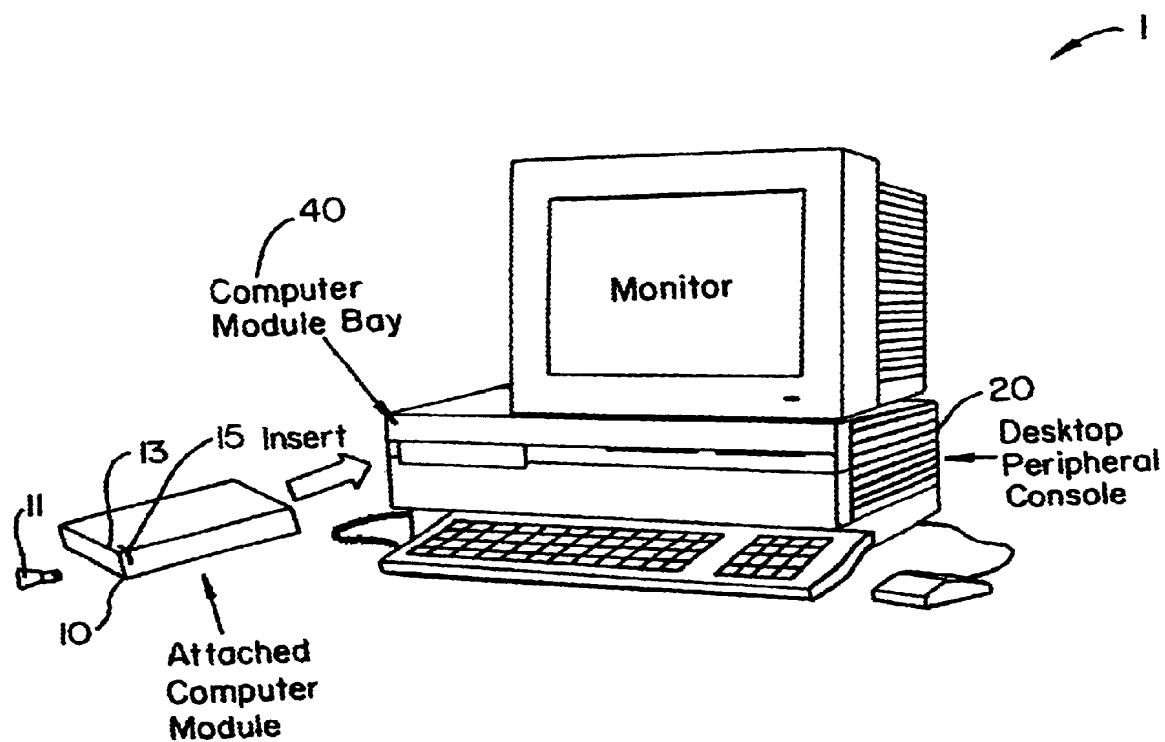
(74) *Attorney, Agent, or Firm*—Townsend and Townsend
and Crew LLP

(57) **ABSTRACT**

A security method for an attached computer module in a computer system. The security method reads a security identification number in an attached computer module and compares it to a security identification number in a console, which houses the attached computer module. Based upon a relationship between these numbers, a security status is selected. The security status determines the security level of operating the computer system.

13 Claims, 8 Drawing Sheets



**FIG. 1**

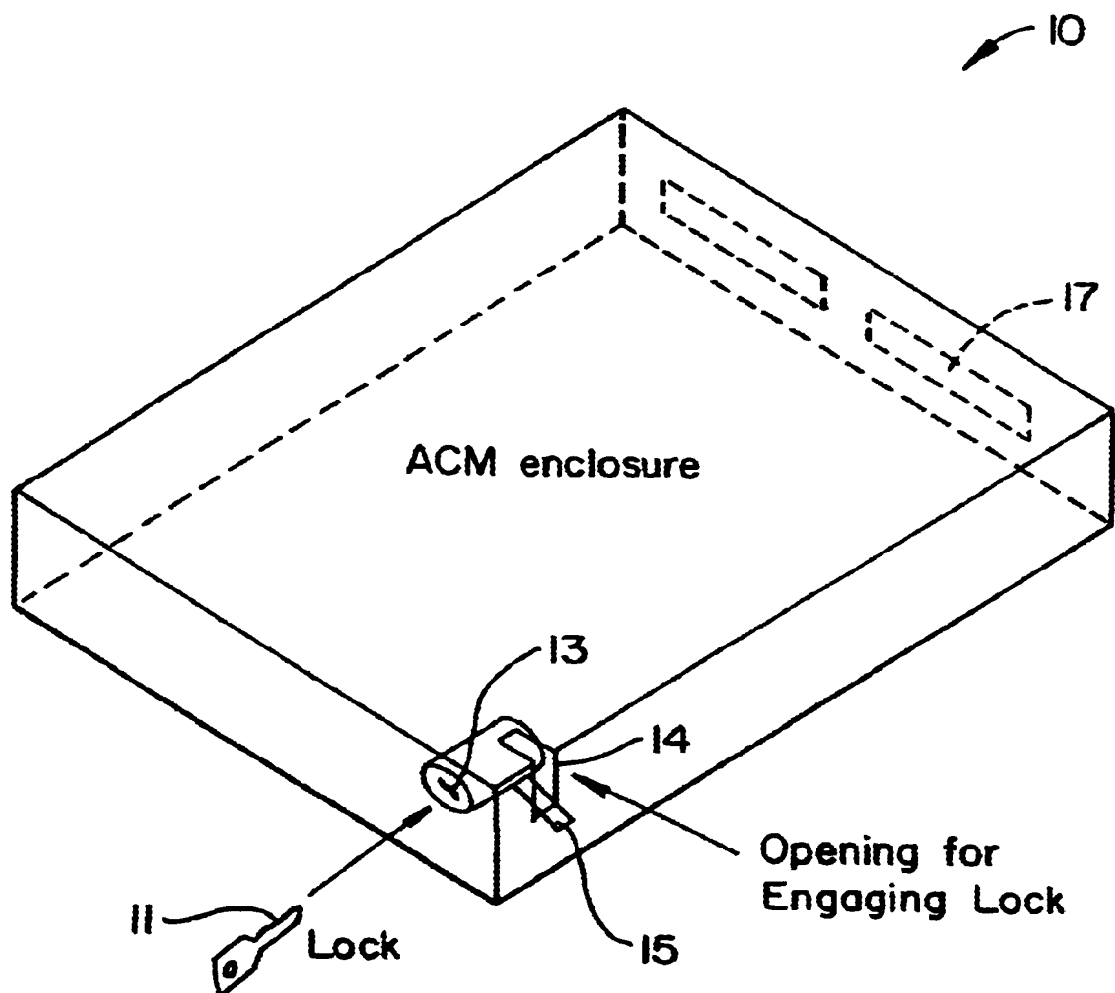


FIG 2

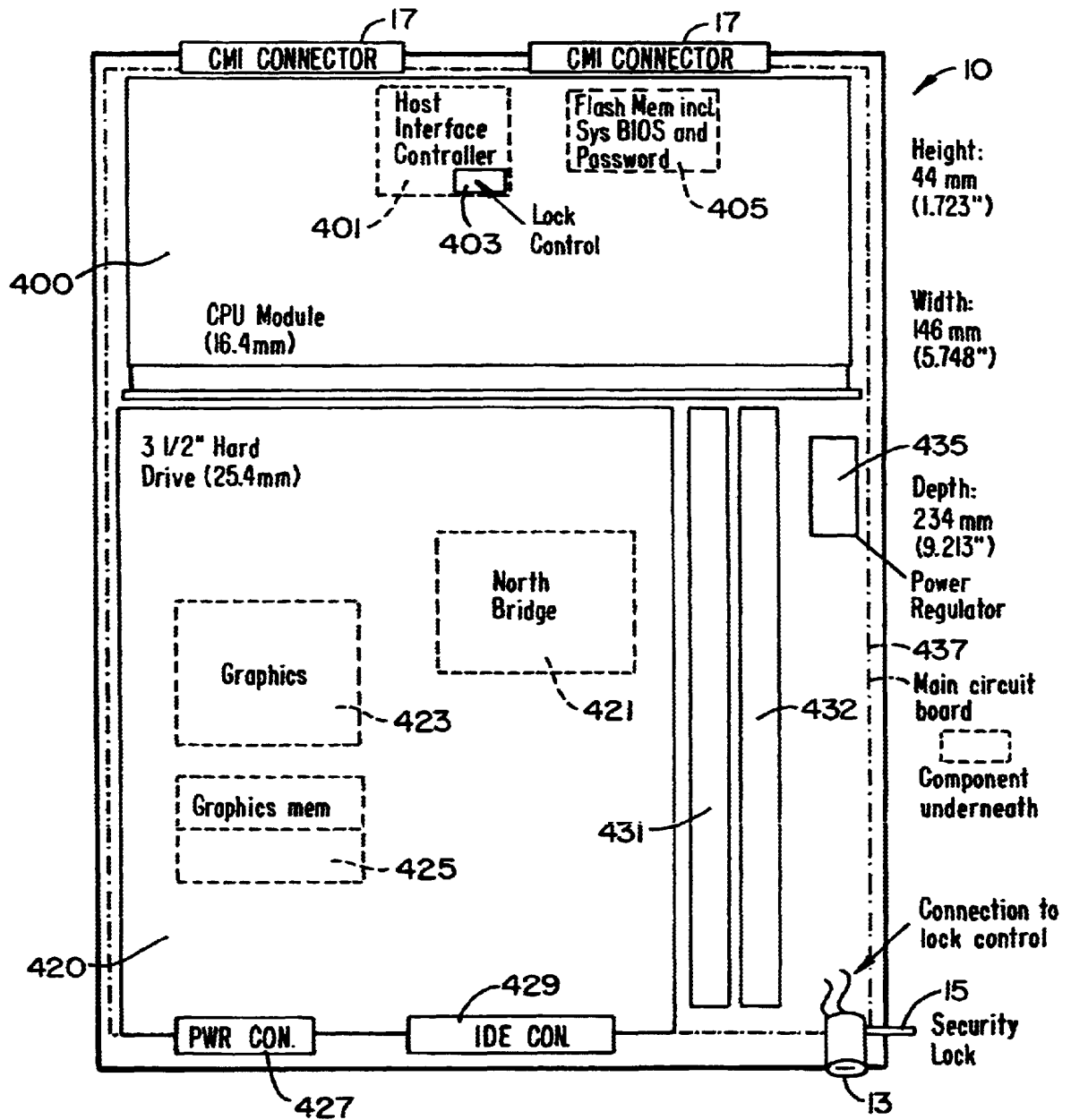
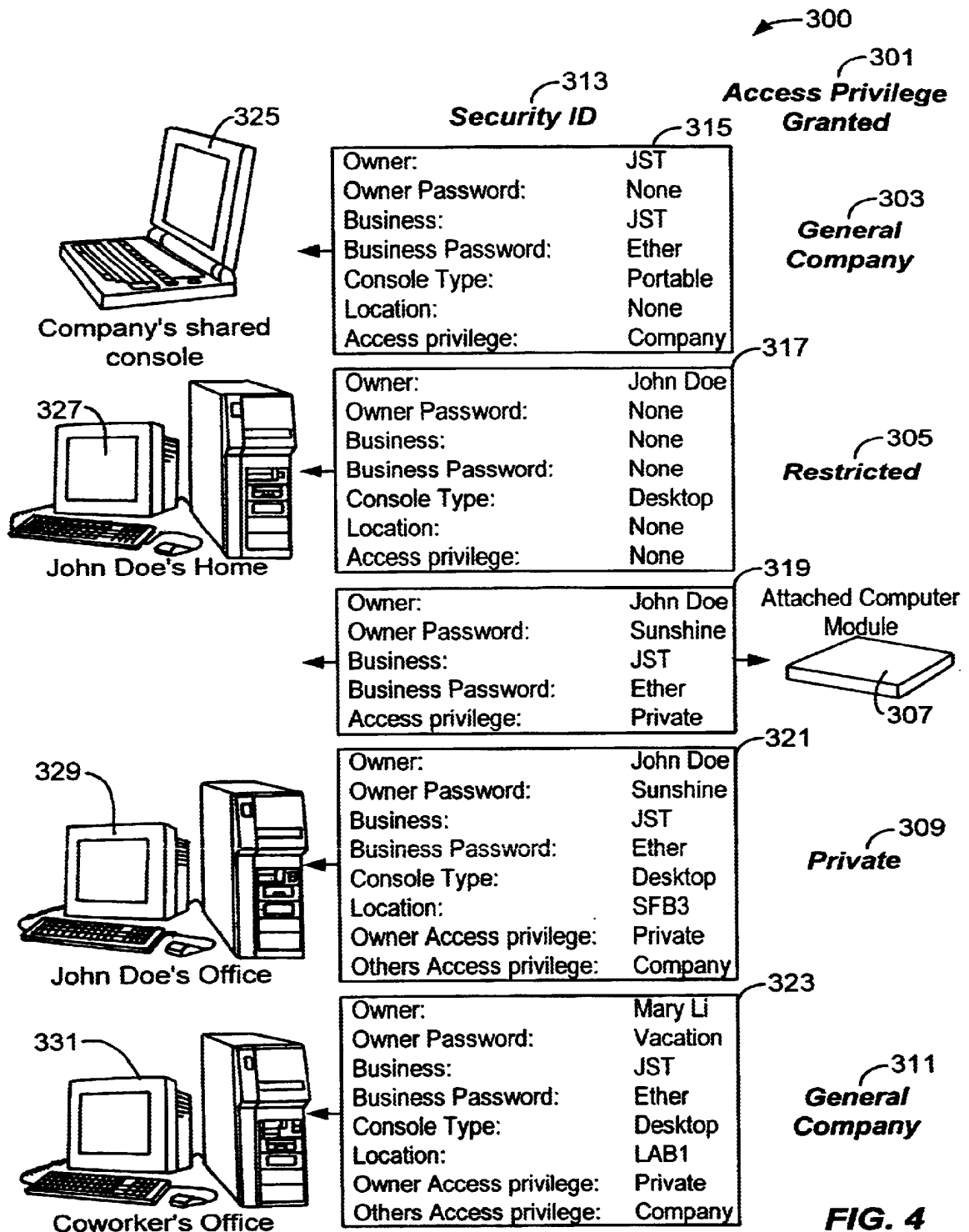
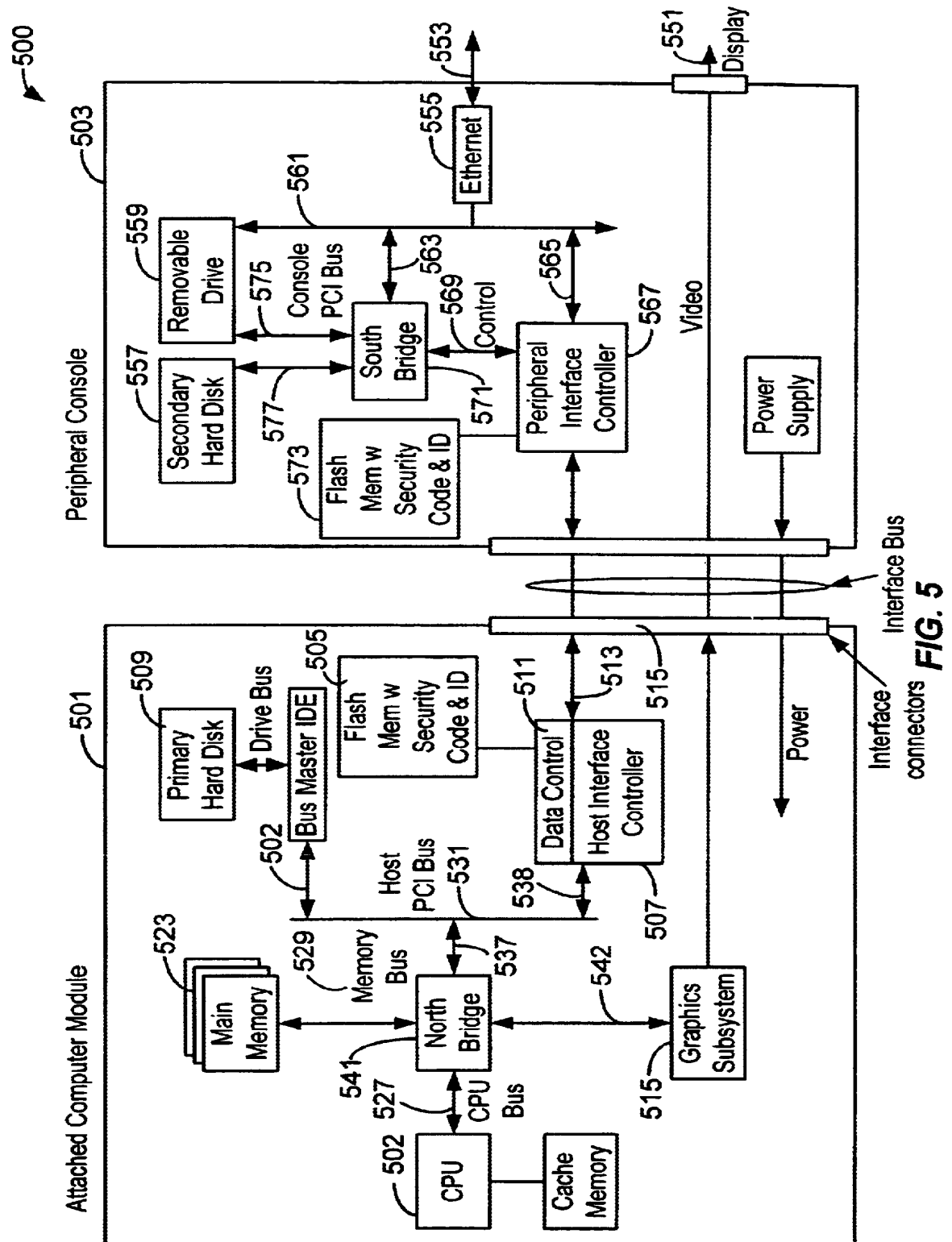


FIG. 3





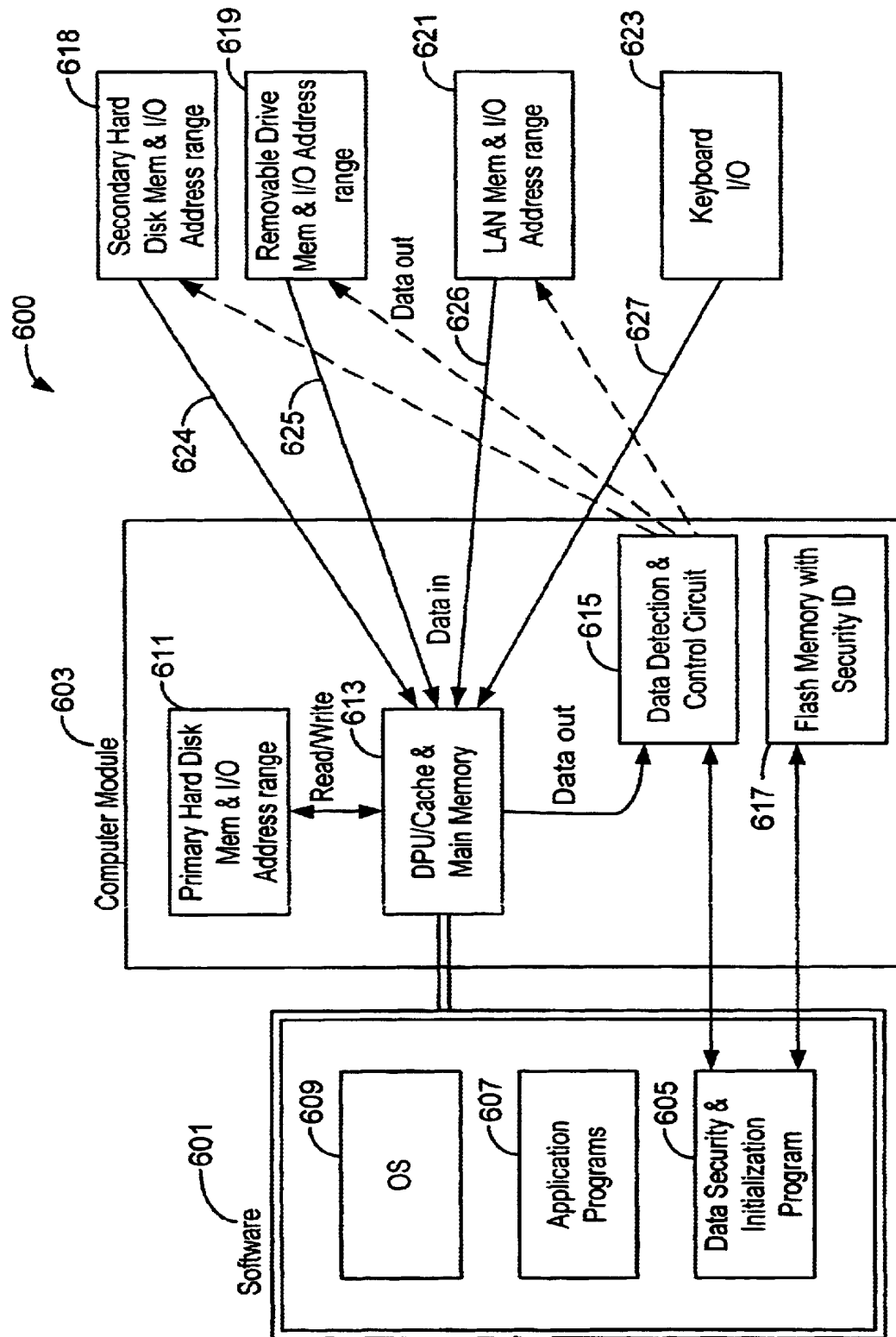


FIG. 6

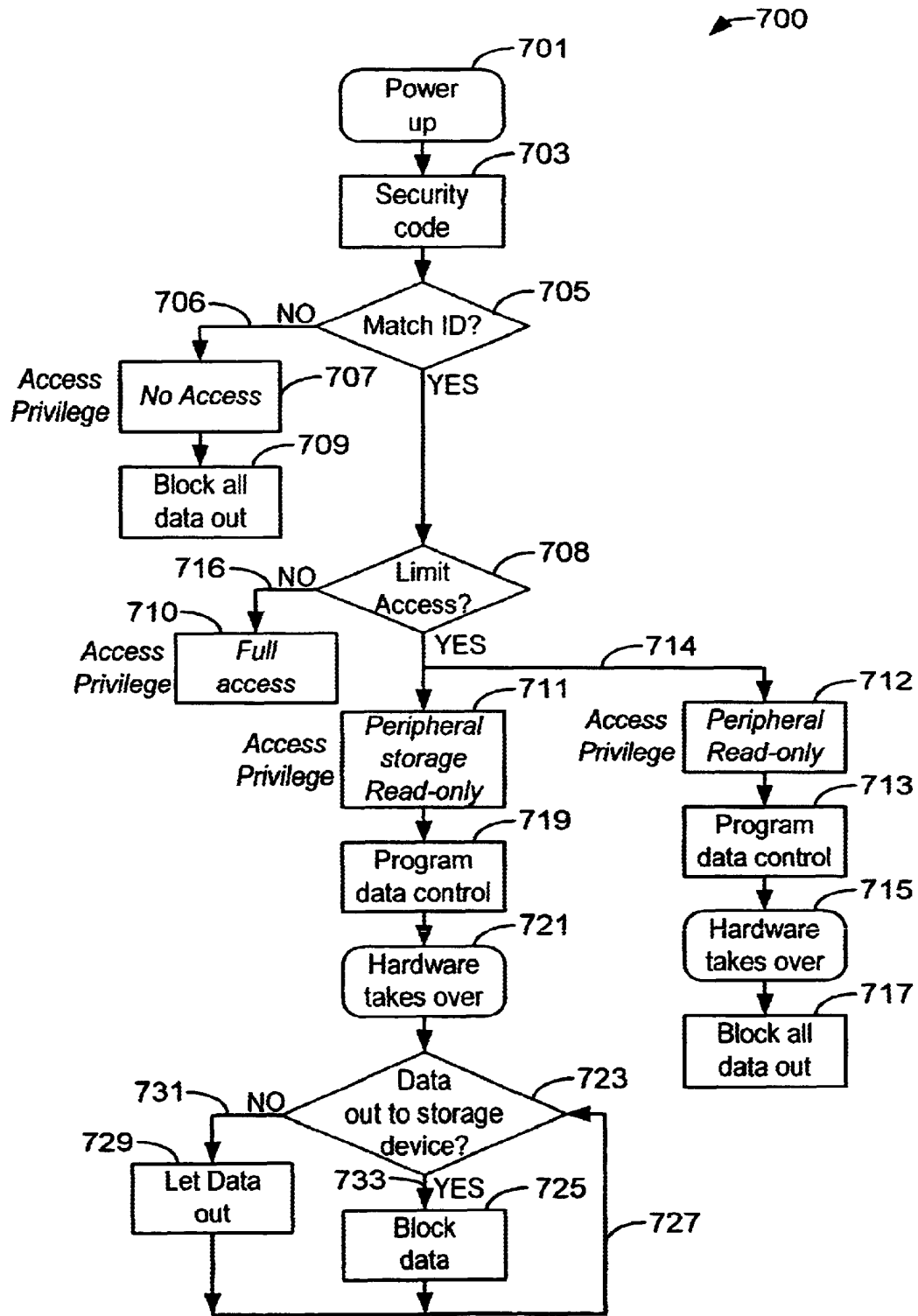


FIG. 7

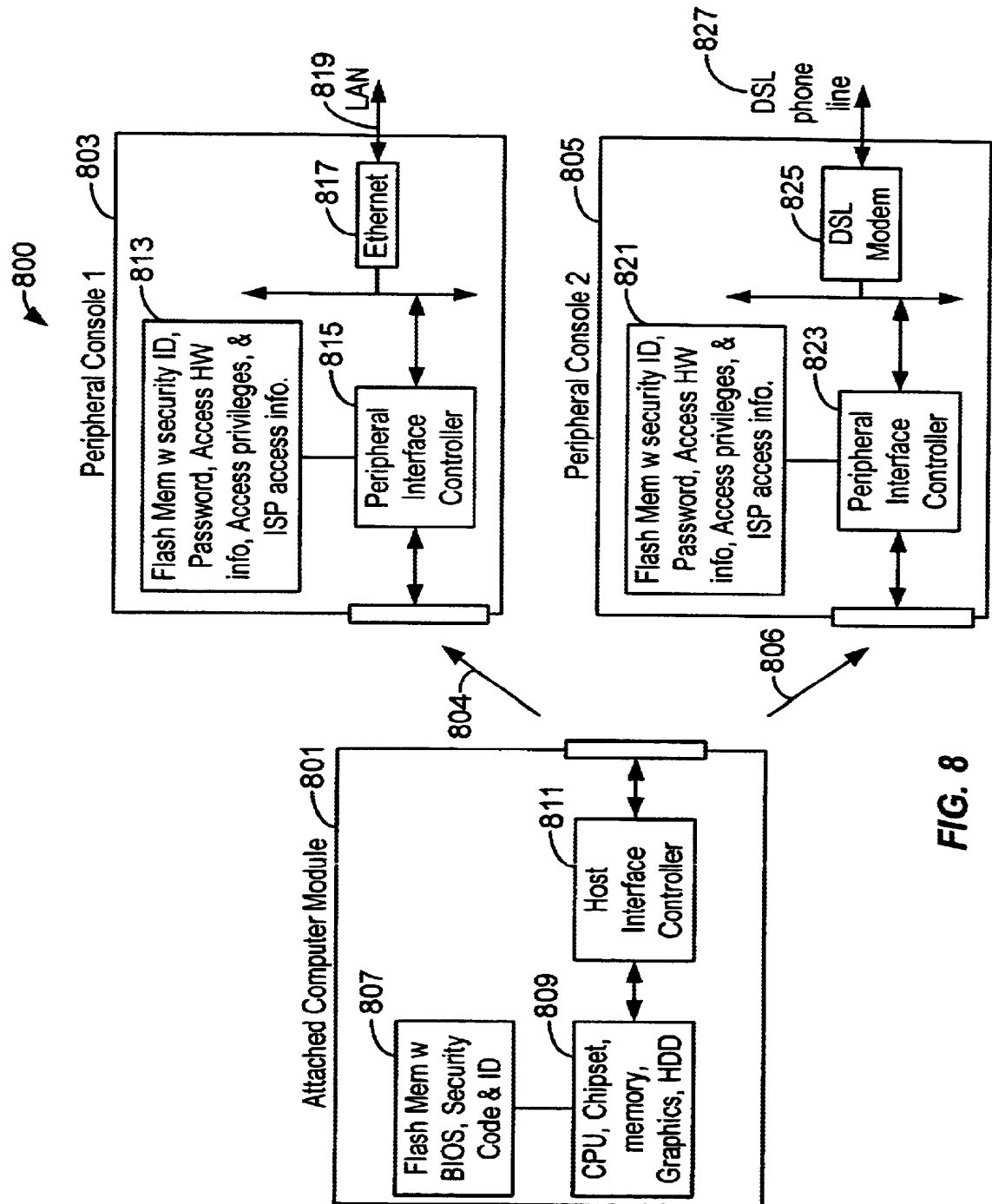


FIG. 8

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DATA SECURITY METHOD AND DEVICE FOR COMPUTER MODULES

BACKGROUND OF THE INVENTION

The present invention relates to computing devices. More particularly, the present invention provides a method and device for securing a personal computer or set-top box. Merely by way of example, the present invention is applied to a modular computing environment for desk top computers, but it will be recognized that the invention has a much wider range of applicability. It can be applied to other portable or modular computing applications.

Many desktop or personal computers, which are commonly termed PCs, have been around and used for over ten years. The PCs often come with state-of-art microprocessors such as the Intel Pentium™ microprocessor chips. They also include a hard or fixed disk drive including memory in the giga-byte range. Additionally, the PCs often include a random access memory integrated circuit device such as a dynamic random access memory device, which is commonly termed DRAM. The DRAM devices now provide up to millions of memory cells (i.e., mega-bit) on a single slice of silicon. PCs also include a high resolution display such as cathode ray tubes or CRTs. In most cases, the CRTs are at least 15 inches or 17 inches or 19 inches in diameter. High resolution flat panel displays are also used with PCs.

Many external or peripheral devices can be used with the PCs. Among others, these peripheral devices include mass storage devices such as a Zip™ Drive product sold by Iomega Corporation of Utah. Other storage devices include external hard drives, tape drives, and others. Additional devices include communication devices such as a modem, which can be used to link the PC to a wide area network of computers such as the Internet. Furthermore, the PC can include output devices such as a printer and other output means. Moreover, the PC can include special audio output devices such as speakers the like.

PCs also have easy to use keyboards, mouse input devices, and the like. The keyboard is generally configured similar to a typewriter format. The keyboard also has the length and width for easily inputting information by way of keys to the computer. The mouse also has a sufficient size and shape to easily move a cursor on the display from one location to another location.

Other types of computing devices include portable computing devices such as "laptop" computers and the like. Although somewhat successful, laptop computers have many limitations. These computing devices have expensive display technology. In fact, these devices often have a smaller flat panel display that has poor viewing characteristics. Additionally, these devices also have poor input devices such as smaller keyboards and the like. Furthermore, these devices have limited common platforms to transfer information to and from these devices and other devices such as PCs.

Up to now, there has been little common ground between these platforms including the PCs and laptops in terms of upgrading, ease-of-use, cost, performance, and the like. Many differences between these platforms, probably somewhat intentional, has benefited computer manufacturers at the cost of consumers. A drawback to having two separate computers is that the user must often purchase both the desktop and laptop to have "total" computing power, where the desktop serves as a "regular" computer and the laptop serves as a "portable" computer. Purchasing both computers

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is often costly and runs "thousands" of dollars. The user also wastes a significant amount of time transferring software and data between the two types of computers. For example, the user must often couple the portable computer to a local area network (i.e., LAN), to a serial port with a modem and then manually transfer over files and data between the desktop and the portable computer. Alternatively, the user often must use floppy disks to "zip" up files and programs that exceed the storage capacity of conventional floppy disks, and transfer the floppy disk data manually.

Another drawback with the current model of separate portable and desktop computer is that the user has to spend money to buy components and peripherals that are duplicated in at least one of these computers. For example, both the desktop and portable computers typically include hard disk drives, floppy drives, CD-ROMs, computer memory, host processors, graphics accelerators, and the like. Because program software and supporting programs generally must be installed upon both hard drives in order for the user to operate programs on the road and in the office, hard disk space is often wasted.

One approach to reduce some of these drawbacks has been the use of a docking station with a portable computer. Here, the user has the portable computer for "on the road" use and a docking station that houses the portable computer for office use. The docking station typically includes a separate monitor, keyboard, mouse, and the like and is generally incompatible with other desktop PCs. The docking station is also generally not compatible with portable computers of other vendors. Another drawback to this approach is that the portable computer typically has lower performance and functionality than a conventional desktop PC. For example, the processor of the portable is typically much slower than processors in dedicated desktop computers, because of power consumption and heat dissipation concerns. As an example, it is noted that at the time of drafting of the present application, some top-of-the-line desktops include 400 MHz processors, whereas top-of-the-line notebook computers include 266 MHz processors.

Another drawback to the docking station approach is that the typical cost of portable computers with docking stations can approach the cost of having a separate portable computer and a separate desktop computer. Further, as noted above, because different vendors of portable computers have proprietary docking stations, computer users are held captive by their investments and must rely upon the particular computer vendor for future upgrades, support, and the like.

To date, most personal computers provide data file security through software only. A wide variety of removable storage media are available for a personal computer. These removable media do not provide any access security protection in hardware. Data encryption program often must be used for protection. Such program is cumbersome to handle for the user requiring extra cost and time. Data encryption is more commonly used for communication over an unprotected network or the Internet. Having a large number of frequently used files managed by encryption software is not practical. Without software security program, any file can be read and copied illegally from a hard disk drive on a PC or any removable media.

PC architecture generally allows freedom of data flow between memory and peripheral devices within the allowed memory and I/O address spaces. In conventional PC architecture, a peripheral bus, i.e. PCI bus, is used to control all data transactions among peripheral devices. PCI bus allows any device to be a bus master and perform data

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transaction with another device. Also when a software program is in control, it can move data between any two devices. There is no hardware or protocol security mechanism on a standard peripheral bus such as PCI Bus to detect or block data transactions. Operating system may have individual files read or write protected. These types of special security feature require significant additional user interaction to control. This is too cumbersome for a typical user to manage. There is no mechanism in current PCs to allow access to the primary hard disk drive and yet prevent copying of its content. The conventional PC is a single machine that does not have a mechanism to perform security ID matching in hardware.

Thus, what is needed are computer systems that provide improved security features to prevent illegal or unauthorized access to information.

SUMMARY OF THE INVENTION

According to the present invention, a technique including a method and device for securing a computer module in a computer system is provided. In an exemplary embodiment, the present invention provides a security system for an attached computer module ("ACM"). In an embodiment, the ACM inserts into a computer module bay (CMB) within a peripheral console to form a functional computer. A security program reads an identification number in a security memory device to determine a security level of the ACM according to one embodiment.

In a specific embodiment, the present invention provides a system for secured information transactions. The system has a console (e.g., computer housing) comprising a peripheral controller housed in the console; and a security memory device (e.g., flash memory device) coupled to the peripheral controller. The system also has an attached computer module (i.e., a removable module with memory and microprocessor) coupled to the console. The attached computer module has a host interface controller housed within the attached computer module to interface to the security memory device through the peripheral controller.

In an alternative embodiment, the present invention provides a security protection method for a computer module. The method includes steps or acts of inserting the computer module into a console. Once the module has been inserted, the method initiates a security program in the module to read a security identification of the console and to read a security identification of the computer module. Based upon a relationship of the console identification and the computer module identification, a predetermined security status is determined from, for example, a look up table or the like. The method then selects the predetermined security status, which can be one of many. The method then operates the computer module based upon the security status.

In a further alternative embodiment, the present invention provides a method for identifying a user for a computer module. The method includes inserting a computer module into a console; and initiating a security program in memory of the computer module. The method prompts a plurality of input fields corresponding to respective input information on a user interface to be provided by a user of the computer module. Next, the method inputs the input information into the user interface of the computer module. The input information includes a user (e.g., owner) name, a user (e.g., owner) password, a business name, a business password, and a location.

Still further, the present invention provides a system for secured information transactions, e.g., data security, elec-

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tronic commerce, private communications. The system includes a console comprising a peripheral controller housed in the console. A user identification input device (e.g., keyboard, retinal reader, finger print reader, voice recognition unit) is coupled to the peripheral controller. The user identification input device is provided for user identification data of the user. The system has an attached computer module coupled to the console. The attached computer module has a security memory device (e.g., flash memory device) stored with the user identification data.

Numerous benefits are achieved using the present invention over previously existing techniques. The present invention provides mechanical and electrical security systems to prevent theft or unauthorized use of the computer system in a specific embodiment. Additionally, the present invention substantially prevents accidental removal of the ACM from the console. In some embodiments, the present invention prevents illegal or unauthorized use during transit. The present invention is also implemented using conventional technologies that can be provided in the present computer system in an easy and efficient manner. Depending upon the embodiment, one or more of these benefits can be available. These and other advantages or benefits are described throughout the present specification and are described more particularly below.

These and other embodiments of the present invention, as well as its advantages and features, are described in more detail in conjunction with the text below and attached FIGS.

BRIEF DESCRIPTION OF THE DRAWINGS

FIG. 1 is a simplified diagram of a computer system according to an embodiment of the present invention;

FIG. 2 is a simplified diagram of a computer module according to an embodiment of the present invention;

FIG. 3 is a simplified top-view diagram of a computer module according to an embodiment of the present invention;

FIG. 4 is a simplified illustration of security systems according to embodiments of the present invention;

FIG. 5 is a simplified diagram of a computer module in a console according to an embodiment of the present invention;

FIG. 6 is a simplified diagram of a security method for a module according to an embodiment of the present invention; and

FIG. 7 is a simplified diagram of a method according to an embodiment of the present invention.

FIG. 8 is a simplified diagram of a system 800 according to an alternative embodiment of the present application.

DESCRIPTION OF THE SPECIFIC EMBODIMENTS

FIG. 1 is a simplified diagram of a computer system 1 according to an embodiment of the present invention. This diagram is merely an illustration and should not limit the scope of the claims herein. One of ordinary skill in the art would recognize other variations, modifications, and alternatives. The computer system 1 includes an attached computer module (i.e., ACM) 10, a desktop console 20, among other elements. The computer system is modular and has a variety of components that are removable. Some of these components (or modules) can be used in different computers, workstations, computerized television sets, and portable or laptop units.

In the present embodiment, ACM 10 includes computer components, as will be described below, including a central

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processing unit ("CPU"), IDE controller, hard disk drive, computer memory, and the like. The computer module bay (i.e., CMB) **40** is an opening or slot in the desktop console. The CMB houses the ACM and provides communication to and from the ACM. The CMB also provides mechanical protection and support to ACM **10**. The CMB has a mechanical alignment mechanism for mating a portion of the ACM to the console. The CMB further has thermal heat dissipation sinks, electrical connection mechanisms, and the like. Some details of the ACM can be found in co-pending U.S. patent application Ser. Nos. 09/149,882 and 09/149,548 filed Sep. 8, 1998 commonly assigned, and hereby incorporated by reference for all purposes.

In a preferred embodiment, the present system has a security system, which includes a mechanical locking system, an electrical locking system, and others. The mechanical locking system includes at least a key **11**. The key **11** mates with key hole **13** in a lock, which provides a mechanical latch **15** in a closed position. The mechanical latch, in the closed position, mates and interlocks the ACM to the computer module bay. The mechanical latch, which also has an open position, allows the ACM to be removed from the computer module bay. Further details of the mechanical locking system are shown in the FIG. below.

FIG. 2 is a simplified diagram of a computer module **10** according to an embodiment of the present invention. This diagram is merely an illustration and should not limit the scope of the claims herein. One of ordinary skill in the art would recognize other variations, modifications, and alternatives. Some of the reference numerals are similar to the previous FIG. for easy reading. The computer module **10** includes key **11**, which is insertable into keyhole **13** of the lock. The lock has at least two position, including a latched or closed position and an unlatched or open position. The latched position secures the ACM to the computer module bay. The unlatched or open position allows the ACM to be inserted into or removed from the computer bay module. As shown, the ACM also has a slot or opening **14**, which allows the latch to move into and out of the ACM. The ACM also has openings **17** in the backside for an electrical and/or mechanical connection to the computer module bay, which is connected to the console.

FIG. 3 is a simplified top-view diagram **10** of a computer module for computer system according to an embodiment of the present invention. This diagram is merely an illustration and should not limit the scope of the claims herein. One of ordinary skill in the art would recognize other variations, modifications, and alternatives. The layout diagram illustrates the top-view of the module **10**, where the backside components (e.g., Host Interface Controller) are depicted in dashed lines. The layout diagram has a first portion, which includes a central processing unit ("CPU") module **400**, and a second portion, which includes a hard drive module **420**. A common printed circuit board **437** houses these modules and the like. Among other features, the ACM includes the central processing unit module **400** with a cache memory **405**, which is coupled to a north bridge unit **421**, and a host interface controller **401**. The host interface controller includes a lock control **403**. As shown, the CPU module is disposed on a first portion of the attached computer module, and couples to connectors **17**. Here, the CPU module is spatially located near connector **17**.

The CPU module can use a suitable microprocessing unit, microcontroller, digital signal processor, and the like. In a specific embodiment, the CPU module uses, for example, a 400 MHz Pentium II microprocessor module from Intel Corporation and like microprocessors from AMD

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Corporation, Cyrix Corporation (now National Semiconductor Corporation), and others. In other aspects, the microprocessor can be one such as the Compaq Computer Corporation Alpha Chip, Apple Computer Corporation PowerPC G3 processor, and the like. Further, higher speed processors are contemplated in other embodiments as technology increases in the future.

In the CPU module, host interface controller **401** is coupled to BIOS/flash memory **405**. Additionally, the host interface controller is coupled to a clock control logic, a configuration signal, and a peripheral bus. The present invention has a host interface controller that has lock control **403** to provide security features to the present ACM. Furthermore, the present invention uses a flash memory that includes codes to provide password protection or other electronic security methods.

The second portion of the attached computer module has the hard drive module **420**. Among other elements, the hard drive module includes north bridge **421**, graphics accelerator **423**, graphics memory **425**, a power controller **427**, an IDE controller **429**, and other components. Adjacent to and in parallel alignment with the hard drive module is a personal computer interface ("PCI") bus **431**, **432**. A power regulator **435** is disposed near the PCI bus.

In a specific embodiment, north bridge unit **421** often couples to a computer memory, to the graphics accelerator **423**, to the IDE controller, and to the host interface controller via the PCI bus. Graphics accelerator **423** typically couples to a graphics memory **423**, and other elements. IDE controller **429** generally supports and provides timing signals necessary for the IDE bus. In the present embodiment, the IDE controller is embodied as a 643U2 PCI-to IDE chip from CMD Technology, for example. Other types of buses than IDE are contemplated, for example EIDE, SCSI, USB, and the like in alternative embodiments of the present invention.

The hard drive module or mass storage unit **420** typically includes a computer operating system, application software program files, data files, and the like. In a specific embodiment, the computer operating system may be the Windows98 operating system from Microsoft Corporation of Redmond Washington. Other operating systems, such as WindowsNT, MacOS8, Unix, and the like are also contemplated in alternative embodiments of the present invention. Further, some typical application software programs can include Office98 by Microsoft Corporation, Corel Perfect Suite by Corel, and others. Hard disk module **420** includes a hard disk drive. The hard disk drive, however, can also be replaced by removable hard disk drives, read/write CD ROMs, flash memory, floppy disk drives, and the like. A small form factor, for example 2.5", is currently contemplated, however, other form factors, such as PC card, and the like are also contemplated. Mass storage unit **240** may also support other interfaces than IDE.

In a specific embodiment, the present invention provides a file and data protection security system and method for a removable computer module or ACM. ACM contains the primary hard disk drive (HDD) where the operating system, application programs, and data files reside. The security system is used to prevent illegal access and copying of any file residing on the HDD inside ACM. An ACM is a self-contained computing device that can be armed with security software and hardware to protect its owner's private files and data. ACM docks with a computer bay in a wide variety of peripheral consoles. The combined ACM and peripheral console function as a personal computer. A com-

puter module interface bus connects ACM and peripheral device. In some embodiments, all ACM data passes through computer module interface (CMI) bus to reach any device in the peripheral console, i.e. floppy drive, removable media, secondary hard disk drive, modem, and others. CMI bus data transfer is controlled by a pair of interface controllers on either side of the bus. This partitioning of a personal computer offer a way of protecting against illegal access of data residing within ACM by guarding data transaction through the computer module interface bus.

In a specific embodiment, a secured ACM has an enclosure that includes the following components:

- 1) ACPU,
- 2) Main memory,
- 3) A primary Hard Disk Drive (HDD),
- 4) Operating System, application software, data files on primary HDD,
- 5) Interface circuitry and connectors to peripheral console,
- 6) Flash memory used for storing security code and ID,
- 7) Data detection and control circuitry to manage data flow to peripheral console,
- 8) Circuit board connecting the above components, and others.

A peripheral console includes some of the following elements:

- 1) Input means, e.g. keyboard and mouse,
- 2) Display means, e.g. CRT monitor, or integrated LCD display,
- 3) Removable storage media subsystem, e.g. Floppy drive, CDROM drive,
- 4) Communication device, e.g. LAN or modem,
- 5) Computer Module Bay, interface device and connectors to ACM,
- 6) Flash memory with security ID,
- 7) Power supply or battery system, and other devices.

The Computer Module Bay (CMB) is an opening in a peripheral console that receives ACM. CMB provides mechanical protection and electrical connection to ACM. The Computer Module Interface bus is made up of 3 bus components: video bus, peripheral data bus, and power bus. Video Bus consists of video output of graphics devices, i.e. analog RGB and control signals for monitor, or digital video signals to drive flat panel displays. Power bus supplies the power for ACM. Peripheral data bus is a high speed, compressed, peripheral bridge bus managed by a Host Interface Controller in ACM and a peripheral Interface Controller in peripheral console. In some embodiments, all peripheral data transaction passes through the interface controllers.

The implementation of the secured ACM generally includes the following elements:

- 1) A programmable Flash memory controlled by the Peripheral Interface Controller containing the security ID for the peripheral console,
- 2) A programmable Flash memory controlled by the Host Interface Controller containing hardware specific security code and ID for the computer module,
- 3) A data detection and control circuitry within Host Interface Controller to detect and manage data going out of ACM, and
- 4) A low level hardware dependent security code to perform security ID matching, hardware programming to manage data flow,

- 5) A high-level security program to manage user interface, program security ID, program security level, and other functions.

The hardware and software implementation allow more flexibility in the level of security protection offered to an ACM owner. Some examples of security levels are:

- 1) No access—Security IDs do not match according to owner's requirement. The Host Interface Controller blocks all peripheral data traffic between ACM and peripheral console except for keyboard and mouse,
- 2) Peripheral Read-only—No files can be written to any peripheral devices. All peripheral devices in peripheral console are managed as Read-only devices. The primary hard disk drive in ACM can be accessed freely,
- 3) Limited access—Certain peripheral devices are allowed read/write access, i.e. modem, and other devices are Read-only, i.e. removable media devices,
- 4) Full access—No restriction, and others.

Upon power up, the low level security code is executed to compare security ID between the respective flash memory between ACM and peripheral console. Typical security ID can include:

- 1) User ID
- 2) User password
- 3) User Access privilege
- 4) Business ID
- 5) Business password
- 6) Equipment ID
- 7) Equipment access privilege, and any other security IDs.

The user through the security program can activate different levels of password protection, which can be stored in a look up table. The company through the security program can control different levels of access privilege of a user, a business group, or equipment. The security code then program the security level allowed by the access privilege determined by the security ID matching result. For example, if an unidentified peripheral console is detected upon power up by the low level security code, e.g. a home unit, the access privilege can set to Peripheral Read-only. With Read-only access privilege for all peripheral devices in peripheral console, the data detection and control circuitry is programmed to monitor all data traffic going to the peripheral console. Any memory block transfer to peripheral console will be detected and blocked. Under this mode, a user can use the computer with free access to the primary HDD in ACM. Any files can be read from other storage media in the peripheral console. But no files from the primary HDD can be copied to another media.

The data detection circuitry separately monitors peripheral bus operation type and memory address range being accessed. A specific address range for memory accesses and for I/O accesses can be programmed for the data detection circuitry to flag a match. A data blocking circuitry is triggered by the detection circuitry when a match occurs, and blank out the data that is being sent to the peripheral console. For the security system to be effective, a temper resistant enclosure must be used to prevent removal of the hard disk drive and the flash memory inside ACM. Further details are shown throughout the present specification and more particularly below.

FIG. 4 is a simplified illustration of security systems according to embodiments of the present invention. This illustration is merely an example, which should not limit the scope of the claims herein. One of ordinary skill in the art would recognize other variations, modifications, and alter-

natives. The systems show various examples of ways to implement the present invention. Here, a user relies upon certain consoles to access information. A company's shared portable console **325** can access general company information **303**. Selected security identification information **315** is entered into the shared console to access the information via a network. The information generally includes owner, owner password, business, business password, console type, location, and access privilege information, which is displayed on a user display. The owner is generally the user name. Owner password is the user password. The business is the business unit name and business password is the business unit password. The console type can be portable for laptops, notebooks, and the like. Alternatively, the console type can be a desktop. The location generally specifies the desktop location or address for a networked system. Alternatively, the location can also be a home location. Access privilege can be categorized into many different levels. For example, the user can access general company information, but not information directed to other business units. The user can also be limited to access his/her private information, which is company related. Many other types of information can be restricted or accessed depending upon the embodiment.

Other types of access can be granted depending upon the consoles. For example, various consoles include, among others, a console at a user's home, e.g., "John Doe's," a console in the user's office **329**, a console in a co-worker's office **331**, which the user can access. The access from John Doe's home console uses security identification **317** and provides restricted access **305**. The user's use of the module **307** can be from a variety of consoles and is accessed using security identification **319**. Here, access privilege is private, which allows the user to access private personal information or private company information that the user has created. The user's access from his office relies upon security identification **321**, which grants access to private information and general company information. The co-worker's console can also be used with security identification **323**, which allows the user to access general company information but not private information of John Doe, for example. Depending upon the console used by the user, the security system can provide partial or full access to information on servers via network as well as an attached computer module. Information can also be limited to read only for certain information sources such as a server, a hard drive, a floppy drive, and others.

In a specific embodiment, the present invention also provides a security feature for the ACM **307**. Here, the user of the ACM can be granted access to information in the ACM if the correct security identification information **319** is provided to the combination of ACM and console. Once the correct information is provided, the user can access the information on the hard drive of the ACM, which can be for private use. Other levels of access and security can also be provided depending upon the application.

FIG. 5 is a simplified diagram **500** of a computer module in a console according to an embodiment of the present invention. This diagram is merely an illustration which should not limit the scope of the claims herein. One of ordinary skill in the art would recognize other variations, modifications, and alternatives. The block diagram **500** includes an attached computer module **501** and a peripheral console **503**, as well as other elements as desired. These elements have a variety of features such as those noted above, as well as others. In the present diagram, different reference numerals are used to show the operation of the present system.

The block diagram **500** illustrates attached computer module **501**. The module **501** has a central processing unit **502**, which communicates to a north bridge **541**, by way of a CPU bus **527**. The north bridge couples to main memory **523** via memory bus **529**. The main memory can be any suitable high speed memory device or devices such as dynamic random access memory ("DRAM") integrated circuits and others. The DRAM includes at least 32 Meg. or 64 Meg. and greater of memory, but can also be less depending upon the application. Alternatively, the main memory can be coupled directly with the CPU in some embodiments. The north bridge also couples to a graphics subsystem **515** via bus **542**. The graphics subsystem can include a graphics accelerator, graphics memory, and other devices. Graphics subsystem transmits a video signal to an interface connector, which couples to a display, for example.

The attached computer module also includes a primary hard disk drive **509** that serves as a main memory unit for programs and the like. The hard disk can be any suitable drive that has at least 2 GB and greater. As merely an example, the hard disk is a Marathon **2250** (2.25 GB, 2 1/2 inch drive) product made by Seagate Corporation of Scotts Valley, but can be others. The hard disk communicates to the north bridge by way of a hard disk drive controller and bus lines **502** and **531**. The hard disk drive controller couples to the north bridge by way of the host PCI bus **531**, which connects bus **537** to the north bridge. The hard disk includes computer codes that implement a security program according to the present invention. Details of the security program are provided below.

The attached computer module also has a flash memory device **505** with a BIOS. The flash memory device **505** also has codes for a user password that can be stored in the device. The flash memory device generally permits the storage of such password without a substantial use of power, even when disconnected. As merely an example, the flash memory device has at least 512 kilobits or greater of memory, or 1 megabits or greater of memory. The flash memory device can store a security identification number or the like. The flash memory device is generally non-volatile and can preserve information even when the power is turned off, for example. The flash memory generally has at least 128 kilobits storage cells or more. The flash memory can be any product such as a W29C020 product made by a company called Winbond of Taiwan, but can also be others. The flash memory cell and user identification will be more fully described below in reference to the FIGS. A host interface controller **507** communicates to the north bridge via bus **535** and host PCI bus. The host interface controller also has a data control **511**. Host interface controller **507** communicates to the console using bus **513**, which couples to connection **515**.

Peripheral console **503** includes a variety of elements to interface to the module **501**, display **551**, and network **553**. The console forms around south bridge **571**, which couples to bus **563**, which couples to bus **561**. Bus **561** is in communication with network card **555**, which is a local area network for Ethernet, for example. South bridge also couples through control **569** to peripheral interface controller **567**, which also communicates to bus **561**. Peripheral interface controller also couples to host interface controller through connection **515** and bus **513**. The peripheral console has a primary removable drive **559** connected to south bridge through bus **575**. South bridge also couples to secondary hard disk through bus **577**.

In a specific embodiment, the peripheral console also has a serial EEPROM memory device **575**, which is coupled to

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the peripheral interface controller. The memory device can store a security identification number or the like. The memory device is generally non-volatile and can preserve information even when the power is turned off, for example. The memory generally has at least 16 kilobits of storage cells or more. Preferably, the memory device is a 16 kilobit device or 64 megabit device or greater, depending upon the application. The memory can be any product such as a X24320 product made by a company called Xicor, but can also be others. The memory cell and user identification will be more fully described below in reference to the FIGS.

FIG. 6 is a simplified diagram of a security method **600** for a module according to an embodiment of the present invention. This diagram is merely an illustration which should not limit the scope of the claims herein. One of ordinary skill in the art would recognize other variations, modifications, and alternatives. The present method shows an example of how the present security method can be implemented. The present method uses a combination of software **601** and hardware **603**, which is in the computer module. A plurality of external devices can be accessed depending upon the embodiment. These external devices include a secondary hard drive **618**, a removable drive **619**, a network (e.g., LAN, modem) device **621**, and others. A keyboard **623** is also shown, which can act locally.

The software **601** includes an operating system **609**, application programs **607**, and a data security and initialization program **605**. Other programs can also exist. Additionally, some of these programs may not exist. Preferably, the data security and initialization program exists. This data security and initialization program is initiated once the attached computer module is inserted into the console. The program interface and oversees a variety of hardware features, which will be used to control access to the external devices, for example. Of course, the particular configuration of the software will depend upon the application.

Hardware features can be implemented using a primary hard disk **611** coupled to a CPU/cache combination, which includes a main memory. The main memory is often a volatile memory such as dynamic random access memory. Data from any one of the external devices can enter the CPU/cache combination. For example, the secondary hard disk memory and I/O address range data is transferred **624** to the CPU/cache combination. The removable drive memory and I/O address range data can also transfer **625** to the CPU/cache combination. The LAN memory and I/O address range data can also transfer **626** to the CPU/cache combination. Keyboard data can also transfer **627** to the CPU/cache combination. To write data from the module into any one of these external elements, the data security program interfaces with the data detection and control circuit to determine of such data should be transferred to any one of the external elements. As noted, the external elements include, among others, secondary hard disk, and removable drive. Here, the data security program checks the security identification number with other numbers to determine the security access level. There are many other ways that the present invention can be implemented. These methods are described more fully below.

FIG. 7 is a simplified diagram **700** of a method according to an embodiment of the present invention. This diagram is merely an illustration which should not limit the scope of the claims herein. One of ordinary skill in the art would recognize other variations, modifications, and alternatives. The present method begins at power up, which is step **701**. The present method reads a security code, which has been

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entered by a user, for example, in step **703**. The security code can be a string of characters, including numbers and letters. The security code is preferably a mixture of numbers and letters, which are at least about 6 characters in length, but is not limited.

The present method reads (step **703**) the security code, which has been entered. Next, the security code is compared with a stored code, which is in flash memory or the like (step **705**). If the compared code matches with the stored code, the method resumes to step **708**. Alternatively, the method goes to step **707** via branch **706** where no access is granted. When no access is granted, all data are blocked out from the user that attempts to log onto the system. Alternatively, the method determines if a certain level of access is granted, step **708**. Depending upon the embodiment, the present method can grant full access, step **710**, via branch **716**. The present method allows full access based upon information stored in the flash memory device. Alternatively, the method can allow the user to access a limited amount of information.

Here, the present method allows for at least one or more than two levels of access. In a specific embodiment, the present method allows for the user of the module to access peripheral storage (step **711**). The access privilege is read-only. The user can read information on the peripheral storage including hard disks and the like. Once the user accesses the storage, the method data control, step **719**, takes over, where the hardware prevents the user from accessing other information, step **721**. In a specific embodiment, the method can allow information to be removed from the peripheral storage. If the method allows for data to be removed, step **723**, the method goes through branch **731** to let data out, which can occur through the module. Alternatively, the method goes to block data (step **725**) via branch **733**. Depending upon the embodiment, the method returns to the decision block, step **723**. Alternatively, the method traverses branch **714** to a peripheral read-only process, step **712**. The read-only process programs data control, step **713**. Next, the hardware takes over (step **715**). The method blocks all data from being accessed by the user, step **717**.

FIG. 8 is a simplified diagram of a system **800** according to an alternative embodiment of the present invention. This diagram is merely an example which should not limit the scope of the claims herein. One of ordinary skill in the art would recognize many other variations, modifications, and alternatives. The system **800** includes an attached computer module **801**, which can be inserted into one of a plurality of console devices to create a "plug and play" operation. For example, the console device can be peripheral console **801** or peripheral console **805**. Each peripheral console can have similar or different connection characteristics. Peripheral console **803** couples to a local area network using Ethernet **817**. Peripheral console **805** couples to a DSL line **827** through a DSL modem **825**. Other consoles can also be included to use other types of networks such as ADSL, Cable Modem, wireless, Token Ring, and the like.

As shown, the attached computer module has elements such as a memory region **807**, which stores BIOS information, a security code, and a security identification number on a flash memory device or the like. The memory region couples to a central processing region **809**, which can include CPU, chipset, cache memory, graphics, and a hard disk drive, as well as other features. The central processing region couples to a host interface controller, which interfaces the attached computer module to one of the peripheral consoles. Any of the above information can also be included in the attached computer module.

Each peripheral console also has a variety of elements. These elements include a region **813**, **821**, which has a flash

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memory device with a security identification number, a password, access information, access privileges, internet service provider access information, as well as other features, which were previously noted. The peripheral console also has an interface controller **815, 823**, which couples region **813, 821**, respectively to a networking device **817, 825**. The networking device can be an Ethernet card **817**, which allows communication to the local area network **819**. Alternatively, the networking device can be a DSL modem **825**, which allows communication to a DSL (or ADSL) phone line. Other types of networking device can also be used, depending upon the application.

Each console provides a selected connection based upon set of predefined factors. These factors include communication hardware information so that software in attached computer module can read and allow a connection to a network. Here, access information can be provided to the user. Information about connection information will also be included. This connection information includes telephone numbers, account numbers, passwords (local), or a company password. The console and module combination will take care of charges, etc. based upon time bases. Module will have credit card information, but will have security. In a specific embodiment, the module inserts into the console. The module then asks the console which hardware will be used. If the hardware is an Ethernet connect, the module configures connection information to access the Ethernet connection. Alternatively, if the hardware requires a DSL connection, the module configures connection information to access the DSL connection. Other configuration information such as company server information, password, can also be provided.

Although the functionality above has been generally described in terms of a specific sequence of steps, other steps can also be used. Here, the steps can be implemented in a combination of hardware, firmware, and software. Either of these can be further combined or even separated. Depending upon the embodiment, the functionality can be implemented in a number of different ways without departing from the spirit and scope of the claims herein. One of ordinary skill in the art would recognize other variations, modifications, and alternatives.

While the above is a full description of the specific embodiments, various modifications, alternative constructions and equivalents may be used. Therefore, the above description and illustrations should not be taken as limiting the scope of the present invention which is defined by the appended claims.

What is claimed is:

1. A security protection method for a computer module, said method comprising:
 - inserting the computer module into a console;
 - initiating a security program in said module to read a security identification of said console and to read a security identification of said computer module;
 - determining of a predetermined security status based upon a relationship of said console identification and said computer module identification;

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selecting said predetermined security status; and
operating said computer module based upon said security status.

2. The method of claim 1 wherein said predetermined security status disables a network access to the computer module.

3. The method of claim 1 wherein said predetermined security status disables a secondary storage of information from said computer module to substantially prevent information to be transferred from a memory of the computer module to said secondary storage.

4. The method of claim 1 wherein said security program is provided in a system BIOS.

5. The method of claim 1 wherein said step of initiating reads said security identification of said computer module from a flash memory device.

6. The method of claim 1 wherein said step of initiating reads said security identification of said console from a flash memory device.

7. The method of claim 1 wherein said console is selected from a desktop home computing device, an office desktop computing device, a mobile computing device, a television set-top computing device, and a co-worker's computing device.

8. A system for secured information transactions, the system comprising:

a console comprising a peripheral controller housed in the console;

a user identification input device coupled to the peripheral controller, the user identification input device being provided for user identification data; and

an attached computer module coupled to the console, the attached computer module comprising a security memory device stored with the user identification data.

9. The system of claim 8 wherein the user identification input device is a finger print reader.

10. The system of claim 8 wherein the user identification input device is a voice processing device.

11. A method for operating a module computer into one of a plurality of network systems, the method comprising:

providing a computer module, the module comprising a connection program;

inserting the computer module into a computer console, the computer console having access to a network;

receiving connection information from the computer console;

configuring the connection program to adapt to the connection information; and

establish a connection between the computer module and a server coupled to the network.

12. The method of claim 11 wherein the connection information comprises a connection protocol for providing the connection.

13. The method of claim 12 wherein the connection protocol is selected from TCP/IP, or mobile IP.

* * * * *

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Reissue of: William W.Y. Chu

Patent No.: 6,643,777

Issued: November 4, 2003

For: DATA SECURITY METHOD AND DEVICE FOR COMPUTER MODULES

Mail Stop: Reissue

Commissioner for Patents

P.O. Box 1450

Alexandria, VA 22313-1450

PRELIMINARY AMENDMENT

Prior to examination of the above-identified application, please amend the present application as follows:

Amendments to the Drawings begin on page 2 of this paper.

Amendments to the Specification begin on page 3 of this paper.

Amendments to the Claims are reflected in the listing of the claims which begins on page 14 of this paper.

Remarks/Arguments begin on page 19 of this paper.

IN THE DRAWINGS

Attachment: 12 New Sheets FIG. 9 through FIG. 24.

The present application is amended to specifically include certain figures from U.S. Patent No. 6,216,185, U.S. Patent No. 6,345,330, and U.S. Provisional Application No. 60/083,886.

IN THE SPECIFICATION:

Please add the following new paragraphs beginning at col. 1, line 6:

Notice: More than one reissue application has been filed for the reissue of U.S. Patent No. 6,643,777. The reissue applications are U.S. Application Nos. 11/056,604 (a parent reissue application), 11/545,056 (which is a reissue continuation of the parent reissue application), 12/561,138 (which is a reissue continuation of the parent reissue application), 13/294,108 (which is a reissue continuation of U.S. Application No. 12/561,138), and / , (the present application, which is a reissue continuation of U.S. Application No. 13/294,108).

This application is a reissue continuation of U.S. Application No. 13/294,108, which is a reissue continuation of U.S. Application No. 12/561,138, which is a reissue continuation of U.S. Application No. 11/056,604, which is a reissue of U.S. Patent No. 6,643,777, which are incorporated herein by reference.

Please add the following new paragraphs beginning at col. 4, line 51:

FIG. 9 depicts a peripheral console configuration.

FIG. 10 is a block diagram of one embodiment of a computer system employing the present invention.

FIG. 11 is a block diagram of an attached computing module (ACM).

FIG. 12 is a block diagram of a peripheral console (PCON).

FIG. 13 is a block diagram of one embodiment of a computer system using the interface of the present invention.

FIG. 14 is a detailed block diagram of one embodiment of the host interface controller of the present invention.

FIG. 15 is a detailed block diagram of one embodiment of the PIC of the present invention.

FIG. 16 is a schematic diagram of the signal lines PCK, PD0 to PD3, and PCN.

FIG. 17 is a partial block diagram of a computer system using the interface of the present invention as a bridge between the north and south bridges of the computer system.

FIG. 18 is a partial block diagram of a computer system in which the north and south bridges are integrated with the host and peripheral interface controllers, respectively.

FIG. 19 shows an attached computer module with Integrated CPU/NB/Graphics and Integrated HIC/SB.

FIG. 20 shows an attached computer module with single chip fully integrated: CPU, Cache, Core Logic, Graphics controller and Interface controller.

FIGS. 21 and 22 are tables including the pin number, symbol, signal, standard and description for the pins on the peripheral and video connectors, respectively.

FIG. 23 is a table showing the symbols, signals, data rate and description of signals in a first embodiment of the XPBus.

FIG. 24 is a table showing different types of first nibbles and their corresponding data packet types.

Please replace the paragraph beginning at col. 8, line 51 with the following amended paragraph:

The data detection circuitry separately monitors peripheral bus operation type and memory address range being accessed. A specific address range for memory accesses and for I/O accesses can be programmed for the data detection circuitry to flag a match. A data blocking circuitry is triggered by the detection circuitry when a match occurs, and blank out the data that is being sent to the peripheral console. For the security system to be effective, a [temper]~~temper~~ resistant enclosure must be used to prevent removal of the hard disk drive and the flash memory inside ACM. Further details are shown throughout the present specification and more particularly below.

Please add the following new paragraphs beginning at col. 13, line 33:

A personal computer system that comprises two physically separate units and the interconnection between them is disclosed. The first unit, an attached computing module (ACM), contains the core computing power and environment for a computer user. The second unit, a peripheral console (PCON), contains the power supply and primary input and output devices for the computer system. An ACM and a PCON are coupled with one another to form a fully functional personal computer system.

FIG. 9 depicts a notebook computer PCON configuration. The opening of the computer bay 992 is visible at the side of the PCON unit 900. The PCON 900 provides an integrated LCD

display panel 910 as the user's primary display device. The PCON 900 provides an integrated keyboard 922 as the user's primary input device.

FIG. 10 is a block diagram of the components in one computer system. The computer system comprises an attached computer module (ACM) 1000, a peripheral console (PCON) 1001, and the interconnection apparatus 1003 between them. The ACM 1000 includes the central processing unit (CPU) 1010, system memory 1020, high performance devices 1050, primary mass storage 1030, and related interface and support circuitry 1040. The PCON 1001 includes primary display 1011, primary input 1021, secondary mass storage 1051, other devices 1061, expansion slots 1071, the primary power supply 1031, and related interface and support circuitry 1041. The interconnection apparatus 1003 includes circuitry to convey power and operational signals between the ACM 1000 and PCON 1001.

Within the ACM 1000, the CPU 1010 executes instructions and manipulates data stored in the system memory 1020. The CPU 1010 and system memory 1020 represent the user's core computing power. The core computing power may also include high performance devices 1050 such as advanced graphics processor chips that greatly increase overall system performance and which, because of their speed, need to be located close to the CPU 1010. The primary mass storage 1030 contains persistent copies of the operating system software, application software, configuration data, and user data. The software and data stored in the primary mass storage device 1030 represent the user's computing environment. Interface and support circuitry 1040 primarily includes interface chips and signal busses that interconnect the CPU 1010, system memory 1020, high performance devices 1050, and primary mass storage 1030. The interface and support circuitry 1040 also connects ACM-resident components with the ACM-to-PCON interconnection apparatus 1003 as needed.

Within the PCON 1001, the primary display component 1011 may include an integrated display device or connection circuitry for an external display device. This primary display device 1011 may be, for example, an LCD, plasma, or CRT display screen used to display text and graphics to the user for interaction with the operating system and application software. The primary display component 1011 is the primary output of the computer system, i.e., the paramount vehicle by which programs executing on the CPU 1010 can communicate toward the user.

The primary input component 1021 of the PCON 1001 may include an integrated input device or connection circuitry for attachment to an external input device. The primary input 1021 may be, for example, a keyboard, touch screen, keypad, mouse, trackball, digitizing pad, or some combination thereof to enable the user to interact with the operating system and application software. The primary input component 1021 is the paramount vehicle by which programs executing on the CPU 1010 receive signals from the user.

The PCON 1001 may contain secondary mass storage 1051 to provide additional high capacity storage for data and software. Secondary mass storage 1051 may have fixed or removable media and may include, for example, devices such as diskette drives, hard disks, CD-ROM drives, DVD drives, and tape drives.

The PCON 1001 may be enhanced with additional capability through the use of integrated “Other Devices” 1061 or add-on cards inserted into the PCON’s expansion slots 1071. Examples of additional capability include sound generators, LAN connections, and modems. Interface and support circuitry 1041 primarily includes interface chips, driver chips, and signal busses that interconnect the other components within the PCON 1001. The interface and support circuitry 1041 also connects PCON-resident components with the ACM-to-PCON interconnection apparatus 1003 as needed.

Importantly, the PCON 1001 houses the primary power supply 1031. The primary power supply 1031 has sufficient capacity to power both the PCON 1001 and the ACM 1000 for normal operation. Note that the ACM 1000 may include a secondary “power supply” in the form, for example, of a small battery. Such a power supply would be included in the ACM 1000 to maintain, for example, a time-of-day clock, configuration settings when the ACM 1000 is not attached to a PCON, or machine state when moving an active ACM immediately from one PCON to another. The total energy stored in such a battery would, however, be insufficient to sustain operation of the CPU 1010 at its rated speed, along with the memory 1020 and primary mass storage 1030, for more than a fraction of an hour, if the battery were able to deliver the required level of electrical current at all.

FIG. 11 is a block diagram of an attached computing module (ACM) 1100. The physical ACM package 1100 contains the ACM functional components 1101 and the ACM side of the ACM-to-PCON Interconnection 1700. The ACM 1101 comprises a CPU component 1110, a

system memory component 1120, a primary mass storage component 1130, a high performance devices components 1150, and an interface and support component 1140.

The ACM side of the ACM-to-PCON Interconnection 1700 comprises a Host Interface Controller (HIC) component 1720 and an ACM connector component 1730. The HIC 1720 and connector 1730 components couple the ACM functional components 1100 with the signals of an ACM-to-PCON interface bus 1710 used to operatively connect an ACM with a PCON. The ACM-to-PCON interface bus 1710 comprises conveyance for electrical power 1714 and signals for a peripheral bus 1712, video 1716, video port 1717, and console type 1718. The preferred ACM-to-PCON Interconnection 1700 is described in detail in a companion U.S. patent application, Ser. No. 09/149,882, entitled “A Communication Channel and Interface Devices for Bridging Computer Interface Buses,” by the same inventor, filed on September 8, 1998, and hereby incorporated by reference. The preferred ACM-to-PCON interconnection 1700 includes circuitry to transmit and receive parallel bus information from multiple signal paths as a serial bit stream on a single signal path. This reduces the number of physical signal paths required to traverse the interconnection 1700. Further, employing low-voltage differential signaling (LVDS) on the bit stream data paths provides very reliable, high-speed transmission across cables. This represents a further advantage of the present invention.

Clocking circuitry 1144 generates clock signals for distribution to other components within the ACM 1100 that require a timing and synchronization clock source. The CPU 1110 is one such component. Often, the total power dissipated by a CPU is directly proportional to the frequency of its main clock signal. The presently described embodiment of the ACM 1100 includes circuitry that can vary the frequency of the main CPU clock signal conveyed to the CPU 1110 via signal path 1162, in response to a signal received from the host interface controller (HIC) 1720 via signal path 1161. The generation and variable frequency control of clocking signals is well understood in the art. By varying the frequency, the power consumption of the CPU 1110 (and thus the entire ACM 1100) can be varied.

The variable clock rate generation may be exploited to match the CPU power consumption to the available electrical power. Circuitry in the host interface controller (HIC) 1720 of the presently described embodiment adjusts the frequency control signal sent via signal path 1161 to the clocking circuitry 1144, based on the “console type” information signal 1718 conveyed from the peripheral console (PCON) by the CPU-to-PCON interconnection 1700.

FIG. 12 is a block diagram of a peripheral console (PCON). A peripheral console couples with an ACM to form an operating personal computer system. The peripheral console (PCON) supplies an ACM with primary input, display, and power supply; the ACM supplies the core computing power and environment of the user. In the presently described embodiment the physical PCON package 1200 contains the PCON functional components 1201 and the PCON side of the ACM-to-PCON Interconnection 1800. The PCON functional components 1201 comprise primary display 1210, a primary input 1220, a primary power supply 1230, interface and support 1240, secondary mass storage 1250, other devices 1260, and expansion slots 1270.

The PCON side of the ACM-to-PCON Interconnection 1800 comprises a Peripheral Interface Controller (PIC) component 1840, a PCON connector component 1850, console-type component 1842, and flash memory device 1848. The PIC 1840 and connector 1850 components couple the PCON functional components 1201 with the signals of an ACM-to-PCON interface bus 1810 used to operatively connect an ACM with a PCON. The ACM-to-PCON interface bus 1810 comprises conveyance for electrical power 1814 and signals for a peripheral bus 1812, video 1816, video port 1817, and console-type 1818. The preferred ACM-to-PCON Interconnection 1800 is described in detail in the U.S. patent application entitled "A Communication Channel and Interface Devices for Bridging Computer Interface Buses," already incorporated herein by reference.

Connector component 1850 may be selected to mate directly with the connector component 1730 of an ACM (shown in FIG. 11). Alternatively, connector component 1850 may be selected to mate with, for example, the connector on one end of a cable intervening between the PCON and an ACM in a particular embodiment. The ACM-to-PCON interconnection described in the aforementioned companion patent application has the advantage of providing reliable signal conveyance across low cost cables.

Flash memory device 1848 provides non-volatile storage. This storage may be accessible to devices in both the ACM and the PCON, including the host interface controller and the peripheral interface controller 1840 to which it is connected. As such, flash memory 1848 may be used to store configuration and security data to facilitate an intelligent mating between an ACM and a PCON that needs no participation of the CPU.

The secondary mass storage component 1250 of the PCON functional circuitry 1201 of the presently described embodiment comprises diskette drive 1254, hard disk drive 1252, and

CD-ROM drive 1256. Secondary mass storage 1250 generally provides low-cost, non-volatile storage for data files which may include software program files. Data files stored on secondary mass storage 1250 are not part of a computer user's core computing power and environment. Secondary mass storage 1250 may be used to store, for example, seldom used software programs, software programs that are used only with companion hardware devices installed in the same peripheral console 1200, or archival copies of data files that are maintained in primary mass storage 1130 of an ACM (shown in FIG. 11). Storage capacities for secondary mass storage 1250 devices may vary from the 1.44 megabytes of the 3.5-inch high density diskette drive 1254, to more than 10 gigabytes for a large format (5-inch) hard disk drive 1252. Hard disk drive 1252 employs fixed recording media, while diskette drive 1254 and CD-ROM drive 1256 employ removable media. Diskette drive 1254 and hard disk drive 1252 support both read and write operations (i.e., data stored on their recording media may be both recalled and modified) while CD-ROM drive 1256 supports only read operations.

Two PCI or PCI-like buses are interfaced using a non-PCI or non-PCI-like channel. PCI control signals are encoded into control bits, and the control bits, rather than the control signals that they represent, and are transmitted on the interface channel. At the receiving end, the control bits representing control signals are decoded back into PCI control signals prior to being transmitted to the intended PCI bus.

The fact that control bits rather than control signals are transmitted on the interface channel allows using a smaller number of signal channels and a correspondingly small number of conductive lines in the interface channel than would otherwise be possible. This is because the control bits can be more easily multiplexed at one end of the interface channel and recovered at the other end than control signals. This relatively small number of signal channels used in the interface channel allows using LVDS channels for the interface. As mentioned above, an LVDS channel is more cable friendly, faster, consumes less power, and generates less noise than a PCI bus channel. Therefore, an LVDS channel is advantageously used for the hereto unused purpose of interfacing PCI or PCI-like buses. The relatively smaller number of signal channels in the interface also allows using connectors having smaller pins counts. As mentioned above an interface having a smaller number of signal channels and, therefore, a smaller number of conductive lines is less bulky and less expensive than one having a larger number of signal

channels. Similarly, connectors having a smaller number of pins are also less expensive and less bulky than connectors having a larger number of pins.

In one embodiment, the present invention encompasses an apparatus for bridging a first computer interface bus and a second computer interface bus, in a microprocessor based computer system where each of the first and second computer interface buses have a number of parallel multiplexed address/data bus lines and operate at a clock speed in a predetermined clock speed range having a minimum clock speed and a maximum clock speed. The apparatus comprises an interface channel having a clock channel and a plurality of bit channels for transmitting bits; a first interface controller coupled to the first computer interface bus and to the interface channel to encode first control signals from the first computer interface bus into first control bits to be transmitted on the interface channel and to decode second control bits received from the interface channel into second control signals to be transmitted to the first computer interface bus; and a second interface controller coupled to the interface channel and the second computer interface bus to decode the first control bits from the interface channel into third control signals to be transmitted on the second computer interface bus and to encode fourth control signals from the second computer interface bus into the second control bits to be transmitted on the interface channel.

In one embodiment, the first and second interface controllers comprise a host interface controller (HIC) and a peripheral interface controller (PIC), respectively, the first and second computer interface buses comprise a primary PCI and a secondary PCI bus, respectively, and the interface channel comprises an LVDS channel.

In a preferred embodiment, the interface channel has a plurality of serial bit channels numbering fewer than the number of parallel bus lines in each of the PCI buses and operates at a clock speed higher than the clock speed at which any of the bus lines operates. More specifically, the interface channel includes two sets of unidirectional serial bit channels which transmit data in opposite directions such that one set of bit channels transmits serial bits from the HIC to the PIC while the other set transmits serial bits from the PIC to the HIC. For each cycle of the PCI clock, each bit channel of the interface channel transmits a packet of serial bits.

The HIC and PIC each include a bus controller to interface with the first and second computer interface buses, respectively, and to manage transactions that occur therewith. The HIC and PIC also include a translator coupled to the bus controller to encode control signals

from the first and second computer interface buses, respectively, into control bits and to decode control bits from the interface channel into control signals. Additionally, the HIC and PIC each include a transmitter and a receiver coupled to the translator. The transmitter converts parallel bits into serial bits and transmits the serial bits to the interface channel. The receiver receives serial bits from the interface channel and converts them into parallel bits.

FIG. 13 is a block diagram of one embodiment of a computer system 1300 using the interface of the present invention. Computer system 1300 includes an attached computer module (ACM) 1305 and a peripheral console 1310, which are described in greater detail in the application of William W. Y. Chu, Ser. No. 09/149,548, for "Personal Computer Peripheral Console With Attached Computer Module" filed on Sep. 8, 1998 and incorporated herein by reference. The ACM 1305 and the peripheral console 1310 are interfaced through an exchange interface system (XIS) bus 1315. The XIS bus 1315 includes power bus 1316, video bus 1317 and peripheral bus (XPBus) 1318, which is also herein referred to as an interface channel. The power bus 1316 transmits power between ACM 1305 and peripheral console 1310. In a preferred embodiment power bus 1316 transmits power at voltage levels of 3.3 volts, 5 volts and 12 volts. Video bus 1317 transmits video signals between the ACM 1305 and the peripheral console 1310. In a preferred embodiment, the video bus 1317 transmits analog Red Green Blue (RGB) video signals for color monitors, digital video signals (such as Video Electronics Standards Association (VESA) Plug and Display's Transition Minimized Differential Signaling (TMDS) signals for flat panel displays), and television (TV) and/or super video (S-video) signals. The XPBus 1318 is coupled to host interface controller (HIC) 1319 and to peripheral interface controller (PIC) 1320, which is also sometimes referred to as a bay interface controller.

In the embodiment shown in FIG. 13, HIC 1319 is coupled to an integrated unit 1321 that includes a CPU, a cache and a north bridge. In another embodiment, such as that shown in FIG. 17, the CPU 1705 and north bridge 1710 are separate rather than integrated units. In yet another embodiment, such as that shown in FIG. 18, the HIC and PIC are integrated with the north and south bridges, respectively, such that integrated HIC and north bridge unit 1805 includes an HIC and a north bridge, while integrated PIC and south bridge unit 1810 includes a PIC and a south bridge. FIG. 19 shows an attached computer module with integrated CPU/NB/Graphics 1915 and Integrated HIC/SB 1920. FIG. 20 shows an attached computer module with single chip 2025 fully integrated: CPU, Cache, Core Logic, Graphics controller and Interface controller.

FIG. 14 is a detailed block diagram of one embodiment of the HIC of the present invention. As shown in FIG. 14, HIC 1600 comprises bus controller 1610, translator 1620, transmitter 1630, receiver 1640, a PLL 1650, an address/data multiplexer (A/D MUX) 1660, a read/write controller (RD/WR Cntl) 1670, a video serial to parallel converter 1680 and a CPU control & general purpose input/output latch/driver (CPU CNTL & GPIO latch/driver) 1690.

HIC 1600 is coupled to an optional flash memory BIOS configuration unit 1601. Flash memory unit 1601 stores basic input output system (BIOS) and PCI configuration information and supplies the BIOS and PCI configuration information to A/D MUX 1660 and RD/WR Control 1670, which control the programming, read, and write of flash memory unit 1601.

Bus controller 1610 is coupled to the host PCI bus, which is also referred to herein as the primary PCI bus, and manages PCI bus transactions on the host PCI bus. Bus controller 1610 includes a slave (target) unit 1611 and a master unit 1616. Both slave unit 1611 and master unit 1616 each include two first in first out (FIFO) buffers, which are preferably asynchronous with respect to each other since the input and output of the two FIFOs in the master unit 1616 as well as the two FIFOs in the slave unit 1611 are clocked by different clocks, namely the PCI clock and the PCK. Additionally, slave unit 1611 includes encoder 1622 and decoder 1623, while master unit 1616 includes encoder 1627 and decoder 1628. The FIFOs 1612, 1613, 1617 and 1618 manage data transfers between the host PCI bus and the XPBus, which in the embodiment shown in FIG. 14 operate at 33 MHz and 66 MHz, respectively. PCI address/data (AD) from the host PCI bus is entered into FIFOs 1612 and 1617 before they are encoded by encoders 1622 and 1627. Encoders 1622 and 1627 format the PCI address/data bits to a form more suitable for parallel to serial conversion prior to transmittal on the XPBus. Similarly, address and data information from the receivers is decoded by decoders 1623 and 1628 to a form more suitable for transmission on the host PCI bus.

The multiplexed parallel A/D bits and some control bits input to transmitter 1630 are serialized by parallel to serial converters 1632 of transmitter 1630 into 10 bit packets. These bit packets are then output on data lines PD0 to PD3 of the XPBus. Other control bits are serialized by parallel to serial converter 1633 into 10 bit packets and sent out on control line PCN of the XPBus.

FIG. 15 is a detailed block diagram of one embodiment of the PIC of the present invention. PIC 11100 is nearly identical to HIC 1600 in its function, except that HIC 1600

interfaces the host PCI bus to the XDBus while PIC 11100 interfaces the secondary PCI bus to the XDBus. Similarly, the components in PIC 11100 serve the same function as their corresponding components in HIC 1600. Reference numbers for components in PIC 11100 have been selected such that a component in PIC 11100 and its corresponding component in HIC 1600 have reference numbers having the same two least significant digits. Thus for example, the bus controller in PIC 11100 is referenced as bus controller 11110 while the bus controller in HIC 1600 is referenced as bus controller 1610. As many of the elements in PIC 11100 serve the same functions as those served by their corresponding elements in HIC 1600 and as the functions of the corresponding elements in HIC 1600 have been described in detail above, the function of elements of PIC 11100 having corresponding elements in HIC 1600 will not be further described herein. Reference may be made to the above description of FIG. 14 for an understanding of the functions of the elements of PIC 11100 having corresponding elements in HIC 1600.

FIG. 16 is a schematic diagram of lines PCK, PD0 to PD3, and PCN. These lines are unidirectional LVDS lines for transmitting clock signals and bits from the HIC to the PIC. The bits on the PD0 to PD3 and the PCN lines are sent synchronously within every clock cycle of the PCK. Another set of lines, namely PCKR, PDR0 to PDR3, and PCNR, are used to transmit clock signals and bits from the PIC to HIC. The lines used for transmitting information from the PIC to the HIC have the same structure as those shown in FIG. 16, except that they transmit data in a direction opposite to that in which the lines shown in FIG. 16 transmit data. In other words they transmit information from the PIC to the HIC. The bits on the PDR0 to PDR3 and the PCNR lines are sent synchronously within every clock cycle of the PCKR. Some of the examples of control information that may be sent in the reverse direction, i.e., on PCNR line, include a request to switch data bus direction because of a pending operation (such as read data available), a control signal change in the target requiring communication in the reverse direction, target busy, and transmission error detected.

The XDBus which includes lines PCK, PD0 to PD3, PCN, PCKR, PDR0 to PDR3, and PCNR, has two sets of unidirectional lines transmitting clock signals and bits in opposite directions. The first set of unidirectional lines includes PCK, PD0 to PD3, and PCN. The second set of unidirectional lines includes PCKR, PDR0 to PDR3, and PCNR. Each of these unidirectional set of lines is a point-to-point bus with a fixed transmitter and receiver, or in other words a fixed master and slave bus. For the first set of unidirectional lines, the HIC is a fixed

transmitter/master whereas the PIC is a fixed receiver/slave. For the second set of unidirectional lines, the PIC is a fixed transmitter/master whereas the HIC is a fixed receiver/slave. The LVDS lines of XPBus, a cable friendly and remote system I/O bus, transmit fixed length data packets within a clock cycle.

The XPBus lines, PD0 to PD3, PCN, PDR0 to PDR3 and PCNR, and the video data and clock lines, VPD and VPCCK, are not limited to being LVDS lines, as they may be other forms of bit based lines. For example, in another embodiment, the XPBus lines may be IEEE 1394 lines.

It is to be noted that although each of the lines PCK, PD0 to PD3, PCN, PCKR, PDR0 to PDR3, PCNR, VPCCK, and VPD is referred to as a line, in the singular rather than plural, each such line may contain more than one physical line. For example, in the embodiment shown in FIG. 16, each of lines PCK, PD0 to PD3 and PCN includes two physical lines between each driver and its corresponding receiver. The term line, when not directly preceded by the terms physical or conductive, is herein used interchangeably with a signal or bit channel of one or more physical lines for transmitting a signal. In the case of non-differential signal lines, generally only one physical line is used to transmit one signal. However, in the case of differential signal lines, a pair of physical lines is used to transmit one signal. For example, a pair of physical lines together transmit a signal in a bit line or bit channel in an LVDS or IEEE 1394 interface.

A bit based line (i.e., a bit line) is a line for transmitting serial bits. Bit based lines typically transmit bit packets and use a serial data packet protocol. Examples of bit lines include an LVDS line, an IEEE 1394 line, and a Universal Serial Bus (USB) line.

FIGS. 21 and 22 are tables including the pin number, symbol, signal, standard and description for the pins on the peripheral and video connectors, respectively. FIG. 23 is a table showing the symbols, signals, data rate and description of signals on the XPBus, where RTN indicates a ground (GND) reference. In the above tables, P&D stands for plug and display and is a trademark of the Video Electronics Standards Association (VESA) for the Plug and Display standard, DDC2:SCL and DDC2:SDA stand for the VESA display data channel (DDC) standard 2 clock and data signals, respectively, SV stands for super video, V33 is 3.3 volts, and V5 is 5.0 volts. TMDS stands for Transition Minimized Differential Signaling and is a trademark of Silicon Images and refers to their Panel Link technology, which is in turn a trademark for their LVDS technology. TMDS is used herein to refer to the Panel Link technology or technologies compatible therewith.

The reserved data packet types can be used to support non-PCI bus transactions, e.g., USB transactions. The bits sent in the first nibble of each data packet indicate the type of the data packet. FIG. 24 is a table showing different types of first nibbles and their corresponding data packet types.

IN THE CLAIMS

1-13. (Cancelled)

14. (New) A computer for information transactions, comprising:

a central processing unit directly connected to a first Low Voltage Differential Signal (LVDS) channel comprising two sets of unidirectional, serial bit channels to transmit data in opposite directions;

a main memory directly connected to the central processing unit; and

a peripheral bridge directly coupled to the central processing unit without any intervening Peripheral Component Interconnect ("PCI") bus, wherein the peripheral bridge directly conveys an encoded serial bit stream of address and data bits of a PCI bus transaction over a second LVDS channel comprising two sets of unidirectional, serial bit channels to transmit data in opposite directions.

15. (New) The computer of claim 14, further comprising a connector coupled to a console, wherein the second LVDS channel communicates the encoded serial bit stream of address and data bits of the PCI bus transaction to the console.

16. (New) The computer of claim 15 further comprising a graphics controller that conveys digital video display information from the connector to the console.

17. (New) The computer of claim 15 wherein the console comprises a mass storage device that couples to the second LVDS channel.

18. (New) A computer system, comprising:

a console comprising a Liquid Crystal Display (LCD) display and a first Low Voltage Differential Signal (LVDS) channel comprising two sets of unidirectional, serial bit channels to transmit data in opposite directions; and

a computer coupled to the console through a connector, the computer comprising

an integrated central processing unit and graphics controller in a single chip directly connected to a second LVDS channel comprising two sets of unidirectional, serial bit channels to transmit data in opposite directions; and

a mass storage unit coupled to the central processing unit and graphics controller in a single chip;

wherein the graphics controller conveys digital video display information to the LCD display through the connector upon coupling to the console.

19. (New) The computer system of claim 18 wherein the computer further comprises a peripheral bridge directly coupled to the central processing unit without any intervening Peripheral Component Interconnect ("PCI") bus, the peripheral bridge directly conveying an encoded serial bit stream of address and data bits of a PCI bus transaction.

20. (New) The computer system of claim 19 wherein the peripheral bridge conveys the encoded serial bit stream of address and data bits of the PCI bus transaction to the first LVDS channel upon coupling of the computer to the console.

21. (New) A computer, comprising:

a central processing unit directly connected to a first Low Voltage Differential Signal (LVDS) channel comprising two sets of unidirectional, serial bit channels to transmit Universal Serial Bus (USB) Protocol data in opposite directions;

a second LVDS channel comprising two sets of unidirectional, serial bit channels to transmit data in opposite directions;

a connector coupled to the first LVDS channel; and

a main memory directly coupled to the central processing unit.

22. (New) The computer of claim 21 wherein the second LVDS channel communicates an encoded serial bit stream of address and data bits of a Peripheral Component Interconnect ("PCI") bus transaction.

23. (New) The computer of claim 21 wherein the first LVDS channel conveys Universal Serial Bus (USB) Protocol data to a console through the connector.

24. (New) A computer, comprising:

an integrated central processing unit and graphics controller in a single chip directly connected to a Low Voltage Differential Signal (LVDS) channel comprising two sets of unidirectional, serial bit channels to transmit data in opposite directions; and

a main memory directly coupled to the integrated central processing unit and graphics controller; and

a differential signal channel directly extending from the integrated central processing unit and graphics controller to convey digital video display information.

25. (New) The computer of claim 24 wherein the LVDS channel conveys an encoded serial bit stream of address and data bits of a Peripheral Component Interconnect ("PCI") bus transaction.

26. (New) The computer of claim 24 further comprising a connector coupled to a console.

27. (New) The computer of claim 26 wherein the computer conveys Universal Serial Bus (USB) protocol data through the connector to the console.

28. (New) The computer of claim 26 further comprising a second differential signal channel comprising two sets of unidirectional, serial bit channels to transmit data in opposite directions, wherein the second differential signal channel conveys Universal Serial Bus (USB) protocol data through the connector to the console.

29. (New) A modular computer system, comprising:

a console comprising a first Low Voltage Differential Signal (LVDS) channel comprising two sets of unidirectional, serial bit channels to transmit data in opposite directions; and

a computer coupled to the console through a connector, the computer comprising

a central processing unit,

a mass storage unit coupled to the central processing unit,

a second LVDS channel comprising two sets of unidirectional, serial bit channels to transmit data in opposite directions, and

a peripheral bridge directly coupled to the central processing unit without any intervening Peripheral Component Interconnect bus, wherein the peripheral bridge directly conveys an encoded serial bit stream of address and data bits of a Peripheral Component Interconnect (“PCI”) bus transaction over the second LVDS channel; and

wherein the second LVDS channel communicates to the first LVDS channel in the console upon the computer coupling to the console.

30. (New) The modular computer system of claim 29 wherein the second LVDS channel conveys the encoded serial bit stream of the PCI bus transaction to the first LVDS channel upon coupling of the computer module to the console.

31. (New) The modular computer system of claim 30 wherein the console further comprises a mass storage device that couples to the first and second LVDS channels.

32. (New) A modular computer system, comprising:

a console comprising a power supply; and

a computer coupled to the console through a connector, the computer comprising

a central processing unit,

a first Low Voltage Differential Signal (LVDS) channel comprising two sets of unidirectional, multiple serial bit channels to transmit data in opposite directions,

a peripheral bridge directly coupled to the first LVDS channel to communicate an encoded serial bit stream of address and data bits of a Peripheral Component Interconnect (“PCI”) bus transaction, the peripheral controller directly coupled to the central processing unit without any intervening PCI bus, and

wherein the power supply supplies power to the computer upon coupling to the console.

33. (New) The computer system of claim 32 further comprising a second LVDS channel that conveys the encoded serial bit stream of address and data bits of the PCI bus transaction, wherein the second LVDS channel directly extends from the central processing unit.

34. (New) A modular computer system, comprising:
a console comprising a first Low Voltage Differential Signal (LVDS) channel comprising
two sets of unidirectional, serial bit channels to transmit data in opposite directions; and
a computer that couples to the console, the computer comprising
an integrated central processing unit and graphics controller in a single chip,
directly connected to a second LVDS channel comprising two sets of unidirectional, serial bit
channels to transmit data in opposite directions, and
a connector that couples to the first LVDS channel in the console.

35. (New) The modular computer system of claim 34 wherein the second LVDS channel
conveys an encoded serial bit stream of address and data bits of a Peripheral Component
Interconnect ("PCI") bus transaction.

36. (New) The modular computer system of claim 34 wherein the first LVDS channel
conveys an encoded serial bit stream of address and data bits of a Peripheral Component
Interconnect ("PCI") bus transaction.

37. (New) The modular computer system of claim 34 wherein the computer conveys
Universal Serial Bus (USB) protocol data to the console upon the computer coupling to the
console.

38. (New) A computer, comprising:
a central processing unit;
a main memory directly connected to the central processing unit;
a peripheral bridge directly coupled to the central processing unit without any intervening
Peripheral Component Interconnect (PCI) bus, wherein the peripheral bridge directly conveys an
encoded serial bit stream of address and data bits of a Peripheral Component Interconnect (PCI)
bus transaction over a first Low Voltage Differential Signal (LVDS) channel comprising two sets
of unidirectional, serial bit channels to transmit data in opposite directions; and
a mass storage device directly coupled the peripheral bridge.

39. (New) The computer of claim 38 further comprising a graphics controller coupled to the peripheral bridge.

40. (New) A computer, comprising:

a central processing unit directly connected to a first Low Voltage Differential Signal (LVDS) channel to convey an encoded serial bit stream of address and data bits of a Peripheral Component Interconnect (PCI) bus transaction;

a main memory directly connected to the central processing unit; and

a peripheral bridge directly coupled to the central processing unit without any intervening PCI bus, wherein the peripheral bridge directly conveys the encoded serial bit stream of address and data bits of the (PCI) bus transaction over a second LVDS channel comprising two sets of unidirectional, serial bit channels to transmit data in opposite directions.

41. (New) The computer of claim 40 further comprising a connector coupled to a console, wherein the second LVDS channel communicates the encoded serial bit stream of address and data bits of the PCI bus transaction to the console.

42. (New) The computer of claim 41 further comprising a graphics controller to convey digital video display information from the connector to the console.

43. (New) The computer of claim 41 wherein the console comprises a peripheral device that couples to the second LVDS channel.

44. (New) A computer, comprising:

an integrated central processing unit and graphics controller in a single chip directly connected to a first Low Voltage Differential Signal (LVDS) channel comprising two sets of unidirectional, serial bit channels to transmit data in opposite directions;

a main memory directly coupled to the integrated central processing unit and graphics controller; and

a mass storage device comprising flash memory.

45. (New) The computer of claim 44 wherein the integrated graphics controller conveys digital video display signals through a second differential signal channel.

46. (New) The computer of claim 45 wherein the second differential signal channel conveys Transition Minimized Differential Signaling (TDMS) information.

47. (New) The computer of claim 44 wherein the first LVDS channel conveys an encoded serial bit stream of address and data bits of a Peripheral Component Interconnect (PCI) bus transaction.

48. (New) The computer of claim 44 further comprising a connector that conveys Universal Serial Bus (USB) protocol information to a console.

49. (New) The computer of claim 48 further comprising a second LVDS channel comprising two sets of unidirectional, serial bit channels to transmit data in opposite directions, wherein the second LVDS channel conveys said USB protocol information to the console through the connector.

50. (New) A computer, comprising:

a Central Processing Unit (CPU) directly connected to a Low Voltage Differential Signal (LVDS) channel comprising two sets of multiple, unidirectional, serial bit channels to convey an encoded serial bit stream of encoded address and data bits of a Peripheral Component Interconnect ("PCI") bus transaction in opposite directions;

a main memory directly connected to the CPU; and

a mass storage device coupled to the CPU.

51. (New) The computer of claim 50 further comprising a connector, wherein the connector connects to a console comprising a power supply, and the power supply supplies power to the computer upon coupling to the console.

52. (New) The computer of claim 50 wherein the mass storage device comprises flash memory.

53. (New) A computer, comprising:

an integrated central processing unit and graphics controller in a single chip directly connected to a first Low Voltage Differential Signal (LVDS) channel comprising two sets of multiple, unidirectional, serial bit channels to convey an encoded serial bit stream of encoded address and data bits of a Peripheral Component Interconnect (PCI) bus transaction in opposite directions;

a main memory directly coupled to the integrated central processing unit and graphics controller; and

an Ethernet communication device coupled to the first LVDS channel.

54. (New) The computer of claim 53 further comprising a connector, wherein the connector connects to a console comprising a power supply, and the power supply supplies power to the computer upon coupling to the console.

REMARKS

This is a preliminary amendment of the present continuation reissue of U.S. Application 13/294,108, which is a continuation reissue of U.S. Application No. 12/561,138, which is a continuation reissue of U.S. Application No. 11/056,604, for the reissue of U.S. Patent No. 6,643,777 (the “777 patent”). Claims 1-13 are cancelled, and new claims 14-54 are added. Accordingly, claims 14-54 are now pending.

Drawings and Specification

At col. 5, lines 9-13, the ‘777 patent incorporated by reference U.S. Application Nos. 09/149,548, now issued as U.S. Patent No. 6,216,185 (the “185 patent”) and 09/149,882, now issued as U.S. Patent No. 6,345,330 (the “330 patent”), which, in turn, claimed the benefit of and incorporated by reference U.S. Provisional Application No. 60/083,886 (the “886 provisional application”) (*See* checked incorporation by reference box in utility patent application transmittal of U.S. Application No. 09/149,882 filed on September 8, 1998). By this preliminary amendment, the present application is amended to specifically include certain figures and text from the ‘185 patent, the ‘330 patent, and the ‘886 provisional application. Specifically, the present application is amended to add new FIG. 9 through FIG. 24, as well as accompanying text at col. 4, line 51 and col. 13, line 33. This corresponds to: (a) FIG. 2b, FIG. 3, FIG. 4, and FIG. 7 of the ‘185 patent; (b) the text of the ‘185 patent at col. 2, lines 35-43; col. 3, lines 22-23, 25-28, and 36; col. 4, lines 10-15 and 33-67; col. 5, lines 1-67; col. 6, lines 1-13; col. 8, lines 34-55; col. 13, lines 1-47; and col. 15, lines 24-47; (c) FIG. 2, FIG. 3, FIG. 4, FIG. 6, FIG. 11, FIG. 18, FIG. 19, FIG. 20, and FIG. 35 of the ‘330 patent; (d) the text of the ‘330 patent at col. 2, lines 20-67; col. 3, lines 1-38, 45-53, and 57-58; col. 4, lines 3-4, 21-25, 35-36, and 66-67; col. 5, lines 66-67, col. 6, lines 1-35; col. 7, lines 28-66; col. 8, lines 61-67; col. 11, lines 52-67; col. 12, lines 1-6; col. 13, lines 46-62, col. 15, lines 11-67; col. 16, lines 1-5 and col. 19, lines 13-15 and 22-25; (e) Figure 8 and Figure 9 of the ‘886 provisional application; and (f) the text of the ‘886 provisional application as originally included in legends of Figure 8 and Figure 9.

Status of Claims and Support for Claim Changes

As noted above, claims 1-13 are cancelled, and new claims 14-54 are added by this paper. The new claims include limitations of the type previously considered in parent applications. Entry and consideration of the foregoing amendments is respectfully requested.

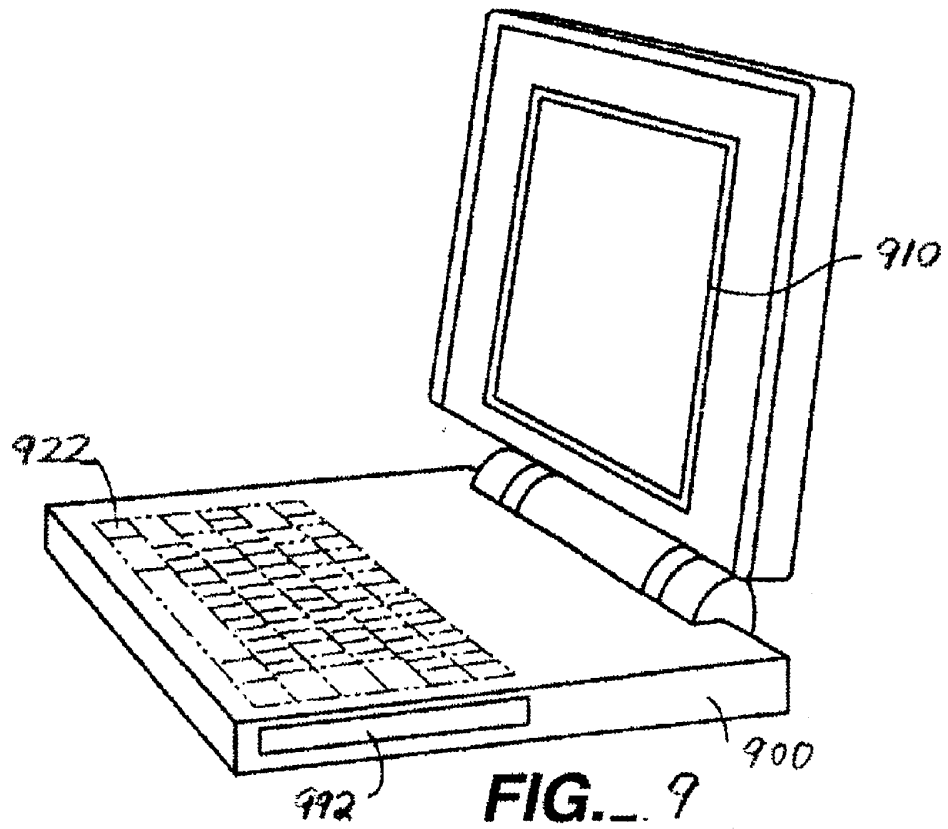
The Director is hereby authorized to charge any appropriate fees under 37 C.F.R. §§1.16, 1.17, and 1.21 that may be required by this paper, and to credit any overpayment, to Deposit Account No. 50-1283.

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Respectfully submitted,
Cooley LLP
By: _____

William S. Galliani
Reg. No. 33,885

NEW SHEET



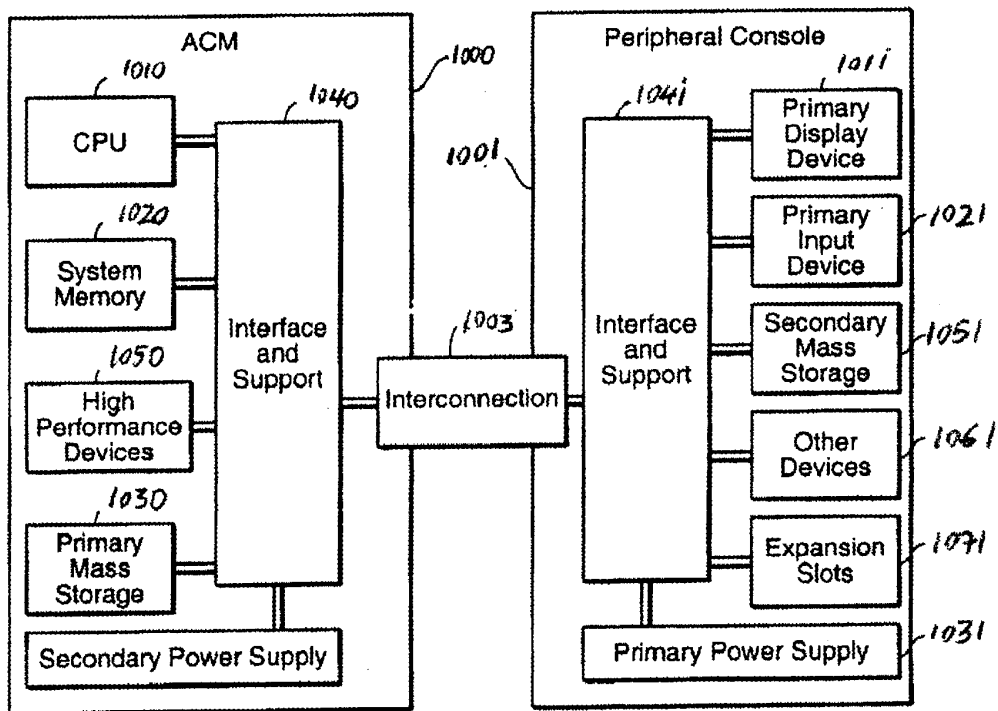


FIG. 10

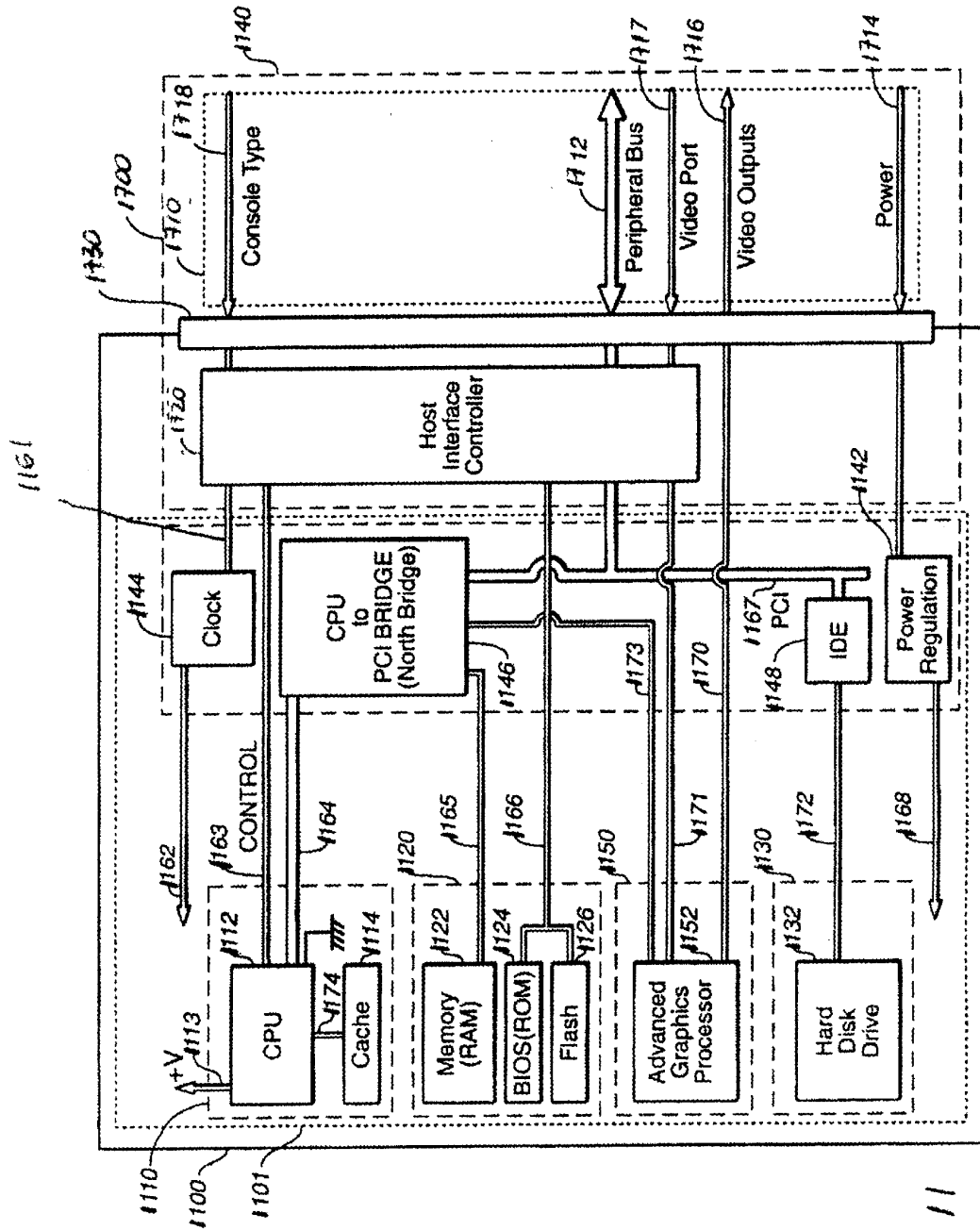


FIG. 11

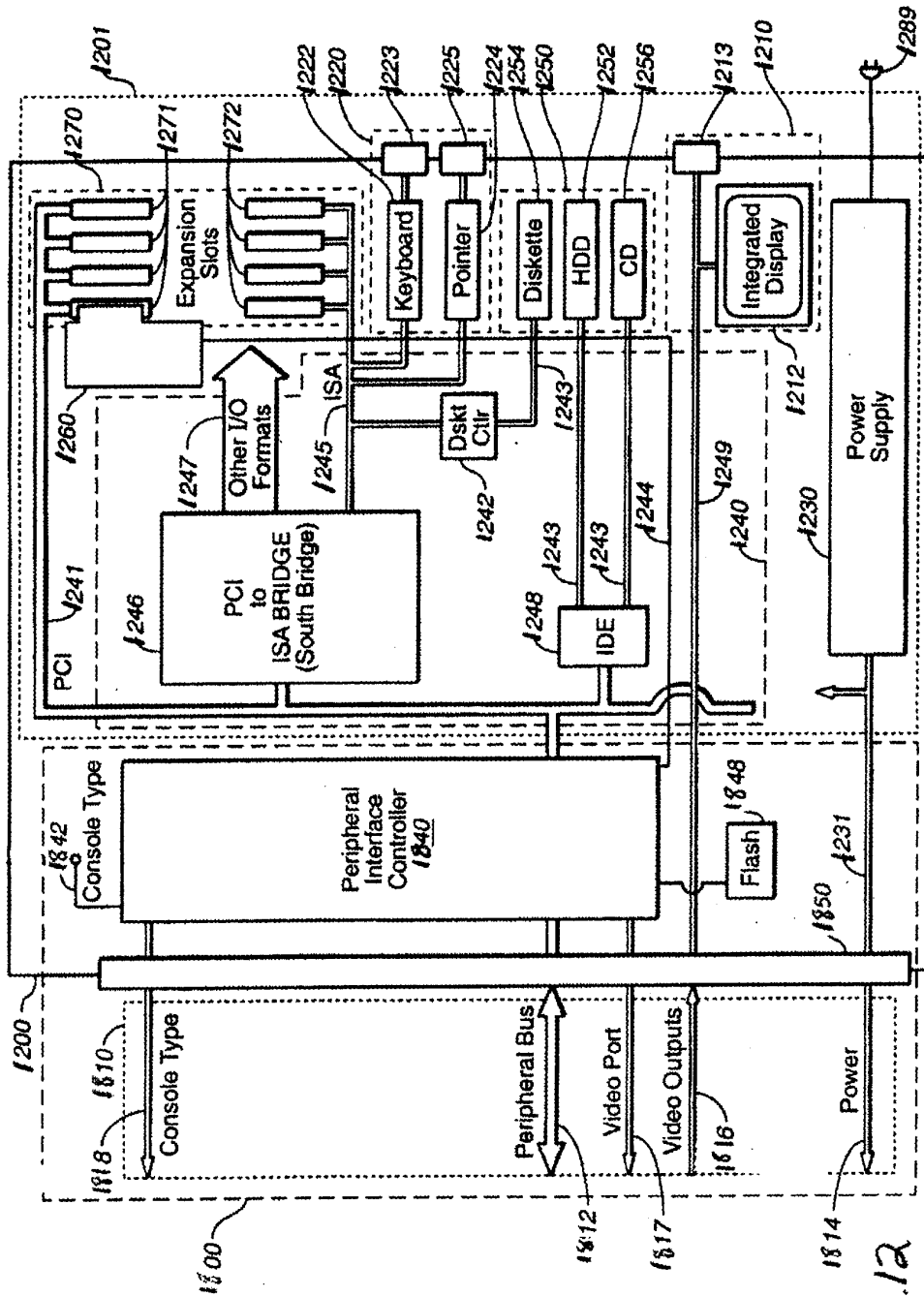


FIG. 12

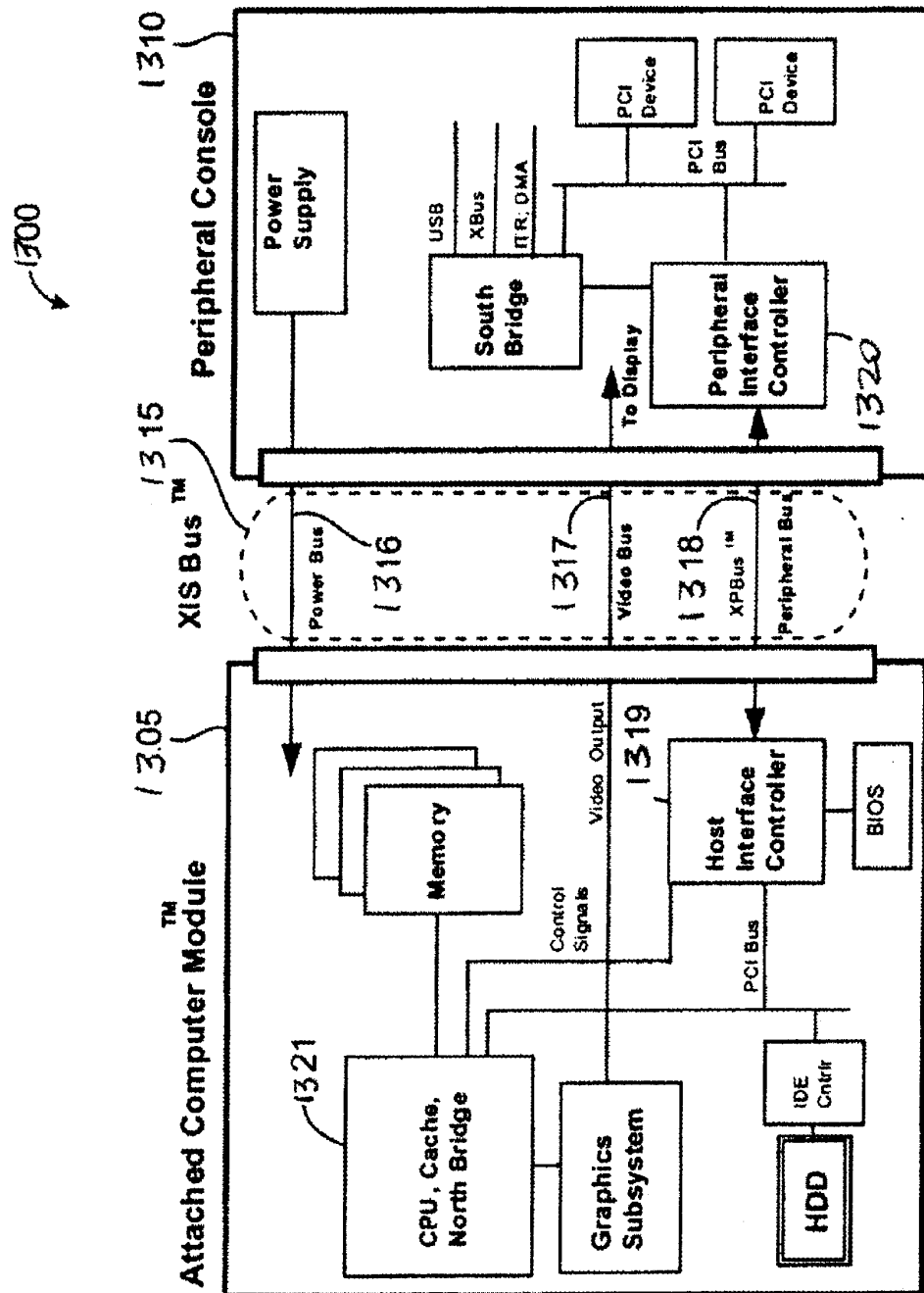


FIG. 13

NEW SHEET

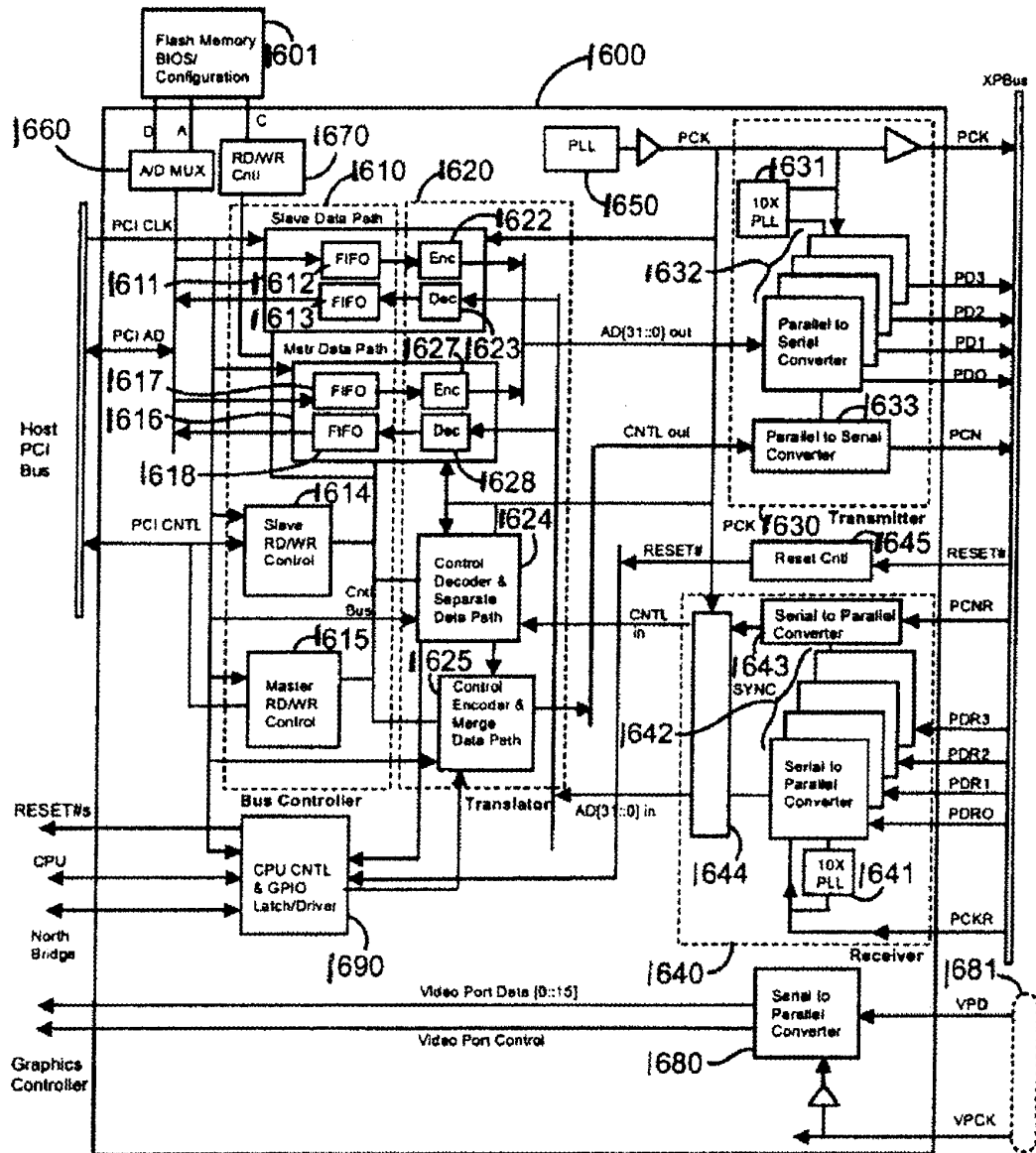


FIG. 14

NEW SHEET

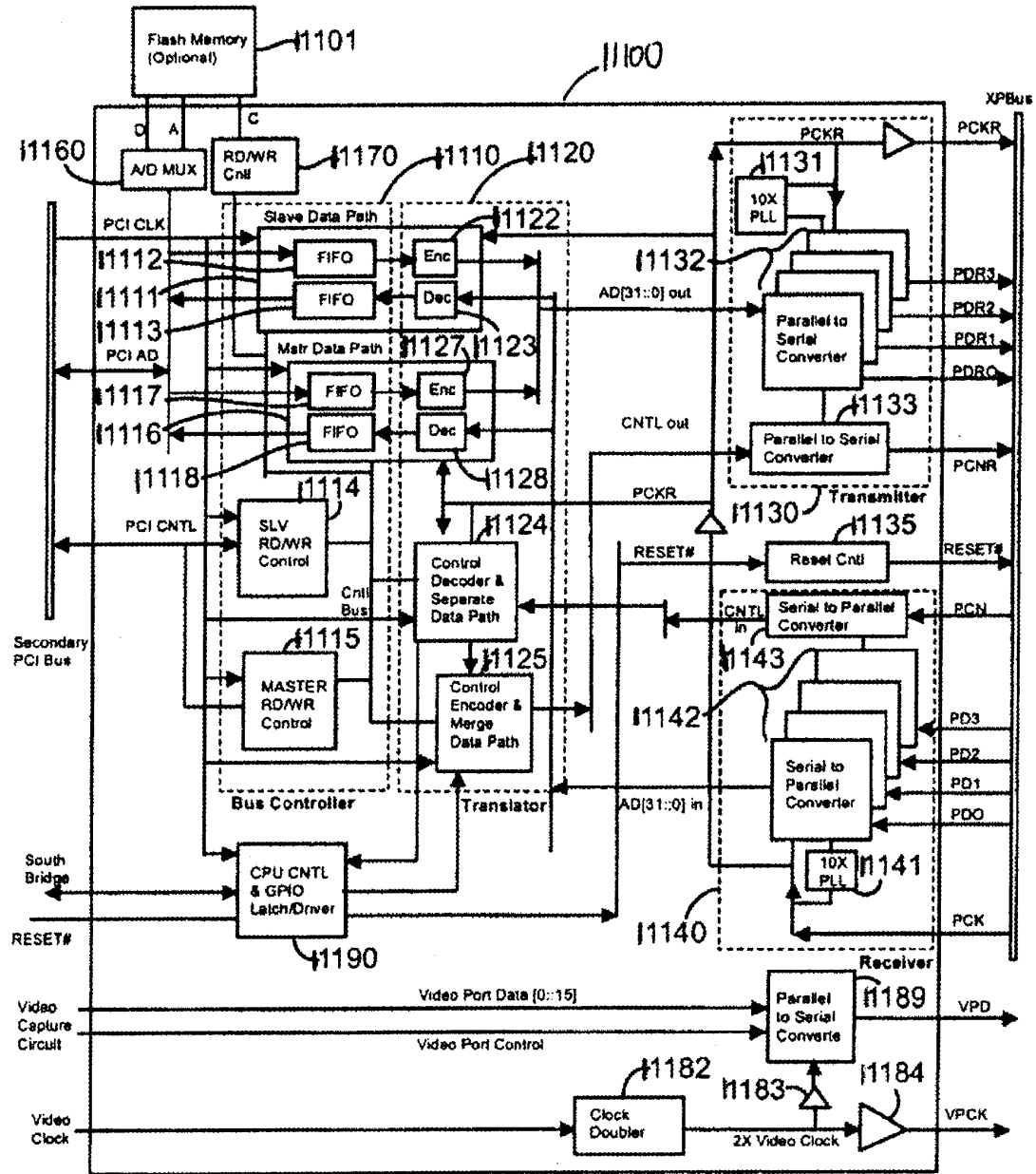


FIG. 15

NEW SHEET

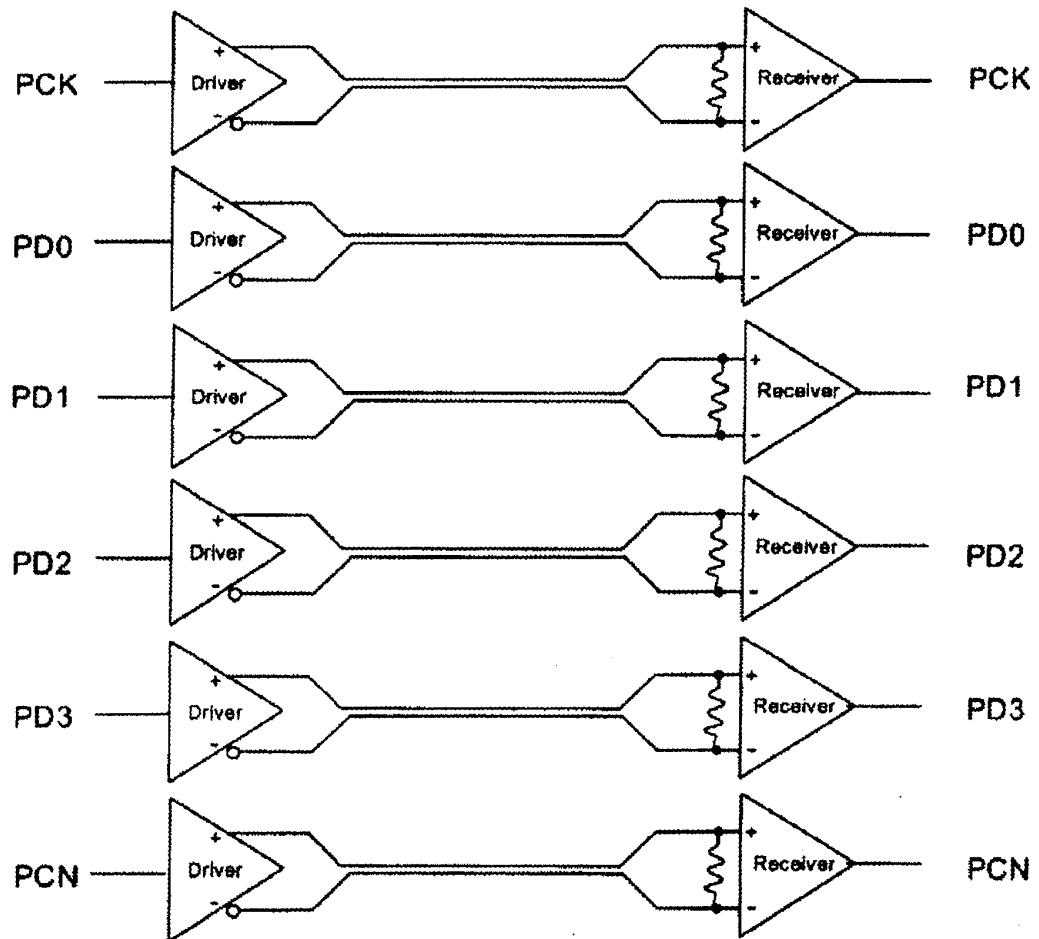


FIG. 16

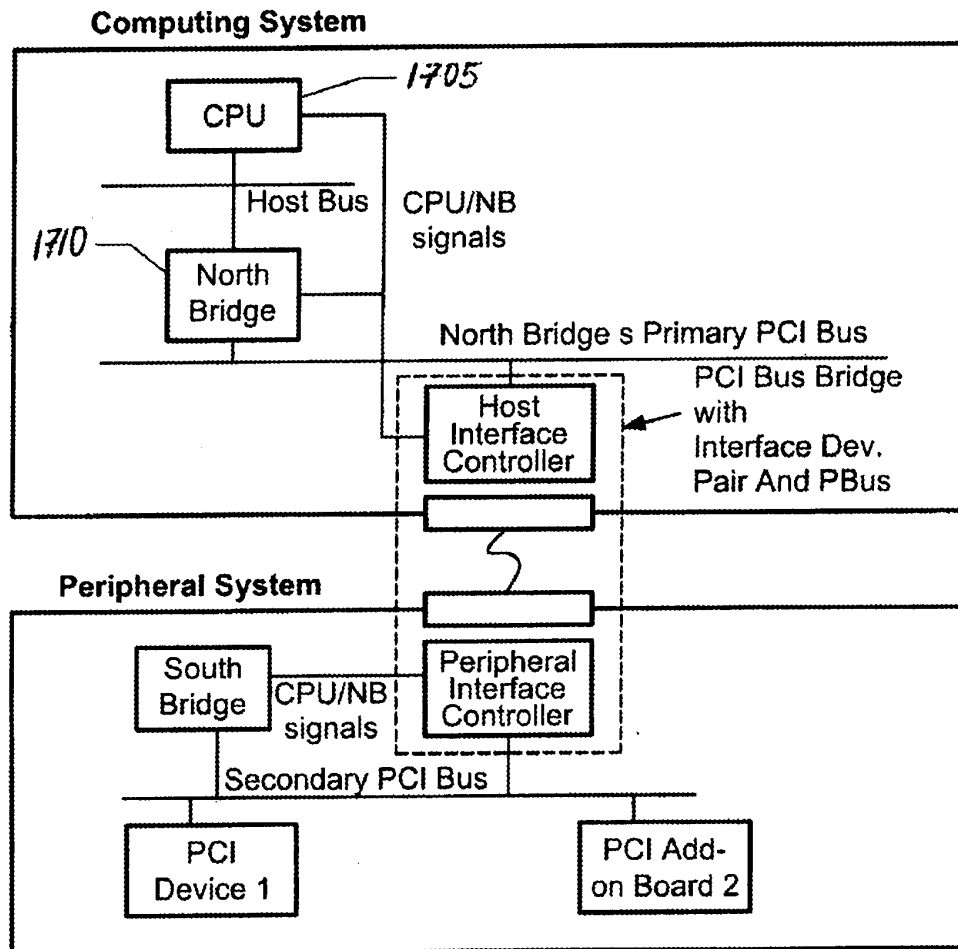


FIGURE 17

NEW SHEET

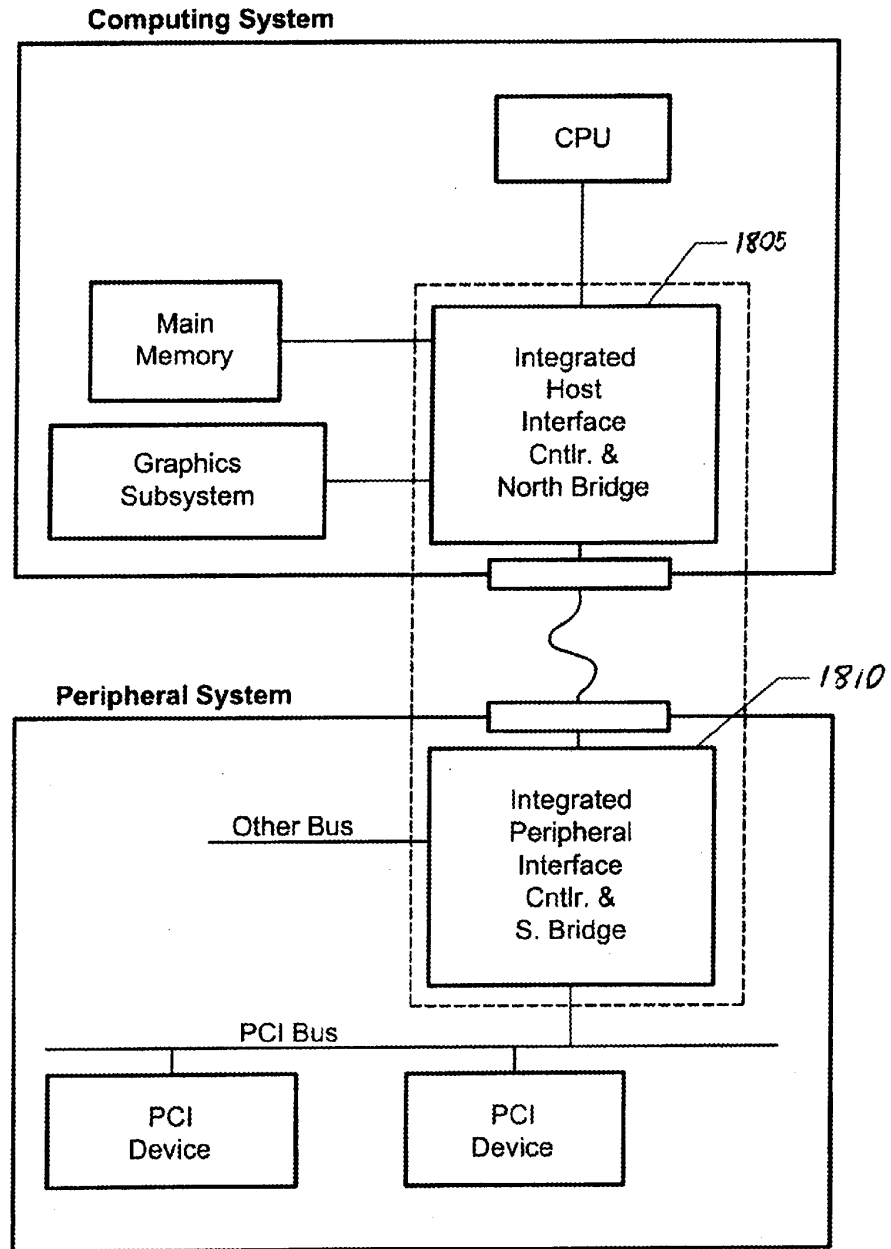
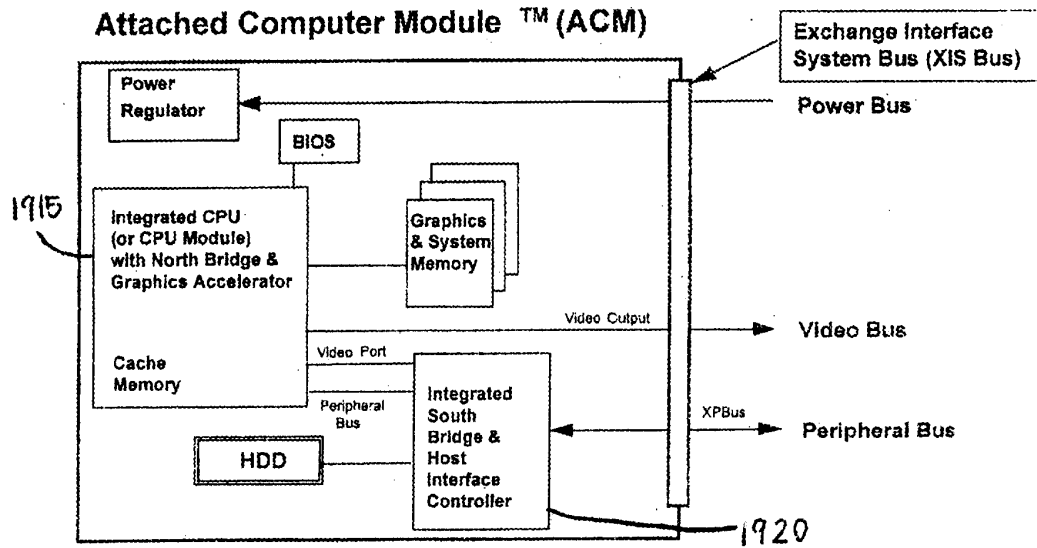


FIGURE 18

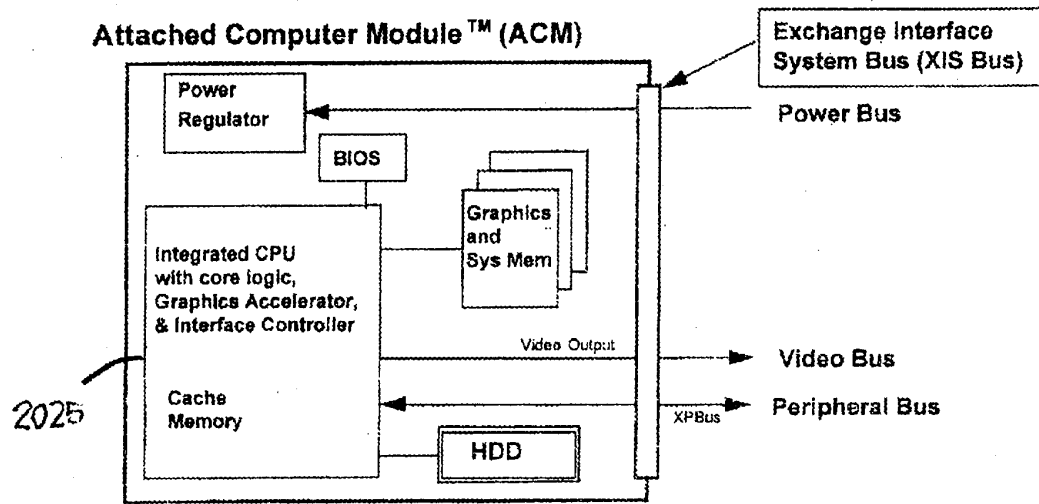
NEW SHEET



Attached Computer Module with Integrated CPU/NB/Graphics and Integrated HIC/SB

FIG. 19

NEW SHEET



Attached Computer Module with Single Chip fully integrated: CPU, Cache, Core logic, Graphics controller and Interface controller

FIG. 20

Pin No.	Symbol	Signal	Standard	Description
P2	PDR0 +	LVDS		Peripheral data reverse 0 +
P3	PDR0 -	LVDS		Peripheral data reverse 0 -
P5	PDR1 +	LVDS		Peripheral data reverse 1 +
P6	PDR1 -	LVDS		Peripheral data reverse 1 -
P8	PDR2 +	LVDS		Peripheral data reverse 2 +
P9	PDR2 -	LVDS		Peripheral data reverse 2 -
P11	PCKR +	LVDS		Peripheral clock reverse +
P12	PCKR -	LVDS		Peripheral clock reverse -
P15	PDR3 +	LVDS		Peripheral data reverse 3 +
P16	PDR3 -	LVDS		Peripheral data reverse 3 -
P18	PCNR +	LVDS		Peripheral control reverse +
P19	PCNR -	LVDS		Peripheral control reverse -
P24	PD0 +	LVDS		Peripheral data 0 +
P25	PD0 -	LVDS		Peripheral data 0 -
P27	PD1 +	LVDS		Peripheral data 1 +
P28	PD1 -	LVDS		Peripheral data 1 -
P30	PD2 +	LVDS		Peripheral data 2 +
P31	PD2 -	LVDS		Peripheral data 2 -
P33	PCK +	LVDS		Peripheral clock +
P34	PCK -	LVDS		Peripheral clock -
P37	PD3 +	LVDS		Peripheral data 3 +
P38	PD3 -	LVDS		Peripheral data 3 -
P40	PCN +	LVDS		Peripheral control +
P41	PCN -	LVDS		Peripheral control -
P13	Config 0	Static	3.3v or GND	Configuration bit 0
P35	Config 1	Static	3.3v or GND	Configuration bit 1
P1P4,P7,P10, P14,P17,P23,P26, P29,P32,P36,P39	GND		GND	Ground

FIG. 21

Pin No.	Symbol	Signal	Standard	Description
V2	Red Video	Analog		Video
V4	Green Video	Analog		Video
V6	Blue Video	Analog		Video
V8	HSYNC			Horizontal Sync
V9	VSNC			Vertical Sync
V11	DDC2 SCL		VESA DDC std 2	DDC Clock
V12	DDC2 SDA		VESA DDC std 2	DDC Data
V14	TV-CV/CNTL 0			TV Composite Video
V15	SV Y/CNTL 1		Super Video	SV Luminance or Control 1
V16	SV C/CNTL 2		Super Video	SV Chrominance or Control 2
V24	D0 +	TMDS	VESA P & D	Data 0 +
V25	D0 -	TMDS	VESA P & D	Data 0 -
V27	CLK +	TMDS	VESA P & D	Clock +
V28	CLK -	TMDS	VESA P & D	Clock -
V30	D1 +	TMDS	VESA P & D	Data 1 +
V31	D1 -	TMDS	VESA P & D	Data 1 -
V33	D2 +	TMDS	VESA P & D	Data 2 +
V34	D2 -	TMDS	VESA P & D	Data 2 -
V37	VPCK +	LVDS		Video Port Pixel Clock +
V38	VPCK -	LVDS		Video Port Pixel Clock -
V40	VPD +	LVDS		Video Port Pixel Data +
V41	VPD -	LVDS		Video Port Pixel Data -
V13	Config 2		3.3v or GND	Configuration bit 2
V35	Config 3		3.3v or GND	Configuration bit 3
V1, V3, V5, V7, V10, V23, V26, V29, V32, V36, V39, V42, V43, V44	GND		GND	Ground

FIG. 22

NEW SHEET

	Symbol	Signal	Data Rate	Description
1	PD0 RTN			GND
2	PD0 +	Synch. To PCK	10 x clock rate	Computer to Peripheral LVDS Data 0 +
3	PD0 -			Computer to Peripheral LVDS Data 0 -
4	PD1 RTN			GND
5	PD1 +	Synch. To PCK	10 x clock rate	Computer to Peripheral LVDS Data 1 +
6	PD1 -			Computer to Peripheral LVDS Data 1 -
7	PD2 RTN			GND
8	PD2 +	Synch. To PCK	10 x clock rate	Computer to Peripheral LVDS Data 2 +
9	PD2 -			Computer to Peripheral LVDS Data 2 -
10	PD3 RTN			GND
11	PD3 +	Synch. To PCK	10 x clock rate	Computer to Peripheral LVDS Data 3 +
12	PD3 -			Computer to Peripheral LVDS Data 3 -
13	PCK RTN			GND
14	PCK +	Clock	Clock rate	Computer to Peripheral LVDS Clock +
15	PCK -			Computer to Peripheral LVDS Clock -
16	PCN RTN			GND
17	PCN +	Synch. To PCK	10 x clock rate	Computer to Peripheral LVDS Control +
18	PCN -			Computer to Peripheral LVDS Control -
19	PDR0 RTN			GND
20	PDR0 +	Synch. To PCKR	10 x clock rate	Peripheral to Computer LVDS Data 0 +
21	PDR0 -			Peripheral to Computer LVDS Data 0 -
22	PDR1 RTN			GND
23	PDR1 +	Synch. To PCKR	10 x clock rate	Peripheral to Computer LVDS Data 1 +
24	PDR1 -			Peripheral to Computer LVDS Data 1 -
25	PDR2 RTN			GND
26	PDR2 +	Synch. To PCKR	10 x clock rate	Peripheral to Computer LVDS Data 2 +
27	PDR2 -			Peripheral to Computer LVDS Data 2 -
28	PDR3 RTN			GND
29	PDR3 +	Synch. To PCKR	10 x clock rate	Peripheral to Computer LVDS Data 3 +
30	PDR3 -			Peripheral to Computer LVDS Data 3 -
31	PCKR RTN			GND
32	PCKR +	Reverse Dir. Clock	Clock rate	Peripheral to Computer LVDS Clock +
33	PCKR -			Peripheral to Computer LVDS Clock -
34	PCNR RTN			GND
35	PCNR +	Synch. To PCKR	10 x Clock rate	Peripheral to Computer LVDS Control +
36	PCNR -			Peripheral to Computer LVDS Control -
37	RESET#		Asynchronous	Reset

FIG. 23

ID bits (P0 P1 P2 P3)	Data Packet Type
XX00	PCI 1st address/data segment
XX10	PCI 2nd address/data segment
0001	Control 1st segment with PCI response
1001	Control 1st segment without PCI response
0101	Control 2nd segment with PCI response
1101	Control 2nd segment without PCI response
0011	Reserved
1011	Reserved
0111	Initialization
1111	NOOP

FIG. 24

REISSUE APPLICATION DECLARATION BY THE INVENTOR

Docket Number (Optional)

ACQI-006/05US 310578-2072

I hereby declare that

Each inventor's residence, mailing address and citizenship are stated below next to their name.

I believe the inventors named below to be the original and first inventor(s) of the subject matter which is described and claimed in patent number 6643777 granted November 4, 2003 and for which a reissue patent is sought on the invention entitled DATA SECURITY METHOD AND DEVICE FOR COMPUTER MODULES

the application of which

☒ is attached hereto.

☐ was filed on _____ as reissue application number _____

and was amended on _____
(If applicable)

I have reviewed and understand the contents of the above-identified application, including the claims, as amended by any amendment referred to above.

I acknowledge the duty to disclose information which is material to patentability as defined in 37 CFR 1.56.

☐ I hereby claim foreign priority benefits under 35 U.S.C. 119(a)-(d) or (f), or 365(b). Attached is form PTO/SB/02B (or equivalent) listing the foreign applications

I verily believe the original patent to be wholly or partly inoperative or invalid, for the reasons described below. (Check all boxes that apply.)

☐ by reason of a defective specification or drawing.

☒ by reason of the patentee claiming more or less than he had the right to claim in the patent

☐ by reason of other errors

At least one error upon which reissue is based is described below. If the reissue is a broadening reissue, such must be stated with an explanation as to the nature of the broadening.

Claim 8 of U.S. Patent No. 6,643,777 recites a "user identification input device." Elimination of this term broadens the scope of the claimed invention, as recited at least in new claim 14.

The present application is a reissue continuation of U.S. Application No. 13/294,108, which is a reissue continuation of U.S. Application No. 12/561,138, which is a reissue continuation of U.S. Application No. 11/056,604, for the reissue of U.S. Patent No. 6,643,777. An intent for broadening was indicated in U.S. Application No. 11/056,604 within 2 years of the grant of the original patent.

(Page 1 of 2)

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1045062 v1/HN

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(REISSUE APPLICATION DECLARATION BY THE INVENTOR, page 2)

Docket Number (Optional)
ACQI-006/05US 310578-2072

All errors corrected in this reissue application arose without any deceptive intention on the part of the applicant.

Note: To appoint a power of attorney, use form PTO/SB/81.

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WARNING:

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I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine and imprisonment, or both, under 18 U.S.C. 1001, and that such willful false statements may jeopardize the validity of the application, any patent issuing thereon, or any patent to which this declaration is directed.

Full name of sole or first inventor (given name, family name)

William W. Y. Chu

Inventor's signature

Date

Residence

Citizenship

Los Altos, CA

US

Mailing Address

1320 Miravalle Avenue, Los Altos, CA 94024

Full name of second joint inventor (given name, family name)

Inventor's signature

Date

Residence

Citizenship

Mailing Address

☐ Additional joint inventors or legal representative(s) are named on separately numbered sheets forms PTO/SB/02A or 02LR attached hereto.

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1045002 v1A-1N

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				Filing Date	July 30, 2012
				First Named Inventor	William W. Y. Chu
				Art Unit	
				Examiner Name	
Sheet	1	of	5	Attorney Docket Number	ACQI-006/05US 310578-2072

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		Number-Kind Code ² (if known)			
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		Attorney Docket Number	ACQI-006/05US 310578-2072
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				First Named Inventor	William W. Y. Chu
				Art Unit	
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Sheet	4	of	5	Attorney Docket Number	ACQI-006/05US 310578-2072

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		Country Code ³ "Number" ⁴ "Kind Code" ⁵ (if known)				
		EP 0722138 A1	7/17/1996	International Business Machines Corporation		
		JP 6-289953	10/18/1994	Hitachi, Ltd.		
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		WO 94/00970	1/6/1994	Oakeleigh Systems, Inc.		
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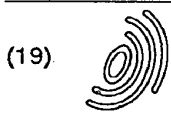
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(54) A cartridge-based design for portable and fixed computers

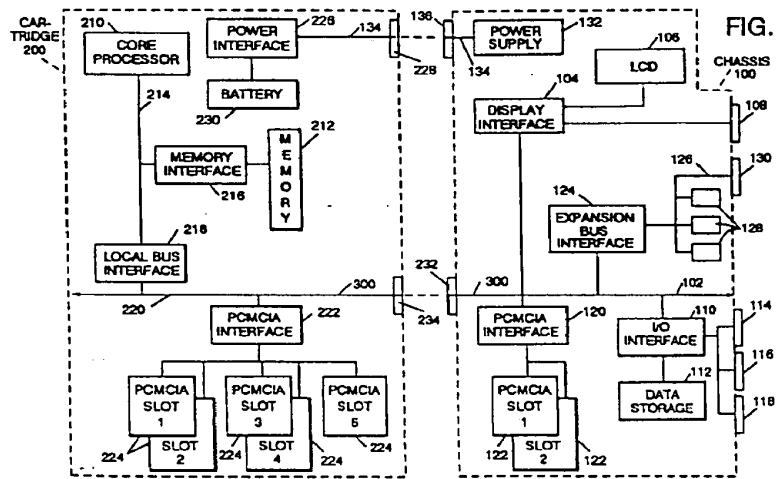
(57) A computer system includes a chassis and a cartridge having separate functional components that interface with one another over a common bus. The chassis includes a plurality of user interface modules, which are generally designed and packaged according to a particular application/work mode, each coupled to a first bus. The cartridge, on the other hand, includes components that can be shared among the various applications/work modes. Specifically, the cartridge has a core processor and memory coupled to a second bus, and at least one slot for housing a communication module that is coupled to the second bus.

internal device to its associated external peripheral device.

In addition, the cartridge may be designed to be configured by the user to have a first form and a second form. The cartridge of the first form may be utilized for portable computer processing systems such as laptop, notebook and sub-notebook systems. The cartridge of the second form may be designed to be narrow enough to be utilized in smaller portable computer processing systems, such as hand-held systems.

In another aspect, the computer system includes a chassis having an internal connector with a first portion in electrical contact with a first external peripheral device, and second portion in electrical contact with a second external peripheral device. An adapter is coupled between an internal device and the internal connector. The internal device is associated with either the first or second external peripheral devices. The adapter has either a first portion that connects the internal device to the first portion of the internal connector or a second portion that connects the internal device to the second portion of the internal connector in order to couple the

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Description

This application is related to U.S. Application No. (attorney docket No. YO994.288), filed concurrently herewith.

The invention relates to computer processing systems, and, more particularly, to the packaging of components of computer processing systems.

Computer processing systems on the market today can be segmented generally into two distinct categories: portable and fixed. Portable computer processing systems are designed to be portable between different work sites (i.e. office, home and travel) and may be characterized, for example, as luggable computer systems, laptop computer systems, notebook computer systems, sub-notebook computer systems, tablet computer systems and hand held computer systems, sometimes called Personal Digital Assistants (PDAs). On the other hand, fixed computer processing systems are intended to remain stationary in a single work site and may be characterized, for example, as desktop computer processing systems and tower computer processing systems.

Portable computer processing systems include components functionally equivalent to those of the larger fixed computer processing systems; yet the components of the portable computer processing system are designed and packaged for restricted dimensional and weight specifications required for portability. Such components often include, for example, a microprocessor, associated memory, a lightweight and compact keyboard and display, and PCMCIA standard devices such as fax-modems, wired local area network adapters, wireless local area network interface modules, digital data exchange adapters and hard disk drives. Yet, because of the dimensional and weight restrictions associated with the components of the portable computer processing system, the associated costs of the portable computer processing system are much greater than the costs of comparable fixed computer processing systems, and these additional costs are reflected in the purchase price of portable computer processing systems.

Moreover, a user may require two or more computer systems in separate applications/work modes. For example, a user may require a fixed desktop computer system for work and a portable laptop computer system for travel and home-use. In this case, the user is required to expend a heavy investment in purchasing the separate computer systems, which may limit the market for both the fixed and portable computer processing systems.

Because of these limiting cost factors, there is a long standing need in the field of computer processing systems to provide efficient and flexible computer processing systems while achieving low costs.

In another aspect, the invention relates to connecting means for connecting various peripheral devices internal to the chassis of a computer processing system, such as a PCMCIA fax-modem, to an associated peripheral device external to the chassis of the computer processing system, such as telephone line linked to a

telephone network. Typically, various internal peripheral devices are uniquely connected to their associated external peripheral device. For example, an internal PCMCIA fax-modem may be designed to extend out through a slot in the chassis and include a unique connector at its exposed end to mate with a telephone line. However, such unique connecting means among the various peripheral devices may create problems in portable computer processing systems, wherein a user must first disconnect the peripheral devices to move the computer processing system from, for example, a home environment to a work environment, and then reconnect the peripherals upon return, thereby experiencing undue delay and frustration.

The above-stated problems and related problems of the prior art are solved with the principles of the present invention, a cartridge-based design for portable and fixed computers. The computer system of the present invention includes a first chassis having a plurality of user interface modules each coupled to a first bus, and a second chassis having a plurality of user interface modules each coupled to a second bus. The user interface modules provide an interface to devices such as a keyboard, a mouse, a display, a speaker, a microphone, a data storage device or various other input/output devices which are generally designed and packaged according to a particular application/work mode (e.g., desk-based, taking home in the evenings, traveling, hand held).

The cartridge, on the other hand, includes components that can be shared among the various applications/work modes. Specifically, the cartridge has a core processor and memory coupled to a third bus, and possibly at least one slot for housing a module that is coupled to the third bus. The module may be, for example, a PCMCIA fax-modem, wired local-area network adapter card, or a data storage device such as PCMCIA hard disk drive. The third bus of the cartridge may be detachably connected to the first bus of the first chassis to form a first functional system, or the third bus of the cartridge may be detachably connected to the second bus of the second chassis to form a second functional system.

By detachably connecting the core processor, memory, and modules of the cartridge to the user interface modules of the separate chassis, the cartridge alone may be transferred from one environment to another. In each environment, the chassis may be optimized for use in their respective applications/work mode. By sharing components between computer processing systems in separate environments, the cost of the computer processing system in each environment is substantially decreased. Furthermore, the use of multiple user interfaces optimized for different work modes or tasks is allowed.

Moreover, the cartridge may be shared across various platforms. For example, both a fixed computer system and a portable computer processing system could incorporate the cartridge of the present invention. By sharing components between the two platforms, the cost of the desktop computer processing system and a port-

able computer processing system is substantially decreased.

In addition, the cartridge may be designed to be configured by the user in a first form and a second form. For example, the cartridge may include a first portion connected to a second portion by a hinge. The cartridge of the first form may be utilized for portable computer processing systems such as laptop, notebook and sub-notebook systems. The cartridge of the second form may be designed to be narrow enough to be utilized in smaller portable computer processing systems, such as handheld systems. By sharing components among the various portable computer processing systems, the costs of such systems is substantially decreased.

In another aspect, the computer system of the present invention includes a chassis having an internal connector with a first portion in electrical contact with a first external peripheral device. A second portion of the internal connector is in electrical contact with a second external peripheral device. An adapter is coupled between an internal device and the internal connector. The internal device is associated with either the first or second external peripheral devices. The adapter has either a first portion that connects the internal device to the first portion of the internal connector or a second portion that connects the internal device to the second portion of the internal connector in order to couple the internal device to its associated external peripheral device.

The benefits of using the adapter in conjunction with the internal connector of the chassis are two-fold. First, the user is not required to match the internal device to its associated external peripheral device because the connection between the two is automatic. And second, the internal device may be disconnected from the chassis without disturbing the associated external peripheral device, thus providing a user-friendly system.

FIG. 1 is a functional block diagram of a computer processing system in accordance with the present invention.

FIG. 2 is an isometric view of the cartridge of FIG. 1 configured in a first form.

FIG. 3 is an isometric view of the cartridge of FIG. 1 configured in a second form.

FIG. 4 is an isometric top view of the cartridge of FIG. 2 with PCMCIA cards inserted into slots 3, 4 and 5 plugged into a tablet style user interface chassis.

FIG. 5 is an isometric top view of the cartridge of FIG. 3 with PCMCIA cards inserted into slots 3 and 4 plugged into a hand held PDA style user interface chassis.

FIG. 6 is an exploded isometric view of the cartridge of FIG. 1 configured in a first form.

FIG. 7 is an exploded isometric view of the cartridge of FIG. 1 configured in a second form.

FIG. 8 illustrates adapters for connecting various PCMCIA cards to their respective peripheral devices in accordance with the present invention.

FIG. 9(a) is a functional block diagram of the adapters of FIG. 8 used in conjunction with a chassis to connect PCMCIA cards to their respective peripheral devices.

FIG. 9(b) is a cross-sectional side elevational view of FIG. 9(a).

FIG. 1 illustrates a computer processing system in accordance with the present invention. The computer processing system includes a chassis 100 detachably connected to a cartridge 200. The chassis 100 includes a plurality of user interface modules that provide an interface to devices such as a keyboard, a mouse, a display, a speaker, a microphone, a data storage device or various other input/output devices which are generally designed and packaged according to a particular application/work mode (e.g., desk-based, taking home in the evenings, traveling, hand held). The cartridge 200, on the other hand, includes components having computer functions (e.g. processing, memory, data storage) and communications functions that can be shared among the various applications/work modes. The cartridge 200 and the chassis 100 interface with one another over a common bus 300, for example, a PCI standard bus. The common bus 300 may include one or more parallel buses and/or one or more serial buses, such as an ACCESS bus, an INTEL serial bus, or an IEEE P.1394 serial bus. By detachably connecting the computer functions of the cartridge 200 to the user interface modules of the chassis 100, the cartridge 200 may be transferred from one environment to another. In each environment, the cartridge 200 may be connected to separate chassis' 100 which are optimized for use in their respective applications/work mode. By sharing components between computer processing systems in separate environments, the cost of the computer processing system in each environment is substantially decreased. Furthermore, the use of multiple user interfaces optimized for different work modes or tasks is allowed.

Specifically, the chassis 100 includes a plurality of user interface modules coupled to a first bus 102, which corresponds to the common bus 300. The user interface modules may include a display interface 104 for driving an LCD display 106 integrated into the chassis 100 or an external display connected to the chassis 100 via connector 108. The display interface typically includes a graphics controller and associated memory. The user interface modules may also include an I/O interface 110 that provides an interface to I/O devices such as a data storage device 112, an external keyboard or pointing device (i.e. mouse) via connector 114, and external peripheral devices via a serial port 116 and a parallel port 118. The data storage device 112 may be, for example, a magnetic hard disk drive, a tape back-up drive, a CD-ROM drive or an optical drive. The external peripheral devices connected to the serial port 116 and/or parallel port 118 may include a printer, a communication device such as a modem, a pointing device such as a mouse, and a data processing device that processes I/O data. The data processing device may be, for example,

a video interface adapter for processing video information or an analog to digital processing device for processing analog signals input to and/or output from the system, such as voice signals input to the system from a microphone and output from the system by a speaker.

The user interface modules may also include a PCMCIA interface 120 for driving at least one PCMCIA device inserted into PCMCIA slots 122. The chassis 100 of FIG. 1 includes two PCMCIA slots 122 for example only; thus, the chassis 100 may include one or a plurality of PCMCIA slots 122 depending upon the design. The PCMCIA device inserted into the PCMCIA slots 122 may be a wired local-area network adapter, a wireless local area network interface module or a digital data exchange adapter which are used primarily in the specific location of the chassis 100. The PCMCIA device may also perform any of the functions described above with respect to the I/O interface 110. The utilization of the PCMCIA standard bus structure and PCMCIA dimensional configurations with regard to interface 120, slots 122 and the respective devices inserted into the slots 122 is for convenience purposes only, and it is well understood by those of skill in the art that a similar standard may be substituted for the PCMCIA standard.

Furthermore, the chassis 100 may include an expansion bus interface 124 that bridges the first bus 102 to an expansion bus 126, which may be, for example, an AT standard bus. The expansion bus interface 124 converts data transmitted over the first bus 102 to the expansion bus 126, and converts data transmitted over the expansion bus 126 to the first bus 102. The chassis 100 may also include expansion slots 128 and an expansion bus connector 130 coupled to the expansion bus 126 to provide an interface to additional peripheral devices such as a network interface card, a CD-ROM, and other forms of communication and storage devices. The chassis 100 of FIG. 1 includes three expansion slots 128 for example only; thus, the chassis 100 may include one or a plurality of expansion slots 128 depending upon the design.

Moreover, the chassis 100 may include a power supply 132 that provides power to each of the user interface modules and to the cartridge 200 via power bus 134 and connector 136. The power supply 132 may include a voltage conversion circuit that converts AC line power to the appropriate DC voltage levels required by the modules. The power supply 132 may also include a battery that supplies the appropriate DC voltage levels to the modules when the voltage conversion circuit is inactive. The power bus 134 and common bus 300 may share a single connector pair, for example, connectors 232, 234 and/or the power bus 134 may be part of the common bus 300.

The cartridge 200 of FIG. 1 includes components having computer functions that can be shared among the various applications/work modes. Specifically, the cartridge 200 includes a core processor 210 coupled to memory 212 via a high-speed processor bus 214 and memory interface 216. The memory 212 may be system dynamic memory, cache memory, and/or non-volatile memory. The memory interface 216 performs functions

such as address decoding and bus control such that the core processor 210 can read data from and write data to the memory 212. The memory interface 216 may also perform functions such as dynamic memory refresh. A processor bus interface 218 bridges the processor bus 214 to a second bus 220, which corresponds to the common bus 300. The processor bus interface 218 converts data transmitted over the processor bus 214 to the second bus 220 and converts data transmitted over the second bus 220 to the processor bus 214.

The cartridge 200 may also include components having functions that can be shared among the various applications/work modes. Specifically, the cartridge 200 may include a PCMCIA interface 222 coupled to the second bus 220 for driving at least one PCMCIA device inserted into PCMCIA slots 224. The cartridge 200 of FIG. 1 includes five PCMCIA slots 224 for example only; thus, the cartridge 200 may include one or a plurality of PCMCIA slots 224 depending upon the design. The PCMCIA device may be a communication device, such as a wired local-area network adapter, a wireless local area network interface module, a digital data exchange adapter, a data storage device such as a hard disk, or a data processing device that processes I/O data. The data processing device may be, for example, a video interface adapter for processing video information or an analog to digital processing device for processing analog signals input to and/or output from the system, such as voice signals input to the system from a microphone and output from the system by a speaker. The PCMCIA slots 224 may be of different configurations (i.e., Type II and Type III). To provide the user with flexibility in choosing the location of specific PCMCIA devices, preferably each of the PCMCIA slots 224 have Type II configurations. Again, the utilization of the PCMCIA standard bus structure and PCMCIA dimensional configurations with regard to interface 222, slots 224 and the respective devices inserted into the slots 224 is for convenience purposes only, and it is well understood by those of skill in the art that a similar standard may be substituted for the PCMCIA standard.

The cartridge 200 may also include a power interface 132 that provides the appropriate DC voltage levels to each of the components of the cartridge 200. The power interface 226 may be coupled to the power bus 134 of the chassis 100 by mating connector 228 to connector 136. The power interface 226 may also include a battery 230 that supplies the appropriate DC voltage levels to the components of the cartridge 200 when the cartridge 200 is separated from the chassis 100. It is contemplated that the battery 230 may be packaged in a PCMCIA device configuration and housed in a dedicated PCMCIA slot 224, thus expending one of the PCMCIA slots 224.

The components of the cartridge 200 interface with the modules of the chassis 100 over the common bus 300. The common bus 300 is constructed by mating connector 232 of the chassis 100 with connector 234 of the cartridge 200, which connects the first bus 102 of the

chassis 100 to the second bus 220 of the cartridge 200. By detachably connecting the computer functions of the cartridge 200 to the user interface modules of the chassis 100, the cartridge 200 may be transferred from one environment to another. In each environment, the cartridge 200 may be connected to separate chassis' 100 which are optimized for use in their respective applications/work mode. Moreover, by sharing components between computer processing systems in separate environments, the cost of the computer processing system in each environment is substantially decreased.

The cartridge 200 of FIG. 1 may be designed such that the cartridge 200 can be configured by the user to have a first form and a second form. As shown in FIGS. 2 and 3, the cartridge 200 may include a first portion 400 connected to a second portion 500 by hinges 600 or other suitable connection devices. In this case, the electrical connections between the first portion and the second portion may be provided by a flexible cable 650. The two portions need not have identical dimensions as shown in FIG. 2.

FIG. 2 illustrates the first form of the cartridge 200 having, for example, a characteristic length, width and height of 7.5 inches, 6.0 inches and 0.5 inches, respectively, which is suitable for use in desktop, laptop, notebook and sub-notebook or other large pen or keyboard based computer processing systems. On the other hand, FIG. 3 illustrates the second form of the cartridge 200 having, for example, a characteristic length, width and height of 7.5 inches, 3.0 inches, 1.0 inches, respectively, which is suitable for a hand held device. As shown in FIG. 3, the second form has a thickness that is twice the thickness of the first form and a width that is half the width of the first form and narrow enough to be readily grasped with one hand. Because the cartridge 200 can take two forms: a first form that is wide yet thin and a second form that is narrower but thicker than the first form, the cartridge 200 can be more easily integrated both into larger computer processing systems which for ergonomic reasons have a constrained thickness and into hand-held systems which have a constrained width.

The cartridge 200 of FIG. 2 may also be configured to have a first form having, for example, a characteristic length, width and height of 7.5 inches, 6.0 inches and 0.5 inches, respectively, and a second form having, for example, a characteristic length, width and height of 3.75 inches, 6.0 inches, 1.0 inches, respectively. In this case, the second form has a thickness that is twice the thickness of the first form and a length that is half the length of the first form and narrow enough to be readily grasped with one hand.

FIG. 4 shows the cartridge 200 of the first form as depicted in FIG. 2 with PCMCIA cards inserted into slots 3, 4 and 5 plugged into a tablet style user interface chassis.

FIG. 5 shows the cartridge 200 of the second form as depicted in FIG. 3 with PCMCIA cards inserted into slots 3 and 4 plugged into a hand held PDA style user interface chassis.

FIGS. 6 and 7 illustrate the cartridge 200 that utilizes at least one pair of hinged connectors 660 (for example, two pairs are shown), instead of hinges and flexible cable, to join the first portion 400 to the second portion 500. FIG. 6 illustrates the first form of the cartridge 200, which is wide and slim and thus suitable for use in desktop, laptop, notebook, sub-note book or other large pen or keyboard based computer processing systems. FIG. 7 illustrates the second form of the cartridge 200, which is narrow and thick and thus suitable for a hand held device.

Moreover, the first portion 400 may include components having computer functions (i.e., core processor 210, memory 212, memory interface 216, and local bus interface 218), and the second portion 500 may include PCMCIA components (i.e., PCMCIA interface 222 and associated devices). Using the hinged connector pairs 660 allows the first portion 400 to be disconnected from the second portion 500. In this case, the first form of the cartridge 200 may include, for example, the first and second portions 400, 500 connected as shown in FIG. 6, which is suitable for use in desktop, laptop, notebook, sub-note book or other large pen or keyboard based computer processing systems. On the other hand, the second form of the cartridge 200 may include only the first portion 400, which may be suitable for a hand held device.

In another aspect, the computer system of the present invention as shown in FIGS. 8, 9(a) and 9(b) may include a chassis 700 that provides a cableless connection between at least two internal devices housed within the chassis 700 and external connectors of the chassis 700 that connect to external peripheral devices associated with each of the internal devices. For example, as depicted in FIGS. 8, 9(a) and 9(b), the internal devices may be a PCMCIA modem card 710, a PCMCIA wireless communication card 720 and a PCMCIA wired local area network adapter card 725. The external peripheral devices associated with each of the internal devices may be a phone line adapter 730, an antenna 740 and a local-area network connector 745, respectively. Normally, the internal devices are connected directly or indirectly via cables to their associated external peripheral devices. These cables are often annoying because they must be disconnected whenever the internal device is removed from the chassis, they must be associated with the correct internal device and external peripheral device, and they often exit the front or side of the chassis 700 in an inconvenient and unattractive manner. The computer system of the present invention eliminates the need for such annoying cables.

Specifically, the chassis 700 includes an internal connector 750 that connects to at least two internal devices. As shown in FIGS. 8, 9(a) and 9(b), the internal devices may be a PCMCIA modem card 710, a wireless PCMCIA communication card 720 or a wired PCMCIA local-area adapter card 725. The internal devices are separately associated with external peripheral devices. For example, as shown in FIGS. 8, 9(a) and 9(b), the

PCMCIA modem card 710 is associated with the phone line adapter 730, the wireless PCMCIA communication card 720 is associated with the antenna 740, and the wired PCMCIA local-area network adapter card is associated with the local-area network connector 745. A first portion 760 of the internal connector 750 is in electrical contact with a first external peripheral device, for example, the phone line adapter 730. A second portion 770 of the internal connector is in electrical contact with a second external peripheral device, for example, the antenna 740. A unique adapter 780 is coupled between each internal device and the internal connector 750. The adapter 780 has either a first portion 790 that connects the internal device to the first portion 760 of the internal connector 750 or a second portion 800 that connects the internal device to the second portion 770 of the internal connector 750 in order to couple the internal device to its associated external peripheral device.

As described above, the adapters 780 and the internal connector 750 provide a cableless connection between two internal devices and their associated external peripheral devices. However, the present invention is not limited in this respect and may be used connection three or more internal devices and their associated external peripheral devices. For example, as shown in FIGS. 8 and 9(a), the internal connector 750 may include a third portion 810 in electrical contact with a third external peripheral device, for example, the local area network adapter 745. The adapter 780 then has either a first portion 790 that connects the internal device to the first portion 760 of the internal connector 750 or a second portion 800 that connects the internal device to the second portion 770 of the internal connector 750 or a third portion 820 that connects the internal device to the third portion 810 of the internal connector 750 such that the internal device is coupled to its associated external peripheral device.

The benefits of using the adapters 780 in conjunction with the internal connector 750 of the chassis 700 are two-fold. First, as long as the appropriate adapter 780 is affixed to the respective internal device, the user is not required to match the internal device to its associated external peripheral device because the connection between the two is automatic. And second, the internal device may be disconnected from the chassis 700 without disturbing the associated external peripheral device, thus providing a user-friendly system. Typically, the adapters 780 remain affixed to their respective internal device ready for insertion into another chassis 700.

Although the invention has been shown and described with respect to the particular embodiments thereof, it should be understood by those skilled in the art that the foregoing and various other changes, omissions, and additions in the form and detail thereof may be made without departing from the spirit and scope of the invention.

Claims

1. A computer system comprising:
a first chassis having at least one user interface module coupled to a first bus;
a second chassis, different than said first chassis, having at least one user interface module coupled to a second bus; and
a cartridge having a core processor and memory, coupled to a third bus;
wherein said third bus of said cartridge is detachably connected to said first bus of said first chassis to form a first functional system, and said third bus of said cartridge is detachably connected to said second bus of said second chassis to form a second functional system.
2. The computer system of claim 1, wherein said at least one user interface module of said first chassis is optimized for use in a first mode, and said at least one user interface module of said second chassis is optimized for use in a second mode different than said first mode.
3. The computer system of claim 1, wherein said first, second and third buses each comprise a plurality of buses.
4. The computer system of claim 3, wherein said plurality of buses of said first bus connects to said plurality of buses of said third bus through a first common connector, and said plurality of buses of said second bus connects to said plurality of buses of said third bus through a second common connector.
5. The computer system of claim 3, wherein said plurality of buses of said first bus connects to said plurality of buses of said third bus through separate first connectors, and said plurality of buses of said second bus connects to said plurality of buses of said third bus through separate second connectors.
6. The computer system of claim 1, wherein said cartridge can be configured by a user of said computer system to have a first form and a second form.
7. The computer system of claim 6, wherein said cartridge comprises a first portion connected to a second portion by at least one hinge and a cable.
8. The computer system of claim 6, wherein said cartridge comprises a first portion connected to a second portion by at least one hinged connector.
9. The computer system of claim 6, wherein said cartridge of said first form comprises a first portion connected to a second portion by a first connector, and said cartridge of said second form comprises said

- first portion connected to said second portion by a second connector different than said first connector.
10. The computer system of claim 6, wherein said first form has a predetermined width, length, and thickness, and said second form has a width approximately half the width of said first form and a thickness approximately twice the thickness of said first form. 5
 11. The computer system of claim 10, wherein said width of said second form is narrow enough to be readily grasped with one hand. 10
 12. The computer system of claim 6, wherein said first form has a predetermined width, length, and thickness, and said second form has a length approximately half the length of said first form and a thickness approximately twice the thickness of said first form. 15
 13. The computer system of claim 12, wherein said length of said second form is short enough to be readily grasped with one hand. 20
 14. The computer system of claim 1, wherein said cartridge comprises at least one slot for housing a module that is coupled to said second bus. 25
 15. The computer system of claim 14, wherein said module is an wireless communication module, a modem, a wired local area network adapter, a digital communication module, an analog communication module, a data storage device, or a data processing device. 30
 16. The computer system of claim 20, wherein said data storage device is a hard disk drive. 35
 17. The computer system of claim 14, wherein said module is a data processing device. 40
 18. The computer system of claim 22, wherein said data processing device is a video interface adapter. 45
 19. The computer system of claim 22, wherein said data processing device processes analog signals input to and/or output from the computer system. 50
 20. The computer system of claim 24, wherein said analog signals are voice signals. 55
 21. The computer system of claim 14, wherein said slot is a PCMCIA standard slot.
 22. The computer system of claim 14, wherein one of said first chassis and said second chassis has an internal connector having a first portion in electrical contact with a first external peripheral device, a second portion in electrical contact with said second external peripheral device and a third portion in electrical contact with a third external peripheral device, said module being associated with one of said first, second and third external peripheral devices; and said computer system further comprises an adapter for coupling said module to said internal connector, said adapter having one of a first portion that connects to said first portion of said internal connector, a second portion that connects to said second portion of said internal connector, and a third portion that connects to said third portion of said internal connector.
 23. The computer system of claim 14, wherein one of said first chassis and said second chassis has an internal connector having a first portion in electrical contact with a first external peripheral device and a second portion in electrical contact with a second external peripheral device, said module being associated with one of said first external peripheral device and said second external peripheral device; and said computer system further comprises an adapter for coupling said module to said internal connector, said adapter having one of a first portion that connects to said first portion of said internal connector and a second portion that connects to said second portion of said internal connector.
 24. The computer system of claim 28, wherein said module is a PCMCIA device.
 25. The computer system of claim 28, wherein said module is a modem and said one of said first and second external peripheral devices is a telephone line.
 26. The computer system of claim 28, wherein said module is a wired local area network adapter and said one of said first and second external peripheral devices is a wired local-area network communication link.
 27. The computer system of claim 28, wherein said module is a wireless communication module and said one of said first and second peripheral devices comprises an antenna.
 28. The computer system of claim 28, wherein said module is a data communication module and said one of said first and second peripheral devices is a data communication link.
 29. The computer system of claim 28, wherein said module is a video interface adapter and said one of said first and second peripheral devices is video link.

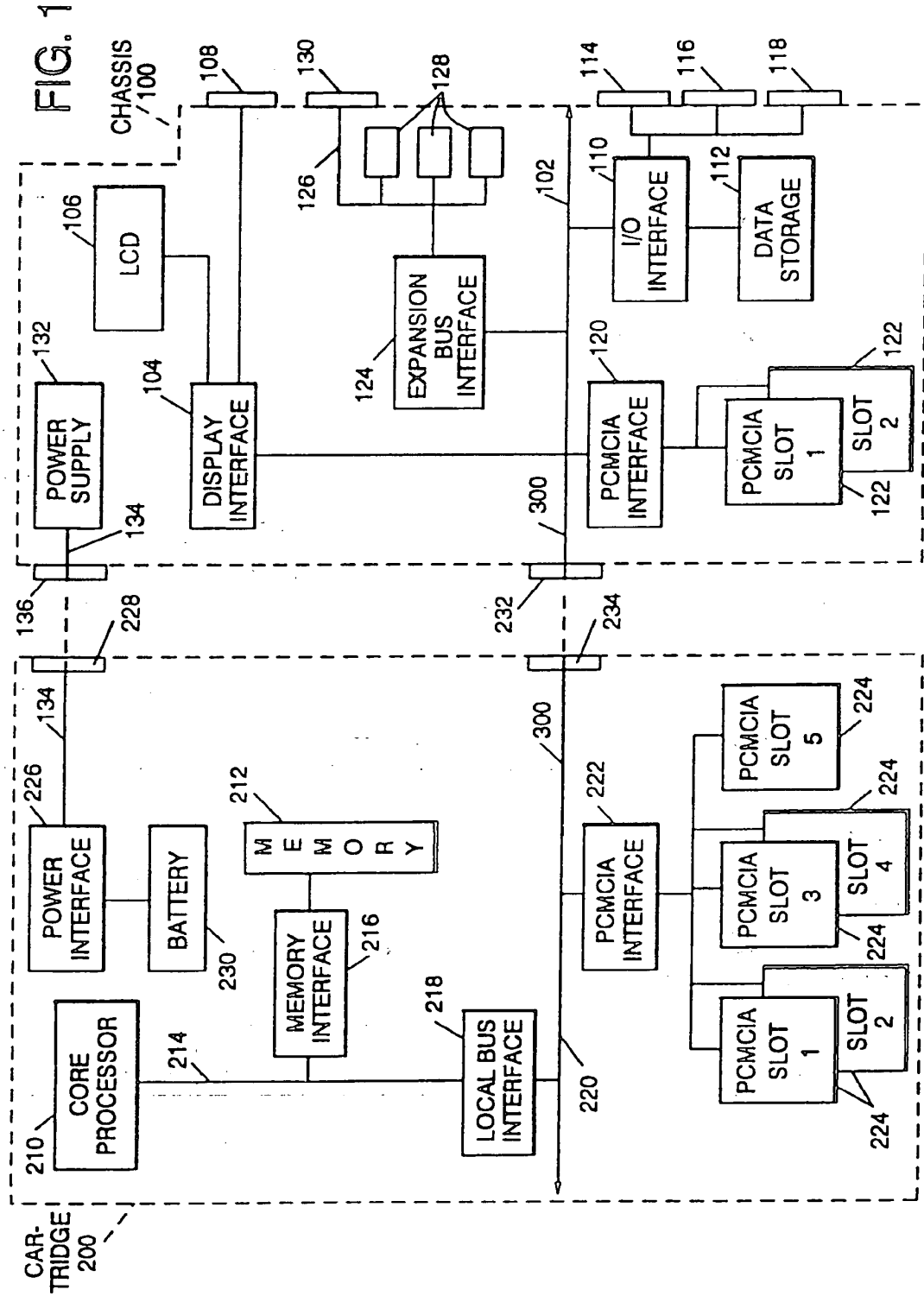


FIG. 2

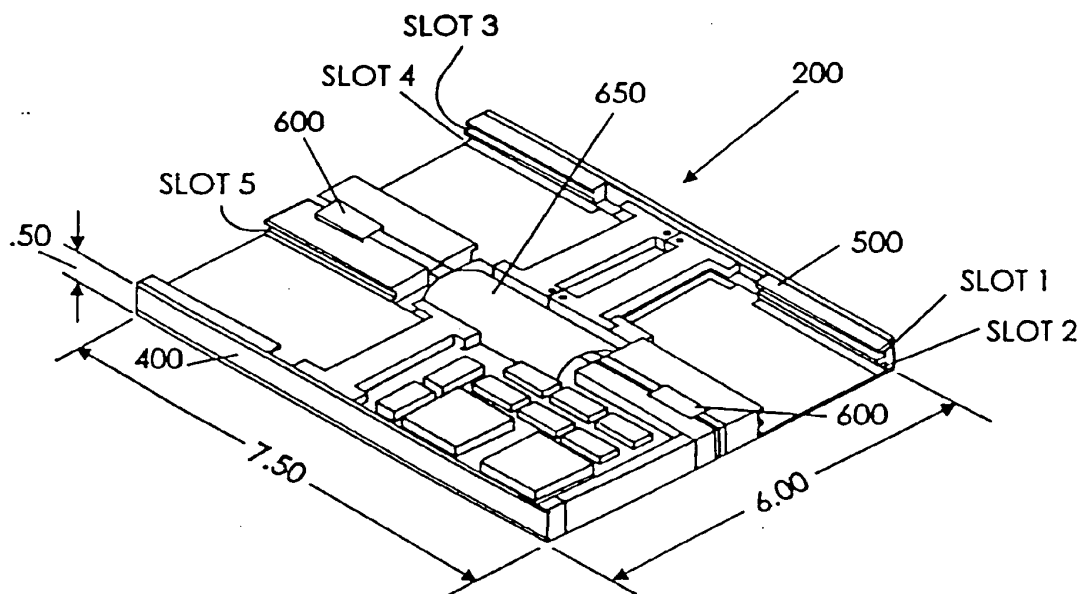


FIG. 3

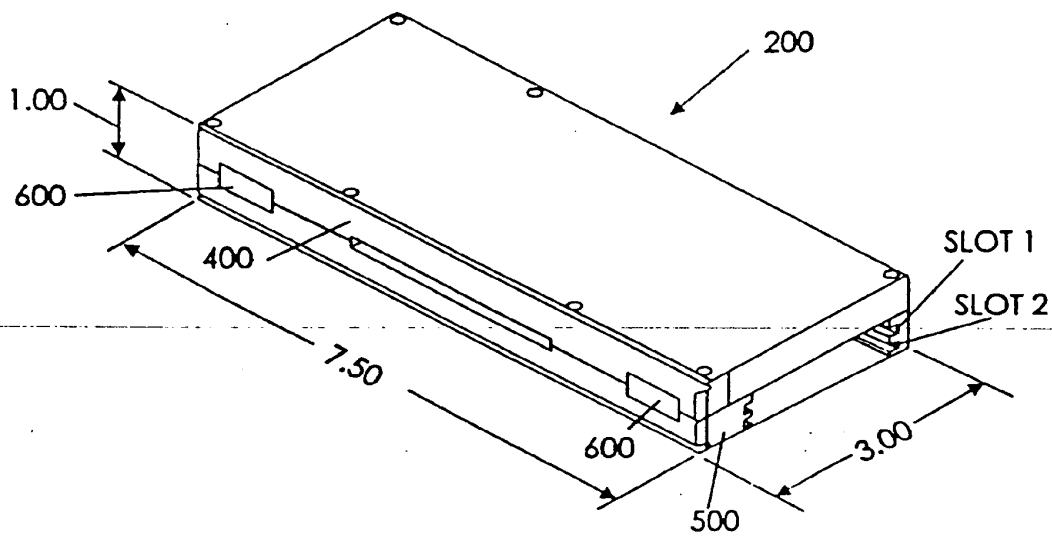


FIG. 4

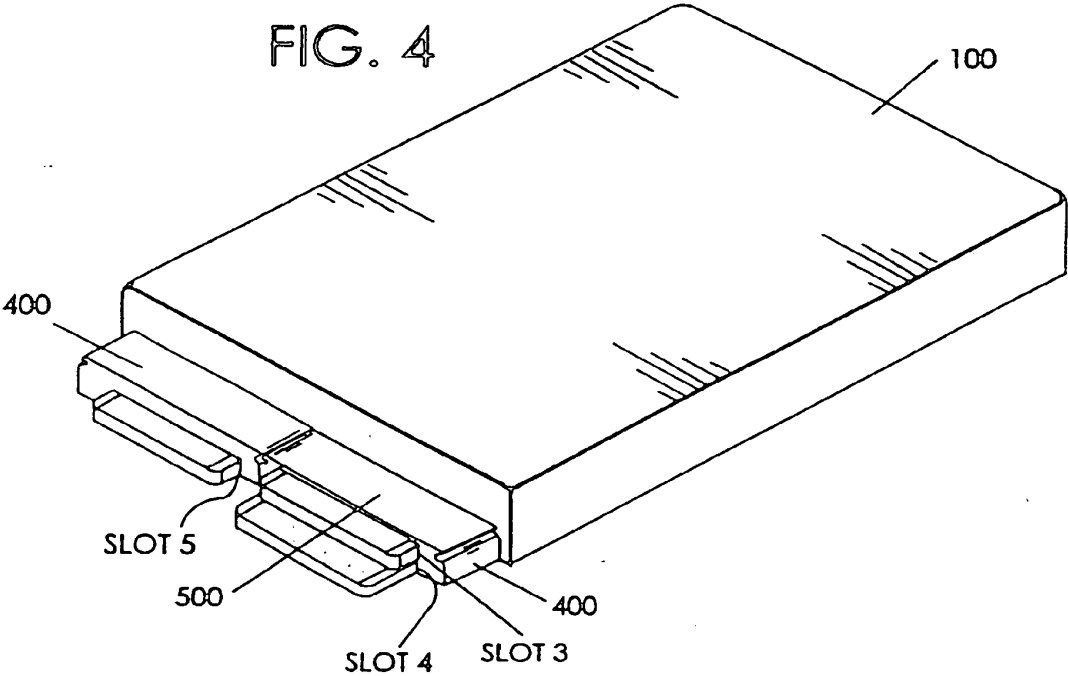


FIG. 5

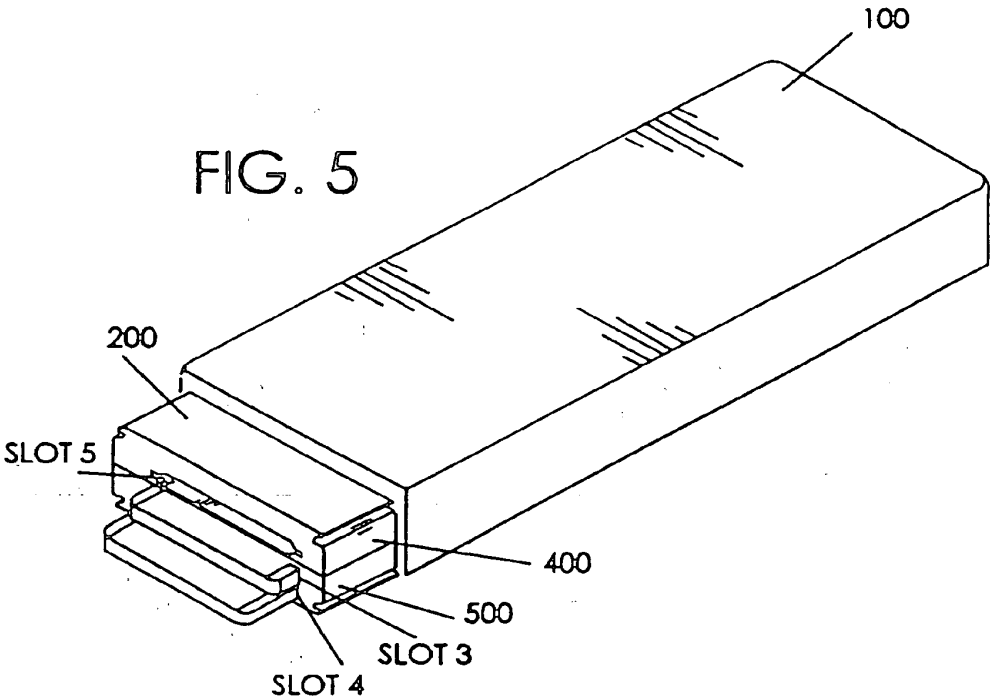
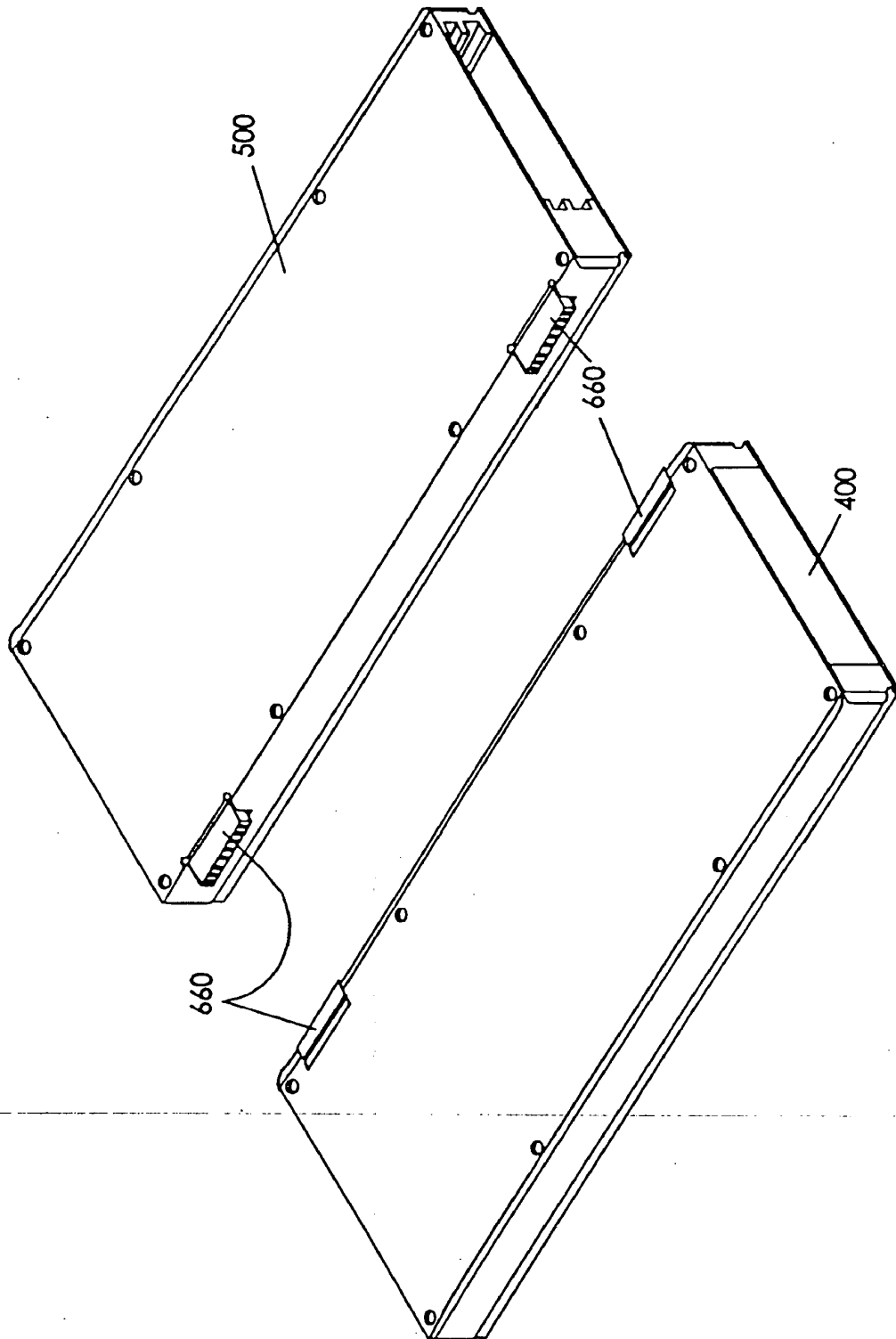


FIG. 6



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G06F	1/16 1/20 1/06	7165-5B 7165-5B	G06F 1/00	312 K 360 D

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Continued on the last page

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(54) (TITLE OF THE INVENTION)

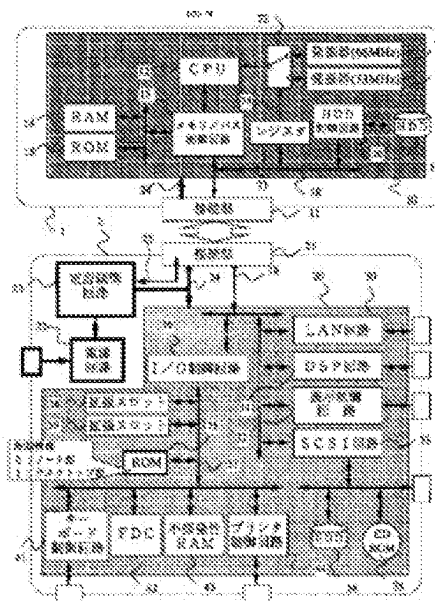
**Detachable Information Processing
Device**

(57) Abstract

(OBJECT) To provide means for expanding the range of use of PPMs, appertaining to detachable data processing devices structured from PPMs and DSs.

(CONSTITUTION) A ROM for storing information indicating a DS cooling capability is provided, and also a selecting circuit for selecting a plurality of oscillator circuits and CPU operating frequencies is provided in a PPM. Given this, information is read out from the ROM at the time of system startup, to identify the cooling capability of the DS, and a CPU operating frequency that produces a quantity of heat for which the operation of the PPM can be assured is set.

(EFFECTS) While it is not possible to use the maximum performance of the PPM, this enables the use of a DS with a multifunctional cooling capability, increasing the combined utility.



13: Memory/Bus Control Circuit

70: Oscillator (66 MHz)

71: Oscillator (33 MHz)

73: Register

18: HDD Control Circuit

11: Connecting Portion

21: Connecting Portion

23: Power Supply Control Circuit

22: Power Supply Circuit

38: Expansion Slot

39: Expansion Slot

[LEFT OF ROM] Cooling
Information:

0: Notebook-Type

1: Desktop-Type

41: Keyboard Control Circuit

36: I/O Control Circuit

43: Non-Volatile RAM

44: Printer Control Circuit

30: LAN Circuit

31: DSP Circuit

32: Display Control Circuit

33: SCSI Circuit

(SCOPE OF PATENT CLAIMS)

(CLAIM 1) A detachable data processing device comprising:
a personal processor module (hereinafter termed a "PPM"),
structured from: a CPU; a memory; a local bus to which
various types of devices are connected;

a memory/bus controlling circuit enabling the transmission
and reception of data between the CPU, the memory, and
the devices on the local bus; and a connecting portion
capable of exchanging information with an external
information device using the local bus; and

a docking station (hereinafter abbreviated "DS")
comprising: a local bus connecting portion capable of
connecting to the PPM; any given number of devices on the
local bus; and a power supply circuit for supplying power;
wherein:

the CPU is able to access a device on the local bus of the
DS when the PPM and the DS are in a connected state;

comprising:

means for generating a plurality of clocks at different
frequencies;

a selecting circuit for providing to the CPU a clock
selected from the plurality of clocks;

a register, on the CPU local bus, for storing clock selection
information; and

means for storing DS cooling capability information,
accessible through the DS local bus; wherein

a program is provided in the memory so as to set the
register with specific selection information, each time the
power supply is turned ON, in accordance with the cooling
capability that is stored within the DS, so as to control the
amount of heat produced by the PPM in accordance with the
DS cooling capability.

(DETAILED DESCRIPTION OF THE INVENTION)

(0001)

(AREA OF USE IN INDUSTRY) The present invention relates
to a detachable information processing device wherein a
specific component can be detached and is portable, in the
field of information processing devices such as
workstations and personal computers, and pertains to
means for expanding the scope of applicability so as to
enable the use of components in a large variety of
combinations.

(0002)

(PRIOR ART) At present, there is a diversification of the
forms of use of personal computers as personal computers
are becoming ubiquitous. One of these is a trend wherein a
single individual uses a plurality of personal computers. As
a specific example, one may consider a businessman who
uses three machines: a desktop personal computer used at
the office, a notebook personal computer carried on
business trips, and an inexpensive personal computer used
at home.

(0003) A detachable personal computer has appeared on the
market in response to such needs. The thought process is
one of being able to detach for use, from the desktop
computer used in the office, only those elements that must
be carried away. The basic structure is that of a notebook
personal computer and a docking station (hereinafter
termed a "DS"), where, when the notebook personal
computer is connected, it can be used as a desktop personal
computer. There is the "Electronic Information Device and
Docking Station," disclosed in Japanese Unexamined

Patent Application Publication H4-263304, as this type of
prior art.

(0004)

(PROBLEM SOLVED BY THE PRESENT INVENTION) In the prior
art set forth above, the target is for the notebook personal
computer to be portable; however, in the present invention
the object is to improve the portability, and a system is
envisioned wherein a single component comprising the
CPU, the memory, and the hard disk device from the
desktop PC can be detached from the main unit. Here the
component set forth above is defined as a personal
processor module (hereinafter abbreviated "PPM") and the
main unit other than the PPM is defined as the docking
station (hereinafter abbreviated "DS"). The PPM and the
DS can be envisioned as having the same relationship as a
cassette tape and the video deck in a video system. While
the PPM and the DS do not function at all individually,
when the PPM and the DS are connected, they function as a
usable personal computer.

(0005) In this type of detachable information processing
device, the PPMs can be considered to be of a variety of
different types of products with different processing
capabilities, memory capacities, and the like, and the DSs
can be considered to be a variety of different types of
products depending on the state of use, such as a notebook-
type, a desktop-type, or the like. In particular, the amount
of heat that is generated by a PPM that can be used in a
notebook-type DS, which is a packaging structure that has a
small case and lacks a fan, and the like, and thus has little
cooling capability, is limited. Because of this, even if a
high-performance PPM with a large power consumption
were physically attached to a DS, in practice it could not be
used. In practice, while the power consumption of a
notebook PC is about 10 W, a 100 MIPS-class CPU alone
is more than 10 W. In this way, the control of heat
production is an issue, and reduces the combined utility of
the PPM and the DS. Consequently, the problem to be
solved by the present invention is to increase the combined
utility, taking into consideration the amount of heat
produced and the cooling capability.

(0006)

(MEANS FOR SOLVING THE PROBLEM) In order to solve the
problem set forth above, a ROM for storing information
indicating a DS cooling capability is provided, and also a
selecting circuit for selecting a plurality of oscillator
circuits and CPU operating frequencies is provided in a
PPM.

(0007)

(OPERATION) At the time of system startup, information is
read out from the ROM to identify the cooling capability of
the DS. In response, a CPU operating frequency that
produces an amount of heat for which the operation of the
PPM is assured is selected. An oscillator corresponding to
this frequency is selected by the selecting circuit. Given the
above, while it is not possible to use the maximum
performance of the PPM, this enables the use of a DS with
a multifunctional cooling capability, increasing the
combined utility.

(0008)

(EXAMPLES OF EMBODIMENT) An example of embodiment
of the present invention will be described below. FIG. 1
and FIG. 2 will be used first to explain a product image of a

detachable information processing device that is structured from a PPM and a DS. FIG. 1 is an external view when the PPM has been removed, and FIG. 2 is an external view when the PPM is attached to the DS. In these figures, identical components are assigned identical codes. In the figures, 1 is a PPM, 2 is a DS, 3 is a PPM insertion slot in the DS 2, 4 is a display device, and 5 is a keyboard. When the detachable information processing device is used, the PPM 1 is inserted into the DS 2, as illustrated in FIG. 2. On the other hand, when the PPM is transported, the DS 2 is removed, as illustrated in FIG. 1. The user need only transport the detached PPM 1. For example, when used at both the workplace and at home, only a single PPM 1 and docking stations need be purchased. When compared to a notebook information processing device, the display device 4 and the keyboard 5 are not included in the PPM 1, and thus the device is small and lightweight, and superior in terms of portability. The internal structure of the PPM 1 and of the DS 2 will be explained next.

(0009) Fig. 3 is a block diagram of a detachable information processing device. In this figure, identical codes are assigned to the circuit blocks that have the same functions as in FIG. 1. The PPM 1 is structured from a system circuit 10 of the electronic circuit portion, and a connecting portion 11 that bridges to the DS 2. In the system circuit 10, 12 is a CPU, 13 is a memory/bus controlling circuit, 14 is a random access memory (hereinafter abbreviated "RAM"), 15 is a read only memory (hereinafter abbreviated "ROM"), 19 is a non-volatile RAM from which the data that has been written is not lost even if the power supply is turned off, 16 is a hard disk drive (hereinafter abbreviated "HDD") controlling circuit, 17 is an HDD, and 18 is a local bus. 24 is a power supply line to the system circuit 10. The DS 2 is structured from an electronic circuit portion system circuit 20, a connecting portion 21 that bridges to the PPM 1, and a power supply control circuit 23 that converts from AC (alternating current) to DC (direct current) and that controls the power supply to a power supply circuit 22, the system circuit 20, and the like. The power supply control circuit 23 not only supplies power to the system circuit 10 through the connecting portions 21 and 11, but also detects whether or not the PPM 1 is connected, through a connection information signal line 25. Additionally, the system circuits 10 and 20 can send and receive various types of data through the local bus 18 that is connected by the connecting portions 11 and 21. In this way, the PPM 1 and the DS 2 are attachable/detachable with the connecting portions 11 and 21 as the contact points.

(0010) The detailed structure of the system circuit 20 within the DS 2 will be explained here. As devices that are connected through the local bus 18, 30 is a LAN circuit connecting to a network, 31 is a DSP circuit for performing digital processing of signals such as audio and video signals, 32 is a display control circuit 32 for displaying necessary information on a display device 4, 33 is a SCSI control circuit for controlling the movement of data to/from a file device, or the like, 34 and 35 are an HDD and a CD-ROM that are controlled by the SCSI circuit 33, and 36 is an I/O control circuit for bridging between the local bus 18 and an I/O bus 37. As devices that are connected to the I/O bus 37, 37 through 38 are expansion slots into which

various types of I/O cards may be installed, 41 is a keyboard control circuit for controlling the keyboard 5, 42 is an FDC for controlling a floppy disk, 43 is a non-volatile RAM for storing various types of system information, and 44 is a printer control circuit for controlling a printer. All of these devices within the system circuit 20 are accessed by the CPU 12 within the PPM 1 in the state wherein the connecting portions 11 and 22 are connected. The overall operation of the system in this case will be explained below.

(0011) When the power supply circuit 22 begins to supply power, the power supply control circuit 23 detects, through the connection information signal line 25, whether or not the PPM 1 is connected. If connected, then the supply of power through the power supply line 24 to the DS 2 system circuit 20 and to the PPM 1 system circuit 10 commences. The CPU 12 that receives this supply of power begins its operations. First a program that is stored within the ROM 15 is executed. This program not only sets up the information that is required for the initialization of the various devices within the system circuit 10 and the system circuit 20, but also confirms the operations thereof. If there are no problems in any of the devices, then the CPU 12 issues a read command to the HDD control circuit 16 to download, into the RAM 14, a system program that is stored on the HDD 17. Once the download has been completed, then the CPU 12 executes this system program. The system program is typically known as the "operating system" (hereinafter abbreviated as "OS"), and as specific products, there are MS-DOS and UNIX. While the fundamental OS operations are identical, there are differences in the operating environment depending on the types of I/O that are used. In order to absorb the differences in the operating environments, programs known as "device drivers" that are compatible with the various I/Os are downloaded from the HDD 17 into the RAM 14. Once the device drivers have been set up and the startup of the OS has been completed, then the user runs various types of application software as necessary. For example, when one considers a word processor as the application software, the operation thereof may be summarized as follows. If the program is stored in the HDD 17, then the OS issues, to the device driver of the HDD control circuit 16, an instruction to readout the applicable program. This causes the device driver to send a command to the HDD control circuit 16, to thereby transfer the program from the HDD 17 to the RAM 14. Once the transfer has been completed, the program is executed to launch the word processor. After the startup, an instruction is issued to the device driver of the SCSI circuit 33 in order to readout a document file that is stored on the HDD 34 or on the CD-ROM 35, to thereby transfer the document file data from the HDD 34 or the CD-ROM 35 to the RAM 14. In order to display this data, the device driver of a display control circuit 32 is used to transfer the necessary data from the RAM 14 to the display control circuit 32. The display control circuit 32 converts this data into visual data that can be displayed, and sends the data to the display device 4. In order to edit the document that is displayed, edit data that has been inputted through the keyboard 5 is received by the keyboard control circuit 41, and the device driver thereof is used to transfer this data into the RAM 14. The document file that is already stored

in the RAM 14 is edited in accordance with this edit data, and the data after editing is again sent to the display control circuit 32, to display, on the display device 4, the document after editing. The device drivers corresponding to the various types of I/O are used in this way to perform a variety of tasks. When transferring document files to other information devices that are connected via a network, the device driver of the LAN circuit 30 is used; the device driver of the DSP circuit 31 is used for audio output of the document data; the device driver of the SCSI circuit 33 is used for storing the document file to the HDD 34; the device driver of the print control circuit 44 is used for printing the document; and the device driver of the FDC 42 is used for storing the document to a floppy disk.

(0012) As described above, in the detachable information processing device according to the present invention, the PPM 1 can be attached to the DS 2 to structure a single complete system. This type of detachable information processing device that is structured from a PPM and a DS must be compatible with a broad range of applications, from a high-performance desktop-type to a small and lightweight notebook-type. In particular, when a PPM that uses a high-performance CPU is used in a notebook-type DS, the cooling means for the PPM, which produces a great deal of heat, becomes a problem. Here it is possible to give up the use of the PPM at full power, to use the PPM with performance matching the cooling capability of the notebook-type DS. A specific example of embodiment of this is described below.

(0013) FIG. 4 is a block diagram of a detachable information processing device wherein the performance of the PPM can be adjusted in accordance with the cooling capability of the DS. In this figure, identical codes are assigned to identical signal lines and to circuit blocks that have the same functions as in FIG. 3. In the figure, 70 is an oscillator for producing a 66 MHz clock signal, 71 is an oscillator for producing a 33 MHz clock signal, 72 is a selecting circuit for the aforementioned clock signals, 73 is a register wherein the CPU 12 can set one bit, 74 is a selection signal line wherein the signal level is determined in accordance with the data in the register 73, and 75 is a ROM for storing the cooling information for the DS 2. The cooling information that is stored in the ROM 75 indicates that the DS 2 is a notebook type when this information is 0, and indicates that the DS 2 is a desktop-type when this information is 1. The CPU 12 is able to read in this information to identify whether the connected DS 2 is a desktop-type or a notebook-type. Additionally, the CPU 12 is able to select an operating frequency of either 66 MHz or 33 MHz by writing information to the register 73. Specifically, the selecting circuit 72 selects the oscillator 70 when the signal level of the selection signal line 74 is "H", or selects the oscillator 71 when the signal is "L". Consequently, when the CPU 12 writes a "1", the selection signal line 74 outputs a "H" level on the selection signal line 74, causing the 66 MHz clock signal of the oscillator 70 to be the clock for the CPU 12. Conversely, when the CPU 12 writes a "0", the selection signal line 74 outputs a "L" level on the selection signal line 74, causing the 33 MHz clock signal of the oscillator 71 to be the clock for the CPU 12. The amount of heat produced by the PPM 1 wherein the CPU 12 is operating at 33 MHz can be kept to

a level that is not a problem for the cooling capability of the notebook-type DS. On the other hand, when it comes to the amount of heat that is produced by the PPM 1 when operating at 66 MHz, the cooling capability of the notebook-type DS is inadequate, but this amount of heat is not a problem for a desktop-type DS. These functions are transparent to the user, but instead the operating speed is selected by a program that is stored in the ROM 15. A flow chart of this program is described below.

(0014) FIG. 5 is a flow chart for setting the operating frequency of the CPU 12. This will be explained below. After the power supply is turned on, the CPU 12 reads out the cooling information from the ROM 75. If the cooling information is "1", then a "1" is written to the register 73, to thereby select the 66 MHz clock. Conversely, if the cooling information is "0", then a "0" is written to the register 73, to thereby select the 33 MHz clock. After the operating frequency of the CPU 12 has been set, then the configuration is detected, and the system is started up. Thereafter, the application software is launched to perform the desired tasks.

(0015) (EFFECTS OF THE INVENTION) As described above, a high-performance PPM purchased by the user can be used even in a notebook-type by reducing the operating speed thereof, expanding its scope of application. In particular, because, in the present example of embodiment, the system determines the operating speed automatically, the user need not be aware of the relationship between the operating speed and the cooling capability. This also prevents incidents that could be caused by user error in the settings. The combined utility of the PPM and the DS can be improved thereby.

(BRIEF DESCRIPTION OF THE DRAWINGS)

FIG. 1 is an external view of a detachable information processing device as set forth in an example of embodiment according to the present invention.

FIG. 2 is an external view of the same detachable information processing device.

FIG. 3 is a block diagram of the same detachable information processing device.

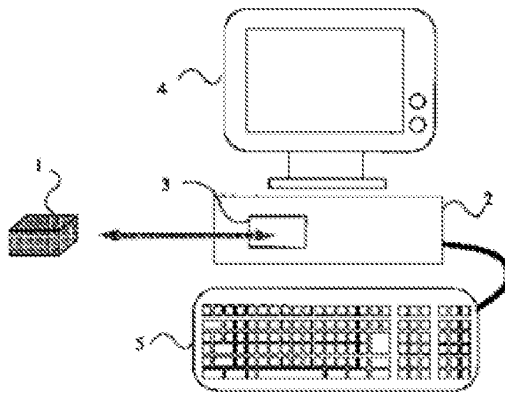
Fig. 4 is a block diagram illustrating an example of embodiment according to the present invention.

FIG. 5 is a flowchart for the same.

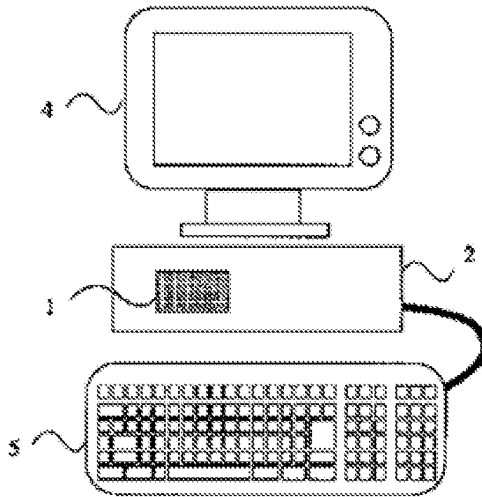
(Explanation of Codes)

- 1: PPM
- 2: DS
- 10: System Circuit
- 20: System Circuit
- 18: Local Bus
- 11: Connecting Portion
- 21: Connecting Portion
- 70: Oscillating Device
- 71: Oscillating Device
- 72: Selecting Circuit
- 73: Register
- 75: ROM
- 36: I/O Controlling Circuit

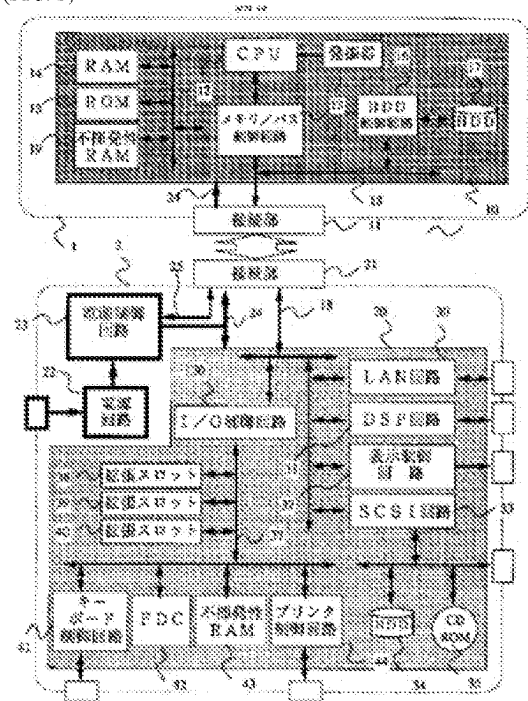
(FIG. 1)



(FIG. 2)

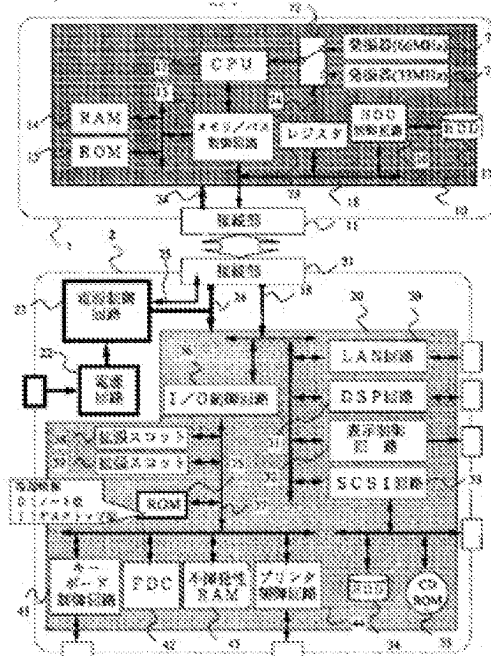


(FIG. 3)



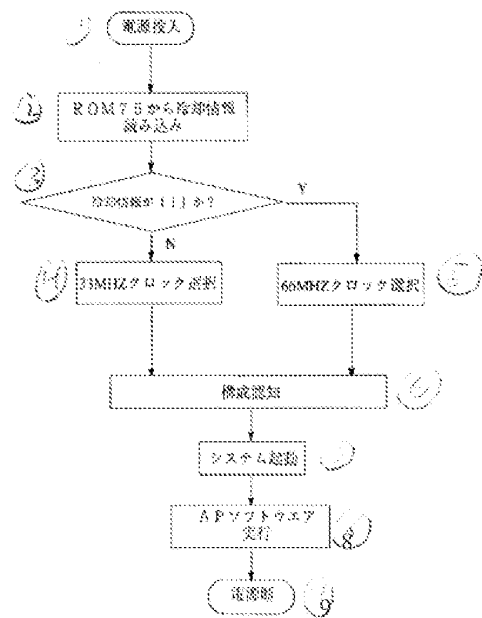
- 13: Memory/Bus Control Circuit
- [NEXT TO 16] Oscillator
- 16: HDD Control Circuit
- 11: Connecting Portion
- 21: Connecting Portion
- 23: Power Supply Control Circuit
- 22: Power Supply Circuit
- 38: Expansion Slot
- 39: Expansion Slot
- 40: Expansion Slot
- 41: Keyboard Control Circuit
- 36: I/O Control Circuit
- 43: Non-Volatile RAM
- 44: Printer Control Circuit
- 30: LAN Circuit
- 31: DSP Circuit
- 32: Display Control Circuit
- 33: SCSI Circuit

(FIG. 4)



- 13: Memory/Bus Control Circuit
- 70: Oscillator (66 MHz)
- 71: Oscillator (33 MHz)
- 73: Register
- 18: HDD Control Circuit
- 11: Connecting Portion
- 21: Connecting Portion
- 23: Power Supply Control Circuit
- 22: Power Supply Circuit
- 38: Expansion Slot
- 39: Expansion Slot
- [LEFT OF ROM] Cooling Information:
0: Notebook-Type
1: Desktop-Type
- 41: Keyboard Control Circuit
- 36: I/O Control Circuit
- 43: Non-Volatile RAM
- 44: Printer Control Circuit
- 30: LAN Circuit
- 31: DSP Circuit
- 32: Display Control Circuit
- 33: SCSI Circuit

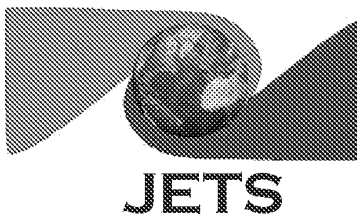
(FIG. 5)



- [1] Power Supply On
- [2] Read in the cooling information from the ROM 75.
- [3] Is the cooling information "1"?
- [4] Select the 33 MHz clock.
- [5] Select the 66 MHz clock.
- [6] Configuration identification.
- [7] System startup.
- [8] Execute AP software.
- [9] Power Supply Off

Continued from FrontPage

(51) Int. Cl. ⁵	Identification codes	JPO file numbers	FI	Technical indications
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January 8, 2010

I, Dr. Warren Smith, Principal Translator at JETS: Japanese-English Technology Services of Durham, New Hampshire, hereby attest that I am familiar with the Japanese language, and have personally translated, from Japanese to English, and delivered via email to Emily Doan of Covington & Burling LLP this day the following Japanese Unexamined Patent Application Publication:

JP6-289953 Pub. Oct. 18, 1994 / Hitachi

I further attest that all reasonable care and effort has been used to ensure that the translation provided is true, complete, accurate, fair and impartial.

I declare under penalty of perjury under the laws of the United States of America that the foregoing is true and correct.

Executed this 8th day of January 2010 in Durham, New Hampshire.

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WO9218924

Publication Title:

A COMPUTER COMPRISING AT LEAST TWO EASILY INTERCONNECTABLE PARTS

Abstract:

Abstract of WO9218924

The invention refers to a computer incorporating components necessary for data processing, such as e.g. main board with CPU, primary and secondary memory and electronics for driving peripheral equipment such as monitor, keyboard, printer, etcetera, and which computer is composed by at least two easily interconnectable parts. The invention is realized in that the computer consists on one hand of a docking station intended mainly for stationary installation and on the other hand a detachable and easily moveable module, and that the docking station at least incorporates or is connected to a power supply, electronic components for driving the peripheral equipment such as monitor, keyboard, printer and that the module incorporates at least the CPU, a primary and secondary memory, and that the module is arranged to be moveable between and to be dockable in, or connectable to different docking stations, and that the module and the docking station, when joined together form an integral unit.

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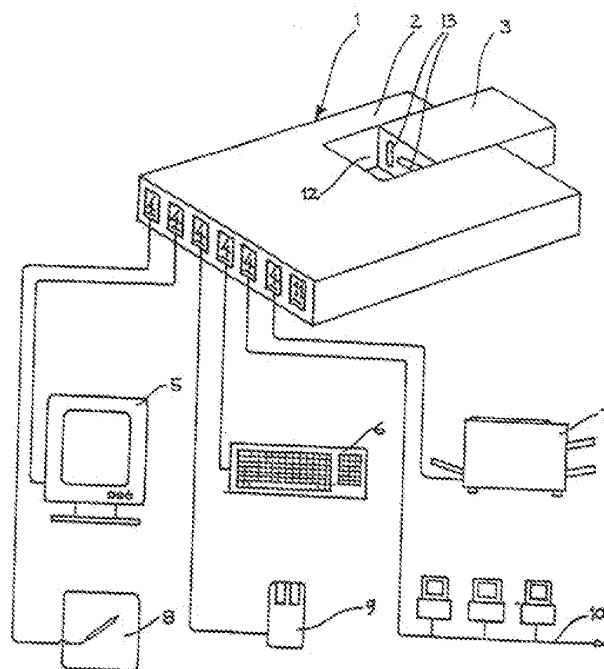
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(54) Title: A COMPUTER COMPRISING AT LEAST TWO EASILY INTERCONNECTABLE PARTS

(57) Abstract

The invention refers to a computer incorporating components necessary for data processing, such as e.g. main board with CPU, primary and secondary memory and electronics for driving peripheral equipment such as monitor, keyboard, printer, etcetera, and which computer is composed by at least two easily interconnectable parts. The invention is realized in that the computer consists on one hand of a docking station intended mainly for stationary installation and on the other hand a detachable and easily moveable module, and that the docking station at least incorporates or is connected to a power supply, electronic components for driving the peripheral equipment such as monitor, keyboard, printer and that the module incorporates at least the CPU, a primary and secondary memory, and that the module is arranged to be moveable between and to be dockable in, or connectable to different docking stations, and that the module and the docking station, when joined together form an integral unit.



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A COMPUTER COMPRISING AT LEAST TWO EASILY INTERCONNEC- TABLE PARTS

Introduction

5

The invention refers to a computer incorporating components necessary for data processing, such as e.g. main board with CPU, primary and secondary memory and electronic components for driving peripheral equipment such as monitor unit, keyboard, printer, etcetera, and which computer consists of at least two easily
10 interconnectable parts.

Background of the invention

15 The computers available on the market today are normally rather expensive and bulky. The complete units are furthermore rather heavy. Most computers are of stationary type i.e. they are not intended to be easily portable between different work sites, and they therefore are neither easy to move, to install or to start up. Installation of a computer requires a certain knowledge and also carefulness in
20 order to avoid damages to the sensitive parts of the system. Beside the physical placement and positioning of the computer box and the monitor installation normally involves that a number of connections must be made e.g. connection of the computer to a possible network, interconnection of keyboard and computer, connection of monitor, printer, mouse, connection of mains voltage, etcetera.

25

It is often desirable to be able to carry along all programmes and all "private" data from one work site to another in a simple manner. This requirement can come up e.g. when visiting a client's office, during travel, in a car, a boat, etcetera. The user thereby has access to, and can easily work, with the same software and data at
30 several different work sites. It is then necessary to have a working tool which is easy to carry along and easy to start up in order to allow the user swiftly to start his work, without the need for making a timewasting installation of the computer at the new location. It is thus of critical importance that the starting up time can be reduced.

35

Prior art

For the purpose of facilitating the transfer of data from one computer to another it has earlier been developed movable secondary memories (hard discs). These systems require that a complete computer equipment is available at each work site, except for the hard disc itself, which is brought along. This means that the computer with its central processor unit (CPU), memory (RAM), mathematic processor unit (MPU) and other internal equipment such as drive electronics for the peripheral equipment, etcetera, must be available at every work station. Unfortunately these components are the most expensive parts of a computer system. Cost development can be expected to go towards cheaper components, but ever bigger capacity is on the other hand required from the computers for being able to handle the ever more complex softwares. The system with moveable hard disc(s) therefore will become comparatively expensive as at least two complete computers and one moveable hard disc have to be used.

In more recent time small portable computers, so called notebook computers have been developed. These computers however suffer from a number of crucial drawbacks. The battery powered computers are often rather heavy and bulky and must normally be carried along as an extra briefcase. The operating time will furthermore be rather short as the mechanical components such as floppy disc drives, hard discs, etcetera, consume much energy.

The graphic display unit will not give the same resolution and not the color quality, a fixedly installed monitor unit normally can offer. Display units based on liquid crystal technique are often slow and have smaller display surface. The portable display units furthermore require that surrounding light falling thereon is reduced and that the display surface is viewed straight from the front as the viewing angle is limited. The keyboards are also small and inconvenient to work with. Portable computers when not powered by built-in batteries, furthermore have to be connected to mains voltage via a cable, which then must be carried along. Then the use is limited by the distance to a voltage tap.

Said drawbacks contribute to the fact that portable computers are manufactured and marketed in smaller series resulting in substantially higher prices as compared to corresponding computers intended for "fixed installation". This is consequently a

clear competitive drawback.

With known technique it is thus today possible to transfer and use programmes and data between two or more computer stations. The transfer may take place e.g. via data discettes, or, as mentioned via moveable hard discs. The firstmentioned is an inexpensive solution but requires a comprehensive work and it is in practice almost unused when it concerns data between different work stations. The technique furthermore requires expensive standard computers (with central processor units and RAM-storages) at the different work sites.

The portable computes are neither a sound alternative, i.a. due to their high price, their limited display unit quality and due to the fact that series of connections must be made before any real work can start (connection to mains voltage, network, further peripheral equipment, such as printer, mouse, etcetera).

Purpose and most essential features of the invention

The purpose of the invention is to provide a computer which eliminates the abovementioned drawbacks and combines the capacity of a powerful computer with a convenient flexible and cost efficient utilization and the use of which can be compared to having access both to a stationary and to a portable computer. The invention shall make possible simple installation at home, at the work site, at the customer's office, in the car, in the boat, in the weekend cottage, in the caravan, etcetera, and it also shall reduce the need of file transfer between different computer stations.

Another purpose of the invention is to make the most expensive and valuable parts of the computer unusable to others than the owner, or to personnel authorized by the owner, and the parts shall be easy to lock for reducing the risk for theft.

A further purpose of the invention is to make possible up-grading of older computer systems in a simple manner in order to achieve larger computer capacity at a lower cost and with additional user advantages gained with the invention. This is obtained by the features defined in the claims.

Drawing list

The invention herinafter will be further described with reference to the accompanying drawings, wherein

5

Fig 1, schematically shows a work station, with the parts included therein, in accordance with the invention,

Fig 2, shows more in detail, the parts included in the computer according to the invention and,

10

Fig 3, shows a module according to the invention, with the components forming part thereof and shown partly broken up.

Prefered embodiment

15

In figure 1 is shown a work station built in accordance with the invention. The work station mainly comprises a computer 1 and peripheral equipment 5-9. The computer 1 consists in turn of a docking station 2 and a module 3 inserted therein. A series of peripheral units such as a monitor 5, a keyboard 6, a laser printer 7, a digitizer 8 and a mouse 9 are connected to the computer 1 via connectors 4. The computer is further equipped with a connection intended for an external network 10. For driving the computer 1 is required mains current, wich is supplied via a connector for mains voltage 11.

20

The docking station 2 is mainly intended for stationary installation at a work site whereas the module 3 is detachable and intended to be easily moveable. For this purpose the docking station 2 is provided with a recess 12, the inner measures of which mainly corresponds to the outer measures of the module 3 and in which recess 12 the module 3 can be pushed in and be connected to the docking station 2 electrically and/or as to signals e.g. via electrical connectors 13, 22 or contact-free via optical members (not shown). The optical system may for instance comprise signal transfer units (not shown), having transmitting and recieving functions, and being positioned in the module 3 as well as in the docking station 2, and by means of which signal transmission is effected in a contact-free mode, e.g. via optical member such as laser optics, LED technique or the like. The signal transmission is effected at a speed about 100 MBaud.

30

35

The connecors 13, 22 are preferably of conventional type with a male part and a

female part. For transmission of the data via the data bus, the connector 13, 22 incorporates a number of contact pins, e.g. 90. The connector 13, 22 incorporates either an integral or separate part for transmission of drive current. For this purpose is normally required 4 contact pins. The connector 13 in the module 3 is preferably recessed into the casing in order to reduce the risk for mechanical damages to the contact pins, whereas the male part of the connector 22 is provided in the docking station 2, where it is well protected for mechanical damages.

Preferably the module 3 is designed with the same installation dimensions as a normally 3.5" floppy discette drive but it may of course also be designed with larger or smaller installation dimensions. Packing of the necessary electronics within the smaller dimensions is made possible by new generation of moveable auxiliary storages (e.g. hard discs) that has been developed. As an example it can be mentioned that a hard disc known as PraireTek (registered trademark) with a 2.5" disc has the external dimensions 100 x 70 x 15 mm and accomodates 20 Mb. A somewhat bigger but for this purpose quite useful hard disc accomodates 40 Mb and the development goes towards hard discs having higher capacity. It is of course possible also to use stationary electronic storages as secondary memory.

In Fig. 2 the parts incorporated in the computer 1 are further shown. In the module 3 there is e.g. provided a secondary memory 14, preferably a hard disc drive (HDD), also other expensive electronics, such as main board 15 with a central processor unit (CPU) 16, a control program unit for the computer (BIOS) 17, primary storages (RAM) 18, etcetera. It also shall be possible optionally to install a matematical coprocessor (MPU) 19 in existing base. The module 3 also contains an electronics unit, so called IDE interface 20, for driving/controlling the hard disc drive 14. An internal bus 21 interconnects the different internal units of the module 3 as to signals. The CPU 16 may be either a 80286 processor or a 80386SX processor having an operation frequency of e.g. 16 MHz. The size of the primary storage 18 is 1 Mb but it is easily expandable up to 8 Mb or more by addition of circuits in the different storage banks (RAM 1, RAM 2 etcetera).

The connector 13 engages the connector 22 when the module 3 is pushed into the docking station 2. The "internal bus" (multi conductor) 21 of the module 3 thereby is connected to the "external bus" 29 of the docking station 2, which is provided on the bus board of the docking station (not shown). The bus board thereby consequently replaces certain functions normally maintained by the conventional

main board. The computer bus thus extends through the module 3 and also through the docking station 2. When the module 3 and the docking station 2 are separated from each other the bus thereby is divided into two physical parts and data processing may not be accomplished.

5

To the external bus 29 is connected a graphic adapter 24, a keyboard contact 25, a parallel port 26, a serial port 27 and a network adapter 30. There are empty board positions 31 for expansion boards.

10 The connectors 13, 22 may consist of further parts, wherein beside the bus connection there is possibility directly to connect an additional hard disc drive, an additional floppy discette drive, etcetera.

15 The graphic adapter 24 controls, in a manner known per se the graphic of the monitor unit 5. The keyboard 6 is controlled by means of a function intended therefore and integral with the CPU 16. Via a parallel port unit 26 and/or via the serial port unit 27 it is possible to connect e.g. a laser printer 7, a mouse 9, a digitizer 8 etcetera, to the computer.

20 The network adapter 30 makes possible the communication with other computers (not shown). The docking station 2 includes, besides the docking space 12 itself, other electronic units necessary for the function of the computer 1. A power supply unit 23 is thus provided for supply of power to the docking station 2 and for controlling its peripheral equipment but also for the current requirement of the
25 module 3. The current is transformed in the power supply unit 23 to voltage levels suited for the computer and its electronics, e.g. +/- 5V and +/- 12 V.

30 One or more floppy discette drives (FDD) may also be located in the docking station 2 as well as an additional hard disc drive 28 controlled from the module 3 via separate conduits (not shown).

35 The invention may also be applied for older computers, which easily can be rebuilt to suit the new technique. In one of the standard spaces, which has normally been reserved for an auxiliary discette drive or an auxiliary hard disc drive, it is then possible to mount a cassette especially designed for the purpose, which thereby operates as a docking station. The conventional main board then is exchanged for a "bus board" without CPU. This means that older computers do not have to be

discarded e.g. when the capacity of the computer system has to be expanded.

5 In figure 3 is shown, partly in broken up mode, an example of the appearance of a module 3 according to the invention in practice. Connectors 13 are provided in one gable of the module 3 for interconnection of the internal and the external bus, a possible external discette drive unit and/or an additional hard disc drive.

10 The computer according to the invention is provided with a code system, which inhibits the possibility for unauthorized persons to use the computer. The code system is implemented in the software in known manner; but it may also be accomplished as an electronic unit positioned in the module 3. This will reduce the attractiveness for thefts and the data security will increase.

15 By the structural design is achieved that several computer installations, as mentioned above, can be obtained at comparatively low cost in that expensive components must not be doubled, that software and data may be transported in a convenient and safe manner and that the need for set ups has been practically eliminated at transport between different work stations i.e. the set up time/start time is short.

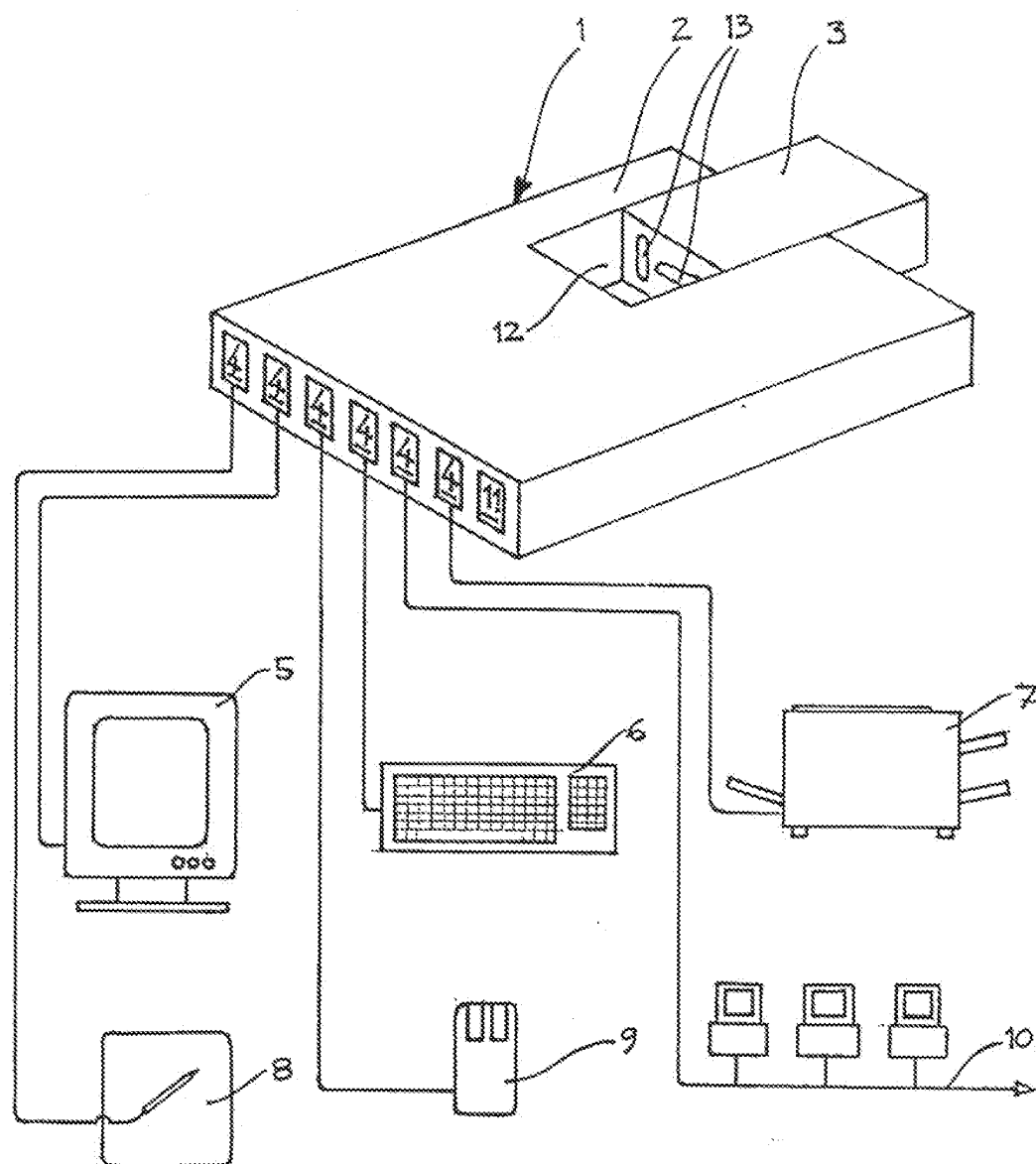
20 The invention is of course not limited to the embodiment described but may be varied within the scope of the appended claims. It thus is quite possible to build in a docking unit in the dashboard of a car, a boat or the like. It is also possible to mount a docking unit below the tabletop at the work site or just on or in the wall adjacent the work site in question. When there is too little space at the location where it is desirable to place the docking station 2, it is possible to position space requiring electronic components separately in a cover of its own, which via cables is connected to the docking station 2.

30

Claims

- 5 1. A computer comprising components necessary for data processing, such as e.g. main board with CPU, primary and secondary memory and electronics for driving peripheral equipment such as monitor, keyboard, printer etcetera, and which computer is composed by at least two easily interconnectable parts,
characterized therein,
- 10 that one of the parts is an easily movable module (3), and that this module (3) incorporates at least the CPU, primary and secondary memory of the computer and, that the module (3) is arranged to be connected to or docked in a docking station (2) intended for stationary installation and, that the module (3) and the docking station (2) thereby form an integral unit and an operating computer.
- 15 2. A computer as claimed in claim 1,
characterized therein,
that the docking station (2) incorporates, or is connected to, at least a power supply (23) and electronic unit (20-24) for driving the peripheral equipment such as e.g.
- 20 monitor (5), keyboard (6) and printer (7).
3. A computer as claimed in claim 1 or 2 ,
characterized therein ,
that the module (3) is arranged to be moveable between, dockable in, or
- 25 connectable to different docking stations (2).
4. A computer as claimed in anyone of the above claims,
characterized therein ,
that signal transmission units with transmitting and receiving functions are provided
- 30 in the module (3) as well in the docking station (2) and by means of which the signal transmission between the module (3) and the docking station (2) is effected contactfree e.g. via optical members such as laser optics, LED technique or the like.

1/3

FIGURE 1

2/3

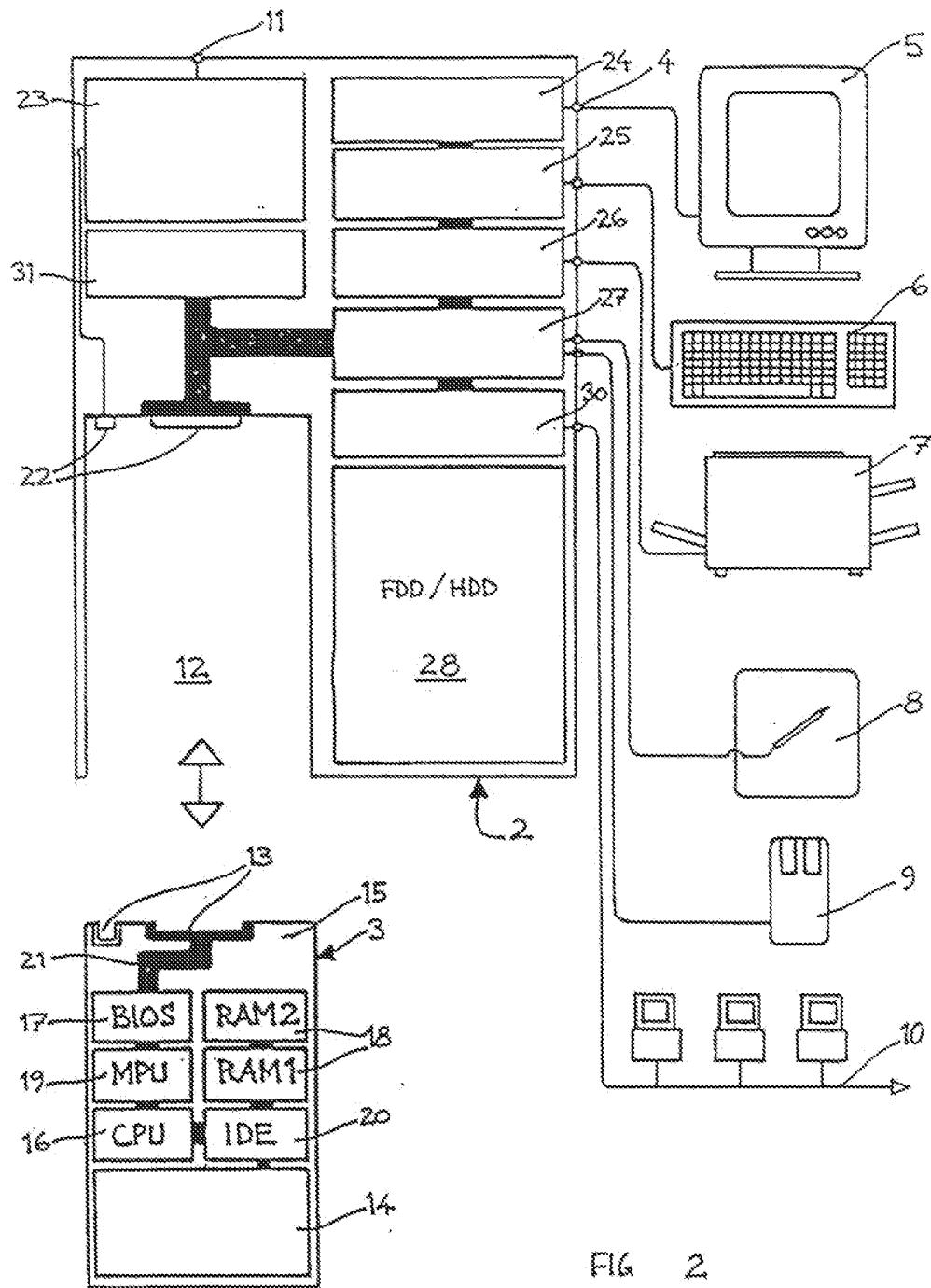


FIG 2

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3/3

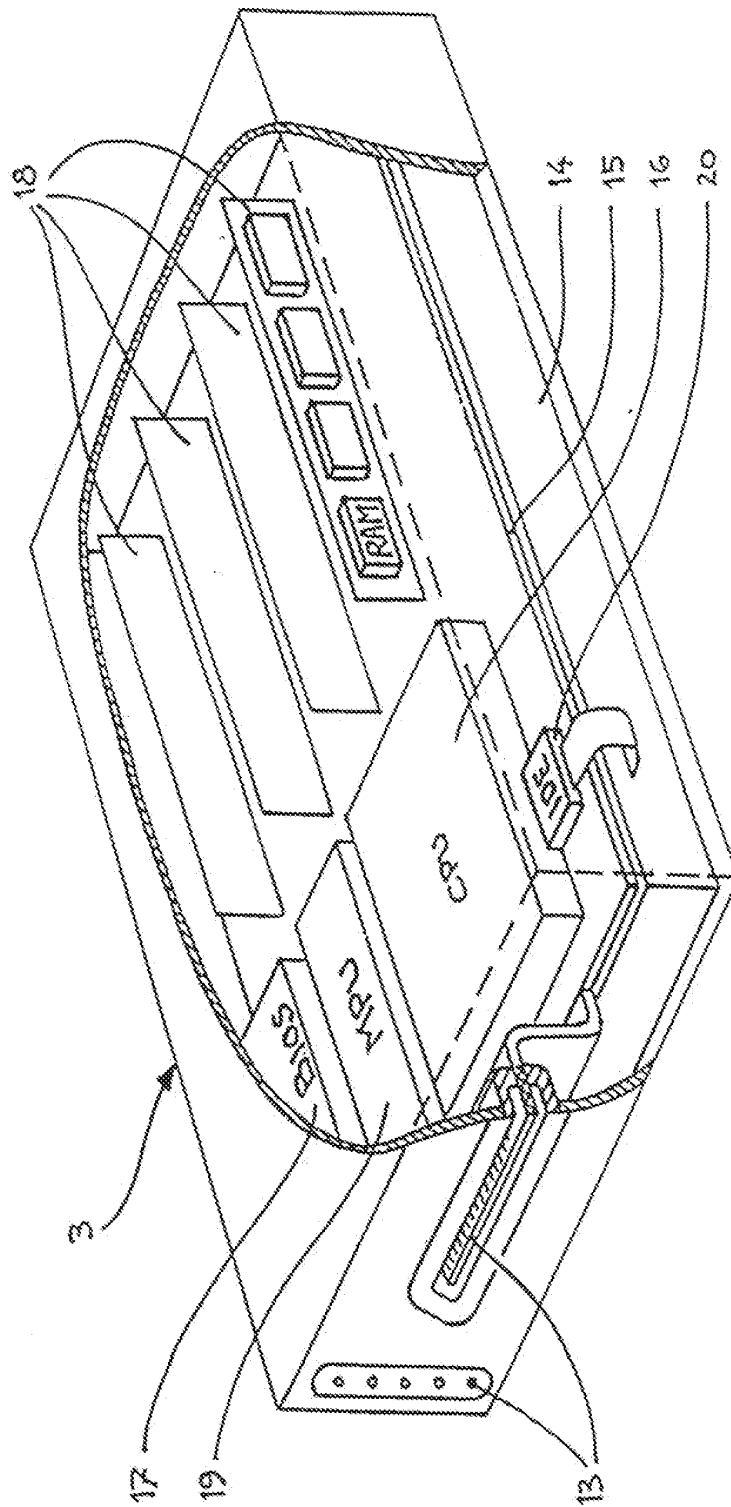


FIG 3

SUBSTITUTE SHEET

INTERNATIONAL SEARCH REPORT

International Application No PCT/SE 92/00253

I. CLASSIFICATION OF SUBJECT MATTER (If several classification symbols apply, indicate all) ⁶ According to International Patent Classification (IPC) or to both National Classification and IPC IPC5: G 06 F 1/16																										
II. FIELDS SEARCHED <div style="text-align: center; font-size: small;">Minimum Documentation Searched⁷</div> <table style="width: 100%; border: none;"> <tr> <td style="width: 30%; border: none; vertical-align: top;"> <div style="border: 1px solid black; padding: 2px;">Classification System</div> <div style="border: 1px solid black; padding: 2px; margin-top: 10px;">IPC5</div> </td> <td style="width: 70%; border: none; vertical-align: top;"> <div style="border: 1px solid black; padding: 2px;">Classification Symbols</div> <div style="border: 1px solid black; padding: 2px; margin-top: 10px;">G 06 F</div> </td> </tr> </table> <div style="text-align: center; font-size: x-small; margin-top: 10px;">Documentation Searched other than Minimum Documentation to the extent that such Documents are included in Fields Searched⁸</div>			<div style="border: 1px solid black; padding: 2px;">Classification System</div> <div style="border: 1px solid black; padding: 2px; margin-top: 10px;">IPC5</div>	<div style="border: 1px solid black; padding: 2px;">Classification Symbols</div> <div style="border: 1px solid black; padding: 2px; margin-top: 10px;">G 06 F</div>																						
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SE,DK,FI,NO classes as above																										
III. DOCUMENTS CONSIDERED TO BE RELEVANT⁹ <table border="1" style="width: 100%; border-collapse: collapse; font-size: x-small;"> <thead> <tr> <th style="width: 10%;">Category *</th> <th style="width: 60%;">Citation of Document,¹¹ with indication, where appropriate, of the relevant passages¹²</th> <th style="width: 30%;">Relevant to Claim No.¹³</th> </tr> </thead> <tbody> <tr> <td style="text-align: center; vertical-align: top;">X</td> <td style="vertical-align: top;">US, A, 4769764 (ISAAC LEVANON) 6 September 1988, see column 5, line 62 - column 6, line 12; column 8, line 1 - line 42; figures 2,7A,7B</td> <td style="text-align: center; vertical-align: top;">1-3</td> </tr> <tr> <td style="text-align: center; vertical-align: top;">Y</td> <td style="text-align: center; vertical-align: top;">---</td> <td style="text-align: center; vertical-align: top;">4</td> </tr> <tr> <td style="text-align: center; vertical-align: top;">Y</td> <td style="vertical-align: top;">US, A, 4942534 (YOKOYAMA ET AL) 17 July 1990, see column 2, line 66 - column 3, line 18; figure 3</td> <td style="text-align: center; vertical-align: top;">4</td> </tr> <tr> <td style="text-align: center; vertical-align: top;">A</td> <td style="text-align: center; vertical-align: top;">---</td> <td style="text-align: center; vertical-align: top;">1-3</td> </tr> <tr> <td style="text-align: center; vertical-align: top;">Y</td> <td style="vertical-align: top;">EP, A2, 142013 (MARTE, GERHARD) 22 May 1985, see page 1, line 1 - line 10; figure 1</td> <td style="text-align: center; vertical-align: top;">4</td> </tr> <tr> <td style="text-align: center; vertical-align: top;">A</td> <td style="text-align: center; vertical-align: top;">---</td> <td style="text-align: center; vertical-align: top;">1-3</td> </tr> <tr> <td colspan="3" style="text-align: center; vertical-align: top;">-----</td> </tr> </tbody> </table>			Category *	Citation of Document, ¹¹ with indication, where appropriate, of the relevant passages ¹²	Relevant to Claim No. ¹³	X	US, A, 4769764 (ISAAC LEVANON) 6 September 1988, see column 5, line 62 - column 6, line 12; column 8, line 1 - line 42; figures 2,7A,7B	1-3	Y	---	4	Y	US, A, 4942534 (YOKOYAMA ET AL) 17 July 1990, see column 2, line 66 - column 3, line 18; figure 3	4	A	---	1-3	Y	EP, A2, 142013 (MARTE, GERHARD) 22 May 1985, see page 1, line 1 - line 10; figure 1	4	A	---	1-3	-----		
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<div style="display: flex; justify-content: space-between; font-size: x-small;"> <div style="width: 48%;"> <p>* Special categories of cited documents:¹⁰</p> <p>"A" document defining the general state of the art which is not considered to be of particular relevance</p> <p>"E" earlier document but published on or after the international filing date</p> <p>"L" document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)</p> <p>"O" document referring to an oral disclosure, use, exhibition or other means</p> <p>"P" document published prior to the international filing date but later than the priority date claimed</p> </div> <div style="width: 48%;"> <p>"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention</p> <p>"X" document of particular relevance, the claimed invention cannot be considered novel or cannot be considered to involve an inventive step</p> <p>"Y" document of particular relevance, the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art.</p> <p>"B" document member of the same patent family</p> </div> </div>																										
IV. CERTIFICATION <table style="width: 100%; border: none;"> <tr> <td style="width: 50%; border: none; vertical-align: top;"> <div style="border: 1px solid black; padding: 2px; font-size: x-small;">Date of the Actual Completion of the International Search</div> <div style="border: 1px solid black; padding: 2px; margin-top: 10px;">17th July 1992</div> </td> <td style="width: 50%; border: none; vertical-align: top;"> <div style="border: 1px solid black; padding: 2px; font-size: x-small;">Date of Mailing of this International Search Report</div> <div style="border: 1px solid black; padding: 2px; margin-top: 10px;">1992 -07- 20</div> </td> </tr> <tr> <td style="border: none; vertical-align: top;"> <div style="border: 1px solid black; padding: 2px; font-size: x-small;">International Searching Authority</div> <div style="border: 1px solid black; padding: 2px; margin-top: 10px; text-align: center;">SWEDISH PATENT OFFICE</div> </td> <td style="border: none; vertical-align: top;"> <div style="border: 1px solid black; padding: 2px; font-size: x-small;">Signature of Authorizing Officer</div> <div style="border: 1px solid black; padding: 2px; margin-top: 10px; text-align: center;"> Katarina Fredriksson </div> </td> </tr> </table>			<div style="border: 1px solid black; padding: 2px; font-size: x-small;">Date of the Actual Completion of the International Search</div> <div style="border: 1px solid black; padding: 2px; margin-top: 10px;">17th July 1992</div>	<div style="border: 1px solid black; padding: 2px; font-size: x-small;">Date of Mailing of this International Search Report</div> <div style="border: 1px solid black; padding: 2px; margin-top: 10px;">1992 -07- 20</div>	<div style="border: 1px solid black; padding: 2px; font-size: x-small;">International Searching Authority</div> <div style="border: 1px solid black; padding: 2px; margin-top: 10px; text-align: center;">SWEDISH PATENT OFFICE</div>	<div style="border: 1px solid black; padding: 2px; font-size: x-small;">Signature of Authorizing Officer</div> <div style="border: 1px solid black; padding: 2px; margin-top: 10px; text-align: center;"> Katarina Fredriksson </div>																				
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Form PCT/ISA/210 (second sheet) (January 1985)

ANNEX TO THE INTERNATIONAL SEARCH REPORT
ON INTERNATIONAL PATENT APPLICATION NO. PCT/SE 92/00253

This annex lists the patent family members relating to the patent documents cited in the above-mentioned international search report. The members are as contained in the Swedish Patent Office EDP file on 29/05/92. The Swedish Patent Office is in no way liable for these particulars which are merely given for the purpose of information.

Patent document cited in search report	Publication date	Patent family member(s)	Publication date
US-A- 4769764	88-09-06	NONE	
US-A- 4942534	90-07-17	JP-A- 1150879	89-06-13
EP-A2- 142013	85-05-22	NONE	

PCT

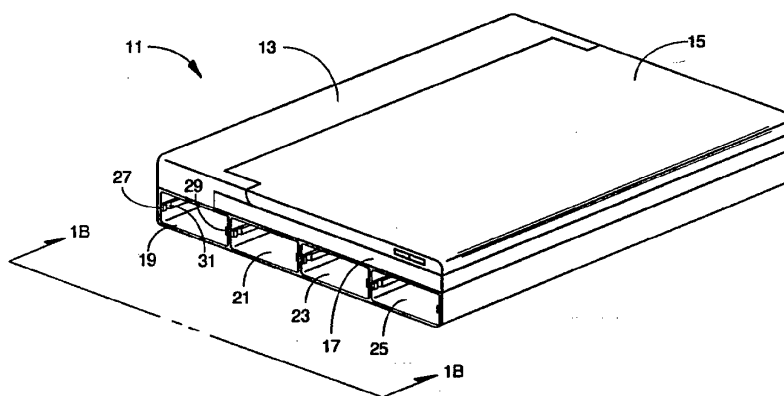
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INTERNATIONAL APPLICATION PUBLISHED UNDER THE PATENT COOPERATION TREATY (PCT)

(51) International Patent Classification ⁵ : H05K 7/10, G06F 1/16	A1	(11) International Publication Number: WO 94/00970 (43) International Publication Date: 6 January 1994 (06.01.94)
(21) International Application Number: PCT/US93/06146 (22) International Filing Date: 29 June 1993 (29.06.93) (30) Priority data: 07/905,480 29 June 1992 (29.06.92) US (71) Applicant: OAKLEIGH SYSTEMS, INC. [US/US]; 810 E. Arques Avenue, Sunnyvale, CA 94086 (US). (72) Inventor: KIKINIS, Dan ; 20264 Ljepava Drive, Saratoga, CA 95070 (US). (74) Agent: BOYS, Donald, R.; P.O. Box 187, Aromas, CA 95004 (US).		(81) Designated States: JP, European patent (AT, BE, CH, DE, DK, ES, FR, GB, GR, IE, IT, LU, MC, NL, PT, SE). Published <i>With international search report.</i>

(54) Title: MODULAR NOTEBOOK COMPUTER



(57) Abstract

A modular notebook computer has a framework (11) with module bays (19, 21, 23, 25) for receiving CPU modules, power modules, and peripheral function modules such as floppy and hard disk drives. The framework has a built-in compressed bus and a variety of function modules which can be plugged into any one of the module bays. Function modules include, but are not limited to, CPU, power, floppy disk, hard disk, RAM memory, LAN communication, modem, FAX communication, and data acquisition.

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Modular Notebook Computer

Field of the Invention

The present invention is in the area of portable computer systems, and is particularly relevant to portable computers known as notebook computers.

Background of the Invention

Notebook computers are popular among computer users who travel and need to take their work along. They are smaller and lighter than laptops, and are therefore more portable. The evolution to smaller and lighter portable computers, however, is not without problems. For one thing, smaller portable computers means less space for battery packs, which usually means shorter useful life between recharges. Another problem related to smaller size is a difficulty in providing versatility. Smaller size naturally means less space to provide a broad choice in peripheral devices and options.

Yet another problem is related to addresses and data byte size. State-of-the-art computers are capable of 32 bit addresses and 32 bit data words. A 32 bit computer, though, typically needs a bus structure with nearly 100 active signals, equating to high pin count and extensive device and component density. Such high density in a small computer creates many other problems, such as problems with heat dissipation. These are a few of the many problems in designing and developing notebook computers.

What is needed is a new design for a notebook computer based on a bus structure allowing 32-bit capability with a minimum pin count, utilizing, for example, multiplexing of address and data on a single 32 bit structure, and utilizing only state-of-the-art technology to minimize power (hence buffer) requirements, which also minimizes heat and equipment complexity and

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density problems. Modularity needs to be raised to a new level by making virtually all components modular and "plug-in", including CPUs, power packs, and all of the various known sorts of peripheral devices.

Summary of the Invention

In an embodiment of the present invention a frame work for a modular computer is provided having a frame and enclosure for supporting and housing other elements and module bays for docking functional modules. The frame and enclosure supports a Notebus for address, power control, and data transmission between module bays, including a compressed bus architecture with data and address words sharing one set of parallel traces, and at least one power trace for transmitting electrical power. The framework also has an electrical power conversion unit for accepting electrical power from outside the framework, converting it to voltage and current levels needed by the module bays, and supplying the converted power to the power trace of the Notebus. In addition, there is a display screen and a keyboard for input and output, and each module bay has a receiving connector for receiving a mating connector on a function module and providing connection to the Notebus.

In one embodiment the framework has a central spine housing a portion of the Notebus, and a plurality of module bays arranged to either side of the notebus. In this embodiment each module bay has a receiving connector, guides for guiding a function module into position, a latching device for holding the function module in the module bay with the mating connector engaged in the receiving connector, and an expulsion mechanism for expelling a function module upon initiation by an operator.

A CPU module is provided according to an embodiment of the invention with a CPU mounted in a case configured

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to guide into and dock in a module bay of the framework provided. A state translator resides in the CPU module, and is connected to translate between the states of the CPU and the states of the Notebus. In one embodiment the CPU module has on-board RAM for providing quick memory response without bus wait states.

A modular computer according to the present invention has a framework as described above, plus a CPU function module docked in a module bay and connected to the Notebus. There are power modules provided according to embodiments of the invention for providing power, and more than one such power module may be used to provide extended operating time. There are also function modules provided for such as floppy disks, hard disk drives, LAN communication, additional RAM, modem communication, serial communication, and FAX transmission over phone lines.

The modularity of the present invention is unique in providing modular CPU coupling, which allows a user to upgrade the modular computer to a more powerful CPU, or to a CPU dedicated to, or especially designed for, a particular need. The modularity also allows a user to tailor the computer to provide longer (or shorter) time between recharges.

Brief Description of the Drawings

Fig. 1A is an isometric view of a modular notebook computer framework according to an embodiment of the present invention.

Fig. 1B is a view of the computer framework of Fig. 1A from one side from the vantage of line 1B-1B on Fig. 1A.

Fig. 2 is a sectioned plan view of the computer framework of Fig. 1A taken according to section line 2-2 of Fig. 1B.

Fig. 3 is an isometric illustration showing a

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function module according to the present invention associated with a docking bay of the framework of Fig. 1A.

Fig. 4 is another view of a function module according to the present invention.

Fig. 5 is a block diagram of a compressed bus and connection to docking bays in a computer framework according to an embodiment of the present invention.

Fig. 6 is a block diagram of a CPU function module according to an embodiment of the present invention.

Fig. 7 is a block diagram of a power supply function module according to an embodiment of the present invention, with indication of connections to the internal bus structure and power conversion unit of the computer.

Fig. 8 is a block diagram of a floppy disk drive function module used in the invention.

Fig. 9 is a block diagram of a hard disk drive module used in an embodiment of the invention.

Fig. 10 is a block diagram of a "flash card" memory module according to an embodiment of the present invention.

Fig. 11 is a block diagram of a LAN module according to an embodiment of the present invention.

Fig. 12 is a block diagram of a modem module according to an embodiment of the present invention.

Fig. 13 is a block diagram of a FAX module according to an embodiment of the present invention.

Fig. 14 is a block diagram of a data acquisition module according to an embodiment of the present invention.

Description of the Preferred Embodiments

General Description

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Fig. 1A is an isometric drawing of a notebook computer framework 11 according to the invention. Framework 11 comprises a back housing 13, a tilt-up flat panel display 15, shown closed, a keyboard 17, and a plurality of module bays for plugging in function modules. Back housing 13 includes a power unit for converting electrical input on a wide variety of standards to the form required by the computer. For example, there is a port (not shown) for connecting to a standard household outlet, rated at 120 V., 60 Hz, alternating current. The power unit will convert the input to outputs as needed by the computer bus and functional modules. There are also input ports for 6 V. DC, 12 V. DC, 9 V. DC, and others, and the power unit in one embodiment of the present invention is capable of recognizing the input characteristics by sampling, and switching to proper on-board circuitry to utilize the input.

In the embodiment shown by Fig. 1A four module bays 19, 21, 23, and 25 are shown along one side of the framework. There are four more module bays along the other side of the framework opposite the module bays shown. There could be more or fewer module bays, but eight is convenient and a good balance between the need to stay small and simple, and to also have adequate versatility.

Fig. 1B is an end view of the notebook computer framework of Fig. 1 in the direction of arrows 1B-1B of Fig. 1A. Each of the module bays has a set of guide and positioning rails such as rails 27 and 29 in bay 19. The rails are to position and guide a function module inserted into the module bay. Each rail in a set has a detent such as detent 31 for latching a module when the module is fully inserted in the bay. Each bay also has a connector such as connector 33 in bay 19. The connectors are for coupling to a mating connector on a function module inserted in a bay. It will be apparent to a

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person with skill in the art that there are a number of equivalent ways guide rails, detents, and coupling may be accomplished.

Fig. 2 is a plan section view just above the module bays taken along section line 2-2 of Fig. 1B. Bays 19, 21, 23, and 25 are shown on one side of the section view, and bays 35, 37, 39, and 41 along the opposite side. A printed circuit board structure 57 is fastened in a substantially vertical position down the center of frame 59, and connectors 33, 43, 45, 47, 49, 51, 53, and 55 are connected to the printed circuit board structure and present their pin structure outward toward the respective bay areas. In the presently described embodiment the internal connectors are male connectors, but this is not a requirement of the invention.

As also shown in Fig. 1A, each module bay has a pair of opposed rails located vertically at about the midpoint of the height of the module bay. Rails 27 and 29 serve module bay 19, and similar rails are located in each of the other module bays.

Fig. 3 is an isometric view of a function module 61 according to the invention aligned with module bay 25 of framework 11. Module 61 includes guides 63 and 65 on opposite sides for engaging rails 67 and 69 when module 61 is inserted into bay 25. The module has two spring-loaded detent levers (lever 73 is shown) for engaging detents in guide rails 67 and 69 when the module is fully inserted. Detent 71 is shown in rail 67 in Fig. 3.

Each module bay has a compression spring mechanism engaged by a function module as the module nears full insertion, so there is an outward force on the module when the detent levers engage the detents. Mechanism 75 (Fig. 2) is exemplary. To insert a module one aligns the guides in the module with the guide rails and pushes the module into the module bay until the detents engage.

Button 79 on front face 77 of the module is for retracting the detent levers of the module, in which case

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the spring mechanism ejects the module, much as is the case with some floppy disk drives.

Fig. 4 is an isometric view of function module 61, showing back face 81 opposite front face 77. The back face includes a recessed female connector receptacle 83 in the preferred embodiment, for mating with male connectors positioned in each pod bay, such as connector 33 in Fig. 1B and Fig. 2. A second detent lever 74 is opposite lever 73 of Fig. 3.

In the embodiment described above, and in many other embodiments, the notebook computer framework of the present invention comprises a frame with module bays and connectors as described above for "plugging in" function modules, power supply units, and other peripheral devices. The framework also comprises display 15, keyboard 17, and an internal bus structure hereinafter termed the Notebus, which is described in additional detail below, in the section titled "Notebus Bus Structure".

The function modules, as represented by module 61 in Fig. 3 and Fig. 4, are provided in a wide variety of different models capable of a wide variety of different functions. For example, framework 11 has no "on-board" CPU, battery power, or system memory. These functions and all other functions are provided by different models of function modules which may be inserted in any one or a combination of the available module bays. Other kinds of function modules that may be inserted include floppy-disk drives, hard-disk drives, "flashcard" memory modules, LAN and modem adapters, Fax modules, specialty modules such as data acquisition modules adapted to specific equipment, and more. The function modules are also described in more detail in the section below titled "Function Modules".

Electronic Architecture

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Fig. 5 is a block diagram showing internal elements of Notebook computer framework 11, connected to show the electronic architecture of the notebook computer according to the invention. Power input and conversion unit 85 is housed in back housing 13 (Fig. 1) and has ports 87 for power inputs. Unit 85 senses the input conditions and selects appropriate circuitry to convert the input to the voltages needed to power the other elements of the system. Output from the conversion unit is to Notebus 89, which comprises paths for power as well as for digital information such as data and addresses. Because there are a wide variety of function modules, as indicated above and described in more detail below, there needs typically to be more than one power line in the Notebus. For example, the notebook computer of the invention comprises hard disk drive modules, and these modules are preferably provided without their own "on board" power source. The motor drive for the hard disk requires a different power (voltage and current) than does a CPU, for example, so there are parallel power lines of differing size and voltage level in the notebus. A typical Notebus will have, for example, a line for 24V DC, another for 12V DC, and yet another for 5V DC, as well as multiple ground lines.

Notebus 89 connects to a video display controller 91 including Video Random Access Memory (VRAM) which both powers and controls display 15, which in the preferred embodiment is a flat panel display driven by analog driver lines on analog bus 93. Notebus 89 also connects to a keyboard controller 95 which powers and controls keyboard 17 over link 97, accepting keystroke input and converting the input to digital data for transmission on Notebus 89. The keyboard controller may be physically mounted in the keyboard or in framework 11.

Notebus 89 also connects as illustrated in Fig. 5 to each of the module bays, such as bay 19, through connectors, such as connector 33. When a function

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module, such as module 61, is inserted into a module bay, the mating connector in the back of the function module mates with the connector from the Notebus, and circuitry inside the function module is then connected to the Notebus.

Notebus Bus Structure

The Notebus comprises, as stated above, both power and data paths. The digital lines are capable of carrying 32 addresses and conveying data in 32 bit word length. To minimize pin count and routing complexity, addresses and data are multiplexed on a single set of 32 traces in the overall bus structure. One with skill in the art will recognize that this type of bus is what is known in the art as a low-pin-count or compressed bus. In this kind of bus different types of signals, such as address and data signals, share signal paths through multiplexing. For example, the same set of data lines are used to carry both 32-bit addresses and data words of 32-bit length.

In the Notebus of the present invention, some control signals, such as interrupt arbitration signals, may also share the data lines. Typical examples of buses that are exemplary as usable for the Notebus (with the exception of power supply analog lines in the Notebus) are the "S-Bus" implemented by Sun Microsystems, the "Turbochannel" Bus from Digital Equipment Corporation, and buses compatible with the IEEE-488 standard.

The Notebus is a high-speed backplane bus for interconnecting processor, memory and peripheral device modules. The Notebus also supplies standard operating and standby power supply voltages and electrical ground to all module bays.

Function Modules

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Fig. 3 and Fig. 4 show, as described above, two different views of a function module according to the present invention. Also as stated above, function modules may have many different functions. There are as many different functions, in fact, as there are possibilities for discrete peripheral devices, plus power and CPU modules. An individual function module is provided for each function, and in each case the function module has a physical size and form compatible with the bays, guide rails, and connectors for "plugging in" to framework 11.

The "face" of a function module, being the exposed face when the module is "plugged in" (see face 77 in Fig. 3) may have elements specific to the type of module. For example, a CPU module may have no indicators or other elements on the front face, while a floppy disc module will typically have an opening for inserting a floppy disk and a "key" or button for releasing and ejecting the floppy disk.

A unique feature of the present invention is that the CPU for the notebook computer is provided as a CPU function module. This provides an ability for a user to tailor the CPU power to the other modules and application for the notebook computer, and an easy upgrade to more powerful CPUs.

Fig. 6 is a diagram of a CPU module 99 plugged into a bay in a notebook computer according to the present invention. In this case (referring to Fig. 2) the module is plugged into bay 19 having connector 33. This is exemplary, as the module could just as well be plugged into any open bay of framework 11. By virtue of being plugged into connector 33 or another module connector, internal elements of the CPU module are connected to Notebus 89.

The internal elements for module 99 comprise CPU 103, a state translator 105, and RAM memory 113. CPU 103 may be any of a wide variety of CPUs (also called in some

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cases MPUs) available in the art, for example Intel 80386 or 80486 models, MIPS, RISC implementations, and many others. CPU 103 communicates with State Translator 105 over paths 107, and State Translator 105 communicates with connector 33, hence Notebus 89, over bus 109 internal to the module, which is an extension of bus 89 when the module is plugged into bus 89.

State translator 105 is a chip or chip set designed to translate commands and requests of the CPU to commands and requests compatible with the Notebus. It was mentioned above that CPU 103 may be one of a wide variety of CPUs, and that Notebus 89 may be any one of a wide variety of compressed buses. It will be apparent to one with skill in the art that there may be an even wider variety of state translators 105 for translating between the CPU and the Notebus. The state translator is theoretically a different device for each possible combination of CPU and Notebus.

RAM memory module 113 comprises conventional RAM chips mounted on a PCB as is known in the art, and connectable to state translator 105 by a plug or connector interface, such as an edge connector. The purpose of having a RAM module "on board" the CPU module is to provide for rapid memory access, which will be much slower if the RAM is made available in a separate module at one of the other module bays. Memory at another module bay is on the Notebus, and will be subject to bus contention and wait states. The plug-in nature of the RAM unit relative to the CPU module allows different amounts of memory to be provided with a CPU module in the notebook computer of the present invention.

As described above, Notebus 89 comprises not only the shared data and address lines, but also power and ground connections for the modules plugged into the various bays. Paths 109 and 107 therefore comprise power and ground lines for CPU 103 and Translator 105.

If, for example, CPU 103 is an INTEL 80486

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microprocessor, State Translator 105 will be a translator for accommodating the state machine of the 80486 to the state machine of the Notebus, which may be any one of the buses described above for bus 89, or another compressed bus. There are many equivalent ways a translator may be implemented for the specific case. Given the manufacturers available design information for the CPU and the equivalent information for bus 89, it is within the skill of workers in the art without undue experimentation to implement the translator and the required connections. This is conventional technology. The implementation of the translator on a module with a CPU to plug into a module bay in the notebook computer is unique to the present invention.

In the invention, state translators may be implemented in a single chip set or circuitry set to be capable of translating between a number of CPUs and a number of different bus possibilities. One might, for example, design and implement a translator with the necessary circuitry and intelligence to translate between three different CPUs and three different compressed buses. The state translator could be made hardware or software programmable to select one CPU and one bus from the available selections at some convenient time in the manufacturing cycle, or even at the time of selection of modules to make up a notebook computer.

As an example of a hardware programmable translator, a translator could be built to have certain traces cut as a near final step in manufacture as a way of selecting the CPU and bus pair. Translators could also be programmable by virtue of on-board EPROM or EEPROM devices. As an example of software programmability, translators could be implemented with microprocessor technology and software programmable. A CPU module could be plugged into a connector on a special programming unit, for example, before installation in a notebook computer according to the present invention, and

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be sent certain commands to set up on board software to translate between the desired CPU and bus. It will be apparent to one with skill in the art that there are many possible variations in the implementation of the translators.

Fig. 7 shows a power module 111 plugged into a bay in the notebook computer according to an embodiment of the present invention. The purpose of a power module is to provide a source of power for the computer, which includes any modules plugged into the module bays. As is common in notebook computers in the art, there may be a battery, typically rechargeable, in framework 11, and the battery may also be replaceable and rechargeable through power input lines 87. In the case of an on-board battery pack, there is the option of using all module bays for other than power packs.

Preferably framework 11, sans function modules, has no power capability other than power plugged into one of input lines 87, which may be converted to the power characteristics needed by the computer and distributed on the power lines of the Notebus. For portability, power is typically supplied by one (or more) power modules 111 plugged into one or more of the module bays.

Module 111 has a battery pack 101 which is connected via lines 117 to (in this case for example) connector 33, and hence to Notebus 89. Because there are several supply lines in the Notebus for supplying power to function modules at different voltage and with different current capability, the power lines in the Notebus for connecting a power module 111 are not the same as the lines for supplying power to a module. There is instead a separate set of power lines to pins on the module bay connectors, such as connector 33, which connect as input to power input and conversion unit 85, much as do input ports 87.

In Fig. 7, lines 119 and 121 connect power module 11 to conversion unit 85, where the power input from the

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power module is sensed and treated as a power source, much as is done for power input lines 87. This power is converted to the needed voltages and current capabilities, and put back out on the power supply output lines to the module bays. In Fig. 7 line 119 is ground, and arrow 123 represents all of the data/address, control, and power output lines to the module bays. Lines represented by arrow 123, plus lines 119 and 121 are Notebus 89. Although not shown in Fig. 7, there are connections for line 119 and for line 121 to each of the module bay connectors.

Power modules such as module 111 may be plugged into a connector on a charging module separate from the notebook computer, using the same connector used for plugging into the Notebus via a module bay of framework 11, and recharged for later use with a modular notebook computer according to the invention. This allows a user to keep spare power modules ready for use, and to recharge modules without connecting the computer itself to a charging unit. Moreover, the provision of power modules allows a user to provide more or less portable time to the notebook computer by using one or more than one power module.

Fig. 8 shows a floppy disk drive (FDD) module 125 plugged into a module bay in a notebook computer according to an embodiment of the present invention. Module 125 comprises a conventional FDD unit 129 for nominal 3.5 inch disks with conventional circuitry mounted in a case 130 to provide a module with guides, latches, and a connector matable with connector 35 to be able to plug into a module bay in the notebook computer of the present invention. The case comprises an opening 131 for inserting and withdrawing a floppy disk, and an eject button 133 for ejecting a floppy disk.

A controller 127 communicates with unit 129 over lines 126 and with connector 33 (hence Notebus 89) over lines 128. The unit also derives power from the

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appropriate pins on connector 33, but these pins and lines are not shown. Controller 127 is an ASIC chip or chip set for translating between the notebus and the FDD unit. Given the data storage standards of the FDD unit and the characteristics of bus 89, it is within the scope of workers with ordinary skill in the art to implement controller 127 without undue experimentation.

Fig. 9 shows a hard disk drive (HDD) module 135 according to an embodiment of the present invention plugged into bus 89 in a module bay of framework 11. HDD module 135 comprises a conventional HDD unit 139 mounted in a case 137 to be compatible with plugging into a notebook computer according to the present invention. As in the case of the FDD module described above, a controller 141 is provided to translate between Notebus 89 and the HDD unit. Controller 141 communicates with HDD unit 139 over lines 143, and with connector 33 over lines 145. Connector 33 is exemplary of any one of the module connectors in the notebook computer.

Given the characteristics of HDD unit 139 and of Notebus 89, it is within the skill of workers in the art to implement controller 141 without undue experimentation. Power line connections are not shown. In implementing controller 141 there are several protocols that may be used. One is the ST506 standard known in the art. Another is the IDE standard known in the art. Yet another is an enhanced IDE, called EIDE, known to the inventors, and the subject of a separate patent application to be filed. In the EIDE protocol, there may be multiple IDE devices daisy-chained and addressed as secondary IDE devices with an additional select number.

Fig. 10 shows a "flash card" memory module 147 plugged into connector 33 of the notebook computer of the invention. "Flash cards" are RAM memory cards known in the art pluggable into typically parallel ports to make connection with internal bus structures of a computer.

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Module 147 comprises a conventional "flash card" 151 mounted in a case 149 compatible with the module bay of a notebook computer according to the present invention. As in cases described above, a controller 153 is needed to accomplish communication between the memory structure of the "flash card" and bus 89. Controller 153 communicates with "flash card" unit 151 over lines 155 and with connector 33 over lines 157. There may optionally be an opening 159 in case 149 and a connector (not shown) within unit 151 for inserting and withdrawing flash cards, so relatively large collections of data may be plugged in as desired. Alternatively the interface may be the modular interface afforded by the plug-in module 147. Again, given the known characteristics of the flash card and of bus 89, implementation of the controller is a matter within the skill of workers in the art.

Fig. 11 shows a LAN module 161 plugged into connector 33 of a notebook computer according to an embodiment of the present invention. In the embodiment shown in Fig. 11 a conventional LAN card, such as an Ethernet card, is mounted in a case 163 to be compatible with plugging into a module bay of a notebook computer according to an embodiment of the present invention. LAN card 167 communicates with a conventional connector 165 in the face of the case of module 161 that is exposed when the module is plugged into a bay. This is a conventional connector of the sort known in the art for connecting computers on a network.

Within module 161, in a first alternative, conventional LAN card 167 interfaces to a controller 169 communicating over lines 171 and 173, and the controller translates between bus 89 and the conventional LAN card. In a second alternative, a LAN card is provided with the translation built-in, so no separate controller is needed. The first alternative is preferable.

Fig. 12 shows a modem module 175 plugged into

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connector 33 in a bay of a notebook computer according to an embodiment of the present invention. Modem module 175 comprises a conventional modem card 181 mounted in a case 177 to be compatible with plugging into a module bay. In this case, and other cases above, where the term "conventional" is used in conjunction with a card or unit, it is meant that the circuitry and function is conventional. The size may be adjusted to be compatible with a module case for plugging into a bay of a notebook computer according to the present invention.

Modem card 181 connects over lines 183 to a telephone interface 179, which may comprise more than one "jack" so a hand set may also be connected. Card 181 communicates to Notebus 89 over lines 187 and 189 through controller 185, which translates between the conventional card and the compressed bus. Alternatively, the translation components may be implemented on a single card along with the modem circuitry.

Fig. 13 shows a FAX module 191 plugged into connector 33 of a module bay in an embodiment of the present invention. Module 191 comprises a conventional FAX card 199 mounted in a case 193 to be compatible with plugging into a module bay in the present invention. Fax card 199 communicates over lines 197 with a telephone interface 195, which may, as in the case of the modem module described above, have more than a single telephone "jack".

A controller 201 provides an interface for the conventional FAX card between the card and Notebus 89 over lines 203 and 205. Alternatively, the controller may be implemented on the same card as the FAX circuitry. In yet another alternative, the FAX capability and the modem capability described above may be implemented into a single module.

Fig. 14 shows a specialty data acquisition module 207 plugged into connector 33 in a module bay in a notebook computer according to an embodiment of the

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present invention. Module 207 comprises a circuit card 215 mounted in a case 209 to be compatible with plugging into a module bay. Card 215 communicates over lines 213 to an interface 211 which may comprise one or several acquisition leads for connecting to outside equipment. For example, a data module may be provided for following the output of the vertical and horizontal sweep of an oscilloscope, and would have at least two input leads; one for the vertical and one for the horizontal sweep. Card 215 communicates over lines 217 to connector 33, hence Notebus 89. The circuitry on card 215 is designed to digitize the input if the input is analog, and to be compatible with Notebus 89. Given the characteristics of signals to be measured and the characteristics of Notebus 89, implementation of such a card is within the ordinary skill in the art. There are, in addition to the modules described herein, other modules that may be designed and built to extend the utility of the modular notebook computer of the present invention.

It will be evident to one with skill in the art that there are many changes that might be made without departing from spirit and scope of the present invention. Many of these alternatives have been described above. For example, there may be more than the eight module bays described, or fewer. Similarly, there are many ways modules may be built to be pluggable into a framework such as framework 11. There are similarly many different kinds of connectors that might be utilized. There are many kinds of compressed buses that can be used, and many kinds of modules that may be provided, and many other changes that might be made within the spirit and scope of the invention.

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What is claimed is:

1. A framework for a modular computer comprising:
frame and enclosure means for supporting and
housing elements of the framework, said frame and
enclosure means having module bays for docking functional
modules;

notebus means for address, power, control, and data
transmission between module bays, said notebus means
including a compressed bus architecture wherein data and
address words share one set of parallel traces, and at
least one power trace for transmitting electrical power;
electrical power conversion means for accepting
electrical power from outside said framework, converting
said outside electrical power to voltage and current
levels needed by said module bays, and supplying said
electrical power to said at least one power trace in said
notebus means;

display means connected to said notebus means for
displaying text and graphical information; and
keyboard means connected to said notebus means for
a user to input text and commands to said notebus;
each said module bay having a receiving connector
for receiving a mating connector on a function module and
providing connection to said notebus means.

2. A framework as in claim 1 wherein said frame and
enclosure means has a central spine housing a portion of
said notebus, and a plurality of module bays arranged to
each side of said central spine, each of said module bays
having guide means for accepting and guiding a module
into said module bay, a latching means for holding said
module when received with said mating connector engaged
in said receiving connector, and expulsion means operable
by a user for expelling a module from said module bay.

3. A CPU module for plugging into a module bay of a

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framework for a modular computer, said module bay having a receiving connector with pins connected to individual traces of a bus means within said framework, said CPU module comprising:

a casing for supporting and housing elements of said CPU module;

guide means for engaging guides in said module bay and guiding said CPU module into and out of said module bay when engaging and disengaging;

mating connector means for engaging said receiving connector to connect traces within said module to said bus;

CPU means mounted within said casing of said CPU module;

state translator means connected to said module connector and to said CPU means for translating signals between said bus and said CPU means.

4. A CPU module as in claim 3 further comprising RAM memory means connected to said state translator means, said RAM memory means for providing RAM memory with minimum access time to said CPU means.

5. A modular computer comprising:

frame and enclosure means for supporting and housing elements of the modular computer, said frame and enclosure means having module bays for docking functional modules;

notebus means for address, power, control, and data transmission between module bays, said notebus means including a compressed bus architecture wherein data and address words share one set of parallel traces, at least one power trace for transmitting electrical power to module bays, and connecting to a receiving connector in each of said module bays;

electrical power conversion means for accepting electrical power from outside said framework, converting

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said outside electrical power to voltage and current levels needed by said module bays, and supplying said electrical power to said at least one power trace in said notebus means;

display means connected to said notebus means for displaying text and graphical information;

keyboard means connected to said notebus means for a user to input text and commands to said notebus; and a CPU module docked in one of said module bays, said CPU module having module connector means engaging said receiving connector, connecting traces within said module to said bus, CPU means mounted within said CPU module, and state translator means connected to said module connector and to said CPU means for translating signals between said bus and said CPU means.

6. A power module for plugging into a module bay of a framework for a modular computer, said module bay having a receiving connector with pins connected to individual traces of a bus means within said framework, said power module comprising:
a casing for supporting and housing elements of said power module;
guide means for engaging guides in said module bay and guiding said power module into and out of said module bay when engaging and disengaging;
module connector means for engaging said receiving connector to connect traces within said power module to said bus means; and
electrical power storage means mounted within said power module for supplying electrical power to said modular computer.

7. An I/O function module for plugging into a module bay of a framework for a modular computer, said module bay having a receiving connector with pins connected to individual traces of a bus means within said framework,

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said function module comprising:
a casing for supporting and housing elements of
said function module;
guide means for engaging guides in said module bay
and guiding said function module into and out of said
module bay;
module connector means for engaging said receiving
connector to connect traces within said function module
to said bus means; and
I/O function means mounted within said function
module for performing an I/O function for said modular
computer, said I/O function means connected to said bus
through said module connector means.

8. An I/O function module as in claim 7 wherein said
module is a floppy disk module having a port for
inserting and ejecting a floppy disk, said port
accessible with said floppy disk module engaged in said
module bay, reading and writing means, and a disk
controller configured to operate said floppy disk module
from said bus means

9. An I/O function module as in claim 7 wherein said
module is a hard disk module, having at least one hard
disk, reading and writing means, and a disk controller
configured to operate said hard disk module from said bus
means.

10. An I/O function module as in claim 7 wherein said
module is a RAM memory module, having RAM memory
connectable to and accessible by said bus means with said
RAM memory module plugged into said module bay.

11. An I/O function module as in claim 7 wherein said
module is a LAN module for providing communication
between said modular computer and other computer systems
on a local area network.

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12. An I/O function module as in claim 7 wherein said module is a modem module for providing communication between said modular computer and other computer systems over a telephone connection.

13. An I/O function module as in claim 7 wherein said module is a serial communication module for providing communication between said modular computer and other computer systems over a serial link.

14. An I/O function module as in claim 7 wherein said module is a facsimile module for providing FAX transmission and reception over telephone lines.

15. An I/O module as in claim 7 wherein said module is a specialty module for data acquisition from an instrument, said function module capable of transmitting commands to the instrument over a communication link, receiving data from the instrument, and translating data for transmission on said bus means.

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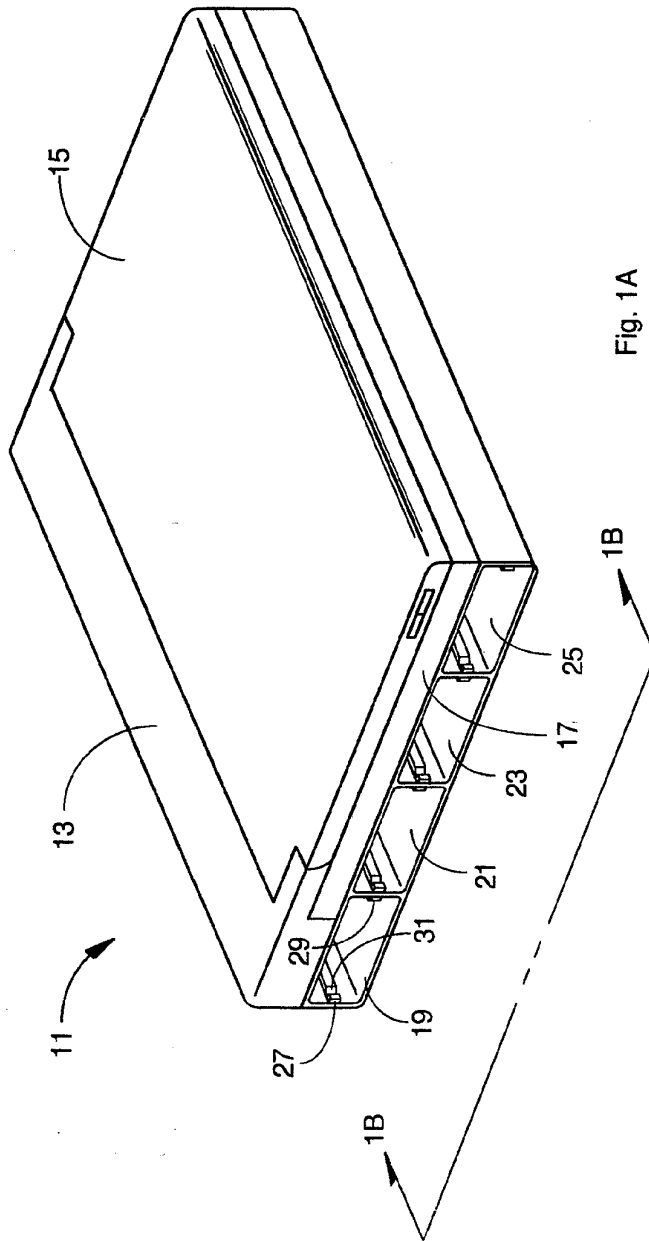


Fig. 1A

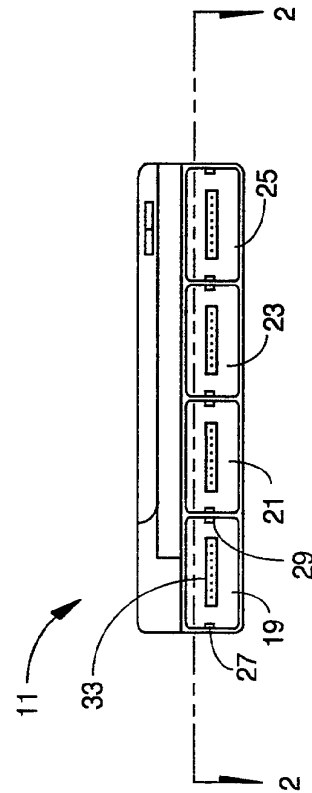


Fig. 1B

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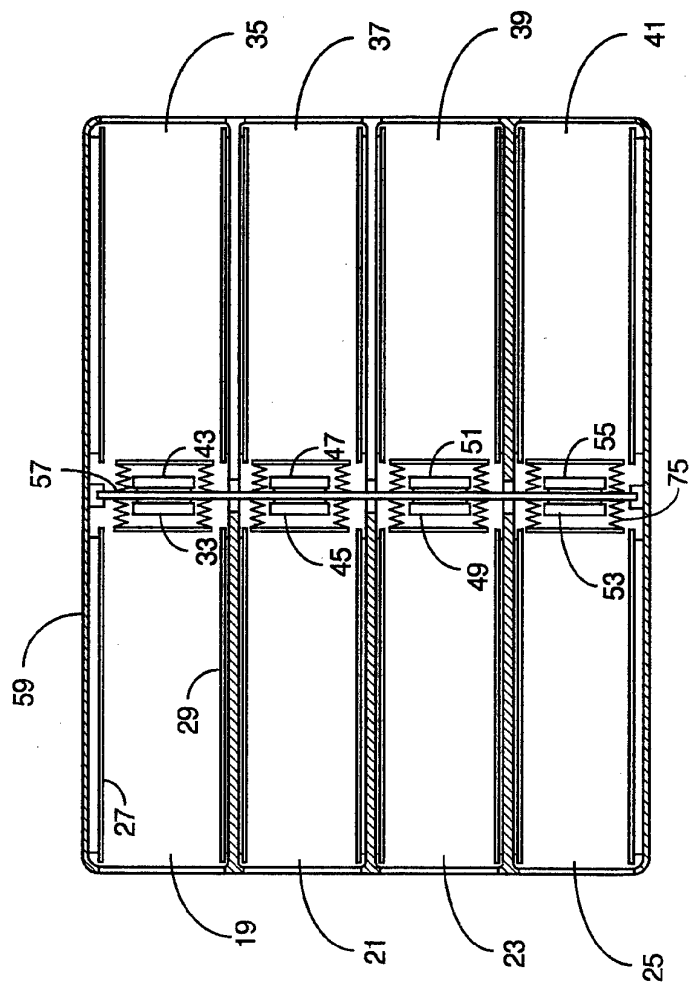


Fig. 2

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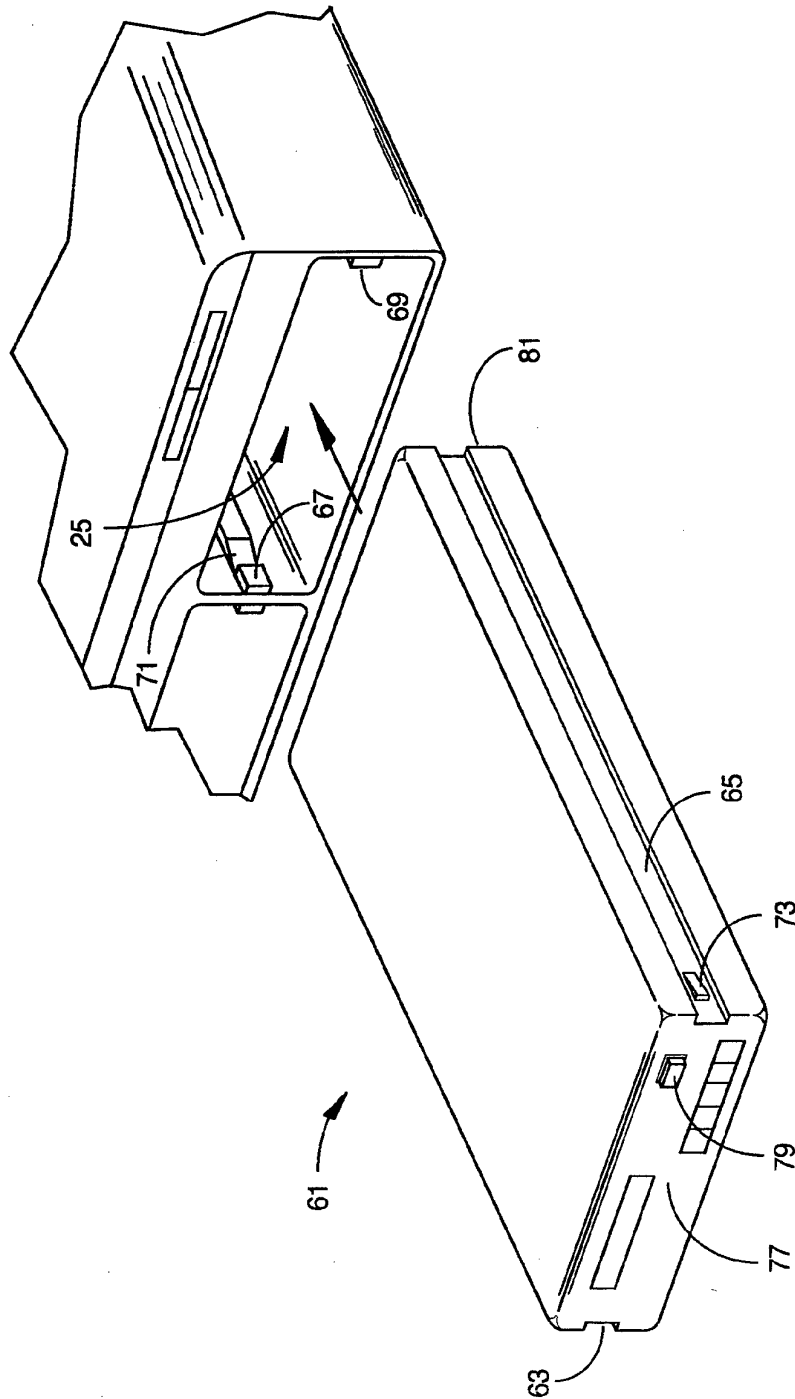


Fig. 3

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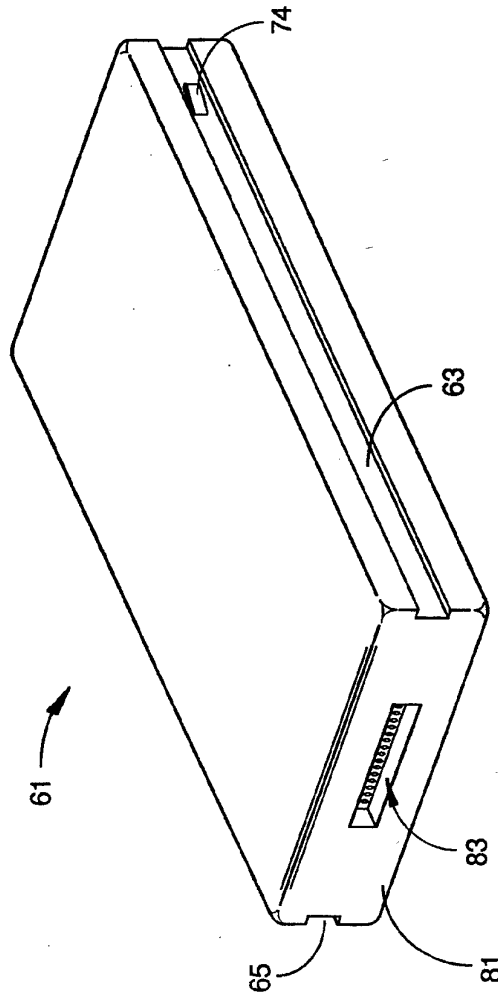


Fig. 4

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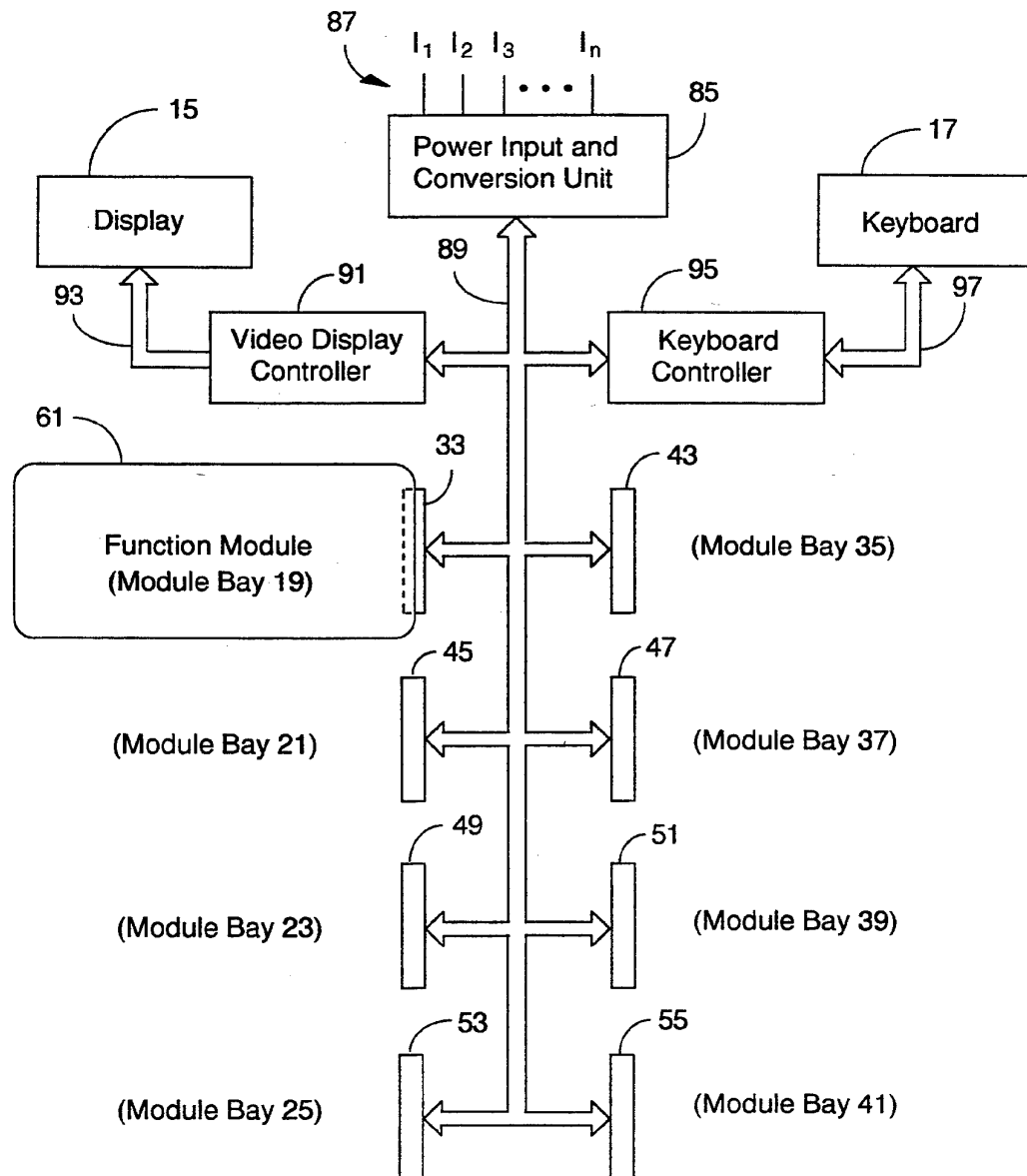


Fig. 5

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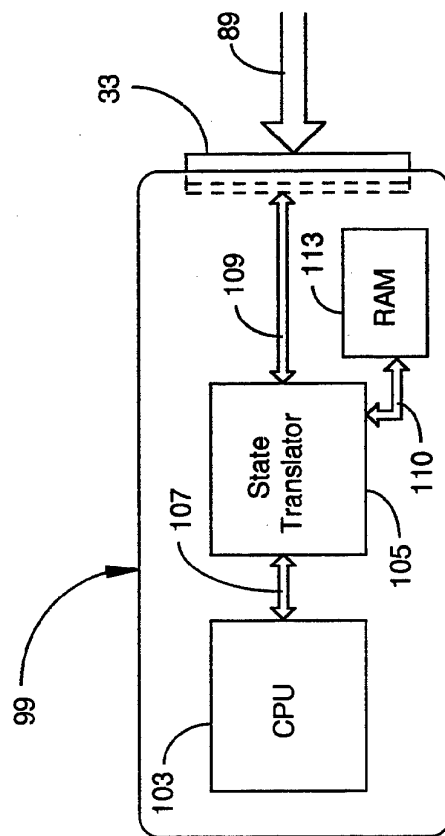


Fig. 6

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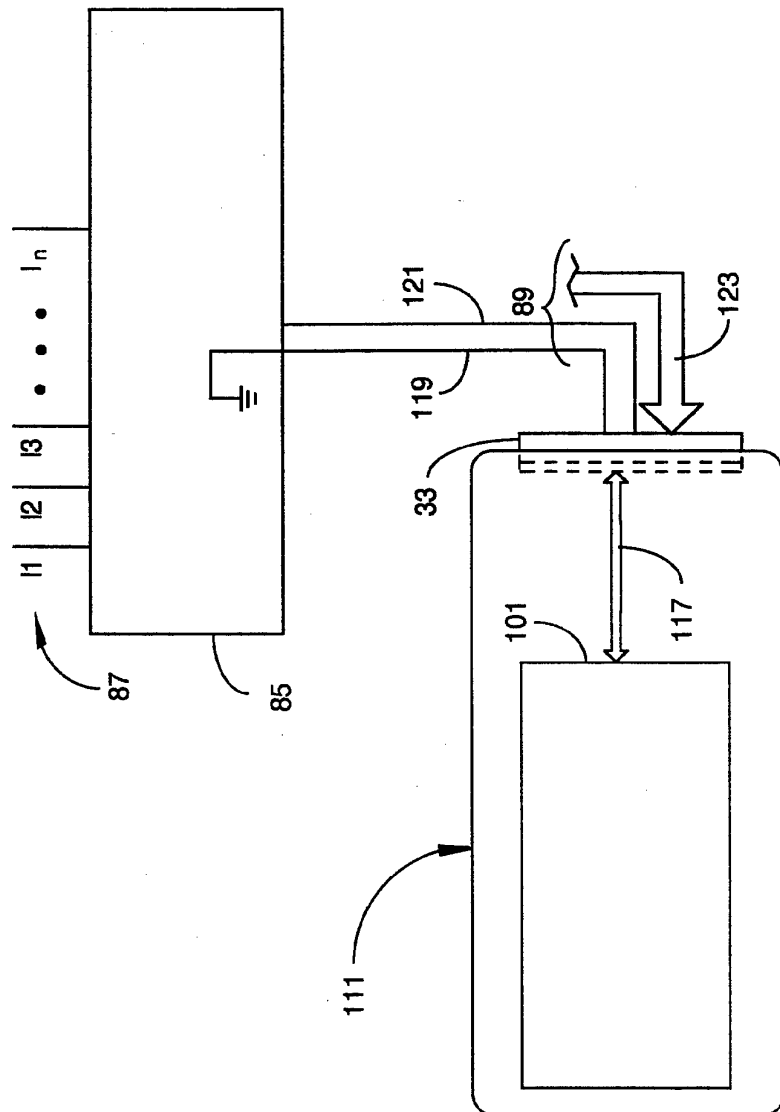


Fig. 7

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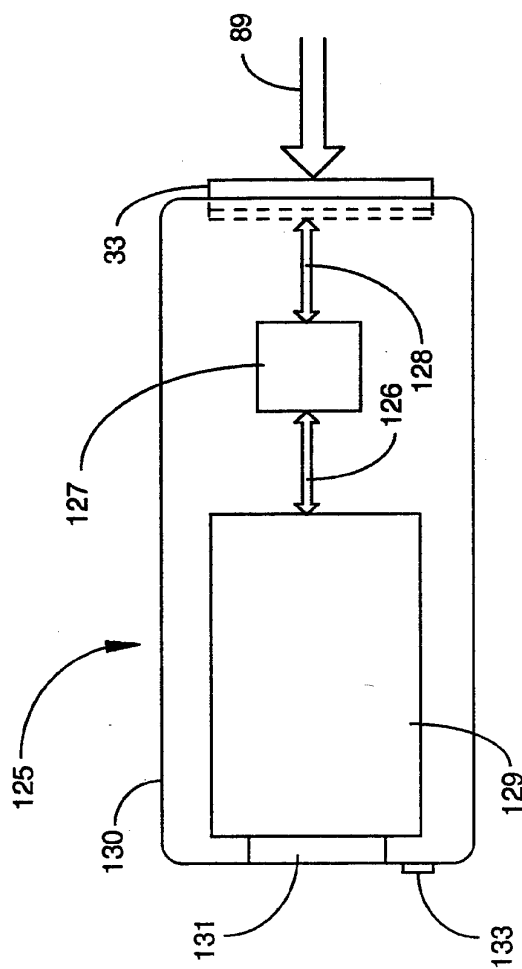


Fig. 8

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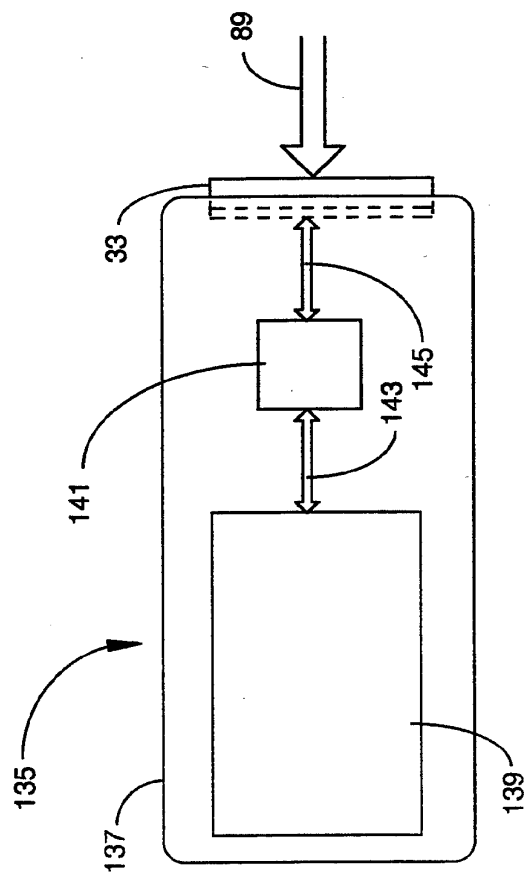


Fig. 9

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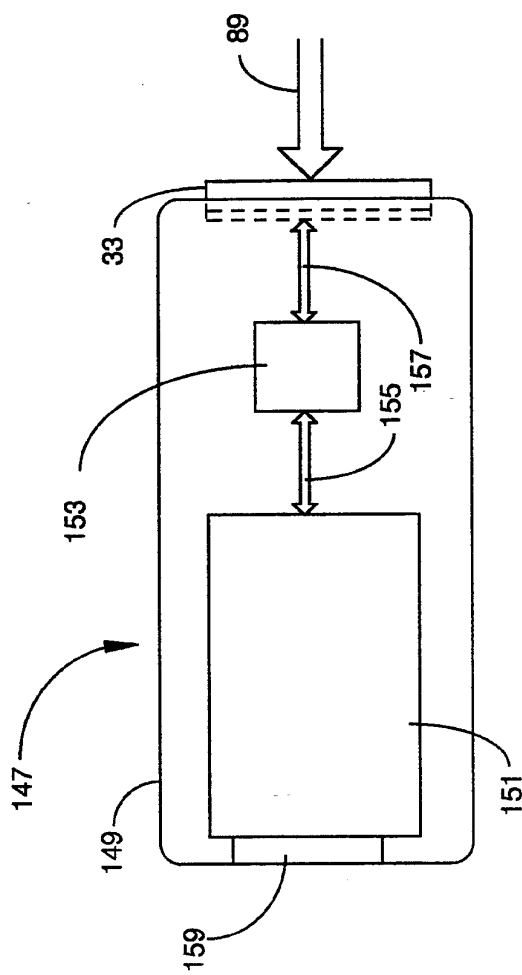


Fig. 10

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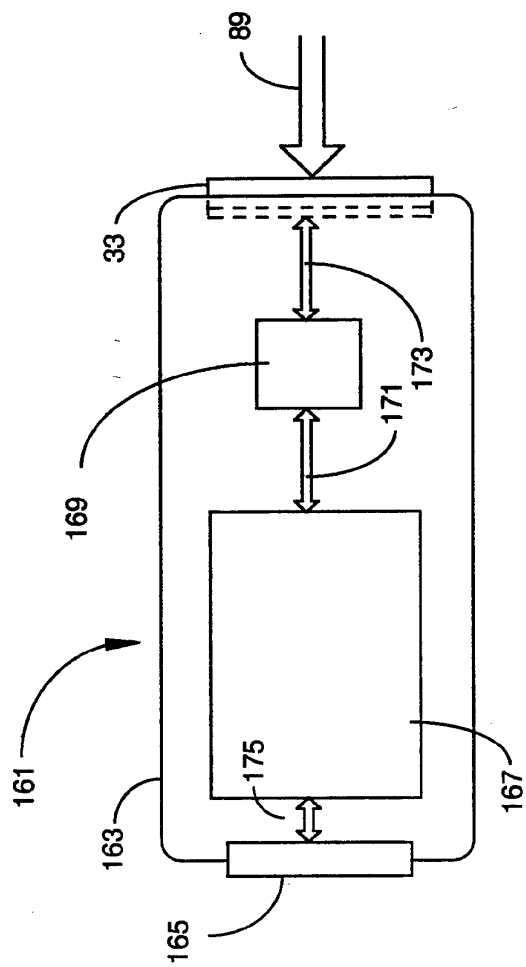


Fig. 11

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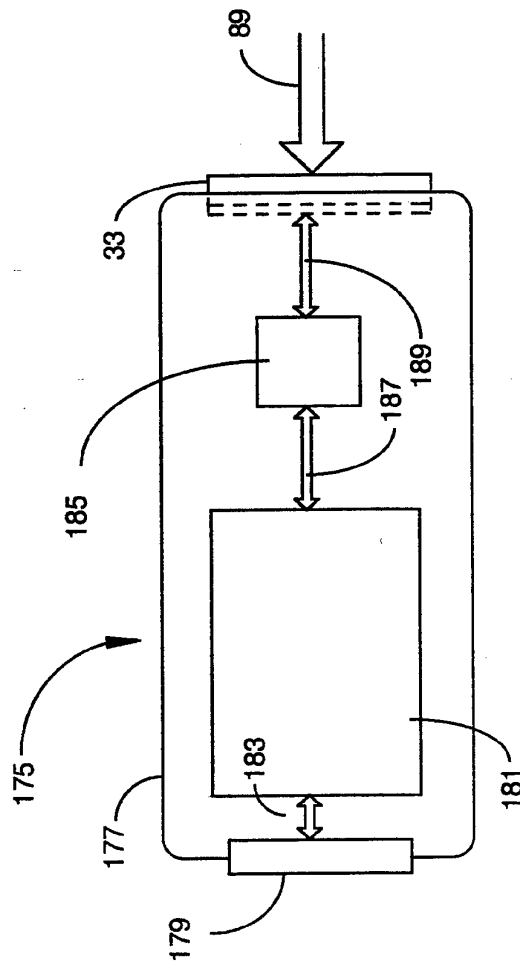


Fig. 12

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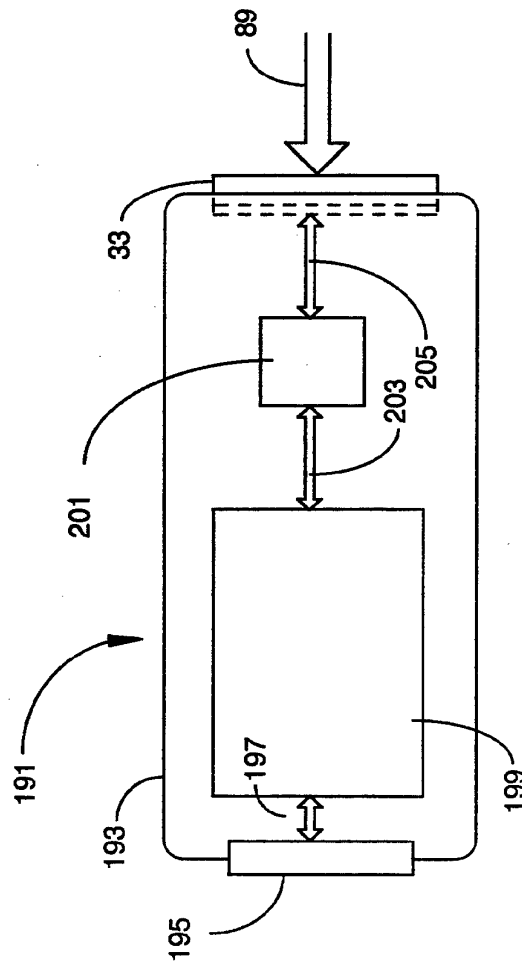


Fig. 13

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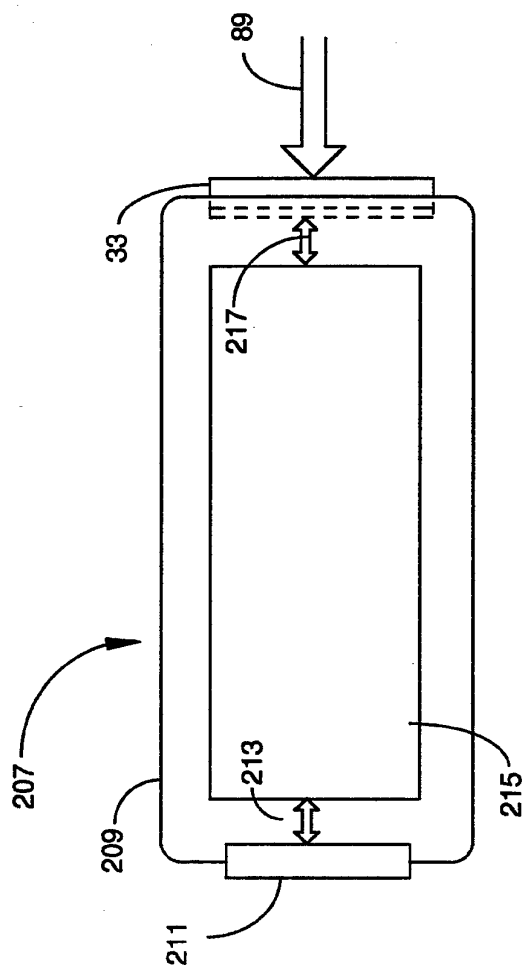


Fig. 14

INTERNATIONAL SEARCH REPORT

International application No.
PCT/US93/06146

A. CLASSIFICATION OF SUBJECT MATTER

IPC(5) : H05K 7/10; G06F 1/16

US CL : 361/395

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)

U.S. : 361/380, 390, 391, 392, 393, 394, 399, 415; 364/708

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
Y	US, A, 4,894,792 (Mitchell et al) 16 January 1990 See the entire document.	1-15
Y	US, A, 4,991,058 (Watkins et al) 05 February 1991, See the entire document.	2
Y	EP, A, 0,387,749 (Skordou et al) 19 September 1990, See the entire document.	2
Y	US, A, 4,680,674 (Moore) 14 July 1987 See the entire document.	2-6

☒ Further documents are listed in the continuation of Box C. ☐ See patent family annex.

* Special categories of cited documents:	*T	later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention
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INTERNATIONAL SEARCH REPORT

International application No.
PCT/US93/06146

C (Continuation). DOCUMENTS CONSIDERED TO BE RELEVANT		
Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
Y	US, A, 4,941,841 (Darden et al) 17 July 1990, See the entire document.	2-15
Y	BYTE, June 1983, pages 150-154, 156, 159, 160, 162, and 164, Wayne Clingingsmith, "A Machine for All Processors".	1-15
A	US, A, 4,530,066 (Ohwaki et al) 16 July 1985, See the entire document.	1-15
A	US, A, 4,926,365 (Hsieh) 15 May 1990, See the entire document.	1-15
Y	"The Siemens Microcomputer Module System SMP 80", November, 1977, components report XII, pages 181-184, Irmfried Bromme.	1-15

Form PCT/ISA/210 (continuation of second sheet)(July 1992)*

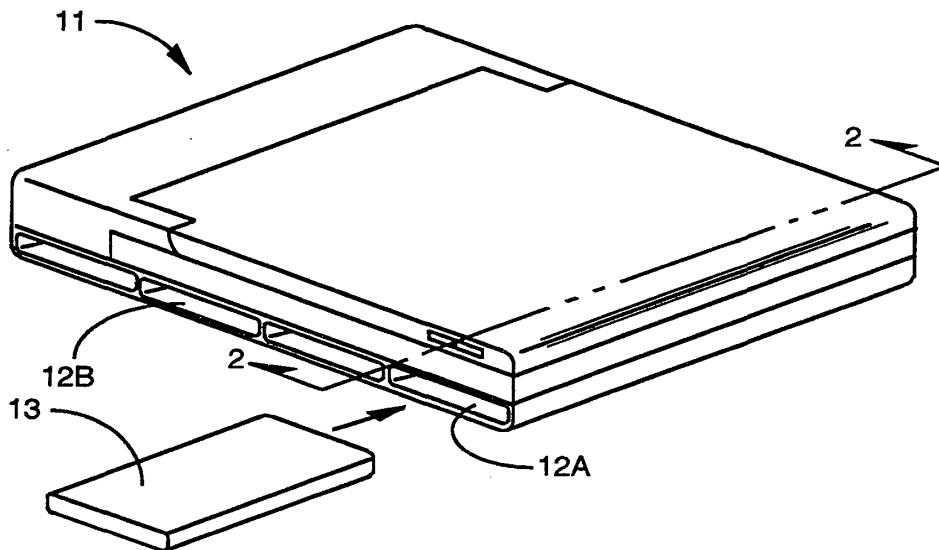


INTERNATIONAL APPLICATION PUBLISHED UNDER THE PATENT COOPERATION TREATY (PCT)

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(21) International Application Number: PCT/US94/13211 (22) International Filing Date: 14 November 1994 (14.11.94) (30) Priority Data: 08/152,431 12 November 1993 (12.11.93) US (71) Applicant: OAKLEIGH SYSTEMS, INC. [US/US]; Suite 110, 430 North Mary Avenue, Sunnyvale, CA 94086 (US). (72) Inventor: KIKINIS, Dan; 20264 Ljepava Drive, Saratoga, CA 95070 (US). (74) Agent: BOYS, Donald, R.; P.O. Box 187, Aromas, CA 95004 (US).		(81) Designated States: CN, JP, European patent (AT, BE, CH, DE, DK, ES, FR, GB, GR, IE, IT, LU, MC, NL, PT, SE). Published <i>With international search report.</i> <i>Before the expiration of the time limit for amending the claims and to be republished in the event of the receipt of amendments.</i>

(54) Title: COOLING A LARGE MICROPROCESSOR IN A SMALL MODULE**(57) Abstract**

A modular computer (11) with docking bays (12A, 12B) for receiving functional modules (13) and connecting the functional modules (13) to internal computer circuitry has translatable heat-sink structures (17, 19) for contacting docked functional modules (13) to extract waste heat generated by operation of the functional modules (13). The structures (17, 19) are mechanically actuated to retract to provide clearance for insertion and withdrawal of functional modules (13), and in some instances, the translation of the heat-sink structures (17, 19) is by electrically operable actuators, which may be actuated by signals from a CPU of the modular computer (11). In these instances, the computer (11) may be configured to require a security code or special input sequence to retract the heat-sink structures (17, 19) allowing a module (13) to be removed.



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Cooling a Large Microprocessor in a Small Module

Field of the Invention

This invention is in the area of portable computers, and pertains more specifically to apparatus and methods for using large microprocessors in small portable computers.

Background of the Invention

Portable computers such as notebooks and palmtops are popular among computer users who travel and need to take their work along. They are smaller and lighter than laptops, and are therefore more portable. It is currently possible to build very small computers, and to provide a great deal of modularity and therefore flexibility in the application of such machines.

It is known to the inventors, for example, to build a palmtop or notebook computer wherein various modules are inserted into bays and make connection therein to a bus structure. In such modular portable computers the modules provide divisible electronic functions. Taken to the extreme, nearly every independent function may be incorporated into a module as a peripheral. In a modular computer of this sort, the framework without the modules may comprise essentially a bus structure and a power conversion unit. Functional modules may include interchangeable CPUs, memory devices of various sorts, system control logic, peripheral communication devices, I/O devices, and more. Also, modules may assume a wide variety of shapes and sizes, such as the well-known Personal Computer Memory Card International Association (PCMCIA) form factor standards.

The modular concept gives the user a choice of functional configurations in one portable computer. For example, while traveling

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a user may require a modem but not a floppy disk drive, and the modular concept lets the user select the functions he/she needs. The modular concept also allows a portable computer to be smaller and more portable than it would be if all the functions that might be needed have to be incorporated. Size is a very competitive criterion in commanding market share. The evolution to smaller and lighter modular computers, however, is not without problems.

One of the problems in such a modular computer is dissipating heat from the individual modules. Incorporation of a CPU module into portable computer architecture is very desirable, because it provides ability to tailor the CPU power to other modules and software applications. It also allows a computer owner to upgrade to more powerful CPUs as they become available. However, incorporating a large microprocessor in a module configured for a modular portable computer creates a significant concentration of heat to dissipate.

Heat generation by large microprocessors in functional modules is so great that a prudent approach to packaging is imperative. Also, the conventional approaches of cooling fans and the like are solutions that pose an additional burden in the design of portable computers, requiring more space and larger power supplies. In addition, high running temperature degrades computer performance and can lead to failure. Manufacturers that do not address thermal implications that directly affect CPU performance risk premature microprocessor failures. An overheated CPU can cause various problems, ranging from data corruption to the loss of file-allocation tables to the microprocessor shutting itself down.

It is likely that future trends in development will result in faster, hotter microprocessors, which will require ever more efficient ways to transfer heat to the surroundings. As one example, Intel's

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new Pentium™, scheduled to succeed the 486 family of microprocessors, has about 3 million transistors, producing heat at a high rate, which, if not disposed of properly, can limit chip performance. It is estimated the Pentium CPU will generate as much as 16 watts during operation.

Intel has established a certification procedure with microcomputer manufacturers to qualify general-purpose computers for safe Pentium use, and few manufacturers have enough cooling for full certification. And the contemplated use of these devices in functional modules and other electronic devices for use in portable computers will require extraordinary efforts to remove waste heat.

The present invention addresses the above-described problems particularly pertaining to use of high-performance microprocessors in modular, portable general-purpose computers. What is needed is a method of removing CPU-generated waste heat economically and effectively within the small confines of a modular, portable computer, guaranteeing optimal processing performance, longevity and reliability.

Summary of the Invention

In an embodiment of the present invention, a computer having a docking bay for receiving a functional module has a module cooling system comprising a heat-sink structure within the docking bay for contacting and cooling a functional module in docked position, and a translation means for moving the heat-sink structure against a module in docked position to accomplish heat absorption from the module. In various embodiments, heat-sink structures have a flexible, heat-conductive interface for conforming intimately to modules, and special shapes to securely retain docked modules. In embodiments with

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electrically operable actuators, the computer may be configured to require a special input sequence or other security code to release a module for removal from a docking bay.

Cooling apparatus and methods according to embodiments of the present invention provide for efficiently removing heat from functional modules configured to be added to a compatible computer structure. By providing efficient cooling, full operating potential of modules, particularly modules having high-performance microprocessors, may be ensured.

Brief Description of the Drawings

Fig. 1 is an isometric view of a modular, portable general-purpose computer, showing a function module in position for docking.

Fig. 2A is a cross-sectional view along line 2-2 of Fig.1 showing one module docking bay in a modular computer having disengaged cooling elements according to an embodiment of the invention.

Fig. 2B is a side elevation view of a portion of one cooling structure, guided on vertical guide pins with extension springs, and operated by a movable cam bar.

Fig. 3 is another cross-sectional view along line 2-2 on Fig.1 showing the cooling elements engaged.

Fig. 4 is a cross-sectional view similar to Fig.2 showing cooling elements with locking means incorporated into the elements.

Fig. 5 is a cross-sectional similar to Fig. 4 showing the cooling elements engaged.

Fig. 6 is a cross-sectional view similar to Fig. 5 showing opposing cooling elements with locking means, each having a layer of compressible heat-conducting material facing the module.

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Fig. 7 is a cross-sectional view immediately inside two adjacent bays in a plane parallel to the openings of the bays in the embodiments described.

Description of the Preferred Embodiments

Fig. 1 is an isometric view of a portable general-purpose computer framework 11 according to an embodiment of the present invention. There are, along two sides of framework 11, a series of docking bays such as bays 12A and 12B configured to receive function modules 13. The modules are configured to provide functional characteristics for the computer system as described above. More particularly, modules are expected to be used comprising microprocessors and the like that generate considerable waste heat. A representative functional module 13 is shown in position to be inserted in bay 12a.

Fig. 2A is a cross-sectional view of docking bay 12A in the direction of arrows 2-2 of Fig. 1, showing function module 13 inserted into docking bay 12A, engaging a connector 15 which provides electrical connection to an internal bus structure. Cooling structures 17 and 19 shown above and below module 13 are, in this embodiment, heat absorbent and conductive plates made of highly heat-conductive and heat absorbent material, such as copper. Cooling structures 17 and 19 are spaced apart from the inserted position of a module by a distance above and below the line of insertion and withdrawal, such that they do not interfere with inserting or withdrawing of a module.

The placement and size of cooling structures 17 and 19 may vary widely, depending on configuration of the system, including the dimensions of modules accommodated in the docking bays. Also,

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although two opposing cooling structures 17 and 19 are shown in this embodiment, in other embodiments there may be only one, either above or below the docking position of a module in the docking bay.

To actively cool a module in a docking bay, the cooling structures must be brought into intimate contact with the module. There are a number of equivalent ways this may be done.

Fig. 2B is a side elevation view of a portion of one cooling structure 17 in an embodiment of the invention, wherein structure 17 is guided on three or more vertical guide pins. Two guide pins 16 and 18 are shown, in this case fastened through and to structure 17. Fastening may be by soldering, welding, screw threads, or by other conventional means.

Pins 16 and 18 in this embodiment pass through guide bores 20 and 22 in an upper wall structure 24 of the particular docking bay, and extend into an enclosure above wall 24. Extension springs 32 and 34 are placed in assembly to urge structure 17 away from wall 24 (toward the position of a functional module docked in the docking bay).

Each of pins 16 and 18, and others not shown, have a longitudinal slot, such as slots 26 and 28, for passage of a cam bar 30. Cam bar 30 is translatable at right angles to pins 16 and 18, and is shaped with risers and plateaus, as is known in the mechanical arts, to retract and extend pins 16 and 18, and therefore structure 17.

Cam bar 30 may be activated (translated) in a number of different ways. In the embodiment shown, cam bars in each module bay are connected to a slide lever (not shown) configured on an edge of the external case of the modular computer. Once functional modules are in place, a user may activate the external lever to engage the cooling structures. In the case of cooling structures both above and below the position of a functional module in a bay, there may be

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additional cam bars and guide pin structures for the lower structures as well as for the upper structures.

It will be apparent to those with skill in the art that there are many other mechanical systems useful to move cooling structures in the manner required to engage docked function modules. Rotary cams may be used, for example, instead of the cam bars described, and there are many ways external levers, slides, and the like may be implemented to actuate the cam devices and engage the cooling structures. The mechanisms described herein are exemplary.

In another embodiment, activation of the cooling structures may be accomplished by a mechanism moved in the last portion of the translation of a module into a module bay. Such mechanisms are well known in the art. In this case a user-operable linkage is made available to disengage cooling structures 17 and 19 so modules may be removed.

Cooling structures 17 and 19 are activated in some embodiments by electrically operable actuators, such as solenoids, motors, and the like, to close automatically on insertion of a function module. This activation configuration is particularly useful for maximum security. In these embodiments control routines operable on the modular computer cause the actuators to operate. The control routines in some embodiments require a user to enter a code at the keyboard or other input to operate the actuators to engage and disengage. In other embodiments actuation is accomplished by the system BIOS as a part of startup procedures.

Control routines may also include password protection as a means of security. In yet another embodiment, actuators are signalled by control routines available via a CPU function module after insertion. In this case, the CPU function module is first inserted and powered-up through established bus protocols. Machine control

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routines that control cooling structure engagement then initiate the modular computer's mechanized framework.

It will be apparent to those with skill in the art that there are a wide variety of ways that control routines may be implemented to provide actuation of mechanisms for moving cooling structures to engage function modules.

Fig. 3 is an elevation view similar to Fig. 2, showing cooling structures 17 and 19 engaged, urged against functional module 13. The support and engagement mechanisms are not shown in Fig. 3. In this intimate engagement, waste heat generated by module 13 may be readily absorbed by cooling structures 17 and 19.

It is preferred that the cooling structure or structures urged against a functional module be configured to aid in retaining the module in position in the docking bay. Besides providing a means of retaining modules against accidental displacement, structures configured for retention may also provide security for expensive modules.

Fig. 4 is a side view similar to Fig. 2 showing cooling structures 36 and 38 having extensions 40 and 42 respectively configured to retain a function module when the function modules are engaged. In the disengaged position shown in Fig. 4, cooling structures 36 and 38 are capable of being disengaged (retracted) a sufficient amount that extensions 40 and 42 do not interfere with docking procedures.

Fig. 5 is similar to Fig. 4, except cooling structures 36 and 38 are extended to engage function module 13, such that extensions 40 and 42 prevent the function module from being withdrawn while the cooling structures are engaged. Extensions 40 and 42 may be configured to move a function module to a final position fully engaging connector 15.

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In the embodiments described above the cooling structures are heat sinks fashioned as plates of heat absorbing and conducting material. In another embodiment the cooling structures are Peltier devices. They may take other forms as well. The size and design of heat sinks may differ in specific docking bays to accommodate particular modules, which will vary in waste heat production according to the function of the module. CPU modules, for example, are expected to be the worst offenders in generating waste heat. In many cases a modular computer will need no more than one cooled docking bay, that bay reserved for the CPU module.

Fig. 6 shows cooling structures 36 and 38 having a layer of compressible heat-conducting material 27 such as Chomerics (TM) aluminum oxide-filled rubber or flexible polymer. In this aspect of the invention a pad of such material is mounted by a heat-resisting adhesive to each cooling structure. In this aspect of the invention, the heat-conducting layered material compresses against the inserted function module. A more continuous thermal contact is made ensuring efficient heat conduction across the interface between the function module and the cooling structure. In an alternative embodiment, the compressive material may be affixed to the corresponding sides of the computer module.

Figure 7 is a cross-sectional view immediately inside two adjacent bays 12A and 12B in Fig. 1 in a plane parallel to the openings of the bays. Module bay opening 12A is an end bay while 12B is an interior bay. Module 13 is shown in some intermediate stage of insertion. Cooling structures 17 and 19 are shown in the full open or some intermediate stage of closing. In this aspect of the embodiment, cooling structures 17 and 19 close to secure function module 13 and to contact an interconnected bus system of additional thermal-conducting structures 33 and 31. The distances D1 and D2

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are approximately equal, making a thermal loop between occupied docking bays and other internal conducting structures when opposing cooling structures close.

Within all regions of common contact between the moving and stationary heat sinks the mating surfaces are covered in this embodiment with a compressible heat-conducting material to ensure continuous thermal contact between adjacent surfaces. Conducting structure 31 is exposed to the outside air and may be a structural part of the portable computer's case. Conducting structure 31 may ring the entire outside perimeter of the case and may also interconnect to the interior heat-sink bus shown as conducting structure 33. The interior heat-sink bus in this embodiment is an integral part of the supporting framework of the portable computer.

Surfaces 53A, 53B, and 53C may be shaped to maximize heat transfer to the outside air via radiation and convection, such as by grooves or fins. In another embodiment, the heat-sink bus or any individual heat-conducting structure may be connected via a heat conduction interface to an outside heat transferring device, apparatus or structure. For example, at any point along surfaces 53A, 53B and 53C a larger heat sink may be attached in a way to further conduct heat away from the interior of the computer.

It will be apparent to one skilled in the art that there are a relatively large number of changes that can be made in the embodiments described without departing from the spirit and scope of the present invention. Some of these alternatives have already been described, such as the incorporation of an interconnecting heat-sink bus system, and the many ways that actuating mechanisms may be configured. There are similarly many dimensional changes and variations in materials that may be incorporated within the spirit and scope of the invention.

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What is claimed is:

1. In a computer having a docking bay for receiving a functional module, a module cooling system comprising:
a heat-sink structure within the docking bay for contacting and cooling a functional module in docked position; and
translation means for moving the heat-sink structure against a module in docked position to accomplish heat absorption from the module.
2. A module cooling system as in claim 1 wherein the docking bay is configured to dock a functional module fashioned according to a PCMCIA standard.
3. A module cooling system as in claim 1 wherein the heat-sink structure is a substantially flat metal cooling plate.
4. A module cooling system as in claim 1 further comprising a layer of flexible, heat-conducting material affixed to the heat-sink structure for providing a conformal interface between the heat sink structures and a docked functional module.
5. A module cooling system as in claim 1 wherein the translation means comprises mechanical means for translating the heat-sink structure, including a lever operable by a user to translate the heat-sink structure.
6. A module cooling system as in claim 1 wherein the translation means comprises mechanical means for translating the heat-sink

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structure, and the mechanical means is operated by an electrically operable actuator.

7. A module cooling system as in claim 6 wherein the electrically operable actuator is responsive to electrical signals initiated by a CPU.

8. A computer system comprising:

a docking bay for docking a functional module;

a heat-sink structure within the docking bay movable to a position to contact any functional module docked; and

translation means for moving the heat-sink structure against a module in docked position to accomplish heat absorption from the module.

9. A computer system as in claim 8 wherein the docking bay is configured to dock a functional module fashioned according to a PCMCIA standard.

10. A computer system as in claim 8 wherein the heat-sink structure is a substantially flat metal cooling plate.

11. A computer system as in claim 8 further comprising a layer of flexible, heat-conducting material affixed to the heat-sink structure for providing a conformal interface between the heat-sink structure and a functional module.

12. A computer system as in claim 8 wherein the translation means comprises mechanical means for translating the heat-sink structure, including a lever operable by a user to translate the heat-sink structure.

- 13 -

13. A computer system as in claim 8 wherein the translation means comprises mechanical means for translating the heat sink structure, and the mechanical means is operated by an electrically operable actuator.

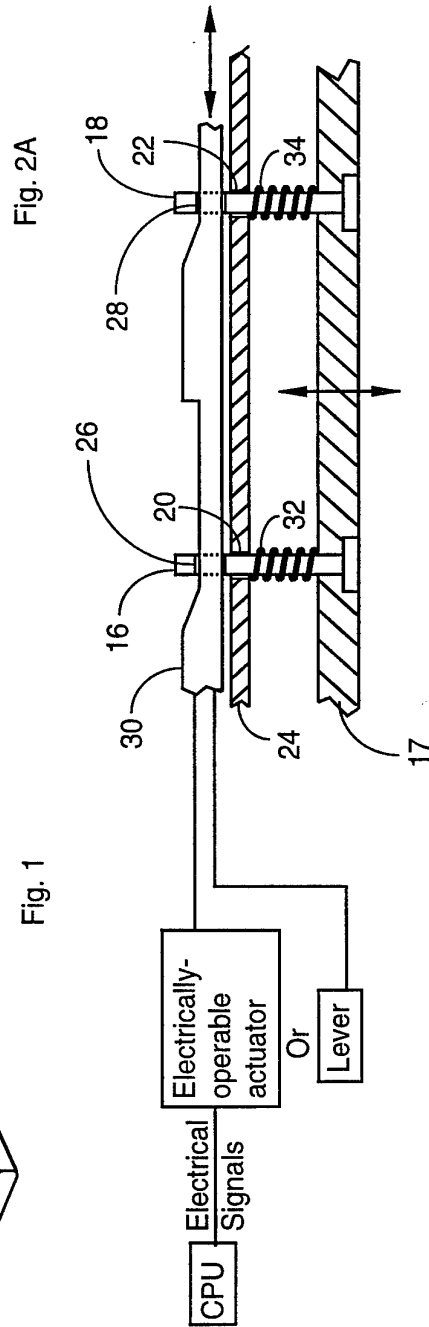
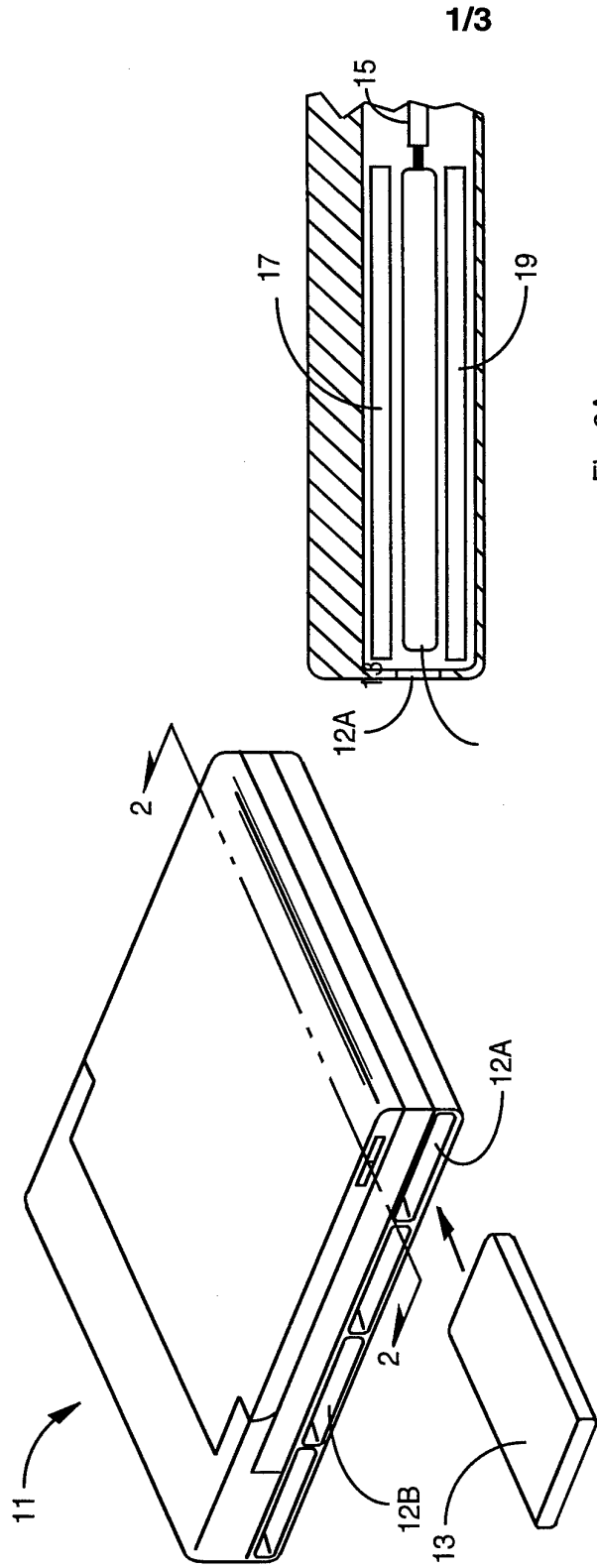
14. A computer system as in claim 13 wherein the electrically operable actuator is responsive to electrical signals initiated by a CPU.

15. A computer system as in claim 14 wherein the translation means is configured to require a pre programmed security code to enable translation of the heat-sink structure away from a docked module.

16. A computer system as in claim 8 wherein the heat-sink structure is configured to retain a docked module in docked position with the heat-sink structure in contact with the module.

17. A method for cooling a functional module in a docking bay of a modular computer comprising the steps of:

- docking the functional module in the module bay;
- advancing a heat-sink structure into contact with the functional module; and
- extracting heat from the functional module into the heat-sink structure.



2/3

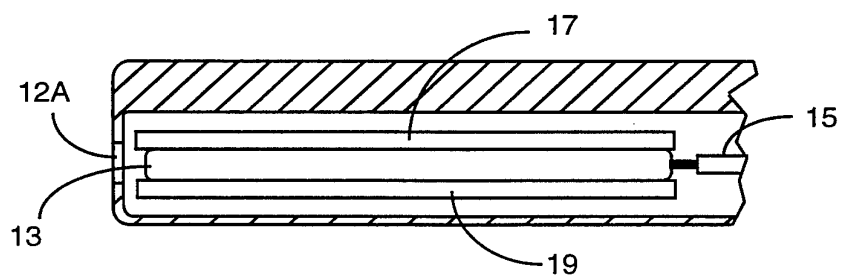


Fig. 3

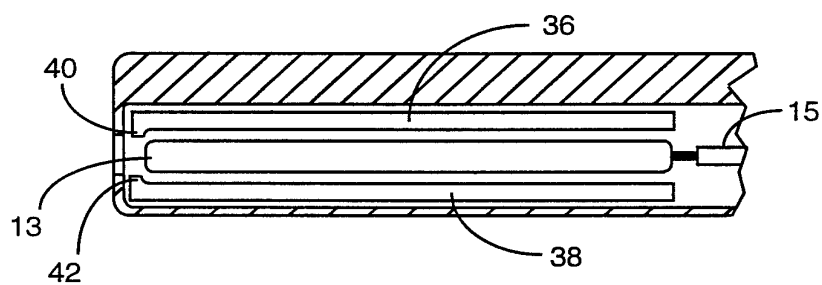


Fig. 4

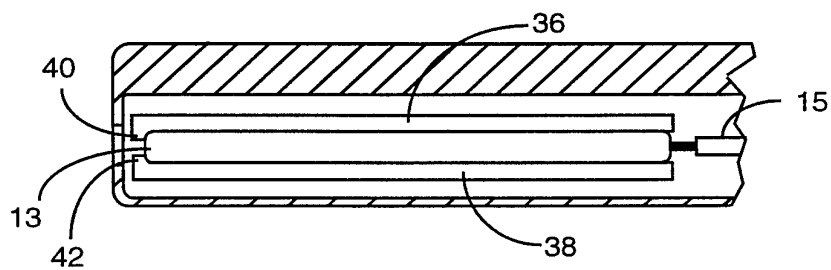


Fig. 5

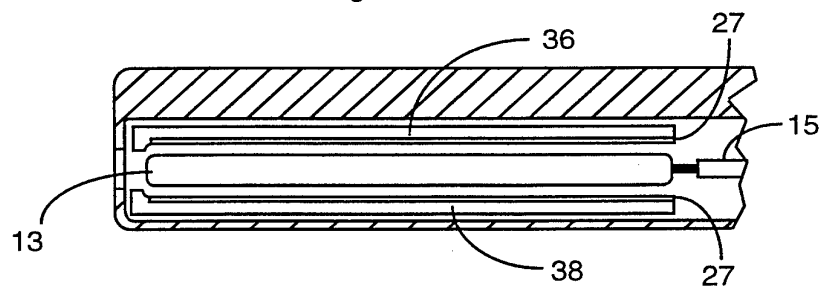


Fig. 6

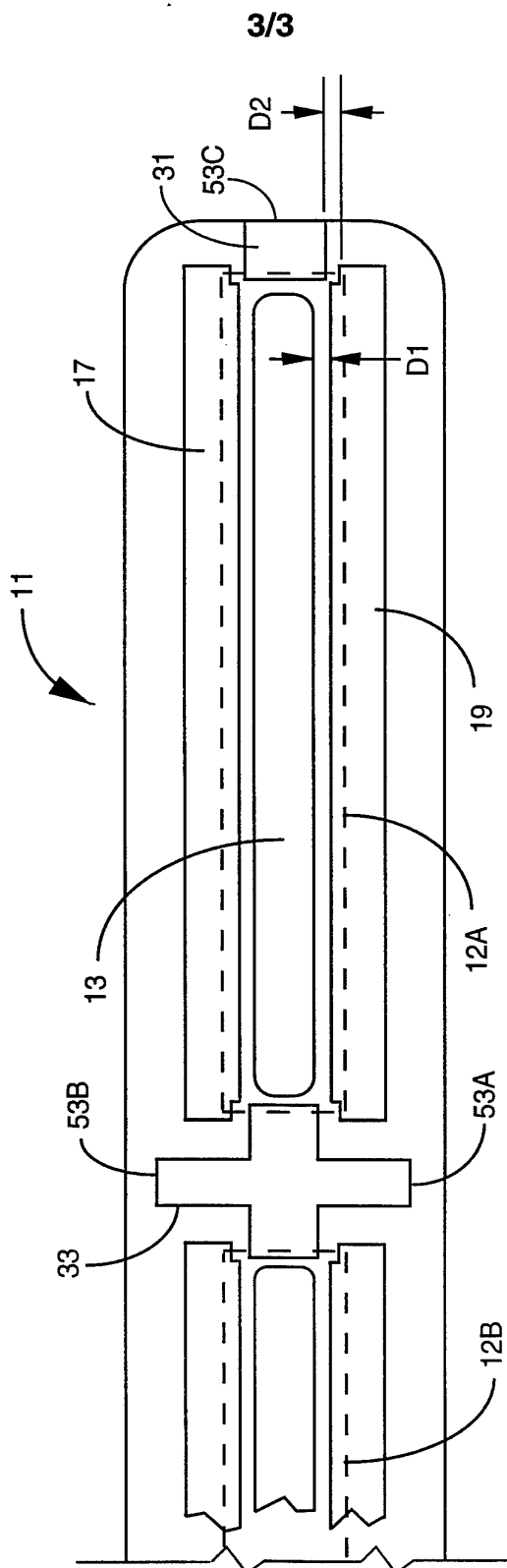


Fig. 7

INTERNATIONAL SEARCH REPORT

International application No.
PCT/US94/13211**A. CLASSIFICATION OF SUBJECT MATTER**

IPC(6) :H02B 1/00; H05K 7/20

US CL :257/718; 361/687, 704, 710

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)

U.S. : 174/16.3; 165/80.3, 185; 257/718-719, 726-727; 361/687-690, 704, 707-711, 720

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X -- Y	US, A, 4,825,337 (KARPMAN) 25 April 1989, see entire document.	1-5,8-12, 16-17 ----- 6-7,13-15

☐

Further documents are listed in the continuation of Box C.

☐

See patent family annex.

•

Special categories of cited documents:

"T"

later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention

A

document defining the general state of the art which is not considered to be of particular relevance

"X"

document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone

E

earlier document published on or after the international filing date

L

document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)

"Y"

document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art

O

document referring to an oral disclosure, use, exhibition or other means

P

document published prior to the international filing date but later than the priority date claimed

&

document member of the same patent family

Date of the actual completion of the international search

21 FEBRUARY 1995

Date of mailing of the international search report

06 MAR 1995

Name and mailing address of the ISA/US
Commissioner of Patents and Trademarks
Box PCT
Washington, D.C. 20231

Authorized officer

THOMPSON, GREG

Facsimile No. (703) 305-3230

Telephone No. (703) 308-2249

Form PCT/ISA/210 (second sheet)(July 1992)*

Electronic Patent Application Fee Transmittal				
Application Number:				
Filing Date:				
Title of Invention:		Data Security Method and Device for Computer Modules		
First Named Inventor/Applicant Name:		William W. Y. Chu		
Filer:		William S. Galliani/Bobbie Jutras		
Attorney Docket Number:		ACQI-006/05US 310578-2072		
Filed as Large Entity				
Reissue (Utility) Filing Fees				
Description	Fee Code	Quantity	Amount	Sub-Total in USD(\$)
Basic Filing:				
Utility Reissue Basic	1014	1	380	380
Design and utility Reissue Basic	1114	1	620	620
Design and utility Reissue Basic	1314	1	750	750
Pages:				
Claims:				
Reissue claims in excess of 20 for large	1205	21	60	1260
Independent claims reissue large	1204	9	250	2250
Miscellaneous-Filing:				

Description	Fee Code	Quantity	Amount	Sub-Total in USD(\$)
Petition:				
Patent-Appeals-and-Interference:				
Post-Allowance-and-Post-Issuance:				
Extension-of-Time:				
Miscellaneous:				
Total in USD (\$)				5260

Electronic Acknowledgement Receipt	
EFS ID:	13377173
Application Number:	13562210
International Application Number:	
Confirmation Number:	1045
Title of Invention:	Data Security Method and Device for Computer Modules
First Named Inventor/Applicant Name:	William W. Y. Chu
Customer Number:	58249
Filer:	William S. Galliani/Bobbie Jutras
Filer Authorized By:	William S. Galliani
Attorney Docket Number:	ACQI-006/05US 310578-2072
Receipt Date:	30-JUL-2012
Filing Date:	
Time Stamp:	20:38:44
Application Type:	Reissue (Utility)

Payment information:

Submitted with Payment	yes
Payment Type	Deposit Account
Payment was successfully received in RAM	\$ 5260
RAM confirmation Number	7181
Deposit Account	501283
Authorized User	
<p>The Director of the USPTO is hereby authorized to charge indicated fees and credit any overpayment as follows:</p> <p>Charge any Additional Fees required under 37 C.F.R. Section 1.16 (National application filing, search, and examination fees)</p> <p>Charge any Additional Fees required under 37 C.F.R. Section 1.17 (Patent application and reexamination processing fees)</p>	

File Listing:					
Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1	Transmittal Reissue Application	ACQI-006-05US_07-30-12_ReissueTransmittal.pdf	55648	no	1
			74242ec3b8e44b109ace8ed532edaa4e87033d4c		
Warnings:					
Information:					
2		6643777.pdf	232273	yes	16
			636564741caf0ec2e39dde5bc301e1b7a0e03113		
	Multipart Description/PDF files in .zip description				
	Document Description		Start	End	
	Abstract		1	1	
	Drawings-only black and white line drawings		2	9	
	Specification		10	15	
	Claims		16	16	
Warnings:					
Information:					
3		ACQI-006-05US_07-30-12_PreliminaryAmd.pdf	174341	yes	25
			82a5ee20e6a63a4e03b5a5e7481935acce02ec9a		
	Multipart Description/PDF files in .zip description				
	Document Description		Start	End	
	Preliminary Amendment		1	1	
	Drawings-only black and white line drawings		2	2	
	Specification		3	15	
	Claims		16	23	
	Applicant Arguments/Remarks Made in an Amendment		24	25	
Warnings:					
Information:					
4	Drawings-only black and white line drawings	ACQI-006-05US_07-30-12_PreliminaryAmdFigs.pdf	5503812	no	16
			20c5146b212216061018d770028abede711ef17f		

Warnings:					
Information:					
5	Oath or Declaration filed	ACQI-006-05US_07-30-12_Reiss ueDeclaration.pdf	734368 25e531d01ac1c015be4ee57e962bb76222 c613c	no	2
Warnings:					
Information:					
6	Power of Attorney	ACQI-006-05US_07-30-12_POA. pdf	306055 54f7ab30f6e358f5836eebca1e007c54c7c8f 55e	no	2
Warnings:					
Information:					
7	Consent of Assignee accompanying the declaration	ACQI-006-05US_07-30-12_Reiss ueConsentOfAssignee.pdf	321702 1c7f4983e90faf5f23e3ad04237179d1cd8 2fef	no	1
Warnings:					
Information:					
8	Assignee showing of ownership per 37 CFR 3.73(b).	ACQI-006-05US_07-30-12_373 bStatement.pdf	372482 e8c0b1060ec28d6cf16ca0d255cb6d48407 b651c	no	1
Warnings:					
Information:					
9	Transmittal Letter	ACQI-006-05US_07-30-12_IDS. pdf	32344 5d025689fa89712b94f12fadf17ab7f52646 d671	no	2
Warnings:					
Information:					
10	Information Disclosure Statement (IDS) Form (SB08)	ACQI-006-05US_07-30-12_IDSL istOfReferences.pdf	187369 60f20edfcf5f07eef17a746a2432fb5b08027 da4	no	5
Warnings:					
Information:					
This is not an USPTO supplied IDS fillable form					
11	Foreign Reference	EP0722138.pdf	775964 2c1544896891a9042d1cb3e393781698fe8 bd2c	no	12
Warnings:					
Information:					
12	Foreign Reference	JP6-289953.pdf	201953 0f46e9296fafbd6d32da720221b148b54c02 5ca8	no	7
Warnings:					
Information:					

13	Non Patent Literature	NPL-Boosten.pdf	126906 b68fc690ec94087a5d760dd0cc3e59866e862fdd	no	2
Warnings:					
Information:					
14	Foreign Reference	WO9218924.pdf	2296842 e1c8239c01c31f87456b9095fa9b2c17d53423ca	no	16
Warnings:					
Information:					
15	Foreign Reference	WO9400970.pdf	1248487 b0c0cec9c157ee61a9b49985f7996a7ab2abcl1c	no	41
Warnings:					
Information:					
16	Foreign Reference	WO9513640.pdf	693128 102d1efe700db56997cb0ff16a8c5a619ef6ee57	no	19
Warnings:					
Information:					
17	Fee Worksheet (SB06)	fee-info.pdf	38238 9b7d081ad19a67cce6ecc9e34881bb078641b064	no	2
Warnings:					
Information:					
Total Files Size (in bytes):			13301912		
<p>This Acknowledgement Receipt evidences receipt on the noted date by the USPTO of the indicated documents, characterized by the applicant, and including page counts, where applicable. It serves as evidence of receipt similar to a Post Card, as described in MPEP 503.</p> <p><u>New Applications Under 35 U.S.C. 111</u> If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application.</p> <p><u>National Stage of an International Application under 35 U.S.C. 371</u> If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.</p> <p><u>New International Application Filed with the USPTO as a Receiving Office</u> If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.</p>					

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of: William W. Y. Chu Confirmation No.: To be assigned

Serial No.: To be assigned

Filed: Herewith

For: DATA SECURITY METHOD AND DEVICE FOR COMPUTER MODULES

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

**POWER BY ASSIGNEE
AND STATEMENT UNDER 37 C.F.R. §3.73(b)**

The Assignee of the entire right, title, and interest in the above-identified application hereby grants the registered practitioners of Cooley LLP included in the Customer Number provided below power to act, prosecute, and transact all business in the U.S. Patent and Trademark Office in connection with this application, any applications claiming priority to this application, and any patents issuing therefrom.

The Assignee certifies that to the best of its knowledge and belief it is the owner of the entire right, title, and interest in and to the above-identified application as evidenced by:

- ☐ An assignment document, a copy of which is enclosed herewith and is being recorded with the U.S. patent and Trademark Office concurrently herewith;
- ☒ An assignment previously recorded in the U.S. Patent and Trademark Office on November 1, 2011 at Reel 027154, Frame 0398.

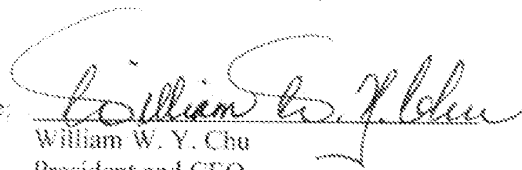
Please direct all telephone calls and correspondence to:

CUSTOMER NUMBER: **58249**

COOLEY LLP
ATTN: Patent Group
777 6th Street NW, Suite 1100
Washington, DC 20001
Tel: (650) 843-5622 | Fax: (202) 842-7899

The undersigned (whose title is supplied below) is empowered to sign this statement on behalf of the Assignee.

Date: 7/27/2012

Signature: 

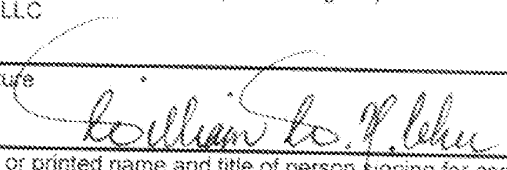
Name: William W. Y. Chu

Title: President and CEO

Company: Acqis LLC

PTO/SB/53 (09-07)
Approved for use through 08/31/2013. DMH 0651-0033
U.S. Patent and Trademark Office, U.S. DEPARTMENT OF COMMERCE

Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it displays a valid OMB control number.

REISSUE APPLICATION: CONSENT OF ASSIGNEE; STATEMENT OF NON-ASSIGNMENT		Docket Number (Optional) ACQI-006/06US 310678-2072
This is part of the application for a reissue patent based on the original patent identified below.		
Name of Patentee(s) Acqis LLC		
Patent Number 6643777	Date Patent Issued November 4, 2003	
Title of Invention DATA SECURITY METHOD AND DEVICE FOR COMPUTER MODULES		
<p>1. <input checked="" type="checkbox"/> Filed herein is a statement under 37 CFR 3.73(b). (Form PTO/SB/96)</p> <p>2. <input type="checkbox"/> Ownership of the patent is in the inventor(s), and no assignment of the patent is in effect.</p> <p>One of boxes 1 or 2 above must be checked. If multiple assignees, complete this form for each assignee. If box 2 is checked, skip the next entry and go directly to "Name of Assignee".</p> <p>The written consent of all assignees and inventors owning an undivided interest in the original patent is included in this application for reissue.</p> <p>The assignee(s) owning an undivided interest in said original patent is/are <u>Acqis LLC</u>, and the assignee(s) consents to the accompanying application for reissue.</p>		
Name of assignee/inventor (if not assigned) Acqis LLC		
Signature 	Date 7/27/2012	
Typed or printed name and title of person signing for assignee (if assigned) William W. Y. Chu, President and CEO		

This Collection of information is required by 37 CFR 1.172. The information is required to obtain or retain a benefit by the public, which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 5 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual's case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS address send TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.

If you need assistance in completing the form, call 1-800-PTO-9199 and select option 2

STATEMENT UNDER 37 CFR 3.73(b)

Applicant/Patent Owner: Acqis LLC

Application No./Patent No.: 6,643,777 Filed/Issue Date: November 4, 2003

Entitled: DATA SECURITY METHOD AND DEVICE FOR COMPUTER MODULES

Acqis LLC

(Name of Assignee)

a corporation

(Type of Assignee, e.g., corporation, partnership, university, government agency, etc.)

states that it is:

1. ☒ the assignee of the entire right, title, and interest in;
 2. ☐ an assignee of less than the entire right, title and interest in
(The extent (by percentage) of its ownership interest is ____ %); or
 3. ☐ the assignee of an undivided interest in the entirety of (a complete assignment from one of the joint inventors was made)
- in the patent application/patent identified above by virtue of either:

A. ☒ An assignment from the inventor(s) of the patent application/patent identified above. The assignment was recorded in the United States Patent and Trademark Office on November 1, 2011 at Reel 027154, Frame 0398, or for which a copy thereof is attached.

OR

B. ☐ A chain of title from the inventor(s), of the patent application/patent identified above, to the current assignee as follows:

1. From: _____ To: _____
The document was recorded in the United States Patent and Trademark Office at Reel ____ Frame ____ or for which a copy thereof is attached.
2. From: _____ To: _____
The document was recorded in the United States Patent and Trademark Office at Reel ____ Frame ____ or for which a copy thereof is attached.
3. From: _____ To: _____
The document was recorded in the United States Patent and Trademark Office at Reel ____ Frame ____ or for which a copy thereof is attached.

☐ Additional documents in the chain of title are listed on a supplemental sheet(s).

☐ As required by 37 CFR 3.73(b)(1)(i), the documentary evidence of the chain of title from the original owner to the assignee was, or concurrently is being, submitted for recordation pursuant to 37 CFR 3.11.

[NOTE: A separate copy (i.e., a true copy of the original assignment document(s)) must be submitted to Assignment Division in accordance with 37 CFR Part 2, to record the assignment in the records of the USPTO. See MPEP 302.08]

The undersigned (whose title is supplied below) is authorized to act on behalf of the assignee.

Signature

William W. Y. Chu

Printed or Typed Name

Date

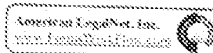
7/27/2012

President and CEO

Title

This collection of information is required by 37 CFR 3.73(b). The information is required to obtain or retain a benefit by the public which is to be paid by the USPTO to process an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.11 and 1.14. This collection is estimated to take 12 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1480, Alexandria, VA 22313-1480. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. SEND TO: Commissioner for Patents, P.O. Box 1480, Alexandria, VA 22313-1480.

If you need assistance in completing the form, call 1-800-PTO-9199 and select option 2.



IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In Re Application of: William W. Y. Chu Confirmation No.:

Serial No.: To be assigned Group Art Unit:

Filed: July 30, 2012 Examiner:

For: DATA SECURITY METHOD AND DEVICE FOR COMPUTER MODULES

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

INFORMATION DISCLOSURE STATEMENT UNDER 37 C.F.R. §1.97(b)

In accordance with the duty of disclosure set forth in 37 C.F.R. §1.56, Applicant(s) hereby submits the following information in conformance with 37 C.F.R. §§1.97 and 1.98.

- ☒ Pursuant to 37 C.F.R. §1.98, a copy of each non-US patent document cited in the attached Form PTO/SB/08 is enclosed.
- ☐ No copies of the publications listed on the attached Form PTO/SB/08 are being provided pursuant to 37 C.F.R. §1.98(d) because the publications were previously cited by or submitted to the Office in prior Application Serial No. 13/087,912 to which the above-identified application claims priority under 35 U.S.C. §120.
- ☒ No copies of any U.S. patents or U.S. patent application publications listed on the attached Form PTO/SB/08 are being provided pursuant to 37 C.F.R. §1.98.
- ☐ Publication(s) _____ listed on the attached Form PTO/SB/08 were cited in a foreign search or examination report corresponding to _____ application serial no. _____ and mailed on _____.
- ☐ Enclosed is a copy of a non-English publication(s) _____ Pursuant to §609 of the M.P.E.P., Applicant submits the attached foreign search or examination report, which cites such non-English language publication(s).
- ☐ Enclosed is a copy of a non-English publication(s) _____ English language publication _____ (copy enclosed) claims priority from this non-English publication.

- ☐ Enclosed is an explanation of non-English publication(s) _____ for which an English translation is not available.
- ☐ Enclosed is an English translation of non-English publication(s) _____ cited in the attached Form PTO/SB/08.
- ☐ Enclosed is a copy of pending patent Application Serial No. _____.

This Information Disclosure Statement is filed within any one of the following time periods:

- ☒ within three months from the filing date of this national application other than a CPA under 37 C.F.R. § 1.53(d);
- ☐ within three months from the date of entry of the national stage as set forth in 37 C.F.R. §1.491 in this international application;
- ☐ before the mailing date of a first office action on the merits; or
- ☐ before the mailing of a first office action after the filing of a request for continued examination under 37 C.F.R. § 1.114.


It is respectfully requested that the Examiner consider the above-noted information and return an initialed copy of the attached Form PTO/SB/08 to the undersigned.

Date: July 30, 2012

Customer No. 58249
COOLEY LLP
777 6th Street NW, Suite 1100
Washington, DC 20001
Tel: (650) 843-5622
Fax: (202) 842-7899

Respectfully submitted,
COOLEY LLP

By: _____


William S. Galliani
Reg. No. 33,885

Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it displays a valid OMB control number.

PATENT APPLICATION FEE DETERMINATION RECORD Substitute for Form PTO-875					Application or Docket Number 13/562,210		Filing Date 07/30/2012		<input type="checkbox"/> To be Mailed	
APPLICATION AS FILED – PART I										
(Column 1)			(Column 2)		SMALL ENTITY <input type="checkbox"/> OR		OTHER THAN SMALL ENTITY			
FOR	NUMBER FILED	NUMBER EXTRA	RATE (\$)	FEE (\$)	OR	RATE (\$)	FEE (\$)			
<input type="checkbox"/> BASIC FEE (37 CFR 1.16(a), (b), or (c))	N/A	N/A	N/A			N/A				
<input type="checkbox"/> SEARCH FEE (37 CFR 1.16(k), (l), or (m))	N/A	N/A	N/A			N/A				
<input type="checkbox"/> EXAMINATION FEE (37 CFR 1.16(o), (p), or (q))	N/A	N/A	N/A			N/A				
TOTAL CLAIMS (37 CFR 1.16(i))	minus 20 =	*	X \$ =		OR	X \$ =				
INDEPENDENT CLAIMS (37 CFR 1.16(h))	minus 3 =	*	X \$ =			X \$ =				
<input type="checkbox"/> APPLICATION SIZE FEE (37 CFR 1.16(s))	If the specification and drawings exceed 100 sheets of paper, the application size fee due is \$250 (\$125 for small entity) for each additional 50 sheets or fraction thereof. See 35 U.S.C. 41(a)(1)(G) and 37 CFR 1.16(s).									
<input type="checkbox"/> MULTIPLE DEPENDENT CLAIM PRESENT (37 CFR 1.16(j))										
			TOTAL			TOTAL				
APPLICATION AS AMENDED – PART II										
(Column 1)			(Column 2)		(Column 3)		SMALL ENTITY OR		OTHER THAN SMALL ENTITY	
AMENDMENT	07/30/2012	CLAIMS REMAINING AFTER AMENDMENT	HIGHEST NUMBER PREVIOUSLY PAID FOR	PRESENT EXTRA	RATE (\$)	ADDITIONAL FEE (\$)	RATE (\$)	ADDITIONAL FEE (\$)		
	Total (37 CFR 1.16(i))	* 41	Minus	** 41	= 0	X \$ =		OR	X \$60=	0
	Independent (37 CFR 1.16(h))	* 12	Minus	***12	= 0	X \$ =		OR	X \$250=	0
	<input type="checkbox"/> Application Size Fee (37 CFR 1.16(s))							OR		
	<input type="checkbox"/> FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))							OR		
					TOTAL ADD'L FEE		OR	TOTAL ADD'L FEE	0	
AMENDMENT	Total (37 CFR 1.16(i))	*	Minus	**	=	X \$ =		OR	X \$ =	
	Independent (37 CFR 1.16(h))	*	Minus	***	=	X \$ =		OR	X \$ =	
	<input type="checkbox"/> Application Size Fee (37 CFR 1.16(s))							OR		
	<input type="checkbox"/> FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))							OR		
						TOTAL ADD'L FEE		OR	TOTAL ADD'L FEE	
<p>* If the entry in column 1 is less than the entry in column 2, write "0" in column 3.</p> <p>** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 20, enter "20".</p> <p>*** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 3, enter "3".</p> <p>The "Highest Number Previously Paid For" (Total or Independent) is the highest number found in the appropriate box in column 1.</p>										

Legal Instrument Examiner:
/CORALIA BETANCOURT/

This collection of information is required by 37 CFR 1.16. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 12 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

If you need assistance in completing the form, call 1-800-PTO-9199 and select option 2.

PATENT APPLICATION FEE DETERMINATION RECORD Substitute for Form PTO-875						Application or Docket Number 13/562,210			
APPLICATION AS FILED - PART I									
(Column 1)		(Column 2)		SMALL ENTITY		OTHER THAN SMALL ENTITY			
FOR	NUMBER FILED	NUMBER EXTRA	RATE(\$)	FEE(\$)		RATE(\$)	FEE(\$)		
BASIC FEE (37 CFR 1.16(a), (b), or (c))	N/A	N/A	N/A			N/A	380		
SEARCH FEE (37 CFR 1.16(k), (l), or (m))	N/A	N/A	N/A			N/A	620		
EXAMINATION FEE (37 CFR 1.16(o), (p), or (q))	N/A	N/A	N/A			N/A	750		
TOTAL CLAIMS (37 CFR 1.16(i))	41	minus 20 = 21				x 60 =	1260		
INDEPENDENT CLAIMS (37 CFR 1.16(h))	12	minus 3 = 9				x 250 =	2250		
APPLICATION SIZE FEE (37 CFR 1.16(s))	If the specification and drawings exceed 100 sheets of paper, the application size fee due is \$310 (\$155 for small entity) for each additional 50 sheets or fraction thereof. See 35 U.S.C. 41(a)(1)(G) and 37 CFR 1.16(s).						0.00		
MULTIPLE DEPENDENT CLAIM PRESENT (37 CFR 1.16(j))							0.00		
				TOTAL		TOTAL	5260		
* If the difference in column 1 is less than zero, enter "0" in column 2.									
APPLICATION AS AMENDED - PART II									
(Column 1)		(Column 2)		(Column 3)		SMALL ENTITY		OTHER THAN SMALL ENTITY	
AMENDMENT A		CLAIMS REMAINING AFTER AMENDMENT		HIGHEST NUMBER PREVIOUSLY PAID FOR	PRESENT EXTRA	RATE(\$)	ADDITIONAL FEE(\$)	RATE(\$)	ADDITIONAL FEE(\$)
	Total (37 CFR 1.16(i))	*	Minus	**	=	x	=	x	=
	Independent (37 CFR 1.16(h))	*	Minus	***	=	x	=	x	=
	Application Size Fee (37 CFR 1.16(s))								
	FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))								
						TOTAL ADD'L FEE		TOTAL ADD'L FEE	
(Column 1)		(Column 2)		(Column 3)		SMALL ENTITY		OTHER THAN SMALL ENTITY	
AMENDMENT B		CLAIMS REMAINING AFTER AMENDMENT		HIGHEST NUMBER PREVIOUSLY PAID FOR	PRESENT EXTRA	RATE(\$)	ADDITIONAL FEE(\$)	RATE(\$)	ADDITIONAL FEE(\$)
	Total (37 CFR 1.16(i))	*	Minus	**	=	x	=	x	=
	Independent (37 CFR 1.16(h))	*	Minus	***	=	x	=	x	=
	Application Size Fee (37 CFR 1.16(s))								
	FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))								
						TOTAL ADD'L FEE		TOTAL ADD'L FEE	
* If the entry in column 1 is less than the entry in column 2, write "0" in column 3. ** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 20, enter "20". *** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 3, enter "3". The "Highest Number Previously Paid For" (Total or Independent) is the highest found in the appropriate box in column 1.									



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United States Patent and Trademark Office
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Alexandria, Virginia 22313-1450
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APPLICATION NUMBER	FILING or 371(c) DATE	GRP ART UNIT	FIL FEE REC'D	ATTY DOCKET NO	TOT CLAIMS	IND CLAIMS
13/562,210	07/30/2012	2115	5260	ACQI-006/05US 310578-2072	41	12

CONFIRMATION NO. 1045

58249
COOLEY LLP
ATTN: Patent Group
Suite 1100
777 - 6th Street, NW
WASHINGTON, DC 20001

FILING RECEIPT



Date Mailed: 08/16/2012

Receipt is acknowledged of this reissue patent application. The application will be taken up for examination in due course. Applicant will be notified as to the results of the examination. Any correspondence concerning the application must include the following identification information: the U.S. APPLICATION NUMBER, FILING DATE, NAME OF APPLICANT, and TITLE OF INVENTION. Fees transmitted by check or draft are subject to collection. Please verify the accuracy of the data presented on this receipt. **If an error is noted on this Filing Receipt, please submit a written request for a Filing Receipt Correction. Please provide a copy of this Filing Receipt with the changes noted thereon. If you received a "Notice to File Missing Parts" for this application, please submit any corrections to this Filing Receipt with your reply to the Notice. When the USPTO processes the reply to the Notice, the USPTO will generate another Filing Receipt incorporating the requested corrections**

Applicant(s)

William W. Y. Chu, Los Altos, CA;

Assignment For Published Patent Application

ACQIS LLC.

Power of Attorney: The patent practitioners associated with Customer Number 58249

Domestic Priority data as claimed by applicant

This application is a REI of 09/312,199 05/14/1999 PAT 6643777

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If Required, Foreign Filing License Granted: 08/15/2012

The country code and number of your priority application, to be used for filing abroad under the Paris Convention, is **US 13/562,210**

Projected Publication Date: None, application is not eligible for pre-grant publication

Non-Publication Request: No

Early Publication Request: No

Title

Data Security Method and Device for Computer Modules

Preliminary Class

713

PROTECTING YOUR INVENTION OUTSIDE THE UNITED STATES

Since the rights granted by a U.S. patent extend only throughout the territory of the United States and have no effect in a foreign country, an inventor who wishes patent protection in another country must apply for a patent in a specific country or in regional patent offices. Applicants may wish to consider the filing of an international application under the Patent Cooperation Treaty (PCT). An international (PCT) application generally has the same effect as a regular national patent application in each PCT-member country. The PCT process **simplifies** the filing of patent applications on the same invention in member countries, but **does not result** in a grant of "an international patent" and does not eliminate the need of applicants to file additional documents and fees in countries where patent protection is desired.

Almost every country has its own patent law, and a person desiring a patent in a particular country must make an application for patent in that country in accordance with its particular laws. Since the laws of many countries differ in various respects from the patent law of the United States, applicants are advised to seek guidance from specific foreign countries to ensure that patent rights are not lost prematurely.

Applicants also are advised that in the case of inventions made in the United States, the Director of the USPTO must issue a license before applicants can apply for a patent in a foreign country. The filing of a U.S. patent application serves as a request for a foreign filing license. The application's filing receipt contains further information and guidance as to the status of applicant's license for foreign filing.

Applicants may wish to consult the USPTO booklet, "General Information Concerning Patents" (specifically, the section entitled "Treaties and Foreign Patents") for more information on timeframes and deadlines for filing foreign patent applications. The guide is available either by contacting the USPTO Contact Center at 800-786-9199, or it can be viewed on the USPTO website at <http://www.uspto.gov/web/offices/pac/doc/general/index.html>.

For information on preventing theft of your intellectual property (patents, trademarks and copyrights), you may wish to consult the U.S. Government website, <http://www.stopfakes.gov>. Part of a Department of Commerce initiative, this website includes self-help "toolkits" giving innovators guidance on how to protect intellectual property in specific countries such as China, Korea and Mexico. For questions regarding patent enforcement issues, applicants may call the U.S. Government hotline at 1-866-999-HALT (1-866-999-4158).

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NOT GRANTED

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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of: William W. Y. Chu Confirmation No.: 1045
Serial No.: 13/562,210 Examiner: Not yet assigned
Filed: July 30, 2012 Group Art Unit: 2115
For: DATA SECURITY METHOD AND DEVICE FOR COMPUTER MODULES

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

REQUEST FOR CORRECTION OF FILING RECEIPT

The Filing Receipt for the above-identified patent application contains the following errors in the **Domestic Priority data as claimed by applicant**:

This application is a RIC of 13/294,108 11/10/2011 PAT RE43602

Which is a RIC of 12/561,138 09/16/2009 PAT RE42984

Which is a RIC of 11/056,604 02/10/2005 PAT RE41092

Which is a REI of 09/312,199 05/14/1999 PAT 6,643,777

The priority claims are made in a Preliminary Amendment submitted with the Reissue Continuation papers on July 30, 2012. Please issue an Updated Filing Receipt for this patent application.

The Commissioner is hereby authorized to charge any appropriate fees under 37 C.F.R. §§1.16, 1.17, and 1.21 that may be required by this paper, and to credit any overpayment, to Deposit Account No. 50-1283.

Date: October 9, 2012

Customer No. 58249
COOLEY LLP
777 6th Street NW, Suite 1100
Washington, DC 20001

Tel: (650) 843-5622
Fax: (202) 842-7899

Respectfully submitted,
COOLEY LLP

By: 

William S. Galliani
Reg. No. 33,885

Electronic Acknowledgement Receipt	
EFS ID:	13946023
Application Number:	13562210
International Application Number:	
Confirmation Number:	1045
Title of Invention:	Data Security Method and Device for Computer Modules
First Named Inventor/Applicant Name:	William W. Y. Chu
Customer Number:	58249
Filer:	Jason C. Fan/Bobbie Jutras
Filer Authorized By:	Jason C. Fan
Attorney Docket Number:	ACQI-006/05US 310578-2072
Receipt Date:	09-OCT-2012
Filing Date:	30-JUL-2012
Time Stamp:	20:02:08
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	no
------------------------	----

File Listing:

Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1	Request for Corrected Filing Receipt	ACQI-006-05US_10-09-12_Req ForCorrFR.pdf	30117 cbb87848f22efc196356218ee5aebf92f1edf9ba	no	1

Warnings:

Information:

This Acknowledgement Receipt evidences receipt on the noted date by the USPTO of the indicated documents, characterized by the applicant, and including page counts, where applicable. It serves as evidence of receipt similar to a Post Card, as described in MPEP 503.

New Applications Under 35 U.S.C. 111

If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application.

National Stage of an International Application under 35 U.S.C. 371

If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.

New International Application Filed with the USPTO as a Receiving Office

If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.



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APPLICATION NUMBER	FILING or 371(c) DATE	GRP ART UNIT	FIL FEE REC'D	ATTY DOCKET NO	TOT CLAIMS	IND CLAIMS
13/562,210	07/30/2012	2403	5260	ACQI-006/05US 310578-2072	41	12

CONFIRMATION NO. 1045

CORRECTED FILING RECEIPT



58249
COOLEY LLP
ATTN: Patent Group
Suite 1100
777 - 6th Street, NW
WASHINGTON, DC 20001

Date Mailed: 10/22/2012

Receipt is acknowledged of this reissue patent application. The application will be taken up for examination in due course. Applicant will be notified as to the results of the examination. Any correspondence concerning the application must include the following identification information: the U.S. APPLICATION NUMBER, FILING DATE, NAME OF APPLICANT, and TITLE OF INVENTION. Fees transmitted by check or draft are subject to collection. Please verify the accuracy of the data presented on this receipt. **If an error is noted on this Filing Receipt, please submit a written request for a Filing Receipt Correction. Please provide a copy of this Filing Receipt with the changes noted thereon. If you received a "Notice to File Missing Parts" for this application, please submit any corrections to this Filing Receipt with your reply to the Notice. When the USPTO processes the reply to the Notice, the USPTO will generate another Filing Receipt incorporating the requested corrections**

Inventor(s)

William W. Y. Chu, Los Altos, CA;

Applicant(s)

William W. Y. Chu, Los Altos, CA;

Assignment For Published Patent Application

ACQIS LLC.

Power of Attorney: The patent practitioners associated with Customer Number 58249

Domestic Priority data as claimed by applicant

This application is a CON of 13/294,108 11/10/2011 PAT RE43602
which is a CON of 12/561,138 09/16/2009 PAT RE42984
which is a CON of 11/056,604 02/10/2005 PAT RE41092
which is a REI of 09/312,199 05/14/1999 PAT 6643777

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If Required, Foreign Filing License Granted: 08/15/2012

The country code and number of your priority application, to be used for filing abroad under the Paris Convention, is **US 13/562,210**

Projected Publication Date: None, application is not eligible for pre-grant publication

Non-Publication Request: No

Early Publication Request: No

Title

Data Security Method and Device for Computer Modules

Preliminary Class

726

PROTECTING YOUR INVENTION OUTSIDE THE UNITED STATES

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The grant of a license does not in any way lessen the responsibility of a licensee for the security of the subject matter as imposed by any Government contract or the provisions of existing laws relating to espionage and the national security or the export of technical data. Licensees should apprise themselves of current regulations especially with respect to certain countries, of other agencies, particularly the Office of Defense Trade Controls, Department of State (with respect to Arms, Munitions and Implements of War (22 CFR 121-128)); the Bureau of Industry and Security, Department of Commerce (15 CFR parts 730-774); the Office of Foreign Assets Control, Department of Treasury (31 CFR Parts 500+) and the Department of Energy.

NOT GRANTED

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1 of 1 DOCUMENT

UNITED STATES PATENT AND TRADEMARK OFFICE GRANTED PATENT

6643777

[Link to Claims Section](#)

November 4, 2003

Data security method and device for computer modules

REISSUE:

February 10, 2005 - Reissue Application filed Ex. Gp.: 2131; Re. S.N. 11/056,604 , (O.G. May 3, 2005)
February 10, 2005 - Reissue Application filed Ex. Gp.: 2131; Re. S.N. 11/056,604 , (O.G. May 3, 2005)
October 6, 2006 - Reissue Application filed, Ex. Gp.: 2131; Re. S.N. 11/545,056 , (O.G. September 30, 2008)
September 16, 2009 - Reissue Application filed, Ex. Gp.: 2115; Re. S.N. 12/561,138 , (O.G. October 20, 2009)
January 26, 2010 - This patent was reissued as Reissue Patent RE 41,092 (O.G. January 26, 2010) ,
November 29, 2011 - This patent was reissued as Reissue Patent RE 42,984 (O.G. November 29, 2011) ,
February 7, 2012 - This patent was reissued as Reissue Patent RE 43,171 (O.G. February 7, 2012) ,
June 30, 2012 - Reissue Application filed, Ex. Gp.: 2115; Re. S.N. 13/562,210 , (O.G. September 11, 2012)
August 21, 2012 - This patent was reissued as Reissue Patent RE 43,602 (O.G. August 21, 2012) ,

INVENTOR: Chu, William W. Y. - Los Altos, California

APPL-NO: 312199 (09)

FILED-DATE: May 14, 1999

GRANTED-DATE: November 4, 2003

ASSIGNEE-PRE-ISSUE:

May 14, 1999 - ASSIGNMENT OF ASSIGNOR'S INTEREST (SEE DOCUMENT FOR DETAILS)., ACQUIS TECHNOLOGY, INC. 1621 W. EL CAMINO REALMOUNTAIN VIEW, CALIFORNIA, 94040, Reel and Frame Number: 009971/0653

ASSIGNEE-AT-ISSUE:

Acquis Technology, Inc., Mountain View, California, United States company or corporation (02)

ASSIGNEE-AFTER-ISSUE:

November 1, 2011 - ASSIGNMENT OF ASSIGNOR'S INTEREST (SEE DOCUMENT FOR DETAILS)., ACQUIS LLC, 411 INTERCHANGE STREET, MCKINNEY, TEXAS, UNITED STATES OF AMERICA (US), 75069, Reel and Frame Number: 027154/0398

312199 (09) 6643777 November 4, 2003

LEGAL-STATUS:

May 14, 1999 - ASSIGNMENT
May 3, 2005 - REISSUE APPLICATION FILED
May 4, 2007 - FEE PAYMENT
September 30, 2008 - REISSUE APPLICATION FILED
October 20, 2009 - REISSUE APPLICATION FILED
November 1, 2011 - ASSIGNMENT
December 6, 2011 - REISSUE APPLICATION FILED
May 4, 2007 - Payment of Maintenance Fee, 4th Yr, Small Entity.

IPC-MAIN-CL: [7] G06F 009#00**IPC-MAIN-CL:** [8] G06F 021#00 (20060101) Advanced Inventive 20051008 (A I R M EP)**PRIM-EXMR:** Hua, Ly V.

CORE TERMS: computer, module, console, memory, peripheral, user, interface, drive, bus, controller, hard disk, identification, flash, host, couple, hardware, password, software, desktop, storage, bridge, removable, network, graphics, mechanical, display, computer system, portable computer, keyboard, coupled

ENGLISH-ABST:

A security method for an attached computer module in a computer system. The security method reads a security identification number in an attached computer module and compares it to a security identification number in a console, which houses the attached computer module. Based upon a relationship between these numbers, a security status is selected. The security status determines the security level of operating the computer system.

No Documents Found

No documents were found for your search terms

"6643777 or 6,643,777"

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- OR -

Click "Search Using Natural Language" to run your search as Natural Language search.

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- Use a less restrictive date range.
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- OR -

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- Remove some search terms.
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- Use a less restrictive date range.
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File 670:LitAlert 1973-2011/UD=201140
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Set	Items	Description
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? e pn=us 6643777

Ref	Items	Index-term
E1	3	PN=US 6643656
E2	2	PN=US 6643765
E3	0	*PN=US 6643777
E4	1	PN=US 6643885
E5	1	PN=US 6644049
E6	1	PN=US 6644120
E7	1	PN=US 6644224
E8	3	PN=US 6644241
E9	1	PN=US 6644295
E10	2	PN=US 6644333

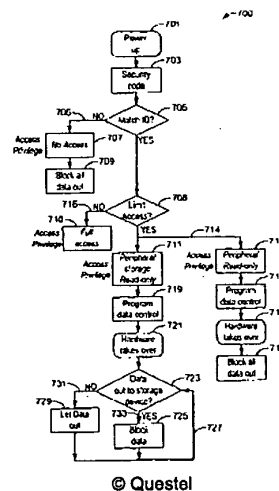
Data security method and device for computer modules US6643777

<ul style="list-style-type: none"><u>Patent Assignee</u> ACQIS ACQIS TECHNOLOGY NEOEDGE NETWORKS<u>Inventor</u> CHU WILLIAM W Y<u>International Patent Classification</u> G06F-001/00;G06F-001/26;G06F-007/00;G06F-007/04;G06F-009/00;G06F-011/00;G06F-011/30;G06F-017/00;G06F-017/30;G06F-021/00;H04L-009/32<u>US Patent Classification</u> 707999009;713193000;726002000;726003000;726004000;726016000;726017000;726027000;726036000	<ul style="list-style-type: none"><u>Publication Information</u> US6643777 B1 20031104 [US6643777]<u>Priority Details</u> 1999US-0312199 19990514 2005US-0056604 20050210 2006US-0545056 20061006 2009US-0561138 20090916 2011US-13294108 20111110																				
<ul style="list-style-type: none"><u>Fampat family</u><table><tr><td>US6643777</td><td>B1</td><td>20031104</td><td>[US6643777]</td></tr><tr><td>USRE41092</td><td>E1</td><td>20100126</td><td>[USRE41092]</td></tr><tr><td>USRE42984</td><td>E1</td><td>20111129</td><td>[USRE42984]</td></tr><tr><td>USRE43171</td><td>E1</td><td>20120207</td><td>[USRE43171]</td></tr><tr><td>USRE43602</td><td>E1</td><td>20120821</td><td>[USRE43602]</td></tr></table>		US6643777	B1	20031104	[US6643777]	USRE41092	E1	20100126	[USRE41092]	USRE42984	E1	20111129	[USRE42984]	USRE43171	E1	20120207	[USRE43171]	USRE43602	E1	20120821	[USRE43602]
US6643777	B1	20031104	[US6643777]																		
USRE41092	E1	20100126	[USRE41092]																		
USRE42984	E1	20111129	[USRE42984]																		
USRE43171	E1	20120207	[USRE43171]																		
USRE43602	E1	20120821	[USRE43602]																		

• **Abstract:**

(USRE43602)

A security method for an attached computer module in a computer system. The security method reads a security identification number in an attached computer module and compares it to a security identification number in a console, which houses the attached computer module. Based upon a relationship between these numbers, a security status is selected. The security status determines the security level of operating the computer system.



Action Taken

(US6643777)

LEGAL DETAILS FOR US6643777

Actual or expected expiration date=2019-05-14

Legal state=ALIVE

Status=GRANTED

Event publication date=1999-05-14

Event code=Application details

Event indicator=Pos

Event type=Examination events

Application details

Application country=US US09312199

Application date=1999-05-14

Standardized application number=1999US-09312199

Event publication date=1999-05-14

Event code=Assignment

Event type=Change of name or address

Event type=Reassignment

Assignment

OWNER:ACQIS TECHNOLOGY, INC., CALIFORNIA

Effective date of the event=1999-05-06

ASSIGNMENT OF ASSIGNORS INTEREST ASSIGNOR:CHU, WILLIAM W.Y. REEL/FRAME:009971/0653.

Event publication date=2003-11-04

Event code=Reexamination certificate first reexamination

Event indicator=Pos

Event type=Event indicating In Force

Granted patent as first publication

Publication country=US

Publication number=US6643777

Publication stage Code=B1

Publication date=2003-11-04

Standardized publication number=US6643777

Event publication date=2005-05-03

Event code=Reissue application filed

Event type=Opposition and reexamination events

Reissue application filed

Reissue appl. filed

Effective date of the event=2005-02-10

Event publication date=2008-09-30

Event code=Reissue application filed

Event type=Opposition and reexamination events

Reissue application filed

Reissue appl. filed

Effective date of the event=2006-10-06

Event publication date=2007-05-04

Event code=Fee payment

Event indicator=Pos

Event type=Event indicating In Force

Event type=Payment or non-payment notifications

Fee payment

Year of payment of annual fees=4

Event publication date=2009-10-20

Event code=Reissue application filed

Event type=Opposition and reexamination events

Reissue application filed

Reissue appl. filed

Effective date of the event=2009-09-16

Event publication date=2011-11-01

Event code=Assignment

Event type=Change of name or address

Event type=Reassignment

Assignment

OWNER:ACQIS LLC, TEXAS

Effective date of the event=2011-11-01

ASSIGNMENT OF ASSIGNORS INTEREST ASSIGNOR:ACQIS TECHNOLOGY, INC. REEL/FRAME:027154/0398.

Event publication date=2011-12-06

Event code=Reissue application filed

Event type=Opposition and reexamination events

Reissue application filed

Reissue appl. filed

Effective date of the event=2011-11-10

Event publication date=2012-09-11

Event code=Reissue application filed

Event type=Opposition and reexamination events

Reissue application filed

Reissue appl. filed

Effective date of the event=2012-06-30

Action Taken

(USRE41092)

LEGAL DETAILS FOR USRE41092

Actual or expected expiration date=2025-02-10

Legal state=ALIVE
Status=GRANTED

Event publication date=2005-02-10
Event code=Application details
Event indicator=Pos
Event type=Examination events

Application details

Application country=US US11056604
Application date=2005-02-10
Standardized application number=2005US-11056604

Event publication date=2009-03-27
Event code=Assignment
Event type=Change of name or address
Event type=Reassignment

Assignment

OWNER:ACQIS TECHNOLOGY, INC., CALIFORNIA
Effective date of the event=1999-05-06

ASSIGNMENT OF ASSIGNORS INTEREST ASSIGNOR:CHU, WILLIAM W.Y. REEL/FRAME:022463/0447.

Event publication date=2010-01-26
Event code=Reissue
Event indicator=Pos
Event type=Event indicating In Force

Reissue

Publication country=US
Publication number=USRE41092
Publication stage Code=E1
Publication date=2010-01-26
Standardized publication number=USRE41092

Action Taken

(USRE42984)

LEGAL DETAILS FOR USRE42984

Actual or expected expiration date=2025-02-10
Legal state=ALIVE
Status=GRANTED

Event publication date=2009-09-16
Event code=Application details
Event indicator=Pos
Event type=Examination events

Application details

Application country=US US12561138
Application date=2009-09-16
Standardized application number=2005US-12561138

Event publication date=2011-11-29
Event code=Reissue
Event indicator=Pos

Event type=Event indicating In Force

Reissue

Publication country=US
 Publication number=USRE42984
 Publication stage Code=E1
 Publication date=2011-11-29
 Standardized publication number=USRE42984

Action Taken

(USRE43171)

LEGAL DETAILS FOR USRE43171

Actual or expected expiration date=2026-10-06
 Legal state=ALIVE
 Status=GRANTED

Event publication date=2006-10-06
 Event code=Application details
 Event indicator=Pos
 Event type=Examination events

Application details

Application country=US US11545056
 Application date=2006-10-06
 Standardized application number=2006US-11545056

Event publication date=2012-02-07
 Event code=Reissue
 Event indicator=Pos
 Event type=Event indicating In Force

Reissue

Publication country=US
 Publication number=USRE43171
 Publication stage Code=E1
 Publication date=2012-02-07
 Standardized publication number=USRE43171

Action Taken

(USRE43602)

LEGAL DETAILS FOR USRE43602

Actual or expected expiration date=2025-02-10
 Legal state=ALIVE
 Status=GRANTED

Event publication date=2011-11-10
 Event code=Application details
 Event indicator=Pos
 Event type=Examination events

Application details

Application country=US US13294108
 Application date=2011-11-10
 Standardized application number=2005US-13294108

Event publication date=2012-08-21

Event code=Reissue
Event indicator=Pos
Event type=Event indicating In Force

Reissue

Publication country=US
Publication number=USRE43602
Publication stage Code=E1
Publication date=2012-08-21
Standardized publication number=USRE43602 •



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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
13/562,210	07/30/2012	William W. Y. Chu	ACQI-006/05US 310578-2072	1045
58249	7590	11/19/2012		
COOLEY LLP ATTN: Patent Group 777 - 6th Street, NW Suite 1100 WASHINGTON, DC 20001			EXAMINER SONG, HOSUK	
			ART UNIT 2435	PAPER NUMBER
			MAIL DATE 11/19/2012	DELIVERY MODE PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	13/562,210	CHU, WILLIAM W. Y.	
	Examiner	Art Unit	
	Hosuk Song	2435	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1) ☒ Responsive to communication(s) filed on 30 July 2012.

2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.

3) ☐ An election was made by the applicant in response to a restriction requirement set forth during the interview on ____; the restriction requirement and election have been incorporated into this action.

4) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

5) ☒ Claim(s) 14-54 is/are pending in the application.

5a) Of the above claim(s) ____ is/are withdrawn from consideration.

6) ☒ Claim(s) 14-23 and 29-43 is/are allowed.

7) ☒ Claim(s) 24-27, 44, 47, 48 and 50-54 is/are rejected.

8) ☒ Claim(s) 28, 45, 46 and 49 is/are objected to.

9) ☐ Claim(s) ____ are subject to restriction and/or election requirement.

Application Papers

10) ☐ The specification is objected to by the Examiner.

11) ☒ The drawing(s) filed on 30 July 2012 is/are: a) ☒ accepted or b) ☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

12) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

13) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a) ☐ All b) ☐ Some * c) ☐ None of:

1. ☐ Certified copies of the priority documents have been received.

2. ☐ Certified copies of the priority documents have been received in Application No. ____.

3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)

2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)

3) ☒ Information Disclosure Statement(s) (PTO/SB/08)

Paper No(s)/Mail Date 7/30/12.

4) ☐ Interview Summary (PTO-413)

Paper No(s)/Mail Date. ____.

5) ☐ Notice of Informal Patent Application

6) ☐ Other: ____.

DETAILED ACTION

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

Claims 24-27,44,47-48,50-54 are rejected under 35 U.S.C. 102(e) as being anticipated by Nobutani et al(US 6,487,614).

Claim 24: Nobutani disclose an integrated central processing unit and graphics controller in a single chip directly connected to a Low Voltage Differential Signal (LVDS) channel comprising two sets of unidirectional serial bit channels to transmit data in opposite directions in (fig.1 and col.4,lines 26-41). Nobutani disclose a main memory directly coupled to the integral central processing unit and graphics controller to convey digital video display information in (fig.2,3 and col.4,lines 8-25).

Claim 25: Nobutani disclose LVDS channel conveys an encoded serial bit stream of address and data bits of a Peripheral Component Interconnect (“PCI”) bus transaction in (col.1,lines 14-25;col.4,lines 8-25).

Claim 26: Nobutani disclose a connector coupled to a console in (fig.2).

Claim 27: Nobutani disclose computer conveys Universal Serial Bus protocol data through the connector to the console in (col.2,lines 49-67).

Claim 44: Nobutani disclose an integrated central processing unit and graphics controller in a single chip directly connected to a first Low Voltage Differential Signal (LVDS) channel comprising two sets of unidirectional, serial bit channel to transmit data in opposite directions in (fig.1 and col.4,lines 26-

Art Unit: 2435

41). Nobutani disclose a main memory directly coupled to the integrated central processing unit and graphics controller and a mass storage device comprising flash memory in (fig.2 and col.12,lines 3-7).

Claim 47: Nobutani disclose first LVDS channel conveys an encoded serial bit stream of address and data bits of a Peripheral Component Interconnect(PCI) bus transaction in (col.1,lines 14-25;col.4,lines 8-25).

Claim 48: Nobutani disclose a connector that conveys Universal Serial Bus protocol information to a console in (col.2,lines 49-67).

Claim 50: Nobutani disclose a Central Processing Unit(CPU) directly connected to a Low Voltage Differential Signal(LVDS) channel comprising two set of multiple, unidirectional, serial bits channels to convey an encoded serial bit stream of encoded address and data bits of a Peripheral Component Interconnect(PCI) bus transaction in opposite directions in (fig.1 and col.4,lines 26-41). Nobutani disclose a main memory directly connected to the CPU and a mass storage device coupled to the CPU in (fig.2 and col.12,lines 3-7).

Claim 51: Nobutani disclose connector connects to a console comprising a power supply, and the power supply supplies the power to the computer upon coupling to the console in (fig.2).

Claim 52: Nobutani disclose mass storage device comprises flash memory in (fig.2 and col.12,lines 3-7).

Claim 53: Nobutani disclose an integrated central processing unit and graphics controller in a single chip directly connected to a first Low Voltage Differential Signal (LVDS) channel in (fig.2); comprising two sets of multiple, unidirectional , serial bit channels to convey an encoded serial bit stream of encoded address and data bits of a Peripheral Component Interconnect(PCI) bus transaction in opposite directions in (fig.1 and col.4,lines 26-41). Nobutani disclose a main memory directly coupled to the integrated central processing unit and graphics controller and an Ethernet communication device coupled to the first LVDS channel in (fig.2 and col.4,lines 8-25).

Art Unit: 2435

Claim 54: Nobutani disclose connector connects to a console comprising a power supply, and the power supply supplies the power to the computer upon coupling to the console in (fig.2).

Allowable Subject Matter

Claims 14-23,29-43 are allowed.

Claims 28,45-46,49 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

USPTO Contact Information

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Hosuk Song whose telephone number is (571)272-3857. The examiner can normally be reached on mon-fri.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Kambiz Zand can be reached on 5712723811. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/Hosuk Song/

Application/Control Number: 13/562,210

Page 5

Art Unit: 2435

Primary Examiner, Art Unit 2435

Notice of References Cited	Application/Control No. 13/562,210	Applicant(s)/Patent Under Reexamination CHU, WILLIAM W. Y.	
	Examiner Hosuk Song	Art Unit 2435	Page 1 of 1

U.S. PATENT DOCUMENTS

*		Document Number Country Code-Number-Kind Code	Date MM-YYYY	Name	Classification
*	A	US-6,487,614	11-2002	Nobutani et al.	710/20
*	B	US-6,202,115	03-2001	Khosrowpour, Farzad	710/312
	C	US-			
	D	US-			
	E	US-			
	F	US-			
	G	US-			
	H	US-			
	I	US-			
	J	US-			
	K	US-			
	L	US-			
	M	US-			

FOREIGN PATENT DOCUMENTS

*		Document Number Country Code-Number-Kind Code	Date MM-YYYY	Country	Name	Classification
	N					
	O					
	P					
	Q					
	R					
	S					
	T					

NON-PATENT DOCUMENTS

*		Include as applicable: Author, Title Date, Publisher, Edition or Volume, Pertinent Pages)
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	V	
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*A copy of this reference is not being furnished with this Office action. (See MPEP § 707.05(a).)
Dates in MM-YYYY format are publication dates. Classifications may be US or foreign.



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low voltage differential signal and

Searching for: low voltage differential signal and computer architecture ([start a new search](#))Found 2,304 within *The ACM Guide to Computing Literature* (Bibliographic citations from major publishers in computing)Limit your search to [Publications from ACM and Affiliated Organizations](#) (Full-Text collection: 360,430 items)

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- 1 [Architecture and design of a simultaneously bidirectional single-ended high speed chip-to-chip interface](#)
 Robert Orzel
 January 2002 *Architecture and design of a simultaneously bidirectional single-ended high speed chip-to-chip interface*
Publisher: Sun Microsystems, Inc.
 Full text available: [PDF](#) (5.45 MB)
Bibliometrics: Downloads (6 Weeks): , Downloads (12 Months): 2, Downloads (Overall): 19, Citation Count: 0

Advances in integrated circuit technologies permit faster clocking speed and increased logic density in chips. However, advances in chip packaging technologies have not kept pace; hence the number of input/output pins a input/output bandwidth per chip ...

- 2 [The BlackWidow High-Radix Clos Network](#)
 Steve Scott, Dennis Abts, John Kim, William J. Dally
 June 2006 *ISCA '06: Proceedings of the 33rd annual international symposium on Computer Architecture*
Publisher: ACM
 Full text available: [PDF](#) (815.14 KB)
Bibliometrics: Downloads (6 Weeks): 5, Downloads (12 Months): 74, Downloads (Overall): 679, Citation Count: 21

This paper describes the radix-64 folded-Clos network of the Cray BlackWidow scalable vector multiprocessor. We describe the BlackWidow network which scales to 32K processors with a worstcase diameter of seven hops, and underlying high-radix router ...

Also published in:

May 2006 *SIGARCH Computer Architecture News* Volume 34 Issue 2

- 3 [A message-passing hardware/software cosimulation environment for reconfigurable computing systems](#)
 Manuel Sadaña, Emanuel Hamalho, Paul Chow
 January 2009 *International Journal of Reconfigurable Computing* , Volume 2009
Publisher: Hindawi Publishing Corp.
 Full text available: [PDF](#) (865.94 KB)
Bibliometrics: Downloads (6 Weeks): 3, Downloads (12 Months): 16, Downloads (Overall): 68, Citation Count: 0


High-performance reconfigurable computers (HPRCs) provide a mix of standard processors and FPGAs to collecti accelerate applications. This introduces new design challenges, such as the need for portable programming mode across HPRCs and system-level ...

- 4 [CMOS current-mode integrating receivers for Gbytes/s parallel links](#)
 Fei Yuan, Tao Wang
 September 2008 *Microelectronics Journal* , Volume 39 Issue 9
Publisher: Elsevier Science Publishers B. V.
Bibliometrics: Downloads (6 Weeks): n/a, Downloads (12 Months): n/a, Downloads (Overall): n/a, Citation Count: C

This paper presents the design of fully differential current-mode integrating receivers for Gbytes/s parallel links. class A and class AB configurations are considered. The proposed receivers consist of a transimpedance front-en that provides a ...

Keywords: Active inductors, Class A and class AB integrating receivers, Parallel links

- 5 [Using At-Speed BIST to Test LVDS Serializer/Deserializer Function](#)
 Magnus Eickensand, Fredrik Franzen, Ken Elliter
 April 2002 *Journal of Electronic Testing: Theory and Applications* , Volume 18 Issue 2
Publisher: Kluwer Academic Publishers

Full text available:  [Publisher Site](#)

Bibliometrics: Downloads (6 Weeks): n/a, Downloads (12 Months): n/a, Downloads (Overall): n/a, Citation Count: C

LVDS is the acronym for Low-Voltage-Differential-Signaling and is described in both the ANSI/TIA/EIA-644 and I 1596.3 standards. High performance yet Low Power and EMI have made LVDS a popular choice for high-speed c to-card serial links. A typical ...

Keywords: At-speed, BIST, LVDS, differential

6 [Architecture and performance of dynamic offloader for cluster network](#)

[Keiichi Aoki](#), [Hiroyuki Maruoka](#), [Keisaku Wada](#), [Masataka Ono](#)

December 2006 **ISPA'06: Proceedings of the 4th international conference on Parallel and Distributed Processing and Applications**

Publisher: Springer-Verlag

Bibliometrics: Downloads (6 Weeks): n/a, Downloads (12 Months): n/a, Downloads (Overall): n/a, Citation Count: C

This paper presents an architecture of the dynamic offloading mechanism, called Maestro Dynamic Offloading Mechanism (MDO), for the intelligent cluster network Maestro2. By using MDO, programmers can offload software modules to the network interface and ...

7 [A novel hardware-software co-design for automatic white balance](#)

[Chin-Hsing Chen](#), [Sun-Yen Jan](#), [Wen-Tzeng Huang](#)

September 2007 **MIV'07: Proceedings of the 7th Conference on 7th WSEAS International Conference on Multimedia, Internet & Video Technologies - Volume 7**, Volume 7

Publisher: World Scientific and Engineering Academy and Society (WSEAS)

Bibliometrics: Downloads (6 Weeks): n/a, Downloads (12 Months): n/a, Downloads (Overall): n/a, Citation Count: C

As electronic techniques is continuous improved rapidly cameras or video camcorders used for image retrieval technology and development become digitalized. The color of the photographs would look very different due to differences in light projection ...

Keywords: automatic white balance, charge-coupled device, embedded processor, hardware-software co-design system on a programmable chip

8 [Performance evaluation of offloading software modules to cluster network](#)

[Keiichi Aoki](#), [Hiroyuki Maruoka](#), [Keisaku Wada](#), [Masataka Ono](#)

February 2007 **PDCN'07: Proceedings of the 25th conference on Proceedings of the 25th IASTED International Multi Conference: parallel and distributed computing and networks**

Publisher: ACTA Press

Bibliometrics: Downloads (6 Weeks): n/a, Downloads (12 Months): n/a, Downloads (Overall): n/a, Citation Count: C

A design of software to offload user-defined software modules to Maestro2 cluster network, named Maestro dynamic offloading mechanism (MDO), and results of its performance evaluation are described. Maestro2 is a high-performance network for clusters. ...


Keywords: cluster network, offloading, performance evaluation

9 [Hardware support for language aware information mining](#)

[Michael Freeman](#), [Thimal Jayasekiriya](#)

October 2006 **KES'06: Proceedings of the 10th international conference on Knowledge-Based Intelligent Information and Engineering Systems - Volume Part III**, Volume Part III

Publisher: Springer-Verlag

Full text available:  [Publisher Site](#)

Bibliometrics: Downloads (6 Weeks): n/a, Downloads (12 Months): n/a, Downloads (Overall): n/a, Citation Count: C



Information retrieval from text or 'text mining' is the process of extracting interesting and non-trivial knowledge unstructured text. With the ever increasing amounts of information stored on the web or archived within a computer system, ...

10 [Embedded DSP Processor Design: Application Specific Instruction Set Processors](#)

[Dake Liu](#)

May 2008 Embedded DSP Processor Design: Application Specific Instruction Set Processors

Publisher: Morgan Kaufmann Publishers Inc.

Full text available:  [The ACM Learning Center](#),  [PDF](#) (15.69 MB)

Bibliometrics: Downloads (6 Weeks): 9, Downloads (12 Months): 119, Downloads (Overall): 119, Citation Count: 2

This book provides design methods for Digital Signal Processors and Application Specific Instruction set Processors based on the author's extensive, industrial design experience. Top-down and bottom-up design methodologies are

presented, providing valuable ...

Keywords: Circuits, Data Processing, Electricity, Microelectronics


11 Sun labs: the second fifty technical reports

Jeanie Treichel, Katie Chiu, Christopher Wu, Jeanne Wagon

January 2009

Sun labs: the second fifty technical reports

Publisher: Sun Microsystems, Inc.

Full text available:  [Pdf](#) (19.47 MB)

Bibliometrics: Downloads (6 Weeks): 4, Downloads (12 Months): 15, Downloads (Overall): 51, Citation Count: 0

Since the establishment of Sun Labs in 1991, Sun Labs researchers have been publishing technical reports on the technologies developed in their projects. The importance of these reports cannot be underestimated. This commemorative issue spans the years ...



12 System Level Design with Rosetta

Ferry Alexander

November 2006

System Level Design with Rosetta

Publisher: Morgan Kaufmann Publishers Inc.

Full text available:  [The ACM Learning Center](#),  [PDF](#) (4.67 MB)

Bibliometrics: Downloads (6 Weeks): 5, Downloads (12 Months): 57, Downloads (Overall): 57, Citation Count: 6

The steady and unabated increase in the capacity of silicon has brought the semiconductor industry to a watershed challenge. Now a single chip can integrate a radio transceiver, a network interface, multimedia functions, all the "glue" needed to hold ...



Keywords: Computer Architecture, Digital, Electronics, Microelectronics

13 Communications of the ACM: Volume 51 issue 7

July 2008

Communications of the ACM

Publisher: ACM

Full text available:  [Digital Edition](#),  [Pdf](#) (6.54 MB)

Bibliometrics: Downloads (6 Weeks): 88, Downloads (12 Months): 1000, Downloads (Overall): 8797, Citation Count: 5



14 On-Chip Communication Architectures: System on Chip Interconnect

Giovanni De Micheli, Luca Benini

April 2008

On-Chip Communication Architectures: System on Chip Interconnect

Publisher: Morgan Kaufmann Publishers Inc.

Full text available:  [The ACM Learning Center](#),  [PDF](#) (3.52 MB)

Bibliometrics: Downloads (6 Weeks): 15, Downloads (12 Months): 103, Downloads (Overall): 103, Citation Count: 5

Over the past decade, system-on-chip (SoC) designs have evolved to address the ever increasing complexity of applications, fueled by the era of digital convergence. Improvements in process technology have effectively shrunk board-level components so ...



Keywords: Circuits, Computer Science, Electricity, Microelectronics

15 XRDS: Crossroads, The ACM Magazine for Students: Volume 17 issue 4

June 2011

XRDS: Crossroads, The ACM Magazine for Students

Publisher: ACM

Full text available:  [Digital Edition](#),  [PDF](#) (3.97 MB)

Bibliometrics: Downloads (6 Weeks): 72, Downloads (12 Months): 371, Downloads (Overall): 670, Citation Count: 4

16 Communications of the ACM: Volume 51 issue 9

September 2008

Communications of the ACM

Publisher: ACM

Full text available:  [Digital Edition](#),  [Pdf](#) (8.68 MB)



Bibliometrics: Downloads (6 Weeks): 55, Downloads (12 Months): 685, Downloads (Overall): 6857, Citation Count: 5

17 Communications of the ACM: Volume 53 issue 5

May 2010

Communications of the ACM

Publisher: ACM



Full text available:  [Digital Edition](#),  [Pdf](#) (8.92 MB)

Bibliometrics: Downloads (6 Weeks): 129, Downloads (12 Months): 1852, Downloads (Overall): 8926, Citation Count: 5

18 Reconfigurable Computing: The Theory and Practice of FPGA-Based Computation

Scott Hauck, Andre DeHon

November 2007 Reconfigurable Computing: The Theory and Practice of FPGA-Based Computation
Publisher: Morgan Kaufmann Publishers Inc.


Full text available:  [The ACM Learning Center](#),  PDF (8.85 MB)

Bibliometrics: Downloads (6 Weeks): 19, Downloads (12 Months): 152, Downloads (Overall): 152, Citation Count: 2

The main characteristic of Reconfigurable Computing is the presence of hardware that can be reconfigured to implement specific functionality more suitable for specially tailored hardware than on a simple uniprocessor. Reconfigurable computing systems ...

Keywords: Applied, Computer Science, Electricity


19 [Power reduction techniques for microprocessor systems](#)

 [Vasanth Venkatachalam, Michael Franz](#)

September 2005

Computing Surveys (CSUR), Volume 37 Issue 3

Publisher: ACM 

Full text available:  PDF (602.33 KB)

Bibliometrics: Downloads (6 Weeks): 20, Downloads (12 Months): 283, Downloads (Overall): 6261, Citation Count:

Power consumption is a major factor that limits the performance of computers. We survey the "state of the art" techniques that reduce the total power consumed by a microprocessor system over time. These techniques are applied at various ...

Keywords: Energy dissipation, power reduction

20 [Packaging the Blue Gene/L supercomputer](#)

[P. Coteus, H. R. Bickford, T. M. Cipella, P. G. Crumley, A. Gara, S. A. Hall, G. V. Kocsay, A. P. Lanzetta, L. S. Mok, Rand, B. Swetz, I. Takken, P. La Rocca, C. Marroquin, P. R. Germann, M. J. Jeanson](#)

March 2005

IBM Journal of Research and Development, Volume 49 Issue 2

Publisher: IBM Corp.





Bibliometrics: Downloads (6 Weeks): n/a, Downloads (12 Months): n/a, Downloads (Overall): n/a, Citation Count: 4


As 1999 ended, IBM announced its intention to construct a one-petaflop supercomputer. The construction of this system was based on a cellular architecture--the use of relatively small but powerful building blocks used together in sufficient quantities ...

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Search Notes 	Application/Control No. 13562210	Applicant(s)/Patent Under Reexamination CHU, WILLIAM W. Y.
	Examiner HOSUK SONG	Art Unit 2435

SEARCHED			
Class	Subclass	Date	Examiner
726	2-9,16-21,34,36	11/15/12	HS
713	182-183,192-194	11/15/12	HS
710	1,7,8,15,20,22,100	11/15/12	HS

SEARCH NOTES		
Search Notes	Date	Examiner
EAST, foreign patent database, IBM TDB, USPGPUB	11/15/12	HS
NPL	11/15/12	HS

INTERFERENCE SEARCH			
Class	Subclass	Date	Examiner

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Receipt date: 07/30/2012

PTO/SB/08a (07-09)

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INFORMATION DISCLOSURE STATEMENT BY APPLICANT <i>(Use as many sheets as necessary)</i>		Application Number	To be assigned
		Filing Date	July 30, 2012
		First Named Inventor	William W. Y. Chu
		Art Unit	
		Examiner Name	
Sheet 1 of 5	Attorney Docket Number	ACQI-006/05US 310578-2072	

U. S. PATENT DOCUMENTS					
Examiner Initials*	Cite No. ¹	Document Number	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Page, Columns, Lines, Where Relevant Passages or Relevant Figures Appear
		Number-Kind Code ² (If known)			
/H.S./		US- 4769764	9/6/1988	Levanon	
		US- 4799258	1/17/1989	Davies	
		US- 5085499	2/4/1992	Mutone	
		US- 5103446	4/7/1992	Fischer	
		US- 5191581	3/2/1993	Woodbury et al.	
		US- 5198806	3/30/1993	Lord	
		US- 5319771	6/7/1994	Takeda	
		US- 5463742	10/31/1995	Kobayashi	
		US- 5519843	5/21/1996	Moran et al.	
		US- 5539616	7/23/1996	Kikinis	
		US- 5546463	8/13/1996	Caputo et al.	
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		US- 5623637	4/22/1997	Jones et al.	
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		US- 5640302	6/17/1997	Kikinis	
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		US- 5689654	11/18/1997	Kikinis et al.	
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		US- 5751711	5/12/1998	Sakaue	
		US- 5751950	5/12/1998	Crisan	
		US- 5754924	6/9/1998	Hong	
		US- 5774704	6/30/1998	Williams	
		US- 5815681	9/29/1998	Kikinis	
		US- 5838932	11/17/1998	Alzien	
		US- 5857085	1/5/1999	Zhang et al.	
Examiner Signature	/Hosuk Song/			Date Considered	11/14/2012

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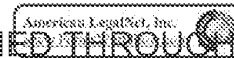
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		First Named Inventor	William W. Y. Chu
		Art Unit	
		Examiner Name	
Sheet 2 of 5	Attorney Docket Number	ACQI-006/05US 310578-2072	

/H.S./	US- 5862381	1/19/1999	Advani et al.	
	US- 5878211	3/2/1999	Delagrangue et al.	
	US- 5884049	3/16/1999	Atkinson	
	US- 5907566	5/25/1999	Benson et al.	
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	US- 5,991,833	11/23/1999	Wandler et al.	
	US- 5,999,476	12/7/1999	Dutton et al.	
	US- 5999952	12/7/1999	Jenkins et al.	
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	US- 6012145	1/4/2000	Mathers et al.	
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	US- 6069615	5/30/2000	Abraham et al.	
	US- 6070214	5/30/2000	Ahern	
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	US- 6157534	12/5/2000	Gallagher et al.	
	US- 6161157	12/12/2000	Tripathi	
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	US- 6256689	7/3/2001	Khosrowpour	
	US- 6266539	7/24/2001	Pardo	
Examiner Signature	/Hosuk Song/		Date Considered	11/14/2012

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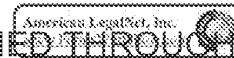
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		First Named Inventor	William W. Y. Chu
		Art Unit	
		Examiner Name	
Sheet 3 of 5	Attorney Docket Number	ACQI-006/05US 310578-2072	

/H.S./	us- 6301637	10/9/2001	Krull et al.	
	us- 6304895 B1	10/16/2001	Schneider et al.	
	us- 6311268 B1	10/30/2001	Chu	
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	us- 6324605	11/27/2001	Rafferty et al.	
	us- 6332180 B1	12/18/2001	Kauffman et al.	
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	us- 6378009 B1	4/23/2002	Pinkston, II et al.	
	us- 6401124 B1	6/4/2002	Yang et al.	
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	us- 6643777	11/4/2003	Chu	
	us- 6718415 B1	4/6/2004	Chu	
	us- 7099981	8/29/2006	Chu	
	us- 7146446 B2	12/5/2006	Chu	
	us- 7328297	2/5/2008	Chu	
	us- 7363415 B2	4/22/2008	Chu	
	us- 7363416	4/22/2008	Chu	
	us- 7376779	5/20/2008	Chu	
	us- 7676624 B2	3/9/2010	Chu	
	us- 7818487 B2	10/19/2010	Chu	
	us- 8041873	10/18/2011	Chu	
	us- 8234436	7/31/2012	Chu	
	us- RE41076	1/12/2010	Chu	
	us- RE41092	1/26/2010	Chu	
	us- RE41961	11/23/2010	Chu	
	us- RE41294	4/27/2010	Chu	
Examiner Signature	/Hosuk Song/		Date Considered	11/14/2012

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		Filing Date	July 30, 2012
		First Named Inventor	William W. Y. Chu
		Art Unit	
		Examiner Name	
Sheet 4 of 5	Attorney Docket Number	ACQI-006/05US 310578-2072	

/H.S./	US- RE42814	10/4/2011	Chu	
	US- RE42984	11/29/2011	Chu	
	US- RE43119	1/17/2012	Chu	
	US- RE43171	2/7/2012	Chu	
	US- 2001/0011312 A1	8/2/2001	Chu	
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	US- 2008/0244149 A1	10/2/2008	Chu	
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	US- 2010/0174844 A1	7/8/2010	Chu	
	US- 2011/0208893 A1	8/25/2011	Chu	
	US-			
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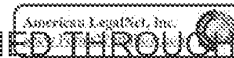
FOREIGN PATENT DOCUMENTS						
Examiner Initials*	Cite No. ¹	Foreign Patent Document Country Code ² Number ³ Kind Code ⁴ (if known)	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear	†
/H.S./		EP 0722138 A1	7/17/1996	International Business Machines Corporation		
		JP 6-289953	10/18/1994	Hitachi, Ltd.		
		WO 92/18924	10/29/1992	Wallsten		
		WO 94/00970	1/6/1994	Oakeigh Systems, Inc.		
		WO 95/13640	5/18/1995	Oakeigh Systems, Inc.		

Examiner Signature	 /Hosuk Song/	Date Considered	11/14/2012
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				Examiner Name	
				Attorney Docket Number	ACQI-006/05US 310578-2072
Sheet	5	of	5		

[illegible]

Examiner Signature	6-12-2011 /Hosuk Song/	Date Considered	11/14/2012
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This collection of information is required by 37 CFR 1.97 and 1.98. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 2 hours to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.

ALL REFERENCES CONSIDERED EXCEPT WHERE INDICATED THROUGHOUT /H.S./

EAST Search History**EAST Search History (Prior Art)**

Ref #	Hits	Search Query	DBs	Default Operator	Plurals	Time Stamp
S1	285	(low adj3 voltage adj4 differential adj4 signal) and serial adj3 bit adj4 channel	US-PGPUB; USPAT	OR	ON	2012/11/14 07:51
S2	25	(low adj3 voltage adj4 differential adj4 signal) and serial adj3 bit adj4 channel	US-PGPUB; USPAT	OR	ON	2012/11/14 07:51
S3	167	(low adj3 voltage adj4 differential adj4 signal) and serial adj3 bit	US-PGPUB; USPAT	OR	ON	2012/11/14 07:52
S4	294	(low adj3 voltage adj4 differential adj4 signal) and serial and USB	US-PGPUB; USPAT	OR	ON	2012/11/14 07:57
S5	249	(low adj3 voltage adj4 differential adj4 signal) and serial and PCI	US-PGPUB; USPAT	OR	ON	2012/11/14 08:00
S6	594	(low adj3 voltage adj4 differential adj4 signal or LVDS) and serial adj3 bit	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2012/11/14 10:58
S7	308	(low adj3 voltage adj4 differential adj4 signal or LVDS) and serial adj3 bit and (PCI or peripheral adj3 component adj4 interconnect)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2012/11/15 06:29
S8	337	(PCI or peripheral adj3 component adj4 interface) and (LVDS or low adj3 voltage adj4 differential adj5 signal) near5 (channel or link or path or line)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2012/11/15 07:52
S9	226	(PCI or peripheral adj3 component adj4 interface) and (LVDS or low adj3 voltage adj4 differential adj5 signal) and (serial adj3 bit) and (plug adj4 play or USB)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2012/11/15 07:53
S10	32	(PCI or peripheral adj3 component adj4 interface) and (LVDS or low adj3 voltage adj4 differential adj5 signal) near5 (channel or link or path or line or bus) near7 (plural\$4 or many or multiple or second)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2012/11/15 07:54
S11	287	(PCI or peripheral adj3 component adj4 interface) and (LVDS or low adj3 voltage adj4 differential adj5 signal) near5 (channel or link or path or line) and (both or unidirect\$4 or two adj3 way)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2012/11/15 08:04
S12	131	(PCI or peripheral adj3 component adj4 interface) and (LVDS or low adj3 voltage adj4 differential adj5 signal) near5 (channel or link or path or line) and (both or unidirect\$4 or two adj3 way) and (serial adj3 bit)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2012/11/15 08:09
S13	3346	726/2.ccls.	US-PGPUB;	OR	ON	2012/11/15

			USPAT; EPO; JPO; DERWENT; IBM_TDB			08:25
S14	3561	726/3.ccls.	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2012/11/15 08:26
S15	4734	726/4.ccls.	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2012/11/15 08:26
S16	2945	726/5.ccls.	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2012/11/15 08:32
S17	1920	726/6.ccls.	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2012/11/15 08:33
S18	1801	726/7.ccls.	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2012/11/15 08:33
S19	685	726/8.ccls.	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2012/11/15 08:37
S20	1457	726/9.ccls.	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2012/11/15 08:38
S21	671	726/16.ccls.	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2012/11/15 08:39
S22	1093	726/17.ccls.	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2012/11/15 08:40
S23	700	726/18.ccls.	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2012/11/15 08:41
S24	1044	726/19.ccls.	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2012/11/15 08:42
S25	683	726/20.ccls.	US-PGPUB;	OR	ON	2012/11/15

			USPAT; EPO; JPO; DERWENT; IBM_TDB			08:42
S26	1197	726/21.ccls.	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2012/11/15 08:43
S27	680	726/34.ccls.	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2012/11/15 08:51
S28	128	726/36.ccls.	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2012/11/15 08:51
S29	2735	713/182.ccls.	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2012/11/15 08:52
S30	1126	713/183.ccls.	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2012/11/15 08:52
S31	360	713/192.ccls.	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2012/11/15 08:52
S32	4419	713/193.ccls.	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2012/11/15 08:52
S33	1240	713/194.ccls.	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2012/11/15 08:52
S34	1722	710/1.ccls.	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2012/11/15 08:54
S35	364	710/7.ccls.	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2012/11/15 08:54
S36	3148	710/8.ccls.	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2012/11/15 08:54
S37	1906	710/15.ccls.	US-PGPUB;	OR	ON	2012/11/15

			USPAT; EPO; JPO; DERWENT; IBM_TDB			08:54
S38	762	710/20.ccls.	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2012/11/15 08:54
S39	2327	710/22.ccls.	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2012/11/15 08:54
S40	2091	710/100.ccls.	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2012/11/15 08:54
S41	1	(low adj3 voltage adj4 differential adj4 signal or LVDS) and serial adj3 bit and 710/1.ccls.	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2012/11/15 09:18
S42	0	(low adj3 voltage adj4 differential adj4 signal or LVDS) and serial adj3 bit and 710/7.ccls.	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2012/11/15 09:18
S43	0	(low adj3 voltage adj4 differential adj4 signal or LVDS) and serial adj3 bit and 710/8.ccls.	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2012/11/15 09:18
S44	0	(low adj3 voltage adj4 differential adj4 signal or LVDS) and serial adj3 bit and 710/15.ccls.	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2012/11/15 09:19
S45	0	(low adj3 voltage adj4 differential adj4 signal or LVDS) and serial adj3 bit and 710/20.ccls.	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2012/11/15 09:19
S46	1	(low adj3 voltage adj4 differential adj4 signal or LVDS) and serial adj3 bit and 710/22.ccls.	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2012/11/15 09:19
S47	5	(low adj3 voltage adj4 differential adj4 signal or LVDS) and serial adj3 bit and 710/100.ccls.	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2012/11/15 09:19
S48	4	(low adj3 voltage adj4 differential adj4 signal or LVDS) and serial adj3 bit and 726/2.ccls.	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2012/11/15 09:19
S49	1	(low adj3 voltage adj4 differential adj4	US-PGPUB;	OR	ON	2012/11/15

		signal or LVDS) and serial adj3 bit and 726/3.ccls.	USPAT; EPO; JPO; DERWENT; IBM_TDB			09:20
S50	1	(low adj3 voltage adj4 differential adj4 signal or LVDS) and serial adj3 bit and 726/4.ccls.	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2012/11/15 09:21
S51	0	(low adj3 voltage adj4 differential adj4 signal or LVDS) and serial adj3 bit and 726/5.ccls.	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2012/11/15 09:25
S52	0	(low adj3 voltage adj4 differential adj4 signal or LVDS) and serial adj3 bit and 726/6.ccls.	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2012/11/15 09:27
S53	1	(low adj3 voltage adj4 differential adj4 signal or LVDS) and serial adj3 bit and 726/7.ccls.	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2012/11/15 09:31
S54	0	(low adj3 voltage adj4 differential adj4 signal or LVDS) and serial adj3 bit and 726/8.ccls.	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2012/11/15 09:33
S55	3	(low adj3 voltage adj4 differential adj4 signal or LVDS) and serial adj3 bit and 726/9.ccls.	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2012/11/15 13:26
S56	0	(low adj3 voltage adj4 differential adj4 signal or LVDS) and serial adj3 bit and 726/16.ccls.	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2012/11/15 13:26
S57	0	(low adj3 voltage adj4 differential adj4 signal or LVDS) and serial adj3 bit and 726/17.ccls.	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2012/11/15 13:27
S58	3	(low adj3 voltage adj4 differential adj4 signal or LVDS) and serial adj3 bit and 726/18.ccls.	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2012/11/15 13:27
S59	0	(low adj3 voltage adj4 differential adj4 signal or LVDS) and serial adj3 bit and 726/19.ccls.	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2012/11/15 13:27
S60	0	(low adj3 voltage adj4 differential adj4 signal or LVDS) and serial adj3 bit and 726/20.ccls.	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2012/11/15 13:28
S61	0	(low adj3 voltage adj4 differential adj4	US-PGPUB;	OR	ON	2012/11/15

		signal or LVDS) and serial adj3 bit and 726/21.ccls.	USPAT; EPO; JPO; DERWENT; IBM_TDB			13:28
S62	2	(low adj3 voltage adj4 differential adj4 signal or LVDS) and serial adj3 bit and 726/34.ccls.	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2012/11/15 13:28
S63	2	(low adj3 voltage adj4 differential adj4 signal or LVDS) and serial adj3 bit and 726/36.ccls.	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2012/11/15 13:28
S64	0	(low adj3 voltage adj4 differential adj4 signal or LVDS) and serial adj3 bit and 713/182.ccls.	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2012/11/15 13:28
S65	2	(low adj3 voltage adj4 differential adj4 signal or LVDS) and serial adj3 bit and 713/183.ccls.	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2012/11/15 13:29
S66	0	(low adj3 voltage adj4 differential adj4 signal or LVDS) and serial adj3 bit and 713/192.ccls.	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2012/11/15 13:29
S67	5	(low adj3 voltage adj4 differential adj4 signal or LVDS) and serial adj3 bit and 713/193.ccls.	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2012/11/15 13:29
S68	0	(low adj3 voltage adj4 differential adj4 signal or LVDS) and serial adj3 bit and 713/194.ccls.	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2012/11/15 13:29

11/16/2012 6:34:59 AM

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BIB DATA SHEET


CONFIRMATION NO. 1045

SERIAL NUMBER 13/562,210	FILING or 371(c) DATE 07/30/2012 RULE	CLASS 726	GROUP ART UNIT 2435	ATTORNEY DOCKET NO. ACQI-006/05US 310578-2072	
APPLICANTS William W. Y. Chu, Los Altos, CA; ** CONTINUING DATA ***** This application is a CON of 13/294,108 11/10/2011 PAT R,E43,602 which is a CON of 12/561,138 09/16/2009 PAT R,E42,984 which is a CON of 11/056,604 02/10/2005 PAT R,E41,092 which is a REI of 09/312,199 05/14/1999 PAT 6,643,777 ** FOREIGN APPLICATIONS ***** ** IF REQUIRED, FOREIGN FILING LICENSE GRANTED ** 08/15/2012					
Foreign Priority claimed <input type="checkbox"/> Yes <input checked="" type="checkbox"/> No 35 USC 119(a-d) conditions met <input type="checkbox"/> Yes <input checked="" type="checkbox"/> No Verified and Acknowledged <u>/Hosuk Song/</u> Examiner's Signature	<input type="checkbox"/> Met after Allowance Initials _____	STATE OR COUNTRY CA	SHEETS DRAWINGS 8	TOTAL CLAIMS 41	INDEPENDENT CLAIMS 12
ADDRESS COOLEY LLP ATTN: Patent Group 777 - 6th Street, NW Suite 1100 WASHINGTON, DC 20001 UNITED STATES					
TITLE Data Security Method and Device for Computer Modules					
FILING FEE RECEIVED 5260	FEES: Authority has been given in Paper No. _____ to charge/credit DEPOSIT ACCOUNT No. _____ for following:		<input type="checkbox"/> All Fees <input type="checkbox"/> 1.16 Fees (Filing) <input type="checkbox"/> 1.17 Fees (Processing Ext. of time) <input type="checkbox"/> 1.18 Fees (Issue) <input type="checkbox"/> Other _____ <input type="checkbox"/> Credit		

<p align="center">Index of Claims</p> 	Application/Control No. 13562210	Applicant(s)/Patent Under Reexamination CHU, WILLIAM W. Y.
	Examiner HOSUK SONG	Art Unit 2435

✓	Rejected	-	Cancelled	N	Non-Elected	A	Appeal
=	Allowed	÷	Restricted	I	Interference	O	Objected

<input type="checkbox"/> Claims renumbered in the same order as presented by applicant			<input type="checkbox"/> CPA			<input type="checkbox"/> T.D.			<input type="checkbox"/> R.1.47		
CLAIM		DATE									
Final	Original	11/15/2012									
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	26	✓									
	27	✓									
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	36	=									

<p align="center"><i>Index of Claims</i></p> 	Application/Control No. 13562210	Applicant(s)/Patent Under Reexamination CHU, WILLIAM W. Y.
	Examiner HOSUK SONG	Art Unit 2435

✓	Rejected	-	Cancelled	N	Non-Elected	A	Appeal
=	Allowed	÷	Restricted	I	Interference	O	Objected

<input type="checkbox"/> Claims renumbered in the same order as presented by applicant			<input type="checkbox"/> CPA			<input type="checkbox"/> T.D.			<input type="checkbox"/> R.1.47		
CLAIM		DATE									
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	44	✓									
	45	O									
	46	O									
	47	✓									
	48	✓									
	49	O									
	50	✓									
	51	✓									
	52	✓									
	53	✓									
	54	✓									

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Reissue of:	William W.Y. Chu	Confirmation No.:	1045
Application No.:	13/562,210	Examiner:	Song, Hosuk
Filing Date:	July 30, 2012	Art Unit:	2435
For:	DATA SECURITY METHOD AND DEVICE FOR COMPUTER MODULES		

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P.O. Box 1450
Alexandria, VA 22313-1450

AMENDMENT

This communication is in response to the Office Action mailed November 19, 2012, please amend the present application as follows:

Amendments to the Claims begin on page 2.

Remarks begin on page 10.

The Commissioner is hereby authorized to charge any required fees and to credit any overpayments to Cooley LLP's deposit account No. 50-1283.

IN THE CLAIMS

1-13. (Cancelled)

14. (Previously Presented) A computer for information transactions, comprising:
a central processing unit directly connected to a first Low Voltage Differential Signal (LVDS) channel comprising two sets of unidirectional, serial bit channels to transmit data in opposite directions;
a main memory directly connected to the central processing unit; and
a peripheral bridge directly coupled to the central processing unit without any intervening Peripheral Component Interconnect (“PCI”) bus, wherein the peripheral bridge directly conveys an encoded serial bit stream of address and data bits of a PCI bus transaction over a second LVDS channel comprising two sets of unidirectional, serial bit channels to transmit data in opposite directions.

15. (Previously Presented) The computer of claim 14, further comprising a connector coupled to a console, wherein the second LVDS channel communicates the encoded serial bit stream of address and data bits of the PCI bus transaction to the console.

16. (Previously Presented) The computer of claim 15 further comprising a graphics controller that conveys digital video display information from the connector to the console.

17. (Previously Presented) The computer of claim 15 wherein the console comprises a mass storage device that couples to the second LVDS channel.

18. (Previously Presented) A computer system, comprising:
a console comprising a Liquid Crystal Display (LCD) display and a first Low Voltage Differential Signal (LVDS) channel comprising two sets of unidirectional, serial bit channels to transmit data in opposite directions; and
a computer coupled to the console through a connector, the computer comprising

an integrated central processing unit and graphics controller in a single chip directly connected to a second LVDS channel comprising two sets of unidirectional, serial bit channels to transmit data in opposite directions; and

a mass storage unit coupled to the central processing unit and graphics controller in a single chip;

wherein the graphics controller conveys digital video display information to the LCD display through the connector upon coupling to the console.

19. (Previously Presented) The computer system of claim 18 wherein the computer further comprises a peripheral bridge directly coupled to the central processing unit without any intervening Peripheral Component Interconnect (“PCI”) bus, the peripheral bridge directly conveying an encoded serial bit stream of address and data bits of a PCI bus transaction.

20. (Previously Presented) The computer system of claim 19 wherein the peripheral bridge conveys the encoded serial bit stream of address and data bits of the PCI bus transaction to the first LVDS channel upon coupling of the computer to the console.

21. (Previously Presented) A computer, comprising:

a central processing unit directly connected to a first Low Voltage Differential Signal (LVDS) channel comprising two sets of unidirectional, serial bit channels to transmit Universal Serial Bus (USB) Protocol data in opposite directions;

a second LVDS channel comprising two sets of unidirectional, serial bit channels to transmit data in opposite directions;

a connector coupled to the first LVDS channel; and

a main memory directly coupled to the central processing unit.

22. (Previously Presented) The computer of claim 21 wherein the second LVDS channel communicates an encoded serial bit stream of address and data bits of a Peripheral Component Interconnect (“PCI”) bus transaction.

23. (Previously Presented) The computer of claim 21 wherein the first LVDS channel conveys Universal Serial Bus (USB) Protocol data to a console through the connector.

24. (Currently Amended) A computer, comprising:

an integrated central processing unit and graphics controller in a single chip directly connected to a Low Voltage Differential Signal (LVDS) channel comprising two sets of unidirectional, serial bit channels to transmit data in opposite directions; [[and]]

a main memory directly coupled to the integrated central processing unit and graphics controller; [[and]]

a differential signal channel directly extending from the integrated central processing unit and graphics controller to convey digital video display information;

a connector for coupling to a console; and

a second differential signal channel comprising two sets of unidirectional, serial bit channels to transmit data in opposite directions, wherein the second differential signal channel conveys Universal Serial Bus (USB) protocol data through the connector to the console.

25. (Previously Presented) The computer of claim 24 wherein the LVDS channel conveys an encoded serial bit stream of address and data bits of a Peripheral Component Interconnect ("PCI") bus transaction.

26-28. (Cancelled)

29. (Previously Presented) A modular computer system, comprising:

a console comprising a first Low Voltage Differential Signal (LVDS) channel comprising two sets of unidirectional, serial bit channels to transmit data in opposite directions; and

a computer coupled to the console through a connector, the computer comprising

a central processing unit,

a mass storage unit coupled to the central processing unit,

a second LVDS channel comprising two sets of unidirectional, serial bit channels to transmit data in opposite directions, and

a peripheral bridge directly coupled to the central processing unit without any intervening Peripheral Component Interconnect bus, wherein the peripheral bridge directly conveys an encoded serial bit stream of address and data bits of a Peripheral Component Interconnect (“PCI”) bus transaction over the second LVDS channel; and

wherein the second LVDS channel communicates to the first LVDS channel in the console upon the computer coupling to the console.

30. (Previously Presented) The modular computer system of claim 29 wherein the second LVDS channel conveys the encoded serial bit stream of the PCI bus transaction to the first LVDS channel upon coupling of the computer module to the console.

31. (Previously Presented) The modular computer system of claim 30 wherein the console further comprises a mass storage device that couples to the first and second LVDS channels.

32. (Currently Amended) A modular computer system, comprising:
a console comprising a power supply; and
a computer coupled to the console through a connector, the computer comprising
a central processing unit,
a first Low Voltage Differential Signal (LVDS) channel comprising two sets of unidirectional, multiple serial bit channels to transmit data in opposite directions,
a peripheral bridge directly coupled to the first LVDS channel to communicate an encoded serial bit stream of address and data bits of a Peripheral Component Interconnect (“PCI”) bus transaction, the peripheral ~~controller~~ bridge directly coupled to the central processing unit without any intervening PCI bus, and
wherein the power supply supplies power to the computer upon coupling to the console.

33. (Previously Presented) The computer system of claim 32 further comprising a second LVDS channel that conveys the encoded serial bit stream of address and data bits of the PCI bus transaction, wherein the second LVDS channel directly extends from the central processing unit.

34. (Previously Presented) A modular computer system, comprising:
a console comprising a first Low Voltage Differential Signal (LVDS) channel comprising two sets of unidirectional, serial bit channels to transmit data in opposite directions; and
a computer that couples to the console, the computer comprising
an integrated central processing unit and graphics controller in a single chip, directly connected to a second LVDS channel comprising two sets of unidirectional, serial bit channels to transmit data in opposite directions, and
a connector that couples to the first LVDS channel in the console.
35. (Previously Presented) The modular computer system of claim 34 wherein the second LVDS channel conveys an encoded serial bit stream of address and data bits of a Peripheral Component Interconnect (“PCI”) bus transaction.
36. (Previously Presented) The modular computer system of claim 34 wherein the first LVDS channel conveys an encoded serial bit stream of address and data bits of a Peripheral Component Interconnect (“PCI”) bus transaction.
37. (Previously Presented) The modular computer system of claim 34 wherein the computer conveys Universal Serial Bus (USB) protocol data to the console upon the computer coupling to the console.
38. (Previously Presented) A computer, comprising:
a central processing unit;
a main memory directly connected to the central processing unit;
a peripheral bridge directly coupled to the central processing unit without any intervening Peripheral Component Interconnect (PCI) bus, wherein the peripheral bridge directly conveys an encoded serial bit stream of address and data bits of a Peripheral Component Interconnect (PCI) bus transaction over a first Low Voltage Differential Signal (LVDS) channel comprising two sets of unidirectional, serial bit channels to transmit data in opposite directions; and
a mass storage device directly coupled the peripheral bridge.

39. (Previously Presented) The computer of claim 38 further comprising a graphics controller coupled to the peripheral bridge.

40. (Currently Amended) A computer, comprising:

a central processing unit directly connected to a first Low Voltage Differential Signal (LVDS) channel to convey [[an]] a first encoded serial bit stream of address and data bits of a Peripheral Component Interconnect (PCI) bus transaction;

a main memory directly connected to the central processing unit; and

a peripheral bridge directly coupled to the central processing unit without any intervening PCI bus, wherein the peripheral bridge directly conveys [[the]] a second encoded serial bit stream of address and data bits of [[the]] a (PCI) bus transaction over a second LVDS channel comprising two sets of unidirectional, serial bit channels to transmit data in opposite directions.

41. (Currently Amended) The computer of claim 40 further comprising a connector coupled to a console, wherein the second LVDS channel communicates the second encoded serial bit stream of address and data bits of the PCI bus transaction to the console.

42. (Previously Presented) The computer of claim 41 further comprising a graphics controller to convey digital video display information from the connector to the console.

43. (Previously Presented) The computer of claim 41 wherein the console comprises a peripheral device that couples to the second LVDS channel.

44. (Currently Amended) A computer, comprising:

an integrated central processing unit and graphics controller in a single chip directly connected to a first Low Voltage Differential Signal (LVDS) channel comprising two sets of unidirectional, serial bit channels to transmit data in opposite directions, wherein the integrated central processing unit and graphics controller conveys digital video display signals through a second differential signal channel;

a main memory directly coupled to the integrated central processing unit and graphics controller; and

a mass storage device comprising flash memory.

45. (Cancelled)

46. (Currently Amended) The computer of claim [[45]] 44 wherein the second differential signal channel conveys Transition Minimized Differential Signaling (TDMS) information.

47. (Previously Presented) The computer of claim 44 wherein the first LVDS channel conveys an encoded serial bit stream of address and data bits of a Peripheral Component Interconnect (PCI) bus transaction.

48. (Cancelled)

49. (Currently Amended) ~~The computer of claim 48 further comprising~~ A computer, comprising:

an integrated central processing unit and graphics controller in a single chip directly connected to a first Low Voltage Differential Signal (LVDS) channel comprising two sets of unidirectional, serial bit channels to transmit data in opposite directions;

a main memory directly coupled to the integrated central processing unit and graphics controller;

a mass storage device comprising flash memory;

a connector that conveys Universal Serial Bus (USB) protocol information to a console;

and

a second LVDS channel comprising two sets of unidirectional, serial bit channels to transmit data in opposite directions, wherein the second LVDS channel conveys said USB protocol information to the console through the connector.

50. (Previously Presented) A computer, comprising:

a Central Processing Unit (CPU) directly connected to a Low Voltage Differential Signal (LVDS) channel comprising two sets of multiple, unidirectional, serial bit channels to convey an

encoded serial bit stream of encoded address and data bits of a Peripheral Component Interconnect (“PCI”) bus transaction in opposite directions;

a main memory directly connected to the CPU; and

a mass storage device coupled to the CPU.

51. (Previously Presented) The computer of claim 50 further comprising a connector, wherein the connector connects to a console comprising a power supply, and the power supply supplies power to the computer upon coupling to the console.

52. (Previously Presented) The computer of claim 50 wherein the mass storage device comprises flash memory.

53. (Previously Presented) A computer, comprising:

an integrated central processing unit and graphics controller in a single chip directly connected to a first Low Voltage Differential Signal (LVDS) channel comprising two sets of multiple, unidirectional, serial bit channels to convey an encoded serial bit stream of encoded address and data bits of a Peripheral Component Interconnect (PCI) bus transaction in opposite directions;

a main memory directly coupled to the integrated central processing unit and graphics controller; and

an Ethernet communication device coupled to the first LVDS channel.

54. (Previously Presented) The computer of claim 53 further comprising a connector, wherein the connector connects to a console comprising a power supply, and the power supply supplies power to the computer upon coupling to the console.

REMARKS

Applicant thanks the Examiner for the indication that claims 14-23 and 29-43 are allowed. Applicant further thanks the Examiner for the indication of the allowability of claims 28, 45, 46 and 49. Claim 24 is amended to incorporate the limitations of claims 28 and 26. Claims 26-28 are cancelled. Claim 44 is amended to incorporate the limitations of claim 45. Claim 46 is amended for dependency on claim 44. Claim 49 is amended to incorporate limitations from base claims 48 and 44. Claims 32, 40 and 41 are amended for antecedent clarity.

In view of the foregoing, claims 14-25, 29-44, 46-47 and 49 are in a condition for allowance. The only remaining claims of record are claims 50-54. Reconsideration of the rejection of these claims is respectfully requested.

Claim 50 specifies “*a central processing unit directly connected to a Low Voltage Differential Signal (LVDS) channel comprising two sets of multiple, unidirectional serial bit channels to convey an encoded serial bit stream of encoded address and data bits of a Peripheral Component Interconnect (PCI) bus transaction in opposite directions*”.

The Examiner maintains that this limitation is met by U.S. Patent 6,487,614 (Nobutani). Nobutani has a transmitter 2 with a serial encoder connected to unidirectional differential signal channels 15-18. This does not meet the claim limitation of a *central processing unit* directly coupled to an LVDS channel conveying *an encoded serial bit stream in opposite directions*.

Figure 2 of Nobutani discloses a PCI bus 201, but this is a standard parallel PCI bus. Nobutani does not contemplate the claimed *encoded serial bit stream of encoded address and data bits of a PCI bus transaction*. There is no teaching related to an *encoded serial bit stream of encoded address and data bits of a PCI bus transaction* that is conveyed on the claimed LVDS channel. In view of the foregoing, claim 50 and its dependent claims 51-52 should be in a condition for allowance.

Independent claim 53 recites “*an integrated central processing unit and graphics controller in a single chip*”. Nobutani does not disclose such a structure. The claim also recites an LVDS channel conveying “*an encoded serial bit stream of encoded address and data bits of a Peripheral Component Interconnect (PCI) bus transaction in opposite directions*.” Again, Nobutani discloses a standard parallel PCI bus, not the claimed LVDS channel conveying an

encoded PCI bus transaction in opposite directions. Accordingly, independent claim 53 and its dependent claim 54 should be in a condition for allowance.

In sum, all pending claims should be in a condition for allowance. If there are any residual issues that can be resolved through a telephone call, the Examiner is requested to contact the undersigned.

The Director is hereby authorized to charge any appropriate fees under 37 C.F.R. §§1.16, 1.17, and 1.21 that may be required by this paper, and to credit any overpayment, to Deposit Account No. 50-1283.

Date: January 31, 2013

Customer No. 58249
COOLEY LLP
1299 Pennsylvania Ave. NW, Suite 700
Washington, DC 20004

Tel: (650) 843-5622
Fax: (202) 842-7899

Respectfully submitted,
COOLEY LLP

By: 

William S. Galliani
Reg. No. 33,885

Electronic Acknowledgement Receipt	
EFS ID:	14848533
Application Number:	13562210
International Application Number:	
Confirmation Number:	1045
Title of Invention:	Data Security Method and Device for Computer Modules
First Named Inventor/Applicant Name:	William W. Y. Chu
Customer Number:	58249
Filer:	William S. Galliani/Bobbie Jutras
Filer Authorized By:	William S. Galliani
Attorney Docket Number:	ACQI-006/05US 310578-2072
Receipt Date:	31-JAN-2013
Filing Date:	30-JUL-2012
Time Stamp:	19:43:51
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	no
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File Listing:

Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1		ACQI-006-05US_2013-01-31_A mendment.pdf	126372 50d9312d64537aa8e379fb24f91a0f60870f6e5e	yes	11

	Multipart Description/PDF files in .zip description		
	Document Description	Start	End
	Amendment/Req. Reconsideration-After Non-Final Reject	1	1
	Claims	2	9
	Applicant Arguments/Remarks Made in an Amendment	10	11
Warnings:			
Information:			
Total Files Size (in bytes):		126372	
<p>This Acknowledgement Receipt evidences receipt on the noted date by the USPTO of the indicated documents, characterized by the applicant, and including page counts, where applicable. It serves as evidence of receipt similar to a Post Card, as described in MPEP 503.</p> <p><u>New Applications Under 35 U.S.C. 111</u> If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application.</p> <p><u>National Stage of an International Application under 35 U.S.C. 371</u> If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.</p> <p><u>New International Application Filed with the USPTO as a Receiving Office</u> If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.</p>			

Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it displays a valid OMB control number.

PATENT APPLICATION FEE DETERMINATION RECORD Substitute for Form PTO-875					Application or Docket Number 13/562,210		Filing Date 07/30/2012		<input type="checkbox"/> To be Mailed	
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APPLICATION AS FILED – PART I					OTHER THAN SMALL ENTITY				
(Column 1)		(Column 2)		SMALL ENTITY <input type="checkbox"/>		OR		SMALL ENTITY	
FOR	NUMBER FILED	NUMBER EXTRA	RATE (\$)	FEE (\$)	OR		RATE (\$)	FEE (\$)	
<input type="checkbox"/> BASIC FEE (37 CFR 1.16(a), (b), or (c))	N/A	N/A	N/A		OR		N/A		
<input type="checkbox"/> SEARCH FEE (37 CFR 1.16(k), (l), or (m))	N/A	N/A	N/A				N/A		
<input type="checkbox"/> EXAMINATION FEE (37 CFR 1.16(o), (p), or (q))	N/A	N/A	N/A				N/A		
TOTAL CLAIMS (37 CFR 1.16(j))	minus 20 =	*	X \$ =				X \$ =		
INDEPENDENT CLAIMS (37 CFR 1.16(h))	minus 3 =	*	X \$ =				X \$ =		
<input type="checkbox"/> APPLICATION SIZE FEE (37 CFR 1.16(s))			If the specification and drawings exceed 100 sheets of paper, the application size fee due is \$250 (\$125 for small entity) for each additional 50 sheets or fraction thereof. See 35 U.S.C. 41(a)(1)(G) and 37 CFR 1.16(s).						
<input type="checkbox"/> MULTIPLE DEPENDENT CLAIM PRESENT (37 CFR 1.16(j))									
			TOTAL				TOTAL		

* If the difference in column 1 is less than zero, enter "0" in column 2.

APPLICATION AS AMENDED – PART II					OTHER THAN SMALL ENTITY						
(Column 1)		(Column 2)		(Column 3)		SMALL ENTITY		OR		SMALL ENTITY	
AMENDMENT	01/31/2013	CLAIMS REMAINING AFTER AMENDMENT	HIGHEST NUMBER PREVIOUSLY PAID FOR	PRESENT EXTRA	RATE (\$)	ADDITIONAL FEE (\$)	OR		RATE (\$)	ADDITIONAL FEE (\$)	
Total (37 CFR 1.16(j))	*	36	Minus	** 41	=	0	OR		X \$62=	0	
Independent (37 CFR 1.16(h))	*	13	Minus	***12	=	1			X \$250=	250	
<input type="checkbox"/> Application Size Fee (37 CFR 1.16(s))											
<input type="checkbox"/> FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))											
						TOTAL ADD'L FEE		OR		TOTAL ADD'L FEE	250

(Column 1)		(Column 2)		(Column 3)		RATE (\$)	ADDITIONAL FEE (\$)	OR		RATE (\$)	ADDITIONAL FEE (\$)
AMENDMENT		CLAIMS REMAINING AFTER AMENDMENT		HIGHEST NUMBER PREVIOUSLY PAID FOR	PRESENT EXTRA	X \$ =		OR		X \$ =	
Total (37 CFR 1.16(j))	*		Minus	**	=	X \$ =				X \$ =	
Independent (37 CFR 1.16(h))	*		Minus	***	=					X \$ =	
<input type="checkbox"/> Application Size Fee (37 CFR 1.16(s))											
<input type="checkbox"/> FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))								OR			
						TOTAL ADD'L FEE		OR		TOTAL ADD'L FEE	

* If the entry in column 1 is less than the entry in column 2, write "0" in column 3.
 ** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 20, enter "20".
 *** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 3, enter "3".
 The "Highest Number Previously Paid For" (Total or Independent) is the highest number found in the appropriate box in column 1.

Legal Instrument Examiner:
/CAROL BARNES/

This collection of information is required by 37 CFR 1.16. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 12 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
13/562,210	07/30/2012	William W. Y. Chu	ACQI-006/05US 310578-2072	1045
58249	7590	02/21/2013		
COOLEY LLP ATTN: Patent Group 1299 Pennsylvania Avenue, NW Suite 700 Washington, DC 20004			EXAMINER SONG, HOSUK	
			ART UNIT 2435	PAPER NUMBER
			MAIL DATE 02/21/2013	DELIVERY MODE PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No. 13/562,210	Applicant(s) CHU, WILLIAM W. Y.	
	Examiner Hosuk Song	Art Unit 2435	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --
Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 31 January 2013.
- 2a) ☒ This action is **FINAL**. 2b) ☐ This action is non-final.
- 3) ☐ An election was made by the applicant in response to a restriction requirement set forth during the interview on _____; the restriction requirement and election have been incorporated into this action.
- 4) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 5) ☒ Claim(s) 14-25, 29-44, 46, 47 and 49-54 is/are pending in the application.
- 5a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 6) ☐ Claim(s) _____ is/are allowed.
- 7) ☒ Claim(s) 14-25, 29-44, 46, 47 and 49-54 is/are rejected.
- 8) ☐ Claim(s) _____ is/are objected to.
- 9) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

* If any claims have been determined allowable, you may be eligible to benefit from the **Patent Prosecution Highway** program at a participating intellectual property office for the corresponding application. For more information, please see http://www.uspto.gov/patents/init_events/pph/index.jsp or send an inquiry to PPHfeedback@uspto.gov.

Application Papers

- 10) ☐ The specification is objected to by the Examiner.
- 11) ☒ The drawing(s) filed on 30 July 2012 is/are: a) ☒ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some * c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
 2. ☐ Certified copies of the priority documents have been received in Application No. _____.
 3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- | | |
|--|---|
| 1) <input type="checkbox"/> Notice of References Cited (PTO-892) | 3) <input type="checkbox"/> Interview Summary (PTO-413)
Paper No(s)/Mail Date. _____ |
| 2) <input type="checkbox"/> Information Disclosure Statement(s) (PTO/SB/08)
Paper No(s)/Mail Date _____ | 4) <input type="checkbox"/> Other: _____ |

DETAILED ACTION

Reissue Applications

In accordance with 37 CFR 1.175(b)(1), a supplemental reissue oath/declaration under 37 CFR 1.175(b)(1) must be received before this reissue application can be allowed. Supplemental reissue oath is needed as there have been amendment filed (1/31/13) since the filing of the last oath.

Claims 14-25,29-44,46-47,49-54 are rejected as being based upon a defective reissue under 35 U.S.C. 251. See 37 CFR 1.175. The nature of the defect is set forth above.

Receipt of an appropriate supplemental oath/declaration under 37 CFR 1.175(b)(1) will overcome this rejection under 35 U.S.C. 251. An example of acceptable language to be used in the supplemental oath/declaration is as follows:

“Every error in the patent which was corrected in the present reissue application, and is not covered by a prior oath/declaration submitted in this application, arose without any deceptive intention on the part of the applicant.”

See MPEP § 1414.01.

Response to Applicant's Arguments

The previous ground of rejection based on Nobutani patent is withdrawn in view of applicant's argument filed 1/31/13. However, Claims 14-25,29-44,46-47,49-54 are rejected as being based upon a defective reissue under 35 U.S.C. 251. See 37 CFR 1.175. See rejection above.

Conclusion

THIS ACTION IS MADE FINAL. Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of

Art Unit: 2435

the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.


USPTO Contact Information

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Hosuk Song whose telephone number is (571)272-3857. The examiner can normally be reached on mon-fri.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Kambiz Zand can be reached on 5712723811. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/Hosuk Song/
Primary Examiner, Art Unit 2435

Search Notes 	Application/Control No. 13562210	Applicant(s)/Patent Under Reexamination CHU, WILLIAM W. Y.
	Examiner HOSUK SONG	Art Unit 2435

CPC- SEARCHED		
Symbol	Date	Examiner

CPC COMBINATION SETS - SEARCHED		
Symbol	Date	Examiner

US CLASSIFICATION SEARCHED			
Class	Subclass	Date	Examiner
726	2-9,16-21,34,36	2/13/13	HS
713	182-183,192-194	2/13/13	HS
710	1,7,8,15,20,22,100	2/13/13	HS

SEARCH NOTES		
Search Notes	Date	Examiner
EAST, foreign patent database, IBM TDB, USPGPUB	2/13/13	HS
NPL	2/13/13	HS

INTERFERENCE SEARCH			
US Class/ CPC Symbol	US Subclass / CPC Group	Date	Examiner

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US Patent & Trademark Office

SIGN IN SIGN UP

LVDS

Searching for: LVDS ([start a new search](#))Found **248** within *The ACM Guide to Computing Literature* (Bibliographic citations from major publishers in computing)Limit your search to [Publications from ACM and Affiliated Organizations](#) (Full-Text collection: **371,076** items)

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Refine by Keywords
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1 [Using At-Speed BIST to Test LVDS Serializer/Deserializer Function](#)

Magnus Eickersand, Fredrik Franzen, Ken Fritter

April 2002

Journal of Electronic Testing: Theory and Applications, Volume 18 Issue 2**Publisher:** Kluwer Academic PublishersFull text available: [Publisher Site](#)**Bibliometrics:** Downloads (6 Weeks): n/a, Downloads (12 Months): n/a, Downloads (Overall): n/a, Citation Count

LVDS is the acronym for Low-Voltage-Differential-Signaling and is described in both the ANSI/TIA/EIA-644 and IEEE 1596.3 standards. High performance yet Low Power and EMI have made LVDS a popular choice for high-speed card-to-card serial links. A typical ...

Keywords: At-speed, BIST, LVDS, differential2 [A high speed low jitter LVDS output driver for serial links](#)

Junsheng Lv, Hao Ju, Li Yuan, Jianzhong Zhao, Feng Zhang, Bin Wu, Jianhua Jiang, Yumei Zhou

September 2011

Analog Integrated Circuits and Signal Processing, Volume 68 Issue 3**Publisher:** Kluwer Academic Publishers**Bibliometrics:** Downloads (6 Weeks): n/a, Downloads (12 Months): n/a, Downloads (Overall): n/a, Citation Count

A high speed, low jitter low voltage differential signaling (LVDS) output driver for high speed serial transmissi is presented. Based on the comparison among four typical output driver architectures and the analysis of the output signal swing, an additional ...

Keywords: Bandgap reference, High speed serial link, Low jitter, Low voltage differential signaling, Output driver3 [Design of an all-digital LVDS driver](#)

Hungwen Lu, Hsin-Wen Wang, Chauchin Su, Chen-Nan Jimmy Lu

August 2009

IEEE Transactions on Circuits and Systems Part I: Regular Papers, Volume 56 Issue 8**Publisher:** IEEE Press**Bibliometrics:** Downloads (6 Weeks): n/a, Downloads (12 Months): n/a, Downloads (Overall): n/a, Citation Count

This paper presents an all-digital low-voltage-differential-signaling (LVDS) driver design for Serial Advanced Technology Attachment II. A simultaneous-switching-noise reduction technique and an autocalibration mechanism are implemented to suppress switching ...

Keywords: low-voltage-differential-signaling (LVDS) driver, simultaneous switching noise (SSN)4 [An ultralow-power 10-Gbits/s LVDS output driver](#)

Khaidoon Abugharbieh, Shoba Krishnan, Jitendra Mohan, Varadarajan Devnath, Ivan Duzevik

January 2010

IEEE Transactions on Circuits and Systems Part I: Regular Papers, Volume 57 Issue**Publisher:** IEEE Press**Bibliometrics:** Downloads (6 Weeks): n/a, Downloads (12 Months): n/a, Downloads (Overall): n/a, Citation Count

This paper describes a new topology and implementation of a 10-Gbits/s low-voltage differential-signaling (LVDS) voltage-mode output driver designed for high-speed data-transfer applications. Using a positive-feedback technique, the driver achieves ultralow-power ...

Keywords: impedance matching, low power, low-voltage differential signaling (LVDS), output drivers5 [A VLSI for deskewing and fault tolerance in LVDS links](#)

Gloria Torralba, Veselin Angelov, Vicente González, Ivan Kisel, Volker Lindenstruth, Juno Marcos, Christian Reichling, Enrique Sanchez, Jesus Soret, José Torres

June 2005

RTC'05: Proceedings of the 14th IEEE-NPSS conference on Real time**Publisher:** IEEE Computer Society

ADVANCED SEARCH

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Bibliometrics: Downloads (6 Weeks): n/a, Downloads (12 Months): n/a, Downloads (Overall): n/a, Citation Count

The device presented at this work is a switch implemented in a 0.35 μm CMOS process for compensating the skew which affects parallel data signal transmissions and for providing fault tolerance in large scale scalable systems, for instance used in ...

Keywords: LVDS, delay units, fault tolerance, granularity, parallel links, skew compensation

6 [LVDS-type on-chip transmission line interconnect with passive equalizers in 90 nm CMOS process](#)

[Akiko Miyayama, Hiroyuki Ito, Takahiro Ishii, Kenichi Okada, Kazuya Masu](#)

January 2008

ASP-DAC '08: Proceedings of the 2008 Asia and South Pacific Design Automation Conference

Publisher: IEEE Computer Society Press

Full text available: [PDF](#) (186.72 KB)

Bibliometrics: Downloads (6 Weeks): 1, Downloads (12 Months): 7, Downloads (Overall): 78, Citation Count:

This paper demonstrates a low voltage differential signaling (LVDS)-type on-chip transmission line (TL) interconnect to solve delay issues on global interconnects. The proposed on-chip TL interconnect can achieve 10.5 Gbps signaling and has smaller delay, ...

7 [The Design of Bi-CMOS LVDS Output Buffer with ESD Protection Circuit Using 90nm CMOS Technology](#)

[Yongseok Koo, Kwangyeob Lee, Jaeshang Kwack, Jongil Won, Kuidong Kim](#)

September 2008

ENICS '08: Proceedings of the 2008 International Conference on Advances in Electronics and Micro-electronics

Publisher: IEEE Computer Society

Full text available: [Publisher Site](#)

Bibliometrics: Downloads (6 Weeks): n/a, Downloads (12 Months): n/a, Downloads (Overall): n/a, Citation Count

This paper presents the design of novel LVDS (Low-Voltage-Differential-Signaling) output buffer for Gb/s per-p operation using 90nm CMOS technology. The proposed LVDS driver is designed to reduce chip area, using a novel bipolar transistor switch. The ...

Keywords: LVDS, Bi-CMOS, ESD, 90nm CMOS

8 [A LVDS Transceiver Chip Design in 0.5 \$\mu\text{m}\$ CMOS Technology](#)

[Fei Zhao, Yong Xu, Miaoying Li, Chaoling Shen, Lu Tang](#)

May 2008

CISP '08: Proceedings of the 2008 Congress on Image and Signal Processing, Vol. 1 - Volume 01, Volume 01

Publisher: IEEE Computer Society

Full text available: [Publisher Site](#)

Bibliometrics: Downloads (6 Weeks): n/a, Downloads (12 Months): n/a, Downloads (Overall): n/a, Citation Count

The paper presents the design and implementation of input/output interface circuits, fully compatible with low voltage differential signal (LVDS) standard. Due to the low voltage differential transmission technique, the low power consumption and high ...

Keywords: LVDS, low power consumption, high transmission speed

9 [Using At-Speed BIST to Test LVDS Serializer/Deserializer Function](#)

[Magnus Eckersand, Ken Fällster, Fredrik Franzen](#)

May 2001

ETW '01: Proceedings of the IEEE European Test Workshop (ETW'01)

Publisher: IEEE Computer Society

Full text available: [Publisher Site](#)

Bibliometrics: Downloads (6 Weeks): n/a, Downloads (12 Months): n/a, Downloads (Overall): n/a, Citation Count

LVDS has become a popular choice for high-speed card-to-card serial links. A typical application is the serializer/deserializer (ser/des) function where wide TTL datastreams including clock is converted to a serial LVDS bit stream, sent over a cable, ...

10 [SCI-LVDS 500 MHz differential pad drivers in a standard CMOS process](#)

[Oluf Bagger, Thomas Nielsen, Kim Schultze](#)

January 1995

Analog Integrated Circuits and Signal Processing, Volume 7 Issue 1

Publisher: Kluwer Academic Publishers

Bibliometrics: Downloads (6 Weeks): n/a, Downloads (12 Months): n/a, Downloads (Overall): n/a, Citation Count

11 [Design and realization of 1.3 Gb/s off-chip transmission circuitry using 0.35 \$\mu\text{m}\$ CMOS technology](#)

[Heng-Shou Hsu, Yu-Hong Chang](#)

June 2012 **Analog Integrated Circuits and Signal Processing** , Volume 71 Issue 3

Publisher: Kluwer Academic Publishers

Bibliometrics: Downloads (6 Weeks): n/a, Downloads (12 Months): n/a, Downloads (Overall): n/a, Citation Count

Low-voltage-differential-signaling (LVDS) is one of the very popular technologies which simultaneously addresses low dynamic power consumption and high data rate transmission in modern high speed circuit applications. In this paper, system level integration ...

Keywords: Data rate, High-speed transmitter, Low dynamic power consumption, Low voltage differential signaling (LVDS), Off-chip data transmission

12 High-speed driver with built-in self detection functions for off-chip transmission

Heng-Shou Hsu, Guan-Yu Lu

October 2012

Analog Integrated Circuits and Signal Processing , Volume 73 Issue 1

Publisher: Kluwer Academic Publishers

Bibliometrics: Downloads (6 Weeks): n/a, Downloads (12 Months): n/a, Downloads (Overall): n/a, Citation Count

Although low-voltage differential signaling (LVDS) is one of the very popular technologies which simultaneously address low dynamic power consumption and high data rate transmission in modern high speed circuit applications. However, signal integrity ...


Keywords: Built-in self detection, High-speed driver, Low voltage differential signaling (LVDS), Signal integrity

13 Design and implementation of a switched bus-based home network interconnection system

Yang-Keun Ahn, Kwang-Seon Choi, Young-Choon Park, Kwang-Mo Jung, Seong-Dong Kim

May 2006 **TELE-INFO'06: Proceedings of the 5th WSEAS international conference on Telecommunications and informatics**

Publisher: World Scientific and Engineering Academy and Society (WSEAS)

Full text available:  [Publisher Site](#)

Bibliometrics: Downloads (6 Weeks): n/a, Downloads (12 Months): n/a, Downloads (Overall): n/a, Citation Count

In this paper, we present the design of a Home Network System using a HomeStation-Chipset based on Serial Switched Bus Technology. We describe the features of HomeStation-Chipset, a Serial Switched Bus Technology. The Home Network System Bus, which is ...

Keywords: LVDS, SerDes, home network, interconnection networks, switched bus

14 DSP/FPGA-based Controller Architecture for Flexible Joint Robot with Enhanced Impedance Performance

J.B. Huang, Z.W. Xie, H. Liu, K. Sun, Y.Q. Liu, Z.N. Jiang

November 2008

Journal of Intelligent and Robotic Systems , Volume 53 Issue 3

Publisher: Kluwer Academic Publishers

Bibliometrics: Downloads (6 Weeks): n/a, Downloads (12 Months): n/a, Downloads (Overall): n/a, Citation Count

Some practical issues associated with enhancing the Cartesian impedance performance of flexible joint manipulator are investigated. A digital signal processing/field programmable gate array (DSP/FPGA) structure proposed to realize the singular perturbation ...


Keywords: DSP, FPGA, Flexible joint, Impedance control, M-LVDS serial data bus, Torque ripple

15 An all-digital phase-locked loop with high resolution for local on-chip clock synthesis

Oliver Schrape, Frank Winkler, Steffen Zedler, Markus Petri, Eckhard Grass, Ulrich Jagdhold

September 2010 **PATMOS'10: Proceedings of the 20th international conference on Integrated circuit and system design: power and timing modeling, optimization and simulation**

Publisher: Springer-Verlag

Full text available:  [Publisher Site](#)

Bibliometrics: Downloads (6 Weeks): n/a, Downloads (12 Months): n/a, Downloads (Overall): n/a, Citation Count

In this paper an All-Digital Phase-Locked Loop (ADPLL) with a high resolution and a wide frequency range for local on-chip clock generation is described. The proposed ADPLL has an operating range from 250MHz to 1.3GHz and a resolution of 25 ps. In contrast ...

Keywords: ADPLL, LVDS, PID controller, all-digital phase-locked loop, clock generator, event driven matlab model

16 Design of D-PHY chip for mobile display interface supporting MIPI standard

Doo-Hwan Kim, Beom-Dae Kim, Kyoungrok Cho

December 2012

Microelectronics Journal , Volume 43 Issue 12

Publisher: Elsevier Science Publishers B. V.

Bibliometrics: Downloads (6 Weeks): n/a, Downloads (12 Months): n/a, Downloads (Overall): n/a, Citation Count

This paper presents a MIPI (Mobile Industry Processor Interface) D-PHY (physical layer) analog part that meet the MIPI Alliance standard that supports high-speed (HS) transmitter (HS-TX) and receiver (HS-RX) modes as

well as low-power (LP)-TX, LP-RX, ...

Keywords: D-PHY, LVDS, MIPI (Mobile Industry Processor Interface), SLVS, Small swing

17 [2 Gbps SerDes design based on IBM Cu-11 \(130nm\) standard cell technology](#)

[Hashed Zafer Bhatti, Manly Deneau, Jeff Draper](#)

April 2006

GLSVLSI '06: Proceedings of the 16th ACM Great Lakes symposium on VLSI

Publisher: ACM [Request Permissions](#)

Full text available: [PDF](#) (392.48 KB)

Bibliometrics: Downloads (6 Weeks): 5, Downloads (12 Months): 16, Downloads (Overall): 378, Citation Count:

This paper introduces a standard cell based design for a Serializer and Deserializer (SerDes) communication link. The proposed design is area, power and design time efficient as compared to conventional SerDes Designs, making it very attractive for modest ...

Keywords: CDR, CML driver, DLL, LVDS, PLL, SerDes, duty cycle correction (DCC), jitter and skew compensation, phase detection, standard cell based serializer and deserializer circuits for high speed signaling

18 [The design of image acquisition system based on CMOS digital](#)

[Chen Lei, Liu Ying, Li Xingguang, Chen Dianren](#)

November 2009 **IITA'09:** Proceedings of the 3rd international conference on Intelligent information technology application

Publisher: IEEE Press

Bibliometrics: Downloads (6 Weeks): n/a, Downloads (12 Months): n/a, Downloads (Overall): n/a, Citation Count

A low power consumption image acquisition system with the core controller of CPLD, based on LVDS interface and CMOS digital image sensor was designed here. We analyzed the work timing of LVDS interface ship DS90C124 and CMOS digital image sensor MT9V011, ...

Keywords: CMOS digital image sensor, CPLD, LVDS interface, image acquisition system

19 [The Design of Image Acquisition System Based on CMOS Digital Image Sensor](#)

[Chen Lei, Liu Ying, Li Xingguang, Chen Dianren](#)

November 2009 **IITA '09: Proceedings of the 2009 Third International Symposium on Intelligent Information Technology Application - Volume 03**, Volume 03

Publisher: IEEE Computer Society

Full text available: [Publisher Site](#)

Bibliometrics: Downloads (6 Weeks): n/a, Downloads (12 Months): n/a, Downloads (Overall): n/a, Citation Count

A low power consumption image acquisition system with the core controller of CPLD, based on LVDS interface and CMOS digital image sensor was designed here. We analyzed the work timing of LVDS interface ship DS90C124 and CMOS digital image sensor MT9V011, ...

Keywords: CMOS digital image sensor, LVDS interface, CPLD, image acquisition system

20 [Research on LXI Trigger Bus](#)

[Li Zhi, Zhou Fenglong, Yao Xuejuan](#)

May 2009

ICCESS '09: Proceedings of the 2009 International Conference on Embedded Software and Systems

Publisher: IEEE Computer Society

Full text available: [Publisher Site](#)

Bibliometrics: Downloads (6 Weeks): n/a, Downloads (12 Months): n/a, Downloads (Overall): n/a, Citation Count

LXI (LAN eXtensions for Instrumentation), which is a new generation automation test system platform based on the mature Ethernet, has become an open-standard in the test and measure fields, and also LXI trigger bus is one key functional attribute for ...

Keywords: LXI, trigger bus, M-LVDS

Result page: [1](#) [2](#) [3](#) [4](#) [5](#) [6](#) [7](#) [8](#) [9](#) [10](#) [next](#)

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EAST Search History**EAST Search History (Prior Art)**

Ref #	Hits	Search Query	DBs	Default Operator	Plurals	Time Stamp
S69	29	(low adj3 voltage adj4 differential adj4 signal or LVDS) and serial adj3 bit adj4 channel	US-PGPUB; USPAT	OR	ON	2013/02/13 10:14
S70	31	(low adj3 voltage adj4 differential adj4 signal or LVDS) and serial adj3 bit adj4 channel	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2013/02/13 10:14
S71	604	(low adj3 voltage adj4 differential adj4 signal or LVDS) and serial adj3 bit	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2013/02/13 10:15
S72	1471	(low adj3 voltage adj4 differential adj4 signal or LVDS) and serial and USB	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2013/02/13 10:15
S73	1052	(low adj3 voltage adj4 differential adj4 signal or LVDS) and serial and PCI	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2013/02/13 10:16
S74	309	(low adj3 voltage adj4 differential adj4 signal or LVDS) and serial adj3 bit and (PCI or peripheral adj3 component adj4 interconnect)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2013/02/13 10:17
S75	1744	710/1.ccls.	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2013/02/13 10:17
S76	373	710/7.ccls.	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2013/02/13 10:17
S77	3217	710/8.ccls.	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2013/02/13 10:17
S78	1956	710/15.ccls.	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2013/02/13 10:18
S79	775	710/20.ccls.	US-PGPUB;	OR	ON	2013/02/13

			USPAT; EPO; JPO; DERWENT; IBM_TDB			10:18
S80	2374	710/22.ccls.	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2013/02/13 10:18
S81	2109	710/100.ccls.	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2013/02/13 10:18
S82	2815	713/182.ccls.	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2013/02/13 10:18
S83	1165	713/183.ccls.	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2013/02/13 10:18
S84	377	713/192.ccls.	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2013/02/13 10:18
S85	4549	713/193.ccls.	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2013/02/13 10:18
S86	1278	713/194.ccls.	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2013/02/13 10:18
S87	3529	726/2.ccls.	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2013/02/13 10:18
S88	3764	726/3.ccls.	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2013/02/13 10:19
S89	5003	726/4.ccls.	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2013/02/13 10:19
S90	3098	726/5.ccls.	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2013/02/13 10:19
S91	2033	726/6.ccls.	US-PGPUB;	OR	ON	2013/02/13

			USPAT; EPO; JPO; DERWENT; IBM_TDB			10:19
S92	1927	726/7.ccls.	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2013/02/13 10:20
S93	717	726/8.ccls.	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2013/02/13 10:20
S94	1526	726/9.ccls.	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2013/02/13 10:20
S95	702	726/16.ccls.	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2013/02/13 10:20
S96	1158	726/17.ccls.	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2013/02/13 10:22
S97	737	726/18.ccls.	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2013/02/13 10:23
S98	1103	726/19.ccls.	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2013/02/13 10:25
S99	714	726/20.ccls.	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2013/02/13 10:36
S100	1254	726/21.ccls.	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2013/02/13 10:38
S101	712	726/34.ccls.	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2013/02/13 10:39
S102	140	726/36.ccls.	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2013/02/13 10:39
S103	132	(PCI or peripheral adj3 component adj4	US-PGPUB;	OR	ON	2013/02/13


		interface) and (LVDS or low adj3 voltage adj4 differential adj5 signal) near5 (channel or link or path or line) and (both or unidirect\$4 or two adj3 way) and (serial adj3 bit)	USPAT; EPO; JPO; DERWENT; IBM_TDB			10:49
S104	227	(PCI or peripheral adj3 component adj4 interface) and (LVDS or low adj3 voltage adj4 differential adj5 signal) and (serial adj3 bit) and (plug adj4 play or USB)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2013/02/13 11:11
S105	33	(PCI or peripheral adj3 component adj4 interface) and (LVDS or low adj3 voltage adj4 differential adj5 signal) near5 (channel or link or path or line or bus) near7 (plural\$4 or many or multiple or second)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2013/02/13 11:15
S106	1	(low adj3 voltage adj4 differential adj4 signal or LVDS) and serial adj3 bit and 710/1.ccls.	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2013/02/13 11:16
S107	0	(low adj3 voltage adj4 differential adj4 signal or LVDS) and serial adj3 bit and 710/7.ccls.	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2013/02/13 11:16
S108	0	(low adj3 voltage adj4 differential adj4 signal or LVDS) and serial adj3 bit and 710/8.ccls.	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2013/02/13 11:16
S109	0	(low adj3 voltage adj4 differential adj4 signal or LVDS) and serial adj3 bit and 710/15.ccls.	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2013/02/13 11:17
S110	0	(low adj3 voltage adj4 differential adj4 signal or LVDS) and serial adj3 bit and 710/20.ccls.	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2013/02/13 11:17
S111	1	(low adj3 voltage adj4 differential adj4 signal or LVDS) and serial adj3 bit and 710/22.ccls.	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2013/02/13 11:18
S112	5	(low adj3 voltage adj4 differential adj4 signal or LVDS) and serial adj3 bit and 710/100.ccls.	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2013/02/13 11:19
S113	0	(low adj3 voltage adj4 differential adj4 signal or LVDS) and serial adj3 bit and 713/182.ccls.	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2013/02/13 11:21
S114	2	(low adj3 voltage adj4 differential adj4 signal or LVDS) and serial adj3 bit and 713/183.ccls.	US-PGPUB; USPAT; EPO; JPO; DERWENT;	OR	ON	2013/02/13 11:21

			IBM_TDB			
S115	0	(low adj3 voltage adj4 differential adj4 signal or LVDS) and serial adj3 bit and 713/192.ccls.	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2013/02/13 11:22
S116	5	(low adj3 voltage adj4 differential adj4 signal or LVDS) and serial adj3 bit and 713/193.ccls.	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2013/02/13 11:25
S117	0	(low adj3 voltage adj4 differential adj4 signal or LVDS) and serial adj3 bit and 713/194.ccls.	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2013/02/13 11:25
S118	4	(low adj3 voltage adj4 differential adj4 signal or LVDS) and serial adj3 bit and 726/2.ccls.	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2013/02/13 11:37
S119	1	(low adj3 voltage adj4 differential adj4 signal or LVDS) and serial adj3 bit and 726/3.ccls.	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2013/02/13 11:37
S120	1	(low adj3 voltage adj4 differential adj4 signal or LVDS) and serial adj3 bit and 726/4.ccls.	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2013/02/13 11:38
S121	0	(low adj3 voltage adj4 differential adj4 signal or LVDS) and serial adj3 bit and 726/5.ccls.	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2013/02/13 11:39
S122	0	(low adj3 voltage adj4 differential adj4 signal or LVDS) and serial adj3 bit and 726/6.ccls.	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2013/02/13 11:40
S123	1	(low adj3 voltage adj4 differential adj4 signal or LVDS) and serial adj3 bit and 726/7.ccls.	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2013/02/13 11:40
S124	0	(low adj3 voltage adj4 differential adj4 signal or LVDS) and serial adj3 bit and 726/8.ccls.	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2013/02/13 11:40
S126	3	(low adj3 voltage adj4 differential adj4 signal or LVDS) and serial adj3 bit and 726/9.ccls.	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2013/02/13 11:40
S127	0	(low adj3 voltage adj4 differential adj4 signal or LVDS) and serial adj3 bit and 726/16.ccls.	US-PGPUB; USPAT; EPO; JPO; DERWENT;	OR	ON	2013/02/13 11:41

			IBM_TDB			
S128	0	(low adj3 voltage adj4 differential adj4 signal or LVDS) and serial adj3 bit and 726/17.ccls.	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2013/02/13 11:41
S129	3	(low adj3 voltage adj4 differential adj4 signal or LVDS) and serial adj3 bit and 726/18.ccls.	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2013/02/13 11:41
S130	0	(low adj3 voltage adj4 differential adj4 signal or LVDS) and serial adj3 bit and 726/19.ccls.	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2013/02/13 11:41
S131	0	(low adj3 voltage adj4 differential adj4 signal or LVDS) and serial adj3 bit and 726/20.ccls.	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2013/02/13 11:42
S132	0	(low adj3 voltage adj4 differential adj4 signal or LVDS) and serial adj3 bit and 726/21.ccls.	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2013/02/13 11:42
S133	2	(low adj3 voltage adj4 differential adj4 signal or LVDS) and serial adj3 bit and 726/34.ccls.	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2013/02/13 11:42
S134	2	(low adj3 voltage adj4 differential adj4 signal or LVDS) and serial adj3 bit and 726/36.ccls.	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2013/02/13 11:42


2/ 14/ 2013 6:28:53 AM

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<p align="center">Index of Claims</p> 	Application/Control No. 13562210	Applicant(s)/Patent Under Reexamination CHU, WILLIAM W. Y.
	Examiner HOSUK SONG	Art Unit 2435

✓	Rejected	-	Cancelled	N	Non-Elected	A	Appeal
=	Allowed	÷	Restricted	I	Interference	O	Objected

<input type="checkbox"/> Claims renumbered in the same order as presented by applicant				<input type="checkbox"/> CPA		<input type="checkbox"/> T.D.		<input type="checkbox"/> R.1.47	
CLAIM		DATE							
Final	Original	11/15/2012	02/13/2013						
	1	-	-						
	2	-	-						
	3	-	-						
	4	-	-						
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	8	-	-						
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	13	-	-						
	14	=	✓						
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	26	✓	-						
	27	✓	-						
	28	O	-						
	29	=	✓						
	30	=	✓						
	31	=	✓						
	32	=	✓						
	33	=	✓						
	34	=	✓						
	35	=	✓						
	36	=	✓						

<p align="center"><i>Index of Claims</i></p> 	Application/Control No. 13562210	Applicant(s)/Patent Under Reexamination CHU, WILLIAM W. Y.
	Examiner HOSUK SONG	Art Unit 2435

✓	Rejected	-	Cancelled	N	Non-Elected	A	Appeal
=	Allowed	÷	Restricted	I	Interference	O	Objected

<input type="checkbox"/> Claims renumbered in the same order as presented by applicant				<input type="checkbox"/> CPA		<input type="checkbox"/> T.D.		<input type="checkbox"/> R.1.47	
CLAIM		DATE							
Final	Original	11/15/2012	02/13/2013						
	37	=	✓						
	38	=	✓						
	39	=	✓						
	40	=	✓						
	41	=	✓						
	42	=	✓						
	43	=	✓						
	44	✓	✓						
	45	O	-						
	46	O	✓						
	47	✓	✓						
	48	✓	-						
	49	O	✓						
	50	✓	✓						
	51	✓	✓						
	52	✓	✓						
	53	✓	✓						
	54	✓	✓						

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re application of:
William W. Y. Chu

Confirmation No.: 1045

Serial No.: 13/562,210

Examiner: Song, Hosuk

Filed: July 30, 2012

Art Unit: 2435

For: DATA SECURITY METHOD AND DEVICE FOR COMPUTER MODULES

Mail Stop Amendment
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

RESPONSE

This communication is in response to the final Office Action mailed February 21, 2013.

Remarks begin on page 2.

The Commissioner is hereby authorized to charge any required fees and to credit any overpayments to Cooley LLP's deposit account No. 50-1283.

REMARKS

Applicant submits a supplemental declaration for reissue patent application to overcome the rejection. Accordingly, the application is in a condition for allowance.

Date: April 17, 2013

Customer No. 58249
COOLEY LLP
1299 Pennsylvania Ave. NW, Suite 700
Washington, DC 20004

Tel: (650) 843-5622
Fax: (202) 842-7899

Respectfully submitted,
COOLEY LLP

By: 

William S. Galliani
Reg. No. 33,885

PTO/SB/15 (09-07)

Approved for use through 03/31/2013 OMB 0851-0033

U.S. Patent and Trademark Office, U.S. DEPARTMENT OF COMMERCE

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**SUPPLEMENTAL DECLARATION
FOR REISSUE
PATENT APPLICATION
TO CORRECT "ERRORS" STATEMENT
(37 CFR 1.175)**

Attorney Docket Number	ACQI-008/03US 310578-2072
First Named Inventor	William W. Y. Chu
COMPLETE if known	
Application Number	13/582,210
Filing Date	July 30, 2012
Art Unit	2435
Examiner Name	Song, Hosuk

WE hereby declare that:

Every error in the patent which was corrected in the present reissue application, and which is not covered by the prior oath(s) and/or declaration(s) submitted in this application, arose without any deceptive intention on the part of the applicant.

WARNING:

Petitioner/applicant is cautioned to avoid submitting personal information in documents filed in a patent application that may contribute to identity theft. Personal information such as social security numbers, bank account numbers, or credit card numbers (other than a check or credit card authorization form PTO-2038 submitted for payment purposes) is never required by the USPTO to support a petition or an application. If this type of personal information is included in documents submitted to the USPTO, petitioners/applicants should consider redacting such personal information from the documents before submitting them to the USPTO. Petitioner/applicant is advised that the record of a patent application is available to the public after publication of the application (unless a non-publication request in compliance with 37 CFR 1.213(a) is made in the application) or issuance of a patent. Furthermore, the record from an abandoned application may also be available to the public if the application is referenced in a published application or an issued patent (see 37 CFR 1.14). Checks and credit card authorization forms PTO-2038 submitted for payment purposes are not retained in the application file and therefore are not publicly available.

WE hereby declare that all statements made herein of my/our own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under 18 U.S.C. 1001 and that such willful false statements may jeopardize the validity of the application or any patent issued thereon.

Name of Sole or First Inventor:		<input type="checkbox"/> A petition has been filed for this unsigned inventor	
Given Name (first and middle (if any))		Family Name or Surname	
William W. Y.		Chu	
Inventor's Signature	<i>William W. Y. Chu</i>	Date	March 13, 2013
Name of Second Inventor:		<input type="checkbox"/> A petition has been filed for this unsigned inventor	
Given Name (first and middle (if any))		Family Name or Surname	
Inventor's Signature		Date	

☐ Additional inventors or legal representatives are being named on the _____ supplemental sheets PTO/SB/02A or 02LR attached hereto.

This collection of information is required by 37 CFR 1.175. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 36 U.S.C. 122 and 37 CFR 1.11 and 1.14. This collection is estimated to take 1.8 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1480, Alexandria, VA 22313-1480. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. SEND TO: Commissioner for Patents, P.O. Box 1480, Alexandria, VA 22313-1480.

If you need assistance in completing the form, call 1-800-PTO-9196 and select option 2.

Electronic Acknowledgement Receipt	
EFS ID:	15547717
Application Number:	13562210
International Application Number:	
Confirmation Number:	1045
Title of Invention:	Data Security Method and Device for Computer Modules
First Named Inventor/Applicant Name:	William W. Y. Chu
Customer Number:	58249
Filer:	William S. Galliani/Bobbie Jutras
Filer Authorized By:	William S. Galliani
Attorney Docket Number:	ACQI-006/05US 310578-2072
Receipt Date:	17-APR-2013
Filing Date:	30-JUL-2012
Time Stamp:	20:21:51
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	no
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File Listing:

Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1	Amendment After Final	ACQI-006-05US_2013-04-17_Response.pdf	22946 30a1cc08b31a68678283599ed6d9f19ee6bf3a4d	no	2

Warnings:

Information:

2	Supp reissue dec filed in accord with MPEP 1414.01.	ACQI-006-05US_2013-04-17_SupplReissueDecl.pdf	<div>1173437</div> <div>121cc966f10ebd1ac72a99e298add1fd0c7fbba5</div>	no	1
Warnings:					
Information:					
Total Files Size (in bytes):			1196383		
<p>This Acknowledgement Receipt evidences receipt on the noted date by the USPTO of the indicated documents, characterized by the applicant, and including page counts, where applicable. It serves as evidence of receipt similar to a Post Card, as described in MPEP 503.</p> <p><u>New Applications Under 35 U.S.C. 111</u> If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application.</p> <p><u>National Stage of an International Application under 35 U.S.C. 371</u> If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.</p> <p><u>New International Application Filed with the USPTO as a Receiving Office</u> If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.</p>					

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re application of:
William W. Y. Chu

Confirmation No.: 1045

Serial No.: 13/562,210

Examiner: Song, Hosuk

Filed: July 30, 2012

Art Unit: 2435

For: DATA SECURITY METHOD AND DEVICE FOR COMPUTER MODULES

Mail Stop Amendment
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

SUPPLEMENTAL RESPONSE

This communication is in response to a telephone call received from Examiner Song on April 24, 2013.

Amendments to the claims begin on page 2.

Remarks begin on page 10.

The Commissioner is hereby authorized to charge any required fees and to credit any overpayments to Cooley LLP's deposit account No. 50-1283.

IN THE CLAIMS

1-13. (Cancelled)

14. (Previously Presented) A computer for information transactions, comprising:
a central processing unit directly connected to a first Low Voltage Differential Signal (LVDS) channel comprising two sets of unidirectional, serial bit channels to transmit data in opposite directions;
a main memory directly connected to the central processing unit; and
a peripheral bridge directly coupled to the central processing unit without any intervening Peripheral Component Interconnect ("PCI") bus, wherein the peripheral bridge directly conveys an encoded serial bit stream of address and data bits of a PCI bus transaction over a second LVDS channel comprising two sets of unidirectional, serial bit channels to transmit data in opposite directions.

15. (Previously Presented) The computer of claim 14, further comprising a connector coupled to a console, wherein the second LVDS channel communicates the encoded serial bit stream of address and data bits of the PCI bus transaction to the console.

16. (Previously Presented) The computer of claim 15 further comprising a graphics controller that conveys digital video display information from the connector to the console.

17. (Previously Presented) The computer of claim 15 wherein the console comprises a mass storage device that couples to the second LVDS channel.

18. (Previously Presented) A computer system, comprising:
a console comprising a Liquid Crystal Display (LCD) display and a first Low Voltage Differential Signal (LVDS) channel comprising two sets of unidirectional, serial bit channels to transmit data in opposite directions; and
a computer coupled to the console through a connector, the computer comprising

an integrated central processing unit and graphics controller in a single chip directly connected to a second LVDS channel comprising two sets of unidirectional, serial bit channels to transmit data in opposite directions; and

a mass storage unit coupled to the central processing unit and graphics controller in a single chip;

wherein the graphics controller conveys digital video display information to the LCD display through the connector upon coupling to the console.

19. (Previously Presented) The computer system of claim 18 wherein the computer further comprises a peripheral bridge directly coupled to the central processing unit without any intervening Peripheral Component Interconnect (“PCI”) bus, the peripheral bridge directly conveying an encoded serial bit stream of address and data bits of a PCI bus transaction.

20. (Previously Presented) The computer system of claim 19 wherein the peripheral bridge conveys the encoded serial bit stream of address and data bits of the PCI bus transaction to the first LVDS channel upon coupling of the computer to the console.

21. (Previously Presented) A computer, comprising:

a central processing unit directly connected to a first Low Voltage Differential Signal (LVDS) channel comprising two sets of unidirectional, serial bit channels to transmit Universal Serial Bus (USB) Protocol data in opposite directions;

a second LVDS channel comprising two sets of unidirectional, serial bit channels to transmit data in opposite directions;

a connector coupled to the first LVDS channel; and

a main memory directly coupled to the central processing unit.

22. (Previously Presented) The computer of claim 21 wherein the second LVDS channel communicates an encoded serial bit stream of address and data bits of a Peripheral Component Interconnect (“PCI”) bus transaction.

23. (Previously Presented) The computer of claim 21 wherein the first LVDS channel conveys Universal Serial Bus (USB) Protocol data to a console through the connector.

24. (Amended) A computer, comprising:

an integrated central processing unit and graphics controller in a single chip directly connected to a Low Voltage Differential Signal (LVDS) channel comprising two sets of unidirectional, serial bit channels to transmit data in opposite directions; [and]

a main memory directly coupled to the integrated central processing unit and graphics controller; [and]

a differential signal channel directly extending from the integrated central processing unit and graphics controller to convey digital video display information;

a connector for coupling to a console; and

a second differential signal channel comprising two sets of unidirectional, serial bit channels to transmit data in opposite directions, wherein the second differential signal channel conveys Universal Serial Bus (USB) protocol data through the connector to the console.

25. (Previously Presented) The computer of claim 24 wherein the LVDS channel conveys an encoded serial bit stream of address and data bits of a Peripheral Component Interconnect ("PCI") bus transaction.

26-28. (Cancelled)

29. (Previously Presented) A modular computer system, comprising:

a console comprising a first Low Voltage Differential Signal (LVDS) channel comprising two sets of unidirectional, serial bit channels to transmit data in opposite directions; and

a computer coupled to the console through a connector, the computer comprising

a central processing unit,

a mass storage unit coupled to the central processing unit,

a second LVDS channel comprising two sets of unidirectional, serial bit channels to transmit data in opposite directions, and

a peripheral bridge directly coupled to the central processing unit without any intervening Peripheral Component Interconnect bus, wherein the peripheral bridge directly conveys an encoded serial bit stream of address and data bits of a Peripheral Component Interconnect (“PCI”) bus transaction over the second LVDS channel; and

wherein the second LVDS channel communicates to the first LVDS channel in the console upon the computer coupling to the console.

30. (Previously Presented) The modular computer system of claim 29 wherein the second LVDS channel conveys the encoded serial bit stream of the PCI bus transaction to the first LVDS channel upon coupling of the computer module to the console.

31. (Previously Presented) The modular computer system of claim 30 wherein the console further comprises a mass storage device that couples to the first and second LVDS channels.

32. (Amended) A modular computer system, comprising:

a console comprising a power supply; and

a computer coupled to the console through a connector, the computer comprising

a central processing unit,

a first Low Voltage Differential Signal (LVDS) channel comprising two sets of unidirectional, multiple serial bit channels to transmit data in opposite directions,

a peripheral bridge directly coupled to the first LVDS channel to communicate an encoded serial bit stream of address and data bits of a Peripheral Component Interconnect (“PCI”) bus transaction, the peripheral [controller] bridge directly coupled to the central processing unit without any intervening PCI bus, and

wherein the power supply supplies power to the computer upon coupling to the console.

33. (Previously Presented) The computer system of claim 32 further comprising a second LVDS channel that conveys the encoded serial bit stream of address and data bits of the PCI bus transaction, wherein the second LVDS channel directly extends from the central processing unit.

34. (Previously Presented) A modular computer system, comprising:
a console comprising a first Low Voltage Differential Signal (LVDS) channel comprising
two sets of unidirectional, serial bit channels to transmit data in opposite directions; and
a computer that couples to the console, the computer comprising
an integrated central processing unit and graphics controller in a single chip,
directly connected to a second LVDS channel comprising two sets of unidirectional, serial bit
channels to transmit data in opposite directions, and
a connector that couples to the first LVDS channel in the console.
35. (Previously Presented) The modular computer system of claim 34 wherein the second
LVDS channel conveys an encoded serial bit stream of address and data bits of a Peripheral
Component Interconnect (“PCI”) bus transaction.
36. (Previously Presented) The modular computer system of claim 34 wherein the first LVDS
channel conveys an encoded serial bit stream of address and data bits of a Peripheral Component
Interconnect (“PCI”) bus transaction.
37. (Previously Presented) The modular computer system of claim 34 wherein the computer
conveys Universal Serial Bus (USB) protocol data to the console upon the computer coupling to
the console.
38. (Previously Presented) A computer, comprising:
a central processing unit;
a main memory directly connected to the central processing unit;
a peripheral bridge directly coupled to the central processing unit without any intervening
Peripheral Component Interconnect (PCI) bus, wherein the peripheral bridge directly conveys an
encoded serial bit stream of address and data bits of a Peripheral Component Interconnect (PCI)
bus transaction over a first Low Voltage Differential Signal (LVDS) channel comprising two sets
of unidirectional, serial bit channels to transmit data in opposite directions; and
a mass storage device directly coupled the peripheral bridge.

39. (Previously Presented) The computer of claim 38 further comprising a graphics controller coupled to the peripheral bridge.

40. (Amended) A computer, comprising:

a central processing unit directly connected to a first Low Voltage Differential Signal (LVDS) channel to convey [an] a first encoded serial bit stream of address and data bits of a Peripheral Component Interconnect (PCI) bus transaction;

a main memory directly connected to the central processing unit; and

a peripheral bridge directly coupled to the central processing unit without any intervening PCI bus, wherein the peripheral bridge directly conveys [the] a second encoded serial bit stream of address and data bits of [the] a (PCI) bus transaction over a second LVDS channel comprising two sets of unidirectional, serial bit channels to transmit data in opposite directions.

41. (Amended) The computer of claim 40 further comprising a connector coupled to a console, wherein the second LVDS channel communicates the second encoded serial bit stream of address and data bits of the PCI bus transaction to the console.

42. (Previously Presented) The computer of claim 41 further comprising a graphics controller to convey digital video display information from the connector to the console.

43. (Previously Presented) The computer of claim 41 wherein the console comprises a peripheral device that couples to the second LVDS channel.

44. (Amended) A computer, comprising:

an integrated central processing unit and graphics controller in a single chip directly connected to a first Low Voltage Differential Signal (LVDS) channel comprising two sets of unidirectional, serial bit channels to transmit data in opposite directions, wherein the integrated central processing unit and graphics controller conveys digital video display signals through a second differential signal channel;

a main memory directly coupled to the integrated central processing unit and graphics controller; and

a mass storage device comprising flash memory.

45. (Cancelled)

46. (Amended) The computer of claim [45] 44 wherein the second differential signal channel conveys Transition Minimized Differential Signaling (TDMS) information.

47. (Previously Presented) The computer of claim 44 wherein the first LVDS channel conveys an encoded serial bit stream of address and data bits of a Peripheral Component Interconnect (PCI) bus transaction.

48. (Cancelled)

49. (Amended) [The computer of claim 48 further comprising] A computer, comprising:
an integrated central processing unit and graphics controller in a single chip directly connected to a first Low Voltage Differential Signal (LVDS) channel comprising two sets of unidirectional, serial bit channels to transmit data in opposite directions;

a main memory directly coupled to the integrated central processing unit and graphics controller;

a mass storage device comprising flash memory;

a connector that conveys Universal Serial Bus (USB) protocol information to a console;

and

a second LVDS channel comprising two sets of unidirectional, serial bit channels to transmit data in opposite directions, wherein the second LVDS channel conveys said USB protocol information to the console through the connector.

50. (Previously Presented) A computer, comprising:

a Central Processing Unit (CPU) directly connected to a Low Voltage Differential Signal (LVDS) channel comprising two sets of multiple, unidirectional, serial bit channels to convey an encoded serial bit stream of encoded address and data bits of a Peripheral Component Interconnect ("PCI") bus transaction in opposite directions;

a main memory directly connected to the CPU; and

a mass storage device coupled to the CPU.

51. (Previously Presented) The computer of claim 50 further comprising a connector, wherein the connector connects to a console comprising a power supply, and the power supply supplies power to the computer upon coupling to the console.

52. (Previously Presented) The computer of claim 50 wherein the mass storage device comprises flash memory.

53. (Previously Presented) A computer, comprising:
an integrated central processing unit and graphics controller in a single chip directly connected to a first Low Voltage Differential Signal (LVDS) channel comprising two sets of multiple, unidirectional, serial bit channels to convey an encoded serial bit stream of encoded address and data bits of a Peripheral Component Interconnect (PCI) bus transaction in opposite directions;

a main memory directly coupled to the integrated central processing unit and graphics controller; and

an Ethernet communication device coupled to the first LVDS channel.

54. (Previously Presented) The computer of claim 53 further comprising a connector, wherein the connector connects to a console comprising a power supply, and the power supply supplies power to the computer upon coupling to the console.

REMARKS

Applicant submits a Terminal Disclaimer as requested by Examiner Song. Applicant also re-presents the claims submitted on January 31, 2013 using underlining and brackets for omitted matter.


Accordingly, the application is in condition for allowance. The Examiner is invited to contact the undersigned if there are any residual issues that can be resolved through a telephone call.

Date: May 1, 2013

Customer No. 58249
COOLEY LLP
1299 Pennsylvania Ave. NW, Suite 700
Washington, DC 20004

Tel: (650) 843-5622
Fax: (202) 842-7899

Respectfully submitted,
COOLEY LLP


By: _____
William S. Galliani
Reg. No. 33,885

**TERMINAL DISCLAIMER TO OBTAIN A DOUBLE PATENTING
REJECTION OVER A "PRIOR" PATENT**

Docket Number (Optional)
ACQI-006/05US 310578-2072

In re Application of: William W. Y. Chu

Application No.: 13/562,210

Filed: July 30, 2012

For: DATA SECURITY METHOD AND DEVICE FOR COMPUTER MODULES

The owner*, Acqis LLC, of 100 percent interest in the instant application hereby disclaims, except as provided below, the terminal part of the statutory term of any patent granted on the instant application which would extend beyond the expiration date of the full statutory term of **prior patent** No. RE 43,984 and RE43,602 as the term of said **prior patent** is presently shortened by any terminal disclaimer. The owner hereby agrees that any patent so granted on the instant application shall be enforceable only for and during such period that it and the **prior patent** are commonly owned. This agreement runs with any patent granted on the instant application and is binding upon the grantee, its successors or assigns.

In making the above disclaimer, the owner does not disclaim the terminal part of the term of any patent granted on the instant application that would extend to the expiration date of the full statutory term of the **prior patent**, "as the term of said **prior patent** is presently shortened by any terminal disclaimer," in the event that said **prior patent** later:

- expires for failure to pay a maintenance fee;
- is held unenforceable;
- is found invalid by a court of competent jurisdiction;
- is statutorily disclaimed in whole or terminally disclaimed under 37 CFR 1.321;
- has all claims canceled by a reexamination certificate;
- is reissued; or
- is in any manner terminated prior to the expiration of its full statutory term as presently shortened by any terminal disclaimer.

Check either box 1 or 2 below, if appropriate.

1. ☒ For submissions on behalf of a business/organization (e.g., corporation, partnership, university, government agency, etc.), the undersigned is empowered to act on behalf of the business/organization.

I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code and that such willful false statements may jeopardize the validity of the application or any patent issued thereon.

2. ☒ The undersigned is an attorney or agent of record. Reg. No. 33,885



Signature

May 1, 2013

Date

William S. Galliani

Typed or printed name

(650) 843-5622

Telephone Number

- ☒ Terminal disclaimer fee under 37 CFR 1.20(d) included.

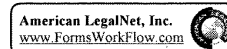
WARNING: Information on this form may become public. Credit card information should not be included on this form. Provide credit card information and authorization on PTO-2038.

*Statement under 37 CFR 3.73(b) is required if terminal disclaimer is signed by the assignee (owner).
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This collection of information is required by 37 CFR 1.321. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.11 and 1.14. This collection is estimated to take 12 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.

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1122079 v1/HN



Electronic Patent Application Fee Transmittal				
Application Number:		13562210		
Filing Date:		30-Jul-2012		
Title of Invention:		Data Security Method and Device for Computer Modules		
First Named Inventor/Applicant Name:		William W. Y. Chu		
Filer:		William S. Galliani/Bobbie Jutras		
Attorney Docket Number:		ACQI-006/05US 310578-2072		
Filed as Large Entity				
Utility under 35 USC 111(a) Filing Fees				
Description	Fee Code	Quantity	Amount	Sub-Total in USD(\$)
Basic Filing:				
Pages:				
Claims:				
Miscellaneous-Filing:				
Petition:				
Patent-Appeals-and-Interference:				
Post-Allowance-and-Post-Issuance:				
Extension-of-Time:				

Description	Fee Code	Quantity	Amount	Sub-Total in USD(\$)
Miscellaneous:				
Statutory or Terminal Disclaimer	1814	1	160	160
Total in USD (\$)				160

Electronic Acknowledgement Receipt	
EFS ID:	15669253
Application Number:	13562210
International Application Number:	
Confirmation Number:	1045
Title of Invention:	Data Security Method and Device for Computer Modules
First Named Inventor/Applicant Name:	William W. Y. Chu
Customer Number:	58249
Filer:	William S. Galliani/Bobbie Jutras
Filer Authorized By:	William S. Galliani
Attorney Docket Number:	ACQI-006/05US 310578-2072
Receipt Date:	01-MAY-2013
Filing Date:	30-JUL-2012
Time Stamp:	19:37:17
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	yes
Payment Type	Deposit Account
Payment was successfully received in RAM	\$ 160
RAM confirmation Number	6148
Deposit Account	501283
Authorized User	
<p>The Director of the USPTO is hereby authorized to charge indicated fees and credit any overpayment as follows:</p> <p>Charge any Additional Fees required under 37 C.F.R. Section 1.16 (National application filing, search, and examination fees)</p> <p>Charge any Additional Fees required under 37 C.F.R. Section 1.17 (Patent application and reexamination processing fees)</p>	

File Listing:					
Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1		ACQI-006-05US_2013-05-01_S upplResp-TD.pdf	211885 4d3d9e2c971146745b790e516693c2fac0df 2c6b	yes	11
	Multipart Description/PDF files in .zip description				
	Document Description	Start	End		
	Amendment After Final	1	1		
	Claims	2	9		
	Applicant Arguments/Remarks Made in an Amendment	10	10		
	Statutory disclaimers per MPEP 1490.	11	11		
Warnings:					
Information:					
2	Fee Worksheet (SB06)	fee-info.pdf	30350 9aae973c68146b7884270b75fb3fb02ab1fd c207	no	2
Warnings:					
Information:					
Total Files Size (in bytes):			242235		
<p>This Acknowledgement Receipt evidences receipt on the noted date by the USPTO of the indicated documents, characterized by the applicant, and including page counts, where applicable. It serves as evidence of receipt similar to a Post Card, as described in MPEP 503.</p> <p><u>New Applications Under 35 U.S.C. 111</u> If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application.</p> <p><u>National Stage of an International Application under 35 U.S.C. 371</u> If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.</p> <p><u>New International Application Filed with the USPTO as a Receiving Office</u> If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.</p>					

Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it displays a valid OMB control number.

PATENT APPLICATION FEE DETERMINATION RECORD Substitute for Form PTO-875				Application or Docket Number 13/562,210		Filing Date 07/30/2012		<input type="checkbox"/> To be Mailed	
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ENTITY: <input checked="" type="checkbox"/> LARGE <input type="checkbox"/> SMALL <input type="checkbox"/> MICRO										
APPLICATION AS FILED – PART I										
(Column 1)		(Column 2)								
FOR	NUMBER FILED	NUMBER EXTRA			RATE (\$)	FEE (\$)				
<input type="checkbox"/> BASIC FEE (37 CFR 1.16(a), (b), or (c))	N/A	N/A			N/A					
<input type="checkbox"/> SEARCH FEE (37 CFR 1.16(k), (l), or (m))	N/A	N/A			N/A					
<input type="checkbox"/> EXAMINATION FEE (37 CFR 1.16(o), (p), or (q))	N/A	N/A			N/A					
TOTAL CLAIMS (37 CFR 1.16(i))	minus 20 =	*			X \$ =					
INDEPENDENT CLAIMS (37 CFR 1.16(h))	minus 3 =	*			X \$ =					
<input type="checkbox"/> APPLICATION SIZE FEE (37 CFR 1.16(s))	If the specification and drawings exceed 100 sheets of paper, the application size fee due is \$310 (\$155 for small entity) for each additional 50 sheets or fraction thereof. See 35 U.S.C. 41(a)(1)(G) and 37 CFR 1.16(s).									
<input type="checkbox"/> MULTIPLE DEPENDENT CLAIM PRESENT (37 CFR 1.16(j))										
* If the difference in column 1 is less than zero, enter "0" in column 2.					TOTAL					

APPLICATION AS AMENDED – PART II									
(Column 1)		(Column 2)		(Column 3)					
AMENDMENT	05/01/2013	CLAIMS REMAINING AFTER AMENDMENT		HIGHEST NUMBER PREVIOUSLY PAID FOR	PRESENT EXTRA			RATE (\$)	ADDITIONAL FEE (\$)
	Total (37 CFR 1.16(i))	* 36	Minus	** 36	= 0			X \$80 =	0
	Independent (37 CFR 1.16(h))	* 12	Minus	*** 13	= 0			X \$420 =	0
	<input type="checkbox"/> Application Size Fee (37 CFR 1.16(s))								
	<input type="checkbox"/> FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))								
						TOTAL ADD'L FEE		0	
(Column 1)		(Column 2)		(Column 3)					
AMENDMENT		CLAIMS REMAINING AFTER AMENDMENT		HIGHEST NUMBER PREVIOUSLY PAID FOR	PRESENT EXTRA			RATE (\$)	ADDITIONAL FEE (\$)
	Total (37 CFR 1.16(i))	*	Minus	**	=			X \$ =	
	Independent (37 CFR 1.16(h))	*	Minus	***	=			X \$ =	
	<input type="checkbox"/> Application Size Fee (37 CFR 1.16(s))								
	<input type="checkbox"/> FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))								
						TOTAL ADD'L FEE			
<p>* If the entry in column 1 is less than the entry in column 2, write "0" in column 3.</p> <p>** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 20, enter "20".</p> <p>*** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 3, enter "3".</p> <p>The "Highest Number Previously Paid For" (Total or Independent) is the highest number found in the appropriate box in column 1.</p>									

LIE
/BRENDA J. DENNY/

This collection of information is required by 37 CFR 1.16. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 12 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

If you need assistance in completing the form, call 1-800-PTO-9199 and select option 2.

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re application of:
William W. Y. Chu

Confirmation No.: 1045

Serial No.: 13/562,210

Examiner: Song, Hosuk

Filed: July 30, 2012

Art Unit: 2435

For: DATA SECURITY METHOD AND DEVICE FOR COMPUTER MODULES

Mail Stop Amendment
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

RESUBMISSION OF TERMINAL DISCLAIMER

This resubmission of the Terminal Disclaimer is filed to correct a typographic error in the Terminal Disclaimer filed on May 1, 2013 via the Electronic Filing System.

Remarks begin on page 2.

The Commissioner is hereby authorized to charge any required fees and to credit any overpayments to Cooley LLP's deposit account No. 50-1283.

REMARKS

Applicant submits a revised Terminal Disclaimer to correct a typographical error in the previously submitted document which listed prior patent RE43,984. The patent number should have been listed as RE42,984.

Accordingly, the application is in condition for allowance. The Examiner is invited to contact the undersigned if there are any residual issues that can be resolved through a telephone call.

Date: May 2, 2013

Customer No. 58249
COOLEY LLP
1299 Pennsylvania Ave. NW, Suite 700
Washington, DC 20004

Tel: (650) 843-5622
Fax: (202) 842-7899

Respectfully submitted,
COOLEY LLP

By: 

William S. Galliani
Reg. No. 33,885

**TERMINAL DISCLAIMER TO OBVIATE A DOUBLE PATENTING
REJECTION OVER A "PRIOR" PATENT**

Docket Number (Optional)
ACQI-006/05US 310578-2072

In re Application of: William W. Y. Chu

Application No.: 13/562,210

Filed: July 30, 2012

For: DATA SECURITY METHOD AND DEVICE FOR COMPUTER MODULES

The owner*, Acqis LLC, of 100 percent interest in the instant application hereby disclaims, except as provided below, the terminal part of the statutory term of any patent granted on the instant application which would extend beyond the expiration date of the full statutory term of **prior patent** No. RE 42,984 and RE43,602 as the term of said **prior patent** is presently shortened by any terminal disclaimer. The owner hereby agrees that any patent so granted on the instant application shall be enforceable only for and during such period that it and the **prior patent** are commonly owned. This agreement runs with any patent granted on the instant application and is binding upon the grantee, its successors or assigns.

In making the above disclaimer, the owner does not disclaim the terminal part of the term of any patent granted on the instant application that would extend to the expiration date of the full statutory term of the **prior patent**, "as the term of said **prior patent** is presently shortened by any terminal disclaimer," in the event that said **prior patent** later:

- expires for failure to pay a maintenance fee;
- is held unenforceable;
- is found invalid by a court of competent jurisdiction;
- is statutorily disclaimed in whole or terminally disclaimed under 37 CFR 1.321;
- has all claims canceled by a reexamination certificate;
- is reissued; or
- is in any manner terminated prior to the expiration of its full statutory term as presently shortened by any terminal disclaimer.

Check either box 1 or 2 below, if appropriate.

1. ☒ For submissions on behalf of a business/organization (e.g., corporation, partnership, university, government agency, etc.), the undersigned is empowered to act on behalf of the business/organization.

I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code and that such willful false statements may jeopardize the validity of the application or any patent issued thereon.

2. ☒ The undersigned is an attorney or agent of record. Reg. No. 33,885



Signature

May 2, 2013

Date

William S. Galliani

Typed or printed name

(650) 843-5622

Telephone Number

- ☒ Terminal disclaimer fee under 37 CFR 1.20(d) included.

WARNING: Information on this form may become public. Credit card information should not be included on this form. Provide credit card information and authorization on PTO-2038.

*Statement under 37 CFR 3.73(b) is required if terminal disclaimer is signed by the assignee (owner).
Form PTO/SB/96 may be used for making this certification. See MPEP § 324.

This collection of information is required by 37 CFR 1.321. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.11 and 1.14. This collection is estimated to take 12 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.

If you need assistance in completing the form, call 1-800-PTO-9199 and select option 2.

Electronic Acknowledgement Receipt	
EFS ID:	15675792
Application Number:	13562210
International Application Number:	
Confirmation Number:	1045
Title of Invention:	Data Security Method and Device for Computer Modules
First Named Inventor/Applicant Name:	William W. Y. Chu
Customer Number:	58249
Filer:	William S. Galliani/Bobbie Jutras
Filer Authorized By:	William S. Galliani
Attorney Docket Number:	ACQI-006/05US 310578-2072
Receipt Date:	02-MAY-2013
Filing Date:	30-JUL-2012
Time Stamp:	15:16:27
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	no
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File Listing:

Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1	Statutory disclaimers per MPEP 1490.	ACQI-006-05US_2013-05-02_Re submissionOfTD.pdf	83230 53581d363df24720cd2852b0e131fb07591700fb	no	3

Warnings:

Information:

This Acknowledgement Receipt evidences receipt on the noted date by the USPTO of the indicated documents, characterized by the applicant, and including page counts, where applicable. It serves as evidence of receipt similar to a Post Card, as described in MPEP 503.

New Applications Under 35 U.S.C. 111


If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application.

National Stage of an International Application under 35 U.S.C. 371

If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.

New International Application Filed with the USPTO as a Receiving Office

If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.


Application Number 	Application/Control No. 13/562,210	Applicant(s)/Patent under Reexamination CHU, WILLIAM W. Y.	
Document Code - DISQ		Internal Document – DO NOT MAIL	

TERMINAL DISCLAIMER	<input type="checkbox"/> APPROVED	<input checked="" type="checkbox"/> DISAPPROVED
Date Filed : 5/01/13	This patent is subject to a Terminal Disclaimer	

Approved/Disapproved by:

<p>Felicia D. Roberts</p> <p>Patent number RE 43,984 is incorrect. It should read RE 42,984.</p>
--



U.S. Patent and Trademark Office

Application Number 	Application/Control No. 13/562,210	Applicant(s)/Patent under Reexamination CHU, WILLIAM W. Y.	
Document Code - DISQ		Internal Document – DO NOT MAIL	

TERMINAL DISCLAIMER	<input checked="" type="checkbox"/> APPROVED	<input type="checkbox"/> DISAPPROVED
Date Filed : 5/2/13	This patent is subject to a Terminal Disclaimer	

Approved/Disapproved by:
Felicia D. Roberts RE 42,984 and RE 43,602

U.S. Patent and Trademark Office

Application Number  	Application/Control No. 13/562210	Applicant(s)/Patent under Reexamination REIS.REVFORM
Document Code - SRNT	Internal Document – DO NOT MAIL	

Original Patent Number of Patent to be reissued: 6643777	Notice of Reissue Published in O.G. date: 9/11/2012
<p>This reissue patent is subjected Terminal Disclaimer that</p> <p> <input checked="" type="checkbox"/> was filed during the prosecution of the reissue application <input type="checkbox"/> was of record prior to the filing of the reissue application </p> <p>The maintenance fee status is:</p> <p> <input checked="" type="checkbox"/> is up to date <input type="checkbox"/> was not required </p> <p>Physical surrender of the letter patent:</p> <p> <input type="checkbox"/> was made <input type="checkbox"/> was not made, but a statement of loss/inaccessibility was provided by applicant(s) <input checked="" type="checkbox"/> is not required </p>	
Final SPRE review trs 5/6/2013	



UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

NOTICE OF ALLOWANCE AND FEE(S) DUE

58249 7590 06/10/2013
COOLEY LLP
ATTN: Patent Group
1299 Pennsylvania Avenue, NW
Suite 700
Washington, DC 20004

EXAMINER

SONG, HOSUK

ART UNIT

PAPER NUMBER

2435

DATE MAILED: 06/10/2013

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
13/562,210	07/30/2012	William W. Y. Chu	ACQI-006/05US 310578-2072	1045

TITLE OF INVENTION: Data Security Method and Device for Computer Modules

APPLN. TYPE	ENTITY STATUS	ISSUE FEE DUE	PUBLICATION FEE DUE	PREV. PAID ISSUE FEE	TOTAL FEE(S) DUE	DATE DUE
nonprovisional	UNDISCOUNTED	\$1780	\$0	\$0	\$1780	09/10/2013

THE APPLICATION IDENTIFIED ABOVE HAS BEEN EXAMINED AND IS ALLOWED FOR ISSUANCE AS A PATENT. PROSECUTION ON THE MERITS IS CLOSED. THIS NOTICE OF ALLOWANCE IS NOT A GRANT OF PATENT RIGHTS. THIS APPLICATION IS SUBJECT TO WITHDRAWAL FROM ISSUE AT THE INITIATIVE OF THE OFFICE OR UPON PETITION BY THE APPLICANT. SEE 37 CFR 1.313 AND MPEP 1308.

THE ISSUE FEE AND PUBLICATION FEE (IF REQUIRED) MUST BE PAID WITHIN THREE MONTHS FROM THE MAILING DATE OF THIS NOTICE OR THIS APPLICATION SHALL BE REGARDED AS ABANDONED. THIS STATUTORY PERIOD CANNOT BE EXTENDED. SEE 35 U.S.C. 151. THE ISSUE FEE DUE INDICATED ABOVE DOES NOT REFLECT A CREDIT FOR ANY PREVIOUSLY PAID ISSUE FEE IN THIS APPLICATION. IF AN ISSUE FEE HAS PREVIOUSLY BEEN PAID IN THIS APPLICATION (AS SHOWN ABOVE), THE RETURN OF PART B OF THIS FORM WILL BE CONSIDERED A REQUEST TO REAPPLY THE PREVIOUSLY PAID ISSUE FEE TOWARD THE ISSUE FEE NOW DUE.

HOW TO REPLY TO THIS NOTICE:

I. Review the ENTITY STATUS shown above. If the ENTITY STATUS is shown as SMALL or MICRO, verify whether entitlement to that entity status still applies.

If the ENTITY STATUS is the same as shown above, pay the TOTAL FEE(S) DUE shown above.

If the ENTITY STATUS is changed from that shown above, on PART B - FEE(S) TRANSMITTAL, complete section number 5 titled "Change in Entity Status (from status indicated above)".

For purposes of this notice, small entity fees are 1/2 the amount of undiscounted fees, and micro entity fees are 1/2 the amount of small entity fees.

II. PART B - FEE(S) TRANSMITTAL, or its equivalent, must be completed and returned to the United States Patent and Trademark Office (USPTO) with your ISSUE FEE and PUBLICATION FEE (if required). If you are charging the fee(s) to your deposit account, section "4b" of Part B - Fee(s) Transmittal should be completed and an extra copy of the form should be submitted. If an equivalent of Part B is filed, a request to reapply a previously paid issue fee must be clearly made, and delays in processing may occur due to the difficulty in recognizing the paper as an equivalent of Part B.

III. All communications regarding this application must give the application number. Please direct all communications prior to issuance to Mail Stop ISSUE FEE unless advised to the contrary.

IMPORTANT REMINDER: Utility patents issuing on applications filed on or after Dec. 12, 1980 may require payment of maintenance fees. It is patentee's responsibility to ensure timely payment of maintenance fees when due.

PART B - FEE(S) TRANSMITTAL

**Complete and send this form, together with applicable fee(s), to: Mail Mail Stop ISSUE FEE
Commissioner for Patents
P.O. Box 1450
Alexandria, Virginia 22313-1450
or Fax (571)-273-2885**

INSTRUCTIONS: This form should be used for transmitting the ISSUE FEE and PUBLICATION FEE (if required). Blocks 1 through 5 should be completed where appropriate. All further correspondence including the Patent, advance orders and notification of maintenance fees will be mailed to the current correspondence address as indicated unless corrected below or directed otherwise in Block 1, by (a) specifying a new correspondence address; and/or (b) indicating a separate "FEE ADDRESS" for maintenance fee notifications.

CURRENT CORRESPONDENCE ADDRESS (Note: Use Block 1 for any change of address)

58249 7590 06/10/2013
COOLEY LLP
ATTN: Patent Group
1299 Pennsylvania Avenue, NW
Suite 700
Washington, DC 20004

Note: A certificate of mailing can only be used for domestic mailings of the Fee(s) Transmittal. This certificate cannot be used for any other accompanying papers. Each additional paper, such as an assignment or formal drawing, must have its own certificate of mailing or transmission.

Certificate of Mailing or Transmission

I hereby certify that this Fee(s) Transmittal is being deposited with the United States Postal Service with sufficient postage for first class mail in an envelope addressed to the Mail Stop ISSUE FEE address above, or being facsimile transmitted to the USPTO (571) 273-2885, on the date indicated below.

(Depositor's name)
(Signature)
(Date)

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
13/562,210	07/30/2012	William W. Y. Chu	ACQI-006/05US 310578-2072	1045

TITLE OF INVENTION: Data Security Method and Device for Computer Modules

APPLN. TYPE	ENTITY STATUS	ISSUE FEE DUE	PUBLICATION FEE DUE	PREV. PAID ISSUE FEE	TOTAL FEE(S) DUE	DATE DUE
nonprovisional	UNDISCOUNTED	\$1780	\$0	\$0	\$1780	09/10/2013

EXAMINER	ART UNIT	CLASS-SUBCLASS
SONG, HOSUK	2435	726-020000

1. Change of correspondence address or indication of "Fee Address" (37 CFR 1.363).
☐ Change of correspondence address (or Change of Correspondence Address form PTO/SB/122) attached.
☐ "Fee Address" indication (or "Fee Address" Indication form PTO/SB/47; Rev 03-02 or more recent) attached. **Use of a Customer Number is required.**

2. For printing on the patent front page, list
 (1) the names of up to 3 registered patent attorneys or agents OR, alternatively, 1 _____
 (2) the name of a single firm (having as a member a registered attorney or agent) and the names of up to 2 registered patent attorneys or agents. If no name is listed, no name will be printed. 2 _____
 3 _____

3. ASSIGNEE NAME AND RESIDENCE DATA TO BE PRINTED ON THE PATENT (print or type)

PLEASE NOTE: Unless an assignee is identified below, no assignee data will appear on the patent. If an assignee is identified below, the document has been filed for recordation as set forth in 37 CFR 3.11. Completion of this form is NOT a substitute for filing an assignment.

(A) NAME OF ASSIGNEE

(B) RESIDENCE: (CITY and STATE OR COUNTRY)

Please check the appropriate assignee category or categories (will not be printed on the patent): ☐ Individual ☐ Corporation or other private group entity ☐ Government

4a. The following fee(s) are submitted:

- ☐ Issue Fee
☐ Publication Fee (No small entity discount permitted)
☐ Advance Order - # of Copies _____

4b. Payment of Fee(s): (Please first reapply any previously paid issue fee shown above)

- ☐ A check is enclosed.
☐ Payment by credit card. Form PTO-2038 is attached.
☐ The Director is hereby authorized to charge the required fee(s), any deficiency, or credit any overpayment, to Deposit Account Number _____ (enclose an extra copy of this form).

5. **Change in Entity Status** (from status indicated above)

☐ Applicant certifying micro entity status. See 37 CFR 1.29

☐ Applicant asserting small entity status. See 37 CFR 1.27

☐ Applicant changing to regular undiscounted fee status.

NOTE: Absent a valid certification of Micro Entity Status (see form PTO/SB/15A and 15B), issue fee payment in the micro entity amount will not be accepted at the risk of application abandonment.

NOTE: If the application was previously under micro entity status, checking this box will be taken to be a notification of loss of entitlement to micro entity status.

NOTE: Checking this box will be taken to be a notification of loss of entitlement to small or micro entity status, as applicable.

NOTE: The Issue Fee and Publication Fee (if required) will not be accepted from anyone other than the applicant; a registered attorney or agent; or the assignee or other party in interest as shown by the records of the United States Patent and Trademark Office.

Authorized Signature _____

Date _____

Typed or printed name _____

Registration No. _____

This collection of information is required by 37 CFR 1.311. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 12 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, Virginia 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, Virginia 22313-1450.

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UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
13/562,210	07/30/2012	William W. Y. Chu	ACQI-006/05US 310578-2072	1045
58249	7590	06/10/2013	EXAMINER	
COOLEY LLP			SONG, HOSUK	
ATTN: Patent Group			ART UNIT	
1299 Pennsylvania Avenue, NW			PAPER NUMBER	
Suite 700			2435	
Washington, DC 20004			DATE MAILED: 06/10/2013	

Determination of Patent Term Extension or Adjustment under 35 U.S.C. 154 (b)

A reissue patent is for "the unexpired part of the term of the original patent." See 35 U.S.C. 251. Accordingly, the above-identified reissue application is not eligible for Patent Term Extension or Adjustment under 35 U.S.C. 154(b).

Any questions regarding the Patent Term Extension or Adjustment determination should be directed to the Office of Patent Legal Administration at (571)-272-7702. Questions relating to issue and publication fee payments should be directed to the Customer Service Center of the Office of Patent Publication at 1-(888)-786-0101 or (571)-272-4200.

Privacy Act Statement

The Privacy Act of 1974 (P.L. 93-579) requires that you be given certain information in connection with your submission of the attached form related to a patent application or patent. Accordingly, pursuant to the requirements of the Act, please be advised that: (1) the general authority for the collection of this information is 35 U.S.C. 2(b)(2); (2) furnishing of the information solicited is voluntary; and (3) the principal purpose for which the information is used by the U.S. Patent and Trademark Office is to process and/or examine your submission related to a patent application or patent. If you do not furnish the requested information, the U.S. Patent and Trademark Office may not be able to process and/or examine your submission, which may result in termination of proceedings or abandonment of the application or expiration of the patent.

The information provided by you in this form will be subject to the following routine uses:

1. The information on this form will be treated confidentially to the extent allowed under the Freedom of Information Act (5 U.S.C. 552) and the Privacy Act (5 U.S.C. 552a). Records from this system of records may be disclosed to the Department of Justice to determine whether disclosure of these records is required by the Freedom of Information Act.
2. A record from this system of records may be disclosed, as a routine use, in the course of presenting evidence to a court, magistrate, or administrative tribunal, including disclosures to opposing counsel in the course of settlement negotiations.
3. A record in this system of records may be disclosed, as a routine use, to a Member of Congress submitting a request involving an individual, to whom the record pertains, when the individual has requested assistance from the Member with respect to the subject matter of the record.
4. A record in this system of records may be disclosed, as a routine use, to a contractor of the Agency having need for the information in order to perform a contract. Recipients of information shall be required to comply with the requirements of the Privacy Act of 1974, as amended, pursuant to 5 U.S.C. 552a(m).
5. A record related to an International Application filed under the Patent Cooperation Treaty in this system of records may be disclosed, as a routine use, to the International Bureau of the World Intellectual Property Organization, pursuant to the Patent Cooperation Treaty.
6. A record in this system of records may be disclosed, as a routine use, to another federal agency for purposes of National Security review (35 U.S.C. 181) and for review pursuant to the Atomic Energy Act (42 U.S.C. 218(c)).
7. A record from this system of records may be disclosed, as a routine use, to the Administrator, General Services, or his/her designee, during an inspection of records conducted by GSA as part of that agency's responsibility to recommend improvements in records management practices and programs, under authority of 44 U.S.C. 2904 and 2906. Such disclosure shall be made in accordance with the GSA regulations governing inspection of records for this purpose, and any other relevant (i.e., GSA or Commerce) directive. Such disclosure shall not be used to make determinations about individuals.
8. A record from this system of records may be disclosed, as a routine use, to the public after either publication of the application pursuant to 35 U.S.C. 122(b) or issuance of a patent pursuant to 35 U.S.C. 151. Further, a record may be disclosed, subject to the limitations of 37 CFR 1.14, as a routine use, to the public if the record was filed in an application which became abandoned or in which the proceedings were terminated and which application is referenced by either a published application, an application open to public inspection or an issued patent.
9. A record from this system of records may be disclosed, as a routine use, to a Federal, State, or local law enforcement agency, if the USPTO becomes aware of a violation or potential violation of law or regulation.

Notice of Allowability	Application No. 13/562,210	Applicant(s) CHU, WILLIAM W. Y.	
	Examiner Hosuk Song	Art Unit 2435	AIA (First Inventor to File) Status No

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address--

All claims being allowable, PROSECUTION ON THE MERITS IS (OR REMAINS) CLOSED in this application. If not included herewith (or previously mailed), a Notice of Allowance (PTOL-85) or other appropriate communication will be mailed in due course. **THIS NOTICE OF ALLOWABILITY IS NOT A GRANT OF PATENT RIGHTS.** This application is subject to withdrawal from issue at the initiative of the Office or upon petition by the applicant. See 37 CFR 1.313 and MPEP 1308.

1. ☒ This communication is responsive to Amendment After Final filed on 4/17/13.
☐ A declaration(s)/affidavit(s) under **37 CFR 1.130(b)** was/were filed on ____.
2. ☐ An election was made by the applicant in response to a restriction requirement set forth during the interview on ____; the restriction requirement and election have been incorporated into this action.
3. ☒ The allowed claim(s) is/are 14-25,29-44,46,47 and 49-54. As a result of the allowed claim(s), you may be eligible to benefit from the **Patent Prosecution Highway** program at a participating intellectual property office for the corresponding application. For more information, please see http://www.uspto.gov/patents/init_events/pph/index.jsp or send an inquiry to PPHfeedback@uspto.gov.
4. ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

Certified copies:

a) ☐ All b) ☐ Some *c) ☐ None of the:

1. ☐ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. ____.
3. ☐ Copies of the certified copies of the priority documents have been received in this national stage application from the International Bureau (PCT Rule 17.2(a)).

* Certified copies not received: ____.

Interim copies:

a) ☐ All b) ☐ Some c) ☐ None of the: Interim copies of the priority documents have been received.

Applicant has THREE MONTHS FROM THE "MAILING DATE" of this communication to file a reply complying with the requirements noted below. Failure to timely comply will result in ABANDONMENT of this application.
THIS THREE-MONTH PERIOD IS NOT EXTENDABLE.

5. ☐ CORRECTED DRAWINGS (as "replacement sheets") must be submitted.
☐ including changes required by the attached Examiner's Amendment / Comment or in the Office action of Paper No./Mail Date ____.

Identifying indicia such as the application number (see 37 CFR 1.84(c)) should be written on the drawings in the front (not the back) of each sheet. Replacement sheet(s) should be labeled as such in the header according to 37 CFR 1.121(d).

6. ☐ DEPOSIT OF and/or INFORMATION about the deposit of BIOLOGICAL MATERIAL must be submitted. Note the attached Examiner's comment regarding REQUIREMENT FOR THE DEPOSIT OF BIOLOGICAL MATERIAL.

Attachment(s)

1. <input type="checkbox"/> Notice of References Cited (PTO-892) 2. <input type="checkbox"/> Information Disclosure Statements (PTO/SB/08), Paper No./Mail Date ____ 3. <input type="checkbox"/> Examiner's Comment Regarding Requirement for Deposit of Biological Material 4. <input type="checkbox"/> Interview Summary (PTO-413), Paper No./Mail Date ____	5. <input type="checkbox"/> Examiner's Amendment/Comment 6. <input checked="" type="checkbox"/> Examiner's Statement of Reasons for Allowance 7. <input type="checkbox"/> Other ____
--	--

/Hosuk Song/
Primary Examiner, Art Unit 2435

Reasons for Allowance

The following is an examiner's statement of reasons for allowance: The remarks submitted by the Applicant have been considered and are persuasive. Claims 14-25,29-44,46-47,49-54 are allowed.

Any comments considered necessary by applicant must be submitted no later than the payment of the issue fee and, to avoid processing delays, should preferably accompany the issue fee. Such submissions should be clearly labeled "Comments on Statement of Reasons for Allowance."

USPTO Contact Information

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Hosuk Song whose telephone number is (571)272-3857. The examiner can normally be reached on mon-fri.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Joseph Hirl can be reached on 5712723685. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/Hosuk Song/
Primary Examiner, Art Unit 2435

Please enter. /H.S/

Attorney Docket No. ACQI-006/05US 310578-2072

PATENT

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re application of:

William W. Y. Chu

Confirmation No.: 1045

Serial No.: 13/562,210

Examiner: Song, Hosuk

Filed: July 30, 2012

Art Unit: 2435

For: DATA SECURITY METHOD AND DEVICE FOR COMPUTER MODULES

Mail Stop Amendment

Commissioner for Patents

P.O. Box 1450

Alexandria, VA 22313-1450

SUPPLEMENTAL RESPONSE

This communication is in response to a telephone call received from Examiner Song on April 24, 2013.

Amendments to the claims begin on page 2.

Remarks begin on page 10.

The Commissioner is hereby authorized to charge any required fees and to credit any overpayments to Cooley LLP's deposit account No. 50-1283.



US Patent & Trademark Office

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Results 1 - 20 of 25

Sort by relevance in expanded fc

Result page: 1 2 next

- 1 [A Reflective NetGAP Logic Framework Design](#)
Songsen Yu, Yipu Zhan, Qinglin Cai, Yong-Hua Wang
August 2008 **PEITS '08**: Proceedings of the 2008 Workshop on Power Electronics and Intelligent Transportation Sys
Publisher: IEEE Computer Society
Full text available: [Publisher Site](#)
Bibliometrics: Downloads (6 Weeks): n/a, Downloads (12 Months): n/a, Downloads (Overall): n/a, Citation Count:

Adopting expert hardware to physical isolate the Trusted network from the Non-Trusted network can prevent all k of attack basing on network layer and operating system layer etc. This paper comes up with network isolation sys model based on Reflective ...

Keywords: NetGAP, Reflective GAP, physical isolation, Trusted network
- 2 [Proceedings of the 14th international conference on Principles of distributed systems](#)
Chenyang Lu, Ikshimitsu Mazuzawa, Mohamed Moshan
December 2010 **OPODIS '10**: Proceedings of the 14th international conference on Principles of distributed systems
Publisher: Springer-Verlag
Bibliometrics: Downloads (6 Weeks): 0, Downloads (12 Months): 6, Downloads (Overall): 30, Citation Count: 39
- 3 [Reconfigurable Computing: The Theory and Practice of FPGA-Based Computation](#)
Scott Hauck, Andre DeHon
November 2007 Reconfigurable Computing: The Theory and Practice of FPGA-Based Computation
Publisher: Morgan Kaufmann Publishers Inc.
Full text available: [The ACM Learning Center](#), PDF (8.85 MB)
Bibliometrics: Downloads (6 Weeks): 19, Downloads (12 Months): 222, Downloads (Overall): 222, Citation Count: 29


The main characteristic of Reconfigurable Computing is the presence of hardware that can be reconfigured to implement specific functionality more suitable for specially tailored hardware than on a simple uniprocessor. Reconfigurable computing systems ...
Keywords: Applied, Computer Science, Electricity
- 4 [On-Chip Communication Architectures: System on Chip Interconnect](#)
Giovanni De Micheli, Luca Benini
April 2008 On-Chip Communication Architectures: System on Chip Interconnect
Publisher: Morgan Kaufmann Publishers Inc.
Full text available: [The ACM Learning Center](#), PDF (3.52 MB)
Bibliometrics: Downloads (6 Weeks): 11, Downloads (12 Months): 142, Downloads (Overall): 149, Citation Count: 54

Over the past decade, system-on-chip (SoC) designs have evolved to address the ever increasing complexity of applications, fueled by the era of digital convergence. Improvements in process technology have effectively shrunk board-level components so ...
Keywords: Circuits, Computer Science, Electricity, Microelectronics
- 5 [Continuous Remote Mobile Identity Management Using Biometric Integrated Touch-Display](#)

Tao Feng, Ziyi Liu, Bogdan Carbutar, Dainis Bumber, Weidong Shi

December 2012 **MI CROW '12**: Proceedings of the 2012 45th Annual IEEE/ACM International Symposium on Microarchitecture Workshops

Publisher: IEEE Computer Society

Full text available:  PDF (2.25 MB)

Bibliometrics: Downloads (6 Weeks): n/a, Downloads (12 Months): n/a, Downloads (Overall): n/a, Citation Count: 0

Abstract While enriching the user experiences, the development of mobile devices and applications introduces new security and privacy vulnerabilities for the remote services accessed by mobile device users. A trusted and usable authentication architecture for ...

Keywords: mobile device online authentication, continuous implicit authentication, biometric touch-display

6 [Keeping Secrets in Hardware: The Microsoft Xbox™ Case Study](#)

[Andrew Huang](#)

August 2002 **CHES '02**: Revised Papers from the 4th International Workshop on Cryptographic Hardware and Embedded Systems

Publisher: Springer-Verlag

Bibliometrics: Downloads (6 Weeks): n/a, Downloads (12 Months): n/a, Downloads (Overall): n/a, Citation Count: 6


This paper discusses the hardware foundations of the cryptosystem employed by the Xbox™ video game console Microsoft. A secret boot block overlay is buried within a system ASIC. This secret boot block decrypts and verifies portions of an external ...

7 [How to make business with computer vision technology](#)

[Giovanni E. Garibotto](#)

September 2005 **ICI AP'05**: Proceedings of the 13th international conference on Image Analysis and Processing

Publisher: Springer-Verlag

Full text available:  [Publisher Site](#)

Bibliometrics: Downloads (6 Weeks): n/a, Downloads (12 Months): n/a, Downloads (Overall): n/a, Citation Count:

Business development in highly competitive new markets is strongly dependent on the level of technology innovation. Actually, the real success of a new product is affected by many other factors in the development chain, including customer requirements ...

8 [A low-power transceiver design for FlexRay-based communication systems](#)

Chua-Chin Wang, Chih-Lin Chen, Jie-Jyun Li, Gang-Neng Sung, Tai-Hao Yeh, Chun-Ying Juan

April 2013 **Microelectronics Journal**, Volume 44 Issue 4

Publisher: Elsevier Science Publishers B. V.

Bibliometrics: Downloads (6 Weeks): n/a, Downloads (12 Months): n/a, Downloads (Overall): n/a, Citation Count: 0

This paper presents a FlexRay Transceiver (FRT) used in an in-vehicle network compliant with FlexRay physical layer standards. FlexRay is a new standard for data/signal communication among ECUs (electronic control unit) installed in a vehicle. FRT at ...

Keywords: Automobile electronic, Bus Driver, FlexRay, In-vehicle networking

9 [Home station, novel architecture of home gateway and its implementations](#)

[Kwang-Soon Choi](#), [Seung-Ok Lim](#), [Young-Choon Park](#), [Kwang-Mo Jung](#)

December 2004 **AI C'04**: Proceedings of the 4th WSEAS International Conference on Applied Informatics and Communications

Publisher: World Scientific and Engineering Academy and Society (WSEAS)

Bibliometrics: Downloads (6 Weeks): 0, Downloads (12 Months): 0, Downloads (Overall): 1, Citation Count: 2

Although a number of home networking solutions such as wired and wireless technologies, middleware technologies and home gateway technologies have been emerging, none of them dominates the home networking market with satisfying users' demand on higher ...

Keywords: common protocol, home gateway, home network, home station, residential gateway

10 [FPGA Architecture: Survey and Challenges](#)

[Ian Kuon](#), [Russell Tessier](#), [Jonathan Rose](#)

February 2008 **Foundations and Trends® in Electronic Design Automation**, Volume 2 Issue 2

Publisher: Now Publishers Inc.

Bibliometrics: Downloads (6 Weeks): n/a, Downloads (12 Months): n/a, Downloads (Overall): n/a, Citation Count: 10


Field-Programmable Gate Arrays (FPGAs) have become one of the key digital circuit implementation media over the last decade. A crucial part of their creation lies in their architecture, which governs the nature of their programmable logic functionality ...

11 [Localized algorithms for coverage boundary detection in wireless sensor networks](#)

[Chi Zhang](#), [Yanchao Zhang](#), [Yuguang Fang](#)

January 2009 **Wireless Networks**, Volume 15 Issue 1

Publisher: Springer-Verlag New York, Inc.

Full text available:  PDF (1.34 MB)

Bibliometrics: Downloads (6 Weeks): 10, Downloads (12 Months): 46, Downloads (Overall): 418, Citation Count: 3

Connected coverage, which reflects how well a target field is monitored under the base station, is the most important performance metric used to measure the quality of surveillance that wireless sensor networks (WSNs) can provide facilitate the measurement ...

Keywords: computational geometry, connected coverage, localized algorithm, wireless sensor networks (WSNs)

12 [Traversable Region Modeling for Outdoor Navigation](#)

Cristina Gastejon, Beatriz L. Roca, Dolores Blanco, Luis Moreno

August 2005

Journal of Intelligent and Robotic Systems, Volume 43 Issue 2-4


Publisher: Kluwer Academic Publishers

Bibliometrics: Downloads (6 Weeks): n/a, Downloads (12 Months): n/a, Downloads (Overall): n/a, Citation Count:

This article presents a new methodology to build, in real-time, compact local and global maps for outdoor navigation. The environment information is obtained from a 3D laser range. The navigation model, called Traversable Regions Model (TRM), is based ...

Keywords: 3D scanner laser, navigation map, outdoor, robot mapping, traversability


13 [An exploratory study of identifier renamings](#)

 Leih M. Eshkevari, Vanara Arasudivya, Massimiliano Di Penta, Jesse Oliveto, Yann-Gaël Guéhéneuc, Giuliana Anton

May 2011

MSR '11: Proceedings of the 8th Working Conference on Mining Software Repositories

Publisher: ACM 

Full text available:  PDF (975.52 KB)

Bibliometrics: Downloads (6 Weeks): 7, Downloads (12 Months): 64, Downloads (Overall): 120, Citation Count: 1

Identifiers play an important role in source code understandability, maintainability, and fault-proneness. This paper reports a study of identifier renamings in software systems, studying how terms (identifier atomic components) change in source code ...

Keywords: identifier renaming, mining repositories, software evolution

14 [Design and Synthesis of a Multiprocessor System-on-Chip Architecture for Real-Time Biomedical Signal Processing in Gamma Cameras](#)

Kai Sun, Meng Wang, Zhi Shao, Hui Liu, Hongxing Wei, Jianming Wang

April 2010

Journal of Signal Processing Systems, Volume 59 Issue 1

Publisher: Kluwer Academic Publishers

Bibliometrics: Downloads (6 Weeks): n/a, Downloads (12 Months): n/a, Downloads (Overall): n/a, Citation Count:

MPSoC (Multi-Processor System-on-Chip) architecture is becoming increasingly used because it can provide design much more opportunities to meet specific performance and power goals. In this paper, we propose an MPSoC architecture for implementing ...

Keywords: Multiprocessor system-on-chip, Real time


15 [A closer look at security in random number generators design](#)

Walter Fischer

May 2012

COSADE'12: Proceedings of the Third international conference on Constructive Side-Channel Analysis Secure Design

Publisher: Springer-Verlag

Full text available:  Publisher Site

Bibliometrics: Downloads (6 Weeks): n/a, Downloads (12 Months): n/a, Downloads (Overall): n/a, Citation Count:

The issue of random number generation is crucial for the implementation of cryptographic systems. Random numbers are often used in key generation processes, authentication protocols, zero-knowledge protocols, padding, in many signature and encryption ...

Keywords: cryptographic hardware, data security, digital design, random number generation, statistical tests

16 [Proceedings of the 2008 Asia and South Pacific Design Automation Conference](#)

Chong-Min Kyung, Kiyoungh Choi, Seungho Ha

January 2008

ASP-DAC '08: Proceedings of the 2008 Asia and South Pacific Design Automation Conference

Publisher: IEEE Computer Society Press

Bibliometrics: Downloads (6 Weeks): 200, Downloads (12 Months): 1845, Downloads (Overall): 20515, Citation Count:

It is our great pleasure and honor to welcome you to the 13th ASP-DAC, January 21 - 24, 2008 held in Seoul, Korea. Astounding growth of economy in Asia for the last quarter century is based on the zeal and quest for the development of industry and information ...


17 [A programmable receiver for communication systems and its application to impulse radio](#)

Roman Merz, Cyril Bottonat, Frédéric Chastelain, Pierre-André Farine

January 2009

Research Letters in Communications, Volume 2009

Publisher: Hindawi Publishing Corp.

Full text available:  [PDF](#) (454.98 KB)

Bibliometrics: Downloads (6 Weeks): 0, Downloads (12 Months): 3, Downloads (Overall): 30, Citation Count: 1

The design of a programmable receiver for an ultra wideband (UWB) communication is presented. The receiver is a fast analog to digital converter (ADC) and a field programmable gate array (FPGA) allowing a rapid performance evaluation for various ...


18 [Electromagnetic eavesdropping risks of flat-panel displays](#)

Marius G. Kuhn

May 2004

PET'04: Proceedings of the 4th international conference on Privacy Enhancing Technologies

Publisher: Springer-Verlag

Full text available:  [Publisher Site](#)

Bibliometrics: Downloads (6 Weeks): n/a, Downloads (12 Months): n/a, Downloads (Overall): n/a, Citation Count: 3

Electromagnetic eavesdropping of computer displays – first demonstrated to the general public by van Eck in 1981 not restricted to cathode-ray tubes. Modern flat-panel displays can be at least as vulnerable. They are equally driven by ...



19 [Optimizing investment strategies with the reconfigurable hardware platform RIVYERA](#)

Christoph Starke, Vasco Grossmann, Lars Wienbrandt, Sven Koschnicke, John Carlstens, Manfred Schimmier

January 2012

International Journal of Reconfigurable Computing, Volume 2012

Publisher: Hindawi Publishing Corp.

Full text available:  [Publisher Site](#),  [PDF](#) (1.41 MB)

Bibliometrics: Downloads (6 Weeks): 3, Downloads (12 Months): 7, Downloads (Overall): 7, Citation Count:

The hardware structure of a processing element used for optimization of an investment strategy for financial markets is presented. It is shown how this processing element can be multiply implemented on the massively parallel FPGA-machine RIVYERA. This ...

20 [Challenges in a future IP/ethernet-based in-car network for real-time applications](#)

Hyung-Jae Lim, Lars Völken, Daniel Herrscher

June 2011

DAC '11: Proceedings of the 48th Design Automation Conference

Publisher: ACM

Full text available:  [PDF](#) (397.02 KB)

Bibliometrics: Downloads (6 Weeks): 8, Downloads (12 Months): 59, Downloads (Overall): 105, Citation Count: 1

In current vehicles, a large number of control units are connected by several automotive specific communication technologies facilitating innovative distributed applications. At the same time, computers and entertainment devices use IP and commodity communications ...

Keywords: QoS, ethernet, in-vehicle communication, performance evaluation, simulation

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14


Issue Classification 	Application/Control No. 13562210	Applicant(s)/Patent Under Reexamination CHU, WILLIAM W. Y.
	Examiner HOSUK SONG	Art Unit 2435

NONE (Assistant Examiner) _____ (Date) _____		Total Claims Allowed: 36	
/HOSUK SONG/ Primary Examiner. Art Unit 2435 (Primary Examiner) _____ (Date) _____		4/18/13 O.G. Print Claim(s) 14	O.G. Print Figure 1

Issue Classification 	Application/Control No. 13562210	Applicant(s)/Patent Under Reexamination CHU, WILLIAM W. Y.
	Examiner HOSUK SONG	Art Unit 2435

<input type="checkbox"/> Claims renumbered in the same order as presented by applicant <input type="checkbox"/> CPA <input type="checkbox"/> T.D. <input type="checkbox"/> R.1.47															
Final	Original	Final	Original	Final	Original	Final	Original	Final	Original	Final	Original	Final	Original	Final	Original
1	1	17	17	30	33	44	49								
2	2	18	18	31	34	45	50								
3	3	19	19	32	35	46	51								
4	4	20	20	33	36	47	52								
5	5	21	21	34	37	48	53								
6	6	22	22	35	38	49	54								
7	7	23	23	36	39										
8	8	24	24	37	40										
9	9	25	25	38	41										
10	10		26	39	42										
11	11		27	40	43										
12	12		28	41	44										
13	13	26	29		45										
14	14	27	30	42	46										
15	15	28	31	43	47										
16	16	29	32		48										

NONE (Assistant Examiner) _____ (Date) _____		Total Claims Allowed: 36	
/HOSUK SONG/ Primary Examiner. Art Unit 2435 (Primary Examiner) _____ (Date) _____		O.G. Print Claim(s) 14	O.G. Print Figure 1

Search Notes 	Application/Control No. 13562210	Applicant(s)/Patent Under Reexamination CHU, WILLIAM W. Y.
	Examiner HOSUK SONG	Art Unit 2435

CPC- SEARCHED		
Symbol	Date	Examiner

CPC COMBINATION SETS - SEARCHED		
Symbol	Date	Examiner

US CLASSIFICATION SEARCHED			
Class	Subclass	Date	Examiner
726	2-9,16-21,34,36	4/18/13	HS
713	182-183,192-194	4/18/13	HS
710	1,7,8,15,20,22,100	4/18/13	HS

SEARCH NOTES		
Search Notes	Date	Examiner
EAST, foreign patent database, IBM TDB, USPGPUB	4/18/13	HS
NPL	4/18/13	HS

INTERFERENCE SEARCH			
US Class/ CPC Symbol	US Subclass / CPC Group	Date	Examiner
726	2-9,16-21,34,36	4/18/13	HS
713	182-183,192-194	4/18/13	HS
710	1,7,8,15,20,22,100	4/18/13	HS

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Please enter. /H.S/

Attorney Docket No. ACQI-006/05US 310578-2072

PATENT

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re application of:
William W. Y. Chu

Confirmation No.: 1045

Serial No.: 13/562,210

Examiner: Song, Hosuk

Filed: July 30, 2012

Art Unit: 2435

For: DATA SECURITY METHOD AND DEVICE FOR COMPUTER MODULES

Mail Stop Amendment
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

RESPONSE

This communication is in response to the final Office Action mailed February 21, 2013.

Remarks begin on page 2.

The Commissioner is hereby authorized to charge any required fees and to credit any overpayments to Cooley LLP's deposit account No. 50-1283.

REMARKS

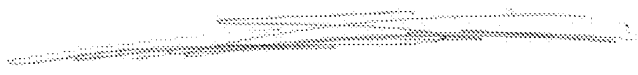
Applicant submits a supplemental declaration for reissue patent application to overcome the rejection. Accordingly, the application is in a condition for allowance.

Date: April 17, 2013

Customer No. 58249
COOLEY LLP
1299 Pennsylvania Ave. NW, Suite 700
Washington, DC 20004

Tel: (650) 843-5622
Fax: (202) 842-7899

Respectfully submitted,
COOLEY LLP

By: 
William S. Galliani
Reg. No. 33,885

EAST Search History

EAST Search History (Prior Art)

Ref #	Hits	Search Query	DBs	Default Operator	Plurals	Time Stamp
S135	294	(low adk3 voltage adj4 differential adj4 signal) and serial adj3 bit adj4 channel	US-PGPUB; USPAT	OR	ON	2013/04/18 15:14
S136	300	(low adk3 voltage adj4 differential adj4 signal or LVDS) and serial adj3 bit adj4 channel	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2013/04/18 15:15
S137	33	(low adj3 voltage adj4 differential adj4 signal or LVDS) and serial adj3 bit adj4 channel	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2013/04/18 15:15
S138	353	(low adj3 voltage adj4 differential adj4 signal) and serial and USB	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2013/04/18 15:16
S139	1073	(low adj3 voltage adj4 differential adj4 signal or LVDS) and serial and PCI	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2013/04/18 15:16
S140	614	(low adj3 voltage adj4 differential adj4 signal or LVDS) and serial adj3 bit	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2013/04/18 15:16
S141	312	(low adj3 voltage adj4 differential adj4 signal or LVDS) and serial adj3 bit and (PCI or peripheral adj3 component adj4 interconnect)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2013/04/18 15:17
S142	346	(PCI or peripheral adj3 component adj4 interface) and (LVDS or low adj3 voltage adj4 differential adj5 signal) near5 (channel or link or path or line)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2013/04/18 15:17
S143	229	(PCI or peripheral adj3 component adj4 interface) and (LVDS or low adj3 voltage adj4 differential adj5 signal) and (serial adj3 bit) and (plug adj4 play or USB)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2013/04/18 15:18
S144	34	(PCI or peripheral adj3 component adj4 interface) and (LVDS or low adj3 voltage adj4 differential adj5 signal) near5 (channel or link or path or line or bus) near7 (plural\$4 or many or multiple or second)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2013/04/18 15:19
S145	293	(PCI or peripheral adj3 component adj4	US-PGPUB;	OR	ON	2013/04/18

		interface) and (LVDS or low adj3 voltage adj4 differential adj5 signal) near5 (channel or link or path or line) and (both or unidirect\$4 or two adj3 way)	USPAT; EPO; JPO; DERWENT; IBM_TDB			15:19
S146	133	(PCI or peripheral adj3 component adj4 interface) and (LVDS or low adj3 voltage adj4 differential adj5 signal) near5 (channel or link or path or line) and (both or unidirect\$4 or two adj3 way) and (serial adj3 bit)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2013/04/18 15:21
S147	3657	726/2.ccls.	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2013/04/18 15:22
S148	3924	726/3.ccls.	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2013/04/18 15:23
S149	5194	726/4.ccls.	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2013/04/18 15:23
S150	3221	726/5.ccls.	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2013/04/18 15:23
S151	2115	726/6.ccls.	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2013/04/18 15:23
S152	2042	726/7.ccls.	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2013/04/18 15:24
S153	744	726/8.ccls.	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2013/04/18 15:24
S154	1595	726/9.ccls.	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2013/04/18 15:24
S155	725	726/16.ccls.	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2013/04/18 15:24
S156	1212	726/17.ccls.	US-PGPUB; USPAT; EPO; JPO; DERWENT;	OR	ON	2013/04/18 15:24

			IBM_TDB			
S157	772	726/18.ccls.	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2013/04/18 15:24
S158	1139	726/19.ccls.	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2013/04/18 15:24
S159	748	726/20.ccls.	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2013/04/18 15:24
S160	1294	726/21.ccls.	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2013/04/18 15:24
S161	731	726/34.ccls.	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2013/04/18 15:25
S162	150	726/36.ccls.	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2013/04/18 15:25
S163	2880	713/182.ccls.	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2013/04/18 15:26
S164	1192	713/183.ccls.	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2013/04/18 15:26
S165	390	713/192.ccls.	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2013/04/18 15:26
S166	4634	713/193.ccls.	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2013/04/18 15:26
S167	1311	713/194.ccls.	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2013/04/18 15:26
S168	1761	710/1.ccls.	US-PGPUB; USPAT; EPO; JPO; DERWENT;	OR	ON	2013/04/18 15:26

			IBM_TDB			
S169	380	710/7.ccls.	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2013/04/18 15:26
S170	3286	710/8.ccls.	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2013/04/18 15:26
S171	1996	710/15.ccls.	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2013/04/18 15:26
S172	784	710/20.ccls.	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2013/04/18 15:26
S173	2401	710/22.ccls.	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2013/04/18 15:26
S174	2123	710/100.ccls.	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2013/04/18 15:27
S175	1	(low adj3 voltage adj4 differential adj4 signal or LVDS) and serial adj3 bit and 710/1.ccls.	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2013/04/18 15:27
S176	0	(low adj3 voltage adj4 differential adj4 signal or LVDS) and serial adj3 bit and 710/7.ccls.	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2013/04/18 15:27
S177	0	(low adj3 voltage adj4 differential adj4 signal or LVDS) and serial adj3 bit and 710/8.ccls.	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2013/04/18 15:28
S178	0	(low adj3 voltage adj4 differential adj4 signal or LVDS) and serial adj3 bit and 710/15.ccls.	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2013/04/18 15:28
S179	0	(low adj3 voltage adj4 differential adj4 signal or LVDS) and serial adj3 bit and 710/20.ccls.	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2013/04/18 15:29
S180	1	(low adj3 voltage adj4 differential adj4 signal or LVDS) and serial adj3 bit and 710/22.ccls.	US-PGPUB; USPAT; EPO; JPO; DERWENT;	OR	ON	2013/04/18 15:29


			IBM_TDB			
S181	5	(low adj3 voltage adj4 differential adj4 signal or LVDS) and serial adj3 bit and 710/100.ccls.	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2013/04/18 15:29
S182	4	(low adj3 voltage adj4 differential adj4 signal or LVDS) and serial adj3 bit and 726/2.ccls.	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2013/04/18 15:30
S183	1	(low adj3 voltage adj4 differential adj4 signal or LVDS) and serial adj3 bit and 726/3.ccls.	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2013/04/18 15:30
S184	1	(low adj3 voltage adj4 differential adj4 signal or LVDS) and serial adj3 bit and 726/4.ccls.	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2013/04/18 15:30
S185	0	(low adj3 voltage adj4 differential adj4 signal or LVDS) and serial adj3 bit and 726/6.ccls.	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2013/04/18 15:40
S186	1	(low adj3 voltage adj4 differential adj4 signal or LVDS) and serial adj3 bit and 726/7.ccls.	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2013/04/18 15:40
S187	0	(low adj3 voltage adj4 differential adj4 signal or LVDS) and serial adj3 bit and 726/8.ccls.	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2013/04/18 15:40
S188	3	(low adj3 voltage adj4 differential adj4 signal or LVDS) and serial adj3 bit and 726/9.ccls.	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2013/04/18 15:40
S189	0	(low adj3 voltage adj4 differential adj4 signal or LVDS) and serial adj3 bit and 726/16.ccls.	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2013/04/18 15:41
S190	0	(low adj3 voltage adj4 differential adj4 signal or LVDS) and serial adj3 bit and 726/17.ccls.	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2013/04/18 15:41
S191	3	(low adj3 voltage adj4 differential adj4 signal or LVDS) and serial adj3 bit and 726/18.ccls.	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2013/04/18 15:42
S192	0	(low adj3 voltage adj4 differential adj4 signal or LVDS) and serial adj3 bit and 726/19.ccls.	US-PGPUB; USPAT; EPO; JPO; DERWENT;	OR	ON	2013/04/18 15:42

			IBM_TDB			
S193	0	(low adj3 voltage adj4 differential adj4 signal or LVDS) and serial adj3 bit and 726/20.ccls.	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2013/04/18 15:42
S194	0	(low adj3 voltage adj4 differential adj4 signal or LVDS) and serial adj3 bit and 726/21.ccls.	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2013/04/18 15:42
S195	2	(low adj3 voltage adj4 differential adj4 signal or LVDS) and serial adj3 bit and 726/34.ccls.	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2013/04/18 15:42
S196	2	(low adj3 voltage adj4 differential adj4 signal or LVDS) and serial adj3 bit and 726/36.ccls.	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2013/04/18 15:42
S197	0	(low adj3 voltage adj4 differential adj4 signal or LVDS) and serial adj3 bit and 713/182.ccls.	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2013/04/18 15:43
S199	2	(low adj3 voltage adj4 differential adj4 signal or LVDS) and serial adj3 bit and 713/183.ccls.	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2013/04/18 15:43
S200	0	(low adj3 voltage adj4 differential adj4 signal or LVDS) and serial adj3 bit and 713/192.ccls.	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2013/04/18 15:44
S201	5	(low adj3 voltage adj4 differential adj4 signal or LVDS) and serial adj3 bit and 713/193.ccls.	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2013/04/18 15:44
S202	0	(low adj3 voltage adj4 differential adj4 signal or LVDS) and serial adj3 bit and 713/194.ccls.	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2013/04/18 15:45
S203	7	(unidirection\$4 and (LVDS or low adj3 voltage adj4 differential adj5 signal) and serial and bit and stream and bridge).CLM.	US-PGPUB; USPAT	OR	ON	2013/04/18 15:49
S204	7	(unidirection\$4 and (LVDS or low adj3 voltage adj4 differential adj5 signal) and serial and bit and stream and bridge and channel).CLM.	US-PGPUB; USPAT	OR	ON	2013/04/18 15:49
S205	7	(unidirection\$4 and (LVDS or low adj3 voltage adj4 differential adj5 signal) and serial and bit and stream and bridge and channel and encod\$4).CLM.	US-PGPUB; USPAT	OR	ON	2013/04/18 15:49
S206	4	(unidirection\$4 and (LVDS or low adj3	US-PGPUB;	OR	ON	2013/04/18

		voltage adj4 differential adj5 signal) and serial and bit and stream and bridge and channel and graphics and controller).CLM.	USPAT			15:50
S207	5	(unidirection\$4 and (LVDS or low adj3 voltage adj4 differential adj5 signal) and serial and bit and stream and single and chip and channel and graphics and controller).CLM.	US-PGPUB; USPAT	OR	ON	2013/04/18 15:50
S208	12	(unidirection\$4 and (LVDS or low adj3 voltage adj4 differential adj5 signal) and serial and bit and channel and opposite and (USB or universal adj3 serial adj4 bus)).CLM.	US-PGPUB; USPAT	OR	ON	2013/04/18 15:52
S209	8	(unidirection\$4 and (LVDS or low adj3 voltage adj4 differential adj5 signal) and serial and bit and channel and opposite and (USB or universal adj3 serial adj4 bus) and two and connector).CLM.	US-PGPUB; USPAT	OR	ON	2013/04/18 15:53
S210	34	(PCI or peripheral adj3 component adj4 interface) and (LVDS or low adj3 voltage adj4 differential adj5 signal) near5 (channel or link or path or line or bus) near7 (plural\$4 or many or multiple or second)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2013/04/18 16:03

4/ 19/ 2013 6:46:36 AM

C:\ Users\ hsong\ Documents\ EAST\ Workspaces\ 13562210.wsp

Index of Claims 	Application/Control No. 13562210	Applicant(s)/Patent Under Reexamination CHU, WILLIAM W. Y.
	Examiner HOSUK SONG	Art Unit 2435

✓	Rejected	-	Cancelled	N	Non-Elected	A	Appeal
=	Allowed	÷	Restricted	I	Interference	O	Objected

<input type="checkbox"/> Claims renumbered in the same order as presented by applicant					<input type="checkbox"/> CPA		<input type="checkbox"/> T.D.		<input type="checkbox"/> R.1.47	
CLAIM		DATE								
Final	Original	11/15/2012	02/13/2013	04/18/2013						
1	1	-	-	-						
2	2	-	-	-						
3	3	-	-	-						
4	4	-	-	-						
5	5	-	-	-						
6	6	-	-	-						
7	7	-	-	-						
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14	14	=	✓	✓						
15	15	=	✓	✓						
16	16	=	✓	✓						
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	28	O	-	-						
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29	32	=	✓	✓						
30	33	=	✓	✓						
31	34	=	✓	✓						
32	35	=	✓	✓						
33	36	=	✓	✓						

<p align="center">Index of Claims</p> 	Application/Control No. 13562210	Applicant(s)/Patent Under Reexamination CHU, WILLIAM W. Y.
	Examiner HOSUK SONG	Art Unit 2435

✓	Rejected	-	Cancelled	N	Non-Elected	A	Appeal
=	Allowed	÷	Restricted	I	Interference	O	Objected

<input type="checkbox"/> Claims renumbered in the same order as presented by applicant					<input type="checkbox"/> CPA		<input type="checkbox"/> T.D.		<input type="checkbox"/> R.1.47	
CLAIM		DATE								
Final	Original	11/15/2012	02/13/2013	04/18/2013						
34	37	=	✓	✓						
35	38	=	✓	✓						
36	39	=	✓	✓						
37	40	=	✓	✓						
38	41	=	✓	✓						
39	42	=	✓	✓						
40	43	=	✓	✓						
41	44	✓	✓	✓						
	45	O	-	-						
42	46	O	✓	✓						
43	47	✓	✓	✓						
	48	✓	-	-						
44	49	O	✓	✓						
45	50	✓	✓	✓						
46	51	✓	✓	✓						
47	52	✓	✓	✓						
48	53	✓	✓	✓						
49	54	✓	✓	✓						

PART B - FEE(S) TRANSMITTAL

Complete and send this form, together with applicable fee(s), to: **Mail Stop ISSUE FEE**
Commissioner for Patents
P.O. Box 1450
Alexandria, Virginia 22313-1450
or Fax (571)-273-2885

INSTRUCTIONS: This form should be used for transmitting the ISSUE FEE and PUBLICATION FEE (if required). Blocks 1 through 5 should be completed where appropriate. All further correspondence including the Patent, advance orders and notification of maintenance fees will be mailed to the current correspondence address as indicated unless corrected below or directed otherwise in Block 1, by (a) specifying a new correspondence address; and/or (b) indicating a separate "FEE ADDRESS" for maintenance fee notifications.

CURRENT CORRESPONDENCE ADDRESS (Note: Use Block 1 for any change of address)

58249 7590 06/10/2013
COOLEY LLP
ATTN: Patent Group
1299 Pennsylvania Avenue, NW
Suite 700
Washington, DC 20004

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Certificate of Mailing or Transmission

I hereby certify that this Fee(s) Transmittal is being deposited with the United States Postal Service with sufficient postage for first class mail in an envelope addressed to the Mail Stop ISSUE FEE address above, or being facsimile transmitted to the USPTO (571) 273-2885, on the date indicated below.

(Depositor's name)
(Signature)
(Date)

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
13/562,210	07/30/2012	William W. Y. Chu	ACQI-006/05US 310578-2072	1045

TITLE OF INVENTION: Data Security Method and Device for Computer Modules

APPL.N. TYPE	ENTITY STATUS	ISSUE FEE DUE	PUBLICATION FEE DUE	PREV. PAID ISSUE FEE	TOTAL FEE(S) DUE	DATE DUE
nonprovisional	UNDISCOUNTED	\$1780	\$0	\$0	\$1780	09/10/2013

EXAMINER	ART UNIT	CLASS-SUBCLASS
SONG, HOSUK	2435	726-020000

1. Change of correspondence address or indication of "Fee Address" (37 CFR 1.363).
☐ Change of correspondence address (or Change of Correspondence Address form PTO/SB/122) attached.
☐ "Fee Address" indication (or "Fee Address" Indication form PTO/SB/47; Rev 03-02 or more recent) attached. **Use of a Customer Number is required.**

2. For printing on the patent front page, list
 (1) the names of up to 3 registered patent attorneys or agents OR, alternatively,
 (2) the name of a single firm (having as a member a registered attorney or agent) and the names of up to 2 registered patent attorneys or agents. If no name is listed, no name will be printed.
 1 Cooley LLP
 2 _____
 3 _____

3. ASSIGNEE NAME AND RESIDENCE DATA TO BE PRINTED ON THE PATENT (print or type)

PLEASE NOTE: Unless an assignee is identified below, no assignee data will appear on the patent. If an assignee is identified below, the document has been filed for recordation as set forth in 37 CFR 3.11. Completion of this form is NOT a substitute for filing an assignment.

(A) NAME OF ASSIGNEE

ACQIS LLC

(B) RESIDENCE: (CITY and STATE OR COUNTRY)

McKINNEY, TEXAS

Please check the appropriate assignee category or categories (will not be printed on the patent): ☐ Individual ☒ Corporation or other private group entity ☐ Government

4a. The following fee(s) are submitted:

- ☒ Issue Fee
☐ Publication Fee (No small entity discount permitted)
☐ Advance Order - # of Copies _____

4b. Payment of Fee(s): (Please first reapply any previously paid issue fee shown above)

- ☐ A check is enclosed.
☐ Payment by credit card. Form PTO-2038 is attached.
☒ The Director is hereby authorized to charge the required fee(s), any deficiency, or credit any overpayment, to Deposit Account Number **50-1283** (enclose an extra copy of this form).

5. **Change in Entity Status** (from status indicated above)

- ☐ Applicant certifying micro entity status. See 37 CFR 1.29
- ☐ Applicant asserting small entity status. See 37 CFR 1.27
- ☐ Applicant changing to regular undiscounted fee status.

NOTE: Absent a valid certification of Micro Entity Status (see form PTO/SB/15A and 15B), issue fee payment in the micro entity amount will not be accepted at the risk of application abandonment.

NOTE: If the application was previously under micro entity status, checking this box will be taken to be a notification of loss of entitlement to micro entity status.

NOTE: Checking this box will be taken to be a notification of loss of entitlement to small or micro entity status, as applicable.

NOTE: The Issue Fee and Publication Fee (if required) will not be accepted from anyone other than the applicant; a registered attorney or agent; or the assignee or other party in interest as shown by the records of the United States Patent and Trademark Office.

Authorized Signature



Date June 26, 2013

Typed or printed name Jason C. Fan for William S. Galliani

Registration No. 54,092 | 33,885

This collection of information is required by 37 CFR 1.311. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 12 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, Virginia 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, Virginia 22313-1450.

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Electronic Patent Application Fee Transmittal				
Application Number:		13562210		
Filing Date:		30-Jul-2012		
Title of Invention:		Data Security Method and Device for Computer Modules		
First Named Inventor/Applicant Name:		William W. Y. Chu		
Filer:		William S. Galliani/Bobbie Jutras		
Attorney Docket Number:		ACQI-006/05US 310578-2072		
Filed as Large Entity				
Utility under 35 USC 111(a) Filing Fees				
Description	Fee Code	Quantity	Amount	Sub-Total in USD(\$)
Basic Filing:				
Pages:				
Claims:				
Miscellaneous-Filing:				
Petition:				
Patent-Appeals-and-Interference:				
Post-Allowance-and-Post-Issuance:				
Utility Appl Issue Fee	1501	1	1780	1780
Extension-of-Time:				

Description	Fee Code	Quantity	Amount	Sub-Total in USD(\$)
Miscellaneous:				
Total in USD (\$)				1780

Electronic Acknowledgement Receipt	
EFS ID:	16166045
Application Number:	13562210
International Application Number:	
Confirmation Number:	1045
Title of Invention:	Data Security Method and Device for Computer Modules
First Named Inventor/Applicant Name:	William W. Y. Chu
Customer Number:	58249
Filer:	William S. Galliani/Bobbie Jutras
Filer Authorized By:	William S. Galliani
Attorney Docket Number:	ACQI-006/05US 310578-2072
Receipt Date:	26-JUN-2013
Filing Date:	30-JUL-2012
Time Stamp:	19:30:12
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	yes
Payment Type	Deposit Account
Payment was successfully received in RAM	\$ 1780
RAM confirmation Number	6712
Deposit Account	501283
Authorized User	
<p>The Director of the USPTO is hereby authorized to charge indicated fees and credit any overpayment as follows:</p> <p>Charge any Additional Fees required under 37 C.F.R. Section 1.16 (National application filing, search, and examination fees)</p> <p>Charge any Additional Fees required under 37 C.F.R. Section 1.17 (Patent application and reexamination processing fees)</p>	

File Listing:					
Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1	Issue Fee Payment (PTO-85B)	ACQI-006-05US_2013-06-26_IF Payment.pdf	92143 844fe14459aae9b37d53e61ea554dcf3161 b1cdf	no	2
Warnings:					
Information:					
2	Fee Worksheet (SB06)	fee-info.pdf	30319 854f2e12fc9710267862bf8c37d2cbc89693 43cc	no	2
Warnings:					
Information:					
Total Files Size (in bytes):			122462		
<p>This Acknowledgement Receipt evidences receipt on the noted date by the USPTO of the indicated documents, characterized by the applicant, and including page counts, where applicable. It serves as evidence of receipt similar to a Post Card, as described in MPEP 503.</p> <p><u>New Applications Under 35 U.S.C. 111</u> If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application.</p> <p><u>National Stage of an International Application under 35 U.S.C. 371</u> If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.</p> <p><u>New International Application Filed with the USPTO as a Receiving Office</u> If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.</p>					



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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
13/562,210	07/30/2012	William W. Y. Chu	ACQI-006/05US 310578-2072	1045
58249	7590	07/12/2013		
COOLEY LLP ATTN: Patent Group 1299 Pennsylvania Avenue, NW Suite 700 Washington, DC 20004			EXAMINER SONG, HOSUK	
			ART UNIT 2435	PAPER NUMBER
			NOTIFICATION DATE 07/12/2013	DELIVERY MODE ELECTRONIC

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

zpatdcdocketing@cooley.com

Supplemental Notice of Allowability	Application No. 13/562,210	Applicant(s) CHU, WILLIAM W. Y.	
	Examiner Hosuk Song	Art Unit 2435	AIA (First Inventor to File) Status No

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address--

All claims being allowable, PROSECUTION ON THE MERITS IS (OR REMAINS) CLOSED in this application. If not included herewith (or previously mailed), a Notice of Allowance (PTOL-85) or other appropriate communication will be mailed in due course. **THIS NOTICE OF ALLOWABILITY IS NOT A GRANT OF PATENT RIGHTS.** This application is subject to withdrawal from issue at the initiative of the Office or upon petition by the applicant. See 37 CFR 1.313 and MPEP 1308.

1. ☐ This communication is responsive to _____.
 ☐ A declaration(s)/affidavit(s) under **37 CFR 1.130(b)** was/were filed on _____.

2. ☐ An election was made by the applicant in response to a restriction requirement set forth during the interview on _____; the restriction requirement and election have been incorporated into this action.

3. ☒ The allowed claim(s) is/are 14-25,29-44,46,47,49-54. As a result of the allowed claim(s), you may be eligible to benefit from the **Patent Prosecution Highway** program at a participating intellectual property office for the corresponding application. For more information, please see http://www.uspto.gov/patents/init_events/pph/index.jsp or send an inquiry to PPHfeedback@uspto.gov.

4. ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

Certified copies:

a) ☐ All b) ☐ Some *c) ☐ None of the:

1. ☐ Certified copies of the priority documents have been received.

2. ☐ Certified copies of the priority documents have been received in Application No. _____.

3. ☐ Copies of the certified copies of the priority documents have been received in this national stage application from the International Bureau (PCT Rule 17.2(a)).

* Certified copies not received: _____.

Applicant has THREE MONTHS FROM THE "MAILING DATE" of this communication to file a reply complying with the requirements noted below. Failure to timely comply will result in ABANDONMENT of this application.
THIS THREE-MONTH PERIOD IS NOT EXTENDABLE.

5. ☐ CORRECTED DRAWINGS (as "replacement sheets") must be submitted.
 ☐ including changes required by the attached Examiner's Amendment / Comment or in the Office action of Paper No./Mail Date _____.

Identifying indicia such as the application number (see 37 CFR 1.84(c)) should be written on the drawings in the front (not the back) of each sheet. Replacement sheet(s) should be labeled as such in the header according to 37 CFR 1.121(d).

6. ☐ DEPOSIT OF and/or INFORMATION about the deposit of BIOLOGICAL MATERIAL must be submitted. Note the attached Examiner's comment regarding REQUIREMENT FOR THE DEPOSIT OF BIOLOGICAL MATERIAL.

Attachment(s)

1. <input type="checkbox"/> Notice of References Cited (PTO-892) 2. <input type="checkbox"/> Information Disclosure Statements (PTO/SB/08), Paper No./Mail Date _____ 3. <input type="checkbox"/> Examiner's Comment Regarding Requirement for Deposit of Biological Material 4. <input type="checkbox"/> Interview Summary (PTO-413), Paper No./Mail Date _____	5. <input checked="" type="checkbox"/> Examiner's Amendment/Comment 6. <input type="checkbox"/> Examiner's Statement of Reasons for Allowance 7. <input type="checkbox"/> Other _____
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/Hosuk Song/ Primary Examiner, Art Unit 2435	
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EXAMINER'S AMENDMENT

An examiner's amendment to the record appears below. Should the changes and/or additions be unacceptable to applicant, an amendment may be filed as provided by 37 CFR 1.312. To ensure consideration of such an amendment, it **MUST** be submitted no later than the payment of the issue fee.

The application has been amended as follows.

IN THE SPECIFICATION:

Please amend beginning at col.1, line 6 of the specification as follows.

Notice: More than one reissue application has been filed for the reissue of U.S. Patent No. 6,643,777. The reissue applications are U.S. Application Nos. 11/056,604(a parent reissue case application), 11/545,056 (which is a reissue continuation of the parent reissue application), 12/561,138 (which is a reissue continuation of the parent reissue application), 13/294,108 (which is a reissue continuation of U.S. Application No. 12/561,138), and [[/ ,]] 13/562,210 (the present application, which is a reissue continuation of U.S. Application No. 13/294,108).

This application is a reissue continuation of U.S. Application No. 13/294,108, which is a reissue continuation of U.S. Application No. 12/561,138, which is a reissue continuation of U.S. Application No. 11/056,604, which is reissue of U.S. Patent No. 6,643,777, which are incorporated herein by reference.

USPTO Contact Information

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Hosuk Song whose telephone number is (571)272-3857. The examiner can normally be reached on mon-fri.

Art Unit: 2435

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Joseph Hirl can be reached on 5712723685. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/Hosuk Song/
Primary Examiner, Art Unit 2435

Change(s) applied

to document,

/M.X.H./

6/13/2013

IN THE SPECIFICATION:

after the title

Please add the following new paragraphs beginning ~~at col. 1, line 6:~~

Notice: More than one reissue application has been filed for the reissue of U.S. Patent No. 6,643,777. The reissue applications are U.S. Application Nos. 11/056,604 (a parent reissue application), 11/545,056 (which is a reissue continuation of the parent reissue application), 12/561,138 (which is a reissue continuation of the parent reissue application), 13/294,108 (which is a reissue continuation of U.S. Application No. 12/561,138), and / , (the present application, which is a reissue continuation of U.S. Application No. 13/294,108).

This application is a reissue continuation of U.S. Application No. 13/294,108, which is a reissue continuation of U.S. Application No. 12/561,138, which is a reissue continuation of U.S. Application No. 11/056,604, which is a reissue of U.S. Patent No. 6,643,777, which are incorporated herein by reference.

Please add the following new paragraphs beginning at col. 4, line 51:

FIG. 9 depicts a peripheral console configuration.

FIG. 10 is a block diagram of one embodiment of a computer system employing the present invention.

FIG. 11 is a block diagram of an attached computing module (ACM).

FIG. 12 is a block diagram of a peripheral console (PCON).

FIG. 13 is a block diagram of one embodiment of a computer system using the interface of the present invention.

FIG. 14 is a detailed block diagram of one embodiment of the host interface controller of the present invention.

FIG. 15 is a detailed block diagram of one embodiment of the PIC of the present invention.

FIG. 16 is a schematic diagram of the signal lines PCK, PD0 to PD3, and PCN.

FIG. 17 is a partial block diagram of a computer system using the interface of the present invention as a bridge between the north and south bridges of the computer system.

FIG. 18 is a partial block diagram of a computer system in which the north and south bridges are integrated with the host and peripheral interface controllers, respectively.



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APPLICATION NO.	ISSUE DATE	PATENT NO.	ATTORNEY DOCKET NO.	CONFIRMATION NO.
13/562,210	08/27/2013	RE44468	ACQI-006/05US 310578-2072	1045

58249 7590 08/07/2013
COOLEY LLP
ATTN: Patent Group
1299 Pennsylvania Avenue, NW
Suite 700
Washington, DC 20004

ISSUE NOTIFICATION

The projected patent number and issue date are specified above.

Determination of Patent Term Extension or Adjustment under 35 U.S.C. 154 (b)

A reissue patent is for "the unexpired part of the term of the original patent." See 35 U.S.C. 251. Accordingly, the above-identified reissue application is not eligible for Patent Term Extension or Adjustment under 35 U.S.C. 154(b).

Any questions regarding the Patent Term Extension or Adjustment determination should be directed to the Office of Patent Legal Administration at (571)-272-7702. Questions relating to issue and publication fee payments should be directed to the Application Assistance Unit (AAU) of the Office of Data Management (ODM) at (571)-272-4200.

APPLICANT(s) (Please see PAIR WEB site <http://pair.uspto.gov> for additional applicants):

William W. Y. Chu, Los Altos, CA;

The United States represents the largest, most dynamic marketplace in the world and is an unparalleled location for business investment, innovation, and commercialization of new technologies. The USA offers tremendous resources and advantages for those who invest and manufacture goods here. Through SelectUSA, our nation works to encourage and facilitate business investment. To learn more about why the USA is the best country in the world to develop technology, manufacture products, and grow your business, visit SelectUSA.gov.