

**UNITED STATES DISTRICT COURT  
FOR THE WESTERN DISTRICT OF TEXAS  
WACO DIVISION**

ACQIS, LLC

Plaintiff,

v.

MITAC COMPUTING TECHNOLOGY  
CORPORATION and MITAC  
HOLDINGS CORPORATION,

Defendants,

ASUSTEK COMPUTER, INC.,

Defendant,

INVENTEC CORPORATION,

Defendant,

LENOVO GROUP LTD. et al.,

Defendants,

WIWYNN CORPORATION,

Defendant.

Civil Action No.

The Honorable Alan Albright

Civil Action No.: 6:20-cv-962-ADA

Civil Action No.: 6:20-cv-965-ADA

Civil Action No.: 6:20-cv-966-ADA

Civil Action No.: 6:20-cv-967-ADA

Civil Action No.: 6:20-cv-968-ADA

**DEFENDANTS' PRELIMINARY INVALIDITY CONTENTIONS**

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## I. EXHIBIT LIST

EXHIBIT #	Description
EXHIBIT A	9,529,768 Exemplary Prior Art Charts
EXHIBIT B	9,703,750 Exemplary Prior Art Charts
EXHIBIT C	RE44,654 Exemplary Prior Art Charts
EXHIBIT D	8,977,797 Exemplary Prior Art Charts
EXHIBIT E	7,676,624 Exemplary Prior Art Charts
EXHIBIT F	8,041,873 Exemplary Prior Art Charts
EXHIBIT G	RE46,947 Exemplary Prior Art Charts
EXHIBIT H	RE44,468 Exemplary Charts
EXHIBIT I	8,626,977 Exemplary Prior Art Charts
EXHIBIT J	8,756,359 Exemplary Prior Art Charts
EXHIBIT K	RE44,739 Exemplary Prior Art Charts
EXHIBIT L	RE45,140 Exemplary Prior Art Charts
EXHIBIT M	9,529,769 Exemplary Prior Art Charts
EXHIBIT O	RE43,602 Exemplary Prior Art Charts
EXHIBIT P	RE42,984 Exemplary Prior Art Charts
EXHIBIT Q	IPR Petitions (the “IPR Charts”)

## II. INTRODUCTION

Pursuant to the Court’s Order Governing Proceedings – Patent Case, dated June 24, 2021 (hereinafter, “OGP”), Defendants ASUSTek Computer, Inc. (“ASUSTek”), Inventec Corporation (“Inventec”), Lenovo Group Ltd. et al. (collectively “Lenovo”), MiTAC Computing Technology Corporation (“MiTAC”), and Wiwynn Corporation (“Wiwynn”), (collectively “Defendants”) hereby provide their Preliminary Invalidity Contentions (the “Invalidity Contentions”) to Plaintiff ACQIS, LLC (“Plaintiff” or “ACQIS”).<sup>1</sup>

### **A. Reservation of Rights Due to Plaintiff’s Incomplete Document Production, Lack of Discovery, and Plaintiff’s Deficient Infringement Contentions**

Defendants’ Invalidity Contentions reflect Defendants’ current knowledge, thinking, and contentions in the present action, based upon the knowledge, information and/or belief presently available to Defendants. Discovery in this case has not yet commenced. Defendants also have not had the opportunity to conduct third party discovery relating to various third party product prior art and expressly reserve the right to amend these contentions subject to third party discovery. These third parties may include, without limitation, the authors, inventors, or assignees of the prior art publications identified in these contentions.

Defendants also reserve the right to amend the contentions due to Plaintiff’s lack of production in compliance with the local rules, and its confusing, inconsistent, and incomplete infringement contentions. For example, Plaintiff has not produced most of the prior art known to it, including all prior art identified by other Defendants or accused infringers against the Asserted Patents or their related patents. Further, Plaintiff has not produced any non-publicly available

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<sup>1</sup> Defendants submit their respective Preliminary Invalidity Contentions as a single consolidated document for the convenience of all parties. Statements made herein regarding patents and/or claims not asserted against certain defendants shall not be attributed to those defendants.

invalidity contentions or charts that Plaintiff has in its possession from other parties or alleged infringers, which demonstrate the alleged invalidity of any Asserted Patent or related patent.

Plaintiff also has not complied with the OGP and timely provided the complete file histories of the Asserted Patents, including providing the non-patent literature identified on the face of the Patents and included in the prosecution histories. In fact, on Saturday, June 26, 2021 Plaintiff produced 42GB of data, consisting of the “true and correct copies” of certain complete file histories, which should have been produced with Plaintiff’s Preliminary Infringement Contentions, served May 17, 2021 (the “Preliminary Infringement Contentions” or “Infringement Contentions”). This production includes some of the publications listed on the face of the Asserted Patents, which constitute part of the file histories. These publications were accessible to ACQIS (who filed them with the patent office), but not Defendants, as the non-patent literature filed with the USPTO are not provided to the general public. Thus, these were the only portions of the file histories that Defendants could not easily compile and gather on their own, yet this was the portion ACQIS failed to produce. Moreover, the original production was not capable of being downloaded. Consequently, at this time, Defendants have not had time to review this voluminous, belated production in a sufficient manner, but are diligently working to complete their review and will supplement and amend these disclosures in a timely manner as necessary.

Plaintiff’s Preliminary Infringement Contentions do not adequately identify any accused instrumentality with sufficient specificity or comply with the OGP governing patent proceedings in this case. The Infringement Contentions do not include “a chart setting forth where in the accused product(s) each element of the asserted claim(s) can be found” or properly identify the earliest priority date for each asserted claim. As but one example, Wiwynn advised Plaintiff of these deficiencies in numerous letters, including letters submitted on June 1, 2021 and June 4,

2021. Plaintiff only recently responded, over a month later, without revising its contentions to address any of the deficiencies. Defendants submit their Preliminary Invalidity Contentions without waiving or contradicting these positions. Defendants maintain and reiterate that Plaintiff's Infringement Contentions are deficient.

Nothing in these Preliminary Invalidity Contentions should be treated as or considered an admission that any of Defendants' accused technology meets any limitations of the Asserted Claims. Moreover, nothing in these Preliminary Invalidity Contentions should be treated as an admission regarding the interpretation of any claim.

Further, nothing stated herein should be treated as or considered an admission or suggestion that Defendants agree with Plaintiff regarding the scope, validity and/or enforceability of any of the Asserted Claims or the claim constructions advanced directly or implicitly by Plaintiff in its Infringement Contentions. These Preliminary Invalidity Contentions are based on Defendants current understanding of ACQIS's positions concerning the scope and construction of the claims of the asserted patents, and is not, and should in no way be seen as, an adoption or admission of any particular claim scope or construction for any term or limitation. Plaintiff's Infringement Contentions contradict the teachings of the Asserted Patents, contradict the understanding of the claim terms by a person of ordinary skill, and are vague and conclusory concerning how the claim limitations supposedly read on the accused products. The Infringement Contentions further fail to chart or identify where in the accused products numerous claim limitations are supposedly met.

Nonetheless, Defendants have based their Preliminary Invalidity Contentions, at least in part, on Defendants' current understanding and interpretation of Plaintiff's Infringement Contentions. As noted above, Defendants disagree with Plaintiff's interpretation or meaning of

various terms and phrases, but Defendants rely on Plaintiff's (deficient) contentions as a basis for forming these invalidity disclosures, because "that which infringes if later, anticipates if earlier." *Peters v. Active Mfg. Co.*, 129 U.S. 530, 537 (1889). Thus, Defendants reserve the right to supplement or amend their contentions, if ACQIS (1) provides any information that it failed to provide in its Infringement Contentions or otherwise clarifies its infringement position with respect to the Asserted Claims; (2) amends or alters its infringement contentions in any way; or (3) attempts to rely upon any information at trial, in a hearing, or during a deposition that it failed to provide in its Infringement Contentions. Defendants specifically anticipate that, when or if, ACQIS actually amends its contentions in an attempt to show how the accused products allegedly include the limitations of the claims (and not just the claim limitations ACQIS selectively chose to chart), that belated amendment/disclosure will require amending or supplementing the Preliminary Invalidity Contentions as well.

Further, claim constructions by the Court may significantly affect the scope of the Asserted Claims. Additionally, any ruling by this Court in this or any related proceeding, another District Court, and/or the Federal Circuit involving the Asserted Patents or related patents will likely affect Defendants' Preliminary Invalidity Contentions as well. Further, claim construction positions taken by ACQIS and/or other parties in other lawsuits or IPRs involving the Asserted Patents and/or related patents (the "Related Lawsuits" and "Related IPRs"), may also affect these contentions and necessitate amendments, supplements or changes to them.<sup>2</sup>

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<sup>2</sup> As set forth in the inter partes review petitions filed by third party Intel Corporation ("Intel IPRs"), the Lenovo Defendants are real parties-in-interest and stipulate that if the Board institutes IPR on the Intel IPRs, they will not advance the same Grounds or the same references relied upon in the petition(s) instituted.

In conclusion, Defendants reserve the right to supplement, amend or change, without prejudice, the Preliminary Invalidity Contentions, including, by way of example and not limitation, based on (1) any actual or potential claim construction positions asserted by ACQIS, (2) any construction, ruling, interpretation or clarification of the meaning of claim terms by the Court, (3) any newly identified, amended, supplemented, or in any way altered infringement or validity theories or positions that ACQIS or its expert witness(es) may assert, (4) any findings as to the priority date of the asserted claims, (5) and any additional evidence, including information concerning the prior art or ACQIS’s alleged priority, conception, and reduction to practice dates for any of the Asserted Claims, which is identified or able to be reviewed, once discovery commences and/or once sufficient time allows, including any prior art or contentions from any related lawsuit or IPR, and for any other reason, in accordance with the Federal Rules of Civil Procedure, the Local Rules, the Court’s orders and other applicable rules and statutes.

## B. Asserted Patents and Asserted Claims

In its Preliminary Infringement Contentions, Plaintiff asserted the following “Asserted Patents” and “Asserted Claims”:<sup>3</sup>

Asserted Patents	Asserted Claims
9,529,768	1, 3-18, 21, 22, 30, 33-36, 39, 40
9,703,750	1, 2, 4, 5, 6, 7, 10, 11, 12, 18-21, 24-27, 29, 31, 34, 35, 37, 38, 44-50
8,977,797	7, 8, 10, 14, 16, 36, 38
8,041,873	54, 77, 97
7,676,624	6, <sup>4</sup> 11

<sup>3</sup> The ’624 Patent Family Asserted Patents are shown in green and the Reissue Asserted Patents are shown in blue.

<sup>4</sup> The Eastern District of Texas invalidated Claim 6 as indefinite due to the claim language “wherein each of the computer modules is similar in design to each other.” *ACQIS v. Alcatel-Lucent USA, Inc.*, Case No. 6:13-cv-638, Summary Judgment Order (April 13, 2015). That order was not vacated, and ACQIS did not seek reconsideration of that order. Wiwynn reminded

8,756,359	1-8, 17, 19-21
8,626,977	1, 4, 6-17
9,529,769	19
RE44,654	14, 23
RE44,468	14, 21, 26, 29, 35, 37, 45
RE46,947	14, 19, 35, 48, 51, 54, 57
RE44,739	14, 18, 29-32
RE43,602	14
RE42,984	40, 52
RE45,140	14, 17, 30, 31, 35

Accordingly, Defendants have limited their Invalidity Contentions to Plaintiff's Asserted Claims from the Asserted Patents.

Each Defendant joins these Invalidity Contentions only to the extent that these contentions are applicable and relevant to any of the particular claims asserted against that Defendant. As set forth in its Infringement Contentions, ACQIS has asserted different and overlapping subsets of the Asserted Claims against each Defendants, and Defendants' service of joint Invalidity Contentions should not be construed as an acknowledgement or admission that ACQIS has, or is, asserting any claim against any Defendant that ACQIS has not specifically identified to that Defendant. If the Court allows Plaintiff to identify other patents or additional or different claims from the Asserted Patents as allegedly infringed, Defendants will supplement and amend their Invalidity Contentions to address any such new patents or claims.

### **C. The Applicable Priority Date(s)**

#### **1. Defendants' Reservation of Rights**

Nothing in the OGP requires Defendants to identify or opine on the priority date relevant to the Asserted Claims. Further, discovery into this issue is not yet admissible in this case, and

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ACQIS of this ruling in its Letter on June 4, 2021. On July 1, ACQIS finally sent a letter indicating they would drop this claim, but ACQIS has not yet amended their Contentions doing so.

Plaintiff has not sought any discovery into Defendants' contentions regarding the priority date(s) applicable to the Asserted Claims. Accordingly, Defendants reserve all rights to challenge any priority date(s) to which Plaintiffs contends the Asserted Claims may be entitled, including all priority date(s) identified by Plaintiff in this or related proceedings, including Related Lawsuits or Related IPRs.

Moreover, Plaintiff's own identification of its claimed priority date is deficient, even though Plaintiff's priority date contention *is* actually required by the Court's OGP. For every patent and claim, Plaintiff has alleged, without support, explanation or justification, that the priority date is "at least as early as" January 15, 1998 for some, but not all, Defendants. (See ACQIS Preliminary Infringement Contentions against Wiwynn, ASUS, MiTAC, and Inventec at 1-2.) However, without support, explanation or justification, Plaintiff has also alleged that the priority date for All Asserted Claims is "at least as early as July 1998." (See ACQIS Preliminary Infringement Contentions against Lenovo at 1-2.) Plaintiff's contradictory allegations regarding the priority date for the Asserted Claims are at minimum confusing and misleading, and strongly suggest that Plaintiff's contentions in this regard lack a good faith basis in law or fact. ACQIS's deficient contention is highly prejudicial to Defendants in preparing their Preliminary Invalidity Contentions because the relevant priority date is a significant factor in searching for and reviewing prior art.

Moreover, ACQIS's identification of priority dates is inconsistent with the position that it has taken with respect to the priority dates of many of the asserted claims in response to pending *inter partes review* petitions ("Samsung IPRs") filed by third party Defendant Samsung in March 2021. In ACQIS's preliminary responses to the Samsung IPRs, ACQIS changed its position on priority with respect to the '750, '768, '797, RE'654, and RE'140 patents. Rather than maintaining its January or July 1998 priority dates, for the '624 Patent Family Patents at issue in the Samsung

IPRs (i.e., the '750, '797 and '768 patents), ACQIS now appears to be asserting May 12, 2000 as the applicable priority date for most of the asserted claims:

Because every application in the priority chain of the '750 patent complied with the rules of § 1.57 and, in any event, those rules do not apply to priority applications, the '750 patent is entitled to a priority date of no later than May 12, 2000, the filing date of the '758 application. Based on this priority date, *none* of the references relied on in the Petition qualifies as prior art. The Petition should be denied.

(POPR at 4-5 (IPR2021-00604).)

Similarly, for the Reissue Patents challenged by Samsung (i.e., RE'654 and RE'140), ACQIS now appears to be asserting May 14, 1999 as the applicable priority date for most of the asserted claims:

Because every application in the priority chain of the '654 patent complied with the rules of § 1.57 and, in any event, those rules do not apply to priority applications, the '654 patent is entitled to a priority date of no later than May 14, 1999, the filing date of the '199 application. Based on this priority date, none of the references relied on in the Petition qualifies as prior art. The Petition should be denied

(POPR at 4-5 (IPR2021-00608).)

Nonetheless, in section II.C.2 below, Defendants provide a preliminary, non-binding, exemplary statement regarding the priority date(s) applicable to the Asserted Claims. Nothing stated below is an admission or acknowledgement that any claim is supported by sufficient written disclosure under 35 U.S.C. §112. As explained in Section IV.B of the Invalidity Contentions, the Asserted Claims lack written description support and are therefore invalid under §112.

## **2. Defendants' Preliminary Statement Regarding Applicable Priority Date(s)**

ACQIS is not entitled to rely on the May 14, 1999 filing date of U.S. Provisional App. 60/134,122 (the "'122 Provisional"). The '624 Patent Family Patents are all purportedly

“continuations” claiming priority to U.S. Application No. 09/569,758, filed on May 12, 2000 (the “’758 Application”). The ’758 Application incorporated by reference U.S. App. 09/149,882 (“’882 Application”) (issued as U.S. 6,345,330 (“Chu’330”)), which purports to claim priority to the ’122 Provisional, filed May 14, 1999. The ’122 Provisional is a short, 3-page “white letter paper,” that contains just 3 figures.<sup>5</sup> The ’122 Provisional purports to disclose a novel “dual computer module” configuration. (’122 Provisional at Fig. 1.) However, the Asserted Claims in this case are completely different from the supposedly novel dual computer module system in the short, 3-page disclosure of the ’122 Provisional. Nothing in the ’122 Provisional discloses the alleged combination of elements in each of the Asserted Claims. Thus, the Asserted Patents in the ’624 Patent Family Patents are not entitled to claim the benefit of the May 14, 1999 filing date of the ’122 Provisional.

Similarly, the Reissue Patents purport to claim priority back to the ultimate parent application, U.S. Appl. 09/312,199 (the “’199 Application”), filed on May 14, 1999 (and later issued as U.S. Patent No. 6,643,777 (the “’777 patent”)). The ’777 patent, titled “Data Security Method and Device for Computer Modules,” issued from the ’199 Application, which contains just eight figures. The short ’199 Application discloses a “security method for an attached computer module in a computer system.” *Id.* Abstract.

For at least the reasons discussed in the Related IPRs, the ’758 Application and the ’199 Application (“the Original Applications”) do not support the claimed inventions as a whole, as they do not disclose or support the claimed **combination** of elements of the Asserted Claims. Therefore, Asserted Patents cannot claim priority to the Original Applications. Instead, the earliest date ACQIS might be entitled to claim priority is on or around April 15, 2011, when ACQIS first

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<sup>5</sup> The ’750 patent, by contrast, contains at least 35 figures and 48 columns of condensed text.

added new matter to the '624 Patent Family Patents. In particular, on April 15, 2011, ACQIS amended the '624 Patent Family's specification for the first time to add new matter from U.S. Provisional Application No. 60/083,886 (the "'886 Provisional"). The same or similar new matter from the '886 Provisional was first added to the Reissue Patent Family specification on or around June 17, 2011. The '886 provisional was not part of the disclosure of the '758 Application or '199 Application. ACQIS may attempt to argue that the disclosure in the Asserted Patents' specification that came from the '886 Provisional in April 2011, provides written description support for the Asserted Claims. However, ACQIS amended the newly added '886 Provisional material in order to attempt to support at least the combination of elements in the Asserted Claims. Because the '886 Provisional material was essential new matter, the earliest priority the Asserted Claims would be entitled to would be April 15, 2011, when the essential, new matter was first added to any of the patent families.

To the extent ACQIS successfully argues that a claim does not require the disclosure from the '886 Provisional for written description support, that claim would still not be entitled to claim priority to the Original Application (for at least the reasons provided above). Instead, the earliest priority date that would be applicable to that claim, would be when the relevant '882 Provisional application's disclosure was first added to the patent's family chain. Relatedly, the earliest priority date applicable to the '624 Patent and '873 Patents would be March 31, 2005, for the reasons provided herein. For example, ACQIS first attempted to add new, essential material from the '882 Provisional application to the '624 Patent Family's specification on March 31, 2005. Similarly, ACQIS first purported to add new, essential material from the '882 Provisional application to the Reissue Patent Family's specification on or around Oct. 6, 2006 (and at various other subsequent

dates through Nov. 10, 2011).<sup>6</sup> The '882 application's disclosure added to the Asserted Patent's specifications by amendment, included certain, limited material related to the Asserted Claims. For example, this newly added material included the first mention of low voltage differential signals (LVDS). Thus, in the alternative, Defendants allege that Asserted Claims would at most be entitled to claim priority to the date when ACQIS first added the relevant '882 Provisional application's disclosure to the Asserted Patents' Family chain.

Because of the range of alleged priority dates applicable to the numerous Asserted Patents, including the incorrect, unsupported, and inconsistent dates identified by ACQIS in its Preliminary Infringement Contentions and in the IPRs, Defendants have been forced to search for prior art from at least 1998 until 2011. The prior art that invalidates the Asserted Patents based on this search, which has been located thus far and been subject to review, is identified below. Defendants anticipate that additional disclosures, discovery, Court rulings, and/or IPR rulings on the applicable priority date(s) would allow for narrowing the amount of art needed for review and allow for more focused searching efforts, and at least for this reason, may necessitate amending or supplementing these contentions. ACQIS's unjustified and unsupported assertions of "January 15, 1998" or "July 1998" has precluded any ability to do such focused searching at this stage.

Defendants thus reserve all rights to amend and/or supplement their Invalidity Contentions upon a finding that any of the Asserted Patents is not entitled to the priority dates claimed asserted by ACQIS. In particular, Defendants reserve all rights to amend and/or supplement its disclosures

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<sup>6</sup> The Reissue Patents first incorporated the '882 Provisional application disclosure at different dates. On Oct. 6, 2006, RE'171 was filed as a *new* reissue application chain from the '777 patent. It improperly added new material from the '882 Application. Similarly, on Sept. 16, 2009, RE'984 improperly added new material from the '882 Application. Finally, on Nov. 10, 2011, RE'602 improperly added new material from the '882 Application.

with further prior art to the extent that the Court determines a priority date subsequent to any of the dates asserted by ACQIS.

#### **D. Overview of the “State of the Art”**

The art identified in the Preliminary Invalidity Contentions reflects the common knowledge and the state of the art prior to the claimed and/or actual priority dates of the Asserted Claims. As such, the prior art references identified in the Preliminary Invalidity Contentions reflect the “state of the art” as of the alleged invention dates of the Asserted Claims. The identified references illustrate the scope and content of the prior art, the knowledge of those skilled in the relevant field, as well as the motivations of skilled persons to modify and combine known systems and components during the relevant time period. The prior art references that Defendants provide in their Invalidity Charts are thus not the only references that demonstrate each claim element. Defendants will also rely on other, non-charted, substantially similar prior art, which Defendants (and/or their experts) contend represents or exemplifies the state of the art. For example, uncharted references may be used to show that the technology field was saturated with examples of certain claim limitations (such as those discussed below), and thus that the limitation/element was well known to a POSITA prior to the applicable priority date.

Defendants anticipate that their experts will also opine on and provide the state of the art, including references known to them as experts in the field. Further, Defendants’ experts may rely upon the state of the art to base, in part, damages opinions, teaching, suggestion and/or motivation to combine various prior art references, and to support opinions and positions relating to the scope of the claims, understanding of persons of ordinary skill in the art, and Defendants’ 112 invalidity defenses.

Below, Defendants further provide a preliminary, non-binding statement regarding the State of the Art at the various applicable priority dates at issue here.

Prior to the claimed priority date and/or the actual priority dates, the elements of the Asserted Claims were well known in the art. Further, the benefits or enhancements made by using and incorporating these known elements were also well known to POSITAs. In other words, POSITAs would have known why a computer interface designer would choose one mode of communication over another--because the known benefits and tradeoffs of the various systems were well known.

For example, serial communication buses (sending one data bit at a time) have been known for over 100 years. The telegraph (for sending Morse code) is an early, exemplary serial bus system, which was originally invented in the **1800s**. Serial communication data transmission has also remained consistently popular and widely adopted by most telecommunication systems, throughout the 1900s and up to today, and it has long been the practice to interface these systems with computers and devices. An exemplary, widely adopted serial communication data transmission standard is the RS-232 standard, introduced in 1960. Serial communication buses were also known and used in personal computing devices.

The personal computer revolution that started in the early 1980s, was enhanced due to standardized bus interfaces (for example, IBM's ISA bus and the PCI bus specification).<sup>7</sup> A POSITA would have known that a benefit of standardizing the interfaces and connectors was that this allowed customization of individual computer systems through the mixing and matching of peripherals such as video devices, printers, memory, etc. Many early buses were primarily parallel bus systems.

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<sup>7</sup> The IBM ISA bus was developed in by the early 1980s. The original PCI bus specification was released in 1992. The PCI bus is also Applicant Admitted Prior Art (AAPA) in this case.

However, the parallel interfaces were usually replaced with serial interfaces (sending one bit at a time) and serialized interfaces (a small number of bits sent at a time), because of the obvious and long known benefits to a POSITA of serial systems over parallel systems. As one example, the Scalable Coherent Interface (SCI) project (IEEE P1596) was designed “to avoid the limits that are inherent in bus technology.” Gustavson, D.B., “The Scalable Coherent Interface and Related Standards Projects,” Stanford Linear Accelerator Center, Menlo Park, California, September 1991 (“Gustavson 1991”). Gustavson 1991 explained:

The SC1 link design was further refined by applying lessons learned in practical multiprocessor systems. The link signals are differential, because differential signals produce the least system ground noise and are least sensitive to noise from other sources. The links are unidirectional because bidirectional links create noise when the drivers are turned off or on to reverse the direction of the link, and because turn-around delays increase with cable length, a scalability problem. The links are fast and narrow because interface chips are expected to be pin-limited.

*Id.* at 2 (emphasis added). Further, Gustavson 1991 discusses serialized bus communications, namely SerialBus (IEEE P1394), which was a related project developing a high speed serial bus used for I/O, including in consumer products. *Id.* at 5.

Defendants further identify the following additional examples of other serial or serialized interfaces that were well-known before the claimed priority date and/or the actual priority date:

- Universal Serial Bus (USB) (originally introduced Jan. 1996),
- IEEE 1394 (and the original FireWire) (1986-1995),
- I<sup>2</sup>C Bus by Phillips Semiconductors (1982);
- Atari Serial Input/Output system (Atari SIO) (1978);
- Serial Peripheral Interface (SPI) developed by Motorola (mid 1980s);
- IEEE 802.3 (and all variations) (Ethernet) (started in 1973, standard formalized in 1983);
- SATA (Serial ATA) (presented in Aug. 2000 at the Intel Developer Forum) and SATA 1.0 (released at the end of 2000)
- PCI Express (a serialized version of the PCI standard) (at least by 2002);
- Serial Attached SCSI (SAS) bus protocol (2004)

As discussed below, the Asserted Patents specifically reference IEEE 1394 as admitted prior art. *E.g.*, U.S. Pat. No. 9,703,750 (“’750 Patent”), at col. 24:50 (“the XPBus lines may be IEEE 1394 lines”); *see also* cols. 12:14-30; 22:39-40; 24:65-25:5.

Further, before the claimed and/or actual priority date(s) of the Asserted Claims, “low-voltage differential signaling” or LVDS, was also well known in the prior art, as were the benefits of using LVDS. LVDS is a serial communication standard, and thus has the same benefits of serial over parallel systems. Further, LVDS’s other benefits were known, such as highspeed data throughput, low power use, cost efficiencies and noise control. *See* U.S. Patent No. 5,822,571 to Goodrum (“Goodrum ‘571”) at 57:31-45 (“The method of signaling is true differential which provides several advantages, with differential buffers used to send and receive signals over the cable 28. First the true differential method is less expensive than fiber optics for this short distance and less complex to interface than other serial methods. Differential signaling provides significant common mode noise immunity and common mode operating range, is available in ASICs and is faster than TTL. When using twisted pair and shielding, it minimizes electromagnetic radiation. When using low voltage swings, it minimizes power dissipation. The signaling levels chosen as a target are described in the IEEE Draft Standard for Low-Voltage Differential Signals (LVDS) for Scaleable Coherent Interface (SCI), Draft 1.10 (May 5, 1995).”)

LVDS technology and its benefits were well known before even the earliest applicable priority date at issue here. In fact, LVDS (a serial communication protocol) is an admittedly known prior art item in Asserted Patents’ file histories (including related patent file histories). For example, the Asserted Patents admit that the invention relied upon known LVDS technology. (’750 patent at 21:26-34 (“TMDS stands for Transition Minimized Differential Signaling and is a trademark of Silicon Images and refers to their Panel Link technology, which is in turn a trademark

for their LVDS technology. TMDS is used herein to refer to the Panel Link technology or technologies compatible therewith...”).) Another example of a well-known LVDS technology is the Ethernet protocol, which is a serial, LVDS protocol that was widely known and used prior to any applicable priority date at issue here. Similarly, in 1996, National Semiconductor released (as open source, freely available to the public) its well-known Flat Panel Display Link (FPD-Link) high speed digital video interface standard. FPD-Link was quickly adopted and incorporated in to the Open LVDS Display Interface Specification (OpenLVDI).

Examples of other, well-known LVDS systems, known before the alleged and/or actual applicable priority dates here, include:

- “IEEE Std 1596.3-1996, IEEE Standard for Low-Voltage Differential Signals (LVDS) for Scalable Coherent Interface (SCI)” from 1996;
- ANSI/TIA/EIA/-644 (Ethernet) (1995);
- Flat Panel Display Link (FPD-Link) (created by National Semiconductor (now TI)) (1996)
- OpenLVDI (Open LVDS Display Interface Specification (OpenLVDI) (began in 1997)
- TIA-485(-A) (March 1998);
- IEEE 802.3 (and all variations) (Ethernet) (started in 1973, standard formalized in 1983);
- Video Electronics Standards Association (VESA), Plug and Display (P&D) Standard, P&D and Digital Transition Minimized Differential Signaling (TMDS) Video Transmission Overview (1997);
- National Semiconductor’s LVDS Owner’s Manual (1997)
- TI’s LVDS Application and Data Handbook (Nov. 2002);
- TI’s LVDS Application and Data Handbook (Nov. 2008);
- TI’s “MuxIt” family of products;
- TI’s SN65LVDS151 and other serializer products;
- FPD-Link II (2006)
- FPD-Link III (known by at least 2009; formally released 2010)

The above are exemplary of well-known technology, incorporated in the Asserted Claims at issue here. Of course, other basic computer technology incorporated into the Asserted Claims here was also well known long before the alleged and/or actual priority dates, such as the use of central processor, system and main memory, power, Universal Serial Bus (USB), etc.

Defendant further identify the following products that Defendants believe were made, used and/or sold before the alleged and/or actual priority date of the Asserted Claims, and which provide further evidence of the State of the Art:

<b>Product Name</b>	<b>Manufacturer</b>
IBM S/390 Parallel Enterprise Server Generation 4	IBM
Fujitsu Granpower 6000	Fujitsu
Fujitsu Granpower 7000	Fujitsu
NEC Express 5800/ 130Pro	NEC
GS700FR	Toshiba
if Server TB Series	Oki Electric
9000V Series	Hitachi
FLORA-SS1 and FLORA-SB1	Hitachi
BeBox	Be, Inc.
SYM21002	Symbios (now part of LSI)
SYM53C876, SYM53C885,	Symbios (now part of LSI)
Alpha 21264 Microprocessor Data Sheet	Compaq Computer Corporation
Via K8T890	Via Technologies, Inc.
PCI Express Compiler	Altera
RF10-S02 Notebook	Samsung
NP400B2B-A01 Notebook, NP-RF710-S02US, NP-RF711-S01US, NPRF711-S02US	Samsung
MacBook Pro and other models	Apple
Latitude D410	Dell

Defendants anticipate discovery into these and other products from ACQIS, third parties, and/or Defendants' experts, will likely provide additional information relevant to Defendants' Invalidity Positions. In particular, Defendants anticipate that discovery may show these or other products are likely prior art that invalidate the Asserted Claims, either alone or in combination with other art. At this time, Defendants identify the above as relevant background art, but expressly reserve the right to rely on the references as invalidating prior art as discovery commences.

Further, ACQIS's own Applicant Admitted Prior Art (AAPA) confirms that the technology at issue here and its benefits, were known in the art, before the alleged date of invention. All Applicant remarks made during prosecution of any Asserted Patent and/or Related Patent (including during any post-issuance procedures, such as IPRs) are relevant to the state of the art and as potential AAPA. The file histories of all Asserted Patents and Related Patents (including post-issuance proceedings) are expressly identified and incorporated herein. Exemplary AAPA statements made by ACQIS include:

- '750 patent at 1:50-65 ("Many desktop or personal computers, which are commonly termed PCs, have been around and used for over ten years. The PCs often come with state-of-art microprocessors such as the Intel Pentium™ microprocessor chips. They also include a hard or fixed disk drive such as memory in the giga-bit range. Additionally, the PCs often include a random access memory integrated circuit device such as a dynamic random access memory device, which is commonly termed DRAM. The DRAM devices now provide up to millions of memory cells (i.e., mega-bit) on a single slice of silicon. PCs also include a high resolution display such as cathode ray tubes or CRTs. In most cases, the CRTs are at least 15 inches or 17 inches or 20 inches in diameter. High resolution flat panel displays are also used with PCs."); *see also*, RE'947 at 1:52-65
- *Id.* at 1:65-2:15 ("Many external or peripheral devices can be used with the PCs. Among others, these peripheral devices include mass storage devices such as a Zip™ Drive product sold by Iomega Corporation of Utah. Other storage devices include external hard drives, tape drives, and others. Additional devices include communication devices such as a modem, which can be used to link the PC to a wide area network of computers such as the Internet. Furthermore, the PC can include output devices such as a printer and other output means. Moreover, the PC can include special audio output devices such as speakers the like..."); *see also*, RE'947 at 1:6-2:16
- *Id.* at 3:44-48 (in the Background section a prior art device that has an "interface between the primary and secondary PCI buses" between a Notebook PC and a Docking System.)
- *Id.* at 3:23-4:1 ("Interfaces coupling two independent computer buses are well known in the art. A block diagram of a computer system utilizing such a prior art interface is shown in FIG. 5....")
- *Id.* at 3:1-9 ("Dual CPU systems have been available through Intel's architecture. For example, two Pentium II cartridges can be plugged into two "slot 1" card slots on a motherboard to form a Dual-processor system. The two CPU's share a common

host bus that connects to the rest of the system, e.g. main memory, hard disk drive, graphics subsystem, and others. Dual CPU systems have the advantage of increased CPU performance for the whole system. Adding a CPU cartridge requires no change in operating systems and application software.”

- *Id.* at 21:20-29; (“FIG. 12 is a table showing the symbols, signals, data rate and description of signals on the XDBus, where RTN indicates a ground (GND) reference. In the above tables, P&D stands for plug and display and is a trademark of the Video Electronics Standards Association (VESA) for the Plug and Display standard, DDC2:SCL and DDC2:SDA stand for the VESA display data channel (DDC) standard 2 clock and data signals, respectively, SV stands for super video, V33 is 3.3 volts, and V5 is 5.0 volts....”); *see also*, RE’947 at 21:54-67
- *Id.* at 21:26-34 (“TMDS stands for Transition Minimized Differential Signaling and is a trademark of Silicon Images and refers to their Panel Link technology, which is in turn a trademark for their LVDS technology. TMDS is used herein to refer to the Panel Link technology or technologies compatible therewith...”); *see also*, RE’947 at 21:54-3:4)
- *Id.* at 28:45-30 (“...IDE controllers and busses, and the PCI bus are well known and understood in the industry...”)
- *Id.* at 29:7-15 (“Power regulation circuitry 1742 receives electrical power via the electrical power conduction path 1914 of the CPU-to-PCON Interconnection 1900, conditions and distributes it to the other circuitry in the ACM using power distribution bus. Such regulation and distribution is well known and understood in the art.”)
- *Id.* at 30:40-47 (“...Similarly, grounding plate 2032 electrically couples to EMI/ESD-sensitive components, such as a microprocessor, by methods well known in the art...”)
- *Id.* at 31:35-56 (“...Main circuit board 2110 provides electrical connections for circuitry within the ACM and mounting for many of its components 1724, 1722, 17221, 1752, 1742, 1748, 1920, and 1930. The fabrication and use of such circuit boards is well known and understood in the art. Connector 2122 is also mounted on main circuit board 2110 and mates with mobile processor module 2120. Mobile processor module 2120 represents a form of packaging for a microprocessor and related components. The illustrated mobile processor module 2120 is a self-contained unit that includes a microprocessor 1712, CPU cache 1714, and CPU bridge 1746 operatively interconnected by the manufacturer. An example of one such module is the Pentium Processor with MMX Technology Mobile Module from Intel Corporation (order number 24 3515-001, September 1997). One skilled in the art recognizes that discrete microprocessor, cache, and bridge could have been employed and mounted directly to the main circuit board.”)
- *Id.* at 33:30-45 (“...Pointer interface circuitry 1822 interfaces a standard computer pointing device (not shown), such as a computer mouse attached at connector 1825,

to ISA bus 1845. Computer keyboards, pointing devices, connectors 1823. 1825. keyboard interface circuitry 1822, and pointer interface circuitry 1824 are well known in the art...”)

- *Id.* at 33:47-52 (“The power supply may be of the switching variety well known in the art that receives electrical energy from an AC source 1889, such as a wall outlet.”)
- *Id.* at 32:64-34:13 (“...Peripheral bridge 1846 couples PCI peripheral bus 1841 with peripheral busses of other formats such as ISA peripheral bus 1845 and others 1847. PCI and ISA peripheral busses are industry standards, well known and understood in the art. Other peripheral busses 1847 may include, for example, a bus compliant with the universal serial bus (USB) industry standard...”)
- *Id.* at 34:29-35 (“Some embodiments of PCON 1800 may take advantage of VLSI integrated circuits such as an 82371SB (PIIX4) integrated circuit from Intel Corporation. An 82371 SB integrated circuit includes circuitry for both the peripheral bridge 1846 and the IDE controller 1848 in a single package.”)
- *Id.* at 37:5-12 (“IDE controller 429 generally supports and provides timing signals necessary for the IDE bus. In the present embodiment, the IDE controller is embodied as a 643U2 PCI-to IDE chip from CMD Technology, for example. Other types of buses than IDE are contemplated, for example EIDE, SCSI, USB, and the like in alternative embodiments of the present invention...”)
- RE’947 at 2:59-3:9 (“One approach to reduce some of these drawbacks has been the use of a docking station with a portable computer. Here, the user has the portable computer for “on the road” use and a docking station that houses the portable computer for office use. The docking station typically includes a separate monitor, keyboard, mouse, and the like and is generally incompatible with other desktop PCs. The docking station is also generally not compatible with portable computers of other vendors. Another drawback to this approach is that the portable computer typically has lower performance and functionality than a conventional desktop PC. For example, the processor of the portable is typically much slower than processors in dedicated desktop computers, because of power consumption and heat dissipation concerns. As an example, it is noted that at the time of drafting of the present application, some top-of-the-line desktops include 400 MHz processors, whereas top-of-the-line notebook computers include 266 MHz processors...”)
- *Id.* at 2:59-3:9 (“A wide variety of removable storage media are available for a personal computer...”)
- *Id.* at 3:30-50 (“PC architecture generally allows freedom of data flow between memory and peripheral devices within the allowed memory and I/O address spaces. In conventional PC architecture, a peripheral bus, i.e. PCI bus, is used to control all data transactions among peripheral devices. PCI bus allows any device to be a bus master and perform data transaction with another device. Also when a software program is in control, it can move data between any two devices..”)

- *Id.* at 11:22-28 (“programs and the like. The hard disk can be any suitable drive that has at least 2 GB and greater. As merely an example, the hard disk is a Marathon 2250 (2.25 GB, 2 ½ inch drive) product made by Seagate Corporation of Scotts Valley, but can be others.”)
- *Id.* at 11:35-50 (“The attached computer module also has a flash memory device 505 with a BIOS. ...The flash memory can be any product such as a W29C020 product made by a company called Winbond of Taiwan, but can also be others...”)
- *Id.* at 12:4-17 (“In a specific embodiment, the peripheral console also has a serial EEPROM memory device 575, which is coupled to the peripheral interface controller. The memory device can store a security identification number or the like. The memory device is generally non-volatile and can preserve information even when the power is turned off, for example. The memory generally has at least 16 kilobits of storage cells or more. Preferably, the memory device is a 16 kilobit device or 64 megabit device or greater, depending upon the application. The memory can be any product such as a X24320 product made by a company called Xicor, but can also be others...”)
- *Id.* at 19:30-41 (“Video bus 1317 transmits video signals between the ACM 1305 and the peripheral console 1310. In a preferred embodiment, the video bus 1317 transmits analog Red Green Blue (RGB) video signals for color monitors, digital video signals (such as Video Electronics Standards Association (VESA) Plug and Display's Transition Minimized Differential Signaling (TMDS) signals for flat panel displays), and television (TV) and/or super video (S-video) signals....”)
- *Id.* at 21:31-54 (“The XPBus lines, PD0 to PD3, PCN, PDR0 to PDR3 and PCNR, and the video data and clock lines, VPD and VPCK, are not limited to being LVDS lines, as they may be other forms of bit based lines. For example, in another embodiment, the XPBus lines may be IEEE 1394 lines...However, in the case of differential signal lines, a pair of physical lines is used to transmit one signal. For example, a pair of physical lines together transmit a signal in a bit line or bit channel in an LVDS or IEEE 1394 interface...A bit based line (i.e., a bit line) is a line for transmitting serial bits. Bit based lines typically transmit bit packets and use a serial data packet protocol. Examples of bit lines include an LVDS line, an IEEE 1394 line, and a Universal Serial Bus (USB) line.”)

In addition, much of the art identified in these Invalidity Contentions reflects common knowledge and the state of the art at the time of the earliest filing date(s) of the Asserted Patents. Defendants may rely on additional citations, references, expert testimony, fact testimony and other corroborating evidence, and other material to provide context and background illustrating the knowledge of a person of ordinary skill in the art at the time of the claimed inventions and/or to

aid in understanding the cited portions of the references and/or cited features of the physical embodiments.

### **III. Invalidity Under 35 U.S.C. §102 and §103**

Below, Defendants provide their preliminary list of Identified Prior Art and their Invalidity Charts, demonstrating where, in the identified prior art, each element of the Asserted Claims is met.

Defendants' prior art investigation is just beginning, as discovery has not even commenced in this case. Plaintiff has not all produced the patents, publications or other prior art listed on the face of the Asserted Patents or related patents, nor has Plaintiff produced the majority of the prior art, invalidity contentions or positions known to it (and not presently available to the Defendants), that have been provided to Plaintiff in the Related Lawsuits or Related IPRs, or through informal discussion with potential other, alleged infringers. All such contentions and/or identification of prior art are highly relevant to this case and to these Invalidity Contentions. Moreover, Plaintiff has not shown where in the Accused Products the majority of the claim limitations are met, and therefore, Defendants' understanding as to what Plaintiff alleges the claim limitations mean cannot be evaluated.

Thus, as stated above, Defendants reserve the right to amend these Preliminary Invalidity Contentions after discovery commences, including as prior art *known to Plaintiff, but not to Defendants*, is identified and produced by Plaintiff, in this case.

#### **A. Defendants' "Identified Prior Art"**

Pursuant to the OGP, and subject to Defendants' reservation of rights, Defendants identify each item of prior art that Defendants contend anticipates each Asserted Claim and/or renders each Asserted Claim obvious, alone or in combination with one or more other prior art references. The below sections, Sections III.A.1-4 constitute Defendants' "Identified Prior Art."

## 1. Prior Art Patents and Patent Applications

Begbates	Endbates	Patent or Publication Number
PRIORART-0000033	PRIORART-0000062	U.S. Patent App. No. 60/083,886
PRIORART-0000239	PRIORART-0000261	U.S. Patent App. No. 60/083,886
PRIORART-0000408	PRIORART-0000422	U.S. Patent No. 6,088,752
PRIORART-0000604	PRIORART-0000611	U.S. Patent No. 5,815,735
PRIORART-0000707	PRIORART-0000745	U.S. Patent No. 6,216,185
PRIORART-0000746	PRIORART-0000815	U.S. Patent No. 6,345,330
PRIORART-0001143	PRIORART-0001164	U.S. Patent No. 6,425,033
PRIORART-0001205	PRIORART-0001229	U.S. Patent No. 6,611,249
PRIORART-0001236	PRIORART-0001249	U.S. Patent No. 5,608,608
PRIORART-0001264	PRIORART-0001319	U.S. Patent No. 6,742,068
PRIORART-0001342	PRIORART-0001526	U.S. Patent No. 6,101,322
PRIORART-0001527	PRIORART-0001552	U.S. Patent No. 6,148,357
PRIORART-0002537	PRIORART-0002700	U.S. Patent No. 5,729,720
PRIORART-0002701	PRIORART-0002771	U.S. Patent No. 6,223,265
PRIORART-0002772	PRIORART-0002777	U.S. Patent No. 5,948,091
PRIORART-0002778	PRIORART-0002785	U.S. Patent No. 6,324,606
PRIORART-0002786	PRIORART-0002793	U.S. Patent No. 6,324,606
PRIORART-0002965	PRIORART-0002982	U.S. Patent No. 6,606,678
PRIORART-0004181	PRIORART-0004200	U.S. Patent No. 5,986,641
PRIORART-0004201	PRIORART-0004210	U.S. Patent No. 6,051,990
PRIORART-0004260	PRIORART-0004279	U.S. Patent No. 5,986,641
PRIORART-0004280	PRIORART-0004315	U.S. Patent No. 6,600,492
PRIORART-0005257	PRIORART-0005266	U.S. Patent No. 6,901,207
PRIORART-0005277	PRIORART-0005288	U.S. Patent No. 6,161,157
PRIORART-0005289	PRIORART-0005358	U.S. Patent No. 6,345,330
PRIORART-0005359	PRIORART-0005380	U.S. Patent No. 4,486,739
PRIORART-0005381	PRIORART-0005388	U.S. Patent No. 4,670,837
PRIORART-0005389	PRIORART-0005445	U.S. Patent No. 4,750,177
PRIORART-0005446	PRIORART-0005459	U.S. Patent No. 5,062,059
PRIORART-0005460	PRIORART-0005471	U.S. Patent No. 5,068,823
PRIORART-0005472	PRIORART-0005483	U.S. Patent No. 5,227,957
PRIORART-0005484	PRIORART-0005494	U.S. Patent No. 5,335,321
PRIORART-0005495	PRIORART-0005543	U.S. Patent No. 5,355,467
PRIORART-0005544	PRIORART-0005565	U.S. Patent No. 5,408,618
PRIORART-0005566	PRIORART-0005598	U.S. Patent No. 5,428,806
PRIORART-0005599	PRIORART-0005614	U.S. Patent No. 5,452,468
PRIORART-0005615	PRIORART-0005627	U.S. Patent No. 5,481,207
PRIORART-0005628	PRIORART-0005639	U.S. Patent No. 5,588,850

PRIORART-0005640	PRIORART-0005653	U.S. Patent No. 5,604,880
PRIORART-0005654	PRIORART-0005667	U.S. Patent No. 5,608,608
PRIORART-0005668	PRIORART-0005681	U.S. Patent No. 5,608,608
PRIORART-0005682	PRIORART-0005691	U.S. Patent No. 5,649,124
PRIORART-0005692	PRIORART-0005855	U.S. Patent No. 5,729,720
PRIORART-0005856	PRIORART-0006019	U.S. Patent No. 5,729,720
PRIORART-0006020	PRIORART-0006183	U.S. Patent No. 5,729,720
PRIORART-0006184	PRIORART-0006197	U.S. Patent No. 5,737,524
PRIORART-0006198	PRIORART-0006213	U.S. Patent No. 5,742,844
PRIORART-0006214	PRIORART-0006372	U.S. Patent No. 5,754,837
PRIORART-0006373	PRIORART-0006406	U.S. Patent No. 5,764,924
PRIORART-0006407	PRIORART-0006414	U.S. Patent No. 5,815,735
PRIORART-0006415	PRIORART-0006623	U.S. Patent No. 5,822,512
PRIORART-0006624	PRIORART-0006832	U.S. Patent No. 5,822,512
PRIORART-0006833	PRIORART-0006993	U.S. Patent No. 5,822,550
PRIORART-0006994	PRIORART-0007177	U.S. Patent No. 5,822,571
PRIORART-0007178	PRIORART-0007361	U.S. Patent No. 5,822,571
PRIORART-0007362	PRIORART-0007545	U.S. Patent No. 5,822,571
PRIORART-0007546	PRIORART-0007561	U.S. Patent No. 5,857,075
PRIORART-0007562	PRIORART-0007574	U.S. Patent No. 5,862,350
PRIORART-0007575	PRIORART-0007725	U.S. Patent No. 5,867,717
PRIORART-0007726	PRIORART-0007753	U.S. Patent No. 5,933,614
PRIORART-0007754	PRIORART-0007767	U.S. Patent No. 5,941,965
PRIORART-0007768	PRIORART-0007780	U.S. Patent No. 5,941,968
PRIORART-0007781	PRIORART-0007786	U.S. Patent No. 5,948,091
PRIORART-0007787	PRIORART-0007792	U.S. Patent No. 5,948,091
PRIORART-0007793	PRIORART-0007798	U.S. Patent No. 5,948,091
PRIORART-0007799	PRIORART-0007810	U.S. Patent No. 5,953,206
PRIORART-0007811	PRIORART-0007852	U.S. Patent No. 5,961,623
PRIORART-0007853	PRIORART-0007859	U.S. Patent No. 5,965,957
PRIORART-0007860	PRIORART-0007882	U.S. Patent No. 5,977,796
PRIORART-0007883	PRIORART-0007902	U.S. Patent No. 5,986,641
PRIORART-0007903	PRIORART-0007922	U.S. Patent No. 5,986,641
PRIORART-0007923	PRIORART-0007979	U.S. Patent No. 5,987,590
PRIORART-0007980	PRIORART-0008036	U.S. Patent No. 5,987,590
PRIORART-0008037	PRIORART-0008044	U.S. Patent No. 6,003,105
PRIORART-0008045	PRIORART-0008054	U.S. Patent No. 6,012,145
PRIORART-0008055	PRIORART-0008432	U.S. Patent No. 6,023,587
PRIORART-0008433	PRIORART-0008617	U.S. Patent No. 6,035,362
PRIORART-0008618	PRIORART-0008628	U.S. Patent No. 6,041,372

PRIORART-0008629	PRIORART-0008639	U.S. Patent No. 6,041,372
PRIORART-0008640	PRIORART-0008650	U.S. Patent No. 6,041,372
PRIORART-0008651	PRIORART-0008660	U.S. Patent No. 6,051,990
PRIORART-0008661	PRIORART-0008677	U.S. Patent No. 6,057,862
PRIORART-0008678	PRIORART-0008708	U.S. Patent No. 6,058,443
PRIORART-0008709	PRIORART-0008722	U.S. Patent No. 6,081,143
PRIORART-0008723	PRIORART-0008737	U.S. Patent No. 6,088,752
PRIORART-0008738	PRIORART-0008794	U.S. Patent No. 6,091,705
PRIORART-0008795	PRIORART-0008979	U.S. Patent No. 6,101,322
PRIORART-0008980	PRIORART-0009167	U.S. Patent No. 6,105,119
PRIORART-0009168	PRIORART-0009175	U.S. Patent No. 6,125,414
PRIORART-0009176	PRIORART-0009201	U.S. Patent No. 6,148,357
PRIORART-0009202	PRIORART-0009267	U.S. Patent No. 6,154,772
PRIORART-0009268	PRIORART-0009279	U.S. Patent No. 6,161,157
PRIORART-0009280	PRIORART-0009291	U.S. Patent No. 6,161,157
PRIORART-0009292	PRIORART-0009318	U.S. Patent No. 6,170,025
PRIORART-0009319	PRIORART-0009345	U.S. Patent No. 6,170,025
PRIORART-0009346	PRIORART-0009372	U.S. Patent No. 6,170,025
PRIORART-0009373	PRIORART-0009411	U.S. Patent No. 6,216,185
PRIORART-0009412	PRIORART-0009450	U.S. Patent No. 6,216,185
PRIORART-0009451	PRIORART-0009537	U.S. Patent No. 6,226,723
PRIORART-0009538	PRIORART-0009595	U.S. Patent No. 6,247,084
PRIORART-0009596	PRIORART-0009653	U.S. Patent No. 6,247,084
PRIORART-0009654	PRIORART-0009711	U.S. Patent No. 6,247,084
PRIORART-0009712	PRIORART-0009730	U.S. Patent No. 6,314,479
PRIORART-0009731	PRIORART-0009749	U.S. Patent No. 6,314,479
PRIORART-0009758	PRIORART-0009827	U.S. Patent No. 6,345,330
PRIORART-0009828	PRIORART-0009896	U.S. Patent No. 6,389,029
PRIORART-0009897	PRIORART-0009965	U.S. Patent No. 6,389,029
PRIORART-0009966	PRIORART-0010034	U.S. Patent No. 6,389,029
PRIORART-0010035	PRIORART-0010056	U.S. Patent No. 6,425,033
PRIORART-0010057	PRIORART-0010123	U.S. Patent No. 6,434,562
PRIORART-0010124	PRIORART-0010145	U.S. Patent No. 6,434,654
PRIORART-0010146	PRIORART-0010154	U.S. Patent No. 6,490,686
PRIORART-0010155	PRIORART-0010163	U.S. Patent No. 6,490,686
PRIORART-0010164	PRIORART-0010190	U.S. Patent No. 6,496,895
PRIORART-0010191	PRIORART-0010200	U.S. Patent No. 6,557,065
PRIORART-0010201	PRIORART-0010218	U.S. Patent No. 6,567,876
PRIORART-0010219	PRIORART-0010254	U.S. Patent No. 6,600,492
PRIORART-0010255	PRIORART-0010290	U.S. Patent No. 6,600,492

PRIORART-0010291	PRIORART-0010301	U.S. Patent No. 6,600,747
PRIORART-0010302	PRIORART-0010312	U.S. Patent No. 6,600,747
PRIORART-0010313	PRIORART-0010323	U.S. Patent No. 6,600,747
PRIORART-0010324	PRIORART-0010389	U.S. Patent No. 6,636,922
PRIORART-0010390	PRIORART-0010405	U.S. Patent No. 6,643,777
PRIORART-0010406	PRIORART-0010420	U.S. Patent No. 6,665,020
PRIORART-0010421	PRIORART-0010435	U.S. Patent No. 6,665,020
PRIORART-0010436	PRIORART-0010494	U.S. Patent No. 6,690,676
PRIORART-0010495	PRIORART-0010553	U.S. Patent No. 6,690,676
PRIORART-0010554	PRIORART-0010612	U.S. Patent No. 6,690,676
PRIORART-0010613	PRIORART-0010626	U.S. Patent No. 6,718,415
PRIORART-0010627	PRIORART-0010640	U.S. Patent No. 6,718,415
PRIORART-0010641	PRIORART-0010696	U.S. Patent No. 6,742,068
PRIORART-0010697	PRIORART-0010706	U.S. Patent No. 6,801,207
PRIORART-0010707	PRIORART-0010716	U.S. Patent No. 7,146,506
PRIORART-0010717	PRIORART-0010739	U.S. Patent No. 7,146,510
PRIORART-0010740	PRIORART-0010755	U.S. Patent No. 8,253,750
PRIORART-0010756	PRIORART-0010771	U.S. Patent No. 8,253,750
PRIORART-0010772	PRIORART-0010817	U.S. Patent Pub. No. 2003/0135771
PRIORART-0010818	PRIORART-0010863	U.S. Patent Pub. No. 2003/0135771
PRIORART-0011132	PRIORART-0011165	U.S. Patent No. Re. 36,381
PRIORART-0012787	PRIORART-0012796	U.S. Patent No. 5,594,882
PRIORART-0012797	PRIORART-0012829	U.S. Patent No. 5,727,211
PRIORART-0012830	PRIORART-0012861	U.S. Patent No. 5,760,637
PRIORART-0012862	PRIORART-0012869	U.S. Patent No. 6,003,105
PRIORART-0012870	PRIORART-0012881	U.S. Patent No. 6,070,207
PRIORART-0012882	PRIORART-0012896	U.S. Patent No. 6,070,214
PRIORART-0012897	PRIORART-0012917	U.S. Patent No. 6,516,375
PRIORART-0012918	PRIORART-0012930	U.S. Patent No. 7,657,678
PRIORART-0009750	PRIORART-0009757	U.S. Patent No. 6,324,606

Any physical embodiments of the references described in the above Identified Prior Art, which physical embodiments were publicly available (e.g. used, offered for sale, or sold) before the claimed or actual priority dates of the Asserted Patents, also constitute prior art. Defendants are not limited to the patent or application identified above, but also rely on material that expressly identifies any physical embodiment of such patent or application as applicable prior art.

## 2. Prior Art Publications, Public Uses, Public Offers for Sale/Sales:

Begbates	Endbates	Title
PRIORART-0000001	PRIORART-0000008	ServerNet SAN I/O Architecture
PRIORART-0000009	PRIORART-0000032	ServerNet-II: a Reliable Interconnect for Scalable High Performance Cluster Computing
PRIORART-0000063	PRIORART-0000091	Application of the Scalable Coherent Interface to Data Acquisition at LHC
PRIORART-0000092	PRIORART-0000106	Architecture and Implementation of Memory Channel 2
PRIORART-0000107	PRIORART-0000131	HyperTransport Technology I/O Link ("HyperTransport White Paper (#25012A)")
PRIORART-0000132	PRIORART-0000138	Parallel Fiber-Optic SCI Links
PRIORART-0000139	PRIORART-0000142	CMOS VLSI Implementation of Gigabyte/Second Computer Network Links
PRIORART-0000143	PRIORART-0000149	Interface Issues in Displaying Graphics and Video on High Resolution Flat Panel Displays
PRIORART-0000150	PRIORART-0000238	Tao: An Architecturally Balanced Reconfigurable Hardware Processor
PRIORART-0000262	PRIORART-0000370	A Data Servicing Subsystem for the Chidi Reconfigurable Processor
PRIORART-0000371	PRIORART-0000407	A Comparison of Three Gigabit Technologies: SCI, Myrinet and SGI/Cray T3D
PRIORART-0000423	PRIORART-0000580	Alpha 21264 Microprocessor Data Sheet
PRIORART-0000581	PRIORART-0000582	PCI Express Compiler
PRIORART-0000583	PRIORART-0000589	Microprocessor Report - K7 Challenges Intel
PRIORART-0000590	PRIORART-0000597	Channel Link Moving and Shaping Information In Point-To-Point Applications
PRIORART-0000598	PRIORART-0000599	Apple Thunderbolt
PRIORART-0000600	PRIORART-0000603	VLSI: High Density Initiative deep submicron ASIC cell libraries feature hand-crafted layouts
PRIORART-0000612	PRIORART-0000640	Application of the Scalable Coherent Interface to Data Acquisition at LHC
PRIORART-0000641	PRIORART-0000669	Application of the Scalable Coherent Interface to Data Acquisition at LHC
PRIORART-0000670	PRIORART-0000687	An Introduction to PCI Express
PRIORART-0000688	PRIORART-0000706	SCI Implementation Study for LHCb Data Acquisition
PRIORART-0000816	PRIORART-0001142	Universal Serial Bus Specification, Revision 1.1
PRIORART-0001165	PRIORART-0001168	The VESA Digital Flat Panel (DFP) Standard, A White Paper

PRIORART-0001169	PRIORART-0001204	The Design and Performance Evaluation of the DI-multicomputer
PRIORART-0001230	PRIORART-0001235	EveryMac.Com Apple MacBook Pro 13-Inch "Core i5" 2.3 Early 2011 Specs
PRIORART-0001250	PRIORART-0001255	GranPower 5000 - High-Performance Technology
PRIORART-0001256	PRIORART-0001258	GranPower 5000 - High-Reliability Technology of Electro-Mechanical Design
PRIORART-0001259	PRIORART-0001263	Fujitsu Granpower 5000 Model 670
PRIORART-0001320	PRIORART-0001341	Gigabit Media Independent Interface Proposal
PRIORART-0001553	PRIORART-0001690	The IEEE 1355 Standard
PRIORART-0001691	PRIORART-0001699	Tnet: A reliable System Area Network
PRIORART-0001700	PRIORART-0001723	HyperTransport Consortium White Paper HTC_WP04
PRIORART-0001724	PRIORART-0001745	HyperTransport Technology: Simplifying System Design ("HyperTransport System Design")
PRIORART-0001746	PRIORART-0001771	HyperTransport Consortium Applications Overview White Paper
PRIORART-0001772	PRIORART-0002101	HyperTransport I/O Link Specification Revision 1.10
PRIORART-0002102	PRIORART-0002114	HyperTransport Technology and InfiniBand Architecture ("HyperTransport Infiniband White Paper")
PRIORART-0002115	PRIORART-0002124	Altera HyperTransport Technology
PRIORART-0002125	PRIORART-0002354	HyperTransport I/O Link Specification Revision 1.04 ("HyperTransport Link Specification 1.04")
PRIORART-0002355	PRIORART-0002373	HyperTransport Technology Overview & Consortium Announcement ("Sartori, HyperTransport Overview")
PRIORART-0002374	PRIORART-0002415	Draft Standards for Low-Voltage Differential Signals (LVDS) for Scalable Coherent Interface (SCI) 1.3
PRIORART-0002416	PRIORART-0002421	PCI Express Ethernet Networking
PRIORART-0002422	PRIORART-0002495	Intel 430HX PCIset Design Guide
PRIORART-0002496	PRIORART-0002496	Intel Core i5-2540M Processor
PRIORART-0002497	PRIORART-0002497	Notebook Check Intel Core i5-2540M
PRIORART-0002498	PRIORART-0002498	Intel Core i7-2620M Processor
PRIORART-0002499	PRIORART-0002499	WikiChip Core i7-2620M - Intel
PRIORART-0002500	PRIORART-0002502	Intel Core i5-2410M Processor
PRIORART-0002503	PRIORART-0002536	Variable Structure Modelling Methodology: An Adaptive Computer Architecture Example
PRIORART-0002794	PRIORART-0002795	Lenovo - ThinkPad W510 Page

PRIORART-0002796	PRIORART-0002803	Living With A Sandy Bridge Notebook: Lenovo's ThinkPad X220
PRIORART-0002804	PRIORART-0002832	Application of the Scalable Coherent Interface to Data Acquisition at LHC
PRIORART-0002833	PRIORART-0002898	National Semiconductor LVDS Owner's Manual & Design Guide
PRIORART-0002899	PRIORART-0002902	MacBook Pro Features Page
PRIORART-0002903	PRIORART-0002905	MacBook Pro Performance Page
PRIORART-0002906	PRIORART-0002908	MacBook Pro Specifications Page
PRIORART-0002909	PRIORART-0002917	PCI Express and Advanced Switching: Evolutionary Path to Building Next Generation Interconnects
PRIORART-0002918	PRIORART-0002924	Media Processing with Field-Programmable Gate Arrays on a Microprocessor's Local Bus
PRIORART-0002925	PRIORART-0002931	Memory Channel Network for PCI
PRIORART-0002932	PRIORART-0002963	Mitsubishi Electric Advance - Programmable Logic Controllers Edition
PRIORART-0002964	PRIORART-0002964	Mobile Intel QM67 Express Chipset
PRIORART-0002983	PRIORART-0002987	IBM Netfinity 7000 Sets Performance Record for SAP's R/3 SD Benchmark on 4-Way Intel-Based Systems
PRIORART-0002988	PRIORART-0003032	Open LVDS Display Interface (OpenLDI) Specification v0.95
PRIORART-0003033	PRIORART-0003052	OverClockers Intel i7 2600k (Sandy Bridge) Review
PRIORART-0003053	PRIORART-0003274	PCI Express System Architecture
PRIORART-0003275	PRIORART-0003596	PCI Local Bus Specification
PRIORART-0003597	PRIORART-0004104	PCI Express Base Specification Revision 1.1
PRIORART-0004105	PRIORART-0004106	National Semiconductor: National announces first LVDS devices for host-to-LCD interfacing
PRIORART-0004107	PRIORART-0004111	Chips: Vitesse extends high-performance ASIC line with low-power Standard Cell Family
PRIORART-0004112	PRIORART-0004114	Plug and Display hits the ground running
PRIORART-0004115	PRIORART-0004119	National targets PC arena
PRIORART-0004120	PRIORART-0004122	Low-voltage differential-signaling Ics provide speed impedance match
PRIORART-0004123	PRIORART-0004124	Disk subsystems at center stage
PRIORART-0004125	PRIORART-0004164	QR0001 QuickRing Data Stream Controller
PRIORART-0004165	PRIORART-0004174	The RACE Network Architecture
PRIORART-0004175	PRIORART-0004177	National Semiconductor: National announces first LVDS devices for host-to-LCD interfacing
PRIORART-0004178	PRIORART-0004180	National targets PC arena

PRIORART-0004211	PRIORART-0004238	Intel i7 2600K (Sandy Bridge) Review
PRIORART-0004239	PRIORART-0004239	WikiChip Sandy Bridge (Client) - Microarchitectures - Intel
PRIORART-0004240	PRIORART-0004241	Sandy Bridge Architecture - Real World Technologies
PRIORART-0004242	PRIORART-0004251	Sepia: scalable 3D composition using PCI Pamette
PRIORART-0004252	PRIORART-0004259	ServerNet SAN I/O Architecture
PRIORART-0004316	PRIORART-0004390	Texas Instruments - Comparing Bus Solutions (SLLA067C)
PRIORART-0004391	PRIORART-0004419	LDI Demonstration Kit User Guide (LVDS Display Interface)
PRIORART-0004420	PRIORART-0004423	LVDS SCI Bus Expander (SYM53CI4I)
PRIORART-0004424	PRIORART-0004427	PCI to Ultra2 SCSI I/O Processor (SYM53895)
PRIORART-0004428	PRIORART-0004495	SCSI Bus Expander (Symbios SYM53C141)
PRIORART-0004496	PRIORART-0004501	PCI-to-Ultra2 SCSI Host Adapter (Symbios SYM895iU DataSheet)
PRIORART-0004502	PRIORART-0004504	ThinkPad Laptop Webpage
PRIORART-0004505	PRIORART-0004507	ThinkPad W Series Webpage
PRIORART-0004508	PRIORART-0004521	ThinkPad W510 - Computerworld Article
PRIORART-0004522	PRIORART-0004525	ThinkPad W510 Datasheet
PRIORART-0004526	PRIORART-0004526	ThinkPad W510 Specifications - CNET
PRIORART-0004527	PRIORART-0004528	ThinkPad W510 Webpage
PRIORART-0004529	PRIORART-0004531	ThinkPad W701 - Mobile Venue Article
PRIORART-0004532	PRIORART-0005240	ThinkPad Withdrawn Books Specifications
PRIORART-0005241	PRIORART-0005243	Thinkpad X Series Webpage
PRIORART-0005244	PRIORART-0005246	ThinkPad X220 - CNET Review
PRIORART-0005247	PRIORART-0005247	ThinkPad X220 - Detailed Specifications
PRIORART-0005248	PRIORART-0005251	ThinkPad X220 Datasheet
PRIORART-0005252	PRIORART-0005256	Thinkpad X220 Webpage
PRIORART-0005267	PRIORART-0005276	Tnet: A Reliable System Area Network
PRIORART-0010864	PRIORART-0011131	Universal Serial Bus Specification Rev. 1.0
PRIORART-0011166	PRIORART-0011274	VESA Plug and Display Standard Version 1
PRIORART-0011275	PRIORART-0011418	VTA PT880 Pro North Bridge Data Sheet
PRIORART-0011419	PRIORART-0011445	Sandy Bridge - Wiki Chip
PRIORART-0011446	PRIORART-0011458	Wikipedia Macintosh models
PRIORART-0011459	PRIORART-0011459	Withdrawn Product Specifications
PRIORART-0011460	PRIORART-0011749	2nd Generation Intel Core Processor Family Mobile Datasheet
PRIORART-0011750	PRIORART-0012008	Accelerated Graphics Port Interface Specification
PRIORART-0012009	PRIORART-0012010	Altera PCI Express Compiler

PRIORART-0012011	PRIORART-0012016	Granpower 6000 Hardware of Granpower 6000 Series
PRIORART-0012017	PRIORART-0012022	Granpower 7000 High-Reliability Technology for GRANPOWER 7000 Series
PRIORART-0012023	PRIORART-0012332	Future I/O Specification
PRIORART-0012333	PRIORART-0012340	The Scalable Coherent Interface and Related Standards Projects
PRIORART-0012341	PRIORART-0012442	Intel CA810 Motherboard
PRIORART-0012443	PRIORART-0012489	VIA K8T890 Data Sheet
PRIORART-0012490	PRIORART-0012697	An Efficient Runtime System Combining Dataflow, Multithreading, and Distributed Shared Memory
PRIORART-0012698	PRIORART-0012752	PanelLink Technology Version 0.40 ("PanelLink")
PRIORART-0012753	PRIORART-0012781	LDI Demonstration Kit User Guide (LVDS Display Interface) ("LDI User Guide")
PRIORART-0012782	PRIORART-0012786	SCSI Product Offerings
PRIORART-0012931	PRIORART-0013580	Universal Serial Bus Specification, Revision 2.0
PRIORART-0013581	PRIORART-0013640	VESA Flat Panel Display Interface -2 Standard ("VESA FPD-2")
PRIORART-0013641	PRIORART-0013672	Application of the Scalable Coherent Interface to Data Acquisition ("Bogaerts 1995")
PRIORART-0013673	PRIORART-0013678	Lenovo Unveils Sandy Bridge ThinkPads

<b>Prior Art Systems:</b>
ThinkPad X220/X220i
ThinkPad T420s
ThinkPad W510/W520
ThinkPad W701/W701ds
AMD HyperTransport
Memory Channel for PCI
Memory Channel 2
Linc Controller LC-2
AMD K7 System
Alpha 21264 Microprocessor Data Sheet
Cray T3D Massively Parallel Processor (MPP)
RACE Parallel Computer System
QuickRing Interconnect
Chidi Processing System, Chidi Reconfigurable Processor
ServerNet S4000 and S7000 (previously TNet)
Via PT880
SYM895IU
SYM53C141

SYM53C895
Fujitsu Granpower 5000
430HX PCIset
Netfinity 7000 System
Mitsubishi Apricot FT8000 Server
CERN LHCb DAQ Systems

ACQIS has also accused various central processing units and chipsets from Defendants' Accused Products of infringing the Asserted Claims. Some of these CPUs and chipsets were available before April 2011, and therefore, to the extent ACQIS can show the product infringes, the product would also constitute prior art.

Any physical embodiments of the references described in the above Identified Prior Art, which physical embodiments were publicly available (e.g. made, used, offered for sale, or sold) before the claimed or actual priority dates of the Asserted Patents, also constitute prior art. Defendants are not limited to the references identified above, but also rely on material that expressly identifies any physical embodiment of such reference as prior art.

Any citation to one or more of these prior art references/documents, should be construed to constitute not only a citation to the prior art reference/document itself (as a printed publication), but also a reference to the product or system itself. When a reference is a prior public use, offer for sale, or sale, the identified document(s) is being relied upon as exemplary evidence of the prior public use, sale, and/or offer for sale. For the prior art products or systems (e.g. prior public uses, offers for sale and/or sales), Defendants anticipate relying on additional documents to demonstrate the products / system, testimony relating to the products / systems, and other information.

To the extent the prior art being relied upon includes a prior art product/system, Defendants reserve the right to rely on, as invalidating prior art under 35 U.S.C. §§ 102 and/or 103, the product/system itself (including physical embodiments), any literature describing the

product/system as printed publications, and/or any combinations thereof. It would have been obvious to combine any publications describing the product/system with any other such publications, and/or the product/system itself, since such documentation is directed to the same underlying subject matter of the prior art product/system.

Further, Defendants' investigation has just begun, as discovery in this case has not yet commenced. In the course of discovery, Defendants anticipate identifying additional prior art documents describing these prior art public use, offer for sale, and sale and other prior public use, offer for sale, or sale, not presently known or identified as prior art. Further, Defendants anticipate discovery from ACQIS, third parties, and/or Defendants' experts, will likely identify additional product prior art systems. Defendants will amend their contentions as such discovery becomes available.

In addition, Defendants contend that the Identified Prior Art provides evidence of prior invention and making of the invention in the United States by another under 35 U.S.C. § 102(f) and/or (g), as evidenced by the named inventor(s), author(s), organization(s), and publisher(s) involved with each such reference, with the circumstances described and reflected in each reference including publications and system implementation references. Upon information and belief, one or more of the Asserted Claims is invalid because the Asserted Patent fails to list the true inventor(s) who contributed to the conception of the alleged invention recited in the Asserted Claim(s), and/or the claimed invention was made in this country by another who had not abandoned, suppressed, or concealed the alleged invention. Defendants therefore reserve the right to contend that one or more of the Asserted Claims is invalid under pre-AIA 35 U.S.C. § 102(f) and/or (g) to the extent that the named inventor did not invent the subject matter in the Asserted

Claim(s), and/or the alleged invention was made in this country by another inventor who had not abandoned, suppressed, or concealed it.

Defendants also reserve the right to assert that the Asserted Claims are invalid for statutory and obviousness-type double patenting.

### **3. Applicant Admitted Prior Art and Prior Art From the Prosecution Histories**

Defendants also identify all prior art references cited or included in the prosecution histories of the Asserted Patents, related patents and applications, and any foreign counterparts. Defendants further incorporate and identify all prior art references identified on the face of any of the Asserted Patents and any patent related to the Asserted Patents. Defendants further reserve the right to rely upon the prosecution histories of the Asserted Patents and any related patents and patent applications, prior art cited in the prosecution histories of the Asserted Patents and any related patent and patent applications to show the scope or state of the art at the time of the alleged invention.

Defendants further identify all statements made by patent owner, ACQIS, inventor, etc. relating to applicant admitted prior art, including statements made in the '624 Patent Family and the Reissue Patent family. Defendants reserve the right to rely on inventor or applicant's admissions concerning the scope or state of the prior art relevant to the Asserted Claims, the prosecution history for the Asserted Patents and related patents and/or patent applications; any deposition or trial testimony of the named inventor on the Asserted Patents; and any papers filed or served, or evidence submitted, by Plaintiff in connection with this litigation and any proceedings involving one or more of the Asserted Patents and any related patents and/or patent applications.

### **4. Additional Prior Art**

This case has just begun, and discovery has not commenced. Plaintiff has not produced the prior art it is aware of, let alone the non-publicly available invalidity contentions provided to

it from other cases. Defendants believe these contentions will identify additional relevant prior art references. Thus, Defendants hereby rely upon and incorporate by reference, as if originally set forth herein, all prior art identified and all Invalidity Contentions, invalidity claim charts or positions asserted by present, future, or former Defendants or by any party to any other litigation or U.S. Patent and Trademark Office proceeding involving one or more of the Asserted Patents or any related patents (or any of their experts) against any of the Asserted Patents or their related patents (the “**Incorporated Invalidity Disclosures**”). These Incorporated Disclosures include any prior art and/or invalidity claim chart provided in the following matters:

- ACQIS, LLC. V. EMC Corp. Case Nos. 21-1772, 16-1827, 16-1828 (CAFC); ACQIS, LLC v. EMC Corp., 1:14-cv-13560 (DMA); ACQIS LLC v. Samsung Electronics Co., Ltd. et al, Case. No. 2-20-cv-00295 (EDTX); ACQIS LLC v. Alcatel-Lucent USA Inc. et al, Case. No. 6-13-cv-00638 (EDTX); ACQIS LLC v. EMC Corp. Case. No. 6-13-cv-00639 (EDTX); ACQIS LLC v. Ericsson, Inc. Case. No. 6-13-cv-00640 (EDTX); ACQIS LLC v. Huawei Tech., Case. No. 6-13-cv-00641 (EDTX); ACQIS LLC v. International Business Machines Corp. Case. No. 6-13-cv-00546 (EDTX); ACQIS LLC v. International Business Machines Corp. Case. No. 6-09-cv-00148 (EDTX); International Business Machines Corporation v. ACQIS LLC, Case. No. 4-11-cv-04896 (NDCA) and any another other litigation in which Plaintiff (or a related entity) has asserted or will assert one or more of the Asserted Patents or a patent related to one or more of the Asserted Patents (the “**Related Lawsuits**”);
- All existing or future *inter partes* review proceedings involving the Asserted Patents, or any related patents, including IPR2021-01094; IPR2021- 01095; IPR2021-01093; IPR2021- 01099; IPR2021- 01102; IPR2021-01113; IPR2021-01114; IPR2021-01103; IPR2021-01104; IPR2021-01105; IPR2021-01107; IPR2021-01108; IPR2021-01109; IPR2021-01110; IPR2021-0111; IPR2021-01112; IPR2021-00666; IPR2021-00667; IPR2021-00668; IPR2021-00669; IPR2021-00670; IPR2021-00604; IPR2021-00605; IPR2021-00606; IPR2021-00607; IPR2021-00608; IPR2014-01469; IPR2014-01462; IPR2014-01452 (the “**Related IPRs**”); and
- Any invalidity contentions and/or identified prior art relating to the Asserted Patents or related patents and disclosed to ACQIS by any other alleged infringer, including informally as part of settlement negotiations or in any other manner outside of formal lawsuits or proceedings

## B. Defendants’ Preliminary Charts

Pursuant to the Court’s OGP, Exhibits A-P (collectively “The Exemplary Prior Art Charts”) set forth exemplary citations to where in the above identified prior art references each element of the asserted claims can be found.<sup>8</sup>

The IPR Charts in Exhibit Q also provide exemplary citations to where each claim limitation of the Asserted Claims (or from the same or similar limitations in related patents) are found in the current prior art identified in IPRs against the Asserted Patents or related patents.<sup>9</sup>

Defendants’ Preliminary Invalidity Contentions further expressly identify, incorporate and include all other invalidity claim charts, whether in existence currently or generated in the future, ever filed or provided to ACQIS in the Incorporated Invalidity Disclosures (the “Incorporated Invalidity Charts”).<sup>10</sup>

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<sup>8</sup> Defendants have not provided claim charts for each of the references identified because: (i) ACQIS has not produced them, even though these are in ACQIS possession and clearly relevant to Invalidity Contentions in this case, (ii) they have substantially similar disclosures to other prior art for which charts have been provided; (iii) because they are used as supporting references in an obviousness combination; and/or (iv) because this case has just begun, and Defendants have been unable to locate or to sufficiently review the thousands of references identified on the face of the patents or related patents, for example. Defendants reserve the right to revise these disclosures and to more particularly identify and/or rely on any of this art or contentions, as discovery commences. ACQIS cannot allege any prejudice from this, as ACQIS should already have knowledge of these disclosures, as they have or will be provided to ACQIS by other alleged infringers.

<sup>9</sup> The IPR Charts includes the IPR Petitions filed against the Asserted Patents or related patents, of which Defendants are currently aware. Like The Exemplary Prior Art Charts, The IPR Charts further identifies where the prior art identified in the IPRs (and incorporated herein) demonstrate the claim limitations of the Asserted Claims. Although only the petitions are included, Defendants specifically identify the entirety of all IPR filings against the Asserted Patents and/or related patents as relevant to the invalidity issues in this case.

<sup>10</sup>By incorporating other contentions, including the Related Lawsuit and the Related IPR contentions, Defendants do not adopt any claim construction position taken by any party in those proceedings.

The Exemplary Prior Art Charts (Exhibits A-P), the IPR Charts (Exhibit Q), and the “Incorporated Invalidity Charts” from other lawsuits or allegations, are collectively referred to as Defendants’ “Invalidity Charts.”

Defendants’ Invalidity Charts identify the exemplary disclosures within the prior art reference(s) that teach the relevant claim elements and limitations. While Defendants have identified citations in the references for the claim limitations, each and every disclosure of the same limitation in the same reference is not necessarily identified. Instead, in an effort to focus the issues, Defendants cite only portions of the references, even when a reference may contain additional support for or disclosure of a particular claim element – whether explicitly or inherently. For example, where the Invalidity Charts cite a particular figure in a prior art reference, the citation should be understood to encompass any and all text referring or relating to that figure, in addition to the figure itself. Similarly, where a cited portion of text refers to a figure, the citation should be understood to include the figure referred to as well. Thus, Defendants may also rely on uncited portions of the prior art references, any cited documents within any prior art reference, other publications, and the testimony of experts to establish that the limitations of the Asserted Claims are anticipated or rendered obvious and/or that a person of ordinary skill in the art would have been motivated to modify or combine certain of the cited references so as to render the claims obvious.

Additional support showing where each claim limitation is met is also specifically identified to include any further references incorporated within or identified within the charted prior art references. Where a prior art reference incorporates additional disclosure, that additional disclosure is considered part of the primary reference under 35 U.S.C. §102, as a single prior art reference. Even if it is not found to be a single reference under 35 U.S.C. §102, then the

incorporated references are specifically identified as relevant prior art and as prior art that, in combination with the primary reference, would render the Asserted Claims invalid under 35 U.S.C. §103. The references incorporated or identified within the primary reference would be combined with the primary reference at least because the primary reference specifically identifies the incorporated/identified other reference as relevant to the teachings and disclosures of the primary reference.

Further, persons of ordinary skill in the art read a prior art reference as a whole, and in the context of other publications and literature. Accordingly, Defendants will rely on uncited portions of the prior art references and on other publications and expert testimony to provide context, and as aids to understanding and interpreting the portions of references that are cited.

Also, to the extent not expressly mentioned herein, these Invalidity Contentions incorporate by reference (1) any and all prior art identified in documents produced by the Defendants in this case; (2) any prior art of which a named inventor of the Asserted Claims is aware and/or on which he, and/or Plaintiff contends the alleged invention(s) of the Asserted Claims builds upon or improves, including the Applicant Admitted Prior Art; (4) any and all admissions by Plaintiff and/or a named inventor regarding the Asserted Patents including, but not limited to, admissions in the specification of the Asserted Patents, the prosecution of the Asserted Patents and related patents and/or patent applications; and (5) all prior art and/or invalidity contentions that Plaintiff discloses, produces or is aware of in connection with any assertion, transfer of rights or contested proceeding concerning the Patents-in-Suit and related patents and/or patent applications.

### **C. Exemplary Combinations of References and Motivations to Combine**

Nothing in the OGP requires an identification of specific combinations of prior art references or for an allegation regarding any alleged motivation to combine the prior art references. Further, discovery is not yet admissible in this case, and Plaintiff has not sought any discovery into

Defendants' alleged combination of prior art references under §103 and/or a motivation to combine references under §103. Nonetheless, Defendants provide the following preliminary, non-binding, exemplary statement regarding the proposed combinations rendering the Asserted Claims invalid under 35 U.S.C. §103 and a preliminary, exemplary identification of motivation(s) to combine the prior art references.

In the Invalidity Charts, Defendants have provided exemplary alleged combinations under 35 U.S.C. §103, and have not limited the charts to just single references. Nonetheless, these charts and identifications are not binding. Defendants are providing them as courtesy to ACQIS, to provide notice of the numerous reasons the claims are invalid, and as examples of combinations that Defendants will likely assert once discovery commences (and ACQIS produces the prior art and contentions already known to it).

Further, Defendants contend that, and specifically provide notice that, to the extent the references listed in the Exemplary Prior Art Charts and the IPR Charts do not anticipate the Asserted Claims, including through inherency, the references listed in the Exemplary Prior Art Charts (Exs. A-P) and the IPR Charts (Ex. Q) render each Asserted Claim obvious under 35 U.S.C. § 103 alone (e.g., based on the disclosure of the identified primary reference, the State of the Art, the AAPA, and/or knowledge of a POSITA), and/or in combination with one or more other references including those (1) listed in the Exemplary Prior Art Charts or the IPR Charts, (2) one or more other references identified in the Related Lawsuits and/or Related IPRs, (3) one or more references identified in the prosecution histories of the Asserted Patents or related patents, including those identified on the face of the Asserted Patents or related patents and/or (4) based on the State of Art as described in Section II.D (and as further explained by any expert testimony and/or report(s) in this case).

Defendants further expressly identify and incorporate, as if set forth fully herein, all combinations of prior art provided to ACQIS in the Incorporated Invalidity Disclosures.

As to a motivation to combine the Identified Prior Art, according to the Supreme Court, no showing of a specific motivation to combine prior art is required to render a claim invalid under 35 U.S.C. §103. *See KSR Int'l Co. v. Teleflex, Inc.*, 127 S.Ct. 1727, 1739-40 (2007). However, express motivations do exist here for combining the Identified Prior Art to render the Asserted Claims obvious under 35 U.S.C. §103. For example, the combinations of art would have no unexpected results, and at most would simply represent a known alternative to one of skill in the art. *See KSR Int'l Co. v. Teleflex, Inc.*, 127 S.Ct. 1727, 1739-40 (2007). Indeed, the Supreme Court has held that a person of ordinary skill in the art is “a person of ordinary creativity, not an automaton” and “in many cases a person of ordinary skill in the art will be able to fit the teachings of multiple patents together like pieces of a puzzle.” *Id.* at 1742. Thus, to a person of ordinary skill in the art, the asserted claims represent solutions that would have been obvious to try with predictable results.

Further, motivations or rationales to combine the Identified Prior Art include, *inter alia*, (i) common knowledge in the art; (ii) improvement of processes and systems of the identified reference(s); (iii) combining prior art elements according to known methods to yield predictable results; (iv) simple substitution of one known element for another; (v) use of a known technique to improve the operation of this technology; (vi) known work in the field of endeavor; (vii) the promotion of interoperability of systems through the use of accepted standards in the community; (viii) explicit or inherent reference to certain references as being relevant or necessary to the operation of the identified reference(s); (ix) the nature of the problem allegedly solved by the Asserted Patents; (x) the teachings of the cited prior art itself; and/or (xi) the knowledge of a person

of ordinary skill in the art. For example, one or more combinations of the Identified Prior Art would have been obvious, because these references would have been combined using: known methods to yield predictable results; common sense; routine innovation; known techniques in the same way; a simple substitution of one known, equivalent element for another to obtain predictable results; and/or a teaching, suggestion, or motivation in the prior art generally. In addition, it would have been obvious to try combining the Identified Prior Art because there were only a finite number of predictable solutions and/or because known work in one field of endeavor prompted variations based on predictable design incentives and/or market forces either in the same field or a different one. Further, combinations of the Identified Prior Art would have been obvious because the combination represents known potential options with a reasonable expectation of success.

Additional evidence that there would have been a motivation to combine the prior art references identified above and in the Exemplary Prior Art Charts and the IPR Charts, includes the interrelated teachings of the Identified Prior Art; the effects of demands known to the design community or present in the marketplace; the existence of a known problem for which there was an obvious solution encompassed by the Asserted Claims; the existence of a known need or problem in the field of the endeavor at the time of the invention(s); and the background knowledge that would have been possessed by a person having ordinary skill in the art. The Identified Prior Art also address the same technical issues and suggest very similar solutions to those issues discussed in the Asserted Patents and/or those issues generally known at the time of the alleged inventions.

Defendants may rely on the cited and uncited portions of the Identified Prior Art, other publications/references, testimony of fact witnesses (such as the alleged inventor of the Asserted Patents, ACQIS, and Defendants' own witnesses), and/or the testimony of experts (including

testimony from Related Lawsuits or Related IPRs), to establish that a person of ordinary skill in the art would have been motivated to modify or combine the references so as to render the Asserted Claims obvious. Defendants further incorporate the testimony and reports of their expert(s) in this matter, the testimony of ACQIS, ACQIS's experts, or the inventor, and the expert testimony from other Defendants in any related lawsuits or related IPRs.

#### **IV. Identification of Limitations the Defendants Contend Are indefinite or Lack Written Description Support Under Section 112**

As set forth in more detail below, the Asserted Claims of the Asserted Patents are invalid as indefinite and for lack of written description support under 35 U.S.C. §112.

A more detailed basis for Defendants' 35 U.S.C. § 112 invalidity defenses with regard to the Asserted Patents will be set forth in Defendants' claim construction briefs, summary judgment motions and/or expert report(s) on invalidity, to be served in accordance with the Court's Scheduling Order. Defendants reserve the right to amend and/or supplement these disclosures as discovery commences, including based on any disclosures made to Plaintiff (but which have not been produced in this case), including contentions/disclosures from Related Lawsuits, Related IPRs, and including any expert report(s) from Related Lawsuits and Related IPRs.

##### **A. Invalidity Under §112, ¶2 or (b): Indefiniteness**

For at least the reasons set forth below, the Asserted Claims of the Asserted Patents are invalid as indefinite under 35 U.S.C. §112. United States patent law requires that a patent contain one or more claims "particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention." 35 U.S.C. § 112, ¶ 2 or (b). Accordingly, a claim must "give notice to the public of the extent of the legal protection afforded by the patent, so that interested members of the public, e.g., competitors of the patent owner, can determine whether or not they infringe." *Default Proof Credit Card Sys. Inc. v. Home Depot U.S.A., Inc.*, 412 F.3d 1291, 1302-

03 (Fed. Cir. 2005) (internal quotes and citation omitted). According to the Supreme Court, a patent is invalid as indefinite where its claims “fail to inform, with reasonable certainty, those skilled in the art about the scope of the invention.” *Nautilus, Inc. v. Biosig Instruments, Inc.*, 572 U.S. 898, 901, (2014).

Further, for terms of degree, which are inherently subjective terms, “it is not enough...to identify ‘some standard for measuring the scope of the phrase.’” *Interval Licensing LLC v. AOL, Inc.*, 766 F.3d 1364, 1370–71 (Fed. Cir. 2014). Rather, “[t]he claims, when read in light of the specification and the prosecution history, must provide objective boundaries for those of skill in the art.” *Id.*

Relatedly, where claim terms require a reference to understand the terms, and “there is no reference provided in the specification to teach a person of ordinary skill what constitutes” one claim terms versus another or how the two claim terms “are related,” then the claims are invalid as indefinite. *Icon Health & Fitness, Inc. v. Polar Electro Oy*, 656 F. App'x 1008, 1014 (Fed. Cir. 2016) (finding claim invalid as indefinite where “there is no reference provided in the specification to teach a person of ordinary skill what constitutes an in-band communication versus an out-of-band communication (other than the fact that they are different) or how the two are related”); *see also, Abdou v. Alphatec Spine, Inc.*, No. 12-CV-1804 BEN RBB, 2014 WL 6611422, at \*9 (S.D. Cal. Nov. 19, 2014) (finding relationship terms invalid as indefinite and noting that: “There is no question that the relationship terms lack any quantitative parameters...Likewise, neither “in proximity” nor any other language in the specification otherwise defines what the proximity would be in any specific way and “first surface” is not further described in any way that would define what or where the surface should be...”).

Defendants identify at least the following exemplary limitations (and the variations thereof) from the Asserted Claims of the Asserted Patents which Defendants contend are indefinite:

- “a coupling site”/ “a first coupling site”/ “a second coupling site”
- “system memory module” / “memory modules”
- “mass storage device”
- “the modular computer”
- “modular”
- “a serial communication controller”
- “an interface controller”/ “a first interface controller” / “an interface device”
- “single chip”
- “integrated”
- “each of the computer modules is similar in design to each other”
- “each of the computer modules operates fully independent of each other”
- “a plurality of computer modules, each computer module coupled to one of the coupling sites through the connector, and comprising a processing unit, a main memory coupled to the processing unit, and an interface controller coupled to a differential signal channel comprises two sets of unidirectional low voltage serial bit channels in opposite directions transmitting encoded PCI bus transaction data;”
- “without any intervening PCI bus”/ “without any intervening Peripheral Component Interconnect (“PCI”) bus”
- “to preserve the PCI bus transaction”
- “improve peripheral data communication speed between the computer and the console”
- “opposite directions” / “opposite direction”
- “multiple...pairs” / “two sets...pairs”
- “multiple...channels”/ “two sets...channels”
- “increasing data throughput”
- “Low Voltage” / “Low Voltage Differential Signal (LVDS) channel”/ “LVDS channel” / “the first LVDS channel”
- “PLL clock circuitry generates different clock frequencies” / “Phase-Locked Loop (PLL) clock circuitry capable of generating different clock frequencies”
- “the interface controller is configurable to convey the PCI bus transaction with different serialized forms through the LVDS channel on different numbers of differential signal pairs”

- “the second LVDS channel is configurable in different numbers of differential signal pairs to transmit the PCI bus transaction”
- “LVDS channel conveys encoded address and data bits”
- “integrated graphics subsystem directly outputs digital video display signals”
- “integrated central processing unit and graphics subsystem directly outputs digital video display signals”
- “integrated central processing unit and graphics subsystem directly outputs digital video display signals to a third differential signal channel”
- “integrated central processing unit and graphics subsystem directly outputs digital video display information”
- “graphics subsystem directly outputs digital video display data to a third unidirectional”
- “different numbers”
- “point-to-point data communication link”
- “plug and play operations”
- “in different numbers of differential signal pairs” / “on different numbers of differential signal line pairs”

Based on the specifications, prosecution histories, and the claim language as a whole, the above terms “fail to inform, with reasonable certainty, those skilled in the art about the scope of the invention.” Therefore, the Asserted Claims that contain the above limitations (or variations thereof) are invalid as indefinite (including any claims that depend from an indefinite claim). Every Asserted Claim contains at least one of the above limitations or variations thereof. Therefore, each and every Asserted Claim of the Asserted Patents is invalid as indefinite.

Further, the Asserted Claims are indefinite under *IPXL*, because the claims, *in their entirety*, recite both a method and apparatus. Where, as here, a claim “recites both a system and the method for using that system, it does not apprise a person of ordinary skill in the art of its scope, and it is invalid under section 112, paragraph 2.” *IPXL Holdings, L.L.C. v. Amazon.com, Inc.*, 430 F.3d 1377, 1384 (Fed. Cir. 2005). Defendants allege that all of the Asserted Claims are invalid under the *IPXL* standard, for impermissibly mixing apparatus and method claim limitations. For example, the ’750 patent claims impermissibly recite both a system and the

method for using that system. (*see, e.g.*, '750 patent claim 1 and 2 (“A computer, comprising: an integrated central processing unit and interface controller in a single chip...” (claim 1) and “...wherein the interface controller **configures** the first LVDS channel to convey the PCI bus transaction at different data transfer rates based on the different clock frequencies generated by the PLL clock circuitry.” (claim 2)).) The RE'468 and RE'947 patents' claims similarly mix impermissible apparatus claims with their method of use. (RE'468 (“A computer, comprising:.. a peripheral bridge directly coupled to the central processing unit without any intervening Peripheral Component Interconnect (PCI) bus, wherein the peripheral bridge **directly conveys** an encoded serial bit stream of address and data bits of a Peripheral Component Interconnect (PCI)...”).)

Nothing in Defendants' Invalidity Contentions should be construed as an admission that any of the Asserted Claims are somehow definite. As noted above, Defendants contend that the claims reciting the exemplary terms above are indefinite. To the extent that the Court later finds these terms sufficiently definite, the prior art meets these limitations for all the reasons set forth in these Invalidity Contentions, including as shown in the Invalidity Charts.

#### **B. Invalidity Under § 112, ¶1 or (a): Lack of Written Description and Lack of an Enabling Disclosure**

As detailed below, the specification of the Asserted Patents lacks written description support for the alleged claimed inventions of the Asserted Claims, as required by 35 U.S.C. § 112, ¶1 or (a). To satisfy the written description requirement of 35 U.S.C. § 112, ¶ 1 or (a), the specification of a patent must “clearly allow persons of ordinary skill in the art to recognize that the inventor invented what is claimed” and “had possession of the claimed subject matter as of the filing date.” *Ariad Pharm., Inc. v. Eli Lilly & Co.*, 598 F.3d 1336, 1351 (Fed. Cir. 2010) (*en banc*). In particular, an adequate written description must “demonstrate that the patentee possessed the full

scope of the invention recited in [the] claim.” *LizardTech, Inc. v. Earth Res. Mapping, Inc.*, 424 F.3d 1336, 1345 (Fed. Cir. 2005).

Although not required or called for at this time under the OGP, Case Schedule or requested in any valid discovery request, Defendants further provide a preliminary, non-binding exemplary contention regarding the Asserted Claims’ compliance with the enablement statute. Specifically, Defendants contend the specification of each of the Asserted Patents also lacks an enabling disclosure as required by 35 U.S.C. § 112, ¶1 or (a). To satisfy the enablement requirement, “the specification of a patent must teach those skilled in the art how to make and use the full scope of the claimed invention without undue experimentation.” *Genentech, Inc. v. Novo Nordisk A/S*, 108 F.3d 1361, 1365 (Fed. Cir. 1997) (quotations omitted); *see also, Sitrick v. Dreamworks, LLC*, 516 F.3d 993, 1000 (Fed. Cir. 2008) (holding that the inventors must set forth sufficient information in the specification to enable one of ordinary skill in the art to make and use the invention without undue experimentation).

Defendants contend that at least the following claim terms (and the variations thereof) lack written description support and/or are not enabled by the specification:

**’624 Patent**

- “a plurality of computer modules, each computer module coupled to one of the coupling sites through the connector, and comprising a processing unit, a main memory coupled to the processing unit, and an interface controller coupled to a differential signal channel comprises two sets of unidirectional low voltage serial bit channels in opposite directions transmitting encoded PCI bus transaction data” (’624 patent, claim 11)
- “wherein each of the computer modules operates fully independent of each other, and wherein the interface controller couples to the console through the differential signal channel for data communication, through the connector of the coupling site” (’624 patent, claim 11)

**’873 Patent**

- “a peripheral bridge directly coupled to the processing unit, the peripheral bridge comprising an interface controller directly coupled to the LVDS channel” (‘873 patent, claim 54, 97)
- “a low voltage differential signal (LVDS) channel comprising two sets of unidirectional, multiple serial bit channels to transmit data in opposite directions for communicating an encoded serial bit stream of Peripheral Component Interconnect (PCI) bus transaction;” (‘873 patent, claim 54, 77, 97)
- “wherein the processing unit is configured to couple to an external network through the LVDS channel” (‘873 patent, claim 97)

### **’768 Patent**

- “wherein the PLL clock circuitry generates different clock frequencies, and the interface controller conveys the PCI bus transaction through the LVDS channel based on the different clock frequencies” (’768 patent, claim 1)
- “wherein the interface controller conveys the PCI bus transaction through the LVDS channel based on a selected frequency of the different clock frequencies” (’768 patent, claim 2)
- “wherein the interface controller is configurable to convey the PCI bus transaction with different serialized forms through the LVDS channel on different numbers of differential signal pairs.” (’768 patent, claim 3)
- “an integrated peripheral bridge, interface controller, and Phase-Locked Loop (PLL) clock circuitry in a single chip, directly coupled to the central processing unit without any intervening PCI bus” (’768 patent, claim 4)
- “wherein the PLL clock circuitry generates different clock frequencies, and the interface controller conveys the PCI bus transaction through the LVDS channel based on the different clock frequencies.” (’768 patent, claim 4)
- “wherein the interface controller conveys the PCI bus transaction with different data rate frequencies through the LVDS channel based on the different clock frequencies.” (’768 patent, claim 5)
- “wherein the interface controller is configurable to convey the PCI bus transaction with different serialized forms through the LVDS channel on different numbers of differential signal pairs.” (’768 patent, claim 6)
- “wherein the interface controller couples to Phase-Locked Loop (PLL) clock circuitry, and wherein the interface controller generates a data transfer signal to convey the PCI bus

transaction through the LVDS channel based on one of the different clock frequencies generated by the PLL clock circuitry” (’768 patent, claim 17)

- “a second Low Voltage Differential Signal (LVDS) channel comprising two sets of unidirectional, differential signal pairs transmitting data serially in opposite directions, wherein the second LVDS channel is a point-to-point data communication link” (’768 patent, claim 33)
- “wherein the computer couples to a console and wherein the central processing unit communicates to the console through the second LVDS channel utilizing a Universal Serial Bus (USB) protocol.” (’768 patent, claim 34)
- “wherein the interface controller generates a data transfer signal to convey the PCI bus transaction through the first LVDS channel based on one of the different clock frequencies generated by the PLL clock circuitry.” (’768 patent, claim 35)
- “wherein the interface controller generates different data transfer frequencies to convey the PCI bus transaction through the LVDS channel based on different clock frequencies generated by the PLL clock circuitry” (’768 patent, claim 25)
- “a second Low Voltage Differential Signal (LVDS) channel comprising two sets of unidirectional, differential signal pairs transmitting data serially in opposite directions to convey data using a Universal Serial Bus (USB) protocol” (’768 patent, claim 40)

#### **’797 Patent**

- “populating the sockets with system memory to improve system performance” (’797 patent, claim 16)
- “conveying Universal Serial Bus (USB) protocol data from the integrated CPU and graphics controller chip, over the first LVDS channel for external USB protocol data communication” (’797 patent, claim 33)
- “configuring the interface controller to generate different data transfer frequencies to convey the PCI bus transaction through the LVDS channel based on different clock frequencies generated by the PLL clock circuitry” (’797 patent, claim 38)

#### **’750 Patent**

- “wherein the interface controller configures the first LVDS channel to convey the PCI bus transaction at different data transfer rates based on the different clock frequencies generated by the PLL clock circuitry” (’750 patent, claim 2)

- “wherein the interface controller configures the first LVDS channel to convey the PCI bus transaction at different data transfer rates based on the different clock frequencies generated by the PLL clock circuitry” (’750 patent, claim 4)
- “a connector adapted to convey a serial bit stream of Universal Serial Bus (USB) protocol data packets in a second Low Voltage Differential Signal (LVDS) channel comprising two unidirectional, differential signal pairs that transmit data in opposite directions” (’750 patent, claim 4)
- “wherein the computer further comprises a third LVDS channel adapted to convey Universal Serial Bus (USB) protocol data packets” (’750 patent, claim 7)
- “a connector adapted to convey digital video display information from a second differential signal channel coupled directly from the integrated central processing unit and graphics subsystem” (’750 patent, claim 10)
- “wherein the interface controller configures the first LVDS channel with different numbers of unidirectional, differential signal pairs to convey the PCI bus transaction at different data transfer rates” (’750 patent, claim 11)
- “a second LVDS channel coupled to a mass storage device, comprising two sets of unidirectional, differential signal pairs transmitting data serially in opposite directions, wherein the second LVDS channel is a point-to-point data communication link” (’750 patent, claim 21)
- “wherein the PLL clock circuitry generates different clock frequencies, and the interface controller configures the first LVDS channel to convey the PCI bus transaction at different data transfer rates based on the different clock frequencies generated by the PLL clock circuitry” (’750 patent, claim 23)
- “a second LVDS channel coupled to the connector, adapted to convey Universal Serial Bus (USB) protocol data packets, wherein the second LVDS channel comprises two unidirectional, differential signal pairs that transmit data packets in opposite directions” (’750 patent, claim 24)
- “wherein the PLL clock circuitry generates different clock frequencies, and the interface controller configures the first LVDS channel to convey the PCI bus transaction at different data transfer rates based on the different clock frequencies generated by the PLL clock circuitry” (’750 patent, claim 33)
- “wherein the PLL clock circuitry generates different clock frequencies, and the interface controller is directly connected to the first LVDS channel and configures the first LVDS channel to convey the PCI bus transaction at different data transfer rates based on the different clock frequencies generated by the PLL clock circuitry” (’750 patent, claim 45)

- “a second LVDS channel comprising two sets of unidirectional, differential signal pairs transmitting data serially in opposite directions, wherein the second LVDS channel is a point-to-point data communication link to convey Universal Serial Bus (USB) protocol data packets.” (’750 patent, claim 46)
- “wherein the interface controller configures the first LVDS channel with different numbers of unidirectional, differential signal pairs to convey the PCI bus transaction at different data transfer rates” (’750 patent, claim 47)
- “wherein the first LVDS channel conveys Universal Serial Bus (USB) protocol through the connector to the console” (’750 patent, claim 48)
- “providing a Low Voltage Differential Signal (LVDS) channel to convey Universal Serial Bus (USB) protocol through the connector, the first LVDS channel comprising two unidirectional, serial bit channels that transmit data in opposite directions.” (’750 patent, claim 50)

#### **’769 Patent**

- “providing a first Low Voltage Differential Signal (LVDS) channel to convey Universal Serial Bus (USB) protocol data through the connector, wherein the LVDS channel comprises two unidirectional, serial bit channels that transmit data in opposite directions” (’769 patent, claim 19)

#### **’359 Patent**

- “wherein the second LVDS channel is adapted to transmit data packets in accordance with a Universal Serial Bus (USB) protocol” (’359 patent, claim 1)
- “wherein the second LVDS channel is adapted to transmit data packets in accordance with a Universal Serial Bus (USB) protocol” (’359 patent, claim 6)
- “wherein the central processing unit conveys Universal Serial Bus (USB) protocol data to the console through the second LVDS channel” (’359 patent, claim 17)
- “wherein the second channel is adapted to transmit data packets in accordance with a Universal Serial Bus (USB) protocol” (’359 patent, claim 19)

#### **’977 Patent**

- “a serial bit channel that couples to the connector, wherein the serial bit channel is adapted to transmit data packets in accordance with a Universal Serial Bus (USB) protocol” (’977 patent, claim 1)

- “wherein the second LVDS channel conveys Universal Serial Bus (USB) protocol signals” (’977 patent, claim 11)
- “wherein the third LVDS channel conveys Universal Serial Bus (USB) protocol signals” (’977 patent, claim 17)

#### **RE’654 Patent**

- “enabling the PCI bus transaction to be conveyed serially through the second LVDS channel to the console to improve peripheral data communication speed between the computer and the console.” (RE’654, claim 14)
- “a second Low Voltage Differential Signal (LVDS) channel comprising two sets of unidirectional, differential signal pairs transmitting data serially in opposite directions, wherein the second LVDS channel is a point-to-point data communication link” (RE’654 Claim 14)
- “increasing external data communication speed of a computer” (RE’654 patent, claim 20)
- “enabling Universal Serial Bus (USB) protocol data to be conveyed over the second LVDS channel” (RE’654 patent, claims 20, 23)
- “conveying said USB protocol data through the second LVDS channel upon coupling to the console in a plug and play operation” (’654 patent, claims 22, 25) “to improve computer data transaction performance” (RE’654 patent, claim 26)
- “to improve computer storage data access performance” (RE’654 patent, claim 35)
- “connecting system memory directly to the CPU to improve memory data performance of the computer” (RE’654 patent, claim 35)

#### **RE’140 Patent**

- “conveying Universal Serial Bus (USB) protocol information over the first LVDS channel” (RE’140 patent, claim 15)
- “conveying Universal Serial Bus (USB) protocol information through the first LVDS channel” (RE’140 patent, claim 18)
- “conveying Universal Serial Bus (USB) protocol information over the second LVDS channel” (RE’140 patent, claim 20)
- “conveying Universal Serial Bus (USB) protocol information through the first LVDS channel” (RE’140 patent, claim 22)

- “conveying Universal Serial Bus (USB) protocol information over the second LVDS channel” (RE’140 patent, claim 23)
- “conveying Universal Serial Bus (USB) protocol information through the first LVDS channel” (RE’140 patent, claim 26)
- “coupling Universal Serial Bus (USB) protocol information from the LVDS channel to the console” (RE’140 patent, claim 29)
- “conveying Universal Serial Bus (USB) protocol information to the console through the second LVDS channel and the connector” (RE’140 patent, claim 34)
- “conveying Universal Serial Bus (USB) protocol information to the external peripheral through the second LVDS channel and the connector” (’140 patent, claim 36)
- “conveying Universal Serial Bus (USB) protocol information through the first LVDS channel” (’140 patent, claim 37)

#### **RE’468 Patent**

- “a peripheral bridge directly coupled to the central processing unit without any intervening Peripheral Component Interconnect (“PCI”) bus, wherein the peripheral bridge directly conveys an encoded serial bit stream of address and data bits of a PCI bus transaction over a second LVDS channel comprising two sets of unidirectional, serial bit channels to transmit data in opposite directions” (RE’468, claim 14)
- “a central processing unit directly connected to a first Low Voltage Differential Signal (LVDS) channel comprising two sets of unidirectional, serial bit channels to transmit Universal Serial Bus (USB) Protocol data in opposite direction” (RE’468, claim 21)
- “a second LVDS channel comprising two sets of unidirectional, serial bit channels to transmit data in opposite directions, and a peripheral bridge directly coupled to the central processing unit without any intervening Peripheral Component Interconnect bus, wherein the peripheral bridge directly conveys an encoded serial bit stream of address and data bits of a Peripheral Component Interconnect (“PCI”) bus transaction over the second LVDS channel” (RE’468, claim 26)
- “a peripheral bridge directly coupled to the first LVDS channel to communicate an encoded serial bit stream of address and data bits of a Peripheral Component Interconnect (“PCI”) bus transaction, the peripheral bridge directly coupled to the central processing unit without any intervening PCI bus” (RE’468, claim 26)
- “a peripheral bridge directly coupled to the first LVDS channel to communicate an encoded serial bit stream of address and data bits of a Peripheral Component Interconnect (“PCI”)

bus transaction, the peripheral bridge directly coupled to the central processing unit without any intervening PCI bus” (RE’468, claim 29)

- “a peripheral bridge directly coupled to the central processing unit without any intervening Peripheral Component Interconnect (PCI) bus, wherein the peripheral bridge directly conveys an encoded serial bit stream of address and data bits of a Peripheral Component Interconnect (PCI) bus transaction over a first Low Voltage Differential Signal (LVDS) channel comprising two sets of unidirectional, serial bit channels to transmit data in opposite directions” (RE’468, claim 35)
- “a peripheral bridge directly coupled to the central processing unit without any intervening PCI bus, wherein the peripheral bridge directly conveys a second encoded serial bit stream of address and data bits of a (PCI) bus transaction over a second LVDS channel comprising two sets of unidirectional, serial bit channels to transmit data in opposite directions.” (RE’468, claim 37)

#### **RE’947 Patent**

- “the CPU is configured to output a serial bit stream of Universal Serial Bus (USB) protocol information that is conveyed over the LVDS channel” (RE’947, claim 14)
- “a peripheral bridge directly coupled to the central processing unit without any intervening Peripheral Component Interconnect (PCI) bus, wherein the peripheral bridge directly conveys an encoded serial bit stream of address bits, data bits, and byte enable information bits of a PCI bus transaction over the first LVDS channel” (RE’947, claim 35)
- “a peripheral bridge directly coupled to the CPU without any intervening Peripheral Component Interconnect (PCI) bus;” (RE’947, claims 51, 57)

#### **RE’739 Patent**

- “a central processing unit directly connected to a first Low Voltage Differential Signal (LVDS) channel comprising two unidirectional, differential signal pairs to transmit Universal Serial Bus (USB) Protocol data in opposite directions” (RE’739 patent, claim 14)
- “wherein the second LVDS channel transmits Universal Serial Bus (USB) Protocol data through the connector upon coupling to the console” (RE’739 patent, claim 18)
- “wherein the second LVDS channel transmits Universal Serial Bus (USB) Protocol data through the connector” (RE’739 patent, claim 30)

All claims reciting the above terms are neither supported by the specification nor enabled to their full scope. Accordingly, they are invalid under section 112, ¶1 and (a).

The Court's OGP only asks for identification of the limitations from the Asserted Claims that are indefinite or lack written description support under section 112. Nonetheless, in addition to the above limitations, Defendants further identify the *entirety* of the Asserted Claims as lacking written description support and as not enabled by the specifications. Specifically, the specifications of the Asserted Patents do not provide written description support for, nor an enabling disclosure for, the *combination* of limitations claimed in each Asserted Claim, rendering each Asserted Claim invalid for lack of written description support and non-enablement. *See e.g., Purdue Pharma L.P. v. Recro Tech., LLC*, 694 F. App'x 794, 797–98 (Fed. Cir. 2017) (“To the extent [patentee] contends that a person of skill in the art would isolate and combine aspects from various embodiments in the specifications (including patents incorporated by reference...) to obtain the claimed invention, [Patentee] relies upon the wrong test. A description that merely renders the invention obvious does not satisfy the written description requirement.”) (internal quotations omitted).); *Novozymes A/S v. DuPont Nutrition Biosciences APS*, 723 F.3d 1336, 1349 (Fed. Cir. 2013) (noting that for written description support, each claim must be considered “as an integrated whole rather than as a collection of independent limitations”). Again, Defendants specifically allege that all of the Asserted Claims are invalid for lack of written description support, including because the alleged combination of elements in each Asserted Claim is not supported or enabled by the specifications.

Moreover, the Asserted Claims are not supported or enabled by the alleged priority patents or documents. Defendants incorporate their Priority Argument Section II.C above. As explained above, even if the '758 and '199 Applications (“Original Applications”) included the disclosures of the '882, '548 and '493 applications, the Original Applications would still not provide sufficient written description support for the Asserted Claims of the Asserted '624 Family Patents and

Reissue Family Patents, respectively. For example, the following exemplary limitations from the Asserted Claims are not disclosed in the Original Applications: an integrated CPU and graphics controller in a single chip; an integrated central processing unit and interface controller in a single chip; a CPU directly connected to a first LVDS channel; a CPU and interface device directly connected to a first LVDS channel; a peripheral bridge comprising an interface controller directly coupled to the central processing unit without any intervening PCI bus; an integrated central processing unit, interface controller and PLL clock circuitry in a single chip; an integrated peripheral bridge, interface controller, and PLL clock circuitry in a single chip, directly coupled to the central processing unit without any intervening PCI bus; an integrated central processing unit, graphics subsystem and interface controller in a single chip; a central processing unit comprising an interface controller directly connected to a first Low Voltage Differential Signal (LVDS) channel; obtaining an integrated CPU and graphics controller in a single chip; connecting a Central Processing Unit (CPU) directly to a peripheral bridge on a printed circuit board of a computer system; connecting a Low Voltage Differential Signal (LVDS) channel directly to the CPU on the printed circuit board; providing an integrated Central Processing Unit (CPU) and graphics controller in a single chip; coupling an integrated Central Processing Unit (CPU) and graphics controller chip to a connector; and variations of these limitations. At least the identified terms lack written description and/or enablement to the extent that ACQIS asserts that the claims benefit from the priority of the Original Applications. Further, the Original Applications do not support or enable the claimed inventions as a whole, as they do not disclose or support the claimed *combination* of elements of the Asserted Claims.

**V. Identification of Claims the Defendants Contend Are Directed to Ineligible Subject Matter Under Section 101**

As discovery has not yet commenced and this case has just begun, Defendants reserve the right to assert patent ineligibility allegations against the Asserted Patents at a later date.

**VI. The Reissue Patents Are Invalid for Violating the Original Patent/Same Invention Rule and For Adding New Matter**

Identification of additional grounds of invalidity are not required by the OGP, discovery, or schedule at this time. Nonetheless, Defendants provide this preliminary, non-binding, exemplary statement regarding the invalidity of the Reissue Patents for failure to comply with the Original Patent/Same Invention Rule.

Each Asserted Claim from Each Asserted Reissued Patent violates the Original Patent and Same Invention Rule. Further, the Reissue Patents are Invalid for introducing into the application for reissue new matter and/or matter not disclosed in the original patent.

The Reissue Statute provides:

Whenever any patent is, through error, deemed wholly or partly inoperative or invalid, by reason of a defective specification or drawing, or by reason of the patentee claiming more or less than he had a right to claim in the patent, the Director shall, on the surrender of such patent and the payment of the fee required by law, reissue the patent **for the invention disclosed in the original patent**, and in accordance with a new and amended application, for the unexpired part of the term of the original patent. **No new matter shall be introduced into the application for reissue.**

(35 U.S.C. §251(a) (emphasis added).) Under the statute, a reissue patent may sometimes be used to either broaden or narrow claims. 35 U.S.C. § 251. However, the Patent Act forbids the introduction of new matter into the Specification during reissue. *Id.* (“No new matter shall be introduced into the application for reissue.”). The statutory prohibition against the introduction of new matter also generally applies to any attempt to broaden the claims beyond that which was supported by the original Specification. *In re Amos*, 953 F.2d 613, 618–19 (Fed. Cir. 1991). This

is sometimes referred to as the “same invention” requirement based on the Supreme Court’s decision in *U.S. Industrial Chemicals, Inc. v. Carbide & Carbon Chemicals Corp.*, 315 U.S. 668 (1942). The Same Invention Rule has repeatedly been reaffirmed by the Federal Circuit. *See e.g., Hester Indus., Inc. v. Stein, Inc.*, 142 F.3d 1472 (Fed. Cir. 1998); *Antares Pharma, Inc. v. Medac Pharma Inc.*, 771 F.3d 1354 (Fed. Cir. 2014); *Forum US, Inc. v. Flow Valve, LLC*, Appeal No. 2018-1765 (Fed. Circ. June 17, 2019).<sup>11</sup>

According to the Supreme Court and Federal Circuit, “[i]t is well settled that for broadening reissue claims, ‘it is not enough that an invention might have been claimed in the original patent because it was suggested or indicated in the specification.’” *Forum US*, at 8 (quoting *Indus. Chems.*, 315 U.S. at 676) (finding that reissue claims were invalid for violating the Original Patent Rule). Rather, “for broadening reissue claims...‘[i]t must appear from the face of the instrument that what is covered by the reissue was intended to have been covered and secured by the original.’” *Forum US*, at 8 ((quoting *Indus. Chems.*, 315 U.S. at 676.) Indeed, the standard for proving support in the original written description to obtain claims in reissue under § 251, is actually **higher** than that required by § 112 to obtain claims during original prosecution. *See Antares Pharma, Inc.*, 771 F.3d at 1362. For reissue claims, “the specification must **clearly and unequivocally** disclose the newly claimed invention as a separate invention.” *Id.*

Here, the specification of the original patent does not clearly and unequivocally disclose the newly claimed inventions of the reissue claims as a separate invention as required by §251. For example, the original specification does not support the limitations identified above as lacking written description support (Sec. IV.B.). Each of the Asserted Claims of the Asserted Reissue

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<sup>11</sup> The 1952 Patent Act stated that reissue patents must include the same invention. The act was later amended to state that the reissue patents must be based on the “original patent.” Thus, the “same invention” and “original patent” rule are different names for the same requirement/rule.

Patents include at least one of the above limitations (or a variation thereof), which are not supported by the original patent specification. Thus, each of the Asserted Claims of the Reissue Patents are invalid for violating the Same Invention/Original Patent Rule.

In addition to the above exemplary limitations, the original patent specification does not disclose the **combination** of claim elements of each of the Asserted Claims of the Asserted Reissue Patents. Because the original patent specification does not support the newly claimed combination of claim elements in the Asserted Claims of the Asserted Reissue Patents, all of the Asserted Claims violate the Original Patent Rule for this additional reason and are therefore invalid. *See, e.g.,* MPEP § 1412.01 (“Therefore, claims drawn to an invention comprising a newly claimed combination of features that were only disclosed in the original patent as suggested alternatives (and not as a single combination) or only as part of the original invention and not as an invention separate from the original invention would not satisfy the original patent requirement...”)

Further, the Asserted Claims of the Reissue Patents are also invalid for introducing new matter into the specification in violation of §251. For example, in its Response to an IPR regarding the Reissue Family, ACQIS admits that it *both* added new material to the specification (on numerous occasions) and that it added entirely new/different claims from the original patent. (*See, e.g.,* Patent Owner Resp. at 3 (IPR2021-00608 (RE’654)) (ACQIS admitting that in 2011 during prosecution of the Reissue Family, Patent Owner “**again** amended the specification through a later amendment on June 17, 2011 to add the allegedly newly essential material from U.S. Provisional Application no. 60/083,886 (“Chu ’886”), consistent with the subject matter of the new claims submitted therewith...”)).) The Reissue Patents’ Asserted Claims are thus invalid for violating Section §251.

## VII. Defendants' Document Productions

Pursuant to OGP, the Defendants are jointly and concurrently producing the prior art referenced in these Invalidity Contentions, and the accompanying Invalidity Claim Charts.

In addition, based on their investigations to date, each Defendant individually have produced or concurrently produce documents in their possession, custody, or control required to accompany these Invalidity Contentions under the OGP. Each Defendant hereby incorporates into its production all such documents produced by the other Defendants, exclusive of documents related to their respective accused product(s). Each Defendant reserves the right to rely on all such documents produced by any other Defendant.

Defendants further reserve the right to supplement these productions with additional documentation, in accordance with the Federal Rules of Civil Procedure, the Local Rules, the Court's orders and other applicable rules and statutes.

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Dated: July 19, 2021

/s/ Harold Davis

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