

Petition for *Inter Partes* Review of U.S. Reissue Patent No. 45,140  
Claims 14-38

UNITED STATES PATENT AND TRADEMARK OFFICE

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**BEFORE THE PATENT TRIAL AND APPEAL BOARD**

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Intel Corporation  
Petitioner

v.

ACQIS LLC  
Patent Owner

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Case IPR2021-01103

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**PETITION FOR *INTER PARTES* REVIEW OF**  
**U.S. REISSUED PATENT NO. 45,140**  
CHALLENGING CLAIMS 14-38  
UNDER 35 U.S.C. § 312 AND 37 C.F.R. § 42.104

Mail Stop Patent Board  
Patent Trial and Appeal Board  
U.S. Patent and Trademark Office  
P.O. Box 1450  
Alexandria, VA 22313-1450

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**PETITIONER’S EXHIBIT LIST**

<b>Petitioner Exhibit No.</b>	<b>DESCRIPTION</b>
1001	U.S. Reissued Patent No. 45,140 (“RE140”)
1002	Declaration of Dr. Bill Lin
1003	U.S. Patent No. 6,345,330 (“Chu330”)
1004	U.S. Patent Publication No. 2003/0135771 (“Cupps”)
1005	U.S. Patent No. 6,216,185 (“Chu185”)
1006	File history of RE140 (“RE140 FH”)
1007	U.S. Patent No. 6,643,777 (“Chu777”)
1008	U.S. Reissued Patent No. 42,984 (“RE984”)
1009	File history of RE984 (“RE984 FH”)
1010	U.S. Patent Application No. 60/083,886 (“’886 Provisional”)
1011	File history of Chu330 (“Chu330 FH”)
1012	August 12, 2011 Amendment from File History of Control No. 90/010,816 (Reexamination of Chu185)
1013	U.S. Reissued Patent No. 41,092 (“RE092”)
1014	U.S. Reissued Patent No. 43,602 (“RE602”)
1015	U.S. Reissued Patent No. 44,468 (“RE468”)
1016	U.S. Reissued Patent No. 44,654 (“RE654”)
1017	U.S. Patent No. 6,621,760 (“Ahmad”)
1018	<i>Reserved</i>
1019	RE140 with highlights of substantively identical portions from Chu330, Chu185, ’886 Provisional, and Chu777
1020	File history of U.S. Reissued Patent No. 43,602 (“RE602 FH”)
1021	File history of U.S. Reissued Patent No. 44,468 (“RE468 FH”)
1022	<i>ACQIS LLC v. EMC Corp.</i> , Civil Action No. 1:14-cv-13560, No. 185 (D. Mass. Jan. 20, 2017) (EMC Corporation’s Opening Claim Construction Brief)

All emphases, colors, and annotations have been added unless indicated otherwise.

## **I. Introduction**

Intel Corporation (“Petitioner”) requests *inter partes* review (“IPR”) of claims 14-38 (“challenged claims”) of U.S. Reissued Patent No. 45,140 (“RE140” (Ex-1001)).

## **II. Mandatory Notices**

### **A. Related Matters**

ACQIS LLC (“Patent Owner” or “ACQIS”) filed patent infringement actions asserting RE140 against a number of defendants, not including the Petitioner.

- *ACQIS LLC v. Samsung Electronics Co., Ltd. et al.*, Civil Action No. 2:20-cv-00295 (E.D. Tex. 2020),
- *ACQIS LLC v. MITAC Holdings Corp. et al.*, Civil Action No. 6:20-cv-00962 (W.D. Tex. 2020),
- *ACQIS LLC v. ASUSTek Computer Inc.*, Civil Action No. 6:20-cv-00966 (W.D. Tex. 2020), and
- *ACQIS LLC v. Lenovo Group Ltd. et al.*, Civil Action No. 6:20-cv-00967 (W.D. Tex. 2020).

ACQIS has filed the following patent infringement actions on patents that are related (*e.g.*, in the same family or with similar claims) to RE140, also against defendants not including the Petitioner.

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- *ACQIS LLC v. International Business Machines Corp.*, Civil Action No. 6:09-cv-00148 (E.D. Tex. 2009)
  - U.S. Patent No. 6,216,185
  - U.S. Patent No. 6,718,415
  - U.S. Patent No. 7,099,981
  - U.S. Patent No. 7,146,446
  - U.S. Patent No. 7,328,297
  - U.S. Patent No. 7,363,415
  - U.S. Patent No. 7,363,416
  - U.S. Patent No. 7,376,779
- *ACQIS LLC v. International Business Machines Corp.*, Civil Action No. 6:11-cv-00546 (E.D. Tex. 2011)
  - U.S. Patent No. 8,041,873
- *ACQIS LLC v. Alcatel-Lucent USA Inc. et al.*, Civil Action No. 6:13-cv-00638 (E.D. Tex. 2013); *ACQIS LLC v. EMC Corporation*, Civil Action No. 6:13-cv-00639 (E.D. Tex. 2013); *ACQIS LLC v. Ericsson, Inc. et al.*, Civil Action No. 6:13-cv-00640 (E.D. Tex. 2013); *ACQIS LLC v. Huawei Technologies Co., Ltd. et al.*, Civil Action No. 6:13-cv-00641 (E.D. Tex. 2013); and *ACQIS LLC v. EMC Corp.*, Civil Action No. 1:14-cv-13560 (D. Mass. 2014)

Petition for *Inter Partes* Review

U.S. Reissue Patent No. 45,140 (Claims 14-38)

- U.S. Patent No. 7,363,416
- U.S. Patent No. 7,676,624
- U.S. Patent No. 7,818,487
- U.S. Patent No. 8,041,873
- U.S. Reissued Patent No. 41,294
- U.S. Reissued Patent No. 41,961
- U.S. Reissued Patent No. 42,814
- U.S. Reissued Patent No. 42,984
- U.S. Reissued Patent No. 43,119
- U.S. Reissued Patent No. 43,171
- U.S. Reissued Patent No. 44,468
- *ACQIS LLC v. Samsung Electronics Co., Ltd. et al.*, Civil Action No. 2:20-cv-00295 (E.D. Tex. 2020)
  - U.S. Patent No. 8,977,797
  - U.S. Patent No. 9,829,768
  - U.S. Patent No. 9,703,750
  - U.S. Reissued Patent No. 44,654
  - U.S. Reissued Patent No. 45,140
- *ACQIS LLC v. MITAC Holdings Corp. et al.*, Civil Action No. 6:20-cv-00962 (W.D. Tex. 2020)

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U.S. Reissue Patent No. 45,140 (Claims 14-38)

- U.S. Patent No. 8,626,977
  - U.S. Patent No. 8,756,359
  - U.S. Patent No. 8,977,797
  - U.S. Patent No. 9,529,768
  - U.S. Patent No. 9,529,769
  - U.S. Patent No. 9,703,750
  - U.S. Reissued Patent No. 42,984
  - U.S. Reissued Patent No. 43,602
  - U.S. Reissued Patent No. 44,654
  - U.S. Reissued Patent No. 44,739
  - U.S. Reissued Patent No. 45,140
- *ACQIS LLC v. Inventec Corp.*, Civil Action No. 6:20-cv-00965 (W.D. Tex. 2020)
    - U.S. Patent No. 8,756,359
    - U.S. Patent No. 8,977,797
    - U.S. Patent No. 9,529,768
    - U.S. Patent No. 9,703,750
    - U.S. Reissued Patent No. 42,984
    - U.S. Reissued Patent No. 43,602
    - U.S. Reissued Patent No. 44,654

Petition for *Inter Partes* Review  
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- U.S. Reissued Patent No. 44,739
- *ACQIS LLC v. ASUSTeK Computer Inc.*, Civil Action No. 6:20-cv-00966 (W.D. Tex. 2020)
  - U.S. Patent No. 8,626,977
  - U.S. Patent No. 8,756,359
  - U.S. Patent No. 8,977,797
  - U.S. Patent No. 9,529,768
  - U.S. Patent No. 9,529,769
  - U.S. Patent No. 9,703,750
  - U.S. Reissued Patent No. 44,654
  - U.S. Reissued Patent No. 44,739
  - U.S. Reissued Patent No. 45,140
- *ACQIS LLC v. Lenovo Group Ltd. et al.*, Civil Action No. 6:20-cv-00967 (W.D. Tex. 2020)
  - U.S. Patent No. 8,626,977
  - U.S. Patent No. 8,756,359
  - U.S. Patent No. 8,977,797
  - U.S. Patent No. 9,529,768
  - U.S. Patent No. 9,529,769
  - U.S. Patent No. 9,703,750

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- U.S. Reissued Patent No. 44,654
  - U.S. Reissued Patent No. 44,739
  - U.S. Reissued Patent No. 45,140
- *ACQIS LLC v. Wistron Corp. et al.*, Civil Action No. 6:20-cv-00968  
(W.D. Tex. 2020)
  - U.S. Patent No. 7,676,624
  - U.S. Patent No. 8,041,873
  - U.S. Patent No. 8,977,797
  - U.S. Patent No. 9,529,768
  - U.S. Patent No. 9,703,750
  - U.S. Reissued Patent No. 44,468
  - U.S. Reissued Patent No. 44,654
  - U.S. Reissued Patent No. 46,947

EMC has filed IPR petitions for the following patents under the following IPR case numbers:

- IPR2014-01452 against U.S. Reissued Patent No. 43,171
- IPR2014-01462 against U.S. Patent No. 8,041,873
- IPR2014-01469 against U.S. Reissued Patent No. 42,814

Samsung has filed IPR petitions for the following patents under the following IPR case numbers:

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- IPR2021-00666 and IPR2021-00605 against U.S. Patent No. 9,529,768
- IPR2021-00667 and IPR2021-00606 against U.S. Patent No. 8,977,797
- IPR2021-00668 and IPR2021-00604 against U.S. Patent No. 9,703,750
- IPR2021-00669 and IPR2021-00608 against U.S. Reissued Patent No. 44,654
- IPR2021-00670 and IPR2021-00607 against U.S. Reissued Patent No. 45,140

Petitioner has filed or is concurrently filing the following IPR petitions:

- IPR2021-01107, IPR2021-01108, and IPR2021-01109 against U.S. Patent No. 9,529,768
- IPR2021-01110, IPR2021-01111, and IPR2021-01112 against U.S. Patent No. 9,703,750
- IPR2021-01104 and IPR2021-01105 against U.S. Patent No. 8,977,797

**B. Real Parties-in-Interest**

Petitioner identifies itself as a real party-in-interest. Petitioner also identifies Lenovo Group Ltd.; Lenovo PC HK Limited; LCFC (HEFEI) Electronics Technology Co., Ltd.; Lenovo Information Products (Shenzhen) Co., Ltd.; Lenovo (Beijing) Information Technology Ltd.; and Lenovo Centro Tecnológico S. de R.L. de C.V. as additional real parties-in-interest (“RPIs”).



**C. Counsel**

Petitioner is filing a power of attorney appointing the practitioners associated with Customer Number 132,593. Petitioner designates the following lead and back-up counsel:

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**D. Service Information (37 C.F.R. § 42.8(b)(4))**

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### **III. Fees**

Petitioner concurrently submits required fees for this Petition. The Board is authorized to charge Desmarais LLP's deposit account, No. 50-6822, for any fee deficiency.

### **IV. Grounds for Standing**

Petitioner certifies that RE140 is available for IPR and that Petitioner is not estopped or barred from requesting IPR.

### **V. Identification of Challenge and Relief Requested**

#### **A. Identification of Prior Art**

The following references are pertinent to the grounds of unpatentability explained below:

1. U.S. Patent No. 6,345,330 ("Chu330" (Ex-1003)), issued on February 5, 2002, is prior art under 35 U.S.C. § 102(b).<sup>1</sup>

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<sup>1</sup> Because RE140 is, at best, entitled to a priority date of June 17, 2011 (as explained more fully below), the pre-AIA (America Invents Act) statutory framework applies.

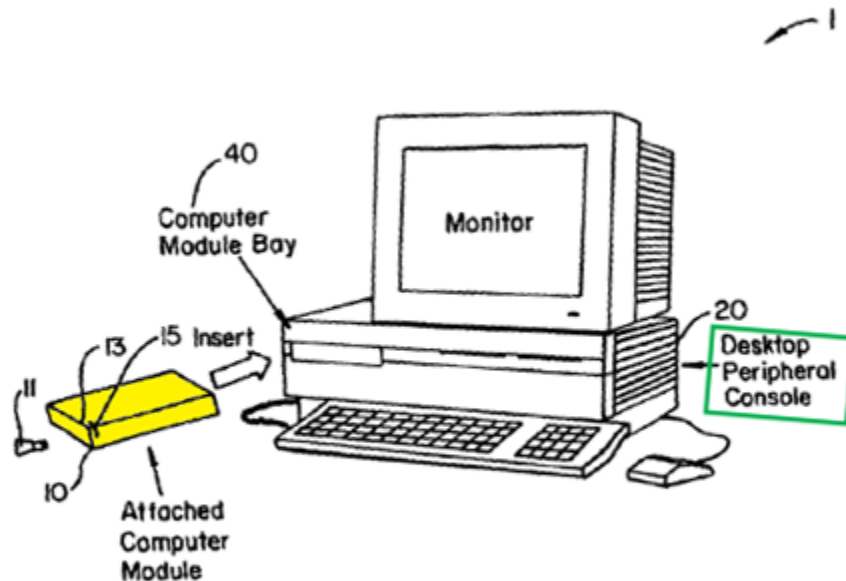
2. U.S. Patent Publication No. 2003/0135771 (“Cupps” (Ex-1004)), published on July 17, 2003, is prior art under at least 35 U.S.C. § 102(b).

### **B. Statutory Grounds of Unpatentability**

Petitioner requests IPR and cancellation of claims 14-38 of RE140 under 35 U.S.C. § 103. This Petition demonstrates that there is a reasonable likelihood that Petitioner will prevail with respect to cancellation of at least one challenged claim. *See* 35 U.S.C. § 314(a).

## **VI. Overview of RE140**

RE140 describes a computer system that includes an attached computer module (“ACM”) and a **peripheral console** (“PCON”). Ex-1001, Figure 1, 13.



**FIG. 1**

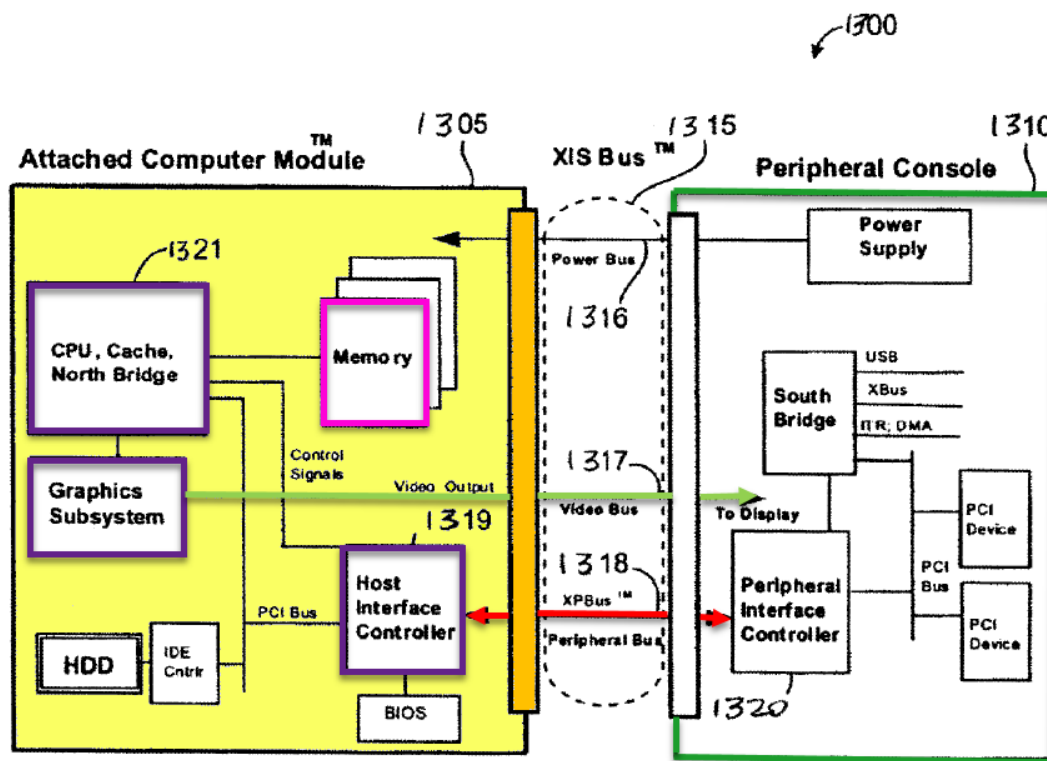


FIG. 13

## ACM

The **ACM** can be inserted into the **PCON**. Ex-1001, 3:51-53, 3:62-64. The **ACM** includes a **central processing unit** (“**CPU**”), a **graphics subsystem**, and a **host interface controller** (“**HIC**”). As shown below in Figure 20 of RE140, certain components, such as the **CPU**, the **graphics subsystem** and the **HIC**, can be integrated together. See Ex-1001, 19:10-13; see also *id.*, Figure 19, 19:3-18.

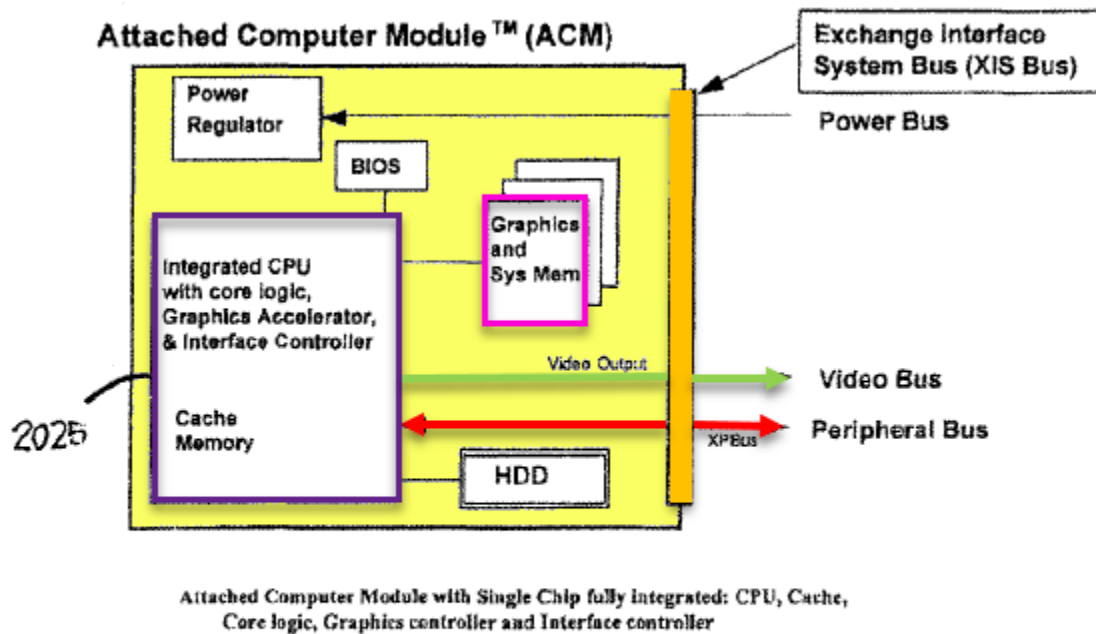
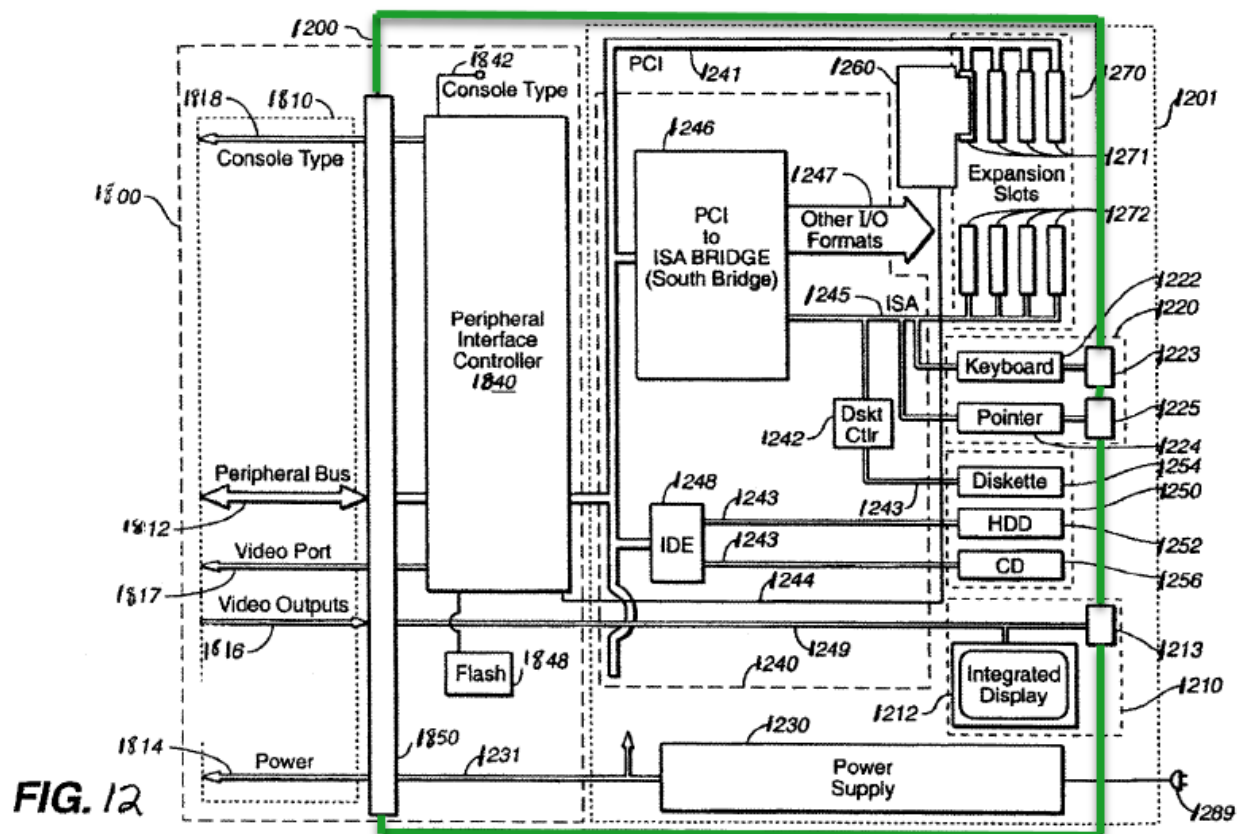


FIG. 20

### Peripheral Console

The **PCON** can have a number of connected components (e.g., mass storage, display). See Ex-1001, 14:62-15:9, 16:23-35. Specifically, the “**PCON** ... [also] comprises a Peripheral Interface Controller (PIC) component 1840 [and] a PCON connector component 1850.” Ex-1001, 16:36-38.



### Communications Interface Between ACM and Peripheral Console

The **HIC** in the **ACM** and the PIC in the **PCON** form a communication interface. Specifically, as shown in Figure 13, “[t]he **ACM 1305** and the **peripheral console 1310** are interfaced through an exchange interface system (XIS) bus 1315” which “includes power bus 1316, **video bus 1317** and **peripheral bus (XPBus) 1318**.” Ex-1001, 18:46-51.

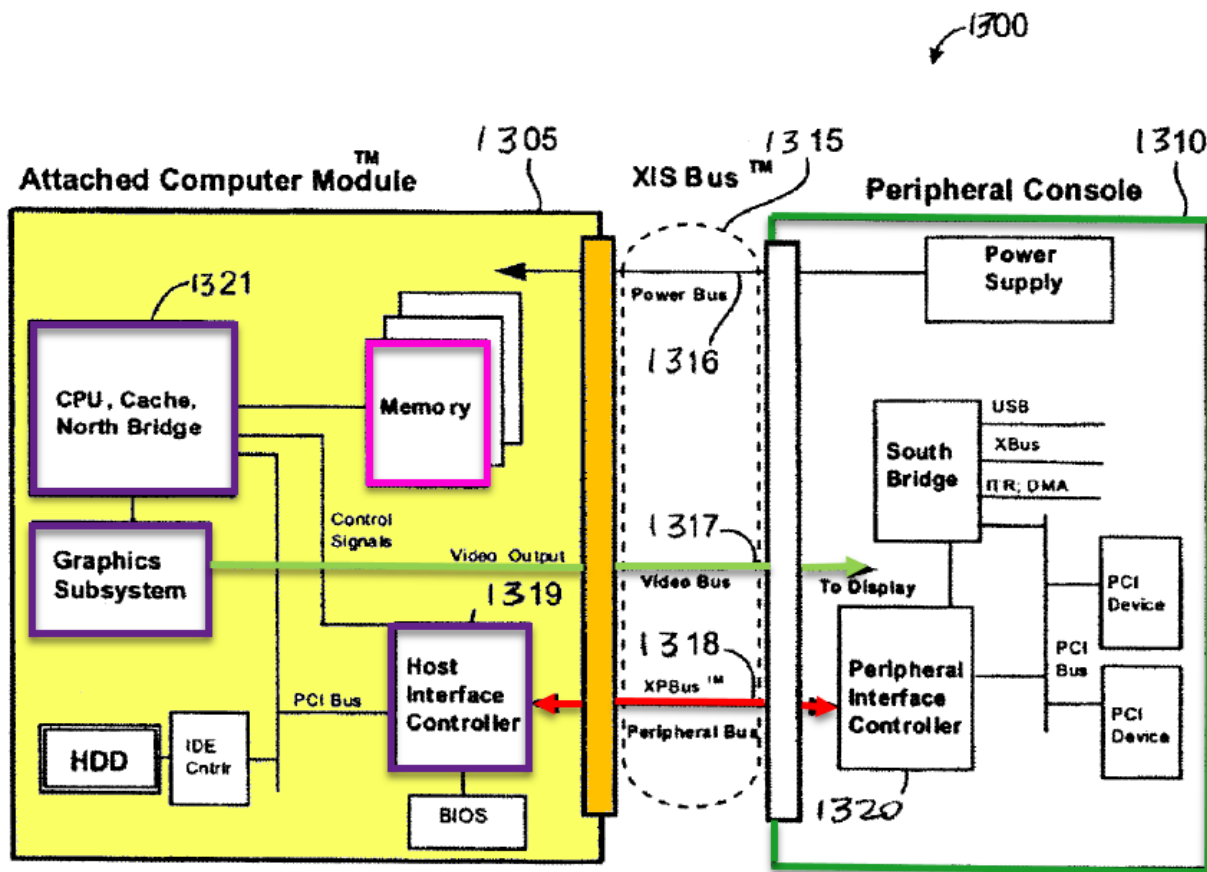


FIG. 13

“**Video bus 1317** transmits video signals between the **ACM 1305** and the **peripheral console 1310** ... such as ... Transition Minimized Differential Signaling (TMDS) signals for flat panel displays.” Ex-1001, 18:54-61.

Local PCI bus transactions are encoded and serialized for transmission over the **XPBus**. See, e.g., Ex-1001, 19:46-49 (“Encoders ... format the PCI address/data bits to a form more suitable for parallel to serial conversion prior to transmittal on the **XPBus**.”). The XPBus includes two sets of unidirectional lines. See Ex-1001,

20:34-42. RE140 explains that “although each of the lines **PCK, PD0 to PD3, PCN, PCKR, PDR0 to PDR3, and PCNR** is referred to as a line, in the singular rather than plural, each such line may contain more than one physical line.” Ex-1001, 20:54-57. The first set of unidirectional lines **PCK, PD0 to PD3, and PCN** are differential signal pairs, as illustrated below in Figure 16. Ex-1001, 20:14-18 (“These lines are *unidirectional LVDS lines* for transmitting clock signals and bits from the HIC to the PIC. The bits on the **PD0 to PD3 and the PCN** lines are sent synchronously within every clock cycle of the **PCK**.”).

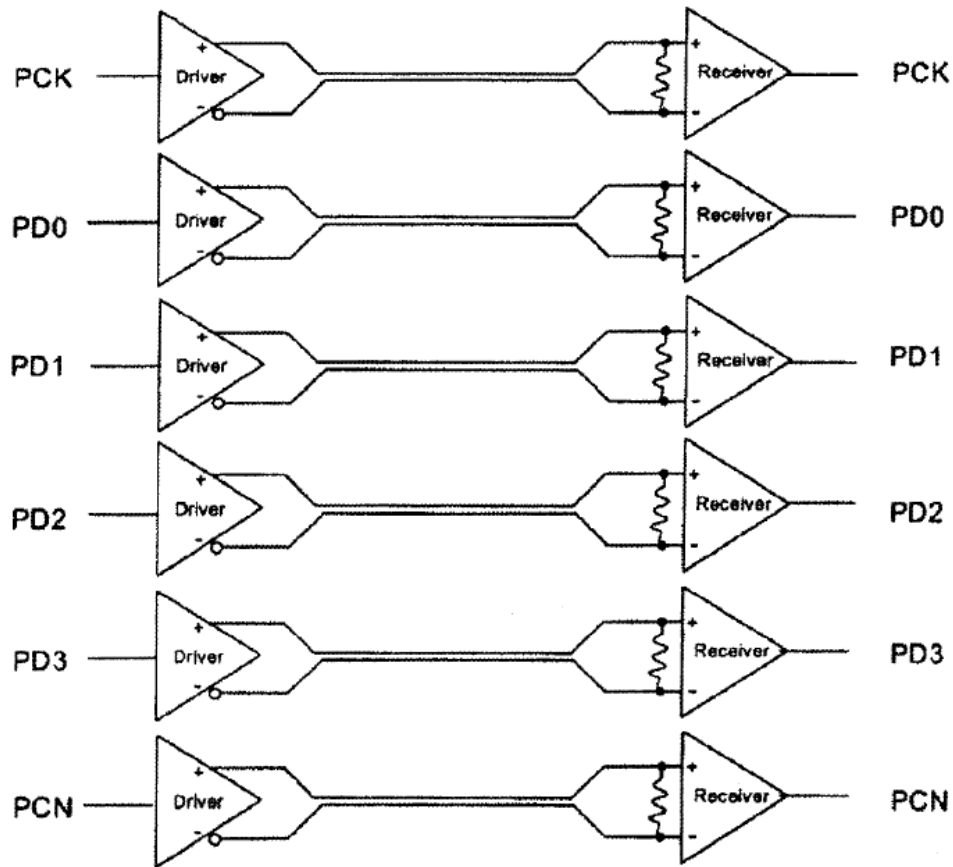


FIG. 16



The second “set of lines, namely **PCKR, PDR0 to PDR3, and PCNR** [not shown in Figure 16] ... are used to transmit clock signals and bits from the PIC to HIC. The lines used for transmitting information from the PIC to the HIC have the same structure as those shown in FIG. 16, except that they transmit data in a direction opposite to that in which the lines shown in FIG. 16 transmit data.” Ex-1001, 20:18-24.

In addition to encoded PCI bus transactions (*e.g.*, **XX00** and **XX10** indicating a first or second segment of PCI address/data, respectively), reserved data packets (*e.g.*, **0011** or **1011**) purportedly can be used to transmit non-PCI bus transactions (*e.g.*, “USB transactions”). *See* Ex-1001, 21:24-25.

ID bits (P0 P1 P2 P3)	Data Packet Type
<b>XX00</b>	PCI 1st address/data segment
<b>XX10</b>	PCI 2nd address/data segment
<b>0001</b>	Control 1st segment with PCI response
<b>1001</b>	Control 1st segment without PCI response
<b>0101</b>	Control 2nd segment with PCI response
<b>1101</b>	Control 2nd segment without PCI response
<b>0011</b>	Reserved
<b>1011</b>	Reserved
<b>0111</b>	Initialization
<b>1111</b>	NOOP

FIG. 24

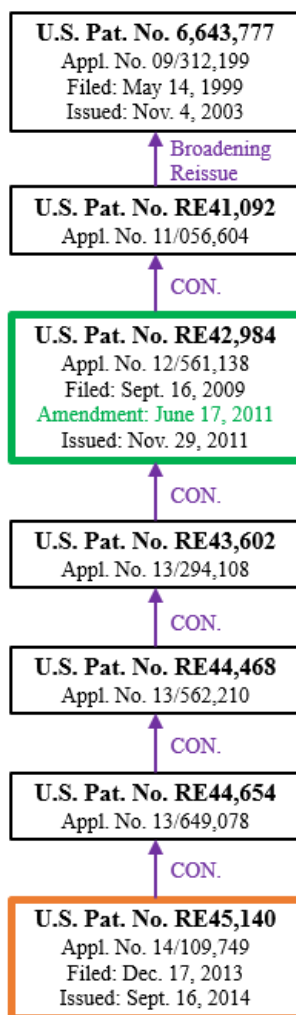
## VII. RE140 Is Not Entitled To A Priority Date Before June 17, 2011

ACQIS filed RE140 on December 17, 2013, claiming priority to U.S. Patent No. 6,643,777 (“Chu777” (Ex-1007)), filed on May 14, 1999, through a series of

Petition for *Inter Partes* Review

U.S. Reissue Patent No. 45,140 (Claims 14-38)

reissue continuations. Ex-1001, Cover, 1:11-31. The related patents to RE140 are illustrated in the patent family tree below:



As more fully explained below, RE140 is, at best, entitled to a priority date only as to the date new matter was added into U.S. Reissued Patent No. 42,984 (“RE984” (Ex-1008))—June 17, 2011.<sup>2</sup>

**A. RE140 Claims Recite Limitations Not Supported By Parent Applications That Precede RE984**

The challenged claims of RE140 recite the following limitations:

- “Integrated CPU/graphics” limitations:
  - claims 14-34: “an integrated ... (CPU) with a graphics controller in a single chip,” and
  - claims 35-38: “an integrated ... (CPU) and graphics controller in a single chip.”
- “CPU-LVDS” limitations:
  - claims 17 and 19-20: “connecting a second LVDS channel directly to the integrated CPU and graphics controller, the second LVDS channel comprising two unidirectional, serial bit channels that transmit data in opposite directions,”

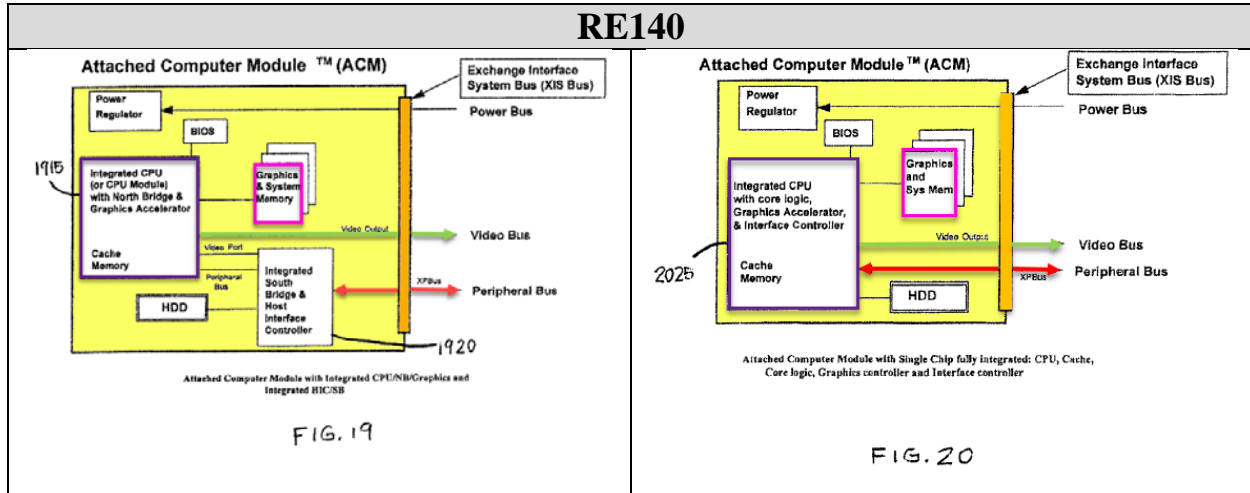
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<sup>2</sup> Petitioner and RPIs do not concede that each of the claims of RE140 is supported by RE140 under 35 U.S.C. § 112.

- claims 22-25 and 35-38: “connecting a first ... (LVDS) channel directly to the integrated CPU and graphics controller, wherein the [first] LVDS channel comprises two unidirectional, serial bit channels that transmit data in opposite directions,” and
- claims 26-34: “connecting a ... (LVDS) channel directly to the integrated CPU and graphics controller, wherein the LVDS channel comprises two unidirectional, serial bit channels that transmit data in opposite directions.”

Figures 19-20 of RE140 and the associated descriptions are the *only* arguable support for the “integrated CPU/graphics” limitations. *See, e.g.*, Ex-1001, 19:8-13 (“FIG. 19 shows an attached computer module with *integrated CPU/NB/Graphics* 1915 and Integrated HIC/SB 1920. FIG. 20 shows an attached computer module with *single chip 2025 fully integrated: CPU*, Cache, Core Logic, *Graphics controller* and Interface controller.”).

Figure 20 and the associated description is the *only* arguable support for the “CPU-LVDS” limitations. *See* Ex-1001, Figure 20 (showing the “direct” connection).



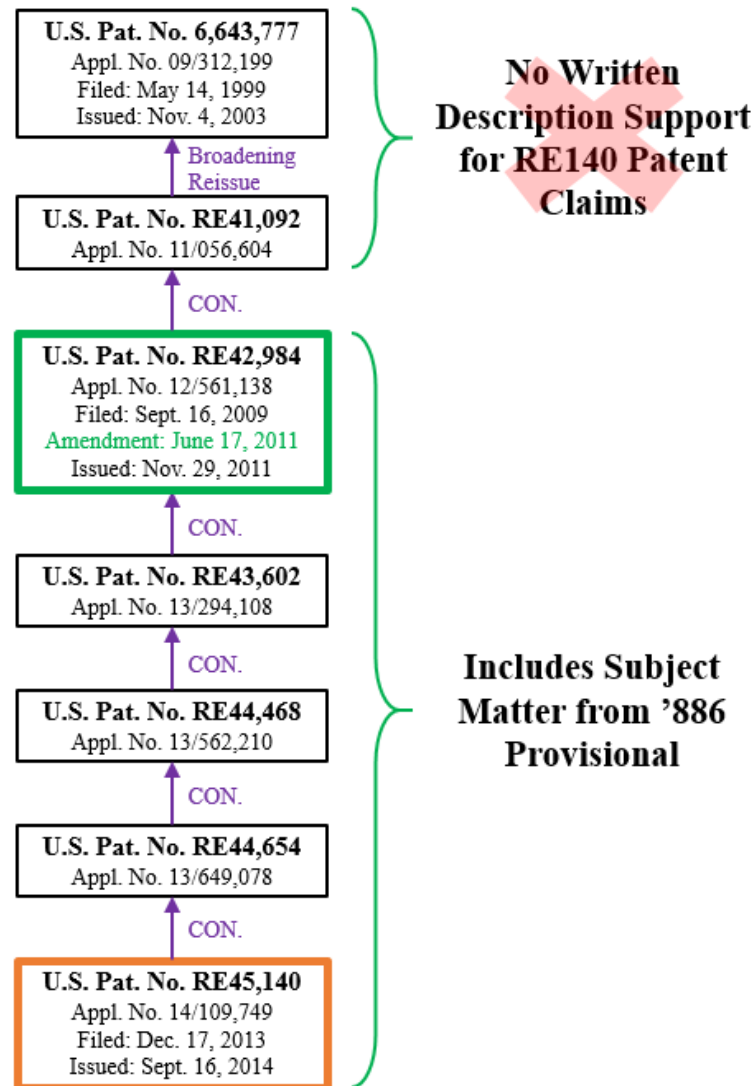
The table below summarizes the specific figures (and their associated description) that arguably support the challenged claims.

<b>Integrated CPU/graphics</b>	<b>CPU-LVDS</b>	<b>Purported Support</b>
<b>14-16</b>		FIGS. 19-20
<b>17</b>	<b>17</b>	FIG. 20
<b>18</b>		FIGS. 19-20
<b>19-20</b>	<b>19-20</b>	FIG. 20
<b>21</b>		FIGS. 19-20
<b>22-25</b>	<b>22-25</b>	FIG. 20
<b>26-29</b>	<b>26-29</b>	FIG. 20
<b>30-34</b>	<b>30-34</b>	FIG. 20
<b>35-38</b>	<b>35-38</b>	FIG. 20

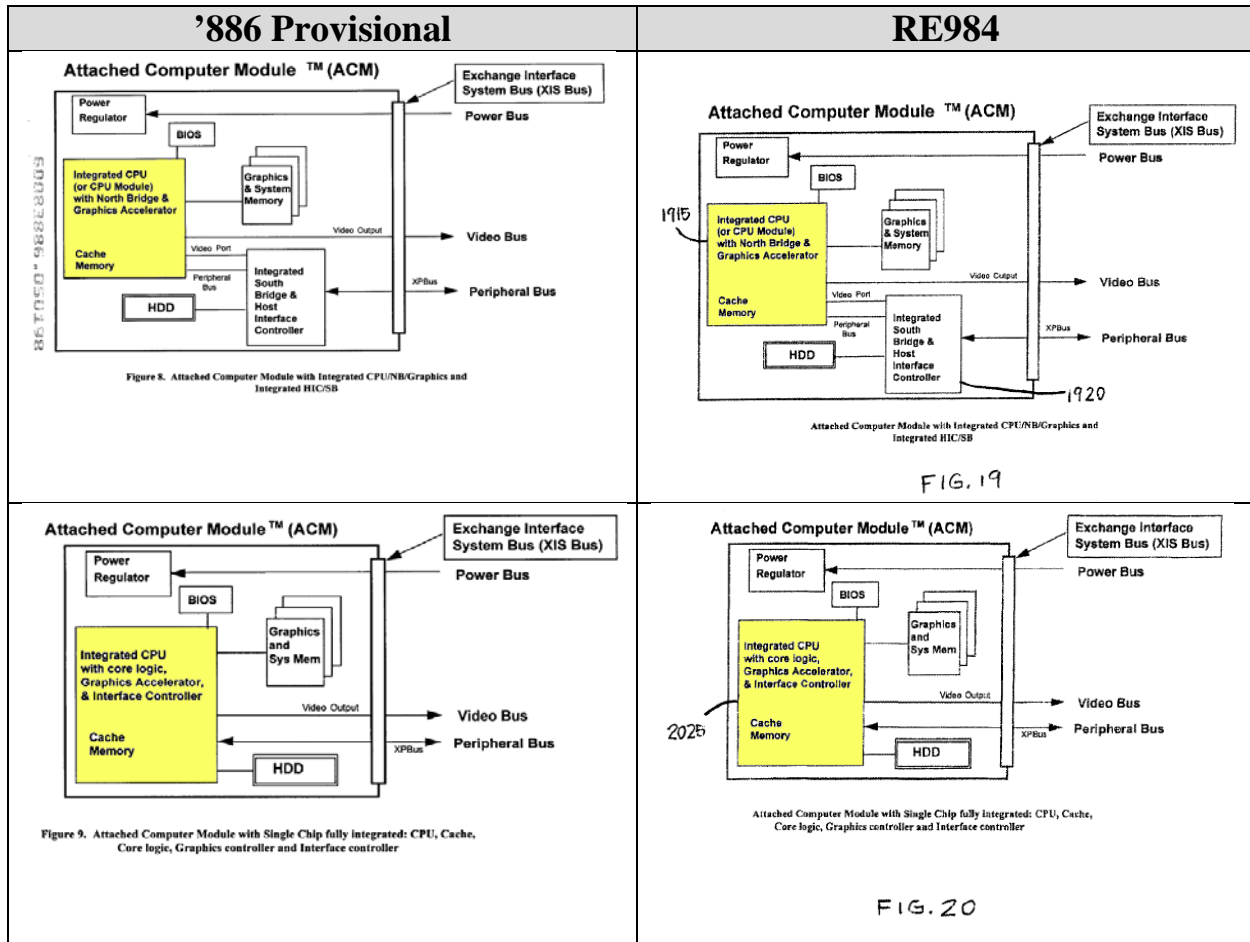
**1. The Purported Written Description Support For The “Integrated CPU/Graphics” And “CPU-LVDS” Limitations Was First Introduced In RE984**

RE140’s purported written description support for the “integrated CPU/graphics” and “CPU-LVDS” limitations was not disclosed in the parent applications that precede RE984. *See generally* Ex-1007, Ex-1013.

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The purported written description support for the “integrated CPU/graphics” and “CPU-LVDS” limitations (*i.e.*, Figures 19-20 and associated descriptions) was added to the specification for the first time in the intervening RE984 on June 17, 2011, as illustrated above in green. *See* Ex-1009 [RE984 FH], 344-377.



As alleged support, ACQIS relied on U.S. Provisional Application No. 60/083,886 (the “’886 Provisional”) (Ex-1010), implicitly admitting that the subject matter for Figures 19-20 was not present in any of the parent applications that preceded RE984. *See* Ex-1009 [RE984 FH], 363 (“[T]he subject application is amended to add new Fig[s]. [19-20] as well as accompanying text [which] corresponds to ... figure 8 and figure 9 of the ’886 provisional application [and] the text of the ’886 provisional application as originally included in legends of figure 8 and figure 9.”).

**B. RE984 Introduced Subject Matter Not Found In Its Parent Applications**

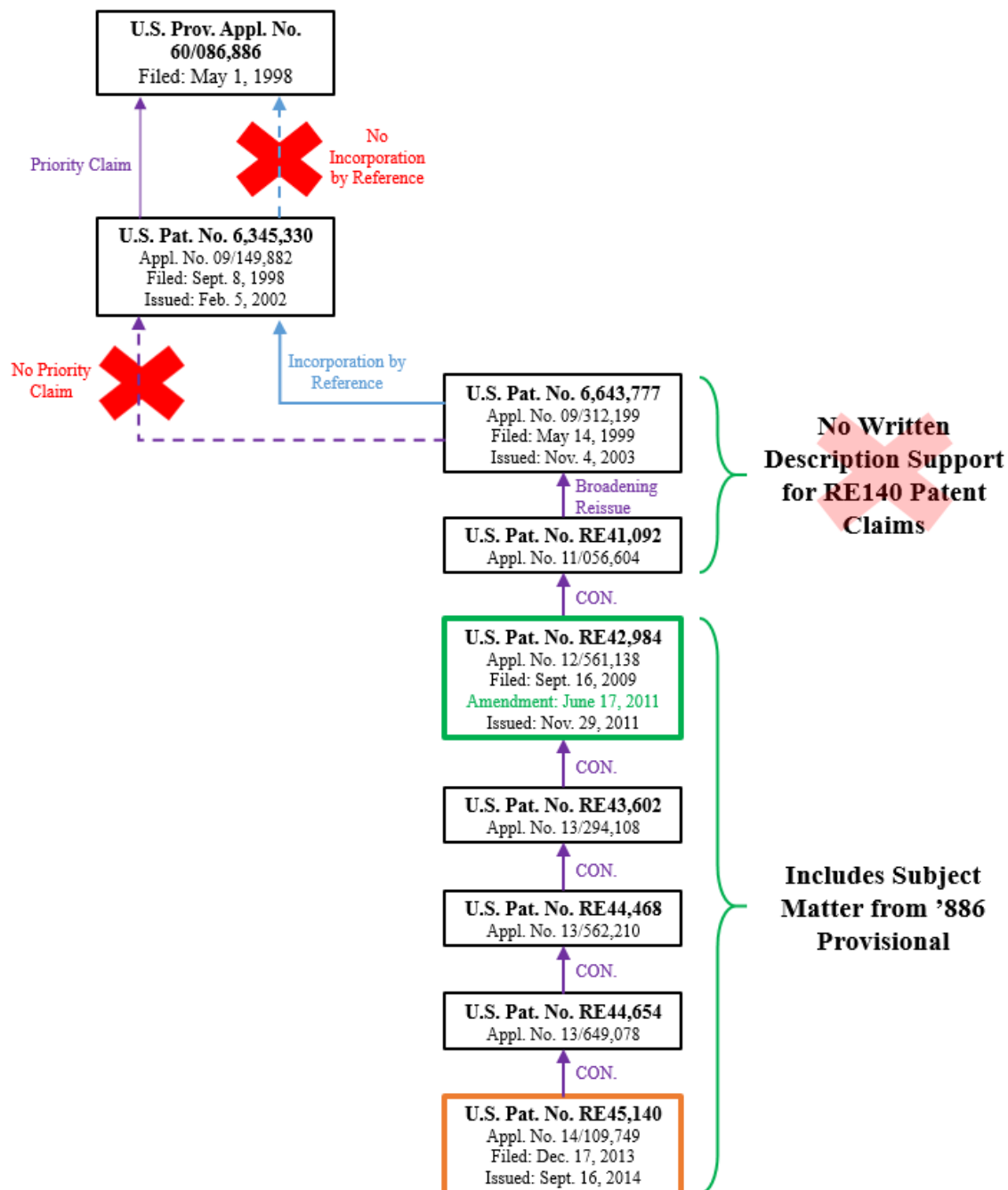
The amendments that introduced Figures 19-20 and associated disclosure to RE984 added new matter, because none of RE984's parent applications properly incorporated by reference the '886 Provisional. As illustrated below, although the Chu777 *incorporated by reference* Chu330<sup>3</sup> (without claiming *priority*), Chu330 never *incorporated by reference* the '886 Provisional. Chu330 merely claimed *priority* to the '886 Provisional.

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<sup>3</sup> See Ex-1007, 5:9-13.



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1. **Materials Incorporated By Reference Must Be Identified  
“With Detailed Particularity” and “Specific[ity]”**

“Incorporation by reference provides a method for integrating material from various documents into a host document ... by citing such material in a manner that

makes clear that the material is effectively part of the host document as if it were explicitly contained therein.” *Zenon Envtl., Inc. v. U.S. Filter*, 506 F.3d 1370, 1378 (Fed. Cir. 2007).

“To incorporate material by reference, the host document must identify ***with detailed particularity*** what ***specific*** material it incorporates and clearly indicate where that material is found in the various documents.” *Droplets, Inc. v. E\*Trade Bank*, 887 F.3d 1309, 1318 (Fed. Cir. 2018). The incorporation by reference is proper only if the host document “identif[ies] ***with detailed particularity*** what specific material it incorporates ***to a person of ordinary skill***” and “directly lead[s] one of ordinary skill” to the document that the patent-drafter intended to be incorporated. *Hollmer v. Harari*, 681 F.3d 1351, 1357 (Fed. Cir. 2012).<sup>4</sup> “[A]mbiguity in incorporation does not suffice.” *Id.*, 1358.

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<sup>4</sup> The reasonable examiner standard does not apply to the analysis of RE140’s priority chain because these patents have issued. See *Harari v. Hollmer* (“*Harari I*”), 602 F.3d 1348 (Fed. Cir. 2010); *Hollmer*, 681 F.3d, 1356 (“Because *Harari I* did ‘not involve an issued patent or language that is intended to appear in an issued patent,’ we held that the proper inquiry focused on the reasonable examiner, not the person of ordinary skill.”) (*quoting Harari I*, 602 F.3d, 1353 n.2). Instead, the reasonable examiner standard applies in “narrow circumstances ... when an

**2. RE984's Parent Applications Never Incorporated By Reference the '886 Provisional**

Chu330 never incorporated by reference the '886 Provisional, much less so “with detailed particularity.” *Hollmer*, 681 F.3d, 1357. In adding Figures 19 and 20 and associated disclosure to RE984, ACQIS alleged that a “checked incorporation by reference box” in a transmittal form was sufficient to incorporate the '886 Provisional into Chu330. *See* Ex-1009, 363.

The checked box in the transmittal form, however, does not identify the '886 Provisional:

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application is at the initial filing stage and the examiner is evaluating an amendment that clarifies ambiguous incorporation by reference language.” *Hollmer*, 681 F.3d, 1357.

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APPLICATION ELEMENTS <small>See MPEP chapter 600 concerning utility patent application contents.</small>	ADDRESS TO: Assistant Commissioner for Patents Box Patent Application Washington, DC 20231
<p>1. <input checked="" type="checkbox"/> Fee Transmittal Form <i>(Submit an original, and a duplicate for fee processing)</i></p> <p>2. <input checked="" type="checkbox"/> Specification [Total Pages <input type="text" value="45"/> ] <i>(preferred arrangement set forth below)</i></p> <ul style="list-style-type: none"> <li>- Descriptive title of the Invention</li> <li>- Cross References to Related Applications</li> <li>- Statement Regarding Fed sponsored R &amp; D</li> <li>- Reference to Microfiche Appendix</li> <li>- Background of the Invention</li> <li>- Brief Summary of the Invention</li> <li>- Brief Description of the Drawings <i>(if filed)</i></li> <li>- Detailed Description</li> <li>- Claim(s)</li> <li>- Abstract of the Disclosure</li> </ul> <p>3. <input checked="" type="checkbox"/> Drawing(s) (35 USC 113) [Total Sheets <input type="text" value="57"/> ]</p> <p>4. <input type="checkbox"/> Oath or Declaration [Total Pages <input type="text" value="1"/> ]</p> <ul style="list-style-type: none"> <li>a. <input type="checkbox"/> Newly executed (original or copy)</li> <li>b. <input type="checkbox"/> Copy from a prior application (37 CFR 1.63(d) <i>(for continuation/divisional with Box 17 completed)</i> <i>[Note Box 5 below]</i></li> <li>i. <input type="checkbox"/> DELETION OF INVENTOR(S) <small>Signed statement attached deleting inventor(s) named in the prior application, see 37 CFR 1.63(d)(2) and 1.33(b)</small></li> </ul> <p>5. <input checked="" type="checkbox"/> Incorporation By Reference <i>(useable if Box 4b is checked)</i> The entire disclosure of the prior application, from which a copy of the oath or declaration is supplied under Box 4b, is considered as being part of the disclosure of the accompanying application and is hereby incorporated by reference therein.</p>	<p>6. <input type="checkbox"/> Microfiche Computer Program <i>(Appendix)</i></p> <p>7. <input type="checkbox"/> Nucleotide and/or Amino Acid Sequence Submission <i>(if applicable, all necessary)</i></p> <ul style="list-style-type: none"> <li>a. <input type="checkbox"/> Computer Readable Copy</li> <li>b. <input type="checkbox"/> Paper Copy (identical to computer copy)</li> <li>c. <input type="checkbox"/> Statement verifying identity of above copies</li> </ul>
ACCOMPANYING APPLICATION PARTS	
<p>8. <input type="checkbox"/> Assignment Papers (cover sheet &amp; document(s))</p> <p>9. <input type="checkbox"/> 37 CFR 3.73(b) Statement <input type="checkbox"/> Power of Attorney <i>(when there is an assignee)</i></p> <p>10. <input type="checkbox"/> English Translation Document <i>(if applicable)</i></p> <p>11. <input type="checkbox"/> Information Disclosure Statement (IDS)/PTO-1449 <input type="checkbox"/> Copies of IDS Citations</p> <p>12. <input type="checkbox"/> Preliminary Amendment</p> <p>13. <input checked="" type="checkbox"/> Return Receipt Postcard (MPEP 503) <i>(Should be specifically itemized)</i></p> <p>14. <input type="checkbox"/> Small Entity Statement(s) <input type="checkbox"/> Statement filed in prior application, Status still proper and desired</p> <p>15. <input type="checkbox"/> Certified Copy of Priority Document(s) <i>(if foreign priority is claimed)</i></p> <p>16. <input type="checkbox"/> .....</p>	
<p>17. If a CONTINUING APPLICATION, check appropriate box and supply the requisite information:</p> <p><input type="checkbox"/> Continuation    <input type="checkbox"/> Divisional    <input type="checkbox"/> Continuation-in-part (CIP) of prior application No: _____</p>	

Ex-1011 [Chu330 FH], 81.<sup>5</sup> Nothing in the transmittal form “identif[ies] with *detailed particularity* what specific material [Chu330] incorporates[.]” *Hollmer*, 681 F.3d, 1357. *See* Ex-1002, ¶¶70-72.

<sup>5</sup> Additionally, the box 5 titled “Incorporation By Reference” states that it is only “useable if Box 4b is checked[.]” (*id.*), but as seen above, Box 4b is not even checked. Even if Box 4b were checked, Box 4b would have been inoperative

Even if the transmittal form of Chu330 included a statement that purportedly incorporated by reference the '886 Provisional—which it did not—that statement would be inoperative because a person of ordinary skill's analysis of what a patent incorporates is limited to the four corners of the patent itself. *Advanced Display System, Inc. v. Kent State University*, 212 F.3d 1272, 1282 (Fed. Cir. 2000) (“[t]o incorporate by reference, the *host document*<sup>6</sup> *must identify* with detailed particularity what specific material it incorporates”). Indeed, a person of ordinary

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because its use was limited “for continuation/divisional with box 17 completed.” *Id.* Again, none of the options for Box 17 includes a check mark—let alone that Chu330 cannot be a “continuation/divisional” of the '**886 Provisional**.

<sup>6</sup> Host document refers to *a patent or printed publication*—not the file history. *See Advanced Display System, Inc. v. Kent State University*, 212 F.3d 1272, 1282 (Fed. Cir. 2000) (“Incorporation by reference provides a method for integrating material from various documents into *a host document—a patent or printed publication* in an anticipation determination—by citing such material in a manner that makes clear that the material is effectively part of the host document as if it were explicitly contained therein”); *see also Hollmer*, 681 F.3d, 1358 (“The incorporation by reference analysis, therefore, is similarly constrained by the *four corners of the application.*”).

skill would not have known if a patent incorporates another document based on a statement buried in a transmittal form. Accordingly, any incorporation by reference statement must have appeared in Chu330 itself. *See* MPEP 608.01(p) (“provid[ing] the public with a **patent disclosure** which minimizes the public’s burden to search for and obtain copies of documents incorporated by reference which may not be readily available.”). Ex-1002, ¶¶70-72.

Nothing in Chu330’s specification could be considered as an adequate incorporation by reference of the ’886 Provisional. In the first paragraph, Chu330 states:

***This application claims any and all benefits as provided by law of U.S. Provisional Application No. 60/083,886 filed May 1, 1998 and of U.S. Provisional Application No. 60/092,706 filed on Jul 14, 1998.***

Ex-1003, 1:7-10. This statement is at best a priority claim to the ’886 Provisional that is distinct from an incorporation by reference. *See In re Seversky*, 474 F.2d 671, 674 (CCPA 1973) (“a mere *reference* to another application, or patent, or publication is not an *incorporation* of anything therein into the application containing such reference for the purposes of the disclosure required by 35 U.S.C. § 112.”). When ACQIS meant to incorporate by reference another document, it did so expressly, such as by stating “[t]his application is being filed concurrently with the application ... [for Chu185] and ***incorporates the material therein by reference.***”

Ex-1003, 1:11-15. ACQIS's failure to include an express statement that incorporates by reference the '886 Provisional cannot be excused. *Hollmer*, 681 F.3d, 1357 ("Patent draftsmanship is an exacting art, and no less care is required in drafting an incorporation by reference statement than in any other aspect of a patent application.") (internal quotations omitted).

For these reasons, Chu330 does not incorporate by reference the '886 Provisional. Accordingly, the material amended into the application of RE984 from the '886 Provisional (corresponding portions highlighted in pink in Ex-1019 of RE140) constitutes new matter relative to the prior applications. *See* Ex-1002, ¶¶57-73.

**C. The Challenged Claims Are Not Entitled To A Priority Date Earlier Than June 17, 2011**

Since Figures 19-20 and their associated disclosures, which purportedly provide written description support for the "integrated CPU/graphics" and "CPU-LVDS" limitations, were only added to RE984 on June 17, 2011, the challenged claims are not entitled to a priority date earlier than the date the new matter was added (*i.e.*, June 17, 2011).<sup>7</sup> Even if ACQIS somehow improperly argues that the

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<sup>7</sup> Although information which is well known need not be described in detail in the specification, sufficient information must nevertheless be provided to show that the

claims are entitled to a priority date as of the filing date of RE984 (*i.e.*, September 16, 2009), prior art relied on in this Petition all precede this date.

### **VIII. Prosecution History of RE140**

During prosecution of RE140, claims 14-38 were rejected under the judicially created doctrine of obviousness-type double patenting. Ex-1006, 203. In response, ACQIS filed a terminal disclaimer. *See* Ex-1006, 230-232, 237-38. The Examiner then allowed the claims of RE140. *See* Ex-1006, 239-245.

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inventor had possession of the invention as claimed. “[I]t is the specification itself that must demonstrate possession. ... [A] description that merely renders the invention obvious does not satisfy the [written description] requirement[.]” *Ariad Pharms., Inc. v. Eli Lilly & Co.*, 598 F.3d 1336, 1352 (Fed. Cir. 2010). *See also Auto. Techs. Int’l, Inc. v. BMW of N. Am., Inc.*, 501 F.3d 1274, 1283 (Fed. Cir. 2007) (“It is the specification, not the knowledge of one skilled in the art, that must supply the novel aspects of an invention”) (*quoting Genentech, Inc. v. Novo Nordisk A/S*, 108 F.3d 1361, 1366, (Fed. Cir. 1997)). The patentee “cannot simply rely on the knowledge of a [POSITA] to serve as a substitute for the missing information in the specification.” *ALZA Corp. v. Andrx Pharms., LLC*, 603 F.3d 935, 941 (Fed. Cir. 2010).



## **IX. Level of Ordinary Skill in the Art**

A person of ordinary skill in the art (“POSITA”) as of the June 17, 2011 priority date of the challenged claims of RE140 would have had a Bachelor of Science or equivalent degree in Computer Science or Electrical Engineering and two years of graduate work, work experience, or the equivalent in computer systems, interfaces, and architecture. Further, additional education could make up for less practical experience, and vice versa.

## **X. Claim Construction**

As explained above in Section II.A [Related Matters], ACQIS has asserted many patents against numerous entities. Below is a summary of the claim terms that appear in the challenged claims, which have been construed in these earlier proceedings (*i.e.*, 6:09-cv-00148, 6:13-cv-00638 to -00641, 1:14-cv-13560, IPR2014-01452, IPR2014-01462, IPR2014-01469).

<b>Claim Term</b>	<b>Adopted/Agreed Construction</b>
“console”	a chassis that connects several components of the computer system
“serial bit channel”	a path on which units of information are transferred serially from one component to another
“LVDS”	a signal represented by the difference in voltage between two lines, where the difference in voltage is low

<b>Claim Term</b>	<b>Adopted/Agreed Construction</b>
“differential signal channel”	a channel for carrying a signal, the signal being represented by the difference in voltage between two lines
“Peripheral Component Interconnect (PCI) bus”	industry standard computer bus known as Peripheral Component Interconnect Local Bus
“Peripheral Component Interconnect (PCI) bus transaction”	information/transaction, in accordance with the PCI standard, for communication with an interconnected peripheral component  OR  a transaction, in accordance with the industry standard PCI Local Bus Specification, for communication with an interconnected peripheral component  OR  PCI industry standard bus transaction
“encoded ... Peripheral Component Interconnect (PCI) bus transaction”	code representing a PCI bus transaction
“encoded ... serial bit stream of Peripheral Component (PCI) bus transaction” and related terms <sup>8</sup>	a PCI bus transaction that has been serialized from a parallel form

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<sup>8</sup> Related terms refer to claim terms that recite “data of a ‘PCI bus transaction’ [that] has been ‘serialized,’ transmitted in ‘serial form’ or transmitted over ‘serial bit channels.’” Ex-1022 [EMC Opening Markman Brief], 15-16.

In an IPR proceeding, terms should be afforded the ordinary and customary meaning, *see* 37 C.F.R. §42.100(b), but only need to be construed when necessary to determine patentability. *See Vivid Techs., Inc. v, Am. Sci. & Eng'g, Inc.*, 200 F.3d 795, 803 (Fed. Cir. 1999). Here, there is no need to apply these constructions because regardless of whether the Board adopts these constructions, Chu330 provide nearly the identical disclosure as RE140.<sup>9</sup>

## **XI. Specific Grounds for Challenge**

This petition presents the following Grounds of invalidity of challenged claims:

<b>Grounds</b>	<b>Claims</b>	<b>Statutory Ground</b>	<b>Prior Art Reference(s)</b>
I	14-38	§103	Chu330, Cupps

The sections below, as supported by the Declaration of Dr. Lin, demonstrate how the challenged claims are unpatentable. *See* 37 C.F.R. 42.104(b)(4)-(5).

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<sup>9</sup> Petitioner/RPIs reserve all rights to raise claim construction arguments and other arguments in any parallel or future litigation.

**A. Ground I: Chu330 in combination with Cupps Renders Obvious Claims 14-38**

**1. Prior Art**

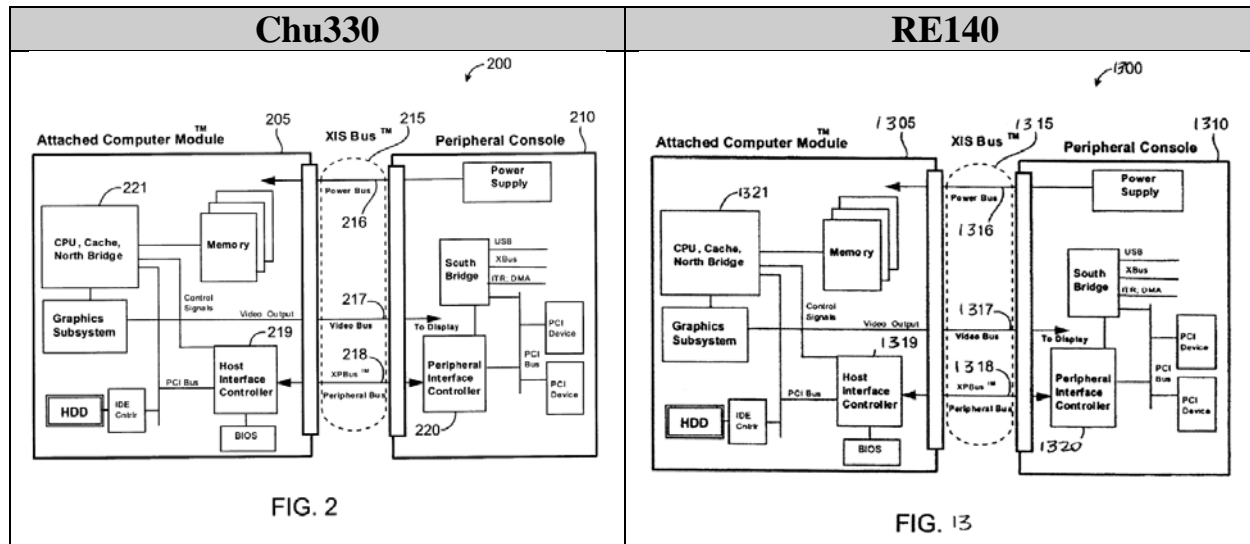
**i. Chu330**

Chu330 was filed on September 8, 1998, more than 8 months prior to the earliest claimed priority date of RE140 (*i.e.*, May 14, 1999 based on Chu777's filing date), and published more than a year before the priority date afforded to RE140 (*i.e.*, June 17, 2011). Chu330 incorporates by reference U.S. Patent No. 6,216,185 ("Chu185"), noting that additional details of the ACM and the PCON can be found in Chu185. *See* Ex-1003, 1:11-15, 1:54-62, 6:1-7. Accordingly, the teachings of Chu185 can be relied on as part of Chu330. *See Advanced Display Sys., Inc. v. Kent State Univ.*, 212 F.3d 1272, 1282 (Fed. Cir. 2000) ("Material ... may still be considered for purposes of anticipation if that material is incorporated by reference into the document.").

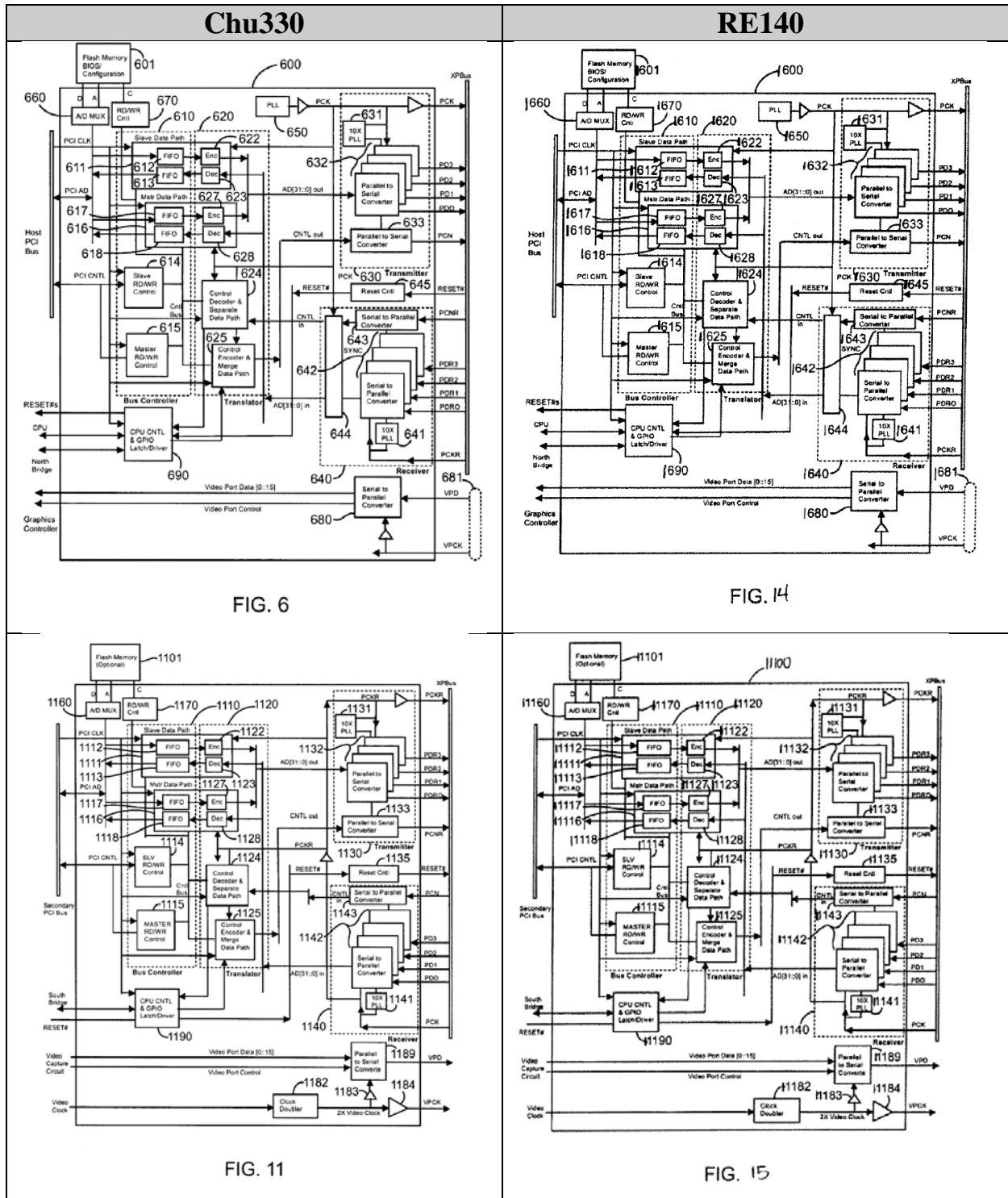
RE140 incorporates by reference Chu330 and Chu185. *See* Ex-1001, 5:67-6:4. In fact, large portions of Chu330 and Chu185 explicitly appear as part of the disclosure of RE140 because ACQIS added them into the reissue applications of RE140 and its parent patents. *See, e.g.*, Ex-1006 [RE140 FH], 125-162; Ex-1009 [RE984 FH], 49-74, 344-377; Ex-1020 [RE602 FH], 23-59; Ex-1021 [RE468 FH],

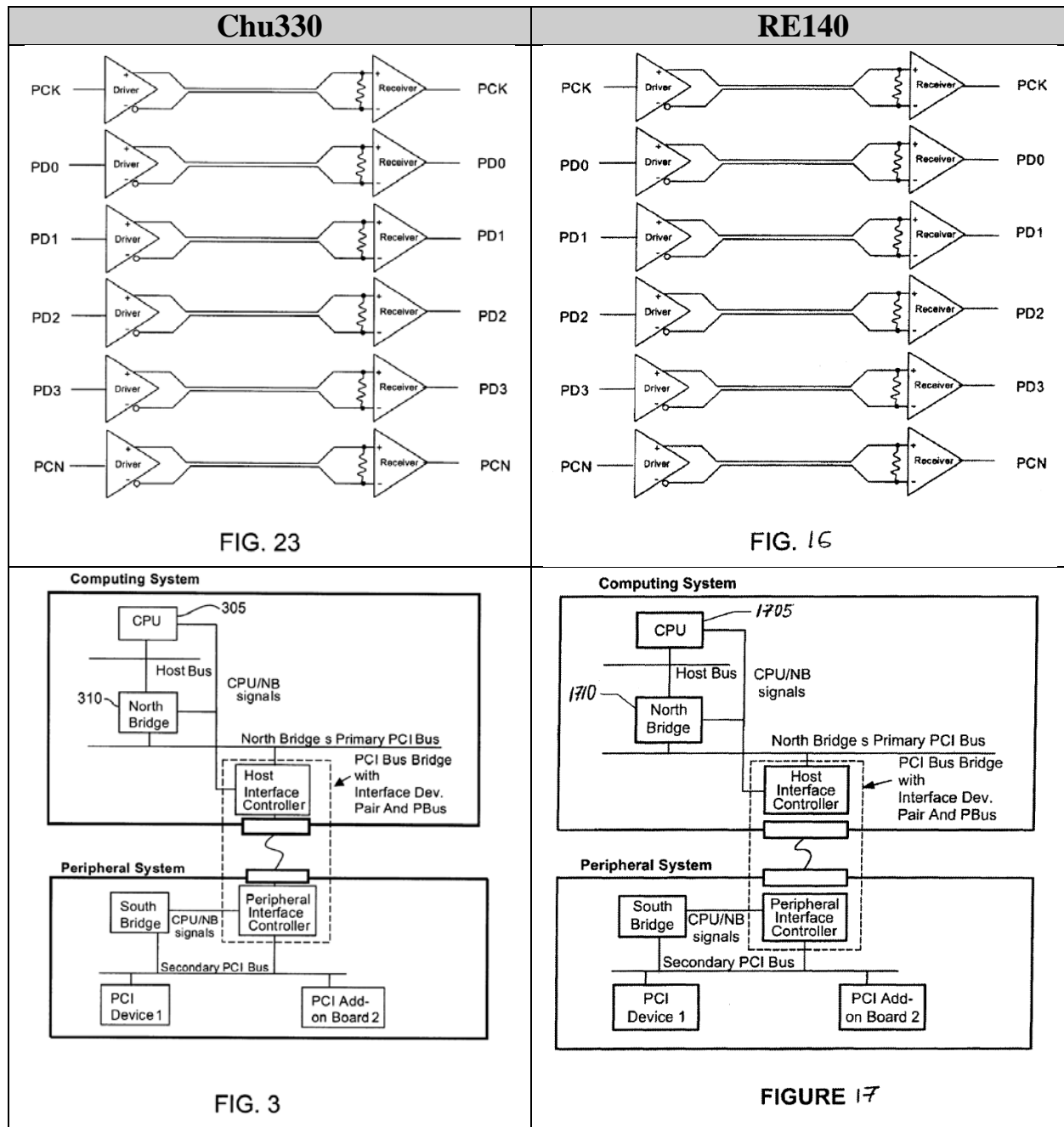
18-58. Ex-1019 shows the portions of RE140 that are substantively identical to Chu330 (in yellow) and Chu185 (in green).<sup>10</sup>

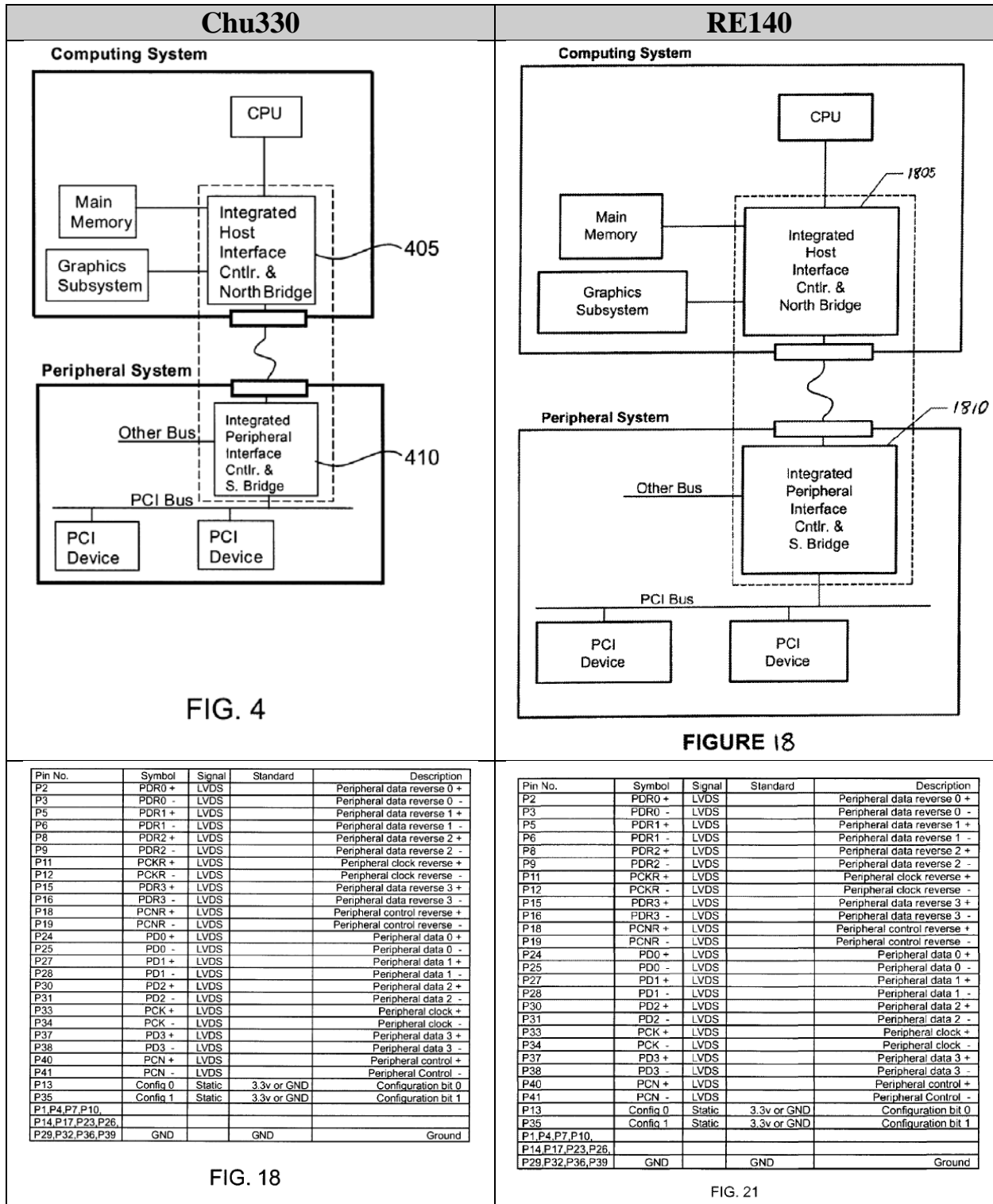
Substantively identical figures from Chu330 are reproduced below.



<sup>10</sup> In addition, Figures 1-8 of RE140 are based on Figures 1-8 of Chu777 (in blue), which is prior art to RE140.









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Chu330					RE140				
Pin No.	Symbol	Signal	Standard	Description	Pin No.	Symbol	Signal	Standard	Description
V2	Red Video	Analog		Video	V2	Red Video	Analog		Video
V4	Green Video	Analog		Video	V4	Green Video	Analog		Video
V6	Blue Video	Analog		Video	V6	Blue Video	Analog		Video
V8	HSYNC			Horizontal Sync	V8	HSYNC			Horizontal Sync
V9	VSNC			Vertical Sync	V9	VSNC			Vertical Sync
V11	DDC2 SCL		VESA DDC std 2	DDC Clock	V11	DDC2 SCL		VESA DDC std 2	DDC Clock
V12	DDC2 SDA		VESA DDC std 2	DDC Data	V12	DDC2 SDA		VESA DDC std 2	DDC Data
V14	TV-CV/CNTL 0			TV Composite Video	V14	TV-CV/CNTL 0			TV Composite Video
V15	SV Y/CNTL 1		Super Video	SV Luminance or Control 1	V15	SV Y/CNTL 1		Super Video	SV Luminance or Control 1
V16	SV C/CNTL 2		Super Video	SV Chrominance or Control 2	V16	SV C/CNTL 2		Super Video	SV Chrominance or Control 2
V24	D0 +	TMDS	VESA P & D	Data 0 +	V24	D0 +	TMDS	VESA P & D	Data 0 +
V25	D0 -	TMDS	VESA P & D	Data 0 -	V25	D0 -	TMDS	VESA P & D	Data 0 -
V27	CLK +	TMDS	VESA P & D	Clock +	V27	CLK +	TMDS	VESA P & D	Clock +
V28	CLK -	TMDS	VESA P & D	Clock -	V28	CLK -	TMDS	VESA P & D	Clock -
V30	D1 +	TMDS	VESA P & D	Data 1 +	V30	D1 +	TMDS	VESA P & D	Data 1 +
V31	D1 -	TMDS	VESA P & D	Data 1 -	V31	D1 -	TMDS	VESA P & D	Data 1 -
V33	D2 +	TMDS	VESA P & D	Data 2 +	V33	D2 +	TMDS	VESA P & D	Data 2 +
V34	D2 -	TMDS	VESA P & D	Data 2 -	V34	D2 -	TMDS	VESA P & D	Data 2 -
V37	VPCK +	LVDS		Video Port Pixel Clock +	V37	VPCK +	LVDS		Video Port Pixel Clock +
V38	VPCK -	LVDS		Video Port Pixel Clock -	V38	VPCK -	LVDS		Video Port Pixel Clock -
V40	VPD +	LVDS		Video Port Pixel Data +	V40	VPD +	LVDS		Video Port Pixel Data +
V41	VPD -	LVDS		Video Port Pixel Data -	V41	VPD -	LVDS		Video Port Pixel Data -
V13	Config 2		3.3v or GND	Configuration bit 2	V13	Config 2		3.3v or GND	Configuration bit 2
V35	Config 3		3.3v or GND	Configuration bit 3	V35	Config 3		3.3v or GND	Configuration bit 3
V1,V3,V5,V7, V10,V23,V26, V29,V32,V36, V39,V42,V43, V44	GND		GND	Ground	V1,V3,V5,V7, V10,V23,V26, V29,V32,V36, V39,V42,V43, V44	GND		GND	Ground

FIG. 19

	Symbol	Signal	Data Rate	Description
1	PD0 RTN			GND
2	PD0 +	Synch. To PCK	10 x clock rate	Computer to Peripheral LVDS Data 0 +
3	PD0 -			Computer to Peripheral LVDS Data 0 -
4	PD1 RTN			GND
5	PD1 +	Synch. To PCK	10 x clock rate	Computer to Peripheral LVDS Data 1 +
6	PD1 -			Computer to Peripheral LVDS Data 1 -
7	PD2 RTN			GND
8	PD2 +	Synch. To PCK	10 x clock rate	Computer to Peripheral LVDS Data 2 +
9	PD2 -			Computer to Peripheral LVDS Data 2 -
10	PD3 RTN			GND
11	PD3 +	Synch. To PCK	10 x clock rate	Computer to Peripheral LVDS Data 3 +
12	PD3 -			Computer to Peripheral LVDS Data 3 -
13	PCK RTN			GND
14	PCK +	Clock	Clock rate	Computer to Peripheral LVDS Clock +
15	PCK -			Computer to Peripheral LVDS Clock -
16	PCN RTN			GND
17	PCN +	Synch. To PCK	10 x clock rate	Computer to Peripheral LVDS Control +
18	PCN -			Computer to Peripheral LVDS Control -
19	PD0 RTN			GND
20	PD0 +	Synch. To PCKR	10 x clock rate	Peripheral to Computer LVDS Data 0 +
21	PD0 -			Peripheral to Computer LVDS Data 0 -
22	PD1 RTN			GND
23	PD1 +	Synch. To PCKR	10 x clock rate	Peripheral to Computer LVDS Data 1 +
24	PD1 -			Peripheral to Computer LVDS Data 1 -
25	PD2 RTN			GND
26	PD2 +	Synch. To PCKR	10 x clock rate	Peripheral to Computer LVDS Data 2 +
27	PD2 -			Peripheral to Computer LVDS Data 2 -
28	PD3 RTN			GND
29	PD3 +	Synch. To PCKR	10 x clock rate	Peripheral to Computer LVDS Data 3 +
30	PD3 -			Peripheral to Computer LVDS Data 3 -
31	PCKR RTN			GND
32	PCKR +	Reverse Dir. Clock	Clock rate	Peripheral to Computer LVDS Clock +
33	PCKR -			Peripheral to Computer LVDS Clock -
34	PCNR RTN			GND
35	PCNR +	Synch. To PCKR	10 x Clock rate	Peripheral to Computer LVDS Control +
36	PCNR -			Peripheral to Computer LVDS Control -
37	RESET#		Asynchronous	Reset

FIG. 20

ID bits (P0 P1 P2 P3)	Data Packet Type
X X 0 0	PCI 1st address/data segment
X X 1 0	PCI 2nd address/data segment
0 0 0 1	Control 1st segment with PCI response
1 0 0 1	Control 1st segment without PCI response
0 1 0 1	Control 2nd segment with PCI response
1 1 0 1	Control 2nd segment without PCI response
0 0 1 1	Reserved
1 0 1 1	Reserved
0 1 1 1	Initialization
1 1 1 1	NOOP

FIG. 35

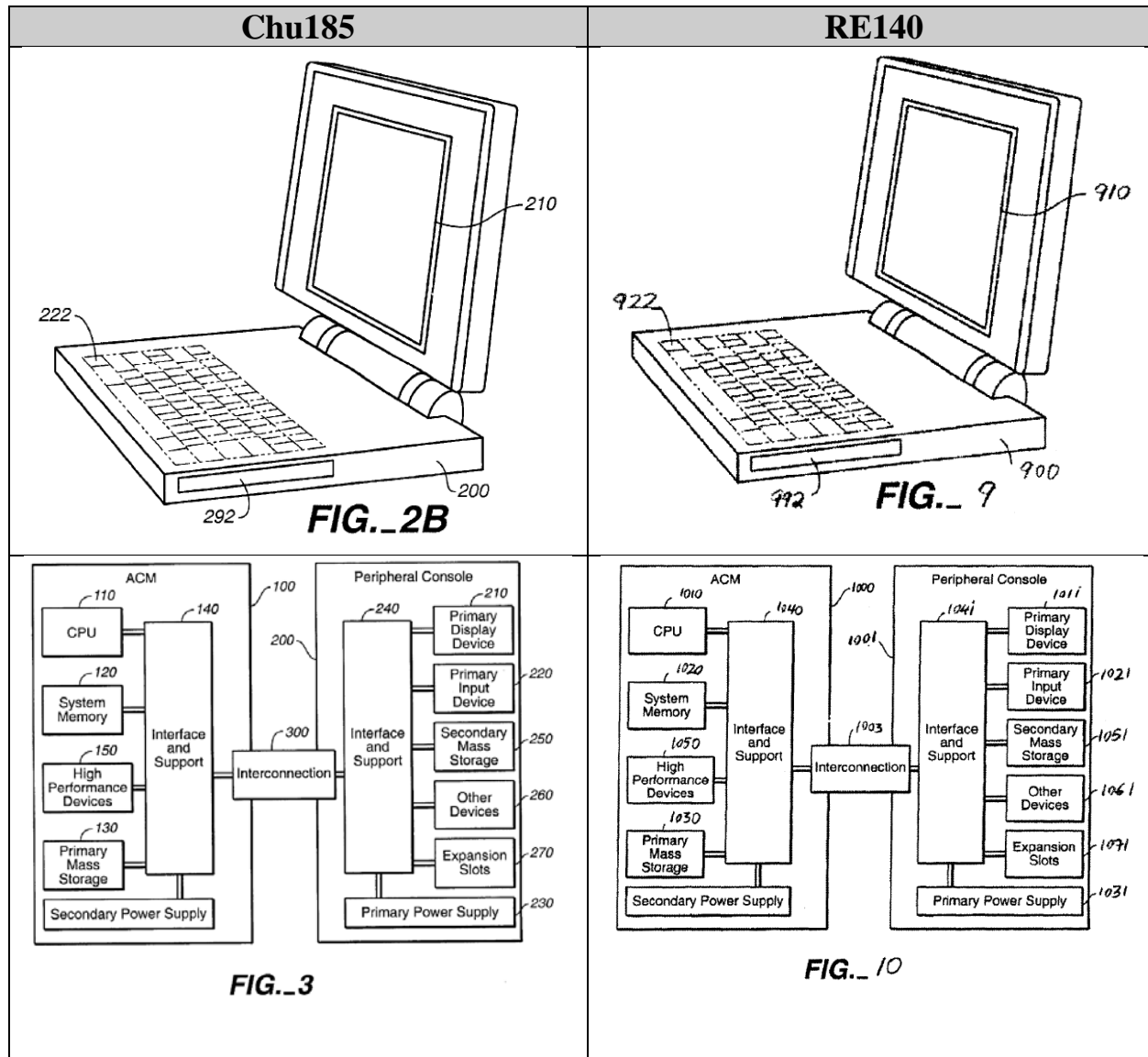
	Symbol	Signal	Data Rate	Description
1	PD0 RTN			GND
2	PD0 +	Synch. To PCK	10 x clock rate	Computer to Peripheral LVDS Data 0 +
3	PD0 -			Computer to Peripheral LVDS Data 0 -
4	PD1 RTN			GND
5	PD1 +	Synch. To PCK	10 x clock rate	Computer to Peripheral LVDS Data 1 +
6	PD1 -			Computer to Peripheral LVDS Data 1 -
7	PD2 RTN			GND
8	PD2 +	Synch. To PCK	10 x clock rate	Computer to Peripheral LVDS Data 2 +
9	PD2 -			Computer to Peripheral LVDS Data 2 -
10	PD3 RTN			GND
11	PD3 +	Synch. To PCK	10 x clock rate	Computer to Peripheral LVDS Data 3 +
12	PD3 -			Computer to Peripheral LVDS Data 3 -
13	PCK RTN			GND
14	PCK +	Clock	Clock rate	Computer to Peripheral LVDS Clock +
15	PCK -			Computer to Peripheral LVDS Clock -
16	PCN RTN			GND
17	PCN +	Synch. To PCK	10 x clock rate	Computer to Peripheral LVDS Control +
18	PCN -			Computer to Peripheral LVDS Control -
19	PD0 RTN			GND
20	PD0 +	Synch. To PCKR	10 x clock rate	Peripheral to Computer LVDS Data 0 +
21	PD0 -			Peripheral to Computer LVDS Data 0 -
22	PD1 RTN			GND
23	PD1 +	Synch. To PCKR	10 x clock rate	Peripheral to Computer LVDS Data 1 +
24	PD1 -			Peripheral to Computer LVDS Data 1 -
25	PD2 RTN			GND
26	PD2 +	Synch. To PCKR	10 x clock rate	Peripheral to Computer LVDS Data 2 +
27	PD2 -			Peripheral to Computer LVDS Data 2 -
28	PD3 RTN			GND
29	PD3 +	Synch. To PCKR	10 x clock rate	Peripheral to Computer LVDS Data 3 +
30	PD3 -			Peripheral to Computer LVDS Data 3 -
31	PCKR RTN			GND
32	PCKR +	Reverse Dir. Clock	Clock rate	Peripheral to Computer LVDS Clock +
33	PCKR -			Peripheral to Computer LVDS Clock -
34	PCNR RTN			GND
35	PCNR +	Synch. To PCKR	10 x Clock rate	Peripheral to Computer LVDS Control +
36	PCNR -			Peripheral to Computer LVDS Control -
37	RESET#		Asynchronous	Reset

FIG. 23

ID bits (P0 P1 P2 P3)	Data Packet Type
X X 0 0	PCI 1st address/data segment
X X 1 0	PCI 2nd address/data segment
0 0 0 1	Control 1st segment with PCI response
1 0 0 1	Control 1st segment without PCI response
0 1 0 1	Control 2nd segment with PCI response
1 1 0 1	Control 2nd segment without PCI response
0 0 1 1	Reserved
1 0 1 1	Reserved
0 1 1 1	Initialization
1 1 1 1	NOOP

FIG. 24

Substantively identical figures from Chu185 are reproduced below.



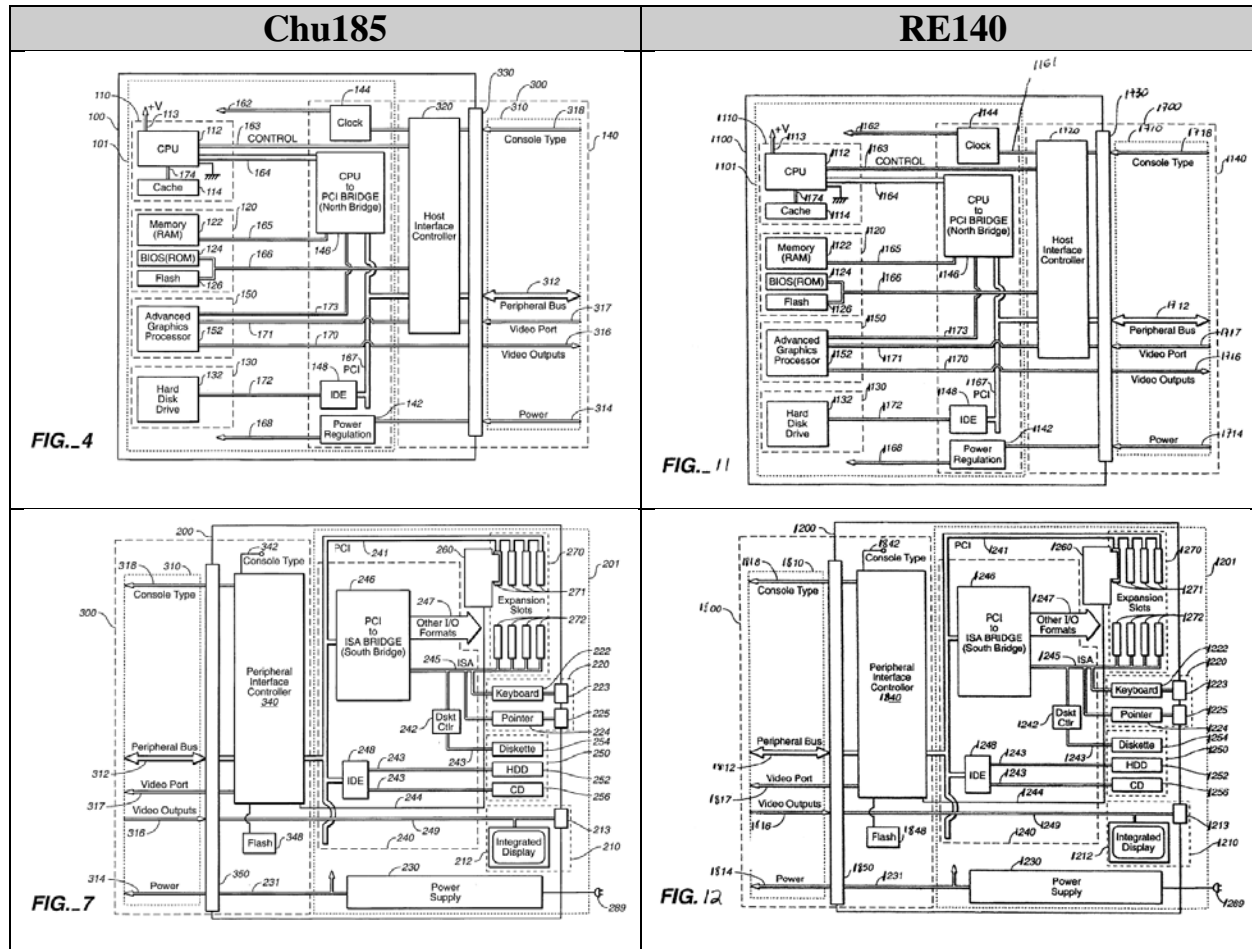
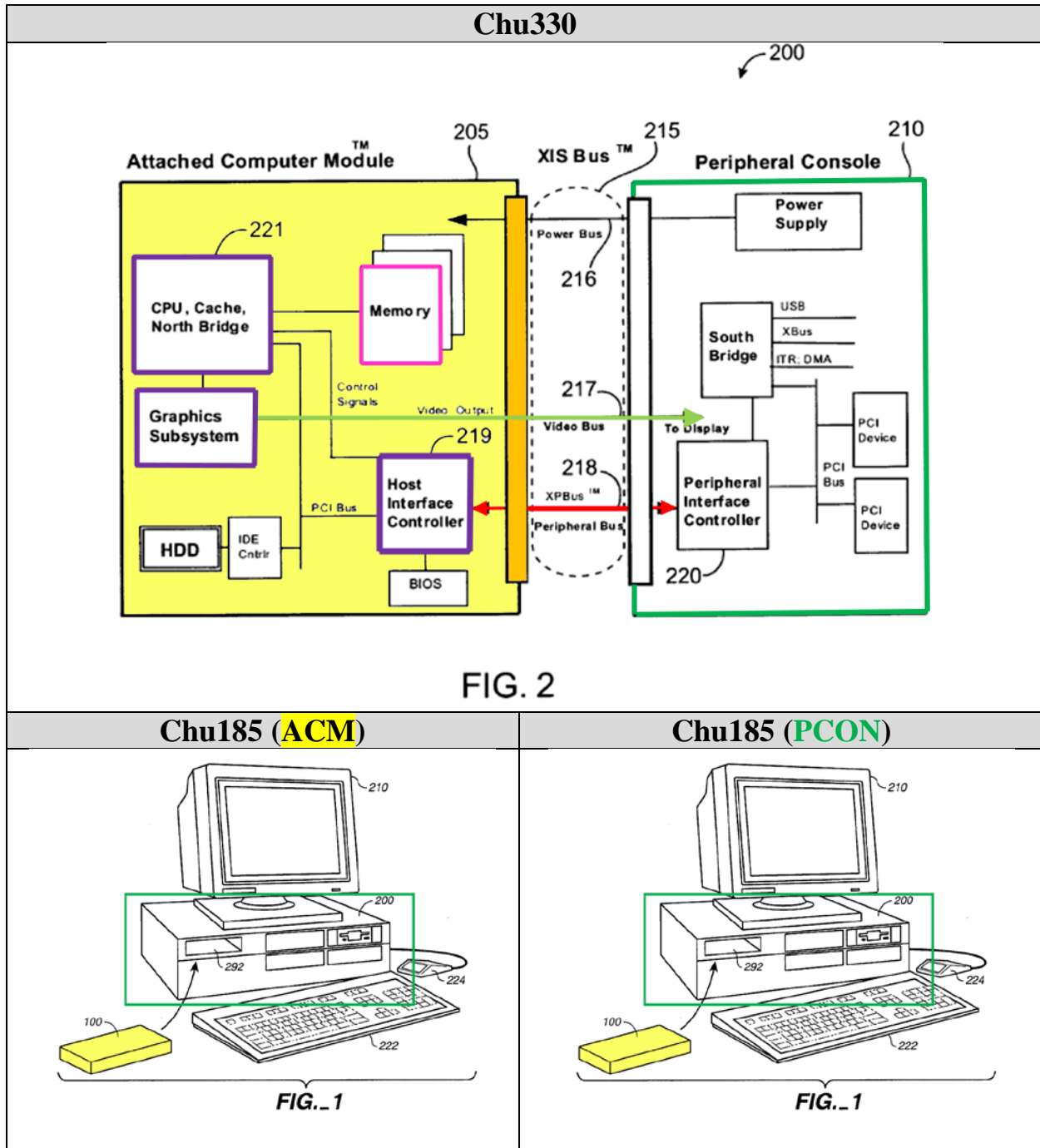
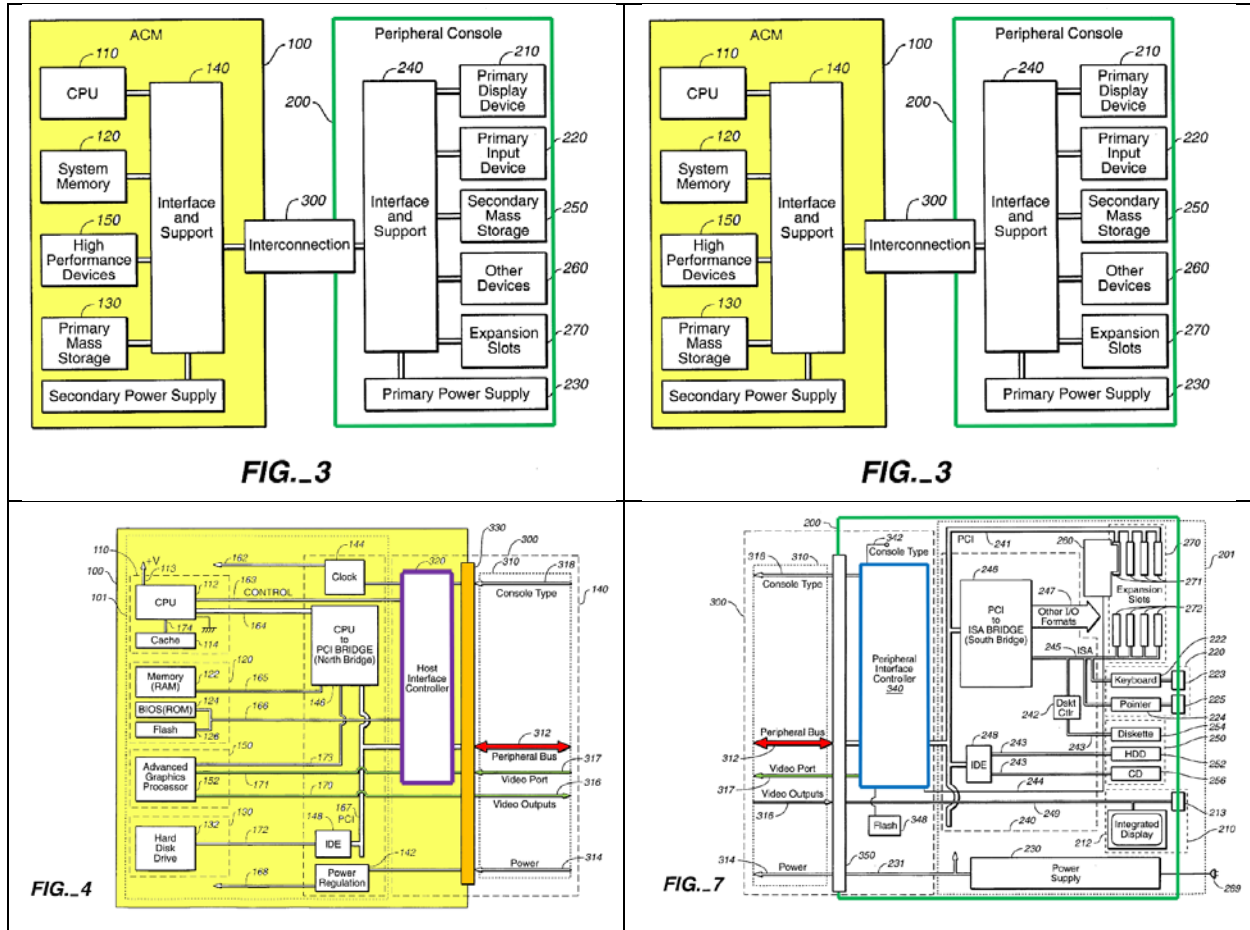


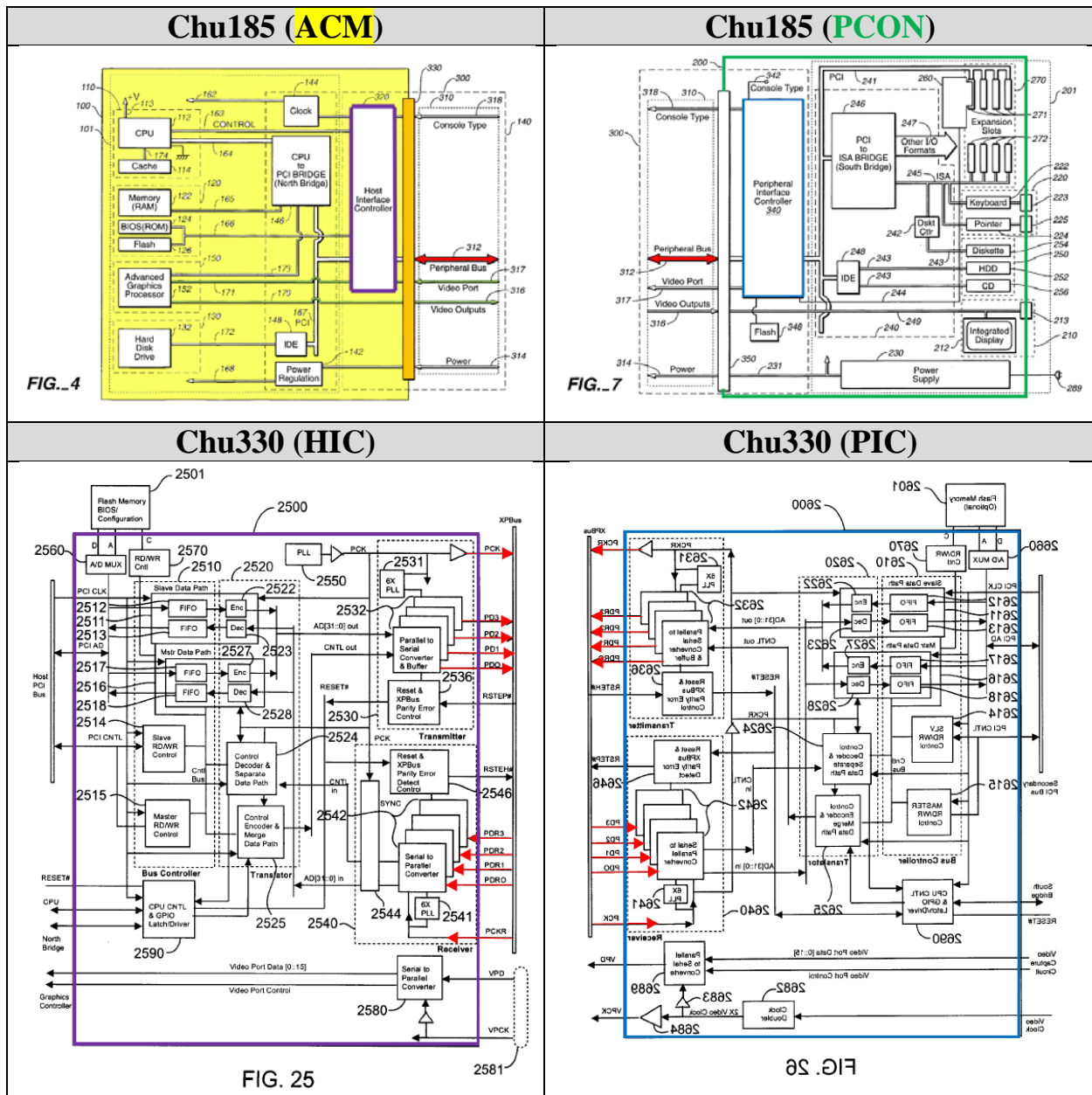
Figure 2 of Chu330 shows a computer system that includes an **ACM 205** and **PCON 210**. Details about **ACM 205** in Figure 2 are found, for example, in Figures 1, 3, and 4 of Chu185, and details about **PCON 210** are found, for example, in Figures 1, 3, and 7 of Chu185. See Ex-1003, 5:66-6:7. See Ex-1002, ¶79.



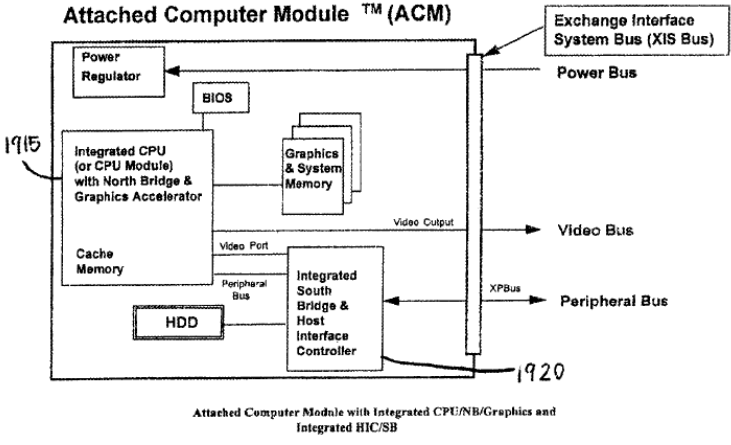


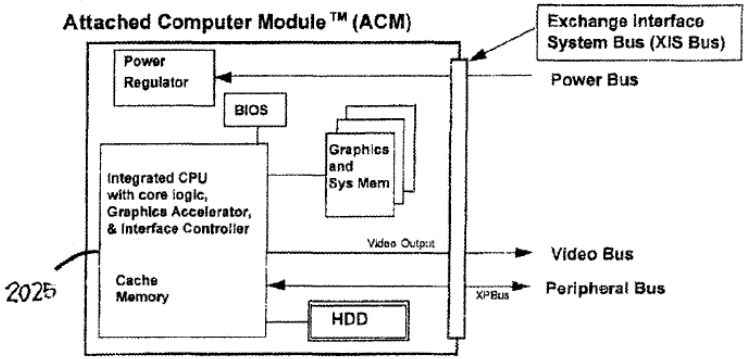
Figures 3, 4, and 7 of Chu185 show the **ACM**-to-**PCON** *Interconnection 300* between **ACM** and **PCON**. As shown in Figures 4 and 7, the **HIC 320** in the **ACM** communicates with the **PIC 340** in the **PCON** through the “**ACM connector component 330**.” See Ex-1005, 5:57-66. Chu185 notes that additional details of the **ACM**-to-**PCON** *Interconnection* can be found in Chu330, which was incorporated by reference into Chu185. Ex-1005, 9:38-42; Ex-1003, 16:25-26, 17:8-12, Figures 6, 11, 25, 26. Chu330 indeed provides additional details about the interconnection between the **HIC** and **PIC** in Figures 25 and 26 (horizontally flipped

below for presentation purposes), such as the **individual lines** between the **HIC** and **PIC**. Figures 6/11 (not shown below) illustrate another example of the interconnection between the **HIC** and **PIC** that is substantially “identical” to Figures 25/26. Ex-1003, 16:25-26, 17:8-17. *See* Ex-1002, ¶¶80-81; *see also* Ex-1002, ¶¶82-88.



Finally, Chu330 and Chu185 do ***not*** incorporate by reference the '886 Provisional. Ex-1003, 1:7-10; Ex-1005, 1:7-10. Accordingly, Chu330 and Chu185 provide substantively identical disclosures to portions of RE140 that ACQIS relies on for written description support of most of the limitations of the challenged claims—except for Figures 19 and 20 of RE140, which purportedly provide support for the “integrated CPU/graphics” and “CPU-LVDS” limitations. *See* Ex-1002, ¶¶91.

Chu330	RE140
Does not exist	 <p>The diagram, labeled FIG. 19, shows an 'Attached Computer Module™ (ACM)' as a large rectangular box. Inside the box, at the top left, is a 'Power Regulator' connected to a 'BIOS' block. Below the BIOS is an 'Integrated CPU (or CPU Module) with North Bridge &amp; Graphics Accelerator' block, which is connected to 'Cache Memory' below it. To the right of the CPU block is a 'Graphics &amp; System Memory' block. Below the CPU block is a 'Video Port' block, which is connected to an 'Integrated South Bridge &amp; Host Interface Controller' block at the bottom right. A 'HDD' (Hard Disk Drive) is connected to the South Bridge block via a 'Peripheral Bus'. The South Bridge block is also connected to an 'XPSus' block. The entire ACM box is connected to an 'Exchange Interface System Bus (XIS Bus)' on the right. This bus has three output lines: 'Power Bus', 'Video Bus', and 'Peripheral Bus'. Handwritten labels '1915' and '1920' point to the CPU block and the South Bridge block respectively. Below the diagram is the caption: 'Attached Computer Module with Integrated CPU/NB/Graphics and Integrated HIC/SB'.</p> <p style="text-align: center;">FIG. 19</p>

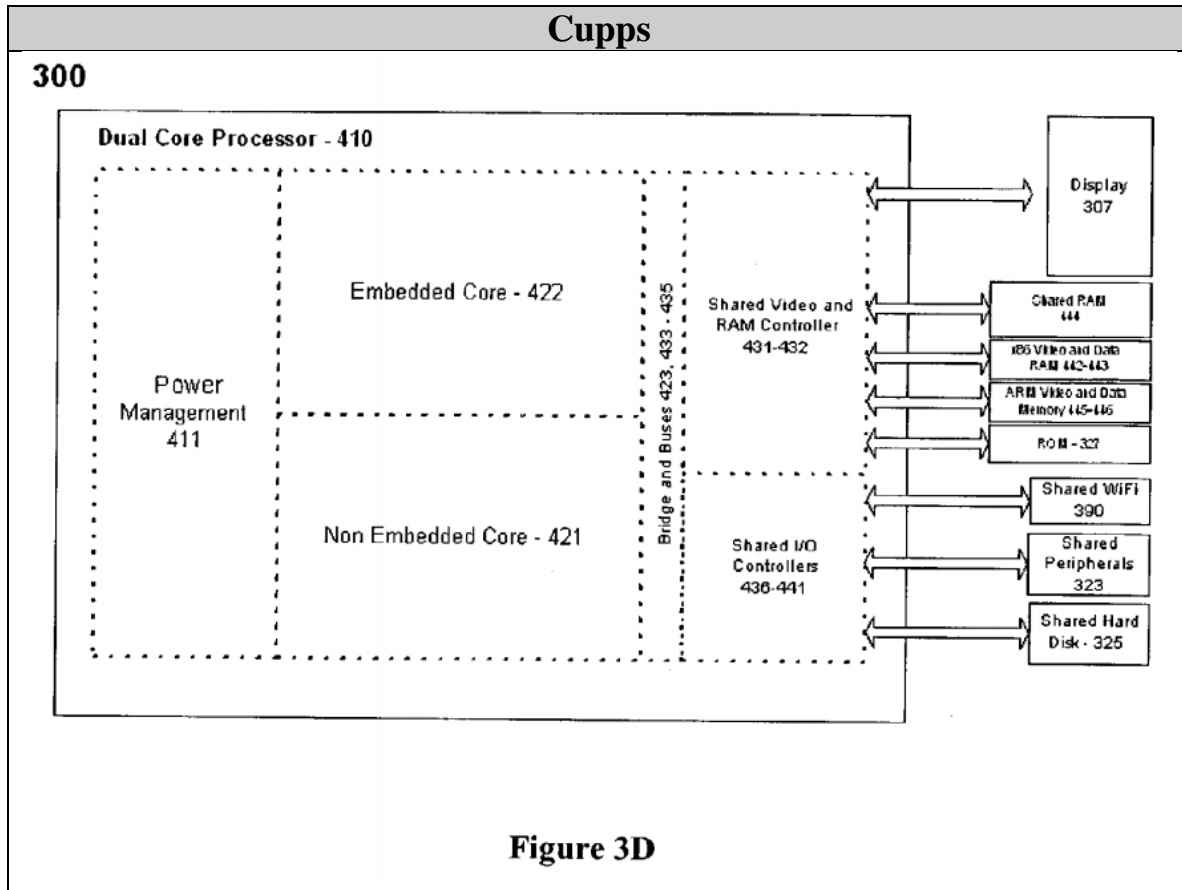
Chu330	RE140
Does not exist	 <p>The diagram shows an Attached Computer Module (ACM) with the following components and connections:</p> <ul style="list-style-type: none"> <li><b>Internal Components:</b> <ul style="list-style-type: none"> <li>Power Regulator</li> <li>BIOS</li> <li>Integrated CPU with core logic, Graphics Accelerator, &amp; Interface Controller</li> <li>Cache Memory</li> <li>Graphics and Sys Mem</li> <li>HDD</li> </ul> </li> <li><b>External Interfaces:</b> <ul style="list-style-type: none"> <li>Exchange Interface System Bus (XIS Bus) - connected to the ACM's interface controller.</li> <li>Power Bus - connected to the Power Regulator.</li> <li>Video Bus - connected to the Graphics and Sys Mem.</li> <li>Peripheral Bus - connected to the ACM's interface controller.</li> <li>XPBus - connected to the Cache Memory.</li> </ul> </li> </ul> <p>2025</p> <p>Attached Computer Module with Single Chip fully integrated: CPU, Cache, Core logic, Graphics controller and Interface controller</p> <p>FIG. 20</p>

## ii. Cupps

Cupps describes “portable computers, which can be carried from place to place with relative convenience.” Ex-1004, [0003]. Cupps teaches combining different functions “in[to] a single device,” *id.*, [0005], such as combining two different processors “in a [single] handheld housing,” *id.*, [0013] or being “integrated into a single integrated circuit processor.” *Id.*, [0015].

For example, Figure 3D shows a “Dual Core Processor 410 [which] combine[s] the functionality of embedded and non-embedded processors with controllers as shown in FIG. 3C onto one integrated circuit.” Ex-1004, [0068], [0163].





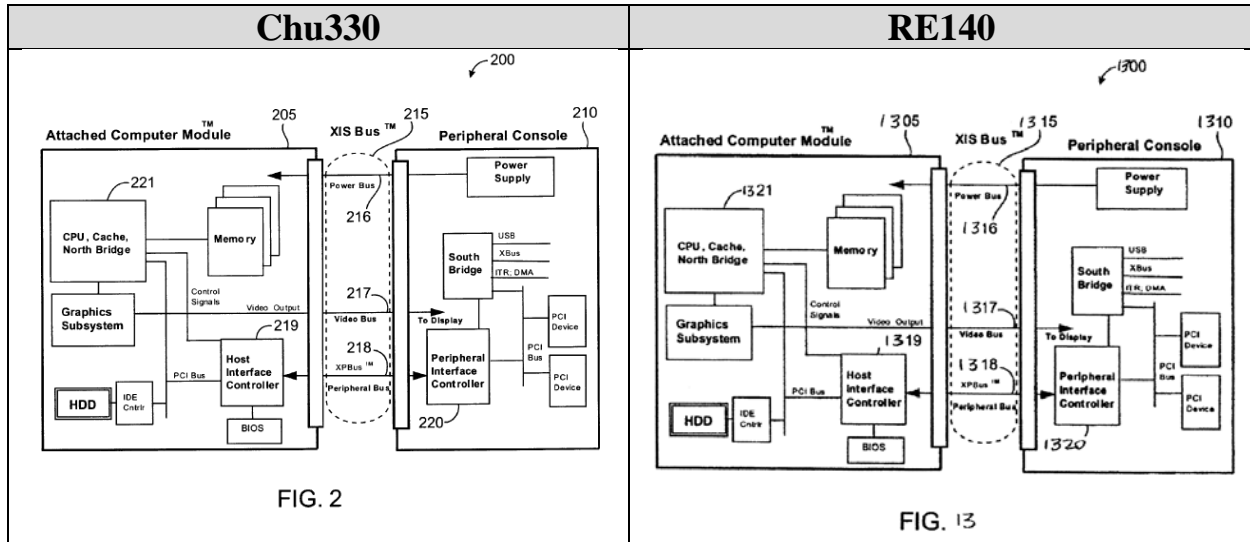
Cupps explains the various benefits of integrating different functionalities into a single chip, such as reduced redundancy, improved power efficiency, improved performance, smaller physical footprint, and sharing peripherals. *See* Ex-1004, [0015], [0069].

## 2. Claim 14

- i. [14pre] A method of improving performance of a computer, comprising:

To the extent the preamble is limiting, Chu330 discloses the preamble. For example, Figure 2 of Chu330 shows a computer system 200 with an “attached

**computer** module (ACM) 205” and a peripheral console (PCON) 210. *See* Ex-1003, 5:66-6:2, 3:45-47, 6:26-35.<sup>11</sup> The ACM 205 of Chu330 meets the preamble’s “computer.” *See* Ex-1002, ¶¶106-108.



Additionally, Chu330 teaches improving computer performance. *See, e.g.,* Ex-1003, 2:10-15 (explaining that an LVDS channel, as discussed in Section XI.A.2.vii [14f] below, improves computer performance because it “is more cable friendly, faster, consumes less power, and generates less noise”);<sup>12</sup> Ex-1004, [0069] (explaining that the benefits of integration include “increased performance” as discussed in Section XI.A.2.ii [14a] below ); *see also* Ex-1005, 4:50-54 (“The core computing power may also include high performance devices 150 such as advanced

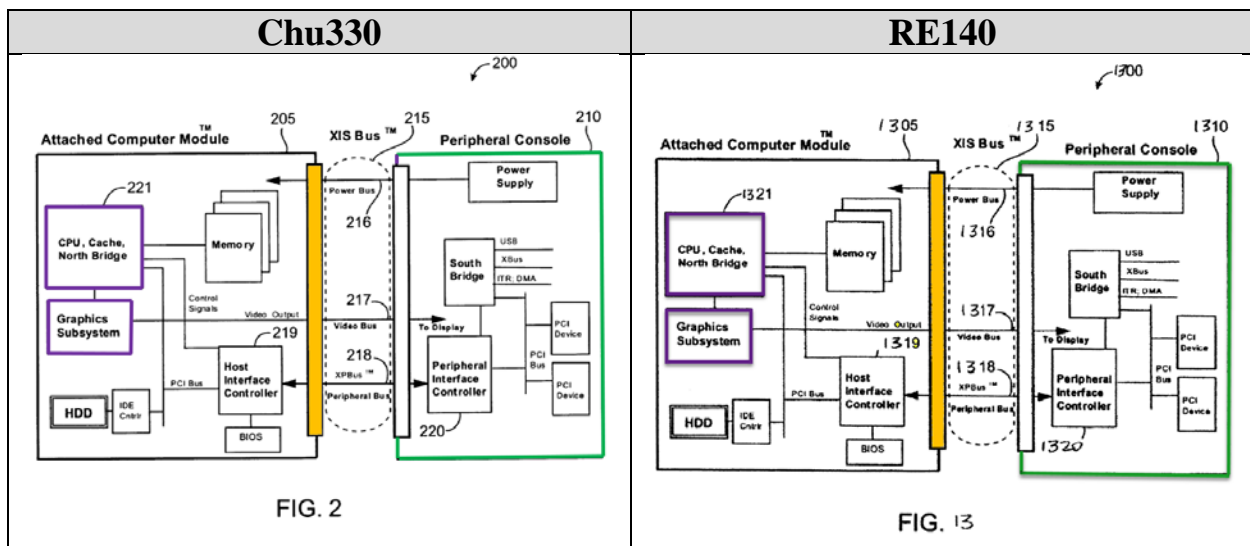
<sup>11</sup> *See* equivalent disclosure in Ex-1001, 18:39-42, 5:15-16, 18:66-19:8, Figure 6.

<sup>12</sup> *See* equivalent disclosure in Ex-1001, 17:39-42.

graphics processor chips that greatly increase overall system performance....”),  
Section XI.A.1.i [Chu330]. *See* Ex-1002, ¶109.

ii. [14a] obtaining an **integrated Central Processing Unit (CPU) with a graphics controller in a single chip**;

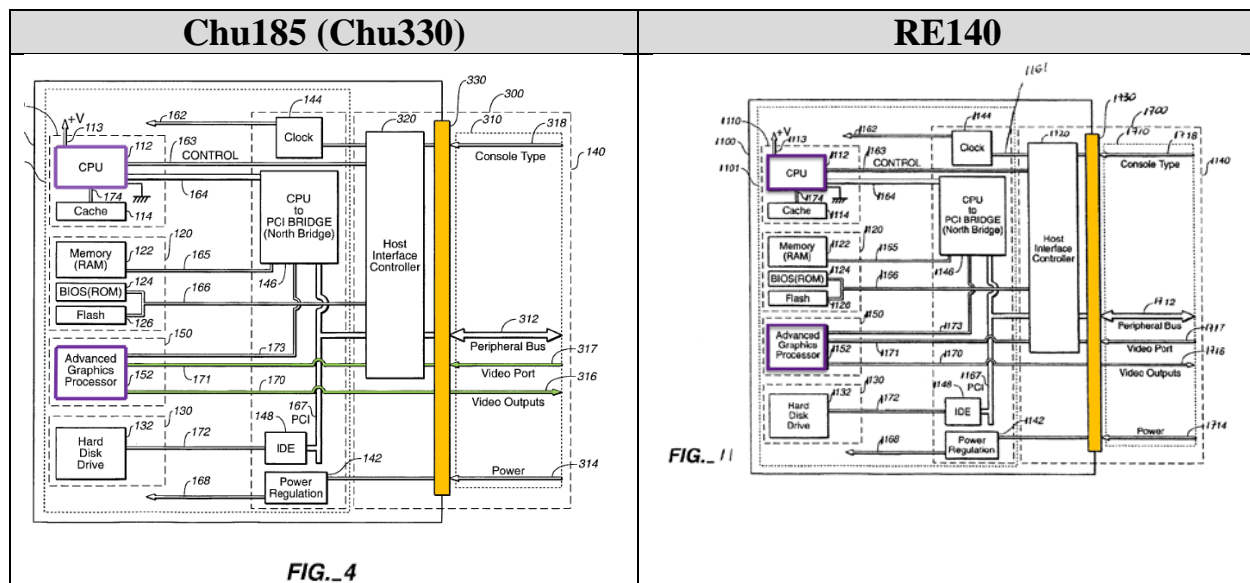
Chu330 discloses a **central processing unit (CPU)**, a **graphics subsystem**,  
and a **host interface controller (HIC)** in the ACM in figure 2. *See* Ex-1003, 5:66-  
6:35,<sup>13</sup> claims 2 and 3; *see also* Ex-1005, 4:47-64, 7:50-54, and Figures 3-4; *see also*  
Section XI.A.1.i [Chu330]. *See* Ex-1002, ¶112.



Chu330 refers to the **graphics subsystem** of Figure 2 as a “**graphics controller**.” *See* Ex-1003, claims 2, 3, 6; 10:6, Figures 6 and 25. Additionally,  
Figure 4 of Chu185 shows the **graphics subsystem** to be an **Advanced Graphics**

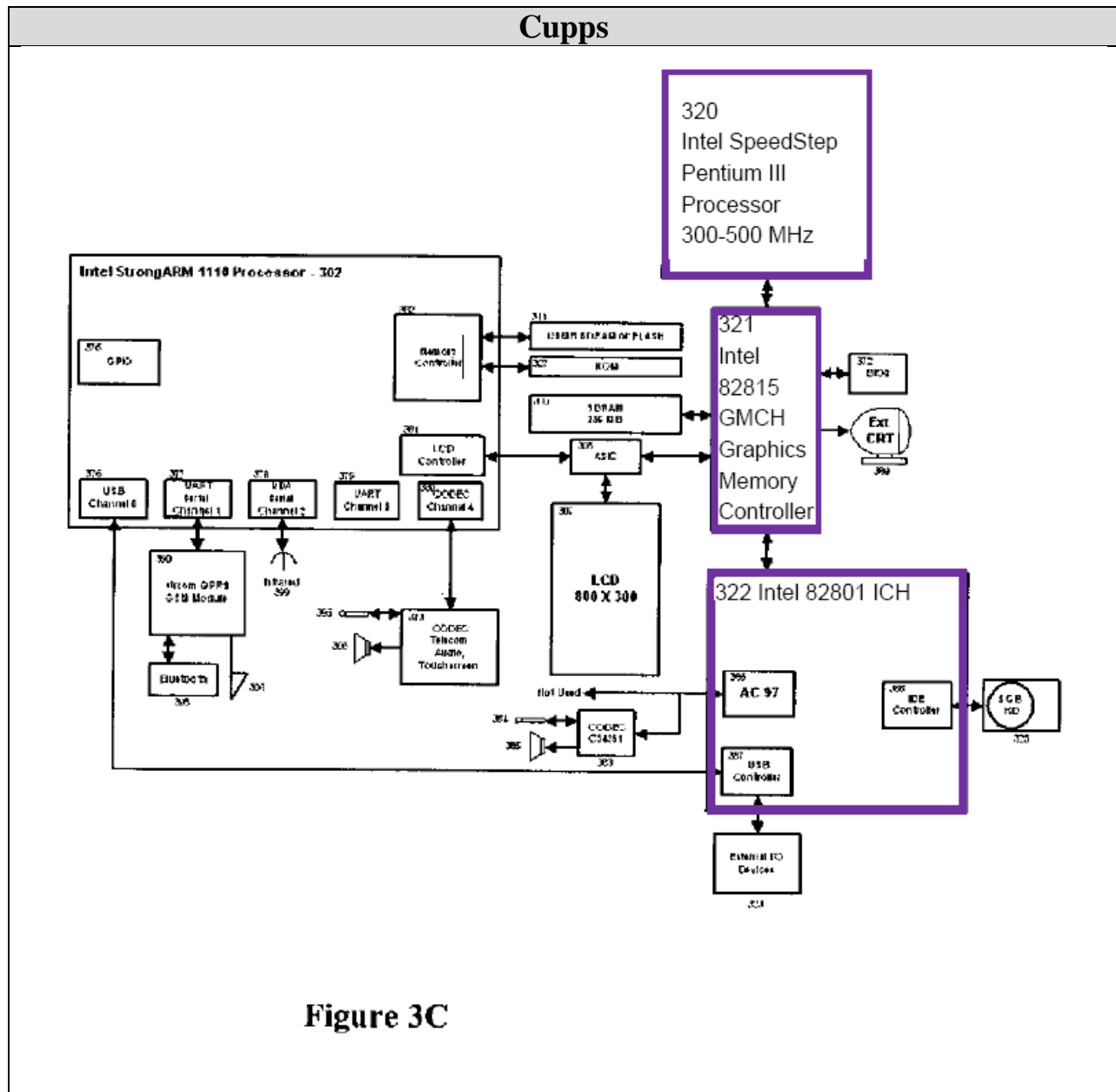
<sup>13</sup> *See* equivalent disclosure in Ex-1001, 18:39-19:8.

**Processor (AGP) 152** that can be “**Model 740 Graphics Device from Intel Corporation.**” Ex-1005, 7:50-54; *see* Section XI.A.1.i [Chu330]. Such graphics processors/accelerators are often called “graphics controllers.” *See* Ex-1017, 1:16-21 (“**graphics controllers/accelerators** such as the **Intel 740**... A typical **graphics controller** such as the **Intel 740**...”). *See* Ex-1002, ¶113.



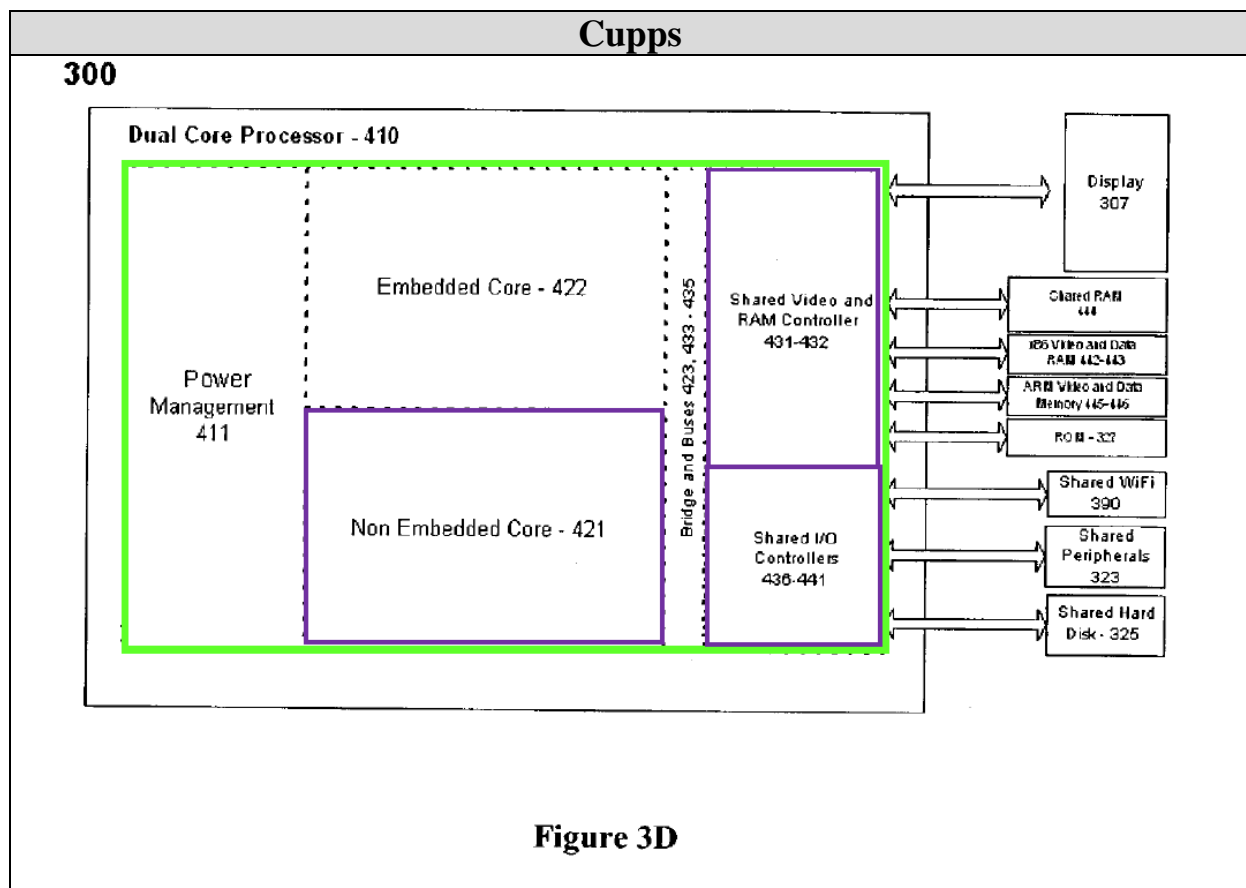
**Integration** of a **CPU**, **graphics controller**, and **HIC in a single chip** was well-known by the priority date afforded to RE140. For example, Figure 3D of Cupps discloses an “integrated circuit 410 utilizing two processor cores” that “*combine[s]* the functionality of embedded and non-embedded *processors with controllers* as shown in FIG. 3C.” Ex-1004, [0163]. Specifically, Cupps shows, in Figure 3C (text edited for clarity), among other components, an **Intel SpeedStep Pentium Processor 320** that is coupled to **Intel 82815 Graphics and Memory**

**Controller Hub (GMCH) 321** that operates with an **Intel 82801 integrated controller hub (ICH) device 322**. Ex-1004, [0086] (“Operating with processor 320 are memory and graphics controller 321, such as Intel 82815 graphics memory controller hub (GMCH) device, and controller and I/O module 322, for example an Intel 82801 integrated controller hub (ICH) device.”), [0180] (discussing “Pentium Class processor 320” is a “CPU”). *See* Ex-1002, ¶¶114-115.



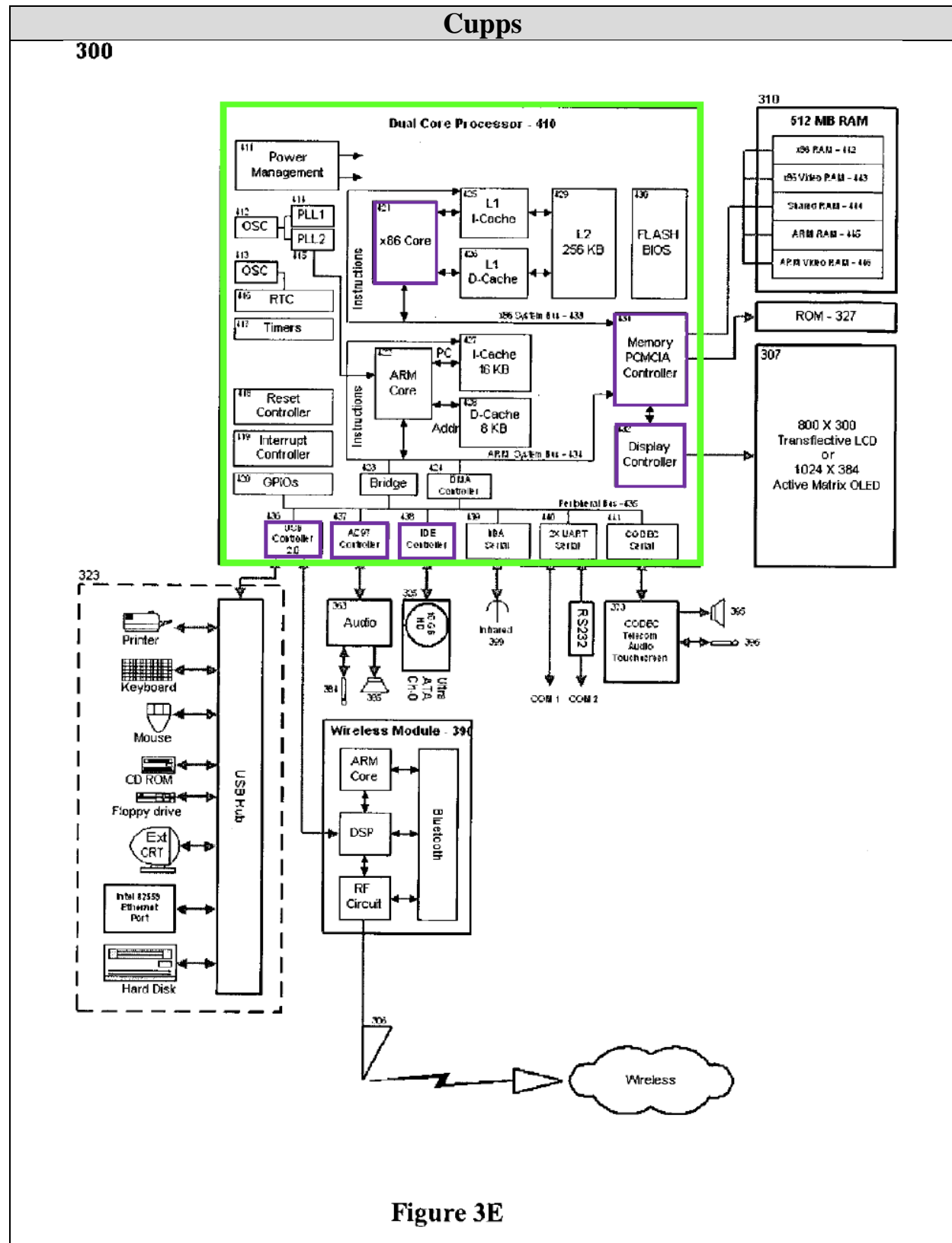
Cupps further teaches that these components in Figure 3C can be **integrated in a single chip**. For example, in Figure 3D, all of the functionalities associated with the **processor 320**, **GMCH 321**, and **ICH 322** are integrated together onto a single die as “**core 421**,” “**shared video and RAM controller 431-432**,” and

“**shared I/O controllers 436-441.**” Ex-1004, [0068] (“The Dual Core Processor 410 combines the functionality of embedded and non-embedded processors with controllers onto **one integrated circuit**”), [0078], [0163] (“an **integrated circuit 410** utilizing two **processor cores 421** and 422 and **controllers 431, 432, 436-441** could be used, as shown in FIGS. 3D and 3E. The purpose of the **Dual Core Processor 410** is to combine the functionality of embedded and **non-embedded processors** with **controllers** as shown in FIG. 3C onto one **integrated circuit** as shown in FIGS. 3D and 3E.”); *see also id.*, [0221] (“processor 302” is “embedded” and “processor 320” is “non-embedded”). *See* Ex-1002, ¶116.

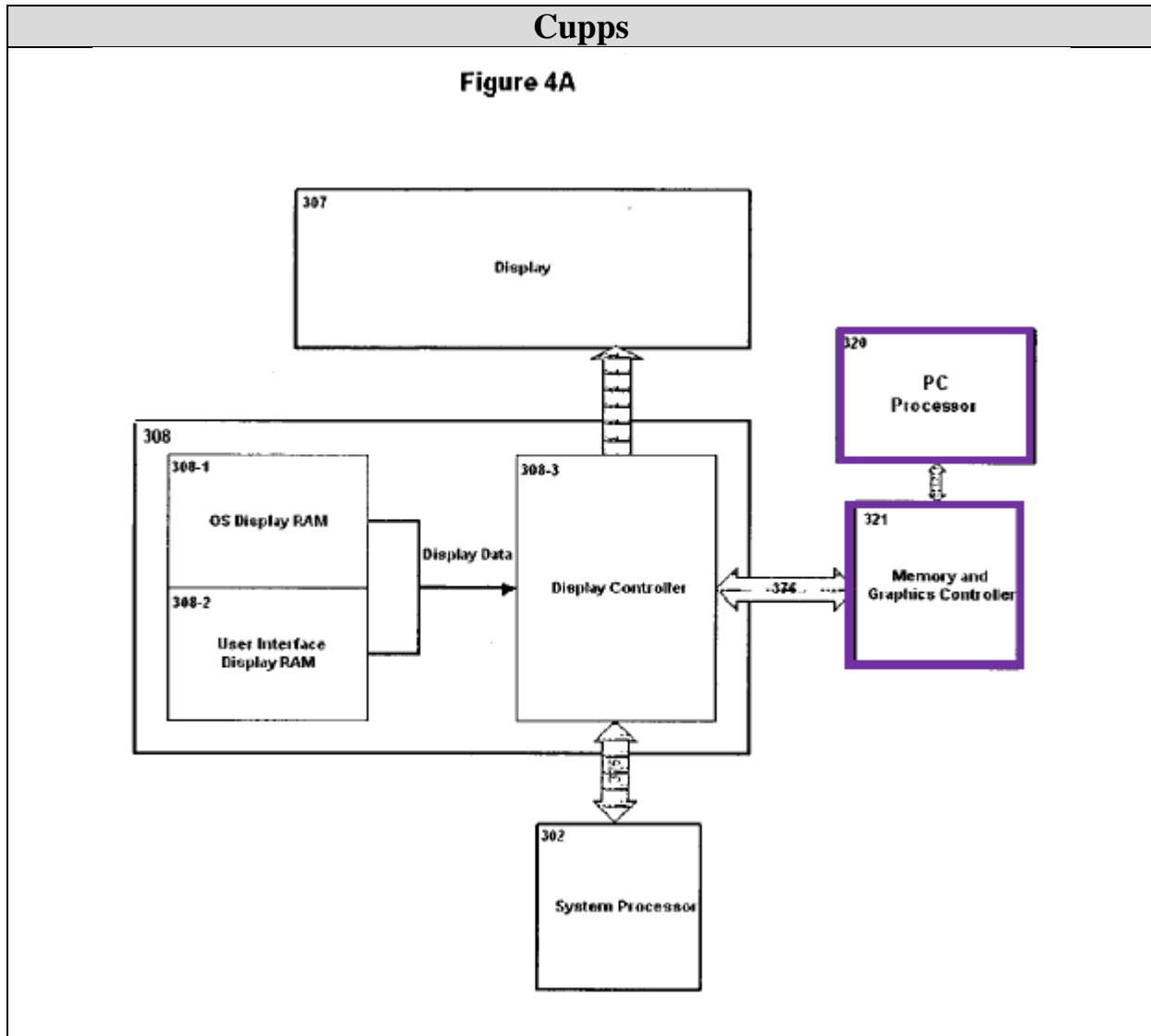


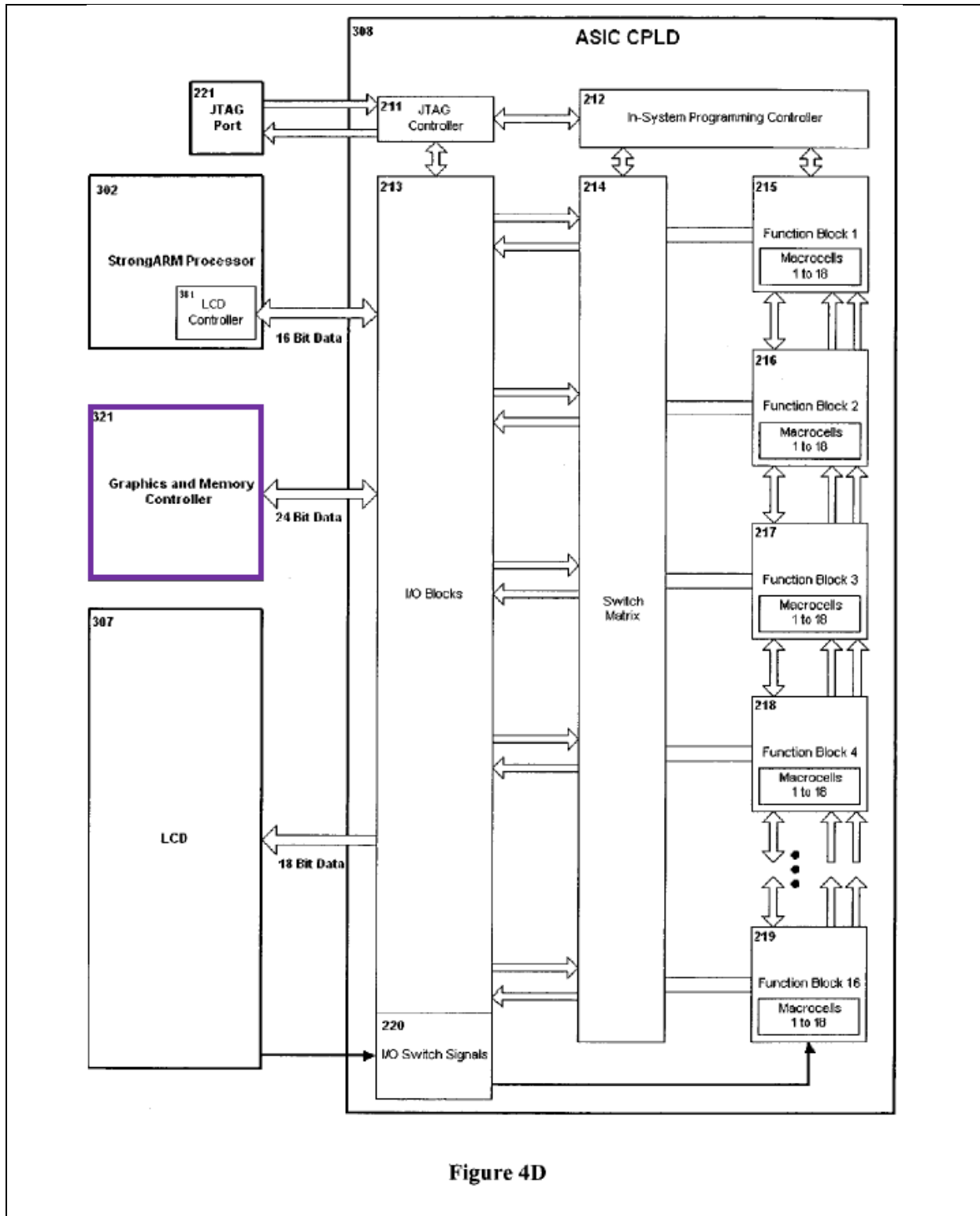
In Figure 3E, the **x86 (non-embedded) core 421** and **various controllers** (*e.g.*, **memory PCMCIA and display controllers 431 and 432**, **USB controller 436**, **AC97 controller 437**, **IDE controller 438**, etc.) are integrated together onto **a single die**. *See* Ex-1004, [0068]. *See* Ex-1002, ¶117.



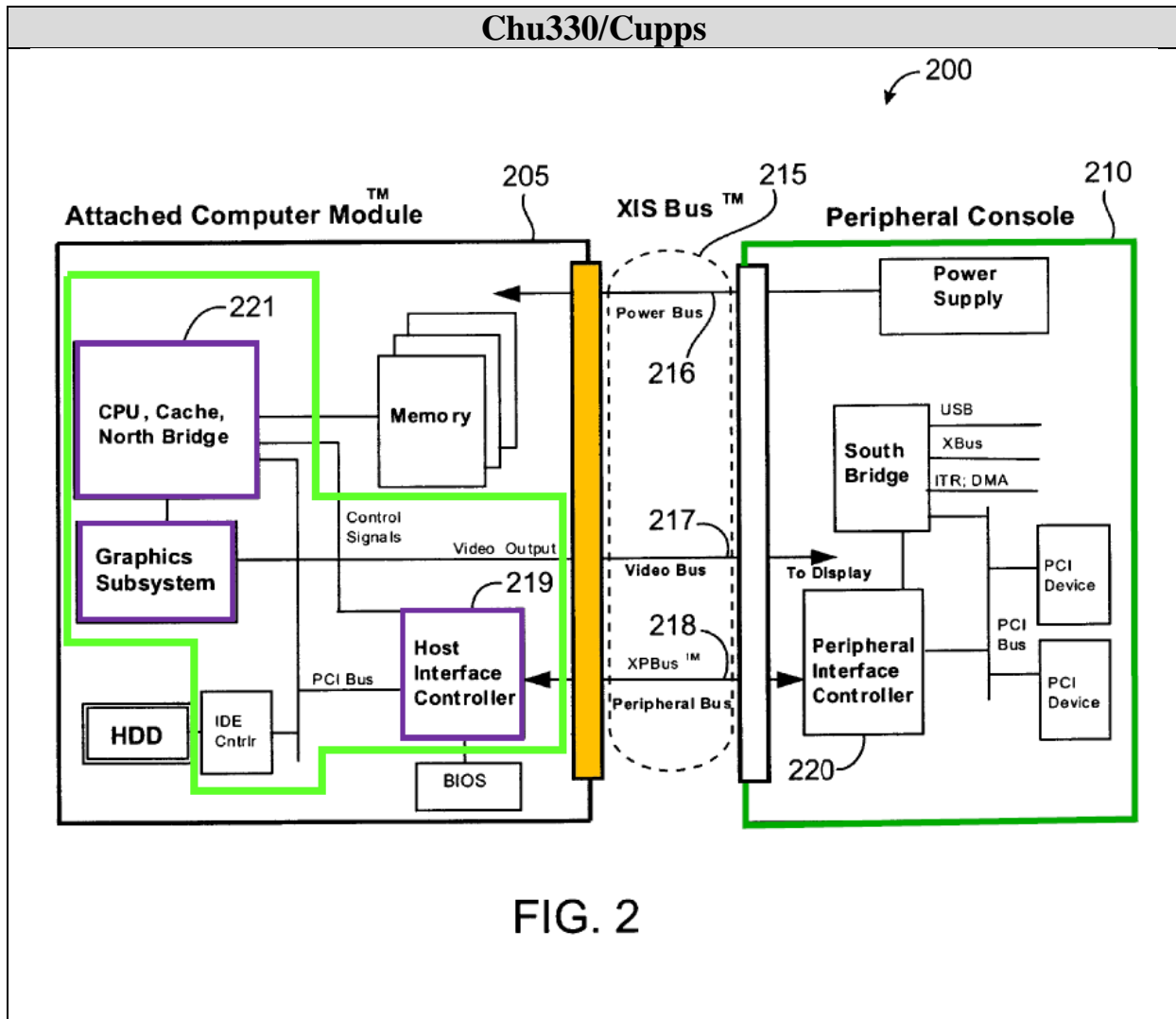


While Figures 3D and 3E do not explicitly show the **GMCH 321** shown in Figure 3C, a POSITA would have understood that the functionality of the **GMCH 321** would also have been integrated into the **integrated circuit chip** shown in Figures 3D and 3E. For example, Cupps makes clear that “display 307 is controlled by display controller 308,” and is “driven by its [] **82815 Graphics Memory and Controller Hub (GMCH) chip**.” Ex-1004, [0105], [0108]. Moreover, Figures 4A and 4D show that the **processor 320** displays data on LCD 307 utilizing the **graphics controller 321** *and* the display controller 308. *See id.*, [0109]-[0110], [0114] (“The **Graphics Memory Controller, FIG. 4D, 321 and FIG. 3C, 321**, then sends the output display data in a 24 bit format, and is passed through the ASIC I/O ... At this point, the user is now seeing a representation of a PC desktop, FIG. 4E, on the LCD, FIG. 3C, 307, and FIG. 4D, 307.”); *see also id.*, [0164] (“The logic ... referenced in FIGS. 3C and 4D, would become part the integrated circuit for the **display and memory controller 431 and 432** of the **Dual Core Processor 410**.”). *See* Ex-1002, ¶118.





A POSITA would have been motivated to combine the teachings of Chu330 and Cupps to integrate Chu330's **CPU**, **graphics controller**, and **HIC in a single chip**, as shown below. See Ex-1002, ¶¶111-122.



*First*, Chu330 teaches that low power consumption is an important design consideration for its computer system. See Ex-1003, 2:10-15 (“It is desirable to use a low voltage differential signal (LVDS) channel in the computer system of the

present invention because an LVDS channel is more cable friendly, faster, *consumes less power*...”). A POSITA would have understood that the power consumption of the ACM can be further reduced by integrating ACM’s internal components in a single chip. In fact, Cupps explicitly teaches such well-known benefits. *See* Ex-1004, [0015] (“Since they are commonly integrated in one processor integrated circuit, ... thereby *improving the efficiency and power conservation of the device*.”); *see also id.*, [0069] (“The benefits ... include ... *improved power efficiency*...”). *See* Ex-1002, ¶¶119-120.

*Second*, a POSITA would have understood that integration leads to management efficiencies, increased performance, and smaller footprint. *See* Ex-1004, [0015] (“[s]ince they are commonly integrated in one processor integrated circuit, they share some components and reduce the overall device chip count.”); *see also id.*, [0069] (explains that the benefits of integration include “(a) no power management redundancy; ... (d) improved thermal management, ... (f) increased performance; (g) smaller physical footprint.”). *See* Ex-1002, ¶¶119-120.

A POSITA would also have had a reasonable expectation of success in integrating ACM’s internal components in a single chip by the priority date afforded to RE140. Chu330’s ACM 205 has substantially similar components as Cupp’s system (*e.g.*, Chu330’s CPU 221 and Cupps’ processor 320/421, Chu330’s graphic subsystem and Cupp’s graphics controller 321/431-432, Chu330’s host interface

controller 219 and Cupps' I/O controller 322/436-441). Cupps teaches that it was well-known to integrate those components onto a single chip with the expectation of achieving various benefits. Accordingly, a POSITA would have had a reasonable expectation of success in integrating Chu330's CPU, graphics subsystem (controller), and HIC in a single chip. See Ex-1002, ¶122.

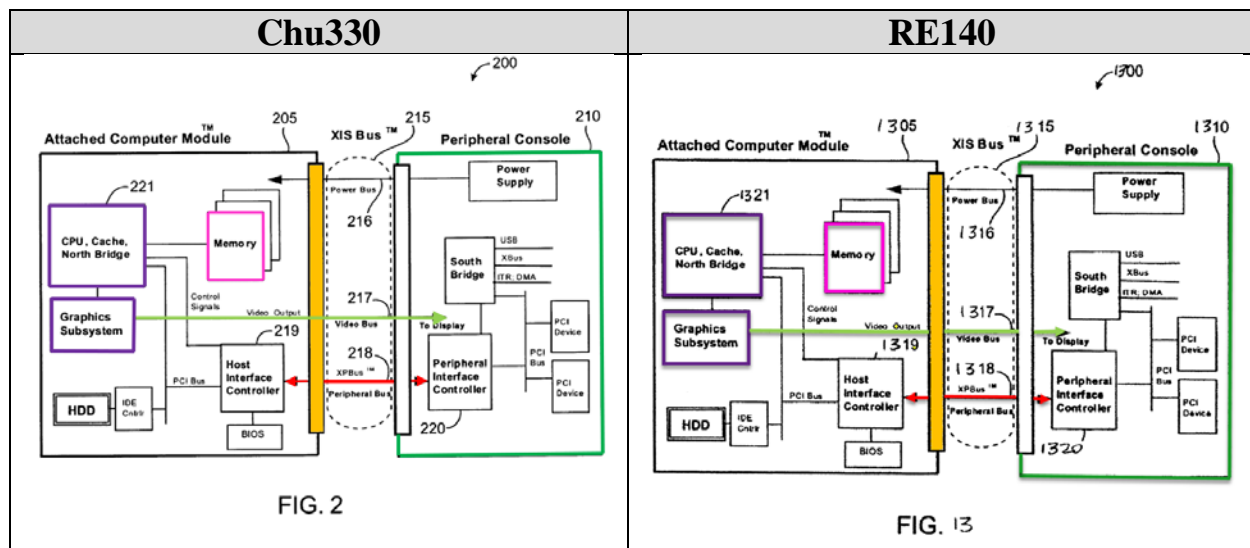
In addition to the above express motivations to combine (*see* MPEP §2143(G)), combining Chu330 with Cupps to integrate Chu330's CPU, graphics subsystem (controller), and HIC in a single chip would have merely amounted to combining prior art elements (*e.g.*, Chu330's CPU, graphics subsystem (controller), and HIC) according to known methods (*e.g.*, integrating in a single chip as taught by Cupps) to yield predictable results of forming a single chip with the expected benefits of, for example, power and management efficiencies and increased performance (*see* MPEP §2143(A)) and amounted to using known integration techniques to improve Chu330's similar system in the same way (*see* MPEP §2143(C)). See Ex-1002, ¶¶119-122.

Accordingly, Chu330 in combination with Cupps renders obvious this limitation by combining “the functionality of embedded and non-embedded processors with controllers [such as graphics controllers]... onto one integrated circuit,” Ex-1004, [0163], [0068], [0221], to obtain “an integrated Central

**Processing Unit (CPU) with a graphics controller in a single chip.”** See Ex-1002, ¶¶111-122.

- iii. [14b] connecting a **Differential Signal channel** directly to the **integrated CPU** and **graphics controller** to output **video data**;

Chu330 discloses a **graphics controller** that outputs **video data**. For example, as shown below, Figure 2 of Chu330 shows a “[v]ideo [o]utput” from the **graphics controller** over a directly-connected **video bus 217**. Chu330 further teaches sending “a **video display signal** from the **graphics controller** to a display.” Ex-1003, claim 3. See Ex-1002, ¶123.



Chu330 further explains that “the video bus 217 transmits ... **digital video signals** (such as ... **Transition Minimized Differential Signaling (TMDS) signals**



for flat panel displays).” Ex-1003, 6:15-22.<sup>14</sup> These **TMDS signals** by definition are conveyed through **differential signal channels**. For example, Figures 28 and 30 show ACM **connector** pin assignments where the TMDS signals for pins E15-E16 are conveyed over a pair of physical lines, as indicated by the **D0+** and **D0-**. Ex-1003, 17:42-67; *see also id.*, 13:38-14:1, Figures 17 and 19 (pins V24-V25). **D0+** and **D0-** refer to Data 0+ and Data 0-, indicating the signal is represented by the difference in voltage between the two lines and that **video data** is conveyed on these lines. *See* Ex-1003, Figure 30. That pair of physical lines together are a **differential signal channel** because Chu330 defines such a pair of physical lines that carry one signal (D0) as a “differential signal line” and because “line” in that context is used interchangeably with a “signal or bit channel.” Ex-1003, 15:57-67. *See* Ex-1002, ¶124.

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<sup>14</sup> *See* equivalent disclosure in Ex-1001, 18:54-65.

Chu330										RE140									
ACM s CMI BUS Connector Plug PIN Position (88 pin):																			
E14	GND	GND	E1	P23	GND	GND	P1												
E15	P&D D0 +	TPA+ /VPD+	E2	P24	PD0 +	PDR0 +	P2												
E16	P&D D0 -	TPA- /VPD-	E3	P25	PD0 -	PDR0 -	P3												
E17	GND	GND	E4	P26	GND	GND	P4												
E18	P&D CLK +	TPB+ /VPCK+	E5	P27	PD1 +	PDR1 +	P5												
E19	P&D CLK -	TPB- /VPCK-	E6	P28	PD1 -	PDR1 -	P6												
E20	GND	1394 Detect	E7	P29	GND	GND	P7												
E21	P&D D1 +	Reserved	E8	P30	PD2 +	PDR2 +	P8												
E22	P&D D1 -	Reserved	E9	P31	PD2 -	PDR2 -	P9												
E23	GND	Reserved	E10	P32	GND	GND	P10												
E24	P&D D2 +	Reserved	E11	P33	PCK +	PCKR +	P11												
E25	P&D D2 -	Reserved	E12	P34	PCK -	PCKR -	P12												
E26	DFF Detect	Config 2	E13	P35	Config 1	Config 0	P13												
V10	GND	V33	V1	P36	GND	GND	P14												
V11	GND	V33	V2	P37	PD3 +	PDR3 +	P15												
V12	GND	V33	V3	P38	PD3 -	PDR3 -	P16												
V13	V33	V33	V4	P39	RSTEP#	RSTEP#	P17												
V14	V33	V33	V5	P40	GREEN VIDEO	RED VIDEO	P18												
V15	V33	V33	V6	P41	GND	GND	P19												
V16	V5	V12	V7	P42	HSYNC	BLUE VIDEO	P20												
V17	V5	V12	V8	P43	VSYNC	GND	P21												
V18	V5	V12	V9	P44	DDC2: SCL	DDC2: SDA	P22												

FIG. 28

Pin No.	Symbol	Signal	Standard	Description
E2	VPD+/TPA+		LVDS or 1394	Video capture port data or 1394
E3	VPD-/TPA-		LVDS or 1394	Video capture port data or 1394
E5	VPCK+/TPA+		LVDS or 1394	Video capture port data or 1394
E6	VPCK-/TPA-		LVDS or 1394	Video capture port data or 1394
E15	D0 +	TMDS	VESA P & D	Data 0 +
E16	D0 -	TMDS	VESA P & D	Data 0 -
E18	CLK +	TMDS	VESA P & D	Clock +
E19	CLK -	TMDS	VESA P & D	Clock -
E21	D1 +	TMDS	VESA P & D	Data 1 +
E22	D1 -	TMDS	VESA P & D	Data 1 -
E24	D2 +	TMDS	VESA P & D	Data 2 +
E25	D2 -	TMDS	VESA P & D	Data 2 -
E13	Config 2			Configuration bit 2
E26	Config 3			Configuration bit 3
E1, E4, E14, E17, E20, E23	GND		GND	Ground

E7	Reserved			Reserved
E8	Reserved			Reserved
E9	Reserved			Reserved
E10	TV-CV/reserved		NTSC	TV Composite Video or reserved
E11	SV Y/reserved		Super Video	SV Luminance or reserved
E12	SV C/reserved		Super Video	SV Chrominance or reserved

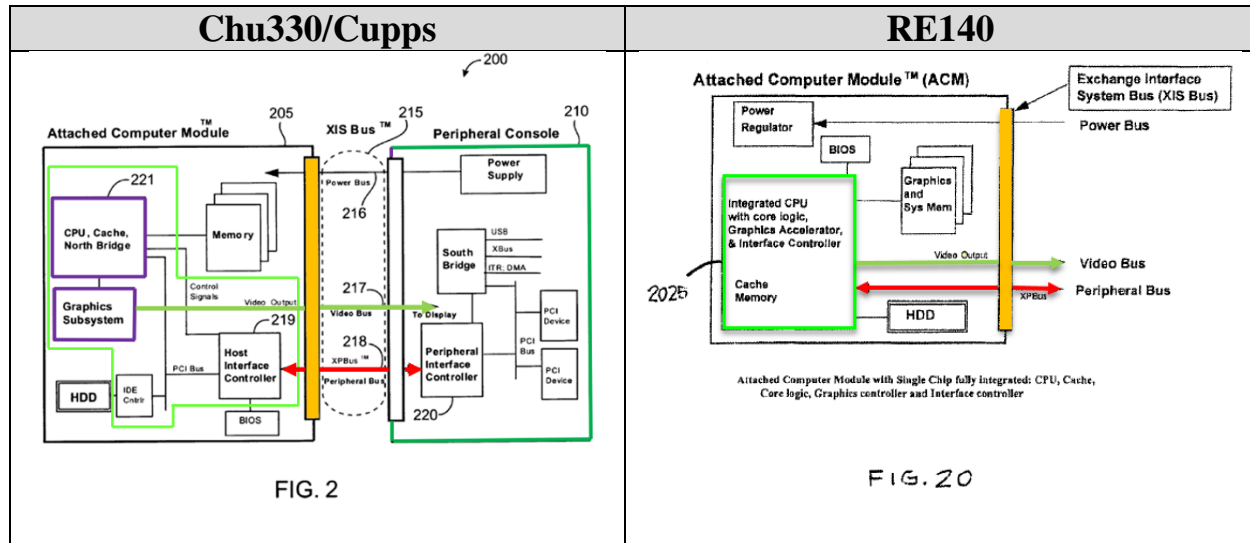
FIG. 30

Pin No.	Symbol	Signal	Standard	Description
V2	Red Video	Analog		Video
V4	Green Video	Analog		Video
V6	Blue Video	Analog		Video
V8	HSYNC			Horizontal Sync
V9	VSING			Vertical Sync
V11	DDC2 SCL		VESA DDC std 2	DDC Clock
V12	DDC2 SDA		VESA DDC std 2	DDC Data
V14	TV-CV/CNTL 0			TV Composite Video
V15	SV Y/CNTL 1		Super Video	SV Luminance or Control 1
V16	SV C/CNTL 2		Super Video	SV Chrominance or Control 2
V24	D0 +	TMDS	VESA P & D	Data 0 +
V25	D0 -	TMDS	VESA P & D	Data 0 -
V27	CLK +	TMDS	VESA P & D	Clock +
V28	CLK -	TMDS	VESA P & D	Clock -
V30	D1 +	TMDS	VESA P & D	Data 1 +
V31	D1 -	TMDS	VESA P & D	Data 1 -
V33	D2 +	TMDS	VESA P & D	Data 2 +
V34	D2 -	TMDS	VESA P & D	Data 2 -
V37	VPCK +	LVDS		Video Port Pixel Clock +
V38	VPCK -	LVDS		Video Port Pixel Clock -
V40	VPD +	LVDS		Video Port Pixel Data +
V41	VPD -	LVDS		Video Port Pixel Data -
V13	Config 2		3.3v or GND	Configuration bit 2
V35	Config 3		3.3v or GND	Configuration bit 3
V1, V3, V5, V7, V10, V23, V26, V29, V32, V36, V39, V42, V43, V44	GND		GND	Ground

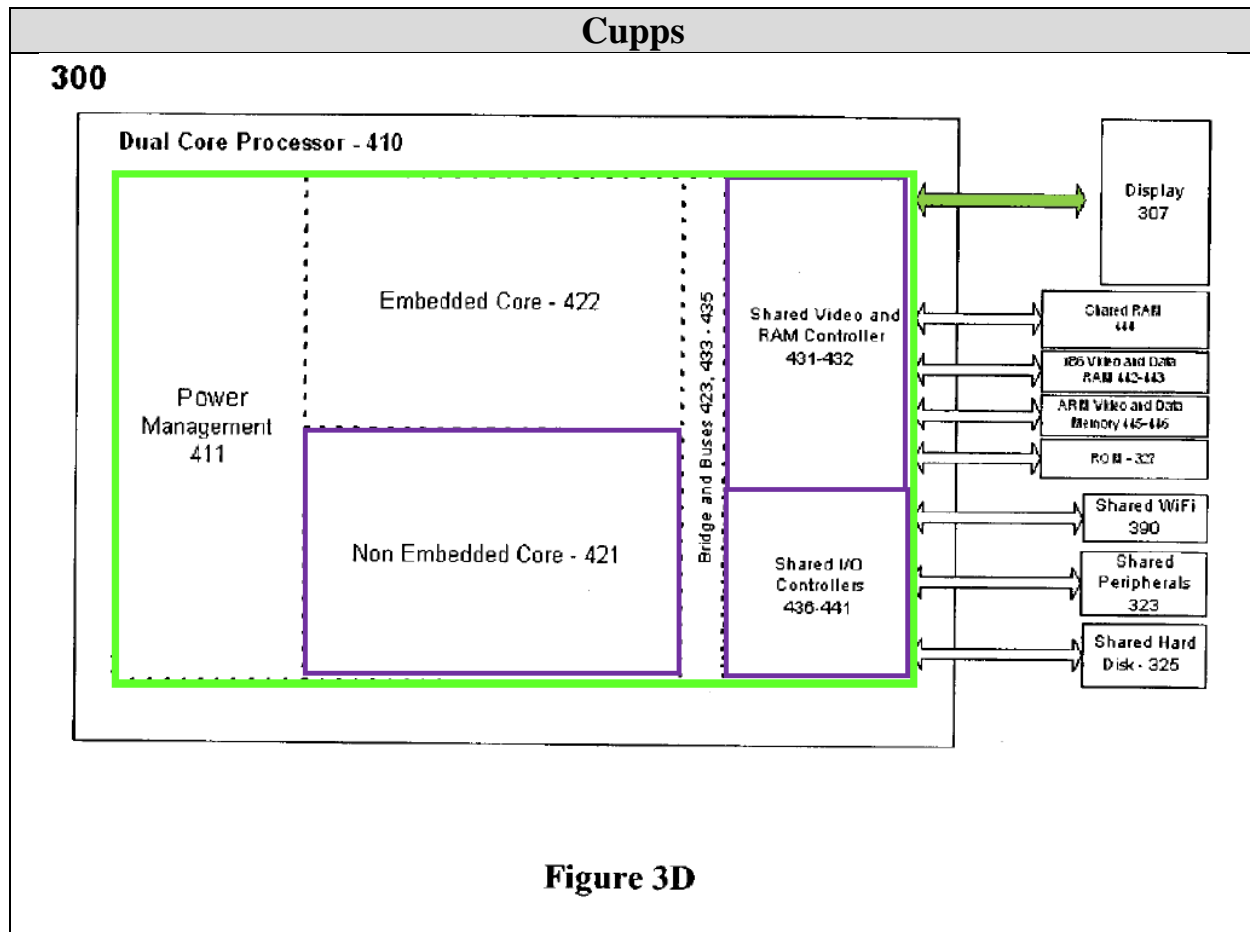
FIG. 22

(Corresponds to Figure 19 of Chu330)

As provided in Section XI.A.2.ii [14a], Chu330 in combination with Cupps provides that the **CPU, graphics controller**, and **HIC** are integrated in **a single chip**. Since the **graphics controller** is directly connected to a **differential signal channel**, such as for **D0+/D0-**, to output **video data**, the **integrated CPU and graphics controller** is also directly connected to the **differential signal channel** to output **video data**, just like Figure 20 of RE140. *See* Ex-1002, ¶125.



Indeed, Cupps shows a **direct connection** between the **integrated chip 410** and display 307 for outputting **video data**. See Ex-1004, [0105], Figure 3D. See Ex-1002, ¶126.



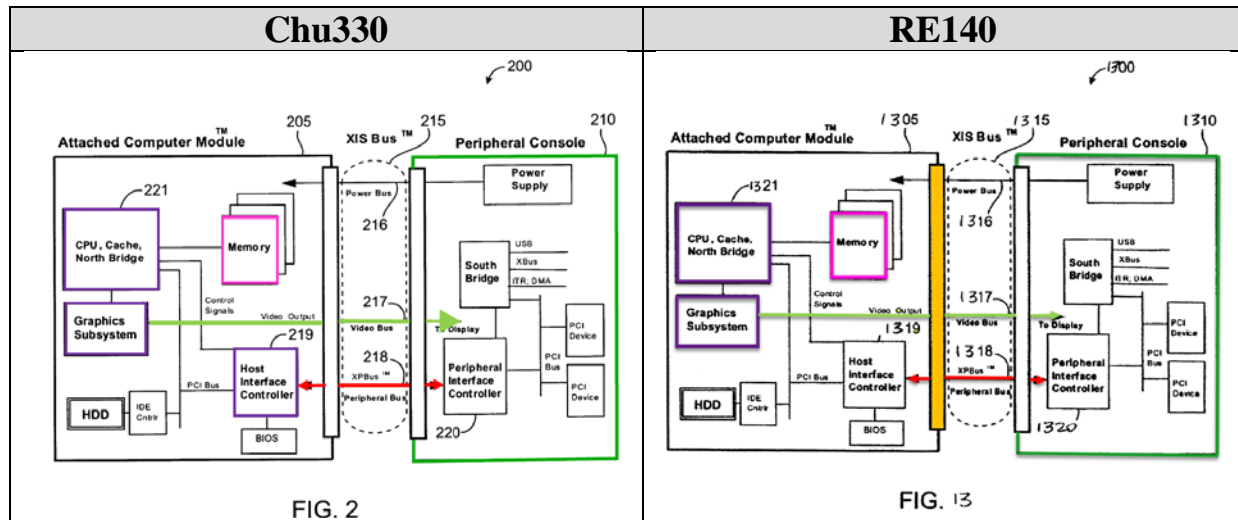
- iv. [14c] conveying Transition Minimized Differential Signaling (TDMS) [sic] signals through the **Differential Signal channel**;

As explained above in Section XI.A.2.iii [14b], Chu330 discloses this limitation, because the **differential signal channel D0+/-** conveys TDMS signals. See Ex-1002, ¶127.

- v. [14d] connecting **memory** directly to the **integrated CPU and graphics controller**;

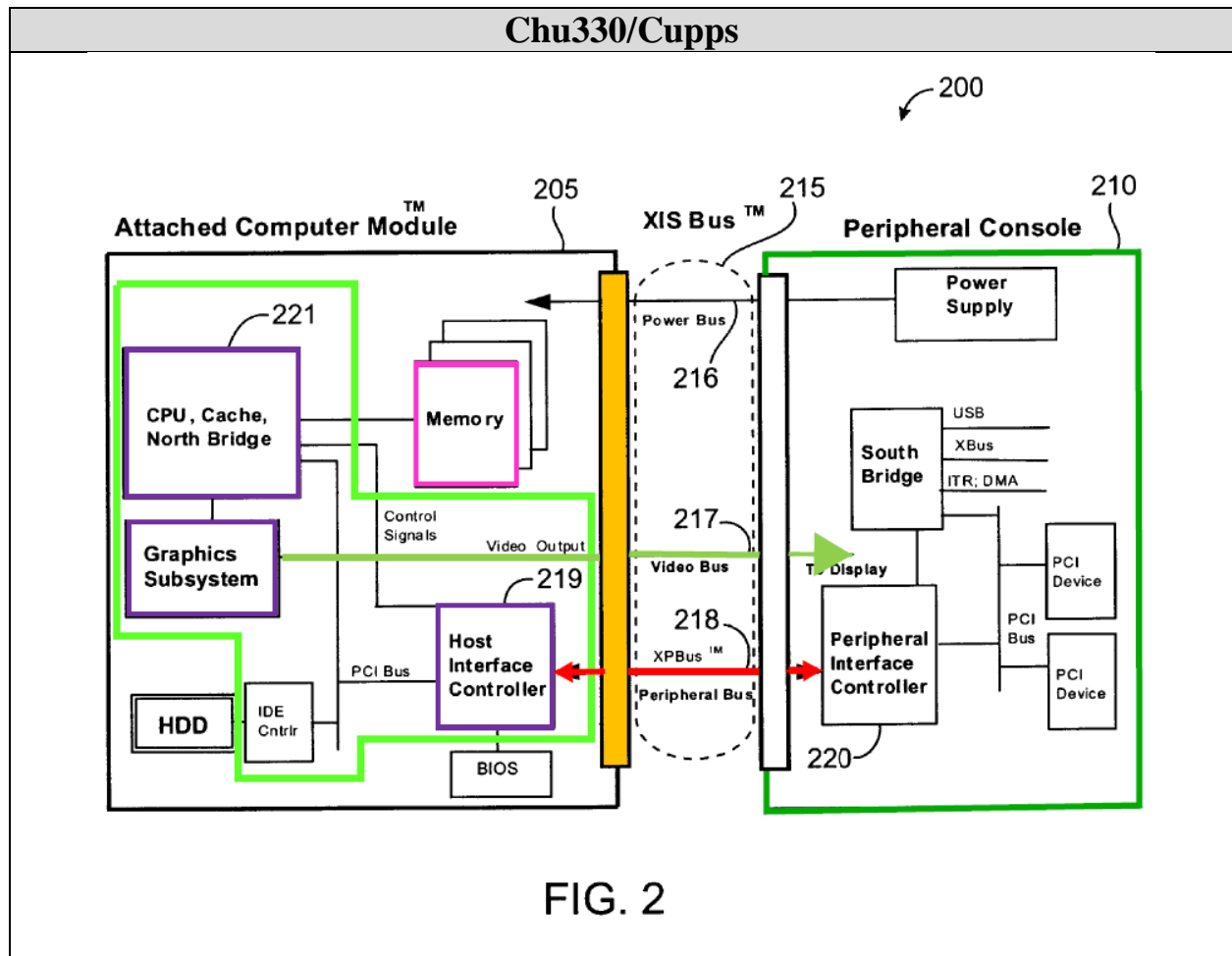
To the extent that RE140 provides written description support for this claim limitation, Figure 2 of Chu330 likewise shows a **memory** directly connected to an

“**integrated unit** 221 that includes a **CPU**.”<sup>15</sup> Ex-1003, 6:26-28, claim 1 (describes the ACM as “including a **central processing unit** and a **main memory**”). See Ex-1002, ¶128.

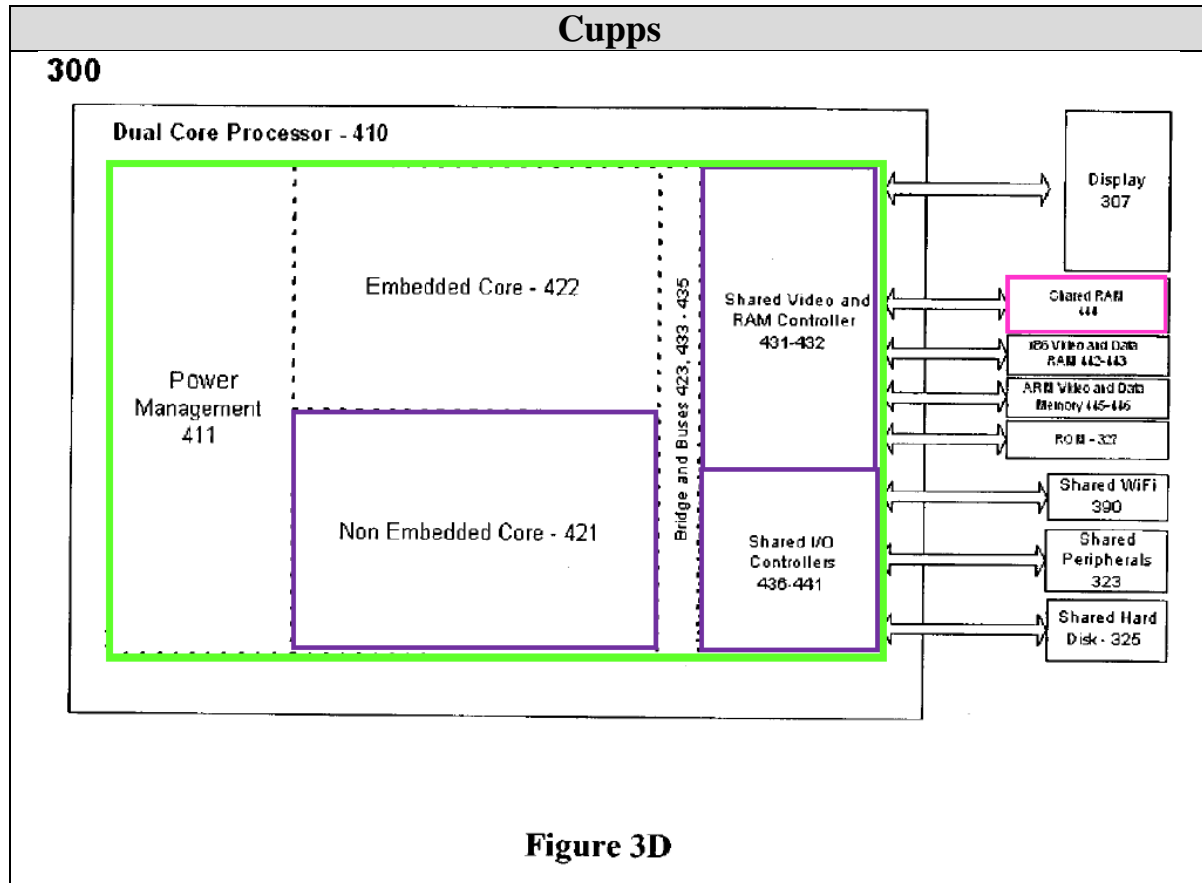


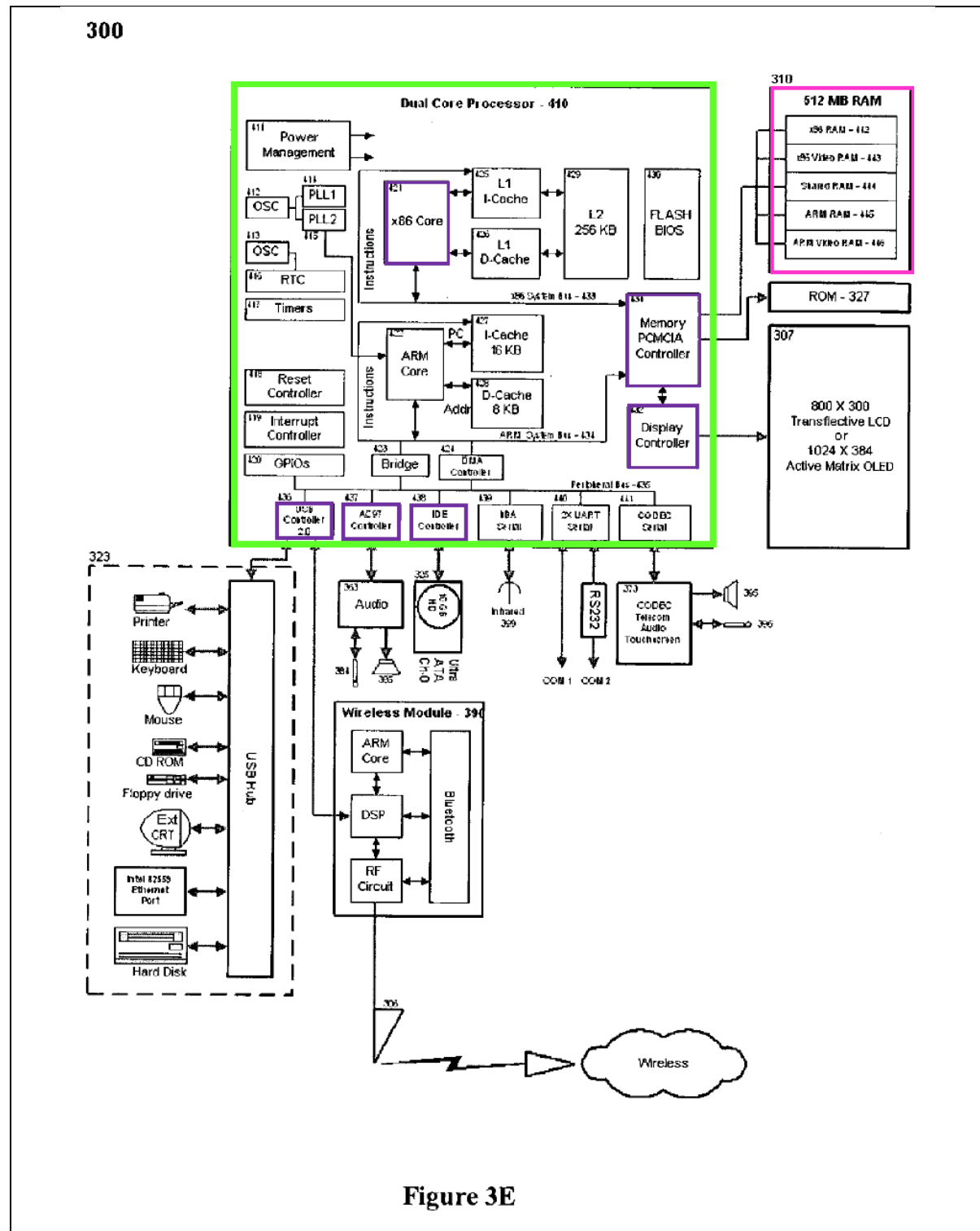
Moreover, as explained in Section XI.A.2.ii [14a], Chu330 in combination with Cupps renders obvious an **integrated CPU and graphics controller**. As shown below, Chu330 in combination with Cupps would result in *directly connecting* the **memory** to the **chip** that forms the **integrated CPU and graphics controller**. See Ex-1002, ¶129.

<sup>15</sup> See equivalent disclosure in Ex-1001, Figure 13.



Indeed, Cupps teaches having **memory** (e.g., **RAM 310, 444**) directly connected to **processor 410** as shown in Figures 3D and 3E. *See, e.g.*, Ex-1004, [0076] (“SDRAM 310 may serve as the main memory for devices 302 and 320 for use by computer programs running on their respective operating systems.”), [0081], [0084], [0173]. *See* Ex-1002, ¶130.







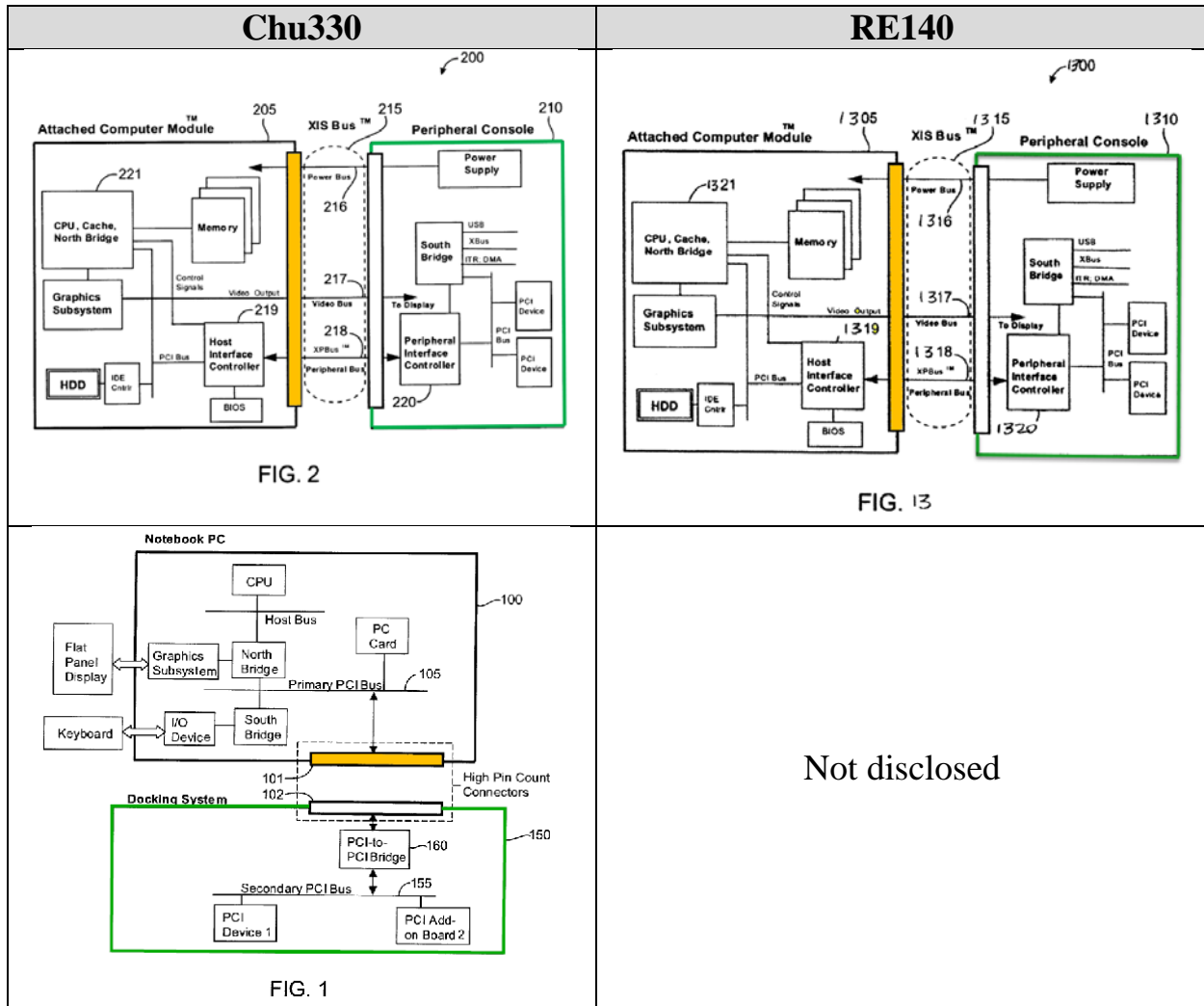
vi. [14e] providing a **connector** for the computer for connection to a **console**; and

Chu330 discloses this limitation. Figure 2 of Chu330 shows a **rectangular box** that provides connection from the ACM to the **PCON** through power bus 216, video bus 217, and XPBus 218. *See* Ex-1003, 6:7-11; *see also id.*, 6:15-25.<sup>16</sup> A POSITA would have understood the **rectangular box** to depict a **connector**, because Figure 1 identifies a similar rectangular box as a “**connector**.” *See* Ex-1003, 1:24-31 (“high pin count connectors 101 and 102”).<sup>17</sup> Like Figure 1, the **rectangular box** in Figure 2 provides the interface between **ACM 205** and **PCON 210**. Hence, the **connector** in Figure 2 provides connection for the ACM to the **PCON 210** (“**console**”). *See* Ex-1002, ¶131.

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<sup>16</sup> *See* equivalent disclosure in Ex-1001, 18:46-51, 18:54-65.

<sup>17</sup> *See* equivalent disclosure in Ex-1001, 3:15-20.



In fact, as explained above in Section XI.A.1.i [Chu330], Chu330 teaches that details of the ACM and **PCON** are found in Chu185. Indeed, Figure 4 of Chu185 explicitly shows an “**ACM connector component 330**” on the ACM side of the ACM-to-PCON Interconnection 300. Ex-1005, 5:57-59; *see also id.*, 4:33-37, 5:49-52.<sup>18</sup> *See* Ex-1002, ¶132.

<sup>18</sup> *See* equivalent disclosure in Ex-1001, 24:20-22, 22:65-23:2, 24:12-15.

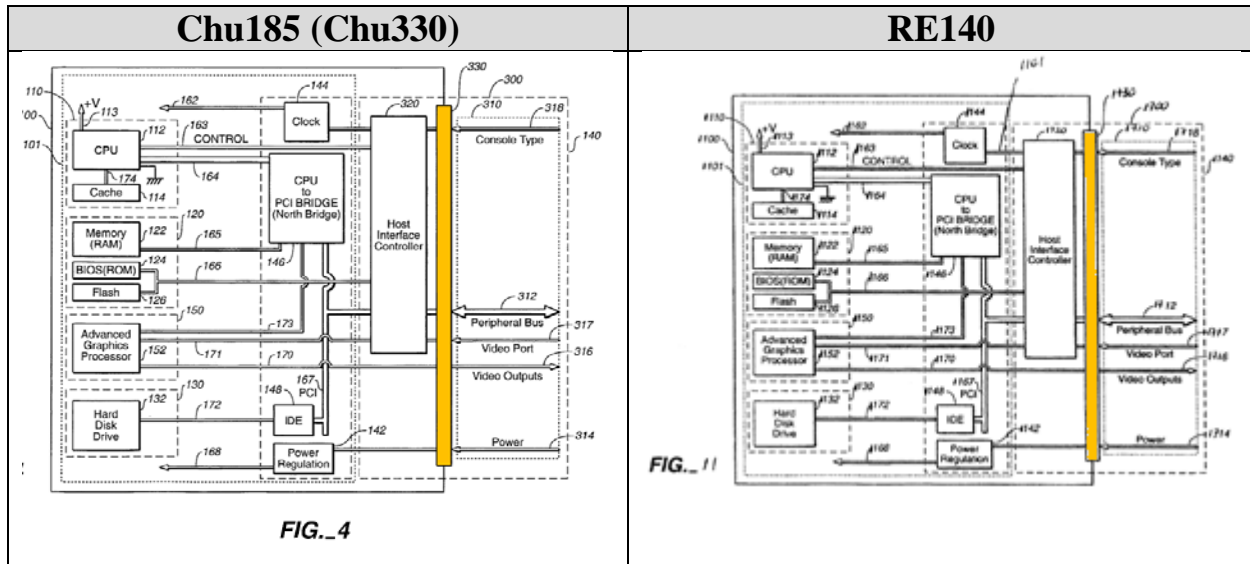


Figure 28 of Chu330 further describes “ACM’s CMI BUS **Connector** Plug PIN Position (88 pin)” that provides connections for data lines and video lines discussed in Figure 2 of Chu330 and Figure 4 of Chu185. Specifically, pins P1-P9, P14-P16, P23-P31, and P36-P38 are for data lines PD0-PD3 and PDR0-PDR3 of the XPBus and pins E14-E25 are for VESA Plug and Display (P&D) TMDS signals for a flat panel display passed on video bus 217. *See* Ex-1003, Figures 27-31, 4:45-60, 6:15-22, 6:36-51, 16:6-18, 17:34-67; *see also id.* Figures 14-16, 17-20 (with pins P18-P19, P40-P41 for PCN, PCNR lines), 4:12-26, 12:58-14:4<sup>19</sup> (discussing connectors between the ACM and the PCON). *See* Ex-1002, ¶133.

<sup>19</sup> *See* equivalent disclosure in Ex-1001, Figures 21-23, 18:54-62, 19:13-15.

### Chu330

**ACM s CMI BUS Connector Plug PIN Position (88 pin):**

E14	GND	GND	E1		P23	GND	GND	P1
E15	P&D D0 +	TPA+ /VPD+	E2		P24	PD0 +	PDR0 +	P2
E16	P&D D0 -	TPA- /VPD-	E3		P25	PD0 -	PDR0 -	P3
E17	GND	GND	E4		P26	GND	GND	P4
E18	P&D CLK +	TPB+ /VPCK+	E5		P27	PD1 +	PDR1 +	P5
E19	P&D CLK -	TPB- /VPCK-	E6		P28	PD1 -	PDR1 -	P6
E20	GND	1394 Detect	E7		P29	GND	GND	P7
E21	P&D D1 +	Reserved	E8		P30	PD2 +	PDR2 +	P8
E22	P&D D1 -	Reserved	E9		P31	PD2 -	PDR2 -	P9
E23	GND	Reserved	E10		P32	GND	GND	P10
E24	P&D D2 +	Reserved	E11		P33	PCK +	PCKR +	P11
E25	P&D D2 -	Reserved	E12		P34	PCK -	PCKR -	P12
E26	DFP Detect	Config 2	E13		P35	Config 1	Config 0	P13
V10	GND	V33	V1		P36	GND	GND	P14
V11	GND	V33	V2		P37	PD3 +	PDR3 +	P15
V12	GND	V33	V3		P38	PD3 -	PDR3 -	P16
V13	V33	V33	V4		P39	RSTEH#	RSTEP#	P17
V14	V33	V33	V5		P40	GREEN VIDEO	RED VIDEO	P18
V15	V33	V33	V6		P41	GND	GND	P19
V16	V5	V12	V7		P42	HSYNC	BLUE VIDEO	P20
V17	V5	V12	V8		P43	VSYN	GND	P21
V18	V5	V12	V9		P44	DDC2: SCL	DDC2: SDA	P22

**FIG. 28**

Petition for *Inter Partes* Review  
U.S. Reissue Patent No. 45,140 (Claims 14-38)

Pin No.	Symbol	Signal	Standard	Description
P2	PDR0 +	LVDS		Peripheral data reverse 0 +
P3	PDR0 -	LVDS		Peripheral data reverse 0 -
P5	PDR1 +	LVDS		Peripheral data reverse 1 +
P6	PDR1 -	LVDS		Peripheral data reverse 1 -
P8	PDR2 +	LVDS		Peripheral data reverse 2 +
P9	PDR2 -	LVDS		Peripheral data reverse 2 -
P11	PCKR +	LVDS		Peripheral clock reverse +
P12	PCKR -	LVDS		Peripheral clock reverse -
P15	PDR3 +	LVDS		Peripheral data reverse 3 +
P16	PDR3 -	LVDS		Peripheral data reverse 3 -
P24	PD0 +	LVDS		Peripheral data 0 +
P25	PD0 -	LVDS		Peripheral data 0 -
P27	PD1 +	LVDS		Peripheral data 1 +
P28	PD1 -	LVDS		Peripheral data 1 -
P30	PD2 +	LVDS		Peripheral data 2 +
P31	PD2 -	LVDS		Peripheral data 2 -
P33	PCK +	LVDS		Peripheral clock +
P34	PCK -	LVDS		Peripheral clock -
P37	PD3 +	LVDS		Peripheral data 3 +
P38	PD3 -	LVDS		Peripheral data 3 -
P13	Config 0	Static	3.3v or GND	Configuration bit 0
P35	Config 1	Static	3.3v or GND	Configuration bit 1
P17	RESTEP#	TTL	3.3v	Reset and Parity Error from console to ACM
P39	RESTEH#	TTL	3.3v	Reset and Parity Error from ACM to console
P18	Red Video	Analog		Video
P40	Green Video	Analog		Video
P20	Blue Video	Analog		Video
P42	HSYNC	TTL		Horizontal Sync
P43	VSYNC	TTL		Vertical Sync
P44	DDC2 SCL	TTL	VESA DDC std 2	DDC Clock
P22	DDC2 SDA	TTL	VESA DDC std 2	DDC Data
P1,P4,P7,P10, P14,P19,P21, P23,P26,P29, P32,P36,P41	GND		GND	Ground

FIG. 29

Petition for *Inter Partes* Review  
U.S. Reissue Patent No. 45,140 (Claims 14-38)

Pin No.	Symbol	Signal	Standard	Description
E2	VPD+/TPA+		LVDS or 1394	Video capture port data or 1394
E3	VPD-/TPA-		LVDS or 1394	Video capture port data or 1394
E5	VPCK+/TPA+		LVDS or 1394	Video capture port data or 1394
E6	VPCK-/TPA-		LVDS or 1394	Video capture port data or 1394
E15	D0 +	TMDS	VESA P & D	Data 0 +
E16	D0 -	TMDS	VESA P & D	Data 0 -
E18	CLK +	TMDS	VESA P & D	Clock +
E19	CLK -	TMDS	VESA P & D	Clock -
E21	D1 +	TMDS	VESA P & D	Data 1 +
E22	D1 -	TMDS	VESA P & D	Data 1 -
E24	D2 +	TMDS	VESA P & D	Data 2 +
E25	D2 -	TMDS	VESA P & D	Data 2 -
E13	Config 2			Configuration bit 2
E26	Config 3			Configuration bit 3
E1, E4, E14, E17,E20,E23	GND		GND	Ground

E7	Reserved			Reserved
E8	Reserved			Reserved
E9	Reserved			Reserved
E10	TV-CV/reserved		NTSC	TV Composite Video or reserved
E11	SV Y/reserved		Super Video	SV Luminance or reserved
E12	SV C/reserved		Super Video	SV Chrominance or reserved

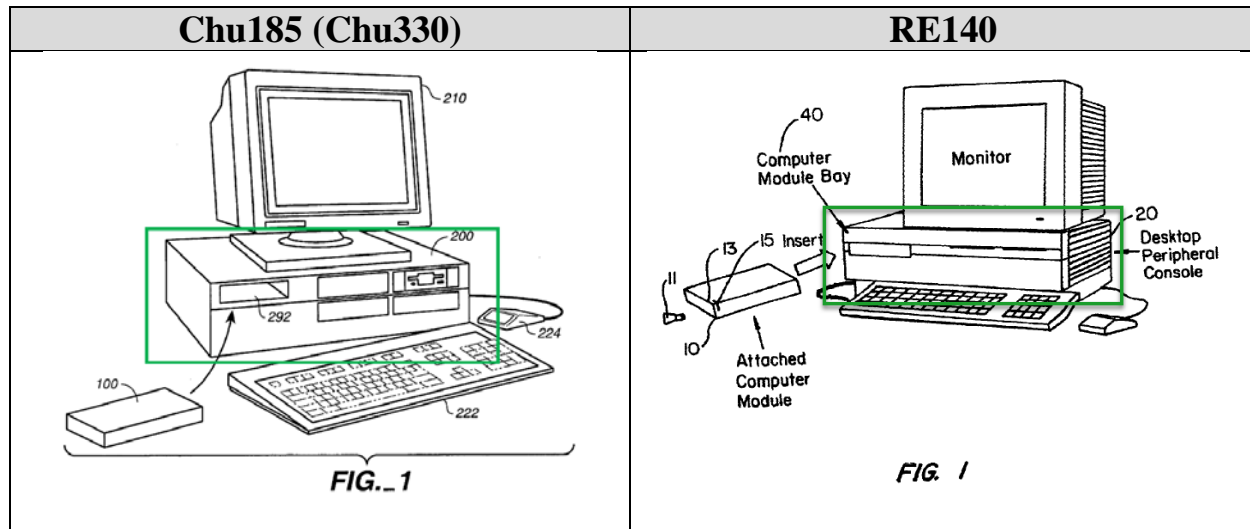
FIG. 30

	Symbol	Signal	Data Rate	Description
1	PD0 RTN			GND
2	PD0 +	Synch. To PCK	6 x clock rate	Computer to Peripheral LVDS Data 0 +
3	PD0 -			Computer to Peripheral LVDS Data 0 -
4	PD1 RTN			GND
5	PD1 +	Synch. To PCK	6 x clock rate	Computer to Peripheral LVDS Data 1 +
6	PD1 -			Computer to Peripheral LVDS Data 1 -
7	PD2 RTN			GND
8	PD2 +	Synch. To PCK	6 x clock rate	Computer to Peripheral LVDS Data 2 +
9	PD2 -			Computer to Peripheral LVDS Data 2 -
10	PD3 RTN			GND
11	PD3 +	Synch. To PCK	6 x clock rate	Computer to Peripheral LVDS Data 3 +
12	PD3 -			Computer to Peripheral LVDS Data 3 -
13	PCK RTN			GND
14	PCK +	Clock	Clock rate	Computer to Peripheral LVDS Clock +
15	PCK -			Computer to Peripheral LVDS Clock -
16	PDR0 RTN			GND
17	PDR0 +	Synch. To PCKR	6 x clock rate	Peripheral to Computer LVDS Data 0 +
18	PDR0 -			Peripheral to Computer LVDS Data 0 -
19	PDR1 RTN			GND
20	PDR1 +	Synch. To PCKR	6 x clock rate	Peripheral to Computer LVDS Data 1 +
21	PDR1 -			Peripheral to Computer LVDS Data 1 -
22	PDR2 RTN			GND
23	PDR2 +	Synch. To PCKR	6 x clock rate	Peripheral to Computer LVDS Data 2 +
24	PDR2 -			Peripheral to Computer LVDS Data 2 -
25	PDR3 RTN			GND
26	PDR3 +	Synch. To PCKR	6 x clock rate	Peripheral to Computer LVDS Data 3 +
27	PDR3 -			Peripheral to Computer LVDS Data 3 -
28	PCKR RTN			GND
29	PCK +	Reverse Dir. Clock	Clock rate	Peripheral to Computer LVDS Clock +
30	PCK -			Peripheral to Computer LVDS Clock -
31	RESTEH#	Host to Peripheral	asynchronous	Reset & Error signal
32	RESTEP#	Peripheral to Host	asynchronous	Reset & Error signal

FIG. 31

Finally, an exemplary **PCON** is shown in Figure 1 of Chu185. Ex-1005, 3:46-52 (“FIG. 1 depicts an exemplary desktop **peripheral console [PCON]** and attached computing module [ACM]. ... The **PCON** also provides connections for a display monitor, a keyboard, and a mouse.”); *see also id.*, 4:47-48 (“ACM 100”), 4:1-2; *see also* Section XI.A.1.i [Chu330]. As shown, “a chassis that connects several components of the computer system” is taught by Chu185 (hence Chu330). *Id.*,

4:33-46 (**PCON** connecting “components” of computer system), Fig. 3. *See* Ex-1002, ¶134.



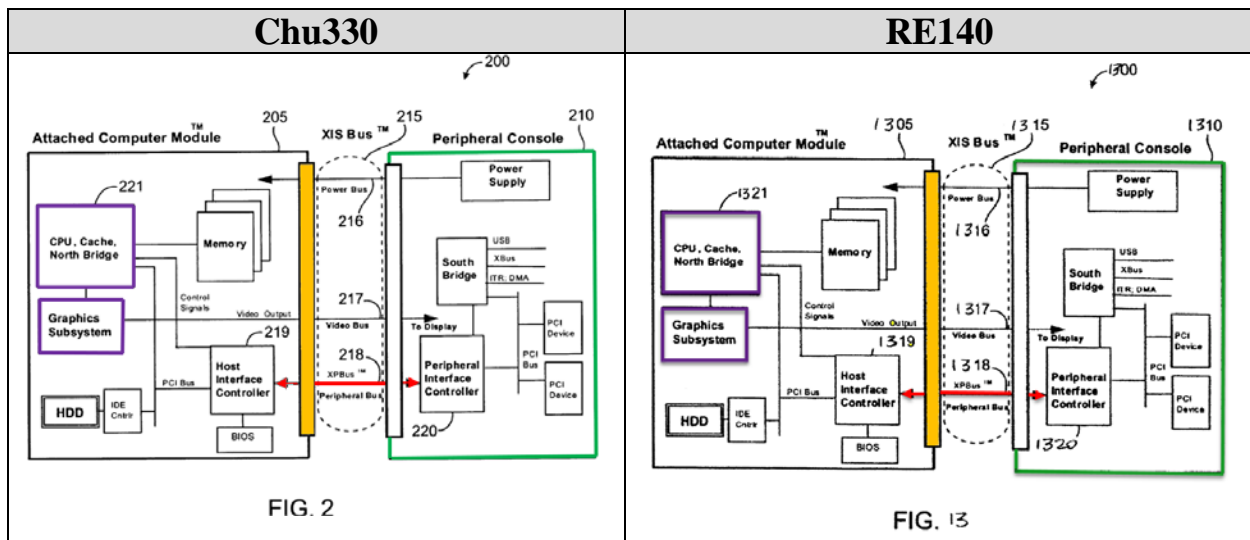
- vii. [14f] providing a **first Low Voltage Differential Signal (LVDS) channel** to couple to the **connector**, the first LVDS channel comprising two unidirectional, serial bit channels that transmit data in opposite directions.<sup>20</sup>

Chu330 discloses this limitation. As explained above in Sections XI.A.2.iii [14b] and XI.A.2.vi [14e], Chu330 teaches a **connector**. As shown below in Figure

<sup>20</sup> ACQIS represented that Chu330 provides support for “said LVDS channel comprises a first plurality of unidirectional, differential signal pairs to convey data in a first direction and a second plurality of unidirectional, differential signal pairs to convey data in a second, opposite direction” “at FIG. 23 and col. 15, line 10 to col. 16, line 5.” Ex-1012, 14.



2 of Chu330, Chu330 teaches an exchange interface system (XIS) bus used for communication between the ACM 205 and the **PCON 210** that is coupled to the **connector**. See Ex-1003, 6:7-11 (“The XIS bus 215 includes power bus 216, video bus 217 and peripheral bus (XPBus) 218, which is also referred to as an interface channel.”).<sup>21</sup> “The **PCON** also provides connections for a display monitor, a keyboard, and a mouse.” Ex-1005, 3:46-52. Chu330 explains that “the interface channel [XPBus] allows using **LVDS channels**.” Ex-1003, 2:36-38.<sup>22</sup> Accordingly, Chu330 teaches providing a **LVDS channel** to couple to the **connector**. See Ex-1002, ¶135.



<sup>21</sup> See equivalent disclosure in Ex-1001, 18:48-51.

<sup>22</sup> See equivalent disclosure in Ex-1001, 17:38-39.

Chu330 also explains that the “interface channel includes two sets of unidirectional serial bit channels which transmit data in opposite directions such that one set of bit channels transmits serial bits from the HIC to the PIC while the other set transmits serial bits from the PIC to the HIC.” Ex-1003, 3:18-23.<sup>23</sup> Specifically, Figure 24 of Chu330 shows “a block diagram ... of the HIC and PIC of the present invention.” Ex-1003, 16:6-8, 6:36-37.<sup>24</sup> As shown, the XPBus includes multiple “lines.” See Ex-1003, 16:6-23, 6:47-51 (“PCK line 591 and PD[0::3] ... PCKR lines 593, the PDR[0::3]....” ).<sup>25</sup> See also *id.*, Figure 5. See Ex-1002, ¶¶136-137.

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<sup>23</sup> See equivalent disclosure in Ex-1001, 18:19-24.

<sup>24</sup> See equivalent disclosure in Ex-1001, 5:17-20.

<sup>25</sup> See equivalent disclosure in Ex-1001, 20:34-37.

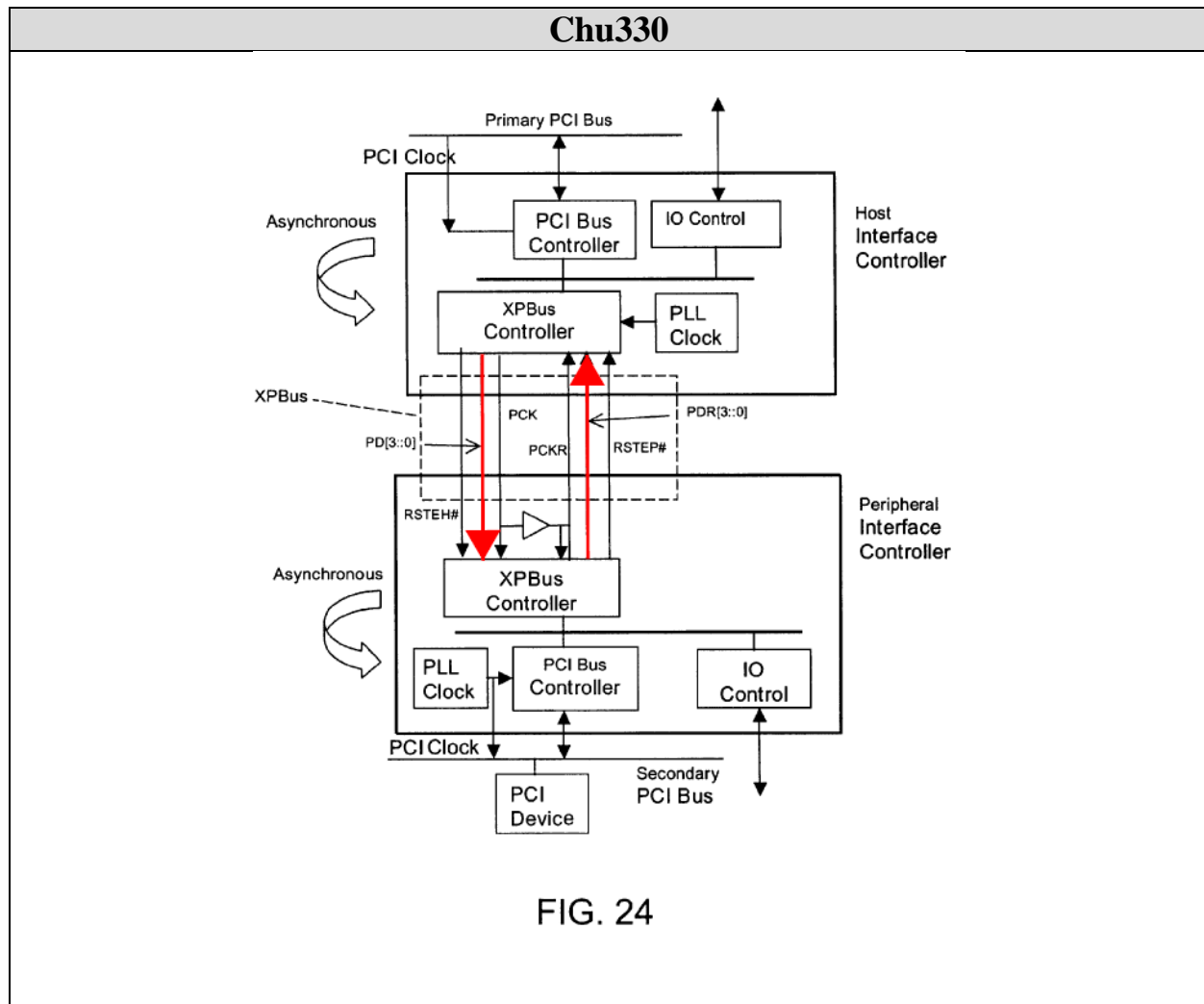
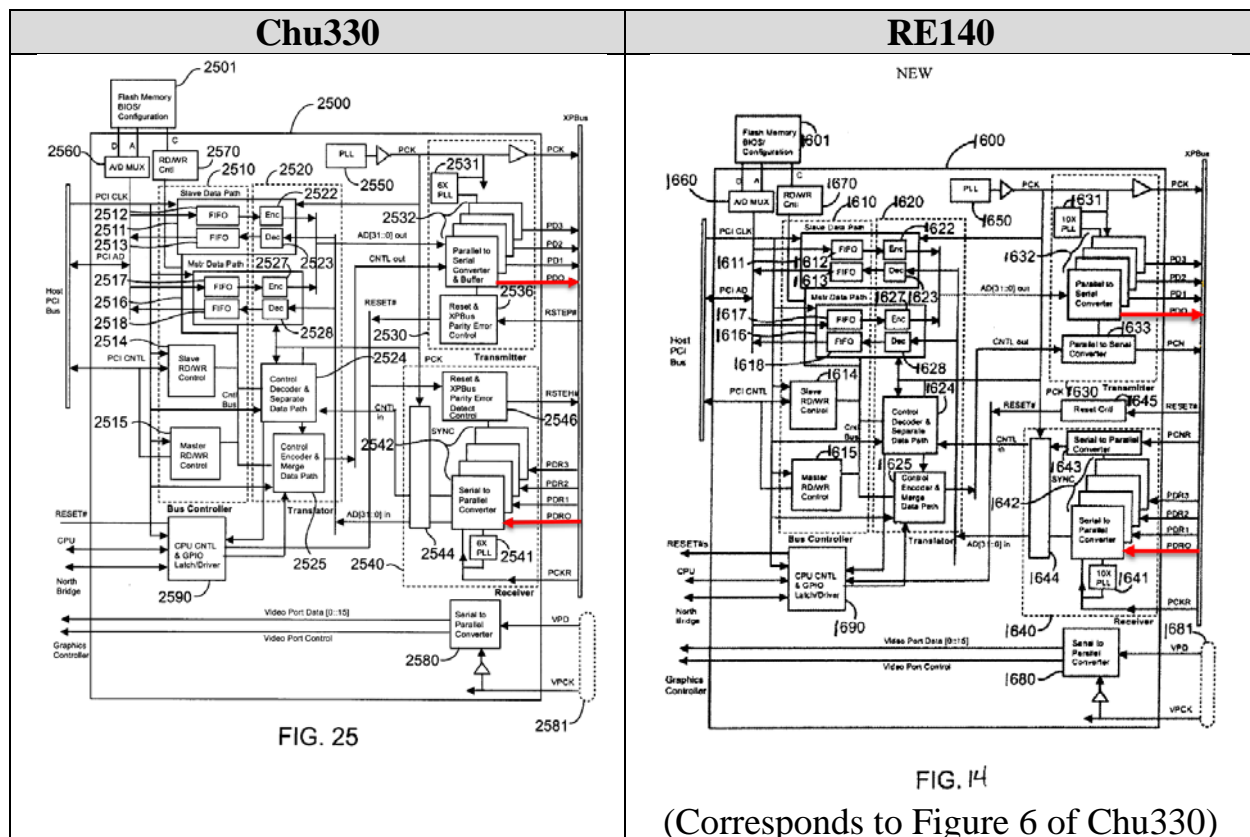


Figure 25 of Chu330 shows a more “detailed block diagram[] of [just] the HIC shown in FIG. 24.” Ex-1003, 16:24-25. “HIC 2500 shown in FIG. 25 is, other than for a few difference [sic], identical to HIC 600 shown in FIG. 6. ... and reference to the description of elements in HIC 600 may be made to understand the function of the corresponding elements in HIC 2500.” Ex-1003, 16:24-17:13, 7:28-10:8,

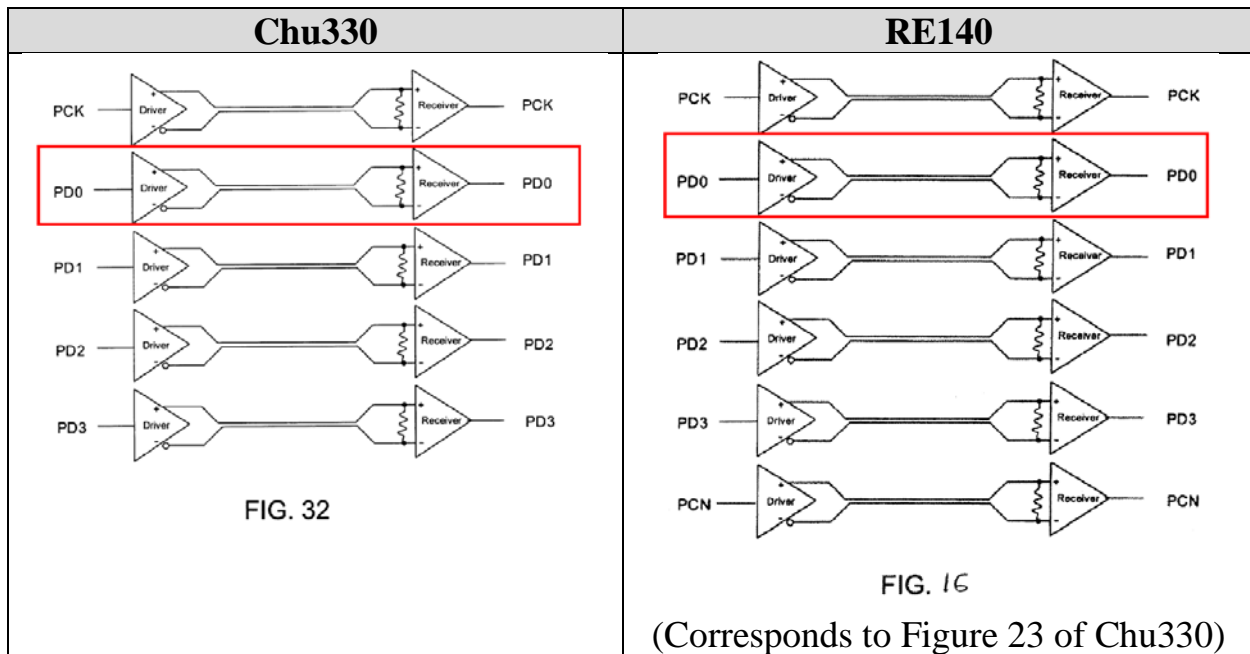
Figures 6, 25.<sup>26</sup> The **first LVDS channel** includes data lines, such as **PD0** and **PDR0**. For example, Chu330 explains that a “differential communication channel [defined in claim 1 between the ACM and PCON] comprises **an LVDS channel**,” and the “differential signal channel comprises at least two pairs of differential signal lines.” Ex-1003, claims 1, 9, and 12. *See* Ex-1002, ¶138.



As shown below, “FIG. 32 is a schematic diagram of the lines PCK and **PD0** to PD3. These lines are unidirectional LVDS lines for transmitting signals from HIC

<sup>26</sup> *See* equivalent disclosure at Ex-1001, 19:14-58.

2500 to PIC 2600.” Ex-1003, 18:1-3. “Another set of lines, namely PCKR and **PDR0** to PDR3 ... have the same structure as those shown in FIG. 33 [sic], except that they transmit information in the opposite direction from that of those shown in FIG. 32.” Ex-1003, 18:3-10; *see also id.*, 15:10-16:5, Figure 23 (with LVDS PCN, PCNR lines).<sup>27</sup> Chu330 further teaches that the difference in voltage between the “pair of physical lines which together transmit a signal” in the LVDS channel is low. Ex-1003, 2:15-17, 15:57-67.<sup>28</sup> *See* Ex-1002, ¶139.



<sup>27</sup> *See* equivalent disclosure in Ex-1001, 20:14-21:7.

<sup>28</sup> *See* equivalent disclosure in Ex-1001, 20:60-64.

Chu330 teaches the **first LVDS channel**, for example including data lines **PD0** and **PDR0**, has “at least two pairs of differential signal lines.” Ex-1003, claims 9 and 12; *see also id.*, 18:1-10 (**PD0**-PD3 of Fig. 32 are each a “unidirectional LVDS [low voltage differential signal] line[]” and **PDR0**-PDR3 each have “the same structure”), 15:10-22, 15:63-67. Specifically, “[t]he XPBus which includes lines PCK, **PD0** to PD3, ... **PDR0** to PDR3, ... has two sets of unidirectional lines transmitting clock signals and bits in opposite directions. The first set of unidirectional lines includes PCK, **PD0** to PD3 .... The second set of unidirectional lines includes PCKR, **PDR0** to PDR3.” Ex-1003, 15:31-36, 16:25-26, 17:8-13; *see also id.*, 15:10-16:5.<sup>29</sup> *See* Ex-1002, ¶140.

Lines **PD0** and **PDR0**, as part of the XPBus or interface channel, are each referred to as a bit line or serial bit channel and are each a path on which bits are transferred serially between the ACM (HIC) and **PCON** (PIC) of Figs. 2, 5, and 24. *See* Ex-1003, Abstract, 2:60-61, 3:18-25 (“the interface channel includes two sets of unidirectional **serial bit channels**”), 6:7-11, 15:51-16:5, Figs. 2, 5, 24-25, 32. Both **PD0** and **PDR0** are data lines and therefore convey data. *See* Ex-1003, 8:61-67, 9:16-22 (discussing “data lines **PD0**” and “**PDR0**”), 16:25-26, 17:8-13, 18:1-10, Figure 32. *See* Ex-1002, ¶141.

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<sup>29</sup> *See* equivalent disclosure in Ex-1001, 20:14-21:7.

**3. Claim 15**

- i. [15] The method of claim 14 further comprises conveying Universal Serial Bus (USB) protocol information over the **first LVDS channel**.<sup>30</sup>**

As explained in Section XI.A.2.vii [14f], Chu330 describes an XPBus including a **first LVDS channel**.

Further, Chu330 discloses the purported transmission of data packets in accordance with a USB protocol over the claimed **first LVDS channel**. For example, Chu330 teaches that “[t]he bits sent in the first nibble of each data packet indicate the type of that data packet.” Ex-1003, 19:22-25, Figures 33-35.<sup>31</sup> In particular, Chu330 teaches that “[t]he reserved data packet types can be used to support non-PCI bus transactions, *e.g.*, USB transactions.” Ex-1003, 19:13-15.<sup>32</sup> In

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<sup>30</sup> ACQIS represented that Chu330 provides support for “serial bit lines transmitting data packets in [sic] USB protocol” at 16:1-5. *See* Ex-1022, 7. The alleged support recites “[a] bit based line (*i.e.*, a bit line) is a line for transmitting serial bits. Bit based lines typically transmit bit packets and use a serial data packet protocol. Examples of bit lines include ... a Universal Serial Bus (USB) line.” Ex-1003, 16:1-5.

<sup>31</sup> *See* equivalent disclosure in Ex-1001, 21:25-28.

<sup>32</sup> *See* equivalent disclosure in Ex-1001, 21:24-25.

other words, Chu330 teaches conveying USB protocol information over and through the XPBus (including the **first LVDS channel**) by utilizing the first nibble within the data packet. *See* Ex-1002, ¶¶142-143.

Chu330		RE140	
ID bits (P0 P1 P2 P3)	Data Packet Type	ID bits (P0 P1 P2 P3)	Data Packet Type
X X 0 0	PCI 1st address/data segment	X X 0 0	PCI 1st address/data segment
X X 1 0	PCI 2nd address/data segment	X X 1 0	PCI 2nd address/data segment
0 0 0 1	Control 1st segment with PCI response	0 0 0 1	Control 1st segment with PCI response
1 0 0 1	Control 1st segment without PCI response	1 0 0 1	Control 1st segment without PCI response
0 1 0 1	Control 2nd segment with PCI response	0 1 0 1	Control 2nd segment with PCI response
1 1 0 1	Control 2nd segment without PCI response	1 1 0 1	Control 2nd segment without PCI response
0 0 1 1	Reserved	0 0 1 1	Reserved
1 0 1 1	Reserved	1 0 1 1	Reserved
0 1 1 1	Initialization	0 1 1 1	Initialization
1 1 1 1	NOOP	1 1 1 1	NOOP

FIG. 35

FIG. 24

#### 4. Claim 16

- i. [16] The method of claim 14 further comprises conveying encoded address and data bits of a Peripheral Component Interconnect (PCI) bus transaction in serial form over the **first LVDS channel**.<sup>33</sup>

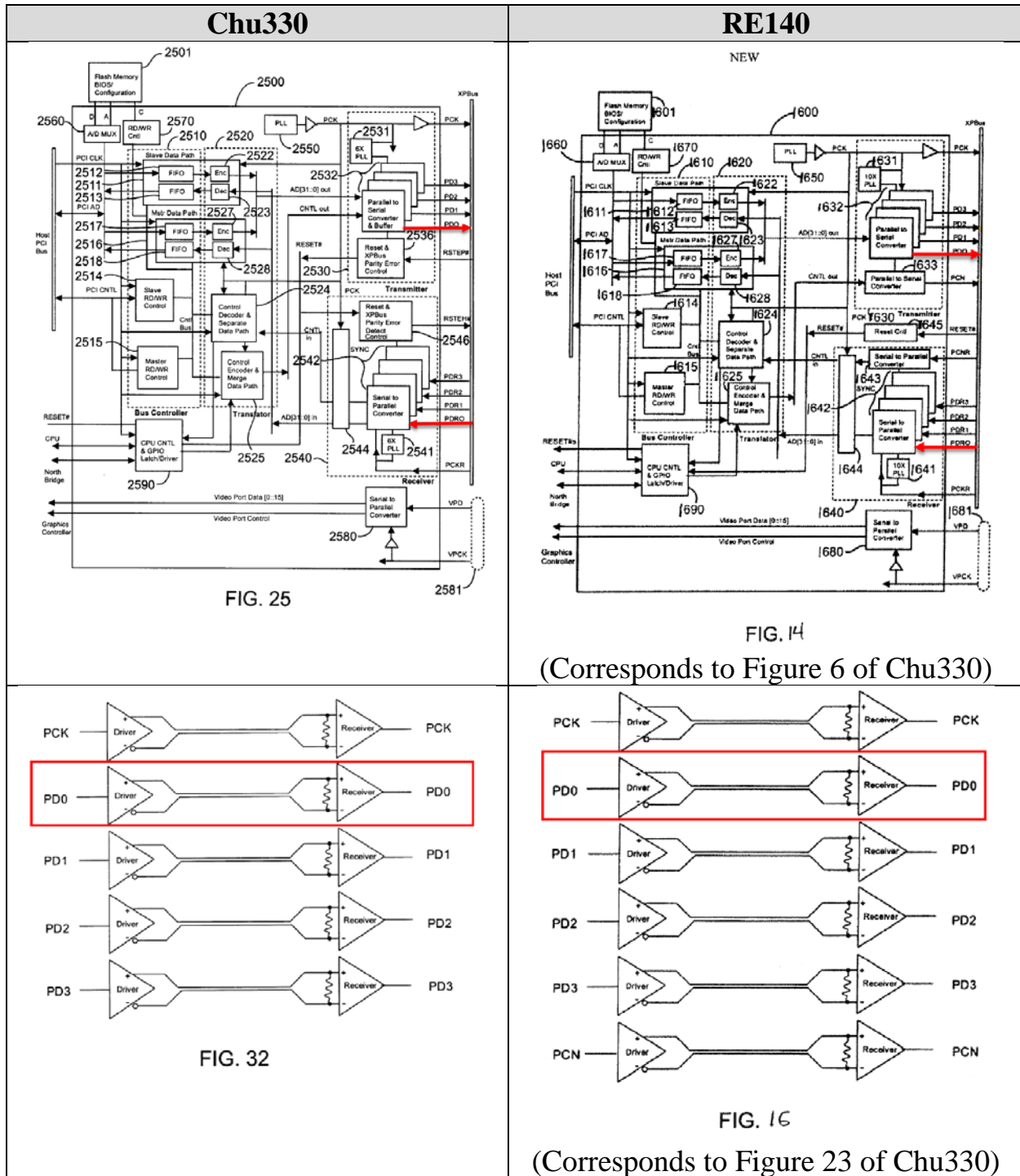
<sup>33</sup> ACQIS represented that the limitation “said LVDS channel ... to convey said encoded Peripheral Component Interconnect bus transaction data” is supported by Chu330 “at FIG. 4; FIG. 6; FIG. 23; col. 6, lines 30-35; col. 7, line 28 to col. 10, line 18; and col. 15, line 10 to col. 16, line 5.” Ex-1012, 13-14. ACQIS further represented that the limitation “said encoded Peripheral Component Interconnect bus transaction data comprises address and data bits of Peripheral Component



Section XI.A.2.vii [14f] discussed in detail how Chu330 teaches a **first LVDS channel** (*e.g.*, including data lines **PD0** and **PDR0**). As discussed above, Chu330 teaches that the “interface channel allows using **LVDS channels** for the interface.” Ex-1003, 2:36-38. *See* Ex-1002, ¶144.

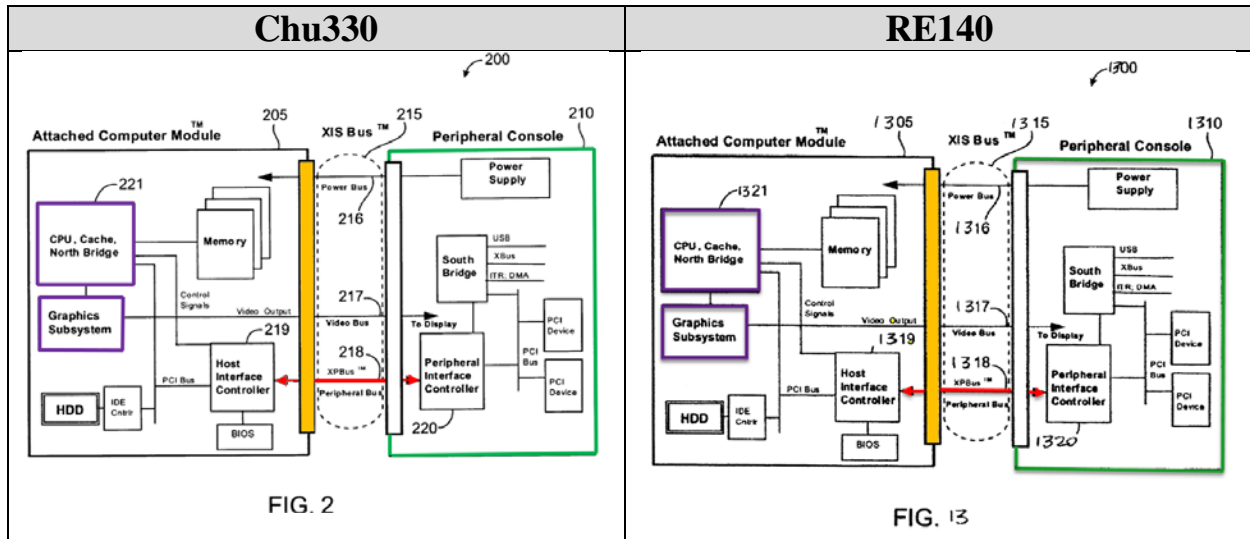
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Interconnect bus transaction in serial form” is supported by Chu330 “at col. 7, line 44 to col. 9, line 43.” Ex-1012, 14.



Chu330 further teaches that the **first LVDS channel** conveys encoded address and data bits of a Peripheral Component Interconnect (PCI) bus transaction in serial

form between the ACM 205 and the PCON 210. Chu330 teaches the “differential signal channel [of claim 1 is] configured to communicate an encoded bit stream comprising PCI bus transactions data bits, system control signal data bits, and peripheral console configuration information data bits, ... separated within the encoded bit stream.” Ex-1003, claim 1. The PCI bus transactions from the ACM are communicated with the PCI Devices that are interconnected through the second PCI bus shown in Figure 2 below. *See* Ex-1003, claim 1 (“a differential signal channel between the computer module and the peripheral console, the differential signal channel configured to communicate an encoded bit stream comprising PCI bus transactions”), claim 14 (“the computer module further comprises a first PCI bus”), claim 15 (“the peripheral console comprises a second PCI bus in electrical communication with the differential signal channel through a second interface controller ... to bridge the first PCI bus to the second PCI bus.”). Chu185 (and hence Chu330) further teaches that the “ACM ... is inserted into the opening of the computer bay ... to interact with the peripheral devices housed in the PCON.” Ex-1005, 3:55-59; *see also id.*, 4:40-44, 5:30-32, 5:59-6:4, 13:1-39, Figures 3-4, 7. Moreover, the PCI bus transactions are in accordance with industry standard PCI Local Bus Specification. *See* Ex-1005, 14:59-61 (“PCI and ISA peripheral busses are industry standards, well known and understood in the art.”). *See* Ex-1002, ¶¶145-146.



Chu330 further teaches that the encoded bits of the PCI bus transaction are transmitted serially from a parallel form. Specifically, Chu330 teaches encoding “PCI address/data (AD) ... bits to a form more suitable for parallel to serial conversion prior to transmittal on the XPBus.” Ex-1003, 7:59-64<sup>34</sup>; *see also id.*, 7:29-30, 16:25-26, 17:8-13 (“elements in HIC 2500 are identical to those in HIC 600 and reference to the description of the elements in HIC 600 may be made to understand the function of the corresponding elements in HIC 2500.”). The “multiplexed parallel A/D bits and some control bits ... are serialized ... into ... bit packets ... then output on *data lines PD0 to PD3* of the XPBus.” Ex-1003, 8:61-65; *see also id.*, 14:5-26 (“The bits transmitted on lines PD0 to PD3 represent 32

<sup>34</sup> See equivalent disclosure in Ex-1001, 19:44-49.

PCI AD[31::0] signals.”), Fig. 21.<sup>35</sup> Chu330 similarly teaches serializing encoded bits into bit packets for conveyance on line PCN. Ex-1003, 8:29-34, 8:65-67; *see also id.*, 16:8-11, 16:35-36. *See* Ex-1002, ¶147.

“Similarly, [with regards to **PDR0-PDR3**,] address and data information from the receivers is decoded ... to a form more suitable for transmission on the host PCI bus.” Ex-1003, 7:64-66<sup>36</sup>; *see also id.*, 16:25-26, 17:8-13. Specifically, “[r]eceiver 640 receives serial bit packets on data lines **PDR0** to PDR3.... [and s]erial to parallel converters 642 convert the serial bit packets received on lines **PDR0** to PDR3 into parallel address/data and control bits [for decoding].” Ex-1003, 9:16-27; *see also id.*, 16:25-26, 17:8-13. Chu330 similarly teaches receiving and converting serial bit packets conveyed on line PCNR into parallel form for decoding. Ex-1003, 8:38-47, 9:27-30; *see also id.*, 16:8-11, 16:35-36. *See* Ex-1002, ¶147.

Chu330 therefore teaches a flow of information in which the bits are transferred in serial form over the **first LVDS channel** between the ACM (HIC) and PCON (PIC) of Figures 2, 5, and 24. *See* Ex-1003, Abstract, 2:60-61, 3:18-25, 6:7-11, 14:16; *see also id.*, 15:51-16:5, 16:65-17:3, 18:33 Fig. 5. *See* Ex-1002, ¶¶146-148.

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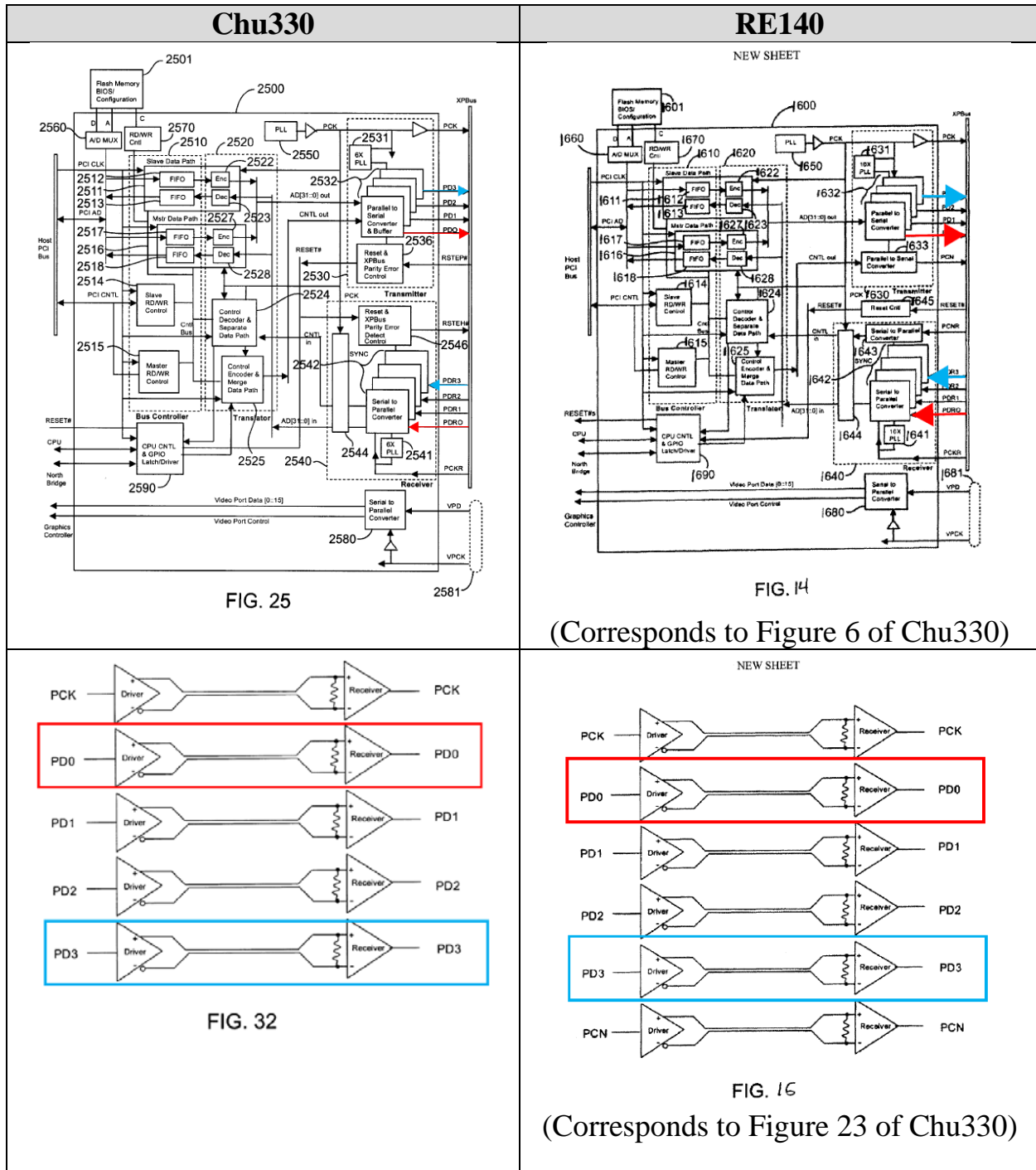
<sup>35</sup> *See* equivalent disclosure in Ex-1001, 19:52-56.

<sup>36</sup> *See* equivalent disclosure in Ex-1001, 19:49-51.

**5. Claim 17**

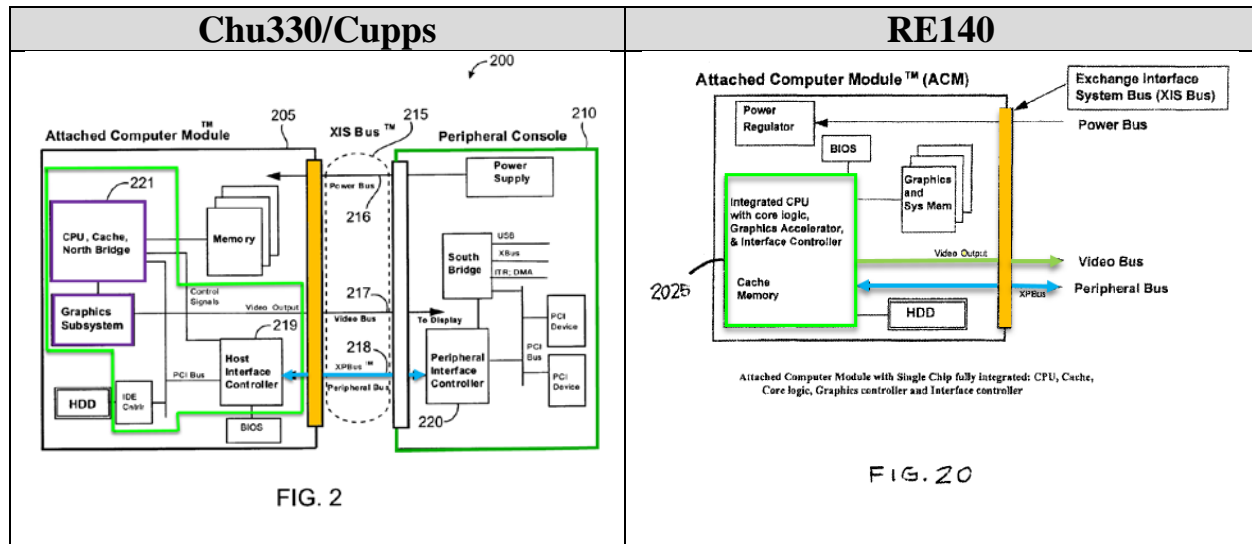
- i. [17] The method of claim 14 further comprises of connecting a **second LVDS channel** directly to the **integrated CPU and graphics controller**, the **second LVDS channel** comprising two unidirectional, serial bit channels that transmit data in opposite directions.

Chu330 explains that “the interface channel [XPBus] allows using **LVDS channels**.” Ex-1003, 2:36-38. Section XI.A.2.vii [14f] discussed in detail how Chu330 teaches the claimed **first LVDS channel** (e.g., including data lines **PD0** and **PDR0**). These discussions regarding the **first LVDS channel** apply equally to show the claimed **second LVDS channel** (e.g., including data lines **PD3** and **PDR3**) comprising two unidirectional, serial bit channels that transmit data in opposite directions. *See* Ex-1002, ¶¶150-153.



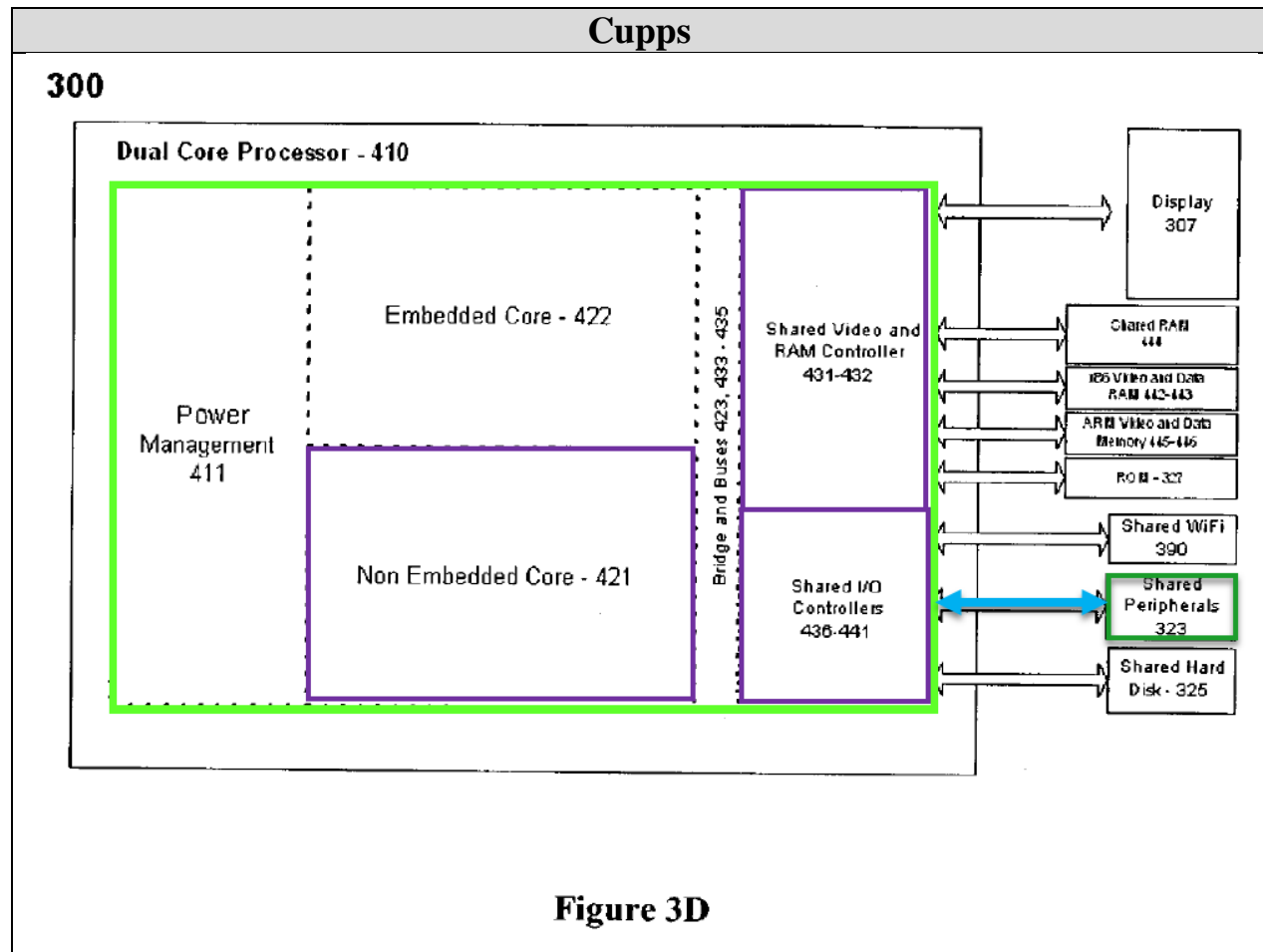
Having **integrated** the **CPU** and **graphics controller** in a **single chip** as discussed in Section XI.A.2.ii [14a], Chu330 in combination with Cupps would have

resulted in directly connecting the XPBus (including the **first LVDS channel** and **second LVDS channel**) to the **integrated CPU and graphics subsystem**, just like that shown in Figure 20 of RE140. See Ex-1002, ¶154.



Indeed, Cupps shows a **direct connection** between the **integrated chip 410** and **shared peripherals 323**. See Ex-1002, ¶155.





## 6. Claim 18

- i. [18pre] A method of improving performance of a computer, comprising:

As explained in Section XI.A.2.i [14pre], Chu330 discloses this limitation.

See Ex-1002, ¶156.

- ii. [18a] obtaining an **integrated** Central Processing Unit (CPU) with a **graphics controller** in a **single chip**;

As explained in Section XI.A.2.ii [14a], Chu330 and Cupps render obvious this limitation. See Ex-1002, ¶157.

- iii. [18b] connecting a **Differential Signal channel** directly to the **integrated CPU and graphics controller** to output **video data**;

As explained in Section XI.A.2.iii [14b], Chu330 and Cupps render obvious this limitation. *See* Ex-1002, ¶158.

- iv. [18c] providing a **connector** for the computer for connection to a **console**;

As explained in Section XI.A.2.vi [14e], Chu330 discloses this limitation. *See* Ex-1002, ¶159.

- v. [18d] providing a first **Low Voltage Differential Signal (LVDS) channel** to couple to the **connector**, the first LVDS channel comprising two unidirectional, serial bit channels that transmit data in opposite directions; and

As explained in Section XI.A.2.vii [14f], Chu330 discloses this limitation. *See* Ex-1002, ¶160.

- vi. [18e] conveying Universal Serial Bus (USB) protocol information through the **first LVDS channel**.

As explained in Section XI.A.3.i [15], Chu330 discloses this limitation. *See* Ex-1002, ¶161.

**7. Claim 19**

- i. [19] The method of claim 18 further comprising connecting a **second LVDS channel** directly to the **integrated CPU and graphics controller**, the **second LVDS channel** comprising two unidirectional, serial bit channels that transmit data in opposite directions.

As explained in Section XI.A.5.i [17], Chu330 and Cupps render obvious this limitation. *See* Ex-1002, ¶162.

**8. Claim 20**

- i. [20] The method of claim 19 further comprising conveying Universal Serial Bus (USB) protocol information over the **second LVDS channel**.

As discussed in Section XI.A.3.i [15], Chu330 discloses this limitation, because the discussions related to conveying USB protocol information over the **first LVDS channel** (*e.g.*, including data lines **PD0** and **PDR0**) apply equally to the **second LVDS channel** (*e.g.*, including data lines **PD3** and **PDR3**). *See* Ex-1002, ¶163.

**9. Claim 21**

- i. [21] The method of claim 18 further comprising conveying Transition Minimized Differential Signaling (TDMS) [sic] signals through the **Differential Signal channel**.

As explained in Sections XI.A.2.iii [14b] and XI.A.2.iv [14c], Chu330 discloses this limitation. *See* Ex-1002, ¶164.

**10. Claim 22**

- i. **[22Pre] A method of improving performance of a computer, comprising:**

As explained in Section XI.A.2.i [14pre], Chu330 discloses this limitation.

*See* Ex-1002, ¶165.

- ii. **[22a] obtaining an integrated Central Processing Unit (CPU) with a graphics controller in a single chip;**

As explained in Section XI.A.2.ii [14a], Chu330 and Cupps render obvious this limitation. *See* Ex-1002, ¶166.

- iii. **[22b] connecting a first Low Voltage Differential Signal (LVDS) channel directly to the integrated CPU and graphics controller, wherein the first LVDS channel comprises two unidirectional, serial bit channels that transmit data in opposite directions;**

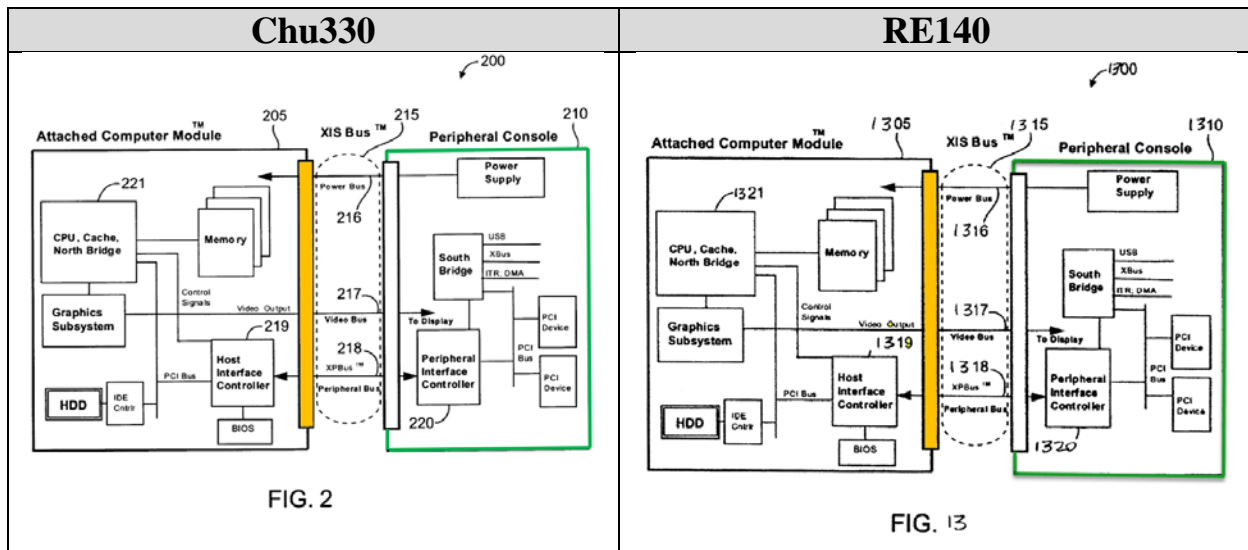
Chu330 and Cupps render obvious this limitation. As explained in Section XI.A.2.vii [14f], Chu330 teaches a **first LVDS channel** (*e.g.*, including data lines **PD0** and **PDR0**) comprising two unidirectional, serial bit channels that transmit data in opposite directions. And as explained in Section XI.A.5.i [17], Chu330 in combination with Cupps would result in directly connecting the **second LVDS channel** to the **integrated CPU and graphics controller**. These discussions regarding a **second LVDS channel** (*e.g.*, including data lines **PD3** and **PDR3**) apply equally to the **first LVDS channel**. *See* Ex-1002, ¶167.

iv. [22c] conveying Universal Serial Bus (USB) protocol information through the **first LVDS channel**;

As explained in Sections XI.A.3.i [15], Chu330 discloses this limitation. See Ex-1002, ¶168.

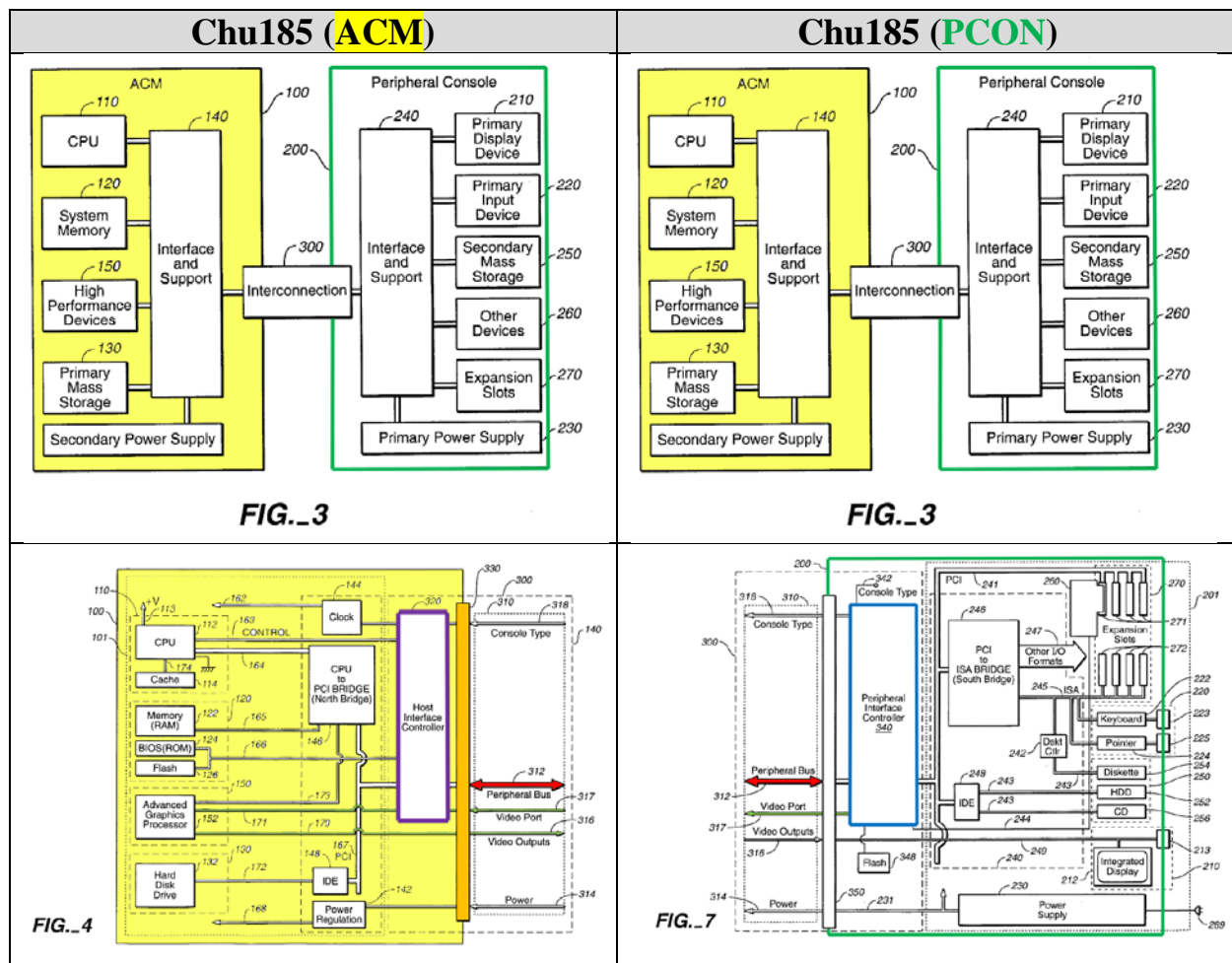
v. [22d] providing a **connector** for the computer for connection to an **external peripheral**; and

Chu330 discloses this limitation. As explained above in Section XI.A.2.vi [14e], Chu330 teaches a **connector** for the computer (ACM) for connection to the **peripheral console**. See Ex-1002, ¶169.



Chu185 (and hence Chu330) further shows in Figs. 3, 4, and 7 an ACM-to-PCON interconnection 300 to “convey ... operational signals between the ACM and PCON.” Ex-1005, 4:33-46. Specifically, the “ACM ... is inserted into the opening of the computer bay ... to interact with the **peripheral devices** housed in the **PCON**.” Ex-1005, 3:55-59; *see also* Section XI.A.1.i [Chu330]. As shown in

Figure 4, the computer (ACM) includes a **connector** configurable for connection to the interconnection 300. Ex-1005, 5:57-6:4. The interconnection 300 connects to **PCON**-resident components, which include **peripherals**, as needed. *Id.*, 4:40-44, 5:30-32, 13:9-13, 13:17-21; *see also id.*, 5:59-6:4, 13:1-39. The **connector** therefore provides connection to a **peripheral** that is external to the ACM. *See* Ex-1002, ¶170.



- vi. [22e] providing a **second LVDS channel** to couple to the **connector**, the **second LVDS channel** comprising two unidirectional, serial bit channels that transmit data in opposite directions.

As discussed in XI.A.2.vii [14f] and XI.A.5.i [17], Chu330 discloses this limitation, because the discussions related to the **first LVDS channel** (e.g., including data lines **PD0** and **PDR0**) apply equally to show a **second LVDS channel** (e.g., including data lines **PD3** and **PDR3**). See Ex-1002, ¶171.

#### 11. Claim 23

- i. [23] The method of claim 22 further comprising conveying Universal Serial Bus (USB) protocol information over the **second LVDS channel**.

As explained in Sections XI.A.3.i [15] and XI.A.3.i [20], Chu330 discloses this limitation. See Ex-1002, ¶172.

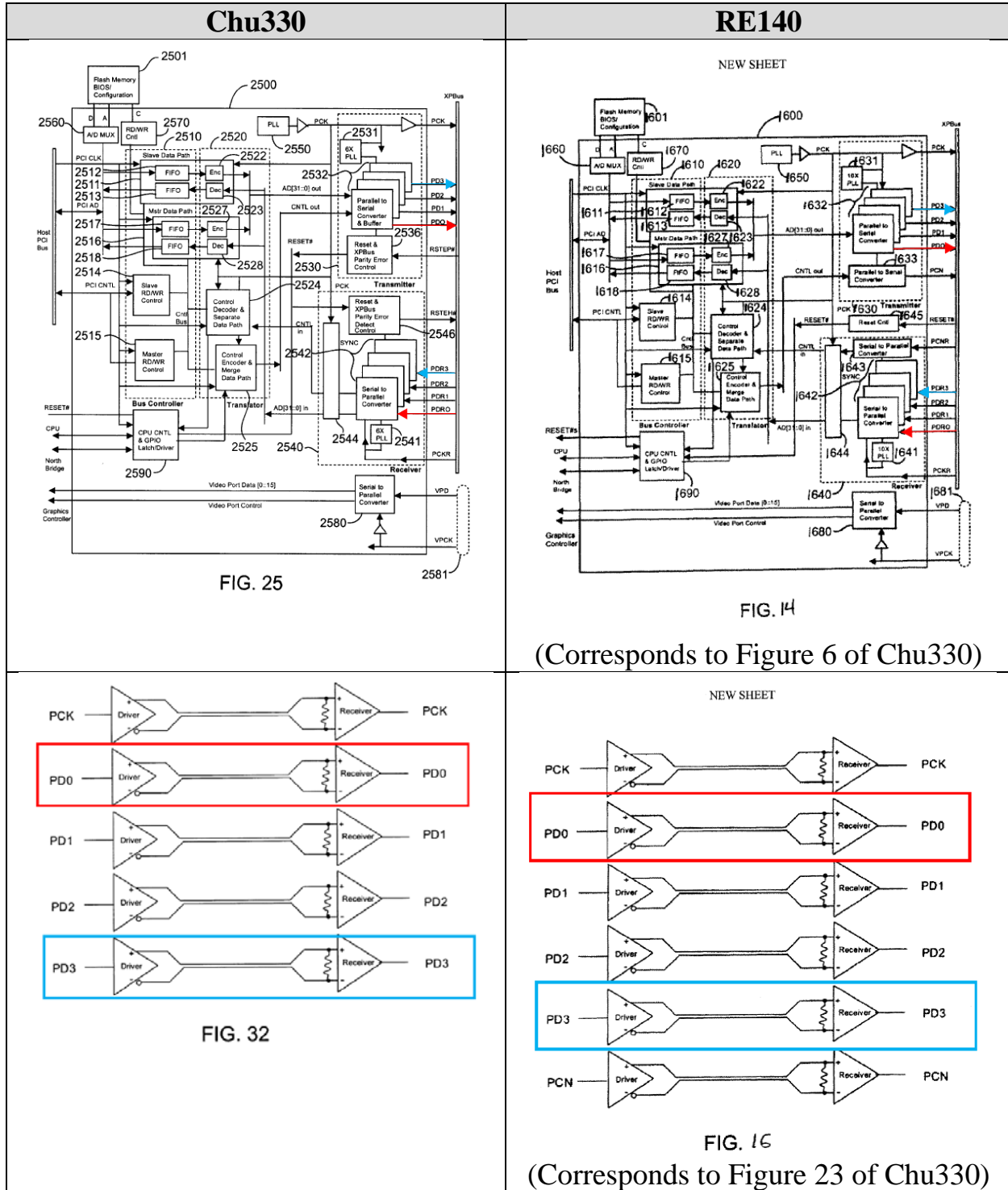
#### 12. Claim 24

- i. [24] The method of claim 22 further comprising conveying encoded address and data bits of a Peripheral Component Interconnect (PCI) bus transaction in serial form over the **second LVDS channel**.

As discussed in Section XI.A.4.i [16], Chu330 discloses this limitation, because the discussions regarding conveying encoded bits of PCI bus transactions over the **first LVDS channel** apply equally to the **second LVDS channel**. See Ex-1002, ¶173.

Further, Chu330's Figures 25 and 32 have been colored to illustrate two different types of data packet transmission (but not occurring simultaneously). As shown, **PD0** and **PDR0** have been colored red to indicate USB protocol information being conveyed through the **first LVDS channel** (although all of the PD0 through PDR3 data lines are utilized in those USB transactions). *See* Ex-1003, 18:13-19. For illustrative purposes, **PD3** and **PDR3** have been colored blue to indicate encoded bits of PCI bus transactions being conveyed at a different time over the **second LVDS channel** (although all of the PD0 through PDR3 data lines are utilized in those PCI bus transactions). *See id.* *See* Ex-1002, ¶174.



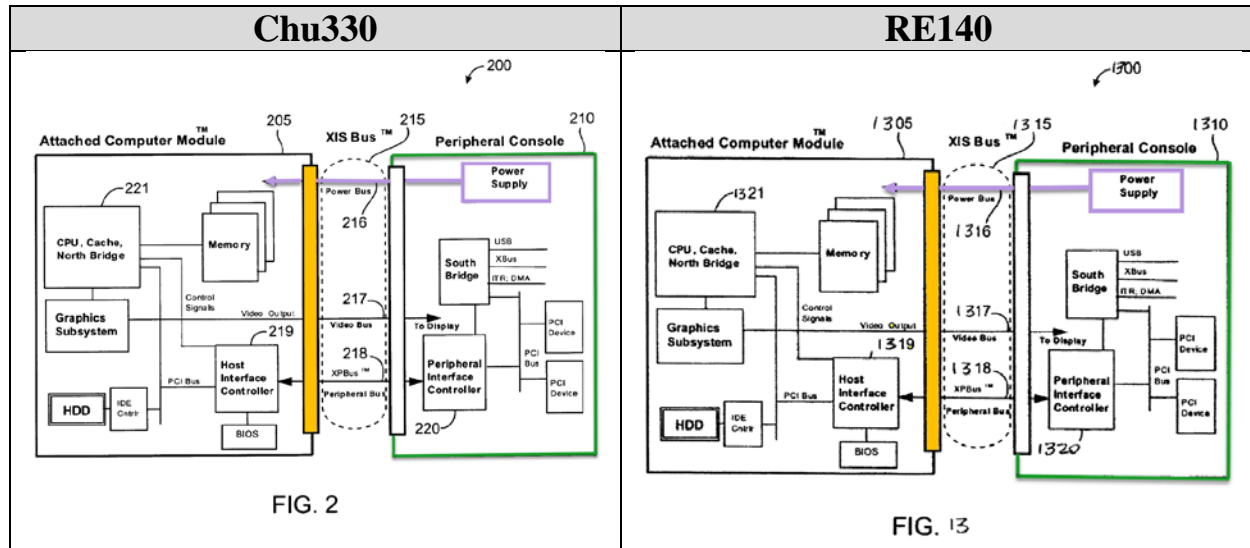


**13. Claim 25**

- i. [25] The method of claim 22 further comprising receiving power from the **connector** upon connection to an **external peripheral power supply**.

Chu330 discloses this limitation. Figure 2 shows a **power supply 216** within the **peripheral console 210** supplying power to the ACM (computer) from the **connector**. Specifically, “[t]he **power bus 216** transmits power between ACM 205 and **peripheral console 210**” through and therefore from the **connector**. Ex-1003, 6:12-13; *see also id.*, claim 1 (“a peripheral console includ[es] a power supply ... and a power bus between the [ACM] and the peripheral console, the power bus configured such that the central processing unit receives power only when the [ACM] is attached to the peripheral console”). Chu330 further explains that the **connector** “may include pins for transmitting video and/or **power** related signals in addition to the PCI related signals, in which case, the cable would have conductive lines for the video bus and/or **power bus**.” Ex-1003, 13:27-31; *see* Ex-1003, Figure 28 (pins V9-V18 for GND, 3.3 volts (V33), 5.0 volts (V5), and 12 volts (V12)), 13:38-62, 17:42-67; *see also* Ex-1003, Figures 17-19, 27, 29-30. *See* Ex-1002, ¶175.

Thus, the ACM receives power from the **connector** upon connection to a **power supply** in the **PCON 210** (i.e., **external** to the ACM (computer)). *See also* Ex-1005, 3:55-59, 5:34-37; Section XI.A.1.i [Chu330]. *See* Ex-1002, ¶175.



#### 14. Claim 26

- i. [26pre] A method of improving performance of a computer, comprising:

As explained in Section XI.A.2.i [14pre], Chu330 discloses this limitation.

See Ex-1002, ¶176.

- ii. [26a] obtaining an **integrated Central Processing Unit (CPU) with a graphics controller in a single chip**;

As explained in Section XI.A.2.ii [14a], Chu330 and Cupps render obvious this limitation. See Ex-1002, ¶177.

- iii. [26b] connecting a **Low Voltage Differential Signal (LVDS) channel** directly to the **integrated CPU and graphics controller**, wherein the **LVDS channel** comprises two unidirectional, serial bit channels that transmit data in opposite directions;

As explained in Sections XI.A.2.vii [14f], XI.A.5.i [17], and XI.A.10.iii [22b], Chu330 and Cupps render obvious this limitation. See Ex-1002, ¶178.

- iv. [26c] conveying Universal Serial Bus (USB) protocol information through the **LVDS channel**;

As explained in Section XI.A.3.i [15], Chu330 discloses this limitation. *See* Ex-1002, ¶179.

- v. [26d] connecting a **Differential Signal channel** directly to the **integrated CPU and graphics controller** to output **video data**; and

As explained in Section XI.A.2.iii [14b], Chu330 and Cupps render obvious this limitation. *See* Ex-1002, ¶180.

- vi. [26e] connecting **memory** directly to the **integrated CPU and graphics controller**.

As explained in Section XI.A.2.v [14d], Chu330 and Cupps render obvious this limitation. *See* Ex-1002, ¶181.

## 15. Claim 27

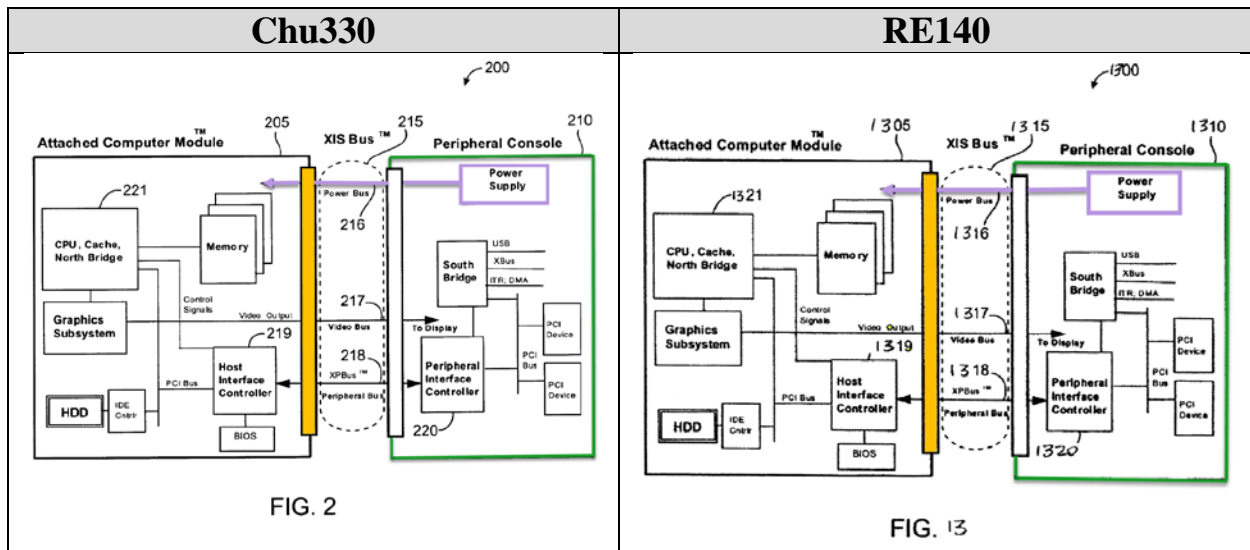
- i. [27] The method of claim 26 further comprising conveying Transition Minimized Differential Signaling (TDMS) [sic] signals through the **Differential Signal channel**.

As explained in Sections XI.A.2.iii [14b] and XI.A.2.iv [14c], Chu330 discloses this limitation. *See* Ex-1002, ¶182.

**16. Claim 28**

- i. [28] The method of claim 26 further comprising providing a **connector** for the computer for connection to a **console** with a **power supply**.

Chu330 discloses this limitation. As explained in Sections XI.A.2.vi [14e] and XI.A.13.i [25], Chu330 discloses this limitation, in which the **console** includes the **power supply**. See Ex-1002, ¶183.



**17. Claim 29**

- i. [29a] The method of claim 26 further comprising providing a **connector** for the computer for connection to a **console**, and

As explained in Section XI.A.2.vi [14e], Chu330 discloses this limitation. See Ex-1002, ¶184.

- ii. **[29b] coupling Universal Serial Bus (USB) protocol information from the LVDS channel to the console.**

Chu330 discloses this limitation. As explained in Sections XI.A.2.vi [14e], XI.A.2.vii [14f], and XI.A.3 [15], Chu330 teaches conveying USB protocol information from the **LVDS channel** that is coupled to the **console** that is connected to the **connector**. See Ex-1002, ¶185.

#### 18. Claim 30

- i. **[30pre] A method of improving performance of a computer, comprising:**

As explained in Section XI.A.2.i [14pre], Chu330 discloses this limitation. See Ex-1002, ¶186.

- ii. **[30a] obtaining an integrated Central Processing Unit (CPU) with a graphics controller in a single chip;**

As explained in Section XI.A.2.ii [14a], Chu330 and Cupps render obvious this limitation. See Ex-1002, ¶187.

- iii. **[30b] connecting a Low Voltage Differential Signal (LVDS) channel directly to the integrated CPU and graphics controller, wherein the LVDS channel comprises two unidirectional, serial bit channels that transmit data in opposite directions;**

As explained in Sections XI.A.2.vii [14f], XI.A.5 [17], and XI.A.10.iii [22b], Chu330 and Cupps render obvious this limitation. See Ex-1002, ¶188.

- iv. [30c] conveying serially encoded address and data of a Peripheral Component Interconnect (PCI) bus transaction through the **LVDS channel**;

As explained in Section XI.A.4.i [16], Chu330 discloses this limitation. *See* Ex-1002, ¶189.

- v. [30d] connecting a **Differential Signal channel** directly to the **integrated CPU and graphics controller** to output **video data**; and

As explained in Section XI.A.2.iii [14b], Chu330 and Cupps render obvious this limitation. *See* Ex-1002, ¶190.

- vi. [30e] connecting **memory** directly to the **integrated CPU and graphics controller**.

As explained in Section XI.A.2.v [14d], Chu330 and Cupps render obvious this limitation. *See* Ex-1002, ¶191.

## 19. Claim 31

- i. [31a] The method of claim 30 further comprising providing a **connector** for the computer for connection to a **console**, and

As explained in Section XI.A.2.vi [14e], Chu330 discloses this limitation. *See* Ex-1002, ¶192.

- ii. **[31b] providing a second LVDS channel that couples to the connector, the second LVDS channel comprising two unidirectional, serial bit channels that transmit data in opposite directions.**

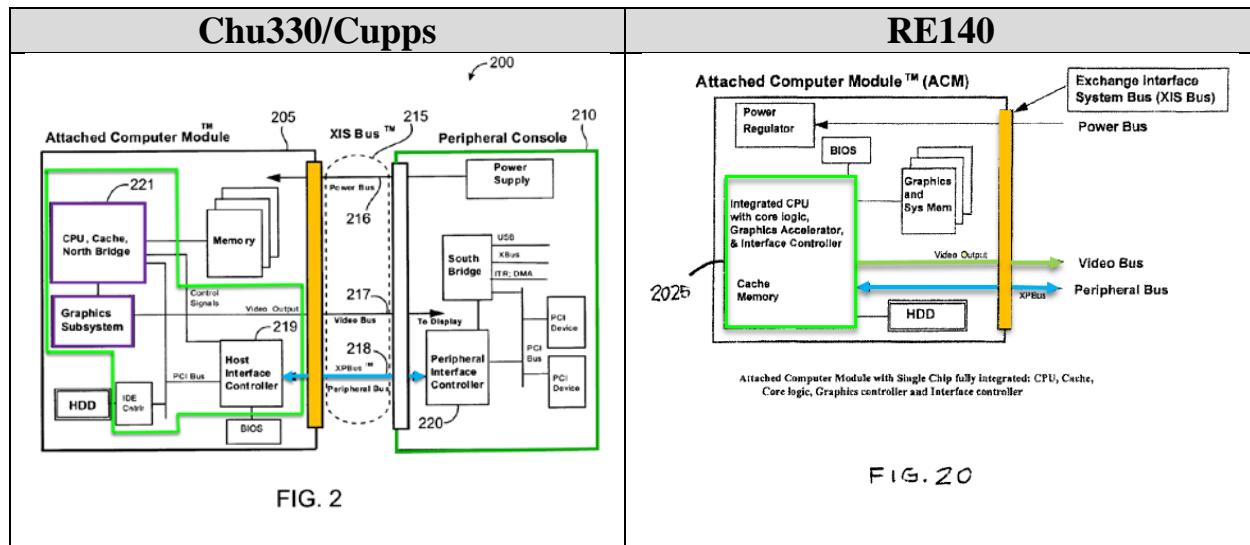
As explained in Sections XI.A.2.vii [14f] and XI.A.10.vi [22e], Chu330 discloses this limitation. *See* Ex-1002, ¶193.

## **20. Claim 32**

- i. **[32] The method of claim 31 further comprising conveying serially encoded address and data of a Peripheral Component Interconnect (PCI) bus transaction to the console through the second LVDS channel and the connector.**

Chu330 discloses this limitation. As explained in Sections XI.A.4.i [16] and XI.A.12.i [24], Chu330 teaches conveying serially encoded address and data of a PCI bus transaction through the second LVDS channel. Additionally, as explained in Sections XI.A.2.vi [14e], XI.A.2.vii [14f], and XI.A.5.i [17], and as shown in Chu330's Figure 2, Chu330 discloses that the XPBus (including the second LVDS channel) conveys data to the console through the connector. *See* Ex-1002, ¶194.



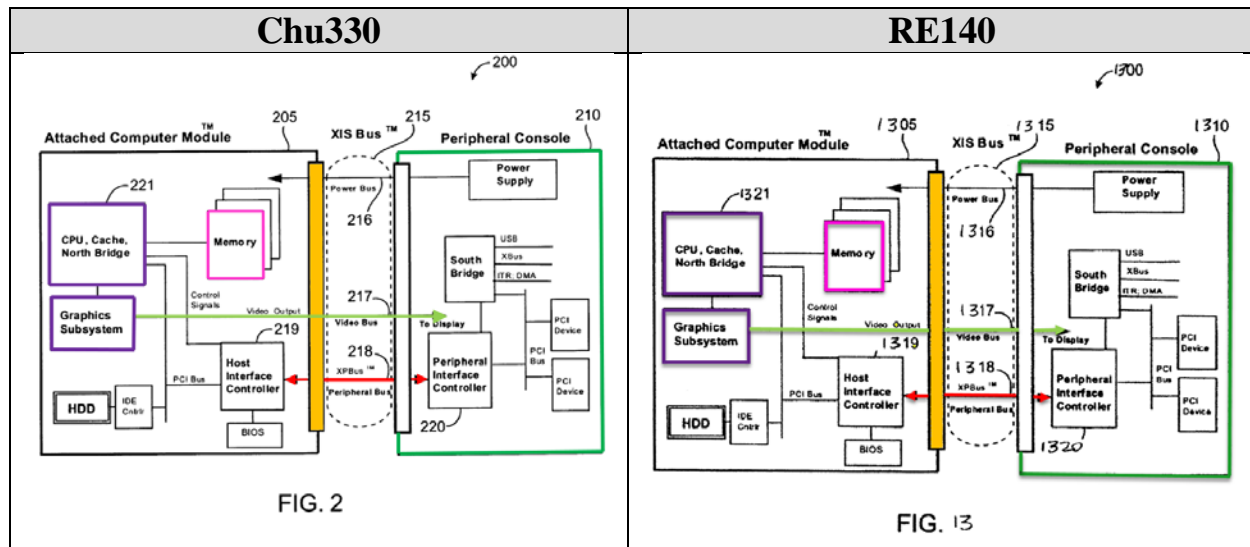


## 21. Claim 33

- i. [33] The method of claim 32 further comprising conveying **video data** to the **console** through the **connector**.

Chu330 discloses this limitation. As explained in Sections XI.A.2.iii [14b] and XI.A.2.iv [14c], and as shown in Chu330's Figure 2, Chu330 discloses conveying **video data** on the **video bus** (comprising a **differential signal channel**). In Figure 2, the **video bus** couples to the **console** through the **connector**. See Ex-1003, 6:7-11 ("The ACM 205 and the **peripheral console 210** are interfaced through an exchange interface system (XIS) bus 215 [including] **video bus 217**....").<sup>37</sup> See also Section XI.A.2.vi [14e]. See Ex-1002, ¶195.

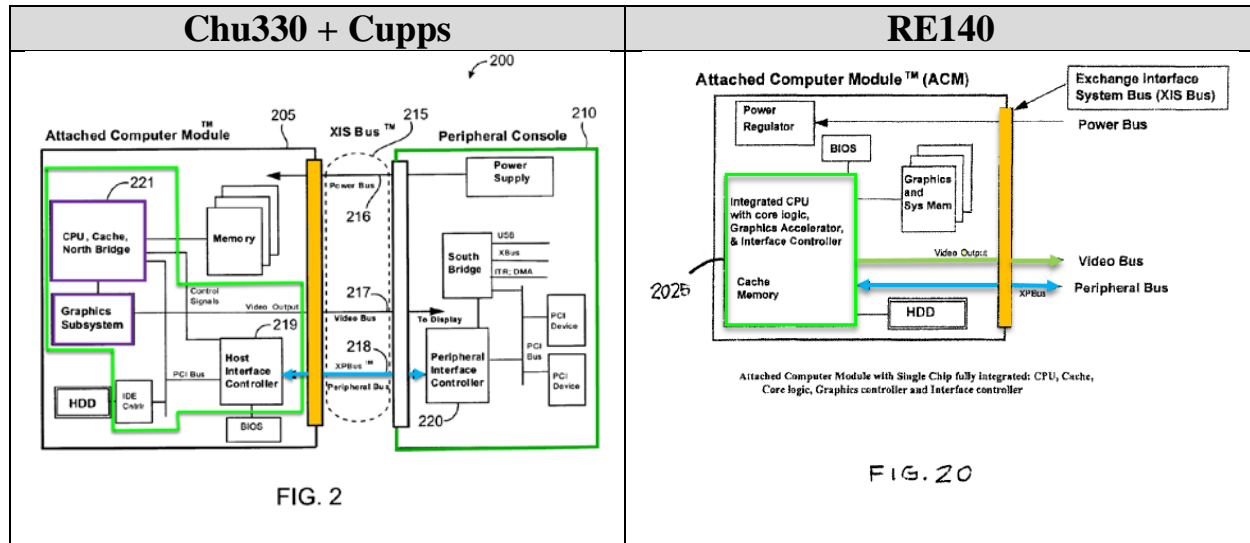
<sup>37</sup> See equivalent disclosure in Ex-1001, 18:46-51.



## 22. Claim 34

- i. [34] The method of claim 31 further comprising conveying Universal Serial Bus (USB) protocol information to the console through the second LVDS channel and the connector.

Chu330 discloses this limitation. As explained in Sections XI.A.3.i [15] and XI.A.8.i [20], Chu330 discloses conveying USB protocol information through the second LVDS channel. Additionally, as explained in Sections XI.A.2.vi [14e] and XI.A.5.i [17], and as shown in Chu330's Figure 2, Chu330 discloses that the XDBus (including the second LVDS channel) conveys data to the console through the connector. See Ex-1002, ¶196.



### 23. Claim 35

- i. [35pre] A method of improving performance of a computer, comprising:

As explained in Section XI.A.2.i [14pre], Chu330 discloses this limitation.

See Ex-1002, ¶197.

- ii. [35a] obtaining an **integrated Central Processing Unit (CPU) with a graphics controller in a single chip**;

As explained in Section XI.A.2.ii [14a], Chu330 and Cupps render obvious this limitation. See Ex-1002, ¶198.

- iii. [35b] connecting a **first Low Voltage Differential Signal (LVDS) channel** directly to the **integrated CPU and graphics controller**, wherein the **first LVDS channel** comprises two unidirectional, serial bit channels that transmit data in opposite directions;

As explained in Sections XI.A.2.vii [14f], XI.A.5.i [17], and XI.A.10.iii [22b], Chu330 and Cupps render obvious this limitation. See Ex-1002, ¶199.

- iv. [35c] connecting a **Differential Signal channel** directly to the **integrated CPU and graphics controller** to output **video data**;

As explained in Section XI.A.2.iii [14b], Chu330 and Cupps render obvious this limitation. *See* Ex-1002, ¶200.

- v. [35d] providing a **connector** for the computer for connection to an **external peripheral**; and

As explained in Sections XI.A.2.vi [14e] and XI.A.10.v [22d], Chu330 discloses this limitation. *See* Ex-1002, ¶201.

- vi. [35e] providing a **second LVDS channel** to couple to the **connector**, the **second LVDS channel** comprising two **unidirectional, serial bit channels** that transmit data in **opposite directions**.

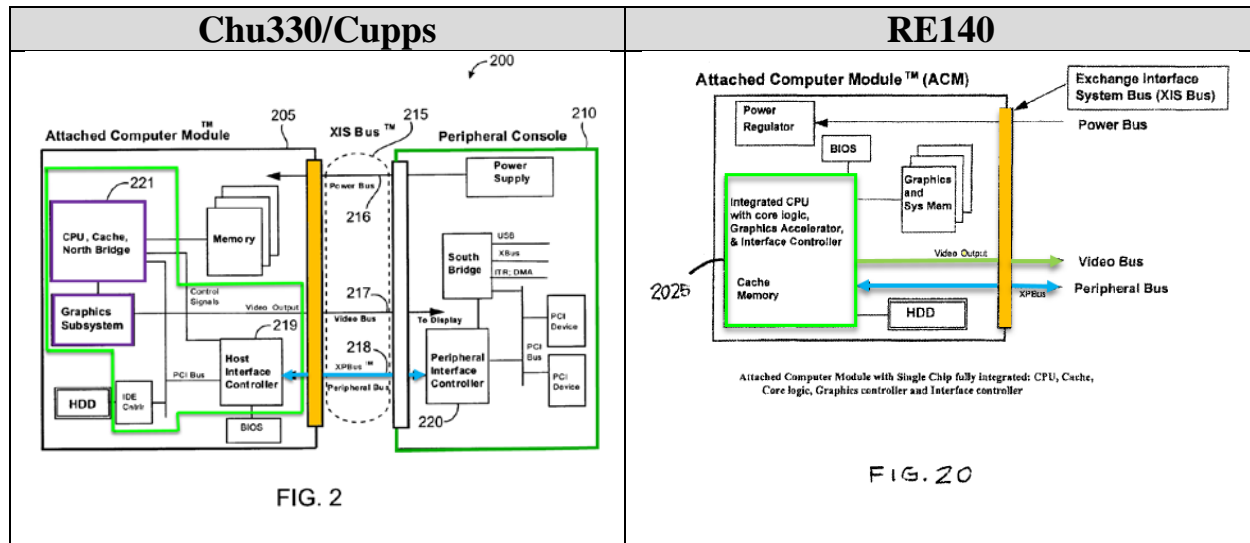
As explained in Sections XI.A.2.vii [14f], XI.A.5.i [17], and XI.A.10.vi [22e], Chu330 discloses this limitation. *See* Ex-1002, ¶202.

## 24. Claim 36

- i. [36] The method of claim 35 further comprising conveying **Universal Serial Bus (USB) protocol information** to the **external peripheral** through the **second LVDS channel** and the **connector**.

Chu330 discloses this limitation. As explained in Sections XI.A.3.i [15] and XI.A.8.i [20], Chu330 discloses conveying USB protocol information through the **second LVDS channel**. Additionally, as explained in Sections XI.A.2.vi [14e], XI.A.5.i [17], and XI.A.10.v [22d], and as shown in Chu330's Figure 2, Chu330

discloses that the XPBus (including the **second LVDS channel**) conveys data to the **external peripheral** through the **connector**. See Ex-1002, ¶¶203-204.



## 25. Claim 37

- i. [37] The method of claim 35 further comprising conveying Universal Serial Bus (USB) protocol information through the **first LVDS channel**.

As explained in Section XI.A.3.i [15], Chu330 discloses this limitation. See Ex-1002, ¶205.

## 26. Claim 38

- i. [38] The method of claim 35 further comprising conveying Transition Minimized Differential Signaling (TDMS) [sic] signals through the **Differential Signal channel**.

As explained in Sections XI.A.2.iii [14b] and XI.A.2.iv [14c], Chu330 discloses this limitation. See Ex-1002, ¶206.

## **XII. Discretionary Factors**

### **A. 35 U.S.C. § 325(d) – Prosecution History**

The Board employs a two-part framework under Section 325: (1) whether the same or substantially the same prior art or arguments have been previously presented to the Office; and (2) if so, whether the Office materially erred in a manner material to the patentability of the challenged claims. *Advanced Bionics, LLC v. Med-El Elektromedizinische Gerate GmbH*, IPR2019-01469, Paper 6, at 8 (PTAB Feb. 13, 2020).

While Chu330 appears on the voluminous list of references considered by the Patent Office, no Examiner cited Chu330 against any claims of RE140 or any of its related applications. Merely signing an information disclosure statement does not warrant denying institution. *See, e.g., Zip Top, LLC v. Stasher, Inc.*, IPR2018-01216, Paper 14, at 35-36 (PTAB Jan. 17, 2019); *Navistar, Inc. v. Fatigue Fracture Tech., LLC*, IPR2018-00853, Paper 13, at 16-17 (PTAB Sept. 12, 2018).

Moreover, the Examiner did not determine the proper priority date of any of the challenged claims during prosecution. The Examiner simply accepted the applicant's representation that RE140 properly incorporated by reference the materials found only in the '886 Provisional. This is consistent with the Patent Office's normal practice. *See In re NTP, Inc.*, 654 F.3d 1268, 1278 (Fed. Cir. 2011) (citing *PowerOasis, Inc. v. T-Mobile USA, Inc.*, 522 F.3d 1299, 1305 (Fed. Cir.

2008)). Hence, references like Cupps, which teach the improperly added new matter (prior to the date the new matter was added), were not previously considered. And the Examiner only issued an obviousness-type double patenting rejection during prosecution.

Finally, even wrongly assuming the Examiner made an implicit determination regarding the priority date, such determination would have been materially erroneous for the reasons discussed above in Section VII [Not Entitled to Priority].

Accordingly, Petitioner respectfully request institution.

**B. 35 U.S.C. § 314(a) – *General Plastic* (GP) Factors and Valve Factor**

This is the only Petition against RE140 by the instant Petitioner and RPIs. While Samsung filed two petitions against RE140 (IPR2021-00607 and IPR2021-00670), Petitioner/RPIs are unrelated to Samsung and no coordination of IPR filing efforts was carried out with Samsung. *See Google LLC v. Uniloc 2017*, IPR2020-00396, Paper 11 at 10-11 (PTAB Aug.03, 2020); *Toshiba Am. Info. Sys. V. Wallelex Microelectronics Ltd.*, IPR2018-01538, Paper 11 at 22 (PTAB March 05, 2019).

Having learned of ACQIS’s new wave of patent assertions that implicate Petitioner’s products and technology filed on October 15, 2020 (collectively “WDTX cases”), Petitioner’s counsel diligently pursued potential invalidity challenges that included analyzing the asserted patents, prior validity challenges against related patents, known and newly discovered prior art references, and

developing potential challenges to the asserted patents. These efforts were ongoing when Samsung independently filed IPR petitions challenging RE140.

Petitioner/RPIs did not discuss or coordinate any IPR strategy with Samsung. The Grounds presented in this Petition were developed solely on Petitioner/RPIs' own and Petitioner was actively drafting the IPR petitions when Samsung filed its IPRs. Petitioner/RPIs do not know whether Samsung knew or should have known about the secondary prior art reference (Cupps) relied on in the instant Petition. Moreover, while Samsung relies on Chu330 as a secondary reference in both its Grounds, the instant Petition relies on Chu330 as the primary reference. As a result, mapping of the claim limitations to the prior art references are different between Samsung's and the instant petition.

Moreover, to avoid allegation of utilizing Patent Owner's Preliminary Response (POPR) as a "roadmap," Petitioner accelerated its analysis and drafting efforts to file the instant Petition prior to the due date of the POPR to Samsung's petition for RE140.

Accordingly, these factors favor institution.

**C. 35 U.S.C. § 314(a) – Fintiv Factors**

Petitioner Intel is not a named defendant in any of the litigations involving the challenged patent. *See* Section II.A [Related Matters]. Although the Lenovo entities



(named as RPIs) are named defendants, the factors set forth in *Apple Inc. v. Fintiv, Inc.*, IPR2020-00019, Paper 11 (March 20, 2020) favor institution.

**1. Factor 1**

Petitioner cannot itself move the court for a stay in the parallel litigation. Moreover, the district court has not yet considered whether a stay would be appropriate in any of the ongoing WDTX cases.<sup>38</sup> In these situations, the Board “will not attempt to predict” how the court will proceed. *Sand Revolution II, LLC v. Cont’l Intermodal Group-Trucking LLC*, IPR2019-01393, Paper 24 at 7 (PTAB June 16, 2020). This factor is at best neutral.

**2. Factor 2**

The court’s scheduling order for the WDTX cases estimated a trial date of December 12, 2022, *approximately 18 months after* the filing date of the instant Petition. Samsung’s litigation is proceeding more quickly, with an estimated trial date of February 7, 2022. But multiple trials are scheduled for the same date, (*see* IPR2021-00605, Petition, 113), and the Board has previously noted that this favors institution. *See Samsung Electronics Co., Ltd. v. Acorn Semi, LLC*, IPR2020-01272, Paper 20 at 40-42 (Feb. 10, 2021). More importantly, given that Petitioner is not a

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<sup>38</sup> In the Samsung (EDTX) litigation, the parties have completed briefing on Samsung’s motion to stay pending IPR in April 2021.

party to any of the litigations and RPIs' trial date is estimated to be approximately the same time as the expected final written decision date, the second *Fintiv* factor weighs against denial.

### **3. Factor 3**

This factor also weighs against denial. The Petition is being filed at the early stages of the WDTX cases, in which preliminary infringement contentions were served only on May 17, 2021, invalidity contentions have not been served, claim construction positions have not been briefed, and discovery is stayed until Markman, which is estimated to be held on October 20, 2021. Although that precedes the estimated institution decision date, because no claim terms need be construed for the purposes of the instant IPR, any investment in the parallel WDTX cases is expected to have little effect in the instant proceeding. The same is true for the Samsung litigation. Moreover, "fact discovery is still ongoing, expert reports are not yet due, and substantive motion practice is yet to come. ... [and] further effort remains to be expended ... before trial." *See Sand Revolution II, LLC v. Continental Intermodal Group*, IPR2019-01393, Paper 24, 10-11 (June 16, 2020).

### **4. Factor 4**

Claims challenged in the instant Petition have only partial overlap with the claims asserted against the various defendants identified in Section II.A [Related Matters]. Although partial overlap alone may not be significant enough to favor

institution, Patent Owner's litigation tactics to-date justify challenging as many claims as possible in IPR proceedings, which would realistically not be feasible in district court litigation. ACQIS has repeatedly asserted RE140 (and related patents) against multiple defendants. Moreover, ACQIS has alleged infringement of different sets of claims against different defendants. Exercising discretionary denial and thereby allowing claims that were unasserted in the parallel district court litigations to remain unchallenged will likely further incentivize ACQIS to pursue these unchallenged claims against these defendants and/or incentivize additional filings against even more defendants. Moreover, for the claims that overlap against the Lenovo entities (named as RPIs), if the Board institutes IPR on the instant petition, the Lenovo entities are willing to stipulate *not* to advance the same Grounds or even the same references relied upon in the instant petition.<sup>39</sup> Given RPIs' willingness for such a stipulation, there will not be any overlap of the issues between the two proceedings, which mitigates the concerns of duplicated efforts and conflicting decisions. *See VMware, Inc. v. Intellectual Ventures I LLC*, IPR2020-00470, Paper 13 at 20 (PTAB Aug. 18, 2020) (finding that a similar stipulation

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<sup>39</sup> RPIs reserve the right to raise all other validity challenges, including challenges based on product and system prior art.

“mitigates any concerns of duplicative efforts between the district court and the Board, as well as concerns of potentially conflicting decisions”).

### **5. Factor 5**

This factor also favors institution. Although Lenovo entities are named defendants in the parallel litigation, Petitioner Intel is *not*. Denying institution because of concurrent litigations involving RE140 that Petitioner is not a party to would contradict Congress’s intent in enacting the AIA. *See Fintiv*, IPR2020-00019, Paper 11 at 11, n.20 (“If the parallel litigation involves a party different than the petitioner, this fact weighs against exercising authority to deny institution.”).

### **6. Factor 6**

This factor also favors institution. Petitioner has presented compelling Grounds that rely on Chu330 (that contains largely identical disclosure to RE140) in combination with Cupps (that demonstrates that the “integrated CPU/graphics” and “CPU-LVDS” limitations were well-known before the priority date afforded to RE140).

## **XIII. Conclusion**

Petitioner respectfully requests that the Board institute IPR, hold the challenged claims unpatentable, and cancel the challenged claims.

Petition for *Inter Partes* Review  
U.S. Reissue Patent No. 45,140 (Claims 14-38)

Dated: June 25, 2021

Respectfully submitted,

/Yung-Hoon Ha/  
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Petition for *Inter Partes* Review  
U.S. Reissued Patent No. 45,140 (Claims 14-38)

**CERTIFICATION UNDER 37 C.F.R. § 42.24(d)**

I hereby certify that this Petition for *Inter Partes* Review of U.S. Reissued Patent No. 45,140 has, excluding the portions exempted under 37 C.F.R. § 42.24(a), 12,393 words as counted by the word-processing system used to prepare this document, in compliance with 37 C.F.R. § 42.24(d).

Dated: June 25, 2021

Respectfully submitted,

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Petition for *Inter Partes* Review  
U.S. Reissued Patent No. 45,140 (Claims 14-38)

**CERTIFICATE OF SERVICE**

Under 37 C.F.R. §§ 42.6(e) and 42.126, the undersigned certifies that on June 25, 2021, complete copies of the foregoing and any accompanying exhibits were caused to be served by sending them via FedEx International Priority shipping, which is at least as fast and reliable as U.S. Priority Mail Express International, to the correspondence address of record for U.S. Reissued Patent No. 45,140 indicated in PAIR:

COOLEY LLP  
ATTN: IP Docketing Department  
1299 Pennsylvania Avenue, NW  
Suite 700  
Washington DC 20004

Dated: June 25, 2021

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