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UTILITY PATENT APPLICATION TRANSMITTAL <i>(Only for new nonprovisional applications under 37 CFR 1.53(b))</i>	Attorney Docket No.	ACQI-010/19US 310578-2066
	First Inventor	William W. Y. Chu
	Title	MULTIPLE MODULE COMPUTER SYSTEM AND METHOD INCLUDING DIFFERENTIAL SIGNAL CHANNEL COMPRISING UNIDIRECTIONAL SERIAL BIT CHANNELS
	Express Mail Label No.	

APPLICATION ELEMENTS See MPEP chapter 600 concerning utility patent application contents.	ADDRESS TO: Commissioner for Patents P.O. Box 1450 Alexandria VA 22313-1450
1. ☐ Fee Transmittal Form (e.g., PTO/SB/17) 2. ☐ Applicant claims small entity status. See 37 CFR 1.27. 3. ☒ Specification [Total Pages <u>67</u>] Both the claims and abstract must start on a new page (For information on the preferred arrangement, see MPEP 608.01(a)) 4. ☒ Drawing(s) (35 U.S.C. 113) [Total Sheets <u>26</u>]* *including 2 sheets added by Preliminary Amendment 5. Oath or Declaration [Total Sheets <u>3</u>] a. ☐ Newly executed (original or copy) b. ☒ A copy from a prior application (37 CFR 1.63(d)) (for continuation/divisional with Box 18 completed) i. ☐ DELETION OF INVENTOR(s) Signed statement attached deleting inventor(s) name in the prior application, see 37 CFR 1.63(d)(2) and 1.33(b). 6. ☒ Application Data Sheet. See 37 CFR 1.76 7. ☐ CD-ROM or CD-R in duplicate, large table or Computer Program (Appendix) ☐ Landscape Table on CD 8. Nucleotide and/or Amino Acid Sequence Submission (if applicable, items a. - c. are required) a. ☐ Computer Readable Form (CRF) b. Specification Sequence Listing on: i. ☐ CD-ROM or CD-R (2 copies); or ii. ☐ Paper c. ☐ Statements verifying identity of above copies	ACCOMPANYING APPLICATION PARTS 9. ☐ Assignment Papers (cover sheet & document(s)) Name of Assignee <u>ACQIS LLC</u> 10. ☒ 37 CFR 3.73(b) Statement ☒ Power of Attorney (when there is an assignee) 11. ☐ English Translation Document (if applicable) 12. ☒ Information Disclosure Statement (PTO/SB/08 or PTO-1449) ☒ Copies of citations can be found in parent application; copies not provided 13. ☒ Preliminary Amendment 14. ☐ Return Receipt Postcard (MPEP 503) (Should be specifically itemized) 15. ☐ Certified Copy of Priority Document(s) (if foreign priority is claimed) 16. ☐ Nonpublication Request under 35 U.S.C. 122(b)(2)(B)(i). Applicant must attach form PTO/SB/35 or equivalent. 17. ☐ Other: _____

18. If a CONTINUING APPLICATION, check appropriate box, and supply the requisite information below and in the first sentence of the specification following the title, or in an Application Data Sheet under 37 CFR 1.76:

☒ Continuation ☐ Divisional ☐ Continuation-in-part (CIP) of prior application No.: 12/504,534

Prior application information: Examiner Raymond Ngan Phan Art Unit: 2111

19. CORRESPONDENCE ADDRESS					
☐ The address associated with Customer Number		58249		OR ☐ Correspondence address below	
Name					
Address					
City	State	Zip Code			
Country	Telephone	Email			

Signature		Date	April 15, 2011
Name (Print/Type)	Cliff Z. Liu	Registration No. (Attorney/Agent)	50,834

This collection of information is required by 37 CFR 1.53(b). The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.11 and 1.14. This collection is estimated to take 12 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.

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Application Data Sheet 37 CFR 1.76		Attorney Docket Number	ACQI-010/19US 310578-2066
		Application Number	
Title of Invention	MULTIPLE MODULE COMPUTER SYSTEM AND METHOD INCLUDING DIFFERENTIAL SIGNAL CHANNEL COMPRISING UNIDIRECTIONAL SERIAL BIT CHANNELS		
The application data sheet is part of the provisional or nonprovisional application for which it is being submitted. The following form contains the bibliographic data arranged in a format specified by the United States Patent and Trademark Office as outlined in 37 CFR 1.76. This document may be completed electronically and submitted to the Office in electronic format using the Electronic Filing System (EFS) or the document may be printed and included in a paper filed application.			

Secrecy Order 37 CFR 5.2

☐	Portions or all of the application associated with this Application Data Sheet may fall under a Secrecy Order pursuant to 37 CFR 5.2 (Paper filers only. Applications that fall under Secrecy Order may not be filed electronically.)

Applicant Information:

Applicant 1					Remove				
Applicant Authority		☒ Inventor			☐ Legal Representative under 35 U.S.C. 117	☐ Party of Interest under 35 U.S.C. 118			
Prefix	Given Name	Middle Name		Family Name		Suffix			
	William	W.Y.		Chu					
Residence Information (Select One)							☒ US Residency	☐ Non US Residency	☐ Active US Military Service
City	Los Altos		State/Province	CA	Country of Residence i	US			
Citizenship under 37 CFR 1.41(b) i			US						
Mailing Address of Applicant:									
Address 1		1320 Miravalle Avenue							
Address 2									
City	Los Altos			State/Province	CA				
Postal Code		94024		Country i	US				
All Inventors Must Be Listed - Additional Inventor Information blocks may be generated within this form by selecting the Add button.									
Add									

Correspondence Information:

Enter either Customer Number or complete the Correspondence Information section below. For further information see 37 CFR 1.33(a).		
☐ An Address is being provided for the correspondence information of this application.		
Customer Number	58249	
Email Address		Add Email Remove Email

Application Information:

Title of the Invention	MULTIPLE MODULE COMPUTER SYSTEM AND METHOD INCLUDING DIFFERENTIAL SIGNAL CHANNEL COMPRISING UNIDIRECTIONAL SERIAL BIT CHANNELS		
Attorney Docket Number	ACQI-010/19US 310578-2066	Small Entity Status Claimed ☐	
Application Type	Nonprovisional		
Subject Matter	Utility		
Suggested Class (if any)		Sub Class (if any)	
Suggested Technology Center (if any)			
Total Number of Drawing Sheets (if any)	26	Suggested Figure for Publication (if any)	

Application Data Sheet 37 CFR 1.76	Attorney Docket Number	ACQI-010/19US 310578-2066
	Application Number	
Title of Invention	MULTIPLE MODULE COMPUTER SYSTEM AND METHOD INCLUDING DIFFERENTIAL SIGNAL CHANNEL COMPRISING UNIDIRECTIONAL SERIAL BIT CHANNELS	

Publication Information:

☐	Request Early Publication (Fee required at time of Request 37 CFR 1.219)
☐	Request Not to Publish. I hereby request that the attached application not be published under 35 U.S.C. 122(b) and certify that the invention disclosed in the attached application has not and will not be the subject of an application filed in another country, or under a multilateral international agreement, that requires publication at eighteen months after filing.

Representative Information:

Representative information should be provided for all practitioners having a power of attorney in the application. Providing this information in the Application Data Sheet does not constitute a power of attorney in the application (see 37 CFR 1.32). Enter either Customer Number or complete the Representative Name section below. If both sections are completed the Customer Number will be used for the Representative Information during processing.			
Please Select One:	☒ Customer Number	☐ US Patent Practitioner	☐ Limited Recognition (37 CFR 11.9)
Customer Number	58249		

Domestic Benefit/National Stage Information:

This section allows for the applicant to either claim benefit under 35 U.S.C. 119(e), 120, 121, or 365(c) or indicate National Stage entry from a PCT application. Providing this information in the application data sheet constitutes the specific reference required by 35 U.S.C. 119(e) or 120, and 37 CFR 1.78(a)(2) or CFR 1.78(a)(4), and need not otherwise be made part of the specification.			
Prior Application Status	Pending	Remove	
Application Number	Continuity Type	Prior Application Number	Filing Date (YYYY-MM-DD)
	Continuation of	12504534	2009-07-16
Prior Application Status		Remove	
Application Number	Continuity Type	Prior Application Number	Filing Date (YYYY-MM-DD)
12504534	Continuation of	12077503	2008-03-18
Prior Application Status		Remove	
Application Number	Continuity Type	Prior Application Number	Filing Date (YYYY-MM-DD)
12077503	Continuation of	11166656	2005-06-24
Prior Application Status		Remove	
Application Number	Continuity Type	Prior Application Number	Filing Date (YYYY-MM-DD)
11166656	Continuation of	11097694	2005-03-31
Prior Application Status		Remove	
Application Number	Continuity Type	Prior Application Number	Filing Date (YYYY-MM-DD)
11097694	Continuation of	10772214	2004-02-03
Prior Application Status		Remove	

Application Data Sheet 37 CFR 1.76		Attorney Docket Number	ACQI-010/19US 310578-2066	
		Application Number		
Title of Invention	MULTIPLE MODULE COMPUTER SYSTEM AND METHOD INCLUDING DIFFERENTIAL SIGNAL CHANNEL COMPRISING UNIDIRECTIONAL SERIAL BIT CHANNELS			

Application Number	Continuity Type	Prior Application Number	Filing Date (YYYY-MM-DD)
10772214	Continuation of	09569758	2000-05-12
Prior Application Status		Remove	
Application Number	Continuity Type	Prior Application Number	Filing Date (YYYY-MM-DD)
09569758	non provisional of	60134122	1999-05-14
Additional Domestic Benefit/National Stage Data may be generated within this form by selecting the Add button.			Add

Foreign Priority Information:

This section allows for the applicant to claim benefit of foreign priority and to identify any prior foreign application for which priority is not claimed. Providing this information in the application data sheet constitutes the claim for priority as required by 35 U.S.C. 119(b) and 37 CFR 1.55(a).

Remove			
Application Number	Country ⁱ	Parent Filing Date (YYYY-MM-DD)	Priority Claimed
			☒ Yes ☐ No
Additional Foreign Priority Data may be generated within this form by selecting the Add button.			Add

Assignee Information:

Providing this information in the application data sheet does not substitute for compliance with any requirement of part 3 of Title 37 of the CFR to have an assignment recorded in the Office.

Remove			
Assignee 1			
If the Assignee is an Organization check here. ☒			
Organization Name	ACQIS LLC		
Mailing Address Information:			
Address 1	411 Interchange Street		
Address 2			
City	McKinney	State/Province	TX
Country ⁱ	US	Postal Code	75071
Phone Number		Fax Number	
Email Address			
Additional Assignee Data may be generated within this form by selecting the Add button.			Add

Signature:

A signature of the applicant or representative is required in accordance with 37 CFR 1.33 and 10.18. Please see 37 CFR 1.4(d) for the form of the signature.

Signature	/Cliff Z. Liu/		Date (YYYY-MM-DD)	2011-04-15
First Name	Cliff Z.	Last Name	Liu	Registration Number
			50834	

Application Data Sheet 37 CFR 1.76		Attorney Docket Number	ACQI-010/19US 310578-2066
		Application Number	
Title of Invention	MULTIPLE MODULE COMPUTER SYSTEM AND METHOD INCLUDING DIFFERENTIAL SIGNAL CHANNEL COMPRISING UNIDIRECTIONAL SERIAL BIT CHANNELS		

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Privacy Act Statement

The Privacy Act of 1974 (P.L. 93-579) requires that you be given certain information in connection with your submission of the attached form related to a patent application or patent. Accordingly, pursuant to the requirements of the Act, please be advised that: (1) the general authority for the collection of this information is 35 U.S.C. 2(b)(2); (2) furnishing of the information solicited is voluntary; and (3) the principal purpose for which the information is used by the U.S. Patent and Trademark Office is to process and/or examine your submission related to a patent application or patent. If you do not furnish the requested information, the U.S. Patent and Trademark Office may not be able to process and/or examine your submission, which may result in termination of proceedings or abandonment of the application or expiration of the patent.

The information provided by you in this form will be subject to the following routine uses:

1. The information on this form will be treated confidentially to the extent allowed under the Freedom of Information Act (5 U.S.C. 552) and the Privacy Act (5 U.S.C. 552a). Records from this system of records may be disclosed to the Department of Justice to determine whether the Freedom of Information Act requires disclosure of these records.
2. A record from this system of records may be disclosed, as a routine use, in the course of presenting evidence to a court, magistrate, or administrative tribunal, including disclosures to opposing counsel in the course of settlement negotiations.
3. A record in this system of records may be disclosed, as a routine use, to a Member of Congress submitting a request involving an individual, to whom the record pertains, when the individual has requested assistance from the Member with respect to the subject matter of the record.
4. A record in this system of records may be disclosed, as a routine use, to a contractor of the Agency having need for the information in order to perform a contract. Recipients of information shall be required to comply with the requirements of the Privacy Act of 1974, as amended, pursuant to 5 U.S.C. 552a(m).
5. A record related to an International Application filed under the Patent Cooperation Treaty in this system of records may be disclosed, as a routine use, to the International Bureau of the World Intellectual Property Organization, pursuant to the Patent Cooperation Treaty.
6. A record in this system of records may be disclosed, as a routine use, to another federal agency for purposes of National Security review (35 U.S.C. 181) and for review pursuant to the Atomic Energy Act (42 U.S.C. 218(c)).
7. A record from this system of records may be disclosed, as a routine use, to the Administrator, General Services, or his/her designee, during an inspection of records conducted by GSA as part of that agency's responsibility to recommend improvements in records management practices and programs, under authority of 44 U.S.C. 2904 and 2906. Such disclosure shall be made in accordance with the GSA regulations governing inspection of records for this purpose, and any other relevant (i.e., GSA or Commerce) directive. Such disclosure shall not be used to make determinations about individuals.
8. A record from this system of records may be disclosed, as a routine use, to the public after either publication of the application pursuant to 35 U.S.C. 122(b) or issuance of a patent pursuant to 35 U.S.C. 151. Further, a record may be disclosed, subject to the limitations of 37 CFR 1.14, as a routine use, to the public if the record was filed in an application which became abandoned or in which the proceedings were terminated and which application is referenced by either a published application, an application open to public inspections or an issued patent.
9. A record from this system of records may be disclosed, as a routine use, to a Federal, State, or local law enforcement agency, if the USPTO becomes aware of a violation or potential violation of law or regulation.

DECLARATION

As a below named inventor, I hereby declare that:

My residence, post office address and citizenship are as stated next to my name;

I believe I am the original, first and sole inventor (if only one name is listed below) or an original, first and joint inventor (if plural names are listed below) of the subject matter which is claimed and for which a patent is sought on the invention entitled:

MULTIPLE MODULE COMPUTER SYSTEM AND METHOD INCLUDING
DIFFERENTIAL SIGNAL CHANNEL COMPRISING UNIDIRECTIONAL SERIAL BIT
CHANNELS

the specification of which:

(check one)

☒ [X] is attached hereto;

☐ [] was filed as United States Application Serial No. ____ on ____, and was amended on (if applicable);

☐ [] was filed as PCT International Application No. ____ on ____ and was amended under PCT Article 19 or Article 34 on ____ (if applicable);

I have reviewed and understand the contents of the above-identified specification, including the claims, as amended by any amendment referred to above;

I acknowledge the duty to disclose to the U.S. Patent and Trademark Office all information which is known to me to be material to the patentability of said invention in accordance with 37 C.F.R. §1.56;

I hereby claim foreign priority benefits under 35 U.S.C. §119 and/or §365 of any foreign application(s) for patent, any foreign application(s) for inventor's certificate, or any PCT international application(s) designating at least one country other than the United States of America listed below; I have also identified below any foreign application(s) for patent, any foreign application(s) for inventor's certificate, or any PCT international application(s) designating at least one country other than the United States of America filed by me on the same subject matter having a filing date before that of the application(s) of which priority is claimed:

Prior Foreign Application(s)

COUNTRY/INTERNATIONAL	APPLICATION NUMBER	DATE OF FILING (day, month, year)	PRIORITY CLAIMED
			☐ YES ☐ NO
			☐ YES ☐ NO

I hereby claim the benefit under 35 U.S.C. §119(e) of any United States provisional application(s) listed below:

60/134,122
(Application Number)

14/05/1999
(Filing Date) (day, month, year)

(Application Number)

(Filing Date) (day, month, year)

I hereby claim the benefit under 35 U.S.C. §120 and/or §365 of any United States application(s) or of any international application(s) designating the United States of America that is/are listed below and, insofar as the subject matter of each of the claims of this application is not disclosed in the prior application(s) in the manner provided by the first paragraph of 35 U.S.C. §112, I acknowledge the duty to disclose to the U.S. Patent and Trademark Office all information known to me to be material to patentability as defined in 37 C.F.R. §1.56 which became available between the filing date(s) of the prior application(s) and the national or PCT international filing date of this application:

Prior U.S. Application(s) or PCT International Applications Designating the U.S. for benefit under 35 U.S.C. §120

U.S. APPLICATIONS		STATUS (check one)		
U.S. APPLICATION NO.	U.S. FILING DATE (day, month, year)	Pending	Patented	Abandoned
12/077,503	18/03/2008	☒	☐	☐
11/166,656	24/06/2005	☐	☒	☐
11/097,694	31/03/2005	☐	☒	☐
10/772,214	03/02/2004	☐	☒	☐
09/569,758	12/05/2000	☐	☒	☐
PCT APPLICATIONS DESIGNATING THE U.S.				
PCT APPLICATION NO.	PCT FILING DATE (day, month, year)	U.S. APPLICATION NOS. (if any)		
			☐	☐
			☐	☐

I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States

Code and that such willful false statements may jeopardize the validity of the application or any patent issued thereon.

Full name of first inventor:

Inventor's signature William W. Y. Chu Date 7/16/2009
Residence: William W. Y. Chu
Citizen of: United States
Post Office Address: 1320 Miravalle Avenue, Los Altos, CA 94024

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In Re Application of: William W. Y. Chu Confirmation No.: Not Yet Assigned
Serial No.: Not Yet Assigned Group Art Unit: Not Yet Assigned
Filed: July 16, 2009 Examiner: Not Yet Assigned
FOR: MULTIPLE MODULE COMPUTER SYSTEM AND METHOD INCLUDING
DIFFERENTIAL SIGNAL CHANNEL COMPRISING UNIDIRECTIONAL SERIAL
BIT

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

POWER BY ASSIGNEE
AND STATEMENT UNDER 37 C.F.R. §3.73(b)

The Assignee of the entire right, title, and interest in the above-identified application hereby grants the registered practitioners of Cooley Godward Kronish LLP included in the Customer Number provided below power to act, prosecute, and transact all business in the U.S. Patent and Trademark Office in connection with this application, any applications claiming priority to this application, and any patents issuing therefrom.

The Assignee certifies that to the best of its knowledge and belief it is the owner of the entire right, title, and interest in and to the above-identified application as evidenced by:

- ☐ An assignment document, a copy of which is enclosed herewith;
- ☒ An assignment previously recorded in the U.S. Patent and Trademark Office at Reel 022460, Frame 0848; and Reel 022461, Frame 0702.

Please direct all telephone calls and correspondence to:

CUSTOMER NUMBER: **58249**

Attorney Docket No. ACQI-010/10US 310578-2052

Application Serial No.

Page 2

COOLEY GODWARD KRONISH LLP

ATTN: Patent Group

777 6th Street NW, Suite 1100

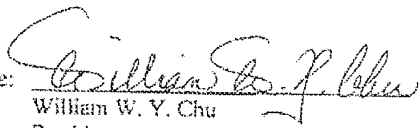
Washington, DC 20001

Tel: (650) 843-5852

Fax: (202) 842-7899

The undersigned (whose title is supplied below) is empowered to sign this statement on behalf of the Assignee.

Date: 7/16/2009

Signature: 

Name: William W. Y. Chu

Title: President

Company: ACQI LLC

797696 v1/PA

Attorney Docket No. ACQI-010/19US 310578-2066

PATENT

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of:	William W.Y. Chu	Confirmation No.:	Unassigned
Application No.:	Unassigned	Group Art Unit:	Unassigned
Filed:	Herewith	Examiner:	Unassigned
Title:	MULTIPLE MODULE COMPUTER SYSTEM AND METHOD INCLUDING DIFFERENTIAL SIGNAL CHANNEL COMPRISING UNIDIRECTIONAL SERIAL BIT CHANNELS		

Mail Stop: Amendment
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

PRELIMINARY AMENDMENT

Prior to examination of the above-identified application, please amend the subject application as follows:

Amendments to the Drawings begin on page 2 of this paper.

Amendments to the Title begin on page 3 of this paper.

Amendments to the Specification begin on page 4 of this paper.

Amendments to the Claims begin on page 6 of this paper.

Remarks/Arguments begin on page 15 of this paper.

The Director is hereby authorized to charge any appropriate fees under 37 C.F.R. §§1.16, 1.17, and 1.21 that may be required by this paper, and to credit any overpayment, to Deposit Account No. 50-1283.

IN THE DRAWINGS

Attachment: New Sheets FIG. 8A and FIG. 8B

The subject application is amended to specifically include certain figures from U.S. Provisional Application No. 60/083,886.

IN THE TITLE

Please amend the title as follows:

MULTIPLE MODULE COMPUTER SYSTEM AND METHOD INCLUDING DIFFERENTIAL SIGNAL
CHANNEL COMPRISING ~~UNDIRECTIONAL~~ UNIDIRECTIONAL SERIAL BIT CHANNELS

IN THE SPECIFICATION

Please replace paragraph no. [0001] with the following paragraph. The amendments to paragraph no. [0001] are indicated by strikethrough and underlining.

[0001] This application is a continuation of U.S. Application No. 12/504,534 filed July 16, 2009, which is a continuation of U.S. Application No. 12/077,503 filed March 18, 2008 (Now U.S. Patent No. 7,676,624), which is a continuation of U.S. nonprovisional Application No. 11/166,656, filed June 24, 2005 (Now U.S. Patent No. 7,376,779), which is a continuation of U.S. nonprovisional Application No. 11/097,694, filed March 31, 2005 (Now U.S. Patent No. 7,363,415), which is a continuation of U.S. nonprovisional Application No. 10/772,214, filed February 3, 2004 (Now U.S. Patent No. 7,099,981), which is a continuation of U.S. nonprovisional Application No. 09/569,758, filed May 12, 2000 (Now U.S. patent no. 6,718,415), and which claimed priority to U.S. Provisional Application No. 60/134,122 filed May 14, 1999. These applications are hereby incorporated by reference in their entirety.

Please add paragraph nos. [0041.1] and [0041.2] as set forth below immediately after original paragraph no. [0041]:

[0041.1] Fig. 8A shows an attached computer module with Integrated CPU/NB/Graphics and Integrated HIC/SB.

[0041.2] Fig. 8B shows an attached computer module with single chip fully integrated: CPU, Cache, Core Logic, Graphics controller and Interface controller.

Please replace paragraph no. [0093] with the following paragraph. The amendments to paragraph no. [0093] are indicated by strikethrough and underlining.

[0093] In the embodiment shown in Fig. 6, HIC 619 is coupled to an integrated unit 621 that includes a CPU, a cache and a north bridge. In another embodiment, such as that shown in Fig. 7, the CPU 705 and north bridge 710 are separate rather than integrated units. In yet another embodiment, such as that shown in Fig. 8, the HIC and PIC are integrated with the north and

south bridges, respectively, such that integrated HIC and north bridge unit 805 includes an HIC and a north bridge, while integrated PIC and south bridge unit 810 includes a PIC and a south bridge. Fig. 8A shows an attached computer module with integrated CPU/NB/Graphics 815 and Integrated HIC/SB 820. Fig. 8B shows an attached computer module with single chip 825 fully integrated: CPU, Cache, Core Logic, Graphics controller and Interface controller.

IN THE CLAIMS

1-43. (Cancelled)

44. (New) A computer system comprising:
a processing unit;
a peripheral bridge to communicate serial bits of Peripheral Component Interconnect (PCI) bus transaction, the peripheral bridge directly coupled to the processing unit;
a low voltage differential signal (LVDS) channel comprising at least two unidirectional, differential signal pairs to convey data in opposite directions, the LVDS channel extending from the peripheral bridge to convey the serial bits of PCI bus transaction, the serial bits of PCI bus transaction comprising PCI address and data bits;
a main memory coupled to the processing unit through the peripheral bridge; and
a peripheral component coupled to the peripheral bridge.
45. (New) The computer system of claim 44, wherein the peripheral component is coupled to the peripheral bridge through the LVDS channel.
46. (New) The computer system of claim 45, wherein the peripheral component is coupled to the processing unit through the LVDS channel and the peripheral bridge.
47. (New) The computer system of claim 45, wherein the peripheral component comprises a serial communication controller.
48. (New) The computer system of claim 44, further comprising a graphics subsystem coupled to the processing unit through the peripheral bridge.
49. (New) The computer system of claim 44, wherein the peripheral bridge comprises a north bridge.

50. (New) The computer system of claim 49, wherein the peripheral bridge comprises an interface controller integrated with the north bridge, the interface controller is coupled to the processing unit without any intervening PCI bus, and the interface controller is configured to output encoded address and data bits of PCI bus transaction in serial form that are conveyed over the LVDS channel.

51. (New) The computer system of claim 44, wherein the serial bits of PCI bus transaction comprise information to permit decoding to create a PCI bus transaction.

52. (New) The computer system of claim 44, wherein the LVDS channel comprises a first plurality of unidirectional, differential signal pairs to convey data in a first direction and a second plurality of unidirectional, differential signal pairs to convey data in a second, opposite direction.

53. (New) A computer system comprising:

a computer module insertable into a console for operation, the computer module comprising

a processing unit,

an integrated interface controller and bridge unit to output encoded address and data bits of Peripheral Component Interconnect (PCI) bus transaction in serial form, the integrated interface controller and bridge unit coupled to the processing unit without any intervening PCI bus,

a low voltage differential signal (LVDS) channel coupled to the integrated interface controller and bridge unit to convey the encoded address and data bits of PCI bus transaction in serial form, and

a main memory coupled to the processing unit through the integrated interface controller and bridge unit.

54. (New) The computer system of claim 53, further comprising a peripheral component coupled to the integrated interface controller and bridge unit through the LVDS channel.

55. (New) The computer system of claim 53, wherein the LVDS channel comprises a first plurality of unidirectional, differential signal pairs to convey data in a first direction and a second plurality of unidirectional, differential signal pairs to convey data in a second, opposite direction.
56. (New) The computer system of claim 53, wherein the integrated interface controller and bridge unit comprises a north bridge and an interface controller integrated with the north bridge.
57. (New) The computer system of claim 53, wherein the computer module comprises an enclosure housing the processing unit, the integrated interface controller and bridge unit, the LVDS channel, and the main memory.
58. (New) The computer system of claim 53, further comprising the console, and the console comprises a power supply to supply power to the computer module upon insertion into the console.
59. (New) The computer system of claim 58, wherein the console comprises a coupling site and a multi-port, serial communication hub controller, and the computer module comprises a serial communication controller to communicate, via a point-to-point link, with the multi-port, serial communication hub controller through the coupling site of the console.
60. (New) A computer system comprising:
 - a processing unit;
 - a low voltage differential signal (LVDS) channel comprising at least two unidirectional serial bit channels to convey data in opposite directions;
 - a north bridge coupled to the processing unit, the north bridge comprising an interface controller to transmit and receive serial bits of Peripheral Component Interconnect (PCI) bus transaction over the LVDS channel;
 - a main memory coupled to the processing unit through the north bridge; and
 - a south bridge coupled to the processing unit through the north bridge.

61. (New) The computer system of claim 60, wherein the south bridge is coupled to the north bridge through the LVDS channel.

62. (New) The computer system of claim 61, further comprising a peripheral component coupled to the processing unit through the south bridge, the LVDS channel, and the north bridge.

63. (New) The computer system of claim 60, wherein the north bridge is directly coupled to the processing unit.

64. (New) The computer system of claim 60, wherein the north bridge and the interface controller are coupled to the processing unit without any intervening PCI bus, and the interface controller is integrated with the north bridge.

65. (New) The computer system of claim 60, wherein the serial bits of PCI bus transaction comprise encoded PCI address and data bits, the LVDS channel extends from the north bridge to convey the encoded PCI address and data bits, and the LVDS channel comprises a first plurality of unidirectional, differential signal pairs to convey data in a first direction and a second plurality of unidirectional, differential signal pairs to convey data in a second, opposite direction.

66. (New) A computer system comprising:

- a processing unit;
- a main memory coupled to the processing unit;
- a first low voltage differential signal (LVDS) channel comprising at least two unidirectional serial bit channels to convey data in opposite directions;
- a first peripheral bridge coupled to the processing unit without any intervening Peripheral Component Interconnect (PCI) bus, the first peripheral bridge coupled to the first LVDS channel to communicate address and data information of PCI bus transaction in serial form over the first LVDS channel; and
- a second peripheral bridge coupled to the first peripheral bridge.

67. (New) The computer system of claim 66, wherein the main memory is coupled to the processing unit through the first peripheral bridge.

68. (New) The computer system of claim 66, wherein the second peripheral bridge is coupled to the first peripheral bridge through the first LVDS channel.

69. (New) The computer system of claim 66, wherein the first LVDS channel comprises two sets of unidirectional, multiple serial bit channels to convey data in opposite directions.

70. (New) The computer system of claim 66, further comprising a mass storage device coupled to the second peripheral bridge.

71. (New) The computer system of claim 66, further comprising a second LVDS channel comprising at least two unidirectional serial bit channels to convey data in opposite directions, and the second peripheral bridge is coupled to the second LVDS channel to communicate PCI bus transaction in serial form over the second LVDS channel.

72. (New) The computer system of claim 66, wherein the first peripheral bridge comprises a north bridge, and the second peripheral bridge comprises a south bridge.

73. (New) The computer system of claim 72, wherein the first peripheral bridge comprises an interface controller integrated with the north bridge, the interface controller is configured to output an encoded serial bit stream of PCI bus transaction, and the first LVDS channel extends from the interface controller to convey the encoded serial bit stream of PCI bus transaction.

74. (New) A computer module comprising:
an enclosure insertable into a console;
a processing unit housed in the enclosure, the processing unit comprising an interface controller to transmit and receive serial bits of Peripheral Component Interconnect (PCI) bus transaction, the serial bits of PCI bus transaction comprising PCI address and data bits;
a system memory housed in the enclosure and directly coupled to the processing unit; and

a low voltage differential signal (LVDS) channel housed in the enclosure, the LVDS channel comprising a first unidirectional, differential signal pair to convey data in a first direction and a second unidirectional, differential signal pair to convey data in a second, opposite direction, the LVDS channel extending from the processing unit to convey the serial bits of PCI bus transaction.

75. (New) The computer module of claim 74, wherein the processing unit and the interface controller are integrated in a single chip.

76. (New) The computer module of claim 75, wherein the processing unit comprises a graphics subsystem integrated in the single chip.

77. (New) The computer module of claim 76, further comprising a graphics memory directly coupled to the processing unit.

78. (New) The computer module of claim 74, further comprising a mass storage device directly coupled to the processing unit.

79. (New) The computer module of claim 74, wherein the interface controller is configured to output encoded address and data bits of PCI bus transaction in serial form that are conveyed over the LVDS channel.

80. (New) The computer module of claim 74, wherein the LVDS channel comprises a third unidirectional, differential signal pair to convey data in the first direction and a fourth unidirectional, differential signal pair to convey data in the second, opposite direction.

81. (New) The computer module of claim 74, wherein the computer module is configured to operate only upon receiving power from the console.

82. (New) The computer module of claim 74, wherein the enclosure defines a set of grooves to engage a corresponding set of rails of the console.

83. (New) A computer system comprising:
a computer module comprising
an enclosure insertable into a console,
an integrated interface controller and processing unit to output encoded address and data bits of Peripheral Component Interconnect (PCI) bus transaction in serial form, the integrated interface controller and processing unit configured as a single chip and housed in the enclosure,
a low voltage differential signal (LVDS) channel housed in the enclosure, the LVDS channel coupled to the integrated interface controller and processing unit to convey the encoded address and data bits of PCI bus transaction in serial form, and
a system memory housed in the enclosure and coupled to the integrated interface controller and processing unit.
84. (New) The computer system of claim 83, wherein the integrated interface controller and processing unit comprises a graphics subsystem integrated in the single chip.
85. (New) The computer system of claim 84, further comprising the console, and the console comprises a LCD display coupled to the graphics subsystem.
86. (New) The computer system of claim 83, further comprising a peripheral component coupled to the integrated interface controller and processing unit through the LVDS channel.
87. (New) The computer system of claim 83, wherein the LVDS channel comprises a first plurality of unidirectional, differential signal pairs to convey data in a first direction and a second plurality of unidirectional, differential signal pairs to convey data in a second, opposite direction.
88. (New) The computer system of claim 83, further comprising the console, and the console comprises a power supply to supply power to the computer module upon insertion into the console.

89. (New) The computer system of claim 88, wherein the console comprises a coupling site and a multi-port, Ethernet hub controller, and the computer module comprises an Ethernet controller to communicate, via a point-to-point Ethernet link, with the multi-port, Ethernet hub controller through the coupling site of the console.

90. (New) A computer system comprising:
 a low voltage differential signal (LVDS) channel comprising at least two unidirectional serial bit channels to convey data in opposite directions;
 a processing unit comprising an interface coupled to the LVDS channel to communicate PCI bus transaction in serial form over the LVDS channel;
 a system memory directly coupled to the processing unit; and
 a peripheral component coupled to the processing unit through the LVDS channel.

91. (New) The computer system of claim 90, wherein the processing unit comprises a graphics subsystem integrated with the processing unit in a single chip.

92. (New) The computer system of claim 91, further comprising a graphics memory directly coupled to the processing unit.

93. (New) The computer system of claim 90, further comprising a mass storage device directly coupled to the processing unit.

94. (New) The computer system of claim 90, wherein the peripheral component comprises a serial communication controller.

95. (New) The computer system of claim 90, wherein the LVDS channel comprises two sets of unidirectional, multiple serial bit channels to convey data in opposite directions.

96. (New) The computer system of claim 90, wherein the interface of the processing unit is configured to output an encoded serial bit stream of PCI address and data information, and the

LVDS channel extends from the interface of the processing unit to convey the encoded serial bit stream.

REMARKS

This is a preliminary amendment of the subject application, which is a continuation of U.S. Application No. 12/504,534 (the “534 parent application”), which is a continuation of U.S. Application No. 12/077,503, which is a continuation of U.S. Application No. 11/166,656, which is a continuation of U.S. Application No. 11/097,694, which is a continuation of U.S. Application No. 10/772,214, which is a continuation of U.S. Application No. 09/569,758 (the “758 parent application”). A copy of the ‘534 parent application (as filed) is submitted herewith, and amendments are set forth by this paper relative to the ‘534 parent application.

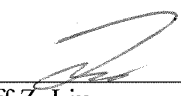
The original ‘758 parent application incorporated by reference U.S. Application No. 09/149,882 (now issued as U.S. Patent No. 6,345,330), which, in turn, claimed the benefit of and incorporated by reference U.S. Provisional Application No. 60/083,886 (the “886 provisional application”) (See checked incorporation by reference box in utility patent application transmittal of U.S. Application No. 09/149,882 filed on September 8, 1998). By this preliminary amendment, the subject application is amended to specifically include certain figures and text from the ‘886 provisional application. Specifically, the subject application is amended to add new FIG. 8A and FIG. 8B, as well as accompanying text for these added figures. This corresponds to: (a) figure 8 and figure 9 of the ‘886 provisional application; and (b) the text of the ‘886 provisional application as originally included in figure legends of figure 8 and figure 9.

Also by this preliminary amendment, claims 1-43 are cancelled, and new claims 44-96 are added. Accordingly, claims 44-96 are now pending in the subject application.

Entry and consideration of the foregoing amendments is respectfully requested.

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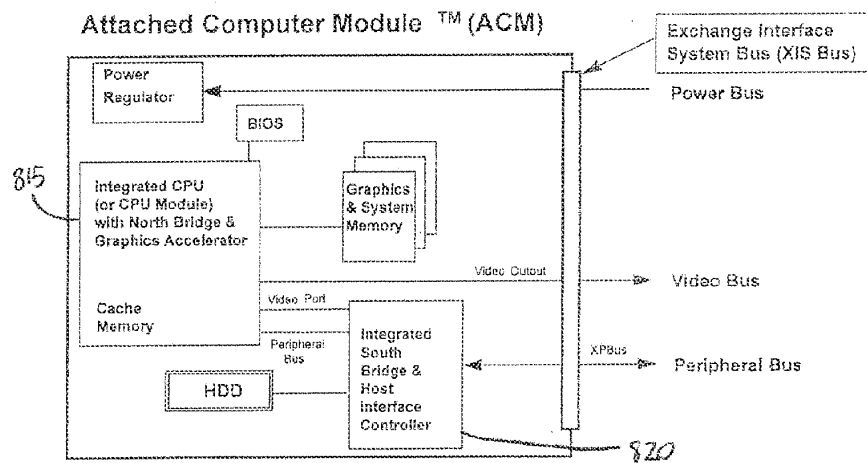


FIG. 8A Attached Computer Module with Integrated CPU/NB/Graphics and Integrated HIC/SB

NEW SHEET

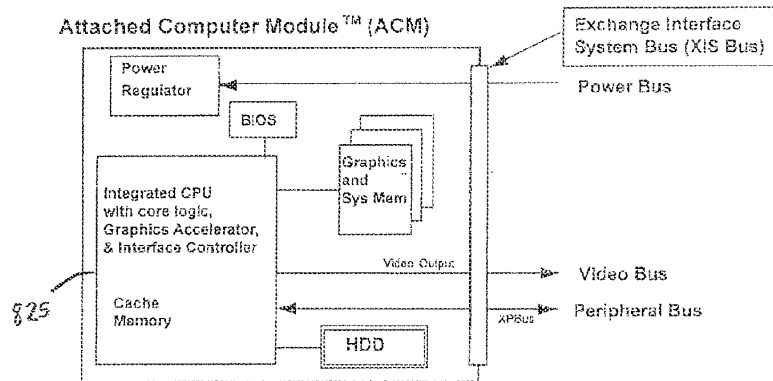


FIG. 8B Attached Computer Module with Single Chip fully integrated: CPU, Cache, Core logic, Graphics controller and Interface controller

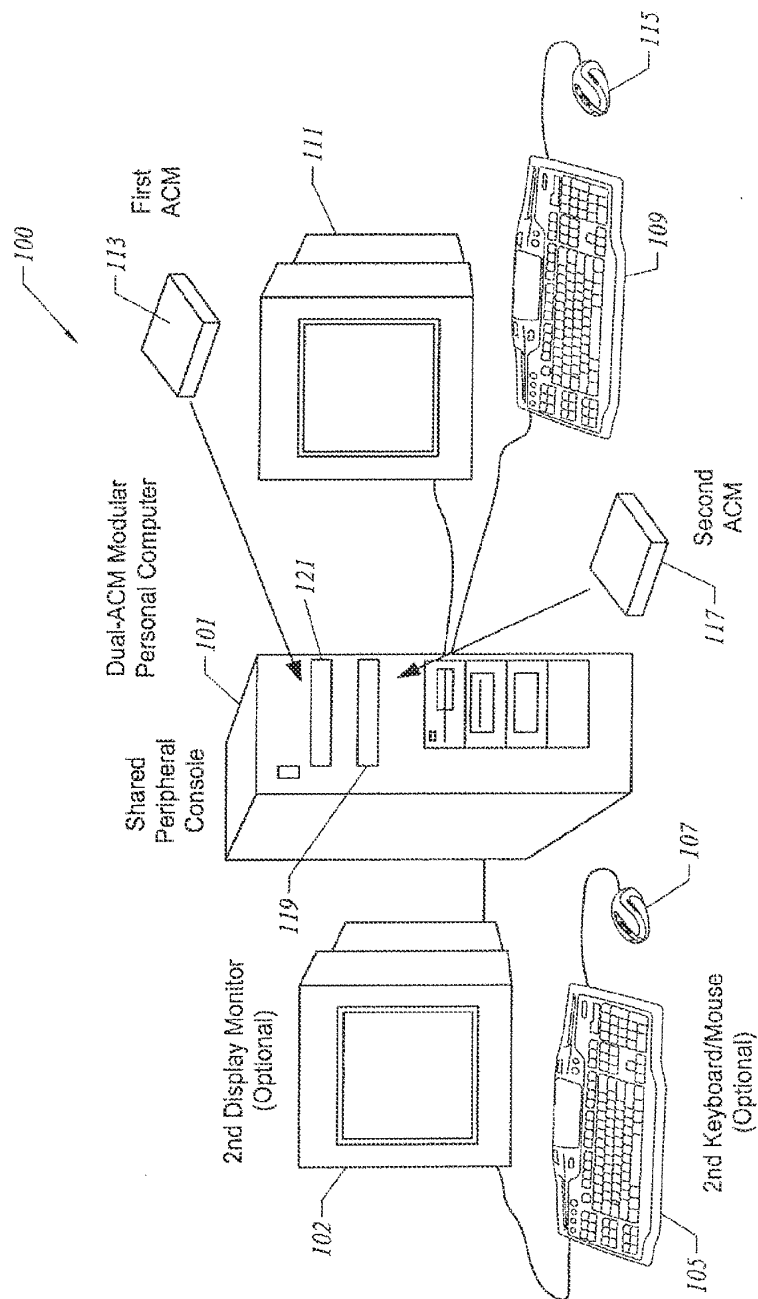


FIGURE 1

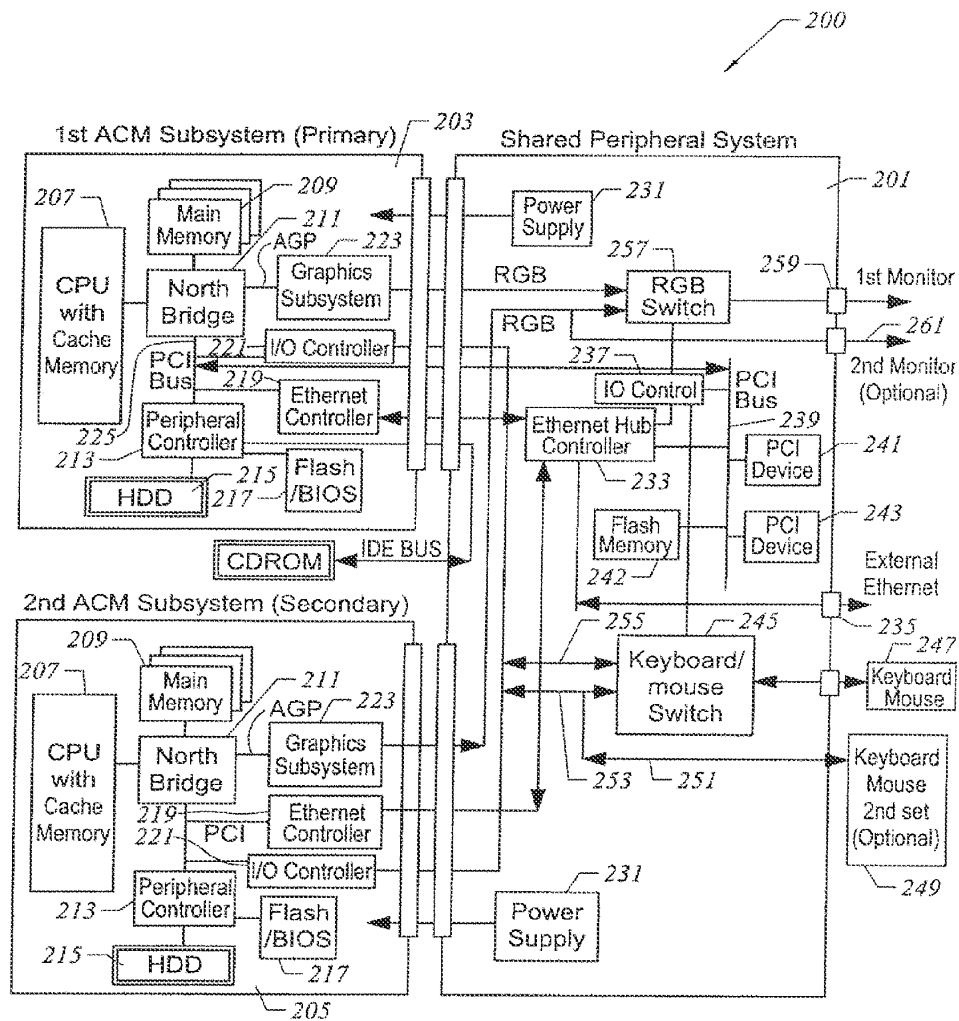


FIGURE 2

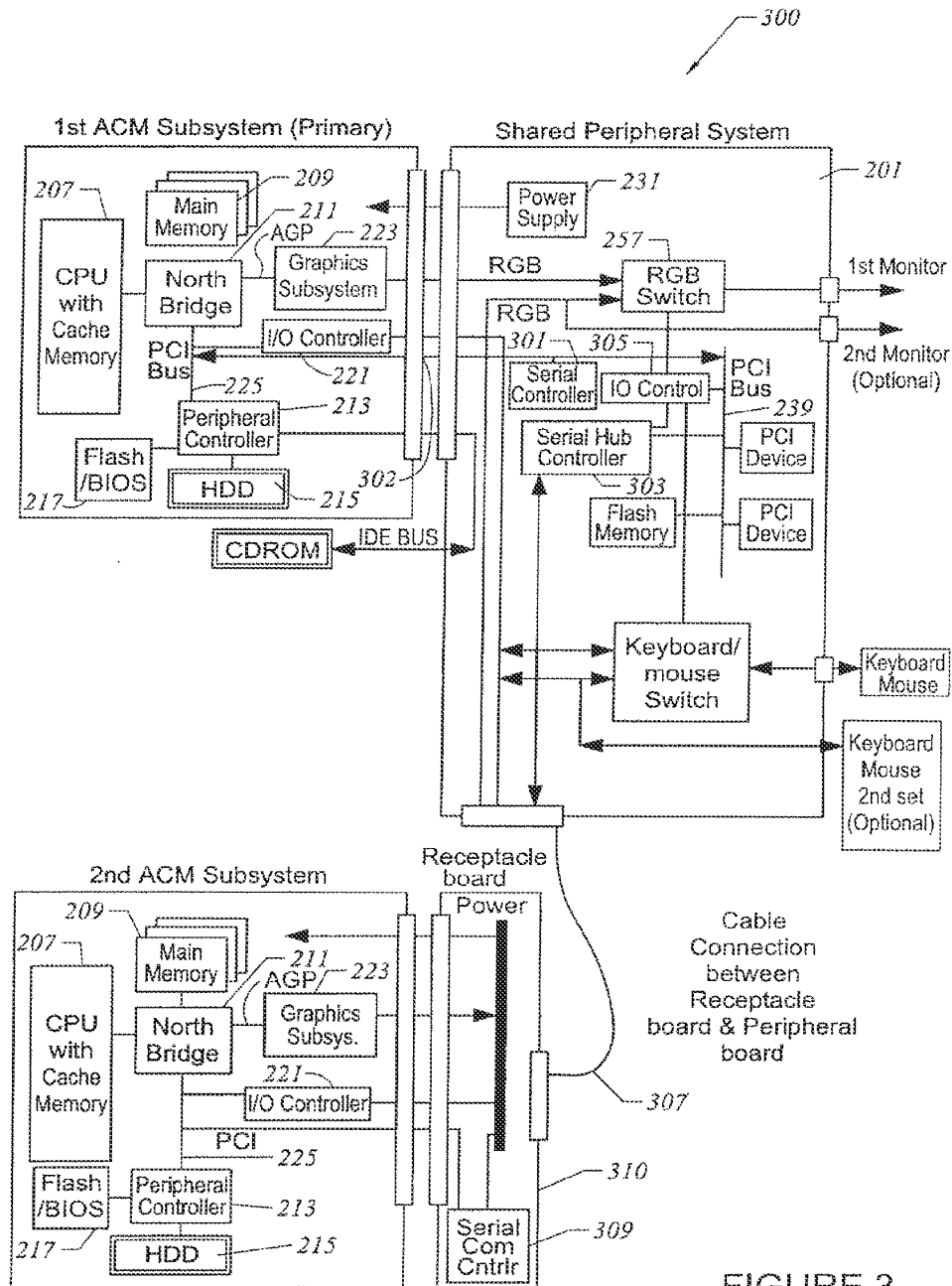


FIGURE 3

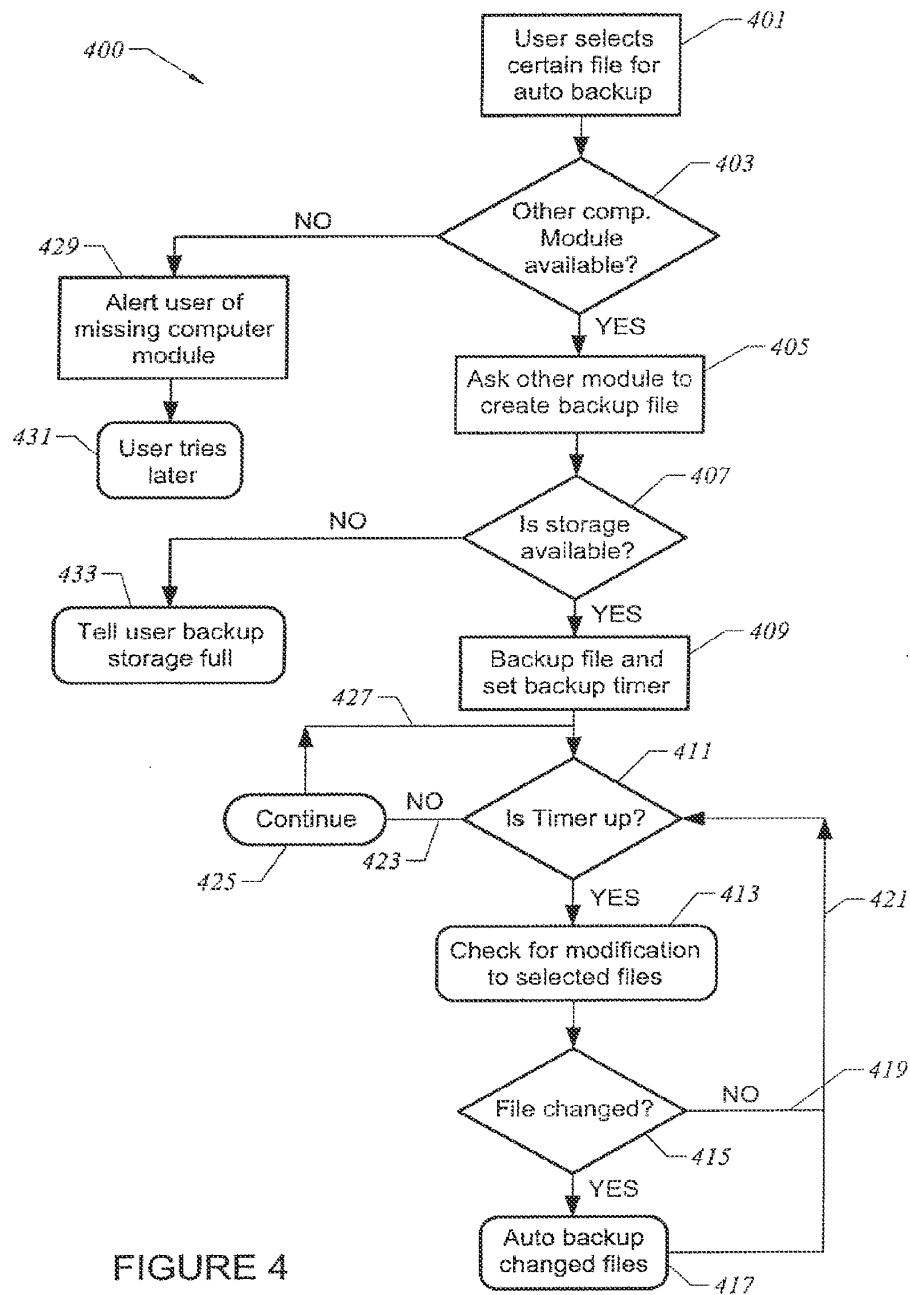


FIGURE 4

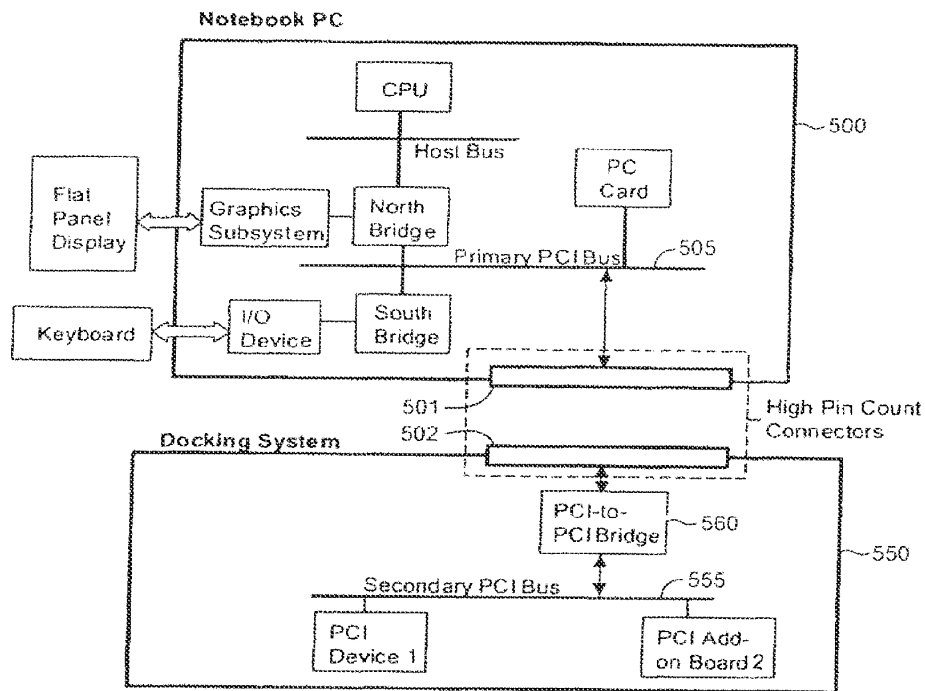


FIGURE 5

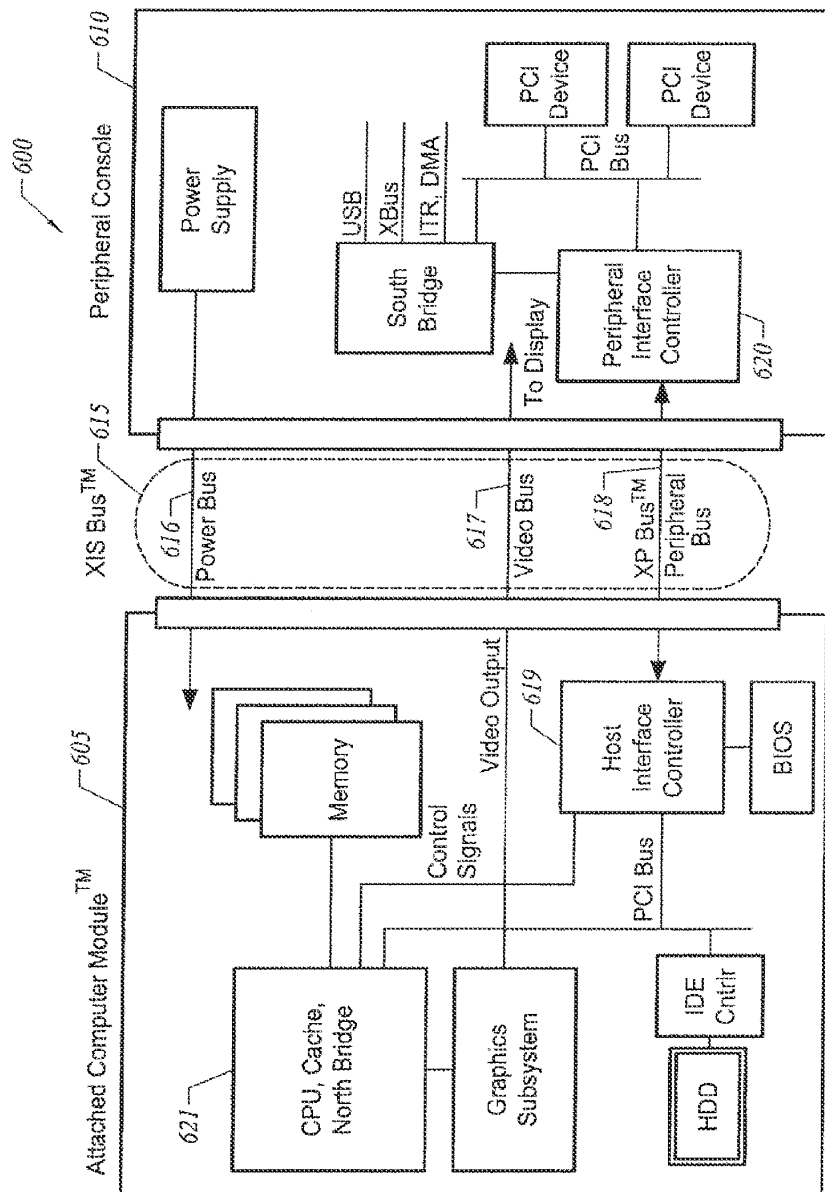


FIGURE 6

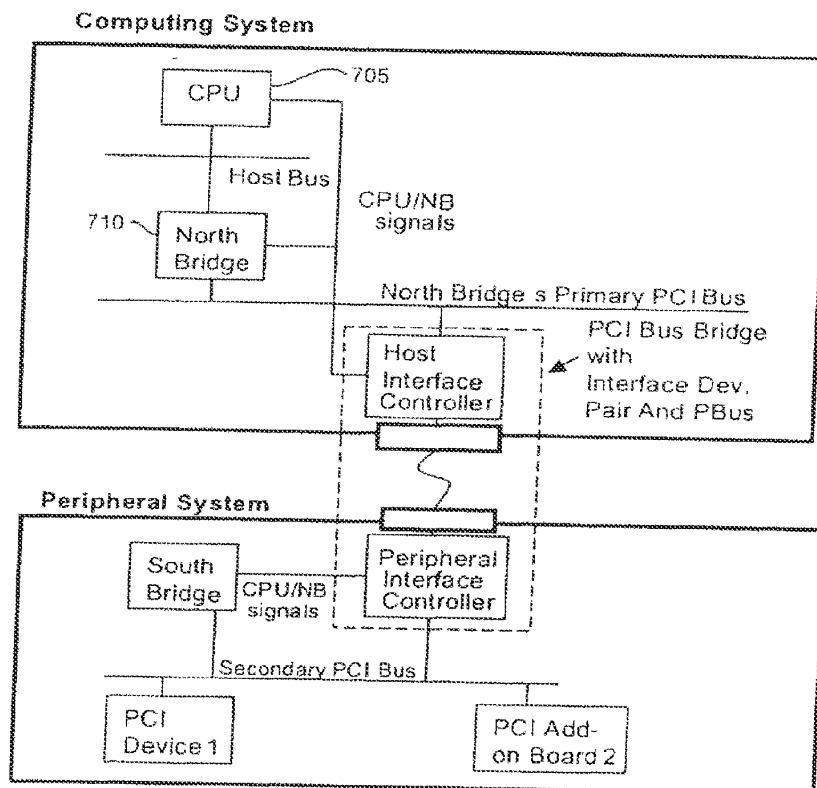


FIGURE 7

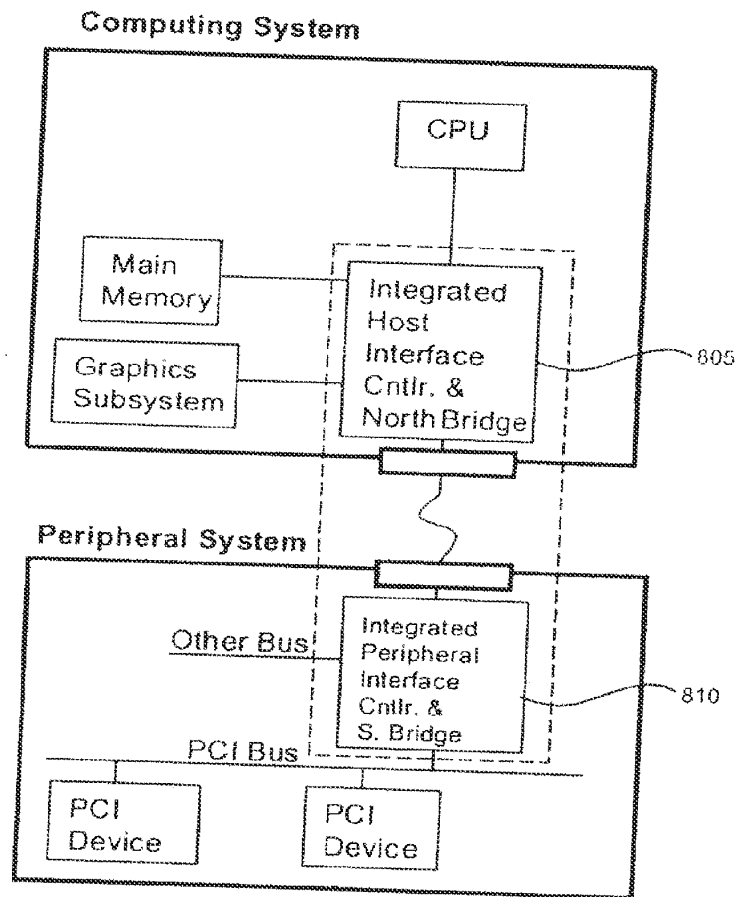


FIGURE 8

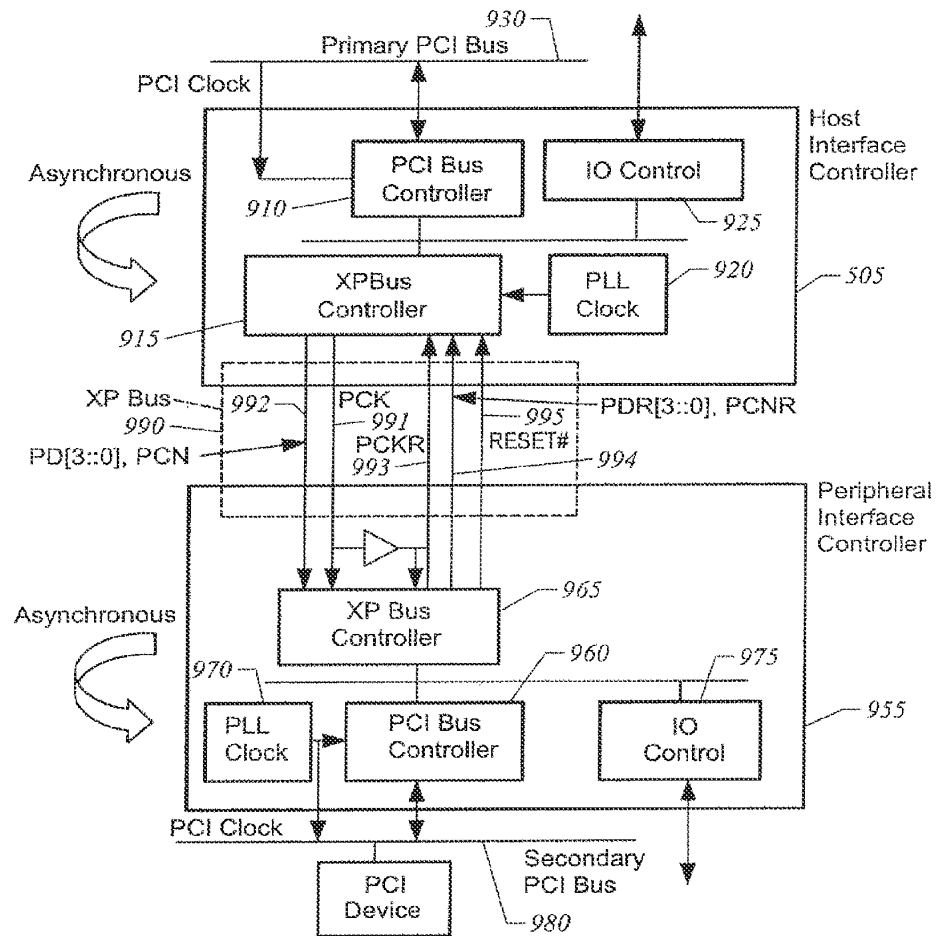


FIGURE 9

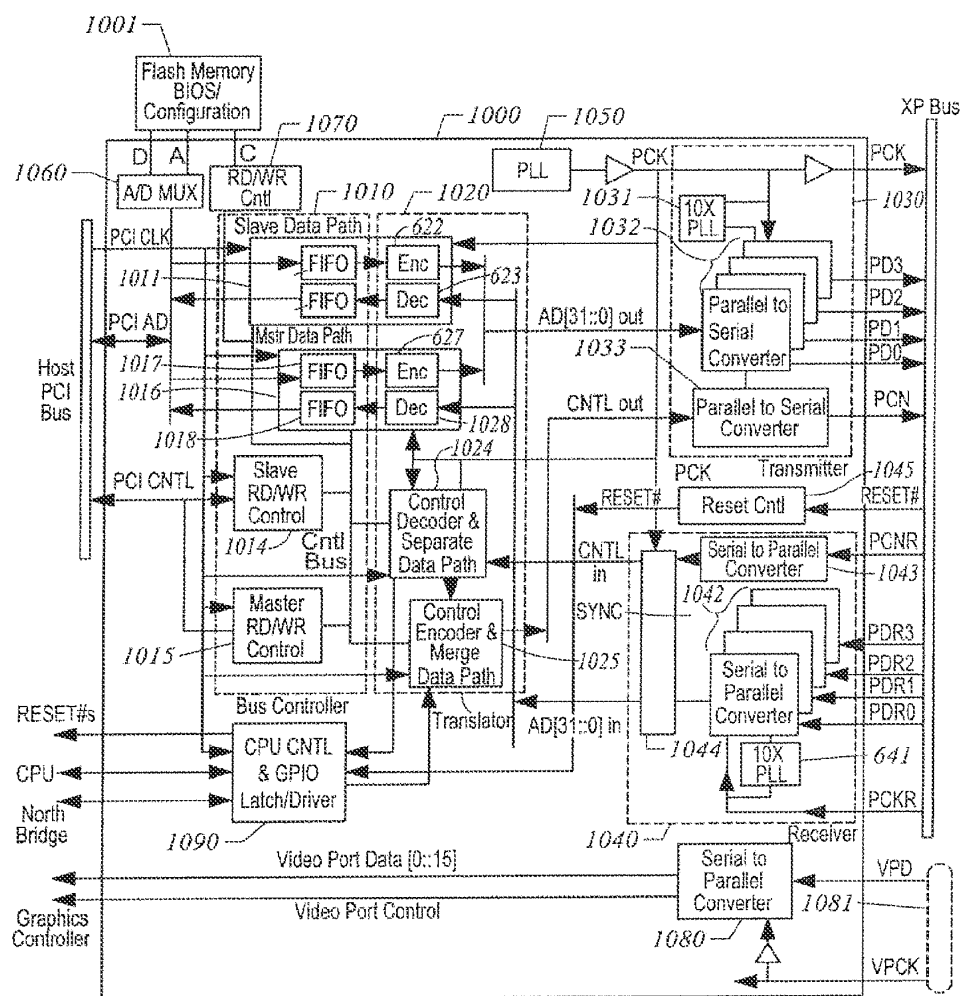


FIGURE 10

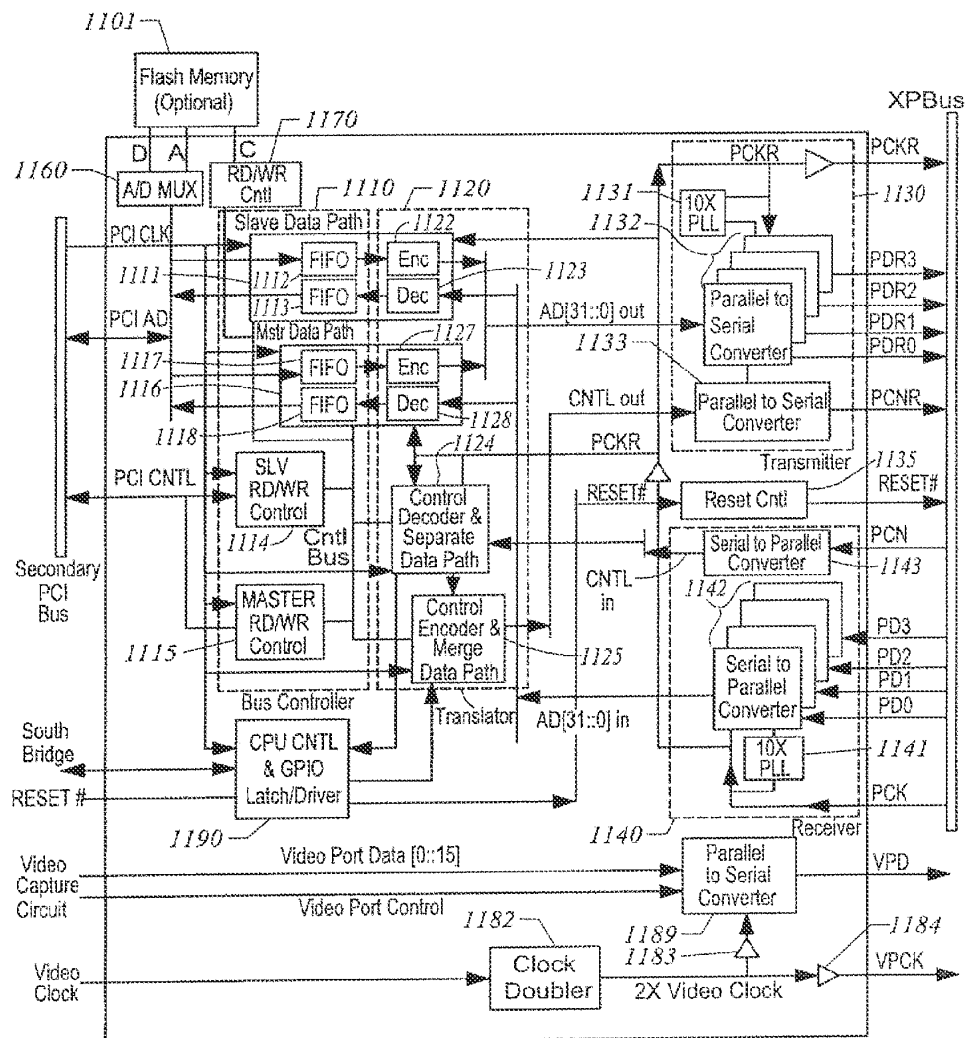


FIGURE 11

	Symbol	Signal	Data Rate	Description
1	PD0 RTN			GND
2	PD0+	Synch. To PCK	10 x clock rate	Computer to Peripheral LVDS Data 0+
3	PD0-			Computer to Peripheral LVDS Data 0-
4	PD1 RTN			GND
5	PD1+	Synch. To PCK	10 x clock rate	Computer to Peripheral LVDS Data 1+
6	PD1-			Computer to Peripheral LVDS Data 1-
7	PD2 RTN			GND
8	PD2+	Synch. To PCK	10 x clock rate	Computer to Peripheral LVDS Data 2+
9	PD2-			Computer to Peripheral LVDS Data 2-
10	PD3 RTN			GND
11	PD3+	Synch. To PCK	10 x clock rate	Computer to Peripheral LVDS Data 3+
12	PD3-			Computer to Peripheral LVDS Data 3-
13	PCK RTN			GND
14	PCK+	Clock	Clock rate	Computer to Peripheral LVDS Clock +
15	PCK-			Computer to Peripheral LVDS Clock -
16	PCN RTN			GND
17	PCN+	Synch. To PCK	10 x clock rate	Computer to Peripheral LVDS Control +
18	PCN-			Computer to Peripheral LVDS Control -
19	PDR0 RTN			GND
20	PDR0+	Synch. To PCKR	10 x clock rate	Peripheral to Computer LVDS Data 0+
21	PDR0-			Peripheral to Computer LVDS Data 0-
22	PDR1 RTN			GND
23	PDR1+	Synch. To PCKR	10 x clock rate	Peripheral to Computer LVDS Data 1+
24	PDR1-			Peripheral to Computer LVDS Data 1-
25	PDR2 RTN			GND
26	PDR2+	Synch. To PCKR	10 x clock rate	Peripheral to Computer LVDS Data 2+
27	PDR2-			Peripheral to Computer LVDS Data 2-
28	PDR3 RTN			GND
29	PDR3+	Synch. To PCKR	10 x clock rate	Peripheral to Computer LVDS Data 3+
30	PDR3-			Peripheral to Computer LVDS Data 3-
31	PCKR RTN			GND
32	PCKR+	Reverse Dir Clock	Clock rate	Peripheral to Computer LVDS Clock +
33	PCKR-			Peripheral to Computer LVDS Clock -
34	PCNR RTN			GND
35	PCNR+	Synch. To PCKR	10 x clock rate	Peripheral to Computer LVDS Control +
36	PCNR-			Peripheral to Computer LVDS Control -
37	RESET#		Asynchronous	Reset

FIGURE 12

[illegible]

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PCK+										PCK-										PCK+								PCK-							
BS0	C0#	A00	A01	A02	A03	A04	A05	A06	A07	BS0																									
BS1	C1#	A08	A09	A10	A11	A12	A13	A14	A15	BS1																									
BS2	C2#	A16	A17	A18	A19	A20	A21	A22	A23	BS2																									
BS3	C3#	A24	A25	A26	A27	A28	A29	A30	A31	BS3																									
0	CN0	CN1	CN2	CN3	CN4	CN5	CN6	CN7	CN8	1	CN9	CN10	CN11	CN12	CN13	CN14	CN15	CN16	CN17																

PCK+										PCK-										PCK+								PCK-							
BS0	BE0#	D00	D01	D02	D03	D04	D05	D06	D07	BS0																									
BS1	BE1#	D08	D09	D10	D11	D12	D13	D14	D15	BS1																									
BS2	BE2#	D16	D17	D18	D19	D20	D21	D22	D23	BS2																									
BS3	BE3#	D24	D25	D26	D27	D28	D29	D30	D31	BS3																									
0	CN0	CN1	CN2	CN3	CN4	CN5	CN6	CN7	CN8	1	CN9	CN10	CN11	CN12	CN13	CN14	CN15	CN16	CN17																

FIGURE 14

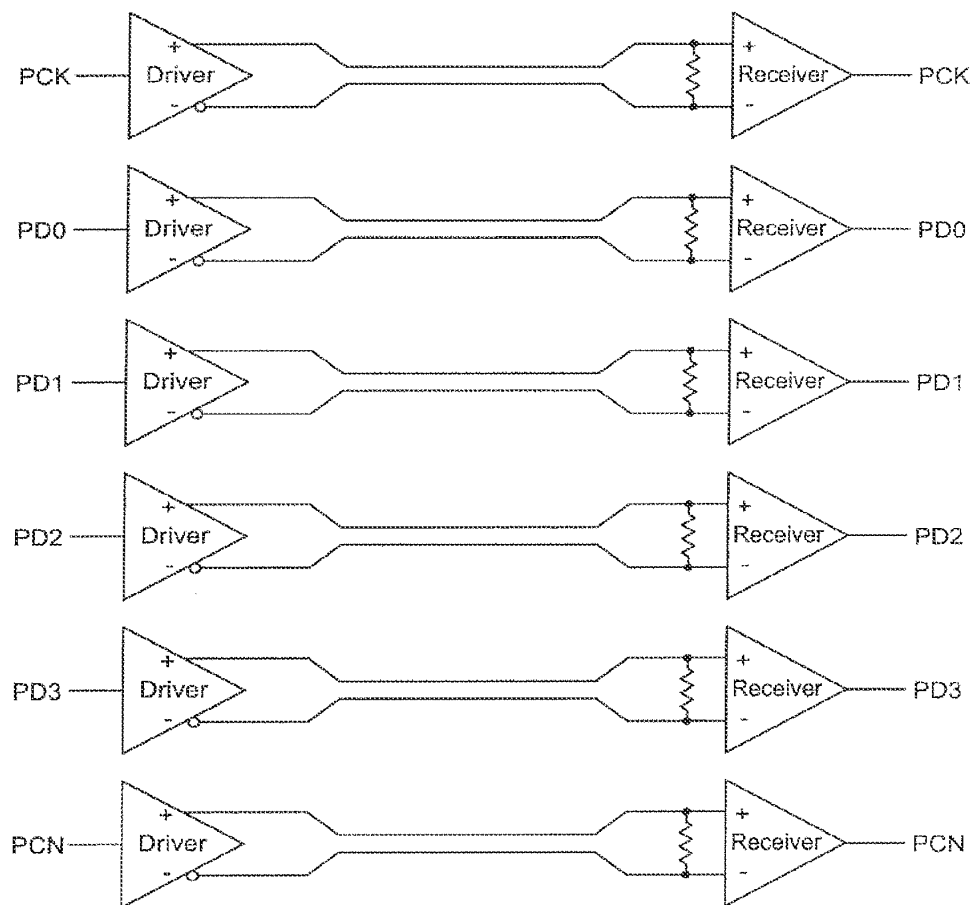


FIGURE 15

Name	Type	Pins	Description
AD[31:0]	TS	32	Multiplexed Address/Data. AD is driven to a valid state when GNT# is asserted.
C/BE[3:0]#	TS	4	Multiplexed Command/Byte Enables. For a two-address transaction, 1st address phase carries the command, and the 2nd address phase carries the transaction type C/BE is driven to a valid state when GNT# is asserted.
FRAME#	STS	1	Indicates beginning and duration of a PCI transaction. When the bus is idle, FRAME# is driven to High for 1 cycle. A pull-up resistor sustains STS signal.
IRDY#	STS	1	Initiator Ready. IRDY# is driven High for 1 cycle if bus is idle, and the state is sustained by a pull-up resistor.
TRDY#	STS	1	Target Ready. When bus is idle, TRDY# is driven High for 1 cycle if bus is idle. An external pull-up resistor sustains STS signal.
DEVSEL#	STS	1	Device Select. DEVSEL# is asserted by target to indicate it is ready to accept the transaction. HIC decodes address of a transaction to decide the need to assert DEVSEL#. As an initiator, HIC waits for 5 cycles to detect assertion of DEVSEL# by the target; otherwise HIC terminates with a master abort. DEVSEL# is driven High for 1 cycle when bus is idle, and the state is sustained by a pull-up resistor.
STOP#	STS	1	Target request to stop transaction. There are 3 cases: STOP#, TRDY# & DEVSEL# asserted: disconnect with data transfer Only STOP# & DEVSEL# asserted: request initiator to retry later Only STOP# asserted: target abort STOP# is driven High for 1 cycle when bus is idle, and the state is sustained by a pull-up resistor.
PAR	TS	1	Even parity for 36 bits of AD & C/BE#. PAR is sent one cycle after address or data is valid. In write transaction, initiator sends PAR one cycle after write data is valid. In read transaction, target sends PAR one cycle after read data is valid.
LOCK#	Input	1	Initiator request lock on target downstream. LOCK# is asserted 1 clock cycle after address phase by an initiator wanting to perform an atomic operation that take more than one transaction to complete. HIC passes the LOCK# request to the secondary PCI bus. HIC does not drive LOCK# or propagate LOCK# upstream.
IDSEL#	Input	1	Chip Select for Type 0 configuration access. During a Type 0 configuration transaction, the initiator asserts IDSEL# during the address phase to select HIC. HIC responds by asserting DEVSEL#.
PERR#	STS	1	Data Parity Error on all transactions except Special Cycle. PERR# is driven one clock cycle after PAR. PERR# is asserted by target during write transactions, and by initiator during read transactions.
SERR#	OD	1	System Error. HIC asserts SERR# under the following conditions: Address parity error. Secondary bus SERR# asserted. Posted write transaction: data parity error on target bus. Posted write transaction discarded. Master abort. Target abort Delayed read or write transaction discarded, and Delayed transaction master timeout.
REQ#	TS	1	Request for bus. If a target retry or disconnect is received in response to initiating a transaction, HIC deasserts REQ# for at least 2 cycles before asserting it again.
GNT#	Input	1	Bus is granted to HIC. HIC can initiate transaction if GNT# is asserted and the bus is idle. When HIC is not requesting bus and GNT# is asserted, HIC must drive AD, C/BE, and PAR to valid logic levels.
CLKRUN#	I/OD	1	Input indicating clock status. HIC can request the central clock resource to start, speed up or maintain the PCI clock. There are 3 clocking states: Clock running, Clock about to stop/slow down, and Clock stopped/slowed.
PCICK	Input	1	PCI Clock. All inputs are sampled on the rising edge of PCICK. Frequency

FIGURE 16

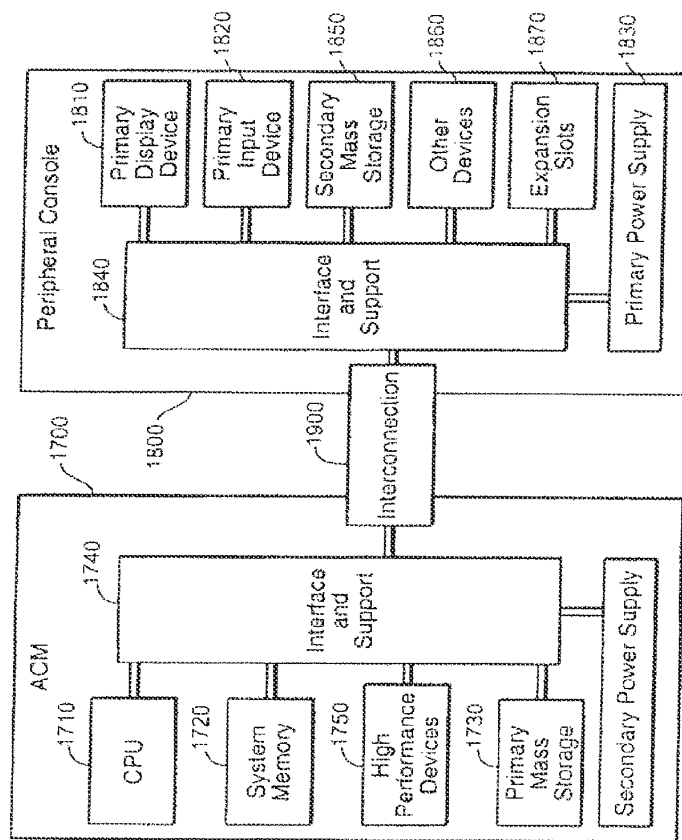


FIGURE 17

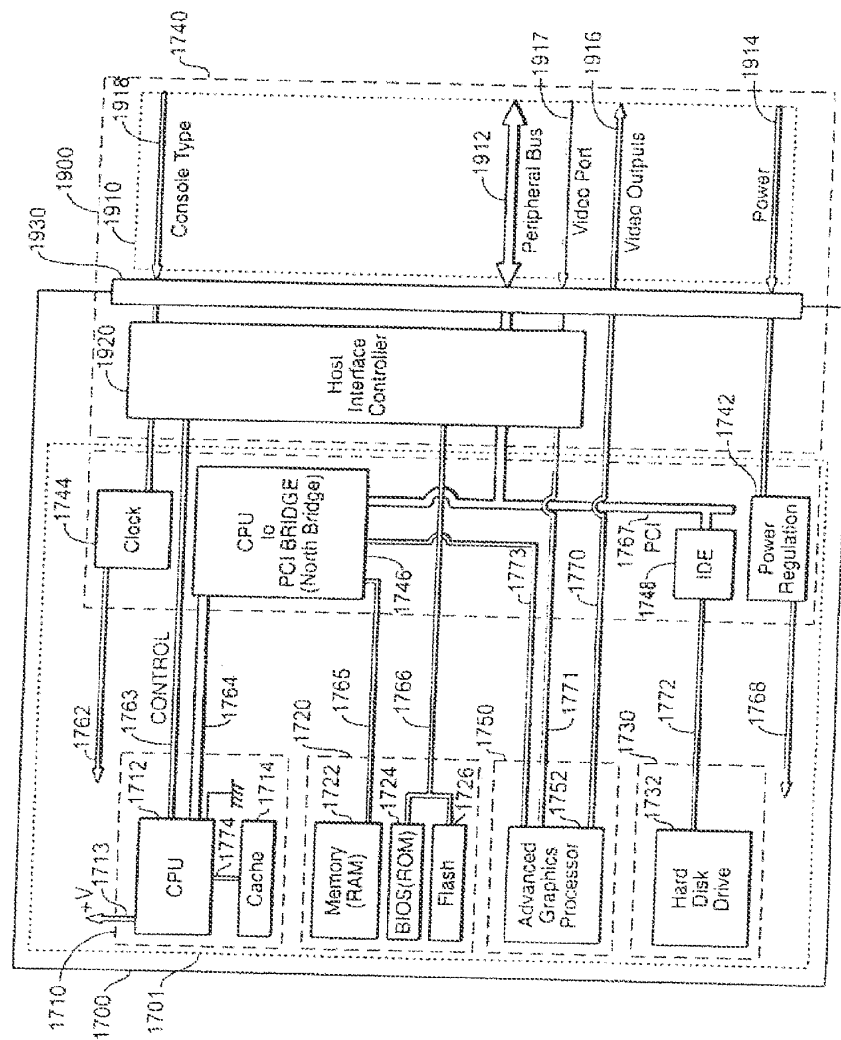


FIGURE 18

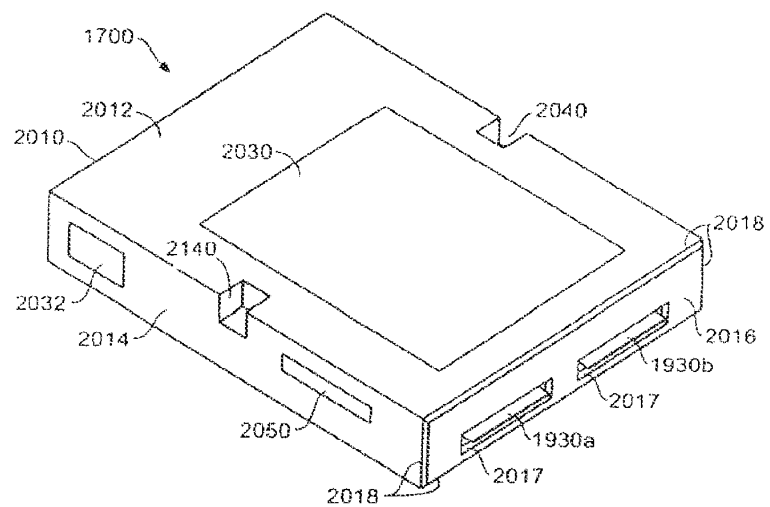


FIGURE 19

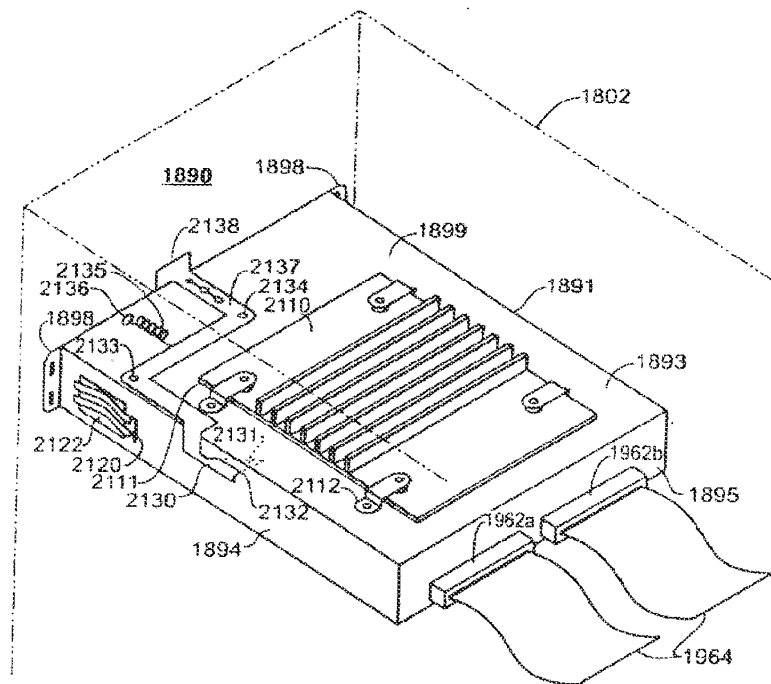
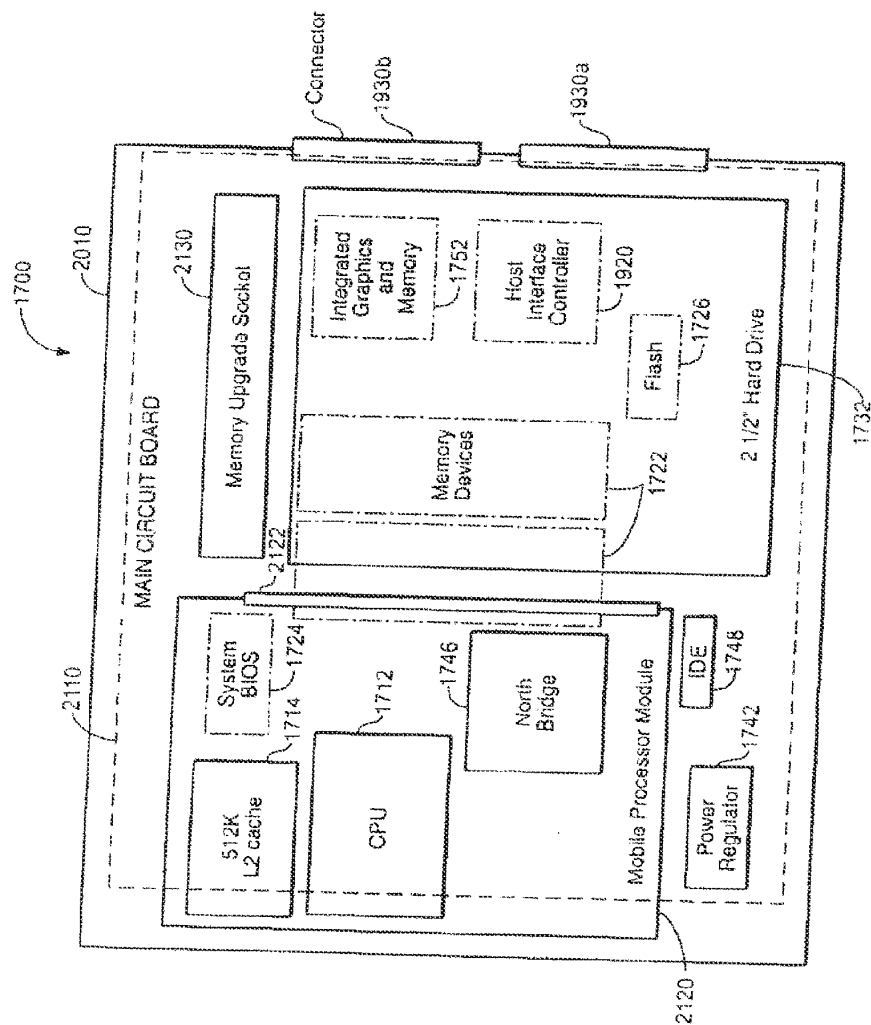
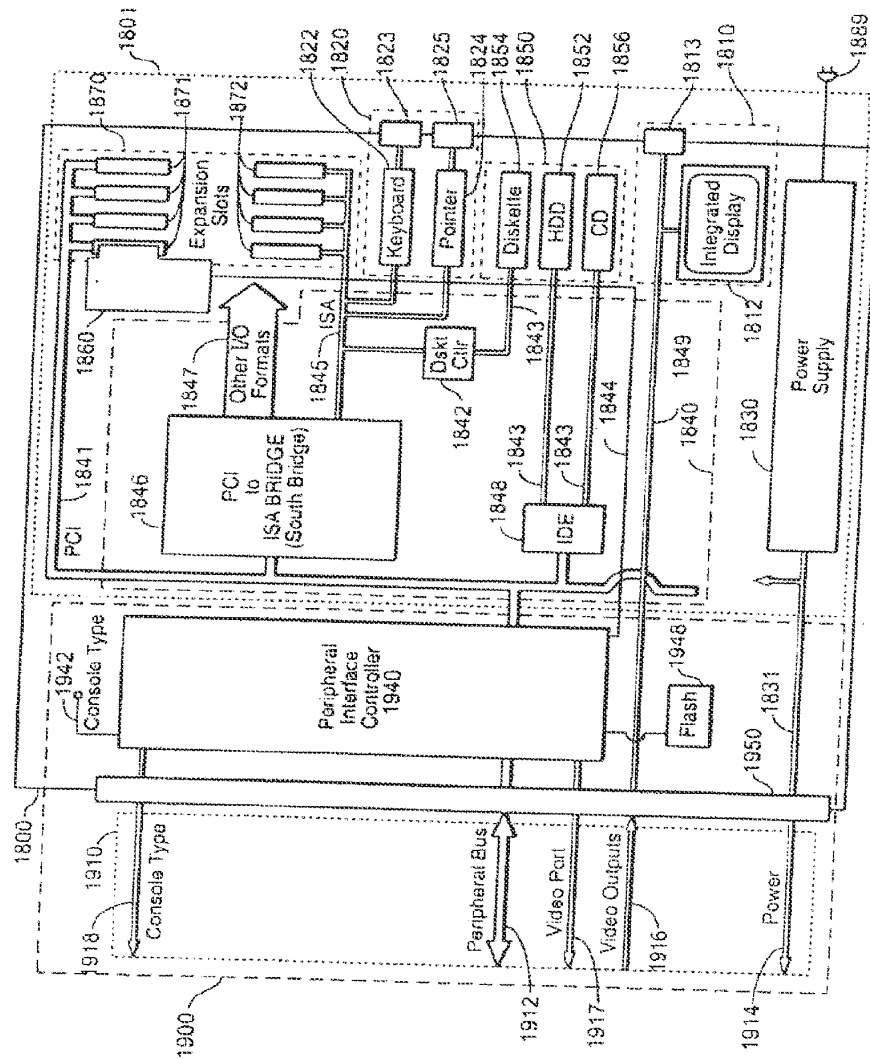


FIGURE 19B





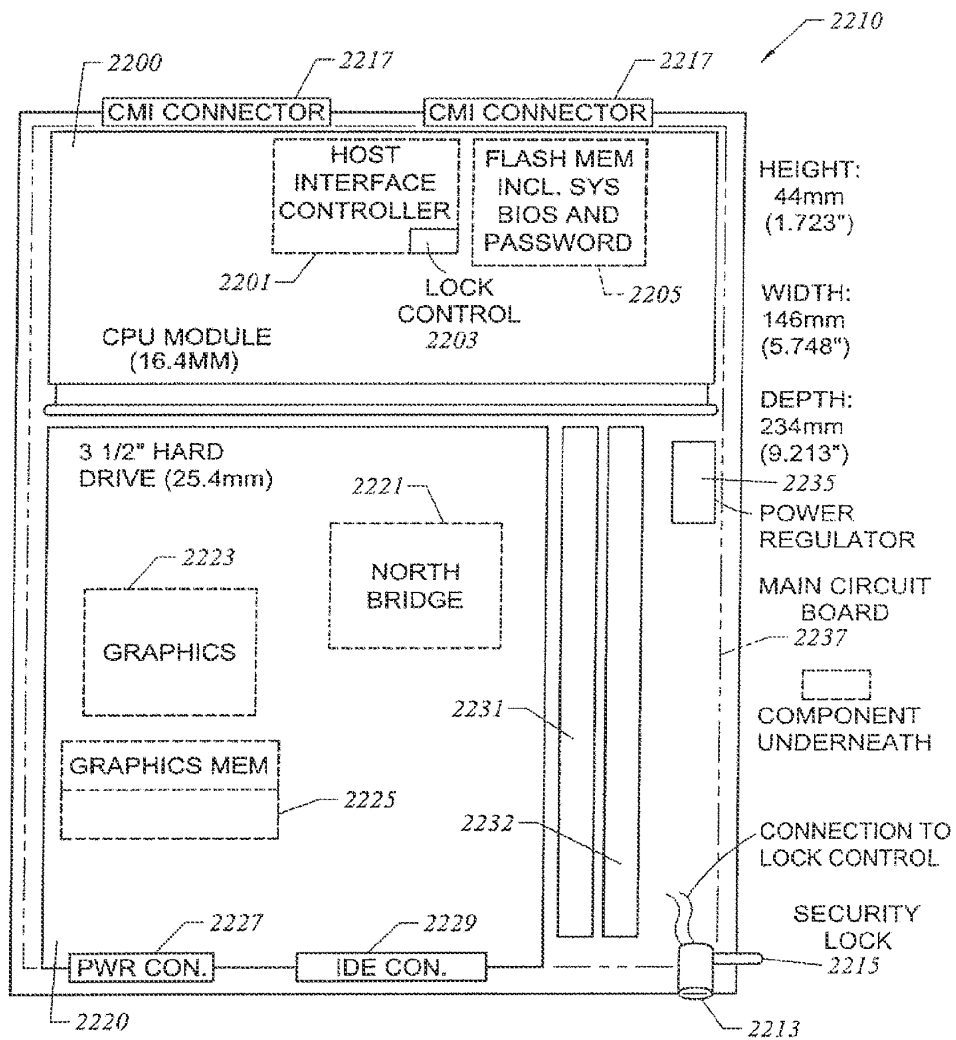


FIGURE 22

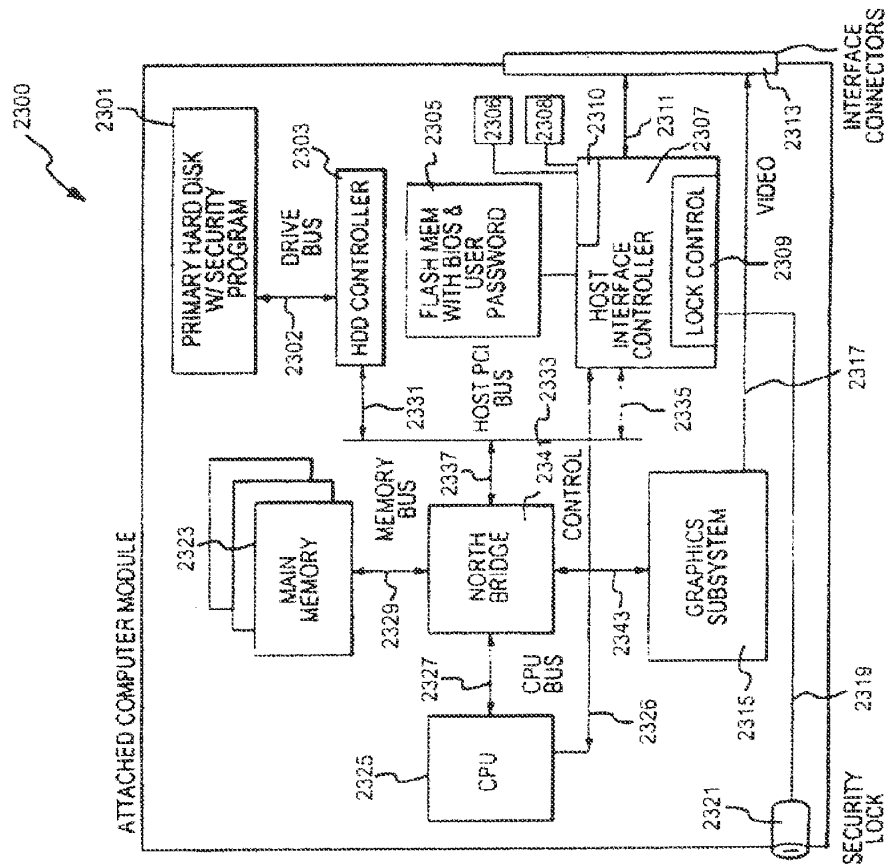


FIGURE 23

**MULTIPLE MODULE COMPUTER SYSTEM AND METHOD INCLUDING
DIFFERENTIAL SIGNAL CHANNEL COMPRISING UNIDIRECTIONAL
SERIAL BIT CHANNELS**

CROSS REFERENCE TO RELATED APPLICATIONS

[0001] This application is a continuation of U.S. Application No. 12/077,503 filed March 18, 2008, which is a continuation of U.S. nonprovisional Application No. 11/166,656, filed June 24, 2005 (Now U.S. Patent No. 7,376,779), which is a continuation of U.S. nonprovisional Application No. 11/097,694, filed March 31, 2005 (Now U.S. Patent No. 7,363,415), which is a continuation of U.S. nonprovisional Application No. 10/772,214, filed February 3, 2004 (Now U.S. Patent No. 7,099,981), which is a continuation of U.S. nonprovisional Application No. 09/569,758, filed May 12, 2000 (Now U.S. patent no. 6,718,415), and which claimed priority to U.S. Provisional Application No. 60/134,122 filed May 14, 1999. These applications are hereby incorporated by reference in their entirety.

BACKGROUND OF THE INVENTION

[0002] The present invention relates to computing devices. More particularly, the present invention provides a system including a plurality of computer modules that can independently operate to provide backup capability, dual processing, and the like. Merely by way of example, the present invention is applied to a modular computing environment for desk top computers, but it will be recognized that the invention has a much wider range of applicability. It can be applied to a server as well as other portable or modular computing applications.

[0003] Many desktop or personal computers, which are commonly termed PCs, have been around and used for over ten years. The PCs often come with state-of-art microprocessors such as the Intel Pentium™ microprocessor chips. They also include a hard or fixed disk drive such as memory in the giga-bit range. Additionally, the PCs often include a random access memory integrated circuit device such as a dynamic random access memory device, which is commonly termed DRAM. The DRAM devices now provide up to millions of memory cells (i.e., mega-bit) on a single slice of silicon. PCs also include a high resolution display such as cathode ray tubes or CRTs. In most cases,

the CRTs are at least 15 inches or 17 inches or 20 inches in diameter. High resolution flat panel displays are also used with PCs.

[0004] Many external or peripheral devices can be used with the PCs. Among others, these peripheral devices include mass storage devices such as a Zip™ Drive product sold by Iomega Corporation of Utah. Other storage devices include external hard drives, tape drives, and others. Additional devices include communication devices such as a modem, which can be used to link the PC to a wide area network of computers such as the Internet. Furthermore, the PC can include output devices such as a printer and other output means. Moreover, the PC can include special audio output devices such as speakers the like.

[0005] PCs also have easy to use keyboards, mouse input devices, and the like. The keyboard is generally configured similar to a typewriter format. The keyboard also has the length and width for easily inputting information by way of keys to the computer. The mouse also has a sufficient size and shape to easily move a cursor on the display from one location to another location.

[0006] Other types of computing devices include portable computing devices such as “laptop” computers and the like. Although somewhat successful, laptop computers have many limitations. These computing devices have poor display technology. In fact, these devices often have a smaller flat panel display that has poor viewing characteristics. Additionally, these devices also have poor input devices such as smaller keyboards and the like. Furthermore, these devices have limited common platforms to transfer information to and from these devices and other devices such as PCs.

[0007] Up to now, there has been little common ground between these platforms including the PCs and laptops in terms of upgrading, ease-of-use, cost, performance, and the like. Many differences between these platforms, probably somewhat intentional, has benefited computer manufacturers at the cost of consumers. A drawback to having two separate computers is that the user must often purchase both the desktop and laptop to have “total” computing power, where the desktop serves as a “regular” computer and the laptop serves as a “portable” computer. Purchasing both computers is often costly and runs “thousands” of dollars. The user also wastes a significant amount of time transferring software and data between the two types of computers. For example, the user must often couple the portable computer to a local area network (i.e., LAN), to a serial

port with a modem and then manually transfer over files and data between the desktop and the portable computer. Alternatively, the user often must use floppy disks to “zip” up files and programs that exceed the storage capacity of conventional floppy disks, and transfer the floppy disk data manually.

[0008] Another drawback with the current model of separate portable and desktop computer is that the user has to spend money to buy components and peripherals that are duplicated in at least one of these computers. For example, both the desktop and portable computers typically include hard disk drives, floppy drives, CD-ROMs, computer memory, host processors, graphics accelerators, and the like. Because program software and supporting programs generally must be installed upon both hard drives in order for the user to operate programs on the road and in the office, hard disk space is often wasted.

[0009] One approach to reduce some of these drawbacks has been the use of a docking station with a portable computer. Here, the user has the portable computer for “on the road” use and a docking station that houses the portable computer for office use.

[0010] Similar to separate desktop and portable computers, there is no commonality between two desktop computers. To date, most personal computers are constructed with a single motherboard that provides connection for CPU and other components in the computer. Dual CPU systems have been available through Intel’s slot 1 architecture. For example, two Pentium II cartridges can be plugged into two “slot 1” card slots on a motherboard to form a Dual-processor system. The two CPU’s share a common host bus that connects to the rest of the system, e.g. main memory, hard disk drive, graphics subsystem, and others. Dual CPU systems have the advantage of increased CPU performance for the whole system. Adding a CPU cartridge requires no change in operating systems and application software. However, dual CPU systems may suffer limited performance improvement if memory or disk drive bandwidth becomes the limiting factor. Also, dual CPU systems have to time-share the processing unit in running multiple applications. CPU performance improvement efficiency also depends on software coding structure. Dual CPU systems provide no hardware redundancy to help fault tolerance. In running multiple applications, memory and disk drive data throughput will become the limiting factor in improving performance with multi-processor systems.

[0011] The present invention generally relates to computer interfaces. More specifically, the present invention relates to an interface channel that interfaces two computer interface buses that operate under protocols that are different from that used by the interface channel.

[0012] Interfaces coupling two independent computer buses are well known in the art. A block diagram of a computer system utilizing such a prior art interface is shown in Fig. 5. In Fig. 5, a primary peripheral component interconnect (PCI) bus 505 of a notebook PC 500 is coupled to a secondary PCI bus 555 in a docking system 550 (also referred to as docking station 550) through high pin count connectors 501 and 502, which are normally mating connectors. The high pin count connectors 501 and 502 contain a sufficiently large number of pins so as to carry PCI bus signals between the two PCI buses without any translation. The main purpose for interfacing the two independent PCI buses is to allow transactions to occur between a master on one PCI bus and a target on the other PCI bus. The interface between these two independent PCI buses additionally includes an optional PCI to PCI bridge 560, located in the docking station 550, to expand the add on capability in docking station 550. The bridge 560 creates a new bus number for devices behind the bridge 560 so that they are not on the same bus number as other devices in the system thus increasing the add on capability in the docking station 550.

[0013] An interface such as that shown in Fig. 5 provides an adequate interface between the primary and secondary PCI buses. However, the interface is limited in a number of ways. The interface transfers signals between the primary and secondary PCI buses using the protocols of a PCI bus. Consequently, the interface is subject to the limitations under which PCI buses operate. One such limitation is the fact that PCI buses are not cable friendly. The cable friendliness of the interface was not a major concern in the prior art. However, in the context of the computer system of the present invention, which is described in the present inventor's (William W.Y. Chu's) application for "Personal Computer Peripheral Console With Attached Computer Module" filed concurrently with the present application on Sep. 8, 1998 and incorporated herein by reference, a cable friendly interface is desired for interfacing an attached computer module (ACM) and a peripheral console of the present invention. Furthermore, as a result of operating by PCI protocols, the prior art interface includes a very large number of signal channels with a corresponding large number of conductive lines (and a similarly large number of pins in

the connectors of the interface) that are commensurate in number with the number of signal lines in the PCI buses which it interfaces. One disadvantage of an interface having a relatively large number of conductive lines and pins is that it costs more than one that uses a fewer number of conductive lines and pins. Additionally, an interface having a large number of conductive lines is bulkier and more cumbersome to handle. Finally, a relatively large number of signal channels in the interface renders the option of using differential voltage signals less viable because a differential voltage signal method would require duplicating a large number of signal lines. It is desirable to use a low voltage differential signal (LVDS) channel in the computer system of the present invention because an LVDS channel is more cable friendly, faster, consumes less power, and generates less noise, including electromagnetic interferences (EMI), than a PCI channel. The term LVDS is herein used to generically refer to low voltage differential signals and is not intended to be limited to any particular type of LVDS technology.

[0014] Thus, what is needed are computer systems that can have multiple computer modules. Each computer module has dedicated memory and disk drive, and can operate independently.

BRIEF SUMMARY OF THE INVENTION

[0015] According to the present invention, a technique including a method and device for multi-module computing is provided. In an exemplary embodiment, the present invention provides a system including a plurality of computer modules that can independently operate to provide backup capability, dual processing, and the like.

[0016] In a specific embodiment, the present invention provides a computer system for multi-processing purposes. The computer system has a console comprising a first coupling site and a second coupling site, e.g., computer module bay. Each coupling site comprises a connector. The console is an enclosure that is capable of housing each coupling site. The system also has a plurality of computer modules, where each of the computer modules is coupled to one of the connectors. Each of the computer modules has a processing unit, a main memory coupled to the processing unit, a graphics controller coupled to the processing unit, and a mass storage device coupled to the processing unit. Each of the computer modules is substantially similar in design to each other to provide independent processing of each of the computer modules in the computer system.

[0017] In an alternative specific embodiment, the present invention provides a multi-processing computer system. The system has a console comprising a first coupling site and a second coupling site. Each coupling site comprises a connector. The console is an enclosure that is capable of housing each coupling site. The system also has a plurality of computer modules, where each of the computer modules is coupled to one of the connectors. Each of the computer modules has a processing unit, a main memory coupled to the processing unit, a graphics controller coupled to the processing unit, a mass storage device coupled to the processing unit, and a video output coupled to the processing unit. Each of the computer modules is substantially similar in design to each other to provide independent processing of each of the computer modules in the computer system. A video switch circuit is coupled to each of the computer modules through the video output. The video switch is configured to switch a video signal from any one of the computer modules to a display.

[0018] Numerous benefits are achieved using the present invention over previously existing techniques. In one embodiment, the invention provides improved processing and maintenance features. The invention can also provide increased CPU performance for the whole system. The invention also can be implemented without changes in operating system and application software. The present invention is also implemented using conventional technologies that can be provided in the present computer system in an easy and efficient manner.

[0019] In another embodiment, the invention provides at least two users to share the same modular desktop system. Each user operates on a different computer module. The other peripheral devices, i.e. CDROM, printer, DSL connection, etc. can be shared. This provides lower system cost, less desktop space and more efficiency. Depending upon the embodiment, one or more of these benefits can be available. These and other advantages or benefits are described throughout the present specification and are described more particularly below.

[0020] In still further embodiments, the present invention provides methods of using multiple computer modules.

[0021] The present invention encompasses an apparatus for bridging a first computer interface bus and a second computer interface bus. where each of the first and second

computer interface buses have a number of parallel multiplexed address/data bus lines and operate at a clock speed in a predetermined clock speed range having a minimum clock speed and a maximum clock speed. The apparatus comprises an interface channel having a clock line and a plurality of bit lines for transmitting bits; a first interface controller coupled to the first computer interface bus and to the interface channel to encode first control signals from the first computer interface bus into first control bits to be transmitted on the interface channel and to decode second control bits received from the interface channel into second control signals to be transmitted to the first computer interface bus; and a second interface controller coupled to the interface channel and the second computer interface bus to decode the first control bits from the interface channel into third control signals to be transmitted on the second computer interface bus and to encode fourth control signals from the second computer interface bus into the second control bits to be transmitted on the interface channel.

[0022] In one embodiment, the first and second interface controllers comprise a host interface controller (HIC) and a peripheral interface controller (PIC), respectively, the first and second computer interface buses comprise a primary PCI and a secondary PCI bus, respectively, and the interface channel comprises an LVDS channel.

[0023] The present invention overcomes the aforementioned disadvantages of the prior art by interfacing two PCI or PCI-like buses using a non-PCI or non-PCI-like channel. In the present invention, PCI control signals are encoded into control bits and the control bits, rather than the control signals that they represent, are transmitted on the interface channel. At the receiving end, the control bits representing control signals are decoded back into PCI control signals prior to being transmitted to the intended PCI bus.

[0024] The fact that control bits rather than control signals are transmitted on the interface channel allows using a smaller number of signal channels and a correspondingly small number of conductive lines in the interface channel than would otherwise be possible. This is because the control bits can be more easily multiplexed at one end of the interface channel and recovered at the other end than control signals. This relatively small number of signal channels used in the interface channel allows using LVDS channels for the interface. As mentioned above, an LVDS channel is more cable friendly, faster, consumes less power, and generates less noise than a PCI bus channel, which is used in the prior art to interface two PCI buses. Therefore, the present invention advantageously

uses an LVDS channel for the hereto unused purpose of interfacing PCI or PCI-like buses. The relatively smaller number of signal channels in the interface also allows using connectors having smaller pins counts. As mentioned above an interface having a smaller number of signal channels and, therefore, a smaller number of conductive lines is less bulky and less expensive than one having a larger number of signal channels. Similarly, connectors having a smaller number of pins are also less expensive and less bulky than connectors having a larger number of pins.

[0025] In one embodiment, the present invention encompasses an apparatus for bridging a first computer interface bus and a second computer interface bus, in a microprocessor based computer system where each of the first and second computer interface buses have a number of parallel multiplexed address/data bus lines and operate at a clock speed in a predetermined clock speed range having a minimum clock speed and a maximum clock speed. The apparatus comprises an interface channel having a clock channel and a plurality of bit channels for transmitting bits; a first interface controller coupled to the first computer interface bus and to the interface channel to encode first control signals from the first computer interface bus into first control bits to be transmitted on the interface channel and to decode second control bits received from the interface channel into second control signals to be transmitted to the first computer interface bus; and a second interface controller coupled to the interface channel and the second computer interface bus to decode the first control bits from the interface channel into third control signals to be transmitted on the second computer interface bus and to encode fourth control signals from the second computer interface bus into the second control bits to be transmitted on the interface channel.

[0026] In one embodiment, the first and second interface controllers comprise a host interface controller (HIC) and a peripheral interface controller (PIC), respectively, the first and second computer interface buses comprise a primary PCI and a secondary PCI bus, respectively, and the interface channel comprises an LVDS channel.

[0027] In a preferred embodiment, the interface channel has a plurality of serial bit channels numbering fewer than the number of parallel bus lines in each of the PCI buses and operates at a clock speed higher than the clock speed at which any of the bus lines operates. More specifically, the interface channel includes two sets of unidirectional serial bit channels which transmit data in opposite directions such that one set of bit

channels transmits serial bits from the HIC to the PIC while the other set transmits serial bits from the PIC to the HIC. For each cycle of the PCI clock, each bit channel of the interface channel transmits a packet of serial bits.

[0028] The HIC and PIC each include a bus controller to interface with the first and second computer interface buses, respectively, and to manage transactions that occur therewith. The HIC and PIC also include a translator coupled to the bus controller to encode control signals from the first and second computer interface buses, respectively, into control bits and to decode control bits from the interface channel into control signals. Additionally, the HIC and PIC each include a transmitter and a receiver coupled to the translator. The transmitter converts parallel bits into serial bits and transmits the serial bits to the interface channel. The receiver receives serial bits from the interface channel and converts them into parallel bits.

[0029] According to the present invention, a technique including a method and device for securing a computer module using a password in a computer system is provided. In an exemplary embodiment, the present invention provides a security system for an attached computer module ("ACM"). In an embodiment, the ACM inserts into a Computer Module Bay (CMB) within a peripheral console to form a functional computer.

[0030] In a specific embodiment, the present invention provides a computer module. The computer module has an enclosure that is insertable into a console. The module also has a central processing unit (i.e., integrated circuit chip) in the enclosure. The module has a hard disk drive in the enclosure, where the hard disk drive is coupled to the central processing unit. The module further has a programmable memory device in the enclosure, where the programmable memory device can be configurable to store a password for preventing a possibility of unauthorized use of the hard disk drive and/or other module elements. The stored password can be any suitable key strokes that a user can change from time to time. In a further embodiment, the present invention provides a permanent password or user identification code stored in flash memory, which also can be in the processing unit, or other integrated circuit element. The permanent password or user identification code is designed to provide a permanent "finger print" on the attached computer module.

[0031] In a specific embodiment, the present invention provides a variety of methods. In one embodiment, the present invention provides a method for operating a computer system such as a modular computer system and others. The method includes inserting an attached computer module (“ACM”) into a bay of a modular computer system. The ACM has a microprocessor unit (e.g., microcontroller, microprocessor) coupled to a mass memory storage device (e.g., hard disk). The method also includes applying power to the computer system and the ACM to execute a security program, which is stored in the mass memory storage device. The method also includes prompting for a user password from a user on a display (e.g., fiat panel, CRT). In a further embodiment, the present method includes a step of reading a permanent password or user identification code stored in flash memory, or other integrated circuit element. The permanent password or user identification code provides a permanent finger print on the attached computer module. The present invention includes a variety of these methods that can be implemented in computer codes, for example, as well as hardware.

[0032] Numerous benefits are achieved using the present invention over previously existing techniques. The present invention provides mechanical and electrical security systems to prevent theft or unauthorized use of the computer system in a specific embodiment. Additionally, the present invention substantially prevents accidental removal of the ACM from the console. In some embodiments, the present invention prevents illegal or unauthorized use during transit. The present invention is also implemented using conventional technologies that can be provided in the present computer system in an easy and efficient manner. Depending upon the embodiment, one or more of these benefits can be available. These and other advantages or benefits are described throughout the present specification and are described more particularly below.

[0033] These and other embodiments of the present invention, as well as its advantages and features, are described in more detail in conjunction with the text below and attached Figs.

BRIEF DESCRIPTION OF THE DRAWINGS

[0034] Fig. 1 is a simplified diagram of a computer system according to an embodiment of the present invention;

[0035] Fig. 2 is a simplified block diagram of a computer system according to an alternative embodiment of the present invention;

[0036] Fig. 3 is a simplified block diagram of a computer system according to a further alternative embodiment of the present invention, and

[0037] Fig. 4 is a simplified flow diagram of a method according to an embodiment of the present invention.

[0038] Fig. 5 is a block diagram of a computer system using a prior art interface between a primary and a secondary PCI bus.

[0039] Fig. 6 is a block diagram of one embodiment of a computer system using the interface of the present invention.

[0040] Fig. 7 is a partial block diagram of a computer system using the interface of the present invention as a bridge between the north and south bridges of the computer system.

[0041] Fig. 8 is a partial block diagram of a computer system in which the north and south bridges are integrated with the host and peripheral interface controllers, respectively.

[0042] Fig. 9 is a block diagram of one embodiment of the host interface controller and the peripheral interface controller of the present invention.

[0043] Fig. 10 is a detailed block diagram of one embodiment of the host interface controller of the present invention.

[0044] Fig. 11 is a detailed block diagram of one embodiment of the PIC of the present invention.

[0045] Fig. 12 is a table showing the symbols, signals, data rate and description of signals in a first embodiment of the XPBus.

[0046] Fig. 13 is a table showing the information transmitted on the XPBus during two clock cycles of the XPBus in one embodiment of the present invention where 10 data bits transmitted in each clock cycle of the XPBus.

[0047] Fig. 14 is a table showing information transmitted on the XPBus during four clock cycles of the XPBus in another embodiment of the present invention where 10 data bits are transmitted in each clock cycle of the XPBus.

[0048] Fig. 15 is a schematic diagram of the signal lines PCK, PD0 to PD3, and PCN.

[0049] Fig. 16 is a table showing the names, types, number of pins dedicated to, and the description of the primary bus PCI signals.

[0050] FIG. 17 is a block diagram of one embodiment of a computer system employing the present invention.

[0051] FIG. 18 is a block diagram of an attached computing module (ACM).

[0052] FIG. 19 illustrates an external view of one embodiment of an ACM.

[0053] FIG. 19b illustrates one possible embodiment of a computer bay.

[0054] FIG. 20 illustrates the internal component layout for one embodiment of an ACM.

[0055] FIG. 21 is a block diagram of a peripheral console (PCON).

[0056] FIG. 22 is a simplified layout diagram of a security system for a computer system according to an embodiment of the present invention; and

[0057] FIG. 23 is a simplified block diagram of a security system for a computer module according to an embodiment of the present invention.

DETAILED DESCRIPTION OF THE INVENTION

[0058] According to the present invention, a technique including a method and device for multi-module computing is provided. In an exemplary embodiment, the present invention provides a system including a plurality of computer modules that can independently operate to provide backup capability, dual processing, and the like.

[0059] Fig. 1 is a simplified diagram of a computer system 100 according to an embodiment of the present invention. This diagram is merely an illustration and should not limit the scope of the claims herein. One of ordinary skill in the art would recognize other variations, modifications, and alternatives. The computer system 100 includes an

attached computer module (i.e., ACM) 113, a desktop console 101, among other elements. The computer system also has another ACM module 117. Each ACM module has a respective slot 121, 119, which mechanically houses and electrically couples each ACM to the computer console. Also shown is a display 111, which connects to the console. Additionally, keyboard 109 and mouse 115 are also shown. A second display 102, keyboard 105, and mouse 107 can be coupled to the console in some optional embodiments to allow more than one user to operate the computer system. The computer system is modular and has a variety of components that are removable. Some of these components (or modules) can be used in different computers, workstations, computerized television sets, and portable or laptop units.

[0060] In the present embodiment, each ACM 113 includes computer components, as will be described below, including a central processing unit (“CPU”), IDE controller, hard disk drive, computer memory, and the like. The computer module bay (i.e., CMB) 121 is an opening or slot in the desktop console. The CMB houses the ACM and provides communication to and from the ACM. The CMB also provides mechanical protection and support to the ACM. The CMB has a mechanical alignment mechanism for mating a portion of the ACM to the console. The CMB further has thermal heat dissipation sinks, electrical connection mechanisms, and the like. Some details of the ACM can be found in co-pending Patent Application Nos. 09/149,882 and 09/149,548 filed 9/8/98, commonly assigned, and hereby incorporated by reference for all purposes.

[0061] In a specific embodiment, the present multiple computer module system has a peripheral console that has two or more computer bays that can receive a removable computer module or ACM. Multiple computer module system can function as a personal computer with only one ACM and the peripheral console. The second and additional ACM can be added later to increase overall system performance and reliability. The ACM operates independently as self-contained computer, communicates with each other through a high-speed serial communication and share most peripheral devices within the peripheral console. Each ACM controls its independent graphics subsystem and drives separate video output signals. A practical implementation is a dual ACM system. In a dual ACM system, two monitors can be used to display the two ACMs’ graphics outputs at the same time. For a single monitor, a RGB switch is used to switch between the video outputs of the two ACMs and can be controlled by a command from the user. Similarly,

input devices (i.e. keyboard and mouse) are switched between the two computer systems with a command from the user. Command from the user can be in the form of either a dedicated key on the keyboard or a special icon on the screen that the mouse can click on.

[0062] In most embodiments, the ACM includes an enclosure such as the one described with the following components, which should not be limiting:

- 1) A CPU with cache memory;
- 2) Core logic device or means;
- 3) Main memory;
- 4) A single primary Hard Disk Drive (“HDD”) that has a security program;
- 5) Flash memory with system BIOS and programmable user password;
- 6) Operating System, application software, data files on primary HDD;
- 7) An interface device and connectors to peripheral console;
- 8) A software controllable mechanical lock, lock control means, and other accessories.

[0063] The ACM connects to a peripheral console with power supply, a display device, an input device, and other elements. Some details of these elements with the present system are described in more detail below. In a dual ACM system, the primary ACM can connect directly to the peripheral board in the peripheral console. The second ACM can connect either directly or indirectly to the peripheral board. For indirect connection, a receptacle board is added to allow a cable connection to the peripheral board. This is to facilitate the mechanical positioning of the second ACM inside the computer chassis. The receptacle board approach can even be used for the primary ACM if a high bandwidth peripheral bus, e.g. PCI Bus, is not connected from the primary ACM to the peripheral board.

[0064] The shared peripheral console has a chassis and a motherboard that connects the following devices:

- 1) Input means, e.g. keyboard and mouse,
- 2) Display means, e.g. RGB monitor,
- 3) Add-on means, e.g. PCI add-on slots,
- 4) Two Computer Module Bays (CMB) with connectors to two ACMs,

- 5) A serial communication Hub controller that interfaces to serial communication controller of both ACMs,
- 6) Shared storage subsystem, e.g. Floppy drive, CDROM drive, DVD drive, or 2nd Hard Drive,
- 7) Communication device, e.g. modem,
- 8) Power supply, and others.

[0065] The computer bay is an opening in the peripheral console that receives an ACM. CMB provides mechanical protection to ACM, mechanical alignment for connector mating, mechanical locking system to prevent theft and accidental removal, and connectors at the end of the opening for connecting to ACM. The interface bus between ACM and the peripheral console has a video bus, peripheral connections, serial communication connection, control signals and power connection. Video bus includes video output of graphics devices, i.e. analog RGB and control signals for monitor. Power connection supplies the power for ACM.

[0066] An implementation of peripheral sharing is the use of Ethernet controllers to bridge the communication between the two ACMs. Some of the peripheral devices residing in the peripheral console are shown in the simplified diagram of Fig. 2. As shown, the diagram is merely an illustration which should not limit the scope of the claims herein. One of ordinary skill in the art would recognize many other variations, alternatives, and modifications. As shown, a primary ACM 203 is connected to PCI peripheral devices in the peripheral console through the PCI bus 225 that passes through the connection between primary ACM 203 and peripheral console 201. As shown, ACM has a CPU module 207 coupled to the PCI bus through a North Bridge 211.

[0067] The CPU module can use a suitable microprocessing unit, microcontroller, digital signal processor, and the like. In a specific embodiment, the CPU module uses, for example, a 400 MHz Pentium II microprocessor module from Intel Corporation and like microprocessors from AMD Corporation, Cyrix Corporation (now National Semiconductor Corporation), and others. In other aspects, the microprocessor can be one such as the Compaq Computer Corporation Alpha Chip, Apple Computer Corporation PowerPC G3 processor, and the like. Further, higher speed processors are contemplated in other embodiments as technology increases in the future.

[0068] In the CPU module, peripheral controller 213 is coupled to BIOS/flash memory 217. Additionally, the peripheral controller is coupled to a clock control logic, a configuration signal, and a peripheral bus. The ACM has the hard drive module 215. Among other elements, the ACM includes north bridge 215, graphics subsystem 223 (e.g., graphics accelerator, graphics memory), an IDE controller, and other components. Adjacent to and in parallel alignment with the hard drive module 215 is the PCI bus. In a specific embodiment, North Bridge unit 211 often couples to a computer memory 209, to the graphics subsystem, and to the peripheral controller via the PCI bus. Graphics subsystem typically couples to a graphics memory, and other elements. IDE controller generally supports and provides timing signals necessary for the IDE bus. In the present embodiment, the IDE controller is embodied as part of a P114XE controller from Intel, for example. Other types of buses than IDE are contemplated, for example EIDE, SCSI, 1394, and the like in alternative embodiments of the present invention.

[0069] The hard drive module or mass storage unit 215 typically includes a computer operating system, application software program files, data files, and the like. In a specific embodiment, the computer operating system may be the Windows98 operating system from Microsoft Corporation of Redmond Washington. Other operating systems, such as WindowsNT, MacOS8, Unix, and the like are also contemplated in alternative embodiments of the present invention. Further, some typical application software programs can include Office98 by Microsoft Corporation, Corel Perfect Suite by Corel, and others. Hard disk module 215 includes a hard disk drive. The hard disk drive, however, can also be replaced by removable hard disk drives, read/write CD ROMs, flash memory, floppy disk drives, and the like. A small form factor, for example 2.5", is currently contemplated, however, other form factors, such as PC card, and the like are also contemplated. Mass storage unit 240 may also support other interfaces than IDE.

[0070] Among other features, the computer system includes an ACM with security protection.

[0071] The ACM also has a network controller, which can be an Ethernet controller 219, which is coupled to the North Bridge through the PCI bus. The North Bridge is coupled to the CPU. The Ethernet controller can be a 10/100 Base, such as Intel's 82559 or the like. Other types of network connection devices can also be used. For example, the

invention can use Gbit Ethernet 1394, and USB 2.0. The network controller couples to a hub 233 in the console, which includes shared peripheral system 201.

[0072] Also shown is the second ACM 205. The second ACM has the same or similar components as the first ACM. Here, like reference numerals have been used for easy cross-referencing, but is not intended to be limiting. In some embodiments, the secondary ACM is not connected to the PCI bus in the peripheral console directly. The secondary ACM 219 accesses peripheral devices controlled by the primary ACM through the Ethernet connection to the primary ACM, e.g. CD-ROM, or PCI modem. The implementation is not restricted to Ethernet serial communication and can use other high-speed serial communication such as USB 2.0, and 1394. The Ethernet hub is coupled to an external output port 235, which connects to an external network.

[0073] The primary hard disk drive in each ACM can be accessed by the other ACM as sharable hard drive through the Ethernet connection. This allows the easy sharing of files between the two independent computer modules. The Ethernet Hub Controller provides the high-speed communication function between the two computer modules. Ethernet data bandwidth of 100 Mbit/sec allows fast data communication between the two computer modules. The secondary ACM access peripheral devices of the primary ACM through the network connection provided by Ethernet link. The operating system, e.g. Windows98, provides the sharing of resources between the two ACMs. In some embodiments, critical data in one ACM can be backup into the other ACM.

[0074] The Ethernet hub also couples to PCI bus 239, which connects to PCI devices 241, 243, e.g., modem, SCSI controller. A flash memory 242 can also be coupled to the PCI bus. The flash memory can store passwords and security information, such as those implementations described in U.S. Serial No. 09/183,493, which is commonly owned, and hereby incorporated by reference. The hub 233 also couples to an I/O control 237, which connects to keyboard/mouse switch 245, which couples to keyboard/mouse 247. Optionally, the keyboard/mouse switch also couples to a second keyboard/house 259 via PS2 or USB signal line 251. The keyboard/mouse switch has at least a first state and a second state, which allow operation of respectively multiple keyboards or a single keyboard. The switch also couples to each I/O controller 221 in each ACM via lines 253, 255. The I/O control 237 also couples to an RGB switch 257, which allows video signals to pass to the first monitor 259. Alternatively, the RGB switch couples to a second

monitor 261. The RGB switch includes analog video switches such as MAXIM's MAX4545.

[0075] The peripheral system 201 also has an independent power supply 231 for each ACM. Each power supply provides power to each ACM. As merely an example, the power supply is a MICRO ATX 150W made by ENLIGHT, but can be others. The power supply is connected or coupled to each ACM through a separate line, for example. The independent power supply allows for independent operation of each ACM in some embodiments.

[0076] The above embodiments are described generally in terms of hardware and software. It will be recognized, however, that the functionality of the hardware can be further combined or even separated. The functionality of the software can also be further combined or even separated. Hardware can be replaced, at times, with software. Software can be replaced, at times, with hardware. Accordingly, the present embodiments should not be construed as limiting the scope of the claims here. One of ordinary skill in the art would recognize other variations, modifications, and alternatives.

[0077] Fig. 3 is a simplified block diagram 300 of a computer system according to an alternative embodiment of the present invention. This diagram is merely an example which should not limit the scope of the claims herein. One of ordinary skill in the art would recognize many other variations, modifications, and alternatives. Like reference numerals are used in this Fig. as the previous Figs. for easy referencing, but are not intended to be limiting. As shown, each ACM includes common elements as the previous Fig. A primary ACM 203 is connected to PCI peripheral devices in the peripheral console through the PCI bus 225 that passes through the connection between primary ACM 203 and peripheral console 201. As shown, ACM has a CPU module 207 coupled to the PCI bus through a North Bridge 211.

[0078] The CPU module can use a suitable microprocessing unit, microcontroller, digital signal processor, and the like. In a specific embodiment, the CPU module uses, for example, a 400 MHz Pentium II microprocessor module from Intel Corporation and like microprocessors from AMD Corporation, Cyrix Corporation (now National Semiconductor Corporation), and others. In other aspects, the microprocessor can be one such as the Compaq Computer Corporation Alpha Chip, Apple Computer Corporation

PowerPC G3 processor, and the like. Further, higher speed processors are contemplated in other embodiments as technology increases in the future.

[0079] In the CPU module, peripheral controller 213 is coupled to BIOS/flash memory 217. Additionally, the peripheral controller is coupled to a clock control logic, a configuration signal, and a peripheral bus. The ACM has the hard drive module 215. Among other elements, the ACM includes north bridge 215, graphics subsystem 223 (e.g., graphics accelerator, graphics memory), an IDE controller, and other components. Adjacent to and in parallel alignment with the hard drive module 215 is the PCI bus. In a specific embodiment, North Bridge unit 211 often couples to a computer memory 209, to the graphics subsystem, and to the peripheral controller via the PCI bus. Graphics subsystem typically couples to a graphics memory, and other elements. IDE controller generally supports and provides timing signals necessary for the IDE bus. In the present embodiment, the IDE controller is embodied as part of a P114XE controller from Intel, for example. Other types of buses than IDE are contemplated, for example EIDE, SCSI, 1394, and the like in alternative embodiments of the present invention.

[0080] The hard drive module or mass storage unit 215 typically includes a computer operating system, application software program files, data files, and the like. In a specific embodiment, the computer operating system may be the Windows98 operating system from Microsoft Corporation of Redmond Washington. Other operating systems, such as WindowsNT, MacOS8, Unix, and the like are also contemplated in alternative embodiments of the present invention. Further, some typical application software programs can include Office98 by Microsoft Corporation, Corel Perfect Suite by Corel, and others. Hard disk module 215 includes a hard disk drive. The hard disk drive, however, can also be replaced by removable hard disk drives, read/write CD ROMs, flash memory, floppy disk drives, and the like. A small form factor, for example 2.5", is currently contemplated, however, other form factors, such as PC card, and the like are also contemplated. Mass storage unit 240 may also support other interfaces than IDE.

[0081] Among other features, the computer system includes an ACM with security protection.

[0082] The ACM also has a network controller, which can be coupled to a serial port 302, which is coupled to the PCI bus in the ACM. The serial port is coupled to the

peripheral console through a serial controller 301 in the serial console. The serial controller is connected to PCI bus 239. The serial controller is also coupled to a serial hub controller 303, which is coupled to the PCI bus and a second ACM. In a specific embodiment, a receptacle board 310 is added to connect to the second ACM. The purpose of the receptacle board is to allow a cable connection 307 to the peripheral board 300. The cable connection is possible because the signals needed to connect to the peripheral board can be limited to video, I/O, serial communication, and power. The serial communication controller can be placed on the receptacle board and not in the ACM. As shown, the serial bus controller couples to the PCI bus. The receptacle board also couples to power, graphics subsystem, I/O controller, and other elements, which may be on a common bus. The overall operation of the present configuration is similar to the previous one except it operates in serial communication mode.

[0083] The Dual ACM system can support different usage models:

[0084] 1. One user using both ACMs concurrently with 1 or 2 monitors, and a common keyboard/mouse.

[0085] 2. Two users using the two separate ACMs at the same time with separate monitors and keyboard/mouse. The 2 users share peripherals, e.g., printer, CDROM, and others. The two users share external networking.

[0086] To support 1 monitor for both ACMs, a video switch in the peripheral console is used to switch between the video outputs of the two ACMs. The system can be set to support either 1 monitor or 2-monitor mode. The user presses a special key on the keyboard or a special icon on the screen to switch the screen display from one ACM to the other. This same action causes the keyboard and mouse connections to switch from one ACM to the other ACM.

[0087] A dual ACM system can save space, wiring, and cost for a 2-person PC setup, with the added benefit that both PC systems can be accessed from one user site for increased system performance if the other user is not using the system. Files can be copied between the primary drive of both system and provides protection against a single ACM failure. Software needs to be developed to manage the concurrent use of two PC subsystems, the automatic sharing of selected files between the two systems, and fault tolerance.

[0088] The design with more than two computer modules can be implemented with the use of multi-port, serial communication hub controller and multi-port I/O switches. In one embodiment, a peripheral console has four computer bays for four separate computer modules. The computer modules communicate through a four port Ethernet hub. The video, keyboard, and mouse switch will cycle through the connection from each computer module to the external monitor, keyboard, and mouse with a push button sequentially. This embodiment is useful for a server that performs different functions concurrently, e.g. email, application hosting, web hosting, firewall, etc.

[0089] The above embodiments are described generally in terms of hardware and software. It will be recognized, however, that the functionality of the hardware can be further combined or even separated. The functionality of the software can also be further combined or even separated. Hardware can be replaced, at times, with software. Software can be replaced, at times, with hardware. Accordingly, the present embodiments should not be construed as limiting the scope of the claims here. One of ordinary skill in the art would recognize other variations, modifications, and alternatives.

[0090] Fig. 4 is a simplified diagram of a method according to an embodiment of the present invention. This diagram is merely an example which should not limit the scope of the claims herein. One of ordinary skill in the art would recognize many other variations, modifications, and alternatives. The present diagram illustrates an automatic file backup procedure from one computer module to the other. As shown, a user selects (step 401) a certain file in one of the computer module for automatic backup. Next, the method determines if another module is available, step 403. If so, the method in the originating module requests the other computer module to create (step 405) backup file. Alternatively, the method alerts the user of the missing or malfunctioning module, step 429. The method then has the user try later 431, once the missing or malfunctioning module has been replaced or repaired. Next, the method determines if there is sufficient storage available in the other computer module for the backup files. If so, the method goes to the next step. (Alternatively, the method prompts (step 433) a message to the user indicating that the storage is full.) In the next step, the method stores the backup file in memory of the other module. After the backup file has been successfully created (step 409), the software in the originating ACM sets a timer to check (step 411) for file modification via branches 423, 427 through continue, step 425 process. If a file selected

for backup has been modified (step 415), then the file is automatically back up to the other ACM again, step 417. Alternatively, the method returns to step 411 through branch 421.

[0091] The above embodiments are described generally in terms of hardware and software. It will be recognized, however, that the functionality of the hardware can be further combined or even separated. The functionality of the software can also be further combined or even separated. Hardware can be replaced, at times, with software. Software can be replaced, at times, with hardware. Accordingly, the present embodiments should not be construed as limiting the scope of the claims here. One of ordinary skill in the art would recognize other variations, modifications, and alternatives.

[0092] Fig. 6 is a block diagram of one embodiment of a computer system 600 using the interface of the present invention. Computer system 600 includes an attached computer module (ACM) 605 and a peripheral console 610, which are described in greater detail in the application of William W. Y. Chu for "Personal Computer Peripheral Console With Attached Computer Module" filed concurrently with the present application on Sep. 8, 1998 and incorporated herein by reference. The ACM 605 and the peripheral console 610 are interfaced through an exchange interface system (XIS) bus 615. The XIS bus 615 includes power bus 616, video bus 617 and peripheral bus (XPBus) 618, which is also herein referred to as an interface channel. The power bus 616 transmits power between ACM 605 and peripheral console 610. In a preferred embodiment power bus 616 transmits power at voltage levels of 3.3 volts, 5 volts and 12 volts. Video bus 617 transmits video signals between the ACM 605 and the peripheral console 610. In a preferred embodiment, the video bus 617 transmits analog Red Green Blue (RGB) video signals for color monitors, digital video signals (such as Video Electronics Standards Association (VESA) Plug and Display's Transition Minimized Differential Signaling (TMDS) signals for flat panel displays), and television (TV) and/or super video (S-video) signals. The XPBus 618 is coupled to host interface controller (HIC) 619 and to peripheral interface controller (PIC) 620, which is also sometimes referred to as a bay interface controller.

[0093] In the embodiment shown in Fig. 6, HIC 619 is coupled to an integrated unit 621 that includes a CPU, a cache and a north bridge. In another embodiment, such as that shown in Fig. 7, the CPU 705 and north bridge 710 are separate rather than integrated units. In yet another embodiment, such as that shown in Fig. 8, the HIC and PIC are

integrated with the north and south bridges, respectively, such that integrated HIC and north bridge unit 805 includes an HIC and a north bridge, while integrated PIC and south bridge unit 810 includes a PIC and a south bridge.

[0094] Fig. 9 is a more detailed block diagram of one embodiment of an HIC 905 and a PIC 955 of the present invention. HIC 905 includes a peripheral component interconnect (PCI) bus controller 910, an XDBus controller 915, a phase lock loop (PLL) clock 920 and an input/output (IO) control 925. Similarly, PIC 955 includes a PCI bus controller 960, an XDBus controller 965, a PLL clock 970 and an IO control 975. PCI bus controllers 910 and 960 are coupled to the primary and secondary PCI buses 930 and 980, respectively, and manage PCI transactions on the primary and secondary PCI buses 930 and 980, respectively. Similarly, XDBus Controllers 915 and 965 are coupled to XDBus 990. XDBus controller 915 drives the PCK line 991 and PD[0:3] and PCN lines 992 while XDBus controller 965 drives the PCKR lines 993, the PDR[0:3] and PCNR lines 994 and the RESET# line 995.

[0095] PCI bus controller 910 receives PCI clock signals from the primary PCI bus 930 and is synchronized to the PCI clock. However, as indicated in Fig. 9, the XDBus controller 915 is asynchronous with the PCI bus controller 910. Instead, the XDBus controller receives a clock signal from the PLL clock 920 and is synchronized therewith. PLL clock 920 generates a clock signal independent of the PCI clock. The asynchronous operation of the PCI bus and the XDBus allows the PCI Bus to change in frequency. for example as in a power down situation, without directly affecting the XDBus clocking. In the embodiment shown in Fig. 9, the PLL clock 920 generates a clock signal having a frequency of 66 MHz, which is twice as large as the 33 MHz frequency of the PCI clock. (The clock signal generated by the PLL clock may have a clock speed different from, including lower than, 66 MHz. For example, in another embodiment, which is discussed in greater detail below, the PLL clock 920 generates a clock signal having a frequency of 132 MHz.)

[0096] The XDBus 990 operates at the clock speed generated by the PLL clock 920. Therefore, PCK, the clock signal from the XDBus controller 915 to XDBus controller 965 has the same frequency as the clock signal generated by PLL clock 920. XDBus controller 965 receives the PCK signal after it has been buffered and operates at the clock speed of PCK. The buffered version of the clock signal PCK is used to generate the clock

signal PCKR, the clock signal from the XDBus controller 965 to XDBus controller 915. Accordingly, PCKR also has the same frequency as that generated by the PLL clock 920. The synchronous operation of PCK and PCKR provides for improved reliability in the system. In another embodiment, PCKR may be generated independently of PCK and may have a frequency different from that of PCK. It is to be noted that even when PCKR is generated from PCK, the slew between PCK and PCKR cannot be guaranteed because of the unknown cable length used for the XDBus. For a cable that is several feet long, the cable propagation delay alone can be several nano seconds.

[0097] As indicated in Fig. 9, PLL clock 970 is asynchronous with the XDBus controller 965. Instead, PLL clock 970 independently generates a clock signal that is used as a PCI clock signal on the secondary PCI bus 980. The secondary PCI bus 980 operates at the same clock speed as the primary PCI bus 930, namely at a frequency of 33 MHz.

[0098] Fig. 10 is a detailed block diagram of one embodiment of the HIC of the present invention. As shown in Fig. 10, HIC 1000 comprises bus controller 1010, translator 1020, transmitter 1030, receiver 1040, a PLL 1050, an address/data multiplexer (A/D MUX) 1060, a read/write controller (RD/WR Cntl) 1070, a video serial to parallel converter 1080 and a CPU control & general purpose input/output latch/driver (CPU CNTL & GPIO latch/driver) 1090.

[0099] HIC 1000 is coupled to an optional flash memory BIOS configuration unit 1001. Flash memory unit 1001 stores basic input output system (BIOS) and PCI configuration information and supplies the BIOS and PCI configuration information to A/D MUX 1060 and RD/WR Control 1070, which control the programming, read, and write of flash memory unit 1001.

[0100] Bus controller 1010 is coupled to the host PCI bus, which is also referred to herein as the primary PCI bus, and manages PCI bus transactions on the host PCI bus. Bus controller 1010 includes a slave (target) unit 1011 and a master unit 1016. Both slave unit 1011 and master unit 1016 each include two first in first out (FIFO) buffers, which are preferably asynchronous with respect to each other since the input and output of the two FIFOs in the master unit 1016 as well as the two FIFOs in the slave unit 1011 are clocked by different clocks, namely the PCI clock and the PCK. Additionally, slave unit 1011 includes encoder 1022 and decoder 1023, while master unit 1016 includes encoder

1027 and decoder 1028. The FIFOs 1012, 1013, 1017 and 1018 manage data transfers between the host PCI bus and the XPBus, which in the embodiment shown in Fig. 10 operate at 33 MHz and 106 MHz, respectively. PCI address/data (AD) from the host PCI bus is entered into FIFOs 1012 and 1017 before they are encoded by encoders 1022 and 1023. Encoders 1022 and 1023 format the PCI address/data bits to a form more suitable for parallel to serial conversion prior to transmittal on the XPBus. Similarly, address and data information from the receivers is decoded by decoders 1023 and 1028 to a form more suitable for transmission on the host PCI bus. Thereafter the decoded data and address information is passed through FIFOs 1013 and 1018 prior to being transferred to the host PCI bus. FIFOs 1012, 1013, 1017 and 1018, allow bus controller 1010 to handle posted and delayed PCI transactions and to provide deep buffering to store PCI transactions.

[0101] Bus controller 1010 also comprises slave read/write control (RD/WR Cntl) 1014 and master read/write control (RD/WR Cntl) 1015. RD/WR controls 1014 and 1015 are involved in the transfer of PCI control signals between bus controller 1010 and the host PCI bus.

[0102] Bus controller 1010 is coupled to translator 1020. Translator 1020 comprises encoders 1022 and 1027, decoders 1023 and 1028, control decoder & separate data path unit 1024 and control encoder & merge data path unit 1025. As discussed above encoders 1022 and 1027 are part of slave data unit 1011 and master data unit 1016, respectively, receive PCI address and data information from FIFOs 1012 and 1017, respectively, and encode the PCI address and data information into a form more suitable for parallel to serial conversion prior to transmittal on the XPBus. Similarly, decoders 1023 and 1028 are part of slave data unit 1011 and master data unit 1016, respectively, and format address and data information from receiver 1040 into a form more suitable for transmission on the host PCI bus. Control encoder & merge data path unit 1025 receives PCI control signals from the slave RD/WR control 1014 and master RD/WR control 1015. Additionally, control encoder & merge data path unit 1025 receives control signals from CPU CNTL & GPIO latch/driver 1090, which is coupled to the CPU and north bridge (not shown in Fig. 10). Control encoder & merge data path unit 1025 encodes PCI control signals as well as CPU control signals and north bridge signals into control bits, merges these encoded control bits and transmits the merged control bits to transmitter 1030, which then transmits the control bits on the data lines PD0 to PD3 and control line PCN

of the XPBus. Examples of control signals include PCI control signals and CPU control signals. A specific example of a control signal is FRAME# used in PCI buses. A control bit, on the other hand is a data bit that represents a control signal. Control decoder & separate data path unit 1024 receives control bits from receiver 1040 which receives control bits on data lines PDR0 to PDR3 and control line PCNR of the XPBus. Control decoder & separate data path unit 1024 separates the control bits it receives from receiver 1040 into PCI control signals, CPU control signals and north bridge signals, and decodes the control bits into PCI control signals, CPU control signals, and north bridge signals all of which meet the relevant timing constraints.

[0103] Transmitter 1030 receives multiplexed parallel address/data (AID) bits and control bits from translator 1020 on the AD[31::0] out and the CNTL out lines, respectively. Transmitter 1030 also receives a clock signal from PLL 1050. PLL 1050 takes a reference input clock and generates PCK that drives the XPBus. PCK is asynchronous with the PCI clock signal and operates at 106 MHz, twice the speed of the PCI clock of 33 MHz. The higher speed is intended to accommodate at least some possible increases in the operating speed of future PCI buses. As a result of the higher speed, the XPBus may be used to interface two PCI or PCI-like buses operating at 106 MHz rather than 33 MHz or having 104 rather than 32 multiplexed address/data lines.

[0104] The multiplexed parallel A/D bits and some control bits input to transmitter 1030 are serialized by parallel to serial converters 1032 of transmitter 1030 into 10 bit packets. These bit packets are then output on data lines PD0 to PD3 of the XPBus. Other control bits are serialized by parallel to serial converter 1033 into 10 bit packets and send out on control line PCN of the XPBus.

[0105] A 10x multiplier 1031 receives PCK, multiplies it by a factor of 10 and feeds a clock signal 10 times greater than PCK into the parallel to serial converters 1032 and 1033. The parallel to serial converters 1032 and 1033 perform bit shifting at 10 times the PCK rate to serialize the parallel bits into 10 bit packets. As the parallel to serial converters 1032 and 1033 shift bits at 10 times the PCK rate, the bit rate for the serial bits output by the parallel to serial converters is 10 times higher than PCK rate, i.e., 1060 MHz. However, the rate at which data packets are transmitted on the XPBus is the same as the PCK rate, i.e., 106 MHz. As the PCI buses operate at a clock and bit rate of 33

MHz, the XPBus has a clock rate that is twice as large and a bit rate per bit line (channel) that is 100 times as large as that of the PCI buses which it interfaces.

[0106] Receiver 1040 receives serial bit packets on data lines PDR0 to PDR3 and control line PCNR. Receiver 1040 also receives PCKR on the XPBus as well as the clock signal PCK from PLL 1050. The synchronizer (SYNC) 1044 of receiver 1040 synchronizes the clock signal PCKR to the locally generated clock signal, PCK, in order to capture the bits received from the XPBus into PCK clock timing.

[0107] Serial to parallel converters 1042 convert the serial bit packets received on lines PDR0 to PDR3 into parallel address/data and control bits that are sent to decoders 1023 and 1028 and control decoder and separate data path unit 1024, respectively. Serial to parallel converter 1043 receives control bit packets from control line PCNR, converts them to parallel control bits and sends the parallel control bits to control decoder & separate data path 1024.

[0108] A 10x multiplier 1041 receives PCKR, multiplies it by a factor of 10 and feeds a clock signal 10 times greater than PCKR into the serial to parallel converters 1042 and 1043. Because the bits on PDR0 to PDR3 and PCNR are transmitted at a bit rate of 10 times the PCKR rate, the serial to parallel converters 1042 and 1043 perform bit shifting at 10 times the PCKR rate to convert the 10 bit packets into parallel bits. It is to be noted that the rate at which bit packets are transmitted on the XPBus is the same as the PCKR rate, i.e., 106 MHz. The parallel data and control bits are thereafter sent to decoders 1023 and 1028 by way of the AD[3:0] in line and to control decoder & separate data path unit 1024 by way of CNTL in lines, respectively.

[0109] Reset control unit 1045 of HIC 1000 receives the signal RESET#, which is an independent system reset signal, on the reset line RESET#. Reset control unit 1045 then transmits the reset signal to the CPU CNTL & GPIO latch/driver unit 1090.

[0110] As may be noted from the above, the 32 line host and secondary PCI buses are interfaced by 10 XPBus lines (PD0, PD1, PD2, PD3, PCN, PDR0, PDR1, PDR2, PDR3, PCNR). Therefore, the interface channel, XPBus, of the present invention uses fewer lines than are contained in either of the buses which it interfaces, namely the PCI buses. XPBus is able to interface such PCI buses without backup delays because the XPBus

operates at a clock rate and a per line (channel) bit rate that are higher than those of the PCI buses.

[0111] In addition to receiving a reset signal, the CPU CNTL & GPIO latch/driver 1090 is responsible for latching input signals from the CPU and north bridge and sending the signals to the translator. It also takes decoded signals from the control decoder & separate data path unit 1024 and drives the appropriate signals for the CPU and north bridge.

[0112] In the embodiment shown in Fig. 10, video serial to parallel converter 1080 is included in HIC 1000. In another embodiment, video serial to parallel converter 1080 may be a separate unit from the HIC 1000. Video serial to parallel converter 1080 receives serial video data on line VPD and a video clock signal VPCK from line VPCK of video bus 1081. It then converts the serial video data into 16 bit parallel video port data and the appropriate video port control signals, which it transmits to the graphics controller (not shown in Fig. 10) on the video port data [0::15] and video port control lines, respectively.

[0113] HIC 1000 handles the PCI bus control signals and control bits from the XPBus representing PCI control signals in the following ways:

1. HIC 1000 buffers clocked control signals from the host PCI bus, encodes them into control bits and sends the encoded control bits to the XPBus;
2. HIC 1000 manages the signal locally; and
3. HIC 1000 receives control bits from XPBus, translates the control bits into PCI control signals and sends the PCI control signals to the host PCI bus.

[0114] Fig. 11 is a detailed block diagram of one embodiment of the PIC of the present invention. PIC 1100 is nearly identical to HIC 1000 in its function, except that HIC 1000 interfaces the host PCI bus to the XPBus while PIC 1100 interfaces the secondary PCI bus to the XPBus. Similarly, the components in PIC 1100 serve the same function as their corresponding components in HIC 1000. Reference numbers for components in PIC 1100 have been selected such that a component in PIC 1100 and its corresponding component in HIC 1000 have reference numbers that differ by 500 and have the same two least significant digits. Thus for example, the bus controller in PIC 1100 is referenced as bus controller 1110 while the bus controller in HIC 1000 is referenced as bus controller 1010. As many of the elements in PIC 1100 serve the same functions as those served by their

corresponding elements in HIC 1000 and as the functions of the corresponding elements in HIC 1000 have been described in detail above, the function of elements of PIC 1100 having corresponding elements in HIC 1000 will not be further described herein. Reference may be made to the above description of Fig. 10 for an understanding of the functions of the elements of PIC 1100 having corresponding elements in HIC 1000.

[0115] As suggested above, there are also differences between HIC 1000 and PIC 1100. Some of the differences between HIC 1000 and PIC 1100 include the following. First, receiver 1140 in PIC 1100, unlike receiver 1040 in HIC 1000, does not contain a synchronization unit. As mentioned above, the synchronization unit in HIC 1000 synchronizes the PCKR clock to the PCK clock locally generated by PLL 1050. PIC 1100 does not locally generate a PCK clock and therefore, it does not have a locally generated PCK clock with which to synchronize the PCK clock signal that it receives from HIC 1000. Another difference between PIC 1100 and HIC 1000 is the fact that PIC 1100 contains a video parallel to serial converter 1189 whereas HIC 1000 contains a video serial to parallel converter 1080. Video parallel to serial converter 1189 receives 16 bit parallel video capture data and video control signals on the Video Port Data [0::15] and Video Port Control lines, respectively, from the video capture circuit (not shown in Fig. 11) and converts them to a serial video data stream that is transmitted on the VPD line to the HIC. The video capture circuit may be any type of video capture circuit that outputs a 16 bit parallel video capture data and video control signals. Another difference lies in the fact that PIC 1100, unlike HIC 1000, contains a clock doubler 1182 to double the video clock rate of the video clock signal that it receives. The doubled video clock rate is fed into video parallel to serial converter 1182 through buffer 1183 and is sent to serial to parallel converter 1080 through buffer 1184. Additionally, reset control unit 1135 in PIC 1100 receives a reset signal from the CPU CNTL & GPIO latch/driver unit 1190 and transmits the reset signal on the RESET# line to the HIC 1000 whereas reset control unit 1045 of HIC 1000 receives the reset signal and forwards it to its CPU CNTL & GPIO latch/driver unit 1090 because, in the above embodiment, the reset signal RESET# is unidirectionally sent from the PIC 1100 to the HIC 1000.

[0116] Like HIC 1000, PIC 1100 handles the PCI bus control signals and control bits from the XPBus representing PCI control signals in the following ways:

1. PIC 1100 buffers clocked control signals from the secondary PCI bus, encodes them and sends the encoded control bits to the XPBus;
2. PIC 1100 manages the signal locally; and
3. PIC 1100 receives control bits from XPBus, translates them into PCI control signals and sends the PCI control signals to the secondary PCI bus.

[0117] PIC 1100 also supports a reference arbiter on the secondary PCI Bus to manage the PCI signals REQ# and GNT#.

[0118] Fig. 12 is a table showing the symbols, signals, data rate and description of signals on the XPBus, where RTN indicates a ground (GND) reference. In the above tables, P&D stands for plug and display and is a trademark of the Video Electronics Standards Association (VESA) for the Plug and Display standard, DDC2:SCL and DDC2:SDA stand for the VESA display data channel (DDC) standard 2 clock and data signals, respectively, SV stands for super video, V33 is 3.3 volts, and V5 is 5.0 volts. TMDS stands for Transition Minimized Differential Signaling and is a trademark of Silicon Images and refers to their Panel Link technology, which is in turn a trademark for their LVDS technology. TMDS is used herein to refer to the Panel Link technology or technologies compatible therewith.

[0119] Fig. 13 is a table showing the information transmitted on the XPBus during two clock cycles of the XPBus in one embodiment of the present invention where 10 data bits are transmitted in each clock cycle of the XPBus. In Fig. 13, A00 to A31 represent 32 bits of PCI address A[31::0], D00 to D31 represent 32 bits of PCI data D[31::0], BS0 to BS3 represent 4 bits of bus status data indicating the status of the XPBus, CM0# to CM3# represent 4 bits of PCI command information, BE0# to BE3# represent 4 bits of PCI byte enable information, and CN0 to CN9 represent 10 bits of control information sent in each clock cycle. As shown in Fig. 13, for each of lines PD0 to PD3, the 10 bit data packets contain one BS bit, one CM/BE bit, and eight AID bits. For the PCN line, the 10 bit data packet contains 10 CN bits. The first clock cycle shown in Fig. 13 comprises an address cycle in which 4 BS bits, 4 CM bits, 32 A bits and 10 CN bits are sent. The second clock cycle comprises a data cycle in which 4 BS bits, 4 BE bits, 32 D bits and 10 CN bits are sent. The bits transmitted on lines PD0 to PD3 represent 32 PCI AD[31::0] signals, 4 PCI C/BE# [3::0] signals, and part of the function of PCI control signals, such as FRAME#, IRDY#, and TRDY#.

[0120] In the embodiment shown in Fig. 13, BS0 to BS3 are sent at the beginning of each clock cycle. The bus status bits indicate the following bus cycle transactions: idle, address transfer, write data transfer, read data transfer, switch XPBus direction, last data transfer, wait, and other cycles.

[0121] Bits representing signals transmitted between the CPU and South Bridge may also be sent on the lines interconnecting the HIC and PIC, such as lines PCN and PCNR. For example, CPU interface signals such as CPU interrupt (INTR), Address 20 Mask (A20M#), Non-Maskable Interrupt (NMI), System Management Interrupt (SMI#), and Stop Clock (STPCLK#), may be translated into bit information and transmitted on the XPBus between the HIC and the PIC.

[0122] Fig. 14 is a table showing the information transmitted on the XPBus during four clock cycles of the XPBus in another embodiment of the present invention where 10 data bits are transmitted in each clock cycle of the XPBus. In this embodiment, the XPBus clock rate is twice as large as the PCI clock rate. This allows sending data and address bits every other XPBus cycle. As can be seen in Fig. 14, there are no address or data bits transmitted during the second or fourth XPBus clock cycle. The fact that the XPBus clock rate is higher than the PCI clock rate allows for compatibility of the XPBus with possible future expansions in the performance of PCI bus to higher data transfer and clock rates.

[0123] In the embodiment shown in Fig. 14, there are 18 control bits, CN0 to CN17, transmitted in every two XPBus clock cycles. The first bit transmitted on the control line in each XPBus clock cycle indicates whether control bits CN0 to CN8 or control bits CN9 to CN17 will be transmitted in that cycle. A zero sent at the beginning of a cycle on the control line indicates that CN0 to CN8 will be transmitted during that cycle, whereas a one sent at the beginning of a cycle on the control line indicates that CN9 to CN17 will be transmitted during that cycle. These bits also indicate the presence or absence of data and address bits during that cycle. A zero indicates that address or data bits will be transmitted during that cycle whereas a one indicates that no address or data bits will be transmitted during that cycle.

[0124] In one embodiment, BS0 and BS1 are used to encode the PCI signals FRAME# and IRDY#, respectively. Additionally, in one embodiment, BS2 and BS3 are used to

indicate the clock speed of the computer bus interface and the type of computer bus interface, respectively. For example, BS2 value of zero may indicate that a 33 MHz PCI bus of 32 bits is used whereas a BS2 value of one may indicate that a 66 MHz PCI bus of 32 bits is used. Similarly, a BS3 value of zero may indicate that a PCI bus is used whereas a BS3 value of one may indicate that another computer interface bus, such as an Institute of Electronics & Electrical Engineers (IEEE) 1394 bus, is used.

[0125] Fig. 15 is a schematic diagram of lines PCK, PD0 to PD3, and PCN. These lines are unidirectional LVDS lines for transmitting clock signals and bits such as those shown in FIGS. 13 and 14 from the HIC to the PIC. The bits on the PD0 to PD3 and the PCN lines are sent synchronously within every clock cycle of the PCK. Another set of lines, namely PCKR, PDR0 to PDR3, and PCNR, are used to transmit clock signals and bits from the PIC to HIC. The lines used for transmitting information from the PIC to the HIC have the same structure as those shown in Fig. 15, except that they transmit data in a direction opposite to that in which the lines shown in Fig. 15 transmit data. In other words they transmit information from the PIC to the HIC. The bits on the PDR0 to PDR3 and the PCNR lines are sent synchronously within every clock cycle of the PCKR. Some of the examples of control information that may be sent in the reverse direction, i.e., on PCNR line, include a request to switch data bus direction because of a pending operation (such as read data available), a control signal change in the target requiring communication in the reverse direction, target busy, and transmission error detected.

[0126] The XPBus which includes lines PCK, PD0 to PD3, PCN, PCKR, PDR0 to PDR3, and PCNR, has two sets of unidirectional lines transmitting clock signals and bits in opposite directions. The first set of unidirectional lines includes PCK, PD0 to PD3, and PCN. The second set of unidirectional lines includes PCKR, PDR0 to PDR3, and PCNR. Each of these unidirectional set of lines is a point-to-point bus with a fixed transmitter and receiver, or in other words a fixed master and slave bus. For the first set of unidirectional lines, the HIC is a fixed transmitter/master whereas the PIC is a fixed receiver/slave. For the second set of unidirectional lines, the PIC is a fixed transmitter/master whereas the HIC is a fixed receiver/slave. The LVDS lines of XPBus, a cable friendly and remote system I/O bus, transmit fixed length data packets within a clock cycle.

[0127] The XPBus lines, PD0 to PD3, PCN, PDR0 to PDR3 and PCNR, and the video data and clock lines, VPD and VPCK, are not limited to being LVDS lines, as they may

be other forms of bit based lines. For example, in another embodiment, the XPBus lines may be IEEE 1394 lines.

[0128] It is to be noted that although each of the lines PCK, PD0 to PD3, PCN, PCKR, PDR0 to PDR3, PCNR, VPCK, and VPD is referred to as a line, in the singular rather than plural. each such line may contain more than one physical line. For example, in the embodiment shown in Fig. 23, each of lines PCK, PD0 to PD3 and PCN includes two physical lines between each driver and its corresponding receiver. The term line, when not directly preceded by the terms physical or conductive, is herein used interchangeably with a signal or bit channel which may consist of one or more physical lines for transmitting a signal. In the case of non-differential signal lines, generally only one physical line is used to transmit one signal. However, in the case of differential signal lines, a pair of physical lines is used to transmit one signal. For example, a bit line or bit channel in an LVDS or IEEE 1394 interface consists of a pair of physical lines which together transmit a signal.

[0129] A bit based line (i.e., a bit line) is a line for transmitting serial bits. Bit based lines typically transmit bit packets and use a serial data packet protocol. Examples of bit lines include an LVDS line, an IEEE 1394 line, and a Universal Serial Bus (USB) line.

[0130] Fig. 16 is a table showing the names, types, number of pins dedicated to, and the description of the primary bus PCI signals. The pins represent those between the host PCI bus and the HIC.

[0131] FIG. 17 is a block diagram of the components in one computer system employing the present invention. The computer system comprises an attached computer module (ACM), a peripheral console (PCON), and the interconnection apparatus between them. The ACM includes the central processing unit (CPU) 1710, system memory 1720, high performance devices 1750, primary mass storage 1730, and related interface and support circuitry 1740. The PCON includes primary display 1810, primary input 1820, secondary mass storage 1750, other devices 1860, expansion slots 1870, the primary power supply 1830, and related interface and support circuitry 1840. The interconnection apparatus 1900 includes circuitry to convey power and operational signals between the ACM and PCON.

[0132] Within the ACM 1700, the CPU 1710 executes instructions and manipulates data stored in the system memory. The CPU 1710 and system memory 1720 represent the user's core computing power. The core computing power may also include high performance devices 1750 such as advanced graphics processor chips that greatly increase overall system performance and which, because of their speed, need to be located close to the CPU. The primary mass storage 1730 contains persistent copies of the operating system software, application software, configuration data, and user data. The software and data stored in the primary mass storage device represent the user's computing environment. Interface and support circuitry 1740 primarily includes interface chips and signal busses that interconnect the CPU, system memory, high performance devices, and primary mass storage. The interface and support circuitry also connects ACM-resident components with the ACM-to-PCON interconnection apparatus as needed.

[0133] Within the PCON 1800, the primary display component 1810 may include an integrated display device or connection circuitry for an external display device. This primary display device may be, for example, an LCD, plasma, or CRT display screen used to display text and graphics to the user for interaction with the operating system and application software. The primary display component is the primary output of the computer system, i.e., the paramount vehicle by which programs executing on the CPU can communicate toward the user.

[0134] The primary input component 1820 of the PCON may include an integrated input device or connection circuitry for attachment to an external input device. The primary input may be, for example, a keyboard, touch screen, keypad, mouse, trackball, digitizing pad, or some combination thereof to enable the user to interact with the operating system and application software. The primary input component is the paramount vehicle by which programs executing on the CPU receive signals from the user.

[0135] The PCON may contain secondary mass storage 1850 to provide additional high capacity storage for data and software. Secondary mass storage may have fixed or removable media and may include, for example, devices such as diskette drives, hard disks, CD-ROM drives, DVD drives, and tape drives.

[0136] The PCON may be enhanced with additional capability through the use of integrated “Other Devices” 1860 or add-on cards inserted into the PCON’s expansion slots 1870. Examples of additional capability include sound generators, LAN connections, and modems. Interface and support circuitry 1840 primarily includes interface chips, driver chips, and signal busses that interconnect the other components within the PCON. The interface and support circuitry also connects PCON-resident components with the ACM-to-PCON interconnection apparatus as needed.

[0137] Importantly, the PCON houses the primary power supply 1830. The primary power supply has sufficient capacity to power both the PCON and the ACM 1700 for normal operation. Note that the ACM may include a secondary “power supply” in the form, for example, of a small battery. Such a power supply would be included in the ACM to maintain, for example, a time-of-day clock, configuration settings when the ACM is not attached to a PCON, or machine state when moving an active ACM immediately from one PCON to another. The total energy stored in such a battery would, however, be insufficient to sustain operation of the CPU at its rated speed, along with the memory and primary mass storage, for more than a fraction of an hour, if the battery were able to deliver the required level of electrical current at all.

[0138] FIG. 18 is a block diagram of an attached computing module (ACM) 1700. The physical ACM package 1700 contains the ACM functional components 1701 and the ACM side of the ACM-to-PCON Interconnection 1900. The ACM 1701 comprises a CPU component 1710, a system memory component 1720, a primary mass storage component 1730, a high performance devices components 1750, and an interface and support component 1740.

[0139] The ACM side of the ACM-to-PCON Interconnection 1900 comprises a Host Interface Controller (HIC) component 1920 and an ACM connector component 1930. The HIC 1920 and connector 1930 components couple the ACM functional components 1700 with the signals of an ACM-to-PCON interface bus 1910 used to operatively connect an ACM with a PCON. The ACM-to-PCON interface bus 1910 comprises conveyance for electrical power 1914 and signals for a peripheral bus 1912, video 1916, video port 1917, and console type 1918. The preferred ACM-to-PCON Interconnection 1900 is described in detail in a companion U.S. patent application, Ser. No. 09/149,882, entitled “A Communication Channel and Interface Devices for Bridging Computer

Interface Buses,” by the same inventor, filed on the same day herewith, and hereby incorporated by reference. The preferred ACM-to-PCON interconnection 1900 includes circuitry to transmit and receive parallel bus information from multiple signal paths as a serial bit stream on a single signal path. This reduces the number of physical signal paths required to traverse the interconnection 1900. Further, employing low-voltage differential signaling (LVDS) on the bit stream data paths provides very reliable, high-speed transmission across cables. This represents a further advantage of the present invention.

[0140] The CPU component 1710 of the ACM functional circuitry 1701 of the presently described embodiment comprises a microprocessor 1712, which is the chief component of the personal computer system, power supply connection point 1713, and cache memory 1714 tightly coupled to the microprocessor 1712 by the CPU-to-cache bus 1714 comprising signal paths for address, data, and control information. The microprocessor 1712 of this embodiment is one of the models from the Pentium II family of processors from Intel Corporation. Microprocessor 1712 receives electrical power from power bus 1768 via connection point 1713. Microprocessor 1712 couples to the Host Interface Controller (HIC) 1920 via CPU-to-HIC bus 1763 comprising signal paths to exchange control information such as an interrupt request. Microprocessor 1712 also couples to CPU Bridge 1746 via CPU main bus 1764 comprising signal paths for address, data, and control information.

[0141] The CPU Bridge component 1746 of the interface and support circuitry 1740 operates to couple the high speed CPU main bus 1764 to specialty buses of varying speeds and capability that connect other computer components. The CPU Bridge of the presently described embodiment incorporates memory controller circuitry, advanced graphics processor support circuitry, and a general, industry-standard PCI bus controller in a single package. A CPU Bridge 1746 such as the 82443LX PCI/AGP Controller from Intel Corporation may be used.

[0142] The system memory component 1720 of the ACM functional circuitry 1701 in the present embodiment comprises main system memory (RAM) 1722, BIOS memory 1724, and flash memory 1726. The system memory 1720 is used to contain data and instructions that are directly addressable by the CPU. The RAM 1722 comprises volatile memory devices such as DRAM or SDRAM memory chips that do not retain their stored contents when power is removed. This form of memory represents the largest proportion

of total system memory 1720 capacity. The BIOS memory 1724 comprises non-volatile memory devices such as ROM or EPROM memory chips that retain their stored contents regardless of the application of power and are read-only memory under normal operating conditions. The BIOS memory 1724 stores, for example, start-up instructions for the microprocessor 1712 and sets of instructions for rudimentary input/output tasks. The flash memory 1726 comprises non-volatile memory devices that retain their stored contents regardless of the application of power. Unlike the BIOS non-volatile memory, however, the stored contents of the flash memory 1726 are easily changed under normal operating conditions. The flash memory 1726 may be used to store status and configuration data, such as security identifiers or ACM specifications like the speed of the microprocessor 1712. Some embodiments may combine the BIOS functions into the flash memory device, thus permitting BIOS contents to be rewritten, improving field upgradability.

[0143] The main system memory (RAM) 1722 is coupled to memory controller circuitry resident within the CPU Bridge 1746 via direct memory bus 1765. The BIOS 1724 and flash memory 1726 are coupled to HIC 1920 via switched memory bus 1766. This permits the BIOS 1724 and flash 1726 memories to be accessed by circuitry in the HIC 1920 or other circuitry connected thereto. The direct memory bus 1765 and the switch memory bus 1766 each comprises conductors to convey signals for data, address, and control information.

[0144] The primary mass storage component 1730 of the ACM functional circuitry 1701 in the present embodiment comprises a compact hard disk drive with an industry-standard, IDE interface. The hard disk drive (HDD) 1732 has a formatted storage capacity sufficient to contain an operating system for the computer, application software desired by the user, and related user configuration and operating parameter data. The HDD 1732 in the present embodiment serves as the “boot” device for the personal computer from which the operating system is loaded into RAM 1722 by the start-up program stored in the BIOS 1724.

[0145] The present HDD 1732 has a capacity of approximately 2,000 megabytes to provide adequate storage for common software configurations and reasonable space for user data. One example of a common software configuration includes the Windows 95 operating system from Microsoft Corporation, a word processing program, a spreadsheet

program, a presentation graphics program, a database program, an email program, and a web browser such as Navigator from Netscape Corporation. The hard disk 1732 stores program and data files for each software component, including files distributed by the vendor as well as files created or updated by operation of the software after it is installed. For example, a word processor program may maintain information about a user's identity and latest preferences in an operating system registry file. Or, for example, the web browser may maintain a file of the user's favorite web sites or most recently viewed web pages. An HDD with 2000 megabyte capacity is readily available in the small size of hard disk (e.g., 2.5-inch or 3.5-inch) to minimize the space required within the ACM for the primary mass storage device 1730.

[0146] The HDD 1732 is coupled to IDE controller circuitry 1748 via IDE bus 1772. The IDE controller circuitry 1748 is coupled to the CPU Bridge 1746 via the Host PCI bus 1767. IDE controllers and busses, and the PCI bus are well known and understood in the industry. The above components operate together to couple the hard disk drive 1732 to the microprocessor 1712.

[0147] The high performance devices component 1750 of the ACM functional circuitry 1701 in the present embodiment comprises an Advanced Graphics Processor (AGP) 1752. The Model 740 Graphics Device from Intel Corporation may be used in the present embodiment as the AGP.

[0148] Increases in computer screen size, graphics resolution, color depth, and visual motion frame rates, used by operating system and application software alike, have increased the computing power required to generate and maintain computer screen displays. An AGP removes a substantial portion of the graphics computing burden from the CPU to the specialized high-performance processor, but a high level of interaction between the CPU and the specialized processor is nonetheless required. To maximize the effective contribution of having a specialized processor in the presently described embodiment, the AGP 1752 is located in the ACM 1700, where it is in close proximity to the microprocessor 1712. The AGP 1752 is coupled to the microprocessor 1712 via the advanced graphics port bus 1773 of the CPU Bridge 1746. The visual display signal generated by the AGP are conveyed toward actual display devices at the peripheral console (PCON) via video signal bus 1770. Video information from a source external to

the ACM and appearing as video port signals 1917 may be conveyed to the AGP 1752 via video port signal path 1771.

[0149] Other types of high performance components may be included in different ACM configurations. For example, an interface to an extremely high speed data communication facility may be desirable in some future computer where CPU-to-network interaction is of comparable intensity to today's CPU-to-graphics interaction. Because such high performance components tend to be high in cost, their inclusion in the ACM is desirable. Inclusion of high cost, high performance components in the ACM concentrates a user's core computing power and environment in a portable package. This represents a further advantage of the invention.

[0150] The interface and support component 1740 of the ACM functional circuitry 1701 in the present embodiment comprises circuitry for power regulation 1742, clocking 1744, CPU Bridge 1746, IDE controller 1748, and signal conveyance paths 1761-1774. The CPU Bridge 1746 couples the CPU component 1710 of the ACM 1700 with the other components of the ACM 1720-1750 and the CPU-to-PCON Interconnection 1900. The CPU Bridge 1746 and IDE controller 1748 have already been discussed. Power regulation circuitry 1742 receives electrical power via the electrical power conduction path 1914 of the CPU-to-PCON Interconnection 1900, conditions and distributes it to the other circuitry in the ACM using power distribution bus 1768. Such regulation and distribution is well known and understood in the art.

[0151] Clocking circuitry 1744 generates clock signals for distribution to other components within the ACM 1700 that require a timing and synchronization clock source. The CPU 1710 is one such component. Often, the total power dissipated by a CPU is directly proportional to the frequency of its main clock signal. The presently described embodiment of the ACM 1700 includes circuitry that can vary the frequency of the main CPU clock signal conveyed to the CPU via signal path 1762, in response to a signal received from the host interface controller (HIC) 1920 via signal path 1761. The generation and variable frequency control of clocking signals is well understood in the art. By varying the frequency, the power consumption of the CPU (and thus the entire ACM) can be varied.

[0152] The variable clock rate generation may be exploited to match the CPU power consumption to the available electrical power. Circuitry in the host interface controller (HIC) 1920 of the presently described embodiment adjusts the frequency control signal sent via signal path 1761 to the clocking circuitry 1744, based on the “console type” information signal 1918 conveyed from the peripheral console (PCON) by the CPU-to-PCON interconnection 1900. In this arrangement, the console type signal originating from a desktop PCON would result in the generation of a maximum speed CPU clock. The desktop PCON, presumably has unlimited power from an electrical wall outlet and does not need to sacrifice speed for power conservation. The console type signal originating from a notebook PCON would, however, result in the generation of a CPU clock speed reduced from the maximum in order to conserve battery power and extend the duration of computer operation obtained from the energy stored in the battery. The console type signal originating from a notepad PCON would result in the generation of a CPU clock speed reduced further yet, the notepad PCON presumably having smaller batteries than the notebook PCON. Inclusion of control signals and circuitry to effect a CPU clock signal varying in frequency according to characteristics of the PCON to which the ACM is connected facilitates the movement of the user’s core computing power and environment to different work settings, which is a further advantage of the present invention.

[0153] FIG. 19 illustrates an external view of one embodiment of an ACM. The case 2010 of the ACM 1700 is generally rectangular in shape, preferably constructed of a strong, lightweight, rigid material that will protect the internal components from mechanical and environmental exposure. Plastics may readily be used to construct the case 2010. The case 2010 completely surrounds the internal components, being generally an 8-sided box. FIG. 19 shows the top 2012, right 2014, and rear 2016 surfaces of the ACM case 2010. Rear edges 2018 of the case joining the rear surface 2016 with its adjoining surfaces may be beveled or rounded to facilitate insertion of the ACM 1700 into the computer bay of the PCON. Notches 2040 may be formed by projecting small surfaces inward from otherwise generally flat surfaces of the ACM case 2010. The notches 2040 may be used to engage with mechanical devices mounted in and about a computer bay. Such mechanical devices can be employed to secure the ACM into position within a computer bay for reliability and security. Openings 2017 are formed into the rear surface 2016 of the ACM case 2010 through which to project connectors

1930a and 1930b. In one embodiment the case 2010 is approximately 5.75 inches wide by 6.5 inches deep by 1.6 inches high.

[0154] Connectors 1930a and 1930b are part of the ACM-to-PCON Interconnection as described earlier in reference to FIGS. 3 and 4. When the ACM 1700 is inserted into the computer bay of a peripheral console (PCON), connectors 1930a and 1930b mate with corresponding connectors located at the rear of the computer bay to electrically couple the ACM with the PCON containing the computer bay. Details concerning the ACM-to-PCON Interconnection can be found in the U.S. patent application entitled “A Communication Channel and Interface Devices for Bridging Computer Interface Buses,” already incorporated herein by reference. The connectors 1930a and 1930b used in one embodiment are connectors complying with the Device Bay industry standard as documented in “Device Bay Interface Specification,” revision 0.85, Feb. 6, 1998. Such connectors have specifically been designed to stand up to the rigors of repeated insertion and withdrawal.

[0155] Cooling plate 2030 forms part of the top surface 2012 of ACM 1700. The cooling plate 2030 may be mounted to, or project through an opening formed in, case 2010. Similarly, electromagnetic interference (EMI)/electrostatic discharge (ESD) grounding plate 2032 forms part of the right surface 2014 of ACM 1700. The grounding plate 2032 may be mounted to, or project through an opening formed in, case 2010. Cooling plate 2030 and grounding plate 2032 compressively mate with counterparts when the ACM is fully inserted into the computer bay. The counterparts located along the boundaries of the computer bay conduct dangerous heat and electrical charges away from the ACM. Inside the ACM, cooling plate 2030 thermally couples to heat-sensitive components such as CPU 1710 by methods well known in the art. Similarly, grounding plate 2032 electrically couples to EMI/ESD-sensitive components, such as a microprocessor, by methods well known in the art.

[0156] LCD display 2050 forms part of the right surface 2014 of ACM 1700. The LCD display may be mounted to, or project through an opening formed in, case 2010. The LCD display may contain indicators about the status of the ACM. Such indicators may display, for example, the time-of-day from a time-of-day clock contained within the ACM, or the amount of charge remaining in an ACM-resident battery, or certain configuration options recorded in flash memory. The LCD display 2050 provides display

capability for a limited amount of information, most useful when the ACM is separated from a PCON (and is thus separated from a full-capability, primary display device).

[0157] FIG. 19b illustrates one possible embodiment of a computer bay. A computer bay 1890 acts as a receptacle for lodging an ACM (such as the one shown in FIG. 20) within a desktop PCON. The illustrated computer bay 1890 provides an ACM with housing and with signal flow, electrical grounding, heat transfer, and mechanical connections. While many physical arrangements between the ACM and PCON are possible, the use of an enclosed computer bay as the one illustrated in FIG. 20b offers many advantages. For example, the illustrated computer bay 1890 provides physical protection for the ACM. The computer bay may also be easily incorporated into industry standard form factors used in the manufacture of desktop personal computers (e.g., the ACM and associated computer bay could be designed to fit within the volume occupied by a standard-size disk drive).

[0158] The computer bay 1890 appearing in FIG. 20b is shown mounted within the confines of PCON case 1802. The computer bay 1890 comprises frame 1891 and signal flow, grounding, cooling, and locking components as described below. Mounting flanges 1898 of frame 1891 may be used to attach the computer bay 1890 to the PCON structure. The computer bay 1890 is prominently defined by frame 1891 generally forming a cavity in which to lodge an ACM. As such, the interior cavity formed by frame 1891 closely approximates the exterior dimensions of a compatible ACM. The top 1893, right 1894, and rear 1895 sides of the computer bay frame 1891 are visible. The computer bay frame 1891 also includes substantial bottom and left sides which are not shown. The front side of the frame 1891 (not shown) is open to allow the insertion of the ACM. Frame 1891 is constructed of metal for strength and to facilitate the conductance of heat and undesired electrical currents away from the ACM.

[0159] In the presently described embodiment, the weight of an inserted ACM is largely borne by the bottom side (not shown) of computer bay frame 1891. Alternative embodiments are possible where, for example, the weight of the ACM is borne by rails running longitudinally down the right and left sides of the computer bay cavity that engage corresponding grooves running longitudinally down the right and left sides of an ACM.

[0160] FIG. 20 illustrates the internal component layout for one embodiment of an ACM. All components are contained within the confines of the ACM case 510, except for connectors 1930a and 1930b which extend from the rear of the ACM 1700 to engage mating connectors (not shown) that will couple the ACM circuitry with the PCON circuitry. Main circuit board 2110 provides electrical connections for circuitry within the ACM and mounting for many of its components 1724, 1722, 17221, 1752, 1742, 1748, 1920, and 1930. The fabrication and use of such circuits boards is well known and understood in the art. Connector 2122 is also mounted on main circuit board 2110 and mates with mobile processor module 2120. Mobile processor module 2120 represents a form of packaging for a microprocessor and related components. The illustrated mobile processor module 2120 is a self-contained unit that includes a microprocessor 1712, CPU cache 1714, and CPU bridge 1746 operatively interconnected by the manufacturer. An example of one such module is the Pentium Processor with MMX Technology Mobile Module from Intel Corporation (order number 24 3515-001, September 1997). One skilled in the art recognizes that discrete microprocessor, cache, and bridge could have been employed and mounted directly to the main circuit board.

[0161] The mobile processor module 2120 blocks the view, from the top, of the system BIOS 1724. Similarly, hard disk drive 1732 hides RAM memory 1722, the high performance graphics processor 1752, the host interface controller 1920, and flash memory 1726. Memory upgrade socket 2130 remains exposed to facilitate installation of additional RAM memory 1722. Power regulator 1742, like the memory upgrade socket, enjoys a generous amount of overhead clearance to accommodate its vertical size. The area including IDE controller 1748 also enjoys overhead clearance to facilitate a cable connection with the hard disk drive 1732.

[0162] The functional interconnection and operation of components contained within the ACM and depicted in FIG. 20 has already been described in relation to FIG. 18 for like numbered items appearing therein.

[0163] FIG. 21 is a block diagram of a peripheral console (PCON). A peripheral console couples with an ACM to form an operating personal computer system. The peripheral console (PCON) supplies an ACM with primary input, display, and power supply; the ACM supplies the core computing power and environment of the user. In the presently described embodiment the physical PCON package 200 contains the PCON

functional components 1801 and the PCON side of the ACM-to-PCON Interconnection 1900. The PCON functional components 1801 comprise primary display 1810, a primary input 1820, a primary power supply 1830, interface and support 1840, secondary mass storage 1850, other devices 1860, and expansion slots 1870.

[0164] The PCON side of the ACM-to-PCON Interconnection 1900 comprises a Peripheral Interface Controller (PIC) component 1940, a PCON connector component 1950, console-type component 1942, and flash memory device 1948. The PIC 1940 and connector 1950 components couple the PCON functional components 1801 with the signals of an ACM-to-PCON interface bus 1910 used to operatively connect an ACM with a PCON. The ACM-to-PCON interface bus 1910 comprises conveyance for electrical power 1914 and signals for a peripheral bus 1912, video 1916, video port 1917, and console-type 1918. The preferred ACM-to-PCON Interconnection 1900 is described in detail in the U.S. patent application entitled “A Communication Channel and Interface Devices for Bridging Computer Interface Buses,” already incorporated herein by reference.

[0165] Connector component 1950 may be selected to mate directly with the connector component 1930 of an ACM (shown in FIG. 18). Alternatively, connector component 1950 may be selected to mate with, for example, the connector on one end of a cable intervening between the PCON and an ACM in a particular embodiment, such as cable 1964 shown in FIG. 19B. The ACM-to-PCON interconnection described in the aforementioned companion patent application has the advantage of providing reliable signal conveyance across low cost cables.

[0166] Flash memory device 1948 provides non-volatile storage. This storage may be accessible to devices in both the ACM and the PCON, including the host interface controller and the peripheral interface controller to which it is connected. As such, flash memory 1948 may be used to store configuration and security data to facilitate an intelligent mating between an ACM and a PCON that needs no participation of the CPU.

[0167] The primary display component 1810 of the PCON functional circuitry 1801 of the presently described embodiment comprises integrated display panel 1812 and video connector 1813. Integrated display panel 1812 is a color LCD display panel having a resolution of 640 horizontal by 480 vertical pixels. 640-by-480 resolution is popularly

considered to be the minimum screen size to make practical use of the application software in widespread use today. One skilled in the art recognizes that the type and resolution of the display can vary greatly from embodiment to embodiment, depending on factors such as cost and intended application. Any display device may be used, without departing from the scope and spirit of the invention, that provides principal visual output to the computer user for operating system and application software executing in its customary and intended fashion using the CPU component (1710 of FIG. 17) of an ACM presently coupled to PCON 1800.

[0168] Integrated display panel 1812 is coupled to video signal bus 1849 and displays a screen image in response to video signals presented on bus 1849. Certain pins of connector 1950 receive video output signals 1916 of the ACM-to-PCON interface bus 1910 from a mated connector that is coupled to an ACM. These certain pins of connector 1950 couple to video signal bus 1849 which conveys the video output signals 316 throughout the PCON 1800 as needed. Video connector 1813 is exposed at the exterior of PCON 1800 and couples to video signal bus 1849. Connector 1813 permits easy attachment of an external display device that is compatible with the signals carried by bus 1849, such as a CRT monitor (not shown). The external display device may be used in addition, or as an alternative, to integrated display panel 1812.

[0169] The isolation of the relatively heavy and sizable primary display 1810 from the core computing power and user environment contained within an ACM represents a further advantage of the present invention.

[0170] The primary input component 1820 of the PCON functional circuitry 1801 of the presently described embodiment comprises keyboard interface circuitry 1822, keyboard connector 1823, pointer interface circuitry 1824, and pointer connector 1825. Keyboard interface circuitry 1822 and pointer interface circuitry 1824 connect to ISA bus 1845 and are thereby coupled to the CPU component (1710 of FIG. 17) of any ACM attached to PCON 1800. Keyboard interface circuitry 1822 interfaces a standard computer keyboard (not shown), attached at connector 1823, to ISA bus 1845. Pointer interface circuitry 1824 interfaces a standard computer pointing device (not shown), such as a computer mouse attached at connector 1825, to ISA bus 1845. Computer keyboards, pointing devices, connectors 1823, 1825, keyboard interface circuitry 1822, and pointer interface circuitry 1824 are well known in the art. The isolation of the relatively heavy and sizable

primary input devices 1820 from the core computing power and user environment contained within an ACM represents a further advantage of the present invention.

[0171] The primary power supply component 1830 of the PCON functional circuitry 1801 of the presently described embodiment provides electrical energy for the sustained, normal operation of the PCON 1800 and any ACM coupled to connector 1950. The power supply may be of the switching variety well known in the art that receives electrical energy from an AC source 1889, such as a wall outlet. Power supply 1830 reduces the alternating current input voltage, to a number of distinct outputs of differing voltages and current capacities. The outputs of power supply 1830 are applied to power bus 1831. Power bus 1831 distributes the power supply outputs to the other circuitry within the PCON 1800. Bus 1831 also connects to certain pins of connector 1950 to provide the electrical power 1914 for an ACM conveyed by ACM-to-PCON interconnection 1900. The isolation of the usually heavy power supply 1830 from the core computing power and user environment contained within the ACM represents a further advantage of the present invention.

[0172] The interface and support component 1840 of the PCON functional circuitry 1801 of the presently described embodiment comprises peripheral bridge 1846, diskette controller 1842, IDE controller 1848, and signal conveyance paths 1841, 1843, 1844, 1845, 1847 and 1849. Peripheral bridge 1846 couples PCI peripheral bus 1841 with peripheral busses of other formats such as ISA peripheral bus 1845 and others 1847. PCI and ISA peripheral busses are industry standards, well known and understood in the art. Other peripheral busses 1847 may include, for example, a bus compliant with the universal serial bus (USB) industry standard. While other embodiments of a peripheral console 1800 may include a single peripheral bus that is coupled to an attached ACM via ACM-to-PCON interconnection 1900, such as PCI bus 1841, this embodiment includes peripheral bridge 1846 to establish additional busses 1845, 1847. The additional busses 1845, 1847 permit the use of the many low-cost and readily available components compatible with these bus specifications.

[0173] Diskette controller 1842 interfaces a floppy disk drive 1854 with the CPU component 1710 of an attached ACM (shown in FIG. 18) so that the CPU may control and use the diskette drive 1854 hardware to store and retrieve data. Diskette controller

1842 couples to the CPU via a connection to ISA bus 1845. Diskette controller 1842 connects to the diskette drive 1854 via one of device cables 1843.

[0174] Similarly, IDE controller 1848 interfaces a hard disk drive 1852 and a CDROM drive 1856 with the CPU component 1710 of an attached ACM (shown in FIG. 18) so that the CPU may control and use the hard disk drive 1852 and CDROM 1856 hardware to store and retrieve data. IDE controller 1848 couples to the CPU via connection to PCI peripheral bus 1841. IDE controller 1848 connects to each of hard disk drive 1852 and CD-ROM drive 1856 via one of device cables 1843. Some embodiments of PCON 1800 may take advantage of VLSI integrated circuits such as an 82371SB (PIIX4) integrated circuit from Intel Corporation. An 82371SB integrated circuit includes circuitry for both the peripheral bridge 1846 and the IDE controller 1848 in a single package.

[0175] The secondary mass storage component 1850 of the PCON functional circuitry 1801 of the presently described embodiment comprises diskette drive 1854, hard disk drive 1852, and CD-ROM drive 1856. Secondary mass storage 1850 generally provides low-cost, non-volatile storage for data files which may include software program files. Data files stored on secondary mass storage 1850 are not part of a computer user's core computing power and environment. Secondary mass storage 1850 may be used to store, for example, seldom used software programs, software programs that are used only with companion hardware devices installed in the same peripheral console 1800, or archival copies of data files that are maintained in primary mass storage 1750 of an ACM (shown in FIG. 18). Storage capacities for secondary mass storage 1850 devices may vary from the 1.44 megabytes of the 3.5-inch high density diskette drive 1854, to more than 10 gigabytes for a large format (5-inch) hard disk drive 1852. Hard disk drive 1852 employs fixed recording media, while diskette drive 1854 and CD-ROM drive 1856 employ removable media. Diskette drive 1854 and hard disk drive 1852 support both read and write operations (i.e., data stored on their recording media may be both recalled and modified) while CD-ROM drive 1856 supports only read operations.

[0176] The other devices component 1860 of the PCON functional circuitry 1801 of the presently described embodiment comprises a video capture card. A video capture card accepts analog television signals, such as those complying with the NTSC standard used for television broadcast in the United States, and digitizes picture frames represented by the analog signal for processing by the computer. Video capture cards at present are

considered a specialty, i.e., not ubiquitous, component of personal computer systems. Digitized picture information from video capture card 1860 is carried via signal conveyance path 1844 to the peripheral interface controller 1940 which transforms it to the video port signals 1917 of the ACM-to-PCON interconnection 1900 for coupling to the advanced graphics processor 1752 in an attached ACM (shown in FIG. 18).

[0177] Video capture card 1860 is merely representative of the many types of “other” devices that may be installed in a PCON to expand the capabilities of the personal computer. Sound cards and laboratory data acquisition cards are other examples. Video capture card 1860 is shown installed in one of expansion slots 1870 for coupling to the interface and control circuitry 1840 of the PCON. Any of other devices 1860 could be coupled to the interface and control circuitry 1840 of the PCON by different means, such as direct installation on the circuit board that includes the interface and control circuitry 1840; e.g., a motherboard.

[0178] The expansion slots component 1870 of the PCON functional circuitry 1801 of the presently described embodiment comprises PCI connectors 1871 and ISA connectors 1872. A circuit card may be inserted into one of the connectors 1871, 1872 in order to be operatively coupled with the CPU 1710 of an attached ACM (shown in FIG. 18). Each of connectors 1871 electrically connects to PCI bus 1841, and may receive and hold a printed circuit card which it electrically couples to PCI bus 1841. Each of connectors 1872 electrically connects to ISA bus 1845, and may receive and hold a printed circuit card which it electrically couples to ISA bus 1845. The PCI 1841 and ISA 1845 busses couple to the CPU 1710 of an attached ACM (shown in FIG. 18) by circuitry already described.

[0179] An embodiment of a detachable computing module in accordance with the present invention, for attachment to a peripheral console for forming a fully operational computer system, comprises, an enclosure, a CPU, a memory coupled to said CPU, and a mass storage coupled to said CPU. The module further comprises interconnection circuitry coupled to said CPU, said interconnection circuitry connectable to a peripheral console. The CPU is uncoupled from any primary input circuitry when said interconnection circuitry is disconnected from a peripheral console.

[0180] An alternative embodiment of a detachable computing module in accordance with the present invention, for attachment to a peripheral console for forming a fully operational computer system, comprises an enclosure, a CPU, a memory coupled to said CPU, and a mass storage coupled to said CPU. The module further comprises interconnection circuitry coupled to said CPU, said interconnection circuitry connectable to a peripheral console. The CPU is uncoupled from any primary output circuitry when said interconnection circuitry is disconnected from a peripheral console.

[0181] Various modifications to the preferred embodiment can be made without departing from the spirit and scope of the invention. (A limited number of modifications have already been described in the preceding discussion.) For example, a particular embodiment may insert another layer of bus bridging between the CPU bridge and the Peripheral bridge. This may be desirable if, for example, a vendor wants to implement a proprietary, general-purpose bus having intermediate performance characteristics that fall between those of the high-performance general purpose bus originating at the CPU, and the slower general purpose PCI bus. Thus, the foregoing description is not intended to limit the invention as set forth.

[0182] In most embodiments, the ACM includes an enclosure such as the one described with the following components, which should not be limiting:

- 1) A CPU with cache memory;
- 2) Core logic device or means;
- 3) Main memory;
- 4) A single primary Hard Disk Drive ("HDD") that has a security program;
- 5) Flash memory with system BIOS and programmable user password;
- 6) Operating System, application software, data files on primary HDD;
- 7) An interface device and connectors to peripheral console;
- 8) A software controllable mechanical lock, lock control means, and other accessories.

[0183] The ACM connects to a peripheral console with power supply, a display device, an input device, and other elements. Some details of these elements with the present security system are described in more detail below.

[0184] FIG. 22 is a simplified layout diagram of a security system for a computer system according to an embodiment of the present invention. This diagram is merely an illustration and should not limit the scope of the claims herein. One of ordinary skill in the art would recognize other variations, modifications, and alternatives. The layout diagram illustrates the top-view of the module 22, where the backside components (e.g., Host Interface Controller) are depicted in dashed lines. The layout diagram has a first portion, which includes a central processing unit (“CPU”) module 2200, and a second portion, which includes a hard drive module 2220. A common printed circuit board 2237 houses these modules and the like. Among other features, the ACM includes the central processing unit module 2200 with a cache memory 2205, which is coupled to a north bridge unit 2221, and a host interface controller 2201. The host interface controller includes a lock control 2203. As shown, the CPU module is disposed on a first portion of the attached computer module, and couples to connectors 2217. Here, the CPU module is spatially located near connector 2217.

[0185] The CPU module can use a suitable microprocessing unit, microcontroller, digital signal processor, and the like. In a specific embodiment, the CPU module uses, for example, a 400 MHz Pentium II microprocessor module from Intel Corporation and like microprocessors from AMD Corporation, Cyrix Corporation (now National Semiconductor Corporation), and others. In other aspects, the microprocessor can be one such as the Compaq Computer Corporation Alpha Chip, Apple Computer Corporation PowerPC G3 processor, and the like. Further, higher speed processors are contemplated in other embodiments as technology increases in the future.

[0186] In the CPU module, host interface controller 2201 is coupled to BIOS/flash memory 2205. Additionally, the host interface controller is coupled to a clock control logic, a configuration signal, and a peripheral bus. The present invention has a host interface controller that has lock control 2203 to provide security features to the present ACM. Furthermore, the present invention uses a flash memory that includes codes to provide password protection or other electronic security methods.

[0187] The second portion of the attached computer module has the hard drive module 2220. Among other elements, the hard drive module includes north bridge 2221, graphics accelerator 2223, graphics memory 2225, a power controller 2227, an IDE controller 2229, and other components. Adjacent to and in parallel alignment with the hard drive

module is a personal computer interface ("PCI") bus 2231, 2232. A power regulator 435 is disposed near the PCI bus.

[0188] In a specific embodiment, north bridge unit 2221 often couples to a computer memory, to the graphics accelerator 2223, to the IDE controller, and to the host interface controller via the PCI bus. Graphics accelerator 2223 typically couples to a graphics memory 2223, and other elements. IDE controller 2229 generally supports and provides timing signals necessary for the IDE bus. In the present embodiment, the IDE controller is embodied as a 643U2 PCI-to IDE chip from CMD Technology, for example. Other types of buses than IDE are contemplated, for example EIDE, SCSI, 1394, and the like in alternative embodiments of the present invention.

[0189] The hard drive module or mass storage unit 2220 typically includes a computer operating system, application software program files, data files, and the like. In a specific embodiment, the computer operating system may be the Windows98 operating system from Microsoft Corporation of Redmond Wash. Other operating systems, such as WindowsNT, MacOS8, Unix, and the like are also contemplated in alternative embodiments of the present invention. Further, some typical application software programs can include Office98 by Microsoft Corporation, Corel Perfect Suite by Corel, and others. Hard disk module 2220 includes a hard disk drive. The hard disk drive, however, can also be replaced by removable hard disk drives, read/write CD ROMs, flash memory, floppy disk drives, and the like. A small form factor, for example 2.5", is currently contemplated, however, other form factors, such as PC card, and the like are also contemplated. Mass storage unit 2240 may also support other interfaces than IDE. Among other features, the computer system includes an ACM with security protection. The ACM connects to the console, which has at least the following elements, which should not be limiting.

- 1) Connection to input devices, e.g. keyboard or mouse;
- 2) Connection to display devices, e.g. Monitor;
- 3) Add-on means, e.g. PCI add-on slots;
- 4) Removable storage media subsystem, e.g. Floppy drive, CDROM drive;
- 5) Communication device, e.g. LAN or modem;
- 6) An interface device and connectors to ACM;
- 7) A computer module bay with a notch in the frame for ACM's lock; and

8) Power supply and other accessories.

[0190] As noted, the computer module bay is an opening in a peripheral console that receives the ACM. The computer module bay provides mechanical support and protection to ACM. The module bay also includes, among other elements, a variety of thermal components for heat dissipation, a frame that provides connector alignment, and a lock engagement, which secures the ACM to the console. The bay also has a printed circuit board to mount and mate the connector from the ACM to the console. The connector provides an interface between the ACM and other accessories.

[0191] FIG. 23 is a simplified block diagram 2300 of a security system for a computer module according to an embodiment of the present invention. This diagram is merely an illustration and should not limit the scope of the claims herein. One of ordinary skill in the art would recognize other variations, modifications, and alternatives. The block diagram 2300 has a variety of features such as those noted above, as well as others. In the present diagram, different reference numerals are used to show the operation of the present system.

[0192] The block diagram is an attached computer module 2300. The module 2300 has a central processing unit, which communicates to a north bridge 2341, by way of a CPU bus 2327. The north bridge couples to main memory 2323 via memory bus 2329. The main memory can be any suitable high speed memory device or devices such as dynamic random access memory ("DRAM") integrated circuits and others. The DRAM includes at least 32 Meg. or 64 Meg. and greater of memory, but can also be less depending upon the application. Alternatively, the main memory can be coupled directly with the CPU in some embodiments. The north bridge also couples to a graphics subsystem 2315 via bus 2342. The graphics subsystem can include a graphics accelerator, graphics memory, and other devices. Graphics subsystem transmits a video signal to an interface connector, which couples to a display, for example.

[0193] The attached computer module also includes a primary hard disk drive that serves as a main memory unit for programs and the like. The hard disk can be any suitable drive that has at least 2 GB and greater. As merely an example, the hard disk is a Marathon 2250 (2.25 GB, 2 1/2 inch drive) product made by Seagate Corporation of Scotts Valley, but can be others. The hard disk communicates to the north bridge by way

of a hard disk drive controller and bus lines 2302 and 2331. The hard disk drive controller couples to the north bridge by way of the host PCI bus, which connects bus 2337 to the north bridge. The hard disk includes computer codes that implement a security program according to the present invention. Details of the security program are provided below.

[0194] The attached computer module also has a flash memory device 2305 with a BIOS. The flash memory device 2305 also has codes for a user password that can be stored in the device. The flash memory device generally permits the storage of such password without a substantial use of power, even when disconnected. As merely an example, the flash memory device has at least 4 Meg. or greater of memory, or 16 Meg. or greater of memory. A host interface controller 2307 communicates to the north bridge via bus 2335 and host PCI bus. The host interface controller also has a Lock control 2309, which couples to a lock. The lock is attached to the module and has a manual override to the lock on the host interface controller in some embodiments. Host interface controller 2307 communicates to the console using bus 2311, which couples to connection 2313.

[0195] In a preferred embodiment, the present invention uses a password protection scheme to electronically prevent unauthorized access to the computer module. The present password protection scheme uses a combination of software, which is a portion of the security program, and a user password, which can be stored in the flash memory device 505. By way of the flash memory device, the password does not become erased by way of power failure or the lock. The password is substantially fixed in code, which cannot be easily erased. Should the user desire to change the password, it can readily be changed by erasing the code, which is stored in flash memory and a new code (i.e., password) is written into the flash memory. An example of a flash memory device can include a Intel Flash 28F800F3 series flash, which is available in 8 Mbit and 16 Mbit designs. Other types of flash devices can also be used, however. Details of a password protection method are further explained below by way of the FIGS.

[0196] In a specific embodiment, the present invention also includes a real-time clock 510 in the ACM, but is not limited. The real-time clock can be implemented using a reference oscillator 14.31818 MHz 508 that couples to a real-time clock circuit. The real-time clock circuit can be in the host interface controller. An energy source 506 such as a

battery can be used to keep the real-time clock circuit running even when the ACM has been removed from the console. The real-time clock can be used by a security program to perform a variety of functions. As merely an example, these functions include: (1) fixed time period in which the ACM can be used, e.g., ACM cannot be used at night; (2) programmed ACM to be used after certain date, e.g., high security procedure during owner's vacation or non use period; (3) other uses similar to a programmable time lock. Further details of the present real-time clock are described in the application listed under Ser. No. 09/183,816 noted above.

[0197] In still a further embodiment, the present invention also includes a permanent password or user identification code to identify the computer module. In one embodiment, the permanent password or user code is stored in a flash memory device. Alternatively, the permanent password or user code is stored in the central processing unit. The password or user code can be placed in the device upon manufacture of such device. Alternatively, the password or user code can be placed in the device by a one time programming techniques using, for example, fuses or the like. The present password or user code provides a permanent "finger print" on the device, which is generally hardware. The permanent finger print can be used for identification purposes for allowing the user of the hardware to access the hardware itself, as well as other systems. These other systems include local and wide area networks. Alternatively, the systems can also include one or more servers. The present password and user identification can be quite important for electronic commerce applications and the like. In one or more embodiments, the permanent password or user code can be combined with the password on flash memory for the security program, which is described below in more detail.

[0198] In one aspect of the invention, the user password is programmable. The password can be programmable by way of the security program. The password can be stored in a flash memory device within the ACM. Accordingly, the user of the ACM and the console would need to have the user password in order to access the ACM. In the present aspect, the combination of a security program and user password can provide the user a wide variety of security functions as follows:

- 1) Auto-lock capability when ACM is inserted into CMB;
- 2) Access privilege of program and data;
- 3) Password matching for ACM removal; and

- 4) Automatic HDD lock out if tempering is detected.

[0199] In still a further embodiment, the present invention also includes a method for reading a permanent password or user identification code to identify the computer module. In one embodiment, the permanent password or user code is stored in a flash memory device. Alternatively, the permanent password or user code is stored in the central processing unit. The password or user code can be placed in the device upon manufacture of such device. Alternatively, the password or user code can be placed in the device by a one time programming techniques using, for example, fuses or the like. The present password or user code provides a permanent “finger print” on the device, which is generally hardware. The permanent finger print can be used for identification purposes for allowing the user of the hardware to access the hardware itself, as well as other systems. These other systems include local and wide area networks. Alternatively, the systems can also include one or more servers. The present method allows a third party confirm the user by way of the permanent password or user code. The present password and user identification can be quite important for electronic commerce applications and the like, which verify the user code or password. In one or more embodiments, the permanent password or user code can be combined with the password on flash memory for the security program.

[0200] The above embodiments are described generally in terms of hardware and software. It will be recognized, however, that the functionality of the hardware can be further combined or even separated. The functionality of the software can also be further combined or even separated. Hardware can be replaced, at times, with software. Software can be replaced, at times, with hardware. Accordingly, the present embodiments should not be construed as limiting the scope of the claims here. One of ordinary skill in the art would recognize other variations, modifications, and alternatives.

[0201] While the above is a full description of the specific embodiments, various modifications, alternative constructions and equivalents may be used. Therefore, the above description and illustrations should not be taken as limiting the scope of the present invention which is defined by the appended claims.

WHAT IS CLAIMED IS:

1. A computer system comprising:
 - a console comprising
 - a plurality of coupling sites,
 - a serial communication hub controller, and
 - an enclosure housing the coupling sites and the serial communication hub controller; and
 - a plurality of computer modules coupled to respective ones of the coupling sites, at least one of the computer modules comprising
 - a processing unit,
 - a main memory coupled to the processing unit,
 - a low voltage differential signal (LVDS) channel comprising two sets of unidirectional, multiple serial bit channels to transmit data in opposite directions,
 - a serial controller coupled to the serial communication hub controller, and
 - a first interface controller coupled to the LVDS channel to communicate an encoded serial bit stream of Peripheral Component Interconnect (PCI) bus transaction.
2. The computer system of claim 1, wherein the computer modules are similar in design to each other.
3. The computer system of claim 1, wherein the console further comprises a second interface controller to communicate with the at least one of the computer modules through the LVDS channel.
4. The computer system of claim 1, wherein the console further comprises a hard disk drive coupled to the at least one of the computer modules.
5. A computer system comprising:
 - a console comprising
 - a plurality of coupling sites, and
 - an enclosure housing the coupling sites; and
 - a plurality of computer modules coupled to respective ones of the coupling sites, each of the computer modules comprising

- a processing unit,
- a main memory coupled to the processing unit,
- a low voltage differential signal (LVDS) channel comprising two sets of unidirectional, multiple serial bit channels in opposite directions,
- an Ethernet controller to communicate with an external network, and
- a first interface controller coupled to the LVDS channel to communicate an encoded serial bit stream of Peripheral Component Interconnect (PCI) bus transaction.

6. The computer system of claim 5, wherein the computer modules are similar in design to each other.

7. The computer system of claim 5, wherein the console further comprises a second interface controller to communicate with the first interface controller of at least one of the computer modules through the LVDS channel of the at least one of the computer modules.

8. The computer system of claim 5, wherein the console further comprises an Ethernet hub controller coupled to the Ethernet controller of at least one of the computer modules to communicate with the external network.

9. A computer system comprising:

- a console comprising

- a plurality of coupling sites, each of the coupling sites comprising a slot,
 - a power supply, and
 - an enclosure housing the coupling sites and the power supply; and

- a plurality of computer modules, each of the computer modules coupled to a respective one of the coupling sites through the slot of the respective one of the coupling sites, each of the computer modules comprising

- a processing unit,

- a main memory coupled to the processing unit,

- a low voltage differential signal (LVDS) channel comprising two sets of unidirectional, multiple serial bit channels in opposite directions, and

- an interface controller coupled to the LVDS channel to transmit encoded Peripheral Component Interconnect (PCI) bus transaction data,

wherein the computer modules receive power from the power supply upon coupling to the console.

10. The computer system of claim 9, wherein the computer modules are similar in design to each other.

11. The computer system of claim 9, wherein at least one of the computer modules further comprises an Ethernet controller to communicate with an external network.

12. The computer system of claim 9, wherein the console further comprises a mass storage device that is shared between the computer modules.

13. A computer system comprising:
a console comprising
a plurality of coupling sites,
a power supply,
a low voltage differential signal (LVDS) channel comprising two sets of unidirectional, multiple serial bit channels in opposite directions,
an interface controller coupled to the LVDS channel to communicate an encoded serial bit stream of Peripheral Component Interconnect (PCI) bus transaction, and
an enclosure housing the coupling sites, the power supply, the LVDS channel, and the interface controller; and
a computer module coupled to one of the coupling sites and comprising
a processing unit,
a main memory coupled to the processing unit, and
a mass storage device coupled to the processing unit,
wherein the computer module receives power from the power supply for operation.

14. The computer system of claim 13, wherein the mass storage device comprises a flash memory.

15. The computer system of claim 13, wherein the computer module further comprises a serial controller coupled to the console for data communication.
16. A computer system comprising:
a console comprising
a plurality of coupling sites, each of the coupling sites comprising a connector,
a pair of unidirectional, multiple serial bit, low voltage differential signal (LVDS) channels to transmit encoded Peripheral Component Interconnect (PCI) bus transaction data in opposite directions, and
an enclosure housing the coupling sites and the LVDS channels; and
a computer module coupled to one of the coupling sites through the connector of the one of the coupling sites, the computer module comprising
a processing unit,
a main memory coupled to the processing unit,
a mass storage device comprising a flash memory, and
a serial communication controller,
wherein the serial communication controller is coupled to the console for data communication upon coupling of the computer module to the console.
17. The computer system of claim 16, wherein the data communication of the serial communication controller comprises Universal Serial Bus (USB) communication.
18. The computer system of claim 16, wherein the computer module further comprises a computing environment for a personal computer user.
19. A computer system comprising:
a console comprising
a plurality of coupling sites, at least one of the coupling sites comprising a connector,
a Digital Versatile Disk (DVD) drive,
a first differential signal channel comprising a pair of unidirectional, serial bit channels to transmit data in opposite directions, and

an enclosure housing the coupling sites, the DVD drive, and the first differential signal channel; and

a computer module coupled to the at least one of the coupling sites through the connector, the computer module comprising

a processing unit,

a main memory coupled to the processing unit,

a mass storage device comprising a flash memory,

a second differential signal channel comprising a pair of unidirectional, serial bit channels to transmit data in opposite directions, and

an interface controller coupled to the console through the second differential signal channel and the connector,

wherein the first differential signal channel and the second differential signal channel are coupled to each other upon insertion of the computer module into the console.

20. The computer system of claim 19, wherein the computer module further comprises a computing environment for a personal computer user.

21. The computer system of claim 19, wherein the console further comprises a power supply, and the computer module receives power from the power supply upon insertion of the computer module into the console.

22. A computer system comprising:

a console comprising

a plurality of coupling sites, each of the coupling sites comprising a connector,

a power supply,

an integrated Liquid Crystal Display (LCD),

a first differential signal channel comprising a pair of unidirectional, serial bit channels to transmit data in opposite directions, and

an enclosure housing the coupling sites, the power supply, the LCD, and the first differential signal channel; and

a computer module coupled to one of the coupling sites through the connector of the one of the coupling sites, the computer module comprising

a processing unit,

a main memory coupled to the processing unit,
a mass storage device comprising a flash memory, and
a second differential signal channel comprising a pair of unidirectional,
serial bit channels to transmit data in opposite directions,
wherein the first differential signal channel and the second differential signal
channel are coupled to each other upon insertion of the computer module into the console,
and the computer module is at least partially powered by the power supply for operation.

23. The computer system of claim 22, wherein the computer module further comprises
a computing environment for a personal computer user.

24. The computer system of claim 22, wherein the console further comprises a Digital
Versatile Disk (DVD) drive.

25. A computer system comprising:
a console comprising
a plurality of coupling sites, each of the coupling sites comprising a
connector, and
a first pair of unidirectional, multiple bit, low voltage differential signal
(LVDS) channels to transmit encoded Peripheral Component Interconnect (PCI) bus
transaction as serial data along a pair of directions that are different from each other; and
a computer module coupled to one of the coupling sites through the connector of
the one of the coupling sites, the computer module comprising
a processing unit,
a main memory coupled to the processing unit,
a mass storage device coupled to the processing unit,
a second pair of unidirectional, multiple bit, LVDS channels to transmit
encoded PCI bus transaction as serial data along a pair of directions that are different from
each other, and
an interface controller coupled to the second pair of LVDS channels,
wherein the interface controller is coupled to the console for data communication
upon coupling of the computer module to the console.

26. The computer system of claim 25, wherein the console further comprises a Digital Versatile Disk (DVD) drive.

27. The computer system of claim 25, wherein the computer module further comprises a password mechanism to control access to the computer module.

28. A computer system comprising:
a console comprising
a plurality of coupling sites, each of the coupling sites comprising a slot,
a mass storage device, and
an enclosure housing the coupling sites and the mass storage device; and
a plurality of computer modules, each of the computer modules coupled to a respective one of the coupling sites through the slot of the respective one of the coupling sites, each of the computer modules comprising
a processing unit,
a main memory coupled to the processing unit,
a low voltage differential signal (LVDS) channel comprising two sets of unidirectional, multiple serial bit channels in opposite directions,
a serial communication controller, and
an interface controller coupled to the LVDS channel to transmit encoded Peripheral Component Interconnect (PCI) bus transaction data,
wherein the computer modules are similar in design to each other, and wherein the mass storage device is coupled to the computer modules during operation.

29. The computer system of claim 28, wherein the serial communication controller of at least one of the computer modules is coupled to the console for data communication.

30. The computer system of claim 28, wherein the console further comprises a power supply to supply power to the computer modules.

31. A computer system comprising:
a console comprising
a plurality of coupling sites, each of the coupling sites comprising a slot,
a mass storage device, and

an enclosure housing the coupling sites and the mass storage device; and
a plurality of computer modules, each of the computer modules coupled to a respective one of the coupling sites through the slot of the respective one of the coupling sites, at least one of the computer modules comprising
a processing unit,
a main memory coupled to the processing unit,
a low voltage differential signal (LVDS) channel comprising two sets of unidirectional, multiple serial bit channels in opposite directions,
a serial communication controller, and
an interface controller coupled to the LVDS channel to transmit encoded Peripheral Component Interconnect (PCI) bus transaction data,
wherein the computer modules are similar in design to each other, and wherein the at least one of the computer modules is configured to provide protection against failure of another one of the computer modules.

32. The computer system of claim 31, wherein the serial communication controller of the at least one of the computer modules is coupled to the console for data communication.

33. The computer system of claim 31, wherein the mass storage device is coupled to the computer modules upon insertion of the computer modules into the console.

34. A computer system comprising:
a plurality of coupling sites;
a power supply;
a low voltage differential signal (LVDS) channel associated with at least one of the coupling sites, the LVDS channel comprising two sets of unidirectional, multiple serial bit channels in opposite directions;
a first interface controller associated with the at least one of the coupling sites and coupled to the LVDS channel to communicate an encoded serial bit stream of Peripheral Component Interconnect (PCI) bus transaction; and
a plurality of computer modules coupled to respective ones of the coupling sites, at least one of the computer modules comprising
a processing unit,

a main memory coupled to the processing unit, and
a second interface controller coupled to the first interface controller
through the LVDS channel,
wherein the computer modules receive power from the power supply for
operation.

35. The computer system of claim 34, wherein at least one of the computer modules
further comprises an Ethernet controller to communicate with an external network.

36. The computer system of claim 34, wherein the computer system further comprises
a mass storage device that is shared between the computer modules.

37. A computer system comprising:
a console comprising
a first coupling site,
a second coupling site,
a power supply,
a first low voltage differential signal (LVDS) channel associated with the
first coupling site, the first LVDS channel comprising two sets of unidirectional, multiple
serial bit channels in opposite directions,
a second LVDS channel associated with the second coupling site, the
second LVDS channel comprising two sets of unidirectional, multiple serial bit channels
in opposite directions,
a first interface controller coupled to at least one of the first LVDS channel
and the second LVDS channel to communicate an encoded serial bit stream of Peripheral
Component Interconnect (PCI) bus transaction, and
an enclosure housing the first coupling site, the second coupling site, the
power supply, the first LVDS channel, the second LVDS channel, and the first interface
controller.

38. The computer system of claim 37, further comprising:
a first computer module coupled to the first coupling site; and
a second computer module coupled to the second coupling site,

wherein at least one of the first computer module and the second computer module comprises

- a processing unit,
- a main memory coupled to the processing unit, and
- a second interface controller to communicate with the console through one of the first LVDS channel and the second LVDS channel.

39. The computer system of claim 38, wherein each of the first computer module and the second computer module receives power from the power supply for operation.

40. A computer system comprising:

- a console comprising
 - a coupling site,
 - a power supply,
 - a first low voltage differential signal (LVDS) channel comprising two sets of unidirectional, multiple serial bit channels in opposite directions to communicate an encoded serial bit stream of Peripheral Component Interconnect (PCI) bus transaction,
 - a second differential channel associated with the coupling site, the second differential channel comprising two sets of unidirectional, serial bit channels in opposite directions,
 - a first interface controller coupled to the second differential channel, and
 - an enclosure housing the coupling site, the power supply, the first LVDS channel, the second differential channel, and the first interface controller.

41. The computer system of claim 40, further comprising:

- a computer module coupled to the coupling site,
- wherein the computer module comprises
 - a processing unit,
 - a main memory coupled to the processing unit, and
 - a second interface controller to communicate, via Universal Serial Bus (USB) communication, with the console through the second differential channel.

42. The computer system of claim 41, wherein the computer module receives at least partial power from the power supply of the console for operation upon coupling to the console.

43. The computer system of claim 41, wherein the computer module further comprises a computing environment for a personal computer user.

ABSTRACT

A computer system for multi-processing purposes. The computer system has a console comprising a first coupling site and a second coupling site. Each coupling site comprises a connector. The console is an enclosure that is capable of housing each coupling site. The system also has a plurality of computer modules, where each of the computer modules is coupled to a connector. Each of the computer modules has a processing unit, a main memory coupled to the processing unit, a graphics controller coupled to the processing unit, and a mass storage device coupled to the processing unit. Each of the computer modules is substantially similar in design to each other to provide independent processing of each of the computer modules in the computer system.

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Examiner Initial*	Cite No	Patent Number	Kind Code ¹	Issue Date	Name of Patentee or Applicant of cited Document	Pages, Columns, Lines where Relevant Passages or Relevant Figures Appear		
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1	Chu, Inter Partes Reexamination of US Patent No. 6,718,415, Application/Control No. 95/001,276 filed December 2, 2009, Exhibit B, US Patent No. 6,718,415 File History, 159 pages	☐
2	Chu, Inter Partes Reexamination of US Patent No. 6,718,415, Application/Control No. 95/001,276 filed December 2, 2009, Exhibit C, Patent Owner's Asserted Claim Construction against Hewlett-Packard Company, 15 pages	☐
3	Chu, Inter Partes Reexamination of US Patent No. 6,718,415, Application/Control No. 95/001,276 filed December 2, 2009, Exhibit D, Patent Owner's Asserted Claim Construction against International Business Machines Corporation, 11 pages	☐
4	Chu, Inter Partes Reexamination of US Patent No. 6,718,415, Application/Control No. 95/001,276 filed December 2, 2009, Exhibit E, QuantumNet.com [1997-10-11], [online], [retrieved on 2009-11-16] Retrieved from the Internet Archive (archive.org) using Internet, 16 pages	☐
5	Chu, Inter Partes Reexamination of US Patent No. 6,718,415, Application/Control No. 95/001,276 filed December 2, 2009, Exhibit F, JIChatCom.com [1997-1-4], [online], [retrieved on 2009-12-2] Retrieved from the Internet Archive (archive.org) using Internet, 15 pages	☐
6	Chu, Inter Partes Reexamination of US Patent No. 6,718,415, Application/Control No. 95/001,276 filed December 2, 2009, Exhibit G, Eversys.com [1996-11-4], [online], [retrieved on 2009-11-16] Retrieved from the Internet Archive (archive.org) using Internet, 17 pages	☐
7	Chu, Inter Partes Reexamination of US Patent No. 6,718,415, Application/Control No. 95/001,276 filed December 2, 2009, Exhibit H, Origin2000 Rackmount Owner's Guide [1998-6-15], [online], [retrieved on 2009-11-16] Retrieved from Silicon Graphics, Inc. using Internet <URL:http://techpubs.sgi.com/library/manuals/3000/007-3415-003/pdf/007-3415-003.pdf>, 149 pages	☐
8	Chu, Inter Partes Reexamination of US Patent No. 6,718,415, Application/Control No. 95/001,276 filed December 2, 2009, Exhibit K, Novell Netware 4.11 documentation [1996], [online], [retrieved on 2009-11-16] Retrieved from Novell Inc. using Internet ,URL:http://www.novell.com/documentation/nw4/docui/>, 14 pages	☐
9	Chu, Inter Partes Reexamination of US Patent No. 6,718,415, Application/Control No. 95/001,276 filed December 2, 2009, Exhibit L, Origin and Onyx2 Theory of Operations Manual [1998-6-15], [online], [retrieved on 2009-11-16] Retrieved from Silicon Graphics, Inc. using Internet <URL:http://techpubs.sgi.com/library/manuals/3000/007-3439-002/pdf/007-3439-002.pdf>, 127 pages	☐
10	Chu, Inter Partes Reexamination of US Patent No. 6,718,415, Application/Control No. 95/001,276 filed December 2, 2009, Exhibit M (Part 1), IRIS Failsafe Administrator's Guide [1997-4-6], [online], [retrieved on 2009-11-16] Retrieved from Silicon Graphics Inc. using Internet <URL:http://techpubs.sgi.com/librarymanuals/3000/007-3109-003/pdf/007-3109-003.pdf>, 115 pages	☐
11	Chu, Inter Partes Reexamination of US Patent No. 6,718,415, Application/Control No. 95/001,276 filed December 2, 2009, Exhibit M (Part 2), IRIS Failsafe Administrator's Guide [1997-4-6], [online], [retrieved on 2009-11-16] Retrieved from Silicon Graphics Inc. using Internet <URL:http://techpubs.sgi.com/librarymanuals/3000/007-3109-003/pdf/007-3109-003.pdf>, 101 pages	☐

INFORMATION DISCLOSURE STATEMENT BY APPLICANT (Not for submission under 37 CFR 1.99)	Application Number		
	Filing Date		
	First Named Inventor	William W.Y. Chu	
	Art Unit		
	Examiner Name		
	Attorney Docket Number	ACQI-010/19US 310578-2066	

12	Chu, Inter Partes Reexamination of US Patent No. 6,718,415, Application/Control No. 95/001,276 filed December 2, 2009, Exhibit N, CAPserver Product Guide, 1995, pp.1-16, 19 pages	☐
13	Chu, Inter Partes Reexamination of US Patent No. 6,718,415, Application/Control No. 95/001,276 filed December 2, 2009, Exhibit O, Declaration Under 37 CFR 1.132 of Vincent P. Conroy, 11-24-2009, 3 pages	☐
14	Chu, Inter Partes Reexamination of US Patent No. 6,718,415, Application/Control No. 95/001,276 filed December 2, 2009, Exhibit AA, Claim Charts with respect to QuantumNet for Anticipation and Obviousness, 60 pages	☐
15	Chu, Inter Partes Reexamination of US Patent No. 6,718,415, Application/Control No. 95/001,276 filed December 2, 2009, Exhibit BB, Claim Charts with respect to Chatcom for Anticipation and Obviousness, 51 pages	☐
16	Chu, Inter Partes Reexamination of US Patent No. 6,718,415, Application/Control No. 95/001,276 filed December 2, 2009, Exhibit CC, Claim Charts with respect to Eversys for Anticipation and Obviousness, 51 pages	☐
17	Chu, Inter Partes Reexamination of US Patent No. 6,718,415, Application/Control No. 95/001,276 filed December 2, 2009, Exhibit DD, Claim Chart with respect to the Origin2000 Manual for Obviousness, 36 pages	☐
18	Chu, Inter Partes Reexamination of US Patent No. 6,718,415, Application/Control No. 95/001,276 filed December 2, 2009, Exhibit EE, Claim Chart with respect to Gallagher for Anticipation and Obviousness, 59 pages	☐
19	Chu, Inter Partes Reexamination of US Patent No. 6,718,415, Application/Control No. 95/001,276 filed December 2, 2009, Request for Inter Partes Reexamination, 44 pages	☐

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¹ See Kind Codes of USPTO Patent Documents at www.USPTO.GOV or MPEP 901.04. ² Enter office that issued the document, by the two-letter code (WIPO Standard ST.3). ³ For Japanese patent documents, the indication of the year of the reign of the Emperor must precede the serial number of the patent document. ⁴ Kind of document by the appropriate symbols as indicated on the document under WIPO Standard ST.16 if possible. ⁵ Applicant is to place a check mark here if English language translation is attached.

Electronic Patent Application Fee Transmittal				
Application Number:				
Filing Date:				
Title of Invention:		MULTIPLE MODULE COMPUTER SYSTEM AND METHOD INCLUDING DIFFERENTIAL SIGNAL CHANNEL COMPRISING UNIDIRECTIONAL SERIAL BIT CHANNELS		
First Named Inventor/Applicant Name:		William W.Y. Chu		
Filer:		Cliff Z. Liu/Kathleen Smith		
Attorney Docket Number:		ACQI-010/19US 310578-2066		
Filed as Large Entity				
Utility under 35 USC 111(a) Filing Fees				
Description	Fee Code	Quantity	Amount	Sub-Total in USD(\$)
Basic Filing:				
Utility application filing	1011	1	330	330
Utility Search Fee	1111	1	540	540
Utility Examination Fee	1311	1	220	220
Pages:				
Claims:				
Claims in excess of 20	1202	33	52	1716
Independent claims in excess of 3	1201	4	220	880
Miscellaneous-Filing:				

Description	Fee Code	Quantity	Amount	Sub-Total in USD(\$)
Petition:				
Patent-Appeals-and-Interference:				
Post-Allowance-and-Post-Issuance:				
Extension-of-Time:				
Miscellaneous:				
Total in USD (\$)				3686

Electronic Acknowledgement Receipt	
EFS ID:	9892210
Application Number:	13087912
International Application Number:	
Confirmation Number:	7269
Title of Invention:	MULTIPLE MODULE COMPUTER SYSTEM AND METHOD INCLUDING DIFFERENTIAL SIGNAL CHANNEL COMPRISING UNIDIRECTIONAL SERIAL BIT CHANNELS
First Named Inventor/Applicant Name:	William W.Y. Chu
Customer Number:	58249
Filer:	Cliff Z. Liu/Kathleen Smith
Filer Authorized By:	Cliff Z. Liu
Attorney Docket Number:	ACQI-010/19US 310578-2066
Receipt Date:	15-APR-2011
Filing Date:	
Time Stamp:	16:01:56
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	yes
Payment Type	Deposit Account
Payment was successfully received in RAM	\$ 3686
RAM confirmation Number	2674
Deposit Account	501283
Authorized User	
The Director of the USPTO is hereby authorized to charge indicated fees and credit any overpayment as follows: Charge any Additional Fees required under 37 C.F.R. Section 1.16 (National application filing, search, and examination fees) Charge any Additional Fees required under 37 C.F.R. Section 1.21 (Miscellaneous fees and charges)	

File Listing:					
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Information:					
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	Power of Attorney		4	5	
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	Specification		4	5	
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Electronic Acknowledgement Receipt	
EFS ID:	9892210
Application Number:	13087912
International Application Number:	
Confirmation Number:	7269
Title of Invention:	MULTIPLE MODULE COMPUTER SYSTEM AND METHOD INCLUDING DIFFERENTIAL SIGNAL CHANNEL COMPRISING UNIDIRECTIONAL SERIAL BIT CHANNELS
First Named Inventor/Applicant Name:	William W.Y. Chu
Customer Number:	58249
Filer:	Cliff Z. Liu/Kathleen Smith
Filer Authorized By:	Cliff Z. Liu
Attorney Docket Number:	ACQI-010/19US 310578-2066
Receipt Date:	15-APR-2011
Filing Date:	
Time Stamp:	16:01:56
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	yes
Payment Type	Deposit Account
Payment was successfully received in RAM	\$ 3686
RAM confirmation Number	2674
Deposit Account	501283
Authorized User	
The Director of the USPTO is hereby authorized to charge indicated fees and credit any overpayment as follows: Charge any Additional Fees required under 37 C.F.R. Section 1.16 (National application filing, search, and examination fees) Charge any Additional Fees required under 37 C.F.R. Section 1.21 (Miscellaneous fees and charges)	

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This Acknowledgement Receipt evidences receipt on the noted date by the USPTO of the indicated documents, characterized by the applicant, and including page counts, where applicable. It serves as evidence of receipt similar to a Post Card, as described in MPEP 503. <u>New Applications Under 35 U.S.C. 111</u> If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application. <u>National Stage of an International Application under 35 U.S.C. 371</u> If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course. <u>New International Application Filed with the USPTO as a Receiving Office</u> If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.					

Substitute for form 1449A/PTO INFORMATION DISCLOSURE STATEMENT BY APPLICANT <i>(use as many sheets as necessary)</i>		Complete if Known	
		Application Number	To be assigned
		Filing Date	Herewith
		First Named Inventor	William W.Y. Chu
		Group Art Unit	
Examiner Name			
Sheet	1 of 8	Attorney Docket Number	ACQI-010/19US 310578-2066

U.S. PATENT DOCUMENTS					
Examiner Initials*	Cite No. ¹	Document Number	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear
		Number-Kind Code ² (if known)			
	1.	US-3,996,585	12-07-1976	Hogan	
	2.	US-4,623,964	11-18-1986	Getz et al.	
	3.	US-4,700,362	10-13-1987	Todd et al.	
	4.	US-4,769,764	09-06-1988	Levanon	
	5.	US-4,872,091	10-03-1989	Maniwa et al.	
	6.	US-4,890,282	12-26-1989	Lambert et al.	
	7.	US-4,918,572	04-17-1990	Tarver et al.	
	8.	US-4,939,735	07-03-1990	Fredericks et al.	
	9.	US-5,056,141	10-08-1991	Dyke	
	10.	US-5,086,499	02-04-1992	Mutone	
	11.	US-5,251,097	10-05-1993	Simmons et al.	
	12.	US-5,278,509	01-11-1994	Haynes et al.	
	13.	US-5,278,730	01-11-1994	Kikinis	
	14.	US-5,293,497	03-08-1994	Free	
	15.	US-5,311,397	05-10-1994	Harshberger et al.	
	16.	US-5,317,477	05-31-1994	Gillett	
	17.	US-5,319,771	06-07-1994	Takeda	
	18.	US-5,331,509	07-19-1994	Kikinis	
	19.	US-5,355,391	10-11-1994	Horowitz et al.	
	20.	US-5,428,806	06-27-1995	Pocrass	
	21.	US-5,436,857	07-25-1995	Nelson et al.	
	22.	US-5,463,742	10-31-1995	Kobayashi	
	23.	US-5,539,616	07-23-1996	Kikinis	
	24.	US-5,550,710	08-27-1996	Rahamim et al.	
	25.	US-5,550,861	08-27-1996	Chan et al.	
	26.	US-5,578,940	11-26-1996	Dillon	
	27.	US-5,600,800	02-04-1997	Kikinis et al.	
	28.	US-5,603,044	02-11-1997	Annapareddy et al.	
	29.	US-5,606,717	02-25-1997	Farmwald et al.	
	30.	US-5,608,608	03-04-1997	Flint et al.	
	31.	US-5,630,057	05-13-1997	Hait	
	32.	US-5,638,521	06-10-1997	Buchala et al.	
	33.	US-5,640,302	06-17-1997	Kikinis	
	34.	US-5,659,773	08-19-1997	Huynh et al.	
	35.	US-5,663,661	09-02-1997	Dillon et al.	
	36.	US-5,673,174	09-30-1997	Hamirani	

Examiner Signature		Date Considered	

*EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant. ¹Unique citation designation number (optional). ²See attached Kinds of U.S. Patent Documents. ³Enter Office that issued the document, by the two-letter code (WIPO Standard ST.3). ⁴For Japanese patent documents, the indication of the year of the reign of the Emperor must precede the serial number of the patent document. ⁵Kind of document by the appropriate symbols as indicated on the document under WIPO Standard ST.16 if possible. ⁶Applicant is to place a check mark here if English language Translation is attached. This collection of information is required by 37 CFR 1.97 and 1.98. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 2 hours to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.

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Substitute for form 1449A/PTO INFORMATION DISCLOSURE STATEMENT BY APPLICANT <i>(use as many sheets as necessary)</i>		Complete if Known	
		Application Number	To be assigned
		Filing Date	Herewith
		First Named Inventor	William W. Y. Chu
		Group Art Unit	
Examiner Name			
Sheet	2 of 8	Attorney Docket No.	ACQI-010/19US 310578-2066

U.S. PATENT DOCUMENTS					
Examiner Initials*	Cite No. ¹	Document Number	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear
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	37.	US-5,680,126	10-21-1997	Kikinis	
	38.	US-5,689,654	11-18-1997	Kikinis	
	39.	US-5,774,704	06-30-1998	Williams	
	40.	US-5,721,837	02-24-1998	Kikinis	
	41.	US-5,721,842	02-24-1998	Beasley et al.	
	42.	US-5,745,733	04-28-1998	Robinson	
	43.	US-5,752,080	05-12-1998	Ryan	
	44.	US-5,764,924	06-09-1998	Hong	
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		Group Art Unit	
Examiner Name			
Sheet	3 of 8	Attorney Docket No.	ACQI-010/19US 310578-2066

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		Group Art Unit	
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Sheet	4 of 8	Attorney Docket No.	ACQI-010/19US 310578-2066

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		Filing Date	Herewith
		First Named Inventor	William W.Y. Chu
		Group Art Unit	
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First Named Inventor	William W.Y. Chu
Art Unit	
Examiner Name	
Attorney Docket Number	ACQI-010/19US 310578-2066

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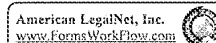
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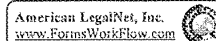
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	BN001	WO 97/00481	01-03-1997	Intel Corporation		

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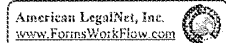
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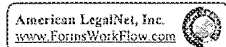
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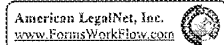
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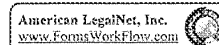
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Application Number	To be assigned
Filing Date	Herewith
First Named Inventor	William W.Y. Chu
Art Unit	
Examiner Name	
Attorney Docket Number	ACQI-010/19US 310578-2066

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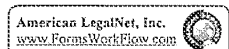
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	C062	PHILLIPS, J., "9800 Disk Card Design Specification," May 26, 1998, White Cross Systems Limited, pages 1-44.	
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First Named Inventor	William W.Y. Chu
Art Unit	
Examiner Name	
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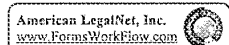
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	C080	MIASKOWSKI, S. (Editor), "A Whale of a System," BYTE, August 1991, 4 pages, Vol. 16, No. 8.	
	C081	Advanced Micro Devices, Inc., "AMD-K6-III Processor Data Sheet," 21918B/0, October 1999, 326 pages.	
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	C089	EVERSYS, "CAPserver Product Brief" [online], [retrieved on 11-16-2009], Retrieved from the Internet: <URL: http://web.archive.org/web/19961104093115/www.eversys.com/CAPbrief.htm >, 10 pages.	
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First Named Inventor	William W.Y. Chu
Art Unit	
Examiner Name	
Attorney Docket Number	ACQI-010/19US 310578-2066

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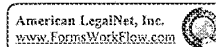
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Attorney Docket Number	ACQI-010/19US 310578-2066

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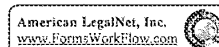
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	C124	ANDERSON, C.R. et al., "IEEE 1355 HS-Links: Present Status and Future Prospects," [online], 1998, [retrieved on 08-11-2010], Retrieved from the Internet: <URL: http://www94.web.cern.ch/HIS/dshs/publications/wotug21/hslink/pdf/hslinkpaper.pdf >, 14 pages.	
	C125	MAMAKOS, L. et al., "Request for Comments 2516 - A method for Transmitting PPP Over Ethernet (PPPoE)," [online], 1999, [retrieved on 08-18-2010], Retrieved from the Internet: <URL: http://tools.ietf.org/html/rfc2516 >, 35 pages.	
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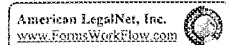
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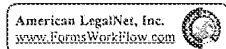
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	CC001	MPL Brochure, "The First Rugged All-in-One Industrial 486FDX-133 MHz PC," IMP486/IPM5 User Manual, 1998, 15 pages.	
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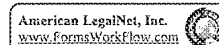
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	DA004	Response for U.S. Patent No. 6,718,415, filed March 6, 2003, 8 pages.	
	DA005	Office Action for U.S. Patent No. 6,718,415, mailed June 4, 2003, 8 pages.	
	DA006	Response for U.S. Patent No. 6,718,415, filed September 4, 2003, 10 pages.	
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	DC002	Response for U.S. Patent No. 7,363,415, filed on April 24, 2007, 25 pages.	
	DD001	Office Action for U.S. Patent No. 7,328,297, mailed February 8, 2007, 5 pages.	
	DD002	Response for U.S. Patent No. 7,328,297, filed April 19, 2007, 32 pages.	
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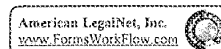
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	EE006	Patent Owner's Response to Office Action in Inter Partes Reexamination of US Patent No. 7,328,297, Control No. 95/001,336, filed October 4, 2010, 49 pages.	
	EE007	Patent Owner's Response to Office Action in Inter Partes Reexamination of US Patent No. 7,328,297, Control No. 95/001,336, Exhibit A, Declaration of William Henry Mangione-Smith under 37 C.F.R. 1.132, filed October 4, 2010, 61 pages.	
	EF001	Request for Inter Partes Reexamination of US Patent No. 7,363,415, Control No. 95/001,424, filed August 25, 2010, 34 pages.	
	EF002	Request for Inter Partes Reexamination of US Patent No. 7,363,415, Control No. 95/001,424, Exhibit AA, Claim Charts with respect to Gallagher and Other References for Obviousness, filed August 25, 2010, 114 pages.	
	EF003	Request for Inter Partes Reexamination of US Patent No. 7,363,415, Control No. 95/001,424, Exhibit AB, Claim Charts with respect to Gallagher and Other References for Obviousness, filed August 25, 2010, 92 pages.	
	EF004	Request for Inter Partes Reexamination of US Patent No. 7,363,415, Control No. 95/001,424, Exhibit BA, Claim Charts with respect to QuantumNet and Other References for Obviousness, filed August 25, 2010, 121 pages.	
	EF005	Request for Inter Partes Reexamination of US Patent No. 7,363,415, Control No. 95/001,424, Exhibit BB, Claim Charts with respect to QuantumNet and Other References for Obviousness, filed August 25, 2010, 99 pages.	
	EF006	Request for Inter Partes Reexamination of US Patent No. 7,363,415, Control No. 95/001,424, Exhibit CA, Claim Charts with respect to Chatcom and Other References for Obviousness, filed August 25, 2010, 91 pages.	
	EF007	Request for Inter Partes Reexamination of US Patent No. 7,363,415, Control No. 95/001,424, Exhibit CB, Claim Charts with respect to Chatcom and Other References for Obviousness, filed August 25, 2010, 94 pages.	
	EF008	Office Action in Inter Partes Reexamination of US Patent No. 7,363,415, Control No. 95/001,424, mailed November 1, 2010, 75 pages.	
	EG001	Request for Inter Partes Reexamination of US Patent No. 7,376,779, Control No. 95/001,475, filed October 27, 2010, 35 pages.	
	EG002	Request for Inter Partes Reexamination of US Patent No. 7,376,779, Control No. 95/001,475, Exhibit AA, Claim Charts with respect to Gallagher and Other References for Obviousness, filed October 27, 2010, 128 pages.	

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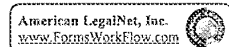
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	EG005	Request for Inter Partes Reexamination of US Patent No. 7,376,779, Control No. 95/001,475, Exhibit BB, Claim Charts with respect to QuantumNet and Other References for Obviousness, filed October 27, 2010, 112 pages.	
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	EG007	Request for Inter Partes Reexamination of US Patent No. 7,376,779, Control No. 95/001,475, Exhibit CB, Claim Charts with respect to Chatcom and Other References for Obviousness, filed October 27, 2010, 118 pages.	
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	EH001	Request for Inter Partes Reexamination of US Patent No. 7,363,416, Control No. 95/001,476, filed October 27, 2010, 37 pages.	
	EH002	Request for Inter Partes Reexamination of US Patent No. 7,363,416, Control No. 95/001,476, Exhibit AA, Claim Charts with respect to Gallagher and Other References for Obviousness, filed October 27, 2010, 70 pages.	
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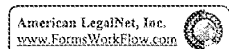
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	EH008	Office Action in Inter Partes Reexamination of US Patent No. 7,363,416, Control No. 95/001,476, mailed December 6, 2010, 63 pages.	
	IC01	"Defendants' Amended Invalidity Contentions," submitted by the Defendants in the U.S. District Court for the Eastern District of Texas, Case No. 6:09-cv-148-LED on March 1, 2010, 18 pages.	
	IC02	"Exhibit A (Asserted Claims)," submitted by the Defendants in the U.S. District Court for the Eastern District of Texas, Case No. 6:09-cv-148-LED on March 1, 2010, 2 pages.	
	IC03	"Exhibit B - Table 1," submitted by the Defendants in the U.S. District Court for the Eastern District of Texas, Case No. 6:09-cv-148-LED on March 1, 2010, 75 pages.	
	IC04	"Exhibit C," submitted by the Defendants in the U.S. District Court for the Eastern District of Texas, Case No. 6:09-cv-148-LED on March 1, 2010, 2 pages.	
	IC05	"Exhibit D," submitted by the Defendants in the U.S. District Court for the Eastern District of Texas, Case No. 6:09-cv-148-LED on March 1, 2010, 106 pages.	
	IC06	"Exhibit E," submitted by the Defendants in the U.S. District Court for the Eastern District of Texas, Case No. 6:09-cv-148-LED on March 1, 2010, 2 pages.	
	IC07	"Invalidity Chart for Base Reference IBM 8260," submitted by the Defendants in the U.S. District Court for the Eastern District of Texas, Case No. 6:09-cv-148-LED on March 1, 2010, 53 pages.	
	IC08	"Invalidity Chart for Base Reference IBM 8265," submitted by the Defendants in the U.S. District Court for the Eastern District of Texas, Case No. 6:09-cv-148-LED on March 1, 2010, 56 pages.	
	IC09	"Invalidity Chart for Base Reference U.S. Patent No. 4,453,215 (Reid)," submitted by the Defendants in the U.S. District Court for the Eastern District of Texas, Case No. 6:09-cv-148-LED on March 1, 2010, 56 pages.	

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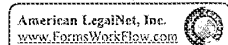
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	IC10	"Invalidity Chart for Base Reference Origin2000," submitted by the Defendants in the U.S. District Court for the Eastern District of Texas, Case No. 6:09-cv-148-LED on March 1, 2010, 56 pages.	
	IC11	"Invalidity Chart for Base Reference QuantumNet," submitted by the Defendants in the U.S. District Court for the Eastern District of Texas, Case No. 6:09-cv-148-LED on March 1, 2010, 49 pages.	
	IC12	"Invalidity Chart for Base Reference U.S. Patent No. 6,564,274 (Heath)," submitted by the Defendants in the U.S. District Court for the Eastern District of Texas, Case No. 6:09-cv-148-LED on March 1, 2010, 57 pages.	
	IC13	"Invalidity Chart for Base Reference U.S. Patent No. 5,577,205," submitted by the Defendants in the U.S. District Court for the Eastern District of Texas, Case No. 6:09-cv-148-LED on March 1, 2010, 60 pages.	
	IC14	"Invalidity Chart for Base Reference U.S. Patent No. 5,802,391," submitted by the Defendants in the U.S. District Court for the Eastern District of Texas, Case No. 6:09-cv-148-LED on March 1, 2010, 61 pages.	
	IC15	"Invalidity Chart for Base Reference U.S. Patent No. 6,715,100," submitted by the Defendants in the U.S. District Court for the Eastern District of Texas, Case No. 6:09-cv-148-LED on March 1, 2010, 64 pages.	
	IC16	"Invalidity Chart for Base Reference Cubix BC/Density," submitted by the Defendants in the U.S. District Court for the Eastern District of Texas, Case No. 6:09-cv-148-LED on March 1, 2010, 64 pages.	
	IC17	"Invalidity Chart for Base Reference JP6-289956," submitted by the Defendants in the U.S. District Court for the Eastern District of Texas, Case No. 6:09-cv-148-LED on March 1, 2010, 62 pages.	
	IC18	"Invalidity Chart for Base Reference Gallagher 068 and Gallagher 503," submitted by the Defendants in the U.S. District Court for the Eastern District of Texas, Case No. 6:09-cv-148-LED on March 1, 2010, 108 pages.	
	IC19	"Invalidity Chart for Base Reference Compaq ProLiant Cluster," submitted by the Defendants in the U.S. District Court for the Eastern District of Texas, Case No. 6:09-cv-148-LED on March 1, 2010, 81 pages.	

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**INFORMATION DISCLOSURE
STATEMENT BY APPLICANT**

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Application Number	To be assigned
Filing Date	Herewith
First Named Inventor	William W.Y. Chu
Art Unit	
Examiner Name	
Attorney Docket Number	ACQI-010/19US 310578-2066

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NON PATENT LITERATURE DOCUMENTS

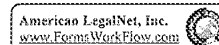
Examiner Initials*	Cite No. ¹	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.	T ²
	IC20	"Invalidity Chart for Base Reference U.S. Patent No. 5,325,517 to Baker et al. (Appendix 1, Exhibit 15)," submitted by the Defendants in the U.S. District Court for the Eastern District of Texas, Case No. 6:09-cv-148-LED on March 1, 2010, 59 pages.	
	IC21	"Invalidity Chart for Japanese Patent Application H7-64672 (Toshiba '672)," submitted by the Defendants in the U.S. District Court for the Eastern District of Texas, Case No. 6:09-cv-148-LED on March 1, 2010, 55 pages.	
	IC22	"Invalidity Chart for Base Reference ChatCom," submitted by the Defendants in the U.S. District Court for the Eastern District of Texas, Case No. 6:09-cv-148-LED on March 1, 2010, 52 pages.	
	IC23	"Invalidity Chart for Base Reference Ziatech Corp. Ketris 9000 System," submitted by the Defendants in the U.S. District Court for the Eastern District of Texas, Case No. 6:09-cv-148-LED on March 1, 2010, 68 pages.	
	IC24	"Invalidity Chart for Base Reference Ziatech STD 32 Star System," submitted by the Defendants in the U.S. District Court for the Eastern District of Texas, Case No. 6:09-cv-148-LED on March 1, 2010, 62 pages.	
	IC25	"Invalidity Chart for Base Reference U.S. Patent No. 7,339,786 (Bottom et al.)," submitted by the Defendants in the U.S. District Court for the Eastern District of Texas, Case No. 6:09-cv-148-LED on March 1, 2010, 57 pages.	
	IC26	"Invalidity Chart for Base References RLX Patents, U.S. Patent Nos. 6,747,878, 6,411,506, 6,325,636, 6,757,748, and 6,985,967 (Hipp et al.)," submitted by the Defendants in the U.S. District Court for the Eastern District of Texas, Case No. 6:09-cv-148-LED on March 1, 2010, 58 pages.	
	IC27	"Invalidity Chart for Base Reference Network Engines P6000 Server," submitted by the Defendants in the U.S. District Court for the Eastern District of Texas, Case No. 6:09-cv-148-LED on March 1, 2010, 59 pages.	
	IC28	"Invalidity Chart for Base Reference Eversys 8000 System," submitted by the Defendants in the U.S. District Court for the Eastern District of Texas, Case No. 6:09-cv-148-LED on March 1, 2010, 60 pages.	
	IC29	"Invalidity Chart for Base Reference Eversys CAPserver," submitted by the Defendants in the U.S. District Court for the Eastern District of Texas, Case No. 6:09-cv-148-LED on March 1, 2010, 59 pages.	

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Application Number	To be assigned
Filing Date	Herewith
First Named Inventor	William W.Y. Chu
Art Unit	
Examiner Name	
Attorney Docket Number	ACQI-010/19US 310578-2066

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of 26

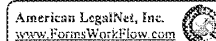
NON PATENT LITERATURE DOCUMENTS

Examiner Initials*	Cite No. ¹	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.	T ²
	IC30	"Invalidity Chart for Base Reference U.S. 5,809,262," submitted by the Defendants in the U.S. District Court for the Eastern District of Texas, Case No. 6:09-cv-148-LED on March 1, 2010, 62 pages.	
	IC31	"Invalidity Chart for Base Reference WhiteCross 9800 System," submitted by the Defendants in the U.S. District Court for the Eastern District of Texas, Case No. 6:09-cv-148-LED on March 1, 2010, 62 pages.	
	IC32	"Invalidity Chart for Base Reference U.S. 5,339,408," submitted by the Defendants in the U.S. District Court for the Eastern District of Texas, Case No. 6:09-cv-148-LED on March 1, 2010, 61 pages.	
	IC33	"Invalidity Chart for Base Reference Tyuluman 536," submitted by the Defendants in the U.S. District Court for the Eastern District of Texas, Case No. 6:09-cv-148-LED on March 1, 2010, 76 pages.	
	IC34	"Invalidity Chart for Base Reference Hong 737," submitted by the Defendants in the U.S. District Court for the Eastern District of Texas, Case No. 6:09-cv-148-LED on March 1, 2010, 77 pages.	
	IC35	"Invalidity Chart for Base Reference U.S. 5,436,857 (Nelson)," submitted by the Defendants in the U.S. District Court for the Eastern District of Texas, Case No. 6:09-cv-148-LED on March 1, 2010, 6 pages.	
	IC36	"Invalidity Chart for Base Reference U.S. 5,999,952 (Jenkins)," submitted by the Defendants in the U.S. District Court for the Eastern District of Texas, Case No. 6:09-cv-148-LED on March 1, 2010, 6 pages.	
	IC37	"Invalidity Chart for Base Reference U.S. 5,608,608 (Flint)," submitted by the Defendants in the U.S. District Court for the Eastern District of Texas, Case No. 6:09-cv-148-LED on March 1, 2010, 6 pages.	
	IC38	"Invalidity Chart for Base Reference U.S. 5,978,821 (Freney)," submitted by the Defendants in the U.S. District Court for the Eastern District of Texas, Case No. 6:09-cv-148-LED on March 1, 2010, 6 pages.	
	IC39	"Invalidity Chart for Base Reference WO 92/18924 (Wallsten)," submitted by the Defendants in the U.S. District Court for the Eastern District of Texas, Case No. 6:09-cv-148-LED on March 1, 2010, 6 pages.	

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Sheet 26

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Application Number	To be assigned
Filing Date	Herewith
First Named Inventor	William W.Y. Chu
Art Unit	
Examiner Name	
Attorney Docket Number	ACQI-010/19US 310578-2066

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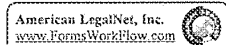
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	IC40	"Invalidity Chart for Base Reference Ergo Moby Brick", submitted by the Defendants in the U.S. District Court for the Eastern District of Texas, Case No. 6:09-cv-148-LED on March 1, 2010, 5 pages.	
	IC41	"Invalidity Chart for Base Reference U.S. Patent No. 5,463,742 (Kobayashi)", submitted by the Defendants in the U.S. District Court for the Eastern District of Texas, Case No. 6:09-cv-148-LED on March 1, 2010, 5 pages.	
	IC42	"Invalidity Chart for Base Reference Japanese Patent Application Publication H6-289953 (Hitachi)", submitted by the Defendants in the U.S. District Court for the Eastern District of Texas, Case No. 6:09-cv-148-LED on March 1, 2010, 5 pages.	
	IC43	"Invalidity Chart for Base Reference Japanese Patent Application Publication H7-84675 (Hitachi)", submitted by the Defendants in the U.S. District Court for the Eastern District of Texas, Case No. 6:09-cv-148-LED on March 1, 2010, 5 pages.	
	IC44	"Invalidity Chart for Base Reference U.S. Patent No. 5,187,645 (Spalding)", submitted by the Defendants in the U.S. District Court for the Eastern District of Texas, Case No. 6:09-cv-148-LED on March 1, 2010, 6 pages.	
	IC45	"Defendants' Notice of Errata Relating to Defendants' P.R. 3-3 Invalidity Contentions," submitted by the Defendants in the U.S. District Court for the Eastern District of Texas, Case No. 6:09-cv-148-LED on March 1, 2010, 14 pages.	
	IF01	"Exhibit 5 - Disclosure of Asserted Claims and Infringement Contentions", submitted by the Plaintiff in the U.S. District Court for the Eastern District of Texas, Case No. 6:09-cv-148-LED, 14 pages.	
	F01	"Memorandum Opinion and Order Construing Claim Terms and Denying Defendants' Motion for Partial Summary Judgment," Issued by the U.S. District Court for the Eastern District of Texas, Case No. 6:09-cv-148-LED on August 2, 2010, 18 pages.	
	H01	"Transcript of Videotaped Deposition of William Mangione-Smith," taken by the Defendants in connection with Case No. 6:09-cv-148-LED in the U.S. District Court for the Eastern District of Texas, September 9, 2010, 192 pages.	

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Electronic Acknowledgement Receipt	
EFS ID:	9893840
Application Number:	13087912
International Application Number:	
Confirmation Number:	7269
Title of Invention:	MULTIPLE MODULE COMPUTER SYSTEM AND METHOD INCLUDING DIFFERENTIAL SIGNAL CHANNEL COMPRISING UNIDIRECTIONAL SERIAL BIT CHANNELS
First Named Inventor/Applicant Name:	William W.Y. Chu
Customer Number:	58249
Filer:	Cliff Z. Liu/Kathleen Smith
Filer Authorized By:	Cliff Z. Liu
Attorney Docket Number:	ACQI-010/19US 310578-2066
Receipt Date:	15-APR-2011
Filing Date:	
Time Stamp:	17:37:38
Application Type:	Utility under 35 USC 111(a)

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Filing Date	Herewith
First Named Inventor	William W.Y. Chu
Art Unit	
Examiner Name	
Attorney Docket Number	ACQI-010/19US 310578-2066

Sheet 14

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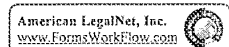
Examiner Initials*	Cite No. ¹	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.	T ²
	DF001	Office Action for U.S. Patent No. 7,363,416, mailed April 12, 2007, 23 pages.	
	DF002	Response for U.S. Patent No. 7,363,416, filed April 24, 2007, 23 pages.	
	DG001	Office Action for U.S. Patent No. 7,376,779, mailed September 28, 2007, 24 pages.	
	DG002	Response for U.S. Patent No. 7,376,779, filed October 16, 2007, 23 pages.	
	DH001	Office Action for U.S. Patent No. 7,676,624, mailed December 1, 2008, 8 pages.	
	DH002	Response for U.S. Patent No. 7,676,624, filed January 13, 2009, 14 pages.	
	DH003	Supplemental Response for U.S. Patent No. 7,676,624, filed on February 6, 2009, 13 pages.	
	DI001	Office Action for U.S. Patent No. 7,818,487, mailed September 29, 2009, 10 pages.	
	DI002	Response for U.S. Patent No. 7,818,487, filed November 6, 2009, 3 pages.	
	DI003	Amendment for U.S. Patent No. 7,818,487, filed May 11, 2010, 15 pages.	
	DI004	Amendment Submitted After Notice of Allowance for U.S. Patent No. 7,818,487, filed August 17, 2010, 14 pages.	
	DJ001	Office Action for U.S. Publication No. 2010/0174844, mailed October 28, 2010, 11 pages.	
	DK001	Office Action for U.S. Patent No. 6,216,185, mailed April 12, 2000, 9 pages.	
	DK002	Response for U.S. Patent No. 6,216,185, filed August 3, 2000, 15 pages.	
	DK003	Office Action for U.S. Patent No. 6,216,185, mailed August 25, 2000, 9 pages.	
	DK004	Response for U.S. Patent No. 6,216,185, filed October 24, 2000, 10 pages.	
	DL001	Office Action for U.S. Patent No. 6,345,330, mailed June 15, 2000, 7 pages.	
	DL002	Amendment for U.S. Patent No. 6,345,330, filed September 12, 2000, 5 pages.	
	DL003	Restriction Requirement for U.S. Patent No. 6,345,330, mailed December 19, 2000, 5 pages.	
	DL004	Amendment filed with Continued Prosecution Application for U.S. Patent No. 6,345,330, filed January 17, 2001, 5 pages.	
	DL005	Office Action for U.S. Patent No. 6,345,330, mailed March 23, 2001, 6 pages.	
	DL006	Response to Office Action for U.S. Patent No. 6,345,330, filed July 19, 2001, 5 pages.	
	DM001	Office Action for U.S. Patent Application No. 09/642,628, mailed April 5, 2001, 9 pages.	
	DO001	Office Action for U.S. Application No. 10/963,825, mailed October 27, 2005, 25 pages.	
	DO002	Response for U.S. Application No. 10/963,825, filed January 9, 2006, 22 pages.	
	DO003	Office Action for U.S. Application No. 10/963,825, mailed May 31, 2006, 29 pages.	
	DO004	Amendment Submitted with RCE for U.S. Application No. 10/963,825, filed July 27, 2006, 29 pages.	
	DO005	Office Action for U.S. Application No. 10/963,825, mailed October 20, 2006, 28 pages.	

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Examiner Name	
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Sheet 15

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Examiner Initials*	Cite No. ¹	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.	T ²
	DO006	Appellants' Brief for U.S. Application No. 10/963,825, filed January 8, 2007, 31 pages.	
	DO007	Revised Appellants' Brief for U.S. Application No. 10/963,825, filed April 20, 2007, 34 pages.	
	DO008	Examiner's Answer for U.S. Application No. 10/963,825, mailed August 8, 2007, 30 pages.	
	DO009	Reply Brief for U.S. Application No. 10/963,825, filed September 4, 2007, 4 pages.	
	DO010	Decision on Appeal for U.S. Application No. 10/963,825, mailed February 4, 2009, 13 pages.	
	DO011	Amendment Submitted with RCE for U.S. Application No. 10/963,825, filed February 20, 2009, 24 pages.	
	DO012	Office Action for U.S. Application No. 10/963,825, mailed May 14, 2009, 5 pages.	
	DO013	Response for U.S. Application No. 10/963,825, filed May 22, 2009, 2 pages.	
	DO014	Office Action for U.S. Application No. 10/963,825, mailed September 15, 2009, 14 pages.	
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	DP005	Supplemental Amendment Submitted with RCE for RE 41,294, filed July 8, 2008, 12 pages.	
	DP006	Office Action for RE 41,294, mailed September 16, 2008, 11 pages.	
	DP007	Response for RE 41,294, filed October 30, 2008, 14 pages.	
	DP008	Supplemental Response for RE 41,294, filed February 20, 2009, 13 pages.	
	DP009	Supplemental Response for RE 41,294, filed August 17, 2009, 3 pages.	
	DP010	Examiner Interview Summary Record, mailed January 15, 2009, 1 page.	
	DQ001	Office Action for RE 41,076, mailed July 13, 2007, 38 pages.	
	DQ002	Response for RE 41,076, filed September 26, 2007, 18 pages.	
	DQ003	Office Action for RE 41,076, mailed October 17, 2007, 55 pages.	
	DQ004	Amendment Submitted with RCE for RE 41,076, filed November 5, 2007, 19 pages.	
	DQ005	Office Action for RE 41,076, mailed February 11, 2008, 62 pages.	
	DQ006	Response for RE 41,076, filed April 7, 2008, 18 pages.	
	DQ007	Office Action for RE 41,076, mailed June 9, 2008, 25 pages.	
	DQ008	Amendment Submitted with RCE for RE 41,076, filed December 8, 2008, 44 pages.	
	DQ009	Office Action for RE 41,076, mailed December 30, 2008, 8 pages.	
	DQ010	Response for RE 41,076, filed January 16, 2009, 14 pages.	

Examiner
SignatureDate
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EX2001 - 00178

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**INFORMATION DISCLOSURE
STATEMENT BY APPLICANT**

(Use as many sheets as necessary)

Complete if Known

Application Number	To be assigned
Filing Date	Herewith
First Named Inventor	William W.Y. Chu
Art Unit	
Examiner Name	
Attorney Docket Number	ACQI-010/19US 310578-2066

Sheet 16

of 26

NON PATENT LITERATURE DOCUMENTS

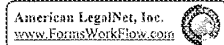
Examiner Initials*	Cite No. ¹	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.	T ²
	DQ011	Amendment Submitted with RCE for RE 41,076, filed August 4, 2009, 2 pages.	
	DQ012	Examiner Interview Summary Record, mailed February 24, 2009, 4 pages.	
	DQ013	Applicant Summary of Interview, filed March 24, 2009, 1 page.	
	DQ014	Examiner Interview Summary Record, mailed September 22, 2009, 5 pages.	
	DR001	Office Action for U.S. Application No. 12/322,858, mailed March 4, 2010, 24 pages.	
	DR002	Response for U.S. Application No. 12/322,858, filed June 4, 2010, 15 pages.	
	DR003	Office Action for U.S. Application No. 12/322,858, mailed June 25, 2010, 22 pages.	
	DR004	Response for U.S. Application No. 12/322,858, filed October 25, 2010, 12 pages.	
	DS001	Office Action for U.S. Application No. 12/577,074, mailed April 13, 2010, 7 pages.	
	DS002	Response for U.S. Application No. 12/577,074, filed July 13, 2010, 3 pages.	
	DS003	Office Action for U.S. Application No. 12/577,074, mailed November 10, 2010, 6 pages.	
	DT001	Office Action for U.S. Application No. 09/312,199, mailed March 26, 2003, 5 pages.	
	DT002	Response for U.S. Application No. 09/312,199, filed June 11, 2003, 5 pages.	
	DU001	Office Action for RE 41,092, mailed September 17, 2008, 8 pages.	
	DU002	Response for RE 41,092, filed October 27, 2008, 27 pages.	
	DU003	Examiner's Amendment for RE 41,092, mailed November 4, 2009, 4 pages.	
	DV001	Office Action for U.S. Application No. 11/545,056, mailed March 12, 2010, 26 pages.	
	DV002	Response for U.S. Application No. 11/545,056, filed June 14, 2010, 18 pages.	
	DW001	Office Action for U.S. Application No. 12/561,138, mailed September 29, 2010, 4 pages.	
	EA001	Request for Ex Parte Reexamination of US Patent No. 6,216,185, Control No. 90/010,816, filed January 8, 2010, 39 pages.	
	EA002	Request for Ex Parte Reexamination of US Patent No. 6,216,185, Control No. 90/010,816, filed January 8, 2010, Exhibit AA to Request Claim Charts with respect to the Hitachi '953 for Anticipation and Obviousness, 136 pages	
	EA003	Request for Ex Parte Reexamination of US Patent No. 6,216,185, Control No. 90/010,816, filed January 8, 2010, Exhibit BB Claim Charts with respect to Kobayashi for Anticipation and Obviousness, 128 pages	
	EA004	Request for Ex Parte Reexamination of US Patent No. 6,216,185, Control No. 90/010,816, filed January 8, 2010, Exhibit CC Claim Charts with respect to Byte for Anticipation and Obviousness, 122 pages	

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SignatureDate
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**INFORMATION DISCLOSURE
STATEMENT BY APPLICANT**

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Complete if Known

Application Number	To be assigned
Filing Date	Herewith
First Named Inventor	William W.Y. Chu
Art Unit	
Examiner Name	
Attorney Docket Number	ACQI-010/19US 310578-2066

Sheet 17

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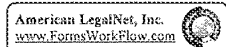
Examiner Initials*	Cite No. ¹	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.	T ²
	EA005	Request for Ex Parte Reexamination of US Patent No. 6,216,185, Control No. 90/010,816, filed January 8, 2010, Exhibit DD Claim Charts with respect to the Hitachi '675 for Anticipation and Obviousness, 119 pages	
	EA006	Office Action in Ex Parte Reexamination of US Patent No. 6,216,185, Control No. 90/010,816, mailed July 27, 2010, 103 pages	
	EA007	Patent Owner's Response to Office Action in Ex Parte Reexamination of US Patent No. 6,216,185, Control No. 90/010,816, filed September 27, 2010, 55 pages	
	EB001	Request for Inter Partes Reexamination of US Patent No. 6,718,415, Control No. 95/001,276, filed December 2, 2009, 44 pages.	
	EB002	Request for Inter Partes Reexamination of US Patent No. 6,718,415, Control No. 95/001,276, filed December 2, 2009, Exhibit O, Declaration Under 37 CFR 1.132 of Vincent P. Conroy, 11-24-2009, 3 pages.	
	EB003	Request for Inter Partes Reexamination of US Patent No. 6,718,415, Control No. 95/001,276, Replacement Exhibit AA, Claim Charts with respect to QuantumNet for Anticipation and Obviousness, filed January 5, 2010, 109 pages.	
	EB004	Request for Inter Partes Reexamination of US Patent No. 6,718,415, Control No. 95/001,276, Replacement Exhibit BB, Claim Charts with respect to Chatcom for Anticipation and Obviousness, filed January 5, 2010, 91 pages.	
	EB005	Request for Inter Partes Reexamination of US Patent No. 6,718,415, Control No. 95/001,276, Replacement Exhibit CC, Claim Charts with respect to QuantumNet for Anticipation and Obviousness, filed January 5, 2010, 85 pages.	
	EB006	Request for Inter Partes Reexamination of US Patent No. 6,718,415, Control No. 95/001,276, Replacement Exhibit DD, Claim Charts with respect to the Origin2000 Manual for Obviousness, filed January 5, 2010, 72 pages.	
	EB007	Request for Inter Partes Reexamination of US Patent No. 6,718,415, Control No. 95/001,276, Replacement Exhibit EE, Claim Charts with respect to Gallagher for Anticipation and Obviousness, filed January 5, 2010, 107 pages.	
	EB008	Office Action in Inter Partes Reexamination of US Patent No. 6,718,415, Control No. 95/001,276, mailed May 26, 2010, 39 pages.	
	EB009	Patent Owner's Response to Office Action in Inter Partes Reexamination of US Patent No. 6,718,415, Control No. 95/001,276, filed July 27, 2010, 41 pages.	

Examiner Signature	Date Considered

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STATEMENT BY APPLICANT**

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Application Number	To be assigned
Filing Date	Herewith
First Named Inventor	William W.Y. Chu
Art Unit	
Examiner Name	
Attorney Docket Number	ACQI-010/19US 310578-2066

Sheet 18

of 26

NON PATENT LITERATURE DOCUMENTS

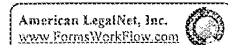
Examiner Initials*	Cite No. ¹	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.	T ²
	EB010	Patent Owner's Response to Office Action in Inter Partes Reexamination of US Patent No. 6,718,415, Control No. 95/001,276, Exhibit A, Declaration of William Henry Mangione-Smith under 37 C.F.R. 1.132, filed July 27, 2010, 29 pages.	
	EC001	Request for Inter Partes Reexamination of US Patent No. 7,099,981, Control No. 95/001,310, filed February 9, 2010, 33 pages	
	EC002	Request for Inter Partes Reexamination of US Patent No. 7,099,981, Control No. 95/001,310, filed December 2, 2009, Exhibit O, Declaration Under 37 CFR 1.132 of Vincent P. Conroy, 11-24-2009, 3 pages.	
	EC003	Request for Inter Partes Reexamination of US Patent No. 7,099,981, Control No. 95/001,310, Exhibit AA, Claim Charts with respect to Gallagher for Anticipation and Obviousness, filed February 9, 2010, 164 pages	
	EC004	Request for Inter Partes Reexamination of US Patent No. 7,099,981, Control No. 95/001,310, Exhibit BB, Claim Charts with respect to QuantumNet for Anticipation and Obviousness, filed February 9, 2010, 158 pages	
	EC005	Request for Inter Partes Reexamination of US Patent No. 7,099,981, Control No. 95/001,310, Exhibit CC, Claim Charts with respect to Chatcom for Anticipation and Obviousness, filed February 9, 2010, 167 pages	
	EC006	Request for Inter Partes Reexamination of US Patent No. 7,099,981, Control No. 95/001,310, Exhibit DD, Claim Charts with respect to the Eversys for Obviousness, filed February 9, 2010, 111 pages	
	EC007	Office Action in Inter Partes Reexamination of US Patent No. 7,099,981, Control No. 95/001,310, mailed July 6, 2010, 83 pages	
	EC008	Patent Owner's Response to Office Action in Inter Partes Reexamination of US Patent No. 7,099,981, Control No. 95/001,310, filed September 3, 2010, 52 pages	
	EC009	Patent Owner's Response to Office Action in Inter Partes Reexamination of US Patent No. 7,099,981, Control No. 95/001,310, Exhibit A, Declaration of William Henry Mangione-Smith under 37 C.F.R. 1.132, filed September 3, 2010, 63 pages	
	ED001	Request for Inter Partes Reexamination of US Patent No. 7,146,446, Control No. 95/001,328, filed March 19, 2010, 35 pages.	
	ED002	Request for Inter Partes Reexamination of US Patent No. 7,146,446, Control No. 95/001,328, Exhibit AA (Part 1), Claim Charts with respect to Gallagher for Anticipation and Obviousness, filed March 19, 2010, 186 pages.	

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Intel Corp. v. ACQIS LLC
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STATEMENT BY APPLICANT**

(Use as many sheets as necessary)

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Application Number	To be assigned
Filing Date	Herewith
First Named Inventor	William W.Y. Chu
Art Unit	
Examiner Name	
Attorney Docket Number	ACQI-010/19US 310578-2066

Sheet 19

of 26

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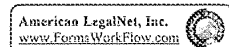
Examiner Initials*	Cite No. ¹	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.	T ²
	ED003	Request for Inter Partes Reexamination of US Patent No. 7,146,446, Control No. 95/001,328, Exhibit AA (Part 2), Claim Charts with respect to Gallagher for Anticipation and Obviousness, filed March 19, 2010, 161 pages.	
	ED004	Request for Inter Partes Reexamination of US Patent No. 7,146,446, Control No. 95/001,328, Exhibit BB (Part 1), Claim Charts with respect to QuantumNet for Anticipation and Obviousness, filed March 19, 2010, 139 pages.	
	ED005	Request for Inter Partes Reexamination of US Patent No. 7,146,446, Control No. 95/001,328, Exhibit BB (Part 2), Claim Charts with respect to QuantumNet for Anticipation and Obviousness, filed March 19, 2010, 128 pages.	
	ED006	Request for Inter Partes Reexamination of US Patent No. 7,146,446, Control No. 95/001,328, Exhibit CC, Claim Charts with respect to Chatcom for Anticipation and Obviousness, filed March 19, 2010, 68 pages.	
	ED007	Office Action in Inter Partes Reexamination of US Patent No. 7,146,446, Control No. 95/001,328, mailed June 24, 2010, 86 pages.	
	ED008	Patent Owner's Response to Office Action in Inter Partes Reexamination of US Patent No. 7,146,446, Control No. 95/001,328, filed August 24, 2010, 45 pages.	
	ED009	Patent Owner's Response to Office Action in Inter Partes Reexamination of US Patent No. 7,146,446, Control No. 95/001,328, Exhibit A, Declaration of William Henry Mangione-Smith under 37 C.F.R. 1.132, filed September 3, 2010, 61 pages.	
	EE001	Request for Inter Partes Reexamination of US Patent No. 7,328,297, Control No. 95/001,336, filed April 19, 2010, 33 pages.	
	EE002	Request for Inter Partes Reexamination of US Patent No. 7,328,297, Control No. 95/001,336, Exhibit AA, Claim Charts with respect to Gallagher for Obviousness, filed April 19, 2010, 131 pages.	
	EE003	Request for Inter Partes Reexamination of US Patent No. 7,328,297, Control No. 95/001,336, Exhibit BB, Claim Charts with respect to QuantumNet for Obviousness, filed April 19, 2010, 139 pages.	
	EE004	Request for Inter Partes Reexamination of US Patent No. 7,328,297, Control No. 95/001,336, Exhibit CC, Claim Charts with respect to Chatcom for Obviousness, filed April 19, 2010, 114 pages.	
	EE005	Office Action in Inter Partes Reexamination of US Patent No. 7,328,297, Control No. 95/001,336, mailed August 4, 2010, 95 pages.	

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PATENT APPLICATION FEE DETERMINATION RECORD Substitute for Form PTO-875					Application or Docket Number 13/087,912		Filing Date 04/15/2011		☐ To be Mailed		
APPLICATION AS FILED – PART I											
(Column 1)			(Column 2)			SMALL ENTITY ☐ OR		OTHER THAN SMALL ENTITY			
FOR	NUMBER FILED	NUMBER EXTRA	RATE (\$)	FEE (\$)	OR		RATE (\$)	FEE (\$)			
☐ BASIC FEE (37 CFR 1.16(a), (b), or (c))	N/A	N/A	N/A				N/A				
☐ SEARCH FEE (37 CFR 1.16(k), (l), or (m))	N/A	N/A	N/A				N/A				
☐ EXAMINATION FEE (37 CFR 1.16(o), (p), or (q))	N/A	N/A	N/A				N/A				
TOTAL CLAIMS (37 CFR 1.16(i))	minus 20 =	*	X \$ =				X \$ =				
INDEPENDENT CLAIMS (37 CFR 1.16(h))	minus 3 =	*	X \$ =				X \$ =				
☐ APPLICATION SIZE FEE (37 CFR 1.16(s)) If the specification and drawings exceed 100 sheets of paper, the application size fee due is \$250 (\$125 for small entity) for each additional 50 sheets or fraction thereof. See 35 U.S.C. 41(a)(1)(G) and 37 CFR 1.16(s).											
☐ MULTIPLE DEPENDENT CLAIM PRESENT (37 CFR 1.16(j))											
* If the difference in column 1 is less than zero, enter "0" in column 2.											
APPLICATION AS AMENDED – PART II											
(Column 1)			(Column 2)			(Column 3)		SMALL ENTITY OR		OTHER THAN SMALL ENTITY	
AMENDMENT	04/15/2011	CLAIMS REMAINING AFTER AMENDMENT		HIGHEST NUMBER PREVIOUSLY PAID FOR	PRESENT EXTRA	RATE (\$)	ADDITIONAL FEE (\$)		RATE (\$)	ADDITIONAL FEE (\$)	
	Total (37 CFR 1.16(i))	* 53	Minus	** 53	= 0	X \$ =		OR	X \$52=	0	
	Independent (37 CFR 1.16(h))	* 7	Minus	*** 7	= 0	X \$ =		OR	X \$220=	0	
	☐ Application Size Fee (37 CFR 1.16(s))										
	☐ FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))										
						TOTAL ADD'L FEE		OR	TOTAL ADD'L FEE	0	
AMENDMENT		CLAIMS REMAINING AFTER AMENDMENT		HIGHEST NUMBER PREVIOUSLY PAID FOR	PRESENT EXTRA	RATE (\$)	ADDITIONAL FEE (\$)		RATE (\$)	ADDITIONAL FEE (\$)	
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	Independent (37 CFR 1.16(h))	*	Minus	***	=	X \$ =		OR	X \$ =		
	☐ Application Size Fee (37 CFR 1.16(s))										
	☐ FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))										
						TOTAL ADD'L FEE		OR	TOTAL ADD'L FEE		
* If the entry in column 1 is less than the entry in column 2, write "0" in column 3. ** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 20, enter "20". *** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 3, enter "3". The "Highest Number Previously Paid For" (Total or Independent) is the highest number found in the appropriate box in column 1.											

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APPLICATION NUMBER	FILING OR 371(C) DATE	FIRST NAMED APPLICANT	ATTY. DOCKET NO./TITLE
13/087,912	04/15/2011	William W.Y. Chu	ACQI-010/19US 310578-2066

CONFIRMATION NO. 7269

58249
COOLEY LLP
ATTN: Patent Group
Suite 1100
777 - 6th Street, NW
WASHINGTON, DC 20001

FORMALITIES LETTER



Date Mailed: 04/28/2011

NOTICE TO FILE CORRECTED APPLICATION PAPERS

Filing Date Granted

An application number and filing date have been accorded to this application. The application is informal since it does not comply with the regulations for the reason(s) indicated below. Applicant is given TWO MONTHS from the date of this Notice within which to correct the informalities indicated below. Extensions of time may be obtained by filing a petition accompanied by the extension fee under the provisions of 37 CFR 1.136(a).

The required item(s) identified below must be timely submitted to avoid abandonment:

- A substitute specification excluding claims in compliance with 37 CFR 1.52, 1.121(b)(3), and 1.125 is required. The substitute specification must be submitted with markings and be accompanied by a clean version (without markings) as set forth in 37 CFR 1.125(c) and a statement that the substitute specification contains no new matter (see 37 CFR 1.125(b)). Since a preliminary amendment was present on the filing date of the application and such amendment is part of the original disclosure of the application, the substitute specification must include all of the desired changes made in the preliminary amendment. See 37 CFR 1.115 and 1.215.

Applicant is cautioned that correction of the above items may cause the specification and drawings page count to exceed 100 pages. If the specification and drawings exceed 100 pages, applicant will need to submit the required application size fee.

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Office of Data Management, Application Assistance Unit (571) 272-4000, or (571) 272-4200, or 1-888-786-0101

PATENT APPLICATION FEE DETERMINATION RECORD Substitute for Form PTO-875						Application or Docket Number 13/087,912	
APPLICATION AS FILED - PART I							
(Column 1)		(Column 2)		SMALL ENTITY		OR OTHER THAN SMALL ENTITY	
FOR	NUMBER FILED	NUMBER EXTRA	RATE(\$)	FEE(\$)		RATE(\$)	FEE(\$)
BASIC FEE (37 CFR 1.16(a), (b), or (c))	N/A	N/A	N/A			N/A	330
SEARCH FEE (37 CFR 1.16(k), (i), or (m))	N/A	N/A	N/A			N/A	540
EXAMINATION FEE (37 CFR 1.16(o), (p), or (q))	N/A	N/A	N/A			N/A	220
TOTAL CLAIMS (37 CFR 1.16(i))	53	minus 20 = *	33			x 52 =	1716
INDEPENDENT CLAIMS (37 CFR 1.16(h))	7	minus 3 = *	4			x 220 =	880
APPLICATION SIZE FEE (37 CFR 1.16(s))	If the specification and drawings exceed 100 sheets of paper, the application size fee due is \$270 (\$135 for small entity) for each additional 50 sheets or fraction thereof. See 35 U.S.C. 41(a)(1)(G) and 37 CFR 1.16(s).						0.00
MULTIPLE DEPENDENT CLAIM PRESENT (37 CFR 1.16(j))							0.00
* If the difference in column 1 is less than zero, enter "0" in column 2.				TOTAL		TOTAL	3686
APPLICATION AS AMENDED - PART II							
AMENDMENT A	(Column 1)	(Column 2)	(Column 3)	SMALL ENTITY		OR OTHER THAN SMALL ENTITY	
	CLAIMS REMAINING AFTER AMENDMENT	HIGHEST NUMBER PREVIOUSLY PAID FOR	PRESENT EXTRA	RATE(\$)	ADDITIONAL FEE(\$)	RATE(\$)	ADDITIONAL FEE(\$)
	Total (37 CFR 1.16(i))	*	Minus **	x	=	x	=
	Independent (37 CFR 1.16(h))	*	Minus ***	x	=	x	=
	Application Size Fee (37 CFR 1.16(s))						
	FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))						
			TOTAL ADD'L FEE		TOTAL ADD'L FEE		
AMENDMENT B	(Column 1)	(Column 2)	(Column 3)	SMALL ENTITY		OR OTHER THAN SMALL ENTITY	
	CLAIMS REMAINING AFTER AMENDMENT	HIGHEST NUMBER PREVIOUSLY PAID FOR	PRESENT EXTRA	RATE(\$)	ADDITIONAL FEE(\$)	RATE(\$)	ADDITIONAL FEE(\$)
	Total (37 CFR 1.16(i))	*	Minus **	x	=	x	=
	Independent (37 CFR 1.16(h))	*	Minus ***	x	=	x	=
	Application Size Fee (37 CFR 1.16(s))						
	FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))						
			TOTAL ADD'L FEE		TOTAL ADD'L FEE		
* If the entry in column 1 is less than the entry in column 2, write "0" in column 3. ** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 20, enter "20". *** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 3, enter "3". The "Highest Number Previously Paid For" (Total or Independent) is the highest found in the appropriate box in column 1.							



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APPLICATION NUMBER	FILING or 371(c) DATE	GRP ART UNIT	FIL FEE REC'D	ATTY. DOCKET NO	TOT CLAIMS	IND CLAIMS
13/087,912	04/15/2011	2111	3686	ACQI-010/19US 310578-2066	53	7

CONFIRMATION NO. 7269

FILING RECEIPT



OC000000047370616

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Date Mailed: 04/28/2011

Receipt is acknowledged of this non-provisional patent application. The application will be taken up for examination in due course. Applicant will be notified as to the results of the examination. Any correspondence concerning the application must include the following identification information: the U.S. APPLICATION NUMBER, FILING DATE, NAME OF APPLICANT, and TITLE OF INVENTION. Fees transmitted by check or draft are subject to collection. Please verify the accuracy of the data presented on this receipt. **If an error is noted on this Filing Receipt, please submit a written request for a Filing Receipt Correction. Please provide a copy of this Filing Receipt with the changes noted thereon. If you received a "Notice to File Missing Parts" for this application, please submit any corrections to this Filing Receipt with your reply to the Notice. When the USPTO processes the reply to the Notice, the USPTO will generate another Filing Receipt incorporating the requested corrections**

Applicant(s)

William W.Y. Chu, Los Altos, CA;

Assignment For Published Patent Application

ACQIS LLC, McKinney, TX

Power of Attorney: The patent practitioners associated with Customer Number 58249

Domestic Priority data as claimed by applicant

This application is a CON of 12/504,534 07/16/2009
which is a CON of 12/077,503 03/18/2008 PAT 7,676,624
which is a CON of 11/166,656 06/24/2005 PAT 7,376,779
which is a CON of 11/097,694 03/31/2005 PAT 7,363,415
which is a CON of 10/772,214 02/03/2004 PAT 7,099,981
which is a CON of 09/569,758 05/12/2000 PAT 6,718,415
which claims benefit of 60/134,122 05/14/1999

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If Required, Foreign Filing License Granted: 04/26/2011

The country code and number of your priority application, to be used for filing abroad under the Paris Convention, is **US 13/087,912**

Projected Publication Date: To Be Determined - pending completion of Corrected Papers

Non-Publication Request: No

Early Publication Request: No

Title

MULTIPLE MODULE COMPUTER SYSTEM AND METHOD INCLUDING DIFFERENTIAL SIGNAL CHANNEL COMPRISING UNIDIRECTIONAL SERIAL BIT CHANNELS

Preliminary Class

710

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Almost every country has its own patent law, and a person desiring a patent in a particular country must make an application for patent in that country in accordance with its particular laws. Since the laws of many countries differ in various respects from the patent law of the United States, applicants are advised to seek guidance from specific foreign countries to ensure that patent rights are not lost prematurely.

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APPLICATION NUMBER	FILING OR 371(C) DATE	FIRST NAMED APPLICANT	ATTY. DOCKET NO./TITLE
13/087,912	04/15/2011	William W.Y. Chu	ACQI-010/19US 310578-2066

CONFIRMATION NO. 7269

POA ACCEPTANCE LETTER



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Date Mailed: 04/28/2011

NOTICE OF ACCEPTANCE OF POWER OF ATTORNEY

This is in response to the Power of Attorney filed 04/15/2011.

The Power of Attorney in this application is accepted. Correspondence in this application will be mailed to the above address as provided by 37 CFR 1.33.

/dpham/

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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of: William W.Y. Chu Confirmation No.: 7269
Application No.: 13/087,912 Group Art Unit: 2111
Filed: April 15, 2011 Examiner:
Title: MULTIPLE MODULE COMPUTER SYSTEM AND METHOD INCLUDING DIFFERENTIAL SIGNAL
CHANNEL COMPRISING UNIDIRECTIONAL SERIAL BIT CHANNELS

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In response to the Notice to File Corrected Application Papers mailed April 28, 2011,
enclosed are:

- ☒ Substitute Specification-Markup
- ☒ Substitute Specification-Clean

The substitute specification includes all of the changes made in the preliminary amendment, with the exception that new Paragraph Nos. [0041.1] and [0041.2] from the Preliminary Amendment have been renumbered as Paragraph Nos. [0042] and [0043] in both the Clean and Markup versions, and the paragraphs following have been renumbered accordingly. No new matter has been added.

The Commissioner is hereby authorized to charge any appropriate fees that may be required by this paper to Deposit Account No. 50-1283.

Respectfully submitted,
Cooley LLP

Date: May 11, 2011

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By: 

Cliff Z. Liu
Reg. No. 50,834

**MULTIPLE MODULE COMPUTER SYSTEM AND METHOD INCLUDING
DIFFERENTIAL SIGNAL CHANNEL COMPRISING ~~UNDIRECTIONAL~~
UNIDIRECTIONAL SERIAL BIT CHANNELS**

CROSS REFERENCE TO RELATED APPLICATIONS

[0001] This application is a continuation of U.S. Application No. 12/504,534 filed July 16, 2009, which is a continuation of U.S. Application No. 12/077,503 filed March 18, 2008 (Now U.S. Patent No. 7,676,624), which is a continuation of U.S. nonprovisional Application No. 11/166,656, filed June 24, 2005 (Now U.S. Patent No. 7,376,779), which is a continuation of U.S. nonprovisional Application No. 11/097,694, filed March 31, 2005 (Now U.S. Patent No. 7,363,415), which is a continuation of U.S. nonprovisional Application No. 10/772,214, filed February 3, 2004 (Now U.S. Patent No. 7,099,981), which is a continuation of U.S. nonprovisional Application No. 09/569,758, filed May 12, 2000 (Now U.S. patent no. 6,718,415), and which claimed priority to U.S. Provisional Application No. 60/134,122 filed May 14, 1999. These applications are hereby incorporated by reference in their entirety.

BACKGROUND OF THE INVENTION

[0002] The present invention relates to computing devices. More particularly, the present invention provides a system including a plurality of computer modules that can independently operate to provide backup capability, dual processing, and the like. Merely by way of example, the present invention is applied to a modular computing environment for desk top computers, but it will be recognized that the invention has a much wider range of applicability. It can be applied to a server as well as other portable or modular computing applications.

[0003] Many desktop or personal computers, which are commonly termed PCs, have been around and used for over ten years. The PCs often come with state-of-art microprocessors such as the Intel PentiumTM microprocessor chips. They also include a hard or fixed disk drive such as memory in the giga-bit range. Additionally, the PCs often include a random access memory integrated circuit device such as a dynamic random access memory

device, which is commonly termed DRAM. The DRAM devices now provide up to millions of memory cells (i.e., mega-bit) on a single slice of silicon. PCs also include a high resolution display such as cathode ray tubes or CRTs. In most cases, the CRTs are at least 15 inches or 17 inches or 20 inches in diameter. High resolution flat panel displays are also used with PCs.

[0004] Many external or peripheral devices can be used with the PCs. Among others, these peripheral devices include mass storage devices such as a Zip™ Drive product sold by Iomega Corporation of Utah. Other storage devices include external hard drives, tape drives, and others. Additional devices include communication devices such as a modem, which can be used to link the PC to a wide area network of computers such as the Internet. Furthermore, the PC can include output devices such as a printer and other output means. Moreover, the PC can include special audio output devices such as speakers the like.

[0005] PCs also have easy to use keyboards, mouse input devices, and the like. The keyboard is generally configured similar to a typewriter format. The keyboard also has the length and width for easily inputting information by way of keys to the computer. The mouse also has a sufficient size and shape to easily move a cursor on the display from one location to another location.

[0006] Other types of computing devices include portable computing devices such as “laptop” computers and the like. Although somewhat successful, laptop computers have many limitations. These computing devices have poor display technology. In fact, these devices often have a smaller flat panel display that has poor viewing characteristics. Additionally, these devices also have poor input devices such as smaller keyboards and the like. Furthermore, these devices have limited common platforms to transfer information to and from these devices and other devices such as PCs.

[0007] Up to now, there has been little common ground between these platforms including the PCs and laptops in terms of upgrading, ease-of-use, cost, performance, and the like. Many differences between these platforms, probably somewhat intentional, has benefited computer manufacturers at the cost of consumers. A drawback to having two separate computers is that the user must often purchase both the desktop and laptop to have “total” computing power, where the desktop serves as a “regular” computer and the laptop serves as a “portable” computer. Purchasing both computers is often costly and

runs “thousands” of dollars. The user also wastes a significant amount of time transferring software and data between the two types of computers. For example, the user must often couple the portable computer to a local area network (i.e., LAN), to a serial port with a modem and then manually transfer over files and data between the desktop and the portable computer. Alternatively, the user often must use floppy disks to “zip” up files and programs that exceed the storage capacity of conventional floppy disks, and transfer the floppy disk data manually.

[0008] Another drawback with the current model of separate portable and desktop computer is that the user has to spend money to buy components and peripherals that are duplicated in at least one of these computers. For example, both the desktop and portable computers typically include hard disk drives, floppy drives, CD-ROMs, computer memory, host processors, graphics accelerators, and the like. Because program software and supporting programs generally must be installed upon both hard drives in order for the user to operate programs on the road and in the office, hard disk space is often wasted.

[0009] One approach to reduce some of these drawbacks has been the use of a docking station with a portable computer. Here, the user has the portable computer for “on the road” use and a docking station that houses the portable computer for office use.

[0010] Similar to separate desktop and portable computers, there is no commonality between two desktop computers. To date, most personal computers are constructed with a single motherboard that provides connection for CPU and other components in the computer. Dual CPU systems have been available through Intel’s slot 1 architecture. For example, two Pentium II cartridges can be plugged into two “slot 1” card slots on a motherboard to form a Dual-processor system. The two CPU’s share a common host bus that connects to the rest of the system, e.g. main memory, hard disk drive, graphics subsystem, and others. Dual CPU systems have the advantage of increased CPU performance for the whole system. Adding a CPU cartridge requires no change in operating systems and application software. However, dual CPU systems may suffer limited performance improvement if memory or disk drive bandwidth becomes the limiting factor. Also, dual CPU systems have to time-share the processing unit in running multiple applications. CPU performance improvement efficiency also depends on software coding structure. Dual CPU systems provide no hardware redundancy to help

fault tolerance. In running multiple applications, memory and disk drive data throughput will become the limiting factor in improving performance with multi-processor systems.

[0011] The present invention generally relates to computer interfaces. More specifically, the present invention relates to an interface channel that interfaces two computer interface buses that operate under protocols that are different from that used by the interface channel.

[0012] Interfaces coupling two independent computer buses are well known in the art. A block diagram of a computer system utilizing such a prior art interface is shown in Fig. 5. In Fig. 5, a primary peripheral component interconnect (PCI) bus 505 of a notebook PC 500 is coupled to a secondary PCI bus 555 in a docking system 550 (also referred to as docking station 550) through high pin count connectors 501 and 502, which are normally mating connectors. The high pin count connectors 501 and 502 contain a sufficiently large number of pins so as to carry PCI bus signals between the two PCI buses without any translation. The main purpose for interfacing the two independent PCI buses is to allow transactions to occur between a master on one PCI bus and a target on the other PCI bus. The interface between these two independent PCI buses additionally includes an optional PCI to PCI bridge 560, located in the docking station 550, to expand the add on capability in docking station 550. The bridge 560 creates a new bus number for devices behind the bridge 560 so that they are not on the same bus number as other devices in the system thus increasing the add on capability in the docking station 550.

[0013] An interface such as that shown in Fig. 5 provides an adequate interface between the primary and secondary PCI buses. However, the interface is limited in a number of ways. The interface transfers signals between the primary and secondary PCI buses using the protocols of a PCI bus. Consequently, the interface is subject to the limitations under which PCI buses operate. One such limitation is the fact that PCI buses are not cable friendly. The cable friendliness of the interface was not a major concern in the prior art. However, in the context of the computer system of the present invention, which is described in the present inventor's (William W.Y. Chu's) application for "Personal Computer Peripheral Console With Attached Computer Module" filed concurrently with the present application on Sep. 8, 1998 and incorporated herein by reference, a cable friendly interface is desired for interfacing an attached computer module (ACM) and a peripheral console of the present invention. Furthermore, as a result of operating by PCI

protocols, the prior art interface includes a very large number of signal channels with a corresponding large number of conductive lines (and a similarly large number of pins in the connectors of the interface) that are commensurate in number with the number of signal lines in the PCI buses which it interfaces. One disadvantage of an interface having a relatively large number of conductive lines and pins is that it costs more than one that uses a fewer number of conductive lines and pins. Additionally, an interface having a large number of conductive lines is bulkier and more cumbersome to handle. Finally, a relatively large number of signal channels in the interface renders the option of using differential voltage signals less viable because a differential voltage signal method would require duplicating a large number of signal lines. It is desirable to use a low voltage differential signal (LVDS) channel in the computer system of the present invention because an LVDS channel is more cable friendly, faster, consumes less power, and generates less noise, including electromagnetic interferences (EMI), than a PCI channel. The term LVDS is herein used to generically refer to low voltage differential signals and is not intended to be limited to any particular type of LVDS technology.

[0014] Thus, what is needed are computer systems that can have multiple computer modules. Each computer module has dedicated memory and disk drive, and can operate independently.

BRIEF SUMMARY OF THE INVENTION

[0015] According to the present invention, a technique including a method and device for multi-module computing is provided. In an exemplary embodiment, the present invention provides a system including a plurality of computer modules that can independently operate to provide backup capability, dual processing, and the like.

[0016] In a specific embodiment, the present invention provides a computer system for multi-processing purposes. The computer system has a console comprising a first coupling site and a second coupling site, e.g., computer module bay. Each coupling site comprises a connector. The console is an enclosure that is capable of housing each coupling site. The system also has a plurality of computer modules, where each of the computer modules is coupled to one of the connectors. Each of the computer modules has a processing unit, a main memory coupled to the processing unit, a graphics controller coupled to the processing unit, and a mass storage device coupled to the processing unit.

Each of the computer modules is substantially similar in design to each other to provide independent processing of each of the computer modules in the computer system.

[0017] In an alternative specific embodiment, the present invention provides a multi-processing computer system. The system has a console comprising a first coupling site and a second coupling site. Each coupling site comprises a connector. The console is an enclosure that is capable of housing each coupling site. The system also has a plurality of computer modules, where each of the computer modules is coupled to one of the connectors. Each of the computer modules has a processing unit, a main memory coupled to the processing unit, a graphics controller coupled to the processing unit, a mass storage device coupled to the processing unit, and a video output coupled to the processing unit. Each of the computer modules is substantially similar in design to each other to provide independent processing of each of the computer modules in the computer system. A video switch circuit is coupled to each of the computer modules through the video output. The video switch is configured to switch a video signal from any one of the computer modules to a display.

[0018] Numerous benefits are achieved using the present invention over previously existing techniques. In one embodiment, the invention provides improved processing and maintenance features. The invention can also provide increased CPU performance for the whole system. The invention also can be implemented without changes in operating system and application software. The present invention is also implemented using conventional technologies that can be provided in the present computer system in an easy and efficient manner.

[0019] In another embodiment, the invention provides at least two users to share the same modular desktop system. Each user operates on a different computer module. The other peripheral devices, i.e. CDROM, printer, DSL connection, etc. can be shared. This provides lower system cost, less desktop space and more efficiency. Depending upon the embodiment, one or more of these benefits can be available. These and other advantages or benefits are described throughout the present specification and are described more particularly below.

[0020] In still further embodiments, the present invention provides methods of using multiple computer modules.

[0021] The present invention encompasses an apparatus for bridging a first computer interface bus and a second computer interface bus. where each of the first and second computer interface buses have a number of parallel multiplexed address/data bus lines and operate at a clock speed in a predetermined clock speed range having a minimum clock speed and a maximum clock speed. The apparatus comprises an interface channel having a clock line and a plurality of bit lines for transmitting bits; a first interface controller coupled to the first computer interface bus and to the interface channel to encode first control signals from the first computer interface bus into first control bits to be transmitted on the interface channel and to decode second control bits received from the interface channel into second control signals to be transmitted to the first computer interface bus; and a second interface controller coupled to the interface channel and the second computer interface bus to decode the first control bits from the interface channel into third control signals to be transmitted on the second computer interface bus and to encode fourth control signals from the second computer interface bus into the second control bits to be transmitted on the interface channel.

[0022] In one embodiment, the first and second interface controllers comprise a host interface controller (HIC) and a peripheral interface controller (PIC), respectively, the first and second computer interface buses comprise a primary PCI and a secondary PCI bus, respectively, and the interface channel comprises an LVDS channel.

[0023] The present invention overcomes the aforementioned disadvantages of the prior art by interfacing two PCI or PCI-like buses using a non-PCI or non-PCI-like channel. In the present invention, PCI control signals are encoded into control bits and the control bits, rather than the control signals that they represent, are transmitted on the interface channel. At the receiving end, the control bits representing control signals are decoded back into PCI control signals prior to being transmitted to the intended PCI bus.

[0024] The fact that control bits rather than control signals are transmitted on the interface channel allows using a smaller number of signal channels and a correspondingly small number of conductive lines in the interface channel than would otherwise be possible. This is because the control bits can be more easily multiplexed at one end of the interface channel and recovered at the other end than control signals. This relatively small number of signal channels used in the interface channel allows using LVDS channels for the interface. As mentioned above, an LVDS channel is more cable friendly, faster,

consumes less power, and generates less noise than a PCI bus channel, which is used in the prior art to interface two PCI buses. Therefore, the present invention advantageously uses an LVDS channel for the hereto unused purpose of interfacing PCI or PCI-like buses. The relatively smaller number of signal channels in the interface also allows using connectors having smaller pins counts. As mentioned above an interface having a smaller number of signal channels and, therefore, a smaller number of conductive lines is less bulky and less expensive than one having a larger number of signal channels. Similarly, connectors having a smaller number of pins are also less expensive and less bulky than connectors having a larger number of pins.

[0025] In one embodiment, the present invention encompasses an apparatus for bridging a first computer interface bus and a second computer interface bus, in a microprocessor based computer system where each of the first and second computer interface buses have a number of parallel multiplexed address/data bus lines and operate at a clock speed in a predetermined clock speed range having a minimum clock speed and a maximum clock speed. The apparatus comprises an interface channel having a clock channel and a plurality of bit channels for transmitting bits; a first interface controller coupled to the first computer interface bus and to the interface channel to encode first control signals from the first computer interface bus into first control bits to be transmitted on the interface channel and to decode second control bits received from the interface channel into second control signals to be transmitted to the first computer interface bus; and a second interface controller coupled to the interface channel and the second computer interface bus to decode the first control bits from the interface channel into third control signals to be transmitted on the second computer interface bus and to encode fourth control signals from the second computer interface bus into the second control bits to be transmitted on the interface channel.

[0026] In one embodiment, the first and second interface controllers comprise a host interface controller (HIC) and a peripheral interface controller (PIC), respectively, the first and second computer interface buses comprise a primary PCI and a secondary PCI bus, respectively, and the interface channel comprises an LVDS channel.

[0027] In a preferred embodiment, the interface channel has a plurality of serial bit channels numbering fewer than the number of parallel bus lines in each of the PCI buses and operates at a clock speed higher than the clock speed at which any of the bus lines

operates. More specifically, the interface channel includes two sets of unidirectional serial bit channels which transmit data in opposite directions such that one set of bit channels transmits serial bits from the HIC to the PIC while the other set transmits serial bits from the PIC to the HIC. For each cycle of the PCI clock, each bit channel of the interface channel transmits a packet of serial bits.

[0028] The HIC and PIC each include a bus controller to interface with the first and second computer interface buses, respectively, and to manage transactions that occur therewith. The HIC and PIC also include a translator coupled to the bus controller to encode control signals from the first and second computer interface buses, respectively, into control bits and to decode control bits from the interface channel into control signals. Additionally, the HIC and PIC each include a transmitter and a receiver coupled to the translator. The transmitter converts parallel bits into serial bits and transmits the serial bits to the interface channel. The receiver receives serial bits from the interface channel and converts them into parallel bits.

[0029] According to the present invention, a technique including a method and device for securing a computer module using a password in a computer system is provided. In an exemplary embodiment, the present invention provides a security system for an attached computer module (“ACM”). In an embodiment, the ACM inserts into a Computer Module Bay (CMB) within a peripheral console to form a functional computer.

[0030] In a specific embodiment, the present invention provides a computer module. The computer module has an enclosure that is insertable into a console. The module also has a central processing unit (i.e., integrated circuit chip) in the enclosure. The module has a hard disk drive in the enclosure, where the hard disk drive is coupled to the central processing unit. The module further has a programmable memory device in the enclosure, where the programmable memory device can be configurable to store a password for preventing a possibility of unauthorized use of the hard disk drive and/or other module elements. The stored password can be any suitable key strokes that a user can change from time to time. In a further embodiment, the present invention provides a permanent password or user identification code stored in flash memory, which also can be in the processing unit, or other integrated circuit element. The permanent password or user identification code is designed to provide a permanent “finger print” on the attached computer module.

[0031] In a specific embodiment, the present invention provides a variety of methods. In one embodiment, the present invention provides a method for operating a computer system such as a modular computer system and others. The method includes inserting an attached computer module (“ACM”) into a bay of a modular computer system. The ACM has a microprocessor unit (e.g., microcontroller, microprocessor) coupled to a mass memory storage device (e.g., hard disk). The method also includes applying power to the computer system and the ACM to execute a security program, which is stored in the mass memory storage device. The method also includes prompting for a user password from a user on a display (e.g., fiat panel, CRT). In a further embodiment, the present method includes a step of reading a permanent password or user identification code stored in flash memory, or other integrated circuit element. The permanent password or user identification code provides a permanent finger print on the attached computer module. The present invention includes a variety of these methods that can be implemented in computer codes, for example, as well as hardware.

[0032] Numerous benefits are achieved using the present invention over previously existing techniques. The present invention provides mechanical and electrical security systems to prevent theft or unauthorized use of the computer system in a specific embodiment. Additionally, the present invention substantially prevents accidental removal of the ACM from the console. In some embodiments, the present invention prevents illegal or unauthorized use during transit. The present invention is also implemented using conventional technologies that can be provided in the present computer system in an easy and efficient manner. Depending upon the embodiment, one or more of these benefits can be available. These and other advantages or benefits are described throughout the present specification and are described more particularly below.

[0033] These and other embodiments of the present invention, as well as its advantages and features, are described in more detail in conjunction with the text below and attached Figs.

BRIEF DESCRIPTION OF THE DRAWINGS

[0034] Fig. 1 is a simplified diagram of a computer system according to an embodiment of the present invention;

[0035] Fig. 2 is a simplified block diagram of a computer system according to an alternative embodiment of the present invention;

[0036] Fig. 3 is a simplified block diagram of a computer system according to a further alternative embodiment of the present invention, and

[0037] Fig. 4 is a simplified flow diagram of a method according to an embodiment of the present invention.

[0038] Fig. 5 is a block diagram of a computer system using a prior art interface between a primary and a secondary PCI bus.

[0039] Fig. 6 is a block diagram of one embodiment of a computer system using the interface of the present invention.

[0040] Fig. 7 is a partial block diagram of a computer system using the interface of the present invention as a bridge between the north and south bridges of the computer system.

[0041] Fig. 8 is a partial block diagram of a computer system in which the north and south bridges are integrated with the host and peripheral interface controllers, respectively.

[0042] Fig. 8A shows an attached computer module with Integrated CPU/NB Graphics and Integrated HIC/SB.

[0043] Fig. 8B shows an attached computer module with single chip fully integrated: CPU, Cache, Core Logic, Graphics controller and Interface controller.

[0044] Fig. 9 is a block diagram of one embodiment of the host interface controller and the peripheral interface controller of the present invention.

[0045] Fig. 10 is a detailed block diagram of one embodiment of the host interface controller of the present invention.

[0046] Fig. 11 is a detailed block diagram of one embodiment of the PIC of the present invention.

[0047] Fig. 12 is a table showing the symbols, signals, data rate and description of signals in a first embodiment of the XPBus.

[0048] Fig. 13 is a table showing the information transmitted on the XPBus during two clock cycles of the XPBus in one embodiment of the present invention where 10 data bits transmitted in each clock cycle of the XPBus.

[0049] Fig. 14 is a table showing information transmitted on the XPBus during four clock cycles of the XPBus in another embodiment of the present invention where 10 data bits are transmitted in each clock cycle of the XPBus.

[0050] Fig. 15 is a schematic diagram of the signal lines PCK, PD0 to PD3, and PCN.

[0051] Fig. 16 is a table showing the names, types, number of pins dedicated to, and the description of the primary bus PCI signals.

[0052] FIG. 17 is a block diagram of one embodiment of a computer system employing the present invention.

[0053] FIG. 18 is a block diagram of an attached computing module (ACM).

[0054] FIG. 19 illustrates an external view of one embodiment of an ACM.

[0055] FIG. 19b illustrates one possible embodiment of a computer bay.

[0056] FIG. 20 illustrates the internal component layout for one embodiment of an ACM.

[0057] FIG. 21 is a block diagram of a peripheral console (PCON).

[0058] FIG. 22 is a simplified layout diagram of a security system for a computer system according to an embodiment of the present invention; and

[0059] FIG. 23 is a simplified block diagram of a security system for a computer module according to an embodiment of the present invention.

DETAILED DESCRIPTION OF THE INVENTION

[0060] According to the present invention, a technique including a method and device for multi-module computing is provided. In an exemplary embodiment, the present invention provides a system including a plurality of computer modules that can independently operate to provide backup capability, dual processing, and the like.

[0061] Fig. 1 is a simplified diagram of a computer system 100 according to an embodiment of the present invention. This diagram is merely an illustration and should not limit the scope of the claims herein. One of ordinary skill in the art would recognize other variations, modifications, and alternatives. The computer system 100 includes an attached computer module (i.e., ACM) 113, a desktop console 101, among other elements. The computer system also has another ACM module 117. Each ACM module has a respective slot 121, 119, which mechanically houses and electrically couples each ACM to the computer console. Also shown is a display 111, which connects to the console. Additionally, keyboard 109 and mouse 115 are also shown. A second display 102, keyboard 105, and mouse 107 can be coupled to the console in some optional embodiments to allow more than one user to operate the computer system. The computer system is modular and has a variety of components that are removable. Some of these components (or modules) can be used in different computers, workstations, computerized television sets, and portable or laptop units.

[0062] In the present embodiment, each ACM 113 includes computer components. as will be described below, including a central processing unit (“CPU”). IDE controller, hard disk drive, computer memory, and the like. The computer module bay (i.e., CMB) 121 is an opening or slot in the desktop console. The CMB houses the ACM and provides communication to and from the ACM. The CMB also provides mechanical protection and support to the ACM. The CMB has a mechanical alignment mechanism for mating a portion of the ACM to the console. The CMB further has thermal heat dissipation sinks, electrical connection mechanisms, and the like. Some details of the ACM can be found in co-pending Patent Application Nos. 09/149,882 and 09/149,548 filed 9/8/98, commonly assigned, and hereby incorporated by reference for all purposes.

[0063] In a specific embodiment, the present multiple computer module system has a peripheral console that has two or more computer bays that can receive a removable computer module or ACM. Multiple computer module system can function as a personal

computer with only one ACM and the peripheral console. The second and additional ACM can be added later to increase overall system performance and reliability. The ACM operates independently as self-contained computer, communicates with each other through a high-speed serial communication and share most peripheral devices within the peripheral console. Each ACM controls its independent graphics subsystem and drives separate video output signals. A practical implementation is a dual ACM system. In a dual ACM system, two monitors can be used to display the two ACMs' graphics outputs at the same time. For a single monitor, a RGB switch is used to switch between the video outputs of the two ACMs and can be controlled by a command from the user. Similarly, input devices (i.e. keyboard and mouse) are switched between the two computer systems with a command from the user. Command from the user can be in the form of either a dedicated key on the keyboard or a special icon on the screen that the mouse can click on.

[0064] In most embodiments, the ACM includes an enclosure such as the one described with the following components, which should not be limiting:

- 1) A CPU with cache memory;
- 2) Core logic device or means;
- 3) Main memory;
- 4) A single primary Hard Disk Drive ("HDD") that has a security program;
- 5) Flash memory with system BIOS and programmable user password;
- 6) Operating System, application software, data files on primary HDD;
- 7) An interface device and connectors to peripheral console;
- 8) A software controllable mechanical lock, lock control means, and other accessories.

[0065] The ACM connects to a peripheral console with power supply, a display device, an input device, and other elements. Some details of these elements with the present system are described in more detail below. In a dual ACM system, the primary ACM can connect directly to the peripheral board in the peripheral console. The second ACM can connect either directly or indirectly to the peripheral board. For indirect connection, a receptacle board is added to allow a cable connection to the peripheral board. This is to facilitate the mechanical positioning of the second ACM inside the computer chassis. The receptacle board approach can even be used for the primary ACM if a high bandwidth

peripheral bus, e.g. PCI Bus, is not connected from the primary ACM to the peripheral board.

[0066] The shared peripheral console has a chassis and a motherboard that connects the following devices:

- 1) Input means, e.g. keyboard and mouse,
- 2) Display means, e.g. RGB monitor,
- 3) Add-on means, e.g. PCI add-on slots,
- 4) Two Computer Module Bays (CMB) with connectors to two ACMs,
- 5) A serial communication Hub controller that interfaces to serial communication controller of both ACMs,
- 6) Shared storage subsystem, e.g. Floppy drive, CDROM drive, DVD drive, or 2nd Hard Drive,
- 7) Communication device, e.g. modem,
- 8) Power supply, and others.

[0067] The computer bay is an opening in the peripheral console that receives an ACM. CMB provides mechanical protection to ACM, mechanical alignment for connector mating, mechanical locking system to prevent theft and accidental removal, and connectors at the end of the opening for connecting to ACM. The interface bus between ACM and the peripheral console has a video bus, peripheral connections, serial communication connection, control signals and power connection. Video bus includes video output of graphics devices, i.e. analog RGB and control signals for monitor. Power connection supplies the power for ACM.

[0068] An implementation of peripheral sharing is the use of Ethernet controllers to bridge the communication between the two ACMs. Some of the peripheral devices residing in the peripheral console are shown in the simplified diagram of Fig. 2. As shown, the diagram is merely an illustration which should not limit the scope of the claims herein. One of ordinary skill in the art would recognize many other variations, alternatives, and modifications. As shown, a primary ACM 203 is connected to PCI peripheral devices in the peripheral console through the PCI bus 225 that passes through the connection between primary ACM 203 and peripheral console 201. As shown, ACM has a CPU module 207 coupled to the PCI bus through a North Bridge 211.

[0069] The CPU module can use a suitable microprocessing unit, microcontroller, digital signal processor, and the like. In a specific embodiment, the CPU module uses, for example, a 400 MHz Pentium II microprocessor module from Intel Corporation and like microprocessors from AMD Corporation, Cyrix Corporation (now National Semiconductor Corporation), and others. In other aspects, the microprocessor can be one such as the Compaq Computer Corporation Alpha Chip, Apple Computer Corporation PowerPC G3 processor, and the like. Further, higher speed processors are contemplated in other embodiments as technology increases in the future.

[0070] In the CPU module, peripheral controller 213 is coupled to BIOS/flash memory 217. Additionally, the peripheral controller is coupled to a clock control logic, a configuration signal, and a peripheral bus. The ACM has the hard drive module 215. Among other elements, the ACM includes north bridge 215, graphics subsystem 223 (e.g., graphics accelerator, graphics memory), an IDE controller, and other components. Adjacent to and in parallel alignment with the hard drive module 215 is the PCI bus. In a specific embodiment, North Bridge unit 211 often couples to a computer memory 209, to the graphics subsystem, and to the peripheral controller via the PCI bus. Graphics subsystem typically couples to a graphics memory, and other elements. IDE controller generally supports and provides timing signals necessary for the IDE bus. In the present embodiment, the IDE controller is embodied as part of a P114XE controller from Intel, for example. Other types of buses than IDE are contemplated, for example EIDE, SCSI, 1394, and the like in alternative embodiments of the present invention.

[0071] The hard drive module or mass storage unit 215 typically includes a computer operating system, application software program files, data files, and the like. In a specific embodiment, the computer operating system may be the Windows98 operating system from Microsoft Corporation of Redmond Washington. Other operating systems, such as WindowsNT, MacOS8, Unix, and the like are also contemplated in alternative embodiments of the present invention. Further, some typical application software programs can include Office98 by Microsoft Corporation, Corel Perfect Suite by Corel, and others. Hard disk module 215 includes a hard disk drive. The hard disk drive, however, can also be replaced by removable hard disk drives, read/write CD ROMs, flash memory, floppy disk drives, and the like. A small form factor, for example 2.5", is

currently contemplated, however, other form factors, such as PC card, and the like are also contemplated. Mass storage unit 240 may also support other interfaces than IDE.

[0072] Among other features, the computer system includes an ACM with security protection.

[0073] The ACM also has a network controller, which can be an Ethernet controller 219, which is coupled to the North Bridge through the PCI bus. The North Bridge is coupled to the CPU. The Ethernet controller can be a 10/100 Base, such as Intel's 82559 or the like. Other types of network connection devices can also be used. For example, the invention can use Gbit Ethernet 1394, and USB 2.0. The network controller couples to a hub 233 in the console, which includes shared peripheral system 201.

[0074] Also shown is the second ACM 205. The second ACM has the same or similar components as the first ACM. Here, like reference numerals have been used for easy cross-referencing, but is not intended to be limiting. In some embodiments, the secondary ACM is not connected to the PCI bus in the peripheral console directly. The secondary ACM 219 accesses peripheral devices controlled by the primary ACM through the Ethernet connection to the primary ACM, e.g. CD-ROM, or PCI modem. The implementation is not restricted to Ethernet serial communication and can use other high-speed serial communication such as USB 2.0, and 1394. The Ethernet hub is coupled to an external output port 235, which connects to an external network.

[0075] The primary hard disk drive in each ACM can be accessed by the other ACM as sharable hard drive through the Ethernet connection. This allows the easy sharing of files between the two independent computer modules. The Ethernet Hub Controller provides the high-speed communication function between the two computer modules. Ethernet data bandwidth of 100 Mbit/sec allows fast data communication between the two computer modules. The secondary ACM access peripheral devices of the primary ACM through the network connection provided by Ethernet link. The operating system, e.g. Windows98, provides the sharing of resources between the two ACMs. In some embodiments, critical data in one ACM can be backup into the other ACM.

[0076] The Ethernet hub also couples to PCI bus 239, which connects to PCI devices 241, 243, e.g., modem, SCSI controller. A flash memory 242 can also be coupled to the PCI bus. The flash memory can store passwords and security information, such as those

implementations described in U.S. Serial No. 09/183,493, which is commonly owned, and hereby incorporated by reference. The hub 233 also couples to an I/O control 237, which connects to keyboard/mouse switch 245, which couples to keyboard/mouse 247. Optionally, the keyboard/mouse switch also couples to a second keyboard/house 259 via PS2 or USB signal line 251. The keyboard/mouse switch has at least a first state and a second state, which allow operation of respectively multiple keyboards or a single keyboard. The switch also couples to each I/O controller 221 in each ACM via lines 253, 255. The I/O control 237 also couples to an RGB switch 257, which allows video signals to pass to the first monitor 259. Alternatively, the RGB switch couples to a second monitor 261. The RGB switch includes analog video switches such as MAXIM's MAX4545.

[0077] The peripheral system 201 also has an independent power supply 231 for each ACM. Each power supply provides power to each ACM. As merely an example, the power supply is a MICRO ATX 150W made by ENLIGHT, but can be others. The power supply is connected or coupled to each ACM through a separate line, for example. The independent power supply allows for independent operation of each ACM in some embodiments.

[0078] The above embodiments are described generally in terms of hardware and software. It will be recognized, however, that the functionality of the hardware can be further combined or even separated. The functionality of the software can also be further combined or even separated. Hardware can be replaced, at times, with software. Software can be replaced, at times, with hardware. Accordingly, the present embodiments should not be construed as limiting the scope of the claims here. One of ordinary skill in the art would recognize other variations, modifications, and alternatives.

[0079] Fig. 3 is a simplified block diagram 300 of a computer system according to an alternative embodiment of the present invention. This diagram is merely an example which should not limit the scope of the claims herein. One of ordinary skill in the art would recognize many other variations, modifications, and alternatives. Like reference numerals are used in this Fig. as the previous Figs. for easy referencing, but are not intended to be limiting. As shown, each ACM includes common elements as the previous Fig. A primary ACM 203 is connected to PCI peripheral devices in the peripheral console through the PCI bus 225 that passes through the connection between primary ACM 203

and peripheral console 201. As shown, ACM has a CPU module 207 coupled to the PCI bus through a North Bridge 211.

[0080] The CPU module can use a suitable microprocessing unit, microcontroller, digital signal processor, and the like. In a specific embodiment, the CPU module uses, for example, a 400 MHz Pentium II microprocessor module from Intel Corporation and like microprocessors from AMD Corporation, Cyrix Corporation (now National Semiconductor Corporation), and others. In other aspects, the microprocessor can be one such as the Compaq Computer Corporation Alpha Chip, Apple Computer Corporation PowerPC G3 processor, and the like. Further, higher speed processors are contemplated in other embodiments as technology increases in the future.

[0081] In the CPU module, peripheral controller 213 is coupled to BIOS/flash memory 217. Additionally, the peripheral controller is coupled to a clock control logic, a configuration signal, and a peripheral bus. The ACM has the hard drive module 215. Among other elements, the ACM includes north bridge 215, graphics subsystem 223 (e.g., graphics accelerator, graphics memory), an IDE controller, and other components. Adjacent to and in parallel alignment with the hard drive module 215 is the PCI bus. In a specific embodiment, North Bridge unit 211 often couples to a computer memory 209, to the graphics subsystem, and to the peripheral controller via the PCI bus. Graphics subsystem typically couples to a graphics memory, and other elements. IDE controller generally supports and provides timing signals necessary for the IDE bus. In the present embodiment, the IDE controller is embodied as part of a P114XE controller from Intel, for example. Other types of buses than IDE are contemplated, for example EIDE, SCSI, 1394, and the like in alternative embodiments of the present invention.

[0082] The hard drive module or mass storage unit 215 typically includes a computer operating system, application software program files, data files, and the like. In a specific embodiment, the computer operating system may be the Windows98 operating system from Microsoft Corporation of Redmond Washington. Other operating systems, such as WindowsNT, MacOS8, Unix, and the like are also contemplated in alternative embodiments of the present invention. Further, some typical application software programs can include Office98 by Microsoft Corporation, Corel Perfect Suite by Corel, and others. Hard disk module 215 includes a hard disk drive. The hard disk drive, however, can also be replaced by removable hard disk drives, read/write CD ROMs, flash

memory, floppy disk drives, and the like. A small form factor, for example 2.5", is currently contemplated, however, other form factors, such as PC card, and the like are also contemplated. Mass storage unit 240 may also support other interfaces than IDE.

[0083] Among other features, the computer system includes an ACM with security protection.

[0084] The ACM also has a network controller, which can be coupled to a serial port 302, which is coupled to the PCI bus in the ACM. The serial port is coupled to the peripheral console through a serial controller 301 in the serial console. The serial controller is connected to PCI bus 239. The serial controller is also coupled to a serial hub controller 303, which is coupled to the PCI bus and a second ACM. In a specific embodiment, a receptacle board 310 is added to connect to the second ACM. The purpose of the receptacle board is to allow a cable connection 307 to the peripheral board 300. The cable connection is possible because the signals needed to connect to the peripheral board can be limited to video, I/O, serial communication, and power. The serial communication controller can be placed on the receptacle board and not in the ACM. As shown, the serial bus controller couples to the PCI bus. The receptacle board also couples to power, graphics subsystem, I/O controller, and other elements, which may be on a common bus. The overall operation of the present configuration is similar to the previous one except it operates in serial communication mode.

[0085] The Dual ACM system can support different usage models:

[0086] 1. One user using both ACMs concurrently with 1 or 2 monitors, and a common keyboard/mouse.

[0087] 2. Two users using the two separate ACMs at the same time with separate monitors and keyboard/mouse. The 2 users share peripherals, e.g., printer, CDROM, and others. The two users share external networking.

[0088] To support 1 monitor for both ACMs, a video switch in the peripheral console is used to switch between the video outputs of the two ACMs. The system can be set to support either 1 monitor or 2-monitor mode. The user presses a special key on the keyboard or a special icon on the screen to switch the screen display from one ACM to the

other. This same action causes the keyboard and mouse connections to switch from one ACM to the other ACM.

[0089] A dual ACM system can save space, wiring, and cost for a 2-person PC setup, with the added benefit that both PC systems can be accessed from one user site for increased system performance if the other user is not using the system. Files can be copied between the primary drive of both system and provides protection against a single ACM failure. Software needs to be developed to manage the concurrent use of two PC subsystems, the automatic sharing of selected files between the two systems, and fault tolerance.

[0090] The design with more than two computer modules can be implemented with the use of multi-port, serial communication hub controller and multi-port I/O switches. In one embodiment, a peripheral console has four computer bays for four separate computer modules. The computer modules communicate through a four port Ethernet hub. The video, keyboard, and mouse switch will cycle through the connection from each computer module to the external monitor, keyboard, and mouse with a push button sequentially. This embodiment is useful for a server that performs different functions concurrently, e.g. email, application hosting, web hosting , firewall, etc.

[0091] The above embodiments are described generally in terms of hardware and software. It will be recognized, however, that the functionality of the hardware can be further combined or even separated. The functionality of the software can also be further combined or even separated. Hardware can be replaced, at times, with software. Software can be replaced, at times, with hardware. Accordingly, the present embodiments should not be construed as limiting the scope of the claims here. One of ordinary skill in the art would recognize other variations, modifications, and alternatives.

[0092] Fig. 4 is a simplified diagram of a method according to an embodiment of the present invention. This diagram is merely an example which should not limit the scope of the claims herein. One of ordinary skill in the art would recognize many other variations, modifications, and alternatives. The present diagram illustrates an automatic file backup procedure from one computer module to the other. As shown, a user selects (step 401) a certain file in one of the computer module for automatic backup. Next, the method determines if another module is available, step 403. If so, the method in the originating

module requests the other computer module to create (step 405) backup file. Alternatively, the method alerts the user of the missing or malfunctioning module, step 429. The method then has the user try later 431, once the missing or malfunctioning module has been replaced or repaired. Next, the method determines if there is sufficient storage available in the other computer module for the backup files. If so, the method goes to the next step. (Alternatively, the method prompts (step 433) a message to the user indicating that the storage is full.) In the next step, the method stores the backup file in memory of the other module. After the backup file has been successfully created (step 409), the software in the originating ACM sets a timer to check (step 411) for file modification via branches 423, 427 through continue, step 425 process. If a file selected for backup has been modified (step 415), then the file is automatically back up to the other ACM again, step 417. Alternatively, the method returns to step 411 through branch 421.

[0093] The above embodiments are described generally in terms of hardware and software. It will be recognized, however, that the functionality of the hardware can be further combined or even separated. The functionality of the software can also be further combined or even separated. Hardware can be replaced, at times, with software. Software can be replaced, at times, with hardware. Accordingly, the present embodiments should not be construed as limiting the scope of the claims here. One of ordinary skill in the art would recognize other variations, modifications, and alternatives.

[0094] Fig. 6 is a block diagram of one embodiment of a computer system 600 using the interface of the present invention. Computer system 600 includes an attached computer module (ACM) 605 and a peripheral console 610, which are described in greater detail in the application of William W. Y. Chu for “Personal Computer Peripheral Console With Attached Computer Module” filed concurrently with the present application on Sep. 8, 1998 and incorporated herein by reference. The ACM 605 and the peripheral console 610 are interfaced through an exchange interface system (XIS) bus 615. The XIS bus 615 includes power bus 616, video bus 617 and peripheral bus (XPBus) 618, which is also herein referred to as an interface channel. The power bus 616 transmits power between ACM 605 and peripheral console 610. In a preferred embodiment power bus 616 transmits power at voltage levels of 3.3 volts, 5 volts and 12 volts. Video bus 617 transmits video signals between the ACM 605 and the peripheral console 610. In a preferred embodiment, the video bus 617 transmits analog Red Green Blue (RGB) video

signals for color monitors, digital video signals (such as Video Electronics Standards Association (VESA) Plug and Display's Transition Minimized Differential Signaling (TMDS) signals for flat panel displays), and television (TV) and/or super video (S-video) signals. The XPBus 618 is coupled to host interface controller (HIC) 619 and to peripheral interface controller (PIC) 620, which is also sometimes referred to as a bay interface controller.

[0095] In the embodiment shown in Fig. 6, HIC 619 is coupled to an integrated unit 621 that includes a CPU, a cache and a north bridge. In another embodiment, such as that shown in Fig. 7, the CPU 705 and north bridge 710 are separate rather than integrated units. In yet another embodiment, such as that shown in Fig. 8, the HIC and PIC are integrated with the north and south bridges, respectively, such that integrated HIC and north bridge unit 805 includes an HIC and a north bridge, while integrated PIC and south bridge unit 810 includes a PIC and a south bridge. Fig. 8A shows an attached computer module with integrated CPU/NB/Graphics 815 and Integrated HIC/SB 820. Fig. 8B shows an attached computer module with single chip 825 fully integrated: CPU, Cache, Core Logic, Graphics controller and Interface controller.

[0096] Fig. 9 is a more detailed block diagram of one embodiment of an HIC 905 and a PIC 955 of the present invention. HIC 905 includes a peripheral component interconnect (PCI) bus controller 910, an XPBus controller 915, a phase lock loop (PLL) clock 920 and an input/output (IO) control 925. Similarly, PIC 955 includes a PCI bus controller 960, an XPBus controller 965, a PLL clock 970 and an IO control 975. PCI bus controllers 910 and 960 are coupled to the primary and secondary PCI buses 930 and 980, respectively, and manage PCI transactions on the primary and secondary PCI buses 930 and 980, respectively. Similarly, XPBus Controllers 915 and 965 are coupled to XPBus 990. XPBus controller 915 drives the PCK line 991 and PD[0::3] and PCN lines 992 while XPBus controller 965 drives the PCKR lines 993, the PDR[0::3] and PCNR lines 994 and the RESET# line 995.

[0097] PCI bus controller 910 receives PCI clock signals from the primary PCI bus 930 and is synchronized to the PCI clock. However, as indicated in Fig. 9, the XPBus controller 915 is asynchronous with the PCI bus controller 910. Instead, the XPBus controller receives a clock signal from the PLL clock 920 and is synchronized therewith. PLL clock 920 generates a clock signal independent of the PCI clock. The asynchronous

operation of the PCI bus and the XDBus allows the PCI Bus to change in frequency. for example as in a power down situation, without directly affecting the XDBus clocking. In the embodiment shown in Fig. 9, the PLL clock 920 generates a clock signal having a frequency of 66 MHz, which is twice as large as the 33 MHz frequency of the PCI clock. (The clock signal generated by the PLL clock may have a clock speed different from, including lower than, 66 MHz. For example, in another embodiment, which is discussed in greater detail below, the PLL clock 920 generates a clock signal having a frequency of 132 MHz.)

[0098] The XDBus 990 operates at the clock speed generated by the PLL clock 920. Therefore, PCK, the clock signal from the XDBus controller 915 to XDBus controller 965 has the same frequency as the clock signal generated by PLL clock 920. XDBus controller 965 receives the PCK signal after it has been buffered and operates at the clock speed of PCK. The buffered version of the clock signal PCK is used to generate the clock signal PCKR, the clock signal from the XDBus controller 965 to XDBus controller 915. Accordingly, PCKR also has the same frequency as that generated by the PLL clock 920. The synchronous operation of PCK and PCKR provides for improved reliability in the system. In another embodiment, PCKR may be generated independently of PCK and may have a frequency different from that of PCK. It is to be noted that even when PCKR is generated from PCK, the slew between PCK and PCKR cannot be guaranteed because of the unknown cable length used for the XDBus. For a cable that is several feet long, the cable propagation delay alone can be several nano seconds.

[0099] As indicated in Fig. 9, PLL clock 970 is asynchronous with the XDBus controller 965. Instead, PLL clock 970 independently generates a clock signal that is used as a PCI clock signal on the secondary PCI bus 980. The secondary PCI bus 980 operates at the same clock speed as the primary PCI bus 930, namely at a frequency of 33 MHz.

[0100] Fig. 10 is a detailed block diagram of one embodiment of the HIC of the present invention. As shown in Fig. 10, HIC 1000 comprises bus controller 1010, translator 1020, transmitter 1030, receiver 1040, a PLL 1050, an address/data multiplexer (A/D MUX) 1060, a read/write controller (RD/WR Cntl) 1070, a video serial to parallel converter 1080 and a CPU control & general purpose input/output latch/driver (CPU CNTL & GPIO latch/driver) 1090.

[0101] HIC 1000 is coupled to an optional flash memory BIOS configuration unit 1001. Flash memory unit 1001 stores basic input output system (BIOS) and PCI configuration information and supplies the BIOS and PCI configuration information to A/D MUX 1060 and RD/WR Control 1070, which control the programming, read, and write of flash memory unit 1001.

[0102] Bus controller 1010 is coupled to the host PCI bus, which is also referred to herein as the primary PCI bus, and manages PCI bus transactions on the host PCI bus. Bus controller 1010 includes a slave (target) unit 1011 and a master unit 1016. Both slave unit 1011 and master unit 1016 each include two first in first out (FIFO) buffers, which are preferably asynchronous with respect to each other since the input and output of the two FIFOs in the master unit 1016 as well as the two FIFOs in the slave unit 1011 are clocked by different clocks, namely the PCI clock and the PCK. Additionally, slave unit 1011 includes encoder 1022 and decoder 1023, while master unit 1016 includes encoder 1027 and decoder 1028. The FIFOs 1012, 1013, 1017 and 1018 manage data transfers between the host PCI bus and the XPBus, which in the embodiment shown in Fig. 10 operate at 33 MHz and 106 MHz, respectively. PCI address/data (AD) from the host PCI bus is entered into FIFOs 1012 and 1017 before they are encoded by encoders 1022 and 1023. Encoders 1022 and 1023 format the PCI address/data bits to a form more suitable for parallel to serial conversion prior to transmittal on the XPBus. Similarly, address and data information from the receivers is decoded by decoders 1023 and 1028 to a form more suitable for transmission on the host PCI bus. Thereafter the decoded data and address information is passed through FIFOs 1013 and 1018 prior to being transferred to the host PCI bus. FIFOs 1012, 1013, 1017 and 1018, allow bus controller 1010 to handle posted and delayed PCI transactions and to provide deep buffering to store PCI transactions.

[0103] Bus controller 1010 also comprises slave read/write control (RD/WR Cntl) 1014 and master read/write control (RD/WR Cntl) 1015. RD/WR controls 1014 and 1015 are involved in the transfer of PCI control signals between bus controller 1010 and the host PCI bus.

[0104] Bus controller 1010 is coupled to translator 1020. Translator 1020 comprises encoders 1022 and 1027, decoders 1023 and 1028, control decoder & separate data path unit 1024 and control encoder & merge data path unit 1025. As discussed above encoders 1022 and 1027 are part of slave data unit 1011 and master data unit 1016, respectively,

receive PCI address and data information from FIFOs 1012 and 1017, respectively, and encode the PCI address and data information into a form more suitable for parallel to serial conversion prior to transmittal on the XPBus. Similarly, decoders 1023 and 1028 are part of slave data unit 1011 and master data unit 1016, respectively, and format address and data information from receiver 1040 into a form more suitable for transmission on the host PCI bus. Control encoder & merge data path unit 1025 receives PCI control signals from the slave RD/WR control 1014 and master RD/WR control 1015. Additionally, control encoder & merge data path unit 1025 receives control signals from CPU CNTL & GPIO latch/driver 1090, which is coupled to the CPU and north bridge (not shown in Fig. 10). Control encoder & merge data path unit 1025 encodes PCI control signals as well as CPU control signals and north bridge signals into control bits, merges these encoded control bits and transmits the merged control bits to transmitter 1030, which then transmits the control bits on the data lines PD0 to PD3 and control line PCN of the XPBus. Examples of control signals include PCI control signals and CPU control signals. A specific example of a control signal is FRAME# used in PCI buses. A control bit, on the other hand is a data bit that represents a control signal. Control decoder & separate data path unit 1024 receives control bits from receiver 1040 which receives control bits on data lines PDR0 to PDR3 and control line PCNR of the XPBus. Control decoder & separate data path unit 1024 separates the control bits it receives from receiver 1040 into PCI control signals, CPU control signals and north bridge signals, and decodes the control bits into PCI control signals, CPU control signals, and north bridge signals all of which meet the relevant timing constraints.

[0105] Transmitter 1030 receives multiplexed parallel address/data (AID) bits and control bits from translator 1020 on the AD[31::0] out and the CNTL out lines, respectively. Transmitter 1030 also receives a clock signal from PLL 1050. PLL 1050 takes a reference input clock and generates PCK that drives the XPBus. PCK is asynchronous with the PCI clock signal and operates at 106 MHz, twice the speed of the PCI clock of 33 MHz. The higher speed is intended to accommodate at least some possible increases in the operating speed of future PCI buses. As a result of the higher speed, the XPBus may be used to interface two PCI or PCI-like buses operating at 106 MHz rather than 33 MHz or having 104 rather than 32 multiplexed address/data lines.

[0106] The multiplexed parallel A/D bits and some control bits input to transmitter 1030 are serialized by parallel to serial converters 1032 of transmitter 1030 into 10 bit packets. These bit packets are then output on data lines PD0 to PD3 of the XPBus. Other control bits are serialized by parallel to serial converter 1033 into 10 bit packets and send out on control line PCN of the XPBus.

[0107] A 10x multiplier 1031 receives PCK, multiplies it by a factor of 10 and feeds a clock signal 10 times greater than PCK into the parallel to serial converters 1032 and 1033. The parallel to serial converters 1032 and 1033 perform bit shifting at 10 times the PCK rate to serialize the parallel bits into 10 bit packets. As the parallel to serial converters 1032 and 1033 shift bits at 10 times the PCK rate, the bit rate for the serial bits output by the parallel to serial converters is 10 times higher than PCK rate, i.e., 1060 MHz. However, the rate at which data packets are transmitted on the XPBus is the same as the PCK rate, i.e., 106 MHz. As the PCI buses operate at a clock and bit rate of 33 MHz, the XPBus has a clock rate that is twice as large and a bit rate per bit line (channel) that is 100 times as large as that of the PCI buses which it interfaces.

[0108] Receiver 1040 receives serial bit packets on data lines PDR0 to PDR3 and control line PCNR. Receiver 1040 also receives PCKR on the XPBus as well as the clock signal PCK from PLL 1050. The synchronizer (SYNC) 1044 of receiver 1040 synchronizes the clock signal PCKR to the locally generated clock signal, PCK, in order to capture the bits received from the XPBus into PCK clock timing.

[0109] Serial to parallel converters 1042 convert the serial bit packets received on lines PDR0 to PDR3 into parallel address/data and control bits that are sent to decoders 1023 and 1028 and control decoder and separate data path unit 1024, respectively. Serial to parallel converter 1043 receives control bit packets from control line PCNR, converts them to parallel control bits and sends the parallel control bits to control decoder & separate data path 1024.

[0110] A 10x multiplier 1041 receives PCKR, multiplies it by a factor of 10 and feeds a clock signal 10 times greater than PCKR into the serial to parallel converters 1042 and 1043. Because the bits on PDR0 to PDR3 and PCNR are transmitted at a bit rate of 10 times the PCKR rate, the serial to parallel converters 1042 and 1043 perform bit shifting at 10 times the PCKR rate to convert the 10 bit packets into parallel bits. It is to be noted

that the rate at which bit packets are transmitted on the XPBus is the same as the PCKR rate, i.e., 106 MHz. The parallel data and control bits are thereafter sent to decoders 1023 and 1028 by way of the AD[3::0] in line and to control decoder & separate data path unit 1024 by way of CNTL in lines, respectively.

[0111] Reset control unit 1045 of HIC 1000 receives the signal RESET#, which is an independent system reset signal, on the reset line RESET#. Reset control unit 1045 then transmits the reset signal to the CPU CNTL & GPIO latch/driver unit 1090.

[0112] As may be noted from the above, the 32 line host and secondary PCI buses are interfaced by 10 XPBus lines (PD0, PD1, PD2, PD3, PCN, PDR0, PDR1, PDR2, PDR3, PCNR). Therefore, the interface channel, XPBus, of the present invention uses fewer lines than are contained in either of the buses which it interfaces, namely the PCI buses. XPBus is able to interface such PCI buses without backup delays because the XPBus operates at a clock rate and a per line (channel) bit rate that are higher than those of the PCI buses.

[0113] In addition to receiving a reset signal, the CPU CNTL & GPIO latch/driver 1090 is responsible for latching input signals from the CPU and north bridge and sending the signals to the translator. It also takes decoded signals from the control decoder & separate data path unit 1024 and drives the appropriate signals for the CPU and north bridge.

[0114] In the embodiment shown in Fig. 10, video serial to parallel converter 1080 is included in HIC 1000. In another embodiment, video serial to parallel converter 1080 may be a separate unit from the HIC 1000. Video serial to parallel converter 1080 receives serial video data on line VPD and a video clock signal VPCCK from line VPCCK of video bus 1081. It then converts the serial video data into 16 bit parallel video port data and the appropriate video port control signals, which it transmits to the graphics controller (not shown in Fig. 10) on the video port data [0::15] and video port control lines, respectively.

[0115] HIC 1000 handles the PCI bus control signals and control bits from the XPBus representing PCI control signals in the following ways:

1. HIC 1000 buffers clocked control signals from the host PCI bus, encodes them into control bits and sends the encoded control bits to the XPBus;
2. HIC 1000 manages the signal locally; and

3. HIC 1000 receives control bits from XPBus, translates the control bits into PCI control signals and sends the PCI control signals to the host PCI bus.

[0116] Fig. 11 is a detailed block diagram of one embodiment of the PIC of the present invention. PIC 1100 is nearly identical to HIC 1000 in its function, except that HIC 1000 interfaces the host PCI bus to the XPBus while PIC 1100 interfaces the secondary PCI bus to the XPBus. Similarly, the components in PIC 1100 serve the same function as their corresponding components in HIC 1000. Reference numbers for components in PIC 1100 have been selected such that a component in PIC 1100 and its corresponding component in HIC 1000 have reference numbers that differ by 500 and have the same two least significant digits. Thus for example, the bus controller in PIC 1100 is referenced as bus controller 1110 while the bus controller in HIC 1000 is referenced as bus controller 1010. As many of the elements in PIC 1100 serve the same functions as those served by their corresponding elements in HIC 1000 and as the functions of the corresponding elements in HIC 1000 have been described in detail above, the function of elements of PIC 1100 having corresponding elements in HIC 1000 will not be further described herein. Reference may be made to the above description of Fig. 10 for an understanding of the functions of the elements of PIC 1100 having corresponding elements in HIC 1000.

[0117] As suggested above, there are also differences between HIC 1000 and PIC 1100. Some of the differences between HIC 1000 and PIC 1100 include the following. First, receiver 1140 in PIC 1100, unlike receiver 1040 in HIC 1000, does not contain a synchronization unit. As mentioned above, the synchronization unit in HIC 1000 synchronizes the PCKR clock to the PCK clock locally generated by PLL 1050. PIC 1100 does not locally generate a PCK clock and therefore, it does not have a locally generated PCK clock with which to synchronize the PCK clock signal that it receives from HIC 1000. Another difference between PIC 1100 and HIC 1000 is the fact that PIC 1100 contains a video parallel to serial converter 1189 whereas HIC 1000 contains a video serial to parallel converter 1080. Video parallel to serial converter 1189 receives 16 bit parallel video capture data and video control signals on the Video Port Data [0::15] and Video Port Control lines, respectively, from the video capture circuit (not shown in Fig. 11) and converts them to a serial video data stream that is transmitted on the VPD line to the HIC. The video capture circuit may be any type of video capture circuit that outputs a 16 bit parallel video capture data and video control signals. Another difference lies in the

fact that PIC 1100, unlike HIC 1000, contains a clock doubler 1182 to double the video clock rate of the video clock signal that it receives. The doubled video clock rate is fed into video parallel to serial converter 1182 through buffer 1183 and is sent to serial to parallel converter 1080 through buffer 1184. Additionally, reset control unit 1135 in PIC 1100 receives a reset signal from the CPU CNTL & GPIO latch/driver unit 1190 and transmits the reset signal on the RESET# line to the HIC 1000 whereas reset control unit 1045 of HIC 1000 receives the reset signal and forwards it to its CPU CNTL & GPIO latch/driver unit 1090 because, in the above embodiment, the reset signal RESET# is unidirectionally sent from the PIC 1100 to the HIC 1000.

[0118] Like HIC 1000, PIC 1100 handles the PCI bus control signals and control bits from the XPBus representing PCI control signals in the following ways:

1. PIC 1100 buffers clocked control signals from the secondary PCI bus. encodes them and sends the encoded control bits to the XPBus;
2. PIC 1100 manages the signal locally; and
3. PIC 1100 receives control bits from XPBus, translates them into PCI control signals and sends the PCI control signals to the secondary PCI bus.

[0119] PIC 1100 also supports a reference arbiter on the secondary PCI Bus to manage the PCI signals REQ# and GNT#.

[0120] Fig. 12 is a table showing the symbols, signals, data rate and description of signals on the XPBus, where RTN indicates a ground (GND) reference. In the above tables, P&D stands for plug and display and is a trademark of the Video Electronics Standards Association (VESA) for the Plug and Display standard, DDC2:SCL and DDC2:SDA stand for the VESA display data channel (DDC) standard 2 clock and data signals, respectively, SV stands for super video, V33 is 3.3 volts, and V5 is 5.0 volts. TMDS stands for Transition Minimized Differential Signaling and is a trademark of Silicon Images and refers to their Panel Link technology, which is in turn a trademark for their LVDS technology. TMDS is used herein to refer to the Panel Link technology or technologies compatible therewith.

[0121] Fig. 13 is a table showing the information transmitted on the XPBus during two clock cycles of the XPBus in one embodiment of the present invention where 10 data bits are transmitted in each clock cycle of the XPBus. In Fig. 13, A00 to A31 represent 32

bits of PCI address A[31:0], D00 to D31 represent 32 bits of PCI data D[31:0], BS0 to BS3 represent 4 bits of bus status data indicating the status of the XPBus, CM0# to CM3# represent 4 bits of PCI command information, BE0# to BE3# represent 4 bits of PCI byte enable information, and CN0 to CN9 represent 10 bits of control information sent in each clock cycle. As shown in Fig. 13, for each of lines PD0 to PD3, the 10 bit data packets contain one BS bit, one CM/BE bit, and eight AID bits. For the PCN line, the 10 bit data packet contains 10 CN bits. The first clock cycle shown in Fig. 13 comprises an address cycle in which 4 BS bits, 4 CM bits, 32 A bits and 10 CN bits are sent. The second clock cycle comprises a data cycle in which 4 BS bits, 4 BE bits, 32 D bits and 10 CN bits are sent. The bits transmitted on lines PD0 to PD3 represent 32 PCI AD[31:0] signals, 4 PCI C/BE# [3:0] signals, and part of the function of PCI control signals, such as FRAME#, IRDY#, and TRDY#.

[0122] In the embodiment shown in Fig. 13, BS0 to BS3 are sent at the beginning of each clock cycle. The bus status bits indicate the following bus cycle transactions: idle, address transfer, write data transfer, read data transfer, switch XPBus direction, last data transfer, wait, and other cycles.

[0123] Bits representing signals transmitted between the CPU and South Bridge may also be sent on the lines interconnecting the HIC and PIC, such as lines PCN and PCNR. For example, CPU interface signals such as CPU interrupt (INTR), Address 20 Mask (A20M#), Non-Maskable Interrupt (NMI), System Management Interrupt (SMI#), and Stop Clock (STPCLK#), may be translated into bit information and transmitted on the XPBus between the HIC and the PIC.

[0124] Fig. 14 is a table showing the information transmitted on the XPBus during four clock cycles of the XPBus in another embodiment of the present invention where 10 data bits are transmitted in each clock cycle of the XPBus. In this embodiment, the XPBus clock rate is twice as large as the PCI clock rate. This allows sending data and address bits every other XPBus cycle. As can be seen in Fig. 14, there are no address or data bits transmitted during the second or fourth XPBus clock cycle. The fact that the XPBus clock rate is higher than the PCI clock rate allows for compatibility of the XPBus with possible future expansions in the performance of PCI bus to higher data transfer and clock rates.

[0125] In the embodiment shown in Fig. 14, there are 18 control bits, CN0 to CN17, transmitted in every two XPBus clock cycles. The first bit transmitted on the control line in each XPBus clock cycle indicates whether control bits CN0 to CN8 or control bits CN9 to CN17 will be transmitted in that cycle. A zero sent at the beginning of a cycle on the control line indicates that CN0 to CN8 will be transmitted during that cycle, whereas a one sent at the beginning of a cycle on the control line indicates that CN9 to CN17 will be transmitted during that cycle. These bits also indicate the presence or absence of data and address bits during that cycle. A zero indicates that address or data bits will be transmitted during that cycle whereas a one indicates that no address or data bits will be transmitted during that cycle.

[0126] In one embodiment, BS0 and BS1 are used to encode the PCI signals FRAME# and IRDY#, respectively. Additionally, in one embodiment, BS2 and BS3 are used to indicate the clock speed of the computer bus interface and the type of computer bus interface, respectively. For example, BS2 value of zero may indicate that a 33 MHz PCI bus of 32 bits is used whereas a BS2 value of one may indicate that a 66 MHz PCI bus of 32 bits is used. Similarly, a BS3 value of zero may indicate that a PCI bus is used whereas a BS3 value of one may indicate that another computer interface bus, such as an Institute of Electronics & Electrical Engineers (IEEE) 1394 bus, is used.

[0127] Fig. 15 is a schematic diagram of lines PCK, PD0 to PD3, and PCN. These lines are unidirectional LVDS lines for transmitting clock signals and bits such as those shown in FIGS. 13 and 14 from the HIC to the PIC. The bits on the PD0 to PD3 and the PCN lines are sent synchronously within every clock cycle of the PCK. Another set of lines, namely PCKR, PDR0 to PDR3, and PCNR, are used to transmit clock signals and bits from the PIC to HIC. The lines used for transmitting information from the PIC to the HIC have the same structure as those shown in Fig. 15, except that they transmit data in a direction opposite to that in which the lines shown in Fig. 15 transmit data. In other words they transmit information from the PIC to the HIC. The bits on the PDR0 to PDR3 and the PCNR lines are sent synchronously within every clock cycle of the PCKR. Some of the examples of control information that may be sent in the reverse direction, i.e., on PCNR line, include a request to switch data bus direction because of a pending operation (such as read data available), a control signal change in the target requiring communication in the reverse direction, target busy, and transmission error detected.

[0128] The XPBus which includes lines PCK, PD0 to PD3, PCN, PCKR, PDR0 to PDR3, and PCNR, has two sets of unidirectional lines transmitting clock signals and bits in opposite directions. The first set of unidirectional lines includes PCK, PD0 to PD3, and PCN. The second set of unidirectional lines includes PCKR, PDR0 to PDR3, and PCNR. Each of these unidirectional set of lines is a point-to-point bus with a fixed transmitter and receiver, or in other words a fixed master and slave bus. For the first set of unidirectional lines, the HIC is a fixed transmitter/master whereas the PIC is a fixed receiver/slave. For the second set of unidirectional lines, the PIC is a fixed transmitter/master whereas the HIC is a fixed receiver/slave. The LVDS lines of XPBus, a cable friendly and remote system I/O bus, transmit fixed length data packets within a clock cycle.

[0129] The XPBus lines, PD0 to PD3, PCN, PDR0 to PDR3 and PCNR, and the video data and clock lines, VPD and VPCK, are not limited to being LVDS lines, as they may be other forms of bit based lines. For example, in another embodiment, the XPBus lines may be IEEE 1394 lines.

[0130] It is to be noted that although each of the lines PCK, PD0 to PD3, PCN, PCKR, PDR0 to PDR3, PCNR, VPCK, and VPD is referred to as a line, in the singular rather than plural. each such line may contain more than one physical line. For example, in the embodiment shown in Fig. 23, each of lines PCK, PD0 to PD3 and PCN includes two physical lines between each driver and its corresponding receiver. The term line, when not directly preceded by the terms physical or conductive, is herein used interchangeably with a signal or bit channel which may consist of one or more physical lines for transmitting a signal. In the case of non-differential signal lines, generally only one physical line is used to transmit one signal. However, in the case of differential signal lines, a pair of physical lines is used to transmit one signal. For example, a bit line or bit channel in an LVDS or IEEE 1394 interface consists of a pair of physical lines which together transmit a signal.

[0131] A bit based line (i.e., a bit line) is a line for transmitting serial bits. Bit based lines typically transmit bit packets and use a serial data packet protocol. Examples of bit lines include an LVDS line, an IEEE 1394 line, and a Universal Serial Bus (USB) line.

[0132] Fig. 16 is a table showing the names, types, number of pins dedicated to, and the description of the primary bus PCI signals. The pins represent those between the host PCI bus and the HIC.

[0133] FIG. 17 is a block diagram of the components in one computer system employing the present invention. The computer system comprises an attached computer module (ACM), a peripheral console (PCON), and the interconnection apparatus between them. The ACM includes the central processing unit (CPU) 1710, system memory 1720, high performance devices 1750, primary mass storage 1730, and related interface and support circuitry 1740. The PCON includes primary display 1810, primary input 1820, secondary mass storage 1750, other devices 1860, expansion slots 1870, the primary power supply 1830, and related interface and support circuitry 1840. The interconnection apparatus 1900 includes circuitry to convey power and operational signals between the ACM and PCON.

[0134] Within the ACM 1700, the CPU 1710 executes instructions and manipulates data stored in the system memory. The CPU 1710 and system memory 1720 represent the user's core computing power. The core computing power may also include high performance devices 1750 such as advanced graphics processor chips that greatly increase overall system performance and which, because of their speed, need to be located close to the CPU. The primary mass storage 1730 contains persistent copies of the operating system software, application software, configuration data, and user data. The software and data stored in the primary mass storage device represent the user's computing environment. Interface and support circuitry 1740 primarily includes interface chips and signal busses that interconnect the CPU, system memory, high performance devices, and primary mass storage. The interface and support circuitry also connects ACM-resident components with the ACM-to-PCON interconnection apparatus as needed.

[0135] Within the PCON 1800, the primary display component 1810 may include an integrated display device or connection circuitry for an external display device. This primary display device may be, for example, an LCD, plasma, or CRT display screen used to display text and graphics to the user for interaction with the operating system and application software. The primary display component is the primary output of the computer system, i.e., the paramount vehicle by which programs executing on the CPU can communicate toward the user.

[0136] The primary input component 1820 of the PCON may include an integrated input device or connection circuitry for attachment to an external input device. The primary input may be, for example, a keyboard, touch screen, keypad, mouse, trackball, digitizing pad, or some combination thereof to enable the user to interact with the operating system and application software. The primary input component is the paramount vehicle by which programs executing on the CPU receive signals from the user.

[0137] The PCON may contain secondary mass storage 1850 to provide additional high capacity storage for data and software. Secondary mass storage may have fixed or removable media and may include, for example, devices such as diskette drives, hard disks, CD-ROM drives, DVD drives, and tape drives.

[0138] The PCON may be enhanced with additional capability through the use of integrated “Other Devices” 1860 or add-on cards inserted into the PCON’s expansion slots 1870. Examples of additional capability include sound generators, LAN connections, and modems. Interface and support circuitry 1840 primarily includes interface chips, driver chips, and signal busses that interconnect the other components within the PCON. The interface and support circuitry also connects PCON-resident components with the ACM-to-PCON interconnection apparatus as needed.

[0139] Importantly, the PCON houses the primary power supply 1830. The primary power supply has sufficient capacity to power both the PCON and the ACM 1700 for normal operation. Note that the ACM may include a secondary “power supply” in the form, for example, of a small battery. Such a power supply would be included in the ACM to maintain, for example, a time-of-day clock, configuration settings when the ACM is not attached to a PCON, or machine state when moving an active ACM immediately from one PCON to another. The total energy stored in such a battery would, however, be insufficient to sustain operation of the CPU at its rated speed, along with the memory and primary mass storage, for more than a fraction of an hour, if the battery were able to deliver the required level of electrical current at all.

[0140] FIG. 18 is a block diagram of an attached computing module (ACM) 1700. The physical ACM package 1700 contains the ACM functional components 1701 and the ACM side of the ACM-to-PCON Interconnection 1900. The ACM 1701 comprises a

CPU component 1710, a system memory component 1720, a primary mass storage component 1730, a high performance devices components 1750, and an interface and support component 1740.

[0141] The ACM side of the ACM-to-PCON Interconnection 1900 comprises a Host Interface Controller (HIC) component 1920 and an ACM connector component 1930. The HIC 1920 and connector 1930 components couple the ACM functional components 1700 with the signals of an ACM-to-PCON interface bus 1910 used to operatively connect an ACM with a PCON. The ACM-to-PCON interface bus 1910 comprises conveyance for electrical power 1914 and signals for a peripheral bus 1912, video 1916, video port 1917, and console type 1918. The preferred ACM-to-PCON Interconnection 1900 is described in detail in a companion U.S. patent application, Ser. No. 09/149,882, entitled "A Communication Channel and Interface Devices for Bridging Computer Interface Buses," by the same inventor, filed on the same day herewith, and hereby incorporated by reference. The preferred ACM-to-PCON interconnection 1900 includes circuitry to transmit and receive parallel bus information from multiple signal paths as a serial bit stream on a single signal path. This reduces the number of physical signal paths required to traverse the interconnection 1900. Further, employing low-voltage differential signaling (LVDS) on the bit stream data paths provides very reliable, high-speed transmission across cables. This represents a further advantage of the present invention.

[0142] The CPU component 1710 of the ACM functional circuitry 1701 of the presently described embodiment comprises a microprocessor 1712, which is the chief component of the personal computer system, power supply connection point 1713, and cache memory 1714 tightly coupled to the microprocessor 1712 by the CPU-to-cache bus 1714 comprising signal paths for address, data, and control information. The microprocessor 1712 of this embodiment is one of the models from the Pentium II family of processors from Intel Corporation. Microprocessor 1712 receives electrical power from power bus 1768 via connection point 1713. Microprocessor 1712 couples to the Host Interface Controller (HIC) 1920 via CPU-to-HIC bus 1763 comprising signal paths to exchange control information such as an interrupt request. Microprocessor 1712 also couples to CPU Bridge 1746 via CPU main bus 1764 comprising signal paths for address, data, and control information.

[0143] The CPU Bridge component 1746 of the interface and support circuitry 1740 operates to couple the high speed CPU main bus 1764 to specialty buses of varying speeds and capability that connect other computer components. The CPU Bridge of the presently described embodiment incorporates memory controller circuitry, advanced graphics processor support circuitry, and a general, industry-standard PCI bus controller in a single package. A CPU Bridge 1746 such as the 82443LX PCI/AGP Controller from Intel Corporation may be used.

[0144] The system memory component 1720 of the ACM functional circuitry 1701 in the present embodiment comprises main system memory (RAM) 1722, BIOS memory 1724, and flash memory 1726. The system memory 1720 is used to contain data and instructions that are directly addressable by the CPU. The RAM 1722 comprises volatile memory devices such as DRAM or SDRAM memory chips that do not retain their stored contents when power is removed. This form of memory represents the largest proportion of total system memory 1720 capacity. The BIOS memory 1724 comprises non-volatile memory devices such as ROM or EPROM memory chips that retain their stored contents regardless of the application of power and are read-only memory under normal operating conditions. The BIOS memory 1724 stores, for example, start-up instructions for the microprocessor 1712 and sets of instructions for rudimentary input/output tasks. The flash memory 1726 comprises non-volatile memory devices that retain their stored contents regardless of the application of power. Unlike the BIOS non-volatile memory, however, the stored contents of the flash memory 1726 are easily changed under normal operating conditions. The flash memory 1726 may be used to store status and configuration data, such as security identifiers or ACM specifications like the speed of the microprocessor 1712. Some embodiments may combine the BIOS functions into the flash memory device, thus permitting BIOS contents to be rewritten, improving field upgradability.

[0145] The main system memory (RAM) 1722 is coupled to memory controller circuitry resident within the CPU Bridge 1746 via direct memory bus 1765. The BIOS 1724 and flash memory 1726 are coupled to HIC 1920 via switched memory bus 1766. This permits the BIOS 1724 and flash 1726 memories to be accessed by circuitry in the HIC 1920 or other circuitry connected thereto. The direct memory bus 1765 and the

switch memory bus 1766 each comprises conductors to convey signals for data, address, and control information.

[0146] The primary mass storage component 1730 of the ACM functional circuitry 1701 in the present embodiment comprises a compact hard disk drive with an industry-standard, IDE interface. The hard disk drive (HDD) 1732 has a formatted storage capacity sufficient to contain an operating system for the computer, application software desired by the user, and related user configuration and operating parameter data. The HDD 1732 in the present embodiment serves as the “boot” device for the personal computer from which the operating system is loaded into RAM 1722 by the start-up program stored in the BIOS 1724.

[0147] The present HDD 1732 has a capacity of approximately 2,000 megabytes to provide adequate storage for common software configurations and reasonable space for user data. One example of a common software configuration includes the Windows 95 operating system from Microsoft Corporation, a word processing program, a spreadsheet program, a presentation graphics program, a database program, an email program, and a web browser such as Navigator from Netscape Corporation. The hard disk 1732 stores program and data files for each software component, including files distributed by the vendor as well as files created or updated by operation of the software after it is installed. For example, a word processor program may maintain information about a user’s identity and latest preferences in an operating system registry file. Or, for example, the web browser may maintain a file of the user’s favorite web sites or most recently viewed web pages. An HDD with 2000 megabyte capacity is readily available in the small size of hard disk (e.g., 2.5-inch or 3.5-inch) to minimize the space required within the ACM for the primary mass storage device 1730.

[0148] The HDD 1732 is coupled to IDE controller circuitry 1748 via IDE bus 1772. The IDE controller circuitry 1748 is coupled to the CPU Bridge 1746 via the Host PCI bus 1767. IDE controllers and busses, and the PCI bus are well known and understood in the industry. The above components operate together to couple the hard disk drive 1732 to the microprocessor 1712.

[0149] The high performance devices component 1750 of the ACM functional circuitry 1701 in the present embodiment comprises an Advanced Graphics Processor (AGP) 1752.

The Model 740 Graphics Device from Intel Corporation may be used in the present embodiment as the AGP.

[0150] Increases in computer screen size, graphics resolution, color depth, and visual motion frame rates, used by operating system and application software alike, have increased the computing power required to generate and maintain computer screen displays. An AGP removes a substantial portion of the graphics computing burden from the CPU to the specialized high-performance processor, but a high level of interaction between the CPU and the specialized processor is nonetheless required. To maximize the effective contribution of having a specialized processor in the presently described embodiment, the AGP 1752 is located in the ACM 1700, where it is in close proximity to the microprocessor 1712. The AGP 1752 is coupled to the microprocessor 1712 via the advanced graphics port bus 1773 of the CPU Bridge 1746. The visual display signal generated by the AGP are conveyed toward actual display devices at the peripheral console (PCON) via video signal bus 1770. Video information from a source external to the ACM and appearing as video port signals 1917 may be conveyed to the AGP 1752 via video port signal path 1771.

[0151] Other types of high performance components may be included in different ACM configurations. For example, an interface to an extremely high speed data communication facility may be desirable in some future computer where CPU-to-network interaction is of comparable intensity to today's CPU-to-graphics interaction. Because such high performance components tend to be high in cost, their inclusion in the ACM is desirable. Inclusion of high cost, high performance components in the ACM concentrates a user's core computing power and environment in a portable package. This represents a further advantage of the invention.

[0152] The interface and support component 1740 of the ACM functional circuitry 1701 in the present embodiment comprises circuitry for power regulation 1742, clocking 1744, CPU Bridge 1746, IDE controller 1748, and signal conveyance paths 1761-1774. The CPU Bridge 1746 couples the CPU component 1710 of the ACM 1700 with the other components of the ACM 1720-1750 and the CPU-to-PCON Interconnection 1900. The CPU Bridge 1746 and IDE controller 1748 have already been discussed. Power regulation circuitry 1742 receives electrical power via the electrical power conduction path 1914 of the CPU-to-PCON Interconnection 1900, conditions and distributes it to the

other circuitry in the ACM using power distribution bus 1768. Such regulation and distribution is well known and understood in the art.

[0153] Clocking circuitry 1744 generates clock signals for distribution to other components within the ACM 1700 that require a timing and synchronization clock source. The CPU 1710 is one such component. Often, the total power dissipated by a CPU is directly proportional to the frequency of its main clock signal. The presently described embodiment of the ACM 1700 includes circuitry that can vary the frequency of the main CPU clock signal conveyed to the CPU via signal path 1762, in response to a signal received from the host interface controller (HIC) 1920 via signal path 1761. The generation and variable frequency control of clocking signals is well understood in the art. By varying the frequency, the power consumption of the CPU (and thus the entire ACM) can be varied.

[0154] The variable clock rate generation may be exploited to match the CPU power consumption to the available electrical power. Circuitry in the host interface controller (HIC) 1920 of the presently described embodiment adjusts the frequency control signal sent via signal path 1761 to the clocking circuitry 1744, based on the “console type” information signal 1918 conveyed from the peripheral console (PCON) by the CPU-to-PCON interconnection 1900. In this arrangement, the console type signal originating from a desktop PCON would result in the generation of a maximum speed CPU clock. The desktop PCON, presumably has unlimited power from an electrical wall outlet and does not need to sacrifice speed for power conservation. The console type signal originating from a notebook PCON would, however, result in the generation of a CPU clock speed reduced from the maximum in order to conserve battery power and extend the duration of computer operation obtained from the energy stored in the battery. The console type signal originating from a notepad PCON would result in the generation of a CPU clock speed reduced further yet, the notepad PCON presumably having smaller batteries than the notebook PCON. Inclusion of control signals and circuitry to effect a CPU clock signal varying in frequency according to characteristics of the PCON to which the ACM is connected facilitates the movement of the user’s core computing power and environment to different work settings, which is a further advantage of the present invention.

[0155] FIG. 19 illustrates an external view of one embodiment of an ACM. The case 2010 of the ACM 1700 is generally rectangular in shape, preferably constructed of a strong, lightweight, rigid material that will protect the internal components from mechanical and environmental exposure. Plastics may readily be used to construct the case 2010. The case 2010 completely surrounds the internal components, being generally an 8-sided box. FIG. 19 shows the top 2012, right 2014, and rear 2016 surfaces of the ACM case 2010. Rear edges 2018 of the case joining the rear surface 2016 with its adjoining surfaces may be beveled or rounded to facilitate insertion of the ACM 1700 into the computer bay of the PCON. Notches 2040 may be formed by projecting small surfaces inward from otherwise generally flat surfaces of the ACM case 2010. The notches 2040 may be used to engage with mechanical devices mounted in and about a computer bay. Such mechanical devices can be employed to secure the ACM into position within a computer bay for reliability and security. Openings 2017 are formed into the rear surface 2016 of the ACM case 2010 through which to project connectors 1930a and 1930b. In one embodiment the case 2010 is approximately 5.75 inches wide by 6.5 inches deep by 1.6 inches high.

[0156] Connectors 1930a and 1930b are part of the ACM-to-PCON Interconnection as described earlier in reference to FIGS. 3 and 4. When the ACM 1700 is inserted into the computer bay of a peripheral console (PCON), connectors 1930a and 1930b mate with corresponding connectors located at the rear of the computer bay to electrically couple the ACM with the PCON containing the computer bay. Details concerning the ACM-to-PCON Interconnection can be found in the U.S. patent application entitled “A Communication Channel and Interface Devices for Bridging Computer Interface Buses,” already incorporated herein by reference. The connectors 1930a and 1930b used in one embodiment are connectors complying with the Device Bay industry standard as documented in “Device Bay Interface Specification,” revision 0.85, Feb. 6, 1998. Such connectors have specifically been designed to stand up to the rigors of repeated insertion and withdrawal.

[0157] Cooling plate 2030 forms part of the top surface 2012 of ACM 1700. The cooling plate 2030 may be mounted to, or project through an opening formed in, case 2010. Similarly, electromagnetic interference (EMI)/electrostatic discharge (ESD) grounding plate 2032 forms part of the right surface 2014 of ACM 1700. The grounding

plate 2032 may be mounted to, or project through an opening formed in, case 2010. Cooling plate 2030 and grounding plate 2032 compressively mate with counterparts when the ACM is fully inserted into the computer bay. The counterparts located along the boundaries of the computer bay conduct dangerous heat and electrical charges away from the ACM. Inside the ACM, cooling plate 2030 thermally couples to heat-sensitive components such as CPU 1710 by methods well known in the art. Similarly, grounding plate 2032 electrically couples to EMI/ESD-sensitive components, such as a microprocessor, by methods well known in the art.

[0158] LCD display 2050 forms part of the right surface 2014 of ACM 1700. The LCD display may be mounted to, or project through an opening formed in, case 2010. The LCD display may contain indicators about the status of the ACM. Such indicators may display, for example, the time-of-day from a time-of-day clock contained within the ACM, or the amount of charge remaining in an ACM-resident battery, or certain configuration options recorded in flash memory. The LCD display 2050 provides display capability for a limited amount of information, most useful when the ACM is separated from a PCON (and is thus separated from a full-capability, primary display device).

[0159] FIG. 19b illustrates one possible embodiment of a computer bay. A computer bay 1890 acts as a receptacle for lodging an ACM (such as the one shown in FIG. 20) within a desktop PCON. The illustrated computer bay 1890 provides an ACM with housing and with signal flow, electrical grounding, heat transfer, and mechanical connections. While many physical arrangements between the ACM and PCON are possible, the use of an enclosed computer bay as the one illustrated in FIG. 20b offers many advantages. For example, the illustrated computer bay 1890 provides physical protection for the ACM. The computer bay may also be easily incorporated into industry standard form factors used in the manufacture of desktop personal computers (e.g., the ACM and associated computer bay could be designed to fit within the volume occupied by a standard-size disk drive).

[0160] The computer bay 1890 appearing in FIG. 20b is shown mounted within the confines of PCON case 1802. The computer bay 1890 comprises frame 1891 and signal flow, grounding, cooling, and locking components as described below. Mounting flanges 1898 of frame 1891 may be used to attach the computer bay 1890 to the PCON structure. The computer bay 1890 is prominently defined by frame 1891 generally forming a cavity

in which to lodge an ACM. As such, the interior cavity formed by frame 1891 closely approximates the exterior dimensions of a compatible ACM. The top 1893, right 1894, and rear 1895 sides of the computer bay frame 1891 are visible. The computer bay frame 1891 also includes substantial bottom and left sides which are not shown. The front side of the frame 1891 (not shown) is open to allow the insertion of the ACM. Frame 1891 is constructed of metal for strength and to facilitate the conductance of heat and undesired electrical currents away from the ACM.

[0161] In the presently described embodiment, the weight of an inserted ACM is largely borne by the bottom side (not shown) of computer bay frame 1891. Alternative embodiments are possible where, for example, the weight of the ACM is borne by rails running longitudinally down the right and left sides of the computer bay cavity that engage corresponding grooves running longitudinally down the right and left sides of an ACM.

[0162] FIG. 20 illustrates the internal component layout for one embodiment of an ACM. All components are contained within the confines of the ACM case 510, except for connectors 1930a and 1930b which extend from the rear of the ACM 1700 to engage mating connectors (not shown) that will couple the ACM circuitry with the PCON circuitry. Main circuit board 2110 provides electrical connections for circuitry within the ACM and mounting for many of its components 1724, 1722, 17221, 1752, 1742, 1748, 1920, and 1930. The fabrication and use of such circuits boards is well known and understood in the art. Connector 2122 is also mounted on main circuit board 2110 and mates with mobile processor module 2120. Mobile processor module 2120 represents a form of packaging for a microprocessor and related components. The illustrated mobile processor module 2120 is a self-contained unit that includes a microprocessor 1712, CPU cache 1714, and CPU bridge 1746 operatively interconnected by the manufacturer. An example of one such module is the Pentium Processor with MMX Technology Mobile Module from Intel Corporation (order number 24 3515-001, September 1997). One skilled in the art recognizes that discrete microprocessor, cache, and bridge could have been employed and mounted directly to the main circuit board.

[0163] The mobile processor module 2120 blocks the view, from the top, of the system BIOS 1724. Similarly, hard disk drive 1732 hides RAM memory 1722, the high performance graphics processor 1752, the host interface controller 1920, and flash

memory 1726. Memory upgrade socket 2130 remains exposed to facilitate installation of additional RAM memory 1722. Power regulator 1742, like the memory upgrade socket, enjoys a generous amount of overhead clearance to accommodate its vertical size. The area including IDE controller 1748 also enjoys overhead clearance to facilitate a cable connection with the hard disk drive 1732.

[0164] The functional interconnection and operation of components contained within the ACM and depicted in FIG. 20 has already been described in relation to FIG. 18 for like numbered items appearing therein.

[0165] FIG. 21 is a block diagram of a peripheral console (PCON). A peripheral console couples with an ACM to form an operating personal computer system. The peripheral console (PCON) supplies an ACM with primary input, display, and power supply; the ACM supplies the core computing power and environment of the user. In the presently described embodiment the physical PCON package 200 contains the PCON functional components 1801 and the PCON side of the ACM-to-PCON Interconnection 1900. The PCON functional components 1801 comprise primary display 1810, a primary input 1820, a primary power supply 1830, interface and support 1840, secondary mass storage 1850, other devices 1860, and expansion slots 1870.

[0166] The PCON side of the ACM-to-PCON Interconnection 1900 comprises a Peripheral Interface Controller (PIC) component 1940, a PCON connector component 1950, console-type component 1942, and flash memory device 1948. The PIC 1940 and connector 1950 components couple the PCON functional components 1801 with the signals of an ACM-to-PCON interface bus 1910 used to operatively connect an ACM with a PCON. The ACM-to-PCON interface bus 1910 comprises conveyance for electrical power 1914 and signals for a peripheral bus 1912, video 1916, video port 1917, and console-type 1918. The preferred ACM-to-PCON Interconnection 1900 is described in detail in the U.S. patent application entitled “A Communication Channel and Interface Devices for Bridging Computer Interface Buses,” already incorporated herein by reference.

[0167] Connector component 1950 may be selected to mate directly with the connector component 1930 of an ACM (shown in FIG. 18). Alternatively, connector component 1950 may be selected to mate with, for example, the connector on one end of a cable

intervening between the PCON and an ACM in a particular embodiment, such as cable 1964 shown in FIG. 19B. The ACM-to-PCON interconnection described in the aforementioned companion patent application has the advantage of providing reliable signal conveyance across low cost cables.

[0168] Flash memory device 1948 provides non-volatile storage. This storage may be accessible to devices in both the ACM and the PCON, including the host interface controller and the peripheral interface controller to which it is connected. As such, flash memory 1948 may be used to store configuration and security data to facilitate an intelligent mating between an ACM and a PCON that needs no participation of the CPU.

[0169] The primary display component 1810 of the PCON functional circuitry 1801 of the presently described embodiment comprises integrated display panel 1812 and video connector 1813. Integrated display panel 1812 is a color LCD display panel having a resolution of 640 horizontal by 480 vertical pixels. 640-by-480 resolution is popularly considered to be the minimum screen size to make practical use of the application software in widespread use today. One skilled in the art recognizes that the type and resolution of the display can vary greatly from embodiment to embodiment, depending on factors such as cost and intended application. Any display device may be used, without departing from the scope and spirit of the invention, that provides principal visual output to the computer user for operating system and application software executing in its customary and intended fashion using the CPU component (1710 of FIG. 17) of an ACM presently coupled to PCON 1800.

[0170] Integrated display panel 1812 is coupled to video signal bus 1849 and displays a screen image in response to video signals presented on bus 1849. Certain pins of connector 1950 receive video output signals 1916 of the ACM-to-PCON interface bus 1910 from a mated connector that is coupled to an ACM. These certain pins of connector 1950 couple to video signal bus 1849 which conveys the video output signals 316 throughout the PCON 1800 as needed. Video connector 1813 is exposed at the exterior of PCON 1800 and couples to video signal bus 1849. Connector 1813 permits easy attachment of an external display device that is compatible with the signals carried by bus 1849, such as a CRT monitor (not shown). The external display device may be used in addition, or as an alternative, to integrated display panel 1812.

[0171] The isolation of the relatively heavy and sizable primary display 1810 from the core computing power and user environment contained within an ACM represents a further advantage of the present invention.

[0172] The primary input component 1820 of the PCON functional circuitry 1801 of the presently described embodiment comprises keyboard interface circuitry 1822, keyboard connector 1823, pointer interface circuitry 1824, and pointer connector 1825. Keyboard interface circuitry 1822 and pointer interface circuitry 1824 connect to ISA bus 1845 and are thereby coupled to the CPU component (1710 of FIG. 17) of any ACM attached to PCON 1800. Keyboard interface circuitry 1822 interfaces a standard computer keyboard (not shown), attached at connector 1823, to ISA bus 1845. Pointer interface circuitry 1822 interfaces a standard computer pointing device (not shown), such as a computer mouse attached at connector 1825, to ISA bus 1845. Computer keyboards, pointing devices, connectors 1823, 1825, keyboard interface circuitry 1822, and pointer interface circuitry 1824 are well known in the art. The isolation of the relatively heavy and sizable primary input devices 1820 from the core computing power and user environment contained within an ACM represents a further advantage of the present invention.

[0173] The primary power supply component 1830 of the PCON functional circuitry 1801 of the presently described embodiment provides electrical energy for the sustained, normal operation of the PCON 1800 and any ACM coupled to connector 1950. The power supply may be of the switching variety well known in the art that receives electrical energy from an AC source 1889, such as a wall outlet. Power supply 1830 reduces the alternating current input voltage, to a number of distinct outputs of differing voltages and current capacities. The outputs of power supply 1830 are applied to power bus 1831. Power bus 1831 distributes the power supply outputs to the other circuitry within the PCON 1800. Bus 1831 also connects to certain pins of connector 1950 to provide the electrical power 1914 for an ACM conveyed by ACM-to-PCON interconnection 1900. The isolation of the usually heavy power supply 1830 from the core computing power and user environment contained within the ACM represents a further advantage of the present invention.

[0174] The interface and support component 1840 of the PCON functional circuitry 1801 of the presently described embodiment comprises peripheral bridge 1846, diskette controller 1842, IDE controller 1848, and signal conveyance paths 1841, 1843, 1844,

1845, 1847 and 1849. Peripheral bridge 1846 couples PCI peripheral bus 1841 with peripheral busses of other formats such as ISA peripheral bus 1845 and others 1847. PCI and ISA peripheral busses are industry standards, well known and understood in the art. Other peripheral busses 1847 may include, for example, a bus compliant with the universal serial bus (USB) industry standard. While other embodiments of a peripheral console 1800 may include a single peripheral bus that is coupled to an attached ACM via ACM-to-PCON interconnection 1900, such as PCI bus 1841, this embodiment includes peripheral bridge 1846 to establish additional busses 1845, 1847. The additional busses 1845, 1847 permit the use of the many low-cost and readily available components compatible with these bus specifications.

[0175] Diskette controller 1842 interfaces a floppy disk drive 1854 with the CPU component 1710 of an attached ACM (shown in FIG. 18) so that the CPU may control and use the diskette drive 1854 hardware to store and retrieve data. Diskette controller 1842 couples to the CPU via a connection to ISA bus 1845. Diskette controller 1842 connects to the diskette drive 1854 via one of device cables 1843.

[0176] Similarly, IDE controller 1848 interfaces a hard disk drive 1852 and a CDROM drive 1856 with the CPU component 1710 of an attached ACM (shown in FIG. 18) so that the CPU may control and use the hard disk drive 1852 and CDROM 1856 hardware to store and retrieve data. IDE controller 1848 couples to the CPU via connection to PCI peripheral bus 1841. IDE controller 1848 connects to each of hard disk drive 1852 and CD-ROM drive 1856 via one of device cables 1843. Some embodiments of PCON 1800 may take advantage of VLSI integrated circuits such as an 82371SB (PIIX4) integrated circuit from Intel Corporation. An 82371SB integrated circuit includes circuitry for both the peripheral bridge 1846 and the IDE controller 1848 in a single package.

[0177] The secondary mass storage component 1850 of the PCON functional circuitry 1801 of the presently described embodiment comprises diskette drive 1854, hard disk drive 1852, and CD-ROM drive 1856. Secondary mass storage 1850 generally provides low-cost, non-volatile storage for data files which may include software program files. Data files stored on secondary mass storage 1850 are not part of a computer user's core computing power and environment. Secondary mass storage 1850 may be used to store, for example, seldom used software programs, software programs that are used only with companion hardware devices installed in the same peripheral console 1800, or archival

copies of data files that are maintained in primary mass storage 1750 of an ACM (shown in FIG. 18). Storage capacities for secondary mass storage 1850 devices may vary from the 1.44 megabytes of the 3.5-inch high density diskette drive 1854, to more than 10 gigabytes for a large format (5-inch) hard disk drive 1852. Hard disk drive 1852 employs fixed recording media, while diskette drive 1854 and CD-ROM drive 1856 employ removable media. Diskette drive 1854 and hard disk drive 1852 support both read and write operations (i.e., data stored on their recording media may be both recalled and modified) while CD-ROM drive 1856 supports only read operations.

[0178] The other devices component 1860 of the PCON functional circuitry 1801 of the presently described embodiment comprises a video capture card. A video capture card accepts analog television signals, such as those complying with the NTSC standard used for television broadcast in the United States, and digitizes picture frames represented by the analog signal for processing by the computer. Video capture cards at present are considered a specialty, i.e., not ubiquitous, component of personal computer systems. Digitized picture information from video capture card 1860 is carried via signal conveyance path 1844 to the peripheral interface controller 1940 which transforms it to the video port signals 1917 of the ACM-to-PCON interconnection 1900 for coupling to the advanced graphics processor 1752 in an attached ACM (shown in FIG. 18).

[0179] Video capture card 1860 is merely representative of the many types of “other” devices that may be installed in a PCON to expand the capabilities of the personal computer. Sound cards and laboratory data acquisition cards are other examples. Video capture card 1860 is shown installed in one of expansion slots 1870 for coupling to the interface and control circuitry 1840 of the PCON. Any of other devices 1860 could be coupled to the interface and control circuitry 1840 of the PCON by different means, such as direct installation on the circuit board that includes the interface and control circuitry 1840; e.g., a motherboard.

[0180] The expansion slots component 1870 of the PCON functional circuitry 1801 of the presently described embodiment comprises PCI connectors 1871 and ISA connectors 1872. A circuit card may be inserted into one of the connectors 1871, 1872 in order to be operatively coupled with the CPU 1710 of an attached ACM (shown in FIG. 18). Each of connectors 1871 electrically connects to PCI bus 1841, and may receive and hold a printed circuit card which it electrically couples to PCI bus 1841. Each of connectors

1872 electrically connects to ISA bus 1845, and may receive and hold a printed circuit card which it electrically couples to ISA bus 1845. The PCI 1841 and ISA 1845 busses couple to the CPU 1710 of an attached ACM (shown in FIG. 18) by circuitry already described.

[0181] An embodiment of a detachable computing module in accordance with the present invention, for attachment to a peripheral console for forming a fully operational computer system, comprises, an enclosure, a CPU, a memory coupled to said CPU, and a mass storage coupled to said CPU. The module further comprises interconnection circuitry coupled to said CPU, said interconnection circuitry connectable to a peripheral console. The CPU is uncoupled from any primary input circuitry when said interconnection circuitry is disconnected from a peripheral console.

[0182] An alternative embodiment of a detachable computing module in accordance with the present invention, for attachment to a peripheral console for forming a fully operational computer system, comprises an enclosure, a CPU, a memory coupled to said CPU, and a mass storage coupled to said CPU. The module further comprises interconnection circuitry coupled to said CPU, said interconnection circuitry connectable to a peripheral console. The CPU is uncoupled from any primary output circuitry when said interconnection circuitry is disconnected from a peripheral console.

[0183] Various modifications to the preferred embodiment can be made without departing from the spirit and scope of the invention. (A limited number of modifications have already been described in the preceding discussion.) For example, a particular embodiment may insert another layer of bus bridging between the CPU bridge and the Peripheral bridge. This may be desirable if, for example, a vendor wants to implement a proprietary, general-purpose bus having intermediate performance characteristics that fall between those of the high-performance general purpose bus originating at the CPU, and the slower general purpose PCI bus. Thus, the foregoing description is not intended to limit the invention as set forth.

[0184] In most embodiments, the ACM includes an enclosure such as the one described with the following components, which should not be limiting:

- 1) A CPU with cache memory;
- 2) Core logic device or means;

- 3) Main memory;
- 4) A single primary Hard Disk Drive (“HDD”) that has a security program;
- 5) Flash memory with system BIOS and programmable user password;
- 6) Operating System, application software, data files on primary HDD;
- 7) An interface device and connectors to peripheral console;
- 8) A software controllable mechanical lock, lock control means, and other accessories.

[0185] The ACM connects to a peripheral console with power supply, a display device, an input device, and other elements. Some details of these elements with the present security system are described in more detail below.

[0186] FIG. 22 is a simplified layout diagram of a security system for a computer system according to an embodiment of the present invention. This diagram is merely an illustration and should not limit the scope of the claims herein. One of ordinary skill in the art would recognize other variations, modifications, and alternatives. The layout diagram illustrates the top-view of the module 22, where the backside components (e.g., Host Interface Controller) are depicted in dashed lines. The layout diagram has a first portion, which includes a central processing unit (“CPU”) module 2200, and a second portion, which includes a hard drive module 2220. A common printed circuit board 2237 houses these modules and the like. Among other features, the ACM includes the central processing unit module 2200 with a cache memory 2205, which is coupled to a north bridge unit 2221, and a host interface controller 2201. The host interface controller includes a lock control 2203. As shown, the CPU module is disposed on a first portion of the attached computer module, and couples to connectors 2217. Here, the CPU module is spatially located near connector 2217.

[0187] The CPU module can use a suitable microprocessing unit, microcontroller, digital signal processor, and the like. In a specific embodiment, the CPU module uses, for example, a 400 MHz Pentium II microprocessor module from Intel Corporation and like microprocessors from AMD Corporation, Cyrix Corporation (now National Semiconductor Corporation), and others. In other aspects, the microprocessor can be one such as the Compaq Computer Corporation Alpha Chip, Apple Computer Corporation PowerPC G3 processor, and the like. Further, higher speed processors are contemplated in other embodiments as technology increases in the future.

[0188] In the CPU module, host interface controller 2201 is coupled to BIOS/flash memory 2205. Additionally, the host interface controller is coupled to a clock control logic, a configuration signal, and a peripheral bus. The present invention has a host interface controller that has lock control 2203 to provide security features to the present ACM. Furthermore, the present invention uses a flash memory that includes codes to provide password protection or other electronic security methods.

[0189] The second portion of the attached computer module has the hard drive module 2220. Among other elements, the hard drive module includes north bridge 2221, graphics accelerator 2223, graphics memory 2225, a power controller 2227, an IDE controller 2229, and other components. Adjacent to and in parallel alignment with the hard drive module is a personal computer interface (“PCI”) bus 2231, 2232. A power regulator 435 is disposed near the PCI bus.

[0190] In a specific embodiment, north bridge unit 2221 often couples to a computer memory, to the graphics accelerator 2223, to the IDE controller, and to the host interface controller via the PCI bus. Graphics accelerator 2223 typically couples to a graphics memory 2223, and other elements. IDE controller 2229 generally supports and provides timing signals necessary for the IDE bus. In the present embodiment, the IDE controller is embodied as a 643U2 PCI-to IDE chip from CMD Technology, for example. Other types of buses than IDE are contemplated, for example EIDE, SCSI, 1394, and the like in alternative embodiments of the present invention.

[0191] The hard drive module or mass storage unit 2220 typically includes a computer operating system, application software program files, data files, and the like. In a specific embodiment, the computer operating system may be the Windows98 operating system from Microsoft Corporation of Redmond Wash. Other operating systems, such as WindowsNT, MacOS8, Unix, and the like are also contemplated in alternative embodiments of the present invention. Further, some typical application software programs can include Office98 by Microsoft Corporation, Corel Perfect Suite by Corel, and others. Hard disk module 2220 includes a hard disk drive. The hard disk drive, however, can also be replaced by removable hard disk drives, read/write CD ROMs, flash memory, floppy disk drives, and the like. A small form factor, for example 2.5”, is currently contemplated, however, other form factors, such as PC card, and the like are also contemplated. Mass storage unit 2240 may also support other interfaces than IDE.

Among other features, the computer system includes an ACM with security protection. The ACM connects to the console, which has at least the following elements, which should not be limiting.

- 1) Connection to input devices, e.g. keyboard or mouse;
- 2) Connection to display devices, e.g. Monitor;
- 3) Add-on means, e.g. PCI add-on slots;
- 4) Removable storage media subsystem, e.g. Floppy drive, CDROM drive;
- 5) Communication device, e.g. LAN or modem;
- 6) An interface device and connectors to ACM;
- 7) A computer module bay with a notch in the frame for ACM's lock; and
- 8) Power supply and other accessories.

[0192] As noted, the computer module bay is an opening in a peripheral console that receives the ACM. The computer module bay provides mechanical support and protection to ACM. The module bay also includes, among other elements, a variety of thermal components for heat dissipation, a frame that provides connector alignment, and a lock engagement, which secures the ACM to the console. The bay also has a printed circuit board to mount and mate the connector from the ACM to the console. The connector provides an interface between the ACM and other accessories.

[0193] FIG. 23 is a simplified block diagram 2300 of a security system for a computer module according to an embodiment of the present invention. This diagram is merely an illustration and should not limit the scope of the claims herein. One of ordinary skill in the art would recognize other variations, modifications, and alternatives. The block diagram 2300 has a variety of features such as those noted above, as well as others. In the present diagram, different reference numerals are used to show the operation of the present system.

[0194] The block diagram is an attached computer module 2300. The module 2300 has a central processing unit, which communicates to a north bridge 2341, by way of a CPU bus 2327. The north bridge couples to main memory 2323 via memory bus 2329. The main memory can be any suitable high speed memory device or devices such as dynamic random access memory ("DRAM") integrated circuits and others. The DRAM includes at least 32 Meg. or 64 Meg. and greater of memory, but can also be less depending upon the

application. Alternatively, the main memory can be coupled directly with the CPU in some embodiments. The north bridge also couples to a graphics subsystem 2315 via bus 2342. The graphics subsystem can include a graphics accelerator, graphics memory, and other devices. Graphics subsystem transmits a video signal to an interface connector, which couples to a display, for example.

[0195] The attached computer module also includes a primary hard disk drive that serves as a main memory unit for programs and the like. The hard disk can be any suitable drive that has at least 2 GB and greater. As merely an example, the hard disk is a Marathon 2250 (2.25 GB, 2 1/2 inch drive) product made by Seagate Corporation of Scotts Valley, but can be others. The hard disk communicates to the north bridge by way of a hard disk drive controller and bus lines 2302 and 2331. The hard disk drive controller couples to the north bridge by way of the host PCI bus, which connects bus 2337 to the north bridge. The hard disk includes computer codes that implement a security program according to the present invention. Details of the security program are provided below.

[0196] The attached computer module also has a flash memory device 2305 with a BIOS. The flash memory device 2305 also has codes for a user password that can be stored in the device. The flash memory device generally permits the storage of such password without a substantial use of power, even when disconnected. As merely an example, the flash memory device has at least 4 Meg. or greater of memory, or 16 Meg. or greater of memory. A host interface controller 2307 communicates to the north bridge via bus 2335 and host PCI bus. The host interface controller also has a Lock control 2309, which couples to a lock. The lock is attached to the module and has a manual override to the lock on the host interface controller in some embodiments. Host interface controller 2307 communicates to the console using bus 2311, which couples to connection 2313.

[0197] In a preferred embodiment, the present invention uses a password protection scheme to electronically prevent unauthorized access to the computer module. The present password protection scheme uses a combination of software, which is a portion of the security program, and a user password, which can be stored in the flash memory device 505. By way of the flash memory device, the password does not become erased by way of power failure or the lock. The password is substantially fixed in code, which

cannot be easily erased. Should the user desire to change the password, it can readily be changed by erasing the code, which is stored in flash memory and a new code (i.e., password) is written into the flash memory. An example of a flash memory device can include a Intel Flash 28F800F3 series flash, which is available in 8 Mbit and 16 Mbit designs. Other types of flash devices can also be used, however. Details of a password protection method are further explained below by way of the FIGS.

[0198] In a specific embodiment, the present invention also includes a real-time clock 510 in the ACM, but is not limited. The real-time clock can be implemented using a reference oscillator 14.31818 MHz 508 that couples to a real-time clock circuit. The real-time clock circuit can be in the host interface controller. An energy source 506 such as a battery can be used to keep the real-time clock circuit running even when the ACM has been removed from the console. The real-time clock can be used by a security program to perform a variety of functions. As merely an example, these functions include: (1) fixed time period in which the ACM can be used, e.g., ACM cannot be used at night; (2) programmed ACM to be used after certain date, e.g., high security procedure during owner's vacation or non use period; (3) other uses similar to a programmable time lock. Further details of the present real-time clock are described in the application listed under Ser. No. 09/183,816 noted above.

[0199] In still a further embodiment, the present invention also includes a permanent password or user identification code to identify the computer module. In one embodiment, the permanent password or user code is stored in a flash memory device. Alternatively, the permanent password or user code is stored in the central processing unit. The password or user code can be placed in the device upon manufacture of such device. Alternatively, the password or user code can be placed in the device by a one time programming techniques using, for example, fuses or the like. The present password or user code provides a permanent "finger print" on the device, which is generally hardware. The permanent finger print can be used for identification purposes for allowing the user of the hardware to access the hardware itself, as well as other systems. These other systems include local and wide area networks. Alternatively, the systems can also include one or more servers. The present password and user identification can be quite important for electronic commerce applications and the like. In one or more embodiments, the

permanent password or user code can be combined with the password on flash memory for the security program, which is described below in more detail.

[0200] In one aspect of the invention, the user password is programmable. The password can be programmable by way of the security program. The password can be stored in a flash memory device within the ACM. Accordingly, the user of the ACM and the console would need to have the user password in order to access the ACM. In the present aspect, the combination of a security program and user password can provide the user a wide variety of security functions as follows:

- 1) Auto-lock capability when ACM is inserted into CMB;
- 2) Access privilege of program and data;
- 3) Password matching for ACM removal; and
- 4) Automatic HDD lock out if tempering is detected.

[0201] In still a further embodiment, the present invention also includes a method for reading a permanent password or user identification code to identify the computer module. In one embodiment, the permanent password or user code is stored in a flash memory device. Alternatively, the permanent password or user code is stored in the central processing unit. The password or user code can be placed in the device upon manufacture of such device. Alternatively, the password or user code can be placed in the device by a one time programming techniques using, for example, fuses or the like. The present password or user code provides a permanent “finger print” on the device, which is generally hardware. The permanent finger print can be used for identification purposes for allowing the user of the hardware to access the hardware itself, as well as other systems. These other systems include local and wide area networks. Alternatively, the systems can also include one or more servers. The present method allows a third party confirm the user by way of the permanent password or user code. The present password and user identification can be quite important for electronic commerce applications and the like, which verify the user code or password. In one or more embodiments, the permanent password or user code can be combined with the password on flash memory for the security program.

[0202] The above embodiments are described generally in terms of hardware and software. It will be recognized, however, that the functionality of the hardware can be

further combined or even separated. The functionality of the software can also be further combined or even separated. Hardware can be replaced, at times, with software. Software can be replaced, at times, with hardware. Accordingly, the present embodiments should not be construed as limiting the scope of the claims here. One of ordinary skill in the art would recognize other variations, modifications, and alternatives.

[0203] While the above is a full description of the specific embodiments, various modifications, alternative constructions and equivalents may be used. Therefore, the above description and illustrations should not be taken as limiting the scope of the present invention which is defined by the appended claims.

**MULTIPLE MODULE COMPUTER SYSTEM AND METHOD INCLUDING
DIFFERENTIAL SIGNAL CHANNEL COMPRISING
UNIDIRECTIONAL SERIAL BIT CHANNELS**

CROSS REFERENCE TO RELATED APPLICATIONS

[0001] This application is a continuation of U.S. Application No. 12/504,534 filed July 16, 2009, which is a continuation of U.S. Application No. 12/077,503 filed March 18, 2008 (Now U.S. Patent No. 7,676,624), which is a continuation of U.S. nonprovisional Application No. 11/166,656, filed June 24, 2005 (Now U.S. Patent No. 7,376,779), which is a continuation of U.S. nonprovisional Application No. 11/097,694, filed March 31, 2005 (Now U.S. Patent No. 7,363,415), which is a continuation of U.S. nonprovisional Application No. 10/772,214, filed February 3, 2004 (Now U.S. Patent No. 7,099,981), which is a continuation of U.S. nonprovisional Application No. 09/569,758, filed May 12, 2000 (Now U.S. patent no. 6,718,415), and which claimed priority to U.S. Provisional Application No. 60/134,122 filed May 14, 1999. These applications are hereby incorporated by reference in their entirety.

BACKGROUND OF THE INVENTION

[0002] The present invention relates to computing devices. More particularly, the present invention provides a system including a plurality of computer modules that can independently operate to provide backup capability, dual processing, and the like. Merely by way of example, the present invention is applied to a modular computing environment for desk top computers, but it will be recognized that the invention has a much wider range of applicability. It can be applied to a server as well as other portable or modular computing applications.

[0003] Many desktop or personal computers, which are commonly termed PCs, have been around and used for over ten years. The PCs often come with state-of-art microprocessors such as the Intel Pentium™ microprocessor chips. They also include a hard or fixed disk drive such as memory in the giga-bit range. Additionally, the PCs often include a random access memory integrated circuit device such as a dynamic random

access memory device, which is commonly termed DRAM. The DRAM devices now provide up to millions of memory cells (i.e., mega-bit) on a single slice of silicon. PCs also include a high resolution display such as cathode ray tubes or CRTs. In most cases, the CRTs are at least 15 inches or 17 inches or 20 inches in diameter. High resolution flat panel displays are also used with PCs.

[0004] Many external or peripheral devices can be used with the PCs. Among others, these peripheral devices include mass storage devices such as a Zip™ Drive product sold by Iomega Corporation of Utah. Other storage devices include external hard drives, tape drives, and others. Additional devices include communication devices such as a modem, which can be used to link the PC to a wide area network of computers such as the Internet. Furthermore, the PC can include output devices such as a printer and other output means. Moreover, the PC can include special audio output devices such as speakers the like.

[0005] PCs also have easy to use keyboards, mouse input devices, and the like. The keyboard is generally configured similar to a typewriter format. The keyboard also has the length and width for easily inputting information by way of keys to the computer. The mouse also has a sufficient size and shape to easily move a cursor on the display from one location to another location.

[0006] Other types of computing devices include portable computing devices such as “laptop” computers and the like. Although somewhat successful, laptop computers have many limitations. These computing devices have poor display technology. In fact, these devices often have a smaller flat panel display that has poor viewing characteristics. Additionally, these devices also have poor input devices such as smaller keyboards and the like. Furthermore, these devices have limited common platforms to transfer information to and from these devices and other devices such as PCs.

[0007] Up to now, there has been little common ground between these platforms including the PCs and laptops in terms of upgrading, ease-of-use, cost, performance, and the like. Many differences between these platforms, probably somewhat intentional, has benefited computer manufacturers at the cost of consumers. A drawback to having two separate computers is that the user must often purchase both the desktop and laptop to have “total” computing power, where the desktop serves as a “regular” computer and the laptop serves as a “portable” computer. Purchasing both computers is often costly and

runs “thousands” of dollars. The user also wastes a significant amount of time transferring software and data between the two types of computers. For example, the user must often couple the portable computer to a local area network (i.e., LAN), to a serial port with a modem and then manually transfer over files and data between the desktop and the portable computer. Alternatively, the user often must use floppy disks to “zip” up files and programs that exceed the storage capacity of conventional floppy disks, and transfer the floppy disk data manually.

[0008] Another drawback with the current model of separate portable and desktop computer is that the user has to spend money to buy components and peripherals that are duplicated in at least one of these computers. For example, both the desktop and portable computers typically include hard disk drives, floppy drives, CD-ROMs, computer memory, host processors, graphics accelerators, and the like. Because program software and supporting programs generally must be installed upon both hard drives in order for the user to operate programs on the road and in the office, hard disk space is often wasted.

[0009] One approach to reduce some of these drawbacks has been the use of a docking station with a portable computer. Here, the user has the portable computer for “on the road” use and a docking station that houses the portable computer for office use.

[0010] Similar to separate desktop and portable computers, there is no commonality between two desktop computers. To date, most personal computers are constructed with a single motherboard that provides connection for CPU and other components in the computer. Dual CPU systems have been available through Intel’s slot 1 architecture. For example, two Pentium II cartridges can be plugged into two “slot 1” card slots on a motherboard to form a Dual-processor system. The two CPU’s share a common host bus that connects to the rest of the system, e.g. main memory, hard disk drive, graphics subsystem, and others. Dual CPU systems have the advantage of increased CPU performance for the whole system. Adding a CPU cartridge requires no change in operating systems and application software. However, dual CPU systems may suffer limited performance improvement if memory or disk drive bandwidth becomes the limiting factor. Also, dual CPU systems have to time-share the processing unit in running multiple applications. CPU performance improvement efficiency also depends on software coding structure. Dual CPU systems provide no hardware redundancy to help

fault tolerance. In running multiple applications, memory and disk drive data throughput will become the limiting factor in improving performance with multi-processor systems.

[0011] The present invention generally relates to computer interfaces. More specifically, the present invention relates to an interface channel that interfaces two computer interface buses that operate under protocols that are different from that used by the interface channel.

[0012] Interfaces coupling two independent computer buses are well known in the art. A block diagram of a computer system utilizing such a prior art interface is shown in Fig. 5. In Fig. 5, a primary peripheral component interconnect (PCI) bus 505 of a notebook PC 500 is coupled to a secondary PCI bus 555 in a docking system 550 (also referred to as docking station 550) through high pin count connectors 501 and 502, which are normally mating connectors. The high pin count connectors 501 and 502 contain a sufficiently large number of pins so as to carry PCI bus signals between the two PCI buses without any translation. The main purpose for interfacing the two independent PCI buses is to allow transactions to occur between a master on one PCI bus and a target on the other PCI bus. The interface between these two independent PCI buses additionally includes an optional PCI to PCI bridge 560, located in the docking station 550, to expand the add on capability in docking station 550. The bridge 560 creates a new bus number for devices behind the bridge 560 so that they are not on the same bus number as other devices in the system thus increasing the add on capability in the docking station 550.

[0013] An interface such as that shown in Fig. 5 provides an adequate interface between the primary and secondary PCI buses. However, the interface is limited in a number of ways. The interface transfers signals between the primary and secondary PCI buses using the protocols of a PCI bus. Consequently, the interface is subject to the limitations under which PCI buses operate. One such limitation is the fact that PCI buses are not cable friendly. The cable friendliness of the interface was not a major concern in the prior art. However, in the context of the computer system of the present invention, which is described in the present inventor's (William W.Y. Chu's) application for "Personal Computer Peripheral Console With Attached Computer Module" filed concurrently with the present application on Sep. 8, 1998 and incorporated herein by reference, a cable friendly interface is desired for interfacing an attached computer module (ACM) and a peripheral console of the present invention. Furthermore, as a result of operating by PCI

protocols, the prior art interface includes a very large number of signal channels with a corresponding large number of conductive lines (and a similarly large number of pins in the connectors of the interface) that are commensurate in number with the number of signal lines in the PCI buses which it interfaces. One disadvantage of an interface having a relatively large number of conductive lines and pins is that it costs more than one that uses a fewer number of conductive lines and pins. Additionally, an interface having a large number of conductive lines is bulkier and more cumbersome to handle. Finally, a relatively large number of signal channels in the interface renders the option of using differential voltage signals less viable because a differential voltage signal method would require duplicating a large number of signal lines. It is desirable to use a low voltage differential signal (LVDS) channel in the computer system of the present invention because an LVDS channel is more cable friendly, faster, consumes less power, and generates less noise, including electromagnetic interferences (EMI), than a PCI channel. The term LVDS is herein used to generically refer to low voltage differential signals and is not intended to be limited to any particular type of LVDS technology.

[0014] Thus, what is needed are computer systems that can have multiple computer modules. Each computer module has dedicated memory and disk drive, and can operate independently.

BRIEF SUMMARY OF THE INVENTION

[0015] According to the present invention, a technique including a method and device for multi-module computing is provided. In an exemplary embodiment, the present invention provides a system including a plurality of computer modules that can independently operate to provide backup capability, dual processing, and the like.

[0016] In a specific embodiment, the present invention provides a computer system for multi-processing purposes. The computer system has a console comprising a first coupling site and a second coupling site, e.g., computer module bay. Each coupling site comprises a connector. The console is an enclosure that is capable of housing each coupling site. The system also has a plurality of computer modules, where each of the computer modules is coupled to one of the connectors. Each of the computer modules has a processing unit, a main memory coupled to the processing unit, a graphics controller coupled to the processing unit, and a mass storage device coupled to the processing unit.

Each of the computer modules is substantially similar in design to each other to provide independent processing of each of the computer modules in the computer system.

[0017] In an alternative specific embodiment, the present invention provides a multi-processing computer system. The system has a console comprising a first coupling site and a second coupling site. Each coupling site comprises a connector. The console is an enclosure that is capable of housing each coupling site. The system also has a plurality of computer modules, where each of the computer modules is coupled to one of the connectors. Each of the computer modules has a processing unit, a main memory coupled to the processing unit, a graphics controller coupled to the processing unit, a mass storage device coupled to the processing unit, and a video output coupled to the processing unit. Each of the computer modules is substantially similar in design to each other to provide independent processing of each of the computer modules in the computer system. A video switch circuit is coupled to each of the computer modules through the video output. The video switch is configured to switch a video signal from any one of the computer modules to a display.

[0018] Numerous benefits are achieved using the present invention over previously existing techniques. In one embodiment, the invention provides improved processing and maintenance features. The invention can also provide increased CPU performance for the whole system. The invention also can be implemented without changes in operating system and application software. The present invention is also implemented using conventional technologies that can be provided in the present computer system in an easy and efficient manner.

[0019] In another embodiment, the invention provides at least two users to share the same modular desktop system. Each user operates on a different computer module. The other peripheral devices, i.e. CDROM, printer, DSL connection, etc. can be shared. This provides lower system cost, less desktop space and more efficiency. Depending upon the embodiment, one or more of these benefits can be available. These and other advantages or benefits are described throughout the present specification and are described more particularly below.

[0020] In still further embodiments, the present invention provides methods of using multiple computer modules.

[0021] The present invention encompasses an apparatus for bridging a first computer interface bus and a second computer interface bus, where each of the first and second computer interface buses have a number of parallel multiplexed address/data bus lines and operate at a clock speed in a predetermined clock speed range having a minimum clock speed and a maximum clock speed. The apparatus comprises an interface channel having a clock line and a plurality of bit lines for transmitting bits; a first interface controller coupled to the first computer interface bus and to the interface channel to encode first control signals from the first computer interface bus into first control bits to be transmitted on the interface channel and to decode second control bits received from the interface channel into second control signals to be transmitted to the first computer interface bus; and a second interface controller coupled to the interface channel and the second computer interface bus to decode the first control bits from the interface channel into third control signals to be transmitted on the second computer interface bus and to encode fourth control signals from the second computer interface bus into the second control bits to be transmitted on the interface channel.

[0022] In one embodiment, the first and second interface controllers comprise a host interface controller (HIC) and a peripheral interface controller (PIC), respectively, the first and second computer interface buses comprise a primary PCI and a secondary PCI bus, respectively, and the interface channel comprises an LVDS channel.

[0023] The present invention overcomes the aforementioned disadvantages of the prior art by interfacing two PCI or PCI-like buses using a non-PCI or non-PCI-like channel. In the present invention, PCI control signals are encoded into control bits and the control bits, rather than the control signals that they represent, are transmitted on the interface channel. At the receiving end, the control bits representing control signals are decoded back into PCI control signals prior to being transmitted to the intended PCI bus.

[0024] The fact that control bits rather than control signals are transmitted on the interface channel allows using a smaller number of signal channels and a correspondingly small number of conductive lines in the interface channel than would otherwise be possible. This is because the control bits can be more easily multiplexed at one end of the interface channel and recovered at the other end than control signals. This relatively small number of signal channels used in the interface channel allows using LVDS channels for the interface. As mentioned above, an LVDS channel is more cable friendly, faster,

consumes less power, and generates less noise than a PCI bus channel, which is used in the prior art to interface two PCI buses. Therefore, the present invention advantageously uses an LVDS channel for the hereto unused purpose of interfacing PCI or PCI-like buses. The relatively smaller number of signal channels in the interface also allows using connectors having smaller pins counts. As mentioned above an interface having a smaller number of signal channels and, therefore, a smaller number of conductive lines is less bulky and less expensive than one having a larger number of signal channels. Similarly, connectors having a smaller number of pins are also less expensive and less bulky than connectors having a larger number of pins.

[0025] In one embodiment, the present invention encompasses an apparatus for bridging a first computer interface bus and a second computer interface bus, in a microprocessor based computer system where each of the first and second computer interface buses have a number of parallel multiplexed address/data bus lines and operate at a clock speed in a predetermined clock speed range having a minimum clock speed and a maximum clock speed. The apparatus comprises an interface channel having a clock channel and a plurality of bit channels for transmitting bits; a first interface controller coupled to the first computer interface bus and to the interface channel to encode first control signals from the first computer interface bus into first control bits to be transmitted on the interface channel and to decode second control bits received from the interface channel into second control signals to be transmitted to the first computer interface bus; and a second interface controller coupled to the interface channel and the second computer interface bus to decode the first control bits from the interface channel into third control signals to be transmitted on the second computer interface bus and to encode fourth control signals from the second computer interface bus into the second control bits to be transmitted on the interface channel.

[0026] In one embodiment, the first and second interface controllers comprise a host interface controller (HIC) and a peripheral interface controller (PIC), respectively, the first and second computer interface buses comprise a primary PCI and a secondary PCI bus, respectively, and the interface channel comprises an LVDS channel.

[0027] In a preferred embodiment, the interface channel has a plurality of serial bit channels numbering fewer than the number of parallel bus lines in each of the PCI buses and operates at a clock speed higher than the clock speed at which any of the bus lines

operates. More specifically, the interface channel includes two sets of unidirectional serial bit channels which transmit data in opposite directions such that one set of bit channels transmits serial bits from the HIC to the PIC while the other set transmits serial bits from the PIC to the HIC. For each cycle of the PCI clock, each bit channel of the interface channel transmits a packet of serial bits.

[0028] The HIC and PIC each include a bus controller to interface with the first and second computer interface buses, respectively, and to manage transactions that occur therewith. The HIC and PIC also include a translator coupled to the bus controller to encode control signals from the first and second computer interface buses, respectively, into control bits and to decode control bits from the interface channel into control signals. Additionally, the HIC and PIC each include a transmitter and a receiver coupled to the translator. The transmitter converts parallel bits into serial bits and transmits the serial bits to the interface channel. The receiver receives serial bits from the interface channel and converts them into parallel bits.

[0029] According to the present invention, a technique including a method and device for securing a computer module using a password in a computer system is provided. In an exemplary embodiment, the present invention provides a security system for an attached computer module (“ACM”). In an embodiment, the ACM inserts into a Computer Module Bay (CMB) within a peripheral console to form a functional computer.

[0030] In a specific embodiment, the present invention provides a computer module. The computer module has an enclosure that is insertable into a console. The module also has a central processing unit (i.e., integrated circuit chip) in the enclosure. The module has a hard disk drive in the enclosure, where the hard disk drive is coupled to the central processing unit. The module further has a programmable memory device in the enclosure, where the programmable memory device can be configurable to store a password for preventing a possibility of unauthorized use of the hard disk drive and/or other module elements. The stored password can be any suitable key strokes that a user can change from time to time. In a further embodiment, the present invention provides a permanent password or user identification code stored in flash memory, which also can be in the processing unit, or other integrated circuit element. The permanent password or user identification code is designed to provide a permanent “finger print” on the attached computer module.

[0031] In a specific embodiment, the present invention provides a variety of methods. In one embodiment, the present invention provides a method for operating a computer system such as a modular computer system and others. The method includes inserting an attached computer module (“ACM”) into a bay of a modular computer system. The ACM has a microprocessor unit (e.g., microcontroller, microprocessor) coupled to a mass memory storage device (e.g., hard disk). The method also includes applying power to the computer system and the ACM to execute a security program, which is stored in the mass memory storage device. The method also includes prompting for a user password from a user on a display (e.g., fiat panel, CRT). In a further embodiment, the present method includes a step of reading a permanent password or user identification code stored in flash memory, or other integrated circuit element. The permanent password or user identification code provides a permanent finger print on the attached computer module. The present invention includes a variety of these methods that can be implemented in computer codes, for example, as well as hardware.

[0032] Numerous benefits are achieved using the present invention over previously existing techniques. The present invention provides mechanical and electrical security systems to prevent theft or unauthorized use of the computer system in a specific embodiment. Additionally, the present invention substantially prevents accidental removal of the ACM from the console. In some embodiments, the present invention prevents illegal or unauthorized use during transit. The present invention is also implemented using conventional technologies that can be provided in the present computer system in an easy and efficient manner. Depending upon the embodiment, one or more of these benefits can be available. These and other advantages or benefits are described throughout the present specification and are described more particularly below.

[0033] These and other embodiments of the present invention, as well as its advantages and features, are described in more detail in conjunction with the text below and attached Figs.

BRIEF DESCRIPTION OF THE DRAWINGS

[0034] Fig. 1 is a simplified diagram of a computer system according to an embodiment of the present invention;

[0035] Fig. 2 is a simplified block diagram of a computer system according to an alternative embodiment of the present invention;

[0036] Fig. 3 is a simplified block diagram of a computer system according to a further alternative embodiment of the present invention, and

[0037] Fig. 4 is a simplified flow diagram of a method according to an embodiment of the present invention.

[0038] Fig. 5 is a block diagram of a computer system using a prior art interface between a primary and a secondary PCI bus.

[0039] Fig. 6 is a block diagram of one embodiment of a computer system using the interface of the present invention.

[0040] Fig. 7 is a partial block diagram of a computer system using the interface of the present invention as a bridge between the north and south bridges of the computer system.

[0041] Fig. 8 is a partial block diagram of a computer system in which the north and south bridges are integrated with the host and peripheral interface controllers, respectively.

[0042] Fig. 8A shows an attached computer module with Integrated CPU/NB Graphics and Integrated HIC/SB.

[0043] Fig. 8B shows an attached computer module with single chip fully integrated: CPU, Cache, Core Logic, Graphics controller and Interface controller.

[0044] Fig. 9 is a block diagram of one embodiment of the host interface controller and the peripheral interface controller of the present invention.

[0045] Fig. 10 is a detailed block diagram of one embodiment of the host interface controller of the present invention.

[0046] Fig. 11 is a detailed block diagram of one embodiment of the PIC of the present invention.

[0047] Fig. 12 is a table showing the symbols, signals, data rate and description of signals in a first embodiment of the XPBus.

[0048] Fig. 13 is a table showing the information transmitted on the XPBus during two clock cycles of the XPBus in one embodiment of the present invention where 10 data bits transmitted in each clock cycle of the XPBus.

[0049] Fig. 14 is a table showing information transmitted on the XPBus during four clock cycles of the XPBus in another embodiment of the present invention where 10 data bits are transmitted in each clock cycle of the XPBus.

[0050] Fig. 15 is a schematic diagram of the signal lines PCK, PD0 to PD3, and PCN.

[0051] Fig. 16 is a table showing the names, types, number of pins dedicated to, and the description of the primary bus PCI signals.

[0052] FIG. 17 is a block diagram of one embodiment of a computer system employing the present invention.

[0053] FIG. 18 is a block diagram of an attached computing module (ACM).

[0054] FIG. 19 illustrates an external view of one embodiment of an ACM.

[0055] FIG. 19b illustrates one possible embodiment of a computer bay.

[0056] FIG. 20 illustrates the internal component layout for one embodiment of an ACM.

[0057] FIG. 21 is a block diagram of a peripheral console (PCON).

[0058] FIG. 22 is a simplified layout diagram of a security system for a computer system according to an embodiment of the present invention; and

[0059] FIG. 23 is a simplified block diagram of a security system for a computer module according to an embodiment of the present invention.

DETAILED DESCRIPTION OF THE INVENTION

[0060] According to the present invention, a technique including a method and device for multi-module computing is provided. In an exemplary embodiment, the present invention provides a system including a plurality of computer modules that can independently operate to provide backup capability, dual processing, and the like.

[0061] Fig. 1 is a simplified diagram of a computer system 100 according to an embodiment of the present invention. This diagram is merely an illustration and should not limit the scope of the claims herein. One of ordinary skill in the art would recognize other variations, modifications, and alternatives. The computer system 100 includes an attached computer module (i.e., ACM) 113, a desktop console 101, among other elements. The computer system also has another ACM module 117. Each ACM module has a respective slot 121, 119, which mechanically houses and electrically couples each ACM to the computer console. Also shown is a display 111, which connects to the console. Additionally, keyboard 109 and mouse 115 are also shown. A second display 102, keyboard 105, and mouse 107 can be coupled to the console in some optional embodiments to allow more than one user to operate the computer system. The computer system is modular and has a variety of components that are removable. Some of these components (or modules) can be used in different computers, workstations, computerized television sets, and portable or laptop units.

[0062] In the present embodiment, each ACM 113 includes computer components. as will be described below, including a central processing unit (“CPU”). IDE controller, hard disk drive, computer memory, and the like. The computer module bay (i.e., CMB) 121 is an opening or slot in the desktop console. The CMB houses the ACM and provides communication to and from the ACM. The CMB also provides mechanical protection and support to the ACM. The CMB has a mechanical alignment mechanism for mating a portion of the ACM to the console. The CMB further has thermal heat dissipation sinks, electrical connection mechanisms, and the like. Some details of the ACM can be found in co-pending Patent Application Nos. 09/149,882 and 09/149,548 filed 9/8/98, commonly assigned, and hereby incorporated by reference for all purposes.

[0063] In a specific embodiment, the present multiple computer module system has a peripheral console that has two or more computer bays that can receive a removable computer module or ACM. Multiple computer module system can function as a personal

computer with only one ACM and the peripheral console. The second and additional ACM can be added later to increase overall system performance and reliability. The ACM operates independently as self-contained computer, communicates with each other through a high-speed serial communication and share most peripheral devices within the peripheral console. Each ACM controls its independent graphics subsystem and drives separate video output signals. A practical implementation is a dual ACM system. In a dual ACM system, two monitors can be used to display the two ACMs' graphics outputs at the same time. For a single monitor, a RGB switch is used to switch between the video outputs of the two ACMs and can be controlled by a command from the user. Similarly, input devices (i.e. keyboard and mouse) are switched between the two computer systems with a command from the user. Command from the user can be in the form of either a dedicated key on the keyboard or a special icon on the screen that the mouse can click on.

[0064] In most embodiments, the ACM includes an enclosure such as the one described with the following components, which should not be limiting:

- 1) A CPU with cache memory;
- 2) Core logic device or means;
- 3) Main memory;
- 4) A single primary Hard Disk Drive ("HDD") that has a security program;
- 5) Flash memory with system BIOS and programmable user password;
- 6) Operating System, application software, data files on primary HDD;
- 7) An interface device and connectors to peripheral console;
- 8) A software controllable mechanical lock, lock control means, and other accessories.

[0065] The ACM connects to a peripheral console with power supply, a display device, an input device, and other elements. Some details of these elements with the present system are described in more detail below. In a dual ACM system, the primary ACM can connect directly to the peripheral board in the peripheral console. The second ACM can connect either directly or indirectly to the peripheral board. For indirect connection, a receptacle board is added to allow a cable connection to the peripheral board. This is to facilitate the mechanical positioning of the second ACM inside the computer chassis. The receptacle board approach can even be used for the primary ACM if a high bandwidth

peripheral bus, e.g. PCI Bus, is not connected from the primary ACM to the peripheral board.

[0066] The shared peripheral console has a chassis and a motherboard that connects the following devices:

- 1) Input means, e.g. keyboard and mouse,
- 2) Display means, e.g. RGB monitor,
- 3) Add-on means, e.g. PCI add-on slots,
- 4) Two Computer Module Bays (CMB) with connectors to two ACMs,
- 5) A serial communication Hub controller that interfaces to serial communication controller of both ACMs,
- 6) Shared storage subsystem, e.g. Floppy drive, CDROM drive, DVD drive, or 2nd Hard Drive,
- 7) Communication device, e.g. modem,
- 8) Power supply, and others.

[0067] The computer bay is an opening in the peripheral console that receives an ACM. CMB provides mechanical protection to ACM, mechanical alignment for connector mating, mechanical locking system to prevent theft and accidental removal, and connectors at the end of the opening for connecting to ACM. The interface bus between ACM and the peripheral console has a video bus, peripheral connections, serial communication connection, control signals and power connection. Video bus includes video output of graphics devices, i.e. analog RGB and control signals for monitor. Power connection supplies the power for ACM.

[0068] An implementation of peripheral sharing is the use of Ethernet controllers to bridge the communication between the two ACMs. Some of the peripheral devices residing in the peripheral console are shown in the simplified diagram of Fig. 2. As shown, the diagram is merely an illustration which should not limit the scope of the claims herein. One of ordinary skill in the art would recognize many other variations, alternatives, and modifications. As shown, a primary ACM 203 is connected to PCI peripheral devices in the peripheral console through the PCI bus 225 that passes through the connection between primary ACM 203 and peripheral console 201. As shown, ACM has a CPU module 207 coupled to the PCI bus through a North Bridge 211.

[0069] The CPU module can use a suitable microprocessing unit, microcontroller, digital signal processor, and the like. In a specific embodiment, the CPU module uses, for example, a 400 MHz Pentium II microprocessor module from Intel Corporation and like microprocessors from AMD Corporation, Cyrix Corporation (now National Semiconductor Corporation), and others. In other aspects, the microprocessor can be one such as the Compaq Computer Corporation Alpha Chip, Apple Computer Corporation PowerPC G3 processor, and the like. Further, higher speed processors are contemplated in other embodiments as technology increases in the future.

[0070] In the CPU module, peripheral controller 213 is coupled to BIOS/flash memory 217. Additionally, the peripheral controller is coupled to a clock control logic, a configuration signal, and a peripheral bus. The ACM has the hard drive module 215. Among other elements, the ACM includes north bridge 215, graphics subsystem 223 (e.g., graphics accelerator, graphics memory), an IDE controller, and other components. Adjacent to and in parallel alignment with the hard drive module 215 is the PCI bus. In a specific embodiment, North Bridge unit 211 often couples to a computer memory 209, to the graphics subsystem, and to the peripheral controller via the PCI bus. Graphics subsystem typically couples to a graphics memory, and other elements. IDE controller generally supports and provides timing signals necessary for the IDE bus. In the present embodiment, the IDE controller is embodied as part of a P114XE controller from Intel, for example. Other types of buses than IDE are contemplated, for example EIDE, SCSI, 1394, and the like in alternative embodiments of the present invention.

[0071] The hard drive module or mass storage unit 215 typically includes a computer operating system, application software program files, data files, and the like. In a specific embodiment, the computer operating system may be the Windows98 operating system from Microsoft Corporation of Redmond Washington. Other operating systems, such as WindowsNT, MacOS8, Unix, and the like are also contemplated in alternative embodiments of the present invention. Further, some typical application software programs can include Office98 by Microsoft Corporation, Corel Perfect Suite by Corel, and others. Hard disk module 215 includes a hard disk drive. The hard disk drive, however, can also be replaced by removable hard disk drives, read/write CD ROMs, flash memory, floppy disk drives, and the like. A small form factor, for example 2.5", is

currently contemplated, however, other form factors, such as PC card, and the like are also contemplated. Mass storage unit 240 may also support other interfaces than IDE.

[0072] Among other features, the computer system includes an ACM with security protection.

[0073] The ACM also has a network controller, which can be an Ethernet controller 219, which is coupled to the North Bridge through the PCI bus. The North Bridge is coupled to the CPU. The Ethernet controller can be a 10/100 Base, such as Intel's 82559 or the like. Other types of network connection devices can also be used. For example, the invention can use Gbit Ethernet 1394, and USB 2.0. The network controller couples to a hub 233 in the console, which includes shared peripheral system 201.

[0074] Also shown is the second ACM 205. The second ACM has the same or similar components as the first ACM. Here, like reference numerals have been used for easy cross-referencing, but is not intended to be limiting. In some embodiments, the secondary ACM is not connected to the PCI bus in the peripheral console directly. The secondary ACM 219 accesses peripheral devices controlled by the primary ACM through the Ethernet connection to the primary ACM, e.g. CD-ROM, or PCI modem. The implementation is not restricted to Ethernet serial communication and can use other high-speed serial communication such as USB 2.0, and 1394. The Ethernet hub is coupled to an external output port 235, which connects to an external network.

[0075] The primary hard disk drive in each ACM can be accessed by the other ACM as sharable hard drive through the Ethernet connection. This allows the easy sharing of files between the two independent computer modules. The Ethernet Hub Controller provides the high-speed communication function between the two computer modules. Ethernet data bandwidth of 100 Mbit/sec allows fast data communication between the two computer modules. The secondary ACM access peripheral devices of the primary ACM through the network connection provided by Ethernet link. The operating system, e.g. Windows98, provides the sharing of resources between the two ACMs. In some embodiments, critical data in one ACM can be backup into the other ACM.

[0076] The Ethernet hub also couples to PCI bus 239, which connects to PCI devices 241, 243, e.g., modem, SCSI controller. A flash memory 242 can also be coupled to the PCI bus. The flash memory can store passwords and security information, such as those

implementations described in U.S. Serial No. 09/183,493, which is commonly owned, and hereby incorporated by reference. The hub 233 also couples to an I/O control 237, which connects to keyboard/mouse switch 245, which couples to keyboard/mouse 247. Optionally, the keyboard/mouse switch also couples to a second keyboard/house 259 via PS2 or USB signal line 251. The keyboard/mouse switch has at least a first state and a second state, which allow operation of respectively multiple keyboards or a single keyboard. The switch also couples to each I/O controller 221 in each ACM via lines 253, 255. The I/O control 237 also couples to an RGB switch 257, which allows video signals to pass to the first monitor 259. Alternatively, the RGB switch couples to a second monitor 261. The RGB switch includes analog video switches such as MAXIM's MAX4545.

[0077] The peripheral system 201 also has an independent power supply 231 for each ACM. Each power supply provides power to each ACM. As merely an example, the power supply is a MICRO ATX 150W made by ENLIGHT, but can be others. The power supply is connected or coupled to each ACM through a separate line, for example. The independent power supply allows for independent operation of each ACM in some embodiments.

[0078] The above embodiments are described generally in terms of hardware and software. It will be recognized, however, that the functionality of the hardware can be further combined or even separated. The functionality of the software can also be further combined or even separated. Hardware can be replaced, at times, with software. Software can be replaced, at times, with hardware. Accordingly, the present embodiments should not be construed as limiting the scope of the claims here. One of ordinary skill in the art would recognize other variations, modifications, and alternatives.

[0079] Fig. 3 is a simplified block diagram 300 of a computer system according to an alternative embodiment of the present invention. This diagram is merely an example which should not limit the scope of the claims herein. One of ordinary skill in the art would recognize many other variations, modifications, and alternatives. Like reference numerals are used in this Fig. as the previous Figs. for easy referencing, but are not intended to be limiting. As shown, each ACM includes common elements as the previous Fig. A primary ACM 203 is connected to PCI peripheral devices in the peripheral console through the PCI bus 225 that passes through the connection between primary ACM 203

and peripheral console 201. As shown, ACM has a CPU module 207 coupled to the PCI bus through a North Bridge 211.

[0080] The CPU module can use a suitable microprocessing unit, microcontroller, digital signal processor, and the like. In a specific embodiment, the CPU module uses, for example, a 400 MHz Pentium II microprocessor module from Intel Corporation and like microprocessors from AMD Corporation, Cyrix Corporation (now National Semiconductor Corporation), and others. In other aspects, the microprocessor can be one such as the Compaq Computer Corporation Alpha Chip, Apple Computer Corporation PowerPC G3 processor, and the like. Further, higher speed processors are contemplated in other embodiments as technology increases in the future.

[0081] In the CPU module, peripheral controller 213 is coupled to BIOS/flash memory 217. Additionally, the peripheral controller is coupled to a clock control logic, a configuration signal, and a peripheral bus. The ACM has the hard drive module 215. Among other elements, the ACM includes north bridge 215, graphics subsystem 223 (e.g., graphics accelerator, graphics memory), an IDE controller, and other components. Adjacent to and in parallel alignment with the hard drive module 215 is the PCI bus. In a specific embodiment, North Bridge unit 211 often couples to a computer memory 209, to the graphics subsystem, and to the peripheral controller via the PCI bus. Graphics subsystem typically couples to a graphics memory, and other elements. IDE controller generally supports and provides timing signals necessary for the IDE bus. In the present embodiment, the IDE controller is embodied as part of a P114XE controller from Intel, for example. Other types of buses than IDE are contemplated, for example EIDE, SCSI, 1394, and the like in alternative embodiments of the present invention.

[0082] The hard drive module or mass storage unit 215 typically includes a computer operating system, application software program files, data files, and the like. In a specific embodiment, the computer operating system may be the Windows98 operating system from Microsoft Corporation of Redmond Washington. Other operating systems, such as WindowsNT, MacOS8, Unix, and the like are also contemplated in alternative embodiments of the present invention. Further, some typical application software programs can include Office98 by Microsoft Corporation, Corel Perfect Suite by Corel, and others. Hard disk module 215 includes a hard disk drive. The hard disk drive, however, can also be replaced by removable hard disk drives, read/write CD ROMs, flash

memory, floppy disk drives, and the like. A small form factor, for example 2.5", is currently contemplated, however, other form factors, such as PC card, and the like are also contemplated. Mass storage unit 240 may also support other interfaces than IDE.

[0083] Among other features, the computer system includes an ACM with security protection.

[0084] The ACM also has a network controller, which can be coupled to a serial port 302, which is coupled to the PCI bus in the ACM. The serial port is coupled to the peripheral console through a serial controller 301 in the serial console. The serial controller is connected to PCI bus 239. The serial controller is also coupled to a serial hub controller 303, which is coupled to the PCI bus and a second ACM. In a specific embodiment, a receptacle board 310 is added to connect to the second ACM. The purpose of the receptacle board is to allow a cable connection 307 to the peripheral board 300. The cable connection is possible because the signals needed to connect to the peripheral board can be limited to video, I/O, serial communication, and power. The serial communication controller can be placed on the receptacle board and not in the ACM. As shown, the serial bus controller couples to the PCI bus. The receptacle board also couples to power, graphics subsystem, I/O controller, and other elements, which may be on a common bus. The overall operation of the present configuration is similar to the previous one except it operates in serial communication mode.

[0085] The Dual ACM system can support different usage models:

[0086] 1. One user using both ACMs concurrently with 1 or 2 monitors, and a common keyboard/mouse.

[0087] 2. Two users using the two separate ACMs at the same time with separate monitors and keyboard/mouse. The 2 users share peripherals, e.g., printer, CDROM, and others. The two users share external networking.

[0088] To support 1 monitor for both ACMs, a video switch in the peripheral console is used to switch between the video outputs of the two ACMs. The system can be set to support either 1 monitor or 2-monitor mode. The user presses a special key on the keyboard or a special icon on the screen to switch the screen display from one ACM to the

other. This same action causes the keyboard and mouse connections to switch from one ACM to the other ACM.

[0089] A dual ACM system can save space, wiring, and cost for a 2-person PC setup, with the added benefit that both PC systems can be accessed from one user site for increased system performance if the other user is not using the system. Files can be copied between the primary drive of both system and provides protection against a single ACM failure. Software needs to be developed to manage the concurrent use of two PC subsystems, the automatic sharing of selected files between the two systems, and fault tolerance.

[0090] The design with more than two computer modules can be implemented with the use of multi-port, serial communication hub controller and multi-port I/O switches. In one embodiment, a peripheral console has four computer bays for four separate computer modules. The computer modules communicate through a four port Ethernet hub. The video, keyboard, and mouse switch will cycle through the connection from each computer module to the external monitor, keyboard, and mouse with a push button sequentially. This embodiment is useful for a server that performs different functions concurrently, e.g. email, application hosting, web hosting , firewall, etc.

[0091] The above embodiments are described generally in terms of hardware and software. It will be recognized, however, that the functionality of the hardware can be further combined or even separated. The functionality of the software can also be further combined or even separated. Hardware can be replaced, at times, with software. Software can be replaced, at times, with hardware. Accordingly, the present embodiments should not be construed as limiting the scope of the claims here. One of ordinary skill in the art would recognize other variations, modifications, and alternatives.

[0092] Fig. 4 is a simplified diagram of a method according to an embodiment of the present invention. This diagram is merely an example which should not limit the scope of the claims herein. One of ordinary skill in the art would recognize many other variations, modifications, and alternatives. The present diagram illustrates an automatic file backup procedure from one computer module to the other. As shown, a user selects (step 401) a certain file in one of the computer module for automatic backup. Next, the method determines if another module is available, step 403. If so, the method in the originating

module requests the other computer module to create (step 405) backup file. Alternatively, the method alerts the user of the missing or malfunctioning module, step 429. The method then has the user try later 431, once the missing or malfunctioning module has been replaced or repaired. Next, the method determines if there is sufficient storage available in the other computer module for the backup files. If so, the method goes to the next step. (Alternatively, the method prompts (step 433) a message to the user indicating that the storage is full.) In the next step, the method stores the backup file in memory of the other module. After the backup file has been successfully created (step 409), the software in the originating ACM sets a timer to check (step 411) for file modification via branches 423, 427 through continue, step 425 process. If a file selected for backup has been modified (step 415), then the file is automatically back up to the other ACM again, step 417. Alternatively, the method returns to step 411 through branch 421.

[0093] The above embodiments are described generally in terms of hardware and software. It will be recognized, however, that the functionality of the hardware can be further combined or even separated. The functionality of the software can also be further combined or even separated. Hardware can be replaced, at times, with software. Software can be replaced, at times, with hardware. Accordingly, the present embodiments should not be construed as limiting the scope of the claims here. One of ordinary skill in the art would recognize other variations, modifications, and alternatives.

[0094] Fig. 6 is a block diagram of one embodiment of a computer system 600 using the interface of the present invention. Computer system 600 includes an attached computer module (ACM) 605 and a peripheral console 610, which are described in greater detail in the application of William W. Y. Chu for “Personal Computer Peripheral Console With Attached Computer Module” filed concurrently with the present application on Sep. 8, 1998 and incorporated herein by reference. The ACM 605 and the peripheral console 610 are interfaced through an exchange interface system (XIS) bus 615. The XIS bus 615 includes power bus 616, video bus 617 and peripheral bus (XPBus) 618, which is also herein referred to as an interface channel. The power bus 616 transmits power between ACM 605 and peripheral console 610. In a preferred embodiment power bus 616 transmits power at voltage levels of 3.3 volts, 5 volts and 12 volts. Video bus 617 transmits video signals between the ACM 605 and the peripheral console 610. In a preferred embodiment, the video bus 617 transmits analog Red Green Blue (RGB) video

signals for color monitors, digital video signals (such as Video Electronics Standards Association (VESA) Plug and Display's Transition Minimized Differential Signaling (TMDS) signals for flat panel displays), and television (TV) and/or super video (S-video) signals. The XPBus 618 is coupled to host interface controller (HIC) 619 and to peripheral interface controller (PIC) 620, which is also sometimes referred to as a bay interface controller.

[0095] In the embodiment shown in Fig. 6, HIC 619 is coupled to an integrated unit 621 that includes a CPU, a cache and a north bridge. In another embodiment, such as that shown in Fig. 7, the CPU 705 and north bridge 710 are separate rather than integrated units. In yet another embodiment, such as that shown in Fig. 8, the HIC and PIC are integrated with the north and south bridges, respectively, such that integrated HIC and north bridge unit 805 includes an HIC and a north bridge, while integrated PIC and south bridge unit 810 includes a PIC and a south bridge. Fig. 8A shows an attached computer module with integrated CPU/NB/Graphics 815 and Integrated HIC/SB 820. Fig. 8B shows an attached computer module with single chip 825 fully integrated: CPU, Cache, Core Logic, Graphics controller and Interface controller.

[0096] Fig. 9 is a more detailed block diagram of one embodiment of an HIC 905 and a PIC 955 of the present invention. HIC 905 includes a peripheral component interconnect (PCI) bus controller 910, an XPBus controller 915, a phase lock loop (PLL) clock 920 and an input/output (IO) control 925. Similarly, PIC 955 includes a PCI bus controller 960, an XPBus controller 965, a PLL clock 970 and an IO control 975. PCI bus controllers 910 and 960 are coupled to the primary and secondary PCI buses 930 and 980, respectively, and manage PCI transactions on the primary and secondary PCI buses 930 and 980, respectively. Similarly, XPBus Controllers 915 and 965 are coupled to XPBus 990. XPBus controller 915 drives the PCK line 991 and PD[0::3] and PCN lines 992 while XPBus controller 965 drives the PCKR lines 993, the PDR[0::3] and PCNR lines 994 and the RESET# line 995.

[0097] PCI bus controller 910 receives PCI clock signals from the primary PCI bus 930 and is synchronized to the PCI clock. However, as indicated in Fig. 9, the XPBus controller 915 is asynchronous with the PCI bus controller 910. Instead, the XPBus controller receives a clock signal from the PLL clock 920 and is synchronized therewith. PLL clock 920 generates a clock signal independent of the PCI clock. The asynchronous

operation of the PCI bus and the XPBus allows the PCI Bus to change in frequency. for example as in a power down situation, without directly affecting the XPBus clocking. In the embodiment shown in Fig. 9, the PLL clock 920 generates a clock signal having a frequency of 66 MHz, which is twice as large as the 33 MHz frequency of the PCI clock. (The clock signal generated by the PLL clock may have a clock speed different from, including lower than, 66 MHz. For example, in another embodiment, which is discussed in greater detail below, the PLL clock 920 generates a clock signal having a frequency of 132 MHz.)

[0098] The XPBus 990 operates at the clock speed generated by the PLL clock 920. Therefore, PCK, the clock signal from the XPBus controller 915 to XPBus controller 965 has the same frequency as the clock signal generated by PLL clock 920. XPBus controller 965 receives the PCK signal after it has been buffered and operates at the clock speed of PCK. The buffered version of the clock signal PCK is used to generate the clock signal PCKR, the clock signal from the XPBus controller 965 to XPBus controller 915. Accordingly, PCKR also has the same frequency as that generated by the PLL clock 920. The synchronous operation of PCK and PCKR provides for improved reliability in the system. In another embodiment, PCKR may be generated independently of PCK and may have a frequency different from that of PCK. It is to be noted that even when PCKR is generated from PCK, the slew between PCK and PCKR cannot be guaranteed because of the unknown cable length used for the XPBus. For a cable that is several feet long, the cable propagation delay alone can be several nano seconds.

[0099] As indicated in Fig. 9, PLL clock 970 is asynchronous with the XPBus controller 965. Instead, PLL clock 970 independently generates a clock signal that is used as a PCI clock signal on the secondary PCI bus 980. The secondary PCI bus 980 operates at the same clock speed as the primary PCI bus 930, namely at a frequency of 33 MHz.

[0100] Fig. 10 is a detailed block diagram of one embodiment of the HIC of the present invention. As shown in Fig. 10, HIC 1000 comprises bus controller 1010, translator 1020, transmitter 1030, receiver 1040, a PLL 1050, an address/data multiplexer (A/D MUX) 1060, a read/write controller (RD/WR Cntl) 1070, a video serial to parallel converter 1080 and a CPU control & general purpose input/output latch/driver (CPU CNTL & GPIO latch/driver) 1090.

[0101] HIC 1000 is coupled to an optional flash memory BIOS configuration unit 1001. Flash memory unit 1001 stores basic input output system (BIOS) and PCI configuration information and supplies the BIOS and PCI configuration information to A/D MUX 1060 and RD/WR Control 1070, which control the programming, read, and write of flash memory unit 1001.

[0102] Bus controller 1010 is coupled to the host PCI bus, which is also referred to herein as the primary PCI bus, and manages PCI bus transactions on the host PCI bus. Bus controller 1010 includes a slave (target) unit 1011 and a master unit 1016. Both slave unit 1011 and master unit 1016 each include two first in first out (FIFO) buffers, which are preferably asynchronous with respect to each other since the input and output of the two FIFOs in the master unit 1016 as well as the two FIFOs in the slave unit 1011 are clocked by different clocks, namely the PCI clock and the PCK. Additionally, slave unit 1011 includes encoder 1022 and decoder 1023, while master unit 1016 includes encoder 1027 and decoder 1028. The FIFOs 1012, 1013, 1017 and 1018 manage data transfers between the host PCI bus and the XPBus, which in the embodiment shown in Fig. 10 operate at 33 MHz and 106 MHz, respectively. PCI address/data (AD) from the host PCI bus is entered into FIFOs 1012 and 1017 before they are encoded by encoders 1022 and 1023. Encoders 1022 and 1023 format the PCI address/data bits to a form more suitable for parallel to serial conversion prior to transmittal on the XPBus. Similarly, address and data information from the receivers is decoded by decoders 1023 and 1028 to a form more suitable for transmission on the host PCI bus. Thereafter the decoded data and address information is passed through FIFOs 1013 and 1018 prior to being transferred to the host PCI bus. FIFOs 1012, 1013, 1017 and 1018, allow bus controller 1010 to handle posted and delayed PCI transactions and to provide deep buffering to store PCI transactions.

[0103] Bus controller 1010 also comprises slave read/write control (RD/WR Cntl) 1014 and master read/write control (RD/WR Cntl) 1015. RD/WR controls 1014 and 1015 are involved in the transfer of PCI control signals between bus controller 1010 and the host PCI bus.

[0104] Bus controller 1010 is coupled to translator 1020. Translator 1020 comprises encoders 1022 and 1027, decoders 1023 and 1028, control decoder & separate data path unit 1024 and control encoder & merge data path unit 1025. As discussed above encoders 1022 and 1027 are part of slave data unit 1011 and master data unit 1016, respectively,

receive PCI address and data information from FIFOs 1012 and 1017, respectively, and encode the PCI address and data information into a form more suitable for parallel to serial conversion prior to transmittal on the XPBus. Similarly, decoders 1023 and 1028 are part of slave data unit 1011 and master data unit 1016, respectively, and format address and data information from receiver 1040 into a form more suitable for transmission on the host PCI bus. Control encoder & merge data path unit 1025 receives PCI control signals from the slave RD/WR control 1014 and master RD/WR control 1015. Additionally, control encoder & merge data path unit 1025 receives control signals from CPU CNTL & GPIO latch/driver 1090, which is coupled to the CPU and north bridge (not shown in Fig. 10). Control encoder & merge data path unit 1025 encodes PCI control signals as well as CPU control signals and north bridge signals into control bits, merges these encoded control bits and transmits the merged control bits to transmitter 1030, which then transmits the control bits on the data lines PD0 to PD3 and control line PCN of the XPBus. Examples of control signals include PCI control signals and CPU control signals. A specific example of a control signal is FRAME# used in PCI buses. A control bit, on the other hand is a data bit that represents a control signal. Control decoder & separate data path unit 1024 receives control bits from receiver 1040 which receives control bits on data lines PDR0 to PDR3 and control line PCNR of the XPBus. Control decoder & separate data path unit 1024 separates the control bits it receives from receiver 1040 into PCI control signals, CPU control signals and north bridge signals, and decodes the control bits into PCI control signals, CPU control signals, and north bridge signals all of which meet the relevant timing constraints.

[0105] Transmitter 1030 receives multiplexed parallel address/data (AID) bits and control bits from translator 1020 on the AD[31::0] out and the CNTL out lines, respectively. Transmitter 1030 also receives a clock signal from PLL 1050. PLL 1050 takes a reference input clock and generates PCK that drives the XPBus. PCK is asynchronous with the PCI clock signal and operates at 106 MHz, twice the speed of the PCI clock of 33 MHz. The higher speed is intended to accommodate at least some possible increases in the operating speed of future PCI buses. As a result of the higher speed, the XPBus may be used to interface two PCI or PCI-like buses operating at 106 MHz rather than 33 MHz or having 104 rather than 32 multiplexed address/data lines.

[0106] The multiplexed parallel A/D bits and some control bits input to transmitter 1030 are serialized by parallel to serial converters 1032 of transmitter 1030 into 10 bit packets. These bit packets are then output on data lines PD0 to PD3 of the XPBus. Other control bits are serialized by parallel to serial converter 1033 into 10 bit packets and send out on control line PCN of the XPBus.

[0107] A 10x multiplier 1031 receives PCK, multiplies it by a factor of 10 and feeds a clock signal 10 times greater than PCK into the parallel to serial converters 1032 and 1033. The parallel to serial converters 1032 and 1033 perform bit shifting at 10 times the PCK rate to serialize the parallel bits into 10 bit packets. As the parallel to serial converters 1032 and 1033 shift bits at 10 times the PCK rate, the bit rate for the serial bits output by the parallel to serial converters is 10 times higher than PCK rate, i.e., 1060 MHz. However, the rate at which data packets are transmitted on the XPBus is the same as the PCK rate, i.e., 106 MHz. As the PCI buses operate at a clock and bit rate of 33 MHz, the XPBus has a clock rate that is twice as large and a bit rate per bit line (channel) that is 100 times as large as that of the PCI buses which it interfaces.

[0108] Receiver 1040 receives serial bit packets on data lines PDR0 to PDR3 and control line PCNR. Receiver 1040 also receives PCKR on the XPBus as well as the clock signal PCK from PLL 1050. The synchronizer (SYNC) 1044 of receiver 1040 synchronizes the clock signal PCKR to the locally generated clock signal, PCK, in order to capture the bits received from the XPBus into PCK clock timing.

[0109] Serial to parallel converters 1042 convert the serial bit packets received on lines PDR0 to PDR3 into parallel address/data and control bits that are sent to decoders 1023 and 1028 and control decoder and separate data path unit 1024, respectively. Serial to parallel converter 1043 receives control bit packets from control line PCNR, converts them to parallel control bits and sends the parallel control bits to control decoder & separate data path 1024.

[0110] A 10x multiplier 1041 receives PCKR, multiplies it by a factor of 10 and feeds a clock signal 10 times greater than PCKR into the serial to parallel converters 1042 and 1043. Because the bits on PDR0 to PDR3 and PCNR are transmitted at a bit rate of 10 times the PCKR rate, the serial to parallel converters 1042 and 1043 perform bit shifting at 10 times the PCKR rate to convert the 10 bit packets into parallel bits. It is to be noted

that the rate at which bit packets are transmitted on the XPBus is the same as the PCKR rate, i.e., 106 MHz. The parallel data and control bits are thereafter sent to decoders 1023 and 1028 by way of the AD[3::0] in line and to control decoder & separate data path unit 1024 by way of CNTL in lines, respectively.

[0111] Reset control unit 1045 of HIC 1000 receives the signal RESET#, which is an independent system reset signal, on the reset line RESET#. Reset control unit 1045 then transmits the reset signal to the CPU CNTL & GPIO latch/driver unit 1090.

[0112] As may be noted from the above, the 32 line host and secondary PCI buses are interfaced by 10 XPBus lines (PD0, PD1, PD2, PD3, PCN, PDR0, PDR1, PDR2, PDR3, PCNR). Therefore, the interface channel, XPBus, of the present invention uses fewer lines than are contained in either of the buses which it interfaces, namely the PCI buses. XPBus is able to interface such PCI buses without backup delays because the XPBus operates at a clock rate and a per line (channel) bit rate that are higher than those of the PCI buses.

[0113] In addition to receiving a reset signal, the CPU CNTL & GPIO latch/driver 1090 is responsible for latching input signals from the CPU and north bridge and sending the signals to the translator. It also takes decoded signals from the control decoder & separate data path unit 1024 and drives the appropriate signals for the CPU and north bridge.

[0114] In the embodiment shown in Fig. 10, video serial to parallel converter 1080 is included in HIC 1000. In another embodiment, video serial to parallel converter 1080 may be a separate unit from the HIC 1000. Video serial to parallel converter 1080 receives serial video data on line VPD and a video clock signal VPCK from line VPCK of video bus 1081. It then converts the serial video data into 16 bit parallel video port data and the appropriate video port control signals, which it transmits to the graphics controller (not shown in Fig. 10) on the video port data [0::15] and video port control lines, respectively.

[0115] HIC 1000 handles the PCI bus control signals and control bits from the XPBus representing PCI control signals in the following ways:

1. HIC 1000 buffers clocked control signals from the host PCI bus, encodes them into control bits and sends the encoded control bits to the XPBus;
2. HIC 1000 manages the signal locally; and

3. HIC 1000 receives control bits from XPBus, translates the control bits into PCI control signals and sends the PCI control signals to the host PCI bus.

[0116] Fig. 11 is a detailed block diagram of one embodiment of the PIC of the present invention. PIC 1100 is nearly identical to HIC 1000 in its function, except that HIC 1000 interfaces the host PCI bus to the XPBus while PIC 1100 interfaces the secondary PCI bus to the XPBus. Similarly, the components in PIC 1100 serve the same function as their corresponding components in HIC 1000. Reference numbers for components in PIC 1100 have been selected such that a component in PIC 1100 and its corresponding component in HIC 1000 have reference numbers that differ by 500 and have the same two least significant digits. Thus for example, the bus controller in PIC 1100 is referenced as bus controller 1110 while the bus controller in HIC 1000 is referenced as bus controller 1010. As many of the elements in PIC 1100 serve the same functions as those served by their corresponding elements in HIC 1000 and as the functions of the corresponding elements in HIC 1000 have been described in detail above, the function of elements of PIC 1100 having corresponding elements in HIC 1000 will not be further described herein. Reference may be made to the above description of Fig. 10 for an understanding of the functions of the elements of PIC 1100 having corresponding elements in HIC 1000.

[0117] As suggested above, there are also differences between HIC 1000 and PIC 1100. Some of the differences between HIC 1000 and PIC 1100 include the following. First, receiver 1140 in PIC 1100, unlike receiver 1040 in HIC 1000, does not contain a synchronization unit. As mentioned above, the synchronization unit in HIC 1000 synchronizes the PCKR clock to the PCK clock locally generated by PLL 1050. PIC 1100 does not locally generate a PCK clock and therefore, it does not have a locally generated PCK clock with which to synchronize the PCK clock signal that it receives from HIC 1000. Another difference between PIC 1100 and HIC 1000 is the fact that PIC 1100 contains a video parallel to serial converter 1189 whereas HIC 1000 contains a video serial to parallel converter 1080. Video parallel to serial converter 1189 receives 16 bit parallel video capture data and video control signals on the Video Port Data [0::15] and Video Port Control lines, respectively, from the video capture circuit (not shown in Fig. 11) and converts them to a serial video data stream that is transmitted on the VPD line to the HIC. The video capture circuit may be any type of video capture circuit that outputs a 16 bit parallel video capture data and video control signals. Another difference lies in the

fact that PIC 1100, unlike HIC 1000, contains a clock doubler 1182 to double the video clock rate of the video clock signal that it receives. The doubled video clock rate is fed into video parallel to serial converter 1182 through buffer 1183 and is sent to serial to parallel converter 1080 through buffer 1184. Additionally, reset control unit 1135 in PIC 1100 receives a reset signal from the CPU CNTL & GPIO latch/driver unit 1190 and transmits the reset signal on the RESET# line to the HIC 1000 whereas reset control unit 1045 of HIC 1000 receives the reset signal and forwards it to its CPU CNTL & GPIO latch/driver unit 1090 because, in the above embodiment, the reset signal RESET# is unidirectionally sent from the PIC 1100 to the HIC 1000.

[0118] Like HIC 1000, PIC 1100 handles the PCI bus control signals and control bits from the XPBus representing PCI control signals in the following ways:

1. PIC 1100 buffers clocked control signals from the secondary PCI bus. encodes them and sends the encoded control bits to the XPBus;
2. PIC 1100 manages the signal locally; and
3. PIC 1100 receives control bits from XPBus, translates them into PCI control signals and sends the PCI control signals to the secondary PCI bus.

[0119] PIC 1100 also supports a reference arbiter on the secondary PCI Bus to manage the PCI signals REQ# and GNT#.

[0120] Fig. 12 is a table showing the symbols, signals, data rate and description of signals on the XPBus, where RTN indicates a ground (GND) reference. In the above tables, P&D stands for plug and display and is a trademark of the Video Electronics Standards Association (VESA) for the Plug and Display standard, DDC2:SCL and DDC2:SDA stand for the VESA display data channel (DDC) standard 2 clock and data signals, respectively, SV stands for super video, V33 is 3.3 volts, and V5 is 5.0 volts. TMDS stands for Transition Minimized Differential Signaling and is a trademark of Silicon Images and refers to their Panel Link technology, which is in turn a trademark for their LVDS technology. TMDS is used herein to refer to the Panel Link technology or technologies compatible therewith.

[0121] Fig. 13 is a table showing the information transmitted on the XPBus during two clock cycles of the XPBus in one embodiment of the present invention where 10 data bits are transmitted in each clock cycle of the XPBus. In Fig. 13, A00 to A31 represent 32

bits of PCI address A[31::0], D00 to D31 represent 32 bits of PCI data D[31::0], BS0 to BS3 represent 4 bits of bus status data indicating the status of the XPBus, CM0# to CM3# represent 4 bits of PCI command information, BE0# to BE3# represent 4 bits of PCI byte enable information, and CN0 to CN9 represent 10 bits of control information sent in each clock cycle. As shown in Fig. 13, for each of lines PD0 to PD3, the 10 bit data packets contain one BS bit, one CM/BE bit, and eight AID bits. For the PCN line, the 10 bit data packet contains 10 CN bits. The first clock cycle shown in Fig. 13 comprises an address cycle in which 4 BS bits, 4 CM bits, 32 A bits and 10 CN bits are sent. The second clock cycle comprises a data cycle in which 4 BS bits, 4 BE bits, 32 D bits and 10 CN bits are sent. The bits transmitted on lines PD0 to PD3 represent 32 PCI AD[31::0] signals, 4 PCI C/BE# [3::0] signals, and part of the function of PCI control signals, such as FRAME#, IRDY#, and TRDY#.

[0122] In the embodiment shown in Fig. 13, BS0 to BS3 are sent at the beginning of each clock cycle. The bus status bits indicate the following bus cycle transactions: idle, address transfer, write data transfer, read data transfer, switch XPBus direction, last data transfer, wait, and other cycles.

[0123] Bits representing signals transmitted between the CPU and South Bridge may also be sent on the lines interconnecting the HIC and PIC, such as lines PCN and PCNR. For example, CPU interface signals such as CPU interrupt (INTR), Address 20 Mask (A20M#), Non-Maskable Interrupt (NMI), System Management Interrupt (SMI#), and Stop Clock (STPCLK#), may be translated into bit information and transmitted on the XPBus between the HIC and the PIC.

[0124] Fig. 14 is a table showing the information transmitted on the XPBus during four clock cycles of the XPBus in another embodiment of the present invention where 10 data bits are transmitted in each clock cycle of the XPBus. In this embodiment, the XPBus clock rate is twice as large as the PCI clock rate. This allows sending data and address bits every other XPBus cycle. As can be seen in Fig. 14, there are no address or data bits transmitted during the second or fourth XPBus clock cycle. The fact that the XPBus clock rate is higher than the PCI clock rate allows for compatibility of the XPBus with possible future expansions in the performance of PCI bus to higher data transfer and clock rates.

[0125] In the embodiment shown in Fig. 14, there are 18 control bits, CN0 to CN17, transmitted in every two XPBus clock cycles. The first bit transmitted on the control line in each XPBus clock cycle indicates whether control bits CN0 to CN8 or control bits CN9 to CN17 will be transmitted in that cycle. A zero sent at the beginning of a cycle on the control line indicates that CN0 to CN8 will be transmitted during that cycle, whereas a one sent at the beginning of a cycle on the control line indicates that CN9 to CN17 will be transmitted during that cycle. These bits also indicate the presence or absence of data and address bits during that cycle. A zero indicates that address or data bits will be transmitted during that cycle whereas a one indicates that no address or data bits will be transmitted during that cycle.

[0126] In one embodiment, BS0 and BS1 are used to encode the PCI signals FRAME# and IRDY#, respectively. Additionally, in one embodiment, BS2 and BS3 are used to indicate the clock speed of the computer bus interface and the type of computer bus interface, respectively. For example, BS2 value of zero may indicate that a 33 MHz PCI bus of 32 bits is used whereas a BS2 value of one may indicate that a 66 MHz PCI bus of 32 bits is used. Similarly, a BS3 value of zero may indicate that a PCI bus is used whereas a BS3 value of one may indicate that another computer interface bus, such as an Institute of Electronics & Electrical Engineers (IEEE) 1394 bus, is used.

[0127] Fig. 15 is a schematic diagram of lines PCK, PD0 to PD3, and PCN. These lines are unidirectional LVDS lines for transmitting clock signals and bits such as those shown in FIGS. 13 and 14 from the HIC to the PIC. The bits on the PD0 to PD3 and the PCN lines are sent synchronously within every clock cycle of the PCK. Another set of lines, namely PCKR, PDR0 to PDR3, and PCNR, are used to transmit clock signals and bits from the PIC to HIC. The lines used for transmitting information from the PIC to the HIC have the same structure as those shown in Fig. 15, except that they transmit data in a direction opposite to that in which the lines shown in Fig. 15 transmit data. In other words they transmit information from the PIC to the HIC. The bits on the PDR0 to PDR3 and the PCNR lines are sent synchronously within every clock cycle of the PCKR. Some of the examples of control information that may be sent in the reverse direction, i.e., on PCNR line, include a request to switch data bus direction because of a pending operation (such as read data available), a control signal change in the target requiring communication in the reverse direction, target busy, and transmission error detected.

[0128] The XDBus which includes lines PCK, PD0 to PD3, PCN, PCKR, PDR0 to PDR3, and PCNR, has two sets of unidirectional lines transmitting clock signals and bits in opposite directions. The first set of unidirectional lines includes PCK, PD0 to PD3, and PCN. The second set of unidirectional lines includes PCKR, PDR0 to PDR3, and PCNR. Each of these unidirectional set of lines is a point-to-point bus with a fixed transmitter and receiver, or in other words a fixed master and slave bus. For the first set of unidirectional lines, the HIC is a fixed transmitter/master whereas the PIC is a fixed receiver/slave. For the second set of unidirectional lines, the PIC is a fixed transmitter/master whereas the HIC is a fixed receiver/slave. The LVDS lines of XDBus, a cable friendly and remote system I/O bus, transmit fixed length data packets within a clock cycle.

[0129] The XDBus lines, PD0 to PD3, PCN, PDR0 to PDR3 and PCNR, and the video data and clock lines, VPD and VPCK, are not limited to being LVDS lines, as they may be other forms of bit based lines. For example, in another embodiment, the XDBus lines may be IEEE 1394 lines.

[0130] It is to be noted that although each of the lines PCK, PD0 to PD3, PCN, PCKR, PDR0 to PDR3, PCNR, VPCK, and VPD is referred to as a line, in the singular rather than plural. each such line may contain more than one physical line. For example, in the embodiment shown in Fig. 23, each of lines PCK, PD0 to PD3 and PCN includes two physical lines between each driver and its corresponding receiver. The term line, when not directly preceded by the terms physical or conductive, is herein used interchangeably with a signal or bit channel which may consist of one or more physical lines for transmitting a signal. In the case of non-differential signal lines, generally only one physical line is used to transmit one signal. However, in the case of differential signal lines, a pair of physical lines is used to transmit one signal. For example, a bit line or bit channel in an LVDS or IEEE 1394 interface consists of a pair of physical lines which together transmit a signal.

[0131] A bit based line (i.e., a bit line) is a line for transmitting serial bits. Bit based lines typically transmit bit packets and use a serial data packet protocol. Examples of bit lines include an LVDS line, an IEEE 1394 line, and a Universal Serial Bus (USB) line.

[0132] Fig. 16 is a table showing the names, types, number of pins dedicated to, and the description of the primary bus PCI signals. The pins represent those between the host PCI bus and the HIC.

[0133] FIG. 17 is a block diagram of the components in one computer system employing the present invention. The computer system comprises an attached computer module (ACM), a peripheral console (PCON), and the interconnection apparatus between them. The ACM includes the central processing unit (CPU) 1710, system memory 1720, high performance devices 1750, primary mass storage 1730, and related interface and support circuitry 1740. The PCON includes primary display 1810, primary input 1820, secondary mass storage 1750, other devices 1860, expansion slots 1870, the primary power supply 1830, and related interface and support circuitry 1840. The interconnection apparatus 1900 includes circuitry to convey power and operational signals between the ACM and PCON.

[0134] Within the ACM 1700, the CPU 1710 executes instructions and manipulates data stored in the system memory. The CPU 1710 and system memory 1720 represent the user's core computing power. The core computing power may also include high performance devices 1750 such as advanced graphics processor chips that greatly increase overall system performance and which, because of their speed, need to be located close to the CPU. The primary mass storage 1730 contains persistent copies of the operating system software, application software, configuration data, and user data. The software and data stored in the primary mass storage device represent the user's computing environment. Interface and support circuitry 1740 primarily includes interface chips and signal busses that interconnect the CPU, system memory, high performance devices, and primary mass storage. The interface and support circuitry also connects ACM-resident components with the ACM-to-PCON interconnection apparatus as needed.

[0135] Within the PCON 1800, the primary display component 1810 may include an integrated display device or connection circuitry for an external display device. This primary display device may be, for example, an LCD, plasma, or CRT display screen used to display text and graphics to the user for interaction with the operating system and application software. The primary display component is the primary output of the computer system, i.e., the paramount vehicle by which programs executing on the CPU can communicate toward the user.

[0136] The primary input component 1820 of the PCON may include an integrated input device or connection circuitry for attachment to an external input device. The primary input may be, for example, a keyboard, touch screen, keypad, mouse, trackball, digitizing pad, or some combination thereof to enable the user to interact with the operating system and application software. The primary input component is the paramount vehicle by which programs executing on the CPU receive signals from the user.

[0137] The PCON may contain secondary mass storage 1850 to provide additional high capacity storage for data and software. Secondary mass storage may have fixed or removable media and may include, for example, devices such as diskette drives, hard disks, CD-ROM drives, DVD drives, and tape drives.

[0138] The PCON may be enhanced with additional capability through the use of integrated “Other Devices” 1860 or add-on cards inserted into the PCON’s expansion slots 1870. Examples of additional capability include sound generators, LAN connections, and modems. Interface and support circuitry 1840 primarily includes interface chips, driver chips, and signal busses that interconnect the other components within the PCON. The interface and support circuitry also connects PCON-resident components with the ACM-to-PCON interconnection apparatus as needed.

[0139] Importantly, the PCON houses the primary power supply 1830. The primary power supply has sufficient capacity to power both the PCON and the ACM 1700 for normal operation. Note that the ACM may include a secondary “power supply” in the form, for example, of a small battery. Such a power supply would be included in the ACM to maintain, for example, a time-of-day clock, configuration settings when the ACM is not attached to a PCON, or machine state when moving an active ACM immediately from one PCON to another. The total energy stored in such a battery would, however, be insufficient to sustain operation of the CPU at its rated speed, along with the memory and primary mass storage, for more than a fraction of an hour, if the battery were able to deliver the required level of electrical current at all.

[0140] FIG. 18 is a block diagram of an attached computing module (ACM) 1700. The physical ACM package 1700 contains the ACM functional components 1701 and the ACM side of the ACM-to-PCON Interconnection 1900. The ACM 1701 comprises a

CPU component 1710, a system memory component 1720, a primary mass storage component 1730, a high performance devices components 1750, and an interface and support component 1740.

[0141] The ACM side of the ACM-to-PCON Interconnection 1900 comprises a Host Interface Controller (HIC) component 1920 and an ACM connector component 1930. The HIC 1920 and connector 1930 components couple the ACM functional components 1700 with the signals of an ACM-to-PCON interface bus 1910 used to operatively connect an ACM with a PCON. The ACM-to-PCON interface bus 1910 comprises conveyance for electrical power 1914 and signals for a peripheral bus 1912, video 1916, video port 1917, and console type 1918. The preferred ACM-to-PCON Interconnection 1900 is described in detail in a companion U.S. patent application, Ser. No. 09/149,882, entitled "A Communication Channel and Interface Devices for Bridging Computer Interface Buses," by the same inventor, filed on the same day herewith, and hereby incorporated by reference. The preferred ACM-to-PCON interconnection 1900 includes circuitry to transmit and receive parallel bus information from multiple signal paths as a serial bit stream on a single signal path. This reduces the number of physical signal paths required to traverse the interconnection 1900. Further, employing low-voltage differential signaling (LVDS) on the bit stream data paths provides very reliable, high-speed transmission across cables. This represents a further advantage of the present invention.

[0142] The CPU component 1710 of the ACM functional circuitry 1701 of the presently described embodiment comprises a microprocessor 1712, which is the chief component of the personal computer system, power supply connection point 1713, and cache memory 1714 tightly coupled to the microprocessor 1712 by the CPU-to-cache bus 1714 comprising signal paths for address, data, and control information. The microprocessor 1712 of this embodiment is one of the models from the Pentium II family of processors from Intel Corporation. Microprocessor 1712 receives electrical power from power bus 1768 via connection point 1713. Microprocessor 1712 couples to the Host Interface Controller (HIC) 1920 via CPU-to-HIC bus 1763 comprising signal paths to exchange control information such as an interrupt request. Microprocessor 1712 also couples to CPU Bridge 1746 via CPU main bus 1764 comprising signal paths for address, data, and control information.

[0143] The CPU Bridge component 1746 of the interface and support circuitry 1740 operates to couple the high speed CPU main bus 1764 to specialty buses of varying speeds and capability that connect other computer components. The CPU Bridge of the presently described embodiment incorporates memory controller circuitry, advanced graphics processor support circuitry, and a general, industry-standard PCI bus controller in a single package. A CPU Bridge 1746 such as the 82443LX PCI/AGP Controller from Intel Corporation may be used.

[0144] The system memory component 1720 of the ACM functional circuitry 1701 in the present embodiment comprises main system memory (RAM) 1722, BIOS memory 1724, and flash memory 1726. The system memory 1720 is used to contain data and instructions that are directly addressable by the CPU. The RAM 1722 comprises volatile memory devices such as DRAM or SDRAM memory chips that do not retain their stored contents when power is removed. This form of memory represents the largest proportion of total system memory 1720 capacity. The BIOS memory 1724 comprises non-volatile memory devices such as ROM or EPROM memory chips that retain their stored contents regardless of the application of power and are read-only memory under normal operating conditions. The BIOS memory 1724 stores, for example, start-up instructions for the microprocessor 1712 and sets of instructions for rudimentary input/output tasks. The flash memory 1726 comprises non-volatile memory devices that retain their stored contents regardless of the application of power. Unlike the BIOS non-volatile memory, however, the stored contents of the flash memory 1726 are easily changed under normal operating conditions. The flash memory 1726 may be used to store status and configuration data, such as security identifiers or ACM specifications like the speed of the microprocessor 1712. Some embodiments may combine the BIOS functions into the flash memory device, thus permitting BIOS contents to be rewritten, improving field upgradability.

[0145] The main system memory (RAM) 1722 is coupled to memory controller circuitry resident within the CPU Bridge 1746 via direct memory bus 1765. The BIOS 1724 and flash memory 1726 are coupled to HIC 1920 via switched memory bus 1766. This permits the BIOS 1724 and flash 1726 memories to be accessed by circuitry in the HIC 1920 or other circuitry connected thereto. The direct memory bus 1765 and the

switch memory bus 1766 each comprises conductors to convey signals for data, address, and control information.

[0146] The primary mass storage component 1730 of the ACM functional circuitry 1701 in the present embodiment comprises a compact hard disk drive with an industry-standard, IDE interface. The hard disk drive (HDD) 1732 has a formatted storage capacity sufficient to contain an operating system for the computer, application software desired by the user, and related user configuration and operating parameter data. The HDD 1732 in the present embodiment serves as the “boot” device for the personal computer from which the operating system is loaded into RAM 1722 by the start-up program stored in the BIOS 1724.

[0147] The present HDD 1732 has a capacity of approximately 2,000 megabytes to provide adequate storage for common software configurations and reasonable space for user data. One example of a common software configuration includes the Windows 95 operating system from Microsoft Corporation, a word processing program, a spreadsheet program, a presentation graphics program, a database program, an email program, and a web browser such as Navigator from Netscape Corporation. The hard disk 1732 stores program and data files for each software component, including files distributed by the vendor as well as files created or updated by operation of the software after it is installed. For example, a word processor program may maintain information about a user’s identity and latest preferences in an operating system registry file. Or, for example, the web browser may maintain a file of the user’s favorite web sites or most recently viewed web pages. An HDD with 2000 megabyte capacity is readily available in the small size of hard disk (e.g., 2.5-inch or 3.5-inch) to minimize the space required within the ACM for the primary mass storage device 1730.

[0148] The HDD 1732 is coupled to IDE controller circuitry 1748 via IDE bus 1772. The IDE controller circuitry 1748 is coupled to the CPU Bridge 1746 via the Host PCI bus 1767. IDE controllers and busses, and the PCI bus are well known and understood in the industry. The above components operate together to couple the hard disk drive 1732 to the microprocessor 1712.

[0149] The high performance devices component 1750 of the ACM functional circuitry 1701 in the present embodiment comprises an Advanced Graphics Processor (AGP) 1752.

The Model 740 Graphics Device from Intel Corporation may be used in the present embodiment as the AGP.

[0150] Increases in computer screen size, graphics resolution, color depth, and visual motion frame rates, used by operating system and application software alike, have increased the computing power required to generate and maintain computer screen displays. An AGP removes a substantial portion of the graphics computing burden from the CPU to the specialized high-performance processor, but a high level of interaction between the CPU and the specialized processor is nonetheless required. To maximize the effective contribution of having a specialized processor in the presently described embodiment, the AGP 1752 is located in the ACM 1700, where it is in close proximity to the microprocessor 1712. The AGP 1752 is coupled to the microprocessor 1712 via the advanced graphics port bus 1773 of the CPU Bridge 1746. The visual display signal generated by the AGP are conveyed toward actual display devices at the peripheral console (PCON) via video signal bus 1770. Video information from a source external to the ACM and appearing as video port signals 1917 may be conveyed to the AGP 1752 via video port signal path 1771.

[0151] Other types of high performance components may be included in different ACM configurations. For example, an interface to an extremely high speed data communication facility may be desirable in some future computer where CPU-to-network interaction is of comparable intensity to today's CPU-to-graphics interaction. Because such high performance components tend to be high in cost, their inclusion in the ACM is desirable. Inclusion of high cost, high performance components in the ACM concentrates a user's core computing power and environment in a portable package. This represents a further advantage of the invention.

[0152] The interface and support component 1740 of the ACM functional circuitry 1701 in the present embodiment comprises circuitry for power regulation 1742, clocking 1744, CPU Bridge 1746, IDE controller 1748, and signal conveyance paths 1761-1774. The CPU Bridge 1746 couples the CPU component 1710 of the ACM 1700 with the other components of the ACM 1720-1750 and the CPU-to-PCON Interconnection 1900. The CPU Bridge 1746 and IDE controller 1748 have already been discussed. Power regulation circuitry 1742 receives electrical power via the electrical power conduction path 1914 of the CPU-to-PCON Interconnection 1900, conditions and distributes it to the

other circuitry in the ACM using power distribution bus 1768. Such regulation and distribution is well known and understood in the art.

[0153] Clocking circuitry 1744 generates clock signals for distribution to other components within the ACM 1700 that require a timing and synchronization clock source. The CPU 1710 is one such component. Often, the total power dissipated by a CPU is directly proportional to the frequency of its main clock signal. The presently described embodiment of the ACM 1700 includes circuitry that can vary the frequency of the main CPU clock signal conveyed to the CPU via signal path 1762, in response to a signal received from the host interface controller (HIC) 1920 via signal path 1761. The generation and variable frequency control of clocking signals is well understood in the art. By varying the frequency, the power consumption of the CPU (and thus the entire ACM) can be varied.

[0154] The variable clock rate generation may be exploited to match the CPU power consumption to the available electrical power. Circuitry in the host interface controller (HIC) 1920 of the presently described embodiment adjusts the frequency control signal sent via signal path 1761 to the clocking circuitry 1744, based on the “console type” information signal 1918 conveyed from the peripheral console (PCON) by the CPU-to-PCON interconnection 1900. In this arrangement, the console type signal originating from a desktop PCON would result in the generation of a maximum speed CPU clock. The desktop PCON, presumably has unlimited power from an electrical wall outlet and does not need to sacrifice speed for power conservation. The console type signal originating from a notebook PCON would, however, result in the generation of a CPU clock speed reduced from the maximum in order to conserve battery power and extend the duration of computer operation obtained from the energy stored in the battery. The console type signal originating from a notepad PCON would result in the generation of a CPU clock speed reduced further yet, the notepad PCON presumably having smaller batteries than the notebook PCON. Inclusion of control signals and circuitry to effect a CPU clock signal varying in frequency according to characteristics of the PCON to which the ACM is connected facilitates the movement of the user’s core computing power and environment to different work settings, which is a further advantage of the present invention.

[0155] FIG. 19 illustrates an external view of one embodiment of an ACM. The case 2010 of the ACM 1700 is generally rectangular in shape, preferably constructed of a strong, lightweight, rigid material that will protect the internal components from mechanical and environmental exposure. Plastics may readily be used to construct the case 2010. The case 2010 completely surrounds the internal components, being generally an 8-sided box. FIG. 19 shows the top 2012, right 2014, and rear 2016 surfaces of the ACM case 2010. Rear edges 2018 of the case joining the rear surface 2016 with its adjoining surfaces may be beveled or rounded to facilitate insertion of the ACM 1700 into the computer bay of the PCON. Notches 2040 may be formed by projecting small surfaces inward from otherwise generally flat surfaces of the ACM case 2010. The notches 2040 may be used to engage with mechanical devices mounted in and about a computer bay. Such mechanical devices can be employed to secure the ACM into position within a computer bay for reliability and security. Openings 2017 are formed into the rear surface 2016 of the ACM case 2010 through which to project connectors 1930a and 1930b. In one embodiment the case 2010 is approximately 5.75 inches wide by 6.5 inches deep by 1.6 inches high.

[0156] Connectors 1930a and 1930b are part of the ACM-to-PCON Interconnection as described earlier in reference to FIGS. 3 and 4. When the ACM 1700 is inserted into the computer bay of a peripheral console (PCON), connectors 1930a and 1930b mate with corresponding connectors located at the rear of the computer bay to electrically couple the ACM with the PCON containing the computer bay. Details concerning the ACM-to-PCON Interconnection can be found in the U.S. patent application entitled “A Communication Channel and Interface Devices for Bridging Computer Interface Buses,” already incorporated herein by reference. The connectors 1930a and 1930b used in one embodiment are connectors complying with the Device Bay industry standard as documented in “Device Bay Interface Specification,” revision 0.85, Feb. 6, 1998. Such connectors have specifically been designed to stand up to the rigors of repeated insertion and withdrawal.

[0157] Cooling plate 2030 forms part of the top surface 2012 of ACM 1700. The cooling plate 2030 may be mounted to, or project through an opening formed in, case 2010. Similarly, electromagnetic interference (EMI)/electrostatic discharge (ESD) grounding plate 2032 forms part of the right surface 2014 of ACM 1700. The grounding

plate 2032 may be mounted to, or project through an opening formed in, case 2010. Cooling plate 2030 and grounding plate 2032 compressively mate with counterparts when the ACM is fully inserted into the computer bay. The counterparts located along the boundaries of the computer bay conduct dangerous heat and electrical charges away from the ACM. Inside the ACM, cooling plate 2030 thermally couples to heat-sensitive components such as CPU 1710 by methods well known in the art. Similarly, grounding plate 2032 electrically couples to EMI/ESD-sensitive components, such as a microprocessor, by methods well known in the art.

[0158] LCD display 2050 forms part of the right surface 2014 of ACM 1700. The LCD display may be mounted to, or project through an opening formed in, case 2010. The LCD display may contain indicators about the status of the ACM. Such indicators may display, for example, the time-of-day from a time-of-day clock contained within the ACM, or the amount of charge remaining in an ACM-resident battery, or certain configuration options recorded in flash memory. The LCD display 2050 provides display capability for a limited amount of information, most useful when the ACM is separated from a PCON (and is thus separated from a full-capability, primary display device).

[0159] FIG. 19b illustrates one possible embodiment of a computer bay. A computer bay 1890 acts as a receptacle for lodging an ACM (such as the one shown in FIG. 20) within a desktop PCON. The illustrated computer bay 1890 provides an ACM with housing and with signal flow, electrical grounding, heat transfer, and mechanical connections. While many physical arrangements between the ACM and PCON are possible, the use of an enclosed computer bay as the one illustrated in FIG. 20b offers many advantages. For example, the illustrated computer bay 1890 provides physical protection for the ACM. The computer bay may also be easily incorporated into industry standard form factors used in the manufacture of desktop personal computers (e.g., the ACM and associated computer bay could be designed to fit within the volume occupied by a standard-size disk drive).

[0160] The computer bay 1890 appearing in FIG. 20b is shown mounted within the confines of PCON case 1802. The computer bay 1890 comprises frame 1891 and signal flow, grounding, cooling, and locking components as described below. Mounting flanges 1898 of frame 1891 may be used to attach the computer bay 1890 to the PCON structure. The computer bay 1890 is prominently defined by frame 1891 generally forming a cavity

in which to lodge an ACM. As such, the interior cavity formed by frame 1891 closely approximates the exterior dimensions of a compatible ACM. The top 1893, right 1894, and rear 1895 sides of the computer bay frame 1891 are visible. The computer bay frame 1891 also includes substantial bottom and left sides which are not shown. The front side of the frame 1891 (not shown) is open to allow the insertion of the ACM. Frame 1891 is constructed of metal for strength and to facilitate the conductance of heat and undesired electrical currents away from the ACM.

[0161] In the presently described embodiment, the weight of an inserted ACM is largely borne by the bottom side (not shown) of computer bay frame 1891. Alternative embodiments are possible where, for example, the weight of the ACM is borne by rails running longitudinally down the right and left sides of the computer bay cavity that engage corresponding grooves running longitudinally down the right and left sides of an ACM.

[0162] FIG. 20 illustrates the internal component layout for one embodiment of an ACM. All components are contained within the confines of the ACM case 510, except for connectors 1930a and 1930b which extend from the rear of the ACM 1700 to engage mating connectors (not shown) that will couple the ACM circuitry with the PCON circuitry. Main circuit board 2110 provides electrical connections for circuitry within the ACM and mounting for many of its components 1724, 1722, 17221, 1752, 1742, 1748, 1920, and 1930. The fabrication and use of such circuits boards is well known and understood in the art. Connector 2122 is also mounted on main circuit board 2110 and mates with mobile processor module 2120. Mobile processor module 2120 represents a form of packaging for a microprocessor and related components. The illustrated mobile processor module 2120 is a self-contained unit that includes a microprocessor 1712, CPU cache 1714, and CPU bridge 1746 operatively interconnected by the manufacturer. An example of one such module is the Pentium Processor with MMX Technology Mobile Module from Intel Corporation (order number 24 3515-001, September 1997). One skilled in the art recognizes that discrete microprocessor, cache, and bridge could have been employed and mounted directly to the main circuit board.

[0163] The mobile processor module 2120 blocks the view, from the top, of the system BIOS 1724. Similarly, hard disk drive 1732 hides RAM memory 1722, the high performance graphics processor 1752, the host interface controller 1920, and flash

memory 1726. Memory upgrade socket 2130 remains exposed to facilitate installation of additional RAM memory 1722. Power regulator 1742, like the memory upgrade socket, enjoys a generous amount of overhead clearance to accommodate its vertical size. The area including IDE controller 1748 also enjoys overhead clearance to facilitate a cable connection with the hard disk drive 1732.

[0164] The functional interconnection and operation of components contained within the ACM and depicted in FIG. 20 has already been described in relation to FIG. 18 for like numbered items appearing therein.

[0165] FIG. 21 is a block diagram of a peripheral console (PCON). A peripheral console couples with an ACM to form an operating personal computer system. The peripheral console (PCON) supplies an ACM with primary input, display, and power supply; the ACM supplies the core computing power and environment of the user. In the presently described embodiment the physical PCON package 200 contains the PCON functional components 1801 and the PCON side of the ACM-to-PCON Interconnection 1900. The PCON functional components 1801 comprise primary display 1810, a primary input 1820, a primary power supply 1830, interface and support 1840, secondary mass storage 1850, other devices 1860, and expansion slots 1870.

[0166] The PCON side of the ACM-to-PCON Interconnection 1900 comprises a Peripheral Interface Controller (PIC) component 1940, a PCON connector component 1950, console-type component 1942, and flash memory device 1948. The PIC 1940 and connector 1950 components couple the PCON functional components 1801 with the signals of an ACM-to-PCON interface bus 1910 used to operatively connect an ACM with a PCON. The ACM-to-PCON interface bus 1910 comprises conveyance for electrical power 1914 and signals for a peripheral bus 1912, video 1916, video port 1917, and console-type 1918. The preferred ACM-to-PCON Interconnection 1900 is described in detail in the U.S. patent application entitled “A Communication Channel and Interface Devices for Bridging Computer Interface Buses,” already incorporated herein by reference.

[0167] Connector component 1950 may be selected to mate directly with the connector component 1930 of an ACM (shown in FIG. 18). Alternatively, connector component 1950 may be selected to mate with, for example, the connector on one end of a cable

intervening between the PCON and an ACM in a particular embodiment, such as cable 1964 shown in FIG. 19B. The ACM-to-PCON interconnection described in the aforementioned companion patent application has the advantage of providing reliable signal conveyance across low cost cables.

[0168] Flash memory device 1948 provides non-volatile storage. This storage may be accessible to devices in both the ACM and the PCON, including the host interface controller and the peripheral interface controller to which it is connected. As such, flash memory 1948 may be used to store configuration and security data to facilitate an intelligent mating between an ACM and a PCON that needs no participation of the CPU.

[0169] The primary display component 1810 of the PCON functional circuitry 1801 of the presently described embodiment comprises integrated display panel 1812 and video connector 1813. Integrated display panel 1812 is a color LCD display panel having a resolution of 640 horizontal by 480 vertical pixels. 640-by-480 resolution is popularly considered to be the minimum screen size to make practical use of the application software in widespread use today. One skilled in the art recognizes that the type and resolution of the display can vary greatly from embodiment to embodiment, depending on factors such as cost and intended application. Any display device may be used, without departing from the scope and spirit of the invention, that provides principal visual output to the computer user for operating system and application software executing in its customary and intended fashion using the CPU component (1710 of FIG. 17) of an ACM presently coupled to PCON 1800.

[0170] Integrated display panel 1812 is coupled to video signal bus 1849 and displays a screen image in response to video signals presented on bus 1849. Certain pins of connector 1950 receive video output signals 1916 of the ACM-to-PCON interface bus 1910 from a mated connector that is coupled to an ACM. These certain pins of connector 1950 couple to video signal bus 1849 which conveys the video output signals 316 throughout the PCON 1800 as needed. Video connector 1813 is exposed at the exterior of PCON 1800 and couples to video signal bus 1849. Connector 1813 permits easy attachment of an external display device that is compatible with the signals carried by bus 1849, such as a CRT monitor (not shown). The external display device may be used in addition, or as an alternative, to integrated display panel 1812.

[0171] The isolation of the relatively heavy and sizable primary display 1810 from the core computing power and user environment contained within an ACM represents a further advantage of the present invention.

[0172] The primary input component 1820 of the PCON functional circuitry 1801 of the presently described embodiment comprises keyboard interface circuitry 1822, keyboard connector 1823, pointer interface circuitry 1824, and pointer connector 1825. Keyboard interface circuitry 1822 and pointer interface circuitry 1824 connect to ISA bus 1845 and are thereby coupled to the CPU component (1710 of FIG. 17) of any ACM attached to PCON 1800. Keyboard interface circuitry 1822 interfaces a standard computer keyboard (not shown), attached at connector 1823, to ISA bus 1845. Pointer interface circuitry 1822 interfaces a standard computer pointing device (not shown), such as a computer mouse attached at connector 1825, to ISA bus 1845. Computer keyboards, pointing devices, connectors 1823, 1825, keyboard interface circuitry 1822, and pointer interface circuitry 1824 are well known in the art. The isolation of the relatively heavy and sizable primary input devices 1820 from the core computing power and user environment contained within an ACM represents a further advantage of the present invention.

[0173] The primary power supply component 1830 of the PCON functional circuitry 1801 of the presently described embodiment provides electrical energy for the sustained, normal operation of the PCON 1800 and any ACM coupled to connector 1950. The power supply may be of the switching variety well known in the art that receives electrical energy from an AC source 1889, such as a wall outlet. Power supply 1830 reduces the alternating current input voltage, to a number of distinct outputs of differing voltages and current capacities. The outputs of power supply 1830 are applied to power bus 1831. Power bus 1831 distributes the power supply outputs to the other circuitry within the PCON 1800. Bus 1831 also connects to certain pins of connector 1950 to provide the electrical power 1914 for an ACM conveyed by ACM-to-PCON interconnection 1900. The isolation of the usually heavy power supply 1830 from the core computing power and user environment contained within the ACM represents a further advantage of the present invention.

[0174] The interface and support component 1840 of the PCON functional circuitry 1801 of the presently described embodiment comprises peripheral bridge 1846, diskette controller 1842, IDE controller 1848, and signal conveyance paths 1841, 1843, 1844,

1845, 1847 and 1849. Peripheral bridge 1846 couples PCI peripheral bus 1841 with peripheral busses of other formats such as ISA peripheral bus 1845 and others 1847. PCI and ISA peripheral busses are industry standards, well known and understood in the art. Other peripheral busses 1847 may include, for example, a bus compliant with the universal serial bus (USB) industry standard. While other embodiments of a peripheral console 1800 may include a single peripheral bus that is coupled to an attached ACM via ACM-to-PCON interconnection 1900, such as PCI bus 1841, this embodiment includes peripheral bridge 1846 to establish additional busses 1845, 1847. The additional busses 1845, 1847 permit the use of the many low-cost and readily available components compatible with these bus specifications.

[0175] Diskette controller 1842 interfaces a floppy disk drive 1854 with the CPU component 1710 of an attached ACM (shown in FIG. 18) so that the CPU may control and use the diskette drive 1854 hardware to store and retrieve data. Diskette controller 1842 couples to the CPU via a connection to ISA bus 1845. Diskette controller 1842 connects to the diskette drive 1854 via one of device cables 1843.

[0176] Similarly, IDE controller 1848 interfaces a hard disk drive 1852 and a CDROM drive 1856 with the CPU component 1710 of an attached ACM (shown in FIG. 18) so that the CPU may control and use the hard disk drive 1852 and CDROM 1856 hardware to store and retrieve data. IDE controller 1848 couples to the CPU via connection to PCI peripheral bus 1841. IDE controller 1848 connects to each of hard disk drive 1852 and CD-ROM drive 1856 via one of device cables 1843. Some embodiments of PCON 1800 may take advantage of VLSI integrated circuits such as an 82371SB (PIIX4) integrated circuit from Intel Corporation. An 82371SB integrated circuit includes circuitry for both the peripheral bridge 1846 and the IDE controller 1848 in a single package.

[0177] The secondary mass storage component 1850 of the PCON functional circuitry 1801 of the presently described embodiment comprises diskette drive 1854, hard disk drive 1852, and CD-ROM drive 1856. Secondary mass storage 1850 generally provides low-cost, non-volatile storage for data files which may include software program files. Data files stored on secondary mass storage 1850 are not part of a computer user's core computing power and environment. Secondary mass storage 1850 may be used to store, for example, seldom used software programs, software programs that are used only with companion hardware devices installed in the same peripheral console 1800, or archival

copies of data files that are maintained in primary mass storage 1750 of an ACM (shown in FIG. 18). Storage capacities for secondary mass storage 1850 devices may vary from the 1.44 megabytes of the 3.5-inch high density diskette drive 1854, to more than 10 gigabytes for a large format (5-inch) hard disk drive 1852. Hard disk drive 1852 employs fixed recording media, while diskette drive 1854 and CD-ROM drive 1856 employ removable media. Diskette drive 1854 and hard disk drive 1852 support both read and write operations (i.e., data stored on their recording media may be both recalled and modified) while CD-ROM drive 1856 supports only read operations.

[0178] The other devices component 1860 of the PCON functional circuitry 1801 of the presently described embodiment comprises a video capture card. A video capture card accepts analog television signals, such as those complying with the NTSC standard used for television broadcast in the United States, and digitizes picture frames represented by the analog signal for processing by the computer. Video capture cards at present are considered a specialty, i.e., not ubiquitous, component of personal computer systems. Digitized picture information from video capture card 1860 is carried via signal conveyance path 1844 to the peripheral interface controller 1940 which transforms it to the video port signals 1917 of the ACM-to-PCON interconnection 1900 for coupling to the advanced graphics processor 1752 in an attached ACM (shown in FIG. 18).

[0179] Video capture card 1860 is merely representative of the many types of “other” devices that may be installed in a PCON to expand the capabilities of the personal computer. Sound cards and laboratory data acquisition cards are other examples. Video capture card 1860 is shown installed in one of expansion slots 1870 for coupling to the interface and control circuitry 1840 of the PCON. Any of other devices 1860 could be coupled to the interface and control circuitry 1840 of the PCON by different means, such as direct installation on the circuit board that includes the interface and control circuitry 1840; e.g., a motherboard.

[0180] The expansion slots component 1870 of the PCON functional circuitry 1801 of the presently described embodiment comprises PCI connectors 1871 and ISA connectors 1872. A circuit card may be inserted into one of the connectors 1871, 1872 in order to be operatively coupled with the CPU 1710 of an attached ACM (shown in FIG. 18). Each of connectors 1871 electrically connects to PCI bus 1841, and may receive and hold a printed circuit card which it electrically couples to PCI bus 1841. Each of connectors

1872 electrically connects to ISA bus 1845, and may receive and hold a printed circuit card which it electrically couples to ISA bus 1845. The PCI 1841 and ISA 1845 busses couple to the CPU 1710 of an attached ACM (shown in FIG. 18) by circuitry already described.

[0181] An embodiment of a detachable computing module in accordance with the present invention, for attachment to a peripheral console for forming a fully operational computer system, comprises, an enclosure, a CPU, a memory coupled to said CPU, and a mass storage coupled to said CPU. The module further comprises interconnection circuitry coupled to said CPU, said interconnection circuitry connectable to a peripheral console. The CPU is uncoupled from any primary input circuitry when said interconnection circuitry is disconnected from a peripheral console.

[0182] An alternative embodiment of a detachable computing module in accordance with the present invention, for attachment to a peripheral console for forming a fully operational computer system, comprises an enclosure, a CPU, a memory coupled to said CPU, and a mass storage coupled to said CPU. The module further comprises interconnection circuitry coupled to said CPU, said interconnection circuitry connectable to a peripheral console. The CPU is uncoupled from any primary output circuitry when said interconnection circuitry is disconnected from a peripheral console.

[0183] Various modifications to the preferred embodiment can be made without departing from the spirit and scope of the invention. (A limited number of modifications have already been described in the preceding discussion.) For example, a particular embodiment may insert another layer of bus bridging between the CPU bridge and the Peripheral bridge. This may be desirable if, for example, a vendor wants to implement a proprietary, general-purpose bus having intermediate performance characteristics that fall between those of the high-performance general purpose bus originating at the CPU, and the slower general purpose PCI bus. Thus, the foregoing description is not intended to limit the invention as set forth.

[0184] In most embodiments, the ACM includes an enclosure such as the one described with the following components, which should not be limiting:

- 1) A CPU with cache memory;
- 2) Core logic device or means;

- 3) Main memory;
- 4) A single primary Hard Disk Drive (“HDD”) that has a security program;
- 5) Flash memory with system BIOS and programmable user password;
- 6) Operating System, application software, data files on primary HDD;
- 7) An interface device and connectors to peripheral console;
- 8) A software controllable mechanical lock, lock control means, and other accessories.

[0185] The ACM connects to a peripheral console with power supply, a display device, an input device, and other elements. Some details of these elements with the present security system are described in more detail below.

[0186] FIG. 22 is a simplified layout diagram of a security system for a computer system according to an embodiment of the present invention. This diagram is merely an illustration and should not limit the scope of the claims herein. One of ordinary skill in the art would recognize other variations, modifications, and alternatives. The layout diagram illustrates the top-view of the module 22, where the backside components (e.g., Host Interface Controller) are depicted in dashed lines. The layout diagram has a first portion, which includes a central processing unit (“CPU”) module 2200, and a second portion, which includes a hard drive module 2220. A common printed circuit board 2237 houses these modules and the like. Among other features, the ACM includes the central processing unit module 2200 with a cache memory 2205, which is coupled to a north bridge unit 2221, and a host interface controller 2201. The host interface controller includes a lock control 2203. As shown, the CPU module is disposed on a first portion of the attached computer module, and couples to connectors 2217. Here, the CPU module is spatially located near connector 2217.

[0187] The CPU module can use a suitable microprocessing unit, microcontroller, digital signal processor, and the like. In a specific embodiment, the CPU module uses, for example, a 400 MHz Pentium II microprocessor module from Intel Corporation and like microprocessors from AMD Corporation, Cyrix Corporation (now National Semiconductor Corporation), and others. In other aspects, the microprocessor can be one such as the Compaq Computer Corporation Alpha Chip, Apple Computer Corporation PowerPC G3 processor, and the like. Further, higher speed processors are contemplated in other embodiments as technology increases in the future.

[0188] In the CPU module, host interface controller 2201 is coupled to BIOS/flash memory 2205. Additionally, the host interface controller is coupled to a clock control logic, a configuration signal, and a peripheral bus. The present invention has a host interface controller that has lock control 2203 to provide security features to the present ACM. Furthermore, the present invention uses a flash memory that includes codes to provide password protection or other electronic security methods.

[0189] The second portion of the attached computer module has the hard drive module 2220. Among other elements, the hard drive module includes north bridge 2221, graphics accelerator 2223, graphics memory 2225, a power controller 2227, an IDE controller 2229, and other components. Adjacent to and in parallel alignment with the hard drive module is a personal computer interface (“PCI”) bus 2231, 2232. A power regulator 435 is disposed near the PCI bus.

[0190] In a specific embodiment, north bridge unit 2221 often couples to a computer memory, to the graphics accelerator 2223, to the IDE controller, and to the host interface controller via the PCI bus. Graphics accelerator 2223 typically couples to a graphics memory 2223, and other elements. IDE controller 2229 generally supports and provides timing signals necessary for the IDE bus. In the present embodiment, the IDE controller is embodied as a 643U2 PCI-to IDE chip from CMD Technology, for example. Other types of buses than IDE are contemplated, for example EIDE, SCSI, 1394, and the like in alternative embodiments of the present invention.

[0191] The hard drive module or mass storage unit 2220 typically includes a computer operating system, application software program files, data files, and the like. In a specific embodiment, the computer operating system may be the Windows98 operating system from Microsoft Corporation of Redmond Wash. Other operating systems, such as WindowsNT, MacOS8, Unix, and the like are also contemplated in alternative embodiments of the present invention. Further, some typical application software programs can include Office98 by Microsoft Corporation, Corel Perfect Suite by Corel, and others. Hard disk module 2220 includes a hard disk drive. The hard disk drive, however, can also be replaced by removable hard disk drives, read/write CD ROMs, flash memory, floppy disk drives, and the like. A small form factor, for example 2.5”, is currently contemplated, however, other form factors, such as PC card, and the like are also contemplated. Mass storage unit 2240 may also support other interfaces than IDE.

Among other features, the computer system includes an ACM with security protection. The ACM connects to the console, which has at least the following elements, which should not be limiting.

- 1) Connection to input devices, e.g. keyboard or mouse;
- 2) Connection to display devices, e.g. Monitor;
- 3) Add-on means, e.g. PCI add-on slots;
- 4) Removable storage media subsystem, e.g. Floppy drive, CDROM drive;
- 5) Communication device, e.g. LAN or modem;
- 6) An interface device and connectors to ACM;
- 7) A computer module bay with a notch in the frame for ACM's lock; and
- 8) Power supply and other accessories.

[0192] As noted, the computer module bay is an opening in a peripheral console that receives the ACM. The computer module bay provides mechanical support and protection to ACM. The module bay also includes, among other elements, a variety of thermal components for heat dissipation, a frame that provides connector alignment, and a lock engagement, which secures the ACM to the console. The bay also has a printed circuit board to mount and mate the connector from the ACM to the console. The connector provides an interface between the ACM and other accessories.

[0193] FIG. 23 is a simplified block diagram 2300 of a security system for a computer module according to an embodiment of the present invention. This diagram is merely an illustration and should not limit the scope of the claims herein. One of ordinary skill in the art would recognize other variations, modifications, and alternatives. The block diagram 2300 has a variety of features such as those noted above, as well as others. In the present diagram, different reference numerals are used to show the operation of the present system.

[0194] The block diagram is an attached computer module 2300. The module 2300 has a central processing unit, which communicates to a north bridge 2341, by way of a CPU bus 2327. The north bridge couples to main memory 2323 via memory bus 2329. The main memory can be any suitable high speed memory device or devices such as dynamic random access memory ("DRAM") integrated circuits and others. The DRAM includes at least 32 Meg. or 64 Meg. and greater of memory, but can also be less depending upon the

application. Alternatively, the main memory can be coupled directly with the CPU in some embodiments. The north bridge also couples to a graphics subsystem 2315 via bus 2342. The graphics subsystem can include a graphics accelerator, graphics memory, and other devices. Graphics subsystem transmits a video signal to an interface connector, which couples to a display, for example.

[0195] The attached computer module also includes a primary hard disk drive that serves as a main memory unit for programs and the like. The hard disk can be any suitable drive that has at least 2 GB and greater. As merely an example, the hard disk is a Marathon 2250 (2.25 GB, 2 1/2 inch drive) product made by Seagate Corporation of Scotts Valley, but can be others. The hard disk communicates to the north bridge by way of a hard disk drive controller and bus lines 2302 and 2331. The hard disk drive controller couples to the north bridge by way of the host PCI bus, which connects bus 2337 to the north bridge. The hard disk includes computer codes that implement a security program according to the present invention. Details of the security program are provided below.

[0196] The attached computer module also has a flash memory device 2305 with a BIOS. The flash memory device 2305 also has codes for a user password that can be stored in the device. The flash memory device generally permits the storage of such password without a substantial use of power, even when disconnected. As merely an example, the flash memory device has at least 4 Meg. or greater of memory, or 16 Meg. or greater of memory. A host interface controller 2307 communicates to the north bridge via bus 2335 and host PCI bus. The host interface controller also has a Lock control 2309, which couples to a lock. The lock is attached to the module and has a manual override to the lock on the host interface controller in some embodiments. Host interface controller 2307 communicates to the console using bus 2311, which couples to connection 2313.

[0197] In a preferred embodiment, the present invention uses a password protection scheme to electronically prevent unauthorized access to the computer module. The present password protection scheme uses a combination of software, which is a portion of the security program, and a user password, which can be stored in the flash memory device 505. By way of the flash memory device, the password does not become erased by way of power failure or the lock. The password is substantially fixed in code, which

cannot be easily erased. Should the user desire to change the password, it can readily be changed by erasing the code, which is stored in flash memory and a new code (i.e., password) is written into the flash memory. An example of a flash memory device can include a Intel Flash 28F800F3 series flash, which is available in 8 Mbit and 16 Mbit designs. Other types of flash devices can also be used, however. Details of a password protection method are further explained below by way of the FIGS.

[0198] In a specific embodiment, the present invention also includes a real-time clock 510 in the ACM, but is not limited. The real-time clock can be implemented using a reference oscillator 14.31818 MHz 508 that couples to a real-time clock circuit. The real-time clock circuit can be in the host interface controller. An energy source 506 such as a battery can be used to keep the real-time clock circuit running even when the ACM has been removed from the console. The real-time clock can be used by a security program to perform a variety of functions. As merely an example, these functions include: (1) fixed time period in which the ACM can be used, e.g., ACM cannot be used at night; (2) programmed ACM to be used after certain date, e.g., high security procedure during owner's vacation or non use period; (3) other uses similar to a programmable time lock. Further details of the present real-time clock are described in the application listed under Ser. No. 09/183,816 noted above.

[0199] In still a further embodiment, the present invention also includes a permanent password or user identification code to identify the computer module. In one embodiment, the permanent password or user code is stored in a flash memory device. Alternatively, the permanent password or user code is stored in the central processing unit. The password or user code can be placed in the device upon manufacture of such device. Alternatively, the password or user code can be placed in the device by a one time programming techniques using, for example, fuses or the like. The present password or user code provides a permanent "finger print" on the device, which is generally hardware. The permanent finger print can be used for identification purposes for allowing the user of the hardware to access the hardware itself, as well as other systems. These other systems include local and wide area networks. Alternatively, the systems can also include one or more servers. The present password and user identification can be quite important for electronic commerce applications and the like. In one or more embodiments, the

permanent password or user code can be combined with the password on flash memory for the security program, which is described below in more detail.

[0200] In one aspect of the invention, the user password is programmable. The password can be programmable by way of the security program. The password can be stored in a flash memory device within the ACM. Accordingly, the user of the ACM and the console would need to have the user password in order to access the ACM. In the present aspect, the combination of a security program and user password can provide the user a wide variety of security functions as follows:

- 1) Auto-lock capability when ACM is inserted into CMB;
- 2) Access privilege of program and data;
- 3) Password matching for ACM removal; and
- 4) Automatic HDD lock out if tempering is detected.

[0201] In still a further embodiment, the present invention also includes a method for reading a permanent password or user identification code to identify the computer module. In one embodiment, the permanent password or user code is stored in a flash memory device. Alternatively, the permanent password or user code is stored in the central processing unit. The password or user code can be placed in the device upon manufacture of such device. Alternatively, the password or user code can be placed in the device by a one time programming techniques using, for example, fuses or the like. The present password or user code provides a permanent “finger print” on the device, which is generally hardware. The permanent finger print can be used for identification purposes for allowing the user of the hardware to access the hardware itself, as well as other systems. These other systems include local and wide area networks. Alternatively, the systems can also include one or more servers. The present method allows a third party confirm the user by way of the permanent password or user code. The present password and user identification can be quite important for electronic commerce applications and the like, which verify the user code or password. In one or more embodiments, the permanent password or user code can be combined with the password on flash memory for the security program.

[0202] The above embodiments are described generally in terms of hardware and software. It will be recognized, however, that the functionality of the hardware can be

further combined or even separated. The functionality of the software can also be further combined or even separated. Hardware can be replaced, at times, with software. Software can be replaced, at times, with hardware. Accordingly, the present embodiments should not be construed as limiting the scope of the claims here. One of ordinary skill in the art would recognize other variations, modifications, and alternatives.

[0203] While the above is a full description of the specific embodiments, various modifications, alternative constructions and equivalents may be used. Therefore, the above description and illustrations should not be taken as limiting the scope of the present invention which is defined by the appended claims.

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International Application Number:	
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Title of Invention:	MULTIPLE MODULE COMPUTER SYSTEM AND METHOD INCLUDING DIFFERENTIAL SIGNAL CHANNEL COMPRISING UNIDIRECTIONAL SERIAL BIT CHANNELS
First Named Inventor/Applicant Name:	William W.Y. Chu
Customer Number:	58249
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Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1	Applicant Response to Pre-Exam Formalities Notice	ACQI01019US_Response.pdf	58645 c15de793010cf9a4cdc25c20f35b1a04d4554243	no	1

Warnings:

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2	Specification	ACQI01019US_Substitute_Markup.pdf	270788 eb0d9a222442b86a370a9dd1ed5c8b64ceb89e25	no	56
Warnings:					
Information:					
3	Specification	ACQI01019US_Substitute_Clean.pdf	270710 f2bc3b88c64cf47c2ec7f61bf556d9a9c5f60e	no	56
Warnings:					
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Total Files Size (in bytes):			600143		
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13/087,912	04/15/2011	2111	3686	ACQI-010/19US 310578-2066	53	7

CONFIRMATION NO. 7269

UPDATED FILING RECEIPT



OC000000047745482

58249
COOLEY LLP
ATTN: Patent Group
Suite 1100
777 - 6th Street, NW
WASHINGTON, DC 20001

Date Mailed: 05/20/2011

Receipt is acknowledged of this non-provisional patent application. The application will be taken up for examination in due course. Applicant will be notified as to the results of the examination. Any correspondence concerning the application must include the following identification information: the U.S. APPLICATION NUMBER, FILING DATE, NAME OF APPLICANT, and TITLE OF INVENTION. Fees transmitted by check or draft are subject to collection. Please verify the accuracy of the data presented on this receipt. **If an error is noted on this Filing Receipt, please submit a written request for a Filing Receipt Correction. Please provide a copy of this Filing Receipt with the changes noted thereon. If you received a "Notice to File Missing Parts" for this application, please submit any corrections to this Filing Receipt with your reply to the Notice. When the USPTO processes the reply to the Notice, the USPTO will generate another Filing Receipt incorporating the requested corrections**

Applicant(s)

William W.Y. Chu, Los Altos, CA;

Assignment For Published Patent Application

ACQIS LLC, McKinney, TX

Power of Attorney: The patent practitioners associated with Customer Number 58249

Domestic Priority data as claimed by applicant

This application is a CON of 12/504,534 07/16/2009
which is a CON of 12/077,503 03/18/2008 PAT 7,676,624
which is a CON of 11/166,656 06/24/2005 PAT 7,376,779
which is a CON of 11/097,694 03/31/2005 PAT 7,363,415
which is a CON of 10/772,214 02/03/2004 PAT 7,099,981
which is a CON of 09/569,758 05/12/2000 PAT 6,718,415
which claims benefit of 60/134,122 05/14/1999

Foreign Applications (You may be eligible to benefit from the **Patent Prosecution Highway** program at the USPTO. Please see <http://www.uspto.gov> for more information.)

If Required, Foreign Filing License Granted: 04/26/2011

The country code and number of your priority application, to be used for filing abroad under the Paris Convention, is **US 13/087,912**

Projected Publication Date: 08/25/2011

Non-Publication Request: No

Early Publication Request: No

Title

MULTIPLE MODULE COMPUTER SYSTEM AND METHOD INCLUDING DIFFERENTIAL SIGNAL CHANNEL COMPRISING UNIDIRECTIONAL SERIAL BIT CHANNELS

Preliminary Class

710

PROTECTING YOUR INVENTION OUTSIDE THE UNITED STATES

Since the rights granted by a U.S. patent extend only throughout the territory of the United States and have no effect in a foreign country, an inventor who wishes patent protection in another country must apply for a patent in a specific country or in regional patent offices. Applicants may wish to consider the filing of an international application under the Patent Cooperation Treaty (PCT). An international (PCT) application generally has the same effect as a regular national patent application in each PCT-member country. The PCT process **simplifies** the filing of patent applications on the same invention in member countries, but **does not result** in a grant of "an international patent" and does not eliminate the need of applicants to file additional documents and fees in countries where patent protection is desired.

Almost every country has its own patent law, and a person desiring a patent in a particular country must make an application for patent in that country in accordance with its particular laws. Since the laws of many countries differ in various respects from the patent law of the United States, applicants are advised to seek guidance from specific foreign countries to ensure that patent rights are not lost prematurely.

Applicants also are advised that in the case of inventions made in the United States, the Director of the USPTO must issue a license before applicants can apply for a patent in a foreign country. The filing of a U.S. patent application serves as a request for a foreign filing license. The application's filing receipt contains further information and guidance as to the status of applicant's license for foreign filing.

Applicants may wish to consult the USPTO booklet, "General Information Concerning Patents" (specifically, the section entitled "Treaties and Foreign Patents") for more information on timeframes and deadlines for filing foreign patent applications. The guide is available either by contacting the USPTO Contact Center at 800-786-9199, or it can be viewed on the USPTO website at <http://www.uspto.gov/web/offices/pac/doc/general/index.html>.

For information on preventing theft of your intellectual property (patents, trademarks and copyrights), you may wish to consult the U.S. Government website, <http://www.stopfakes.gov>. Part of a Department of Commerce initiative, this website includes self-help "toolkits" giving innovators guidance on how to protect intellectual property in specific countries such as China, Korea and Mexico. For questions regarding patent enforcement issues, applicants may call the U.S. Government hotline at 1-866-999-HALT (1-866-999-4158).

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NOT GRANTED

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PATENT APPLICATION FEE DETERMINATION RECORD Substitute for Form PTO-875						Application or Docket Number 13/087,912		
APPLICATION AS FILED - PART I								
(Column 1)		(Column 2)		SMALL ENTITY		OR OTHER THAN SMALL ENTITY		
FOR	NUMBER FILED	NUMBER EXTRA	RATE(\$)	FEE(\$)		RATE(\$)	FEE(\$)	
BASIC FEE (37 CFR 1.16(a), (b), or (c))	N/A	N/A	N/A			N/A	330	
SEARCH FEE (37 CFR 1.16(k), (i), or (m))	N/A	N/A	N/A			N/A	540	
EXAMINATION FEE (37 CFR 1.16(o), (p), or (q))	N/A	N/A	N/A			N/A	220	
TOTAL CLAIMS (37 CFR 1.16(i))	53	minus 20 = *	33			x 52 =	1716	
INDEPENDENT CLAIMS (37 CFR 1.16(h))	7	minus 3 = *	4			x 220 =	880	
APPLICATION SIZE FEE (37 CFR 1.16(s))	If the specification and drawings exceed 100 sheets of paper, the application size fee due is \$270 (\$135 for small entity) for each additional 50 sheets or fraction thereof. See 35 U.S.C. 41(a)(1)(G) and 37 CFR 1.16(s).						0.00	
MULTIPLE DEPENDENT CLAIM PRESENT (37 CFR 1.16(j))							0.00	
* If the difference in column 1 is less than zero, enter "0" in column 2.				TOTAL		TOTAL	3686	
APPLICATION AS AMENDED - PART II								
AMENDMENT A	(Column 1)		(Column 2)		(Column 3)		SMALL ENTITY	OR OTHER THAN SMALL ENTITY
	CLAIMS REMAINING AFTER AMENDMENT	HIGHEST NUMBER PREVIOUSLY PAID FOR	PRESENT EXTRA	RATE(\$)	ADDITIONAL FEE(\$)		RATE(\$)	ADDITIONAL FEE(\$)
	Total (37 CFR 1.16(i))	*	Minus **	=	x =		x =	
	Independent (37 CFR 1.16(h))	*	Minus ***	=	x =		x =	
	Application Size Fee (37 CFR 1.16(s))							
	FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))							
TOTAL ADD'L FEE						TOTAL ADD'L FEE		
AMENDMENT B	(Column 1)		(Column 2)		(Column 3)		SMALL ENTITY	OR OTHER THAN SMALL ENTITY
	CLAIMS REMAINING AFTER AMENDMENT	HIGHEST NUMBER PREVIOUSLY PAID FOR	PRESENT EXTRA	RATE(\$)	ADDITIONAL FEE(\$)		RATE(\$)	ADDITIONAL FEE(\$)
	Total (37 CFR 1.16(i))	*	Minus **	=	x =		x =	
	Independent (37 CFR 1.16(h))	*	Minus ***	=	x =		x =	
	Application Size Fee (37 CFR 1.16(s))							
	FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))							
TOTAL ADD'L FEE						TOTAL ADD'L FEE		
* If the entry in column 1 is less than the entry in column 2, write "0" in column 3. ** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 20, enter "20". *** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 3, enter "3". The "Highest Number Previously Paid For" (Total or Independent) is the highest found in the appropriate box in column 1.								



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APPLICATION NUMBER	FILING OR 371(C) DATE	FIRST NAMED APPLICANT	ATTY. DOCKET NO./TITLE
13/087,912	04/15/2011	William W.Y. Chu	ACQI-010/19US 310578-2066

CONFIRMATION NO. 7269

58249
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WASHINGTON, DC 20001

PUBLICATION NOTICE



OC000000049504026

Title:MULTIPLE MODULE COMPUTER SYSTEM AND METHOD INCLUDING DIFFERENTIAL SIGNAL CHANNEL COMPRISING UNIDIRECTIONAL SERIAL BIT CHANNELS

Publication No.US-2011-0208893-A1

Publication Date:08/25/2011

NOTICE OF PUBLICATION OF APPLICATION

The above-identified application will be electronically published as a patent application publication pursuant to 37 CFR 1.211, et seq. The patent application publication number and publication date are set forth above.

The publication may be accessed through the USPTO's publically available Searchable Databases via the Internet at www.uspto.gov. The direct link to access the publication is currently <http://www.uspto.gov/patft/>.

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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
13/087,912	04/15/2011	William W.Y. Chu	ACQI-010/19US 310578-2066	7269
58249 7590 09/16/2011 COOLEY LLP ATTN: Patent Group Suite 1100 777 - 6th Street, NW WASHINGTON, DC 20001			EXAMINER PHAN, RAYMOND NGAN	
			ART UNIT 2111	PAPER NUMBER
			MAIL DATE 09/16/2011	DELIVERY MODE PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	13/087,912	CHU, WILLIAM W.Y.	
	Examiner	Art Unit	
	RAYMOND PHAN	2111	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1) ☐ Responsive to communication(s) filed on ____.

2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.

3) ☐ An election was made by the applicant in response to a restriction requirement set forth during the interview on ____; the restriction requirement and election have been incorporated into this action.

4) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

5) ☒ Claim(s) 44-96 is/are pending in the application.

5a) Of the above claim(s) 1-43 is/are withdrawn from consideration.

6) ☐ Claim(s) ____ is/are allowed.

7) ☒ Claim(s) 44-96 is/are rejected.

8) ☐ Claim(s) ____ is/are objected to.

9) ☐ Claim(s) ____ are subject to restriction and/or election requirement.

Application Papers

10) ☐ The specification is objected to by the Examiner.

11) ☐ The drawing(s) filed on ____ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

12) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

13) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a) ☐ All b) ☐ Some * c) ☐ None of:

1. ☐ Certified copies of the priority documents have been received.

2. ☐ Certified copies of the priority documents have been received in Application No. ____.

3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)	4) ☐ Interview Summary (PTO-413)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)	Paper No(s)/Mail Date. ____.
3) ☒ Information Disclosure Statement(s) (PTO/SB/08)	5) ☐ Notice of Informal Patent Application
Paper No(s)/Mail Date <u>041511</u> .	6) ☐ Other: ____.

Part III DETAILED ACTION

Notice to Applicant(s)

1. This application has been examined. Claims 44-96 are pending.
2. The Group and/or Art Unit location of your application in the PTO has changed. To aid in correlating any papers for this application, all further correspondence regarding this application should be directed to Group Art Unit 2111.

Specification

3. The title of the invention is not descriptive. A new title is required that is clearly indicative of the invention to which the claims are directed.

Double Patenting

4. The nonstatutory double patenting rejection is based on a judicially created doctrine grounded in public policy (a policy reflected in the statute) so as to prevent the unjustified or improper timewise extension of the "right to exclude" granted by a patent and to prevent possible harassment by multiple assignees. See *In re Goodman*, 11 F.3d 1046, 29 USPQ2d 2010 (Fed. Cir. 1993); *In re Longi*, 759 F.2d 887, 225 USPQ 645 (Fed. Cir. 1985); *In re Van Ornum*, 686 F.2d 937, 214 USPQ 761 (CCPA 1982); *In re Vogel*, 422 F.2d 438, 164 USPQ 619 (CCPA 1970);and, *In re Thorington*, 418 F.2d 528, 163 USPQ 644 (CCPA 1969).

A timely filed terminal disclaimer in compliance with 37 CFR 1.321© may be used to overcome an actual or provisional rejection based on a nonstatutory double patenting ground provided the conflicting application or patent is shown to be commonly owned with this application. See 37 CFR 1.130(b).

Effective January 1, 1994, a registered attorney or agent of record may sign a terminal disclaimer. A terminal disclaimer signed by the assignee must fully comply with 37 CFR 3.73(b).

5. Claims 44, 74 are provisionally rejected on the ground of nonstatutory obviousness-type double patenting as being unpatentable over claim 1 of

copending Application No. 12/504,534. Although the conflicting claims are not identical, they are not patentably distinct from each other because claim 1 of the co-pending Application No. 12/504,534 is similar in scope to claims 44, 47 of the present application with only obvious wording variations.

6. Claims 83, 90 are provisionally rejected on the ground of nonstatutory obviousness-type double patenting as being unpatentable over claim 13 of copending Application No. 12/504,534. Although the conflicting claims are not identical, they are not patentably distinct from each other because claim 13 of the co-pending Application No. 12/504,534 is similar in scope to claims 83, 90 of the present application with only obvious wording variations

This is a provisional obviousness-type double patenting rejection because the conflicting claims have not in fact been patented.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(e) the invention was described in-

(1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effect under this subsection of a national application published under section 122(b) only if the international application designating the United States was published under Article 21(2)(a) of such treaty in the English language; or

(2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that a patent shall not be deemed filed in the United States for the purposes of this subsection based on the filing of an international application filed under the treaty defined in section 351(a).

7. Claims 53-54, 56-57, 83-86, are rejected under 35 U.S.C. § 102(e) as being anticipated by Tripathi et al. (US No. 6,161,157).

In regard to claim 53, 83, Tripathi et al. disclose a computer system comprising: a computer module insertable into a console for operation, the computer module comprising a processing unit, an integrated interface controller and bridge unit to output encoded address and data bits of Peripheral Component Interconnect (PCI) bus transaction in serial form (see col. 4, lines 1-13), the integrated interface controller and bridge unit coupled to the processing unit without any intervening PCI bus, a low voltage differential signal (LVDS) channel coupled to the integrated interface controller and bridge unit to convey the encoded address and data bits of PCI bus transaction in serial form, and a main memory coupled to the processing unit through the integrated interface controller and bridge unit (see figure 1A, col. 4, lines 25-49).

In regard to claim 54, 84, Tripathi et al. disclose further a peripheral component coupled to the integrated interface controller and bridge unit through the LVDS channel (see figure 1A).

In regard to claim 56, Tripathi et al. disclose wherein the integrated interface controller and bridge unit comprises a north bridge and an interface controller integrated with the north bridge (see col. 3, lines 19-27).

In regard to claim 57, 86, Tripathi et al. disclose wherein the computer module comprises an enclosure housing the processing unit, the integrated interface controller and bridge unit, the LVDS channel, and the main memory (see figure 1A).

In regard to claim 85, Tripathi et al. disclose further the console, and the console comprises a LCD display coupled to the graphics subsystem (see figure 1A, col. 3, lines 9-18).

Claim Rejections - 35 USC § 103

8. The following is a quotation of 35 U.S.C. § 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

9. Claims 44-52, 55, 58-82, 87-96 are rejected under 35 U.S.C. § 103(a) as being unpatentable over Tripathi et al. (US No. 6,161,157) in view of Hong (US No. 5,764,924).

In regard to claims 44, 65-66, 74, 90, Tripathi et al. disclose a computer system comprising: a processing unit; a peripheral bridge to communicate serial bits of Peripheral Component Interconnect (PCI) bus transaction, the peripheral bridge directly coupled to the processing unit (see figure 1A); a low voltage differential signal (LVDS) channel (i.e. IEEE-1394), the LVDS channel extending from the peripheral bridge to convey the serial bits of PCI bus transaction, the serial bits of PCI bus transaction comprising PCI address and data bits (see col. 8, line 49 through col. 9, line 19); a main memory coupled to the processing unit through the peripheral bridge (see figure 1A, col. 3, lines 19-27); and a peripheral component coupled to the peripheral bridge (see figure 1A). But Tripathi et al. do not specifically disclose at least two unidirectional, differential signal pairs to convey data in opposite directions. However Hong discloses at least two unidirectional, differential signal pairs to convey data in opposite directions (see figure 2). Therefore, it would have been obvious to a person of an ordinary skill in

the art at the time the invention was made to have combined the teachings of Hong into the teachings of Tripathi et al. because each of Hong and Tripathi et al. teach the data transfer between the mobile computer and the docking station/base and further, because combining the prior art elements of Hong with Tripathi et al. according to known methods would have yielded predictable results, using the techniques of Hong would have improved Tripathi et al. in the same way, and applying the techniques of Hong to improve Tripathi et al. would have yielded predictable results (e.g. reliable serial link connection and high-speed data transfer). [See MPEP 2143].

In regard to claim 45, Tripathi et al. disclose wherein the peripheral component is coupled to the peripheral bridge through the LVDS channel (see figure 1A).

In regard to claim 46, Tripathi et al. disclose wherein the peripheral component is coupled to the processing unit through the LVDS channel and the peripheral bridge (see figure 1A, col. 3, lines 19-27).

In regard to claims 47, 75, 94, Tripathi et al. disclose wherein the peripheral component comprises a serial communication controller (see figure 1A, col. 3, lines 19-27).

In regard to claim 48, 76, 91, Tripathi et al. disclose further comprising a graphics subsystem coupled to the processing unit through the peripheral bridge (i.e. south bridge) (see figure 1A).

In regard to claim 49, Tripathi et al. disclose wherein the peripheral bridge comprises a north bridge (see figure 1A, col. 3, lines 19-27).

In regard to claim 50, Tripathi et al. disclose wherein the peripheral bridge comprises an interface controller integrated with the north bridge, the interface

controller is coupled to the processing unit without any intervening PCI bus, and the interface controller is configured to output encoded address and data bits of PCI bus transaction in serial form that are conveyed over the LVDS channel (see figure 1A, col. 4, lines 25-49).

In regard to claim 51, 79, Tripathi et al. disclose wherein the serial bits of PCI bus transaction comprise information to permit decoding to create a PCI bus transaction (see col. 4, lines 7-13).

In regard to claims 52, 55, 64, 69, 71, 80, 87, 95, Hong discloses wherein the LVDS channel comprises a first plurality of unidirectional, differential signal pairs to convey data in a first direction and a second plurality of unidirectional, differential signal pairs to convey data in a second, opposite direction (see figure 2, col. 3, lines 33-62).

In regard to claim 58, 81-82, 88, Hong and Tripathi et al. fail to teach a power supply to supply power to the computer module upon insertion into the console. However it is extremely well known in the computer art/industry to provide power from the docking station to the portable computer to prolong the battery life. Therefore OFFICIAL NOTICE is taken that it would have been obvious to a person of an ordinary skill in the art at the time the invention was made to provide password protection as is well known in the system of Hong and Tripathi et al. in order to prolong the battery life of the portable computer when docking the docking station.

In regard to claim 59, 89, Tripathi et al. disclose wherein the console comprises a coupling site and a multi-port, serial communication hub controller, and the computer module comprises a serial communication controller to

communicate, via a point-to-point link, with the multi-port, serial communication hub controller through the coupling site of the console (see col. 3, lines 19-27).

In regard to claim 60, Tripathi et al. disclose a computer system comprising: a processing unit (see figure 1A); a low voltage differential signal (LVDS) channel (see figure 1A) comprising a north bridge coupled to the processing unit, the north bridge comprising an interface controller to transmit and receive serial bits of Peripheral Component Interconnect (PCI) bus transaction over the LVDS channel; a main memory coupled to the processing unit through the north bridge; and a south bridge coupled to the processing unit through the north bridge (see figure 1A, col. 3, lines 19-27). But Tripathi et al. do not specifically disclose at least two unidirectional serial bit channels to convey data in opposite directions. However Hong discloses at least two unidirectional serial bit channels to convey data in opposite directions

In regard to claim 61, Tripathi et al. disclose wherein the south bridge is coupled to the north bridge through the LVDS channel (see figure 1A, col. 3, lines 19-27).

In regard to claim 62, 72, Tripathi et al. disclose further a peripheral component coupled to the processing unit through the south bridge, the LVDS channel, and the north bridge (see figure 1A).

In regard to claim 63, Tripathi et al. disclose wherein the north bridge is directly coupled to the processing unit (see figure 1A, col. 3, lines 19-27).

In regard to claim 67, 77, 92, Tripathi et al. disclose wherein the main memory is coupled to the processing unit through the first peripheral bridge (see figure 1A, col. 3, lines 19-27).

In regard to claim 68, Tripathi et al. disclose wherein the second peripheral bridge is coupled to the first peripheral bridge through the first LVDS channel (see figure 1A, col. 3, lines 19-27).

In regard to claims 70, 78, 93, Tripathi et al. disclose further a mass storage device coupled to the second peripheral bridge (see figure 1A).

In regard to claim 73, 96, Tripathi et al. disclose wherein the first peripheral bridge comprises an interface controller integrated with the north bridge (see figure 1A), the interface controller is configured to output an encoded serial bit stream of PCI bus transaction, and the first LVDS channel extends from the interface controller to convey the encoded serial bit stream of PCI bus transaction (see col. 4, lines 25-49).

Conclusion

10. Claims 44-96 are rejected.

11. Any inquiry concerning this communication or earlier communications from the examiner should be directed to examiner Raymond Phan, whose telephone number is (571) 272-3630. The examiner can normally be reached on Monday-Friday from 6:30AM- 4:00PM. The Group Fax No. (571) 273-8300.

Communications via Internet e-mail regarding this application, other than those under 35 U.S.C. 132 or which otherwise require a signature, may be used by the applicant and should be addressed to [raymond.phan@uspto.gov].

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Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see [hop://pair-direct.uspto.gov](http://pair-direct.uspto.gov). Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Any inquiry of a general nature or relating to the status of this application should be directed to the TC 2100 central telephone number is (571) 272-2100.

**/RAYMOND N PHAN/
Primary Examiner, Art Unit 2111**

Application/Control Number: 13/087,912
Art Unit: 2111

Page 10

Notice of References Cited	Application/Control No. 13/087,912	Applicant(s)/Patent Under Reexamination CHU, WILLIAM W.Y.	
	Examiner RAYMOND PHAN	Art Unit 2111	Page 1 of 1

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*		Document Number Country Code-Number-Kind Code	Date MM-YYYY	Name	Classification
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	D	US-			
	E	US-			
	F	US-			
	G	US-			
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INFORMATION DISCLOSURE STATEMENT BY APPLICANT (Not for submission under 37 CFR 1.99)	Application Number		13/087,912	
	Filing Date		04/15/11	
	First Named Inventor	William W.Y. Chu		
	Art Unit	2111		
	Examiner Name	PHAN		
	Attorney Docket Number	ACQI-010/19US 310578-2066		

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		Group Art Unit	2111
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Sheet 1 of 8	Attorney Docket Number	ACQI-010/19US 310578-2066	

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		First Named Inventor	William W.Y. Chu
		Group Art Unit	2111
Examiner Name	PHAN		
Sheet	2 of 8	Attorney Docket No.	ACQI-010/19US 310578-2066

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		Application Number	To be assigned 13/087,912
		Filing Date	Herewith 04/15/11
		First Named Inventor	William W.Y. Chu
		Group Art Unit	2111
Sheet	4 of 8	Examiner Name	PHAN
		Attorney Docket No.	ACQI-010/19US 310578-2066

U.S. PATENT DOCUMENTS					
Examiner Initials*	Cite No. ¹	Document Number	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear
		Number-Kind Code ² (if known)			
	105.	US-6,324,605 B1	11-27-2001	Rafferty et al.	
	106.	US-2009/0157939	06/18/2009	Chu	
	107.	US-5,978,919	11-1999	Doi et al.	
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		Country Code ³ Number ⁴ Kind Code ⁵ (if known)			
	1.	WO 92/18924	10-29-1992		
	2.	WO 94/00097	01-06-1994		
	3.	WO 95/13640	05-18-1995		
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Examiner Signature	/Raymond Phan/	Date Considered	08/16/2011

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	Filing Date	04/15/11
	First Named Inventor	William W. Y. Chu
	Art Unit	2111
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	Attorney Docket Number	ACQI-010/19US 310578-2066

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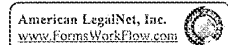
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HN-933500

Substitute for form 1449A/PTO		Complete if Known	
INFORMATION DISCLOSURE STATEMENT BY APPLICANT <i>(Use as many sheets as necessary)</i>		Application Number	To be assigned 13/087,912
		Filing Date	Herewith 04/15/11
		First Named Inventor	William W.Y. Chu
		Art Unit	2111
		Examiner Name	PHAN
Sheet 2 of 26	Attorney Docket Number	ACQI-010/19US 310578-2066	

U. S. PATENT DOCUMENTS					
Examiner Initials*	Cite No. ¹	Document Number	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear
		Number-Kind Code ² (if known)			
	AM001	6,088,620	07-11-2000	Ninomiya et al.	
	AO014	6,104,921	08-15-2000	Cosley et al.	
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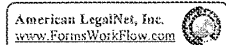
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Examiner Initials*	Cite No. ¹	Foreign Patent Document	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear	T ⁶
		Country Code ³ "Number" ⁴ "Kind Code" ⁵ (if known)				
	B004	JP 6-289953	10-18-1994	Hitachi, Ltd.		
	BN001	WO 97/00481	01-03-1997	Intel Corporation		

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		Examiner Name	PHAN
		Attorney Docket Number	ACQI-010/19US 310578-2066
Sheet	3	of	26

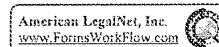
NON PATENT LITERATURE DOCUMENTS			
Examiner Initials*	Cite No. ¹	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.	T ²
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		First Named Inventor	William W.Y. Chu
		Art Unit	2111
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Sheet 4	of 26	Attorney Docket Number	ACQI-010/19US 310578-2066

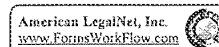
NON PATENT LITERATURE DOCUMENTS			
Examiner Initials*	Cite No. ¹	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.	T ²
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Complete if Known**INFORMATION DISCLOSURE
STATEMENT BY APPLICANT**

(Use as many sheets as necessary)

Sheet 5

of 26

Application Number	To be assigned 13/087,912
Filing Date	Herewith 04/15/11
First Named Inventor	William W.Y. Chu
Art Unit	2111
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NON PATENT LITERATURE DOCUMENTS

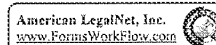
Examiner Initials*	Cite No. ¹	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.	T ²
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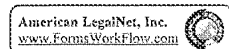
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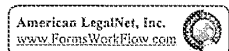
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	C078	PHILLIPS, J., "9800 Processor Card Design Specification," February 25, 1998, White Cross Systems Limited, pages 1-41.	
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		Application Number	To be assigned 13/087,912
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		First Named Inventor	William W.Y. Chu
		Art Unit	2111
		Examiner Name	PHAN
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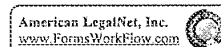
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	C080	MIASKOWSKI, S. (Editor), "A Whale of a System," BYTE, August 1991, 4 pages, Vol. 16, No. 8.	
	C081	Advanced Micro Devices, Inc., "AMD-K6-III Processor Data Sheet," 21918B/0, October 1999, 326 pages.	
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	C111	Sun Microsystems, Inc., "UltraSPARC™ -II CPU Module, Datasheet 400 MHz CPU, 2.0 MP E-Cache," July 1999, 28 pages.	

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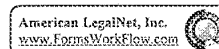
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	C113	Compaq Computer Corporation, et al., "Universal Serial Bus Specification," September 23, 1998, Revision 1.1, 327 pages.	
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	C116	Origin and Onyx Theory of Operations Manual, Document Number 007-3439-002, 1997, Silicon Graphics, Inc., 124 pages.	
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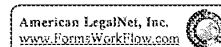
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	C124	ANDERSON, C.R. et al., "IEEE 1355 HS-Links: Present Status and Future Prospects," [online], 1998, [retrieved on 08-11-2010], Retrieved from the Internet: <URL: http://www94.web.cern.ch/HIS/dshs/publications/wotug21/hmlink/pdf/hmlinkpaper.pdf >, 14 pages.	
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	C126	HAAS, S., "The IEEE 1355 Standard: Developments, Performance and Application in High Energy Physics," Thesis for degree of Doctor of Philosophy, University of Liverpool, December 1998, 138 pages.	
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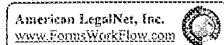
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	CB041	GALITZINE, G., "Industrial Computers," April 1999, Internet Telephony Roundup [online], [retrieved on June 23, 2004]. Retrieved from the Internet at <URL: http://www.tmcnet.com/articles/itmag/0499/0499roundup.htm >, 5 pages.	
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Intel Corp. v. ACQIS LLC
IPR2021-01103
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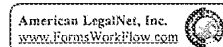
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	CB051	CUBIX Customer Service Support System, "Click on the Front Panel That Matches Your System," ©2000, Cubix [online], [retrieved on June 22, 2004]. Retrieved from the Internet at <URL: http://64.173.211.7/support/techinfo/density/density.htm>, 1 page.	
	CC001	MPL Brochure, "The First Rugged All-in-One Industrial 486FDX-133 MHz PC," IMP486/IPM5 User Manual, 1998, 15 pages.	
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**INFORMATION DISCLOSURE
STATEMENT BY APPLICANT**

(Use as many sheets as necessary)

Complete if Known

Application Number	To be assigned 13/087,912
Filing Date	Herewith 04/15/11
First Named Inventor	William W.Y. Chu
Art Unit	2111
Examiner Name	PHAN
Attorney Docket Number	ACQI-010/19US 310578-2066

Sheet 13

of 26

NON PATENT LITERATURE DOCUMENTS

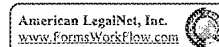
Examiner Initials*	Cite No. ¹	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.	T ²
	CN002	BERST, J., "Hope For The Modular PCs We All Really Want," December 5, 1997, Jesse Berst's Anchor Desk [online], [retrieved on July 10, 1998]. Retrieved from the Internet at: <URL: http://www.zdnet.com/anchordesk/story/story_1504.html >, 3 pages.	
	CN003	BOYD-MERRITT, R., "Upgradable-PC Effort Takes Divergent Paths," EE Times - Headline News [online], [retrieved on July 31, 1998]. Retrieved from the Internet at: <URL: http://techweb.cmp.com/eet/news/97/949news/effort.html >, 3 pages.	
	CN004	FAEGRE, D. S. et al., "CTOS Revealed - Unisys' Best-Kept Secret Is An Operating System Built For Distributed Business Applications," December 1994, Core Technologies, BYTE [online], [retrieved on July 10, 1998]. Retrieved from the Internet at: <URL: http://www.byte.com/art/9412/sec13/art2.htm >, 6 pages.	
	CN005	SPANG, K., "Component House: Design Technology for 'PCs in a Snap' - NeoSystems Offers Building Blocks," Computer Reseller News, April 21, 1997, Issue: 732, Section: Channel Assembly, TechWeb [online], [retrieved on July 31, 1998]. Retrieved from the Internet at: <URL: http://www.techweb.com/se/directlink.cgi?CRN19970421S0054 >, 2 pages.	
	CN006	"Think Modular," June 10, 1997, PC Magazine [online], [retrieved on July 31, 1998]. Retrieved from the Internet at: <URL: http://www.homezdnet.com/pcmag/issues/1611/pcmg0072.htm >, 1 page.	
	DA001	Office Action for U.S. Patent No. 6,718,415, mailed October 10, 2002, 7 pages.	
	DA002	Response for U.S. Patent No. 6,718,415, filed November 7, 2002, 9 pages.	
	DA003	Office Action for U.S. Patent No. 6,718,415, mailed January 29, 2003, 7 pages.	
	DA004	Response for U.S. Patent No. 6,718,415, filed March 6, 2003, 8 pages.	
	DA005	Office Action for U.S. Patent No. 6,718,415, mailed June 4, 2003, 8 pages.	
	DA006	Response for U.S. Patent No. 6,718,415, filed September 4, 2003, 10 pages.	
	DB001	Amendment Submitted With RCE for U.S. Patent No. 7,099,981, filed March 1, 2006, 23 pages.	
	DC001	Office Action for U.S. Patent No. 7,363,415, mailed on April 12, 2007, 23 pages.	
	DC002	Response for U.S. Patent No. 7,363,415, filed on April 24, 2007, 25 pages.	
	DD001	Office Action for U.S. Patent No. 7,328,297, mailed February 8, 2007, 5 pages.	
	DD002	Response for U.S. Patent No. 7,328,297, filed April 19, 2007, 32 pages.	
	DD003	Office Action for U.S. Patent No. 7,328,297, mailed July 12, 2007, 13 pages.	
	DD004	Response for U.S. Patent No. 7,328,297, filed July 23, 2007, 20 pages.	

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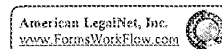
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	EE006	Patent Owner's Response to Office Action in Inter Partes Reexamination of US Patent No. 7,328,297, Control No. 95/001,336, filed October 4, 2010, 49 pages.	
	EE007	Patent Owner's Response to Office Action in Inter Partes Reexamination of US Patent No. 7,328,297, Control No. 95/001,336, Exhibit A, Declaration of William Henry Mangione-Smith under 37 C.F.R. 1.132, filed October 4, 2010, 61 pages.	
	EF001	Request for Inter Partes Reexamination of US Patent No. 7,363,415, Control No. 95/001,424, filed August 25, 2010, 34 pages.	
	EF002	Request for Inter Partes Reexamination of US Patent No. 7,363,415, Control No. 95/001,424, Exhibit AA, Claim Charts with respect to Gallagher and Other References for Obviousness, filed August 25, 2010, 114 pages.	
	EF003	Request for Inter Partes Reexamination of US Patent No. 7,363,415, Control No. 95/001,424, Exhibit AB, Claim Charts with respect to Gallagher and Other References for Obviousness, filed August 25, 2010, 92 pages.	
	EF004	Request for Inter Partes Reexamination of US Patent No. 7,363,415, Control No. 95/001,424, Exhibit BA, Claim Charts with respect to QuantumNet and Other References for Obviousness, filed August 25, 2010, 121 pages.	
	EF005	Request for Inter Partes Reexamination of US Patent No. 7,363,415, Control No. 95/001,424, Exhibit BB, Claim Charts with respect to QuantumNet and Other References for Obviousness, filed August 25, 2010, 99 pages.	
	EF006	Request for Inter Partes Reexamination of US Patent No. 7,363,415, Control No. 95/001,424, Exhibit CA, Claim Charts with respect to Chatcom and Other References for Obviousness, filed August 25, 2010, 91 pages.	
	EF007	Request for Inter Partes Reexamination of US Patent No. 7,363,415, Control No. 95/001,424, Exhibit CB, Claim Charts with respect to Chatcom and Other References for Obviousness, filed August 25, 2010, 94 pages.	
	EF008	Office Action in Inter Partes Reexamination of US Patent No. 7,363,415, Control No. 95/001,424, mailed November 1, 2010, 75 pages.	
	EG001	Request for Inter Partes Reexamination of US Patent No. 7,376,779, Control No. 95/001,475, filed October 27, 2010, 35 pages.	
	EG002	Request for Inter Partes Reexamination of US Patent No. 7,376,779, Control No. 95/001,475, Exhibit AA, Claim Charts with respect to Gallagher and Other References for Obviousness, filed October 27, 2010, 128 pages.	

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Sheet 21	of 26	Attorney Docket Number	ACQI-010/19US 310578-2066

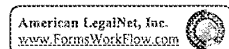
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	EG003	Request for Inter Partes Reexamination of US Patent No. 7,376,779, Control No. 95/001,475, Exhibit AB, Claim Charts with respect to Gallagher and Other References for Obviousness, filed October 27, 2010, 153 pages.	
	EG004	Request for Inter Partes Reexamination of US Patent No. 7,376,779, Control No. 95/001,475, Exhibit BA, Claim Charts with respect to QuantumNet and Other References for Obviousness, filed October 27, 2010, 108 pages.	
	EG005	Request for Inter Partes Reexamination of US Patent No. 7,376,779, Control No. 95/001,475, Exhibit BB, Claim Charts with respect to QuantumNet and Other References for Obviousness, filed October 27, 2010, 112 pages.	
	EG006	Request for Inter Partes Reexamination of US Patent No. 7,376,779, Control No. 95/001,475, Exhibit CA, Claim Charts with respect to Chatcom and Other References for Obviousness, filed October 27, 2010, 112 pages.	
	EG007	Request for Inter Partes Reexamination of US Patent No. 7,376,779, Control No. 95/001,475, Exhibit CB, Claim Charts with respect to Chatcom and Other References for Obviousness, filed October 27, 2010, 118 pages.	
	EG008	Office Action in Inter Partes Reexamination of US Patent No. 7,376,779, Control No. 95/001,475, mailed December 20, 2010, 105 pages.	
	EH001	Request for Inter Partes Reexamination of US Patent No. 7,363,416, Control No. 95/001,476, filed October 27, 2010, 37 pages.	
	EH002	Request for Inter Partes Reexamination of US Patent No. 7,363,416, Control No. 95/001,476, Exhibit AA, Claim Charts with respect to Gallagher and Other References for Obviousness, filed October 27, 2010, 70 pages.	
	EH003	Request for Inter Partes Reexamination of US Patent No. 7,363,416, Control No. 95/001,476, Exhibit AB, Claim Charts with respect to Gallagher and Other References for Obviousness, filed October 27, 2010, 64 pages.	
	EH004	Request for Inter Partes Reexamination of US Patent No. 7,363,416, Control No. 95/001,476, Exhibit BA, Claim Charts with respect to QuantumNet and Other References for Obviousness, filed October 27, 2010, 64 pages.	
	EH005	Request for Inter Partes Reexamination of US Patent No. 7,363,416, Control No. 95/001,476, Exhibit BB, Claim Charts with respect to QuantumNet and Other References for Obviousness, filed October 27, 2010, 71 pages.	

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Sheet 22	of 26		

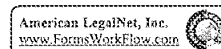
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	EH007	Request for Inter Partes Reexamination of US Patent No. 7,363,416, Control No. 95/001,476, Exhibit CB, Claim Charts with respect to Chatcom and Other References for Obviousness, filed October 27, 2010, 67 pages.	
	EH008	Office Action in Inter Partes Reexamination of US Patent No. 7,363,416, Control No. 95/001,476, mailed December 6, 2010, 63 pages.	
	IC01	"Defendants' Amended Invalidity Contentions," submitted by the Defendants in the U.S. District Court for the Eastern District of Texas, Case No. 6:09-cv-148-LED on March 1, 2010, 18 pages.	
	IC02	"Exhibit A (Asserted Claims)," submitted by the Defendants in the U.S. District Court for the Eastern District of Texas, Case No. 6:09-cv-148-LED on March 1, 2010, 2 pages.	
	IC03	"Exhibit B - Table 1," submitted by the Defendants in the U.S. District Court for the Eastern District of Texas, Case No. 6:09-cv-148-LED on March 1, 2010, 75 pages.	
	IC04	"Exhibit C," submitted by the Defendants in the U.S. District Court for the Eastern District of Texas, Case No. 6:09-cv-148-LED on March 1, 2010, 2 pages.	
	IC05	"Exhibit D," submitted by the Defendants in the U.S. District Court for the Eastern District of Texas, Case No. 6:09-cv-148-LED on March 1, 2010, 106 pages.	
	IC06	"Exhibit E," submitted by the Defendants in the U.S. District Court for the Eastern District of Texas, Case No. 6:09-cv-148-LED on March 1, 2010, 2 pages.	
	IC07	"Invalidity Chart for Base Reference IBM 8260," submitted by the Defendants in the U.S. District Court for the Eastern District of Texas, Case No. 6:09-cv-148-LED on March 1, 2010, 53 pages.	
	IC08	"Invalidity Chart for Base Reference IBM 8265," submitted by the Defendants in the U.S. District Court for the Eastern District of Texas, Case No. 6:09-cv-148-LED on March 1, 2010, 56 pages.	
	IC09	"Invalidity Chart for Base Reference U.S. Patent No. 4,453,215 (Reid)," submitted by the Defendants in the U.S. District Court for the Eastern District of Texas, Case No. 6:09-cv-148-LED on March 1, 2010, 56 pages.	

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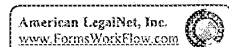
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	IC10	"Invalidity Chart for Base Reference Origin2000," submitted by the Defendants in the U.S. District Court for the Eastern District of Texas, Case No. 6:09-cv-148-LED on March 1, 2010, 56 pages.	
	IC11	"Invalidity Chart for Base Reference QuantumNet," submitted by the Defendants in the U.S. District Court for the Eastern District of Texas, Case No. 6:09-cv-148-LED on March 1, 2010, 49 pages.	
	IC12	"Invalidity Chart for Base Reference U.S. Patent No. 6,564,274 (Heath)," submitted by the Defendants in the U.S. District Court for the Eastern District of Texas, Case No. 6:09-cv-148-LED on March 1, 2010, 57 pages.	
	IC13	"Invalidity Chart for Base Reference U.S. Patent No. 5,577,205," submitted by the Defendants in the U.S. District Court for the Eastern District of Texas, Case No. 6:09-cv-148-LED on March 1, 2010, 60 pages.	
	IC14	"Invalidity Chart for Base Reference U.S. Patent No. 5,802,391," submitted by the Defendants in the U.S. District Court for the Eastern District of Texas, Case No. 6:09-cv-148-LED on March 1, 2010, 61 pages.	
	IC15	"Invalidity Chart for Base Reference U.S. Patent No. 6,715,100," submitted by the Defendants in the U.S. District Court for the Eastern District of Texas, Case No. 6:09-cv-148-LED on March 1, 2010, 64 pages.	
	IC16	"Invalidity Chart for Base Reference Cubix BC/Density," submitted by the Defendants in the U.S. District Court for the Eastern District of Texas, Case No. 6:09-cv-148-LED on March 1, 2010, 64 pages.	
	IC17	"Invalidity Chart for Base Reference JP6-289956," submitted by the Defendants in the U.S. District Court for the Eastern District of Texas, Case No. 6:09-cv-148-LED on March 1, 2010, 62 pages.	
	IC18	"Invalidity Chart for Base Reference Gallagher 068 and Gallagher 503," submitted by the Defendants in the U.S. District Court for the Eastern District of Texas, Case No. 6:09-cv-148-LED on March 1, 2010, 108 pages.	
	IC19	"Invalidity Chart for Base Reference Compaq ProLiant Cluster," submitted by the Defendants in the U.S. District Court for the Eastern District of Texas, Case No. 6:09-cv-148-LED on March 1, 2010, 81 pages.	

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First Named Inventor	William W.Y. Chu
Art Unit	2111
Examiner Name	PHAN
Attorney Docket Number	ACQI-010/19US 310578-2066

NON PATENT LITERATURE DOCUMENTS

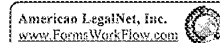
Examiner Initials*	Cite No. ¹	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.	T ²
	IC20	"Invalidity Chart for Base Reference U.S. Patent No. 5,325,517 to Baker et al. (Appendix 1, Exhibit 15)," submitted by the Defendants in the U.S. District Court for the Eastern District of Texas, Case No. 6:09-cv-148-LED on March 1, 2010, 59 pages.	
	IC21	"Invalidity Chart for Japanese Patent Application H7-64672 (Toshiba '672)," submitted by the Defendants in the U.S. District Court for the Eastern District of Texas, Case No. 6:09-cv-148-LED on March 1, 2010, 55 pages.	
	IC22	"Invalidity Chart for Base Reference ChatCom," submitted by the Defendants in the U.S. District Court for the Eastern District of Texas, Case No. 6:09-cv-148-LED on March 1, 2010, 52 pages.	
	IC23	"Invalidity Chart for Base Reference Ziatech Corp. Ketris 9000 System," submitted by the Defendants in the U.S. District Court for the Eastern District of Texas, Case No. 6:09-cv-148-LED on March 1, 2010, 68 pages.	
	IC24	"Invalidity Chart for Base Reference Ziatech STD 32 Star System," submitted by the Defendants in the U.S. District Court for the Eastern District of Texas, Case No. 6:09-cv-148-LED on March 1, 2010, 62 pages.	
	IC25	"Invalidity Chart for Base Reference U.S. Patent No. 7,339,786 (Bottom et al.)," submitted by the Defendants in the U.S. District Court for the Eastern District of Texas, Case No. 6:09-cv-148-LED on March 1, 2010, 57 pages.	
	IC26	"Invalidity Chart for Base References RLX Patents, U.S. Patent Nos. 6,747,878, 6,411,506, 6,325,636, 6,757,748, and 6,985,967 (Hipp et al.)," submitted by the Defendants in the U.S. District Court for the Eastern District of Texas, Case No. 6:09-cv-148-LED on March 1, 2010, 58 pages.	
	IC27	"Invalidity Chart for Base Reference Network Engines P6000 Server," submitted by the Defendants in the U.S. District Court for the Eastern District of Texas, Case No. 6:09-cv-148-LED on March 1, 2010, 59 pages.	
	IC28	"Invalidity Chart for Base Reference Eversys 8000 System," submitted by the Defendants in the U.S. District Court for the Eastern District of Texas, Case No. 6:09-cv-148-LED on March 1, 2010, 60 pages.	
	IC29	"Invalidity Chart for Base Reference Eversys CAPserver," submitted by the Defendants in the U.S. District Court for the Eastern District of Texas, Case No. 6:09-cv-148-LED on March 1, 2010, 59 pages.	

Examiner Signature	/Raymond Phan/	Date Considered	08/16/2011

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Intel Corp. v. ACQIS LLC
IPR2021-01103
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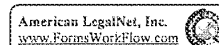
Substitute for form 1448A/PTO		Complete if Known	
INFORMATION DISCLOSURE STATEMENT BY APPLICANT (Use as many sheets as necessary)		Application Number	To be assigned 13/087,912
		Filing Date	Herewith 04/15/11
		First Named Inventor	William W.Y. Chu
		Art Unit	2111
		Examiner Name	PHAN
		Attorney Docket Number	ACQI-010/19US 310578-2066
Sheet 25	of 26		

NON PATENT LITERATURE DOCUMENTS			
Examiner Initials*	Cite No. ¹	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.	T ²
	IC30	"Invalidity Chart for Base Reference U.S. 5,809,262," submitted by the Defendants in the U.S. District Court for the Eastern District of Texas, Case No. 6:09-cv-148-LED on March 1, 2010, 62 pages.	
	IC31	"Invalidity Chart for Base Reference WhiteCross 9800 System," submitted by the Defendants in the U.S. District Court for the Eastern District of Texas, Case No. 6:09-cv-148-LED on March 1, 2010, 62 pages.	
	IC32	"Invalidity Chart for Base Reference U.S. 5,339,408," submitted by the Defendants in the U.S. District Court for the Eastern District of Texas, Case No. 6:09-cv-148-LED on March 1, 2010, 61 pages.	
	IC33	"Invalidity Chart for Base Reference Tyuluman 536," submitted by the Defendants in the U.S. District Court for the Eastern District of Texas, Case No. 6:09-cv-148-LED on March 1, 2010, 76 pages.	
	IC34	"Invalidity Chart for Base Reference Hong 737," submitted by the Defendants in the U.S. District Court for the Eastern District of Texas, Case No. 6:09-cv-148-LED on March 1, 2010, 77 pages.	
	IC35	"Invalidity Chart for Base Reference U.S. 5,436,857 (Nelson)," submitted by the Defendants in the U.S. District Court for the Eastern District of Texas, Case No. 6:09-cv-148-LED on March 1, 2010, 6 pages.	
	IC36	"Invalidity Chart for Base Reference U.S. 5,999,952 (Jenkins)," submitted by the Defendants in the U.S. District Court for the Eastern District of Texas, Case No. 6:09-cv-148-LED on March 1, 2010, 6 pages.	
	IC37	"Invalidity Chart for Base Reference U.S. 5,608,608 (Flint)," submitted by the Defendants in the U.S. District Court for the Eastern District of Texas, Case No. 6:09-cv-148-LED on March 1, 2010, 6 pages.	
	IC38	"Invalidity Chart for Base Reference U.S. 5,978,821 (Freney)," submitted by the Defendants in the U.S. District Court for the Eastern District of Texas, Case No. 6:09-cv-148-LED on March 1, 2010, 6 pages.	
	IC39	"Invalidity Chart for Base Reference WO 92/18924 (Wallsten)," submitted by the Defendants in the U.S. District Court for the Eastern District of Texas, Case No. 6:09-cv-148-LED on March 1, 2010, 6 pages.	

Examiner Signature	/Raymond Phan/	Date Considered	08/16/2011

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Substitute for form 1449A/PTO		Complete if Known	
INFORMATION DISCLOSURE STATEMENT BY APPLICANT <i>(Use as many sheets as necessary)</i>		Application Number	To be assigned 13/087,912
		Filing Date	Herewith 04/15/11
		First Named Inventor	William W.Y. Chu
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		Examiner Name	PHAN
Sheet 26 of 26	Attorney Docket Number	ACQI-010/19US 310578-2066	

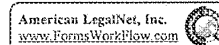
NON PATENT LITERATURE DOCUMENTS			
Examiner Initials*	Cite No. ¹	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.	T ²
	IC40	"Invalidity Chart for Base Reference Ergo Moby Brick", submitted by the Defendants in the U.S. District Court for the Eastern District of Texas, Case No. 6:09-cv-148-LED on March 1, 2010, 5 pages.	
	IC41	"Invalidity Chart for Base Reference U.S. Patent No. 5,463,742 (Kobayashi)", submitted by the Defendants in the U.S. District Court for the Eastern District of Texas, Case No. 6:09-cv-148-LED on March 1, 2010, 5 pages.	
	IC42	"Invalidity Chart for Base Reference Japanese Patent Application Publication H6-289953 (Hitachi)", submitted by the Defendants in the U.S. District Court for the Eastern District of Texas, Case No. 6:09-cv-148-LED on March 1, 2010, 5 pages.	
	IC43	"Invalidity Chart for Base Reference Japanese Patent Application Publication H7-84675 (Hitachi)", submitted by the Defendants in the U.S. District Court for the Eastern District of Texas, Case No. 6:09-cv-148-LED on March 1, 2010, 5 pages.	
	IC44	"Invalidity Chart for Base Reference U.S. Patent No. 5,187,645 (Spalding)", submitted by the Defendants in the U.S. District Court for the Eastern District of Texas, Case No. 6:09-cv-148-LED on March 1, 2010, 6 pages.	
	IC45	"Defendants' Notice of Errata Relating to Defendants' P.R. 3-3 Invalidity Contentions," submitted by the Defendants in the U.S. District Court for the Eastern District of Texas, Case No. 6:09-cv-148-LED on March 1, 2010, 14 pages.	
	IF01	"Exhibit 5 - Disclosure of Asserted Claims and Infringement Contentions", submitted by the Plaintiff in the U.S. District Court for the Eastern District of Texas, Case No. 6:09-cv-148-LED, 14 pages.	
	F01	"Memorandum Opinion and Order Construing Claim Terms and Denying Defendants' Motion for Partial Summary Judgment," Issued by the U.S. District Court for the Eastern District of Texas, Case No. 6:09-cv-148-LED on August 2, 2010, 18 pages.	
	H01	"Transcript of Videotaped Deposition of William Mangione-Smith," taken by the Defendants in connection with Case No. 6:09-cv-148-LED in the U.S. District Court for the Eastern District of Texas, September 9, 2010, 192 pages.	

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HN-933500

Search Notes 	Application/Control No. 13087912	Applicant(s)/Patent Under Reexamination CHU, WILLIAM W.Y.
	Examiner RAYMOND PHAN	Art Unit 2111

SEARCHED			
Class	Subclass	Date	Examiner
710	104-119,62-64,72-73,8-19,300-317	9/5/11	RP

SEARCH NOTES		
Search Notes	Date	Examiner
PALM SEARCH FOR DOUBLE PATENTING	9/1/11	RP

INTERFERENCE SEARCH			
Class	Subclass	Date	Examiner

	/RAYMOND PHAN/ Primary Examiner.Art Unit 2111

Substitute for form 1449A/PTO

**INFORMATION DISCLOSURE
STATEMENT BY APPLICANT**

(Use as many sheets as necessary)

Complete if Known

Application Number	To be assigned 13/087,912
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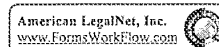
Examiner Initials*	Cite No. ¹	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.	T ²
	DF001	Office Action for U.S. Patent No. 7,363,416, mailed April 12, 2007, 23 pages.	
	DF002	Response for U.S. Patent No. 7,363,416, filed April 24, 2007, 23 pages.	
	DG001	Office Action for U.S. Patent No. 7,376,779, mailed September 28, 2007, 24 pages.	
	DG002	Response for U.S. Patent No. 7,376,779, filed October 16, 2007, 23 pages.	
	DH001	Office Action for U.S. Patent No. 7,676,624, mailed December 1, 2008, 8 pages.	
	DH002	Response for U.S. Patent No. 7,676,624, filed January 13, 2009, 14 pages.	
	DH003	Supplemental Response for U.S. Patent No. 7,676,624, filed on February 6, 2009, 13 pages.	
	DI001	Office Action for U.S. Patent No. 7,818,487, mailed September 29, 2009, 10 pages.	
	DI002	Response for U.S. Patent No. 7,818,487, filed November 6, 2009, 3 pages.	
	DI003	Amendment for U.S. Patent No. 7,818,487, filed May 11, 2010, 15 pages.	
	DI004	Amendment Submitted After Notice of Allowance for U.S. Patent No. 7,818,487, filed August 17, 2010, 14 pages.	
	DJ001	Office Action for U.S. Publication No. 2010/0174844, mailed October 28, 2010, 11 pages.	
	DK001	Office Action for U.S. Patent No. 6,216,185, mailed April 12, 2000, 9 pages.	
	DK002	Response for U.S. Patent No. 6,216,185, filed August 3, 2000, 15 pages.	
	DK003	Office Action for U.S. Patent No. 6,216,185, mailed August 25, 2000, 9 pages.	
	DK004	Response for U.S. Patent No. 6,216,185, filed October 24, 2000, 10 pages.	
	DL001	Office Action for U.S. Patent No. 6,345,330, mailed June 15, 2000, 7 pages.	
	DL002	Amendment for U.S. Patent No. 6,345,330, filed September 12, 2000, 5 pages.	
	DL003	Restriction Requirement for U.S. Patent No. 6,345,330, mailed December 19, 2000, 5 pages.	
	DL004	Amendment filed with Continued Prosecution Application for U.S. Patent No. 6,345,330, filed January 17, 2001, 5 pages.	
	DL005	Office Action for U.S. Patent No. 6,345,330, mailed March 23, 2001, 6 pages.	
	DL006	Response to Office Action for U.S. Patent No. 6,345,330, filed July 19, 2001, 5 pages.	
	DM001	Office Action for U.S. Patent Application No. 09/642,628, mailed April 5, 2001, 9 pages.	
	DO001	Office Action for U.S. Application No. 10/963,825, mailed October 27, 2005, 25 pages.	
	DO002	Response for U.S. Application No. 10/963,825, filed January 9, 2006, 22 pages.	
	DO003	Office Action for U.S. Application No. 10/963,825, mailed May 31, 2006, 29 pages.	
	DO004	Amendment Submitted with RCE for U.S. Application No. 10/963,825, filed July 27, 2006, 29 pages.	
	DO005	Office Action for U.S. Application No. 10/963,825, mailed October 20, 2006, 28 pages.	

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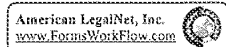
Examiner Initials*	Cite No. ¹	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.	T ²
	DO006	Appellants' Brief for U.S. Application No. 10/963,825, filed January 8, 2007, 31 pages.	
	DO007	Revised Appellants' Brief for U.S. Application No. 10/963,825, filed April 20, 2007, 34 pages.	
	DO008	Examiner's Answer for U.S. Application No. 10/963,825, mailed August 8, 2007, 30 pages.	
	DO009	Reply Brief for U.S. Application No. 10/963,825, filed September 4, 2007, 4 pages.	
	DO010	Decision on Appeal for U.S. Application No. 10/963,825, mailed February 4, 2009, 13 pages.	
	DO011	Amendment Submitted with RCE for U.S. Application No. 10/963,825, filed February 20, 2009, 24 pages.	
	DO012	Office Action for U.S. Application No. 10/963,825, mailed May 14, 2009, 5 pages.	
	DO013	Response for U.S. Application No. 10/963,825, filed May 22, 2009, 2 pages.	
	DO014	Office Action for U.S. Application No. 10/963,825, mailed September 15, 2009, 14 pages.	
	DO015	Response for U.S. Application No. 10/963,825, filed October 1, 2009, 7 pages.	
	DP001	Office Action for RE 41,294, mailed November 16, 2007, 10 pages.	
	DP002	Response for RE 41,294, filed December 20, 2007, 21 pages.	
	DP003	Office Action for RE 41,294, mailed April 15, 2008, 10 pages.	
	DP004	Amendment Submitted with RCE for RE 41,294, filed May 27, 2008, 14 pages.	
	DP005	Supplemental Amendment Submitted with RCE for RE 41,294, filed July 8, 2008, 12 pages.	
	DP006	Office Action for RE 41,294, mailed September 16, 2008, 11 pages.	
	DP007	Response for RE 41,294, filed October 30, 2008, 14 pages.	
	DP008	Supplemental Response for RE 41,294, filed February 20, 2009, 13 pages.	
	DP009	Supplemental Response for RE 41,294, filed August 17, 2009, 3 pages.	
	DP010	Examiner Interview Summary Record, mailed January 15, 2009, 1 page.	
	DQ001	Office Action for RE 41,076, mailed July 13, 2007, 38 pages.	
	DQ002	Response for RE 41,076, filed September 26, 2007, 18 pages.	
	DQ003	Office Action for RE 41,076, mailed October 17, 2007, 55 pages.	
	DQ004	Amendment Submitted with RCE for RE 41,076, filed November 5, 2007, 19 pages.	
	DQ005	Office Action for RE 41,076, mailed February 11, 2008, 62 pages.	
	DQ006	Response for RE 41,076, filed April 7, 2008, 18 pages.	
	DQ007	Office Action for RE 41,076, mailed June 9, 2008, 25 pages.	
	DQ008	Amendment Submitted with RCE for RE 41,076, filed December 8, 2008, 44 pages.	
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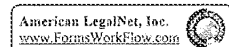
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	DQ013	Applicant Summary of Interview, filed March 24, 2009, 1 page.	
	DQ014	Examiner Interview Summary Record, mailed September 22, 2009, 5 pages.	
	DR001	Office Action for U.S. Application No. 12/322,858, mailed March 4, 2010, 24 pages.	
	DR002	Response for U.S. Application No. 12/322,858, filed June 4, 2010, 15 pages.	
	DR003	Office Action for U.S. Application No. 12/322,858, mailed June 25, 2010, 22 pages.	
	DR004	Response for U.S. Application No. 12/322,858, filed October 25, 2010, 12 pages.	
	DS001	Office Action for U.S. Application No. 12/577,074, mailed April 13, 2010, 7 pages.	
	DS002	Response for U.S. Application No. 12/577,074, filed July 13, 2010, 3 pages.	
	DS003	Office Action for U.S. Application No. 12/577,074, mailed November 10, 2010, 6 pages.	
	DT001	Office Action for U.S. Application No. 09/312,199, mailed March 26, 2003, 5 pages.	
	DT002	Response for U.S. Application No. 09/312,199, filed June 11, 2003, 5 pages.	
	DU001	Office Action for RE 41,092, mailed September 17, 2008, 8 pages.	
	DU002	Response for RE 41,092, filed October 27, 2008, 27 pages.	
	DU003	Examiner's Amendment for RE 41,092, mailed November 4, 2009, 4 pages.	
	DV001	Office Action for U.S. Application No. 11/545,056, mailed March 12, 2010, 26 pages.	
	DV002	Response for U.S. Application No. 11/545,056, filed June 14, 2010, 18 pages.	
	DW001	Office Action for U.S. Application No. 12/561,138, mailed September 29, 2010, 4 pages.	
	EA001	Request for Ex Parte Reexamination of US Patent No. 6,216,185, Control No. 90/010,816, filed January 8, 2010, 39 pages.	
	EA002	Request for Ex Parte Reexamination of US Patent No. 6,216,185, Control No. 90/010,816, filed January 8, 2010, Exhibit AA to Request Claim Charts with respect to the Hitachi '953 for Anticipation and Obviousness, 136 pages	
	EA003	Request for Ex Parte Reexamination of US Patent No. 6,216,185, Control No. 90/010,816, filed January 8, 2010, Exhibit BB Claim Charts with respect to Kobayashi for Anticipation and Obviousness, 128 pages	
	EA004	Request for Ex Parte Reexamination of US Patent No. 6,216,185, Control No. 90/010,816, filed January 8, 2010, Exhibit CC Claim Charts with respect to Byte for Anticipation and Obviousness, 122 pages	

Examiner Signature	/Raymond Phan/	Date Considered	08/16/2011

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HN-933500

ALL REFERENCES CONSIDERED EXCEPT WHERE LINED THROUGH. /R.P./

PTO/SB/08a (07-09)

Approved for use through 07/31/2012. OMB 0651-0031

U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE

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Substitute for form 1449A/PTO INFORMATION DISCLOSURE STATEMENT BY APPLICANT (Use as many sheets as necessary)		Complete if Known	
		Application Number	To be assigned 13/087,912
		Filing Date	Herewith 04/15/11
		First Named Inventor	William W.Y. Chu
		Art Unit	2111
		Examiner Name	PHAN
Sheet 17 of 26	Attorney Docket Number	ACQI-010/19US 310578-2066	

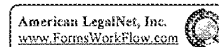
NON PATENT LITERATURE DOCUMENTS			
Examiner Initials*	Cite No. ¹	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.	T ²
	EA005	Request for Ex Parte Reexamination of US Patent No. 6,216,185, Control No. 90/010,816, filed January 8, 2010, Exhibit DD Claim Charts with respect to the Hitachi '675 for Anticipation and Obviousness, 119 pages	
	EA006	Office Action in Ex Parte Reexamination of US Patent No. 6,216,185, Control No. 90/010,816, mailed July 27, 2010, 103 pages	
	EA007	Patent Owner's Response to Office Action in Ex Parte Reexamination of US Patent No. 6,216,185, Control No. 90/010,816, filed September 27, 2010, 55 pages	
	EB001	Request for Inter Partes Reexamination of US Patent No. 6,718,415, Control No. 95/001,276, filed December 2, 2009, 44 pages.	
	EB002	Request for Inter Partes Reexamination of US Patent No. 6,718,415, Control No. 95/001,276, filed December 2, 2009, Exhibit O, Declaration Under 37 CFR 1.132 of Vincent P. Conroy, 11-24-2009, 3 pages.	
	EB003	Request for Inter Partes Reexamination of US Patent No. 6,718,415, Control No. 95/001,276, Replacement Exhibit AA, Claim Charts with respect to QuantumNet for Anticipation and Obviousness, filed January 5, 2010, 109 pages.	
	EB004	Request for Inter Partes Reexamination of US Patent No. 6,718,415, Control No. 95/001,276, Replacement Exhibit BB, Claim Charts with respect to Chatcom for Anticipation and Obviousness, filed January 5, 2010, 91 pages.	
	EB005	Request for Inter Partes Reexamination of US Patent No. 6,718,415, Control No. 95/001,276, Replacement Exhibit CC, Claim Charts with respect to QuantumNet for Anticipation and Obviousness, filed January 5, 2010, 85 pages.	
	EB006	Request for Inter Partes Reexamination of US Patent No. 6,718,415, Control No. 95/001,276, Replacement Exhibit DD, Claim Charts with respect to the Origin2000 Manual for Obviousness, filed January 5, 2010, 72 pages.	
	EB007	Request for Inter Partes Reexamination of US Patent No. 6,718,415, Control No. 95/001,276, Replacement Exhibit EE, Claim Charts with respect to Gallagher for Anticipation and Obviousness, filed January 5, 2010, 107 pages.	
	EB008	Office Action in Inter Partes Reexamination of US Patent No. 6,718,415, Control No. 95/001,276, mailed May 26, 2010, 39 pages.	
	EB009	Patent Owner's Response to Office Action in Inter Partes Reexamination of US Patent No. 6,718,415, Control No. 95/001,276, filed July 27, 2010, 41 pages.	

Examiner Signature	/Raymond Phan/	Date Considered	08/16/2011

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HN-933500

Intel Corp. v. ACQIS LLC
IPR2021-01103
EX2001 - 00372

Substitute for form 1449A/PTO		Complete if Known	
INFORMATION DISCLOSURE STATEMENT BY APPLICANT (Use as many sheets as necessary)		Application Number	To be assigned 13/087,912
		Filing Date	Herewith 04/15/11
		First Named Inventor	William W.Y. Chu
		Art Unit	2111
		Examiner Name	PHAN
		Attorney Docket Number	ACQI-010/19US 310578-2066
Sheet 18	of 26		

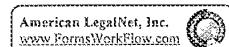
NON PATENT LITERATURE DOCUMENTS			
Examiner Initials*	Cite No. ¹	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.	T ²
	EB010	Patent Owner's Response to Office Action in Inter Partes Reexamination of US Patent No. 6,718,415, Control No. 95/001,276, Exhibit A, Declaration of William Henry Mangione-Smith under 37 C.F.R. 1.132, filed July 27, 2010, 29 pages.	
	EC001	Request for Inter Partes Reexamination of US Patent No. 7,099,981, Control No. 95/001,310, filed February 9, 2010, 33 pages	
	EC002	Request for Inter Partes Reexamination of US Patent No. 7,099,981, Control No. 95/001,310, filed December 2, 2009, Exhibit O, Declaration Under 37 CFR 1.132 of Vincent P. Conroy, 11-24-2009, 3 pages.	
	EC003	Request for Inter Partes Reexamination of US Patent No. 7,099,981, Control No. 95/001,310, Exhibit AA, Claim Charts with respect to Gallagher for Anticipation and Obviousness, filed February 9, 2010, 164 pages	
	EC004	Request for Inter Partes Reexamination of US Patent No. 7,099,981, Control No. 95/001,310, Exhibit BB, Claim Charts with respect to QuantumNet for Anticipation and Obviousness, filed February 9, 2010, 158 pages	
	EC005	Request for Inter Partes Reexamination of US Patent No. 7,099,981, Control No. 95/001,310, Exhibit CC, Claim Charts with respect to Chatcom for Anticipation and Obviousness, filed February 9, 2010, 167 pages	
	EC006	Request for Inter Partes Reexamination of US Patent No. 7,099,981, Control No. 95/001,310, Exhibit DD, Claim Charts with respect to the Eversys for Obviousness, filed February 9, 2010, 111 pages	
	EC007	Office Action in Inter Partes Reexamination of US Patent No. 7,099,981, Control No. 95/001,310, mailed July 6, 2010, 83 pages	
	EC008	Patent Owner's Response to Office Action in Inter Partes Reexamination of US Patent No. 7,099,981, Control No. 95/001,310, filed September 3, 2010, 52 pages	
	EC009	Patent Owner's Response to Office Action in Inter Partes Reexamination of US Patent No. 7,099,981, Control No. 95/001,310, Exhibit A, Declaration of William Henry Mangione-Smith under 37 C.F.R. 1.132, filed September 3, 2010, 63 pages	
	ED001	Request for Inter Partes Reexamination of US Patent No. 7,146,446, Control No. 95/001,328, filed March 19, 2010, 35 pages.	
	ED002	Request for Inter Partes Reexamination of US Patent No. 7,146,446, Control No. 95/001,328, Exhibit AA (Part 1), Claim Charts with respect to Gallagher for Anticipation and Obviousness, filed March 19, 2010, 186 pages.	

Examiner Signature	/Raymond Phan/	Date Considered	08/16/2011

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		First Named Inventor	William W.Y. Chu
		Art Unit	2111
		Examiner Name	PHAN
		Attorney Docket Number	ACQI-010/19US 310578-2066
Sheet 19	of 26		

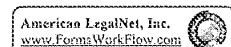
NON PATENT LITERATURE DOCUMENTS			
Examiner Initials*	Cite No. ¹	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.	T ²
	ED003	Request for Inter Partes Reexamination of US Patent No. 7,146,446, Control No. 95/001,328, Exhibit AA (Part 2), Claim Charts with respect to Gallagher for Anticipation and Obviousness, filed March 19, 2010, 161 pages.	
	ED004	Request for Inter Partes Reexamination of US Patent No. 7,146,446, Control No. 95/001,328, Exhibit BB (Part 1), Claim Charts with respect to QuantumNet for Anticipation and Obviousness, filed March 19, 2010, 139 pages.	
	ED005	Request for Inter Partes Reexamination of US Patent No. 7,146,446, Control No. 95/001,328, Exhibit BB (Part 2), Claim Charts with respect to QuantumNet for Anticipation and Obviousness, filed March 19, 2010, 128 pages.	
	ED006	Request for Inter Partes Reexamination of US Patent No. 7,146,446, Control No. 95/001,328, Exhibit CC, Claim Charts with respect to Chatcom for Anticipation and Obviousness, filed March 19, 2010, 68 pages.	
	ED007	Office Action in Inter Partes Reexamination of US Patent No. 7,146,446, Control No. 95/001,328, mailed June 24, 2010, 86 pages.	
	ED008	Patent Owner's Response to Office Action in Inter Partes Reexamination of US Patent No. 7,146,446, Control No. 95/001,328, filed August 24, 2010, 45 pages.	
	ED009	Patent Owner's Response to Office Action in Inter Partes Reexamination of US Patent No. 7,146,446, Control No. 95/001,328, Exhibit A, Declaration of William Henry Mangione-Smith under 37 C.F.R. 1.132, filed September 3, 2010, 61 pages.	
	EE001	Request for Inter Partes Reexamination of US Patent No. 7,328,297, Control No. 95/001,336, filed April 19, 2010, 33 pages.	
	EE002	Request for Inter Partes Reexamination of US Patent No. 7,328,297, Control No. 95/001,336, Exhibit AA, Claim Charts with respect to Gallagher for Obviousness, filed April 19, 2010, 131 pages.	
	EE003	Request for Inter Partes Reexamination of US Patent No. 7,328,297, Control No. 95/001,336, Exhibit BB, Claim Charts with respect to QuantumNet for Obviousness, filed April 19, 2010, 139 pages.	
	EE004	Request for Inter Partes Reexamination of US Patent No. 7,328,297, Control No. 95/001,336, Exhibit CC, Claim Charts with respect to Chatcom for Obviousness, filed April 19, 2010, 114 pages.	
	EE005	Office Action in Inter Partes Reexamination of US Patent No. 7,328,297, Control No. 95/001,336, mailed August 4, 2010, 95 pages.	

Examiner Signature	/Raymond Phan/	Date Considered	08/16/2011

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HN-933500

Intel Corp. v. ACQIS LLC
IPR2021-01103
EX2001 - 00374



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UNITED STATES DEPARTMENT OF COMMERCE
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 Address: COMMISSIONER FOR PATENTS
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 Alexandria, Virginia 22313-1450
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BIB DATA SHEET

CONFIRMATION NO. 7269

SERIAL NUMBER	FILING or 371(c) DATE	CLASS	GROUP ART UNIT	ATTORNEY DOCKET NO.		
13/087,912	04/15/2011	710	2111	ACQI-010/19US 310578-2066		
APPLICANTS William W.Y. Chu, Los Altos, CA; ** CONTINUING DATA ***** This application is a CON of 12/504,534 07/16/2009 which is a CON of 12/077,503 03/18/2008 PAT 7,676,624 which is a CON of 11/166,656 06/24/2005 PAT 7,376,779 which is a CON of 11/097,694 03/31/2005 PAT 7,363,415 which is a CON of 10/772,214 02/03/2004 PAT 7,099,981 which is a CON of 09/569,758 05/12/2000 PAT 6,718,415 which claims benefit of 60/134,122 05/14/1999 ** FOREIGN APPLICATIONS ***** ** IF REQUIRED, FOREIGN FILING LICENSE GRANTED ** 04/26/2011						
Foreign Priority claimed ☐ Yes ☒ No 35 USC 119(a-d) conditions met ☐ Yes ☒ No Verified and /RAYMOND NGAN PHAN/ Acknowledged Examiner's Signature		☐ Met after Allowance Initials	STATE OR COUNTRY CA	SHEETS DRAWINGS 24	TOTAL CLAIMS 53	INDEPENDENT CLAIMS 7
ADDRESS COOLEY LLP ATTN: Patent Group Suite 1100 777 - 6th Street, NW WASHINGTON, DC 20001 UNITED STATES						
TITLE MULTIPLE MODULE COMPUTER SYSTEM AND METHOD INCLUDING DIFFERENTIAL SIGNAL CHANNEL COMPRISING UNIDIRECTIONAL SERIAL BIT CHANNELS						
FILING FEE RECEIVED 3686	FEES: Authority has been given in Paper No. _____ to charge/credit DEPOSIT ACCOUNT No. _____ for following:			☐ All Fees ☐ 1.16 Fees (Filing) ☐ 1.17 Fees (Processing Ext. of time) ☐ 1.18 Fees (Issue) ☐ Other _____ ☐ Credit		

<i>Index of Claims</i> 	Application/Control No. 13087912	Applicant(s)/Patent Under Reexamination CHU, WILLIAM W.Y.
	Examiner RAYMOND PHAN	Art Unit 2111

✓	Rejected	-	Cancelled	N	Non-Elected	A	Appeal
=	Allowed	÷	Restricted	I	Interference	O	Objected

☐ Claims renumbered in the same order as presented by applicant			☐ CPA			☐ T.D.			☐ R.1.47		
CLAIM		DATE									
Final	Original	09/06/2011									
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<i>Index of Claims</i> 	Application/Control No. 13087912	Applicant(s)/Patent Under Reexamination CHU, WILLIAM W.Y.
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CLAIM		DATE									
Final	Original	09/06/2011									
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	72	✓									

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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In Re Application of: William W. Y. Chu Confirmation No.: 7269
Serial No.: 13/087,912 Group Art Unit: 2111
Filed: April 15, 2011 Examiner: Phan, Raymond Ngan
For: COMPUTER SYSTEM INCLUDING PERIPHERAL BRIDGE TO COMMUNICATE
SERIAL BITS OF PERIPHERAL COMPONENT INTERCONNECT BUS
TRANSACTION AND LOW VOLTAGE DIFFERENTIAL SIGNAL CHANNEL TO
CONVEY THE SERIAL BITS (AS AMENDED)

Mail Stop Amendment
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

AMENDMENT/RESPONSE TO OFFICE ACTION

In response to the Office Action dated September 16, 2011, please amend the above-identified patent application in the following manner:

Amendments to the Drawings begin on page 2 of this paper.

Amendments to the Specification begin on page 3 of this paper.

Amendments to the Claims are reflected on the listing of the claims which begins on page 5 of this paper.

Remarks/Arguments begin on page 14 of this paper.

IN THE DRAWINGS

Attachment: New Sheets Fig. 8C and Fig. 24

The subject application is amended to specifically include certain figures from U.S. Provisional Application No. 60/083,886.

IN THE SPECIFICATION

Please amend the title as follows:

~~MULTIPLE MODULE COMPUTER SYSTEM AND METHOD INCLUDING PERIPHERAL BRIDGE TO COMMUNICATE SERIAL BITS OF PERIPHERAL COMPONENT INTERCONNECT BUS TRANSACTION AND LOW VOLTAGE DIFFERENTIAL SIGNAL CHANNEL TO CONVEY THE SERIAL BITS COMPRISING UNIDIRECTIONAL SERIAL BIT CHANNELS~~

Please add paragraph no. [0043.1] as set forth below immediately after paragraph no. [0043]:

[0043.1] In an implementation with South Bridge in Peripheral Console, Fig. 8C shows an example of an attached computer module with Integrated CPU/North Bridge/Graphics and Peripheral Console with Integrated Peripheral Interface Controller and South Bridge.

Please add paragraph no. [0059.1] as set forth below immediately after paragraph no. [0059]:

[0059.1] Fig. 24 shows an attached computer module with a “Plug & Display” port and direct power connection.

Please replace paragraph no. [0095] with the following paragraph. The amendments to paragraph no. [0095] are indicated by strikethrough and underlining.

[0095] In the embodiment shown in Fig. 6, HIC 619 is coupled to an integrated unit 621 that includes a CPU, a cache and a north bridge. In another embodiment, such as that shown in Fig. 7, the CPU 705 and north bridge 710 are separate rather than integrated units. In yet another embodiment, such as that shown in Fig. 8, the HIC and PIC are integrated with the north and south bridges, respectively, such that integrated HIC and north bridge unit 805 includes an HIC and a north bridge, while integrated PIC and south bridge unit 810 includes a PIC and a south bridge. Fig. 8A shows an attached computer module with integrated CPU/NB/Graphics 815 and Integrated HIC/SB 820. Fig. 8B shows an attached computer module with single chip 825 fully

integrated: CPU, Cache, Core Logic, Graphics controller and Interface controller. In an implementation with South Bridge in Peripheral Console, Fig. 8C shows an example of an attached computer module with Integrated CPU/North Bridge/Graphics and Peripheral Console with Integrated Peripheral Interface Controller and South Bridge.

Please replace paragraph no. [0167] with the following paragraph. The amendments to paragraph no. [0167] are indicated by strikethrough and underlining.

[0167] Connector component 1950 may be selected to mate directly with the connector component 1930 of an ACM (shown in FIG. 18). Alternatively, connector component 1950 may be selected to mate with, for example, the connector on one end of a cable intervening between the PCON and an ACM in a particular embodiment, such as cable 1964 shown in FIG. 19B. Fig. 24 shows an attached computer module with a “Plug & Display” port and direct power connection. The ACM-to-PCON interconnection described in the aforementioned companion patent application has the advantage of providing reliable signal conveyance across low cost cables.

IN THE CLAIMS

1-43. (Cancelled)

44. (Currently Amended) A computer system comprising:
a central processing unit;
a peripheral bridge to communicate serial bits of Peripheral Component Interconnect (PCI) bus transaction, the peripheral bridge directly coupled to the central processing unit without any intervening PCI bus;
a low voltage differential signal (LVDS) channel comprising at least two unidirectional, differential signal pairs to convey data in opposite directions, the LVDS channel directly extending from the peripheral bridge to convey the serial bits of PCI bus transaction, the serial bits of PCI bus transaction comprising PCI address and data bits;
a main memory coupled to the central processing unit ~~through the peripheral bridge~~; and
a peripheral component coupled to the peripheral bridge through the LVDS channel.

45-49. (Cancelled)

50. (Currently Amended) The computer system of claim 44 ~~[[49]]~~, wherein the peripheral bridge comprises an interface controller integrated with the ~~north~~ peripheral bridge, the interface controller is coupled to the central processing unit without any intervening PCI bus, and the interface controller is configured to output encoded address and data bits of PCI bus transaction in serial form that are conveyed over the LVDS channel.

51. (Previously Presented) The computer system of claim 44, wherein the serial bits of PCI bus transaction comprise information to permit decoding to create a PCI bus transaction.

52. (Previously Presented) The computer system of claim 44, wherein the LVDS channel comprises a first plurality of unidirectional, differential signal pairs to convey data in a first direction and a second plurality of unidirectional, differential signal pairs to convey data in a second, opposite direction.

53. (Currently Amended) A computer system comprising:
a computer module ~~insertable into~~ configured to couple to a console for operation, the computer module comprising
a central processing unit,
an integrated interface controller and bridge unit to output encoded address and data bits of Peripheral Component Interconnect (PCI) bus transaction in serial form, the integrated interface controller and bridge unit directly coupled to the central processing unit without any intervening PCI bus,
a low voltage differential signal (LVDS) channel directly coupled to the integrated interface controller and bridge unit to convey the encoded address and data bits of PCI bus transaction in serial form, and
a main memory coupled to the central processing unit ~~through the integrated interface controller and bridge unit.~~

54. (Previously Presented) The computer system of claim 53, further comprising a peripheral component coupled to the integrated interface controller and bridge unit through the LVDS channel.

55. (Previously Presented) The computer system of claim 53, wherein the LVDS channel comprises a first plurality of unidirectional, differential signal pairs to convey data in a first direction and a second plurality of unidirectional, differential signal pairs to convey data in a second, opposite direction.

56-58. (Cancelled)

59. (Currently Amended) The computer system of claim 53 ~~[[58]]~~, ~~wherein~~ further comprising the console, the console comprises a coupling site and a multi-port, serial communication hub controller, and the computer module comprises a serial communication

controller to communicate, via a point-to-point link, with the multi-port, serial communication hub controller through the coupling site of the console.

60-73. (Cancelled)

74. (Currently Amended) A computer module comprising:
an enclosure ~~insertable into~~ configured to couple to a console;
a central processing unit housed in the enclosure, the central processing unit comprising an interface ~~controller~~ to transmit and receive serial bits of Peripheral Component Interconnect (PCI) bus transaction, the serial bits of PCI bus transaction comprising PCI address and data bits;
a system memory housed in the enclosure and directly coupled to the central processing unit; and
a low voltage differential signal (LVDS) channel housed in the enclosure, the LVDS channel comprising a first unidirectional, differential signal pair to convey data in a first direction and a second unidirectional, differential signal pair to convey data in a second, opposite direction, the LVDS channel directly extending from the central processing unit to convey the serial bits of PCI bus transaction.

75. (Cancelled)

76. (Currently Amended) The computer module of claim 74 [[75]], wherein the central processing unit comprises a graphics subsystem integrated with the central processing unit in a ~~[[the]]~~ single chip.

77. (Currently Amended) The computer module of claim 76, further comprising a graphics memory directly coupled to the central processing unit.

78. (Currently Amended) The computer module of claim 74, further comprising a mass storage device directly coupled to the central processing unit.

79. (Currently Amended) The computer module of claim 74, wherein the interface ~~controller~~ is configured to output encoded address and data bits of PCI bus transaction in serial form that are conveyed over the LVDS channel.

80-82. (Cancelled)

83. (Currently Amended) A computer system comprising:

a computer module comprising

an enclosure ~~insertable into~~ comprising a connector that is configured to couple to a console,

an integrated interface controller and central processing unit to output encoded address and data bits of Peripheral Component Interconnect (PCI) bus transaction in serial form, the integrated interface controller and central processing unit configured as a single chip and housed in the enclosure,

a low voltage differential signal (LVDS) channel housed in the enclosure and comprising a first plurality of unidirectional, differential signal pairs to convey data in a first direction and a second plurality of unidirectional, differential signal pairs to convey data in a second, opposite direction, the LVDS channel ~~coupled to~~ directly extending from the integrated interface controller and central processing unit to convey the encoded address and data bits of PCI bus transaction in serial form, and

a system memory housed in the enclosure and coupled to the integrated interface controller and central processing unit.

84. (Currently Amended) The computer system of claim 83, wherein the integrated interface controller and central processing unit comprises a graphics subsystem integrated in the single chip.

85. (Currently Amended) The computer system of claim 84, further comprising the console, and the console comprises a LCD display ~~coupled~~ configured to couple to the graphics subsystem.

86. (Currently Amended) The computer system of claim 83, further comprising a peripheral component coupled to the integrated interface controller and central processing unit through the LVDS channel.

87. (Cancelled)

88. (Currently Amended) The computer system of claim 83, further comprising the console, and the console comprises a power supply to supply power to the computer module upon ~~insertion into~~ coupling to the console.

89. (Currently Amended) The computer system of claim 83 ~~[[88]]~~, wherein the console comprises a coupling site and a multi-port, ~~Ethernet~~ serial communication hub controller, and the computer module comprises an ~~Ethernet~~ a serial communication controller to communicate, via a point-to-point ~~Ethernet~~ serial link, with the multi-port, ~~Ethernet~~ serial communication hub controller through the coupling site of the console.

90. (Currently Amended) A computer system comprising:
a low voltage differential signal (LVDS) channel comprising at least two sets of unidirectional, multiple serial bit channels to convey data in opposite directions;
a central processing unit comprising an interface directly coupled to the LVDS channel to communicate address and data bits of PCI bus transaction in serial form over the LVDS channel;
a system memory directly coupled to the central processing unit; and
a peripheral component coupled to the central processing unit through the LVDS channel.

91. (Currently Amended) The computer system of claim 90, wherein the central processing unit comprises a graphics subsystem integrated with the central processing unit in a single chip.

92. (Currently Amended) The computer system of claim 91, further comprising a graphics memory directly coupled to the central processing unit.

93. (Currently Amended) The computer system of claim 90, further comprising a mass storage device directly coupled to the central processing unit.

94. (Previously Presented) The computer system of claim 90, wherein the peripheral component comprises a serial communication controller.

95. (Cancelled)

96. (Currently Amended) The computer system of claim 90, wherein the interface of the central processing unit is configured to output an encoded serial bit stream of PCI address and data information, and the LVDS channel directly extends from the interface of the central processing unit to convey the encoded serial bit stream.

97. (New) A modular computer system comprising:
a modular computer comprising
a connector configured to couple to a console;
a first low voltage differential signal (LVDS) channel comprising at least two sets of unidirectional, multiple serial bit channels to convey data in opposite directions;
an integrated central processing unit and graphics controller configured as a single chip, the integrated central processing unit and graphics controller comprising an interface directly coupled to the first LVDS channel to communicate encoded address and data bits of Peripheral Component Interconnect (PCI) bus transaction in serial form over the first LVDS channel; and
a system memory directly coupled to the integrated central processing unit and graphics controller,
wherein the connector is configured to convey the encoded address and data bits of PCI bus transaction in serial form to the console upon coupling the connector to the console.

98. (New) The modular computer system of claim 97, further comprising a second LVDS channel coupled to the integrated central processing unit and graphics controller to convey digital video data.

99. (New) The modular computer system of claim 98, wherein the connector is coupled to the integrated central processing unit and graphics controller through the second LVDS channel, and the connector is configured to convey the digital video data to the console upon coupling the connector to the console.

100. (New) The modular computer system of claim 99, further comprising the console, the console comprises a LCD display, and the console is configured to receive the digital video data from the integrated central processing unit and graphics controller through the second LVDS channel and the connector.

101. (New) The modular computer system of claim 97, further comprising the console, and the console comprises an interface controller that is configured to couple to the connector for communication of the encoded address and data bits of PCI bus transaction in serial form.

102. (New) The modular computer system of claim 101, wherein the console comprises a mass storage device coupled to the interface controller.

103. (New) A modular computer system comprising:

a modular computer comprising

a connector configured to couple to a console;

a first low voltage differential signal (LVDS) channel comprising at least two sets of unidirectional, multiple serial bit channels to convey data in opposite directions;

an integrated central processing unit and graphics controller configured as a single chip;

a peripheral bridge directly coupled to the integrated central processing unit and graphics controller without any intervening Peripheral Component Interconnect (PCI) bus, the

peripheral bridge directly coupled to the first LVDS channel to communicate encoded address and data bits of PCI bus transaction in serial form over the first LVDS channel; and

a system memory directly coupled to the integrated central processing unit and graphics controller,

wherein the connector is configured to convey the encoded address and data bits of PCI bus transaction in serial form to the console upon coupling the connector to the console.

104. (New) The modular computer system of claim 103, further comprising a second LVDS channel coupled to the integrated central processing unit and graphics controller to convey digital video data.

105. (New) The modular computer system of claim 104, wherein the connector is coupled to the integrated central processing unit and graphics controller through the second LVDS channel, and the connector is configured to convey the digital video data to the console upon coupling the connector to the console.

106. (New) The modular computer system of claim 105, further comprising the console, the console comprises a LCD display, and the console is configured to receive the digital video data from the integrated central processing unit and graphics controller through the second LVDS channel and the connector.

107. (New) The modular computer system of claim 103, further comprising the console, and the console comprises an interface controller that is configured to couple to the connector for communication of the encoded address and data bits of PCI bus transaction in serial form.

108. (New) The modular computer system of claim 107, wherein the console comprises a mass storage device coupled to the interface controller.

109. (New) A computer system comprising:

a first low voltage differential signal (LVDS) channel comprising at least two sets of unidirectional, multiple serial bit channels to convey data in opposite directions;

a central processing unit comprising a peripheral controller integrated with the central processing unit as a single chip, the peripheral controller directly coupled to the first LVDS channel to communicate encoded address and data bits of Peripheral Component Interconnect (PCI) bus transaction in serial form over the first LVDS channel;

a system memory directly coupled to the central processing unit; and

a mass storage device coupled to the central processing unit.

110. (New) The computer system of claim 109, wherein the central processing unit comprises a graphics controller integrated in the single chip, and further comprising a second LVDS channel directly coupled to the graphics controller in the single chip to convey digital video data.

111. (New) The computer system of claim 109, further comprising an enclosure with a connector, and the connector is coupled to the first LVDS channel to convey the encoded address and data bits of PCI bus transaction in LVDS form.

REMARKS

Claims 44-96 were pending in the subject application, and stand rejected. By this paper, Applicant is amending claims 44, 50, 53, 59, 74, 76-79, 83-86, 88-93, and 96, is adding new claims 97-111, and is cancelling claims 45-49, 56-58, 60-73, 75, 80-82, 87, and 95, without prejudice or disclaimer of the subject matter contained therein. Applicant is also amending the drawings and specification.

Drawings and Specification

The subject application is a continuation of U.S. Application No. 12/504,534 (the “534 parent application”), which is a continuation of U.S. Application No. 12/077,503, which is a continuation of U.S. Application No. 11/166,656, which is a continuation of U.S. Application No. 11/097,694, which is a continuation of U.S. Application No. 10/772,214, which is a continuation of U.S. Application No. 09/569,758 (the “758 parent application”).

The original ‘758 parent application incorporated by reference U.S. Application No. 09/149,882 (now issued as U.S. Patent No. 6,345,330), which, in turn, claimed the benefit of and incorporated by reference U.S. Provisional Application No. 60/083,886 (the “886 provisional application”) (*See* checked incorporation by reference box in utility patent application transmittal of U.S. Application No. 09/149,882 filed on September 8, 1998). By this paper, the subject application is amended to specifically include certain figures and text from the ‘886 provisional application. Specifically, the subject application is amended to add new FIG. 8C and FIG. 24, as well as accompanying text for these added figures. This corresponds to: (a) figure 10 and figure 16 of the ‘886 provisional application; and (b) the text of the ‘886 provisional application as originally included in figure legends of figure 10 and figure 16.

Applicant is also amending the title to more closely correspond to the claimed subject matter, in view of the Examiner’s objection to the title.

Double Patenting

The Examiner has rejected claims 44, 74, 83, and 90 on the ground of nonstatutory obviousness-type double patenting as allegedly unpatentable over certain claims of the ‘534

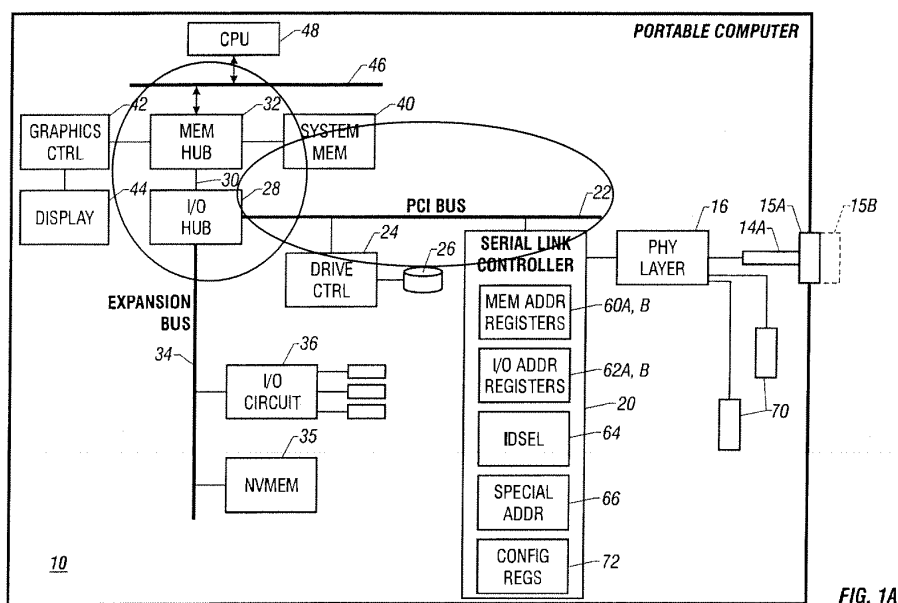
parent application (now issued as U.S. Patent No. 8,041,873). Applicant respectfully traverses these rejections. Nonetheless, in an effort to expedite the prosecution of the subject application and without conceding as to the substance of the rejections, Applicant is submitting a Terminal Disclaimer over U.S. Patent No. 8,041,873 to obviate the rejections.

Claim Rejections – 35 U.S.C. §102 and §103

The Examiner has rejected the claims as allegedly anticipated by Tripathi (U.S. Patent No. 6,161,157) or as allegedly unpatentable over Tripathi in view of Hong (U.S. Patent No. 5,764,924). Applicant respectfully traverses these rejections. Nonetheless, in an effort to expedite the prosecution of the subject application and without conceding as to the substance of the rejections, Applicant is amending the claims to further distinguish over the cited references.

As amended, claim 44 specifies: (1) a central processing unit; and (2) a peripheral bridge to communicate serial bits of Peripheral Component Interconnect (PCI) bus transaction, the peripheral bridge “directly” coupled to the central processing unit “without any intervening PCI bus.”

The Examiner points to Fig. 1A of Tripathi (reproduced below with emphasis added) and, in particular, a serial link controller 20 as presumably corresponding to the claimed peripheral bridge. However, as shown in Fig. 1A of Tripathi, the serial link controller 20 is not “directly” coupled to a CPU 48, but rather is coupled to the CPU 48 through a memory hub 32 and an I/O hub 28. Moreover, Fig. 1A of Tripathi shows a PCI bus 22 coupled between the serial link controller 20 and the CPU 48, and, therefore, the serial link controller 20 is coupled to the CPU 48 with the intervening PCI bus 22, instead of “without any intervening PCI bus.” The deficiencies of Tripathi are not remedied by Hong. For at least these reasons, claim 44 and its dependent claims should be in a condition for allowance.



Claims 53 and 103 specify features similar to those discussed above for claim 44. Therefore, and for at least the reasons applicable for claim 44, claims 53 and 103 and their dependent claims should be in a condition for allowance.

In addition, claim 103 specifies an “integrated” central processing unit and graphics controller configured as “a single chip.” In contrast, Fig. 1A of Tripathi shows a graphics controller 42 as a separate component from the CPU 48, rather than “integrated” with the CPU 48 as “a single chip.” For this additional reason, claim 103 and its dependent claims should be in a condition for allowance.

As amended, claim 74 specifies a central processing unit “comprising” an interface to transmit and receive serial bits of PCI bus transaction. In accordance with this claim, a central processing unit comprises an interface that transmits and receives serial bits of PCI bus transaction, and, therefore, the claimed interface is part of, or is integrated with, the central processing unit. In contrast, Fig. 1A of Tripathi shows the serial link controller 20 as a separate component from the CPU 48, with the memory hub 32, the I/O hub 28, and the PCI bus 22 coupled between the separate serial link controller 20 and the CPU 48. The deficiencies of Tripathi are not remedied by Hong. For at least these reasons, claim 74 and its dependent claims should be in a condition for allowance.

Claims 83, 90, 97, and 109 specify features similar to those discussed above for claim 74. Therefore, and for at least the reasons applicable for claim 74, claims 83, 90, 97, and 109 and their dependent claims should be in a condition for allowance.

With respect to claim 88 (which is dependent from claim 83), the Examiner takes official notice as allegedly well known for a console to supply power to a computer module. Applicant respectfully traverses this official notice, and, if the rejection is maintained, Applicant respectfully requests that the Examiner supply documentary evidence.

In addition, claim 97 specifies an “integrated” central processing unit and graphics controller configured as “a single chip.” In contrast, Fig. 1A of Tripathi shows the graphics controller 42 as a separate component from the CPU 48, rather than “integrated” with the CPU 48 as “a single chip.” For this additional reason, claim 97 and its dependent claims should be in a condition for allowance.

CONCLUSION

In view of the foregoing, Applicant respectfully submits that no further impediments exist to the allowance of this application and, therefore, requests an indication of allowability. However, the Examiner is requested to call the undersigned if any questions or comments arise.

The Director is hereby authorized to charge any appropriate fees under 37 C.F.R. §§1.16, 1.17, and 1.21 that may be required by this paper, and to credit any overpayment, to Deposit Account No. 50-1283.

Date: December 16, 2011

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Respectfully submitted,
COOLEY LLP

By: _____


Cliff Z. Liu
Reg. No. 50,834

Electronic Patent Application Fee Transmittal				
Application Number:		13087912		
Filing Date:		15-Apr-2011		
Title of Invention:		MULTIPLE MODULE COMPUTER SYSTEM AND METHOD INCLUDING DIFFERENTIAL SIGNAL CHANNEL COMPRISING UNIDIRECTIONAL SERIAL BIT CHANNELS		
First Named Inventor/Applicant Name:		William W.Y. Chu		
Filer:		Cliff Z. Liu/Kathleen Smith		
Attorney Docket Number:		ACQI-010/19US 310578-2066		
Filed as Large Entity				
Utility under 35 USC 111(a) Filing Fees				
Description	Fee Code	Quantity	Amount	Sub-Total in USD(\$)
Basic Filing:				
Pages:				
Claims:				
Miscellaneous-Filing:				
Petition:				
Patent-Appeals-and-Interference:				
Post-Allowance-and-Post-Issuance:				
Extension-of-Time:				

Description	Fee Code	Quantity	Amount	Sub-Total in USD(\$)
Miscellaneous:				
Statutory or terminal disclaimer	1814	1	160	160
Total in USD (\$)				160

Electronic Acknowledgement Receipt	
EFS ID:	11643316
Application Number:	13087912
International Application Number:	
Confirmation Number:	7269
Title of Invention:	MULTIPLE MODULE COMPUTER SYSTEM AND METHOD INCLUDING DIFFERENTIAL SIGNAL CHANNEL COMPRISING UNIDIRECTIONAL SERIAL BIT CHANNELS
First Named Inventor/Applicant Name:	William W.Y. Chu
Customer Number:	58249
Filer:	Cliff Z. Liu/Kathleen Smith
Filer Authorized By:	Cliff Z. Liu
Attorney Docket Number:	ACQI-010/19US 310578-2066
Receipt Date:	16-DEC-2011
Filing Date:	15-APR-2011
Time Stamp:	17:15:21
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	yes
Payment Type	Deposit Account
Payment was successfully received in RAM	\$ 160
RAM confirmation Number	4516
Deposit Account	501283
Authorized User	
The Director of the USPTO is hereby authorized to charge indicated fees and credit any overpayment as follows: Charge any Additional Fees required under 37 C.F.R. Section 1.21 (Miscellaneous fees and charges)	

File Listing:					
Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1	New or Additional Drawings	ACQI01019US_NewDrawings_16Dec11.pdf	110222	no	2
			ceec995e21e943bab99e42db733b2c1fbd8bb01		
Warnings:					
Information:					
2		ACQI01019US_TerminalDisclaimer_Amendment_16Dec11.pdf	233505	yes	18
			ffe04fd0f2a8a2ed8f928cf6d084064693a5c91e		
	Multipart Description/PDF files in .zip description				
	Document Description		Start	End	
	Terminal Disclaimer Filed		1	1	
	Amendment/Req. Reconsideration-After Non-Final Reject		2	2	
	Drawings-only black and white line drawings		3	3	
	Specification		4	5	
	Claims		6	14	
	Applicant Arguments/Remarks Made in an Amendment		15	18	
Warnings:					
Information:					
3	Fee Worksheet (SB06)	fee-info.pdf	30792	no	2
			12688f90fc2e8f17567b4df91ab9557edbedd6f1		
Warnings:					
Information:					
Total Files Size (in bytes):			374519		

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New Applications Under 35 U.S.C. 111

If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application.

National Stage of an International Application under 35 U.S.C. 371

If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.

New International Application Filed with the USPTO as a Receiving Office

If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.

NEW SHEET

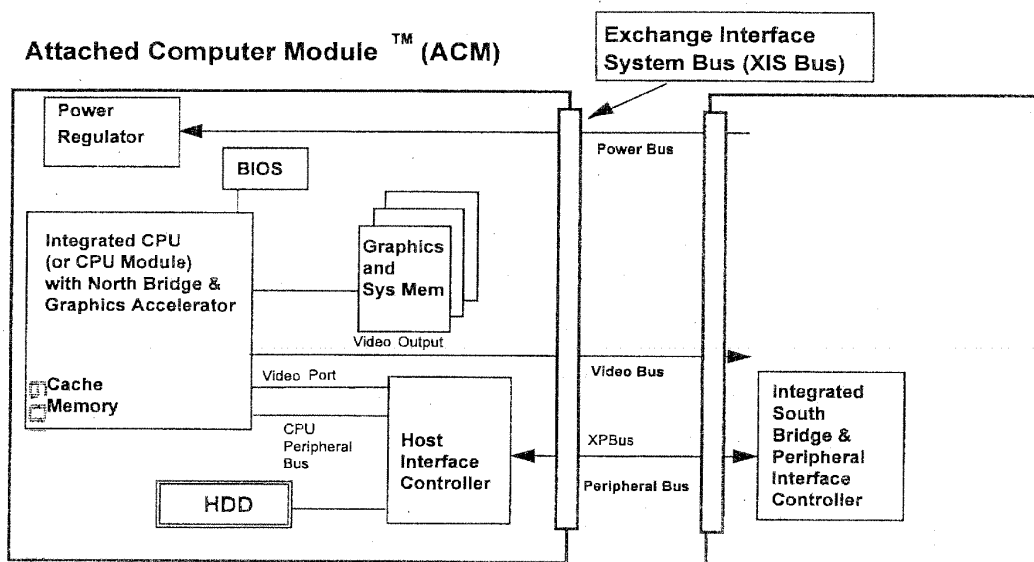


Fig. 8C In the implementation with South Bridge in Peripheral Console, an example of Attached Computer Module with Integrated CPU/North Bridge/Graphics and Peripheral Console with Integrated Peripheral Interface Controller and South Bridge

NEW SHEET

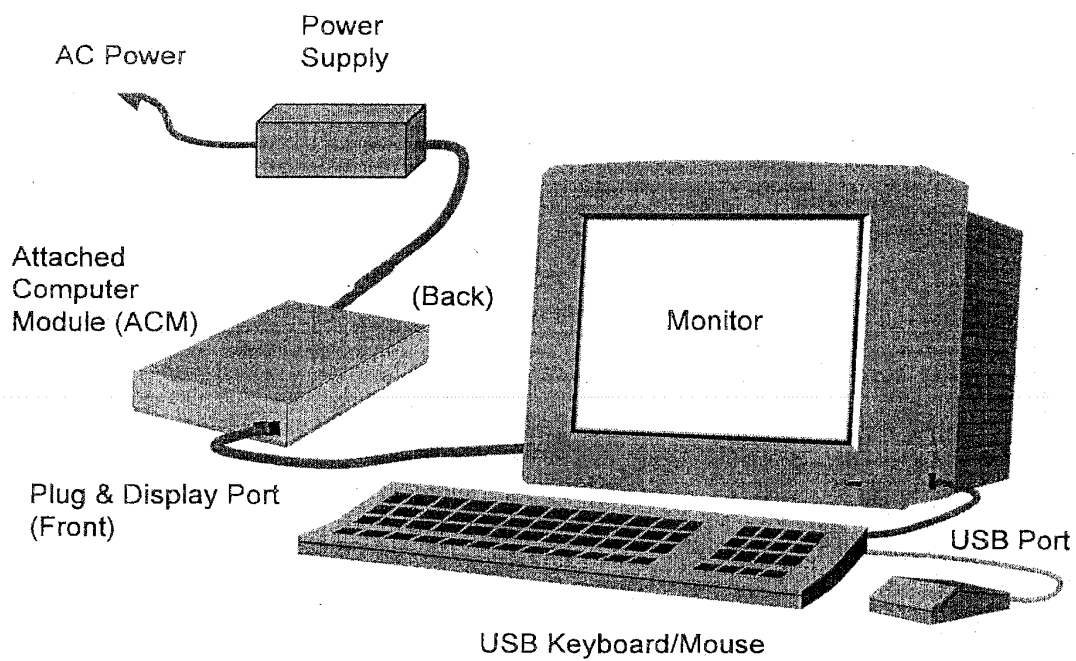


Fig. 24 Attached Computer Module with a "Plug & Display" port and direct power connection.

**TERMINAL DISCLAIMER TO OBVIATE A PROVISIONAL DOUBLE PATENTING
REJECTION OVER A PENDING "REFERENCE" APPLICATION**

Docket Number (Optional)
ACQI-010/19US 310578-
2066

In re Application of: William W. Y. Chu

Application No.: 13/087,912

Filed: April 15, 2011

For: Computer System Including Peripheral Bridge To Communicate Serial Bits Of Peripheral Component Interconnect Bus Transaction And Low Voltage Differential Signal Channel To Convey The Serial Bits

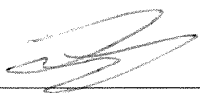
The owner, ACQIS LLC, of 100 percent interest in the instant application hereby disclaims, except as provided below, the terminal part of the statutory term of any patent granted on the instant application which would extend beyond the expiration date of the full statutory term of any patent granted on pending reference Application Number 12/504,534, filed July 16, 2009, as the term of any patent granted on said reference application may be shortened by any terminal disclaimer filed prior to the grant of any patent on the pending reference application. The owner hereby agrees that any patent so granted on the instant application shall be enforceable only for and during such period that it and any patent granted on the reference application are commonly owned. This agreement runs with any patent granted on the instant application and is binding upon the grantee, its successors or assigns. In making the above disclaimer, the owner does not disclaim the terminal part of any patent granted on the instant application that would extend to the expiration date of the full statutory term of any patent granted on said reference application, "as the term of any patent granted on said reference application may be shortened by any terminal disclaimer filed prior to the grant of any patent on the pending reference application," in the event that: any such patent: granted on the pending reference application: expires for failure to pay a maintenance fee, is held unenforceable, is found invalid by a court of competent jurisdiction, is statutorily disclaimed in whole or terminally disclaimed under 37 CFR 1.321, has all claims canceled by a reexamination certificate, is issued, or is in any manner terminated prior to the expiration of its full statutory term as shortened by any terminal disclaimer filed prior to its grant.

Check either box 1 or 2 below, if appropriate.

1. ☐ For submissions on behalf of a business/organization (e.g., corporation, partnership, university, government agency, etc.), the undersigned is empowered to act on behalf of the business/organization.

I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code and that such willful false statements may jeopardize the validity of the application or any patent issued thereon.

2. ☒ The undersigned is an attorney or agent of record. Reg. No. 50,834



Signature

December 16, 2011

Date

Cliff Z. Liu

Typed or printed name

650 843-5852

Telephone Number

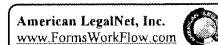
- ☒ Terminal disclaimer fee under 37 CFR 1.20(d) is included.

WARNING: Information on this form may become public. Credit card information should not be included on this form. Provide credit card information and authorization on PTO-2038.

*Statement under 37 CFR 3.73(b) is required if terminal disclaimer is signed by the assignee (owner).
Form PTO/SB/96 may be used for making this statement. See MPEP § 324.

This collection of information is required by 37 CFR 1.321. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.11 and 1.14. This collection is estimated to take 12 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.

If you need assistance in completing the form, call 1-800-PTO-9199 and select option 2.



Application Number 	Application/Control No. 13/087,912	Applicant(s)/Patent under Reexamination CHU, WILLIAM W.Y.	
Document Code - DISQ		Internal Document – DO NOT MAIL	

TERMINAL DISCLAIMER	☒ APPROVED	☐ DISAPPROVED
Date Filed : 12/16/11	This patent is subject to a Terminal Disclaimer	

Approved/Disapproved by:
Angie Walker

U.S. Patent and Trademark Office



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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
13/087,912	04/15/2011	William W.Y. Chu	ACQI-010/19US 310578-2066	7269
58249	7590	03/13/2012	EXAMINER	
COOLEY LLP			PHAN, RAYMOND NGAN	
ATTN: Patent Group				
Suite 1100			ART UNIT	
777 - 6th Street, NW			PAPER NUMBER	
WASHINGTON, DC 20001			2111	
			MAIL DATE	DELIVERY MODE
			03/13/2012	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.		Applicant(s)	
	13/087,912		CHU, WILLIAM W.Y.	
	Examiner		Art Unit	
	RAYMOND PHAN		2111	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1) ☒ Responsive to communication(s) filed on 27 January 2012.

2a) ☒ This action is **FINAL**. 2b) ☐ This action is non-final.

3) ☐ An election was made by the applicant in response to a restriction requirement set forth during the interview on ____; the restriction requirement and election have been incorporated into this action.

4) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

5) ☒ Claim(s) 44,50-55,59,74,76-79,83-86,88-94 and 96-111 is/are pending in the application.

5a) Of the above claim(s) ____ is/are withdrawn from consideration.

6) ☒ Claim(s) 97-108 is/are allowed.

7) ☒ Claim(s) 44,50-55,59,74,76-79,83-86,88-94,96,109 and 111 is/are rejected.

8) ☒ Claim(s) 110 is/are objected to.

9) ☐ Claim(s) ____ are subject to restriction and/or election requirement.

Application Papers

10) ☐ The specification is objected to by the Examiner.

11) ☐ The drawing(s) filed on ____ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

12) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

13) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a) ☐ All b) ☐ Some * c) ☐ None of:

1. ☐ Certified copies of the priority documents have been received.

2. ☐ Certified copies of the priority documents have been received in Application No. ____.

3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)	4) ☐ Interview Summary (PTO-413)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)	Paper No(s)/Mail Date. ____.
3) ☐ Information Disclosure Statement(s) (PTO/SB/08)	5) ☐ Notice of Informal Patent Application
Paper No(s)/Mail Date ____.	6) ☐ Other: ____.

Part III DETAILED ACTION

Notice to Applicant(s)

1. This action is responsive to the following communications: amendment filed on January 27, 2012.
2. This application has been examined. Claims 44, 50-54, 55, 59, 74, 76-79, 83-86, 88-94, 96-111 are pending.

Double Patenting

3. The Terminal Disclaimer is received and approved.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(e) the invention was described in-

(1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effect under this subsection of a national application published under section 122(b) only if the international application designating the United States was published under Article 21(2)(a) of such treaty in the English language; or

(2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that a patent shall not be deemed filed in the United States for the purposes of this subsection based on the filing of an international application filed under the treaty defined in section 351(a).

4. Claims 53-54, 83-86, are rejected under 35 U.S.C. § 102(e) as being anticipated by Tripathi et al. (US No. 6,161,157).

In regard to claim 53, 83, Tripathi et al. disclose a computer system comprising: a computer module insertable into a console for operation, the computer module comprising a processing unit, an integrated interface controller and bridge unit to output encoded address and data bits of Peripheral Component Interconnect (PCI) bus transaction in serial form (see col. 4, lines 1-13), the

integrated interface controller and bridge unit coupled to the processing unit without any intervening PCI bus, a low voltage differential signal (LVDS) channel coupled to the integrated interface controller and bridge unit to convey the encoded address and data bits of PCI bus transaction in serial form, and a main memory coupled to the processing unit through the integrated interface controller and bridge unit (see figure 1A, col. 4, lines 25-49).

In regard to claim 54, 84, Tripathi et al. disclose further a peripheral component coupled to the integrated interface controller and bridge unit through the LVDS channel (see figure 1A).

In regard to claim 86, Tripathi et al. disclose wherein the computer module comprises an enclosure housing the processing unit, the integrated interface controller and bridge unit, the LVDS channel, and the main memory (see figure 1A).

In regard to claim 85, Tripathi et al. disclose further the console, and the console comprises a LCD display coupled to the graphics subsystem (see figure 1A, col. 3, lines 9-18).

Claim Rejections - 35 USC § 103

5. The following is a quotation of 35 U.S.C. § 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

6. Claims 44, 50-52, 55, 59, 74, 76-79, 88-94, 96, 109, 111 are rejected under 35 U.S.C. § 103(a) as being unpatentable over Tripathi et al. (US No. 6,161,157) in view of Hong (US No. 5,764,924).

In regard to claims 44, 74, 90, 109, Tripathi et al. disclose a computer system comprising: a processing unit; a peripheral bridge to communicate serial bits of Peripheral Component Interconnect (PCI) bus transaction, the peripheral bridge directly coupled to the processing unit (see figure 1A); a low voltage differential signal (LVDS) channel (i.e. IEEE-1394), the LVDS channel extending from the peripheral bridge to convey the serial bits of PCI bus transaction, the serial bits of PCI bus transaction comprising PCI address and data bits (see col. 8, line 49 through col. 9, line 19); a main memory coupled to the processing unit through the peripheral bridge (see figure 1A, col. 3, lines 19-27); and a peripheral component coupled to the peripheral bridge (see figure 1A). But Tripathi et al. do not specifically disclose at least two unidirectional, differential signal pairs to convey data in opposite directions. However Hong discloses at least two unidirectional, differential signal pairs to convey data in opposite directions (see figure 2). Therefore, it would have been obvious to a person of an ordinary skill in the art at the time the invention was made to have combined the teachings of Hong into the teachings of Tripathi et al. because each of Hong and Tripathi et al. teach the data transfer between the mobile computer and the docking station/base and further, because combining the prior art elements of Hong with Tripathi et al. according to known methods would have yielded predictable results, using the techniques of Hong would have improved Tripathi et al. in the same way, and applying the techniques of Hong to improve Tripathi et al. would have yielded predictable results (e.g. reliable serial link connection and high-speed data transfer). [See MPEP 2143].

In regard to claims 94, Tripathi et al. disclose wherein the peripheral component comprises a serial communication controller (see figure 1A, col. 3, lines 19-27).

In regard to claim 76, 91, Tripathi et al. disclose further comprising a graphics subsystem coupled to the processing unit through the peripheral bridge (i.e. south bridge) (see figure 1A).

In regard to claims 50, 111, Tripathi et al. disclose wherein the peripheral bridge comprises an interface controller integrated with the north bridge, the interface controller is coupled to the processing unit without any intervening PCI bus, and the interface controller is configured to output encoded address and data bits of PCI bus transaction in serial form that are conveyed over the LVDS channel (see figure 1A, col. 4, lines 25-49).

In regard to claim 51, 79, Tripathi et al. disclose wherein the serial bits of PCI bus transaction comprise information to permit decoding to create a PCI bus transaction (see col. 4, lines 7-13).

In regard to claims 52, 55, Hong discloses wherein the LVDS channel comprises a first plurality of unidirectional, differential signal pairs to convey data in a first direction and a second plurality of unidirectional, differential signal pairs to convey data in a second, opposite direction (see figure 2, col. 3, lines 33-62).

In regard to claim 88, Hong and Tripathi et al. fail to teach a power supply to supply power to the computer module upon insertion into the console. However it is extremely well known in the computer art/industry to provide power from the docking station to the portable computer to prolong the battery life. Therefore OFFICIAL NOTICE is taken that it would have been obvious to a person of an ordinary skill in the art at the time the invention was made to provide password

protection as is well known in the system of Hong and Tripathi et al. in order to prolong the battery life of the portable computer when docking the docking station.

In regard to claim 59, 89, Tripathi et al. disclose wherein the console comprises a coupling site and a multi-port, serial communication hub controller, and the computer module comprises a serial communication controller to communicate, via a point-to-point link, with the multi-port, serial communication hub controller through the coupling site of the console (see col. 3, lines 19-27).

In regard to claim 77, 92, Tripathi et al. disclose wherein the main memory is coupled to the processing unit through the first peripheral bridge (see figure 1A, col. 3, lines 19-27).

In regard to claims 78, 93, Tripathi et al. disclose further a mass storage device coupled to the second peripheral bridge (see figure 1A).

In regard to claim 96, Tripathi et al. disclose wherein the first peripheral bridge comprises an interface controller integrated with the north bridge (see figure 1A), the interface controller is configured to output an encoded serial bit stream of PCI bus transaction, and the first LVDS channel extends from the interface controller to convey the encoded serial bit stream of PCI bus transaction (see col. 4, lines 25-49).

Response to Arguments

7. In view of amendment and remark filed on January 27, 2012, claims 44-96 have been fully considered but they are not deemed to be persuasive.

With regard to claim 44, Applicants argue that "[t]he patent to Tripathi et al. neither shows nor suggests this aspect of the invention as set forth in Claim 44 (i.e. the central processing unit and a peripheral bridge to communicate serial bits of PCI bus transaction, the peripheral bridge "*directly*" coupled to the central

processing unit “*without any intervening PCI bus*”). The Examiner disagrees. Tripathi et al. apparently relates the north bridge and the interface controller are coupled to the central processing unit without any intervening PCI bus (see col. 3, lines 19-27). From figure 1A, Tripathi et al. teach the CPU is coupled to the front side (or host) bus 46 and then coupled to the north bridge (which, as Tripathi states, replaces the memory and I/O hub shown in Fig 1A). The PCI bus does not intervene between the CPU and the north bridge.

Claim 53 is rejected for at least the same reason as stated above for claim 44.

With regard to claim 74, Applicants argue that “[t]he patent to Tripathi et al. neither shows nor suggests this aspect of the invention as set forth in Claim 74 (i.e. the central processing unit comprises an interface that transmits and receives serial bits of PCI bus transaction and therefore, the claimed interface is part of, or is integrated with, the central processing unit). The Examiner disagrees. Tripathi et al. apparently relates interface controller is integrated with north bridge: (1) an interface controller: “serial link controller 20” coupled to “bus 22” (see figure 1A); (2) the serial link controller is coupled and integrated with the north bridge: “an I/O hub 28 that includes bridge controller for the bus 22 as well as for expansion bus 34” (see col. 3, lines 2-4). Accordingly, Tripathi discloses that the I/O hub is integrated with the serial link controller via the system bus 22 and that the I/O hub could be replaced with a north bridge (see col. 3, lines 19-27).

Claims 83, 90, 97, 109 are rejected for at least the same reason as stated above for claim 74.

With regard to claim 88, the rejection is maintained. The examiner submits a reference that teaches the console to supply power to a computer module (i.e. Gallagher (Pat No. 6,157,534)).

Allowable Subject Matter

8. Claims 97-108 are allowable over the prior of records.
9. Claim 110 is objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Conclusion

10. Claims 44, 50-54, 55, 59, 74, 76-79, 83-86, 88-94, 96, 109, 111 are rejected. Claims 97-108 are allowed. Claim 110 is objected. Claims 45-49, 56-58, 60-73, 75, 80-82, 87, 95 are canceled.

11. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 C.F.R. § 1.136(a).

A SHORTENED STATUTORY PERIOD FOR RESPONSE TO THIS FINAL ACTION IS SET TO EXPIRE THREE MONTHS FROM THE DATE OF THIS ACTION. IN THE EVENT A FIRST RESPONSE IS FILED WITHIN TWO MONTHS OF THE MAILING DATE OF THIS FINAL ACTION AND THE ADVISORY ACTION IS NOT MAILED UNTIL AFTER THE END OF THE THREE-MONTH SHORTENED STATUTORY PERIOD, THEN THE SHORTENED STATUTORY PERIOD WILL EXPIRE ON THE DATE THE ADVISORY ACTION IS MAILED, AND ANY EXTENSION FEE PURSUANT TO 37 C.F.R. § 1.136(a) WILL BE CALCULATED FROM THE MAILING DATE OF THE ADVISORY ACTION. IN NO EVENT WILL THE STATUTORY PERIOD FOR RESPONSE EXPIRE LATER THAN SIX MONTHS FROM THE DATE OF THIS FINAL ACTION.

12. Any inquiry concerning this communication or earlier communications from the examiner should be directed to examiner Raymond Phan, whose telephone number is (571) 272-3630. The examiner can normally be reached on Monday-Friday from 6:30AM- 4:00PM. The Group Fax No. (571) 273-8300.

Communications via Internet e-mail regarding this application, other than those under 35 U.S.C. 132 or which otherwise require a signature, may be used by the applicant and should be addressed to [raymond.phan@uspto.gov].

All Internet e-mail communications will be made of record in the application file. PTO employees do not engage in Internet communications where there exists a possibility that sensitive information could be identified or exchanged unless the record includes a properly signed express waiver of the confidentiality requirements of 35 U.S.C. 122. This is more clearly set forth in the Interim Internet Usage Policy published in the Official Gazette of the Patent and Trademark on February 25, 1997 at 1195 OG 89.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see [hop://pair-direct.uspto.gov](http://pair-direct.uspto.gov). Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Application/Control Number: 13/087,912

Page 9

Art Unit: 2111

Any inquiry of a general nature or relating to the status of this application should be directed to the TC 2100 central telephone number is (571) 272-2100.

/RAYMOND N PHAN/

Primary Examiner, Art Unit 2111

Notice of References Cited	Application/Control No. 13/087,912	Applicant(s)/Patent Under Reexamination CHU, WILLIAM W.Y.	
	Examiner RAYMOND PHAN	Art Unit 2111	Page 1 of 1

U.S. PATENT DOCUMENTS

*		Document Number Country Code-Number-Kind Code	Date MM-YYYY	Name	Classification
*	A	US-6,157,534	12-2000	Gallagher et al.	361/724
	B	US-			
	C	US-			
	D	US-			
	E	US-			
	F	US-			
	G	US-			
	H	US-			
	I	US-			
	J	US-			
	K	US-			
	L	US-			
	M	US-			

FOREIGN PATENT DOCUMENTS

*		Document Number Country Code-Number-Kind Code	Date MM-YYYY	Country	Name	Classification
	N					
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	P					
	Q					
	R					
	S					
	T					

NON-PATENT DOCUMENTS

*		Include as applicable: Author, Title Date, Publisher, Edition or Volume, Pertinent Pages)
	U	
	V	
	W	
	X	

*A copy of this reference is not being furnished with this Office action. (See MPEP § 707.05(a).)
Dates in MM-YYYY format are publication dates. Classifications may be US or foreign.

<i>Index of Claims</i> 	Application/Control No. 13087912	Applicant(s)/Patent Under Reexamination CHU, WILLIAM W.Y.
	Examiner RAYMOND PHAN	Art Unit 2111

✓	Rejected	-	Cancelled	N	Non-Elected	A	Appeal
=	Allowed	÷	Restricted	I	Interference	O	Objected

☐ Claims renumbered in the same order as presented by applicant				☐ CPA		☐ T.D.		☐ R.1.47	
CLAIM		DATE							
Final	Original	09/06/2011	03/09/2012						
	1	-	-						
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<i>Index of Claims</i> 	Application/Control No. 13087912	Applicant(s)/Patent Under Reexamination CHU, WILLIAM W.Y.
	Examiner RAYMOND PHAN	Art Unit 2111

✓	Rejected	-	Cancelled	N	Non-Elected	A	Appeal
=	Allowed	÷	Restricted	I	Interference	O	Objected

☐ Claims renumbered in the same order as presented by applicant				☐ CPA		☐ T.D.		☐ R.1.47	
CLAIM		DATE							
Final	Original	09/06/2011	03/09/2012						
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	42	-	-						
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	44	✓	✓						
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Index of Claims 	Application/Control No. 13087912	Applicant(s)/Patent Under Reexamination CHU, WILLIAM W.Y.
	Examiner RAYMOND PHAN	Art Unit 2111

✓	Rejected	-	Cancelled	N	Non-Elected	A	Appeal
=	Allowed	÷	Restricted	I	Interference	O	Objected

☐ Claims renumbered in the same order as presented by applicant				☐ CPA		☐ T.D.		☐ R.1.47	
CLAIM		DATE							
Final	Original	09/06/2011	03/09/2012						
	73	✓	-						
	74	✓	✓						
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	76	✓	✓						
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<i>Index of Claims</i> 	Application/Control No. 13087912	Applicant(s)/Patent Under Reexamination CHU, WILLIAM W.Y.
	Examiner RAYMOND PHAN	Art Unit 2111

✓	Rejected	-	Cancelled	N	Non-Elected	A	Appeal
=	Allowed	÷	Restricted	I	Interference	O	Objected

☐ Claims renumbered in the same order as presented by applicant				☐ CPA		☐ T.D.		☐ R.1.47	
CLAIM		DATE							
Final	Original	09/06/2011	03/09/2012						
	109		✓						
	110		○						
	111		✓						

Search Notes 	Application/Control No. 13087912	Applicant(s)/Patent Under Reexamination CHU, WILLIAM W.Y.
	Examiner RAYMOND PHAN	Art Unit 2111

SEARCHED			
Class	Subclass	Date	Examiner
710	104-119,62-64,72-73,8-19,300-317	9/5/11	RP
710	104-119,62-64,72-74,8-19,300-317	03/02/12	RP

SEARCH NOTES		
Search Notes	Date	Examiner
PALM SEARCH FOR DOUBLE PATENTING	9/1/11	RP

INTERFERENCE SEARCH			
Class	Subclass	Date	Examiner

	/RAYMOND PHAN/ Primary Examiner.Art Unit 2111

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of: William W. Y. Chu Confirmation No.: 7269
Serial No.: 13/087,912 Group Art Unit: 2111
Filed: April 15, 2011 Examiner: Phan, Raymond Ngan
For: COMPUTER SYSTEM INCLUDING PERIPHERAL BRIDGE TO COMMUNICATE
SERIAL BITS OF PERIPHERAL COMPONENT INTERCONNECT BUS
TRANSACTION AND LOW VOLTAGE DIFFERENTIAL SIGNAL CHANNEL TO
CONVEY THE SERIAL BITS (AS AMENDED)

Mail Stop Amendment
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

AMENDMENT/RESPONSE TO OFFICE ACTION

In response to the Office Action dated March 13, 2012, please amend the above-identified patent application in the following manner:

Amendments to the Claims are reflected on the listing of the claims which begins on page 2.

Remarks/Arguments begin on page 6.

IN THE CLAIMS

1-96. (Cancelled)

97. (Previously Presented) A modular computer system comprising:

a modular computer comprising

a connector configured to couple to a console;

a first low voltage differential signal (LVDS) channel comprising at least two sets of unidirectional, multiple serial bit channels to convey data in opposite directions;

an integrated central processing unit and graphics controller configured as a single chip, the integrated central processing unit and graphics controller comprising an interface directly coupled to the first LVDS channel to communicate encoded address and data bits of Peripheral Component Interconnect (PCI) bus transaction in serial form over the first LVDS channel; and

a system memory directly coupled to the integrated central processing unit and graphics controller,

wherein the connector is configured to convey the encoded address and data bits of PCI bus transaction in serial form to the console upon coupling the connector to the console.

98. (Previously Presented) The modular computer system of claim 97, further comprising a second LVDS channel coupled to the integrated central processing unit and graphics controller to convey digital video data.

99. (Previously Presented) The modular computer system of claim 98, wherein the connector is coupled to the integrated central processing unit and graphics controller through the second LVDS channel, and the connector is configured to convey the digital video data to the console upon coupling the connector to the console.

100. (Previously Presented) The modular computer system of claim 99, further comprising the console, the console comprises a LCD display, and the console is configured to receive the

digital video data from the integrated central processing unit and graphics controller through the second LVDS channel and the connector.

101. (Previously Presented) The modular computer system of claim 97, further comprising the console, and the console comprises an interface controller that is configured to couple to the connector for communication of the encoded address and data bits of PCI bus transaction in serial form.

102. (Previously Presented) The modular computer system of claim 101, wherein the console comprises a mass storage device coupled to the interface controller.

103. (Previously Presented) A modular computer system comprising:
a modular computer comprising
a connector configured to couple to a console;
a first low voltage differential signal (LVDS) channel comprising at least two sets of unidirectional, multiple serial bit channels to convey data in opposite directions;
an integrated central processing unit and graphics controller configured as a single chip;
a peripheral bridge directly coupled to the integrated central processing unit and graphics controller without any intervening Peripheral Component Interconnect (PCI) bus, the peripheral bridge directly coupled to the first LVDS channel to communicate encoded address and data bits of PCI bus transaction in serial form over the first LVDS channel; and
a system memory directly coupled to the integrated central processing unit and graphics controller,
wherein the connector is configured to convey the encoded address and data bits of PCI bus transaction in serial form to the console upon coupling the connector to the console.

104. (Previously Presented) The modular computer system of claim 103, further comprising a second LVDS channel coupled to the integrated central processing unit and graphics controller to convey digital video data.

105. (Previously Presented) The modular computer system of claim 104, wherein the connector is coupled to the integrated central processing unit and graphics controller through the second LVDS channel, and the connector is configured to convey the digital video data to the console upon coupling the connector to the console.

106. (Previously Presented) The modular computer system of claim 105, further comprising the console, the console comprises a LCD display, and the console is configured to receive the digital video data from the integrated central processing unit and graphics controller through the second LVDS channel and the connector.

107. (Previously Presented) The modular computer system of claim 103, further comprising the console, and the console comprises an interface controller that is configured to couple to the connector for communication of the encoded address and data bits of PCI bus transaction in serial form.

108. (Previously Presented) The modular computer system of claim 107, wherein the console comprises a mass storage device coupled to the interface controller.

109. (Currently Amended) A computer system comprising:

- a first low voltage differential signal (LVDS) channel comprising at least two sets of unidirectional, multiple serial bit channels to convey data in opposite directions;

- a central processing unit comprising a peripheral controller integrated with the central processing unit as a single chip, the peripheral controller directly coupled to the first LVDS channel to communicate encoded address and data bits of Peripheral Component Interconnect (PCI) bus transaction in serial form over the first LVDS channel;

- a system memory directly coupled to the central processing unit; and

- a mass storage device coupled to the central processing unit;

wherein the central processing unit comprises a graphics controller integrated in the single chip, and further comprising a second LVDS channel directly coupled to the graphics controller in the single chip to convey digital video data.

110. (Cancelled)

111. (Previously Presented) The computer system of claim 109, further comprising an enclosure with a connector, and the connector is coupled to the first LVDS channel to convey the encoded address and data bits of PCI bus transaction in LVDS form.

REMARKS

Rejected claims 44, 50-55, 59, 74, 76-79, 83-86, 88-94 and 96 are cancelled, without prejudice, to place the application in a condition for allowance. Claims 97-108 are allowed. Claim 110 is object to. The limitations of claim 110 have been added to claim 109; consequently, claim 110 is cancelled. Claim 109 is now allowable, as is its dependent claim 111. In sum, all pending claims are in a condition for allowance.

The Director is hereby authorized to charge any appropriate fees under 37 C.F.R. §§1.16, 1.17, and 1.21 that may be required by this paper, and to credit any overpayment, to Deposit Account No. 50-1283.

Date: April 4, 2012

Customer No. 58249
COOLEY LLP
777 6th Street NW, Suite 1100
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Respectfully submitted,
COOLEY LLP


By: _____
William S. Galliani
Reg. No. 33,885

Electronic Acknowledgement Receipt	
EFS ID:	12492001
Application Number:	13087912
International Application Number:	
Confirmation Number:	7269
Title of Invention:	MULTIPLE MODULE COMPUTER SYSTEM AND METHOD INCLUDING DIFFERENTIAL SIGNAL CHANNEL COMPRISING UNIDIRECTIONAL SERIAL BIT CHANNELS
First Named Inventor/Applicant Name:	William W.Y. Chu
Customer Number:	58249
Filer:	William S. Galliani/Bobbie Jutras
Filer Authorized By:	William S. Galliani
Attorney Docket Number:	ACQI-010/19US 310578-2066
Receipt Date:	06-APR-2012
Filing Date:	15-APR-2011
Time Stamp:	20:05:15
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	no

File Listing:

Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1		ACQI-010-19US_04-06-12_Ame ndment.pdf	59003 b312da06671c2ddd1671da6e980661707a 4e8f39	yes	6

	Multipart Description/PDF files in .zip description		
	Document Description	Start	End
	Amendment After Final	1	1
	Claims	2	5
	Applicant Arguments/Remarks Made in an Amendment	6	6
Warnings:			
Information:			
Total Files Size (in bytes):		59003	
This Acknowledgement Receipt evidences receipt on the noted date by the USPTO of the indicated documents, characterized by the applicant, and including page counts, where applicable. It serves as evidence of receipt similar to a Post Card, as described in MPEP 503. <u>New Applications Under 35 U.S.C. 111</u> If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application. <u>National Stage of an International Application under 35 U.S.C. 371</u> If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course. <u>New International Application Filed with the USPTO as a Receiving Office</u> If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.			

Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it displays a valid OMB control number.

PATENT APPLICATION FEE DETERMINATION RECORD Substitute for Form PTO-875					Application or Docket Number 13/087,912		Filing Date 04/15/2011		☐ To be Mailed			
APPLICATION AS FILED – PART I												
(Column 1)			(Column 2)		SMALL ENTITY ☐		OR		OTHER THAN SMALL ENTITY			
FOR	NUMBER FILED	NUMBER EXTRA	RATE (\$)	FEE (\$)			RATE (\$)	FEE (\$)				
☐ BASIC FEE (37 CFR 1.16(a), (b), or (c))	N/A	N/A	N/A				N/A					
☐ SEARCH FEE (37 CFR 1.16(k), (l), or (m))	N/A	N/A	N/A				N/A					
☐ EXAMINATION FEE (37 CFR 1.16(o), (p), or (q))	N/A	N/A	N/A				N/A					
TOTAL CLAIMS (37 CFR 1.16(i))	minus 20 =	*	X \$	=			OR	X \$	=			
INDEPENDENT CLAIMS (37 CFR 1.16(h))	minus 3 =	*	X \$	=				X \$	=			
☐ APPLICATION SIZE FEE (37 CFR 1.16(s))	If the specification and drawings exceed 100 sheets of paper, the application size fee due is \$250 (\$125 for small entity) for each additional 50 sheets or fraction thereof. See 35 U.S.C. 41(a)(1)(G) and 37 CFR 1.16(s).											
☐ MULTIPLE DEPENDENT CLAIM PRESENT (37 CFR 1.16(j))												
* If the difference in column 1 is less than zero, enter "0" in column 2.												
APPLICATION AS AMENDED – PART II										TOTAL		
(Column 1)			(Column 2)		(Column 3)		SMALL ENTITY		OR		OTHER THAN SMALL ENTITY	
AMENDMENT	04/06/2012	CLAIMS REMAINING AFTER AMENDMENT	MINUS	HIGHEST NUMBER PREVIOUSLY PAID FOR	PRESENT EXTRA	RATE (\$)	ADDITIONAL FEE (\$)			RATE (\$)	ADDITIONAL FEE (\$)	
	Total (37 CFR 1.16(i))	* 14	Minus	** 20	= 0	X \$	=			OR	X \$60=	0
	Independent (37 CFR 1.16(h))	* 3	Minus	***3	= 0	X \$	=			OR	X \$250=	0
	☐ Application Size Fee (37 CFR 1.16(s))											
	☐ FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))											
						TOTAL ADD'L FEE				OR	TOTAL ADD'L FEE	0
(Column 1)			(Column 2)		(Column 3)		SMALL ENTITY		OR		OTHER THAN SMALL ENTITY	
AMENDMENT	CLAIMS REMAINING AFTER AMENDMENT	MINUS	HIGHEST NUMBER PREVIOUSLY PAID FOR	PRESENT EXTRA	RATE (\$)	ADDITIONAL FEE (\$)			RATE (\$)	ADDITIONAL FEE (\$)		
	Total (37 CFR 1.16(i))	*	Minus	**	=	X \$	=			OR	X \$	=
	Independent (37 CFR 1.16(h))	*	Minus	***	=	X \$	=			OR	X \$	=
	☐ Application Size Fee (37 CFR 1.16(s))											
	☐ FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))											
						TOTAL ADD'L FEE				OR	TOTAL ADD'L FEE	
* If the entry in column 1 is less than the entry in column 2, write "0" in column 3. ** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 20, enter "20". *** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 3, enter "3". The "Highest Number Previously Paid For" (Total or Independent) is the highest number found in the appropriate box in column 1.												

This collection of information is required by 37 CFR 1.16. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 12 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

If you need assistance in completing the form, call 1-800-PTO-9199 and select option 2.

Legal Instrument Examiner:
/SHEILA CHAPMAN/



UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

NOTICE OF ALLOWANCE AND FEE(S) DUE

58249 7590 04/23/2012
COOLEY LLP
ATTN: Patent Group
Suite 1100
777 - 6th Street, NW
WASHINGTON, DC 20001

EXAMINER

PHAN, RAYMOND NGAN

ART UNIT

PAPER NUMBER

2111

DATE MAILED: 04/23/2012

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
13/087,912	04/15/2011	William W.Y. Chu	ACQI-010/19US 310578-2066	7269

TITLE OF INVENTION: COMPUTER SYSTEM INCLUDING PERIPHERAL BRIDGE TO COMMUNICATE SERIAL BITS OF PERIPHERAL COMPONENT INTERCONNECT BUS TRANSACTION AND LOW VOLTAGE DIFFERENTIAL SIGNAL CHANNEL TO CONVEY THE SERIAL BITS

APPLN. TYPE	SMALL ENTITY	ISSUE FEE DUE	PUBLICATION FEE DUE	PREV. PAID ISSUE FEE	TOTAL FEE(S) DUE	DATE DUE
nonprovisional	NO	\$1740	\$300	\$0	\$2040	07/23/2012

THE APPLICATION IDENTIFIED ABOVE HAS BEEN EXAMINED AND IS ALLOWED FOR ISSUANCE AS A PATENT. PROSECUTION ON THE MERITS IS CLOSED. THIS NOTICE OF ALLOWANCE IS NOT A GRANT OF PATENT RIGHTS. THIS APPLICATION IS SUBJECT TO WITHDRAWAL FROM ISSUE AT THE INITIATIVE OF THE OFFICE OR UPON PETITION BY THE APPLICANT. SEE 37 CFR 1.313 AND MPEP 1308.

THE ISSUE FEE AND PUBLICATION FEE (IF REQUIRED) MUST BE PAID WITHIN THREE MONTHS FROM THE MAILING DATE OF THIS NOTICE OR THIS APPLICATION SHALL BE REGARDED AS ABANDONED. THIS STATUTORY PERIOD CANNOT BE EXTENDED. SEE 35 U.S.C. 151. THE ISSUE FEE DUE INDICATED ABOVE DOES NOT REFLECT A CREDIT FOR ANY PREVIOUSLY PAID ISSUE FEE IN THIS APPLICATION. IF AN ISSUE FEE HAS PREVIOUSLY BEEN PAID IN THIS APPLICATION (AS SHOWN ABOVE), THE RETURN OF PART B OF THIS FORM WILL BE CONSIDERED A REQUEST TO REAPPLY THE PREVIOUSLY PAID ISSUE FEE TOWARD THE ISSUE FEE NOW DUE.

HOW TO REPLY TO THIS NOTICE:

I. Review the SMALL ENTITY status shown above.

If the SMALL ENTITY is shown as YES, verify your current SMALL ENTITY status:

A. If the status is the same, pay the TOTAL FEE(S) DUE shown above.

B. If the status above is to be removed, check box 5b on Part B - Fee(s) Transmittal and pay the PUBLICATION FEE (if required) and twice the amount of the ISSUE FEE shown above, or

If the SMALL ENTITY is shown as NO:

A. Pay TOTAL FEE(S) DUE shown above, or

B. If applicant claimed SMALL ENTITY status before, or is now claiming SMALL ENTITY status, check box 5a on Part B - Fee(s) Transmittal and pay the PUBLICATION FEE (if required) and 1/2 the ISSUE FEE shown above.

II. PART B - FEE(S) TRANSMITTAL, or its equivalent, must be completed and returned to the United States Patent and Trademark Office (USPTO) with your ISSUE FEE and PUBLICATION FEE (if required). If you are charging the fee(s) to your deposit account, section "4b" of Part B - Fee(s) Transmittal should be completed and an extra copy of the form should be submitted. If an equivalent of Part B is filed, a request to reapply a previously paid issue fee must be clearly made, and delays in processing may occur due to the difficulty in recognizing the paper as an equivalent of Part B.

III. All communications regarding this application must give the application number. Please direct all communications prior to issuance to Mail Stop ISSUE FEE unless advised to the contrary.

IMPORTANT REMINDER: Utility patents issuing on applications filed on or after Dec. 12, 1980 may require payment of maintenance fees. It is patentee's responsibility to ensure timely payment of maintenance fees when due.

PART B - FEE(S) TRANSMITTAL

Complete and send this form, together with applicable fee(s), to: **Mail** Mail Stop ISSUE FEE
Commissioner for Patents
P.O. Box 1450
Alexandria, Virginia 22313-1450
or Fax (571)-273-2885

INSTRUCTIONS: This form should be used for transmitting the ISSUE FEE and PUBLICATION FEE (if required). Blocks 1 through 5 should be completed where appropriate. All further correspondence including the Patent, advance orders and notification of maintenance fees will be mailed to the current correspondence address as indicated unless corrected below or directed otherwise in Block 1, by (a) specifying a new correspondence address; and/or (b) indicating a separate "FEE ADDRESS" for maintenance fee notifications.

CURRENT CORRESPONDENCE ADDRESS (Note: Use Block 1 for any change of address)

58249 7590 04/23/2012
COOLEY LLP
ATTN: Patent Group
Suite 1100
777 - 6th Street, NW
WASHINGTON, DC 20001

Note: A certificate of mailing can only be used for domestic mailings of the Fee(s) Transmittal. This certificate cannot be used for any other accompanying papers. Each additional paper, such as an assignment or formal drawing, must have its own certificate of mailing or transmission.

Certificate of Mailing or Transmission

I hereby certify that this Fee(s) Transmittal is being deposited with the United States Postal Service with sufficient postage for first class mail in an envelope addressed to the Mail Stop ISSUE FEE address above, or being facsimile transmitted to the USPTO (571) 273-2885, on the date indicated below.

(Depositor's name)
(Signature)
(Date)

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
13/087,912	04/15/2011	William W.Y. Chu	ACQI-010/19US 310578-2066	7269

TITLE OF INVENTION: COMPUTER SYSTEM INCLUDING PERIPHERAL BRIDGE TO COMMUNICATE SERIAL BITS OF PERIPHERAL COMPONENT INTERCONNECT BUS TRANSACTION AND LOW VOLTAGE DIFFERENTIAL SIGNAL CHANNEL TO CONVEY THE SERIAL BITS

APPLN. TYPE	SMALL ENTITY	ISSUE FEE DUE	PUBLICATION FEE DUE	PREV. PAID ISSUE FEE	TOTAL FEE(S) DUE	DATE DUE
nonprovisional	NO	\$1740	\$300	\$0	\$2040	07/23/2012

EXAMINER	ART UNIT	CLASS-SUBCLASS
PHAN, RAYMOND NGAN	2111	710-313000

1. Change of correspondence address or indication of "Fee Address" (37 CFR 1.363).
☐ Change of correspondence address (or Change of Correspondence Address form PTO/SB/122) attached.
☐ "Fee Address" indication (or "Fee Address" Indication form PTO/SB/47; Rev 03-02 or more recent) attached. **Use of a Customer Number is required.**

2. For printing on the patent front page, list
(1) the names of up to 3 registered patent attorneys or agents OR, alternatively, 1 _____
(2) the name of a single firm (having as a member a registered attorney or agent) and the names of up to 2 registered patent attorneys or agents. If no name is listed, no name will be printed. 2 _____
3 _____

3. ASSIGNEE NAME AND RESIDENCE DATA TO BE PRINTED ON THE PATENT (print or type)

PLEASE NOTE: Unless an assignee is identified below, no assignee data will appear on the patent. If an assignee is identified below, the document has been filed for recordation as set forth in 37 CFR 3.11. Completion of this form is NOT a substitute for filing an assignment.

(A) NAME OF ASSIGNEE

(B) RESIDENCE: (CITY and STATE OR COUNTRY)

Please check the appropriate assignee category or categories (will not be printed on the patent) : ☐ Individual ☐ Corporation or other private group entity ☐ Government

4a. The following fee(s) are submitted:

☐ Issue Fee
☐ Publication Fee (No small entity discount permitted)
☐ Advance Order - # of Copies _____

4b. Payment of Fee(s): (Please first reapply any previously paid issue fee shown above)

☐ A check is enclosed.
☐ Payment by credit card. Form PTO-2038 is attached.
☐ The Director is hereby authorized to charge the required fee(s), any deficiency, or credit any overpayment, to Deposit Account Number _____ (enclose an extra copy of this form).

5. Change in Entity Status (from status indicated above)

☐ a. Applicant claims SMALL ENTITY status. See 37 CFR 1.27. ☐ b. Applicant is no longer claiming SMALL ENTITY status. See 37 CFR 1.27(g)(2).

NOTE: The Issue Fee and Publication Fee (if required) will not be accepted from anyone other than the applicant; a registered attorney or agent; or the assignee or other party in interest as shown by the records of the United States Patent and Trademark Office.

Authorized Signature _____

Date _____

Typed or printed name _____

Registration No. _____

This collection of information is required by 37 CFR 1.311. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 12 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, Virginia 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, Virginia 22313-1450.

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UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
13/087,912	04/15/2011	William W.Y. Chu	ACQI-010/19US 310578-2066	7269
58249	7590	04/23/2012	EXAMINER PHAN, RAYMOND NGAN	
COOLEY LLP ATTN: Patent Group Suite 1100 777 - 6th Street, NW WASHINGTON, DC 20001			ART UNIT 2111	
			PAPER NUMBER	

DATE MAILED: 04/23/2012

Determination of Patent Term Adjustment under 35 U.S.C. 154 (b)

(application filed on or after May 29, 2000)

The Patent Term Adjustment to date is 0 day(s). If the issue fee is paid on the date that is three months after the mailing date of this notice and the patent issues on the Tuesday before the date that is 28 weeks (six and a half months) after the mailing date of this notice, the Patent Term Adjustment will be 0 day(s).

If a Continued Prosecution Application (CPA) was filed in the above-identified application, the filing date that determines Patent Term Adjustment is the filing date of the most recent CPA.

Applicant will be able to obtain more detailed information by accessing the Patent Application Information Retrieval (PAIR) WEB site (<http://pair.uspto.gov>).

Any questions regarding the Patent Term Extension or Adjustment determination should be directed to the Office of Patent Legal Administration at (571)-272-7702. Questions relating to issue and publication fee payments should be directed to the Customer Service Center of the Office of Patent Publication at 1-(888)-786-0101 or (571)-272-4200.

Privacy Act Statement

The Privacy Act of 1974 (P.L. 93-579) requires that you be given certain information in connection with your submission of the attached form related to a patent application or patent. Accordingly, pursuant to the requirements of the Act, please be advised that: (1) the general authority for the collection of this information is 35 U.S.C. 2(b)(2); (2) furnishing of the information solicited is voluntary; and (3) the principal purpose for which the information is used by the U.S. Patent and Trademark Office is to process and/or examine your submission related to a patent application or patent. If you do not furnish the requested information, the U.S. Patent and Trademark Office may not be able to process and/or examine your submission, which may result in termination of proceedings or abandonment of the application or expiration of the patent.

The information provided by you in this form will be subject to the following routine uses:

1. The information on this form will be treated confidentially to the extent allowed under the Freedom of Information Act (5 U.S.C. 552) and the Privacy Act (5 U.S.C. 552a). Records from this system of records may be disclosed to the Department of Justice to determine whether disclosure of these records is required by the Freedom of Information Act.
2. A record from this system of records may be disclosed, as a routine use, in the course of presenting evidence to a court, magistrate, or administrative tribunal, including disclosures to opposing counsel in the course of settlement negotiations.
3. A record in this system of records may be disclosed, as a routine use, to a Member of Congress submitting a request involving an individual, to whom the record pertains, when the individual has requested assistance from the Member with respect to the subject matter of the record.
4. A record in this system of records may be disclosed, as a routine use, to a contractor of the Agency having need for the information in order to perform a contract. Recipients of information shall be required to comply with the requirements of the Privacy Act of 1974, as amended, pursuant to 5 U.S.C. 552a(m).
5. A record related to an International Application filed under the Patent Cooperation Treaty in this system of records may be disclosed, as a routine use, to the International Bureau of the World Intellectual Property Organization, pursuant to the Patent Cooperation Treaty.
6. A record in this system of records may be disclosed, as a routine use, to another federal agency for purposes of National Security review (35 U.S.C. 181) and for review pursuant to the Atomic Energy Act (42 U.S.C. 218(c)).
7. A record from this system of records may be disclosed, as a routine use, to the Administrator, General Services, or his/her designee, during an inspection of records conducted by GSA as part of that agency's responsibility to recommend improvements in records management practices and programs, under authority of 44 U.S.C. 2904 and 2906. Such disclosure shall be made in accordance with the GSA regulations governing inspection of records for this purpose, and any other relevant (i.e., GSA or Commerce) directive. Such disclosure shall not be used to make determinations about individuals.
8. A record from this system of records may be disclosed, as a routine use, to the public after either publication of the application pursuant to 35 U.S.C. 122(b) or issuance of a patent pursuant to 35 U.S.C. 151. Further, a record may be disclosed, subject to the limitations of 37 CFR 1.14, as a routine use, to the public if the record was filed in an application which became abandoned or in which the proceedings were terminated and which application is referenced by either a published application, an application open to public inspection or an issued patent.
9. A record from this system of records may be disclosed, as a routine use, to a Federal, State, or local law enforcement agency, if the USPTO becomes aware of a violation or potential violation of law or regulation.

Notice of Allowability	Application No.	Applicant(s)	
	13/087,912	CHU, WILLIAM W.Y.	
	Examiner	Art Unit	
	RAYMOND PHAN	2111	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address--

All claims being allowable, PROSECUTION ON THE MERITS IS (OR REMAINS) CLOSED in this application. If not included herewith (or previously mailed), a Notice of Allowance (PTOL-85) or other appropriate communication will be mailed in due course. **THIS NOTICE OF ALLOWABILITY IS NOT A GRANT OF PATENT RIGHTS.** This application is subject to withdrawal from issue at the initiative of the Office or upon petition by the applicant. See 37 CFR 1.313 and MPEP 1308.

1. ☒ This communication is responsive to the Amendment After Final filed on April 6, 2012.
2. ☐ An election was made by the applicant in response to a restriction requirement set forth during the interview on ____; the restriction requirement and election have been incorporated into this action.
3. ☒ The allowed claim(s) is/are 97-109, 111.
4. ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
 - a) ☐ All b) ☐ Some* c) ☐ None of the:
 1. ☐ Certified copies of the priority documents have been received.
 2. ☐ Certified copies of the priority documents have been received in Application No. ____.
 3. ☐ Copies of the certified copies of the priority documents have been received in this national stage application from the International Bureau (PCT Rule 17.2(a)).
 - * Certified copies not received: ____.

Applicant has **THREE MONTHS FROM THE "MAILING DATE"** of this communication to file a reply complying with the requirements noted below. Failure to timely comply will result in ABANDONMENT of this application.
THIS THREE-MONTH PERIOD IS NOT EXTENDABLE.

5. ☐ A SUBSTITUTE OATH OR DECLARATION must be submitted. Note the attached EXAMINER'S AMENDMENT or NOTICE OF INFORMAL PATENT APPLICATION (PTO-152) which gives reason(s) why the oath or declaration is deficient.
6. ☐ CORRECTED DRAWINGS (as "replacement sheets") must be submitted.
 - (a) ☐ including changes required by the Notice of Draftsperson's Patent Drawing Review (PTO-948) attached
 - 1) ☐ hereto or 2) ☐ to Paper No./Mail Date ____.
 - (b) ☐ including changes required by the attached Examiner's Amendment / Comment or in the Office action of Paper No./Mail Date ____.

Identifying indicia such as the application number (see 37 CFR 1.84(c)) should be written on the drawings in the front (not the back) of each sheet. Replacement sheet(s) should be labeled as such in the header according to 37 CFR 1.121(d).

7. ☐ DEPOSIT OF and/or INFORMATION about the deposit of BIOLOGICAL MATERIAL must be submitted. Note the attached Examiner's comment regarding REQUIREMENT FOR THE DEPOSIT OF BIOLOGICAL MATERIAL.

Attachment(s)

1. ☐ Notice of References Cited (PTO-892) 2. ☐ Notice of Draftperson's Patent Drawing Review (PTO-948) 3. ☐ Information Disclosure Statements (PTO/SB/08), Paper No./Mail Date ____ 4. ☐ Examiner's Comment Regarding Requirement for Deposit of Biological Material	5. ☐ Notice of Informal Patent Application 6. ☐ Interview Summary (PTO-413), Paper No./Mail Date ____. 7. ☐ Examiner's Amendment/Comment 8. ☐ Examiner's Statement of Reasons for Allowance 9. ☐ Other ____.

/RAYMOND N PHAN/ Primary Examiner, Art Unit 2111	

Issue Classification 	Application/Control No. 13087912	Applicant(s)/Patent Under Reexamination CHU, WILLIAM W.Y.
	Examiner RAYMOND PHAN	Art Unit 2111

ORIGINAL						INTERNATIONAL CLASSIFICATION												
CLASS		SUBCLASS				CLAIMED					NON-CLAIMED							
710		313				G	0	6	F	13 / 20 (2006.01.01)								
CROSS REFERENCE(S)																		
CLASS	SUBCLASS (ONE SUBCLASS PER BLOCK)																	
710	301	315																

☐ Claims renumbered in the same order as presented by applicant ☐ CPA ☐ T.D. ☐ R.1.47															
Final	Original	Final	Original	Final	Original	Final	Original	Final	Original	Final	Original	Final	Original	Final	Original
	1		17		33		49		65		81	1	97		
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	14		30		46		62		78		94		110		
	15		31		47		63		79		95	14	111		
	16		32		48		64		80		96				

NONE		Total Claims Allowed:	
		14	
(Assistant Examiner)	(Date)		
/RAYMOND PHAN/ Primary Examiner. Art Unit 2111	04/17/2012	O.G. Print Claim(s)	O.G. Print Figure
(Primary Examiner)	(Date)	6	1

OK TO ENTER: /R.P./

Attorney Docket No. ACQI-010/19US 310578-2066

PATENT

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of: William W. Y. Chu Confirmation No.: 7269
Serial No.: 13/087,912 Group Art Unit: 2111
Filed: April 15, 2011 Examiner: Phan, Raymond Ngan
For: COMPUTER SYSTEM INCLUDING PERIPHERAL BRIDGE TO COMMUNICATE
SERIAL BITS OF PERIPHERAL COMPONENT INTERCONNECT BUS
TRANSACTION AND LOW VOLTAGE DIFFERENTIAL SIGNAL CHANNEL TO
CONVEY THE SERIAL BITS (AS AMENDED)

Mail Stop Amendment
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

AMENDMENT/RESPONSE TO OFFICE ACTION

In response to the Office Action dated March 13, 2012, please amend the above-identified patent application in the following manner:

Amendments to the Claims are reflected on the listing of the claims which begins on page 2.

Remarks/Arguments begin on page 6.

<i>Index of Claims</i> 	Application/Control No. 13087912	Applicant(s)/Patent Under Reexamination CHU, WILLIAM W.Y.
	Examiner RAYMOND PHAN	Art Unit 2111

✓	Rejected	-	Cancelled	N	Non-Elected	A	Appeal
=	Allowed	÷	Restricted	I	Interference	O	Objected

☐ Claims renumbered in the same order as presented by applicant						☐ CPA		☐ T.D.		☐ R.1.47	
CLAIM		DATE									
Final	Original	09/06/2011	03/09/2012	04/17/2012							
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	34	-	-	-							
	35	-	-	-							
	36	-	-	-							

<i>Index of Claims</i> 	Application/Control No. 13087912	Applicant(s)/Patent Under Reexamination CHU, WILLIAM W.Y.
	Examiner RAYMOND PHAN	Art Unit 2111

✓	Rejected	-	Cancelled	N	Non-Elected	A	Appeal
=	Allowed	÷	Restricted	I	Interference	O	Objected

☐ Claims renumbered in the same order as presented by applicant						☐ CPA		☐ T.D.		☐ R.1.47	
CLAIM		DATE									
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	72	✓	-	-							

Index of Claims 	Application/Control No. 13087912	Applicant(s)/Patent Under Reexamination CHU, WILLIAM W.Y.
	Examiner RAYMOND PHAN	Art Unit 2111

✓	Rejected	-	Cancelled	N	Non-Elected	A	Appeal
=	Allowed	÷	Restricted	I	Interference	O	Objected

☐ Claims renumbered in the same order as presented by applicant						☐ CPA		☐ T.D.		☐ R.1.47	
CLAIM		DATE									
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11	106		=	=							
9	107		=	=							
12	108		=	=							

<i>Index of Claims</i> 	Application/Control No. 13087912	Applicant(s)/Patent Under Reexamination CHU, WILLIAM W.Y.
	Examiner RAYMOND PHAN	Art Unit 2111

✓	Rejected	-	Cancelled	N	Non-Elected	A	Appeal
=	Allowed	÷	Restricted	I	Interference	O	Objected

☐ Claims renumbered in the same order as presented by applicant		☐ CPA		☐ T.D.		☐ R.1.47			
CLAIM		DATE							
Final	Original	09/06/2011	03/09/2012	04/17/2012					
13	109		✓	=					
	110		○	-					
14	111		✓	=					

Search Notes 	Application/Control No. 13087912	Applicant(s)/Patent Under Reexamination CHU, WILLIAM W.Y.
	Examiner RAYMOND PHAN	Art Unit 2111

SEARCHED			
Class	Subclass	Date	Examiner
710	104-119,62-64,72-73,8-19,300-317	9/5/11	RP
710	104-119,62-64,72-74,8-19,300-317	03/02/12	RP
710	104-119,62-64,72-74,8-19,300-317	04/15/12	RP

SEARCH NOTES		
Search Notes	Date	Examiner
PALM SEARCH FOR DOUBLE PATENTING	9/1/11	RP

INTERFERENCE SEARCH			
Class	Subclass	Date	Examiner
710	313,301,315	04/17/12	RP

	/RAYMOND PHAN/ Primary Examiner.Art Unit 2111

PART B - FEE(S) TRANSMITTAL

**Complete and send this form, together with applicable fee(s), to: Mail Mail Stop ISSUE FEE
Commissioner for Patents
P.O. Box 1450
Alexandria, Virginia 22313-1450
or Fax (571) 273-2885**

INSTRUCTIONS: This form should be used for transmitting the ISSUE FEE and PUBLICATION FEE (if required). Blocks 1 through 5 should be completed where appropriate. All further correspondence including the Patent, advance orders and notification of maintenance fees will be mailed to the current correspondence address as indicated unless corrected below or directed otherwise in Block 1, by (a) specifying a new correspondence address; and/or (b) indicating a separate "FEE ADDRESS" for maintenance fee notifications.

CURRENT CORRESPONDENCE ADDRESS (Note: Use Block 1 for any change of address)

58249
COOLEY LLP
777 6th Street, NW Suite 1100
Washington, DC 20001

Note: A certificate of mailing can only be used for domestic mailings of the Fee(s) Transmittal. This certificate cannot be used for any other accompanying papers. Each additional paper, such as an assignment or formal drawing, must have its own certificate of mailing or transmission.

Certificate of Mailing or Transmission

I hereby certify that this Fee(s) Transmittal is being deposited with the United States Postal Service with sufficient postage for first class mail in an envelope addressed to the Mail Stop ISSUE FEE address above, or being facsimile transmitted to the USPTO (571) 273-2885, on the date indicated below.

(Depositor's name)
(Signature)
(Date)

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
13/087,912	04/15/2011	William W. Y. Chu	ACQI-010/19US 310578-2066	7269

TITLE OF INVENTION: COMPUTER SYSTEM INCLUDING PERIPHERAL BRIDGE TO COMMUNICATE SERIAL BITS OF PERIPHERAL COMPONENT INTERCONNECT BUS TRANSACTION AND LOW VOLTAGE DIFFERENTIAL SIGNAL CHANNEL TO CONVEY THE SERIAL BITS

APPLN. TYPE	SMALL ENTITY	ISSUE FEE	PUBLICATION FEE	TOTAL FEE(S) DUE	DATE DUE
nonprovisional	NO	\$1740	\$300	\$2040	07/23/2012

EXAMINER	ART UNIT	CLASS-SUBCLASS
PHAN, RAYMOND NGAN	2111	710-313000

1. Change of correspondence address or indication of "Fee Address" (37 CFR 1.363).

- ☐ Change of correspondence address (or Change of Correspondence Address Form PTO/SB/122) attached.
☐ "Fee Address" indication (or "Fee Address" Indication form PTO/SB/47; Rev 03-02 or more recent) attached. **Use of a Customer Number is required.**

2. For printing on the patent front page, list

- (1) the names of up to 3 registered patent attorneys or agents OR, alternatively,
(2) the name of a single firm (having as a member a registered attorney or agent) and the names of up to 2 registered patent attorneys or agents. If no name is listed, no name will be printed.

1 COOLEY LLP
2
3

3. ASSIGNEE NAME AND RESIDENCE DATA TO BE PRINTED ON THE PATENT (print or type)

PLEASE NOTE: Unless an assignee is identified below, no assignee data will appear on the patent. If an assignee is identified below, the document has been filed for recordation as set forth in 37 CFR 3.11. Completion of this form is NOT a substitute for filing an assignment.

(A) NAME OF ASSIGNEE

ACQIS LLC

(B) RESIDENCE: (CITY and STATE OR COUNTRY)

MCKINNEY, TEXAS

Please check the appropriate assignee category or categories (will not be printed on the patent): ☐ Individual ☒ Corporation or other private group entity ☐ Government

4a. The following fee(s) are enclosed:

- ☒ Issue Fee
☒ Publication Fee (No small entity discount permitted)
☐ Advance Order - # of Copies _____

4b. Payment of Fee(s):

- ☐ A check in the amount of the fee(s) is enclosed.
☐ Payment by credit card. Form PTO-2038 is attached.
☒ The Director is hereby authorized by charge the required fee(s), or credit any overpayment, to Deposit Account Number 50-1283.

5. Change in Entity Status (from status indicated above)

- ☐ a. Applicant claims SMALL ENTITY status. See 37 CFR 1.27. ☐ b. Applicant is no longer claiming SMALL ENTITY status. See 37 CFR 1.27(g)(2).

The Director of the USPTO is requested to apply the Issue Fee and Publication Fee (if any) or to re-apply any previously paid issue fee to the application identified above. NOTE: The Issue Fee and Publication Fee (if required) will not be accepted from anyone other than the applicant; a registered attorney or agent; or the assignee or other party in interest as shown by the records of the United States Patent and Trademark Office.

Authorized Signature

Date June 26, 2012

Typed or printed name William S. Galliani

Registration No. 33,885

This collection of information is required by 37 CFR 1.311. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 12 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, Virginia 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, Virginia 22313-1450.

Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it displays a valid OMB control number.

Electronic Patent Application Fee Transmittal				
Application Number:		13087912		
Filing Date:		15-Apr-2011		
Title of Invention:		COMPUTER SYSTEM INCLUDING PERIPHERAL BRIDGE TO COMMUNICATE SERIAL BITS OF PERIPHERAL COMPONENT INTERCONNECT BUS TRANSACTION AND LOW VOLTAGE DIFFERENTIAL SIGNAL CHANNEL TO CONVEY THE SERIAL BITS		
First Named Inventor/Applicant Name:		William W.Y. Chu		
Filer:		William S. Galliani/Bobbie Jutras		
Attorney Docket Number:		ACQI-010/19US 310578-2066		
Filed as Large Entity				
Utility under 35 USC 111(a) Filing Fees				
Description	Fee Code	Quantity	Amount	Sub-Total in USD(\$)
Basic Filing:				
Pages:				
Claims:				
Miscellaneous-Filing:				
Petition:				
Patent-Appeals-and-Interference:				
Post-Allowance-and-Post-Issuance:				
Utility Appl issue fee	1501	1	1740	1740
Publ. Fee- early, voluntary, or normal	1504	1	300	300

Description	Fee Code	Quantity	Amount	Sub-Total in USD(\$)
Extension-of-Time:				
Miscellaneous:				
Total in USD (\$)				2040

Electronic Acknowledgement Receipt	
EFS ID:	13113167
Application Number:	13087912
International Application Number:	
Confirmation Number:	7269
Title of Invention:	COMPUTER SYSTEM INCLUDING PERIPHERAL BRIDGE TO COMMUNICATE SERIAL BITS OF PERIPHERAL COMPONENT INTERCONNECT BUS TRANSACTION AND LOW VOLTAGE DIFFERENTIAL SIGNAL CHANNEL TO CONVEY THE SERIAL BITS
First Named Inventor/Applicant Name:	William W.Y. Chu
Customer Number:	58249
Filer:	William S. Galliani/Bobbie Jutras
Filer Authorized By:	William S. Galliani
Attorney Docket Number:	ACQI-010/19US 310578-2066
Receipt Date:	26-JUN-2012
Filing Date:	15-APR-2011
Time Stamp:	20:26:49
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	yes
Payment Type	Deposit Account
Payment was successfully received in RAM	\$ 2040
RAM confirmation Number	10826
Deposit Account	501283
Authorized User	
The Director of the USPTO is hereby authorized to charge indicated fees and credit any overpayment as follows: Charge any Additional Fees required under 37 C.F.R. Section 1.16 (National application filing, search, and examination fees) Charge any Additional Fees required under 37 C.F.R. Section 1.17 (Patent application and reexamination processing fees)	

File Listing:

Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1	Issue Fee Payment (PTO-85B)	ACQI-010-19US_06-26-12_IFP mt.pdf	79423	no	1
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Warnings:**Information:**

2	Fee Worksheet (SB06)	fee-info.pdf	32464	no	2
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Warnings:**Information:**

Total Files Size (in bytes):			111887

This Acknowledgement Receipt evidences receipt on the noted date by the USPTO of the indicated documents, characterized by the applicant, and including page counts, where applicable. It serves as evidence of receipt similar to a Post Card, as described in MPEP 503.

New Applications Under 35 U.S.C. 111

If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application.

National Stage of an International Application under 35 U.S.C. 371

If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.

New International Application Filed with the USPTO as a Receiving Office

If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.

ALL REFERENCES CONSIDERED EXCEPT WHERE LINED THROUGH. /R.P./



PTO/SB/08A (07-05)
Approved for use through 07/31/2006. OMB 0651-0031

Substitute for form 1449A/PTO INFORMATION DISCLOSURE STATEMENT BY APPLICANT (use as many sheets as necessary)		Complete if Known	
		Application Number	To be assigned 13/087,912
		Filing Date	Herewith 04/15/11
		First Named Inventor	William W.Y. Chu
		Group Art Unit	2111
Sheet	4 of 8	Examiner Name	PHAN
		Attorney Docket No.	ACQI-010/19US 310578-2066

Change(s) applied
to document
/A.J.P./
6/28/2012

U.S. PATENT DOCUMENTS					
Examiner Initials*	Cite No. ¹	Document Number	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear
		Number-Kind Code ² (if known)			
	105.	US-6,324,605 B1	11-27-2001	Rafferty et al.	
	106.	US-2009/0157939	06/18/2009	Chu	
	107.	US-5,978,919	11-1999	Doi et al.	
	108.	US-6,009,488	12-28-1999	Kavipurapu	
	109.	US-6,025,989	02-15-2000	Ayd et al.	
	110.	US-6,070,214	05-30-2000	Ahern	
	111.	US-7,099,981 B2	08-29-2006	Chu	
	112.	US-7,416,446 B2	12-05-2006	Chu 7,146,446	
	113.	US-7,328,297 B2	02-05-2008	Chu	
	114.	US-7,363,415 B2	04-22-2008	Chu	
	115.	US-7,363,416 B2	04-22-2008	Chu	
	116.	US-7,376,779 B2	05-20-2008	Chu	
	117.	US-6,161,524	12-19-2000	Akbarian et al.	
	118.	US-7,818,487	10-19-2010	Chu	
	119.	US-7,676,624	03-09-2010	Chu	

FOREIGN PATENT DOCUMENTS					
Examiner Initials*	Cite No. ¹	Foreign Patent Document	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear
		Country Code ³ Number ⁴ Kind Code ⁵ (if known)			
	1.	WO 92/18924	10-29-1992		
	2.	WO 94/00097	01-06-1994		
	3.	WO 95/13640	05-18-1995		
	4.	EP 722138A1	07-17-1996		
	5.	JP 6-289953	10-18-1994		

OTHER - NON PATENT LITERATURE DOCUMENTS			
Examiner Initials*	Cite No. ¹	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.	T ⁶
	1.	Agerwala, T. et al., "SP2 System Architecture", IBM Systems Journal, Vol. 34, No. 2 (1995)	

Examiner Signature	/Raymond Phan/	Date Considered	08/16/2011

*EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant. ¹Unique citation designation number (optional). ²See attached Kinds of U.S. Patent Documents. ³Enter Office that issued the document, by the two-letter code (WIPO Standard ST.3). ⁴For Japanese patent documents, the indication of the year of the reign of the Emperor must precede the serial number of the patent document. ⁵Kind of document by the appropriate symbols as indicated on the document under WIPO Standard ST.16 if possible. ⁶Applicant is to place a check mark here if English language Translation is attached. This collection of information is required by 37 CFR 1.97 and 1.98. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 2 hours to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.

If you need assistance in completing the form, call 1-800-PTO-9199 and select option 2.



Substitute for form 1449A/PTO INFORMATION DISCLOSURE STATEMENT BY APPLICANT <i>(use as many sheets as necessary)</i>		Complete if Known	
		Application Number	To be assigned 13/087,912
		Filing Date	Herewith 04/15/11
		First Named Inventor	William W.Y. Chu
		Group Art Unit	2111
Examiner Name	PHAN		
Sheet	2 of 8	Attorney Docket No.	ACQI-010/19US 310578-2066

U.S. PATENT DOCUMENTS					
Examiner Initials*	Cite No. ¹	Document Number	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear
		Number-Kind Code ² (if known)			
	37.	US-5,680,126	10-21-1997	Kikinis	
	38.	US-5,689,654	11-18-1997	Kikinis	
	39.	US-5,774,704	06-30-1998	Williams	
	40.	US-5,721,837	02-24-1998	Kikinis	
	41.	US-5,721,842	02-24-1998	Beasley et al.	
	42.	US-5,745,733	04-28-1998	Robinson	
	43.	US-5,752,080	05-12-1998	Ryan	
	44.	US-5,764,924	06-09-1998	Hong	
	45.	US-5,795,228	08-18-1998	Trumbull	
	46.	US-5,809,538	09-15-1998	Pollmann	
	47.	US-5,815,681	09-29-1998	Kikinis	
	48.	US-5,819,050	10-06-1998	Boehling et al.	
	49.	US-5,826,048	10-20-1998	Dempsey et al.	
	50.	US-5,848,249	12-08-1998	Garbus	
	51.	US-5,859,669	01-12-1999	Prentice	
	52.	US-5,907,566	05-25-1999	Benson et al.	
	53.	US-5,941,965	08-24-1999	Moroz	
	54.	US-5,948,047	09-07-1999	Jenkins et al.	
	55.	US-5,960,213	~~08-28-1999~~	Wilson 09/1999	
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Change(s) applied
to documents
/A.J.P./
6/28/2012

Examiner Signature	/Raymond Phan/	Date Considered	08/16/2011

*EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant. ¹Unique citation designation number (optional). ²See attached Kinds of U.S. Patent Documents. ³Enter Office that issued the document, by the two-letter code (WIPO Standard ST.3). ⁴For Japanese patent documents, the indication of the year of the reign of the Emperor must precede the serial number of the patent document. ⁵Kind of document by the appropriate symbols as indicated on the document under WIPO Standard ST.16 if possible. ⁶Applicant is to place a check mark here if English language Translation is attached. This collection of information is required by 37 CFR 1.97 and 1.98. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 2 hours to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.

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ISSUE NOTIFICATION

The projected patent number and issue date are specified above.

Determination of Patent Term Adjustment under 35 U.S.C. 154 (b) (application filed on or after May 29, 2000)

The Patent Term Adjustment is 0 day(s). Any patent to issue from the above-identified application will include an indication of the adjustment on the front page.

If a Continued Prosecution Application (CPA) was filed in the above-identified application, the filing date that determines Patent Term Adjustment is the filing date of the most recent CPA.

Applicant will be able to obtain more detailed information by accessing the Patent Application Information Retrieval (PAIR) WEB site (<http://pair.uspto.gov>).

Any questions regarding the Patent Term Extension or Adjustment determination should be directed to the Office of Patent Legal Administration at (571)-272-7702. Questions relating to issue and publication fee payments should be directed to the Application Assistance Unit (AAU) of the Office of Data Management (ODM) at (571)-272-4200.

APPLICANT(s) (Please see PAIR WEB site <http://pair.uspto.gov> for additional applicants):

William W.Y. Chu, Los Altos, CA;

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