

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

PATENT QUALITY ASSURANCE, LLC,
Petitioner,

v.

VLSI TECHNOLOGY LLC,
Patent Owner.

Case IPR2021-01229
Patent 7,523,373

PATENT OWNER'S PRELIMINARY RESPONSE

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I. INTRODUCTION

This is the third petition filed against the '373. Intel filed the first in November 2019 (IPR2020-00158) (the “Intel Petition” or “Intel’s Petition”). Intel’s Petition was rejected under *Fintiv* due to the approaching district court trial of the patent’s validity and related issues, and the parties’ and court’s investment of time and resources in that trial. *Intel Corp. v. VLSI Technology LLC*, IPR2020-00158, Paper 16, 10 (May 20, 2020). That “significant[.]” investment grew dramatically thereafter, culminating in a unanimous jury verdict on March 2, 2021 (the “Verdict”) that found infringement of VLSI’s '373 and 7,725,759 (“’759”) patents.

The Verdict did not go unnoticed and prospectors sprang from the woodwork to shake VLSI down. Just weeks later, on April 23, 2021, an entity calling itself OpenSky formed in Nevada and filed IPR2021-01056, the second petition challenging the '373 patent, largely a copy of Intel’s already rejected petition.

Taking notice of OpenSky’s petition, yet another new entity—“Patent Quality Assurance”—formed in South Dakota to file the present petition, it too a near carbon copy of Intel’s failed petition. Though inspired by OpenSky’s filing but also trailing it, PQA wasted no time in throwing OpenSky under the bus, boasting that it, unlike OpenSky, actually retained the very same experts Intel used

and that OpenSky's declarations were mere hearsay. While that is true and sufficient reason to reject the OpenSky petition, it is no reason to institute PQA's petition. By so retaining Intel's own experts, PQA is working intimately with experts who spent hours-upon-hours working with Intel's attorneys to select art and develop arguments. PQA stands in Intel's shoes even more so than OpenSky does.

Instituting trial of a follow-on to a follow-on of an already rejected petition would be a green light to prospectors—who face no threat of infringement allegations—to challenge *any* patent that is the subject of an infringement verdict. Such harassment, and piling on in this case, should not be encouraged. Indeed, PQA's Petition—the third petition and second follow-on—epitomizes the “repeated” “harassment” that Congress, the Board, and the Federal Circuit have recognized as an abuse of the IPR process.

The Board should deny institution under each of *Fintiv*, *General Plastic*, *Valve*, § 325(d), and the totality of the circumstances, and should the Board institute OpenSky's petition, that is still more reason to deny institution here. *See* Section II. And if more is needed, the Board should outright deny Petitioner's thin grounds on the merits, for at least the reasons identified in Section III.

II. THE BOARD SHOULD DENY INSTITUTION UNDER 35 U.S.C. §§ 314(a) AND 325(d).

After a brief factual background (Section II.A), Patent Owner explains why PQA’s Petition should be denied under *Fintiv* (Section II.B), *General Plastic/Valve* (Section II.C), § 325(d) (Section II.D), and the totality of the circumstances (Section II.E). Furthermore, should OpenSky’s petition be instituted, that is still more reason to deny PQA’s petition (Section II.F).

A. Factual Background.

The three petitions challenging the ’373 and the district court trial are discussed below.

1. The First Petition: Intel’s IPR Petition Was Denied Institution Under *NHK/Fintiv*.

Intel’s Petition was filed on November 20, 2019. After considering ample briefing, the Board denied institution, finding that each *Fintiv* factor either weighed in favor of denial or was neutral. *Intel Corp. v. VLSI Technology LLC*, IPR2020-00158, Paper 16, 7-14 (May 20, 2020). The Board found, *inter alia*, that (1) the related district court proceeding (“District Court Action”) was well-advanced, (2) the parties (Intel and VLSI) had already invested “significant[]” time and resources into that proceeding, and (3) there was substantial overlap between the issues raised in the district court and the Intel Petition. *Id.*, 3, 7-14. The Board thus

found that it would “be an inefficient use of Board, party, and judicial resources to institute the present proceeding.” *Id.*, 14.

Intel sought precedential-opinion-panel review and rehearing, both of which were denied. IPR2020-00158, Paper 19 (POP Oct. 26, 2020), Paper 20 (Dec. 16, 2020). Intel’s appeals of this and related denials were dismissed. *Intel Corp. v. VLSI Technology LLC*, No. 2021-1614 et al., ECF No. 21 (Fed. Cir. May 5, 2021). Intel’s requests for en banc review and panel hearing were rejected. *Id.*, ECF No. 33.

2. The VLSI/Intel Trial Reached A Verdict Of Infringement.

Following the denial of Intel’s Petition, Intel continued to pursue its rejected IPR grounds fervently in the District Court Action. Intel served a 388-page expert report from Dr. Dennis Sylvester directed towards the ’373’s validity, 80 of those pages directed towards the same Harris-based grounds raised in Intel’s IPR. Ex. 2007 [Sylvester Report] ii, iii. Another ground raised the same secondary references (*e.g.*, Abadeer, Bilak, Cornwell, Zhang) used in the Intel Petition. *Id.* VLSI responded with Dr. Thomas Conte’s report which included 160 pages concerning the ’373’s validity, including 70 pages specifically directed towards the Harris-based combinations. Ex. 2003 [Conte Report] vi. Both parties’ experts were deposed at length concerning these and other opinions.

Intel maintained its validity defense until the eve of trial. One week before trial was scheduled, after expert discovery concluded, Intel informed VLSI that it was dropping its invalidity defense to the '373, purportedly to “streamline” the case. Ex. 2004 [Counsel Email]. Trial concluded with a jury verdict on March 2, 2021, finding infringement of both the '373 and '759 patents and awarding \$2.2 billion in damages, \$1.5 billion of which was attributable to infringement of the '373. Ex. 1007 [Verdict] 6. An Intel motion for retrial has been rejected. *VLSI Technology LLC v. Intel Corp.*, No. 6:21-cv-00057, ECF No. 638 (W.D. Tex. Aug. 9, 2021).

3. The Second Petition: OpenSky—A Newly Formed Nevada LLC—Copied Intel’s Rejected Petition And Resubmitted Intel’s Expert Declarations.

On April 23, 2021, less than two months after the verdict, OpenSky formed as a Nevada LLC. Its only apparent business activity is the filing of two IPR petitions against VLSI. *See* IPR2021-01056, Paper 2; IPR2021-01064, Paper 2. OpenSky’s Petition is essentially a copy of Intel’s rejected petition. Indeed, OpenSky’s petition simply refiled the same declarations filed by Intel.

4. The Third (And Present) Petition: Yet Another Newly Formed Entity—Patent Quality Assurance—Also Copied The Intel Petition.

The Verdict and OpenSky’s petition caught the eye of yet more speculators: one week after OpenSky’s petition was filed, another entity, calling itself “Patent

Quality Assurance, LLC,” formed in South Dakota to file the present petition, yet another copycat petition challenging the ’373. *See* IPR2021-01229, Petition; Ex. 2009 [PQA Articles] 1-3.

PQA’s only apparent activity to date is filing an IPR against VLSI. Like OpenSky’s, PQA’s petition copies the Intel Petition (and, thus, its petition is substantially identical to OpenSky’s as well) and relies on declarations from Intel declarants Dr. Singh and Dr. Hall-Ellis. PQA, however, represents that it has “exclusively” retained Dr. Singh and Dr. Hall-Ellis to provide testimony regarding the ’373 and, thus, PQA states that “OpenSky cannot present either expert for cross-examination,” as required under the Board’s rules, and that “OpenSky must either dismiss its petition to refile with a new expert or risk exclusion of its expert declaration as mere hearsay.” Pet., 4-5; *id.*, 5 (“OpenSky’s petition is not properly supported ...”).

B. The *Fintiv* Factors Strongly Favor Denial.

Like the Intel Petition it copies, PQA’s Petition too should be denied under *Apple Inc. v. Fintiv, Inc.*, IPR2020-00019, Paper 11 (Mar. 20, 2020) (precedential). Tellingly, though PQA recognizes that the Intel Petition was denied under *Fintiv* (Pet., 2), PQA neglects to address the *Fintiv* factors, each of which favors denial. Taking the factors in turn, (1) no stay has or will issue as the trial has already concluded, (2) there is no chance the final written decision could issue before trial

as the trial already concluded before the Petition was filed, (3) the already significant investment by the parties and the Court increased dramatically through expert discovery and trial, (4) Intel maintained its IPR validity defenses through expert discovery after which it chose to abandon its validity defenses altogether when the parties reached the courthouse steps, (5) by copying Intel's petition, retaining Intel's experts, and refiling its exhibits, PQA stands in Intel's shoes, and (6) allowing a *second* newly formed entity under no threat of infringement to refile a second copy of an already rejected petition raising defenses the prior petitioner abandoned in order to shakedown a patent owner who prevails after the crucible of trial would set a terrible precedent and encourage the very harassment and serial validity challenges the AIA was meant to avoid.

1. Fintiv Factor #1: No Stay Was Or Will Be Issued Because Trial Has Concluded.

Factor #1—"whether the court granted a stay or evidence exists that one may be granted if a proceeding is instituted"—strongly favors denial. No stay has or will be issued because the trial has already concluded. Ex. 1007 [Verdict]. An Intel motion for retrial has been rejected. Consequently, this factor favors denial. *See, e.g., Nintendo Co., Ltd. v. Gamevice, Inc.*, IPR2020-01197, Paper 13, 11-12 (Jan. 12, 2021) (factor favors denial where ITC hearing concluded making stay

“unlikely”); *Comcast Cable Commc’ns, LLC v. Rovi Guides, Inc.*, IPR2020-00800, Paper 10, 12-13 (Oct. 22, 2020) (similar).

2. *Fintiv* Factor #2: The Trial Concluded Before PQA Filed Its Petition.

Factor #2—“proximity of the court’s trial date to the Board’s projected statutory deadline for a final written decision”—strongly favors denial. Trial concluded over four months before PQA filed its petition. There is no possibility that a final written decision could issue prior to that already concluded trial. A completed trial “strongly favors” denial. *Apple Inc. v. Unwired Planet Int’l Ltd.*, IPR2020-00642, Paper 15, 6-7 (Sept. 9, 2020) (factor 2 “strongly favors” denial where trial already occurred); *Amazon.com, Inc. v. Vocalife LLC*, IPR2020-00864, Paper 22, 10 (Oct. 28, 2020) (same); *Neptune Generics, LLC v. Aventis Pharma S.A.*, IPR2019-00136, Paper 15, 35-37 (May 6, 2019) (similar); *Snap Inc. v. Blackberry Ltd.*, IPR2020-00391, Paper 8, 12-13 (July 13, 2020) (similar); *Ford Motor Co. v. MIT*, IPR2020-00010, Paper 9, 17-20 (Mar. 26, 2020) (similar).

3. *Fintiv* Factor #3: There Was Enormous “Investment In The Parallel Proceeding By The Court And Parties.”

Factor #3—“investment in the parallel proceeding by the court and the parties”—strongly favors denial.

By May 2020—nearly 10 months *before* the Trial—the Board had already found that “the parties already have invested *significantly*” in the District Court

Action. IPR2020-00158, Paper 16, 10. By then, claim construction had occurred and final infringement and invalidity contentions were served. *Id.*, 10. Intel’s invalidity contentions were voluminous. *See* Ex. 2010 [Invalidity Contentions–Cover]; Ex. 2011 [Invalidity Contentions–Harris]; Ex. 2012 [Invalidity Contentions–Abadeer]; Ex. 2013 [Invalidity Contentions–Additional Art].

That “significant[]” investment increased dramatically thereafter. As discussed (Section II.A.2), the parties exchanged hundreds of pages of expert reports assessing the ’373’s validity, including under the same grounds raised in the Petition. Ex. 2007 [Sylvester Report] ii; Ex. 2003 [Conte Report] vi. The parties also exchanged pre-trial disclosures and engaged in summary judgment and motion-in-limine briefing. This multi-year, multi-forum effort culminated in a trial involving live testimony from over a dozen expert and percipient witnesses. The trial was an even more demanding experience than usual due to COVID-19 (Ex. 2014 [Davis Law360 Article]) and a historic ice storm (Ex. 2005 [Bultman Bloomberg Article]). Forty-four attorneys appeared in the case and from multiple law firms per side. Ex. 2015 [Docket] 1-10.

Thus, the Board already found that this factor favored denial and that was before expert discovery, before summary judgment and motion-in-limine practice, and before trial and post-trial proceedings.

4. *Fintiv* Factor #4: There Is Substantial “Overlap Between Issues Raised In The Petition And In The Parallel Proceeding.”

Factor #4—“overlap between issues raised in the petition and in the parallel proceeding”—favors denial.

The Board previously found that there was “substantial overlap” between Intel’s IPR and district court grounds. *Intel*, Paper 16, 12. The Board found that the “same combinations of references asserted in the [p]etition also are asserted in [Intel’s] Final Invalidity Contentions.” *Id.*, 10-11 n.9, 12. PQA’s Petition is a near copy of Intel’s Petition (Ex. 2016 [Intel-PQA Comparison Chart]) and it raises the same references and challenges claims challenged by Intel. PQA relies on the same exhibits and, indeed, submits nearly identical declarations from the same experts. Ex. 2022 [Expert Comparison].

PQA contends that validity was not evaluated on the IPR grounds (Pet., 3) but ignores that the same combinations were raised in Intel’s Final Invalidity Contentions. *Intel*, Paper 16, 12. The parties’ expert reports spent hundreds of pages analyzing the Harris-based combinations. Ex. 2007 [Sylvester Report] ii; Ex. 2003 [Conte Report] vi. It was only after expert discovery concluded and on the eve of trial that Intel abandoned its validity defenses. Ex. 2004 [Dennhardt Email]. Intel’s choice does not change the fact that Intel’s validity defenses were raised both in the IPR and in the district court until the parties reached the

courthouse steps. Intel is a sophisticated company represented by able counsel. The Board should not second-guess Intel's considered and revealing choice to abandon that defense.

Moreover, the Board regularly denies institution in view of a completed district court or ITC proceeding, even where there is little overlap between the litigated issues in that proceeding and in IPR. *Amazon.com, Inc. v. Vocalife LLC*, IPR2020-00864, Paper 22, 12 (factor favored denial where three references not before court); *Snap*, IPR2020-00391, Paper 8, 12-13, 17 (denying institution due to §101 invalidity finding); *Ford Motor*, IPR2020-00010, Paper 9, 17-20 (denying institution where patent owner entered non-infringement stipulation).

5. *Fintiv* Factor #5: Even If PQA Is Unrelated To Intel, This IPR Would Be Highly Duplicative Of Prior Proceedings.

“Even when a petitioner is unrelated to a defendant ... the Board may, nonetheless, exercise the authority to deny institution.” *Fintiv*, Paper 11, 14. An unrelated petitioner should “address any other [] proceedings involving the challenged patent” and explain why its petition “would not be duplicative” of the prior proceedings. *Id.*

In *Fitbit, Inc. v. Philips North America, LLC*, IPR2020-00828, Paper 13 (Nov. 13, 2020), the Board denied institution under *Fintiv* based upon an ongoing litigation that did not involve the petitioner. *Id.*, 11-15. In so doing, the Board

rejected the petitioner’s argument that the third-party litigation was “irrelevant.”

Id., 10, 15-16. In accord, the Board routinely denies institution under *Fintiv*, even where the petitioner is not involved in the district court litigation. *Mylan Labs. Ltd. v. Janssen Pharmaceutica N.V.*, IPR2020-00440, Paper 17, 22-23 (Sept. 16, 2020); *Neptune Generics*, IPR2019-00136, Paper 15, 35-37.

Moreover, granting institution would implicate the precise concerns raised by *Fintiv* with respect to this factor, as it would involve “redoing the work of another tribunal” and be “duplicative” of the prior IPR. As discussed, the parties and the Court invested enormous amounts of time and money litigating validity and infringement issues relating to the ’373. *See* Section II.B.3.

And while PQA purports to be “unrelated to Intel” (Pet., 3), it nevertheless copied Intel’s petition, retained Intel’s experts, and filed materially the same expert declarations and other exhibits. *Valve Corp. v. Elec. Scripting Prods., Inc.*, IPR2019-00062, Paper 11, 9-10 (Apr. 2, 2019) (precedential) (follow-on petition can be denied if “significant relationship” between petitioners); *Ericsson Inc. v. Uniloc 2017, LLC*, IPR2019-01550, Paper 8, 12 (Mar. 17, 2020) (“significant relationship” created where follow-on petitioner picks and chooses from the earlier petitioner’s work product). By so thoroughly copying Intel’s work and retaining Intel’s experts—who presumably spent dozens of hours or more working closely with Intel’s attorneys—PQA is privy to Intel’s privileged and confidential

information and stands in Intel's shoes. *See, e.g., Shadow Traffic Network v. Superior Court*, 24 Cal. App. 4th 1067, 1078-79 (Cal. Ct. App. 1994) ("Embraced within the ambit of the attorney-client privilege are, *inter alia*, statements from counsel to the expert which disclose confidential information communicated by the client when disclosure is reasonably necessary to further the attorney's representation of the client's interest(s).") (excluding counsel who retained expert who had been interviewed for one hour by other side's attorneys). This further supports denial.

6. *Fintiv* Factor #6: "Other Circumstances That Impact The Board's Exercise Of Discretion, Including The Merits" Favor Non-Institution.

Factor #6—"other circumstances that impact the Board's exercise of discretion, including the merits"—strongly supports denial.

Congress intended IPRs to "provide "quick and cost effective alternatives to litigation" and to "establish a more efficient and streamlined patent system that will improve patent quality[.]'" *WesternGeco LLC v. ION Geophysical Corp.*, 889 F.3d 1308, 1317 (Fed. Cir. 2018) (quoting H. REP. NO. 112-98, at 40, 48 (2011)). Furthermore, "Congress recognized the importance of protecting patent owners from patent challengers who could use the new administrative review procedures as 'tools for harassment'" via "repeated litigation and administrative attacks on the validity of a patent.'" *Id.* (quoting H. REP. NO. 112-98, at 40).

Instituting here would set a terrible precedent as it would provide a green light to would-be harassers of patent owners who prevail at trial. These concerns are not speculative. After obtaining a significant judgement concerning two patents, two new entities (PQA and OpenSky) sprang out of the woodwork to file rip-offs of Intel's rejected IPRs challenging the '373 and/or '759 patents. The Board should not condone such tactics as they are fundamentally at odds with its precedents and policy.

PQA cribs from OpenSky's petition too to contend that its petition is necessary to safeguard the "integrity" of the patent system (*compare* Pet., 2 with IPR2021-01056, Pet., 8-9), without explaining why allowing a *second* newly-formed entity to harass a patent owner who prevailed at trial, presumably in the hopes of receiving a payout, would further that end in any way. The Board's precedential cases have found otherwise. *General Plastic Indus. Co., Ltd. v. Canon Kabushiki Kaisha*, IPR2016-01357, Paper 19, 17 (Sept. 6, 2017) (precedential) (recognizing "the potential for abuse of the review process by repeated attacks on patents"); *Valve*, IPR2019-00062, Paper 11, 15 (precedential) ("having multiple petitions challenging the same patent, especially when not filed at or around the same time as in this case, is inefficient and tends to waste resources. ... These serial and repetitive attacks implicate [] efficiency concerns ... and, thus, favor denying institution.").

Also favoring denial is that *Fintiv* is just one of several bases for denial as further explained in Sections II.C-F, and III.

While instituting here would be materially prejudicial to VLSI, the prejudice to PQA is minimal. PQA—which did not exist until after trial and, indeed, until after OpenSky filed its petitions—has no discernible business aside from filing the present petition. It is under no threat of an infringement allegation. *Shanghai Lunion Info. Techs., Ltd. v. Telefonaktiebolaget LM Ericsson*, IPR2018-00995, Paper 12, 23 (Nov. 13, 2018) (“minimal” prejudice in denying petition where petitioner “[had] never been sued for infringement” of the challenged patent); *Amazon.com*, IPR2020-00864, Paper 22, 12 (“Petitioner has not persuasively explained any benefit to resolving the patentability of the additionally challenged claims when they are not asserted against Petitioner.”). Nor did PQA—like most petitioners—spend the time and effort to find its own art or even draft its own petition. Rather, PQA took Intel’s petition off the shelf and retained Intel’s experts, doing hardly anything on its own.

* * * *

Trial has concluded, the parties made huge investments in that litigation, and this IPR would be redundant of the issues-at-hand there. The efficiency and integrity of the system are best served by denial.

C. The General Plastic Factors Strongly Favor Denial.

This is a prime example of an improper follow-on petition that should be denied under *General Plastic/Valve*. Indeed, on the heels of OpenSky’s petition, PQA’s Petition is, in fact, an improper follow-on to an improper follow-on and, like OpenSky’s, it is a near carbon copy of Intel’s petition. Ex. 2016 [Intel-PQA Comparison]. Each of the *General Plastic* factors favors denial. PQA had the benefit of two prior petitions, VLSI’s preliminary response, and the institution decision. This third, repetitive petition is precisely the kind of “harass[ing]” and “repeated attack[] on [a] patent” that “frustrate[s] the purposes of the [AIA] as providing quick and cost effective alternatives to litigation.” *General Plastic*, IPR2016-01357, Paper 19, 17 (Sept. 6, 2017) (precedential). The Petition, like the one it copied, should be denied.

1. *General Plastic* Factor #1: PQA Copied Intel’s Work Product, And All Of The Claims Challenged By PQA Were Challenged Previously By Intel.

Factor #1—“whether the same petitioner previously filed a petition directed to the same claims of the same patent”—favors denial.

The Board has found that this factor favors denial where different petitioners have a “significant relationship” and the follow-on petitioner challenges the same claims. *Valve*, IPR2019-00062, Paper 11, 9-10 (precedential). A “significant relationship” is formed where the follow-on petitioner copies its predecessor’s arguments:

We determine ... that *Petitioner implicitly created such a relationship by using the prior petitioners' work as a menu and picking and choosing from their work product.* The instant Petitioner's decision to use the prior petitions as a roadmap for its own petition ties the interests of all of the petitioners together.

Ericsson, IPR2019-01550, Paper 8, 12.

Here, PQA did not merely “pick[] and choos[e]” from Intel’s petition, but refiled Intel’s Petition as its own, and even retained Intel’s experts. Ex. 2016 [Comparison Chart]. It uses the same arguments and combinations, the same references, almost all of the same exhibits, and nearly identical declarations from the same experts. Indeed, each of the Intel, OpenSky, and PQA petitions are nearly identical.

IPR	Petitioner	Grounds/Claims	Status
IPR2020-00158	Intel	Ground I: Harris/Abadeer/Zhang (cls. 1-7, 9-11, 13, 15-16) Ground II: Harris/Abadeer/Zhang/Cornwell (cls. 2, 11-12) Ground III: Harris/Abadeer/Zhang/Bilak (cl. 8)	Denied
IPR2021-01056	OpenSky	Ground I: Harris/Abadeer/Zhang (cls. 1, 3, 4, 5, 9-11, 13) Ground 2: Harris/Abadeer/Zhang/Cornwell (cls. 2, 11)	Pending
IPR2021-01229	PQA	Ground I: Harris/Abadeer/Zhang (cls. 1-7, 9-11, 13-16) Ground II: Harris/Abadeer/Zhang/Cornwell (cls. 2, 11-12) Ground III: Harris/Abadeer/Zhang/Bilak (cl. 8)	Pending

By wholesale copying Intel’s Petition, refiling Intel’s exhibits, and retaining Intel’s experts, PQA has “implicitly created” a “significant relationship” with at least the previous petitioner Intel, if not both Intel and OpenSky. *Ericsson*, IPR2019-01550, Paper 8, 12; *Samsung Elecs. Co., Ltd. v. Elm 3DS Innovations, LLC*, IPR2017-01305, Paper 11, 18-19 (Oct. 17, 2017) (denying institution under *General Plastic* where petition had “high degree of similarity” to prior petitions filed by different petitioners and petitioner “use[d] the same expert”). Moreover, all but one of the claims challenged here were likewise challenged by Intel which further favors denial. *Valve*, IPR2019-00062, Paper 11, 10; *Ericsson*, IPR2019-01550, Paper 8, 11; *Nichia Corp. v. Document Security Sys., Inc.*, IPR2018-01167, Paper 10, 19 (Nov. 30, 2018) (denying institution under *General Plastic* even where a different petitioner challenged two additional claims under three additional references in view of other similarities).

2. *General Plastic* Factors #2, 4: PQA, Its Members, And The Entire World Were Constructively Aware Of Intel’s Art Since The Intel Petition Was Filed, Nearly Two Years Prior To PQA’s Petition.

The second and fourth factors are (2) “whether at the time of filing of the first petition the petitioner knew of the prior art asserted in the second petition or should have known of it.” and (4) “the length of time that elapsed between the time the petitioner learned of the prior art asserted in the second petition and the filing

of the second petition.” *General Plastic*, 16-17. Together, these factors strongly favor denial.

PQA’s Petition is substantially a copy of Intel’s Petition filed over a year-and-a-half before and it uses the same art. PQA, its members, and everyone else seeking to challenge the ’373’s validity were on notice of Intel’s combinations. *Am. Honda Motor Co., Inc. v. Intellectual Ventures II LLC*, IPR2018-00349, Paper 9, 16 (June 27, 2018) (petitioner on notice of references in earlier petitions because “monitoring litigation activity” “would have apprised” petitioner of those references); *cf. Apple Inc. v. Zomm, LLC*, IPR2019-01030, Paper 8, 11 (Nov. 14, 2019).

PQA provides no information as to when it learned of these references arguing instead that it “was formed on June 14, 2021, after Intel and OpenSky filed their petitions.” But PQA did not spring from nowhere. It was formed by people, including at least Joseph A. Uradnik, a patent attorney who signed PQA’s power of attorney (Paper 2). PQA’s founder(s) were well aware of Intel’s petition, formed within one week of seeing OpenSky’s petition and filed the present Petition, a near carbon copy of Intel’s Petition three weeks after forming. Thus, PQA was formed ***for the very purpose of copying Intel’s Petition.*** It would be an absurdity if *General Plastic/Valve* could be avoided by the mere formation of a new entity. *See Burden v. Versman*, 934 F.2d 164, 168 (8th Cir. 1991) (“the individual

defendants and the [newly-formed] corporations of which they were principals all had knowledge of the Burdens' claim at the time that Universal's property was transferred to them. *See [Farnsworth v. Muscatine Produce & Pure Ice Co., 158 N.W. 741, 747 (Iowa 1916)]* (knowledge of corporation's creators is imputed to corporation itself for purpose of determining good faith)."); *Wilson v. Crab Orchard Dev. Co., 276 N.C. 198, 212 (N.C. 1970)* ("at the time of the assignment to it by the Densons, Crab Orchard was a newly formed corporation completely dominated by Denson and his attorney. ... Consequently, Crab Orchard must be deemed to have acquired the interest in the certificates of deposit with notice of facts then known to Denson") (citing 54 AM. JUR, TRUSTS, § 218).

Given that each of its references is in Intel's Petition, PQA and its member(s), should be deemed to have knowledge of the references around the time Intel filed its petition. *Apple Inc. v. Uniloc 2017 LLC*, IPR2020-00854, Paper 9, 9 (Oct. 28, 2020) (precedential) ("[petitioner] has failed to ... offer an explanation concerning its knowledge, at the time it filed the first petition, of the prior art asserted in the [earlier] IPR and here. Because of the lack of explanation, we conclude that this second *General Plastic* factor weighs in favor of denying institution of the proceeding."); *Ericsson*, IPR2019-01550, Paper 8, 13.

3. General Plastic Factor #3: PQA Had VLSI's Preliminary Response And The Board's Institution Decision Before Filing Its Petition, And Affirmatively Responds To Those Papers.

Factor #3—"whether at the time of filing of the second petition the petitioner already received the patent owner's preliminary response to the first petition or received the Board's decision on whether to institute review in the first petition"—strongly favors denial.

Per the Board:

factor 3 is directed to Petitioner's potential benefit from receiving and having the opportunity to study Patent Owner's Preliminary Response, as well as our institution decisions on the first-filed petitions, prior to its filing of follow-on petitions. ... Multiple, staggered petitions challenging the same patent and same claims raise the potential for abuse. The absence of any restrictions on follow-on petitions would allow petitioners the opportunity to strategically stage their prior art and arguments in multiple petitions, *using our decisions as a roadmap*, until a ground is found that results in the grant of review. All other factors aside, *this is unfair to patent owners and is an inefficient use of the inter partes review process* and other post-grant review processes.

General Plastic, 17-18 (internal citation and footnote omitted).

The Board has repeatedly found that petitioners who modify and tailor arguments in view of a preliminary response or institution decision—called “roadmapping”—strongly favors denial. *Am. Honda Motor*, IPR2018-00349,

Paper 9, 17 (“Petitioner ... appears to have used Patent Owner’s ‘preliminary responses in the earlier-filed IPRs as a roadmap to attempt to improve [Petitioner’s] position in this Petition.’ ... Accordingly, this factor *weighs strongly* against institution.”); *Metall Zug AG v. Carl Zeiss Meditec AG*, IPR2020-01074, Paper 8, 8-9 (Jan. 5, 2021) (similar); *Google LLC v. Uniloc Luxembourg S.A.*, IPR2017-01665, Paper 10, 22 (Jan. 11, 2018) (“Petitioner took the opportunity to attempt to correct deficiencies alleged by Patent Owner in Amazon’s petition. This is precisely the type of roadmapping *General Plastic* counsels against.”).

Such disfavored “roadmapping” is precisely what occurred here. VLSI’s preliminary response was filed on February 24, 2020 and the institution decision issued on May 20, 2020, over a year prior to PQA’s Petition. While PQA mostly copies Intel’s Petition, where it does differ from Intel’s Petition, it does so by adjusting Intel’s arguments based on the prior briefing. *See, e.g.*, Ex. 2016 [Intel-PQA Comparison] 19-20 (bolstering basis for combining Harris and Abadeer); 22-24 (supplementing/altering discussion of limitation 1[f]); 26-28 (supplementing/altering discussion of 1[g]); 29 (supplementing/altering analysis of 1[h]); 29-30 (supplementing/altering analysis of 1[i]). Notably, the sections of Intel’s Petition most altered by PQA correspond to the very arguments presented in VLSI’s preliminary response to Intel’s Petition. IPR2020-00158, Paper 8, 20-25 (discussing limitation 1[h]); 25-32 (discussing limitations 1[g], 1[h], and 1[i]).

PQA availed itself of the benefit of both Intel’s and OpenSky’s petitions, VLSI’s POPR filed in response to the Intel Petition, and the Board’s institution decision thereto. Such improper roadmapping should not be rewarded.

4. General Plastic Factor #5: PQA Provides No Adequate Explanation For The Time Elapsed Before Filing.

Factor #5—“whether the petitioner provides adequate explanation for the time elapsed between the filings of multiple petitions directed to the same claims of the same patent”—strongly favors denial.

As discussed in Section II.C.2, the Petition is a near carbon copy of Intel’s Petition filed over a year-and-a-half earlier. PQA again points to its formation on June 14, 2021 (Pet., 4)—a week after OpenSky’s petition—but, as discussed, the knowledge of a corporation’s creators is imputed to the corporation. *See Burden*, 934 F.2d at 168; *Wilson*, 276 N.C. at 212; Section II.C.2.

PQA further states that institution is necessary to safeguard the “integrity of the patent system” as VLSI was able to obtain a significant judgment. Pet., 2-3. Notwithstanding its professed goals, PQA’s tactics run counter to the AIA’s objectives. “Congress recognized the importance of protecting patent owners from patent challengers who could use the new administrative review procedures as ‘tools for harassment.’” *WesternGeco*, 889 F.3d at 1317. PQA has not provided an “*adequate* explanation” for the time elapsed. Indeed, PQA’s incorporation

shortly after the Intel trial and on the heels of OpenSky's petition with its sole activity being the copying and filing of Intel's earlier petition implies a nefarious intent, presumably to seek a payoff.

5. General Plastic Factors #6, 7: This Petition Would Strain The Resources Of The Board.

Under the sixth and seventh factors, the Board considers “the finite resources of the Board,” and “the requirement under 35 U.S.C. § 316(a)(11) to issue a final determination not later than 1 year after the date on which the Director notices institution of review.” *General Plastic*, 16. These factors, frequently considered together, invoke efficiency considerations and strongly favor denial.

The Board has already expended resources reviewing the Intel Petition. The Board authorized additional briefing on *NHK/Fintiv*, and then denied institution. Following denial, the Board (and the Office) spent further resources considering Intel's request for precedential opinion panel review and reconsideration. IPR2020-00158, Paper 19 (POP Oct. 26, 2020), Paper 20 (Dec. 16, 2020). Prior to considering whether to institute here, the Board will have to spend still further resources considering OpenSky's petition.

Granting institution in this case—a needless follow-on to a needless follow-on—would flood the Board with belated challenges to patents that have already been challenged and/or litigated. With petitions filed by *two* newly formed

entities, this concern is hardly speculative. The Board’s precedent confirms that “having multiple petitions challenging the same patent ... is inefficient and tends to waste resources.” *Valve*, IPR2019-00062, Paper 11, 15 (precedential).

D. PQA’s Petition Should Be Denied Under 35 U.S.C. § 325(d).

The Petition—again, a near carbon copy of the rejected Intel Petition (Ex. 2016 [Intel-PQA Comparison]) that raises precisely the same art—should be rejected under § 325(d), particularly in view of the Federal Circuit’s recent precedential decision in *In re Vivint, Inc.*, -- F.4th--, 2021 U.S. App. LEXIS 29400 (Fed. Cir. Sept. 29, 2021). Section 325(d) provides that, “[i]n determining whether to institute or order a proceeding under this chapter ... the Director may take into account whether, and reject the petition ... because, *the same or substantially the same prior art or arguments previously were presented* to the Office.”

In *Vivint*, the Board had previously denied institution of an IPR petition under § 314(a) without reaching the merits because the petition, the third against that patent, was an example of undesirable, incremental petitioning. *Vivint*, 2021 U.S. App. LEXIS at *3. Thereafter, however, the Office allowed an ex parte reexamination wherein “vast swaths of the *ex parte* reexamination request [were] copied, almost word for word,” (*id.*, *4) from the rejected petition. Importantly, the Federal Circuit found that *though the rejected petitions grounds were never considered on the merits*, they were, nonetheless, “presented” to the Office for

purposes of § 325(d). *Id.*, *9, 13. The Court further found that the Office “abused its discretion and acted arbitrarily and capriciously by ordering reexamination, and thereafter, refusing to terminate that proceeding” in view of § 325(d). *Id.*, *13; *id.*, *14 (“it was arbitrary and capricious for the Patent Office to order reexamination over § 325(d), or, at a minimum, refuse to terminate reexamination ...”). In reversing the Office, the Court noted that the reexamination request “copied, word-for-word, two grounds from the [rejected] petition—the very petition deemed ‘a case of undesirable, incremental petitioning’—into its *ex parte* reexamination request.” *Id.*, 20; *see also, id.* (referring to reexamination as “nearly identical”).

Vivint confirms that denial under § 325(d) is required here. As in *Vivint*, the Petition is nearly identical to the Intel Petition that was rejected under § 314(a). Thus, the same exact “prior art [and] arguments” were—word-for-word—“previously presented to the Office” and, as *Vivint* confirms, it does not matter that the grounds were not rejected on the merits for purposes of § 325(d). Moreover, the basis for denying Intel’s Petition echoes the prior denial in *Vivint*. Whereas the *Vivint* petitioner’s petition was rejected as an “undesirable, incremental petition[],” the Intel Petition was rejected under *Fintiv* because it was duplicative of a district court trial scheduled to occur prior to the IPR final written decision, a trial that has since concluded. IPR2020-00158, Paper 16, 6-14. While the same petitioner filed both the IPR petition and the reexamination in *Vivint*, § 325(d) on its face is not

limited to situations where the same petitioner files both proceedings. *See also Google LLC v. Uniloc Luxembourg S.A.*, IPR2017-02067, Paper 10, 8 (Mar. 29, 2018) (“Applicability of § 325(d) is not limited to situations where the same petitioner has filed a follow-on petition. The statute allows for the exercise of discretion upon consideration only of whether the same or substantially the same prior art or arguments were presented previously to the Office.”).

Thus, just as it was an abuse of discretion for the Office to allow an *ex parte* reexamination to proceed that was a close copy of a prior petition denied under § 314(a), so too would it be error to allow a near carbon copy of the Intel Petition that was likewise rejected under § 314(a) to proceed to trial.

E. The Totality Of The Circumstances Strongly Favor Denial.

It is well-settled that the Board, acting on the Director’s behalf, “has complete discretion to decide not to institute review.” *St. Regis Mohawk Tribe v. Mylan Pharms., Inc.*, 896 F.3d 1322, 1327 (Fed. Cir. 2018); *Harmonic Inc. v. Avid Tech., Inc.*, 815 F.3d 1356, 1367 (Fed. Cir. 2016). This is a clear case for exercising that discretion.

There are three independently sufficient reasons to deny institution. While each reason stands on its own, they are also mutually reinforcing and together clearly demonstrate that denial is appropriate.

There is no comparison between the prejudice that VLSI would suffer if this matter were instituted versus the trivial prejudice PQA would suffer by a denial. VLSI bore the enormous costs of litigating through trial against Intel, in a district court case that included 44 lawyers to obtain a substantial judgment. This trial also included substantial collateral proceedings before the Board and the Federal Circuit. Allowing a *second* new entity to refile Intel's Petition tweaking it only to avail itself of the advantages of roadmapping, is precisely the sort of "repeated" and "harassing" attacks Congress sought to avoid and the Federal Circuit and the Board have recognized patent owners should not be subject to. *WesternGeco*, 889 F.3d. at 1317; *Valve*, IPR2019-00062, Paper 11, 15 (precedential).

By contrast, no "prejudice" to PQA bears mention. PQA formed in the wake of the Verdict in the evident hope of receiving a payoff. It found no art. It crafted no grounds. Instead, PQA just copied from Intel's Petitions and filed literal copies of Intel's exhibits, adjusting Intel's work only to avail itself of the improper advantages of roadmapping (*see* Section II.C.3).

The Petition should be denied. If the Board were to institute here, it would embolden newly formed entities to spring from the woodwork to challenge *any* patent that is the subject of a successful verdict. Such unfettered harassment should not be encouraged.

F. If The OpenSky Petition Is Instituted, That Is All The More Reason To Deny Institution Of The PQA Petition.

If the Board saw fit to institute the OpenSky Petition, that is all the more reason to decline institution here as PQA's Petition is nearly identical to OpenSky's petition and includes the same grounds. Ex. 2033 [OpenSky-PQA Comparison]. It would make no sense for the Board to institute even one follow-on petition much less a second, nearly identical, petition. Not surprisingly, the Board has routinely denied institution of a second similar petition when one is ongoing. *Google LLC v. Uniloc Luxembourg S.A.*, IPR2017-01665, Paper 10, 21 (Jan. 11, 2018) ("Patent Owner argues that the burden of defending against a subsequent case based on the same art 'would be substantial in having to twice overcome, in two separate trials involving separate discovery and potentially even a separate panel, what Petitioner admits is the same arguments concerning the same combination of references.' ... We agree."); *Samsung Elecs. Am., Inc. v. Uniloc 2017 LLC*, IPR2018-01756, Paper 7, 29-30 (Mar. 11, 2019) (denying institution where "most of the prior art and arguments advanced by Petitioner are the same as or substantially the same as the prior art and arguments advanced in [instituted prior IPRs]."); *Apple Inc. v. Uniloc Luxembourg S.A.*, IPR2017-01804, Paper 8, 6 (Jan. 19, 2018) ("If we were to institute trial at this time, Patent Owner

would be required to participate in duplicative proceedings with different petitioners, each having its own counsel ...”) (denying institution).

Respectfully, the Board should not institute even one copy of the rejected Intel Petition. It most certainly should not institute two.

III. PETITIONER FAILS TO DEMONSTRATE A REASONABLE LIKELIHOOD OF SUCCESS AS TO ANY CLAIM (ALL CLAIMS, ALL GROUNDS).

Petitioner’s obviousness combinations fail for numerous reasons.

First, Petitioner’s Harris/Zhang combinations, on which Petitioner relies for all proposed Grounds, do not teach or suggest *switching* a memory between *two regulated voltages* in the manner claimed. Instead, they teach powering the memory with a *single independently adjustable voltage*. Section III.A. Moreover, they do not teach scenarios where the second regulated voltage is greater than the first regulated voltage, as required by the claims. Section III.B.

Second, Petitioner apparently concedes that Harris’s manufacturing-time soft-defect detection embodiment—Harris’s focus—is even further afield of the claimed invention than Harris’s “failure mode” and “low power feature” embodiments, because Petitioner fails to identify subject matter corresponding to multiple claim elements in connection with Harris’s soft-defect detection embodiment. In fact, that embodiment fails to teach providing voltages to any of its circuits in the manner claimed. Section III.C.

Third, to the extent Petitioner conflates Harris’s three distinct embodiments, it has failed to show a POSITA would be motivated or able to combine those embodiments, much less in the manner claimed. Section III.D.

Fourth, Petitioner’s reliance upon Zhang’s voltage regulators—designed to provide a controlled voltage—cannot be squared with Petitioner’s reliance upon Harris’s failure mode embodiment in the combined system. Section III.E.

Fifth, objective considerations of non-obviousness independently disprove Petitioner’s claims of obviousness. Section III.F.

A. Petitioner Fails To Demonstrate Its Combinations Disclose Or Render Obvious Any System That Switches A Memory Between Two Regulated Voltages In The Manner Claimed.

Independent claims 1 and 9 concern a memory that, generally speaking, switches between “first” and “second” regulated voltages. The memory is “provided”/“supplied” with the “first regulated voltage” when it “is at least the value of the minimum operating voltage.” When the first voltage is “less than”/“below” the minimum operating voltage, however, the “second regulated voltage” is “provided”/“supplied.” Ex. 1001 [’373 Patent] cls. 1, 9. In both scenarios, the “first regulated voltage” is supplied to the “functional circuit”/“circuit that provides a function.” *Id.* No plausible reading of the Harris or Zhang references would teach this subject matter.

To the contrary, these references teach a distinct approach that *lacks* the

claimed subject matter. Harris and Zhang at most teach *independently adjusting* a *single* voltage provided to a memory, all while providing a separate voltage to other circuitry. This approach does not switch the memory between multiple regulated voltages in the manner claimed.

Harris's processor contains two separate voltage planes, Vstby and VDD. Ex. 1003 [Harris] 1:66-2:16. Harris uses these voltage planes in a manufacturing-time memory testing embodiment (*id.*, 2:16-23, 3:1-49), a run-time "failure mode" embodiment (3:49-4:3), and a sparsely-described run-time "low power feature" embodiment (4:63-5:4). Ex. 2002 [Conte Decl.] ¶¶ 23-29. These uses differ from one another substantially. As Dr. Conte explains:

Harris generally discloses three embodiments that leverage its separate voltage planes. Each is markedly different from the claimed approach of the '373 Patent.

First, Harris's centerpiece—the application reflected in the bulk of the specification and exclusively in Harris's abstract and title—is an externally driven SDDT embodiment. In this embodiment, the Vstby terminal is powered by "an external current-measuring device or microprocessor tester" that "monitor[s] the current I drawn through Vstby terminal 130 and determine[s] whether or not a soft defect is present." Ex. 1003 [Harris] 3:36-41. The portions of the memory being tested are connected to the Vstby plane. An "external current-measuring device or microprocessor tester" replaces an "on-board

detect circuit,” the elimination of which Harris touts as its chief advantage. *Id.*, 3:1-10.

The first embodiment is meant to be used in connection with design and manufacturing, to “allow a design team to pinpoint manufacturing or design defects in a memory array of a microprocessor.” *Id.*, 3:46-39. Once the part is tested for soft defects in this manner during development or manufacturing phases, there is typically no further need for soft-defect detection testing. For example, this embodiment would typically not be used by end-users after manufacturing has completed for its SDDT purposes.

Second, Harris discusses an embodiment with a “hardware controlled function” of the Vstby plane suitable for a “failure mode.” *Id.*, 3:50-4:3. In the “failure mode,” “the voltage on the Vstby terminal 132 is switched to power the memory 106 to sustain memory contents when either main or VDD power is failing.” The “failure mode” scenario is chiefly useful during end-user operation (*i.e.*, after manufacturing). For example, the “failure mode” embodiment could be useful when the system is operating with at least two power supplies, such as a main power source (*e.g.*, a wall socket) and a battery source. In that regard, Harris’s “failure mode” is distinct from its SDDT embodiment. Harris explicitly distinguishes between the two. *See id.*, 3:64-4:3 (“One function being a VDD failure mode . . . , and the other mode being software controlled mode which allows for the testing of soft defects”).

Third, in an embodiment that Harris states is “other than” the testing and “failure mode” embodiments, Harris teaches a “low power

feature.” In this embodiment, one of the voltage planes continuously powers “at least one memory array” while another voltage plane continuously powers the CPU. *Id.*, 4:59-5:4. Harris does not teach using a switch circuit to vary the voltage provided to the memory in this “low power feature.” Instead, this third embodiment simply relies on Harris’s dual voltage planes to provide separate and independently adjusted voltage levels to the memory and the CPU.

Ex. 2002 [Conte Decl.] ¶¶ 30-34. None of the applications taught by Harris for its voltage planes or its switch resemble the subject matter of the claims-at-issue.

Harris’s “low power feature” does not teach switching the memory between regulated voltages. Instead, that embodiment uses Harris’s separate voltage planes to provide the memory with an independently adjusted voltage using one voltage plane, while providing other circuitry with another independently adjusted voltage using the other voltage plane. That is the extent of the “low power feature” embodiment, and Harris does not mention use of a switch in connection with the “low power feature” at all.

Petitioner’s combination of Harris with Zhang doubles down on this independent-adjustment approach by importing Zhang’s multiple on-die regulators, each of which powers a separate voltage plane and independently adjusts the voltage on such plane according to the needs of its circuits. The circuits are not switched between the planes. Neither Harris nor Zhang teaches a reason to

perform such switching in the “low power feature,” and Petitioner does not identify one.

Harris’s “failure mode” embodiment also does not teach the claimed subject matter, even when—especially when—combined with Zhang. When the memory receives a second voltage during Harris’s “failure mode,” the first voltage is *failing*. This fact is fatal to Petitioner’s theory for multiple independent reasons.

First, a failed voltage does not meet Petitioner’s own definition of a “regulated voltage.” Second, even if a failed voltage were considered regulated, such a hypothetical failed “first regulated voltage” would not be provided to the CPU for risk of electrical damage. Third, if Harris’s “failure mode” were combined with Zhang—even in a way that switches from a failed voltage to a standby voltage—Zhang’s capabilities would eliminate any motivation to provide the failed “first voltage” to any circuit.

Each of these two embodiments is discussed below.¹

¹ To the extent Petitioner relies on the soft-defect detection test embodiment—and it does not appear to do so—its theories fail for the reasons discussed in Section III.C.

1. “Low Power Feature” Embodiment.

Harris’s “low power feature” provides a single “power supply voltage” to the memory. Zhang, similarly, teaches providing a single regulated voltage to memory, and adjusting that voltage to meet performance and power goals. Both references reject *switching* a memory between multiple regulated voltages during normal operation, and instead favor *independently adjusting* a single regulated voltage provided to the memory.

The entirety of Harris’s “low power feature” description is reproduced here:

[T]he test mode of the [data processor] taught herein may be used as a low power feature *wherein the second power supply voltage (Vstby or Vdd) is provided to the at least one memory array* while the first power supply voltage (Vdd or Vstby) which is being supplied to the CPU is lowered so that lower power is consumed in the data processor while data within the at least one memory array is maintained.

Ex. 1003 [Harris] 4:59-5:4. Dr. Conte explains, this embodiment does not switch the memory between Vdd and Vstby:

Harris’s “low power feature” at most teaches *providing only the “second power supply voltage”* (Vstby) to the memory array, not *switching* between the “first power supply voltage” and the “second power supply voltage.” Here, Harris simply takes advantage of the separate voltage planes that its system teaches for purposes of the external SDDT capabilities that Harris describes as “[t]he present invention,” leveraging those separate voltage planes for a “low power

feature” that provides separate operating voltages to the memory and to the CPU. Ex. 1003 [Harris], 3:8-9.

Ex. 2002 [Conte Decl.] ¶ 78.

Further, because Harris teaches the use of a switch in other embodiments, its omission of the switch in connection with the “low power feature” *counsels against* operating the switch in that embodiment. A POSITA would understand that Harris’s omission of specified switch operation in connection with the “low power feature” means that switch operation is neither used nor needed in this embodiment for purposes of varying the respective voltage levels. Ex. 2002 [Conte Decl.] ¶ 79.

In accord, and like Harris’s “low power feature,” Zhang never teaches switching between separate regulated voltages. For example, Zhang’s Figure 2C (reproduced below) includes local voltage regulator 251, which “provides Vcc(local) to power circuit 261 via local power grid 285,” and “local voltage regulators 252-254,” which similarly “provide independent local supply voltages to power circuits 262-264, respectively, via local power grids 286-288.” Ex. 1005 [Zhang] [0027]; Ex. 2002 [Conte Decl.] ¶¶ 46-52.

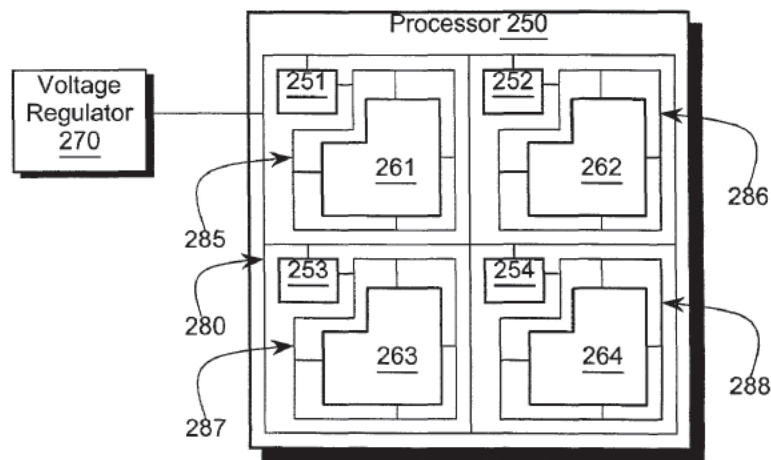


Figure 2C

Zhang teaches that “[e]ach local supply voltage provided by each local voltage regulator 251-254 of FIG. 2C may be *independently adjusted* by processor 250.” *Id.*, [0028]. Echoing Harris’s “low power feature,” Zhang further provides that these separate, independently adjusted voltages can separately power “processor cores” and “memory regions such as a cache.” *Id.*, [0031].

Zhang’s disclosed systems can independently control the respective local voltage regulators, and thereby independently adjust the voltages provided to circuits like individual cores and memories. Zhang does not teach switching its circuits from one regulated voltage to another, nor does it teach a need for such operation. Ex. 2002 [Conte Decl.] ¶¶ 80-82. In view of its capabilities and objectives, Zhang has no need for such functionality. *Id.*

Petitioner’s own stated reasons for combining Harris with Zhang further

confirm that a POSITA would not use a memory that switches between two separate regulated voltages. Petitioner first argues that a POSITA would have been motivated to combine Harris with Zhang “to control [Harris’s] supply voltages, VDD and Vstby.” Pet., 37. Once the VDD and Vstby are independently controlled, however—as they are in Harris’s “low power feature” *and* in Zhang’s system—switching between the two power supply voltages would serve no function recognized, let alone taught, by the references. Neither Petitioner nor its art offer any motivation to switch between two different power supplies in a system capable of independently adjusting voltages separately provided to multiple circuits. Ex. 2002 [Conte Decl.] ¶ 85.

Petitioner next argues that a POSITA would have been motivated to combine Harris with Zhang “to raise or lower VDD and/or VSTBY to decrease power consumption or improve performance.” Pet., 38. In other words, Petitioner’s own position appears to be that a POSITA would have sought and adopted Zhang’s ability to raise or lower each on-die voltage separately and independently. Petitioner fails to explain why, having sought and adopted those features, a POSITA would have had any motivation to further switch a memory between two regulated voltages. Ex. 2002 [Conte Decl.] ¶ 86.

Petitioner’s account of why a POSITA would consult Zhang leaves no room for Harris’s “low power feature.” The only conclusion these arguments support is

that a POSITA aware of both Harris and Zhang would have simply chosen the system of Zhang. Ex. 2002 [Conte Decl.] ¶ 89.

In any event, whether or not Harris’s “low power feature” teaches subject matter not present in Zhang, these references do not combine to render the claimed subject matter obvious. For the reasons discussed above, these references steer away from that approach and teach a distinct mechanism.

Further, because Harris and Zhang counsel a switchless approach, Petitioner’s arguments about why a POSITA would have combined these references with Abadeer and Cornwell also fail. Without a switch circuit to operate at a “set level or threshold” in the manner Petitioner claims Harris works, Petitioner fails to motivate its further combination with Abadeer and Cornwell. Ex. 2002 [Conte Decl.] ¶¶ 63-66; Pet., 26-28, 50-51.

2. “Failure Mode” Embodiment.

Petitioner likewise fails to prove a POSITA would be motivated to arrive at the claimed inventions in view of Harris’s “failure mode” embodiment and Zhang. Even assuming, *arguendo*, that a failed voltage could be a “regulated voltage,” a POSITA would not be motivated to continue providing that failed voltage to the “functional circuit” (or “circuit that provides a function”) in the manner required by the claims. *See, e.g.*, cl. 1 (“while the second regulated voltage is provided as the operating voltage of the memory, the first regulated voltage is provided to the

functional circuit”).

Petitioner claims that “Harris explains when VDD is lowered below the set level or threshold, Vstby should be provided to the memory.” Pet., 45. Harris, however, clarifies that the “VDD voltage drops below a set level or threshold . . .

when either main or VDD power is failing”:

Usually, the voltage level on the terminal VDD 132 is monitored to ensure that a functional voltage is provided for all time on the pin 132. When this VDD voltage level drops below a set level or threshold, the voltage on the Vstby terminal 132 is switched to power the memory 106 to sustain memory contents ***when either main or VDD power is failing***. Normally, Vstby will be powered from a battery back-up source and may or may not be a voltage equal to that supplied by VDD. Therefore, the present invention allows for dual functionality of the voltage standby (Vstby) pin. ***One function being a VDD failure mode where a failure is detected on the VDD pin 132 and Vstby must be substituted for VDD to avoid memory data loss***

Ex. 1003 [Harris] 3:54-67. A failed voltage is not a regulated voltage, as further discussed below in Section III.B.1, and such a scenario does not implicate the arrangement recited by the claims-at-issue.

But even if a failed voltage were a “regulated” voltage, Petitioner does not explain why a POSITA would continue to supply that failed voltage to the “functional circuit”/“circuit that provides a function” as required by the claims. To

the contrary, a POSITA would not understand Harris to teach exposing the CPU to a voltage failure, because doing so could risk physical damage to the chip. As Dr. Conte explains:

CPU circuitry is complex and sensitive, and exposing such circuitry to a failing voltage could have unpredictable, potentially fatal, consequences. A voltage failure is not necessarily a clean, sudden loss of voltage. More commonly, a voltage failure can be characterized by a period of erratic voltage levels as well as, potentially, voltage spikes. If the CPU remained connected to the failing voltage that Harris's "failure mode" reacts to, the CPU would, at best, risk unforeseeable changes to its digital state, such as its registers and execution units, potentially making it impossible to resume correct operation after the failure without a reset. Further still, exposing the CPU to such a voltage could cause the CPU to write random information to the memory, defeating Harris's stated goal for the failure mode to "to sustain memory contents when either main or VDD power is failing." And, unpredictable voltage fluctuations during a failure could risk permanent electrical damage to the CPU, including in the event of a voltage spike. A POSITA would understand that, when a failure is detected, the system disconnects CPU circuitry from VDD in a way that will shield the CPU from the voltage failure, rather than knowingly continue to provide the CPU with a dangerously unpredictable voltage.

Ex. 2002 [Conte Decl.] ¶ 91.

Indeed, Petitioner argues that a POSITA would have combined Harris with

Zhang “to provide both CPU 110 and the memory 106 with a stable voltage.” Pet., 37. Petitioner’s theory that a POSITA would knowingly continue to supply a “failed” voltage to the CPU during the “failure mode” is irreconcilably inconsistent with that proffered motivation. Ex. 2002 [Conte Decl.] ¶ 92.

Petitioner’s strained combination also disregards Zhang’s teachings, which eliminate any motivation to expose the CPU to a failed voltage. As Dr. Conte explains:

If Harris’s “failure mode” were implemented in the combined system of Harris and Zhang, there would be no need to expose the CPU to a failed voltage. The system of Harris is constrained by its primary purpose, the elimination of the on-chip SDDT circuit: accordingly, its switch circuit is placed to switch only the memory to Vstby. But a POSITA focused on the “failure mode” embodiment would understand that, if the switch circuit were to be retained as part of the combined system, the circuit could be placed elsewhere. In fact, having adopted Zhang’s multiple on-die voltage regulators, a POSITA would understand that a sensible use of a switch circuit for a “failure mode” would switch the *entire processor* from a failed Vcc(global) to a standby global supply, so that none of the local voltage regulators or other circuits of the processor would receive the then-failing “first” voltage.

Ex. 2002 [Conte Decl.] ¶ 96; *see also id.*, ¶ 97.

Thus, even assuming, *arguendo*, that a POSITA would be motivated to

include additional circuitry in the combined system to safeguard against the failure of individual voltage regulators, Petitioner has failed to explain why such a POSITA would be motivated to combine the systems of its references in a manner that would *ever* allow a failed voltage to reach any circuit.

B. Petitioner Fails To Demonstrate Its Combinations Disclose Or Render Obvious Any System Wherein “The Second Regulated Voltage Is Greater Than The First Regulated Voltage.”

The claims further require that the “second regulated voltage” is “greater” than the “first regulated voltage.” Petitioner fails to prove this limitation is obvious over its combinations.

Petitioner contends that Harris’s VDD is the “first regulated voltage” and Harris’s Vstby is the “second regulated voltage.” Pet., 35-36, 40. Harris, however, does not suggest that Vstby—a standby voltage (Ex. 1003 [Harris] 4:53-54)—is greater than VDD. To the contrary, Vstby is “normally” battery powered and, consequently, “may not be a voltage equal to that supplied by VDD.” Ex. 1003 [Harris] 3:60-62. In a “normal mode of operation,” Harris’s core is powered by VDD, a “functional voltage.” Ex. 1003 [Harris] 3:1-2, 3:54-56.

As Dr. Conte explains:

A POSITA would understand that, in a system that receives both a standby battery voltage (such as Harris’s Vstby) and a separate voltage unconstrained by the limitations of a battery, such as Harris’s

“functional voltage” VDD, the battery voltage would not be greater than VDD.

A related Harris patent—U.S. Patent No. 5,901,103 (“Harris ’103”)—confirms that Vstby, suitable for a low power mode, would be less than or equal to VDD. Ex. 2017 [Harris ’103] 7:61-8:2. (“In one form, VSTBY can be a voltage *equivalent in value to VDD*. . . . In another form, VSTBY can be a voltage *less than a VDD voltage*.”); 5:35-37 (“If VSTBY is a voltage *lower than VDD*, then VSTBY can be a low power voltage and VDD can be a normal mode functional voltage.”); 4:14-18 (“[I]n FIG. 1, each power control switch 38-42 is coupled to a VDD power supply voltage line and a standby (VSTBY) power supply voltage line, wherein the voltage on the *VDD power supply voltage line is greater than or equal to* that on the standby power supply voltage line.”).

Ex. 2002 [Conte Decl.] ¶¶ 98-99.

Parties to patent disputes frequently debate the meaning of a particular patent’s disclosure. To inform that analysis, parties will often turn to various dictionaries and other evidence of use by POSITAs. There can be no better evidence of meaning, however, than how that term is characterized in a related patent that shares many of the same inventors. *Laryngeal Mask Co. v. Ambu A/S*, 618 F.3d 1367, 1373 (Fed. Cir. 2010) (“This prior art use of the term [by the inventor in his earlier patent applications] would further inform one of skill in the art as to the common meaning of the [disputed] term backplate.”).

Petitioner nevertheless contends that Vstby is greater than VDD in two circumstances particular to the two embodiments of Harris discussed above, namely, (1) when VDD fails, as in Harris's "failure mode" embodiment, *e.g.*, Ex. 1003 [Harris] 3:50-4:3; and (2) when Harris's "test mode" is used as a "low power feature," *e.g.*, *id.*, 4:63-5:4. Neither situation discloses or renders obvious a "second regulated voltage greater than the first regulated voltage." Patent Owner responds in further detail pertaining to each circumstance below.

1. "Failure Mode" Embodiment.

Petitioner first contends that the "second regulated voltage is *greater* than the first regulated voltage" limitation is met when VDD fails or falls below a threshold. Pet., 41-42. Harris, however, clarifies that "VDD voltage level drops below a set level or threshold . . . *when either main or VDD power is failing.*" Ex. 1003 [Harris] 3:57-60. In this specific circumstance of VDD failure, if Vstby is "greater" than VDD, it is only because VDD has *failed*. Petitioner does not even attempt to explain how a *failed* voltage can be said to be a "regulated voltage," as the claim requires.

Indeed, an important purpose of a "regulated voltage" is to receive a controlled voltage level, not one that has uncontrolledly failed. Ex. 2002 [Conte Decl.] ¶ 93. Petitioner's own exhibit states that a voltage regulator is "a device that *maintains the terminal voltage* of a generator or other voltage source *within*

required limits despite variations in input voltage or load.” Ex. 1024 [McGraw-Hill Dictionary] 2269 (cited at Pet., 37; Ex. 1002 [Singh Declaration] ¶ 84). A failed voltage, by Petitioner’s own definition, is not a “regulated voltage.”

In accord, in Petitioner’s Zhang reference, the output voltages (Vcc(local)) of regulators 251- 254—which are used in Petitioner’s combination—are each either set to a specific value to meet a particular timing requirement or are adjusted to save power or respond to changes in frequency of the processor. Ex. 1004 [Zhang] [0028] (“During normal operation ..., each Vcc(local) **may be set to a value** that allows the associated circuit, or a portion thereof, **to meet a timing requirement** at a given frequency.”); *id.* (The value of Vcc(local) “may be adjusted by the processor in accordance with a power management policy” or “adjusted in response to a change in the operating frequency of the processor.”). Petitioner does not provide any evidence that a failed voltage may be a “regulated voltage.” Consequently, because Petitioner fails to demonstrate that VDD is a “regulated voltage” when it fails (including when this “failure mode” embodiment is combined with the local supply voltages of Zhang), Petitioner fails to demonstrate a “second regulated voltage” [Vstby] that is “greater” than a “first **regulated** voltage” [VDD], as required by the claims.

2. “Low Power Feature” Embodiment.

Petitioner alternatively cites Harris’s “low power feature” to argue that this

limitation is met. Pet., 54-55. Petitioner's argument, however, is not faithful to what Harris actually teaches about that embodiment. As Dr. Conte explains:

Harris's "low power embodiment" does not indicate that the "first supply voltage" is "lower" than the "second supply voltage." Petitioner identifies VDD as the "first supply voltage," but never acknowledges that either of the two supply voltages (VDD or Vstby) could be lowered, as expressly taught in Harris. Id., 5:1-2. Assuming that the "second supply voltage" is Vstby and the first supply voltage is VDD, as Petitioner appears to do, Harris does not teach that VDD would fall below Vstby. For example, when VDD is the "first power supply voltage," it could be lowered from 1.0 V to 0.8 V, while Vstby holds at 0.6 V in which case VDD would still be greater than Vstby. This scenario allows the data processor to consume lower power while maintaining the memory, consistent with the specification's description of this embodiment. But Vstby would not be greater than VDD at any point in this low-power scenario. Indeed, the "low power mode" embodiment merely leverages Harris's separate power planes to provide separate voltages to different components on the chip. It does not focus on any particular combination of voltage values or relationships.

Ex. 2002 [Conte Decl.] ¶ 100.

Because Petitioner fails to prove that Vstby is greater than VDD in the "low power feature," Petitioner fails to find any scenario in its references wherein Vstby is greater than VDD—other than when VDD fails and therefore does not

meet Petitioner’s own definition of a “regulated voltage.” Petitioner fails to show that this limitation is met.

C. Petitioner Fails To Demonstrate That Any Combination Based On Harris’s Soft-Defect Detection Embodiment Discloses Or Renders Obvious The Claimed Voltage Levels.

Petitioner does not appear to rely on Harris’s teaching about switching the memory between voltage planes during a soft-defect detection test (“SDDT”). Petitioner instead focuses on Harris’s distinct “failure mode” and “low power feature” embodiments. For example, in connection with claim element 1[i], Petitioner first focuses on the “low power feature” and that embodiment’s provision of separate voltages to the memory and the CPU (Pet., 44-45 (citing Ex. 1003 [Harris] 4:63-5:4)), and then on the “set level or threshold” of the “failure mode” embodiment. *Id.* (citing Ex. 1003 [Harris] 3:57-60). Petitioner thus has not provided an account of how the SDDT embodiment could render all of the subject matter of claim 1 obvious.

Whereas Petitioner does cite to Harris’s SDDT embodiment in connection with the “power supply selector” structure of element 9[g] (Pet., 59), Petitioner otherwise relies on its discussion of claim element 1[i] to establish certain properties that element 9[g] requires of that structure. Petitioner thus has not provided an account of how the SDDT embodiment could render all of the subject matter of claim 9 obvious. As discussed in Section III.D below, Petitioner’s

conflation of embodiments fails to account for the differences in these distinct embodiments, and is improper because Petitioner has failed to offer any reason to combine these embodiments.

Notwithstanding, even if Petitioner did advance a theory based on the SDDT embodiment, that theory would fail for multiple independent reasons, some of which are discussed below.

First, the SDDT embodiment connects the memory to the Vstby plane during an SDDT to measure, externally, the current draw of portions of the memory when those portions are isolated from other circuitry. *E.g.*, Ex. 1003 [Harris] 3:3-7, 32-40. The switch is not operated in connection with lowering a voltage in any way, and Petitioner has not established that Vstby is provided to the memory “when the first regulated voltage is less than[/is below] the value of the minimum operating voltage” as required by elements 1[i] and 9[g]. Ex. 2002 [Conte Decl.] ¶ 64.

In fact, as Dr. Conte explains, a POSITA would understand that the first regulated voltage should not approach such levels:

SDDT takes place in the manufacturing plant. Petitioner does not provide a reason to operate the CPU of Harris at a low voltage during SDDT, and Harris does not motivate saving power or conserving battery charge during SDDT. To the contrary, a POSITA would understand that an important goal of manufacturing is yield, or number

of viable products manufactured per unit time. To the extent the SDDT relies on functions performed by the CPU—for example, to “write a test initiation value to register 142,” Ex. 1003 [Harris] 3:30-32—a POSITA would understand that, to maximize yield, it could be desirable to operate the CPU at the high end of the range of allowable operating voltages and frequencies, in order to speed up its operation and therefore potentially reduce the duration of the soft-defect detection test. The high end of that range would typically be above the minimum operating voltage of the memory.

Ex. 2002 [Conte Decl.] ¶ 102.

Second, the SDDT embodiment expressly powers a *portion* of the memory with Vstby, while powering the remainder of it with VDD—confirming that VDD, Petitioner’s “first regulated voltage,” is neither “less than” nor “below” the memory’s minimum operating voltage: “In all SDDT current test cases, *some portion* of memory 106 will be powered with Vstby 130 while *all other circuitry* in processor 100 is powered by VDD 132.” Ex. 1003 [Harris] 3:25-28. Petitioner does not explain why a voltage lower than the memory’s minimum operating voltage would be provided to the memory in this configuration. Ex. 2002 [Conte Decl.] ¶ 103. To the contrary, Petitioner asserts that “it was . . . known long before the ’373 Patent that while power can be saved by reducing the memory’s voltage . . . , the voltage should remain at least as great as the memory’s minimum operating voltage.” Pet., 7.

Third, Petitioner has not established that the SDDT embodiment uses voltages such that “the second regulated voltage is greater than the first regulated voltage” at any point as required by the claims-at-issue. Petitioner has identified no such teaching in its argument, and does not discuss the relative voltage levels of VDD and Vstby in connection with the SDDT embodiment. Ex. 2002 [Conte Decl.] ¶ 104.

Accordingly, to the extent Petitioner relies on the soft-defect detection embodiment for any portion of its argument, including the “power supply selector” structure of claim element 9[g], its theory fails for at least the three independent reasons above.

D. Petitioner Fails To Establish—Or Even Argue—That Harris’s Different Embodiments Should Be Combined.

Harris teaches three distinct embodiments, and none of these embodiments, including when combined with Petitioner’s other art, teach the claims-at-issue. Petitioner’s claim-element analysis at times appears to conflate these distinct embodiments, which is improper: Harris is not a menu of parts and ideas; it is a disclosure of particular systems. Ex. 2002 [Conte Decl.] ¶¶ 59-72. Petitioner should not be allowed to smuggle improper “common sense” reasoning or unsupported combinations of disclosures by silently conflating them.

First, to the extent that that Petitioner relies on some such implied,

unarticulated “common sense” that would supposedly have steered a POSITA away from the teachings of Petitioner’s own art and in the direction of the claimed approach, the law does not allow such hand-waving to invalidate an examined, issued patent. For example:

In cases in which “common sense” is used to supply a missing limitation, as distinct from a motivation to combine, moreover, our search for a reasoned basis for resort to common sense must be searching. And, this is particularly true where the missing limitation goes to the heart of an invention.

Arendi S.A.R.L. v. Apple, Inc., 832 F.3d 1355, 1363 (Fed. Cir. 2016); *see also, e.g., DSS Tech. Mgm’t v. Apple Inc.*, 885 F.3d 1367, 1374-75 (Fed. Cir. 2018) (rejecting “ordinary creativity” as basis for overcoming missing limitation). Petitioner has failed to provide such a “reasoned basis.”

Second, Petitioner has failed to establish that a POSITA would have combined Harris’s distinct embodiments, or why a POSITA would have done so. Indeed, Harris’s SDDT, “failure mode,” and “low power feature” embodiments are distinct embodiments. A POSITA would understand that any one of them could be implemented without the others. Ex. 2002 [Conte Decl.] ¶¶ 35-39. For example, Harris’s embodiments differ significantly in how they use Harris’s separate voltage planes. The SDDT embodiment uses the Vstby plane to “determine the amount of current being used by a given RAM block when isolated from all other circuitry.”

Ex. 1003 [Harris] 3:4-5, 29-49. By contrast, the “failure mode” embodiment uses the Vstby plane “to power the memory 106 to sustain memory contents when either main or VDD power is failing.” *Id.*, 3:58-59. The “low power feature,” on the other hand, uses the Vstby and VDD planes to provide one voltage to a memory and another, different voltage to a CPU.

As another example, the embodiments are intended for different objectives and different uses cases. As described by Dr. Conte:

For example, the “low power feature” embodiment presumes that the memory and the CPU are on separate voltage planes: that is how they receive separate, independently adjusted voltages. Accordingly, in the event of a voltage failure, the “low power feature” would have nothing to do: the system is already isolating a portion of the chip from the failure.

Second, the “failure mode” embodiment contemplates at least two independent power supplies: “a battery back-up source” and “main or VDD power,” the second of which a POSITA would understand typically to be an unconstrained supply such as a wall socket. Ex. 1003 [Harris], 3:60-61. On the other hand, the “low power mode” embodiment, a POSITA would understand, is meant for mobile, battery-powered operation, when the system is connected to just one power source (such as a battery) constrained by capacity (or “battery life”).

During battery-powered operation, a typical system would lack a second power source: it would already be using its battery to provide

the independently adjusted VDD and Vstby voltages in the manner described. Accordingly, Harris’s “failure mode,” which contemplates “main or VDD power . . . failing,” would have no application in the “low power feature” because there *is* no second voltage source that could be used as a “back-up.” Instead, both of these voltage planes in the “low power feature” would receive their power from the battery. In the event of battery failure, the system would lack an alternate supply.

Ex. 2002 [Conte Decl.] ¶¶ 41-43.

In fact, Harris expressly states that the “low power feature” is not “specifically set out and described above,” *i.e.* in the specification’s discussion of the SDDT and “failure mode” embodiments. Ex. 1003 [Harris] 4:59-63. It also expressly distinguishes between the SDDT and “failure mode” embodiments: “One function being a VDD failure mode . . . , and the other mode being software controlled mode which allows for testing of soft defects using an external SDDT current measurement.” *Id.*, 3:64-4:3.

To the extent Petitioner argues that Harris’s teachings about using its switch in the SDDT and “failure mode” embodiments would have been applied to the “low power feature” embodiment, Petitioner has failed to provide a reason why a POSITA would have been motivated to combine distinct embodiments.

E. Petitioner Fails To Set Forth A Clear And Consistent Account Of Its Harris/Zhang Combination.

Petitioner’s combination should be rejected for the additional reason that

Petitioner fails to provide a consistent account of how the limitations are met. For multiple limitations, Petitioner relies upon Harris's VDD (allegedly the "first regulated voltage") failing (Harris's "failure mode"). Petitioner, however, contends that a POSITA would be motivated to add Zhang's voltage regulators to Harris to convert VDD from an unregulated voltage into a "regulated voltage." Assuming, *arguendo*, that a POSITA would be so motivated, Petitioner fails to prove that Harris's now-regulated VDD would continue to fail under its proffered modification. Consequently, Petitioner fails to demonstrate that Harris's "failure mode" would even be present in the combined system.

Petitioner, again, relies upon Harris's VDD and Vstby as the "first" and "second" voltages, respectively. Pet., 35-36, 40. Petitioner contends a POSITA would be motivated to combine these supply voltages with Zhang's voltage regulators to convert VDD and Vstby into "regulated" voltages. Pet., 37-40.

Petitioner relies extensively and, for at least one limitation present in each claim, exclusively on Harris's VDD failing and, consequently, "drop[ping] below a set level or threshold." Ex. 1003 [Harris] 3:54-4:3; Pet., 34-36. Petitioner also relies on VDD failing for limitations 1[c], [d], [g], [h], and [i]. Pet., 30-31, 34, 42-43, 43-44, 57-59 (claim 9). Indeed, for limitation 1[h], Petitioner relies *exclusively* upon VDD failing. *Id.*, 43-44.

Though Petitioner relies heavily upon VDD failing, if Harris's voltages were

regulated per Zhang as proposed, Petitioner fails to prove that such regulated voltages would “fail” or “drop below a set level or threshold.” Per Petitioner, a voltage regulator provides a “stable, precise voltage” (Pet., 37)—not a voltage that is failing. In accord, (Intel’s) expert, Dr. Singh indicates that “a voltage regulator provides a stable and precise voltage.” Ex. 1002 [Singh Decl.] ¶ 84 (citing Ex. 1024, 2269); *id.*, (a POSITA “would have been motivated to use a voltage regulator as taught by Zhang to provide a stable voltage (for each of VDD and VSTBY) during operation.”).

Thus, per Petitioner, the very purpose of adding a voltage regulator would be to convert Harris’s VDD and Vstby into *stable* voltages. Petitioner does not identify any situation in which the output voltage of a voltage regulator can fail, *e.g.*, as in Harris’s failure mode.

Certainly, the Zhang voltage regulators 251-254 relied upon (Pet., 36) do not output a failing voltage. They are, rather, “set to a value ... to meet a timing requirement ...” Ex. 1004 [Zhang] [0028]. Zhang’s voltage regulators—that maintain a voltage or vary it in a controlled manner—are prototypical and consistent with numerous technical dictionary definitions. Petitioner’s Exhibit 1024 confirms that a voltage regulator is “a device that *maintains the terminal voltage* of a ... voltage source *within required limits* ...” Ex. 1024 [McGraw-Hill Dictionary] 2269 (cited at Pet., 37); *see also* Ex. 2018 [Oxford Dictionary] 519

(similar); Ex. 2019 [Microsoft Computer Dictionary] 558 (similar); Ex. 2020 [Newton's Telecom Dictionary] 936 (similar).

Thus, if Zhang's voltage regulators were combined with Harris, per Petitioner's combination, Petitioner fails to demonstrate that VDD would still fail and, thus, Petitioner has not shown how it can rely upon Harris's VDD failing as it does for so many of the key limitations in question.

Petitioner's failure to address this inconsistency should prove fatal. The Board routinely rejects grounds that rest upon inconsistent arguments. *See. e.g., Facebook, Inc. v. Uniloc USA, Inc.*, IPR2017-01524, Paper 7, 19 (Dec. 4, 2017) (We will not, and cannot, piece together Petitioner's inconsistent and contradictory arguments into a cogent and coherent explanation that supports an obviousness showing."); *Denso Corp. v. Collision Avoidance Techs. Inc.*, IPR2017-01715, Paper 7, 56-57 (Jan. 23, 2018) (similar); *Coherus BioSciences, Inc. v. Hoffman-LaRoche Inc.*, IPR2017-02066, Paper 11, 14 (Mar. 9, 2018) (similar); *Xilinx, Inc. v. PLL Techs., Inc.*, IPR2015-00148, Paper 8, 29-31 (Apr. 28, 2015) (similar).

F. Objective Considerations Of Non-Obviousness Support Rejecting The Petition.

"The objective indica of non-obviousness play an important role as a guard against the statutorily proscribed hindsight reasoning in the obviousness analysis." *WBIP, LLC v. Kohler Co.*, 829 F.3d 1317, 1328 (Fed. Cir. 2016); *Stratoflex, Inc. v.*

Aeorquip Corp., 713 F.2d 1530, 1538 (Fed. Cir. 1983) (“evidence of secondary considerations may often be the most probative and cogent evidence in the record.”). Here, secondary considerations, including commercial success, strongly support a finding of non-obviousness.

Significant for our purposes, both the Federal Circuit and the Board have relied upon an infringement verdict to find objective indica of non-obviousness, such as commercial success. *WBIP*, 829 F.3d at 1330 (“WBIP presented evidence on ... the commercial success of low-carbon monoxide gen-sets, including [accused infringer’s] gen-sets, that incorporate the patented technology.”), 1337 (finding commercial success); *RTI Surgical, Inc. v. LifeNet Health*, IPR2019-00571, Paper 75, 46-47 (PTAB Aug. 4, 2020) (finding nexus via infringement verdict).

Here, the jury awarded \$1.5 billion in damages for Intel’s infringement of the ’373. Ex. 1007 [Verdict] 6; *cf Ecolochem, Inc. v. Southern Cal. Edison Co.*, 227 F.3d 1361, 1377-8 (Fed. Cir. 2000) (commercial success found where invention generated “almost \$13 million in revenue”); *Merck & Co. v. Teva Pharms. USA, Inc.*, 395 F.3d 1364, 1376 (Fed. Cir. 2005) (when “a product attains a high degree of commercial success, there is a basis for inferring that [attempts to a solution] have been made and have failed.”). “Our caselaw provides that the success of an infringing product is considered to be evidence of the commercial success of the claimed invention.” *Brown & Williamson Tobacco Corp. v. Phillip*

Morris Inc., 229 F.3d 1120, 1130 (Fed Cir. 2000).

There is, moreover, an undeniable nexus between the damages awarded and the claimed invention. Intel's products were found to infringe and the damages awarded were determined based upon the value of the patented inventions. The jury was repeatedly instructed to determine damages solely based upon the value of the patented inventions apart from any unpatented features. Ex. 2021 [Jury Instructions] 1,544:14-16 ("You must be careful to ensure that award is no more and no less than the value that the patented inventions have provided to Intel."); 1,545:13-1,546:9 ("The reasonable royalty award must be based on the incremental value that the patented invention adds to the end product. ...Any amount of damages must be based on the value attributable to the patented invention as distinct from unpatented features of the accused products..."). At trial, the jury heard that Intel sold nearly a billion products that infringed the '759 and '373 patents. *Id.*, 1,623:8-11. The jury has already found that Intel's infringement of the '373's claimed inventions were worth \$1.5 billion in value, attributable solely to the patented features, commercial success by any definition.

IV. CONCLUSION

For each of the foregoing reasons, the Board should not institute trial.

Respectfully submitted,

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Dated: October 27, 2021

CERTIFICATE OF COMPLIANCE

Pursuant to 37 C.F.R. § 42.24(d), counsel for Patent Owner VLSI Technology LLC certifies that this document complies with the type-volume limitation of 37 C.F.R. § 42.24(b). According to Microsoft Office Word's word count, this document contains approximately 13,405 words, including any statement of material facts to be admitted or denied in support, and excluding the table of contents, table of authorities, mandatory notices under § 42.8, exhibit list, certificate of service or word count, or appendix of exhibits or claim listing.

Dated: October 27, 2021

By: / Babak Redjaian /

CERTIFICATE OF SERVICE

I hereby certify that, pursuant to 37 C.F.R. § 42.6(e) and with the agreement of counsel for Petitioner, true and correct copies of **PATENT OWNER'S PRELIMINARY RESPONSE** and **EXHIBITS 2002-2023** are being served electronically on October 27, 2021, to the persons below:

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