



SOLID-STATE CIRCUITS

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A PUBLICATION OF THE IEEE SOLID-STATE CIRCUITS COUNCIL

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A 10-GHz 8-b Multiplexer/Demultiplexer Chip Set for the SONET STS-192 System

Kenji Ishida, Hirotugu Wakimoto, Kunio Yoshihara, Mitsuo Konno, Shoichi Shimizu, Yoshiaki Kitaura, Kenichi Tomita, Takashi Suzuki, and Naotaka Uchitomi

Abstract—An ultrahigh-speed 8-b multiplexer (MUX) and demultiplexer (DMUX) chip set has been developed for the synchronous optical network (SONET) next-generation optical-fiber communication systems, which will require data bit rates of about 10 Gb/s. These IC's were designed using three novel concepts: a tree-type architecture giving reliable operation, a dynamic divider with a wide operating range, and a 50- Ω on-chip transmission line with high-speed pulse propagation. They were fabricated using a 0.5- μ m W_N -gate GaAs MESFET process. The DMUX and MUX operated up to 10.4 and 11.4 GHz, respectively, both with an adequate phase margin of more than 230°.

I. INTRODUCTION

IN CURRENT optical-fiber communication systems, the data bit rate is 2.49 Gb/s. Higher data bit rates will be required for future increases in transmission capacity. An ultrahigh-speed data rate of 9.95 Gb/s is expected to be required for the optical-fiber communication systems associated with the synchronous optical network (SONET) STS-192 [1]. Fig. 1 shows an example of multiplexing and demultiplexing stages for the STS-192 system, which allows four-channel transmission with 2.49-Gb/s data rates. In this system, the 8-b multiplexer (MUX) and demultiplexer (DMUX) chip set is indispensable for byte interleaving. High-speed multibit (more than 8 b) MUX and DMUX chip sets have been reported [2]–[4]; however, a chip set with both 8-b signal processing and 10-GHz operation has not yet been reported.

This paper describes an ultrahigh-speed GaAs 8-b MUX and DMUX chip set as a key component of next-generation optical-fiber communication systems. This 8-b MUX and DMUX chip set, operating up to 10 GHz, features a tree-type architecture giving reliable operation, a dynamic divider with a wide operating range, and a newly developed 50- Ω on-chip transmission line (LGCL) with high-speed pulse propagation, in conjunction with an optimized 0.5- μ m W_N -gate GaAs MESFET process.

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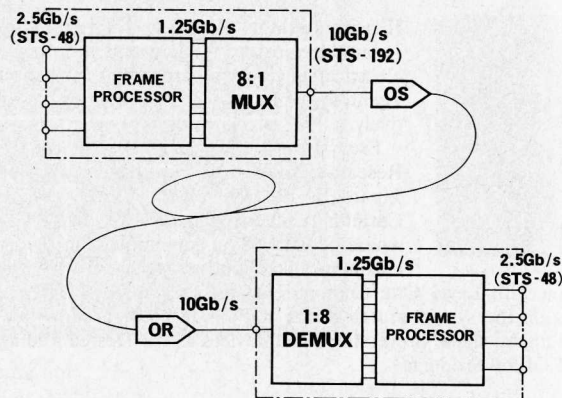


Fig. 1. Example of STS-192 system.

II. CIRCUIT DESIGN

A. Circuit Description

Both MUX and DMUX integrated circuits are implemented with the tree-type architecture and a dynamic divider in order to guarantee stable operation at 10 GHz, as shown in Figs. 2 and 3.

In Fig. 2, the 8-b MUX is realized with a 2-b MUX tree and a 1/8 counter with 1/2 dynamic divider front end. The 2-b MUX is composed of a phase-shifting D-type flip-flop (PS), a master-slave D-type flip-flop (MS), and a 2-b selector (SEL). The selectors for the first and second stages are integrated with the second- and third-stage MS and PS circuits (SMS and SPS). The SMS and SPS are constructed by using a three stacked gate structure [5]. The MS is paired with the PS in each 2-b MUX to increase the timing margin of the selector [6]. The eight-parallel input data streams have a data rate of 1.25 Gb/s. These data streams are multiplexed by 2-b MUX's in the first stage, resulting in four data parallel streams with data rates of 2.5 Gb/s. Similarly, the second and third stages use 2-b MUX's to generate a single output data stream with 10 Gb/s.

Fig. 3 shows a block diagram of the 8-b DMUX, with a 2-b DMUX tree, a 1/8 counter with dynamic divider front end, and a frame shifter. The 2-b DMUX is composed of the MS and the PS, and the PS is created by adding a slave stage to the MS in order to align the output signals. The frame shifter consists of five XOR gates and four selectors for the tree-type architecture.

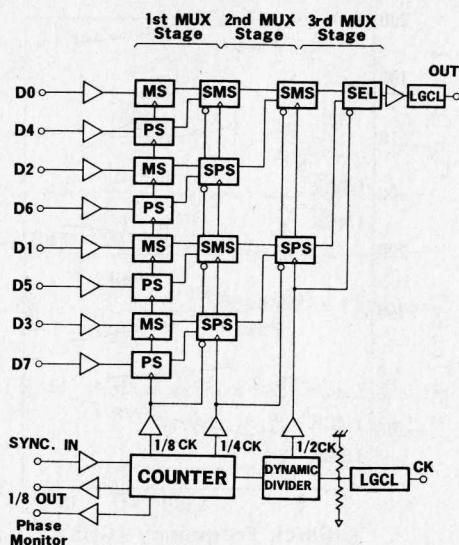


Fig. 2. Block diagram of 8-b MUX. MS: master-slave D flip-flop (DFF); PS: phase-shifting DFF; SMS: MS with 2-b selector; SPS: PS with 2-b selector; LGCL: ladder grounded coplanar line; SEL: 2-b selector.

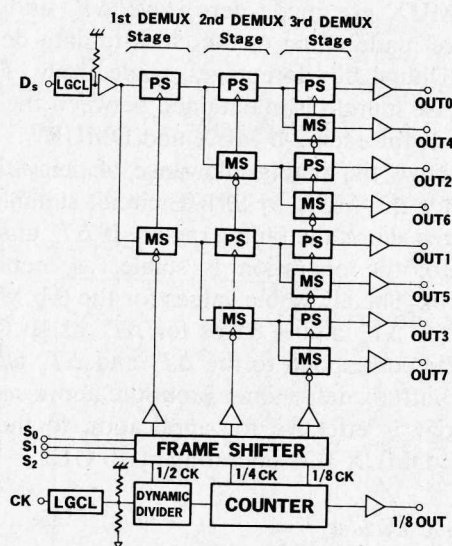


Fig. 3. Block diagram of 8-b DMUX.

The frame shifter rearranges the state of eight parallel output terminals (OUT0–OUT7) by changing a set of select signals (S_0 , S_1 , and S_2).

Both IC's use source-coupled FET logic (SCFL) to implement the master and slave latches as shown in Fig. 4. The logic swing voltage ΔV and threshold voltage V_{th} were determined to be 0.9 and -0.2 V, respectively, in order to maintain a noise margin larger than 0.35 V [5]. The FET gate widths in the flip-flops are determined to be 18, 10, and $4 \mu\text{m}$ for the $1/2\text{CK}$, $1/4\text{CK}$, and $1/8\text{CK}$ flip-flops, respectively, so as to realize both high-speed operation and low power consumption. The final stage of the output buffer used an open drain for the MUX and a source follower for the DMUX. The MUX input and the DMUX output levels and the supply voltage were designed to be ECL compatible, that is, to drive a $50\text{-}\Omega$ load

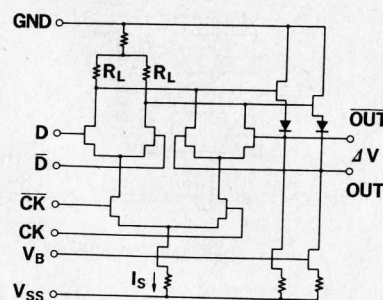


Fig. 4. SCFL circuit configuration.

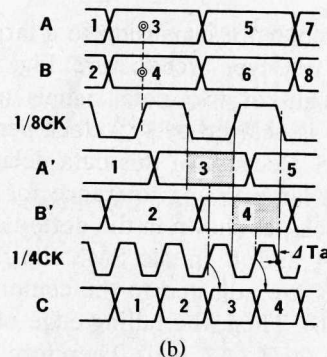
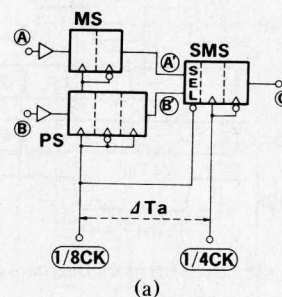


Fig. 5. Two-bit multiplexer: (a) block diagram, and (b) timing chart.

resistor at ECL logic levels (-1.3 ± 0.45 V) and operate on a -5.2 ± 0.5 -V supply voltage.

B. 2-b MUX / DMUX Unit

Two problems must be taken into consideration when designing a MUX with tree-type architecture. First, precise control of the phase difference between the clock and input data signals for the 2-b selector is required. Here, a phase-shifting flip-flop (PS) was introduced to solve this problem [6]. The second problem is to ensure data latch because each stage flip-flop operates with different clocks. Thus, the timing relationships among three different clocks should be strictly determined to ensure reliable operation of the tree-type architecture.

Fig. 5(a) shows a block diagram of the 2-b MUX units. The selector is shown combined with the next-stage master-slave D-type flip-flop (SMS) as previously described. The timing relationships between clocks and signals must be taken into consideration to realize stable operation in this configuration. In particular, the delay time ΔT_a between the $1/8\text{CK}$ and the $1/4\text{CK}$ clock signals is an

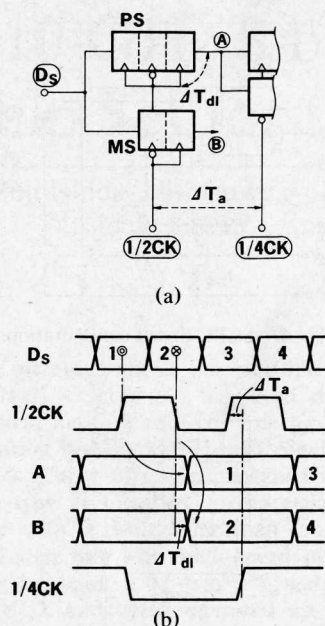


Fig. 6. Two-bit demultiplexer: (a) block diagram, and (b) timing chart.

important parameter for expansion to a larger number of channels in the tree-type architecture. Fig. 5(b) shows the timing relationship of two data signals and two clock signals. Data B is delayed by $1/2$ clock period from data A due to the PS. Because of this data delay, the selector operates with a large timing tolerance for both negative and positive clocks, as shown in the dotted areas. In order to latch data A and B in the SMS flip-flop, the rising edges of $1/4CK$ are adjusted to the center of the dotted areas in Fig. 5(b). Then, the falling edge of $1/8CK$ is set to the edge of $1/4CK$ ($\Delta T_a = 0$). Therefore, this 2-b MUX with MS and PS D-type flip-flops has an important advantage over a conventional circuit without phase adjustment [7], [8].

Fig. 6(a) and (b) shows a block diagram and a timing diagram of the 2-b DMUX unit, respectively. The input data D_s are separated by the complementary pulse of $1/2CK$, and the output data A have the same phase as B due to the PS. Since the data A and B are delayed by ΔT_{dl} compared with the falling edge of $1/2CK$, as shown in Fig. 6(b), the delay time ΔT_a between $1/2CK$ and $1/4CK$ is made equal to ΔT_{dl} in order to maintain a large phase margin for the next stage of the 2-b DMUX unit.

C. Timing Relation of 8-b MUX / DMUX

The same timing relations can be applied to the 8-b MUX and DMUX. In the 8-b MUX and DMUX, there are three clock signals, as shown in Figs. 2 and 3, respectively. Hence, two interclock delay times (ΔT_a and ΔT_b) must be adjusted in order to maintain a large phase margin, where ΔT_a denotes delay time between $1/8CK$ and $1/4CK$ for the MUX and between $1/2CK$ and $1/4CK$ for the DMUX, and ΔT_b is the delay time between $1/4CK$ and $1/2CK$ for the MUX and between $1/4CK$ and $1/8CK$ for the DMUX. Each timing delay is precisely

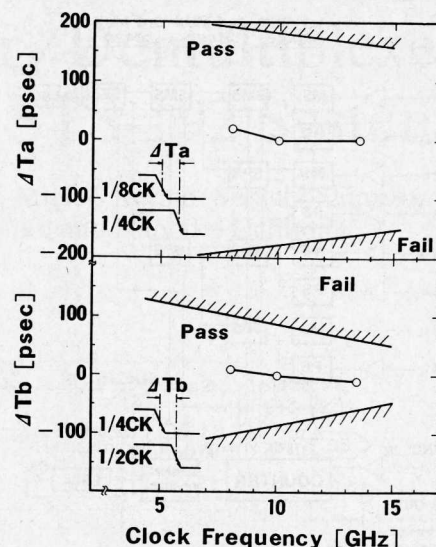


Fig. 7. Timing allowance of delay time, ΔT_a and ΔT_b , as a function of clock frequency.

adjusted using the delay of the buffer as follows: ΔT_a and ΔT_b for MUX are made zero, and ΔT_a and ΔT_b for DMUX are made equal to the clock-to-data delays ΔT_{dl} in the individual flip-flop stages, respectively. Therefore, a large phase margin is maintained between the data and clock signals for each 2-b MUX and DMUX.

Fig. 7 shows the timing allowance of delay times ΔT_a and ΔT_b for the MUX by SPICE circuit simulation. The hatched area shows the failing region. If ΔT_a and ΔT_b are set to zero, the operation is stable, as mentioned in Section II-B. The allowable values for the 8-b MUX were ± 180 ps for ΔT_a and ± 80 ps for ΔT_b at 10 GHz. The open circles correspond to the ΔT_a and ΔT_b adjusted by using the buffer's delay time. From the above results, this methodology is effective for application to the multibit MUX and DMUX IC's operating at 10 GHz.

D. Dynamic Divider

The high-speed counters in the MUX and DMUX IC's require an adequate frequency margin for stable operation at clock frequencies above 10 GHz. The dynamic divider, which meets the requirement for a 10-GHz input stage in the counter, is therefore used [9]–[11].

The fundamental circuit configuration of the $1/2$ dynamic divider is shown in Fig. 8. SCFL circuits were used as buffer amplifiers because of supply voltage compatibility. This divider was designed for a wide operating range by optimizing the FET gate widths of the buffer amplifier and transfer gate. Furthermore, a source-follower stage is adopted in front of the output buffer to reduce load capacitance. Fig. 9 shows maximum operating frequency f_{max} as a function of the W_{gt}/W_{gb} ratio, where W_{gt} and W_{gb} are the FET widths for the transfer gate and the buffer amplifier, respectively. The parameter shows the number of gate fingers in the transfer gates and buffers, which have $18\text{-}\mu\text{m}$ gate width as a basic width. The MESFET's have a threshold voltage of -0.2 V and the

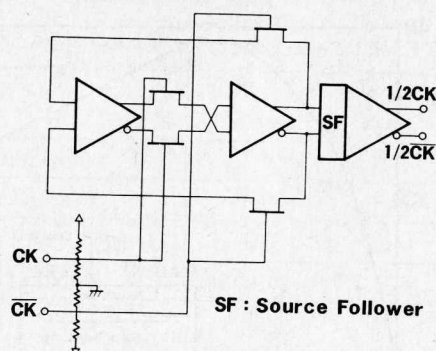


Fig. 8. Block diagram of 1/2 dynamic divider.

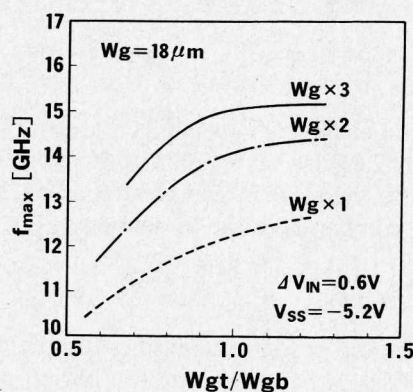
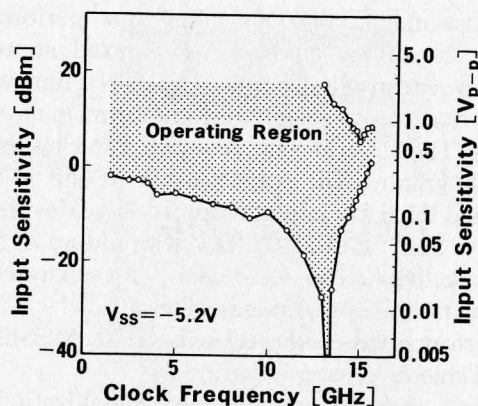
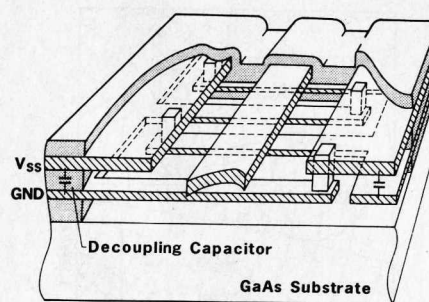
Fig. 9. Maximum operating frequency as a function of W_{gt}/W_{gb} ratio. The parameter is the number of buffer gate fingers.

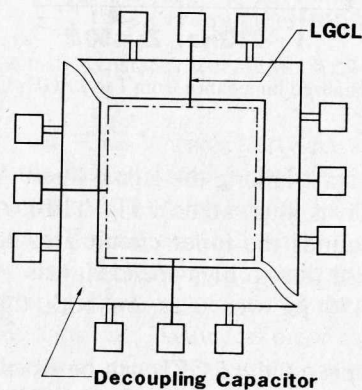
Fig. 10. Input sensitivity as a function of clock frequency.

logic swing is 1.1 V. The input voltage amplitude and the gate width of the source-follower stage were maintained at 0.6 V and 10 μm , respectively. In this figure, f_{max} increases with increasing W_{gt}/W_{gb} ratio. This is caused by the enhanced transconductance of the transfer gates. When the W_{gt}/W_{gb} ratio is larger than 1.0, the f_{max} shows a tendency to saturate. The phenomenon is more pronounced for the large buffer ($W_g \times 3$). On the basis of the above results, the gate width of both the transfer gate and buffers was selected to be 54 μm (18 $\mu\text{m} \times 3$).

Fig. 10 shows the measured data for the test device. This divider can operate from 1.5 to 15 GHz and has



(a)



(b)

Fig. 11. (a) Ladder grounded coplanar line with decoupling capacitor. (b) Chip layout image for using LGCL.

sufficient input sensitivity for the initial 1/2 divider in the MUX and DMUX IC's.

III. LAYOUT DESIGN

Impedance matching is becoming important for ultra-high-speed digital circuits as well as for analog circuits. In particular, there are three requirements for high-speed signal lines on chip: impedance matching, suppression of crosstalk, and power-line noise. The impedance of high-speed I/O ports must match those of the external systems in order to suppress pulse reflection and distortion. To solve these problems, a novel 50- Ω on-chip transmission line, named the ladder grounded coplanar line (LGCL), has been employed for the high-speed signal lines for the clock, MUX output, and DMUX input, as shown in Figs. 2 and 3. As for the DMUX input line and the clock (CK) lines for MUX and DMUX, on-chip termination resistors are placed at the other end of the LGCL in order to propagate the signals without the pulse reflection and distortion.

An LGCL is constructed of two segments with a microstrip line and a coplanar line. This LGCL can be quite freely designed and fabricated by using the two-layer interconnection without back metals. Fig. 11(a) shows the structure of the LGCL with a decoupling capacitor. The second-metal high-speed signal line is placed over the ladder-shape grounded first metal. The decoupling capacitor has a metal-insulator-metal structure and is laid down at both sides of the LGCL to prevent power-line

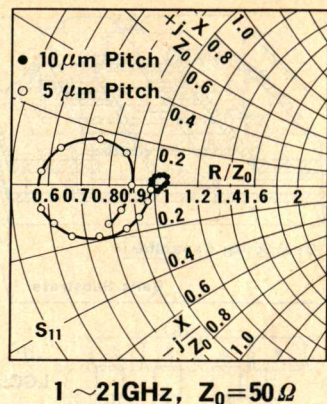


Fig. 12. Normalized impedance from 1 to 21 GHz ($Z_0 = 50 \Omega$).

noise and crosstalk among the signal lines. A chip layout with this LGCL is illustrated in Fig. 11(b). A decoupling capacitor surrounds the inner circuit area to absorb the power-line noise due to high-speed signals. A decoupling capacitor of 150 pF was used on both the MUX and DMUX chips.

The impedance of the LGCL can be exactly controlled by changing the second-metal (signal line) width and first-metal (ground line) width and pitch. Fig. 12 shows the measured data for the LGCL impedance from 1 to 21 GHz. The first-metal and second-metal widths were fixed at 2.5 and 10 μm , respectively, while the first-metal pitch was varied as a parameter. In 5- μm -pitch LGCL (open circles), the impedance strayed from 50 Ω because of the large shunt capacitance. On the other hand, the 10- μm -pitch LGCL (closed circles), which has the optimized capacitor, attained a constant impedance of 50 Ω up to 21 GHz. Therefore, the 10- μm -pitch LGCL was employed as an on-chip signal line.

IV. FABRICATION PROCESS

A. 0.5- μm FET Design

The MUX and DMUX were fabricated using 0.5- μm WN_x -gate GaAs buried p-layer LDD MESFET's with a shallow n-channel layer as shown in Fig. 13 (inset) [12].

In order to obtain maximum cutoff frequency at the target threshold voltage, it is important to determine the optimum ion-implantation energies and dosages for both the n-channel layer and buried p-layer. The buried p-layer dosage was determined by using a two-dimensional device simulator [13] with fixed Mg and Si ion-implantation energies. The Mg ion-implantation energy was fixed at 180 keV to surround the source/drain n^+ regions and Si ion-implantation energy was fixed at 25 keV in order to form a shallow channel layer.

Fig. 13 shows the simulated result for the cutoff frequency f_T as a function of Mg dosage. The threshold voltage of -0.2 V was kept constant through this simulation. f_T increases with increasing Mg dosage because of the enhanced transconductance due to the suppression of

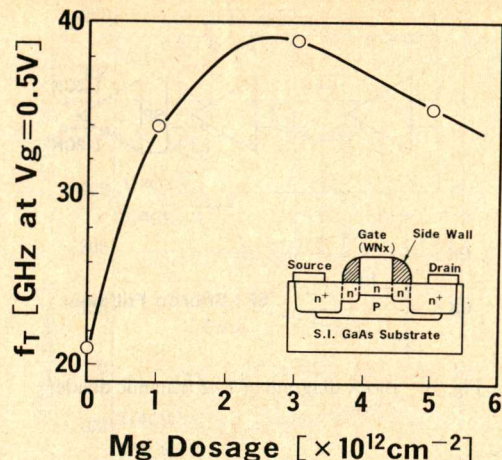


Fig. 13. Cutoff frequency f_T as a function of Mg dosage.

the short-channel effect. Further increases in Mg dosage to more than $2.0 \times 10^{12} \text{ cm}^{-2}$ led to a reduction in f_T , because of the increase in gate-source capacitance and gate leakage current for large Si dosages.

B. Process Conditions

The fabrication process conditions for the MUX and DMUX chip set were as follows: the buried p-layer was formed by Mg ion implantation at 180 keV with a dose of $2.0 \times 10^{12} \text{ cm}^{-2}$ as mentioned above. An n-channel layer was then formed by Si ion implantation at 25 keV with a dose of $8.0 \times 10^{12} \text{ cm}^{-2}$ into undoped semi-insulating 3-in wafers. Post-implantation annealing was performed at 820°C for 20 min in an Ar+AsH₃ mixed atmosphere without any encapsulating film. The WN_x film was deposited by reactive RF magnetron sputtering in an Ar + N₂ mixed gas. The 0.5- μm gate was patterned by modified optical lithography. The source/drain n' and n^+ layers were formed by Si ion implantation at 45 keV with a dose of $1.3 \times 10^{13} \text{ cm}^{-2}$ and at 110 keV with a dose of $5 \times 10^{13} \text{ cm}^{-2}$, respectively. The n^+ region was separated from the gate metal by a 0.3- μm -long sidewall.

The performance of the 0.5- μm GaAs MESFET's is listed in Table I.

First- and second-interconnection metallizations were Ti/Pt/Au. The Au film thickness differed between the first (0.4 μm) and second (1.0 μm) levels, resulting in sheet resistivities of $\rho_s = 0.07 \Omega/\square$ for the first level and $\rho_s = 0.03 \Omega/\square$ for the second level. The interlayer insulating film and passivating film were 0.6- μm -thick SiO₂ and 0.5- μm -thick SiON, respectively. The first-metal insulator second-metal structure distributed capacitance was 0.1 fF/ μm^2 .

Both MUX and DMUX IC's were 3×3 mm². Fig. 14 shows a photomicrograph of the DMUX IC chip, in which approximately 1800 circuit elements are integrated. The inner circuit is surrounded by the decoupling capacitor, composed of a metal-insulator-metal structure. The LGCL was used for DMUX input, MUX output, and clock signal lines.

TABLE I
PERFORMANCE OF 0.5- μm GaAs MESFET's

	Average	Standard Deviation
L_g (μm)	0.50	0.02
V_{th} (mV)	-160	40
K (mS/V \cdot mm)	424	18
f_T (GHz)	40 (at $V_g = 0.4$ V, $V_d = 1$ V)	

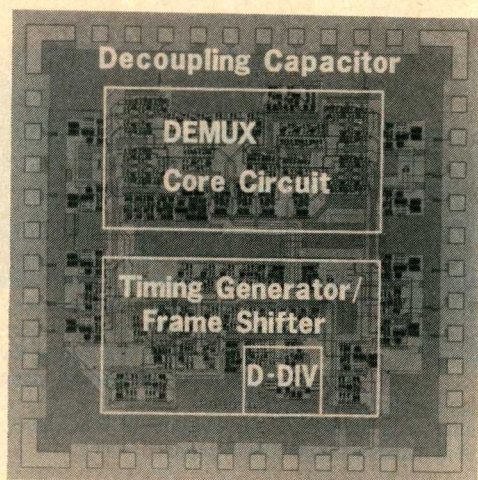
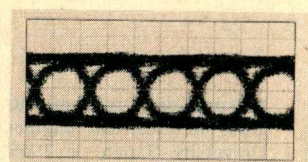
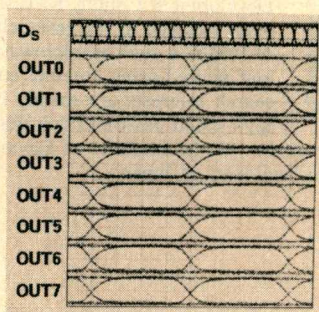


Fig. 14. DMUX photomicrograph.



(a)



(b)

Fig. 15. Operating waveforms at 10 GHz: (a) MUX (0.2 V/div, 50 ps/div), and (b) DMUX (0.5 V/div, 200 ps/div).

V. CHIP PERFORMANCE

High-speed device testing was performed directly on the wafer using a gigahertz-probe system. Fig. 15(a) shows the output waveforms of the MUX operating at 10 Gb/s. An error rate of less than 10^{-10} was confirmed by using a pseudorandom signal with a word length of 2^7-1 . The IC power consumption was 3.8 W including the I/O internal

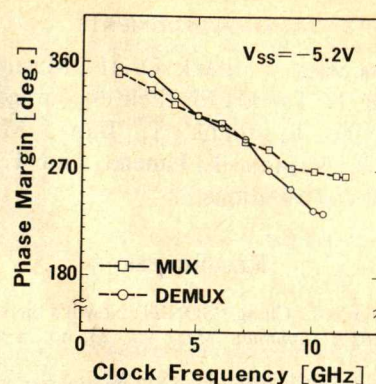


Fig. 16. Phase margin characteristics for MUX(\square) and DMUX(\circ).

circuit at a V_{ss} of -5.2 V. Note that very stable high and low levels in the output signal voltage were maintained. This is attributed to the effects of the LGCL and decoupling capacitor. The rise and fall times defined between 20 and 80% were 35 and 31 ps, respectively. Fig. 15(b) shows the input/output waveforms of the DMUX for a 10-Gb/s input data rate. Again, an error rate of less than 10^{-10} was measured using a pseudorandom signal with a word length of $2^{15}-1$. The IC power consumption of the DMUX was 3.8 W.

Fig. 16 shows the phase margin between the data and the clock signals of the MUX and DMUX. The phase margin is an important characteristic of these high-speed devices used in this system. The MUX and DMUX operated from 1.5 GHz up to 11.4 and 10.4 GHz, respectively. These speeds were limited by the maximum frequencies of the measurement instruments. The phase margins of the MUX and DMUX are denoted by squares and circles, respectively. The phase margin of both MUX and DMUX is 230° even at 10 GHz. This result shows that these MUX and DMUX have phase margins that are sufficient for next-generation optical-fiber communication systems with an ultrahigh-speed data rate of 10 Gb/s.

VI. CONCLUSION

An ultrahigh-speed GaAs 8-b MUX and DMUX chip set has been designed and fabricated with the following features:

- 1) a tree-type architecture which gives reliable operation;
- 2) a dynamic divider with a wide operating range;
- 3) a novel 50- Ω transmission line (the LGCL) for high-speed signal ports and on-chip decoupling capacitor; and
- 4) an optimized 0.5- μm GaAs MESFET process.

Very stable operation at 10 GHz with a phase margin of more than 230° was realized, thus proving the applicability of these IC's to future optical-fiber communication systems (STS-192) as key devices.

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