

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

SAMSUNG ELECTRONICS CO., LTD.
Petitioner

v.

LED WAFER SOLUTIONS LLC
Patent Owner

Patent No. 9,502,612

**DECLARATION OF R. JACOB BAKER, PH.D., P.E.
IN SUPPORT OF PETITION FOR *INTER PARTES* REVIEW
OF U.S. PATENT NO. 9,502,612**

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I, R. Jacob Baker, Ph.D., P.E., declare as follows:

I. INTRODUCTION

1. I have been retained by Samsung Electronics Co., Ltd. (“Petitioner”) as an independent expert consultant in this proceeding before the United States Patent and Trademark Office (“PTO”) regarding U.S. Patent No. 9,502,612 (“the ’612 patent”) (Ex. 1001).¹

2. I am being compensated at my rate of \$655 per hour for the time I spend on this matter.

3. My compensation is in no way contingent on the nature of my findings, the presentation of my findings in testimony, or the outcome of this, or any other proceeding. I have no other interest in this proceeding.

4. I have been asked to consider whether certain references disclose or suggest the limitations recited in claims 1–9 (“the challenged claims”) of the ’612 patent. My opinions are set forth below.

¹ Where appropriate, I refer to exhibits that I understand are to be attached to the petition for *Inter Partes* Review of the ’612 patent.

II. BACKGROUND AND QUALIFICATIONS

5. I presently serve as a Professor of Electrical and Computer Engineering at the University of Nevada, Las Vegas (UNLV). All of my opinions stated in this declaration are based on my own personal knowledge and professional judgment. In forming my opinions, I have relied on my knowledge and experience in designing, developing, researching, and teaching regarding integrated circuit design, including the design and packaging of light emitting diodes (LEDs) and similar structures.

6. I am over 18 years of age and, if I am called upon to do so, I would be competent to testify as to the matters set forth herein. I understand that a copy of my current curriculum vitae, which details my education and professional and academic experience, is being submitted by Petitioner as Exhibit 1003. The following provides an overview of some of my experience that is relevant to the matters set forth in this declaration.

7. I have been teaching electrical engineering at UNLV since 2012. Prior to this position, I was a Professor of Electrical and Computer Engineering at Boise State University from 2000. Prior to my position at Boise State University, I was an Associate Professor of Electrical Engineering between 1998 and 2000 and Assistant Professor of Electrical Engineering between 1993 and 1998 at the University of Idaho. I have been teaching electrical engineering since 1991.

8. I received my Ph.D. in Electrical Engineering from the University of Nevada, Reno in 1993. I also received a MS and BS in Electrical Engineering from UNLV in 1988 and 1986, respectively.

9. As described in my CV, I am a licensed Professional Engineer and have more than 30 years of industry and academic experience, including extensive experience in the design of LEDs, the packaging of LEDs, and circuits that include LEDs. I was involved with Micron, in the early 2000s, evaluating the acquisition of companies developing LED lighting solutions. Further, I have also used LEDs in the design of sensing instrumentation and my funded research involving light sources for detection and ranging.

10. I have taught courses in integrated circuit design (analog, digital, mixed-signal, memory circuit design, etc.), linear circuits, microelectronics, communication systems, power electronics, and fiber optics. As a professor, I have been the main advisor to over 100 Master's and Doctoral students.

11. I am the author of several books covering the area of integrated circuit design including: DRAM Circuit Design: Fundamental and High-Speed Topics (two editions), CMOS Circuit Design, Layout, and Simulation (four editions), and CMOS Mixed-Signal Circuit Design (two editions). I have authored, and coauthored, more than 100 papers and presentations in the areas of solid-state circuit design, and I am the named inventor on 152 granted U.S. patents.

12. I have received numerous awards for my work, including the Frederick Emmons Terman (the “Father of Silicon Valley”) Award. The Terman Award is bestowed annually upon an outstanding young electrical/computer engineering educator in recognition of the educator’s contributions to the profession.

13. I am a Fellow of the IEEE for contributions to memory circuit design. I have also received the IEEE Circuits and Systems Education Award (2011).

14. I have received the President’s Research and Scholarship Award (2005), Honored Faculty Member recognition (2003), and Outstanding Department of Electrical Engineering Faculty recognition (2001), all from Boise State University. I have also received the Tau Beta Pi Outstanding Electrical and Computer Engineering Professor award four of the years I have been at UNLV.

15. I am not an attorney and offer no legal opinions, but in the course of my work, I have had experience studying and analyzing patents and patent claims from the perspective of a person skilled in the art.

III. MATERIALS REVIEWED

16. The opinions contained in this Declaration are based on the documents I reviewed, my professional judgment, as well as my education, experience, and knowledge regarding LEDs, including the fabrication, packaging, and use of LEDs in various applications.

17. In forming my opinions expressed in this Declaration, I reviewed the following materials (and any other materials that I reference in this Declaration): In forming my opinions expressed in this Declaration, I reviewed the U.S. Patent No. 9,502,612 (“the ’612 patent”) (Ex. 1001); Prosecution History of U.S. Patent No. 9,502,612 (Ex. 1004); U.S. Patent Publication No. 2003/0232455 to Tanaka (“Tanaka”) (Ex. 1005); U.S. Patent No. 7,233,028 to Weeks et al. (“Weeks”) (Ex. 1006); U.S. Patent Publication No. 2007/0284602A1 to Chitnis et al. (“Chitnis”) (Ex. 1007); U.S. Patent No. 7,419,839 to Camras et al. (“Camras”) (Ex. 1008); U.S. Patent No. 6,020,602 to Sugawara et al. (“Sugawara”) (Ex. 1009); U.S. Patent No. 7,928,317 to Atanackovic (“Atanackovic”) (Ex. 1010); U.S. Patent No. 7,224,013 to Herner et al. (“Herner”) (Ex. 1011); U.S. Patent No. 7,371,676 to Hembree (“Hembree”) (Ex. 1012); U.S. Patent No. 6,676,287 to Mathis et al. (“Mathis”) (Ex. 1013); Tritt, Thermal Conductivity: Theory, Properties, and Applications, 2004 (“Tritt”) (Ex. 1014); Kane, Processing and Characterization of Benzocyclobutene Optical Waveguides, IEEE Transactions on Components,

Packaging, and Manufacturing Technology, Part B, Vol. 18, No. 3, pp. 565–571, August 1995 (“Kane1”) (Ex. 1015); Kane, Benzocyclobutene Optical Waveguides, IEEE Photonics Technology Letters, Vol. 7, No. 5, pp. 535–537, May 1995 (“Kane2”) (Ex. 1016); Schubert, Light Emitting Diodes, Second Edition, 2006 (“Schubert”) (Ex. 1017); and any other materials I refer to in this Declaration in support of my opinions.

18. In support of my opinions, I have taken into account how a person of ordinary skill in the art (as defined below in Section IV) would have understood the claims and the specification of the ’612 patent at the time of the alleged invention. My opinions take into account how a person of ordinary skill in the art would have understood the ’612 patent, the prior art to the patent, and the state of the art at the time of the alleged invention.

19. As I discuss in detail below, it is my opinion that certain references disclose or suggest all the features recited in claims 1–9 of the ’612 patent.

IV. PERSON OF ORDINARY SKILL IN THE ART

20. Based on my knowledge and experience, I understand what a person of ordinary skill in the art would have known at the time of the alleged invention. My opinions herein are, where appropriate, based on my understandings as to a person of ordinary skill in the art at that time. In my opinion, based on the materials and information I have reviewed, and based on my experience in the technical areas relevant to the '612 patent, a person of ordinary skill in the art at the time of the alleged invention of the '612 patent would have had at least a bachelor's degree in electrical engineering, or the equivalent, and two or more years of experience with integrated circuit design, including the design and packaging of light emitting diodes (LEDs). More education can supplement practical experience and *vice versa*. I apply this understanding in my analysis herein.

21. My analysis of the '612 patent and my opinions in this declaration are from the perspective of one of ordinary skill in the art, as I have defined it above, during the relevant time frame, which I have been asked to assume is the mid-to-late 2013 timeframe (including the October 7, 2013 filing date of the application from which the '612 patent issued). I have been informed that the '612 patent claims priority to a provisional application filed September 20, 2009 (i.e., in the mid-to-late 2009 timeframe). My analysis of the '612 patent and my opinions in this declaration would be the same whether the relevant timeframe was assumed to be the mid-to-

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late 2013 timeframe or the mid-to-late 2009 timeframe. During these time frames, I possessed at least the qualifications of a person of ordinary skill in the art, as defined above.

V. TECHNICAL BACKGROUND

22. In this section, I discuss the state of the art with respect to certain technologies relevant to the subject matter of the '612 patent.

A. Light Emitting Diodes

23. The light emitted by a light emitting diode (LED) results from the recombination of electrons and holes in the LED. (Ex. 1017, 35.)² More specifically, radiative recombination of an electron and a hole in the LED results in the emission of a photon with energy equal to the bandgap energy of the semiconductor, which can be referred to as “electroluminescence.” (*Id.*) Non-radiative recombination produces heat instead of light and is therefore undesirable in most LED applications. (*Id.*)

24. Improved LED performance can be obtained by enhancing radiative recombination in the LED while reducing non-radiative recombination. (*Id.*, 113.) This can be facilitated through the use of double heterostructures in the LED, where an active region is positioned between two confinement layers. (*Id.*) In such a double heterostructure, which is shown in figure 7.1 below, the concentration of free carriers is increased, which in turn increases the rate of radiative recombination. (*Id.*)

² Citations to Schubert correspond to page numbers in the book.

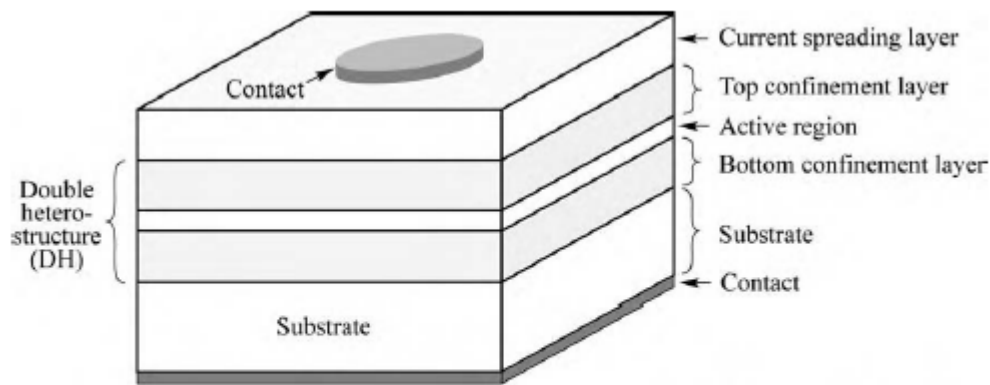


Fig. 7.1. Illustration of a double heterostructure consisting of a bulk or quantum well active region and two confinement layers. The *confinement* layers are frequently called *cladding* layers.

(*Id.*, FIG. 7.1.)

25. The doping levels of the various layers in the LED also impact the efficiency of the LED. (*Id.*, 116, (“Doping of the active region and confinement layers plays a crucial role in the efficiency of double heterostructure (DH) LEDs.”) With respect to the active region, it is typically doped at a relatively low level or left as undoped, intrinsic material. (*Id.*, (“Typically the doping concentration in intentionally doped active regions is either p-type or n-type in the 10^{16} to low 10^{17} cm^{-3} range. Frequently the active layer is left undoped.”).)

26. Because the wavelength of the light emitted by the LED is based on the bandgap energy of the semiconductor material in the LED, different colors of light can be generated using different layers of material in the LED. (*Id.*, 35, 88.) GaInN LEDs were developed in the early 1990s and provide high radiative efficiency for emitting light in the blue and green wavelength range. (*Id.*, 211–212.) Wavelength-

converting materials, such as phosphors, can be used to alter the wavelength of the light generated by the LED. (*Id.*, 348–353.) For example, phosphor powder suspended in an epoxy resin can be formed over a blue-light (short-wavelength) generating LED, where a fraction of the blue light is absorbed by the phosphor and re-emitted as longer-wavelength light. (*Id.*, 353.)

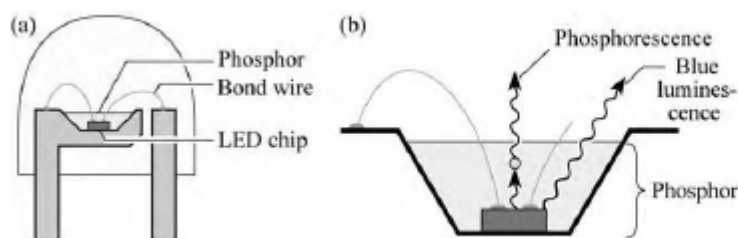


Fig. 21.7. (a) Structure of white LED lamp consisting of a GaInN blue LED chip and a phosphor. (b) Wavelength-converting phosphorescence and blue luminescence (after Nakamura and Fasol, 1997).

(*Id.*, FIG. 21.7.)

27. Current spreading layers, like the one depicted in figure 7.1 above, can be used to improve the light extraction efficiency in LEDs by distributing the current under the top electrode across the top surface. (*Id.*, 127.) In contrast to the electrode, which is often metal and opaque, current spreading layers are transparent, which is why they are often referred to as “window layers.” (*Id.*) “The window layer is the top semiconductor layer located between the upper cladding layer and the top ohmic contact.” (*Id.*)

28. Packaging of LEDs typically includes two electrical leads and a transparent optical window for the light to escape. (*Id.*, 191.) The light extraction efficiency of an LED can be improved by including a dome-shaped encapsulant with

a large refractive index over the LED. (*Id.*, 97.) Such dome-shaped encapsulants can also be used as a lens to control the emission pattern of the LED. (*Id.*) Because LEDs can generate significant heat, thermally conductive paths from the LED to a heatsink are often included in LED packages. (*Id.*, 192–193.) For example, as shown in figure 11.3 below, a heatsink is included to promote extraction of the heat generated by the LED, where the top of the LED is encapsulated by silicone and a plastic lens. (*Id.*)

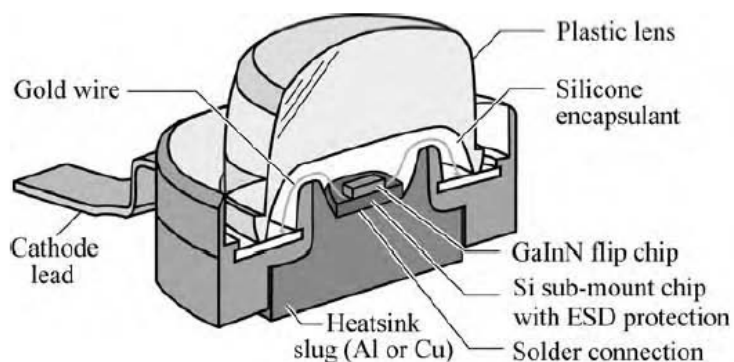


Fig. 11.3. Cross section through high-power package. The heatsink slug can be soldered to a printed circuit board for efficient heat removal. This package, called the *Barracuda package*, was introduced by Lumileds Corp. (adapted from Krames, 2003).

(*Id.*, FIG. 11.3.)

29. As shown in figure 11.3 above, the LED is a “flip chip.” Such “flip chip” LEDs can be grown on sapphire substrates and formed such that both contacts are on the same surface. (*Id.*, 160.) The contacts are initially formed on the top surface of the LED, and then the underlying substrate is either removed or remains when the LED chip is flipped over for mounting contact-side down on another structure. With both of the contacts on the bottom side of the flipped LED chip, the

metal pads do not get in the way of the light being output from the active region of the device, thereby providing better light-emission efficiency. (*Id.*)

VI. OVERVIEW OF THE '612 PATENT

30. The '612 patent relates to “a light emitting diode (LED) device.” (Ex. 1001, 1:21–25; *see also id.*, Abstract, 3:52–4:14.) The '612 patent admits that light emitting diode (LED) devices were conventional and well-known and, with reference to figure 1 below, describes a known prior art Gallium Nitride (GaN) LED device. (*Id.*, 1:29–39, 2:1–3:6, 4:18, 5:4–17, 5:29–45; FIG. 1.)

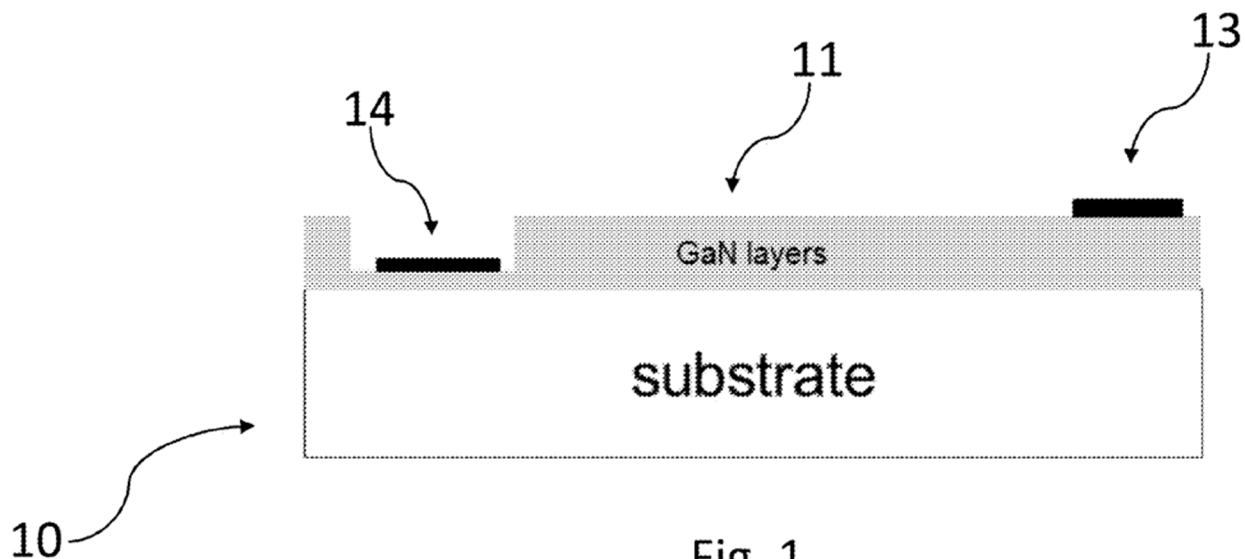


Fig. 1
(Prior Art)

(*Id.*, FIG. 1.)

Modern LED devices are based on semiconducting materials and their properties. For example, some LEDs are made using Gallium Nitride (GaN) which is a type of bandgap

semiconductor suited for use in high power LEDs. Ga LEDs are typically epitaxially grown on a sapphire substrate. These LEDs comprise a P-I-N junction device having an intrinsic (I) layer disposed between a N-type doped layer and a P-type doped layer. The device is driven using suitable electrical driving signals by way of electrodes or contacts coupled to the N and the P type portions of the LED. Electronic activity causes the emission of visible electromagnetic radiation (light) from the intrinsic portion of the device according to the electromotive force applied thereto and configuration of the device.

(*Id.*, 5:4–17.)

31. The prior art GaN LED chip 10 of figure 1 includes GaN layers 11 grown on a substrate 12. (*Id.*, 5:29–32.) The GaN layers 11 include an n-type doped region disposed directly adjacent to substrate 12 and electrically connected to pad 14 and a p-type doped region electrically connected to pad 13. (*Id.*, 5:34–37.) GaN refers to a gallium nitride “which is a type of bandgap semiconductor suited for use in high power LEDs.” (*Id.*, 5:5–7; *see also id.*, 5:33–34 (“GaN is chosen for its wide band-gap and high brightness properties.”).) As noted above, the ’612 patent states that GaN LEDs “comprise a P-I-N junction device having an intrinsic (I) layer disposed between a N-type doped layer and a P-type doped layer.” (*Id.*, 5:9–11.) In other words, the ’612 patent admits that prior art GaN LEDs have an intrinsic region disposed between an n-type doped layer and a p-type doped layer.

33. The figure 5 device further includes an adhesive layer 41, silicon wafer 31, peripheral reflectors 34, 35 (labeled in figure 4), a silicone encapsulation 42 that is an optically transmissive layer, and a relief defined by the silicon wafer 31 and adhesive layer 41. (*Id.*, 6:45–64 (describing silicon wafer 31 and peripheral reflectors 34, 35), 7:22–29 (describing adhesive layer 41), 7:54–58 (describing silicone encapsulation 42), 9:1–28 (describing the relief).) The '612 patent discloses that “[t]here are two types of geometrical reliefs which are evident in the FIG. 5,” namely (i) a “via (hole)” such as vias 51, 52 and (ii) a thermally conducting hole 53. (*Id.*, 9:1–28.)

34. Claims 1–9 of the '612 patent recite limitations relating to the features discussed above. However, as I discuss below in Sections VIII and IX, it is my opinion that all of these features were well known in the art at the relevant time.

VII. CLAIM CONSTRUCTION

35. I understand that claim terms are typically given their ordinary and customary meaning, as would have been understood by a person of ordinary skill in the art, at the time of the alleged invention, which I understand is the mid-to-late 2013 timeframe (including the October 7, 2013 filing date of the application from which the '612 patent issued). (*See also* my discussion at Section IV above regarding my opinions being the same if the relevant timeframe is mid-to-late 2009.) In considering the meaning of the claims, however, I understand that one must consider the language of the claims, the specification, and the prosecution history of record.

VIII. OVERVIEW OF THE PRIOR ART³

A. Tanaka (Ex. 1005)

36. Tanaka is directed to LED devices containing a semiconductor light emitting element:

The present invention relates to a semiconductor GaN-based light emitting element containing gallium nitride and to a method of making the same.

(Ex. 1005, ¶[0002].) For example, Tanaka discloses a semiconductor light-emitting element that emits a blue-color light:

A semiconductor light-emitting element (a blue-color light-emitting diode) for blue-color light emission has been developed and put to practical use. It has a sapphire substrate on which a compound semiconductor crystal containing gallium nitride (GaN) is epitaxially grown by vapor-phase growth of an organic metal compound. Since sapphire differs only slightly in lattice constant from a GaN-based semiconductor crystal, it provides a suitable surface for epitaxially growing a GaN-based compound

³ These summaries of the prior art references in Section VIII are applicable to my analysis below in Section IX. For these reasons, I incorporate these summaries, which reflect how a person of ordinary skill in the art would have understood the references, into my analysis below where appropriate (*see, e.g.*, Section IX below).

shown in FIG. 6, utilizes a blue-color light-emitting diode chip 70 fabricated in a conventional manner. However, the chip is mounted on a sapphire substrate 71 positioned above. In this case, an N-side electrode 52 and a P-side electrode 51 are adjusted in height, and each of the electrodes 51, 52 is connected directly to a respective wiring pattern 80 via an anisotropic conductive layer or a conductive adhesive. **The structure is otherwise the same as in the embodiment shown in FIG. 6, and is not further described.** It may be easily understood that this embodiment enjoys the same benefits as the embodiment shown in FIG. 6. In addition, in this embodiment, when the surface of the sapphire substrate 71 is formed with a metal reflector (not shown), light traveling from the activation layer 73 upward in the figure is reflected toward the light guide 30, which enhances light-emitting which enhances light-emitting efficiency of the semiconductor light-emitting element 10.

(*Id.*, ¶[0072] (emphasis added); *see also id.*, Abstract, ¶[0004] (reproduced above).)

Tanaka discloses, with respect to figure 6, which is also applicable to figure 7:

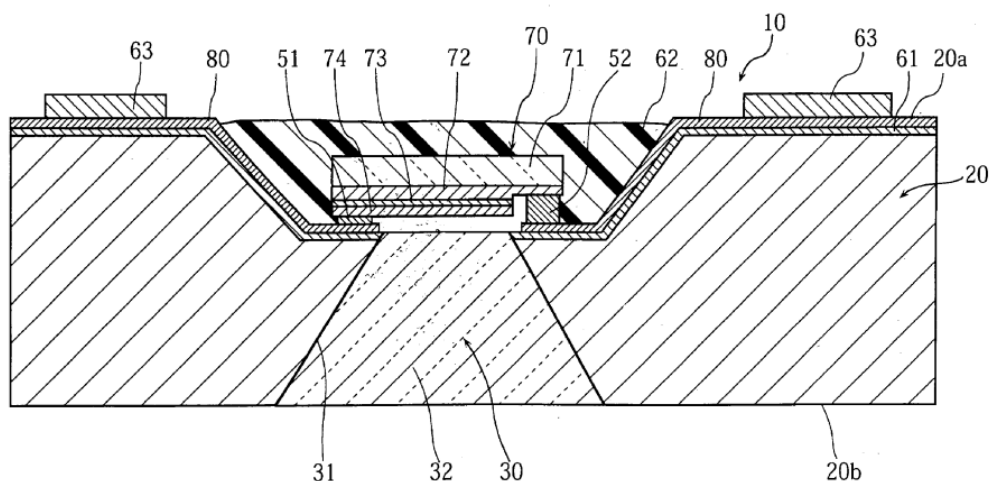
The blue-color light-emitting diode chip 70 fabricated in the conventional manner has a sapphire substrate 71 including an upper surface successively formed with an N-type semiconductor layer 72 (GaN layer or AlGaN layer), an

mounted on a carrier such as a mother substrate 5 with the first surface 20a of the substrate 20 directed down.

(*Id.*, ¶[0071].)

39. As shown in figure 7 of Tanaka, a wiring pattern 80 is disposed on the second LED surface of its semiconductor LED, which includes the N-type semiconductor layer 72, activation layer 73, and P-type semiconductor layer 74:

FIG.7



(*Id.*, FIG. 7.) Tanaka discloses that electrodes 51 and 52 provide electrical connections between the LED chip and the wiring pattern 80.

However, the chip is mounted on a sapphire substrate 71 positioned above. In this case, **an N-side electrode 52 and a P-side electrode 51 are adjusted in height, and each of the electrodes 51, 52 is connected directly to a respective wiring**

pattern 80 via an anisotropic conductive layer or a conductive adhesive.

(*Id.*, ¶[0072] (excerpted and emphasis added).) Tanaka also explains that the wiring pattern 80 is on a monocrystal silicon substrate 20. (*Id.*, ¶[0068].)

40. As shown in figure 7, the light emitting element 10 is also configured with a hole 31. (*Id.*, FIG. 7.) The hole 31 may or may not be filled. (*Id.*, ¶[0053]; *see also id.*, ¶[0016], claims 2, 3.) For example, the hole 31 may be filled with a translucent resin 32, such as epoxy resin. (*Id.*, ¶[0053].) The epoxy resin serves as a light guide 30 for guiding light emitted from the GaN-based semiconductor laminate 40 toward the second surface 20b side while also serving as a protective member for the semiconductor laminate 40. (*Id.*) For example, Tanaka discloses:

In the structure described above, **light emitted from the activation layer 73 of the light-emitting diode chip 70 travels via the transparent sapphire substrate 71 and the light guide 30 to go out efficiently from the second surface 20b.** The P-side electrode 51 which is a full-surface electrode functions as a reflector. Thus, light emitted from the activation layer 73 upward in FIG. 6 is reflected toward the light guide 30 to go out from the second surface 20b of the substrate 20 efficiently without being wasted.

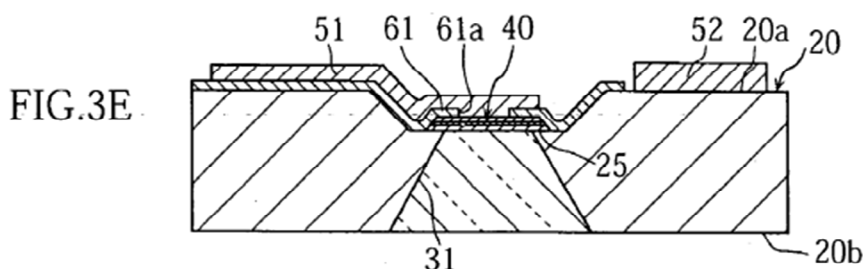
(*Id.*, ¶[0070] (emphasis added).)

As in the first embodiment, **the hole 31 formed in the monocrystal silicon substrate 20 is preferably filled with**

translucent resin 32 such as epoxy resin. The depression 21 on the first surface 20a is also filled with a protective member 62 such as epoxy resin to protect the chip 70 and the bonding wires 75.

(*Id.*, ¶[0069] (emphasis added).)

41. Tanaka discloses the formation of the hole 31 in the context of figure 3E below. Specifically, Tanaka discloses that “the monocrystal silicon substrate 20 is formed with a hole 31 extending from the second surface 20b to partially expose the bottom surface of the GaN-based semiconductor laminate 40.” (*Id.*, ¶[0062].)



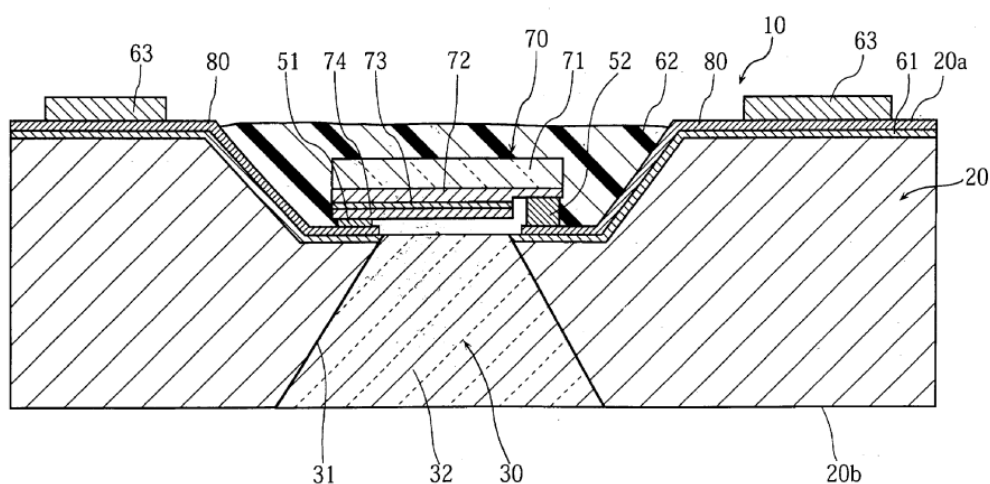
(*Id.*, FIG. 3E; *see also id.*, ¶[0042] (“FIGS. 3A-3E show an example of method of making the semiconductor light-emitting element shown in FIG. 1A;”).) For example, “[t]he monocrystal silicon substrate 20 is formed with a thorough-hole 31 extending thicknesswise from the bottom of the depression 21 to the second surface 20b.” (*Id.*, ¶[0049]; *see also id.*, ¶¶[0050], [0069], [0072].)

42. As I noted above, in the figure 7 embodiment, a P-side electrode 51 and an N-side electrode 52 connect the LED chip to the wiring pattern 80. (Ex. 1005, ¶[0072].) These electrode layers 51 and 52 are made of metal, and can function as

a reflector. (*Id.*, ¶¶[0061] (“The electrode layers 51, 52 are made of an Au- or Ag-based metal material for example.”), [0054] (“[T]he metal electrode layer serves as a reflector for efficiently reflecting light, traveling from the activation layer 42 upward in FIG. 1A, toward the light guide 30, which also results in significant improvement in light-emitting efficiency.”).)

43. The semiconductor light-emitting element 10, as shown in figure 7, also includes a protective member 62:

FIG. 7



(*Id.*, FIG. 7.) The protective member 62 is composed of an epoxy resin to protect the LED chip 70. (*Id.*, ¶[0069].)

B. Weeks (Ex. 1006)

44. Weeks relates to fabrication of LED devices:

The invention provides gallium nitride material devices, structures and methods of forming the same. The devices include

a gallium nitride material formed over a substrate, such as silicon. Exemplary devices include light emitting devices (e.g., LED's, lasers), light detecting devices (such as detectors and sensors), power rectifier diodes and FETs (e.g., HFETs), amongst others.

(Ex. 1006, Abstract, 1:15–17 (“The invention relates generally to semiconductor materials and, more particularly, to gallium nitride materials and methods of producing gallium nitride materials.”); *see also id.*, 1:17–49, 8:51–67 (reproduced below).) Weeks discloses GaN LED structures with a light emitting active region (*id.*, 8:47–50) where a hole or via is provided in order to allow the generated light to be emitted from the LED structure:

In certain embodiments, and as described further below in connection with FIGS. 9–11, 13–14, and 16–18, it may be preferable for via 24 to be free of a contact. That is, a contact is not formed within the via. In some cases, the via may be free of a contact but may have one or more other region(s) or layer(s) formed therein (e.g., a reflective layer), as described further below. In some cases, the via may be free of any material formed therein. When free of material, the via may function as a window that exposes internal layers of the device (e.g., transition layer 15 or gallium nitride material device region 14) to the outside. This exposure may enhance the extraction of light from the device which can be particularly useful in light-emitting devices such as LEDs or lasers. In embodiments in which

via 24 is free of an electrical contact, it should be understood that contacts are formed on other parts of the device including other (non-via) areas of backside 22 or areas of topside 18.

(*Id.*, 8:51–67; *see also id.*, 7:23–41, 8:33–46, 10:8–46, 12:50–56, 13:35–58, 14:60–66, 15:50–60, 16:42–17:11, FIGs. 14, 17, 20 (reproduced below).)

45. Weeks discloses, with respect to the figure 20 embodiment reproduced below, an LED 136 that includes a reflector with two reflection regions: a topside contact 114b and a Distributed Bragg Reflector (DBR) 120b:

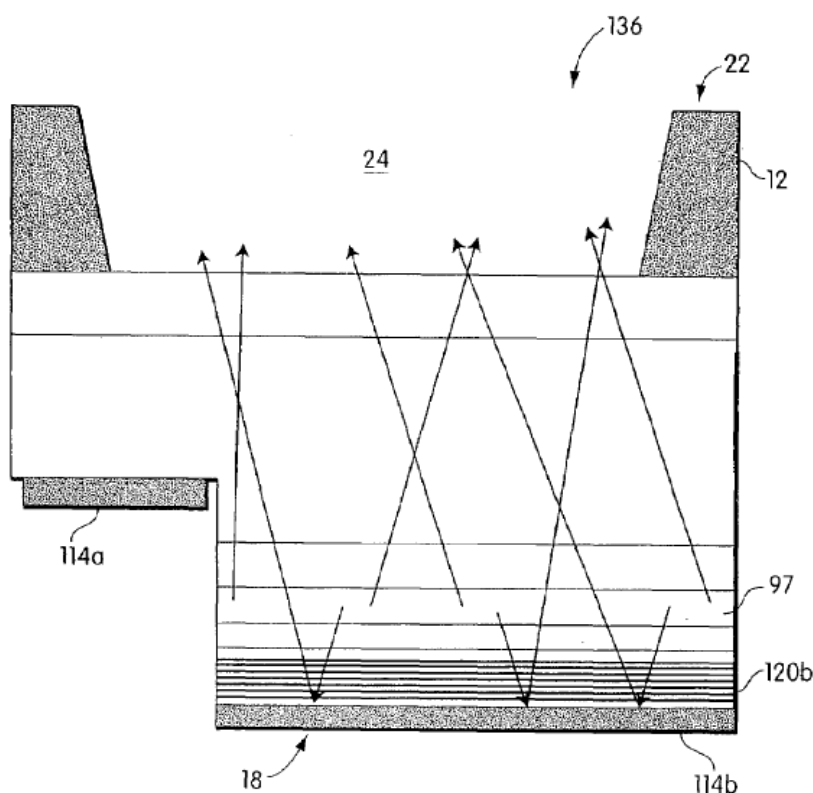


Fig. 20

(*Id.*, FIG. 20.)

FIG. 20 illustrates a light emitting device 136 that has been flipped during use so that backside 22 faces upward and topside 18 faces downward. Topside contact 114b also functions as a reflector region that can upwardly reflect light generated in region 97. The device also includes a second reflector region 120b which may be a Distributed Bragg Reflector (DBR) that includes a number of semiconductor or dielectric layers. Device 136 includes two reflector regions to increase the ability of the device to reflect generated light in the desired direction. It should be understood, however, that other devices may include only one reflector region which may be an electrical contact (e.g., topside contact 114 b) or a layer(s) within the structure of the device. It should be understood that light emitting device 136 may have any suitable layer arrangement including the layer arrangements (or a portion thereof) of the LED embodiments described herein.

(Ex. 1006, 16:62–17:11.)

C. Chitnis (Ex. 1007)

46. Chitnis relates to the fabrication of LED devices:

The present invention relates to electronic and semiconductor devices, and more particularly to light emitting devices and methods of fabricating light emitting devices.

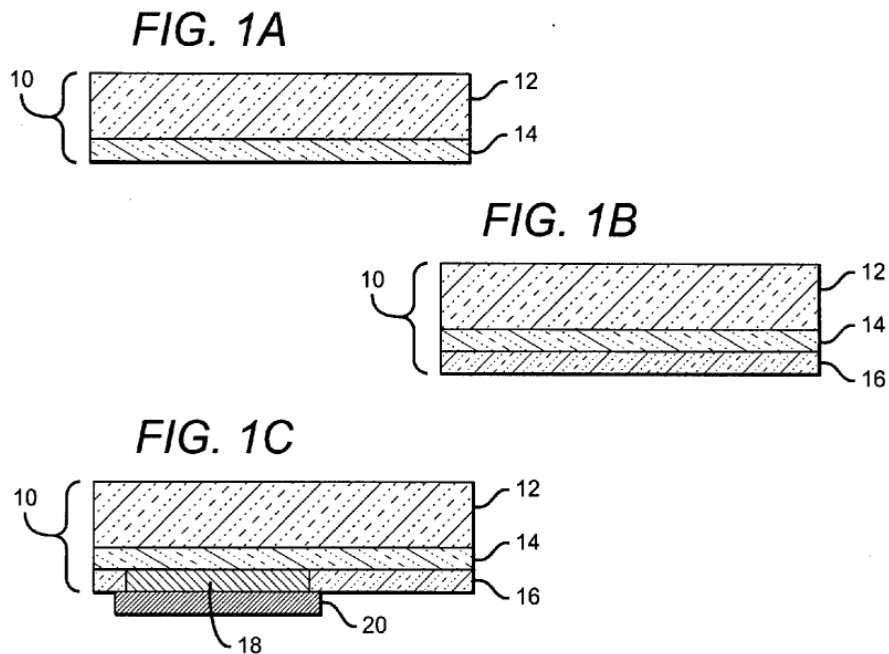
(Ex. 1007, ¶[0004].) Chitnis discloses well-known wafer-level bonding techniques used during LED device fabrication:

Recent developments in wafer-bonding technology have provided the means to integrate different materials into

semiconductor devices. Wafer bonding is a semiconductor manufacturing process in which two semiconductor wafers are bonded to form a single substrate having specific properties. A variety of bonding methods can be used to create integrated electronics, and to combine multifunctional components onto a single die. In particular, wafer bonding provides a means for unifying different materials in semiconductor devices, thus allowing the creation of new devices and microcomponents having properties that cannot be achieved using a single material or single material system. Wafer bonding is commonly used to form silicon-on-insulator (SOI) substrates and can also be used to bond wafers composed of different materials (e.g. GaAs on Si, SiC on Si).

(*Id.*, ¶[0010]; *see also id.*, ¶[0008] (“One approach to reduce package related cost is by wafer level packaging, i.e component assembly/integration at wafer level.”) (excerpted).)

47. Chitnis, for example, discloses bonding an LED wafer 10 shown in figures 1A–1C (including LED grown substrate 12, n- and p-type layers 16, 18, and active region 14) with a submount 40 shown in figure 2 (including a submount wafer 42 and a dielectric material 44):

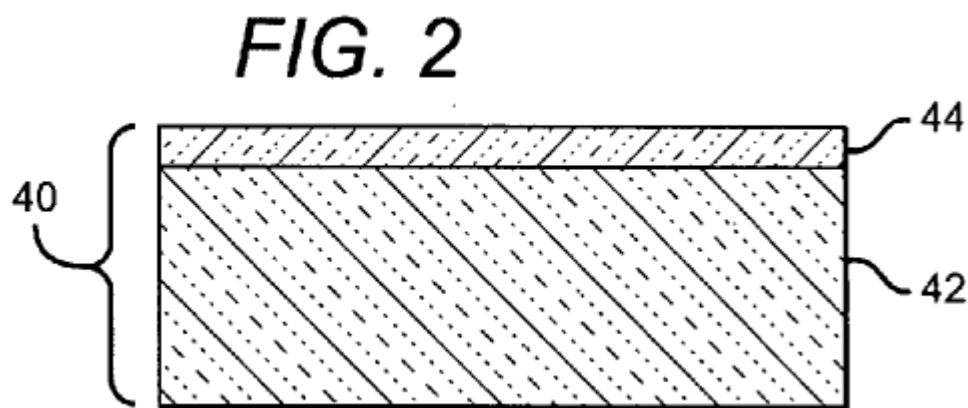


(*Id.*, FIGs. 1A–1C.) Figures 1A–1C show the preparation of an LED wafer 10 prior to wafer bonding. (*Id.*, ¶[0037].) Chitnis explains that the layers 14 may be fabricated from different materials, including gallium nitride:

The layers 14 may be fabricated from different material systems, with preferred material systems being Group-III nitride based material systems. Group-III nitrides refer to those semiconductor compounds formed between nitrogen and the elements in the Group III of the periodic table, usually aluminum (Al), gallium (Ga), and indium (In). The term also refers to ternary and quaternary compounds such as aluminum gallium nitride (AlGaN) and aluminum indium gallium nitride (AlInGaN). In one embodiment, the n- and p-type layers 16, 18 are gallium nitride (GaN) and the active region 14 is InGaN. In alternative embodiments the n- and p-type layers 16, 18 may be

AlGaIn, aluminum gallium arsenide (AlGaAs) or aluminum gallium indium arsenide phosphide (AlGaInAsP).

(*Id.*, ¶[0040].) Figure 2 further shows the preparation of a submount 40 before wafer bonding:



(*Id.*, FIG. 2.)

FIG. 2 shows the preparation of a submount 40 prior to wafer bonding. The submount 40 comprises a submount wafer 42, and a variety of materials can be used for submount wafers according to the invention, including without limitation Si, Ge, SiC, and AlN. In one embodiment, a dielectric layer 44 can be deposited onto the submount wafer 40 prior to deposition of the bond medium. The presence of the dielectric layer can increase the effectiveness or strength of wafer bonding or enhance etch selectivity when a targeted etch depth is required in the submount wafer. Dielectric materials useful for the invention include without limitation SiO₂ and SiN, although other materials may also be used. The thickness of the dielectric layer can vary from

about 0.01 micron to about 25 80 microns. Preferably, the thickness of the dielectric layer can range from about 0.1 to about 10 microns. Besides dielectric, metal such as titanium (Ti), nickel (Ni), tungsten (W) or a combination thereof can also be used as stop layer during via etch or adhesion layer for the bond medium.

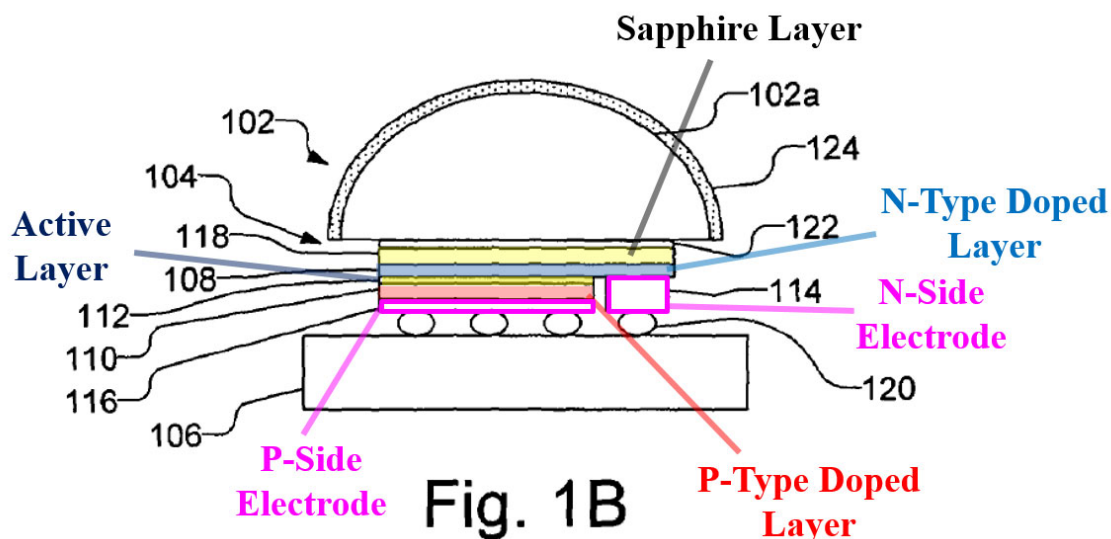
(*Id.*, ¶[0045].)

48. Chitnis explains that “[t]he choice of wafer bonding process used to fabricate a device is dependent upon the type of device, particularly the components and materials used to build the device.” (*Id.*, ¶[0011].) In this regard, Chitnis discloses that “eutectic wafer bonding is based on the use of bonding materials that form a eutectic alloy at specific temperature conditions, and eutectic bonding media such as Au-Si, Au-Sn or Pd-Si are widely used.” (*Id.*) For example, “[f]or chip scale packages (e.g. flip chips), it would be advantageous to create devices at the wafer level with both electrical contacts on the bottom of the chip,” and that “this would require electrically and thermally conducting bond medium selectively deposited to avoid electrical shorting.” (*Id.*)

D. Camras (Ex. 1008)

49. Camras is directed to LED structures formed on a sapphire substrate that includes an n-type layer, a p-type layer, and a light emitting active region. (Ex. 1008, 2:27–32, 2:44–61.) Camras also discloses that the active region 112, shown

in annotated figure 1B below, is between the p-type and n-type layers and emits light when sufficient voltage is applied across contacts 114 and 116. (*Id.*, 2:62–63.)



(*Id.*, FIG. 1B (annotated).)

50. According to Camras, the light emitting active region of the LED between the p- and n-type layers can be a “p-n diode junction associated with the interface of layers 108 and 110” or the active region can include one or more doped or undoped (intrinsic) semiconductor layers. (*Id.*, 2:48–52.) Camras explains that the semiconductor layers 108 and 110 and active region 112 can be formed from various semiconductors, including gallium nitride (GaN). (*Id.*, 3:1–7.)

51. The LED device of Camras also includes electrodes (n-contact 114 and p-contact 116), that provide electrical connections to the n- and p-type semiconductor layers, where the electrodes are on the same side of the LED die 104

in a “flip chip” arrangement. (*Id.*, 2:52–56.) In some embodiments, the contacts are made with metal, either alone or in mixture/alloy form. (*Id.*, 3:8–12.)

52. Camras also discloses a transparent supersubstrate 118 coupled to the n-type semiconductor layer 108 that can be formed from various materials, including sapphire. (*Id.*, 2:56–61.) An independently formed layer of wavelength converting material (e.g., phosphor impregnated glass) 510 is bonded to the sapphire layer using a bonding layer 508. (*Id.*, 7:64–65.) Another bonding layer 509 is used to bond the wavelength converting material 510 to an optical element 506. (*Id.*, 8:38–42, 8:48–54.)

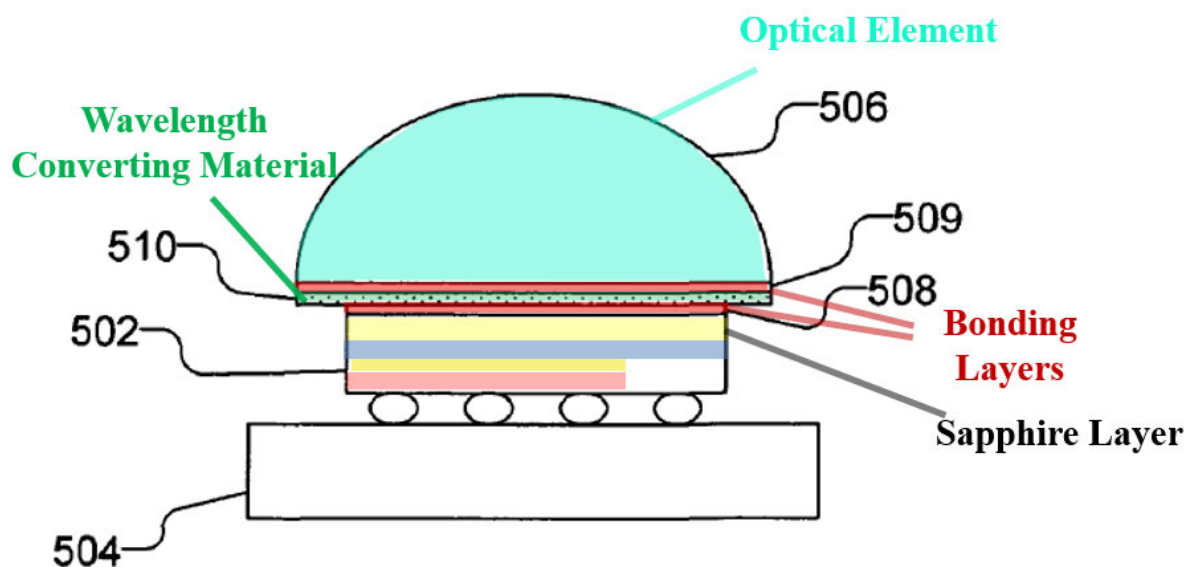


Fig. 5

(*Id.*, FIG. 5 (annotated).)

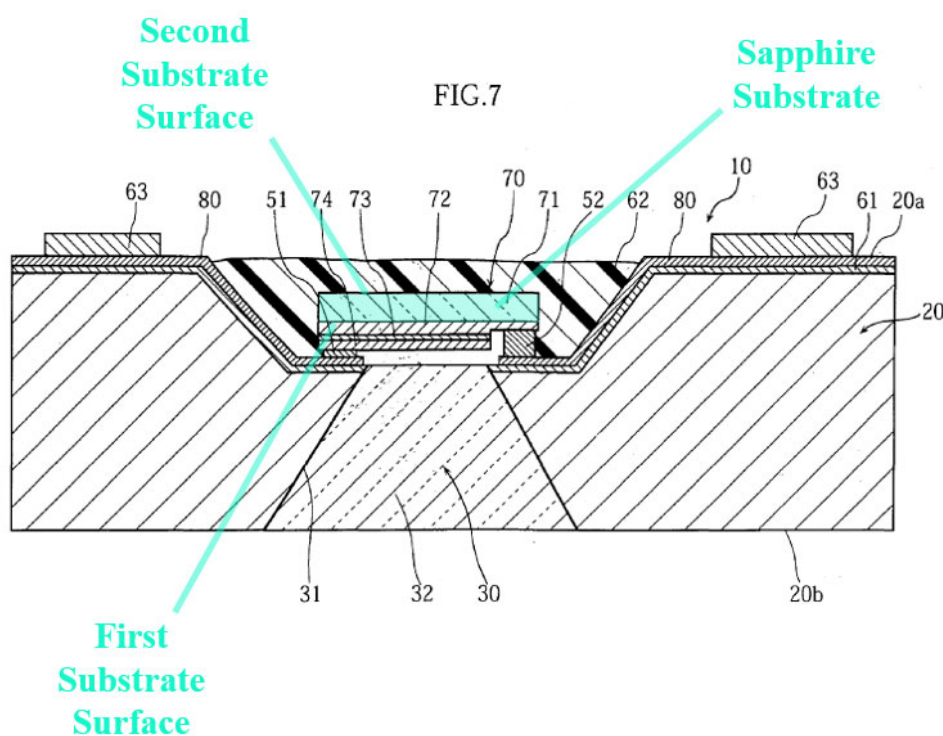
present invention. This embodiment, as in the embodiment shown in FIG. 6, **utilizes a blue-color light-emitting diode chip 70 fabricated in a conventional manner.** However, the chip is mounted on a sapphire substrate 71 positioned above.

(*Id.*, ¶[0072] (excerpted and emphasis added); *see also id.*, Abstract, ¶¶[0004] (“A semiconductor light-emitting element (a blue-color light-emitting diode) for blue-color light emission has been developed and put to practical use. It has a sapphire substrate on which a compound semiconductor crystal containing gallium nitride (GaN) is epitaxially grown . . .”), [0067] (“FIG. 6 is a sectional view showing a semiconductor light-emitting element 10 according to a third embodiment of the present invention. The semiconductor light-emitting element 10 has a monocrystal silicon substrate 20 including a first and a second surfaces 20a, 20b.”), FIG. 6.)⁴

⁴ Reviewing Tanaka in context, a person of ordinary skill in the art would have understood that Tanaka’s description of Figure 7 builds on figure 6, and thus the description of components in Figure 6 applies to similar components in figure 7. Tanaka also states that, aside from the differences specifically described for figure 7, “[t]he structure is otherwise the same as in the embodiment shown in FIG. 6.” (Ex. 1005 ¶[0072], FIGs. 6–7.) Thus, Tanaka’s description corresponding to the components in figure 6 equally applies to the similar components in figure 7 because

b) a substrate having opposing first and second substrate surfaces;

55. In my opinion, Tanaka discloses this feature. For example, Tanaka discloses that its light emitting element 10 (“light emitting device”) includes a sapphire substrate 71 (“substrate”) having opposing first and second surfaces, as seen in the annotated figure 7 below:



(Ex. 1005, FIG. 7 (annotated).)

The blue-color light-emitting diode chip 70 fabricated in the conventional manner **has a sapphire substrate 71** including an

Tanaka does not repeat the description of the functions of the common components shown in its Figures.

upper surface successively formed with an N-type semiconductor layer 72 (GaN layer or AlGaN layer), an activation layer 73 (InGaN layer), and a P-type semiconductor layer 74 (GaN layer or AlGaN layer).

(*Id.*, ¶[0068] (emphasis added); *see also id.*, ¶[0072] (“[T]he [blue-color light-emitting diode] chip [70] is mounted on a sapphire substrate 71.”).)⁵

56. The '612 Patent similarly discloses that its wafer 200 may be made of sapphire. (Ex. 1001, 5:58–60 (“**sapphire** substrate 22”) (emphasis added); *see also* Ex. 1001, 2:1–4 (“Light emitting devices generally include a semiconductor chip, or die, including a p-n junction formed upon an epitaxial layer grown on a substrate, such as, **sapphire.**”) (emphasis added), 5:29–30 (“Gallium Nitride LEDs can be epitaxially grown on . . . **Sapphire** substrates.”) (emphasis added).)

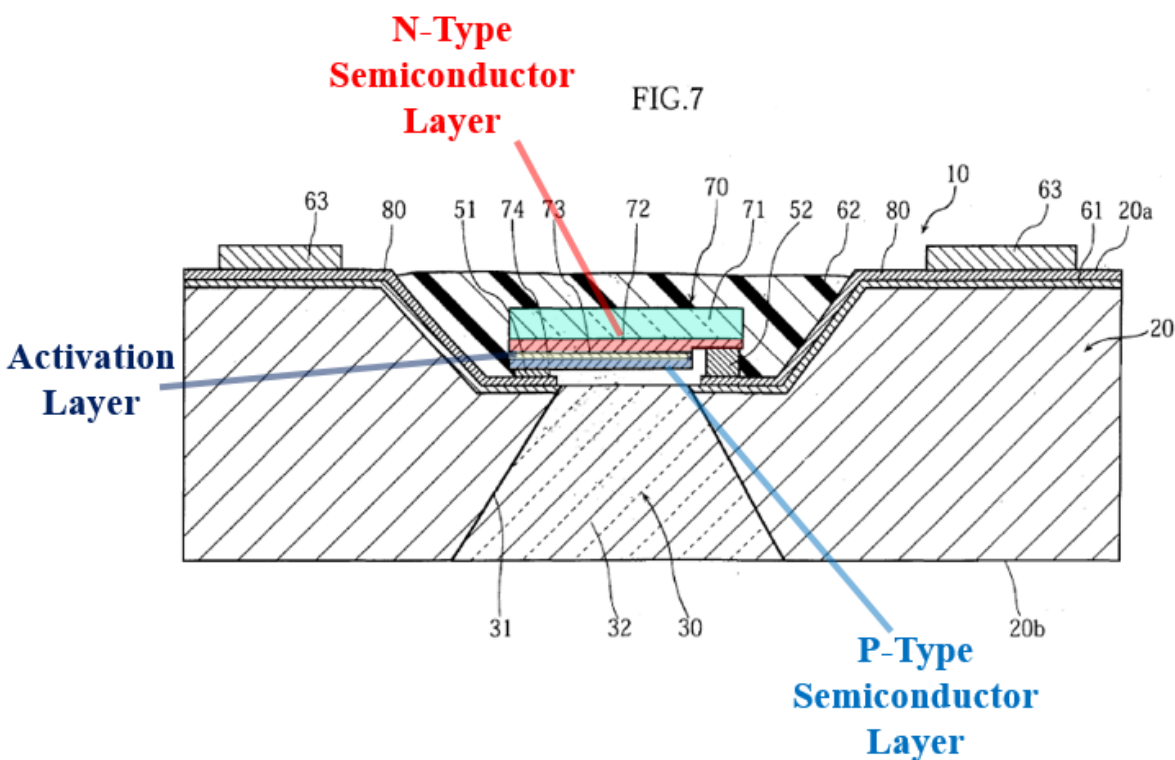
57. Therefore, it is my opinion that Tanaka discloses a substrate having opposing first and second substrate surfaces, as claimed.

c) a semiconductor LED including doped and intrinsic regions thereof, said semiconductor LED having opposing first and second LED surfaces, said first LED surface disposed on the first substrate surface;

58. In my opinion, Tanaka discloses or suggests this feature. For example, Tanaka discloses that its light emitting element 10 (“light emitting device”) includes blue-color light-emitting diode chip 70 with an N-type semiconductor layer 72, a P-

⁵ See my footnote n.4 above.

type semiconductor layer 74, and an activation layer 73 between the N- and P-type layers (collectively, the claimed “semiconductor LED”), as seen in the annotated figure 7 below:



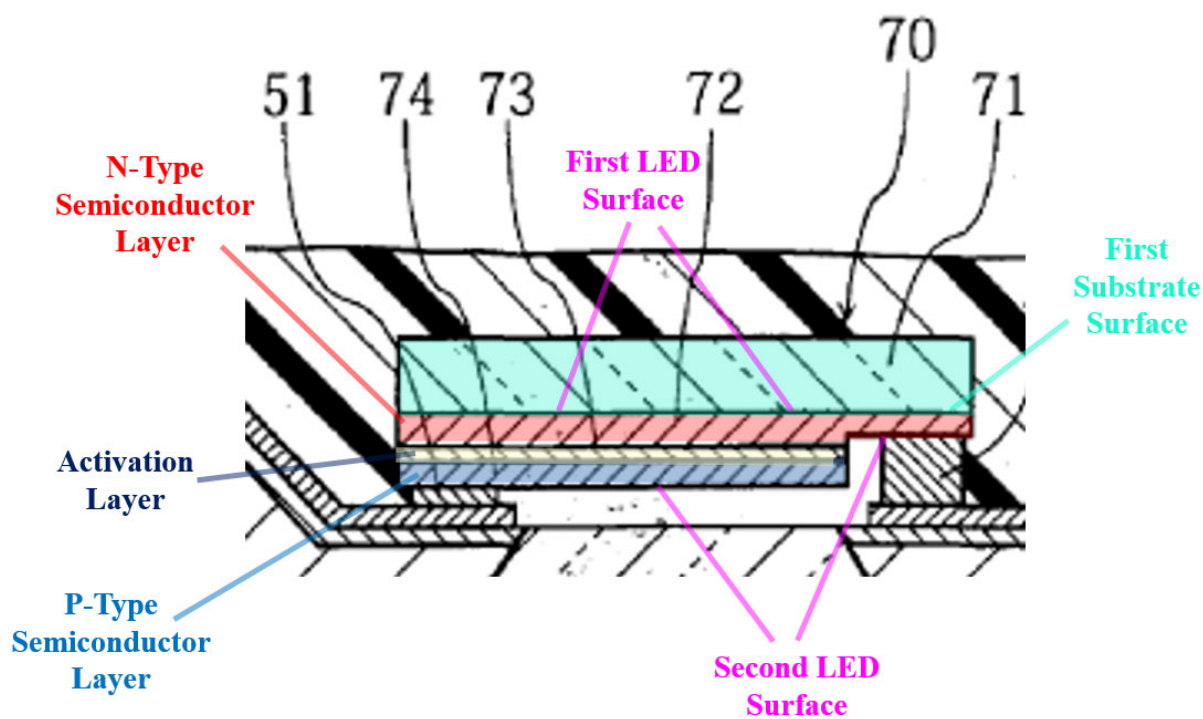
(Ex. 1005, FIG. 7 (annotated).)

The blue-color light-emitting diode chip 70 fabricated in the conventional manner has a sapphire substrate 71 including an upper surface successively formed with an N-type semiconductor layer 72 (GaN layer or AlGaN layer), an

activation layer 73 (InGaN layer), and a P-type semiconductor layer 74 (GaN layer or AlGaN layer).

(*Id.*, ¶[0068]; *see also id.*, ¶[0072].)⁶

59. As shown in the enlarged annotated excerpt of figure 7 below, Tanaka's semiconductor LED has opposing first and second LED surfaces, and the first LED surface is disposed on the first substrate surface of the sapphire substrate 71 ("substrate").



(*Id.*, FIG. 7 (excerpted and annotated).)

⁶ See my footnote n.4 above.

60. It is my opinion that Tanaka also suggests (if not discloses to a person of ordinary skill in the art) that the activation layer 73 includes an “intrinsic region,” as claimed for the three reasons I explain below. First, the lack of any indication of doping (n-type or p-type) of activation layer 73 suggests that activation layer 73 is “intrinsic” (i.e., not doped). In fact, it was well-understood in the LED art that “[f]requently the active layer is left undoped,” as explained by Schubert (Ex. 1017). (Ex. 1017, 117.)⁷

61. Second, Tanaka discloses that the LED device is a gallium nitride (GaN) LED in some embodiments. (Ex. 1005, ¶¶[0002], [0014], [0030], [0068].) The '612 patent admits that prior art GaN LEDs, like that described in Tanaka, “**comprise a P-I-N junction device having an intrinsic (I) layer** disposed between a N-type doped layer and a P-type doped layer.” (Ex. 1001, 5:9–11 (emphasis added); *see also id.*, 5:38–39 (“An active region makes up the interface of the GaN layers between the p-type and n-type regions.”).)⁸

⁷ I refer to Schubert (Ex. 1017) to demonstrate the knowledge of a person of ordinary skill in the art at the time of the alleged invention of the '612 patent.

⁸ Tanaka, like the '612 patent, discloses that its semiconductor LED may comprise gallium nitride (GaN). (Ex. 1005 ¶[0068] (“The blue-color light-emitting diode chip 70 fabricated in the conventional manner has a sapphire substrate 71 including an

62. And, third, this configuration described in the '612 patent is the same configuration illustrated in figure 7 of Tanaka, where the activation layer 73 is interposed between the N-type semiconductor layer 72 and P-type semiconductor layer 74. (Ex. 1005, ¶¶[0068], [0072], FIG. 7.) Atanackovic (Ex. 1010) and Herner (Ex. 1011)⁹, which are contemporaneous references, also support my opinion. For example, Atanackovic (Ex. 1010) also describes a p-i-n semiconductor device including “p-doped and n-doped regions separated by an optically *active intrinsic region*.” (Ex. 1010, 29:15–23.) Similarly, Herner (Ex. 1011) discloses:

upper surface successively formed with **an N-type semiconductor layer 72 (GaN layer or AlGaN layer), an activation layer 73 (InGaN layer), and a P-type semiconductor layer 74 (GaN layer or AlGaN layer).**”) (emphasis added); Ex. 1001, 5:5–7 (“For example, some LEDs are made using Gallium Nitride (GaN) which is a type of bandgap semiconductor suited for use in high power LEDs.”), 5:29–37 (“*Gallium Nitride LEDs* can be epitaxially grown on Silicon, GaN, SiC or Sapphire substrates. FIG. 1 represents a characteristic horizontal-type *Ga LED chip 10 . . .*”).)

⁹ I refer to Atanackovic (Ex. 1010) and Herner (Ex. 1011) to demonstrate the knowledge of a person of ordinary skill in the art at the time of the alleged invention of the '612 patent.

A semiconductor junction diode, for example a p-n diode or a p-i-n diode, has been paired with a dielectric antifuse layer to form a memory cell, for example in the monolithic three dimensional memory array described in the '470 application.

The term junction diode is used herein to refer to a semiconductor device with the property of conducting current more easily in one direction than the other, having two terminal electrodes, and made of semiconducting material which is p-type at one electrode and n-type at the other. Examples include p-n diodes and n-p diodes, which have p-type semiconductor material and n-type semiconductor material in contact, and **p-i-n** and n-i-p diodes, **in which intrinsic (undoped) semiconductor material is interposed between p-type semiconductor material and n-type semiconductor material.**

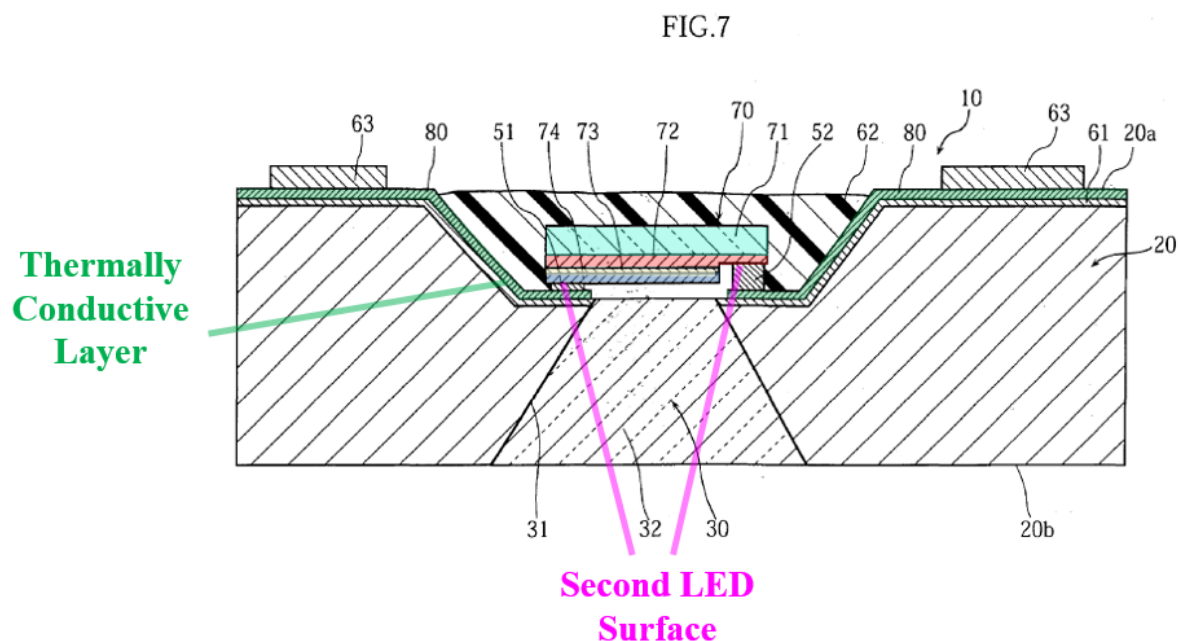
(Ex. 1011, 3:29–58 (excerpted and emphasis added); *see also id.*, FIG. 1.)

63. Therefore, it is my opinion that Tanaka discloses or suggests a semiconductor LED including doped and intrinsic regions thereof, said semiconductor LED having opposing first and second LED surfaces, said first LED surface disposed on the first substrate surface, as claimed.

d) a thermally conductive layer disposed on the second LED surface of the semiconductor LED;

64. In my opinion, Tanaka discloses or suggests this feature. For example, Tanaka discloses a wiring pattern 80 (“thermally conductive layer”) disposed on the second LED surface of its semiconductor LED (which includes the N-type

semiconductor layer 72, activation layer 73, and P-type semiconductor layer 74), as seen in the annotated figure 7 below:



(Ex. 1005, FIG. 7 (annotated).)

[A]n N-side electrode 52 and a P-side electrode 51 are adjusted in height, and each of the electrodes 51, 52 is connected directly to a respective wiring pattern 80 via an anisotropic conductive layer or a conductive adhesive.

(*Id.*, ¶[0072].)

65. A person of ordinary skill in the art would have understood that the wiring pattern 80 is “disposed on” the second LED surface (the lower surface of P-type semiconductor layer 74) at least because it overlaps with the second LED surface in the vertical direction of Tanaka’s figure 7 embodiment (e.g., in the regions

where the P-side electrode 51 and N-side electrode 51 are disposed). (*Id.*, ¶[0072] (excerpted and reproduced above), FIG. 7.)

66. Tanaka's teachings for the wiring pattern 80 being disposed on the second LED surface, given its overlap with the second LED surface, tracks the teachings of the '612 patent. For example, the '612 patent similarly describes an adhesive layer 41 (an example of the claimed thermally conductive layer) overlapping with the second LED surface of the GaN layers (an example of the claimed semiconductor LED) in the vertical direction of the figure 5 embodiment (e.g., in the regions where the n-type pad 55 and p-type pad 56 are disposed).

67. Moreover, it would have been apparent to a person of ordinary skill in the art that the wiring pattern 80 is a "thermally conductive" layer. A person of ordinary skill in the art would have readily understood that such wiring is thermally conductive because it would conduct heat. Indeed, the '612 patent confirms that a material may be "thermally conductive" even at lower levels of thermal conductivity. (*See, e.g.*, Ex. 1001, 7:26–41 (generally describing the adhesive layer 41 as including "material optimized to provide [] heat conduction" and "[a]s a metric for suitable performance, heat conductions of 3 W/mK or more is sufficient"), 10:43–46 (describing the passivation layer 81 as another example of a thermally conductive layer "used to minimize the thermal conductance of the package").) A person of ordinary skill in the art would have also known that a wire is typically used

to determine thermal conductivity of a sample, by measuring the wire temperature over time after inserting the wire into the sample. For example, Mathis (Ex. 1013) describes a hot wire technique to measure thermal conductivity:

The hot wire technique is a transient method of determining thermal conductivity. This means that the temperature rise is measured during a time interval. The method involves inserting an electrically heated wire into a sample. The heat flows out radially from the wire and the temperature of the wire is measured. The plot of these temperatures versus the logarithm of time is used to calculate thermal conductivity. This technique is intrusive and therefore has limitations as to the types of materials that can be tested. (ie. powder and liquid but not solids)

(Ex. 1013, 1:43–52; *see also id.* generally, 1:6–20 (describing thermal conductivity measurement techniques), 2:1–20 (describing modified hot wire techniques for measuring thermal conductivity).)¹⁰ Thus, it is my opinion that the wiring pattern 80 is a thermally conductive layer, as claimed.

68. I have been asked to assume that Tanaka does not necessarily disclose that its wiring pattern 80 is thermally conductive. Under that assumption, it is my opinion that a person of ordinary skill in the art would have been motivated to

¹⁰ I refer to Mathis (Ex. 1013) to demonstrate the knowledge of a person of ordinary skill in the art at the time of the alleged invention of the '612 patent.

configure Tanaka's wiring pattern 80 such that it is made of metal, which is thermally conductive.

69. As I explain below, using such a metal for the wiring pattern 80 would have been a mere design choice. For example, a person of ordinary skill in the art would have understood that metal was a common material used for conductive wires and traces in semiconductor devices. Indeed, such an understanding is supported by Tanaka's disclosure that electrodes 51, 52 are made of metal. (*See* my discussion below at Section IX.A.1.f.) Such a skilled person would have thus known that a wiring pattern like wiring pattern 80 in Tanaka can be made from a limited number of materials, where metals and metal alloys are common materials chosen for such conductive patterns. For example, Hembree (Ex. 1012) describes that conventional wire material used in semiconductor packaging includes metals and alloys:

In addition, the bonding wire 14 can comprise a conventional wire material used in semiconductor packaging, such as solder alloys, gold, gold alloys, copper, copper alloys, silver, silver alloys, aluminum, aluminum-silicon alloys, and aluminum-magnesium alloys. In addition, the wire 14 can comprise a metal, or a metal alloy, that does not contain reductions of hazardous substances (ROHS), such as lead. Exemplary ROHS free metals include lead free solders, such as 97.5% Sn2.5% Ag. Other ROHS free metals include gold, copper and alloys of these metals such as copper coated with a layer of flash gold. Also,

the melting point of the wire 14 should preferably be greater than that of the substrate contact 20A.

(Ex. 1012, 5:60–6:5.)¹¹ Also it was well-known at the time that metals are thermally conductive. For example, Tritt (Ex. 1014) discloses:

Thus, like every other solid material, metals possess a component of heat conduction associated with the vibrations of the lattice called lattice (or phonon) thermal conductivity, κ_p .

(Ex. 1014, 44.)¹² As I have discussed above, the '612 patent confirms that a material may be “thermally conductive” regardless of the degree of its thermal conductivity. (*See, e.g.*, Ex. 1001, 7:26–41, 10:43–46.)

70. Accordingly, at a minimum, a person of ordinary skill in the art would have been motivated to use metal for the wiring pattern 80 in Tanka in view of the teachings of Tanaka and the knowledge of such a skilled person. For instance, as discussed above, given that Tanaka discloses that the wiring pattern 80 is connected to the electrodes 51, 52 (Ex. 1005, ¶[0072]), a person of ordinary skill in the art would have recognized that the wiring pattern is intended to provide an electrical

¹¹ I refer to Hembree (Ex. 1012) to demonstrate the knowledge of a person of ordinary skill in the art at the time of the alleged invention of the '612 patent.

¹² I refer to Tritt (Ex. 1014) to demonstrate the knowledge of a person of ordinary skill in the art at the time of the alleged invention of the '612 patent.

connection to those electrodes and using metal for the wiring pattern 80 would have been a design choice that would accomplish that objective.

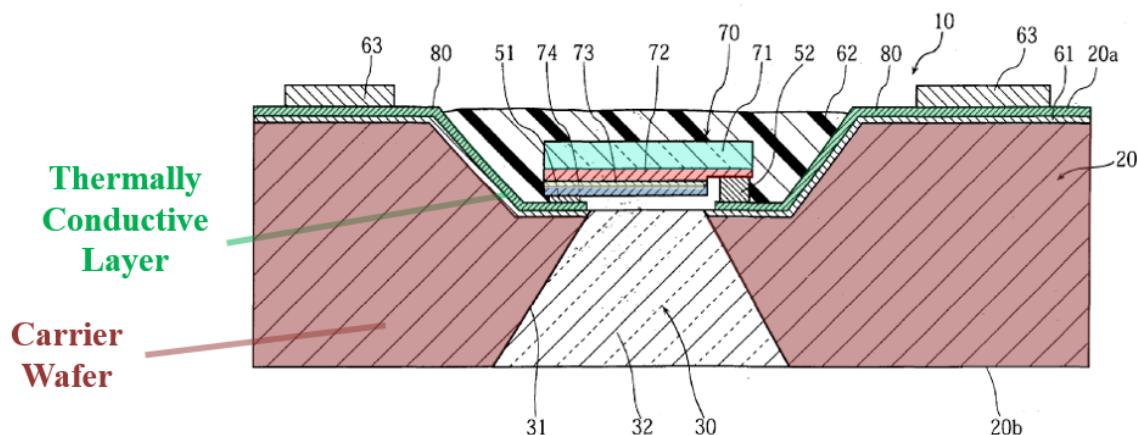
71. Because metals and metal alloys were well-known materials for formation of conductive wires and traces in semiconductor devices, a person of ordinary skill in the art would have understood how to implement the wiring pattern 80 using metal and would have a reasonable expectation of success. Accordingly, a person of ordinary skill in the art would have been motivated to implement the wiring pattern 80 in Tanaka using metal such that it would have been a thermally conductive layer, as claimed.

72. Therefore, it is my opinion that Tanaka discloses or suggests a thermally conductive layer disposed on the second LED surface of the semiconductor LED, as claimed.

e) a carrier wafer disposed on the thermally conductive layer;

73. In my opinion, Tanaka discloses or suggests this feature. For example, Tanaka discloses a monocrystal silicon substrate 20 (“carrier wafer”) disposed on the wiring pattern 80 (“thermally conductive layer”) as seen in the annotated figure 7 below:

FIG.7



(Ex. 1005, FIG. 7 (annotated).)

The blue-color light-emitting diode chip 70 fabricated in the conventional manner has a sapphire substrate 71 including an upper surface successively formed with an N-type semiconductor layer 72 (GaN layer or AlGaN layer), an activation layer 73 (InGaN layer), and a P-type semiconductor layer 74 (GaN layer or AlGaN layer). The N-type semiconductor layer 72 has an exposed portion formed with an N-side electrode 52, whereas the P-type semiconductor layer 74 includes a surface formed with a P-side electrode 51. In this embodiment, the chip is mounted on a depression 21 formed on the first surface 20a with the sapphire substrate 71 positioned below. **Each of the N-side electrode 52 and the P-side electrode 51 is connected, by wire bonding, to a corresponding wiring pattern 80 arranged on the first surface 20a. Wiring patterns 80 corresponding to the N-side electrode 52 and the P-side electrode 54 extend to suitable**

portions on the first surface 20a where bumps 63 are formed.

Each wiring pattern 80 has a lower surface formed with an insulating layer 61 made of e.g. silicon oxide film for insulation from the monocrystal silicon substrate 20.

(*Id.*, ¶[0068] (emphasis added).)¹³

As in the first embodiment, the hole 31 formed in the monocrystal silicon substrate 20 is preferably filled with translucent resin 32 such as epoxy resin. The depression 21 on the first surface 20a is also filled with a protective member 62 such as epoxy resin to protect the chip 70 and the bonding wires 75.

(*Id.*, ¶[0069].)¹⁴

In the structure described above, light emitted from the activation layer 73 of the light-emitting diode chip 70 travels via the transparent sapphire substrate 71 and the light guide 30 to go out efficiently from the second surface 20b. The P-side electrode 51 which is a full-surface electrode functions as a reflector. Thus, light emitted from the activation layer 73 upward in FIG. 6 is reflected toward the light

¹³ See my footnote n.4 above.

¹⁴ See my footnote n.4 above.

guide 30 to go out from the second surface 20*b* of the substrate 20 efficiently without being wasted.

(*Id.*, ¶[0070].)¹⁵

In this embodiment, similarly to the first embodiment, the monocrystal silicon substrate 20 may be formed integrally with a current regulating drive circuit or a logic circuit by wafer process. The semiconductor light-emitting element may be mounted on a carrier such as a mother substrate 5 with the first surface 20*a* of the substrate 20 directed down.

(*Id.*, ¶[0071].)¹⁶

FIG. 7 is a sectional view showing a semiconductor light-emitting element 10 according to a fourth embodiment of the present invention. This embodiment, as in the embodiment shown in FIG. 6, utilizes a blue-color light-emitting diode chip 70 fabricated in a conventional manner. However, the chip is mounted on a sapphire substrate 71 positioned above. **In this case, an N-side electrode 52 and a P-side electrode 51 are adjusted in height, and each of the electrodes 51, 52 is connected directly to a respective wiring pattern 80 via an anisotropic conductive layer or a conductive adhesive. The structure is otherwise the same as in the embodiment shown in FIG. 6, and is not further described. It may be easily**

¹⁵ See my footnote n.4 above.

¹⁶ See my footnote n.4 above.

understood that this embodiment enjoys the same benefits as the embodiment shown in FIG. 6. In addition, in this embodiment, when the surface of the sapphire substrate 71 is formed with a metal reflector (not shown), light traveling from the activation layer 73 upward in the figure is reflected toward the light guide 30, which enhances light-emitting efficiency of the semiconductor light-emitting element 10.

(*Id.*, ¶[0072].)¹⁷

74. A person of ordinary skill in the art would have understood that the monocrystal *silicon* substrate 20 is “disposed on” the wiring pattern 80 at least because it overlaps with the wiring pattern 80 in the vertical direction of Tanaka’s figure 7 embodiment (e.g., in the regions where the insulating layer 61 are disposed).

(*Id.*, ¶[0068] (“Each wiring pattern 80 has a lower surface formed with an insulating layer 61 made of e.g. silicon oxide film for insulation from the monocrystal *silicon* substrate 20.”), FIG. 7.)

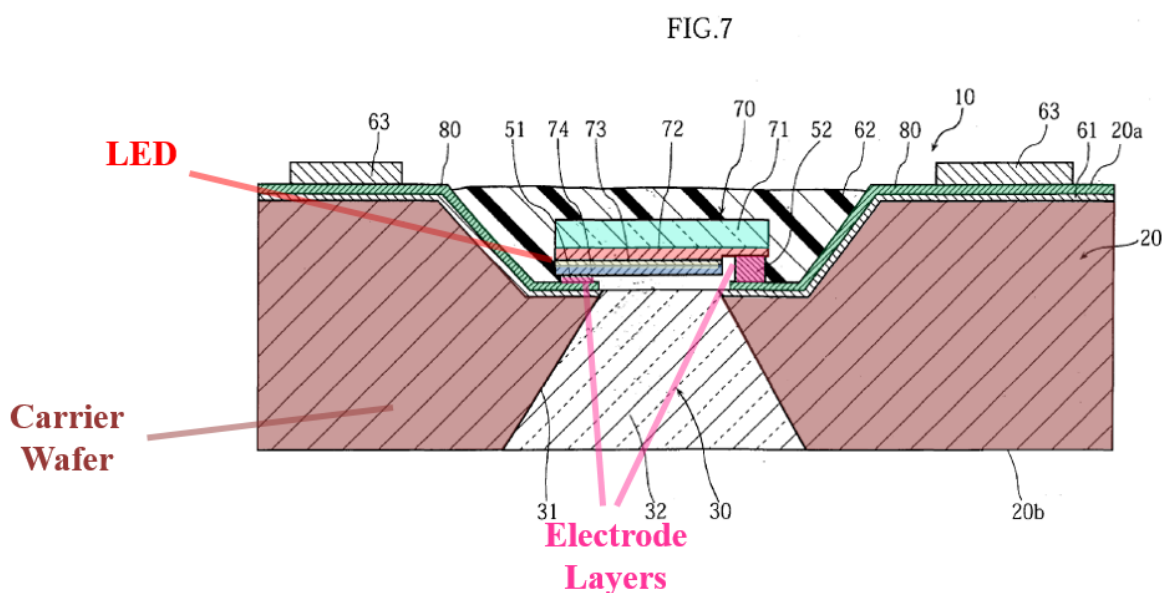
75. Tanaka’s teachings for the monocrystal *silicon* substrate 20 being disposed on the wiring pattern 80 track the teachings of the ’612 patent. For example, the ’612 patent similarly describes a *silicon* wafer 31 (an example of the claimed carrier wafer) overlapping with an adhesive layer 41 (an example of the claimed thermally conductive layer) in the vertical direction of the figure 5

¹⁷ See my footnote n.4 above.

76. Therefore, it is my opinion that Tanaka discloses or suggests a carrier wafer disposed on the thermally conductive layer, as claimed.

f) at least one optically reflective surface disposed between said carrier wafer and said semiconductor LED; and

77. In my opinion, Tanaka discloses or suggests this feature. For example, Tanaka discloses electrode layers 51, 52 (“at least one optically reflective surface”) disposed between the monocrystal silicon substrate 20 (“carrier wafer”) and the N-type semiconductor layer 72, activation layer 73, and P-type semiconductor layer 74 (collectively, the claimed “semiconductor LED”) as seen in the annotated figure 7 below:



(Ex. 1005, FIG. 7 (annotated).)

78. While the embodiment shown in figure 6 of Tanaka uses bonding wires to connect the N- and P-type semiconductor layers to the wiring pattern 80, the figure 7 embodiment includes electrodes 51, 52 that are connected directly to the wiring pattern by, for example, a conductive adhesive. (Ex. 1005, ¶¶[0068] (reproduced below), [0072] (“In this case, an N-side electrode 52 and a P-side electrode 51 are adjusted in height, and each of the electrodes 51, 52 is connected directly to a respective wiring pattern 80 via an anisotropic conductive layer or a conductive adhesive.”).)

The N-type semiconductor layer 72 has an exposed portion formed with an N-side electrode 52, whereas the P-type semiconductor layer 74 includes a surface formed with a P-side electrode 51. In this embodiment, the chip is mounted on a depression 21 formed on the first surface 20a with the sapphire substrate 71 positioned below. Each of the N-side electrode 52 and the P-side electrode 51 is connected, by wire bonding, to a corresponding wiring pattern 80 arranged on the first surface 20a.

(*Id.*, ¶[0068].)

79. Tanaka also discloses that its electrode layers 51 and 52 are made of metal, where such metal electrodes function as reflectors :

The first and second electrode layers 51, 52 are formed by vapor deposition or sputtering, and their coverage areas are selected by

etching. **The electrode layers 51, 52 are made of an Au- or Ag-based metal material for example.**

(*Id.*, ¶[0061] (emphasis added).)

Further, in the illustrated embodiment, the exposed portion of the GaN-based semiconductor laminate 40 at the first surface 20a side is completely covered with a metal electrode layer (the first electrode layer 51). **Consequently, the metal electrode layer serves as a reflector for efficiently reflecting light, traveling from the activation layer 42 upward in FIG. 1A, toward the light guide 30,** which also results in significant improvement in light-emitting efficiency.

(*Id.*, ¶[0054] (excerpted and emphasis added); *see also id.*, ¶[0051] (“The first electrode layer 51 is formed by vacuum sputtering or vapor deposition of an Au- or Ag-based conductive metal optionally combined with etching.”).)¹⁸ Thus, a person of ordinary skill in the art would have understood that Tanaka’s electrode layers 51,

¹⁸ Reviewing Tanaka in context, a person of ordinary skill in the art would have understood that Tanaka’s description of its electrode layers 51, 52, which are described for some of its other figures, are equally applicable to the similar/same electrode layers, which include common reference numbers (51 and 52), in the figure 7 embodiment.

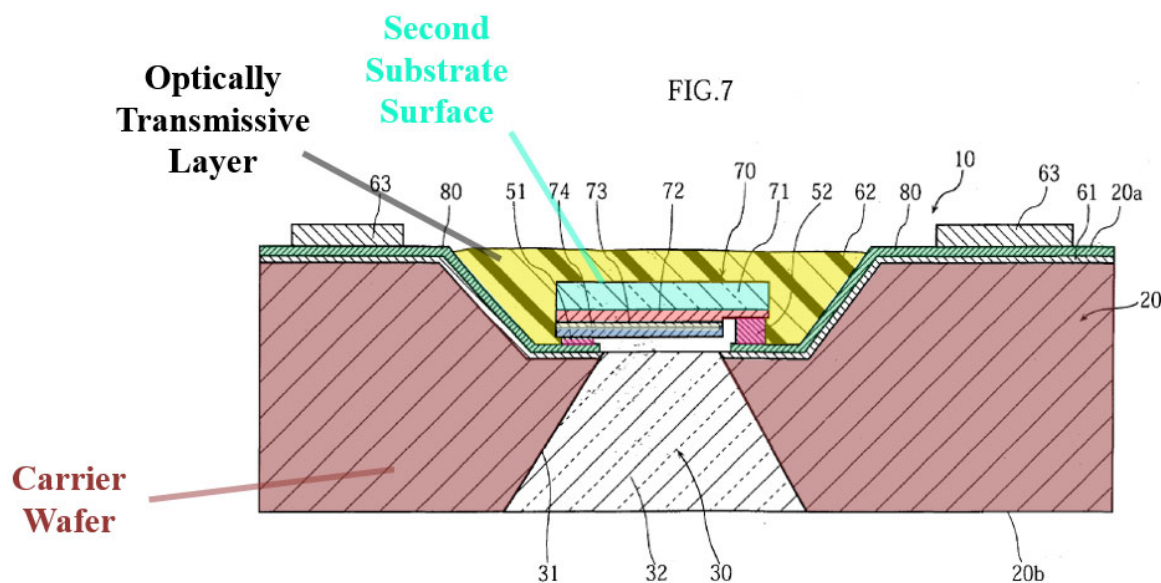
52 provide “at least one optically reflective surface,” as claimed. (Ex. 1005, ¶¶[0051], [0054], [0061], [0072].)

80. For example, a person of ordinary skill in the art would have recognized that irrespective of the LED configuration in Tanaka’s embodiments, a metal electrode would reflect light based on Tanaka’s own description of such electrodes and the knowledge of a person of ordinary skill in the art. Indeed, Tanaka’s electrode layers 51, 52 are much like the ’612 patent’s p-type pad 23, which, as the ’612 patent describes, “can be fabricated to provide optical reflections.” (Ex. 1001, 5:66–6:2.)

81. Therefore, it is my opinion that Tanaka discloses or suggests at least one optically reflective surface disposed between said carrier wafer and said semiconductor LED, as claimed.

g) a substantially optically transmissive layer disposed proximal to the second substrate surface,

82. In my opinion, Tanaka discloses or suggests this feature. For example, Tanaka discloses a protective member 62 (“substantially optically transmissive layer”) disposed proximal to the second substrate surface of sapphire substrate 71 (“substrate”) as seen in the annotated figure 7 below:



(Ex. 1005, FIG. 7 (annotated); *see also* my discussions above at Section IX.A.1.b.)

83. Tanaka’s protective member 62 is a “substantially optically transmissive layer” at least because it is made of epoxy resin that allows for light transmission there through: “The depression 21 on the first surface 20a is also filled with a **protective member 62 such as epoxy resin** to protect the chip 70 and the bonding wires 75.” (Ex. 1005, ¶[0069] (emphasis added).) As Tanaka confirms, the epoxy resin is a material that allows for light transmission as it discloses that the light from the LED chip is emitted through the hole 31, which may be filled with epoxy resin 32, i.e., the same material constituting protective member 62. A person of ordinary skill in the art would have understood that the same epoxy resin would have been used to fill hole 31 and for the protective member 62, as Tanaka discloses

that the resin used to fill the hole also acts as a protective member and using the same resin would have simplified the manufacturing process.

The hole 31 is preferably filled with a translucent resin 32 such as epoxy resin. **The epoxy resin serves as a light guide 30 for guiding light emitted from the GaN-based semiconductor laminate 40 toward from the second surface 20b side while also serving as a protective member for the semiconductor laminate 40.** The epoxy resin may be contain a light scattering material such as fluorescent or metallic particles.

(*Id.*, ¶[0053] (emphasis added); *see also id.*, ¶¶[0054] (“As described above, **when the light guide 30 (epoxy resin 32) contains a fluorescent or light scattering material, light can be adjusted [and] emitted efficiently from the entire mouth of the light guide 30 beyond the second surface 20** while also providing a possibility for color adjustment.”) (emphasis added), [0063] (“Next, the depression 21 of the first surface 20a is filled with a protective member 62, and the hole 31 is filled with translucent resin 32 such as epoxy resin.”), [0069] (“As in the first embodiment, the hole 31 formed in the monocrystal silicon substrate 20 is preferably filled with translucent resin 32 such as epoxy resin.”).)

84. Thus, a person of ordinary skill in the art would have understood based on Tanaka’s disclosures and the knowledge of a person of ordinary skill in the art that the epoxy resin in protective member 62 would have been “substantially optically transmissive,” as claimed.

85. Further, as shown in annotated figure 7 above, the protective member 62 is proximal to the second substrate surface of the sapphire substrate 71.

86. Therefore, it is my opinion that Tanaka discloses or suggests a substantially optically transmissive layer disposed proximal to the second substrate surface, as claimed.

h) wherein the carrier wafer and the thermally conductive layer define a relief to expose at least a portion of the second LED surface.

87. In my opinion, Tanaka discloses or suggests this feature. For example, Tanaka discloses that the monocrystal silicon substrate 20 (“carrier wafer”) and the wiring pattern 80 (“thermally conductive layer”) define an area (“relief”) that includes the hole 31 and exposes at least a portion of the second LED surface of the semiconductor LED (e.g., the bottom surface of the P-type semiconductor layer 74). Tanaka discloses or suggests this feature in at least two ways, as I discuss below.

88. I have been asked to assume a first scenario in which this feature is understood to mean that the claimed relief may be filled with material such that a portion of the second LED surface is covered and not exposed to the environment. In such a scenario, Tanaka discloses an area that includes hole 31 that can be filled with epoxy resin 32. (Ex. 1005, ¶[0053] (“The hole 31 is preferably filled with a translucent resin 32 such as epoxy resin.”).) For example, Tanaka discloses that “as shown in FIG. 3E, the monocrystal silicon substrate 20 is formed with a hole 31

extending from the second surface 20b to partially expose the bottom surface of the GaN-based semiconductor laminate 40.” (Ex. 1005, ¶[0062]; *see also id.*, ¶¶[0049] (“The monocrystal silicon substrate 20 is formed with a thorough-hole 31 extending thicknesswise from the bottom of the depression 21 to the second surface 20b.”), [0050], [0069], [0072].)¹⁹

89. Similar to the semiconductor LED of the figure 7 embodiment, which includes the N-type semiconductor layer 72, activation layer 73, and P-type semiconductor layer 74 (*see my discussion above at Section IX.A.1.c*), the semiconductor laminate 40 in Tanaka’s figure 3E embodiment includes an N-type semiconductor layer 41, an activation layer 42, and a P-type semiconductor layer 43 (*Id.*, ¶¶[0040], [0059]). Thus, when Tanaka describes forming a hole 31 to partially expose the bottom surface of its semiconductor laminate 40 concerning figure 3E (Ex. 1005, ¶[0062]), a person of ordinary skill in the art would have similarly understood that the hole 31 partially exposes the bottom surface of the second LED

¹⁹ Reviewing Tanaka in context, a person of ordinary skill in the art would have understood that Tanaka’s description of its components, e.g., the monocrystal silicon substrate 20 and hole 31, which are described based on some of its other figures, are equally applicable to the similar/same components in the figure 7 embodiment.

This diagram shows a cross-sectional view of a semiconductor device. A central rectangular region is labeled '1' and is surrounded by a yellow hatched area. This yellow area is further enclosed by a green hatched area. The entire structure is built on a red hatched substrate. A red dashed line outlines a trapezoidal region within the substrate, labeled '30'. Inside this region, there are two smaller areas labeled '31' and '32'. The top surface of the device is labeled '20a' and '20b'. Various other labels (63, 80, 51, 74, 73, 72, 70, 71, 52, 62, 80, 10, 61) point to different layers and features. A green arrow points to the yellow hatched area, labeled 'Thermally Conductive Layer'. A red arrow points to the red dashed line, labeled 'Relief'.

90. Moreover, as shown in annotated figure 7 above, the monocrystal silicon substrate 20 and the wiring pattern 80 define the area corresponding to the claimed “relief” because, for example, the area including the hole is formed by etching through the monocrystal silicon substrate 20 (*id.*, ¶[0062]) and the width of the hole near the P-type semiconductor layer 74 is approximate to the gap between the wiring pattern 80.

91. Tanaka’s teachings regarding the area that includes hole 31 and exposes the LED surface tracks the teachings of the ’612 patent. For example, the ’612 patent similarly describes its relief, which it describes as a “via (hole)” or a “thermally

conducting hole” in the figure 5 embodiment, which are formed by etching through the silicon wafer 31 (example of the claimed carrier wafer). (Ex. 1001, 8:60–9:28, FIG. 5.)

92. Tanaka also discloses or suggests this feature where the claimed relief is understood to be free of material such that a portion of the second LED surface is left uncovered and exposed to the environment, as shown in Figure 5 of the ’612 patent. (Ex. 1001, 9:1-28, FIG. 5 (showing a thermally conducting hole 53 exposing a surface of the GaN LED layer to the environment).)

93. For example, Tanaka discloses that “[a]ccording to a preferred embodiment the light guide comprises a hole penetrating the monocrystal silicon substrate thicknesswise, and the GaN-based semiconductor laminate includes a lowermost layer whose surface includes a portion substantially exposed to the second surface.” (Ex. 1005, ¶[0015].) Tanaka also discloses that “the hole **may be preferably filled** with translucent resin.” (*Id.*, ¶[0016] (emphasis added); *see also id.*, ¶[0053] (disclosing that the “hole 31 is **preferably filled** with a translucent resin.”) (emphasis added).)

94. Because Tanaka discloses that hole 31 *may be* filled with a translucent resin, Tanaka discloses, or at least suggests, that hole 31 is left unfilled in some embodiments. My opinion is reinforced by at least claims 2 and 3 of Tanaka. For example, claim 2 recites such a hole where the surface of the lowermost layer of the

semiconductor laminate is exposed, whereas claim 3, which depends from claim 2, states that “the hole is filled with translucent resin.” (*Compare id.*, claim 2 with claim 3.)

95. A person of ordinary skill in the art would have also understood that the extra protection or possible light scattering features of the resin 32 are unnecessary in some applications. In such applications, such a person of ordinary skill in the art would have known not to include resin 32 in the hole 31 to simplify the manufacturing of the LED device and reduce costs.

96. The understanding of a person of ordinary skill in the art that unfilled hole on the backside of such a light emitting device can be used to allow efficient light emission is further supported by Weeks (Ex. 1006).²⁰ For example, Weeks explicitly discloses forming a hole (via) that exposes the surface of an LED, similar to the hole (via) formed in Tanaka’s figure 7 embodiment, where the hole in Weeks “is free of any material formed therein.” (*Id.*, 8:57–58.) As shown in annotated figure 14 of Weeks below, light generated in the active region 97 exits the device through the hole (via) 24.

²⁰ I refer to Weeks (Ex. 1006) to demonstrate the knowledge of a person of ordinary skill in the art at the time of the alleged invention of the ’612 patent.

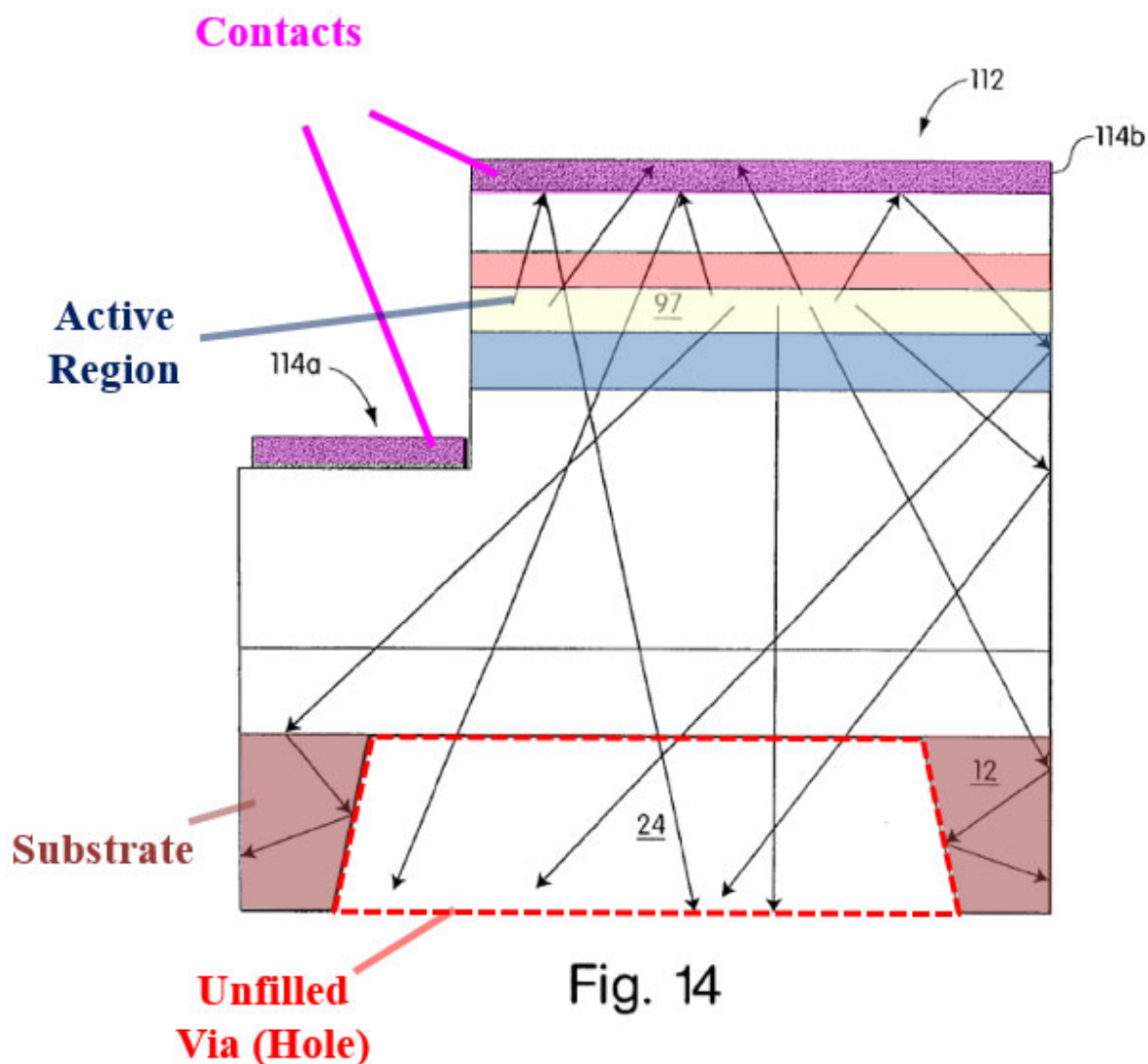


Fig. 14

(*Id.*, FIG. 14 (annotated); *see also id.*, FIG. 1.)

97. Weeks, like Tanaka, discloses GaN LED structures with a light emitting active region, and a hole (via) is provided on the other side to allow the generated light to be emitted from the LED structure. (*Id.*, 8:47–67, 12:50–56, 13:35–58, 14:60–66, 15:50–60, FIGs. 14, 17.) Weeks discloses that in LED embodiments like that shown in figure 14 above, the hole (via) can be left unfilled and free of material

in order to expose the gallium nitride material device to the outside, which can enhance the extraction of light from the device:

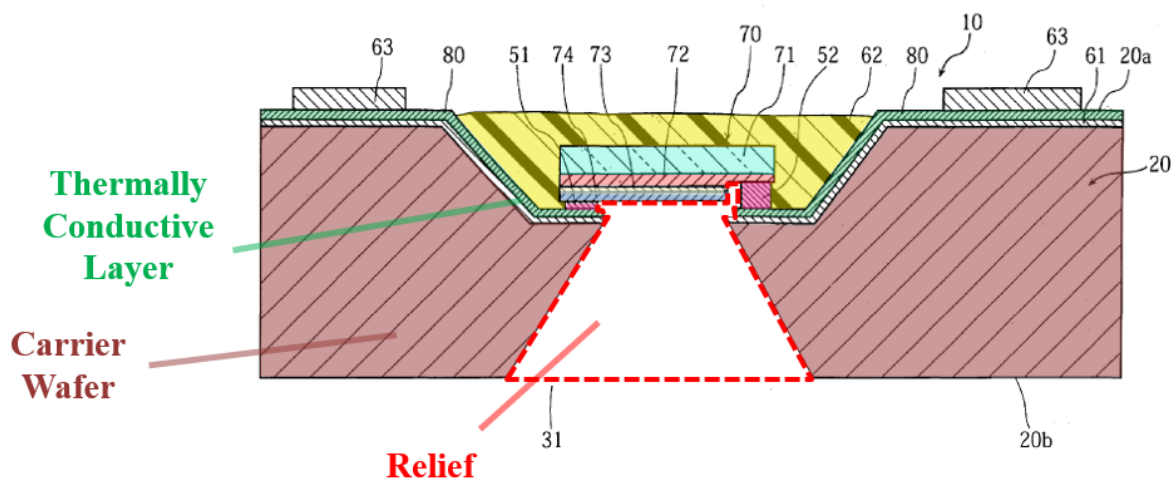
In certain embodiments, and as described further below in connection with FIGS. 9-11, 13-14, and 16-18, it may be preferable for via 24 to be free of a contact. That is, a contact is not formed within the via. In some cases, the via may be free of a contact but may have one or more other regions(s) or layer(s) formed therein (e.g., a reflective layer), as described further below. In some cases, the **via may be free of any material formed therein. When free of material, the via may function as a window that exposes internal layers of the device** (e.g. a transition layer 15 or gallium nitride material device region 14) **to the outside. This exposure may enhance the extraction of light from the device which can be particularly useful in light-emitting devices such as LEDs or lasers.** In embodiments in which via 24 is free of an electrical contact, it should be understood that contacts are formed on other parts of the device including other (non-via) areas of backside 22 or areas of topline 18.

(*Id.*, 8:51–67 (emphasis added).)

98. Thus, Weeks confirms the understanding of a person of ordinary skill in the art concerning Tanaka's disclosure that hole 31 can either be filled or left unfilled. A non-limiting example of Tanaka's light emitting element is seen in modified figure 7 below, where hole 31 is left unfilled. The unfilled hole constitutes

a “relief” defined by the carrier wafer and a thermally conductive layer that exposes portions of the n- and p-doped layers to the outside.

FIG.7



(Ex. 1005, FIG. 7 (modified, annotated).) Therefore, it is my opinion that Tanaka discloses or suggests this feature where the relief is free of material such that a portion of the second LED surface is left uncovered and exposed to the environment, as shown in Figure 5 of the '612 patent.

99. Thus, it is my opinion that Tanaka discloses or suggests that the carrier wafer and the thermally conductive layer define a relief to expose at least a portion of the second LED surface, as claimed.

2. **Claim 2**

a) **The light emitting device of claim 1, said at least one optically reflective surface comprising metal.**

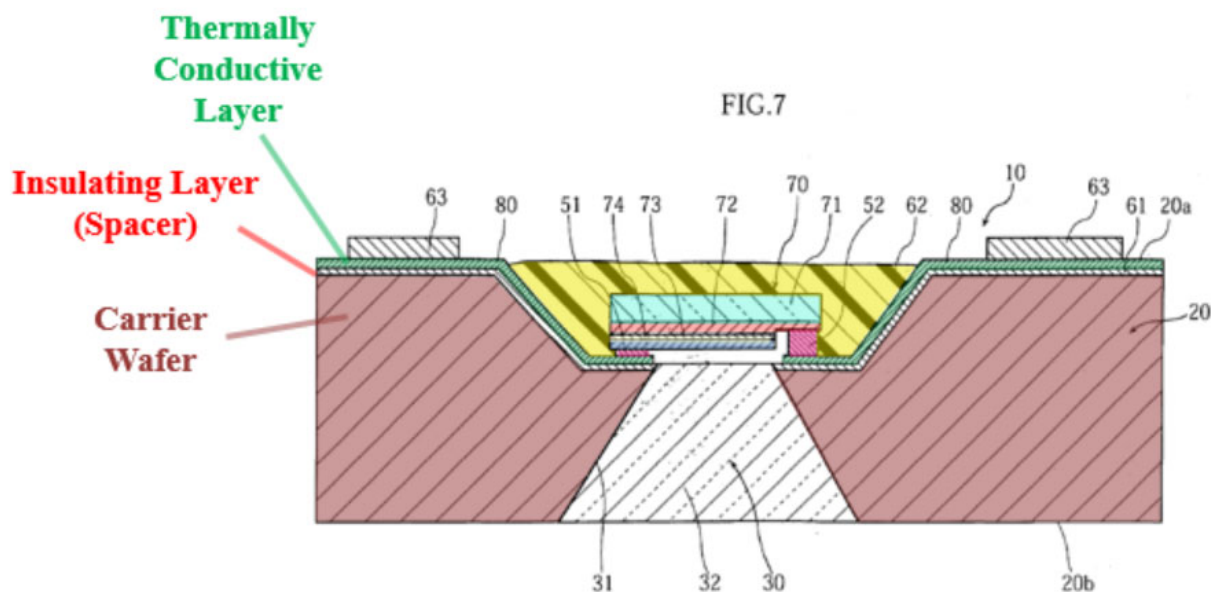
100. In my opinion, Tanaka discloses or suggests this feature. For example, as I noted above, Tanaka discloses that its electrode layers 51, 52 (“at least one optically reflective surface”) include metal. (See my discussions above at Section IX.A.1.f; Ex. 1005, ¶¶[0061] (“The electrode layers 51, 52 are made of an Au- or Ag-based **metal** material for example.”) (emphasis added), [0054] (“Further, in the illustrated embodiment, the exposed portion of the GaN-based semiconductor laminate 40 at the first surface 20a side is completely covered with a **metal** electrode layer (the first electrode layer 51).”) (emphasis added); *see also id.*, ¶[0051] (“The first electrode layer 51 is formed by vacuum sputtering or vapor deposition of an Au- or Ag-based conductive **metal** optionally combined with etching.”) (emphasis added).) Thus, Tanaka discloses or suggests that the at least one optically reflective surface as recited in claim feature 1(f) includes metal.

3. Claim 8

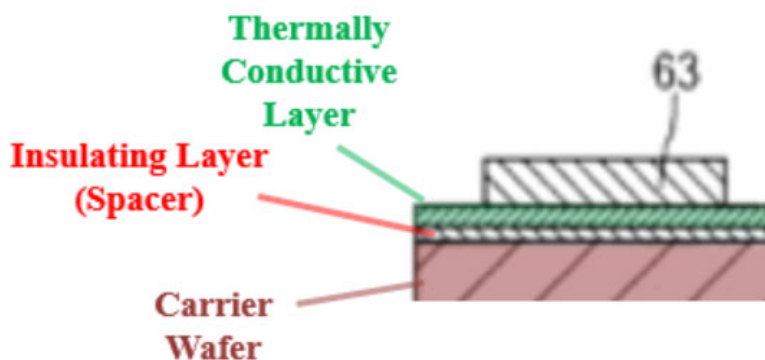
a) **The light emitting device of claim 1, further comprising at least one spacer attached to said carrier wafer; whereby, said at least one optically reflective surface is affixed thereto.²¹**

101. Tanaka discloses or suggests claim 8. For example, Tanaka discloses an insulating layer 61 (“at least one spacer”) attached to the monocrystal silicon substrate 20 (“carrier wafer”), whereby, at least one of the electrodes 51, 52 (“said at least one optically reflective surface”) is affixed thereto, as discussed below. (Ex. 1005, ¶[0072]; *see* my discussion above at Sections IX.A.1.e-f.) The insulating layer 61 (“spacer”) is highlighted in annotated figure 7 and in an enlarged excerpt of figure 7 of Tanaka below.

²¹ I have reviewed the specification of the ’612 patent and I did not find any disclosure describing the “at least one spacer” feature recited in claim 8. (*See, e.g.*, Ex. 1001, generally.)



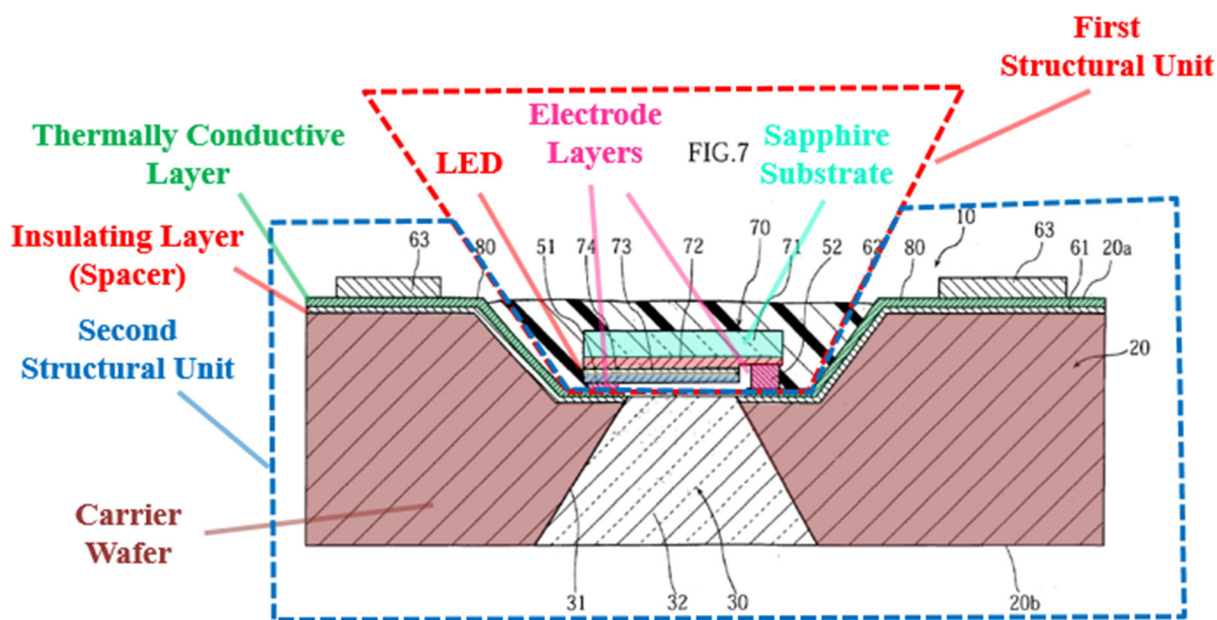
(Ex. 1005, FIG. 7 (annotated).)



(Ex. 1005, FIG. 7 (excerpt, annotated).)

102. In particular, Tanaka discloses with respect to its figure 7 embodiment discussed above with respect to claim 1 that “each of the electrodes 51, 52 is connected directly to a respective wiring pattern 80 via an anisotropic conductive layer or a conductive adhesive.” (Ex. 1005, ¶[0072], FIG. 7.) A person of ordinary skill in the art would have understood that in Tanaka’s LED device, at least the

sapphire substrate 71, semiconductor LED (N-type semiconductor layer 72, activation layer 73, P-type semiconductor layer 74), and electrodes 51, 52 constitute a first structural unit (the blue-color light-emitting diode chip 70) while at least the wiring pattern 80, monocrystal silicon substrate 20, and insulating layer 61 constitute a second structural unit. (*Id.*) The first and second structural units are shown in the annotated figure 7 below.



(Ex. 1005, FIG. 7 (annotated).)

103. With respect to the first structural unit, Tanaka discloses:

The blue-color light-emitting diode chip 70 **fabricated** in the conventional manner has a sapphire substrate 71 including an upper surface successively formed with an N-type

semiconductor layer 72 (GaN layer or AlGaN layer), an activation layer 73 (InGaN layer), and a P-type semiconductor layer 74 (GaN layer or AlGaN layer). **The N-type semiconductor layer 72 has an exposed portion formed with an N-side electrode 52, whereas the P-type semiconductor layer 74 includes a surface formed with a P-side electrode 51.**

(Ex. 1005, ¶[0068].) Thus, a person of ordinary skill in the art would have understood that the *fabricated* blue-color light-emitting diode chip 70 includes each of the sapphire substrate 71, N-type semiconductor layer 72, activation layer 73, P-type semiconductor layer 74, and electrodes 51, 52 such that they constitute a first structural unit in Tanaka's LED device.

104. Similarly, with respect to the second structural unit, Tanaka discloses:

Each of the N-side electrode 52 and the P-side electrode 51 is connected, by wire bonding, to a corresponding **wiring pattern 80 arranged on the first surface 20 a** [of monocrystal silicon substrate 20]. **Wiring patterns 80** corresponding to the N-side electrode 52 and the P-side electrode 54 **extend to suitable portions on the first surface 20 a** where bumps 63 are formed. **Each wiring pattern 80 has a lower surface formed with an insulating layer 61 made of e.g. silicon oxide film for insulation from the monocrystal silicon substrate 20.**

(Ex. 1005, ¶[0068]; *see also id.*, ¶[0067].) A person of ordinary skill in the art would have understood that because wiring pattern 80 is “arranged on” the surface 20a of

the silicon substrate 20 (“carrier wafer”) and “extends to suitable portions on the first surface 20a,” and the wiring pattern is further “formed with” an insulating layer 61, the wiring pattern 80, silicon substrate 20, and insulating layer 61 constitute a second structural unit in Tanaka’s LED device.

105. This understanding is further corroborated by Tanaka’s disclosure that given the substrate 20 is made of monocrystal silicon, a “wafer process maybe performed on the first surface 20a of the substrate 20 to form another element or a set of elements 90” such that the substrate 20 can include elements such as “a current regulating drive circuit or a logic circuit as a part of an IC-built-in semiconductor light-emitting element, or [] a discrete element such as a diode, or sensor or the like.” (Ex. 1005, ¶[0055], FIG. 1B; *see also id.*, ¶[0067] (describing with respect to the figure 6 embodiment that “similarly to the first embodiment [including FIG. 1B], the monocrystal silicon substrate 20 ***may be formed integrally*** with a current regulating drive circuit or a logic circuit by wafer process.”).)²² A person of ordinary skill in the art would have understood that if discrete elements are formed on the first surface 20a of the substrate 20, then a wiring pattern such as wiring pattern 80 connecting such discrete elements would have been included on the first surface 20a of the substrate 20.

²² See my footnote n.4 above.

106. Tanaka's insulating layer 61 ("at least one spacer") is attached to the monocrystal silicon substrate 20 ("carrier wafer") because Tanaka describes that the "wiring pattern 80 has a lower surface formed with an insulating layer 61 . . . for insulation from the monocrystal silicon substrate 20." (Ex. 1005, ¶[0068].) A person of ordinary skill in the art would have understood that the insulating layer 61 is a "spacer" as it provides spacing between the monocrystal silicon substrate 20 and the electrodes 51, 52.

107. Moreover, a person of ordinary skill in the art would have understood that when Tanaka discloses that an anisotropic conductive layer or a conductive adhesive is used to bond electrodes 51, 52 to the wiring pattern 80 (Ex. 1005, ¶[0072]), then the electrodes 51, 52 ("said at least one optically reflective surface"), which are part of the first structural unit, are "affixed to" the insulating layer 61 ("at least one spacer"), which is part of the second structural unit (and is formed at the lower surface of wiring pattern 80).

108. Therefore, Tanaka discloses at least one spacer attached to said carrier wafer; whereby, said at least one optically reflective surface is affixed thereto, as claimed.

4. Claim 9

a) The light emitting device of claim 1, said thermally conductive layer comprises metal.

109. In my opinion, Tanaka discloses or suggests this feature. For example, as I noted above, a person of ordinary skill in the art would have been motivated to configure Tanaka's wiring pattern 80 ("thermally conductive layer") such that it is made of metal, as claimed. (*See* my discussions above at Section IX.A.1.d.) Thus, Tanaka discloses or suggests that the thermally conductive layer comprises metal.

B. Tanaka in Combination with Weeks Discloses or Suggests the Features of Claim 3

110. In my opinion, Tanaka and Weeks disclose or suggest the features of claim 3.

1. Claim 3

a) The light emitting device of claim 1, said at least one optically reflective surface comprising a dielectric stack.

111. In my opinion, Tanaka in combination with Weeks discloses or suggests claim 3. For example, Tanaka discloses that its electrode layers 51, 52 (“at least one optically reflective surface”) may be made of metal. (*See* my discussions above at Sections IX.A.1.f, IX.A.2; Ex. 1005, ¶[0061] (“The electrode layers 51, 52 are made of an Au- or Ag-based **metal** material **for example**.”) (emphasis added).)

112. Tanaka is silent regarding its electrode layers 51, 52 including a dielectric stack. However, Weeks discloses a Distributed Bragg Reflector (DBR) with dielectric layers, and as discussed below, a person of ordinary skill in the art would have been motivated to include such a Distributed Bragg Reflector in an LED device like that depicted in figure 7 of Tanaka in order to further improve reflection of light in a desired direction.

113. Weeks, like Tanaka, relates to fabrication of LED devices. (Ex. 1006, Abstract, 1:15–49, 8:51–67; *see also* my discussions above at Sections VIII.A (Overview of Tanaka), VIII.B (Overview of Weeks).) For example, as noted above, Weeks discloses GaN LED structures with a light emitting active region and a hole

or via is provided on the other side in order to allow the generated light to be emitted from the LED structure. (Ex. 1006, 8:47–67, 12:50–56, 13:35–58, 14:60–66, 15:50–60, FIGs. 14, 17, 20.) Both Tanaka and Weeks are also concerned with improving the reflection of light in LED devices to improve light efficiency. (Ex. 1005, ¶¶[0054] (“[T]he metal electrode layer serves as a reflector for efficiently reflecting light, traveling from the activation layer 42 upward in FIG. 1A, toward the light guide 30, which also results in significant improvement in light-emitting efficiency.”), [0070], [0072]; Ex. 1006, 7:23–41, 8:33–67, 10:8–46, 16:42–17:11.) Thus, a person of ordinary skill in the art would have been motivated to consider Weeks’ teachings when implementing reflective surfaces like those disclosed with respect to Tanaka’s figure 7 embodiment. (*Id.*, ¶[0072].)

114. In this regard, Weeks discloses with respect to its figure 20 embodiment an LED 136 that includes a reflector with two reflection regions: a topside contact 114b (first reflector region) and a Distributed Bragg Reflector (DBR) 120b (second reflector region).

FIG. 20 illustrates a light emitting device 136 that has been flipped during use so that backside 22 faces upward and topside 18 faces downward. **Topside contact 114b also functions as a reflector region** that can upwardly reflect light generated in region 97. The device also includes **a second reflector region**

**120b which may be a Distributed Bragg Reflector (DBR) that
includes a number of semiconductor or dielectric layers.**

(Ex. 1006, 16:62–17:2.)

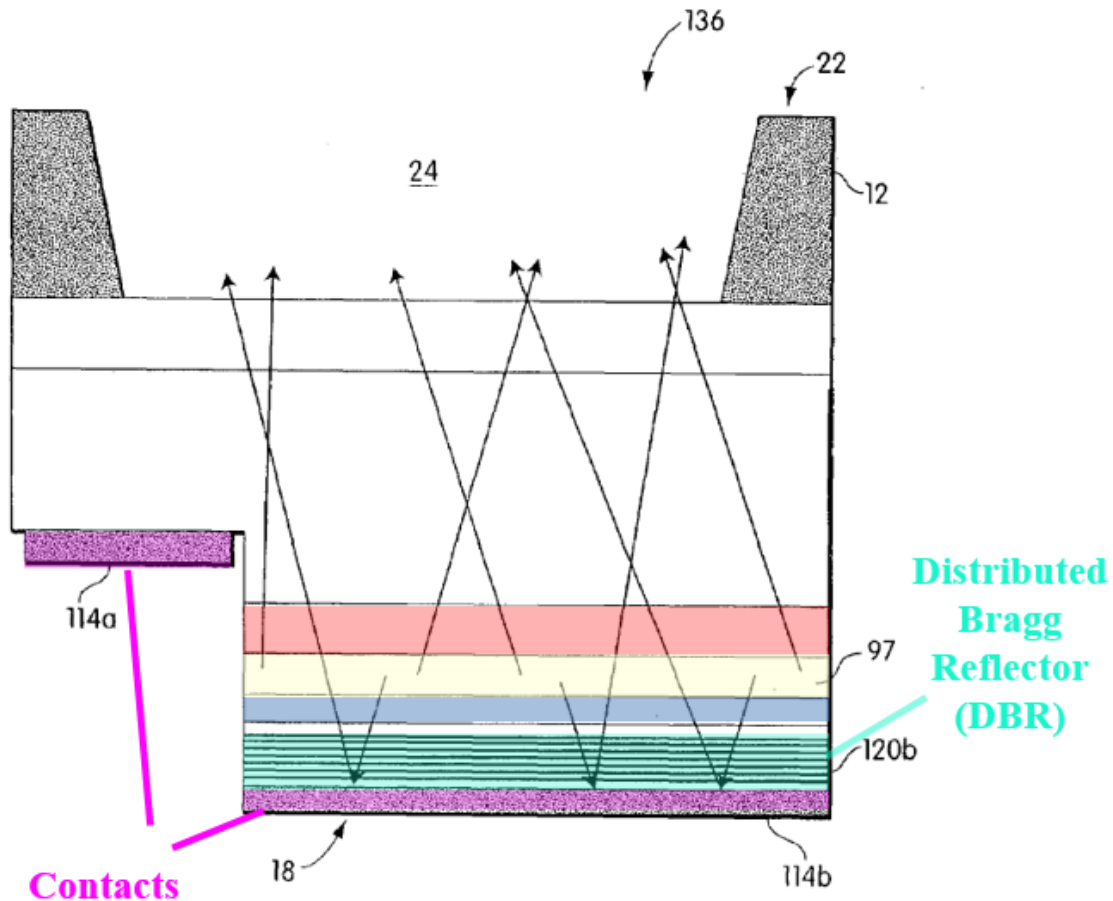
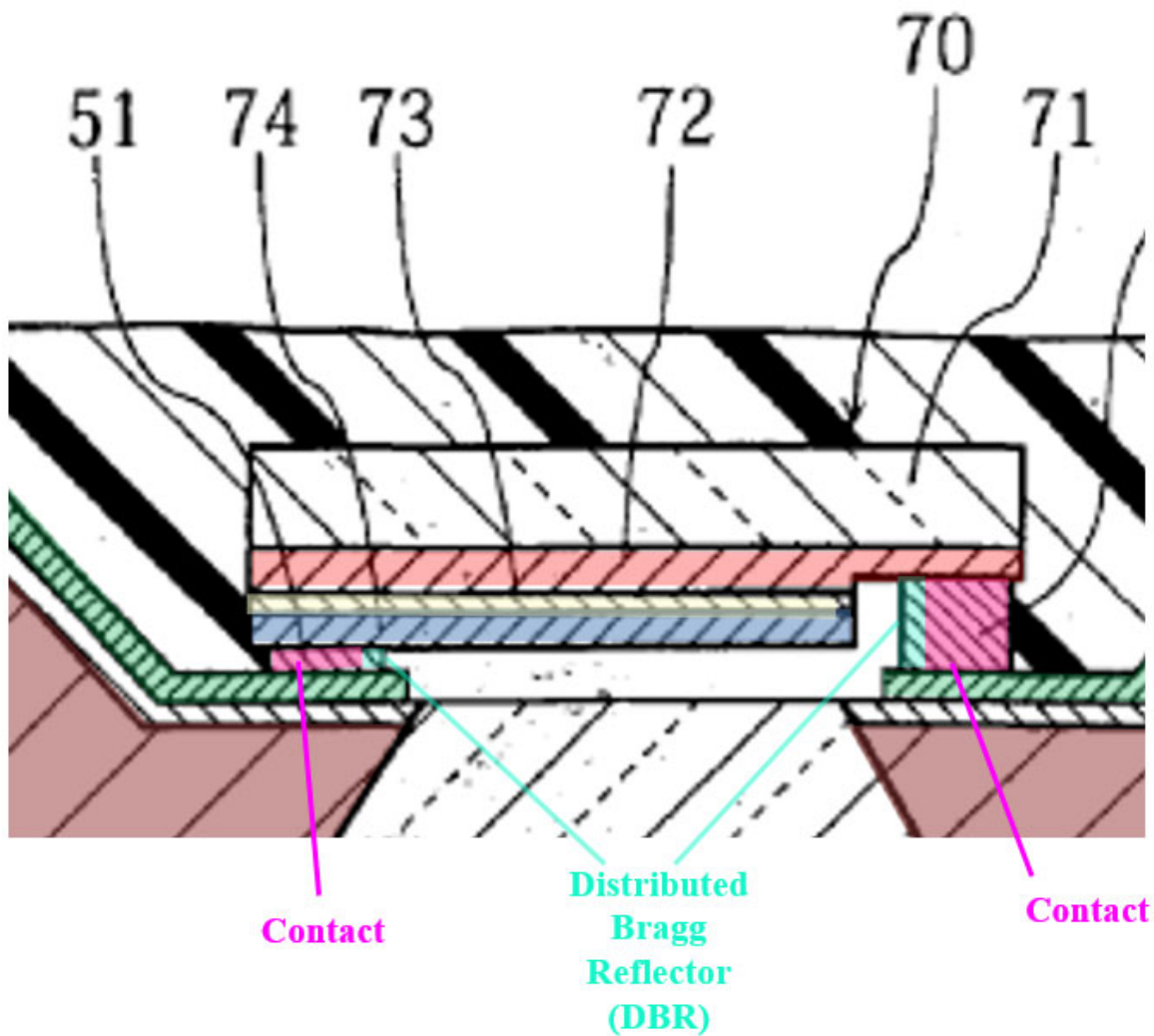


Fig. 20

(*Id.*, FIG. 20 (annotated).)

115. Since the DBR 120b includes a number of dielectric layers (Ex. 1005, ¶[0072]), a person of ordinary skill in the art would have understood that the DBR 120b discloses an optically reflective surface including a dielectric stack, as claimed.

116. As I discuss below, a person of ordinary skill in the art would have been motivated to include a reflective surface like Weeks' DBR 120b with the electrodes 51, 52 in Tanaka's LED device to improve light reflection in the desired direction, and thereby improve device performance. A person of ordinary skill in the art would have been motivated to include such a reflective surface to provide additional layers of protection from light leaking into undesired portions of the device. For example, a person of ordinary skill in the art would have been motivated to include a DBR like the one disclosed in Weeks on the inner sides of electrodes 51 as shown in the enlarged annotated excerpt of figure 7 below, so that the DBR could reflect light toward the desired direction.



(Ex. 1005, FIG. 7 (excerpt, annotated).)

117. Moreover, any light not reflected by the DBR could then be reflected by the surface of the electrodes 51, 52, thus providing a device with improved light reflection capability. That is, the surfaces of electrodes 51, 52 and the surfaces of the DBRs on the inner sides of these electrodes would serve as the claimed at least one optically reflective surface. Indeed, such a configuration would be similar to the configuration disclosed by Weeks' figure 20 embodiment, where the DBR 120b

provides a first layer for light reflection and the contact 114b provides a second layer of light reflection such that any light that is not reflected by DBR 120b is reflected by the contact 114b. (Ex. 1006, 16:62–17:11, FIG. 20.) Weeks specifically recognizes the advantage of such a configuration: “Device 136 includes two reflector regions to increase the ability of the device to reflect generated light in the desired direction.” (*Id.*, 17:2–4, FIG. 20.) Moreover, a person of ordinary skill in the art would have understood that the inclusion of a DBR would provide additional advantages as DBRs can be designed to provide custom reflectances at particular wavelengths, which can be beneficial in certain LED applications. For example, Schubert (Ex. 1017) discloses such an application in Chapter 10 on Reflectors:

The reflectance spectra of a metal mirror and a DBR are compared in Fig. 10.6. Whereas metal reflectors exhibit a broad band with high reflectivity, **DBRs display only a narrow band of high reflectivity denoted as the stop band.** However, while the metal reflector has a certain reflectivity, **the DBR’s reflectivity can be increased by increasing the number of reflector pairs so long as these reflector pairs are fully transparent.**

For LED structures on light-absorbing substrates, about 50% of the light emitted by the active region is absorbed by the substrate. This represents a substantial loss. The absorption of light in the substrate can be avoided by placing a reflector between the substrate and the LED active layers. Light emanating from the

active region towards the substrate will then be reflected and can escape from the semiconductor through the top surface.

Distributed Bragg reflectors (DBRs) are well suited for inclusion between the substrate and the active layers. The schematic LED structure with a DBR is shown in Fig. 10.7. LEDs with DBRs were first demonstrated by Kato et al. (1991) in the AlGaAs/GaAs material system. The LED had a 25-pair AlAs/GaAs or AlGaAs/GaAs DBR and emitted in the infrared at 870 nm

(Ex. 1017, 170–181 (excerpted and emphasis added).)²³

118. Therefore, a person of ordinary skill in the art would have been motivated in light of Weeks' teachings to use a DBR like DBR 120b with multiple dielectric layers as an optically reflective surface in Tanaka's semiconductor LED device (as discussed above) to enhance light-emission efficiency and improve device performance. (Ex. 1005, ¶¶[0054], [0070], [0072]; Ex. 1006, 7:23–41, 8:33–67, 10:8–46, 16:42–17:11.) Such an implementation would have been a straightforward combination of well-known technologies using known methods and would have had predictable results.

²³ I refer to Schubert (Ex. 1017) to demonstrate the knowledge of a person of ordinary skill in the art at the time of the alleged invention of the '612 patent.

119. A person of ordinary skill in the art facing the wide range of needs created by developments in the technical field of Tanaka and Weeks would have appreciated the benefits of using a DBR like Weeks' DBR 120b with Tanaka's LED device. For instance, incorporating the teachings of Weeks regarding the DBR 120b into Tanaka's LED device as proposed would provide the benefit of minimizing the amount of light leaking into undesired portions of the LED device by providing multiple reflective surfaces to direct the generated light in the desired direction. A person of ordinary skill in the art would have been skilled and knowledgeable about configuring Tanaka's LED device to include a DBR like DBR 120b, while considering any known design, and other related concepts, limitations, benefits, and the like to ensure the resulting combination operated properly and as intended. Thus, a person of ordinary skill in the art would have had a reasonable expectation of success in the above modification.

120. Therefore, it is my opinion that the combination of Tanaka and Weeks discloses or suggests at least one optically reflective surface comprising a dielectric stack, as claimed.

C. Tanaka in Combination with Chitnis Discloses or Suggests the Features of Claims 4–7

121. In my opinion, Tanaka and Chitnis disclose or suggest all of the claim elements of claims 4–7. Below, I address each claim element of the claims.

1. Claim 4

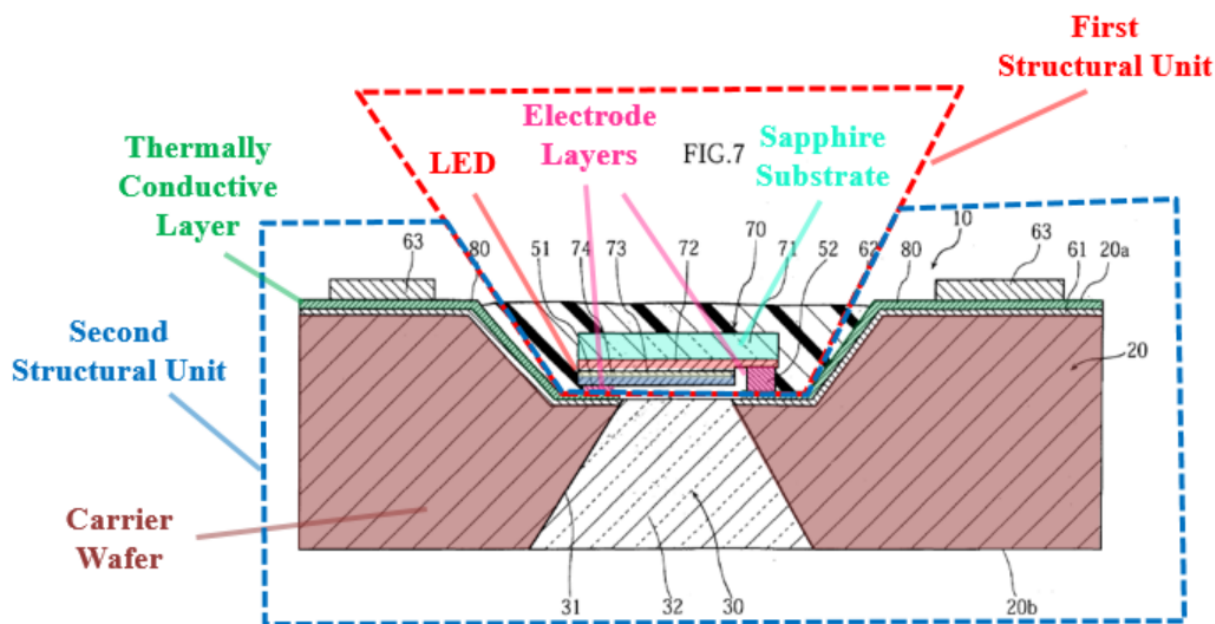
a) The light emitting device of claim 1, wherein said semiconductor LED is affixed to said carrier wafer with an adhesive material which has the property of high thermal conductivity.²⁴

122. In my opinion, Tanaka in combination with Chitnis discloses or suggests claim 4. For example, Tanaka discloses that the blue-color light-emitting diode chip 70 with N-type semiconductor layer 72, activation layer 73, and P-type semiconductor layer 74 (collectively, the claimed “semiconductor LED”) is affixed to the monocrystal silicon substrate 20 (“carrier wafer”) with an adhesive (“adhesive material”). (See my discussions above at Sections IX.A.1.c, IX.A.1.e.) And as I discuss further below, a person of ordinary skill in the art would have been motivated to use an adhesive that had the property of high thermal conductivity in light of the knowledge of such a skilled person and the teachings of Chitnis.

123. For example, as I discussed above with respect to claim 8, a person of ordinary skill in the art would have understood that in Tanaka’s LED device, at least the sapphire substrate 71, semiconductor LED (N-type semiconductor layer 72, activation layer 73, P-type semiconductor layer 74), and electrodes 51, 52 constitute

²⁴ I have reviewed the specification of the ’612 patent and I did not find any disclosure describing the “high thermal conductivity” feature recited in claim 4. (See, e.g., Ex. 1001, generally.)

a first structural unit (the blue-color light-emitting diode chip 70) while at least the wiring pattern 80, monocrystal silicon substrate 20, and insulating layer 61 constitute a second structural unit. (See my discussions above at Section IX.A.3.) The first and second structural units are shown in the annotated figure 7 below.



(Ex. 1005, FIG. 7 (annotated).)

124. As such, a person of ordinary skill in the art would have understood that when Tanaka discloses that a conductive adhesive is used to bond electrodes 51, 52 to the wiring pattern 80, then the N-type semiconductor layer 72, activation layer 73, and P-type semiconductor layer 74 (collectively, “semiconductor LED”), which are part of the first structural unit, would have been affixed by the conductive adhesive to monocrystal silicon substrate 20 (“carrier wafer”), which is part of the second structural unit.

125. Thus, as claimed, Tanaka discloses that the semiconductor LED is affixed to the carrier wafer with an adhesive material.

126. Tanaka is silent about its conductive adhesive having the property of high thermal conductivity, as claimed. Yet as I discuss below, a person of ordinary skill in the art would have been motivated to use a conductive adhesive having the property of high thermal conductivity like that described by Chitnis with an LED device like that depicted in figure 7 of Tanaka to bond an LED chip to a wafer, like that bonding of Tanaka's blue-color light-emitting diode chip 70 (including the claimed "semiconductor LED") with the monocrystal silicon substrate 20 ("carrier wafer").

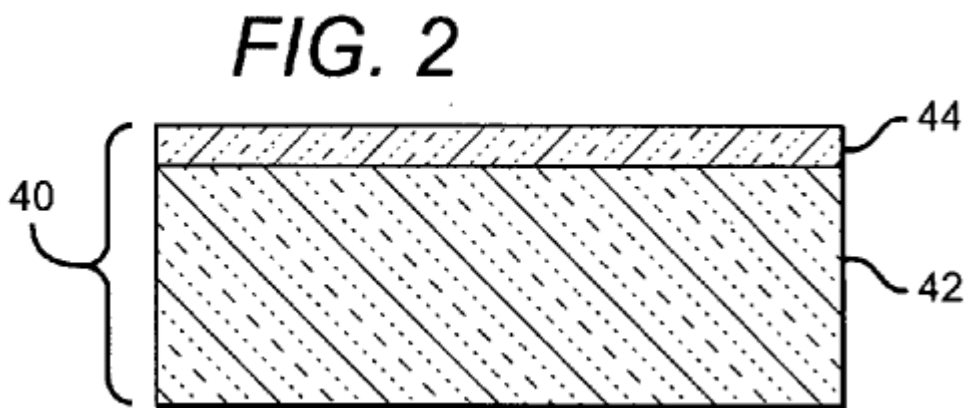
127. Chitnis, like Tanaka, relates to the fabrication of LED devices. (Ex. 1007, ¶[0004].) Through its background, Chitnis discloses well-known wafer-level bonding techniques used during LED device fabrication:

Recent developments in wafer-bonding technology have provided the means to integrate different materials into semiconductor devices. Wafer bonding is a semiconductor manufacturing process in which two semiconductor wafers are bonded to form a single substrate having specific properties. A variety of bonding methods can be used to create integrated electronics, and to combine multifunctional components onto a single die.

(Ex. 1007, ¶[0010] (excerpted); *see also id.*, ¶[0008].)

128. Based on Chitnis' disclosures, a person of ordinary skill in the art would have understood that the wafer-level bonding techniques described by Chitnis are directed to bonding similar structural units as those discussed above for Tanaka.

129. For example, as I noted above, Tanaka teaches bonding a first structural unit, which includes the LED and sapphire substrate, with a second structural unit, which includes the wiring pattern and silicon substrate. (*See* my discussions above at Sections VIII.A (Overview of Tanaka), IX.A.3.) Similarly, Chitnis is directed to bonding an LED wafer 10 shown in figures 1A-1C (including LED grown substrate 12, n- and p-type layers 16, 18, and active region 14) with a submount 40 shown in figure 2 (including a submount wafer 42 and a dielectric material 44). (Ex. 1007, ¶¶[0037], [0040], [0045].)



(*Id.*, FIG. 2; *see also* my discussions above at Section VIII.C (Overview of Chitnis).)

Thus, a person of ordinary skill in the art would have been motivated to consider

Chitnis' teachings when implementing the bonding process disclosed for Tanaka's figure 7 embodiment. (Ex. 1005, ¶[0072].)

130. Chitnis also describes that “[t]he choice of wafer bonding process used to fabricate a device is dependent upon the type of device, particularly the components and materials used to build the device.” (Ex. 1007, ¶[0011].) In this regard, Chitnis discloses that “eutectic wafer bonding is based on the use of bonding materials that form a eutectic alloy at specific temperature conditions, and **eutectic bonding media such as Au-Si, Au-Sn or Pd-Si are widely used.**” (*Id.* (emphasis added); *see also id.* (“For chip scale packages (e.g. flip chips), it would be advantageous to create devices at the wafer level with both electrical contacts on the bottom of the chip,” and that “this would require **electrically and thermally conducting bond medium** selectively deposited to avoid electrical shorting.”) (emphasis added).)

131. A person of ordinary skill in the art would have understood that the type of bonding media disclosed by Chitnis like Au-Si (gold-silicon) or Au-Sn (gold-tin) have the property of high thermal conductivity. This is because gold, silicon, and tin are all known to have high thermal conductivity. For example, Tritt (Ex. 1014) discloses:

High-thermal-conductivity materials like . . . silicon have been extensively studied in part because of their potential applications in thermal management of electronics.

(Ex. 1014, 23 (emphasis added); *see also id.*, 50 (Table 1 showing thermal conductivity of gold is 318 Watts/meter-Kelvin and tin is 64 W/m-K), 129 (Table 1 showing thermal conductivity of silicon is 124 W/m-K).)²⁵

132. A person of ordinary skill in the art would have also understood that the thermal conductivity of Au-Si or Au-Sn would be likewise high. (*E.g.*, Ex. 1014, 23, 50, 129.)

133. While the '612 patent does not provide adequate disclosure on the term “high thermal conductivity,” it discloses for its adhesive layer 41 that it can include “material optimized to provide [] heat conduction” and that “[a]s a metric for suitable performance, heat conductions of 3 W/mK or more is sufficient.” (Ex. 1001, 7:26–41.) Thus, a person of ordinary skill in the art would have understood that conductive adhesives such as Au-Si or Au-Sn, as disclosed by Chitnis, would have had the property of high thermal conductivity, as claimed. For instance, as I discuss above, the thermal conductivity of Au-Si or Au-SN would be higher than the “3 W/mK” heat conduction value described by the '612 patent. And as I discuss below,

²⁵ I refer to Tritt (Ex. 1014) to demonstrate the knowledge of a person of ordinary skill in the art at the time of the alleged invention of the '612 patent.

a person of ordinary skill in the art would have been motivated to use such a conductive adhesive to bond Tanaka's semiconductor LED with the monocrystal silicon substrate 20.

134. A person of ordinary skill in the art would have been motivated in light of Chitnis to use a conductive adhesive with the property of high thermal conductivity in Tanaka's semiconductor device (as I discussed above for claim 1) so that the bond between the first structural unit (including the semiconductor LED) and the second structural unit (including the monocrystal silicon substrate 20) could withstand heat and improve device performance. Such an implementation would have been a straightforward combination of well-known technologies using known methods and would have had predictable results.

135. A person of ordinary skill in the art would have recognized that Tanaka and Chitnis disclose features in a similar technological field. For example, as I discussed above, both Tanaka and Chitnis relate to techniques for fabricating semiconductor LED devices. (*Compare* Ex. 1005, Abstract, ¶¶[0002], [0004], [0014], [0047] *with* Ex. 1007, Abstract, ¶¶[0004]-[0006], [0008], [0010]–[0011]; *see also* my discussions in Sections VIII.A (Overview of Tanaka) and VIII.C (Overview of Chitnis).) Accordingly, a person of ordinary skill in the art would have had reason to consider the teachings of Chitnis when fabricating an LED device as described in

Tanaka given Chitnis discloses the details regarding bonding media for affixing various structures in an LED device like the structures to be bonded in Tanaka.

136. A person of ordinary skill in the art would have further recognized that implementing Chitnis' teachings for an adhesive such as Au-Si or Au-Sn with the property of high thermal conductivity in Tanaka would have improved device performance. For example, configuring Tanaka this way would have allowed the LED's generated heat to be conducted through the device's adhesive and then dissipated in the wiring pattern and attached carrier substrate. Such heat dissipation is desirable to avoid damage to the LED device and to promote proper functionality. A person of ordinary skill in the art facing the many needs created by developments in the technical field of Tanaka and Chitnis would have appreciated the benefits of using a conductive adhesive such as Au-Si or Au-Sn, as described in Chitnis, with Tanaka's LED device such as e.g., ensuring electrical connection between the wiring pattern 80 and electrodes 51, 52.

137. Indeed, as I noted above, Chitnis discloses that "[f]or chip scale packages (e.g. flip chips), it would be advantageous to create devices at the wafer level with both electrical contacts on the bottom of the chip," and that "[t]his would require **electrically and thermally conducting bond medium** selectively deposited to avoid electrical shorting." (Ex. 1007, ¶[0011] (emphasis added).) A person of

ordinary skill in the art would have similarly deposited such a bond medium in Tanaka's device selectively on wiring pattern 80. (Ex. 1005, ¶[0072].)

138. Further, such a skilled person in the art would have been skilled and knowledgeable about configuring Tanaka's LED device to include a conductive adhesive such as Au-Si or Au-Sn, while considering any known design, and other related concepts, limitations, benefits, and the like to ensure the resulting combination operated properly and as intended. Thus, a person of ordinary skill in the art would have had a reasonable expectation of success in using such a thermally conductive adhesive in an LED device like that disclosed by Tanaka.

139. Therefore, it is my opinion that the combination of Tanaka and Chitnis discloses or suggests that the semiconductor LED is affixed to said carrier wafer with an adhesive material which has the property of high thermal conductivity, as claimed.

2. Claim 5

a) The light emitting device of claim 1, wherein said semiconductor LED is affixed to said carrier wafer with an adhesive material which has the property of optical diffusion.²⁶

140. In my opinion, Tanaka in combination with Chitnis discloses or suggests claim 5. For example, as I discussed above with respect to claim 4, Tanaka discloses that its semiconductor LED is affixed to the monocrystal silicon substrate 20 (“carrier wafer”) with an adhesive (“adhesive material”). (*See* my discussions above at Section IX.C.1.)

141. Tanaka discloses bonding its electrodes 51, 52 (part of the first structural unit including the semiconductor LED) to the wiring pattern 80 (part of the second structural unit including monocrystal silicon substrate 20) “via an anisotropic conductive layer or a conductive adhesive” (Ex. 1005, ¶[0072]), but Tanaka is silent about the adhesive having the property of optical diffusion, as claimed. Yet as I discuss below, a person of ordinary skill in the art would have been motivated to use an adhesive having the property of optical diffusion like that described by Chitnis with an LED device like that depicted in figure 7 of Tanaka, to

²⁶ I have reviewed the specification of the ’612 patent and I did not find any disclosure describing the “optical diffusion” feature recited in claim 5. (*See, e.g.*, Ex. 1001, generally.)

bond an LED chip to a wafer, like that bonding of Tanaka's blue-color light-emitting diode chip 70 (including the claimed "semiconductor LED") with the monocrystal silicon substrate 20 ("carrier wafer"). (*See* my discussions above at Section IX.C.1.)

142. For example, as I discussed above in Section IX.C.1, Chitnis, like Tanaka, relates to the fabrication of LED devices (Ex. 1007, ¶[0004]) and further discloses well-known wafer-level bonding techniques during LED device fabrication (*id.*, ¶[0010]). (*See* my discussions above at Section IX.C.1.)

143. While Chitnis discloses using conductive adhesives like Au-Si or Au-Sn as I discussed above with respect to claim 4, Chitnis also discloses using insulating adhesives (e.g., electrically insulating, dielectric bonding media) to bond the LED chip to the submount wafer. (Ex. 1007, ¶¶[0013], [0025], [0047].) Chitnis discloses such insulating adhesives include benzocyclobutene (BCB). (*Id.*, ¶[0047].)

144. A person of ordinary skill in the art would have understood that BCB has the property of optical diffusion as it is used as an optical waveguide. Kane1 (Ex. 1015) and Kane2 (Ex. 1016)²⁷ provide:

In addition, the materials must be easily processed into the desired optical structures. In this paper, we present our work on

²⁷ I refer to Kane1 (Ex. 1015) and Kane2 (Ex. 1016) to demonstrate the knowledge of a person of ordinary skill in the art at the time of the alleged invention of the '612 patent.

using benzocyclobutene as an optical waveguide material. Benzocyclobutene is an advanced organic polymer that is ideally suited as a dielectric layer in high-speed digital circuits. We show that as a waveguide material, single-mode (1300 nm) optical waveguides can be fabricated with losses of 0.81 dB/cm. Detailed processing conditions are discussed.

(Ex. 1015, 1 (excerpted).)

Single-mode optical waveguides at 1300 nm have been fabricated from the organic polymer benzocyclobutene. This material system utilizes a 535 nm photodefinable resin for forming the core of the waveguide, allowing the waveguides to be processed in a fashion similar to a negative photoresist. The processing conditions required for the fabrication of single-mode benzocyclobutene optical waveguides are presented. With the measured losses in the waveguide equal to .81 dB/cm at 1300 nm, this material system is suitable for use in a variety of optical interconnect applications.

(Ex. 1016, 1 (excerpted).) Thus, a person of ordinary skill in the art would have understood that an adhesive such as BCB, as disclosed by Chitnis, would have had the property of optical diffusion, as claimed.

145. As I further discuss below, a person of ordinary skill in the art would have been motivated to use such an optically diffusive adhesive to bond Tanaka's semiconductor LED with the monocrystal silicon substrate 20. Such an

implementation would have been a straightforward combination of well-known technologies using known methods and would have had predictable results.

146. As I have discussed above with respect to claim 4, a person of ordinary skill in the art would have recognized that Tanaka and Chitnis disclose features in a similar technological field. (*See* my discussions above at Section IX.C.1.) Accordingly, a person of ordinary skill in the art would have had reason to consider the teachings of Chitnis when fabricating an LED device as described in Tanaka given Chitnis discloses the details regarding bonding media for affixing various structures in an LED device like the structures to be bonded in Tanaka.

147. A person of ordinary skill in the art would have further recognized that while Tanaka discloses the use of an anisotropic conductive layer or a conductive adhesive between the wiring pattern 80 and electrodes 51, 52 (Ex. 1005, ¶[0072]), a non-conductive adhesive material like BCB could be used in Tanaka's LED device without impeding the functionality of the device. For instance, Chitnis discloses that when an insulating adhesive is used, "vias can be fabricated into the submount wafer and bonding medium after the wafer bonding process (post bond)" and "[t]he vias may subsequently be filled . . . with conductive material to provide electrical contacts to the device." (Ex. 1007, ¶[0025]; *see also id.*, ¶¶[0035], [0048] ("After wafer bonding, one or more vias 52 can be fabricated into the submount 40 and bonding medium layer 50 as needed for a particular device or application.").)

148. In such a scenario, a person of ordinary skill in the art would have understood that the wiring pattern 80 would have served as an alignment guide for forming the holes/vias in Tanaka's LED device, where the vias provide for an electrical connection between the wiring pattern 80 to the electrodes 51, 52. For example, a person of ordinary skill in the art would have understood that this would have been similar to how a bond pad 20 on the LED wafer side of Chitnis' LED device serves as an alignment guide for forming the vias 52. (Ex. 1007, ¶[0048] ("In the embodiment shown, the vias 52 is formed in alignment with the bond pad 20. The vias 52 can be aligned with the bond pad 20 without using difficult and costly alignment processes.").)

149. Moreover, Tanaka discloses using an adhesive to bond electrodes 51, 52 to the wiring pattern 80 in an LED device, but does not disclose the details of bonding techniques. (Ex. 1005, ¶[0072], FIG. 7.) Chitnis, as described above, discloses well-known bonding techniques in LED devices that include bonding LED structures using conductive and insulating adhesives. (Ex. 1007, ¶¶[0011]-[0012].) Thus, a person of ordinary skill in the art would have been motivated to draw from the teachings of Chitnis to implement the bonding in Tanaka's LED device. Based on Chitnis' disclosure, a person of ordinary skill in the art would have known that there were a finite number of identified, predictable solutions for bonding structures during LED device fabrication. (Ex. 1007, ¶¶[0011]-[0013], [0025], [0047].)

Therefore, a person of ordinary skill in the art would have been motivated to try using an insulating adhesive (including BCB) to bond electrodes 51, 52 to wiring pattern 80 in Tanaka, given the limited types of adhesives for bonding structures during LED device fabrication.

150. A person of ordinary skill in the art would have been skilled and knowledgeable about configuring Tanaka's LED device to include an adhesive such as BCB, while considering any known design, and other related concepts, limitations, benefits, and the like to ensure the resulting combination operated properly and as intended. Thus, a person of ordinary skill in the art would have had a reasonable expectation of success in the above modification.

151. Therefore, it is my opinion that the combination of Tanaka and Chitnis discloses or suggests that the semiconductor LED is affixed to said carrier wafer with an adhesive material which has the property of optical diffusion, as claimed.

3. Claim 6

a) The light emitting device of claim 1, wherein said semiconductor LED is affixed to said carrier wafer with an adhesive material which has the property of optical reflection.²⁸

152. In my opinion, Tanaka in combination with Chitnis discloses or suggests claim 6. For example, as I discussed above with respect to claim 4, the Tanaka-Chitnis combination discloses that Tanaka's semiconductor LED is affixed to the monocrystal silicon substrate 20 ("carrier wafer") with a conductive adhesive ("adhesive material") such as Au-Si (gold-silicon) or Au-Sn (gold-tin). (*See my discussions above at Section IX.C.1.*)

153. As confirmed by the '612 patent, gold-tin (Au-Sn) can be used to form a reflective surface and would have the property of optical reflection. (Ex. 1001, 6:3–5.) It is well-known in the art that both gold and tin are metals that have reflecting properties (*E.g.*, Ex. 1001, 6:47–50 (the '612 patent confirms this well-known property that gold has reflecting property: "a reflective material, such as, gold (Au)").) Further, a person of ordinary skill in the art would have understood that an

²⁸ I have reviewed the specification of the '612 patent and I did not find any disclosure describing the "optical reflection" feature recited in claim 6. (*See, e.g.*, Ex. 1001, generally.)

adhesive such as Au-Sn would have the property of optical reflection because the composition contains material with such a reflecting property (e.g., gold.)

154. Therefore, it is my opinion that the combination of Tanaka and Chitnis (as I discussed above with respect to claim 4) discloses or suggests that the semiconductor LED is affixed to said carrier wafer with an adhesive material which has the property of optical reflection, as claimed.

4. Claim 7

a) The light emitting device of claim 1, wherein said semiconductor LED is affixed to said carrier wafer with an adhesive material which has the property of optical transmissivity.²⁹

155. In my opinion, Tanaka in combination with Chitnis discloses or suggests claim 7. For example, as I discussed above with respect to claim 5, the Tanaka-Chitnis combination discloses that Tanaka's semiconductor LED is affixed to the monocrystal silicon substrate 20 ("carrier wafer") with a dielectric adhesive ("adhesive material") such as BCB. (See my discussions above at Section IX.C.2.) Chitnis discloses that such a dielectric adhesive would have the property of optical transmissivity. (Ex. 1007, ¶[0048] ("In the preferred embodiment, the submount

²⁹ I have reviewed the specification of the '612 patent and I did not find any disclosure describing the "optical transmissivity" feature recited in claim 7. (See, e.g., Ex. 1001, generally.)

wafer 42, dielectric layer 44 and **bonding medium layer 50 are substantially transparent** in the infrared (IR) or visible wavelength spectrum.”) (emphasis added); *see also id.*, ¶[0047] (disclosing examples of bond media 50 including BCB).)

156. Therefore, it is my opinion that the combination of Tanaka and Chitnis (as I discussed above with respect to claim 5) discloses or suggests that the semiconductor LED is affixed to said carrier wafer with an adhesive material which has the property of optical transmissivity, as claimed.

D. Tanaka in combination with AAPA Discloses or Suggests the Features of Claims 1, 2, 8, and 9

157. In my opinion, Tanaka and AAPA discloses or suggests all of the claim elements of claims 1, 2, 8, and 9.

158. As I have discussed above, Tanaka discloses or suggests the features of claims 1, 2, 8, and 9, including “a semiconductor LED including doped and intrinsic regions thereof,” as recited in claim element 1.c. In particular, as I discussed above in Section IX.A.1.c, Tanaka would have disclosed or suggested to a person of ordinary skill in the art that activation layer 73 includes an “intrinsic region.” (*See* my discussions above at Section IX.A.1.c.)

159. That said, I have been asked to assume that Tanaka does not necessarily disclose or suggest such an intrinsic region. Under that assumption, it is my opinion that a person of ordinary skill in the art would have been motivated to use an “intrinsic” region in the activation layer 73 of Tanaka’s GaN LED as the inclusion of such an intrinsic layer between p- and n-type layers was a well-known conventional structure, as admitted by the ’612 patent.

160. For example, the ’612 patent explains that “[t]hese LEDs comprise a **P-I-N junction device having an intrinsic (I) layer disposed between a N-type doped layer and a P-type doped layer.** (Ex. 1001, 5:9–11 (emphasis added); *see also id.*, 5:30–31 (“FIG. 1 represents a characteristic horizontal-type Ga LED chip 10. As described, GaN layers 11 are grown upon a substrate 12.”), 5:38–39 (“An

active region makes up the interface of the GaN layers between the p-type and n-type regions.”.)

161. Because such a modification would have constituted applying a known feature (an intrinsic region provided between n- and p-doped layers in a GaN LED) to a particular device (the Tanaka GaN LED) to achieve a predictable result (emission of light by radiative recombination of a hole and an electron in the intrinsic region), thus a person of ordinary skill in the art would have been motivated to use an “intrinsic” region in the activation layer 73 in Tanaka’s GaN LED. For the above reasons, Tanaka in combination with the AAPA, discloses or suggests “a semiconductor LED including doped and intrinsic regions thereof”—i.e., the combined Tanaka-AAPA light-emitting diode chip 70 includes an N-type semiconductor layer 72, a P-type semiconductor layer 74, and an intrinsic activation layer 73.

162. The above modification of Tanaka based on the AAPA does not affect the rest of the analysis in Section IX.A, which applies equally to this ground. Thus, Tanaka in combination with the AAPA discloses or suggests claims 1, 2, 8, and 9 for the reasons discussed in Section IX.A and those discussed above. (*See my discussions above at Section IX.A.*)

E. Tanaka in combination with AAPA and Weeks Discloses or Suggests the Features of Claim 3

163. In my opinion, Tanaka, AAPA, and Weeks disclose or suggest all of the features of claim 3.

164. As I discussed above in Section IX.B, Tanaka in combination with Weeks discloses or suggests all of the claim elements of claim 3. (*See* my discussion above at Section IX.B.) As I also discussed above in Section IX.D, the analysis for claim 1 is modified to include reliance on the AAPA. (*See* my discussion above at Section IX.D.) The reliance on the AAPA does not, however, alter the analysis for claim 3 set forth in Section IX.B. Thus, Tanaka in combination with the AAPA and Weeks discloses or suggests all of the claim elements of claim 3 for reasons similar to those I have discussed above in Section IX.B. (*See* my discussion above at Section IX.B.) For example, the Tanaka-AAPA combination would have been modified based on Weeks for the same reasons discussed above in Section IX.B to arrive at claim 3.

F. Tanaka in combination with AAPA and Chitnis Discloses or Suggests the Features of Claims 4–7

165. In my opinion, Tanaka, AAPA, and Chitnis disclose or suggest all of the claim elements of claims 4–7.

166. As I discussed above in Section IX.C, Tanaka in combination with Chitnis discloses or suggests the features of claims 4–7. (*See* my discussions above at Section IX.C.)

167. As I discussed above in Section IX.D, the analysis for claim 1 is modified to include reliance on the AAPA. (*See* my discussions above at Section IX.D.) That said, the reliance on the AAPA does not alter my analysis for claims 4–7 set forth in Section IX.C above. Thus, it is my opinion that the features of claims 4–7 are also disclosed and suggested by Tanaka in combination with the AAPA and Chitnis for reasons like those as I have discussed above in Section IX.C. (*See* my discussions above at Section IX.C.)

168. For example, the Tanaka-AAPA combination would have been modified based on Chitnis for the same reasons discussed above in Section IX.C to arrive at claims 4–7.

G. Tanaka in combination with Camras Discloses or Suggests the Features of Claims 1, 2, 8, and 9

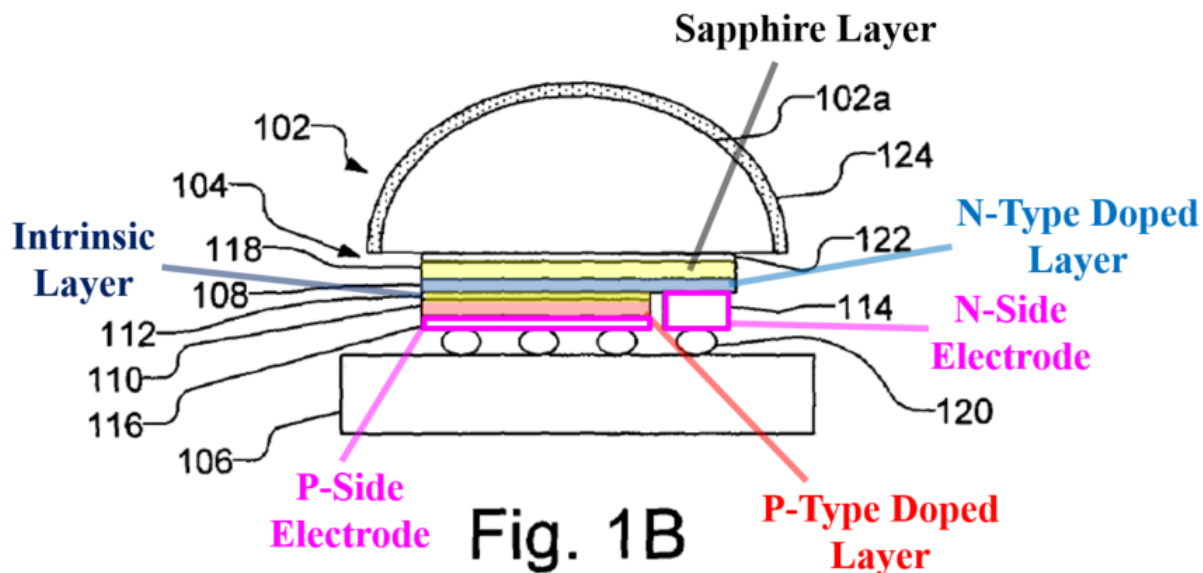
169. In my opinion, Tanaka and Camras disclose or suggest all of the claim elements of claims 1, 2, 8, and 9.

170. As I have discussed above in Section IX.A, Tanaka discloses or suggests the features of claims 1, 2, 8, and 9. (*See* my discussions above at Section IX.A.) And as I have discussed above, Tanaka discloses or suggests “a semiconductor LED including doped and intrinsic regions thereof,” as recited in claim element 1.c. In particular, Tanaka would have disclosed or suggested to a person of ordinary skill in the art that activation layer 73 includes an “intrinsic region.” (*See* my discussions above at Section IX.A.1.c.)

171. Yet, I have been asked to assume that Tanaka does not necessarily disclose or suggest such an intrinsic region between positively and negatively doped regions. Under that assumption, it is my opinion that a person of ordinary skill in the art would have been motivated to use an “intrinsic” region in the activation layer 73 of Tanaka’s GaN LED as the inclusion of such an intrinsic layer between p- and n-type layers in view of Camras.

172. Camras, like Tanaka, is directed to LED structures that include an n-type layer, a p-type layer, and a light emitting active region. (Ex. 1008, 2:27–32, 2:44–61; *see also* my discussions above at Sections VIII.A (Overview of Tanaka), VIII.D (Overview of Camras).) Camras discloses that the light emitting active

region of the LED is between p-type layer 110 and n-type layer 108 and includes intrinsic (undoped) material. (Ex. 1008, 2:44–54 (“**active region 112 includes one or more semiconductor layers that are doped n-type or p-type or are undoped**”) (emphasis added).) Camras also discloses that “[a]ctive region 112 emits light upon application of a suitable voltage across contacts 114 and 116.” (*Id.*, 2:62–63.) Figure 1B of Camras, shown in annotated form below, highlights the intrinsic layer 112 between p-type layer 110 and n-type layer 108.



(*Id.*, FIG. 1B (annotated).)

173. A person of ordinary skill in the art would have looked to Camras for guidance regarding implementing LED devices as disclosed by Tanaka, particularly because Camras and Tanaka are references in the same field that disclose LED devices with many common features. Having looked to Camras, such a person of

ordinary skill in the art would have been motivated to implement the light-emitting activation region 73 in Tanaka so that it includes an intrinsic layer between the p-type and n-type doped regions.

174. The semiconductor LED disclosed by Tanaka is specified to include a p-type layer, an n-type layer, and a light-emitting activation region between those layers. (Ex. 1005, ¶¶[0068], [0070] (“light emitted from the activation layer”).) As I have discussed above, Camras discloses LED structures that include an intrinsic light-emitting layer sandwiched between p-type and n-type regions. (Ex. 1008, 2:44–52.) A person of ordinary skill in the art would have been motivated to use an intrinsic light-emitting layer between the p-type and n-type doped regions, as disclosed by Camras, in conjunction with an LED device as disclosed by Tanaka.

175. Such a person of ordinary skill in the art would have also been motivated to use an intrinsic layer for the light-emitting layer in an LED as disclosed by Tanaka because using an intrinsic layer is one of just a few alternatives disclosed by Camras, where those alternatives include p-type, n-type, and intrinsic semiconductor material. (*Id.*, 2:50–52.) Indeed, as I discussed above in Section IX.A.1.c, the ’612 patent discloses that LEDs with an intrinsic layer between p-type and n-type material were known and in use. (*See* my discussions above at Sections IX.A.1.c and VI; Ex. 1001, 5:9–11, 5:38–39.) Similarly, Sugawara, Atanackovic, and Herner also demonstrate that a person of ordinary skill in the art would have

been aware of the use of intrinsic layers between p- and n-type layers in LEDs. (Ex. 1009, 3:45–51 (“This structure may be realized by forming a pn junction using a p-type semiconductor layer and a n-type semiconductor layer or **by forming a p-i-n junction using an undoped semiconductor layer which acts as an intrinsic semiconductor layer (i-type layer) sandwiched between p-type and n-type semiconductor layers.**”) (excerpted and emphasis added); Ex. 1010, 29:15–23 (“p-doped and n-doped regions separated by an optically **active intrinsic region.**”) (excerpted and emphasis added); Ex. 1011, 3:29–58 (“Examples include p-n diodes and n-p diodes, which have p-type semiconductor material and n-type semiconductor material in contact, and **p-i-n** and n-i-p diodes, **in which intrinsic (undoped) semiconductor material is interposed between p-type semiconductor material and n-type semiconductor material.**”) (excerpted and emphasis added), FIG. 1.)³⁰

176. A person of ordinary skill in the art would have found it straightforward to use an intrinsic layer as disclosed by Camras in an LED device as disclosed by Tanaka because Camras discloses such an intrinsic layer in a device very similar to

³⁰ I refer to Sugawara (Ex. 1009), Atanackovic (Ex. 1010), and Herner (Ex. 1011) to demonstrate the knowledge of a person of ordinary skill in the art at the time of the alleged invention of the '612 patent.

that of Tanaka. Such an implementation would have been a straightforward combination of well-known technologies using known methods and would have had predictable results. Moreover, such a skilled person would have had a reasonable expectation of success because, as demonstrated by Camras, as well as Sugawara, Atanackovic, Herner, and the '612 patent (*see* my discussions above at Sections IX.A.1.c and VI; Ex. 1001, 5:9–11, 5:38–39), LEDs with intrinsic light-emitting layers were well known in the art.

177. For the above reasons, Tanaka in combination with Camras discloses or suggests that the light-emitting diode chip 70 with an N-type semiconductor layer 72, a P-type semiconductor layer 74, and an intrinsic activation layer 73 between the N- and P-type layers constitutes “a semiconductor LED including doped and intrinsic regions thereof.”

178. The above modification of Tanaka based on Camras does not affect the rest of the analysis in Section IX.A, which applies equally to this ground. Thus, Tanaka in combination with Camras discloses or suggests claims 1, 2, 8, and 9 for the reasons discussed in Section IX.A and those discussed above. (*See* my discussion above at Section IX.A.)

H. Tanaka in Combination with Camras and Weeks Discloses or Suggests the Features of Claim 3

179. In my opinion, Tanaka, Camras, and Weeks disclose or suggest all of the claim elements of claim 3.

180. As I discussed above in Section IX.B, Tanaka in combination with Weeks renders disclose or suggest all of the claim elements of claim 3. (*See my discussion above at Section IX.B.*) As I have also discussed above in Section IX.G, the analysis for claim 1 is modified to include reliance on Camras. (*See my discussion above at Section IX.G.*) The reliance on the AAPA does not, however, alter the analysis for claim 3 set forth in Section IX.B. Thus, Tanaka in combination with Camras and Weeks disclose or suggest all of the claim elements of claim 3 for reasons similar to those discussed above in Section IX.B. (*See my discussion above at Section IX.B.*) For example, the Tanaka-Camras combination would have been modified based on Weeks for the same reasons discussed above in Section IX.B to arrive at claim 3.

I. Tanaka in Combination with Camras and Chitnis Discloses or Suggests the Features of Claims 4–7

181. In my opinion, Tanaka, Camras, and Chitnis disclose or suggest all of the claim elements of claims 4–7.

182. As I discussed above in Section IX.C, Tanaka in combination with Chitnis discloses or suggests the features of claim 4–7. (*See my discussion above at*

Section IX.C.) As I have also discussed above in Section IX.G, the analysis for claim 1 is modified to include reliance on Camras. (*See* my discussion above at Section IX.G.) The reliance on Camras does not, however, alter my analysis for claims 4–7 set forth in Section IX.C.

183. Thus, claims 4–7 are disclosed and suggested by Tanaka in combination with Camras and Chitnis for reasons like those discussed above in Section IX.C. (*See* my discussion above at Section IX.C.) For example, the Tanaka-Camras combination would have been modified based on Chitnis for the same reasons discussed above in Section IX.C to arrive at claims 4–7.

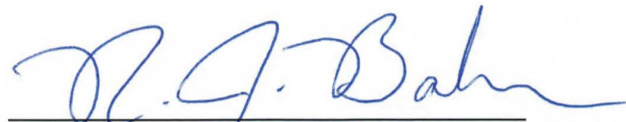
X. CONCLUSION

184. In summary, it is my opinion that all of the features recited in claims 1–9 of the '612 patent are disclosed or suggested by the prior art.

185. I declare that all statements made herein of my knowledge are true, and that all statements made on information and belief are believed to be true, and that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code.

Dated: September 20, 2021

By: _____



R. Jacob Baker, Ph.D., P.E.