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UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

STMICROELECTRONICS, INC.
Petitioner

v.

THE TRUSTEES OF PURDUE UNIVERSITY
Patent Owner

IPR2022-00252
U.S. Patent No. 7,498,633

DECLARATION OF VIVEK SUBRAMANIAN, PH.D.
U.S. PATENT NO. 7,498,633
CHALLENGING CLAIMS 9–11

TABLE OF CONTENTS

I, Vivek Subramanian, declare as follows:

I. INTRODUCTION

1. My name is Vivek Subramanian. I am a Professor of Microtechnology at the École polytechnique fédérale de Lausanne (EPFL) (also known as the Swiss Federal Institute of Technology in Lausanne) in Switzerland. Until recently, I was also a professor of Electrical Engineering and Computer Sciences at the University of California, Berkeley. As of July 1, 2020, I have become an adjunct professor at UC Berkeley upon completion of my move to EPFL.

2. I have been retained as an expert in this proceeding by counsel for STMicroelectronics, Inc. ("ST"). I have been asked for my expert conclusions regarding the validity of claims 9–11 of U.S. Patent No. 7,498,633 (the "'633 patent") (EX1001). For the reasons set forth below, it is my conclusion that claims 9–11 of the '633 patent are invalid.

II. QUALIFICATIONS AND PROFESSIONAL EXPERIENCE

3. My qualifications are stated more fully in my curriculum vitae, which is attached as Exhibit A. Below is a summary of my education, work experience, and other qualifications.

4. I received a bachelor's degree *summa cum laude* in electrical engineering from Louisiana State University in 1994. I received M.S. and Ph.D.

degrees in electrical engineering, in 1996 and 1998, respectively, from Stanford University.

5. Throughout the course of my education, including my B.S., M.S., and Ph.D. degrees, I was involved in the design, fabrication, characterization, and modeling of semiconductor devices, including specifically devices designed for high voltage and high power applications. For example, I have designed high voltage transistors for operation of Flash memory devices using silicon, which have gone into commercial products, and have designed and fabricated high voltage wide bandgap devices for use in MEMS actuators based on zinc oxide.

6. After completing my Ph.D., I held multiple appointments simultaneously between 1998 and 2000. I served as a Consulting Assistant Professor in the Electrical Engineering Department of Stanford University. I also served as a Visiting Research Engineer in the Department of Electrical Engineering and Computer Sciences at the University of California, Berkeley, where my research focused on 25nm metal oxide semiconductor field effect transistor (MOSFET) design and fabrication. I worked on technologies for high-performance transistor processes, and I published several papers as a direct outcome of this technology development.

7. In 2000, I became an assistant professor at the University of California, Berkeley in the Department of Electrical Engineering & Computer Sciences. In 2005, I was promoted to the position of tenured Associate Professor, and in 2011, I was promoted to full Professor. In 2018, I became a full Professor of Microtechnology at EPFL in Switzerland, where I lead the Laboratory for Advanced Fabrication Technologies (LAFT). The lab focuses on the development and application of advanced additive fabrication techniques for realizing precision microelectronic and electromechanical systems. As of 2020, I have completed my move to EPFL and have therefore converted to an adjunct appointment at Berkeley.

8. My research has maintained a large effort on semiconductor devices, including working on various types of high voltage and high power devices, as mentioned above.

9. Starting in 2004, I was a founding technical advisor for Kovio. I led the development of Kovio's first commercial RFID tag product, including the design of both the tag and the reader, and including the development of the underlying proprietary transistor technology. This included the development of the materials, fabrication processes, and device design. My involvement with Kovio ended with Kovio's acquisition by thin film electronics, but Kovio continues to focus on this area.

10. I co-founded Locix Inc. in 2014. Locix develops and sells a range of wireless-enabled products, including proprietary Wi-Fi-based RF localization systems and sub-GHz low-power wireless sensor networks. As CTO of Locix, I led the development of the entire Locix RF product portfolio. I continue to be involved with Locix on a regular basis.

11. I have authored or co-authored over 200 technical papers in international journals and conferences and have been named an inventor or co-inventor on more than 50 patents, many of which cover aspects of semiconductor device design and fabrication.

12. I am being compensated for my time at my ordinary hourly rate of $650. My compensation is not dependent on the outcome of these proceedings or the content of my opinions. To the best of my knowledge, I have no financial interest in either party or in the outcome of this proceeding.

III. MATERIALS CONSIDERED

13. In preparing this declaration, I have reviewed the claims, specification, and file history of the ’633 patent. I understand that the ’633 patent issued from U.S. Patent Application No. 11/338,007, which was filed on January 23, 2006, claiming priority to U.S. Provisional Application No. 60/646,152, filed on January 21, 2005.

14. I have reviewed and understand the references and exhibits cited in this Declaration, including the following:

Exhibit	Description
1001	U.S. Patent No. 7,498,633
1003	U.S. Patent Application Publication No. 2004/0119076 ("*Ryu*")
1004	U.S. Patent No. 6,413,822 ("*Williams*")
1005	U.S. Patent No. 5,233,215 ("*Baliga*")
1006	U.S. Patent No. 6,316,791 ("*Schörner*")
1007	U.S. Patent Application No. 2006/0267092 ("*Jun*")
1008	'633 Patent File History, 4/4/2007 Non-Final Rejection
1009	'633 Patent File History, 8/6/2007 Response to Office Action
1010	'633 Patent File History, 10/12/2007 Final Rejection
1011	'633 Patent File History, 3/12/2008 Response to Office Action
1012	'633 Patent File History, 6/25/2008 Non-Final Rejection
1013	'633 Patent File History, 8/22/2008 Response to Office Action
1014	'633 Patent File History, 12/17/2008 Notice of Allowance
1015	U.S. Patent No. 5,317,184 ("*Rexer*")
1016	"Modern Power Devices," B. Jayant Baliga, 1987 (relevant sections)
1017	A. G. Jost et al., "Implementation of a VLSI Layout Tool on Personal Computers," ACM, 1990
1018	E. S. Kuh et al., "Recent Advances in VLSI Layout," Proceedings of the IEEE, vol 78, no. 2, February 1990
1019	"Power MOSFETs – Theory and Applications," Duncan A. Grant and John Gowar, 1989 ("*Grant*") (relevant sections)
1020	J. A. Cooper, Jr. et al., "SiC Power-Switching Devices—The Second Electronics Revolution?," Proceedings of the IEEE, vol. 90, no. 6, June 2002
1021	U.S. Patent No. 5,510,281 ("*Ghezzo*")

1022	J. A. Cooper, Jr. et al., "Status and Prospects for SiC Power MOSFETs," IEEE Transactions on Electron Devices, vol. 49, no. 4, April 2002
1023	S-H Ryu et al., "10 A, 2.4 kV Power DiMOSFETs in 4H-SiC," IEEE Electron Device Letters, vol. 23, no. 6, June 2002
1024	S-H Ryu et al., "2 kV 4H-SiC DMOSFETs for Low Loss, High Frequency Switching Applications," International Journal of High Speed Electronics and Systems, vol. 14, no. 3, 2004
1025	Plaintiff's Disclosure of Earliest Date of Invention

IV. LEGAL PRINCIPLES

15. I am not an attorney. For the purposes of this declaration, I have been informed by ST's counsel about certain aspects of the law that are relevant to my opinions, as stated in the following paragraphs. I have applied these legal principles in arriving at my conclusions expressed in this declaration.

16. I have been informed and understand that a patent claim is invalid if it would have been obvious to a person of ordinary skill in the art (POSITA) at the time of the alleged invention. This means that, even if all of the requirements of a claim are not found in a single prior art reference, the claim is not patentable if the differences between the subject matter in the prior art and the subject matter in the claim would have been obvious to a POSITA at the time of the alleged invention.

17. I have been informed and understand that a determination of whether a claim was obvious should be based upon several factors, including, among others: (1) the level of ordinary skill in the art at the time of the alleged invention; (2) the

scope and content of the prior art; (3) the differences, if any, that existed between the claimed invention and the prior art; and (4) any objective considerations of nonobviousness.

18. I have been informed and understand that when determining any differences between the invention covered by the patent claims and the prior art, one should not look at the individual differences between the patent claims and the prior art in isolation, but rather consider the claimed invention as a whole and determine whether or not it would have been obvious in light of all of the prior art.

19. I have been informed and understand that a single reference can render a patent claim obvious if any differences between that reference and the claims would have been obvious to a POSITA. Alternatively, the teachings of two or more references may be combined in the same way as disclosed in the claims. I have been informed and understand that when deciding whether to combine the various items described in the prior art, the relevant question is whether the prior art combination would have been obvious to a person with ordinary skill in the art at the time of the invention. I have been further informed that it can be important to identify a teaching, suggestion, or motivation, in either the prior art or the knowledge of persons skilled in the art, that would have prompted a person of ordinary skill in the

relevant field to combine the elements in the prior art in the way the claimed invention does.

20. In determining whether a combination based on either a single reference or multiple references would have been obvious, it is appropriate to consider, among other factors:

- whether the teachings of the prior art references disclose known concepts combined in familiar ways, and when combined, would yield predictable results;
- whether a POSITA would implement a predictable variation, and would see the benefit of doing so;
- whether the claimed elements represent one of a limited number of known design choices, and would have a reasonable expectation of success by a POSITA;
- whether a POSITA would have recognized a reason to combine known elements in the manner described in the claim;
- whether there is some teaching or suggestion in the prior art to make the modification or combination of elements claimed in the patent; and
- whether the innovation applies a known technique that had been used to improve a similar device or method in a similar way.

21. I have been informed and understand that one of ordinary skill in the art has ordinary creativity, and is not an automaton. I have been informed and understand that in considering obviousness, it is important not to determine obviousness using the benefit of hindsight derived from the patent being considered. I have been informed and understand that a patent composed of several elements is not proved obvious merely by demonstrating that each of its elements was independently known in the prior art.

22. I have been informed and understand that to show a motivation to combine, one is not required to show how the references would be physically combined to render a claim obvious. The analysis is not focused on whether the features of one reference can be physically incorporated into the structure of another reference, but rather whether a person of ordinary skill in the art would have been motivated to combine the teachings of the references to achieve the claimed invention. For example, a person of ordinary skill in the art would understand how predictable variations of known concepts could be combined and would recognize that were where multiple tools were available in a toolbox, any could be chosen.

V. LEVEL OF ORDINARY SKILL IN THE ART

23. I have considered the ’633 patent from the perspective of a POSITA at the time of the alleged invention. A POSITA for the ’633 patent would have had the

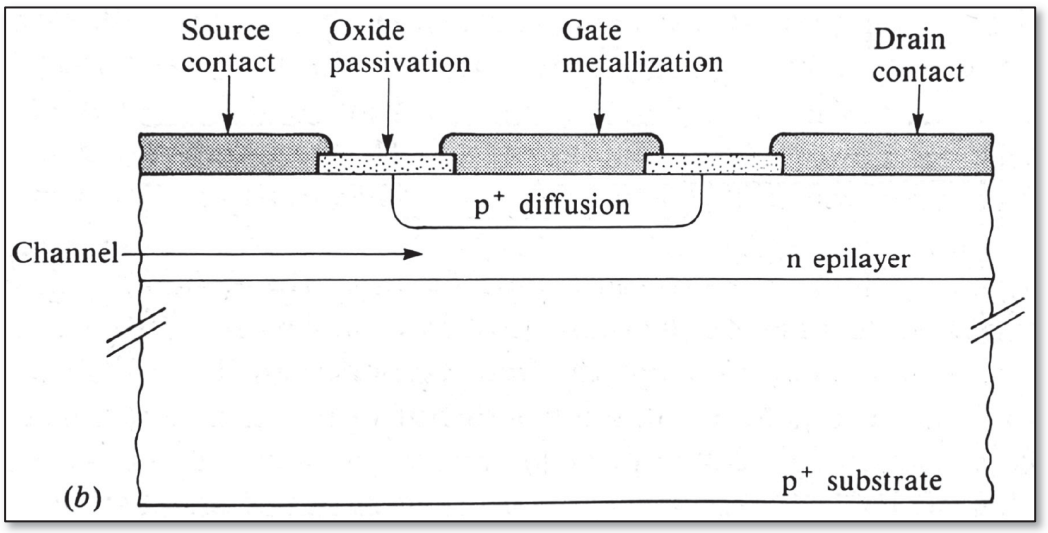
equivalent of a Bachelor's degree in electrical engineering or a related subject and two or more years of experience in the field of semiconductor devices. Less work experience may be compensated by a higher level of education, such as a Master's Degree, and vice versa. At the time of the claimed invention, I would have qualified as a POSITA under this standard.

VI. TECHNICAL BACKGROUND

A. Field-Effect Transistor ("FET")

24. A field-effect transistor ("FET") is a type of transistor that uses an electric field to control the flow of current in a semiconductor. *See* "Power MOSFETs – Theory and Applications," Duncan A. Grant and John Gowar, 1989 ("*Grant*") (EX1019) at 1 ("The metal-oxide-semiconductor field-effect transistor (MOSFET) is the most commonly used active device in the very large-scale integration of digital integrated circuits …. The conductance of a piece of semiconductor depends on the number of free carriers it contains and on their mobility. The effective number of free carriers can be modified by establishing a static electric field in the semiconductor in the direction transverse to the current flow."); EX1015, 1:13–18 ("Semiconductor devices, and more particularly metal oxide semiconductor (MOS) devices used in power applications, are operated when an electric potential is applied across a drain and a source and a voltage is applied to a gate to control current flow between the drain and the source."). A FET generally

includes a source, a drain, and a gate, as *Grant* illustrates in a cross section of a junction field-effect transistor (JFET) in Figure 1.1, reproduced below. *See, e.g.*, *id.* at 2, Figure 1.1.



EX1019, Figure 1.1

25. The flow of current is controlled by applying a voltage (*i.e.*, creating an electric field) to the gate, which in turn alters the conductivity of the channel formed between the drain and the source. *Id.* at 3 ("it is normally ON or in the freely conducting state, and it can be turned OFF by a voltage of suitable polarity applied to the gate. This reverse-biases the gate-channel pn junction and so expands the depletion layer. As a result the effective cross-sectional area of the conducting channel is reduced and its resistance is increased.").

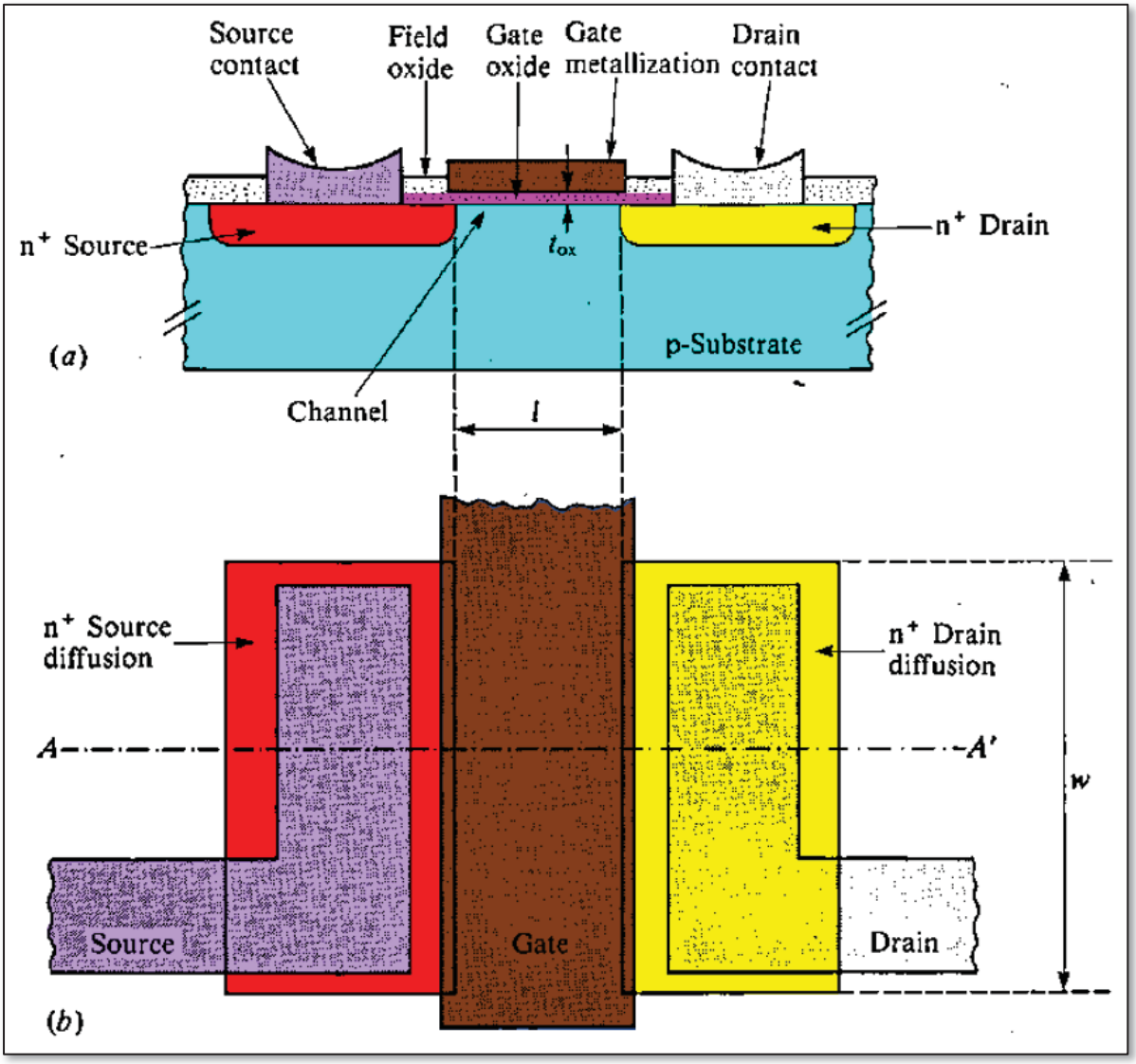
26. *Grant* notes that "[t]he successful manufacture of the JFET depended on the introduction of *planar* silicon technology in 1960" that involves a "combination of processes." EX1019 at 3. *Grant* goes on to explain that these processes include:

> 1. Epitaxial crystal growth from the vapor phase.
>
> 2. The formation of thermally grown silicon dioxide layers for surface passivation, for masking, and as an insulating layer over which metal interconnections may be run.
>
> 3. The photolithographic etching of "windows" in the oxide layer.
>
> 4. The introduction of controlled levels of impurity into selected regions of the silicon through these windows in the oxide, either by diffusion from the vapor phase or by ion implantation.
>
> 5. The deposition by evaporation or sputtering of a thin conducting film (usually Al) and the etching of this film to form a pattern of interconnections on the surface.

Id. *Grant* illustrates the above processes in Figure 1.2. *Id.* at 4. The introduction of impurities is often referred to as "doping."

27. "Further technological refinements in the early 1960s enabled a different type of field-effect transistor to be made. This was the metal-oxide-

semiconductor field-effect transistor (MOSFET)." EX1019 at 5. *Grant* points out that the difference between a JFET and a MOSFET is "[t]he controlling gate electrode is now separated from the semiconductor by a thin insulating layer of gate oxide, as shown in Figure 1.3." *Id.*; *see also* U.S. Patent No. 5,233,215 ("*Baliga*") (EX1005), 1:45–50. ("These device types are commonly referred to as Metal Oxide Semiconductor Field Effect Transistors (MOSFET) because they include a conducting gate electrode, typically metal, that is separated from a semiconductor surface by an intervening insulator, typically silicon dioxide."). In Figure 1.3 (reproduced below), *Grant* illustrates a cross section and a plan view of a MOSFET. EX1009 at 5. When the MOSFET is turned on, current can flow between the source and drain through the channel, shown in the figure and formed in the p-type substrate. The n+ source region, the p-type substrate, and the n+ drain region essentially forms an npn transistor. The source region is annotated in red, the drain region in yellow, the p-type substrate in cyan, the gate in brown, the gate oxide in magenta, and the source contact in lavender. The source contact is often referred to as "source metallization," "source metal," or "source electrode." *See, e.g.*, EX1019, Figure 1.13 (illustrating the source metallization); EX1015, Figure 1, 1:38 ("source metal"); EX1005, 2:64 ("source electrode").



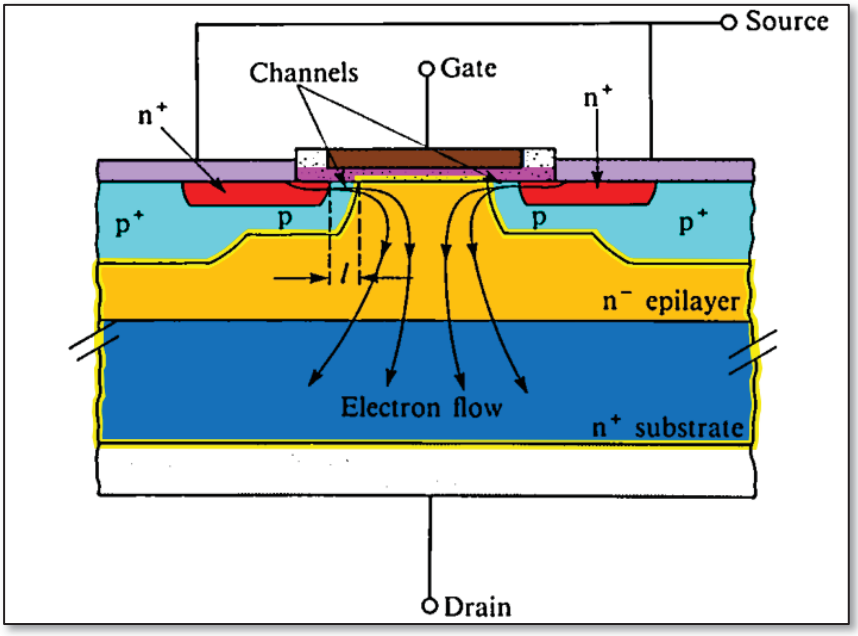
EX1019, Figure 1.3 (annotated)

B. Power MOSFET

28. While useful in a variety of electronics applications, the MOSFET also became "important in devices designed for power applications." EX1019 at 5; *see also* EX1005, 2:14–16 ("In view of the above desirable characteristics, many variations of power MOSFETs have been designed for power devices."). *Grant*

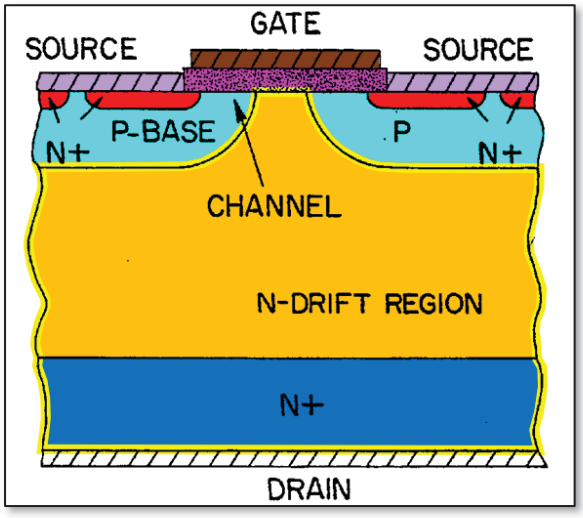
notes that "the decision as to what constitutes a power device is quite arbitrary" and the term is applied to "any device capable of switching at least 1 A" (*i.e.*, turning on and off a current of 1 ampere flowing from the drain to the source). EX1019 at 5–6.

29. *Grant* further notes that "the planar structure of Figure 1.3 is unsatisfactory if it is simply scaled up for higher powers." EX1019 at 8. "[T]he drain-source spacing has to be increased in order to obtain a high voltage blocking capability." *Id.* One solution well known in the art was to change the lateral structure as illustrated in *Grant*'s Figure 1.3 to a vertical structure that uses the substrate material to form the drain region such that "the current flows 'vertically' through the silicon from drain to source." *Id.* This change led to the ***vertical double-diffused MOSFET***, which *Grant* illustrates in Figure 1.11, reproduced below. *Id.* at 13–14.



EX1019, Figure 1.11 (annotated)

30. *Baliga* also illustrates a vertical double-diffused MOSFET in Figure 1, which is reproduced below. EX1005, 6:12–13 ("FIG. 1 is a cross-sectional view of a known DMOSFET device").



EX1005, FIG. 1 (annotated)

31. The term "double-diffused" derives from a manufacturing technique commonly used to form the n+ source regions within the p-type body region: "[t]he p-type 'body' region . . . and the n+ source contact regions are diffused successively through the same window etched in the oxide layer." EX1019 at 14; *see also* EX1005, 2:35–38 ("The p-base region and the n+ source region are typically diffused through a common window defined by the edge of the polysilicon gate."). The p-type body region is often referred to as "p-type wells" or "p-base regions." *See, e.g.*, EX1019 at 146 ("p-type wells"); EX1005, 2:35 ("p-base region"), Figure 1 (illustrating p-base regions).

32. In each of the above *Grant*'s Figure 1.11 and *Baliga*'s Figure 1, the source regions are annotated in red, the p-type body regions in cyan, the gate in brown, the gate oxide in magenta, and the source contacts in lavender. The drain region (outlined in yellow) comprises the substrate (annotated in blue) and the epilayer (annotated in orange). Electrons flow from the source to the drain through the channels formed in the p-type wells, the epilayer, and the substrate. The epilayer is often referred to as the drift region. *Grant* notes that "[t]he drain drift region is particularly critical to the design of a power MOSFET" because "[i]ts principal function is to block and support the full forward voltage held off by the transistor in

its turned-OFF state" and "it has also to carry the full forward current in the ON state." *Id.* at 74.

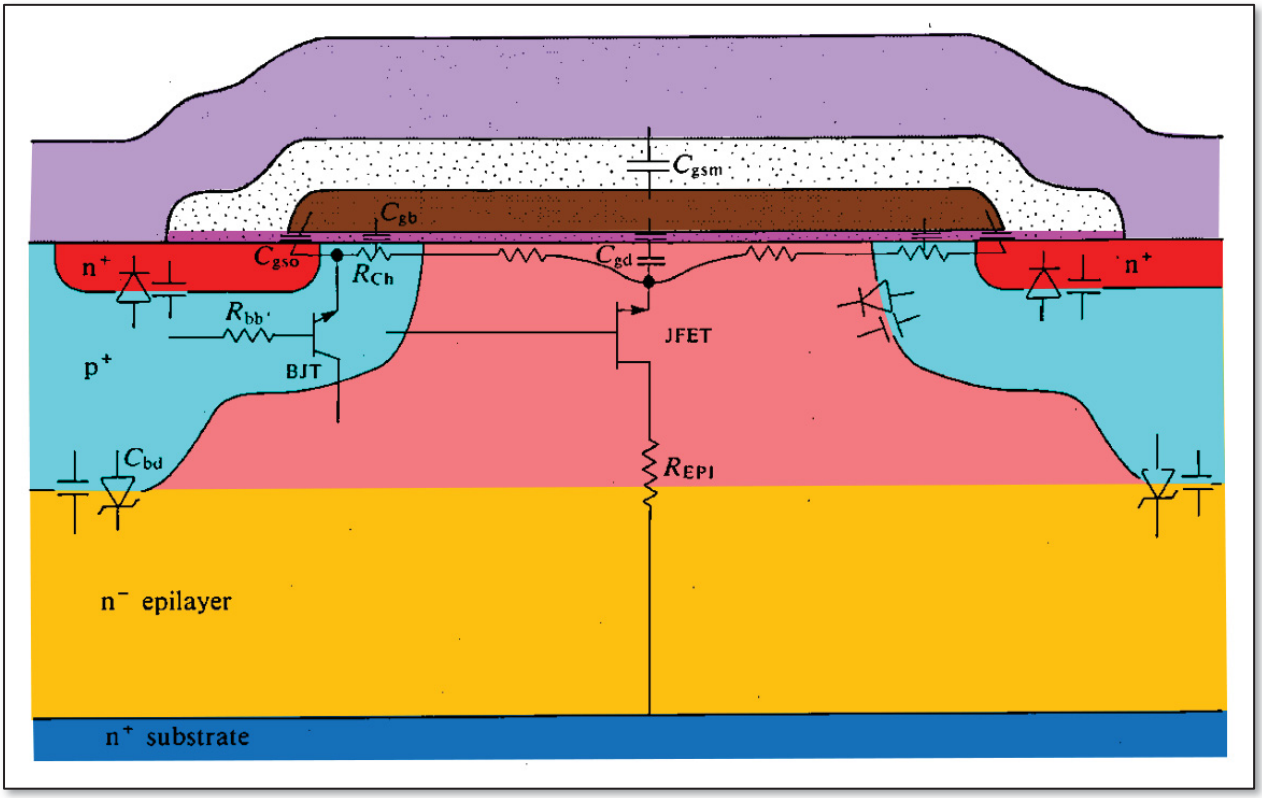
C. On-Resistance

33. According to *Grant*, "[t]he minimization of the ON-state voltage drop is an important consideration in power devices." EX1019 at 18. This ON-state voltage drop depends on the "ON-state drain-source resistance, $R_{DS(on)}$"—also known simply as the "on-resistance." *Id.* U.S. Patent No. 6,413,822 to Williams and Grabowski ("*Williams*"), discussed further herein, explains that the on-resistance of a MOSFET is determined by the "sum of its resistive components," which includes "its substrate resistance (R_{sub})," "its epitaxial drain resistance (R_{epi})," "its source contact resistance (R_c)," *etc.* *See id.*, 1:33–37. *Williams* notes that "[t]he primary design goal for a power MOSFET used as a switch is to achieve the lowest on-resistance by simultaneously minimizing each of its resistive constituents." EX1004, 1:50–52.

34. Indeed, for example, *Grant* recognizes the contribution of the epilayer to the on-resistance and states that "[i]t is thus most important that its contribution R_{EPI} to the total ON-state resistance $R_{DS(on)}$ be kept as small as possible." EX1019 at 74. *Grant* explains that "the epilayer should be no thicker than it has to be in order

to support the maximum blocking voltage" and that "[t]his minimizes dissipation and maximizes the current rating of the device." *Id.* at 74–75.

35. *Grant* also describes that the vertical MOSFET structure includes so-called parasitic elements as a result of the junctions between the n-type and p-type regions. In particular, *Grant* describes the existence of a parasitic "n-channel junction field-effect transistor (JFET) that forms in the epilayer, in between the channel diffusions." EX1019 at 81. *Grant* illustrates this parasitic JFET in Figure 3.15, reproduced below. *Id.* at 80, Figure 3.15. *Grant* explains that "[t]he JFET action occurs in the region between the p diffusions." *Id*. at 81. Accordingly, this region is typically referred to as the "JFET region" of the MOSFET. *See, e.g.*, EX1003, ¶44. The JFET region—in the epilayer and between p diffusions/wells—is annotated in pink in *Grant*'s Figure 3.15 below. *Grant* also points out that "[i]ncreasing the donor doping concentration in the drain throats [(*i.e.*, the JFET regions)] . . . has two beneficial effects"—"the cell size can be reduced and . . . lower $R_{DS(on)}$ can be realized." EX1019 at 83–84.



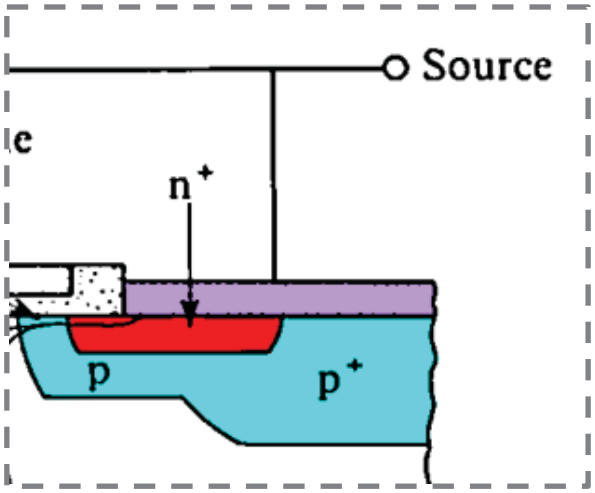
EX1019, Figure 3.15 (annotated)

36. Also to reduce the on-resistance, *Williams* discloses topological configurations (*i.e.*, the physical shape, size, and arrangement of the structures) that minimize the source contact resistance, as will be discussed in more detail below. *See* EX1004, 10:17–18; 16:28–35.

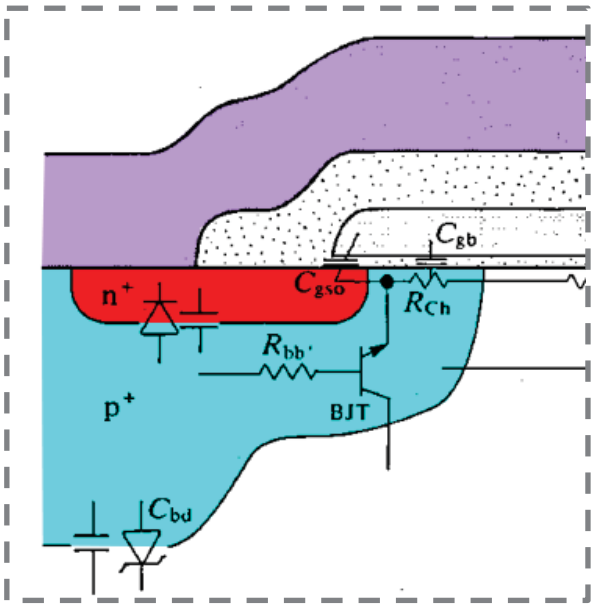
D. Unwanted Activation of Parasitic Components—Latch Up

37. *Grant* notes, and illustrates in Figure 3.15 (reproduced above), an "npn bipolar junction transistor (BJT) formed between the source, the body, and the drain." EX1019 at 81. The parasitic BJT "may be activated, and this can seriously

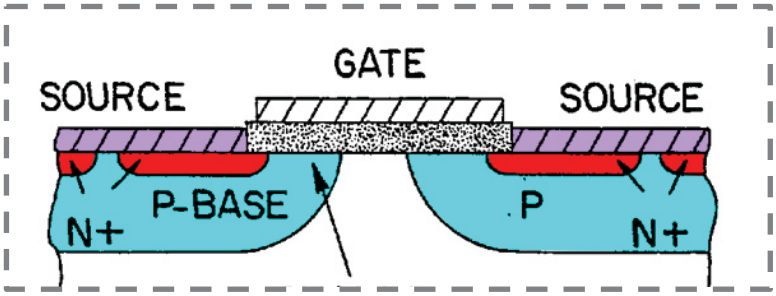
degrade the overall performance of the MOSFET." *See* EX1019 at 81; *see also* EX1007, ¶¶ 6–7 ("[A] parasitical bipolar transistor will exist in the high power MOSFET . . . When the parasitical bipolar transistor turns on, a latch phenomenon will arise to increase the possibility of device breakdown."). This phenomenon is typically known as "latch up." To prevent latch up, "[t]his parasitic bipolar transistor must be kept inactive during all modes of operation of the power MOSFET." EX1016 at 266. "To accomplish this, the P-base region is short-circuited to the N^+-emitter region by the source metallization . . ." *Id.*; *see also* EX1004, 6:8–14 ("The source-to-body short prevents conduction and snapback breakdown of the parasitic NPN bipolar transistor . . . by maintaining the emitter and base at the same potential. Shorting the emitter and base terminals ideally prevents forward-biasing of the emitter-base junction and avoids consequent minority carrier (electron) injection into the MOSFET's body (i.e. base)."). Indeed, as depicted by the annotated excerpts below, it was well known to connect the p-type body or p-base region (*i.e.*, the base of the parasitic BJT; annotated in cyan) to the source region (*i.e.*, the emitter of the parasitic BJT; annotated in red) by an overlying and contacting source metallization (annotated in lavender) to keep the parasitic BJT inactive. *See, e.g.*, EX1019, Figures 1.11 and 3.15; EX1005, Figure 1.



EX1019, Figure 1.11
(excerpted and annotated)

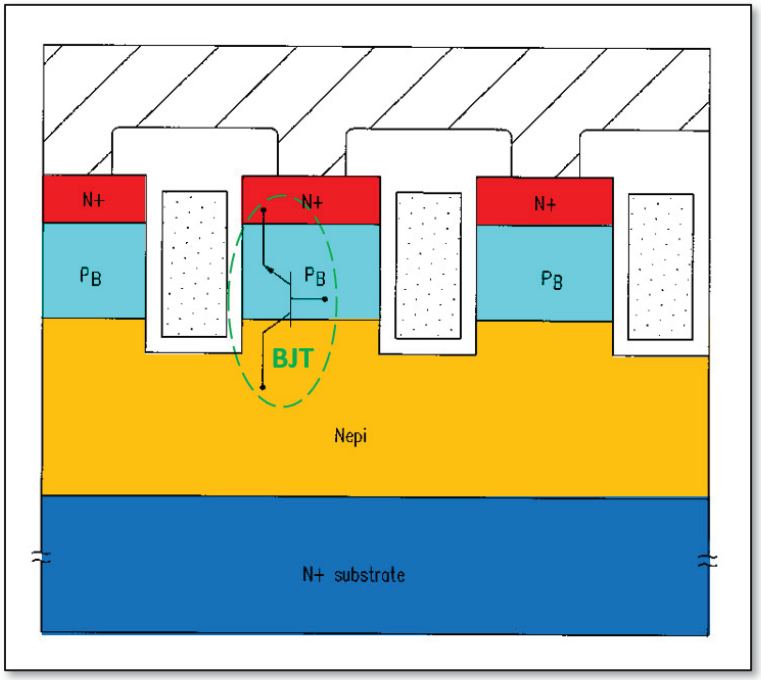


EX1019, Figure 3.15
(excerpted and annotated)



EX1005, FIG. 1(excerpted and annotated)

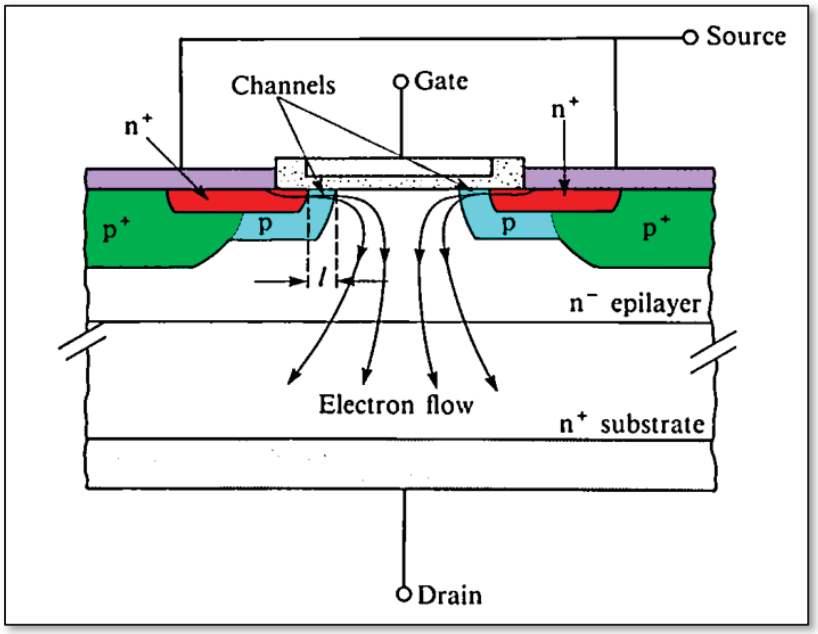
38. Such a parasitic BJT exists in any power MOSFET, regardless of the gate configuration, because the source, the body, and the drain form an npn configuration, *i.e.*, two regions of n-type semiconductor material separated by p-type material. For instance, *Williams* describes and illustrates in Figure 7A (reproduced below) a "parasitic NPN bipolar transistor" in a trench-gate vertical MOSFET. EX1004, 6:9.



EX1004, FIG. 7A (annotated)

39. *Grant* further explains that current flowing through the resistance $R_{bb'}$ (*see Grant*'s Figure 3.15, reproduced above) at the base of the parasitic BJT causes an ohmic voltage drop (as a result of resistance in the connection) which, if it exceeds about 0.6 V, "will initiate transistor action in the parasitic BJT." EX1019 at 87. To reduce resistance and minimize voltage drop, *Grant* notes that "[t]he use of the p+ diffusion to connect the body region back to the source contact can be seen to be an important part of the VDMOS FET design." *Id.* at 90; *see also id.*, Figures 1.11 and 1.13(a) (illustrating p+ diffusion in p-type body regions). "It reduces $R_{bb'}$ . . ." *Id.* Thus, in addition to connecting the body region to the source region, a MOSFET may be ruggedized against inadvertent activation of the parasitic BJT by having p+

diffusion in the p-type body region to reduce the resistance $R_{bb'}$ and keep the ohmic voltage drop low. *See also* EX1004, 16:32–34 ("maximize the P+ contact to the body region (to suppress parasitic bipolar turn-on, prevent snapback and ruggedize the device)"); EX1021, 5:28–30 ("Although an electrical connection can be made directly to the p type base region, the p+ base contact region provides an improved connection."). The p+ diffusions of *Grant*'s Figure 1.11 below are annotated in green. *Grant* cautions, however, that "any mask misalignment that causes the p+ diffusion to be displaced . . . increases $R_{bb'}$ locally." EX1019 at 90.



EX1019, Figure 1.11 (annotated)

E. Silicon Carbide (SiC)

40. Historically, power MOSFETs were fabricated using monocrystalline silicon (*i.e.*, a single-crystal silicon). But by the early 1990s, an alternative material—silicon carbide—was also known to be particularly well suited for use in such devices. EX1005, 4:22–27 ("Almost all power MOSFETs being marketed today are fabricated in monocrystalline silicon . . . [,] as is known to those skilled in the art, crystalline ***silicon carbide is particularly well suited*** for use in semiconductor devices, and in particular, for power semiconductor devices.").[1] Silicon carbide was known to have many benefits, including "a wide bandgap, a high melting point, a low dielectric constant, a high breakdown field strength, a high thermal conductivity and a high saturated electron drift velocity compared to silicon." *Id.*, 4:27–31. "These characteristics would allow silicon carbide power devices to operate at higher temperatures, higher power levels and with lower specific on resistance than conventional silicon based power devices." *Id.*, 4:31–34; *see also* U.S. Patent No. 5,510,281 ("*Ghezzo*") (EX1021), 1:52–56 ("Because SiC has a higher critical electric field than silicon, the specific on-resistance of a SiC

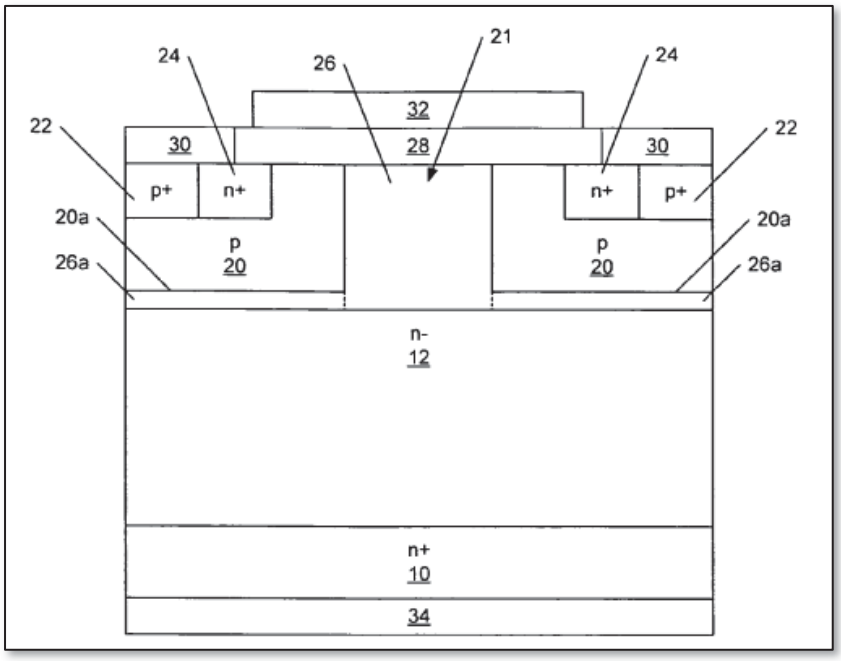
[1] Unless otherwise noted, all emphasis has been added.

DMOS is expected to be significantly lower than that of a silicon DMOS with the same high voltage rating.").

41. Moreover, *Baliga* teaches that "power MOSFET such as the above described DMOSFET . . . can be readily translated into silicon carbide using known manufacturing techniques." EX1005, 4:35–38. *Baliga* goes on to explain how to translate the DMOSFET into a silicon carbide device using known manufacturing techniques, *e.g.*, by using higher temperature, and longer, diffusions to compensate for the lower diffusion coefficient in silicon carbide. *Id.*, 4:38–43. *Ghezzo*, which was filed in 1995, further teaches that "[a] method of implementing vertical power SiC transistor is to replace the conventional double-diffusion with an edge-shifted ***double ion implantation*** sequence to overcome the problem of very small dopant diffusivity in SiC" and that "[t]he channel is formed by successive ion implantation of an acceptor atom (such as boron or aluminum) and a donor atom (such as nitrogen or phosphorous) to form the base and source regions, respectively." EX1021, 1:56–63. Accordingly, SiC power MOSFETs are sometimes referred to as "double-implanted" MOSFETs to distinguish the fabrication technique used to make them from "double-diffused" used in silicon.

F. Visualizing Three-Dimensional Semiconductor Structures

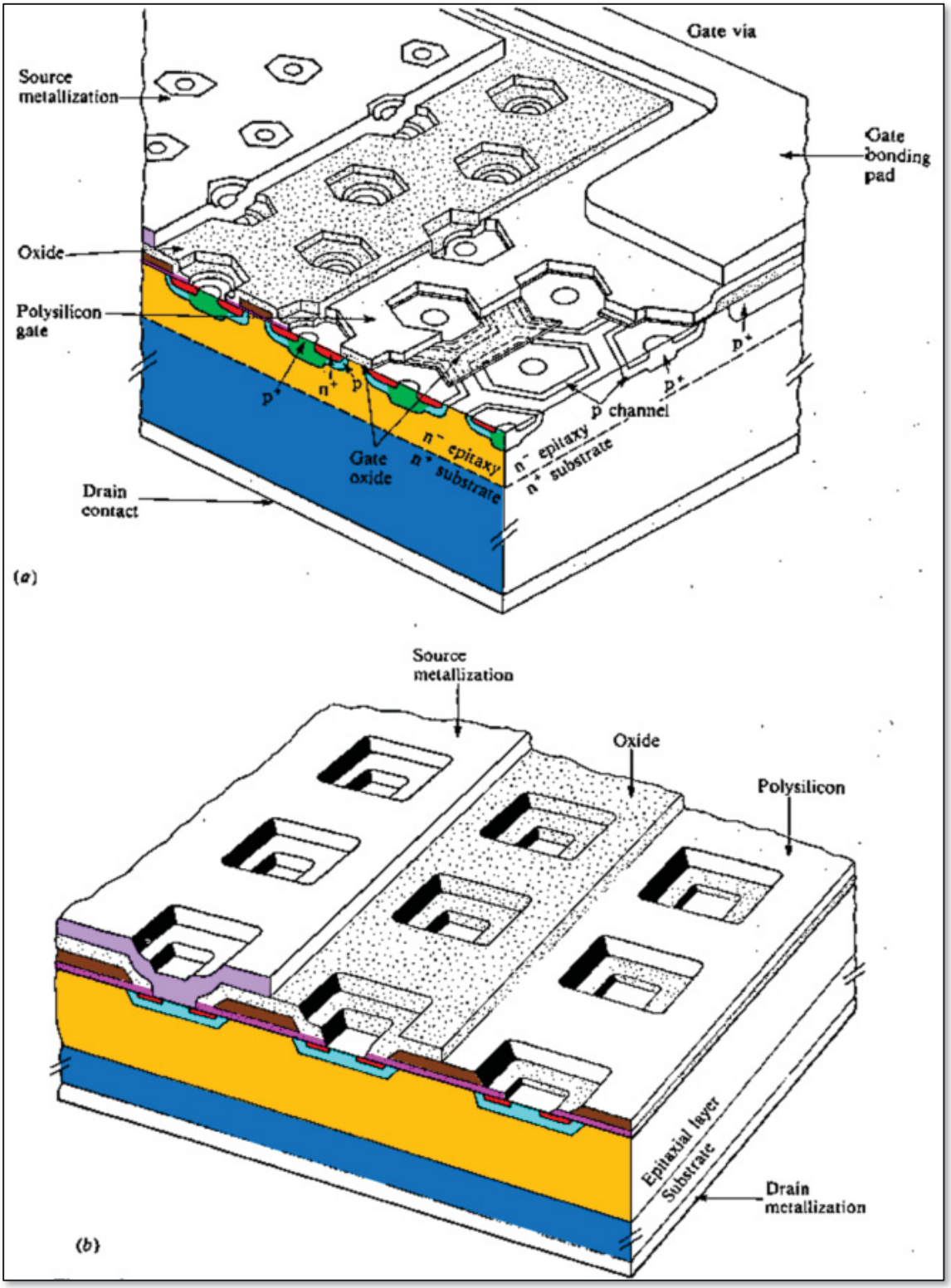
42. Prior art references conventionally use a two-dimensional cross-sectional view to depict a unit cell of a power MOSFET (*e.g.*, as in *Grant*'s Figure 1.11 and *Baliga*'s Figure 1, both reproduced above). U.S. Patent Application Publication No. 2004/0119076 to Ryu ("*Ryu*") (EX1003), discussed in further detail herein, shows a similar example of a cross-sectional view of a unit cell of a MOSFET in Figure 2A, reproduced below. *See* EX1003, ¶51.



EX1003, FIG. 2A

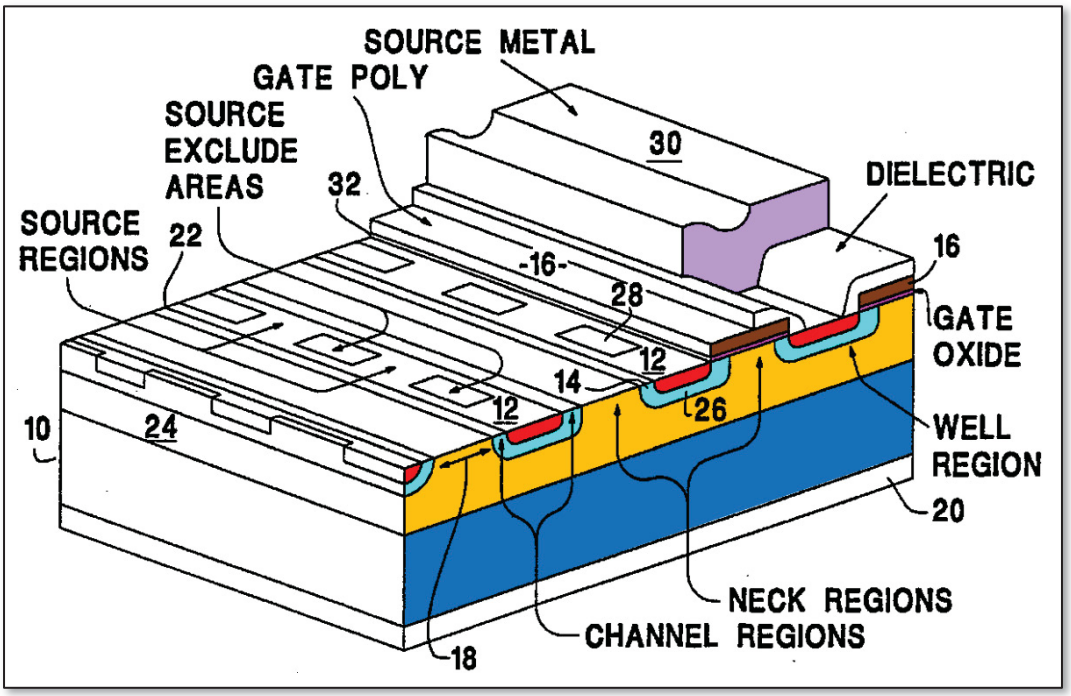
43. MOSFETs may have cross sections that are the same as or similar to the example shown in *Grant*'s Figure 1.11, *Baliga*'s Figure 1, and *Ryu*'s Figure 2A, yet have different—though all well-known—three-dimensional cellular structures.

See EX1016 at 338–339 ("the DMOS structure allows any conceivable cell topology as long as it meets all technological constraints such as alignment tolerances"); *id*., Figures 6.55 and 6.56; EX1019 at 15–17, 70–73, 455–457, Figures 1.13 and 3.9. Such cellular structures may include shapes that are hexagonal, square, circular, linear, or triangular. For example, *Grant*'s Figure 1.13 (reproduced below) illustrates two cellular structures—hexagonal and square—that have similar cross sections.



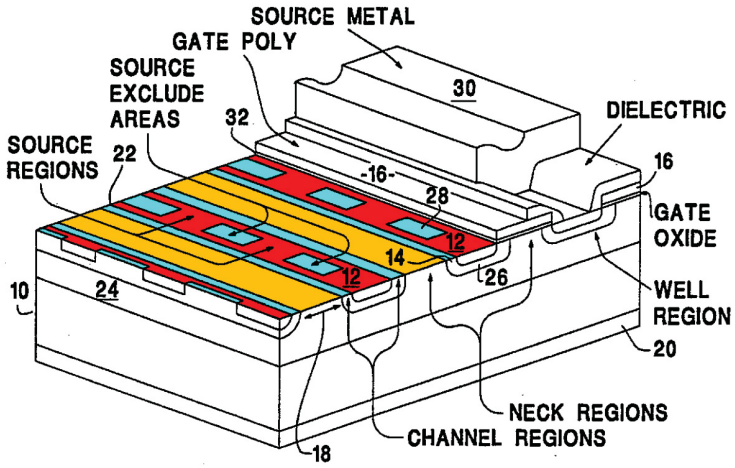
EX1019, Figure 1.13 (annotated)

44. Figure 1 (reproduced below) of U.S. Patent No. 5,317,184 ("*Rexer*") (EX1015) shows a three-dimensional linear cellular design of a MOSFET that also has a similar cross section to those in *Grant*'s Figure 1.13 but a linear shape to its cellular structure.

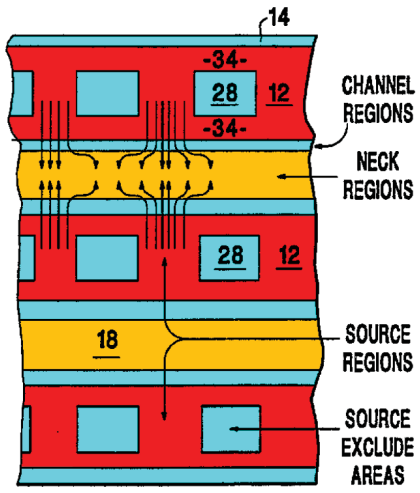


EX1015, FIG. 1 (annotated)

45. In addition to or instead of perspective views, top or plan views of power MOSFETs may be shown. For example, *Rexer* illustrates, in Figure 2, a partial plan view of the surface 22 of its MOSFET of Figure 1, "with the gate oxide, gate, and source metal removed." *Id.*, 1:43–45, 2:34–36. *Rexer*'s Figures 1 and 2 are reproduced and annotated side-by-side below. In *Rexer*'s Figure 2, the linear cellular structure is shown extending left-to-right in the plan view.



EX1015, FIG. 1 (annotated)



EX1015, FIG. 2 (annotated)

46. *Williams* shows top views of other known MOSFET features, for example in its Figure 19E, which is reproduced below. *Williams*'s Figure 19E shows a linear cellular structure extending top-to-bottom.

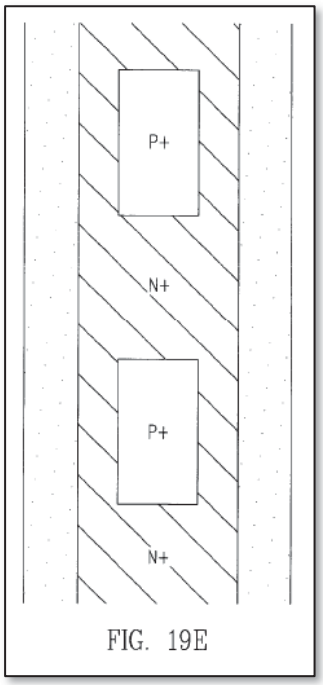


FIG. 19E

EX1004, FIG. 19E

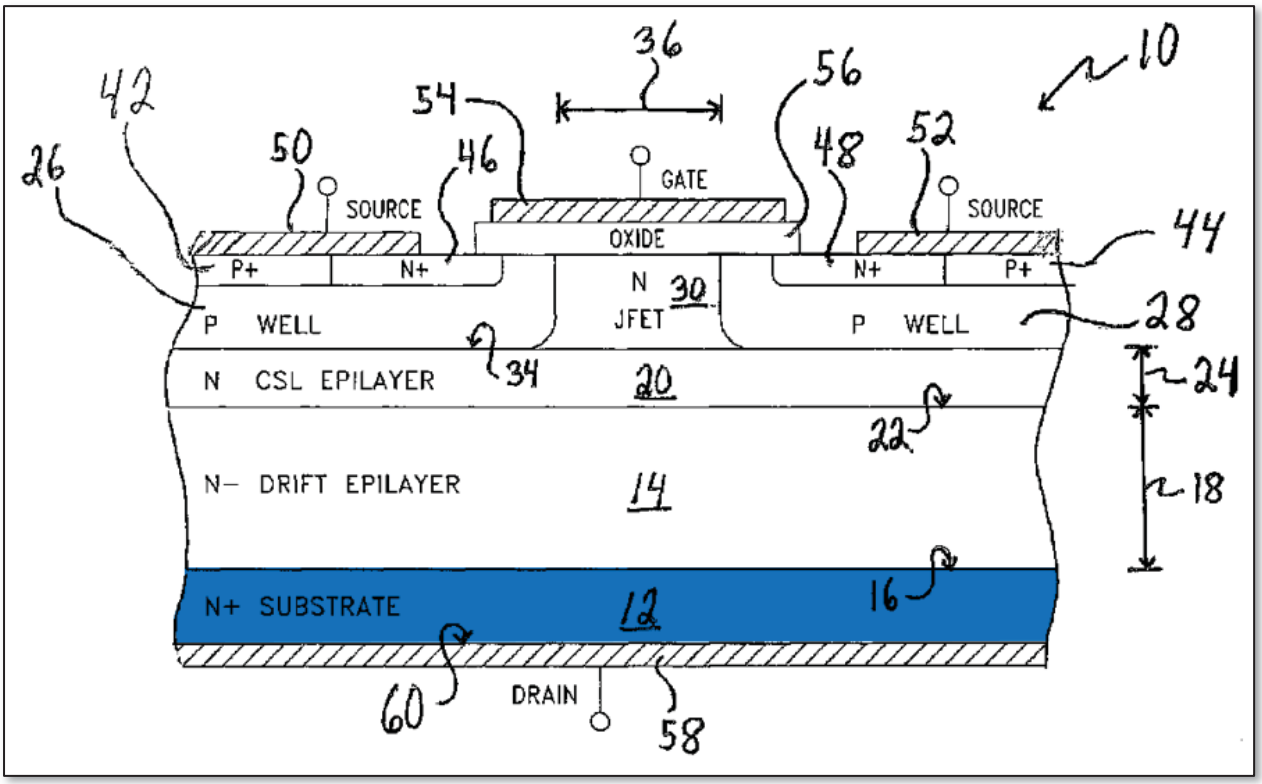
47. The relationships between cross-sectional, perspective, and top views of MOSFETs were well known. For example, a POSITA would have understood that, if a cross-sectional view of a unit cell of a MOSFET like shown in *Ryu*'s Figure 2A were of a linear cellular design like in *Rexer*, then *Ryu*'s cellular structure would extend perpendicular to the page just like the structure shown in *Rexer*'s Figure 1 perspective view. Similarly, a POSITA would have recognized that a top view like shown in *Williams*'s Figure 19E would extend in the same longitudinal direction as the top side of *Rexer's* three-dimensional MOSFET. Relatedly, a POSITA would have understood that a power MOSFET includes a plurality of adjacent unit cells. *See, e.g.*, EX1019, Figure 1.13; EX1015, FIG. 1 (illustrating three full unit cells); *see also* EX1019 at 15 ("High-current capability is obtained by connecting many cells together in parallel.").

VII. OVERVIEW OF THE '633 PATENT

A. The Alleged Invention of the '633 Patent

48. The '633 patent is generally directed to semiconductor devices for high-voltage power applications. EX1001, 1:12–14. In particular, the '633 patent describes and claims a semiconductor device referred to as a "vertical double-implanted metal-oxide semiconductor field-effect transistor," having a structure as depicted in Figure 1. *Id.*, 3:7–8, 4:4-9, Figure 1. The '633 patent notes that Figure 1

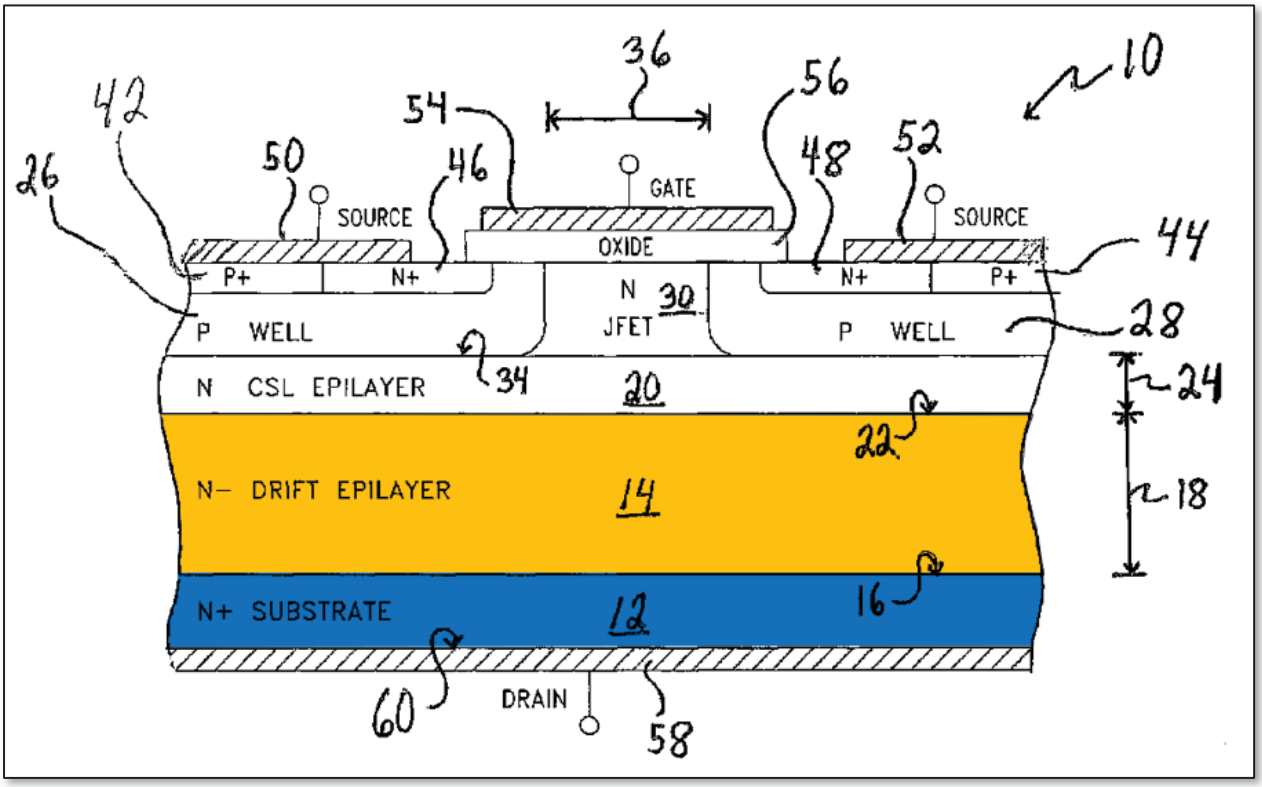
shows "a single 'transistor cell' and that a completely fabricated transistor device may include any number of" these devices. *Id.*, 5:26-30. As the '633 patent's Figure 1 shows, the semiconductor device 10 includes a **substrate 12** (annotated in blue below) that can be formed from silicon-carbide material and doped with N-type impurity to an "N+" concentration. EX1001, 4:4–13.



EX1001, FIG. 1 (annotated)

49. The '633 patent's semiconductor device also includes a **drift layer 14** (annotated in orange below) formed on a front side 16 of the **substrate 12**. *Id.*, 4:20–21. The **drift layer 14** may be epitaxially grown by, for example, a chemical vapor

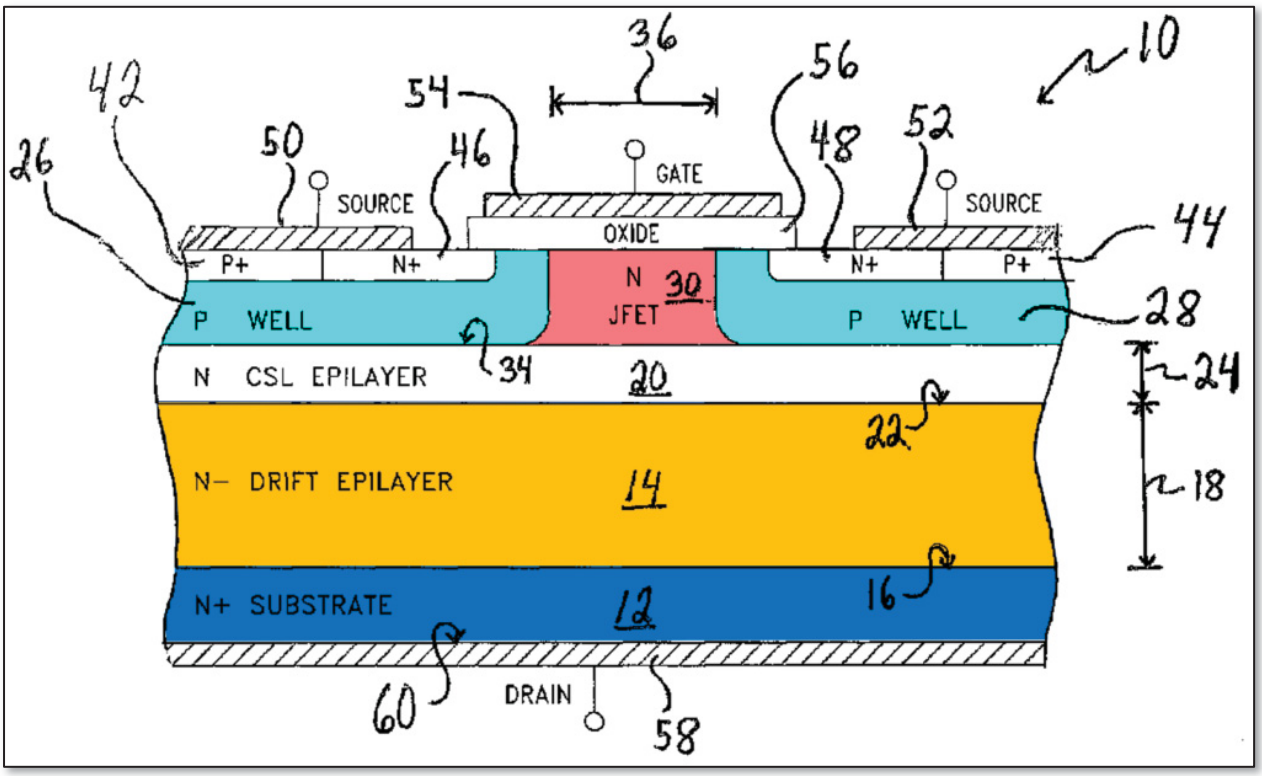
deposition process, formed of silicon-carbide, and doped with N-type impurities to an "N−" concentration. *Id.*, 4:35–41. Not relevant to this petition, the '633 patent's Figure 1 also shows an optional current spreading layer 20 ("CSL").



EX1001, FIG. 1 (annotated)

50. "The semiconductor device 10 also includes two doped semiconductor **wells or base regions 26, 28**" that "are doped with a P-type impurity to a 'P' concentration." *Id.*, 5:23–24, 5:42–43. The region between the **wells 26 and 28** represents the **JFET region 30** (annotated in salmon below). *Id.*, 5:25–26, 6:3–5; *cf.* EX1019 at 81 ("The JFET action occurs in the region between the p diffusions.");

id. at 44 ("JFET region"). The '633 patent notes that "the **wells 26, 28** and the **JFET region 30** may be formed by growing an extra-thick current spreading layer 20 and forming the 'P' **wells 26, 28** using a suitable incorporation process such as an ion implantation process." *Id.*, 5:56–60. Thus, the **JFET region 30** and the current spreading layer 20 have similar doping concentrations (*i.e.*, "N" concentration). *Id.*, 5:54–56, Figure 1 (which labels both **JFET region 30** and current spreading layer 20 as having "N" concentration).



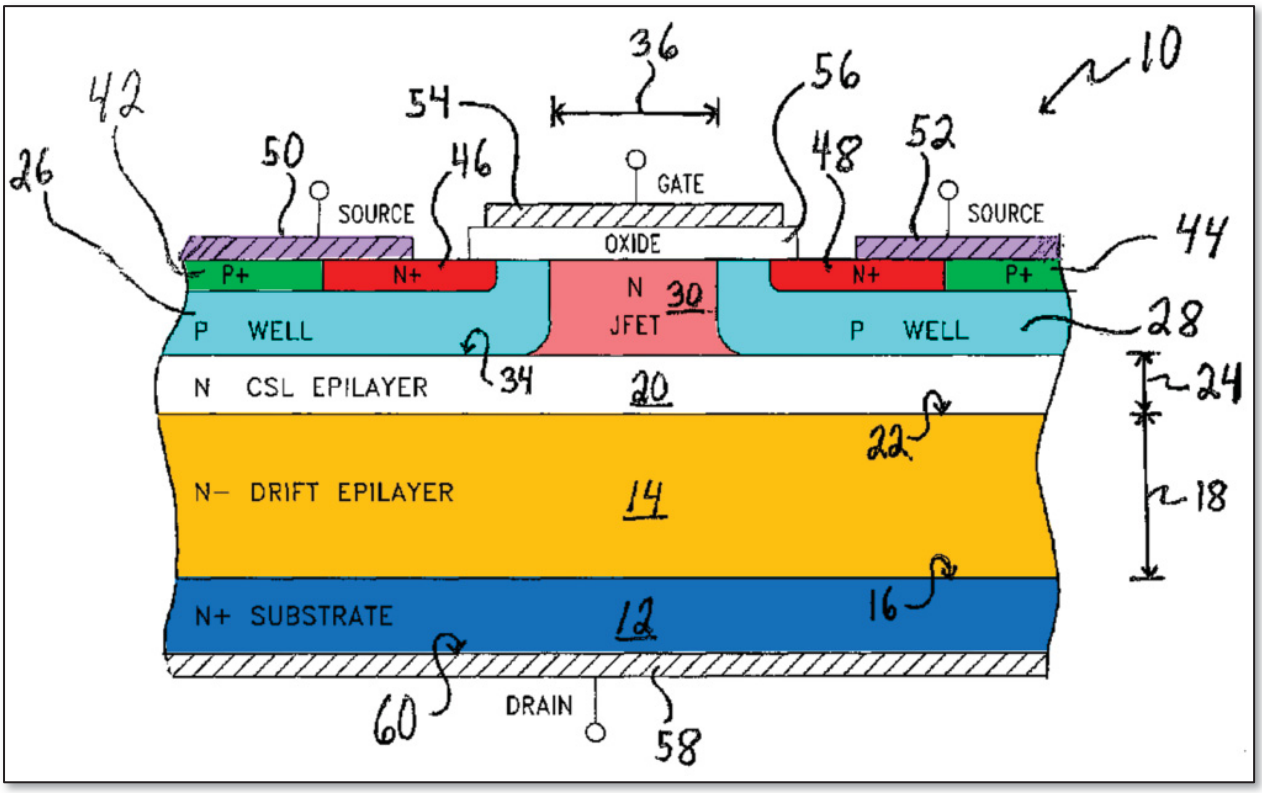
EX1001, FIG. 1 (annotated)

51. Optionally and alternatively, according to the '633 patent, "[b]y forming a **JFET region 30** with a doping concentration that is greater than the

doping concentration of the **drift layer 14**, the specific on-resistance of the semiconductor device 10 may be reduced compared to a MOSFET device having JFET regions and drift layers of substantially equal impurity concentrations." *Id.*, 6:16–21; *cf.* EX1019 at 83–84 ("Increasing the donor doping concentration in the drain throats . . . has two beneficial effects." "[T]he cell size can be reduced and . . . ***lower $R_{DS(on)}$ can be realized***."). The '633 patent also explains that fabricating the **JFET region 30** to have a width 36 of "three micrometers or less," which is short "relative to a typical DMOSFET device [may] reduce the specific on-resistance of the semiconductor device 10." *Id.*, 6:21–26; *cf.* EX1019 at 83–84 ("Increasing the donor doping concentration in the drain throats . . . has two beneficial effects." "[T]he ***cell size can be reduced*** and . . . lower $R_{DS(on)}$ can be realized.").

52. The semiconductor device 10 also includes **source regions 46 and 48** (annotated in red below) "defined in the P **wells 26 and 28**, respectively." EX1001, 6:63–65. "The **source regions 46 and 48** are doped with N-type impurities to an 'N+' concentration." EX1001, 6:65–66. **Base electrode regions 42 and 44** (annotated in green below and alternately referred to as "base contact regions" in the '633 patent specification) are located beside **source regions 46 and 48**, respectively, and are doped with P-type impurities to a "P+" concentration. *Id.*, 6:66–7:2; 7:30. The '633 patent explains that regions **42, 44**, **46, and 48** may be doped "using any

suitable doping technique such as, for example, an ion implantation process or the like." *Id.*, 7:2–4. As Figure 1 illustrates, metallic **source electrodes 50 and 52** (annotated in lavender below) are formed over the **source regions 46 and 48**, respectively. *Id.*, 7:4–6. As shown in Figure 1, the **source electrodes 50 and 52** also extend over the **base electrode regions 42 and 44**.



EX1001, FIG. 1 (annotated)

53. The '633 patent describes a "topological configuration" that, "[b]ecause of semiconductor manufacturing process variations, . . . can result in an undesirable source resistance if the **source regions 46, 48** are misaligned with

respect to the **base contact regions 42, 44** and/or the **source regions 46, 48** are misaligned with respect to the **source electrodes 50, [52]**." *Id.*, 7:39–44, Figure 2. "[T]o reduce the likelihood of misalignment between the source electrodes and the source regions," the '633 patent describes other topological configurations of its semiconductor device having source regions that each include "a plurality of base contact regions" arranged geometrically to increase "the tolerance to manufacturing variability." *Id.*, 7:52–8:6.

54. Whereas Figure 1 shows a cross-sectional side view, Figures 2–4 show views looking down onto the top of the device. *Id.*, 3:52–57. In particular, Figure 3 shows that "the **base contact regions 158, 160** are embodied as small 'islands' or regions within the larger **source regions 154, 156**." *Id.*, 7:57–59. In this arrangement, the "**base contact regions 158, 160** are formed to be located in a central location under the **source metallic electrodes 50, 52** with areas of **source regions 154, 156** spaced between each **base contact regions 158, 160**." *Id.*, 7:59–63. For the sake of illustration, the annotated Figure 3 below shows the "islands" of **base contact regions 158, 160** as if they are visible in the plan (or top) view; however, it is understood that **source electrodes 50, 52** would cover **base contact regions 158, 160** in the physical device such that the "islands" would not be visible in the plan view (as denoted by dashed lines in the original Figure 3).

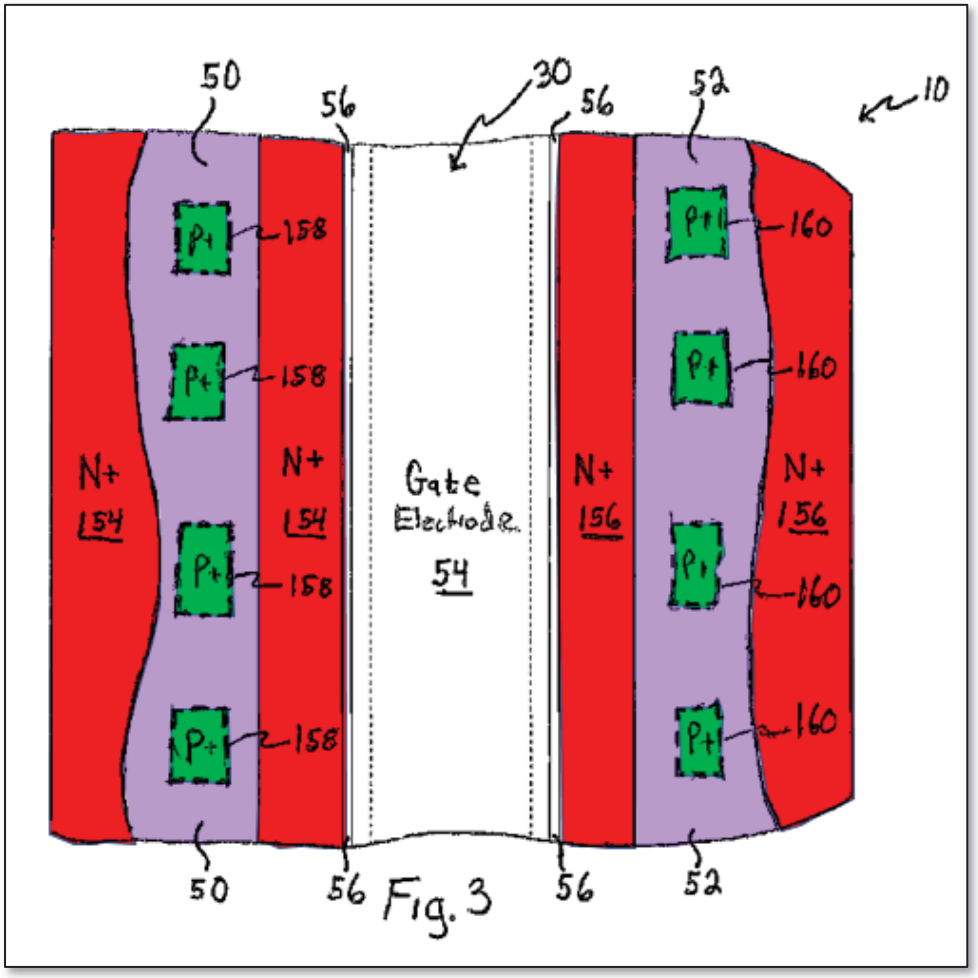


Fig. 3

EX1001, FIG. 3 (annotated)

55. As the ground below demonstrates, the semiconductor structures described and claimed by the '633 patent were well-known in the art before the '633 patent's priority date.

B. Prosecution History

56. The '633 patent issued from U.S. Patent Application No. 11/338,007, which was filed on January 23, 2006, claiming priority to U.S. Provisional

Application No. 60/646,152, filed on January 21, 2005. Independent claims 1, 12, and 17 referenced during prosecution correspond to issued claims 1, 9, and 12, respectively.

57. Based on my review of the correspondence between the patent applicant and the U.S. Patent and Trademark Office, the Examiner issued a non-final Office Action on April 4, 2007, rejecting all originally-filed claims 1–23 as being either anticipated by or obvious over several prior art references. EX1008 at 2–15. In response, the Applicant amended independent claims 1 and 12 to require a silicon-carbide substrate, and claims 12 and 17 to be respectively directed to specific topological configurations of the '633 patent's Figures 3 and 4, among other things. EX1009 at 2–6. The Applicant argued in relevant part that, because "Ono and Zeng are directed toward MOSFET device having silicon substrates, while Kumar is directed toward silicon-carbide MOSFET devices, . . . it is clear that no one of ordinary skill in the art would combine Ono or Zeng with Kumar." *Id.* at 9–10. As I will explain further below, I disagree with the argument that the Applicant advanced. That is, a POSITA would have been motivated to modify prior art silicon carbide references based on teachings regarding silicon structures. EX1005, 4:22–38 ("Almost all power MOSFETs being marketed today are fabricated in

monocrystalline silicon. . . . A power MOSFET . . . can be readily translated into silicon carbide using known manufacturing techniques.").

58. Correctly unpersuaded by the Applicant's argument, the Examiner issued a final Office Action, rejecting all pending claims and noting that, because "Ono and Zeng disclose ***the structure of the DMOS device*** and Kumar teaches the alternative of silicon-carbide with its known advantages[,] one of ordinary skill would indeed consider whether their particular problem would call for silicon-carbide." EX1010 at 12. The Applicant responded with similar arguments, but also further amended claims 12 and 17. *See* EX1011 at 2–9.

59. The Examiner rejected claim 1, maintaining that a POSITA would combine silicon and silicon carbide references, and allowed claims 12 and 17. EX1012 at 2, 9–10. The Examiner also indicated the allowability of claim 1's dependent claim 11, which was directed to the same configuration as claim 17. EX1012 at 9. Thereafter, Applicant amended claim 1 to include the subject matter of claim 11. EX1013 at 2, 8. The Examiner subsequently issued a Notice of Allowance on December 17, 2008, stating that the claimed configurations of the source regions and the base contact regions were not taught by the prior art. EX1014, Notice of Allowability at 2.

60. The Examiner did not have the benefit of *Ryu* and *Williams* , which are not of record. As I will show below, *Ryu* and *Williams*, disclose and render obvious the allegedly inventive features of the ’633 patent, including the configuration recited by issued claim 9 and its dependents, all challenged herein.

VIII. CLAIM CONSTRUCTION

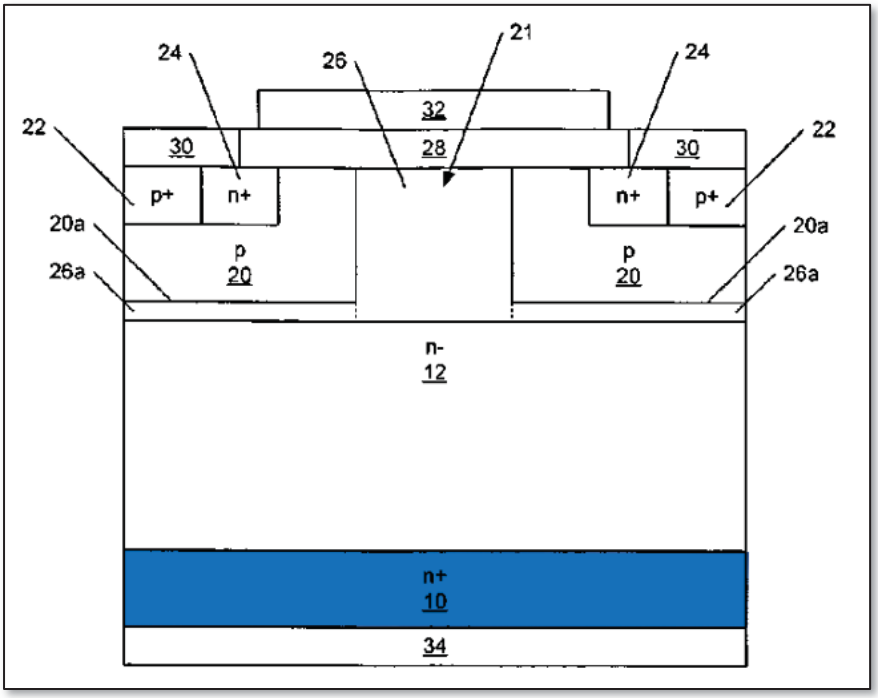
61. I understand that “claim construction” is the process of determining a patent claim’s meaning. I have been informed that claim construction is a matter of law and that in this proceeding, claim construction will be determined by the Patent Trial and Appeal Board (“the Board”). I understand that, during IPR, claims are construed according to the “*Phillips* standard.” I understand that the Board need only construe the claims when necessary to resolve the underlying controversy. I also understand that, given the close correlation between the asserted prior art and the challenged claims of the ’633 patent, the Board need not construe any terms of the challenged claims to resolve the underlying controversy, as any reasonable interpretation of those terms consistent with their plain meaning (as would have been understood by a POSITA at the time of the invention, having taken into consideration the language of the claims, the specification, and the prosecution history of record) reads on the prior art.

IX. OVERVIEW OF THE PRIOR ART REFERENCES

A. Ryu

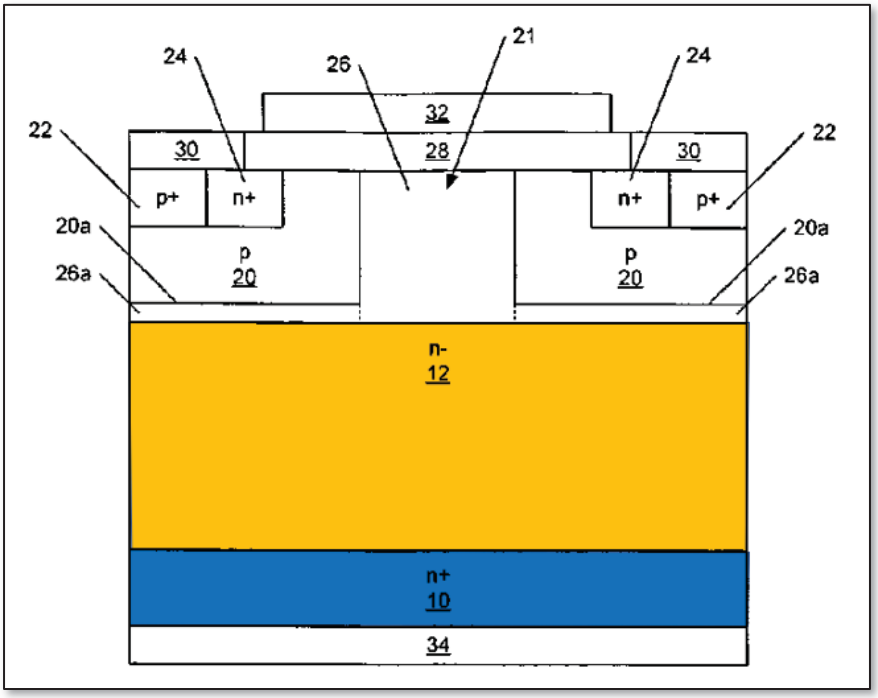
62. U.S. Patent Application Publication No. 2004/0119076 to Ryu ("*Ryu*") (EX1003), like the '633 patent, relates to "semiconductor devices . . . and, more particularly, to silicon carbide (SiC) metal-oxide semiconductor field effect transistors (MOSFETs)." EX1003, ¶3. Also like the '633 patent, *Ryu*'s embodiments of SiC MOSFETs "may reduce on-state resistance." *Id.*, ¶¶39, 64, 65.

63. For example, *Ryu*'s Figure 2A (reproduced below) shows a cross-sectional view of an embodiment of *Ryu*'s vertical MOSFET, which, as explained below, is strikingly similar to the cross-sectional view of '633 patent's MOSFET. EX1003, ¶¶28, 40. In *Ryu*'s Figure 2A, **layer 10** (annotated in blue below) may be a substrate made of silicon carbide and doped to an "n+" concentration. *See id.*, ¶40.



EX1003, FIG. 2A (annotated)

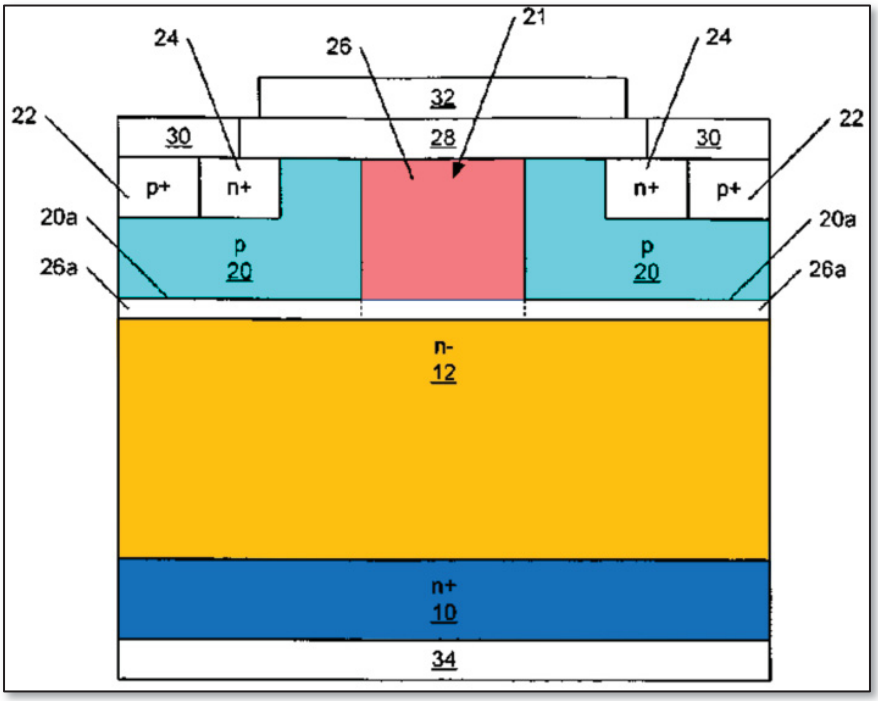
64. *Ryu*'s MOSFET further includes a **drift layer 12** (annotated in orange below) on the substrate **layer 10**. *Id.*, ¶40. Like in the '633 patent, the **drift layer 12** may be an epitaxial layer of silicon carbide and doped to an "n−" concentration. *Id.*



EX1003, FIG. 2A (annotated)

65. *Ryu* discloses that the gap between the **p-wells 20** "may be referred to as the **JFET region 21**" (annotated in salmon below). *Id.*, ¶44. *Ryu* points out that "the gap 21 [(*i.e.*, the **JFET region 21**)] between the **p-wells 20** has a higher carrier concentration than the **drift layer 12**." *Id.*, ¶42; *cf.* EX1001, 6:16–19 ("By forming a JFET region 30 with a doping concentration that is greater than the doping concentration of the drift layer 14, the specific on-resistance of the semiconductor device 10 may be reduced . . ."). According to *Ryu*, "if the gap is too narrow, the resistance of the **JFET region 21** may become very high." EX1003, ¶44. For this

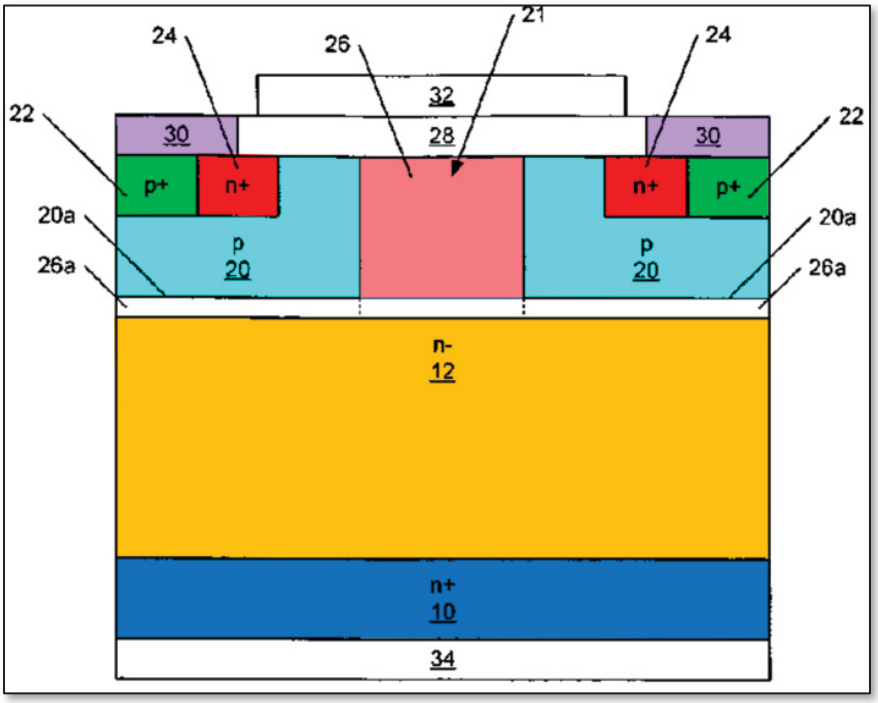
reason, *Ryu* discloses that "gaps of from about 1 μm to about 10 μm are preferred." *Id.*



EX1003, FIG. 2A (annotated)

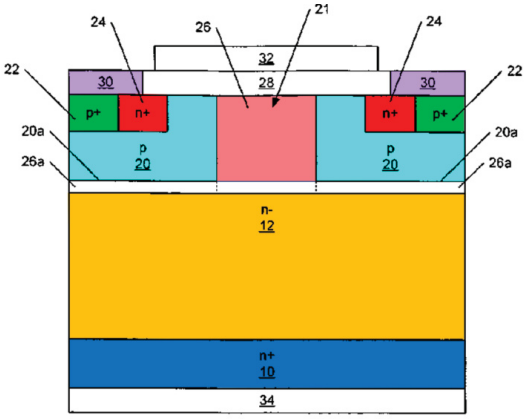
66. *Ryu*'s MOSFET also includes **n+ regions 24** (annotated in red below) and **p+ regions 22** (annotated in green below) disposed within the **p-wells 20**. EX1003, ¶45. The **n+ regions 24** are doped with n-type dopants to a "n+" concentration. *Id.*, ¶¶6, 45, and Figure 1. The **p+ regions 22** are adjacent to the **n+ regions 24** and formed by implanting p-type impurities to a "p+" concentration. *Id.*, ¶55. *Ryu* further discloses **source contacts 30** (annotated in lavender below) "to

provide an ohmic contact to both the **p+ regions 22** and the **n+ regions 24**." EX1003, ¶47.

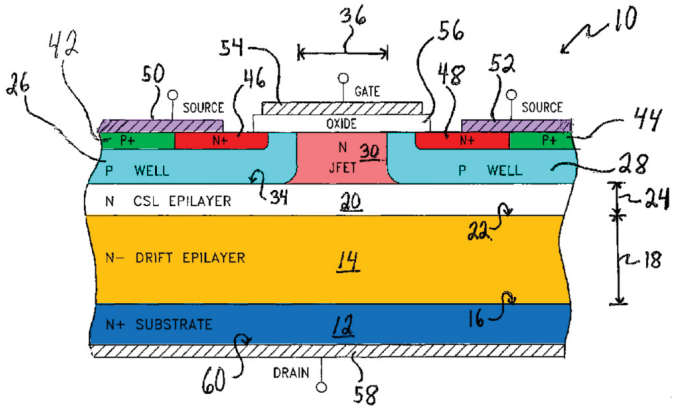


EX1003, FIG. 2A (annotated)

67. Comparing *Ryu*'s Figure 2A with the '633 patent's Figure 1 reveals that that *Ryu* discloses the same relevant semiconductor structure as the '633 patent.



EX1003, FIG. 2A (annotated)



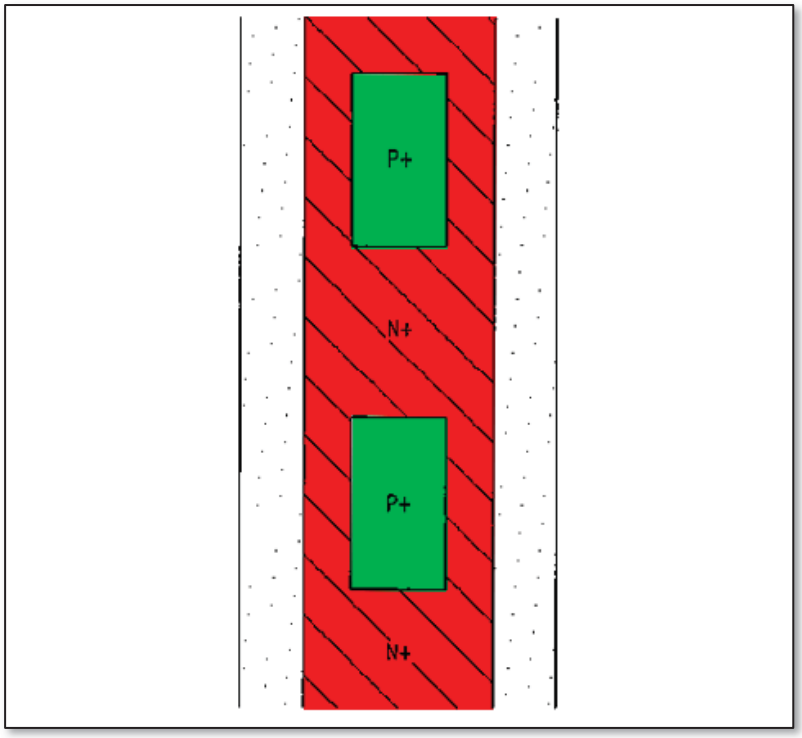
EX1001, FIG. 1 (annotated)

B. Williams

68. U.S. Patent No. 6,413,822 to Williams and Grabowski ("*Williams*") (EX1004), like the '633 patent, relates to vertical MOSFETs. *See, e.g.*, EX1004, 1:7–8, Figure 1. *Williams* notes that "[t]he primary design goal for a power MOSFET used as a switch is to achieve the lowest on-resistance by simultaneously minimizing each of its resistive constituents." *Id.*, 1:50–52. One of these resistive constituents is the source contact resistance. *See id.*, 1:33–37. *Williams* discloses "plan views of various source-body designs" in Figures 19A–19F—including plan views just like those of the '633 patent—to "achieve the lowest possible resistance" by maximizing the area of the **N+ source regions** and/or to "suppress parasitic bipolar turn-on, prevent snapback and ruggedize the device" (*i.e.*, prevent unwanted activation of the parasitic bipolar transistor) by maximizing the contact of the **P+ body contact regions** to the body region. *Id.*, 10:17–18; 16:28–35.

69. Like the '633 patent's source regions 154, 156 with "island" base contact regions 158, 160, *Williams* also discloses a continuous **N+ source region** (annotated in red below) with **P+ body contact windows** (annotated in green below) in Figure 19E. EX1004, 10:23–24; EX1001, Figure 3. Like the '633 patent, *Williams* also uses the term "island," but in reference to the geometry shown in its Figure 19C where the **N+ source regions** are ***not*** continuous, and instead take the

"island" shape. EX1004, 10:20-21 ("FIG. 19C shows continuous P+ body contact region with N+ source 'islands'."). Nevertheless, a POSITA would have readily appreciated that *Williams*'s **P+ body contact "windows"** of Figure 19E correspond to the "island" base contact regions of the '633 patent. *Williams* teaches that such a source-body design provides "better **N+** contact resistance and less **P+** contact area (less rugged)." *Id.*, 17:18–19.



EX1004, FIG. 19E (annotated)

X. SPECIFIC GROUND FOR PETITION

70. In my opinion, for the reasons noted below, claims 9–11 would have been obvious in light of the combined teachings of *Ryu* and *Williams*.

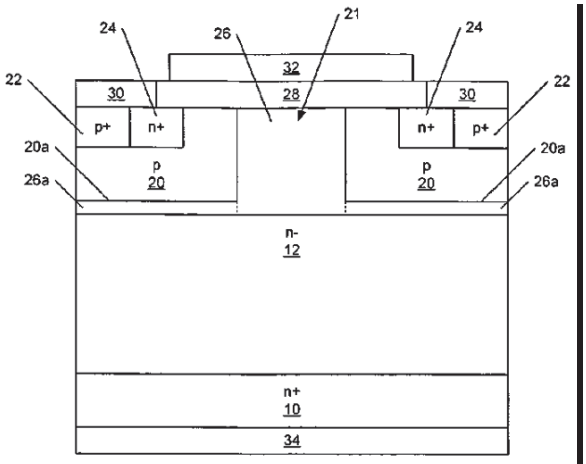
A. Ground I: Claims 9–11 are Obvious Over *Ryu* in View of *Williams*

1. Independent Claim 9

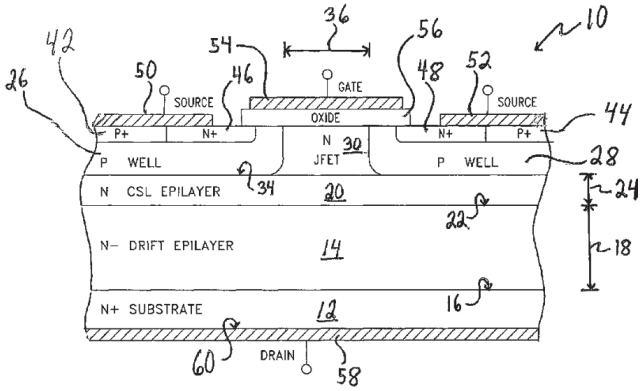
71. The combined teachings of *Ryu* and *Williams* renders claim 9 obvious.

(a) 9[preamble]: "A double-implanted metal-oxide semiconductor field-effect transistor comprising:"

72. In my opinion, even if the preamble is limiting, *Ryu* discloses it. *Ryu* discloses a metal-oxide semiconductor field-effect transistor (MOSFET). EX1003, ¶¶3, 28, 40. *Ryu* explicitly states that Figure 2A is a MOSFET. *Id.*, ¶40 ("MOSFETs according to embodiments of the present invention are illustrated in FIG. 2A."). *Ryu*'s Figure 2A is reproduced below, alongside the '633 patent's Figure 1 for comparison.



EX1003, FIG. 2A



EX1001, FIG. 1

73. *Ryu*'s MOSFET includes a gate contact 32 ("the gate contact is ***metal***"; EX1003, ¶13; *see also id.*, claims 10 and 41), over a gate oxide 28 ("The gate oxide may be thermally grown and may be a nitrided ***oxide*** and/or may be other oxides."';

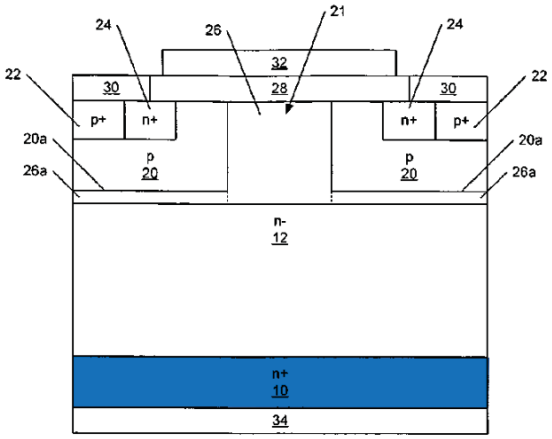
id., ¶46), over a combination of silicon carbide (*i.e.*, a ***semiconductor***) layers 26, 12, and 10 (*id.*, ¶¶40–41), thereby creating a metal-oxide semiconductor device. *Cf.* EX1005, 1:45–50 (describing a MOSFET as including "a conducting gate electrode, typically metal, that is separated from a semiconductor surface by an intervening insulator, typically silicon dioxide.").

74. *Ryu*'s MOSFET is doubly implanted. *Ryu* explains that, during the fabrication process of its MOSFET, using a mask 100, "impurities are implanted into the n-type epitaxial layer 26 to provide the p-wells 20," and in the next step of the process, "n-type impurities are implanted utilizing the mask 104 to provide the n+ regions 24." EX1003, ¶¶ 53–54, Figures 4B and 4C; *cf.* EX1021, 1:56–63 ("***double ion implantation sequence*** . . . by successive ion implantation of an acceptor atom (such as boron or aluminum) and a donor atom (such as nitrogen or phosphorous) ***to form the base and source regions***, respectively."); EX1020 at 960 ("DMOS structure is formed in SiC using a ***double ion implantation with two separate implantation masks***."); EX1022 at 659 ("the base and source regions are formed by ***successive ion implantation*** using aluminum or boron for the p-type base and nitrogen for the n+ source."). *Ryu*'s doubly implanted p-wells 20 and n+ regions 24 configuration is also the same as in the "Vertical ***Doubly Implanted MOSFET*** (DIMOSFET)" that *Ryu* illustrates in Figure 1. *Id.*, ¶¶6, 27, Figure 1.

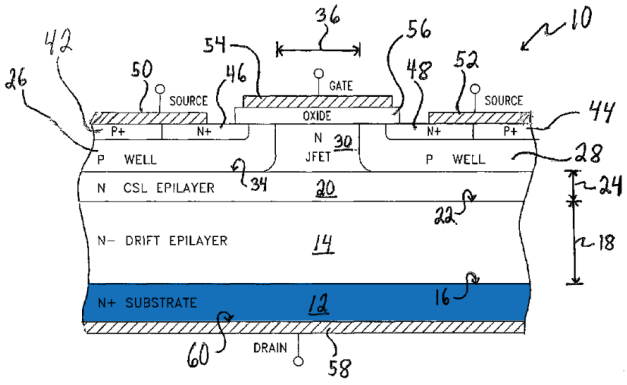
75. Therefore, *Ryu*'s MOSFET corresponds to the '633 patent's "*double-implanted metal-oxide semiconductor field-effect transistor*."

(b) 9[a]: "a silicon-carbide substrate;"

76. *Ryu* discloses element 9[a]. *Ryu* explains that its **layer 10**, which is shown in various figures such as Figures 2A, 2B, 3, and 4E, is made of silicon carbide. For example, *Ryu* states that "…layer 12 of silicon carbide is on an optional n+ ***layer 10 of silicon carbide***." EX1003, ¶40. *Ryu* also explains that **layer 10** can be the substrate. *Id*., ¶56 ("…***layer 10***, which may be formed by a backside implant of n-type impurities in a substrate or ***may be*** an epitaxial layer or ***the substrate itself***"). *Ryu*'s claims 13 and 23, which were published along with the rest of *Ryu* on June 24, 2004, and therefore qualify as prior art, also clearly disclose a silicon carbide substrate. *Id*., claims 13 ("… comprising an n-type ***silicon carbide substrate***"), 23 ("… wherein the n-type silicon carbide layer comprises an n-type ***silicon carbide substrate***."). As shown by *Ryu*'s Figure 2A and the '633 patent's Figure 1, both of which are reproduced below, *Ryu*'s silicon carbide substrate 10 corresponds to the '633 patent's silicon carbide substrate 12.



EX1003, FIG. 2A (annotated)

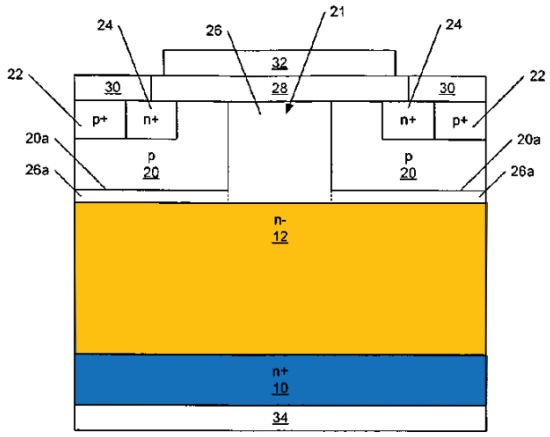


EX1001, FIG. 1 (annotated)

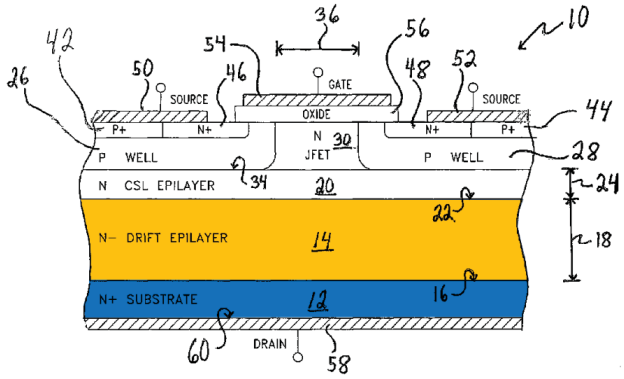
(c) 9[b]: "a drift semiconductor layer formed on a front side of the semiconductor substrate;"

77. *Ryu* discloses element 9[b]. For example, *Ryu*'s Figure 2A (reproduced below, alongside the '633 patent's Figure 1), shows that "a lightly doped n− **drift layer 12** of silicon carbide" (*i.e., "a drift semiconductor layer"*) is on the n+ **layer 10**. EX1003, ¶40.

78. *Ryu* further explains that its **drift layer 12** is "*formed on a front side of the semiconductor substrate*." *Ryu*'s Figure 2A shows that **drift layer 12** is on the front side of substrate 10, just as the drift layer 14 of the '633 patent is on its substrate 12. *Ryu* also makes clear that its **drift layer 12** is formed on substrate 10. *Id.*, ¶53 ("Alternatively, the drift layer 12 may be ***provided on an n+ silicon carbide substrate***.").



EX1003, FIG. 2A (annotated)



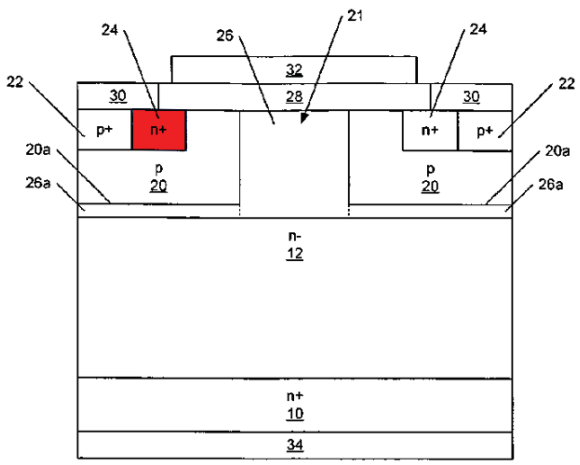
EX1001, FIG. 1 (annotated)

(d) 9[c]: "a first source region;"

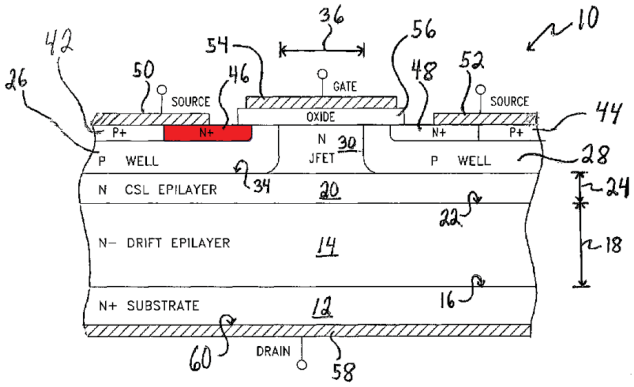
79. *Ryu* discloses element 9[c]. *Ryu* discloses that "**regions of n+ silicon carbide 24** . . . are disposed within p-wells 20." EX1003, ¶45. A POSITA would have understood *Ryu*'s **n+ regions 24** to be source regions because *Ryu*'s **n+ regions 24**: (1) are contacted by source contacts 30; and (2) correspond to the same "source regions" both in *Ryu* and *Ryu*'s other articles describing the same structure.

80. ***First***, *Ryu* explains that ***source*** contacts 30 provide ohmic contact to the **n+ regions 24**. EX1003, ¶47 ("Source contacts 30 … provide an ohmic contact to … the n+ regions 24."); *see also id.*, claims 6 and 36 ("a source contact on the first n-type silicon carbide region"). A POSITA would have understood that the **n+ regions 24** are ***source*** regions because they are contacted by the ***source*** contacts 30. In the same way, the '633 patent forms "source metallic electrode 50, 52 … over the source regions 46, 48, respectively" to achieve the same function. EX1001, 7:4-6.

A comparison below of *Ryu*'s Figure 2A and the '633 patent's Figure 1 also shows that *Ryu*'s **n+ regions 24** correspond to the '633 patent's **source regions 46 and 48** and are similarly of n-type doping at an "n+" concentration.

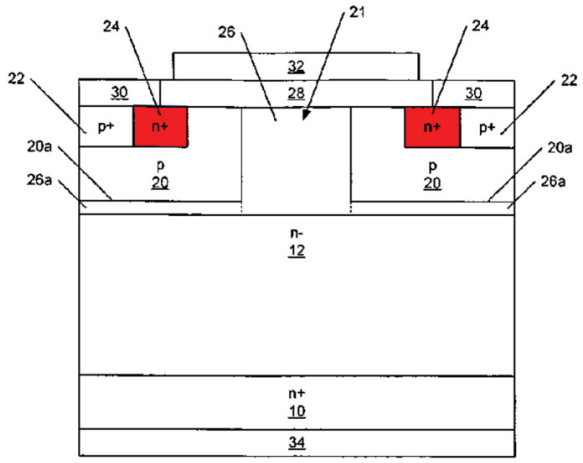


EX1003, FIG. 2A (annotated)

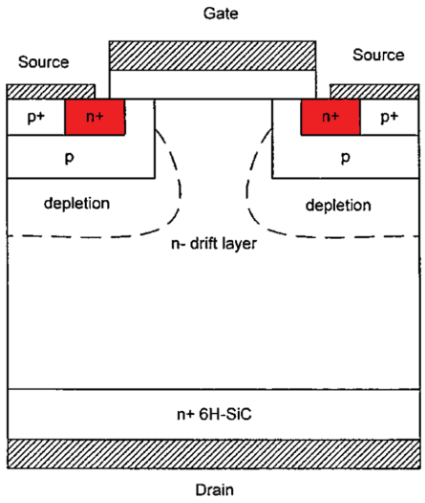


EX1001, FIG. 1 (annotated)

81. ***Second,*** the **n+ regions 24** in *Ryu*'s Figure 2A correspond, in location and in relative position to other structures, to the n+ regions in *Ryu*'s double-implanted MOSFET of Figure 1. *Id.*, ¶27 ("FIG. 1 is a cross-sectional view of a conventional ***DIMOSFET***"). *Ryu*'s Figures 1 and 2A are reproduced below with the n+ regions highlighted in red. *Ryu* explicitly discloses that the n+ regions in Figure 1 are "source regions." *Id.*, ¶6 ("***source regions (n+)***"). A POSITA would have understood that the **n+ regions 24** in Figure 2A correspond to the **n+ regions** in *Ryu*'s Figure 1 and that they were all source regions.

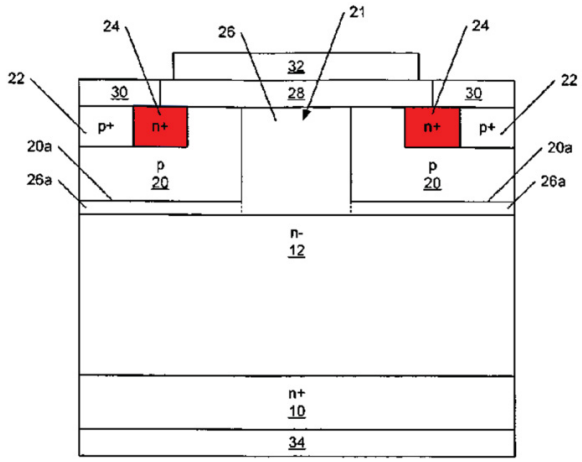


EX1003, FIG. 2A (annotated)

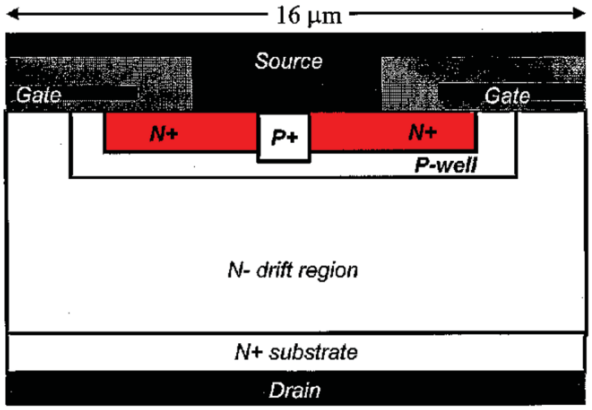


EX1003, FIG. 1 (annotated)

82. Similarly, the **n+ regions 24** in *Ryu*'s Figure 2A correspond to the N+ regions in the "DiMOSFET" that the inventor of *Ryu* presents in Figure 1 (reproduced below side-by-side with *Ryu*'s Figure 2A, with the N+ regions annotated in red) of a 2002 article titled "10 A, 2.4 kV Power DiMOSFETs in 4H-SiC." EX1023, Figure 1; *see also* EX1024, Figure 2. In Ryu's articles, EX1023 and EX1024, the DiMOSFET is drawn with a P-well structure centered and a portion of a gate at each of the left- and right-hand sides. In *Ryu*, EX1003, the same structure is drawn in Figure 2A with a gate centered and a portion of a p-well structure at each of the left- and right-hand sides. It would be readily apparent to a POSITA viewing these two drawings that the same structure is shown, just from a viewpoint shifted slightly to the left or right.



EX1003, FIG. 2A (annotated)



EX1023, FIG. 1 (annotated)

83. Ryu's articles explicitly disclose that the N+ regions are "source regions."

> **A 15 µm thick, 5.5 x 10^{15} cm^{-3} doped n-type epilayer was grown on an n^+, 4H-SiC substrate as the drift layer for the device. P-wells, 0.7 µm deep, were formed via aluminum ion implantation, after which 0.3 µm deep n^+ source regions were formed by nitrogen implantation. The MOS gate length, defined by these two implants, was 0.5 µm.**

EX1024 at 881; *see also* EX1023 at 321 (also describing "***N+ source regions***")

84. Accordingly, a POSITA would have understood *Ryu*'s **n+ regions 24** in Figure 2A to be ***source*** regions.

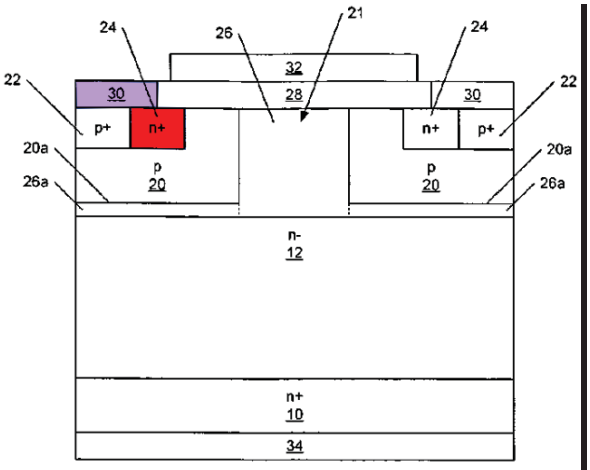
85. Thus, for example, *Ryu* discloses at least a first **n+ region 24** (*i.e.*, "*a first source region*") on the left in Figure 2A and a second n+ region 24 on the right.

(e) 9[d]: "a first source electrode formed over the first source region, the first source electrode defining a longitudinal axis;"

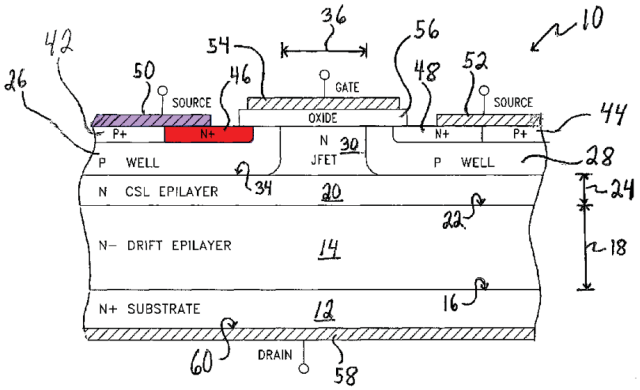
86. The combination of *Ryu* and *Williams* renders element 9[d] obvious. As I will explain below, *Ryu*'s **source contact 30** is a source electrode that is over **source region 24**. Moreover, it would have been obvious for *Ryu*'s **source contact 30** to define a longitudinal axis.

i. "source electrode"

87. *Ryu* discloses that "one or more **source contacts 30**, in some embodiments are formed of nickel (Ni), titanium (Ti), platinum (Pt) or aluminum (Al), combinations thereof . . . to provide an ohmic contact to both the p+ regions 22 and the **n+ regions 24**." EX1003, ¶47. Because *Ryu*'s **source contacts 30** are formed from a conductor, and because they physically contact the **n+ regions 24** (*i.e.,* "source regions"), they are "source electrodes." Moreover, *Ryu*'s **source contacts 30** perform the same function as the '633 patent's source electrodes. *Ryu*'s Figure 2A, for example, shows that the **source contacts 30** are over the **n+ regions 24**, just like the '633 patent's **source electrodes 50 and 52** are over the **source regions 46 and 48**. *See also id.*, claims 6 and 36 ("a ***source contact on*** the first ***n-type*** silicon carbide ***region***").



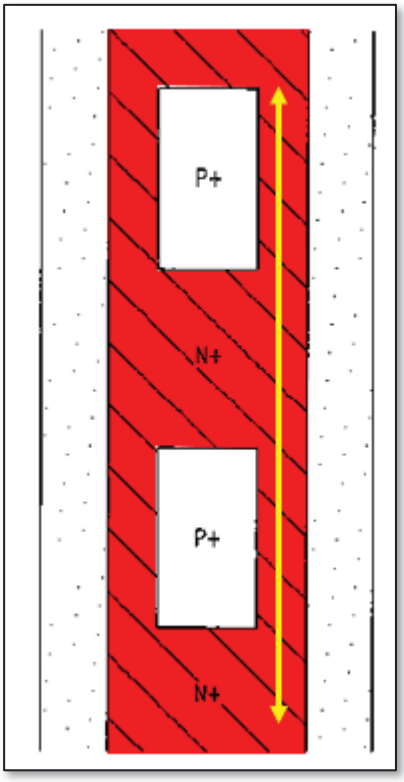
EX1003, FIG. 2A (annotated)



EX1001, FIG. 1 (annotated)

ii. "longitudinal axis"

88. *Ryu* in view of *Williams* teaches that the **source contact 30** defines a longitudinal axis. *Williams* discloses vertical MOSFETs having linear cellular configurations. EX1004, Figures 4A, 7A–7B, and 18. Related to these configurations, *Williams* explains that "[t]he source and body contact construction can also be varied geometrically . . . as shown in the plan views of FIGS. 19A–19F." *Id.*, 16:28-30. As shown in *Williams*'s Figure 19E, for example, the **N+ source region** extends along a "*longitudinal axis*" (*i.e.*, up-down with respect to the page), as annotated using a yellow arrow.

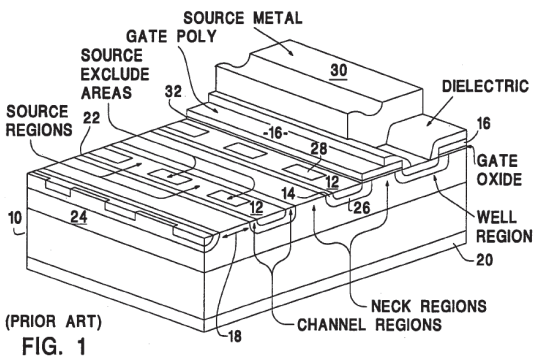


EX1004, FIG. 19E (annotated)

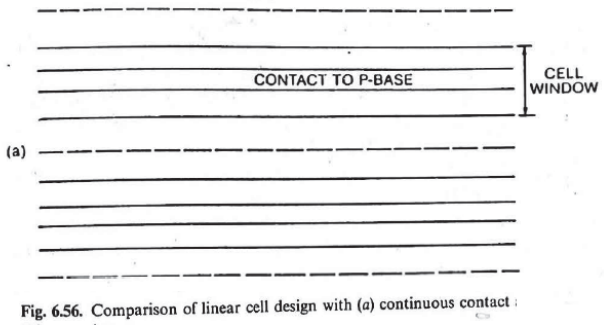
89. The obviousness of using *Williams*'s linear **N+ source region** configuration, which extends along a longitudinal axis, in *Ryu* is further shown by many other references, as I discussed herein, which demonstrate that MOSFETs with linear geometry were notoriously well-known. Moreover, a POSITA would have understood that, for a MOSFET to operate, a source electrode (*e.g.*, a metal or other conductive layer, such as *Ryu*'s **source contacts 30**) would be laid on top of and provide contact to the linear **N+ source region** and that, due to the linear geometry of the **N+ source region**, the source electrode would also extend in the direction of the linear source region and the electrode would thereby define a longitudinal axis.

90. As I discussed above in Section VI.F, *Ryu*'s Figure 2A is a cross-sectional view of a three-dimensional MOSFET and it was known in the art that such a cross section would correspond to a three-dimensional structure such as any of the well-known hexagonal, square, circular, linear, or triangular cellular structures. *See* EX1016 at 338–339 ("the DMOS structure allows any conceivable cell topology as long as it meets all technological constraints such as alignment tolerances"); *id.*, Figures 6.55 and 6.56; EX1019 at 15–17, 70–73, 455–457, Figures 1.13 and 3.9. A POSITA would have found it obvious to fabricate *Ryu*'s MOSFET into any one of these known cellular structures and, in particular, the linear cell structure taught by *Williams*. *See, e.g.*, EX1019 at 455 ("[O]ne manufacturer advocates the use of a linear metal gate structure, in conjunction with a simple four-mask fabrication process, for producing inexpensive high-voltage devices. Another, quite sophisticated interdigitated design has been made for high-frequency application.").

91. A POSITA would have understood that, if fabricated as a linear cell, *Ryu*'s cross-sectional view of its MOSFET would extend perpendicularly to the page. The linear cellular arrangement of *Williams* was well-known in the art, as shown by, for example, *Rexer* (at left, below) and Baliga (at right, below), and as explained above, would have been an obvious design choice for *Ryu*'s cellular structure.



EX1015, FIG. 1



EX1016, FIG. 6.56(a)

92. Linear cells have been commonly used in semiconductor technology since they have often been the easiest and most reliable structures to pattern lithographically. *See, e.g.*, EX1017 at 186 ("One common constraint imposed on VLSI layouts is the "manhattan" property, which requires that every edge of every feature be parallel to either the X or Y axis."); EX1018 at 238 ("A typical example of linear placement is the placement of a linear array, such as in gate matrix layout."). Additionally, most layout tools and software for such purposes have made it convenient to draw linear structures. *See, e.g.*, EX1017 at 186 ("It can be shown that any complex set of manhattan mask features can be represented exactly in the form of a collection of abutting rectangles. It follows that a layout editor which can manipulate only rectangles can be used to create and edit any manhattan design. Indeed, this approach was taken in early 1980's with the Caesar editor from Berkeley . . ."). As a consequence, linear structures have been overwhelmingly the most common structures used in semiconductor layouts. Additionally, for a device that

might be subject to high fields during use, the use of linear cells ensures more uniform and more predictable fields over the axis of the device. Accordingly, because the linear geometry was well known and because a POSITA would have been motivated to use it, it would have been obvious to construct the MOSFET of *Ryu*'s Figure 2A in view of *Williams*'s teachings of a linear cellular structure such that *Ryu*'s **n+ regions 24** and, consequently, *Ryu*'s **source contacts 30** extended perpendicularly to the page, thereby each **source contact 30** defining a longitudinal axis.

93. Thus, *Ryu* in view of *Williams* renders obvious at least a first **source contact 30** (*i.e.*, "*a first source electrode*") on the left, for example, formed over the left **n+ region 24** (*i.e.*, "*the first source region*"), with the first **source contact 30** defining a longitudinal axis.

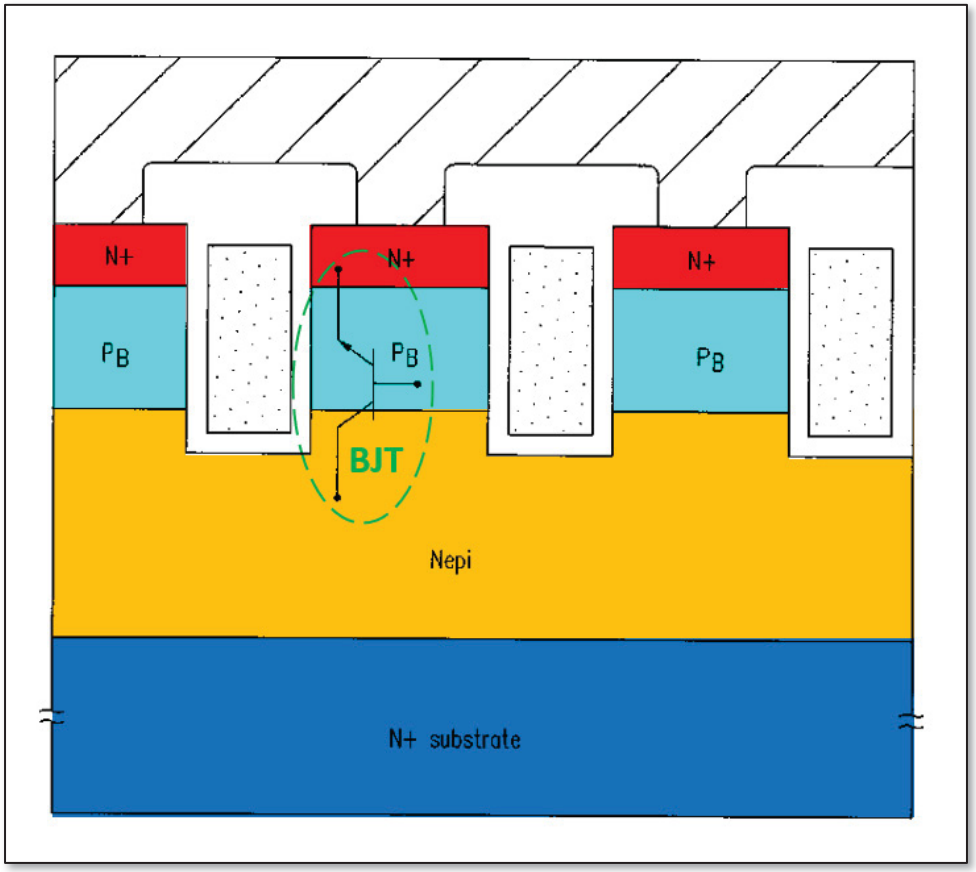
iii. Motivation to Combine Ryu and Williams

94. A POSITA would have been motivated to implement *Ryu*'s MOSFET according to *Williams*'s teachings such that *Ryu*'s MOSFET was formed using a linear cell structure having the **source contacts 30** define and extend along a longitudinal axis.

95. *Ryu* and *Williams* are from the same field of endeavor. Both references are directed to vertical MOSFETs. *Ryu* discloses embodiments of vertical

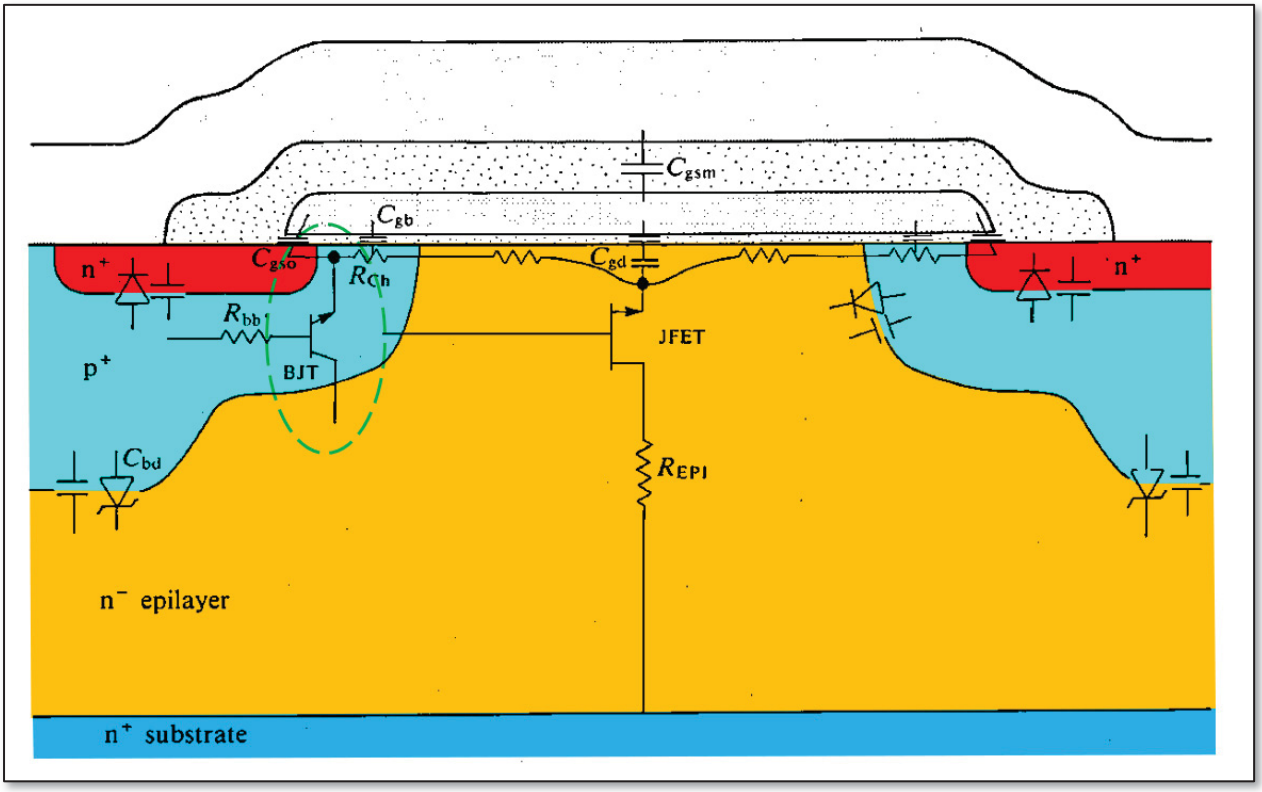
MOSFETs that "may reduce on-state resistance" compared to conventional vertical MOSFETs. EX1003, ¶¶6, 9, 39, Figure 1. *Williams* discloses structures for vertical MOSFETs that are used to reduce on-resistance. *See, e.g.*, EX1004, , Figure 1, 8:15–16 ("reduce the on-resistance of the DMOSFET"), 16:31–32 ("achieve the lowest possible resistance"). Thus, both references are directed to vertical MOSFETs and aim at reducing on-resistance. EX1003, ¶6; EX1004, 1:7–8.

96. Although *Williams* discloses MOSFETs with a so-called trench gate and *Ryu* discloses a MOSFET with a so-called planar gate, a POSITA would nonetheless have been motivated to use *Williams*'s teachings in *Ryu*. This is because *Williams*'s and *Ryu*'s MOSFETs share many common features to which the shape of the gate is irrelevant. For example, both *Williams*'s trench-gated vertical MOSFETs and *Ryu*'s non-trench-gated vertical MOSFET include a parasitic BJT within the epilayer that could inadvertently be activated. For both *Williams* and *Ryu*, the solution to the potential problem caused by this parasitic transistor is the same. For example, *Williams* describes such a "parasitic NPN bipolar transistor," which it illustrates in Figure 7A (reproduced below). EX1004, 6:9.



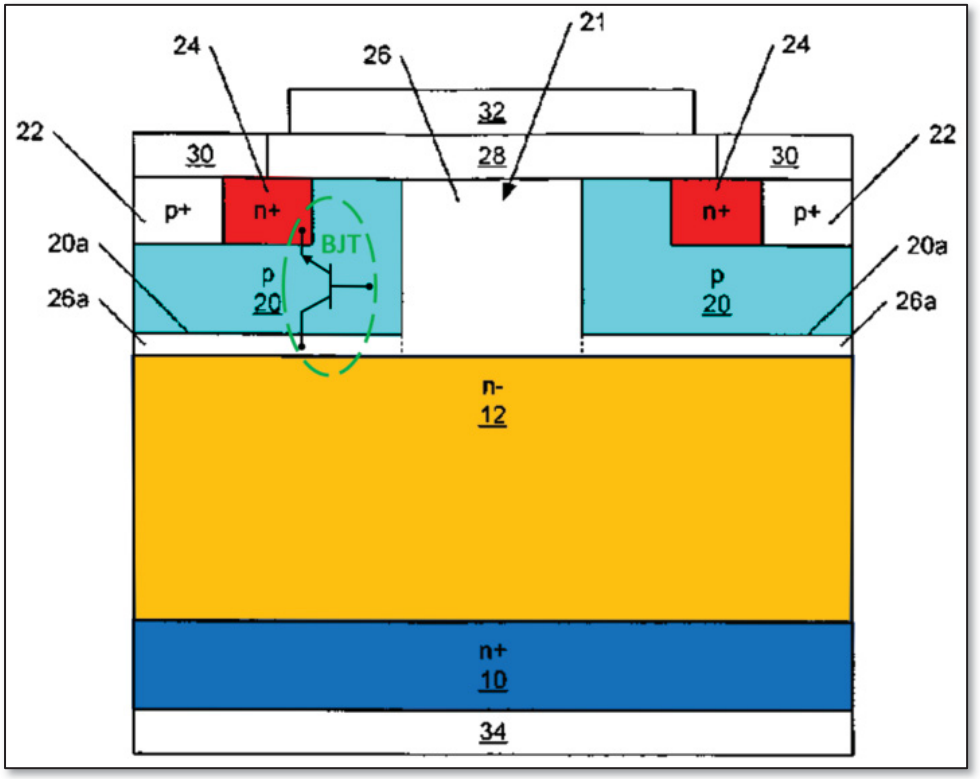
EX1004, FIG. 7A (annotated)

97. *Williams*'s parasitic BJT is formed between the source, the body, and the drain in the same way *Grant* illustrates a parasitic "npn bipolar junction transistor (BJT) formed between the source, the body, and the drain" of a non-trench-gated vertical MOSFET in Figure 3.15, reproduced below. EX1019 at 81.



EX1019, Figure 3.15 (annotated)

98. Based on at least *Grant*'s teachings, a POSITA would have understood that a parasitic npn BJT would also be formed in *Ryu*'s MOSFET between the n+ region 24 (*i.e.*, source region), p-well 20 (*i.e.*, body), and the n-type epitaxial layer 26 (*i.e.*, portion of drain region), as annotated in *Ryu*'s Figure 2A below. *See* EX1003, ¶53.



EX1003, FIG. 2A (annotated)

99. Both *Ryu* and *Williams* prevent the parasitic BJT from activating by shorting the source to the body, via p+ diffusion, using a source electrode. EX1003, Figure 2A (illustrating **source contacts 30** shorting **n+ regions 24** to p-wells 20 via **p+ regions 22**); *see, e.g.*, EX1004, Figure 15D, 15:6–8 ("Metal layer [158] contacts both N+ source region 159 and P+ body contact region 160, thereby shorting the source and body together."). *See also* Section VI.D above. At least because *Ryu* and *Williams* both share the common problem of preventing the parasitic BJT from activating, and both solve that problem in the same way, *i.e.*, by shorting the body

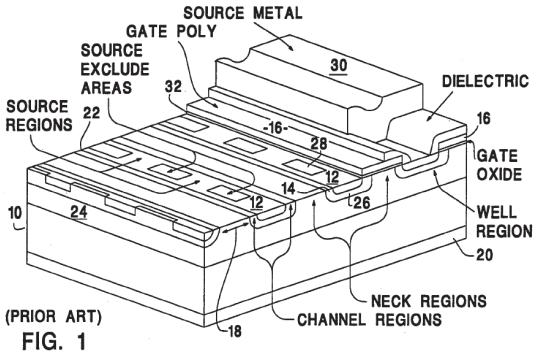
to the source, a POSITA would have recognized that features of *Williams*, such as *Williams*'s well-known linear geometry, were applicable in *Ryu*.

100. Furthermore, although *Ryu* is directed to silicon-carbide MOSFETS and *Williams* to silicon MOSFETs, *Baliga* teaches that conventional power MOSFETs, including silicon MOSFETs, "can be readily translated into silicon carbide using known manufacturing techniques." EX1005, 4:22–38. *Ghezzo* also teaches a method of replacing the conventional double-diffusion used in silicon MOSFETs with a double ion implantation sequence for silicon carbide MOSFETs. EX1021, 1:56–63.

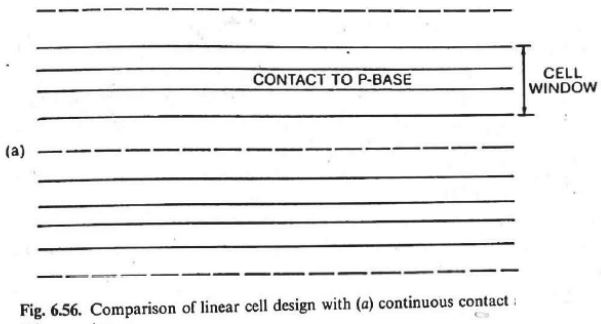
101. Accordingly, a POSITA would have understood that the teachings of *Williams* were directly applicable to *Ryu*'s silicon carbide MOSFETs.

102. Implementing *Ryu*'s MOSFET in a linear cell structure such that *Ryu*'s **n+ regions 24** and, consequently, *Ryu*'s **source contacts 30** define and extend along a longitudinal axis as taught by *Williams* would have yielded expected, predictable results. *Ryu* discloses that "one or more **source contacts 30**, in some embodiments are formed of nickel (Ni), titanium (Ti), platinum (Pt) or aluminum (Al), combinations thereof . . . to provide an ohmic contact to both the p+ regions 22 and the **n+ regions 24**." EX1003, ¶47. *Ryu*'s **source contacts 30** are formed from a conductor in physical contact with the **n+ regions 24**. As I described above,

Williams teaches, in Figure 19E, for example, an **N+ source region** that extends along a longitudinal axis. As also described above, the linear cell arrangement of *Williams* was well-known in the art, as shown by, for example, *Rexer* (at left, below) and Baliga (at right, below), and as explained above, would have been an obvious design choice for *Ryu*'s cell structure having predictable results.



EX1015, FIG. 1



EX1016, FIG. 6.56(a)

103. A POSITA would have been further motivated to combine the teachings of *Ryu* and *Williams* because forming *Ryu*'s structure using *Williams*'s linear cell arrangement would have been obvious to try. As I explained above, MOSFETs may have cross sections that are the same as or similar to the example shown in *Ryu*'s Figure 2A, yet have different—though all well-known—three-dimensional cellular structures. *See* EX1016 at 338–339 ("the DMOS structure allows any conceivable cell topology as long as it meets all technological constraints such as alignment tolerances"); *id*., Figures 6.55 and 6.56; EX1019 at 15–17, 70–73, 455–457, Figures 1.13 and 3.9. Such cellular structures may include shapes that are

hexagonal, square, circular, linear, or triangular. A POSITA could have pursued any of these potential cellular structures, in particular the linear cellular structure, with a reasonable expectation of success because the analysis would have simply involved trying each one of these solutions. *See, e.g.,* EX1019 at 455 ("[O]ne manufacturer advocates the use of a linear metal gate structure, in conjunction with a simple four-mask fabrication process, for producing inexpensive high-voltage devices. Another, quite sophisticated interdigitated design has been made for high-frequency application."). Moreover, this implementation of *Ryu* using a linear cellular structure would have been well within the knowledge and skillset of a POSITA.

iv. Reasonable Expectation of Success in Combining Ryu and Williams

104. A POSITA would also have had a reasonable expectation of success. The combination of *Ryu* and *Williams* represents a straight-forward implementation of steps of the well-understood semiconductor fabrication processes to change the shape and location of the structures, which a POSITA would have been familiar with and been able to implement. The reasons a POSITA would have expected success parallel those that provide motivation for this combination—including because both *Ryu* and *Williams* are directed to vertical MOSFETs. EX1003, ¶¶6, 9, 39, Figure 1; EX1004, Abstract, 1:7–8, Figure 1. As I discussed above, linear cell geometry was well known and a POSITA would have expected a linear cell implementation of

Ryu's structure to operate, just as linear cell implementations of other MOSFETs were known to operate. A POSITA would have had a reasonable expectation of success in implementing *Ryu*'s MOSFET in a linear geometry because *Ryu*'s underlying specification was designed to be extensible and flexible in its application to well-known cellular shapes and layouts. EX1003, ¶¶38 ("This invention may, however, be embodied in many different forms…"), 63, 66.

105. Accordingly, *Ryu* in view of *Williams* renders obvious element 9[d] and a POSITA would have been motivated to combine the teachings of these references and would have had a reasonable expectation of success.

(f) 9[e]: "a plurality of first base contact regions defined in the first source region, each of the plurality of first base contact regions being spaced apart from each other in a direction parallel to the longitudinal axis defined by the first source electrode;"

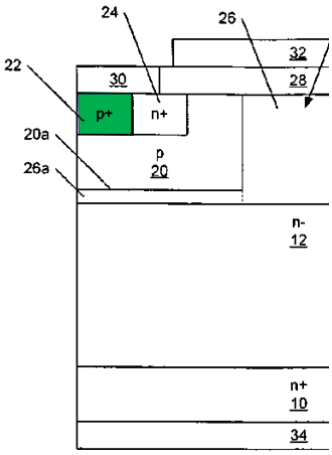
106. The combination of *Ryu* and *Williams* renders element 9[e] obvious. As I will explain below, *Ryu*'s **p+ regions 22** are base contact regions. Moreover, it would have been obvious to form a plurality of *Ryu*'s **p+ regions 22** in the **n+ source regions 24** described in limitation 9[c], above, and spaced apart from each other in a direction parallel to the longitudinal axis defined by the **source contact 30**, all as taught by *Williams*. A POSITA would have been motivated to make this

combination for the reasons discussed below and would have had a reasonable expectation of success in doing so.

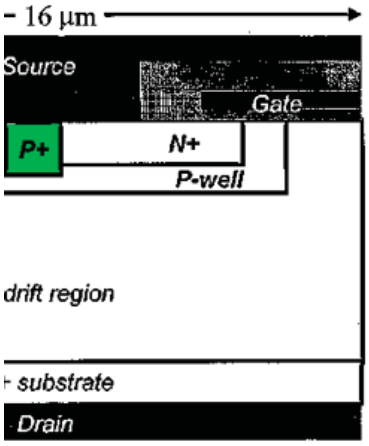
i. "base contact region"

107. *Ryu* discloses that "**regions of n+ silicon carbide 24** and . . . **regions of p+ silicon carbide 22** are disposed within p-wells 20" and that the "**regions of p+ silicon carbide 22** may be adjacent the **regions of n+ silicon carbide 24**." EX1003, ¶45. A POSITA would have understood that *Ryu*'s **p+ regions 22** are base contact regions because *Ryu*'s **p+ regions 22**: (1) correspond to the same "p+ contacts" in *Ryu*'s other articles describing the same structure; and (2) provide low resistance ohmic contact to the p-wells 20 to short the source to the base as was well known in the art.

108. ***First,*** the **p+ regions 22** in *Ryu*'s Figure 2A correspond to the P+ regions in double-implanted MOSFETs that the inventor of *Ryu* illustrates in prior and contemporaneous articles. *See* EX1023, Figure 1 (annotated below along with *Ryu*'s Figure 2A to show the P+ regions in green); EX1024, Figure 2.



EX1003, FIG. 2A
(excerpted annotated)



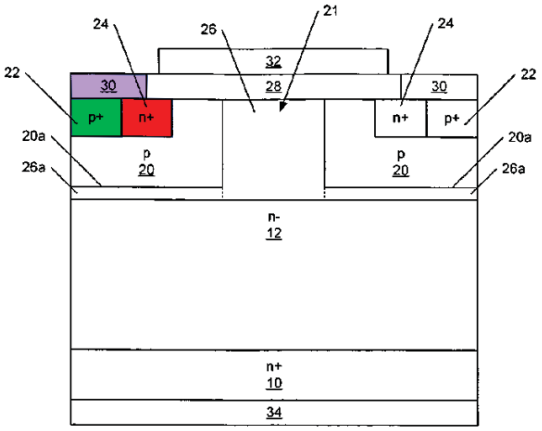
EX1023, FIG. 1
(excerpted and annotated)

109. These P+ regions are explicitly disclosed to be "p^+ contacts to the p-wells." EX1023 at 321 ("A heavy dose aluminum implantation formed ***p^+ contacts to the p-wells***, as wells as the floating guard rings to terminate the edges."); EX1024 at 881 ("A heavy dose aluminum implantation formed ***p^+ contacts to the p-wells*** as wells as the floating guard rings."). Like the p+ region in Ryu's articles, a POSITA would have understood *Ryu*'s **p+ regions 22** provide contacts to the p-wells 20.

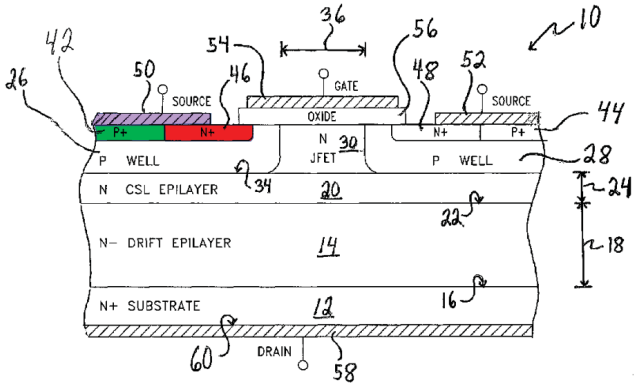
110. ***Second***, a POSITA would have understood that *Ryu*'s **p+ regions 22** provide low resistance ohmic contact to the p-wells 20. *See* Section VI.D above. As *Ghezzo* explains, "[a]lthough an electrical connection can be made directly to the p type base region, the p+ ***base contact region*** provides an improved connection." EX1021, 5:28–30; *see also* EX1004, 6:24–26 ("the integration of a shallow P+ region used to achieve a low resistance ohmic contact to the body"); *id.*, 16:32–34

("maximize the ***P+ contact to the body region*** (to suppress parasitic bipolar turn-on, prevent snapback and ruggedize the device)"); EX1006, 5:59–64 ("The base regions 11 . . . can be doped more heavily by additional implantation of aluminum for a higher latch-up strength . . . in the ***base contact region*** 12 at the source electrode 15, and thus be p+-conducting."). As exemplified by *Ghezzo*, a POSITA would have understood that *Ryu's* p+ region provides the desired low resistance connection to the base, and is therefore a "base contact region."

111. Additionally *Ryu*'s Figure 2A and the '633 patent's Figure 1 are reproduced below. As shown, *Ryu*'s **p+ regions 22** and the '633 patent's "base contact regions" 42 and 44 are both p+ regions that are disposed between the source contact (30 for *Ryu* and 50 for the '633 patent) and the P well (20 for Ryu and 26 for the '633 patent). *Ryu*'s **p+ regions 22** have the same doping with p-type impurities as the "base contact regions" 42 and 44 of the '633 patent. *Cf.* EX1003, ¶¶45, 55 ("…p-type impurities are implanted utilizing the mask 106 to provide the **p+ regions 22**.") EX1001, 6:66–7:2("The base electrode regions 42, 44 are doped with P-type impurities to a 'P+' concentration.") Moreover, *Ryu*'s **p+ regions 22** perform the same function as the '633 patent's "base contact regions" 42 and 44, *i.e.*, both provide low resistance between the source contact and the P well. For these reasons, both are "base contact regions."



EX1003, FIG. 2A (annotated)

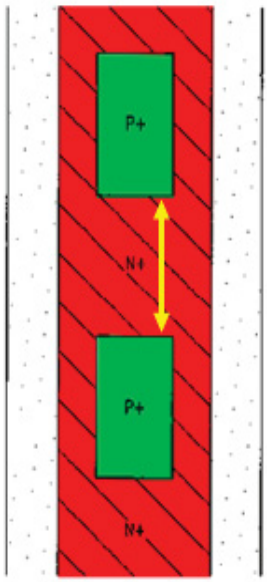


EX1001, FIG. 1 (annotated)

ii. "a plurality of first base contact regions defined in the first source region, each of the plurality of first base contact regions being spaced apart from each other in a direction parallel to the longitudinal axis defined by the first source electrode"

112. *Ryu* does not explicitly disclose a plurality of left **p+ regions 22** defined in the left **n+ region 24** and spaced apart from each other in a direction parallel to the longitudinal axis defined by the left **source contact 30**. However, *Williams* does. Specifically, *Williams* discloses "a continuous **N+ source region** with **P+ body contact** 'windows'" in Figure 19E (reproduced below, alongside the '633 patent's Figure 3 for comparison). EX1004, 10:23–24. As shown in *Williams*'s Figure 19E, the **P+ body contact** windows are "*defined in*" the **N+ source region** and are "*spaced apart from each other in the direction of a longitudinal axis*" (*i.e.*, up-down with respect to the page), as annotated using yellow arrows, in just the same way as

shown in the '633 patent. It would have been obvious to use *Williams*'s configuration of **P+ body contacts** in *Ryu*.



EX1004, FIG. 19E (annotated)

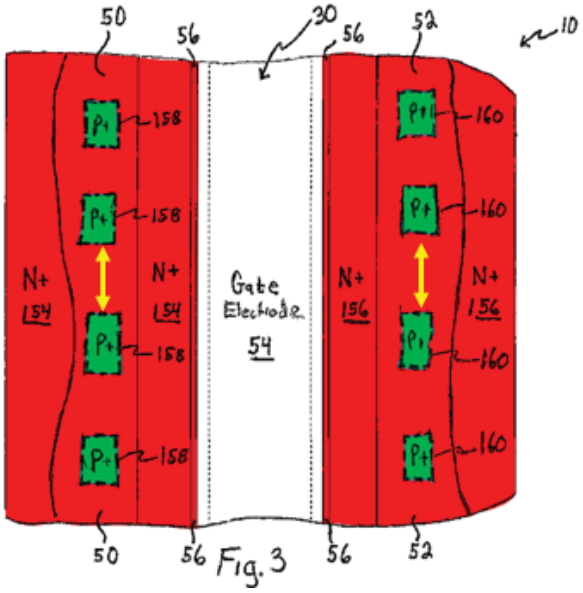


Fig. 3

EX1001, FIG. 3 (annotated)

113. A POSITA would have understood that, for a MOSFET to operate, a source electrode (*e.g.*, a metal or other conductive layer, such as *Ryu*'s **source contacts 30**) would be laid in the direction of the longitudinal axis on top of and make electrical contact to both the **P+ body contact** windows and the **N+ source region**. *See* EX1004, 15:6–8, Figure 15D ("Metal layer [158] contacts both N+ source region 159 and P+ body contact region 160, thereby shorting the source and body together.").

114. Thus, when implemented with *Williams*'s topology, *Ryu*'s **p+ regions 22** would be defined in the **N+ source region** and spaced apart from each other in a

direction parallel to the longitudinal axis defined by the source electrode just as *Williams*'s **P+ body contact** windows are positioned.

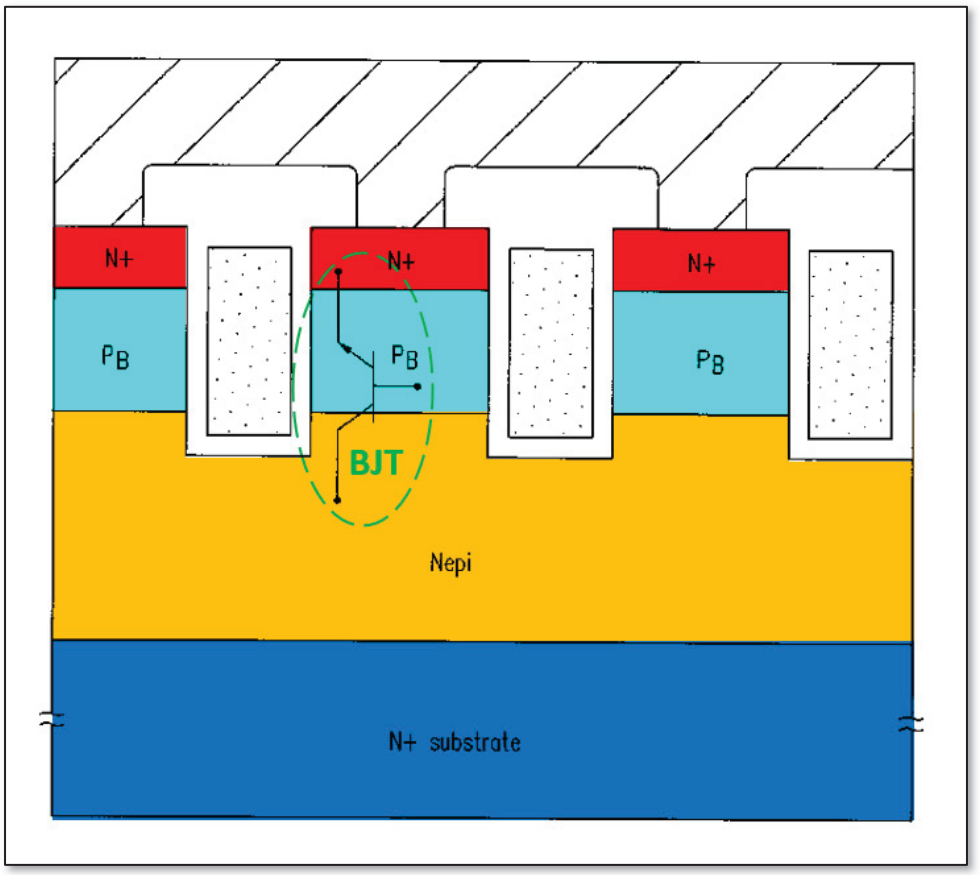
iii. Motivation to Combine Ryu and Williams

115. A POSITA would have been motivated to modify *Ryu*'s MOSFET according to and informed by *Williams*'s teachings such that *Ryu*'s left **p+ region 22** is defined repeatedly in the left **n+ region 24**, and the repeated left **p+ regions 22** are spaced apart from each other in a direction parallel to the longitudinal axis defined by the left **source contact 30**.

116. *Ryu* and *Williams* are from the same field of endeavor. Both references are directed to vertical MOSFETs. *Ryu* discloses embodiments of vertical MOSFETs that "may reduce on-state resistance" compared to conventional vertical MOSFETs. EX1003, ¶¶6, 9, 39, Figure 1. *Williams* discloses structures for vertical MOSFETs that are used to reduce on-resistance. *See, e.g.*, EX1004, Figure 1, 8:15–16 ("reduce the on-resistance of the DMOSFET"), 16:31–32 ("achieve the lowest possible resistance"). Thus, both references are directed to vertical MOSFETs and aim at reducing on-resistance. EX1003, ¶6; EX1004, 1:7–8.

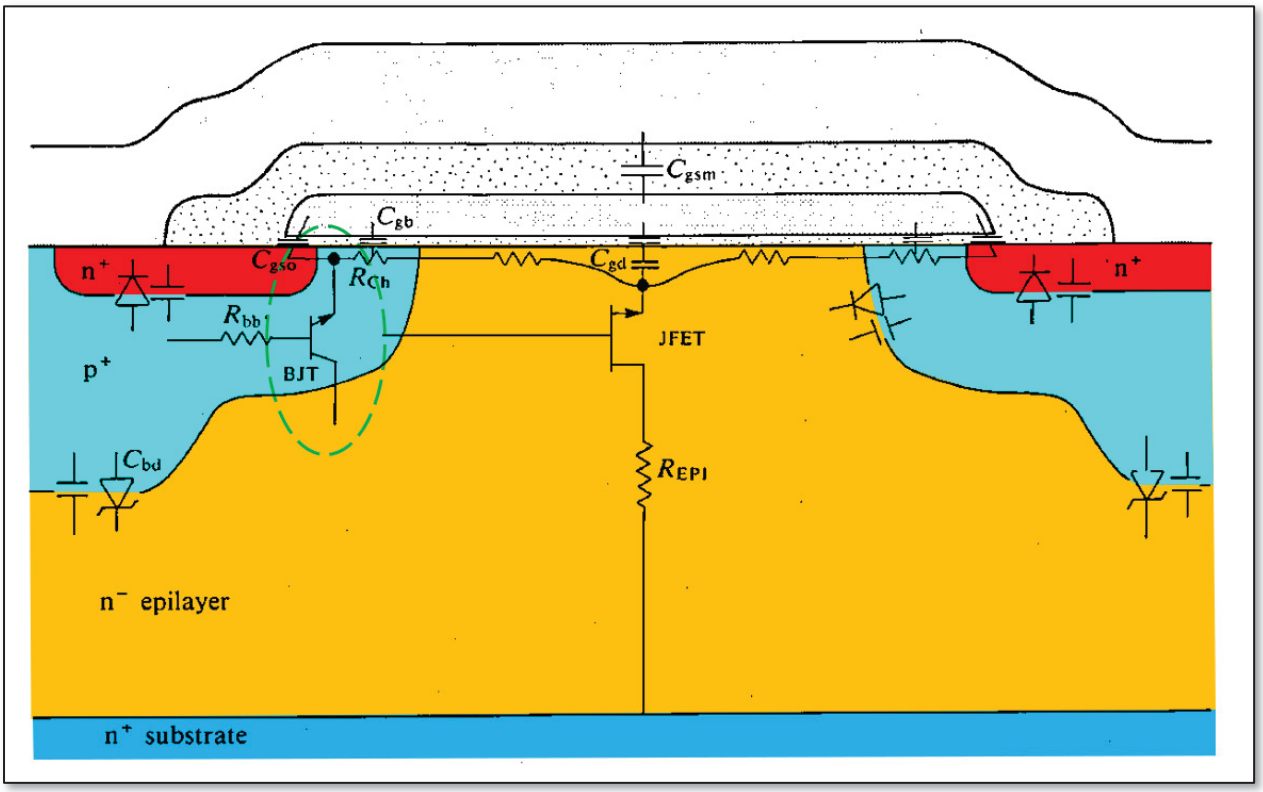
117. Although *Williams* discloses MOSFETs with trench gates and *Ryu* discloses planar gates, a POSITA would nonetheless have been motivated to use *Williams*'s teachings in *Ryu*. This is because *Williams*'s and *Ryu*'s MOSFETs share

many common features to which the shape of the gate is irrelevant. For example, both *Williams*'s trench-gated vertical MOSFETs and *Ryu*'s non-trench-gated vertical MOSFET include a parasitic BJT within the epilayer that could inadvertently be activated. For both *Williams* and *Ryu*, the solution to the potential problem caused by this parasitic transistor is the same. For example, *Williams* describes such a "parasitic NPN bipolar transistor," which it illustrates in Figure 7A (reproduced below). EX1004, 6:9.



EX1004, FIG. 7A (annotated)

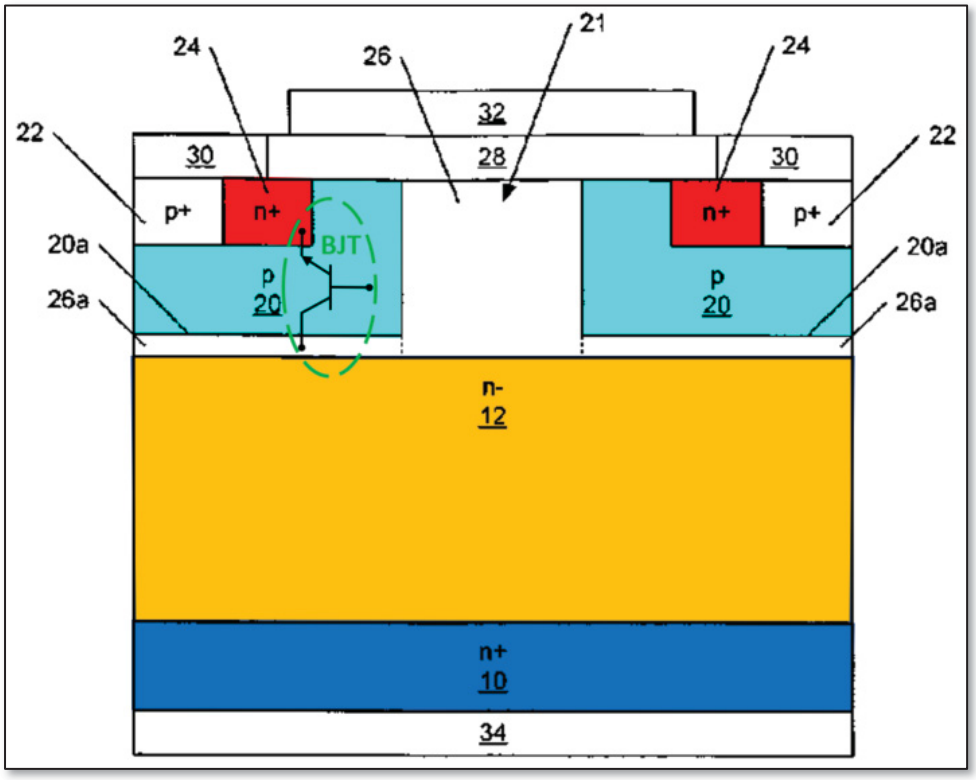
118. *Williams*'s parasitic BJT is formed between the source, the body, and the drain in the same way *Grant* illustrates a parasitic BJT formed between the source, the body, and the drain of a non-trench-gated vertical MOSFET in Figure 3.15, reproduced below.



EX1019, Figure 3.15 (annotated)

119. Based on at least *Grant*'s teachings, a POSITA would have understood that a parasitic npn BJT would also be formed in *Ryu*'s MOSFET between the n+ region 24 (*i.e.*, source region), p-well 20 (*i.e.*, body), and the n-type epitaxial layer

26 (*i.e.*, portion of drain region), as annotated in *Ryu*'s Figure 2A below. *See* EX1003, ¶53.



EX1003, FIG. 2A (annotated)

120. Both *Ryu* and *Williams* prevent activation of the parasitic BJT by shorting the source to the body, via p+ diffusion, using a source electrode. EX1003, Figure 2A (illustrating **source contacts 30** shorting **n+ regions 24** to p-wells 20 via **p+ regions 22**); *see, e.g.*, EX1004, Figure 15D, 15:6–8 ("Metal layer [158] contacts both N+ source region 159 and P+ body contact region 160, thereby shorting the source and body together."). *See also* Section VI.D above. *Williams* further discloses "various source-body designs" in Figures 19A–19F and the need to

maximize the contact of the **P+ body contact regions** to the body region to "suppress parasitic bipolar turn-on, prevent snapback and ruggedize the device." *Id.*, 10:17–18; 16:32–33. A POSITA would have recognized the advantages of using a plurality of **P+ body contact regions** as taught by *Williams*. Lithographically, it has been standard practice to use multiple contact regions rather than one larger contact region, since this simplifies lithographic control and etch uniformity during the fabrication process. As such, when using a longitudinally rectangular structure, disposing a plurality of contact regions on it would have been readily known and obvious to a POSITA; indeed, this has been the most common approach used in the industry. Therefore, a POSITA would have been motivated to use *Williams*'s teachings of multiple and periodic **P+ body contact regions** in *Ryu* to maximize the contact of the p+ regions and ruggedize *Ryu*'s MOSFET against latch up.

121. Furthermore, although *Ryu* is directed to silicon-carbide MOSFETS and *Williams* to silicon MOSFETs, *Baliga* teaches that conventional power MOSFETs, including silicon MOSFETs, "can be readily translated into silicon carbide using known manufacturing techniques." EX1005, 4:22–38. *Ghezzo* also teaches a method of replacing the conventional double-diffusion used in silicon MOSFETs with a double ion implantation sequence for silicon carbide MOSFETs. EX1021, 1:56–63.

122. Accordingly, a POSITA would have understood that the teachings of *Williams* were directly applicable to *Ryu*'s silicon carbide MOSFETs.

123. Implementing *Ryu*'s MOSFET such that *Ryu*'s left **p+ region 22** are defined repeatedly in the left **n+ region 24** as taught by *Williams* would have yielded expected, predictable results. *Ryu* discloses adjacent left **p+ region 22** and left **n+ region 24** disposed within the p-well 20 on the left. EX1003, ¶45, Figure 2A. *Williams* also discloses adjacent N+ source region 12 and a P+ body contact region 13. EX1004, 1:9–10, Figure 1. Additionally, *Williams* discloses a continuous **N+ source region** with **P+ body contact** windows. *Id.*, 10:23–24, Figure 19E. A POSITA would have been motivated to combine the elements taught by *Ryu* and *Williams*—namely, the left **p+ region 22** and left **n+ region 24** as taught by *Ryu*, and the continuous **N+ source region** with **P+ body contact** windows as taught by *Williams*—using known and routine semiconductor fabrication techniques to modify the shape and location of *Ryu*'s left **p+ region 22** and left **n+ region 24** such that the left **p+ region 22** is defined repeatedly in the left **n+ regions 24** because, as *Williams* teaches, such a configuration would help reduce on-resistance, while continuing to provide the needed connection between the **n+ regions 24** and the p-wells 20 via the **p+ regions 22** to ruggedize *Ryu*'s MOSFET against unwanted activation of the parasitic BJT. EX1004, 17:18 ("better N+ contact resistance"); *id,* 6:8–9 ("The

source-to-body short prevents conduction and snapback breakdown of the parasitic NPN bipolar transistor . . .”). This result would have been readily predictable and recognized by a POSITA because, as *Williams* points out, it was well-known that “[t]he primary design goal for a power MOSFET used as a switch is to achieve the lowest on-resistance by simultaneously minimizing each of its resistive constituents.” A POSITA would have been motivated to modify *Ryu*’s p+ regions according to the teachings of *Williams* so as to achieve the lower on-resistance, while maintaining the connection between *Ryu*’s **n+ regions 24** and p-wells 20 via the **p+ regions 22**. EX1004, 1:33–37. As I discussed above in Section VI.C, a lower on-resistance minimizes voltage drop and power dissipation (*i.e.*, power loss), and maximizes the current rating of the MOSFET. *See* EX1019 at 18, 74–75. And as discussed in Section VI.D, connecting the source to the body through p+ regions ruggedizes a MOSFET against unwanted turn on of the parasitic BJT. *See, e.g.*, *id.* at 90, Figure 1.11.

124. A POSITA would have been further motivated to combine the teachings of *Ryu* and *Williams* because it would have been a simple substitution of one known element (adjacent left **p+ region 22** and left **n+ region 24** in *Ryu*) for another (continuous **N+ source region** with **P+ body contact** windows as taught by *Williams*) to obtain predictable results. This substitution would have been readily

achievable by a POSITA via known and routine semiconductor fabrication techniques to form *Ryu*'s adjacent left **p+ region 22** and left **n+ region 24** into a continuous **n+ region 24** with windows of **p+ region 22**.

125. A POSITA would have been further motivated to combine the teachings of *Ryu* and *Williams* because forming *Ryu*'s adjacent left **p+ region 22** and left **n+ region 24** into a continuous **n+ region 24** with windows of **p+ region 22** would have been obvious to try. As *Williams* illustrates in Figures 19A–19F, there were numerous (at least six) known and predictable choices for forming adjacent **N+** and **P+** regions. A POSITA could have pursued these potential solutions with a reasonable expectation of success because the analysis would have simply involved trying each one of these solutions. Thus, it would have been obvious to a POSITA to have formed *Ryu*'s left **p+ region 22** and left **n+ region 24** into a continuous **n+ region 24** with windows of **p+ region 22**, as *Williams* teaches in Figure 19E.

126. The modification of *Ryu*'s left **p+ region 22** and left **n+ region 24** to be in the form of *Williams*'s continuous **N+ source region** with **P+ body contact** windows would have been readily implemented by simply modifying the masks used to form *Ryu*'s left **p+ region 22** and left **n+ region 24**. A POSITA could have implemented this modification using basic semiconductor fabrication techniques to

modify *Ryu*'s masks such that *Ryu*'s left **p+ region 22** and left **n+ region 24** are formed as a continuous **n+ region 24** with windows of **p+ region 22** as taught by *Williams*. This modification would have been well within the knowledge and skillset of a POSITA. Indeed, the '633 patent implicitly confirms this. When the '633 patent discusses the different geometric shapes for the N+/P+ regions in Figures 2, 3 and 4, there is no discussion of special manufacturing steps required, but only the advantages and disadvantages of the shapes themselves.

iv. Reasonable Expectation of Success in Combining Ryu and Williams

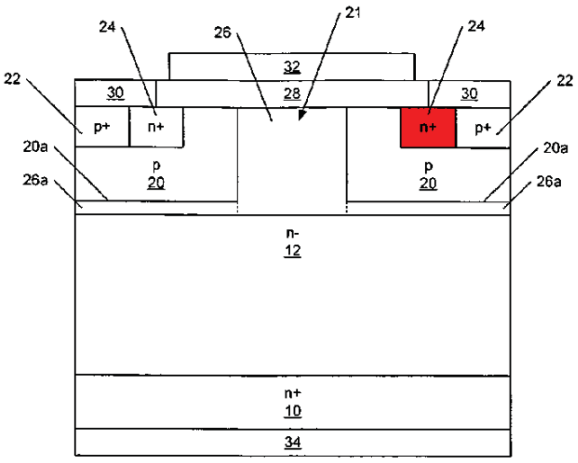
127. A POSITA would also have had a reasonable expectation of success. The combination of *Ryu* and *Williams* represents a straight-forward implementation of steps of the well-understood semiconductor fabrication processes to implement the shape and location of the structures, which a POSITA would have been familiar with and been able to implement, and which *Williams* explains how to accomplish. EX1004, 29:1–19 ("P+ Body Contact Formation"). The reasons a POSITA would have expected success parallel those that provide motivation for this combination—including because both *Ryu* and *Williams* are directed to vertical MOSFETs. EX1003, ¶¶6, 9, 39, Figure 1; EX1004, Abstract, 1:7–8, Figure 1. A POSITA would have had a reasonable expectation of success in modifying *Ryu*'s MOSFET because *Ryu*'s underlying specification was designed to be extensible and flexible. EX1003,

¶¶38 ("This invention may, however, be embodied in many different forms…"), 63, 66. Such modifications were expected to be performed when optimizing the on-resistance and ruggedness of power MOSFETs. *See, e.g.*, EX1004, 16:28–17:19.

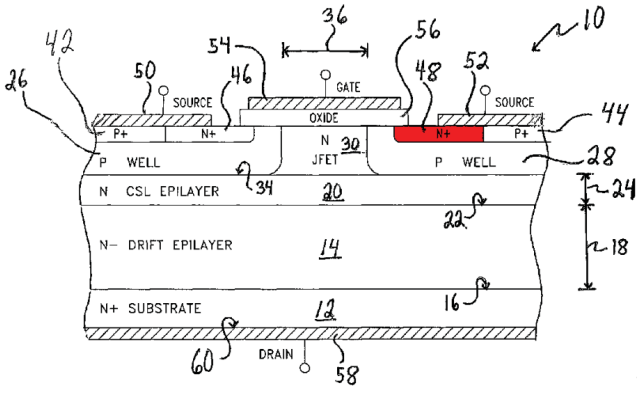
128. Accordingly, *Ryu* in view of *Williams* renders obvious element 9[e] and a POSITA would have been motivated to combine the teachings of these references and would have had a reasonable expectation of success.

(g) 9[f]: "a second source region;"

129. *Ryu* discloses element 9[f]. As I discussed above with respect to element 9[c], *Ryu*'s **n+ regions 24** correspond to the '633 patent's **source regions 46 and 48**. Thus, *Ryu* discloses at least a first n+ region 24 (*i.e.*, "*a first source region*") on the left and a second **n+ region 24** (*i.e.*, "*a second source region*") on the right, for example, as shown in the annotated figures below.



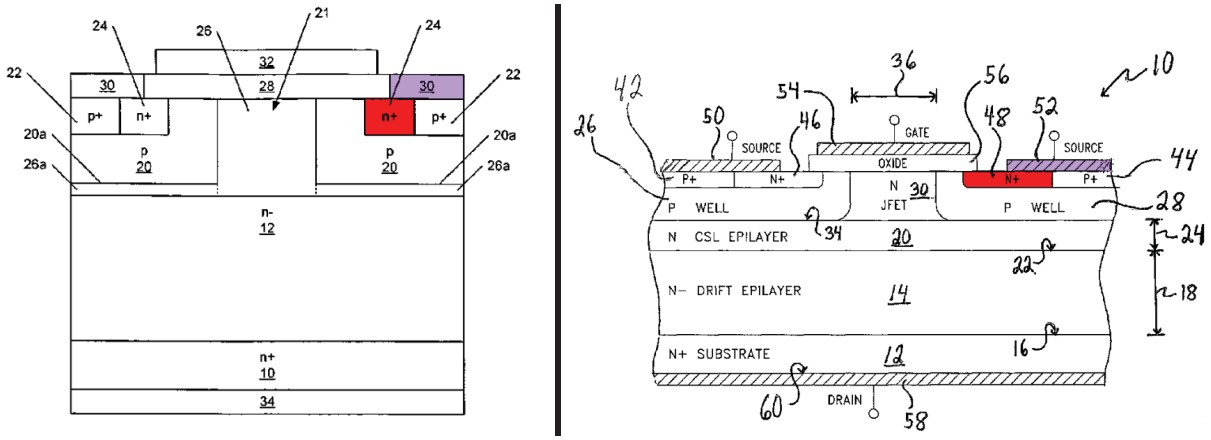
EX1003, FIG. 2A (annotated)



EX1001, FIG. 1 (annotated)

(h) 9[g]: "a second source electrode formed over the second source region, the second source electrode defining a longitudinal axis;"

130. The combination of *Ryu* and *Williams* renders element 9[g] obvious. For the same reasons described for element 9[d], *Ryu* discloses, with respect to Figure 2A (reproduced below, alongside the '633 patent's Figure 1) for example, a second **source contact 30** (*i.e.*, "*a second source electrode*") on the right formed over the right **n+ region 24** (*i.e.*, "*the second source region*"). As further described for element 9[d], a POSITA would have understood that, if fabricated as a linear cell, *Ryu*'s cross-sectional view of its MOSFET would extend perpendicularly to the page, and, therefore, the second **source contact 30** would likewise define a longitudinal axis perpendicular to the page. Also, for the same reasons described for elements 9[d] and 9[e], a POSITA would have found it obvious to implement *Ryu*'s MOSFET using a linear geometry such that the **source contact 30** defines a longitudinal axis.



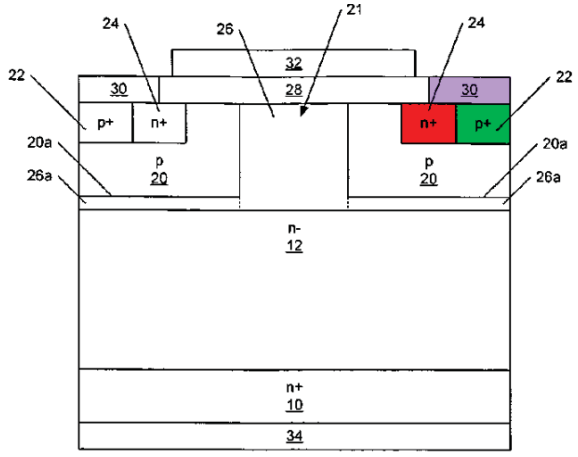
EX1003, FIG. 2A (annotated) | EX1001, FIG. 1 (annotated)

(i) 9[h]: "a plurality of second base contact regions defined in the second source region, each of the plurality of second base contact regions being spaced apart from each other in a direction parallel to the longitudinal axis defined by the second source electrode; and"

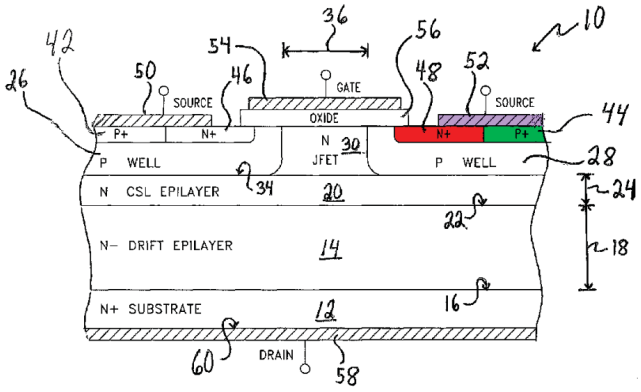
131. For the same reasons described with respect to element 9[e], the combination of *Ryu* and *Williams* renders element 9[h] obvious.

i. "base contact region"

132. As I discussed above with respect to element 9[e], *Ryu*'s **p+ regions 22** correspond to the '633 patent's base contact regions 42 and 44, and the left **p+ region 22** corresponds to a first base contact region. Thus, *Ryu*'s second/right **p+ region 22**, which is adjacent to the right **n+ region 24** (*i.e.*, "*the second source region*"), corresponds to a second base contact region. As also discussed above, a POSITA would have understood that the right **source contact 30** (*i.e.*, "*the second source electrode*") defines a longitudinal axis perpendicular to the page.



EX1003, FIG. 2A (annotated)



EX1001, FIG. 1 (annotated)

ii. "a plurality of second base contact regions defined in the second source region, each of the plurality of second base contact regions being spaced apart from each other in a direction parallel to the longitudinal axis defined by the second source electrode"

133. *Ryu* does not explicitly disclose a plurality of right **p+ regions 22** defined in the right **n+ region 24** and spaced apart from each other in a direction parallel to the longitudinal axis defined by the right **source contact 30**. However, as discussed above with respect to element 9[e], *Williams* discloses "a continuous **N+ source region** with **P+ body contact** 'windows'" in Figure 19E. EX1004, 10:23–24. Using the same rationale as in Sections X.A.1.f.iii and iv, a POSITA would have been motivated to modify *Ryu* in view of *Williams* such that *Ryu*'s right **p+ region 22** is defined repeatedly in the right **n+ region 24**, and the repeated **p+ regions 22** are spaced apart from each other in a direction parallel to the longitudinal

axis defined by the right **source contact 30**, and would have had a reasonable expectation of success in doing so.

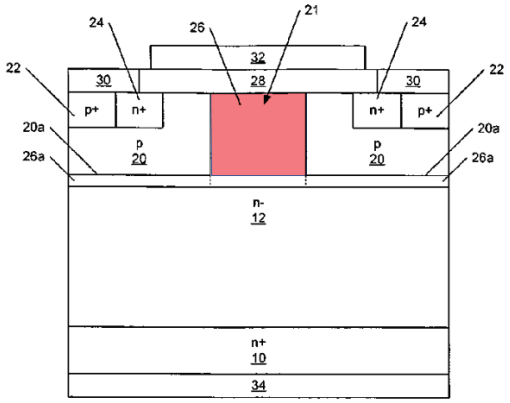
134. Accordingly, *Ryu* in view of *Williams* renders obvious element 9[h].

(j) 9[i]: "a JFET region defined between the first source region and the second source region, the JFET region having a width less than about three micrometers."

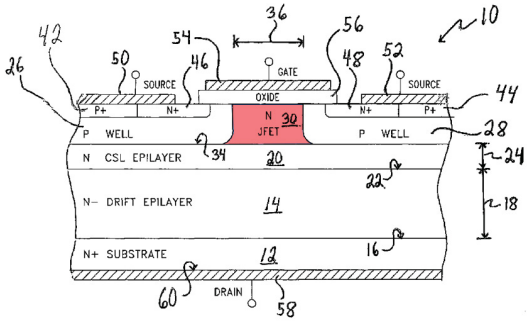
135. *Ryu* discloses element 9[i]. As I will explain below, *Ryu* expressly discloses a "*JFET region.*" *Ryu*'s "JFET region" is defined between the first and second source regions in the same way as in the '633 patent. Moreover, *Ryu*'s "JFET region" is disclosed as having a range of width that substantially overlaps with the range of "*less than about three micrometers*."

i. "a JFET region"

136. *Ryu* expressly discloses that the gap between the p-wells 20 "may be referred to as the **JFET region 21**." EX1003, ¶44; *cf.* EX1001, 6:3–5 ("The remaining region of the additional epitaxial layer between the wells 26, 28 forms the JFET region 30."). *Ryu*'s **JFET region 21** in Figure 2A is shown beside the '633 patent's "JFET region" below, both annotated in salmon.



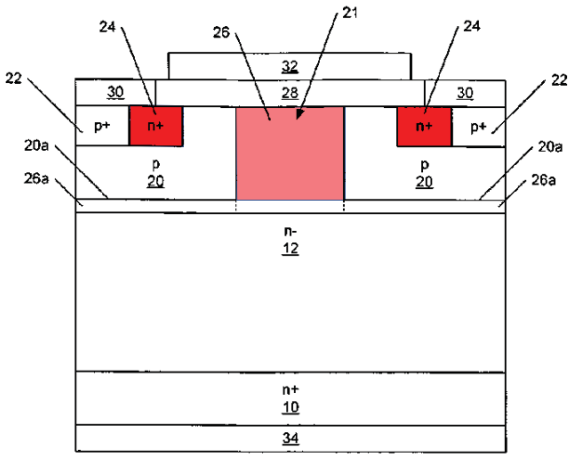
EX1003, FIG. 2A (annotated)



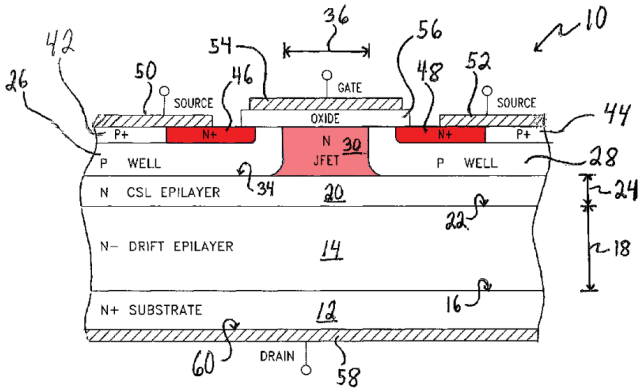
EX1001, FIG. 1 (annotated)

ii. "defined between the first source region and the second source region"

137. *Ryu*'s **n+ regions 24** (*i.e.*, the "*first source region*" and "*second source region*") are disposed within p-wells 20. And *Ryu* states that "the region [between the p-wells 20] may be referred to as the JFET region 21." EX1003, ¶44. The **JFET region 21** is as illustrated in Figure 2A, for example. As such, *Ryu* discloses that the **JFET region 21** is between the first and second source regions. Also, as shown below, *Ryu*'s arrangement is identical to that shown in the '633 patent, where both structures include a portion of each p-well between the JFET region and each source region disposed within each respective p-well. Accordingly, *Ryu*'s **JFET region 21** is "*defined between the first source region and the second source region*" in the same way as the '633 patent's JFET region.



EX1003, FIG. 2A (annotated)



EX1001, FIG. 1 (annotated)

iii. "the JFET region having a width less than about three micrometers"

138. *Ryu* discloses that "if the gap [between the p-wells 20] is too narrow, the resistance of the **JFET region 21** may become very high," and thus "gaps of from about 1 μm to about 10 μm are preferred." EX1003, ¶44. Thus, *Ryu* discloses that the **JFET region 21** may have a width of less than about three micrometers because the recited width of "less than about three micrometers" is disclosed with sufficient specificity by *Ryu*'s disclosure of a JFET width "from about 1 [micrometer] to about 10 [micrometers]."

139. Therefore, *Ryu* in view of *Williams* renders claim 9 obvious.

2. Dependent Claim 10

> **"The double-implanted metal-oxide semiconductor field-effect transistor of claim 9, wherein the JFET region has a width of about one micrometer."**

140. *Ryu* in view of *Williams* renders obvious "*[t]he double-implanted metal-oxide semiconductor field-effect transistor of claim 9*," as discussed above. *Ryu* discloses "*wherein the JFET region has a width of about one micrometer.*" For example, *Ryu* discloses that "if the gap [between the p-wells 20] is too narrow, the resistance of the **JFET region 21** may become very high," and thus "gaps of from about 1 μm to about 10 μm are preferred." EX1003, ¶44. Therefore, *Ryu* discloses the **JFET region 21** may have a width of about one micrometer.

141. Thus, *Ryu* in view of *Williams* renders claim 10 obvious.

3. Dependent Claim 11

> **"The double-implanted metal-oxide semiconductor field-effect transistor of claim 9, wherein the JFET region has a first concentration of first type impurities and the drift semiconductor layer has a second concentration of first type impurities, the first concentration of first type impurities being greater than the second concentration of first type impurities."**

142. *Ryu* in view of *Williams* renders obvious "*[t]he double-implanted metal-oxide semiconductor field-effect transistor of claim 9*," as discussed above. *Ryu* discloses "*wherein the JFET region has a first concentration of first type impurities and the drift semiconductor layer has a second concentration of first type*

impurities, the first concentration of first type impurities being greater than the second concentration of first type impurities." For example, *Ryu* expressly discloses that "the gap 21 [(*i.e.*, the **JFET region 21**)] between the p-wells 20 has a higher carrier concentration than the drift layer 12." EX1003, ¶42. Indeed, because the **JFET region 21** is the gap that remains in region 26 after the p-wells 20 are formed, the **JFET region 21** has the dopant type and concentration of region 26—n-type impurities (*i.e.*, "*first type impurities*") at a concentration of "about 10^{15} to about 5×10^{17} cm^{-3}" (*i.e.*, "*a first concentration*"). EX1003, ¶41. And the **drift layer 12** is doped to an "n−" (*i.e.*, also n-type, "*first type impurities*") concentration of "about 10^{14} to about 5×10^{16} cm^{-3}" (*i.e.*, "*a second concentration*"). *Id.*, ¶40. *Ryu* expressly explains that "[t]he region 26 ***has a higher carrier concentration*** than the carrier concentration of the **drift layer 12** . . . " *Id.*, ¶41. Relatedly, as I discussed in Section VI.C, *Grant* teaches that "[i]ncreasing the donor doping concentration in the drain throats [(*i.e.*, the JFET regions)] . . . has two beneficial effects"—"the cell size can be reduced and . . . lower $R_{DS(on)}$ can be realized." EX1019, 83–84. Thus, a POSITA would have been motivated by such a teaching to make the doping concentration of the JFET region greater than that of the drift region in the epilayer. Accordingly, because *Ryu*'s **JFET region 21** can have a "*first concentration*" that is an order of magnitude, or more, greater than the "*second concentration*" of **drift layer 12**, *Ryu*

discloses "*the first concentration of first type impurities being greater than the second concentration of first type impurities.*"

***Ryu* structure**	**Concentration (cm^{-3})**	**EX1003 cite**
JFET region 21	About 10^{15} to about 5×10^{17} ("*first concentration*")	¶41
Drift layer 12	About 10^{14} to about 5×10^{16} ("*second concentration*")	¶40

143. Thus, *Ryu* in view of *Williams* renders claim 11 obvious.

XI. AVAILABILITY FOR CROSS EXAMINATION

144. In signing this declaration, I recognize that the declaration will be filed as evidence in a contested case before the Patent Trial and Appeal Board of the United States Patent and Trademark Office. I also recognize that I may be subject to cross examination in the case and that cross examination will take place within the United States. If cross examination is required of me, I will appear for cross examination within the United States during the time allotted for cross examination.

XII. RIGHT TO SUPPLEMENT

145. I reserve the right to supplement my opinions in the future to respond to any arguments that the Patent Owner raises and to take into account new information as it becomes available to me.

XIII. JURAT

146. I declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code.

Dated: December _6th____, 2021

Vivek Subramanian

Vivek Subramanian

EXHIBIT A

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Education

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Ph.D. in Electrical Engineering, Stanford University
Stanford, California
Honors earned: Graduate Fellowship, Eastman Kodak Company

9 / 94 - 3 / 96

MS in Electrical Engineering, Stanford University
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8 / 90 - 5 / 94

BS in Electrical Engineering, Louisiana State University
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Honors earned: Summa cum laude, College Honors, Outstanding Senior, Junior and Sophomore, Honors College

Professional Experience

2018 - present

École polytechnique fédérale de Lausanne
Switzerland

8/18 – present: Professor of Microengineering

2000 - present

Department of Electrical Engineering & Computer Sciences, University of California
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7/20 to date: Adjunct Professor
7/18 – 6/20: Chancellor's Professor
7/11 – 6/20: Professor
7/05 – 7/11: Associate Professor
7/00-7/05: Assistant Professor
Research, teaching and service in EECS Department
Honors Earned:

2015 IEEE Kiyo Tomiyasu Award
Best in session and best in track awards, 2013 IMAPS Microelectronics Conference
Outstanding paper award, 2012 IMAPS Microelectronics Conference
2008 Printed Electronics Champion, Printed Electronics USA Conference, November 2008
Outstanding Teaching Award, EECS Department, UC Berkeley, 2005
Best paper award, 2004 IEEE Device Research Conference
Nominated to MIT's Technology Review top 100 young innovators list (TR100), 2002
National Science Foundation Young Investigator (CAREER) Award, FY2002,
Nominated to National Academy of Engineering's *Frontiers of Engineering*, 2002
Winner of 2002 Paul Rappaport Award for best paper in an IEEE EDS Journal

2009 - present

Adjunct Professor, Sunchon National University
Sunchon, Korea
2013 to date: Adjunct Professor, BK21 Program
2009-2013: Adjunct Professor and Principal Investigator, WCU Program
Initiated, managed, and contributed to large multinational research program focused on printed electronics, including displays, energy devices, and RFID

2000 - present

Independent Consultant
Orinda, CA
Consultant to the semiconductor industry and its associated fields in the following areas:

Memory technology and design, Silicon Process Technology
Display / Imager and Flexible Electronics Technology, RFID Technology
Intellectual Property Consulting
Technology Evaluation / Venture Capital due diligence

2014- present

Founder and CTO, Locix Inc.
San Bruno, CA
Senior leadership role in venture-funded startup company working on wireless networking

2004 – 2013 **Founding Scientific Advisor, Kovio, Inc.**
Sunnyvale, CA
Scientific advising to printed electronics startup company

2008 - 2011 **Chief Technical Advisor, QuSwami, Inc.**
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Scientific advising to energy conversion device startup company
Served as CTO from July 2010-June 2011

1998 - 2000 **Consulting Assistant Professor, Electrical Engineering Department, Stanford University.**
Stanford, CA
Advisory role for research group of Prof. Krishna C. Saraswat

1998-2000 **Visiting Research Engineer, Electrical Engineering Department, University of California.**
Berkeley, CA
Research into 25nm MOSFET technologies for giga-scale integration

1998 - 2000 **Founder, Matrix Semiconductor, Inc.**
Santa Clara, CA
Co-founder and technical advisor of startup company working on high-density memory technology
Honors Earned:
Nominated to Scientific American's SA50 List for Visionary Technology
Finalist for 2003 World Technology Award for Information Technology Hardware
Winner, 2005 EDN Innovation Award

1998 **Co-instructor, Electrical Engineering Department, Stanford University.**
Stanford, CA
Co-teaching of EE311, Advanced Integrated Circuit Fabrication Processes

1997 **Intern, Advanced Product Research and Development Laboratory, Motorola Inc.**
Austin, TX
Research into process development issues affecting SiGe SEMFET devices

1996 **Head Teaching Assistant EE410: IC Fabrication Laboratory, Stanford University**
Stanford, CA
Coordination and instruction of EE410, graduate level laboratory course.

1994-1998 **Research Assistant, Electrical Engineering, Stanford University**
Stanford, CA
Research into crystallization of amorphous Si and SiGe films using low thermal budget processes.

Professional Affiliations and Activities

Technical Program Committee, IEEE Electronic Components and Technology Conference, 2014 to 2016
Chair, Scientific Advisory Board, iPACK, Royal Institute of Technology (KTH), Sweden, 2011 to 2016
Tampere Institute of Technology Faculty Search Committee, Finland, 2013
University of Oulu Faculty Search Committee, Finland, 2013
Served as external thesis committee member for several universities world-wide, including University of Cape Town (South Africa), Tampere Institute of Technology (Finland), Technical University of Eindhoven (Netherlands), Indian Institute of Science (India), Indian Institute of Technology (India), 2009 to date
Associate Editor, IEEE Journal of Display Technology, 2008 to date
Technical Program Chair, Large Area, Organic, and Printed Electronics Conference, 2012-2013
Scientific Committee, Large Area, Organic, and Printed Electronics Conference, 2009-2011
Scientific Committee, International Conference on Printed and Flexible Elecronics, 2009-2013
IEEE Electron Devices Society Organic Electronics Committee, 2003 - 2005
Executive Committee, International Electron Device Meeting, 2003 to 2009
Technical Program Committee, International Electron Device Meeting, 2001-2002
Technical Program Committee member, Device Research Conference, 2000-2002
Technical Program Committee member, VLSI-TSA Conference, 2005
Member, Institute of Electrical and Electronic Engineers

List of Patents, Publications and Presentations

Patents

1. “Systems and methods for using ranging to determine locations of wireless sensor nodes based on radio frequency communications between the nodes and various RF-enabled devices”, T. Ylamurto, M. Seth, L. Kong, V. Subramanian, US Patent 10,551,479
2. “Systems and methods for providing communications within wireless sensor networks based on a periodic beacon signal”, T. Ylamurto, V, Pavate, E. Alon, V. Subramanian, US Patent 10,536,901
3. “Systems and methods for using radio frequency signals and sensors to monitor environments”, T. Bakhishev, V. Subramanian, V. Pavate T. Ylamurto, US Patent 10,514,704.
4. “Systems and methods for using radio frequency signals and sensors to monitor environments”, T. Bakhishev, V. Subramanian, V. Pavate T. Ylamurto, US Patent 10,504,364
5. “Systems and methods for coarse and fine time of flight estimates for precise radio frequency localization in the presence of multiple communication paths”, M. Seth, L. Kong, T. Ylamurto, V. Subramanian, US Patent 10,470,156
6. “Methods and apparatus for monitoring wound healing using impedance spectroscopy”, M. Maharbiz, V. Subramanian, A. C. Arias, S. Swisher, A. Liao, M. Lin, F. Pavinatto, Y. Khan, D. Cohen, E. Leeflang, S. Roy, M. Harrison, D. Young, US Patent 10,463,293
7. “Systems and methods for using radio frequency signals and sensors to monitor environments”, T. Bakhishev, V. Subramanian, V. Pavate T. Ylamurto, US Patent 10,156,852.
8. “Systems and methods for determining locations of wireless sensor nodes in a tree network architecture having mesh-based features”, L. Kong, T. Bakhishev, T. Ylamurto, V. Subramanian, M. Seth, US Patent 10,104,508.
9. “Systems and methods for providing wireless asymmetric network architectures of wireless devices with power management features”, V. Subramanian, E. Alon, V. Pavate, US Patent 10,028,220.
10. “Random delay generation for thin-film transistor based circuits”, V Subramanian, M Mao, Z Wang, US Patent 9,985,664
11. “Systems and methods for determining locations of wireless sensor nodes in a network architecture having mesh-based features for localization”, L. Kong, T. Bakhishev, T. Ylamurto, V. Subramanian, M. Seth, US Patent 9,846,220
12. “Systems and methods for determining locations of wireless sensor nodes in a tree network architecture having mesh-based features”, L. Kong, T. Bakhishev, T. Ylamurto, V. Subramanian, M. Seth, US Patent 9,763,054
13. “Through silicon vias and thermocompression bonding using inkjet-printed nanoparticles”, V. Subramanian and J. Sadie, US Patent 9,717,145
14. “Systems and methods for providing wireless asymmetric network architectures of wireless devices with anti-collision features”, V. Subramanian, E. Alon, V. Pavate, US Patent 9,706,489
15. “Systems and methods for determining locations of wireless sensor nodes in an asymmetric network architecture”, V. Subramanian, E. Alon, V. Pavate, US Patent 9,529,076
16. “Systems and methods for providing wireless sensor networks with an asymmetric network architecture”, V. Subramanian, E. Alon, V. Pavate, US Patent 9,380,531
17. “Transparent metal oxide nanoparticle compositions, methods of manufacture thereof and articles comprising the same”, V. Subramanian, S. K. Volkman, US Patent 9,343,202
18. “Three-dimensional nonvolatile memory and method of fabrication”, M. G. Johnson, T. H. Lee, V. Subramanian, P. M. Farmwald, J. M. Cleeves, US Patent 9,214,243
19. “Dense arrays and charge storage devices”, T. H. Lee, V. Subramanian, J. M. Cleeves, I. G. Kouznetsov, M. G. Johnson, P. M. Farmwald, US Patent 9,171,857
20. “Print compatible designs and layout schemes for printed electronics”, Z. Wang, V. Subramanian, L. Cleveland, US Patent 9,155,202
21. “Wireless devices including printed integrated circuitry and methods for manufacturing and using the same”, P. Smith, C. Choi, V. Pavate, J. M. Cleeves, V. Subramanian, R. Young, V. Biviano, US Patent 9,004,366.

22. “Dense arrays and charge storage devices “, T. H. Lee, V. Subramanian, J. M. Cleeves, M. G. Johnson, P. M. Farmwald, I. Kouznetzov, US Patent, 8,981,457.
23. “High reliability surveillance and/or identification tag/devices and methods of making and using the same”, V. Subramanian, P. Smith, V. Pavate, A. Kamath, C. Choi, A. Chandra, J. M. Cleeves, US Patent, 8,933,806.
24. “Surveillance devices with multiple capacitors”, P. Smith, C. Choi, J. M. Cleeves, V. Subramanian, A. Kamath, S. Molesa, US Patent, 8,912,890.
25. “Pillar-shaped nonvolatile memory and method of fabrication”, M. G. Johnson, T. H. Lee, V. Subramanian, P. M. Farmwald, J. M. Cleeeves, US Patent 8,897,056
26. “Dense arrays and charge storage devices”, T. H. Lee, V. Subramanian, J. M. Cleeves, I. G. Kouznetsov, M. G. Johnson, P. M. Farmwald, US Patent 8,853,765
27. “Dense arrays and charge storage devices”, T. H. Lee, V. Subramanian, J. M. Cleeves, I. G. Kouznetsov, M. G. Johnson, P. M. Farmwald, US Patent 8,823,076
28. “Random delay generation for thin-film transistor based circuits”, V. Subramanian, M. Mao, Z. Wang, US Patent 8,810,298
29. “Vertically stacked field programmable nonvolatile memory and method of fabrication”, M. Johnson, T. Lee, V. Subramanian, M. Farmwald, and J. M. Cleeves, US Patent 8,503,215
30. “Process-variation tolerant series-connected NMOS and PMOS diodes, and standard cells, tags, and sensors containing the same”, V. Subramanian, P. Smith, US Patent 8,471,308
31. “Printed compatible designs and layout schemes for printed electronics”, Z. Wang, V. Subramanian, L. Cleveland, US Patent 8,383,952
32. “Method for making surveillance devices with multiple capacitors”, P. Smith, C. Choi, J. M. Cleeves, V. Subramanian, A. Kamath, S. Molesa, US Patent 8,296,943
33. “High reliability surveillance and/or identification tag/devices and methods of making and using the same”, V. Subramanian, P. Smith, V. Pavate, A. Kamath, C. Choi, A. Chandra, and J. M. Cleeves, US Patent 8,264,359
34. “High reliability surveillance and/or identification tag/devices and methods of making and using the same”, V. Subramanian, P. Smith, V. Pavate, A. Kamath, C. Choi, A. Chandra, and J. M. Cleeves, US Patent 8,227,320
35. “Vertically stacked field programmable nonvolatile memory and method of fabrication”, M. Johnson, T. Lee, V. Subramanian, M. Farmwald, and J. M. Cleeves, US Patent 8208282
36. “Reliable tag deactivation”,J. M. Cleeves, V. Subramanian, US Patent 8138921
37. “Combined static and dynamic frequency divider chains using thin film transistors”, V. Subramanian, US Patent 8085068
38. “Process-variation tolerant diode, standard cells including the same, tags and sensors containing the same, and methods for manufacturing the same”, V. Subramanian, P. Smith, US Patent 7932537
39. “Three terminal nonvolatile memory Device with vertical gated diode”, T. H. Lee, V. Subramanian, J. M. Cleeves, M. G. Johnson, P. M. Farmwald, I. G. Kouznetsov, US Patent 7825455
40. “Vertically stacked field programmable nonvolatile memory and method of fabrication”, V. Subramanian, J. M. Cleeves, US Patent 7816189
41. “Multi-mode tags and methods of making and using the same”, P. Smith, J. M. Cleeves, V. Pavate, V. Subramanian, US Patent 7750792
42. “Method of manufacturing complementary diodes”, V. Subramanian, P. Smith, US Patent 7528017
43. “Vertically stacked field programmable nonvolatile memory and method of fabrication”, V. Subramanian, J. M. Cleeves, US Patent 7319053
44. “Vertically stacked field programmable nonvolatile memory and method of fabrication”, V. Subramanian, J. M. Cleeves, US Patent 7265000
45. “Vertically stacked field programmable nonvolatile memory and method of fabrication”, V. Subramanian, J. M. Cleeves, US Patent 7160761
46. “Vertically stacked field programmable nonvolatile memory and method of fabrication”, V. Subramanian, J. M. Cleeves, US Patent 7157314

47. “Dense arrays and charge storage devices”, T. H. Lee, V. Subramanian, J. M. Cleeves, A. J. Walker, C. Petti, I. Kouznetzov, M. G. Johnson, P. M. Farmwald. B. Herner, US Patent 7129538

48. “Patterning three dimensional structures”, C. K. Li, J. N. Knall, M. A. Vyvoda, J. M. Cleeves, V. Subramanian, US Patent 7071565

49. “Monolithic three dimensional array of charge storage devices containing a planarized layer”, T. H. Lee, V. Subramanian, J. M. Cleeves, A. J. Walker, C. J. Petti, I. G. Kouznetzov, M. G. Johnson, P. M. Farmwald, and B. Herner, US Patent 6881994

50. “Thermal processing for three dimensional circuits”, V. Subramanian, J. M. Cleeves, J. N. Knall, C. K. Li, and M. A. Vyvoda, US Patent 6,770,939

51. “Vertically stacked field programmable nonvolatile memory and method of fabrication”, M. G. Johnson, T. H. Lee, V. Subramanian, and P. M. Farmwald, US Patent 6780711

52. “Multigate semiconductor device with vertical channel current and method of fabrication”, J. M. Cleeves and V. Subramanian, US Patent 6677204

53. “Thermal processing for three dimensional circuits”, V. Subramanian, J. M. Cleeves, J. N. Knall, C. K. Li, and M. A. Vyvoda, US Patent 6624011

54. “Multigate semiconductor device with vertical channel current and method of fabrication”, J. M. Cleeves and V. Subramanian, US Patent 6580124

55. “Patterning three dimensional structures”, C. K. Li, J. N. Knall, M. A. Vyvoda, J. M. Cleeves, and V. Subramanian, US Patent 6627530

56. “Low cost three-dimensional memory array”, M. Johnson, T. Lee, V. Subramanian, P. Farmwald, J. Knall, US Patent 6515888

57. “Integrated circuit structure including three-dimensional memory array”, M. Johnson, T. Lee, V. Subramanian, P. M. Farmwald, J. M. Cleeves, US Patent 6385074.

58. “FINFET transistor structures having double gate channel extending vertically from a substrate and methods of manufacture”, C. Hu, T-J. King, V. Subramanian, L. Chang, X. Huang, Y-K. Choi, J. T. Kedzierski, N. Lindert, J. Bokor, W-C. Lee, US Patent 6413802

59. “Vertically stacked field programmable nonvolatile memory and method of fabrication”, M. Johnson, T. Lee, V. Subramanian, M. Farmwald, and J. M. Cleeves, US Patent 6185122.

60. “Vertically Stacked Field Programmable Nonvolatile Memory and Method of Fabrication”, M. Johnson, T. Lee, V. Subramanian, M. Farmwald, and J. M. Cleeves, US Patent 6034882.

61. “Vertically Stacked Field Programmable Nonvolatile Memory and Method of Fabrication”, M. Johnson, T. Lee, V. Subramanian, M. Farmwald, and J. M. Cleeves, US Patent 6351406.

62. “Vertically Stacked Field Programmable Nonvolatile Memory and Method of Fabrication”, M. Johnson, T. Lee, V. Subramanian, M. Farmwald, and J. M. Cleeves, US Patent 6483736.

Invited Magazine Articles, Books, Chapters, and Monographs

1. Chapter in “Inkjet Technology for Digital Fabrication”, Editors: Ian M. Hutchings, Graham D. Martin, Wiley, ISBN: 978-0470681985

2. Chapter in “Applications of Organic and Printed Electronics: A Technology-Enabled Revolution (Integrated Circuits and Systems), Editor: E. Cantatore, ISB: 978-1-461-43159-6

3. Chapter in “Inkjet-based Micromanufacturing”, Editors: Korvink, Smith, Shin, Wiley, ISBN: 978-3-527-31904-6

4. Chapter in “Organic Electronics II. More Materials and Applications", Editor: H. Klauk, Wiley, ISBN: 978-3-527-32647-1

5. Chapter in “Transparent Electronics: From Synthesis to Applications”, Editors: A. Facchetti and T. Marks, Wiley, ISBN: 978-0-470-99077-3, 2010.

6. Chapter in “The chemistry of inkjet inks”, Editor: S. Magdassi, World Scientific Publishing Company, ISBN: 978-9812818218, 2009

7. Chapter in "Organic Field-Effect Transistors", Editors: Z. Bao, and J. Locklin, CRC Press, ISBN: 978-0849380808, 2007
8. "Developments in printed RFID", V. Subramanian, Pira Publishing, UK, 2006.
9. "3D Chips: Future Possibilities", V. Subramanian, Silicon India, Feb 2003, pp. 24-25

Invited Conference Presentations

1. ***Invited,*** "Materials, Process, and Device Innovations for High-Performance Printed Electronics", PRINSE'18 – The 5th Printed Intelligence Industry Seminar on Manufacturing Solutions for Customer Needs and Vision to the Future, Oulu, Finland, Jan 31-Feb 1, 2018.
2. ***Invited¸*** "Highly scaled gravure printed organic transistors for high-performance printed organic electronics", High-frequency printed and direct-written organic-hybrid integrated circuits (HEROIC) Workshop, Milan, Italy, Nov 8-10, 2017.
3. ***Keynote,*** "Printed Electronics: Innovations in Materials, Processes, and Devices", Association of International Metallizers, Coaters, and Laminators (AIMCAL) R2R Conference USA 2017, Tampa, FL, Oct-15-18, 2017.
4. ***Invited,*** "High-performance gravure printed organic transistors", 2017 European Materials Research Society Meeting, Strasbourg, France, May 22-26, 2017
5. ***Invited,*** "Printed Electronics: Innovations in Materials, Processes, and Devices", 2017 International Thin Film Transistor Conference (ITC 2017), Austin, TX, February 23-24, 2017.
6. ***Invited,*** "High-speed Printing of Transistors: From Inks to Devices", 2016 International Society of Coating Science and Technology Symposium (ISCST), Pittsburgh, PA, September 18-21, 2016.
7. ***Keynote***, "Printed Electronics: Innovations in Materials, Processes, and Devices", 2016 Canadian Printable Flexible Wearable electronics Symposium (CPES2016), April 19-20, Oakville, Canada
8. ***Keynote***, "Printed Electronics: Innovations in Materials, Processes, and Device", 2016 Society of Vacuum Coaters Techcon, Indianapolis, IN, May 10-13, 2016.
9. ***Invited***, Subramanian, Vivek, Chung, Seungjun, Grau, Gerd and Scheideler, William J., "71-2: Invited Paper: Printed Transistors and MEMS for Large-Area Electronics", 2016 Society for Information Display Symposium, San Francisco, May 20-27, 2016.
10. ***Keynote,*** "Printed Electronics: Innovations in Materials, Processes, and Devices", 31st Philippine Chemistry Congress, Iloilo, Philippines, April 13-15, 2016.
11. ***Keynote,*** "Advanced Processes, Materials, and Devices for Emerging Printed Electronics Applications", 3rd Swiss Conference on Printed Electronics and Functional Materials, Neuchatel, Switzerland, Oct 1-2, 2015.
12. ***Invited,*** "High-performance printed organic transistors: Materials, processes, and devices", V. Subramanian, G. Grau, H. Kang, and R. Kitsomboonloha, 2015 American Chemical Society National Meeting and Exposition, Boston, MA, Aug 17th, 2015.
13. ***Invited***, Subramanian, Vivek, Jaewon Jang, William Scheideler, and Sarah Swisher. "39.1: Invited Paper: Printed Inorganic Transistors Based on Transparent Oxides." In SID Symposium Digest of Technical Papers, vol. 46, no. 1, pp. 587-590. 2015.
14. ***Plenary,*** "Printed Electronics: Advanced Technologies Enabling New Applications", 2015 Flexible and Printed Electronics Conference, Monterey, CA, February 23-26, 2015.
15. ***Invited***, "High-resolution gravure printing of organic thin film transistors for high-performance printed electronic systems", V. Subramanian, R. Kitsomboonloha, J. Cen, H. Kang, G. Grau, and W. J. Scheideler, Materials Research Society Fall Meeting, Boston, MA, Dec 3, 2014.
16. ***Invited,*** "Advanced printed electronics technologies for novel ubiquitous human interactive systems", 2014 CMOS Emerging Technologies Research Symposium, Grenoble, France, July 6-8, 2014.
17. ***Invited,*** "Printed Electronics: A pathway to functionally-rich systems", 64th annual IEEE Electronic Components and Technology Conference, Orland, FL, May 27, 2014.
18. ***Invited***, "Printed Electronics: The Confluence of Printing and Semiconductors", Canadian Printed Electronics Symposium, Montreal, Canada, April 9, 2013.

19. ***Invited "***Modeling, scaling, and integration of gravure printing for fast switching Organic FETs", V. Subramanian, S. J. S. Morris, H. Kang, Materials Research Society Fall 2012 Meeting, Boston, MA, Nov 25-30, 2012

20. ***Invited***, "Printed Nanoparticles as routes to high-performance printed conductors: Synthesis, Printing Processes, and Device Applications", V. Subramanian, H. Kang, R. Kitsomboonloha, and S. K. Volkman, The 2012 International Conference on Flexible and Printed Electronics ICFPE2012, Tokyo, Japan, September 6th - 8th, 2012

21. ***Invited*** "Advanced Printing Processes for High-Performance Printed Transistors", V. Subramanian, Flextech Workshop on Printing Electronics - Ink and Substrate Interactions, Kalamazoo, MI, August 1-2, 2012

22. ***Invited*** "High-performance Printed Transistors: Materials, Processes, and Devices", V. Subramanian, 2nd CPEM International Symposium "Organic Semiconductors and Printed Electronics", Gyeonggi, South Korea, May 10th, 2012.

23. ***Invited*** "Highly-Scaled Gravure and Inkjet Printed Organic Transistors: Tools, Processes, and Devices", Hongki Kang & Vivek Subramanian, 2012 Flextech Flexible Electronics and Display Conference, Phoenix, AZ, Feb 5-9, 2012.

24. ***Plenary*** "Nanomaterials for printed electronics: synthesis, design, and applications", V. Subramanian, International Conference on Nano Science and Nano Technology, Sunchon, Korea, November 11th, 2011.

25. ***Invited*** "Advances in scaling of printed transistors", V. Subramanian, International Seminar on Printed Electronics, Seoul, Korea, June 8th, 2011.

26. ***Invited*** "High-Performance Fully Printed Transistors: Materials, Processes, and Device Characteristics", V. Subramanian, H. Tseng, R. Kitsomboonloha, and A. de la Fuente Vornbrock, 2011 Electrochemical Society Meeting, Montreal, Canada, May 2011

27. ***Invited*** "From Droplets to Devices: Printed Transistor Processes, Integration, and Characteristics", Vivek Subramanian, Daniel Soltman, Huai-Yuan Tseng, Rungrot Kitsomboonloha and Alejandro de la Fuente Vornbrock, Materials Research Society Spring Meeting, San Francisco, CA, April 2011

28. ***Keynote*** "Printed electronics: Innovations in tools, materials, devices, and applications", V. Subramanian, 2011 Korea Printed Electronics Association (KoPeA) meeting, Seoul, Korea, March 2011

29. ***Keynote*** "Printed RF tags and sensors: the confluence of printing and semiconductors", V. Subramanian, F. Liao, and H-Y. Tseng, The European Microwave Integrated Circuits Conference 2010, Paris, France, September 2010.

30. ***Invited*** "Droplet-on-demand direct patterning of active materials: materials, modeling, and integration", V. Subramanian, The 2010 IEEE Lithography Workshop, Kuai, Hawaii, November 2010

31. ***Plenary*** "Printed electronics: where are we, and where are we going", V. Subramanian, 2010 Large Area Organic, and Printed Electronics Convention (LOPE-C), Frankfurt, Germany, June 2010.

32. ***Keynote*** "Printed RFID: Technology Trends and Outlook", V. Subramanian, IEEE International Conference on RFID 2010, Orlando, Florida, April 2010.

33. ***Invited*** "Mechanistic studies on sintering of nanoparticles for formation of solution-processed thin films", 2010 Spring meeting of the Materials Research Society, San Francisco, CA, April 2010.

34. ***Invited*** "Printed Electronics: the confluence of printing and semiconductors", Vivek Subramanian, 2009 International Conference on Flexible and Printing Electronics, Jeju Island, Korea, Nov 2009.

35. ***Invited*** "Organic Transistor Vapor and Biosensors – Technology Status and Implementation Issues", Vivek Subramanian, Frank Liao, Lakshmi Jagannathan, Electrochemical Society Meeting, Vienna, Austria, October 2009.

36. ***Invited*** "Printed transistors for low-cost electronics: the confluence of printing and printable electronic materials", Vivek Subramanian, Alejandro de la Fuente Vornbrock, Steven Molesa, Daniel Soltman, Huai-Yuan Tseng, and Steven K. Volkman, SPIE Optics + Photonics, August 2-6, 2009, San Diego, CA

37. Invited "Printed Zinc Oxide Based Electronics: Materials, Devices, and Outlook", V. Subramanian, S. K. Volkman, and D. R. Redinger, LOPE-C, June 23-25, 2009, Frankfurt, Germany

38. Invited "Printed Devices for Low-Cost Electronics: Technology Status and Outlook", V. Subramanian, PETEC Inaugural Event, March 17, 2009, Durham, United Kingdom

39. invited "Printed Electronic Tags and Sensors for Smart Packaging Applications", Vivek Subramanian, Josephine Chang, Lakshmi Jagannathan, Frank Liao, Steve Molesa, David Redinger, Daniel Soltman, Huai-Yuan Tseng, Steve Volkman, Shong Yin, 2009 Flexible Electronics and Display Conference, Phoenix, AZ, Feb 2-5, 2009.

40. ***invited*** "Electronic Nose Sensors for Consumer Packaging", V. Subramanian, IDTechEx Printed Electronics USA, San Jose, CA, Dec 2-5, 2008.

41. ***invited*** "Solution-Processed Transparent Transistors for Low-Cost, Flexible Displays", V. Subramanian, S. K. Volkman, and D. R. Redinger, LEOS 2008: The 21st Annual Meeting of the IEEE Lasers and Electro-Optics Society, Newport Beach, CA, 9-13 November, 2008.

42. ***invited*** "Organic chemical and biosensors for smart packages", V. Subramanian, IDTechEx Printed Electronics Asia, Tokyo, Japan, Oct 8-9, 2008.

43. ***invited*** "Printed Electronics for Low-Cost Tags, Displays, and Sensors", V. Subramanian, 1st International Conference on R2R Printed Electronics, Seoul, Korea, April 30-May 2, 2008.

44. ***invited*** "Printed organic RFID tags: technology, roadmaps, and challenges", V. Subramanian, 1st Plastic Electronics Asia Conference and Showcase, Seoul, Korea, June 24-26, 2008

45. ***invited*** "Power supply considerations and solutions for printed electronic tags and sensors", V. Subramanian, IDTechEx Printed Electronics Europe, Dresden, Germany, April 8-9, 2008

46. ***invited*** "Printed Chemical and Biosensors: Technology, Design and Challenges", GOSPEL Workshop on Plastic Chemical Sensors, Dresden, Germany, April 9, 2008

47. ***Plenary*** "Printed Electronics For Low-Cost Electronic Systems: Technology Status and Application Development", Vivek Subramanian, Josephine B. Chang, Alejandro de la Fuente Vornbrock, Daniel C. Huang, Lakshmi Jagannathan, Frank Liao, Brian Mattis, Steven Molesa, David R. Redinger, Daniel Soltman, Steven K. Volkman, Qintao Zhang, 38th European Solid State Device Research Conference, Edinburgh, Scotland, September 15-19, 2008

48. ***invited*** "Printed Organic Transistors for Low-cost Tags, Displays, and Sensors: Technology, Modeling and Challenges", Vivek Subramanian, Alejandro de la Fuente Vornbrock, Huai-Yuan Tseng and Shong Yin, Materials Research Society Fall Meeting, Boston, MA, Dec 1-4, 2008.

49. ***invited*** "Printed Electronics for Low-Cost Tags and Sensors", Vivek Subramanian, Sixth Annual Workshop on Microelectronics and Electron Devices, April 18, 2008.

50. ***invited*** "Printed organic RF tags, chemical sensors and biosensors", Vivek Subramanian, International Symposium for Flexible Electronics and Display, Hsinchu, Taiwan, Nov 18, 2007.

51. ***invited*** "Printed Tags and Sensors for RFID: Opportunities and Challenges", Vivek Subramanian, Printed Electronics USA 2007, San Francisco, CA, Nov 14, 2007.

52. ***invited*** "Printed RFID Tags: Materials, Processes, and Devices", Vivek Subramanian, Daniel Soltman, Daniel Huang, Steven Molesa, 2007 AiChE Annual Meeting, Salt Lake City, UT, Nov. 8, 2007.

53. ***invited*** "Printed organic RFID tags: technology, roadmaps, and challenges", Vivek Subramanian, 3rd Global Plastic Electronics Conference and Showcase, Frankfurt, Germany, Oct 30, 2007.

54. ***invited*** "Printed organic transistors: technology, characteristics, and modeling", Vivek Subramanian, Alejandro de la Fuente Vornbrock, Daniel Soltman, Huai-Yuan Tseng, and Steve Molesa, 212th meeting of the Electrochemical Society, Washington, DC, Oct 8, 2007.

55. ***invited*** "Printed electronic tags and sensors - device, materials, and circuit issues", Vivek Subramanian, 2007 Organic Electronics Conference and Exhibition, Frankfurt, Germany, Sept 25, 2007.

56. ***invited*** "Inkjet printing of transistors, diodes, and passive components for smart tags", Vivek Subramanian, Innovations in Inkjet: 3rd DPI Inkjet Workshop, Eindhoven Institute of Technology, Netherlands, June 28-29, 2007.

57. ***invited*** "Printed organic transistors", A. de la Fuente and V. Subramanian, Industry Forum on Printed Electronics, Chicago, IL, April 23-24, 2007

58. ***invited*** "From Materials to Circuits: Implications of printed materials on printed RFID", V. Subramanian, 2007 Pira printed RFID conference, Frankfurt, Germany, June 4-6, 2007.

59. ***keynote*** "Droplet on demand lithography: An enabling technology for low-cost electronics", V. Subramanian, A. de la Fuente Vornbrock, S. Molesa, D. Redinger, Q. Zhang, and S. K. Volkman, SPIE Advanced lithography, 27th February, 2007

60. ***invited*** "Printed RFID tags: performance needs and technology trends", V. Subramanian, 2007 IDTechEx Smart labels USA , Boston, MA, Febraury 20-23, 2007.

61. ***keynote*** "Printed Organic Transistors for low-cost tagging and sensing applications", V. Subramanian, J. Chang, A. de la Fuente Vornbrock, S. Molesa, D. Soltman, and Q. Zhang. 6th International IEEE Conference on Polymers and Adhesives in Microelectronics and Photonics, Tokyo, January 15th-18th, 2007.

62. ***invited*** "Nano Inks for Printed RFID", V. Subramanian, Pira Nanoscale Inks and Pigment Technologies Conference, Chicago, IL, Sept 27-28, 2006.

63. ***invited*** "Toward Printed RFID: Materials, Processes, and Devices", V. Subramanian, 5th Annual Printed Electronics and Displays Conference and Trade Fair, Las Vegas, Oct 11-13, 2006.

64. ***invited*** "Inkjetted Organic Transistors for Smart Tagging Applications", Vivek Subramanian, Jean M. J. Frechet, Steven Molesa, Josephine Chang, Amanda R. Murphy, Alejandro de la Fuente Vornbrock, Steven Volkman, 2006 AiChE Annual Meeting, Nov 17th, 2006

65. ***invited focal paper*** "All-printed electronics: Materials, Devices, and Circuit Implications", V.Subramanian, J. Chang, S. Molesa, D. Redinger, and S. Volkman, Digital Fabrication 2006, Denver, CO, Sept 17-22, 2006.

66. ***invited*** "Printed transistors and passive components for low-cost electronics applications", V. Subramanian, J. B. Chang, S. E. Molesa, S. K. Volkman, and D. R. Redinger, International Symposium on VLSI Technology, Systems and Applications (VLSI-TSA) April, 2006, pp. 68-9.

67. ***invited*** "Advanced printed materials and devices for RFID applications", V. Subramanian, IDTechEx Printed Electronics Europe, April 19-21, 2006.

68. ***invited*** "Printed Electronic Nose Vapor Sensors for Consumer Product Monitoring", V. Subramanian, J. Lee, V. Liu, S. Molesa, IEEE International Solid State Circuits Conference, Paper 15.3, February, 2006.

69. ***invited*** "Nanotechnology in Printed Electronics: Nanoparticles, Nanorods, and Nanowhy", V. Subramanian, Pira Pack Electronics Conference, January 25-26, 2006.

70. ***invited*** "All-printed RFID Tags: Materials, Devices, and Circuit Implications", Vivek Subramanian, Paul C. Chang, Daniel Huang, Josephine B. Lee, Steven E. Molesa, David R. Redinger, and Steven K. Volkman, VLSI Design, 2006, Hyderabad India, Jan 2006.

71. ***invited*** "Printed organic transistors: materials and technology", Vivek Subramanian, Pacifichem 2005: American Chemical Society Pacific Basin meeting, December 15-20, 2005, Honolulu, HI,

72. ***invited*** "Low-cost arrayed gas sensors for environmental monitoring". Vivek Subramanian, Josephine Lee and Vincent Liu, Materials Research Society Fall Symposium, Paper S2.1, Boston, MA, December 2005.

73. ***invited*** "Prospects for All-printed RFID: Materials, Devices, Circuits", V. Subramanian, International Workshop on Radio Frequency Identification (RFID) and Wirelss Sensors, 11-13 November, 2005, Kanpur, India.

74. ***invited*** "Printed electronics for low-cost tagging applications", V. Subramanian, 2005 International Symposium on Flexible Electronics and Display, Hsinchu, Taiwan, October 2005.

75. ***invited*** "Printed electronic nose gas sensors", Vivek Subramanian, Plastic Electronics 2005, Frankfurt, Germany, Oct 4-5, 2005

76. ***invited*** "Uses of nanotechnology in printed electronics", Vivek Subramanian, Printed Electronics 205, Pira International, Thistle Marble Arch, London, UK, Sept 14-15, 2005

77. ***invited*** "Printed organic transistors for low-cost RFID applications", Vivek Subramanian, Proceedings of SPIE-The International Society for Optical Engineering vol. 5940, (594013/1-594013/9) , pp. 170-178, 2005.

78. ***invited*** "Advanced printed materials and devices for ultra-low-cost RFID", Vivek Subramanian, Printed RFID: Achieving low cost tags through printed electronics – Pira International, Gatwick, Surrey, UK, May 10-11, 2005.

79. ***Plenary session invited talk*** "Printed Organic Transistors for Ultra-low-cost RFID Applications", Vivek Subramanian, Paul C. Chang, Josephine B. Lee, Steven E. Molesa, and Steven K. Volkman, Polytronic 2004: 4th International IEEE Conference on Polymers and Adhesives in Microelectronics and Photonics, Portland, Oregon, USA, 12 September 2004.

80. ***invited*** "Materials, Device, and Circuits Issues for low-cost printed RFID", V. Subramanian, 2nd Cintelliq Organic Semiconductor Conference, 2004 (OSC-2004), Cambridge, England, October 2004.

81. ***invited*** "All-printed flexible organic thin film transistors: Current status and outlook for the future", V. Subramanian, J. M. J. Fréchet, P. C. Chang, D. C. Huang, J. B. Lee, F. Liao, B. A. Mattis, S. Molesa, A. R. Murphy, D. R. Redinger, and S. K. Volkman, 206th meeting of the Electrochemical Society, Honolulu, HI, October 2004.

82. ***invited*** "Nanoscale organic transistors: towards gain in molecular devices", V. Subramanian, P. C. Chang, J. B. Lee, T. Le, A. Murphy, J. M. J. Frechet, and A. Liddle, 2004 IEEE Nanoscale Devices and Systems Integration Conference, Miami, FL, 2004.

83. ***invited*** "Towards Printed Low-Cost RFID Tags: Device, Materials and Circuit Technologies", V. Subramanian, 2nd Advanced Technology Workshop on Printing an Intelligent Future: Printed Organic and Molecular Electronic Technologies, Boston, MA, March 16-19, 2003.

84. ***invited*** "Prospects for organic semiconductor based devices and circuits: applications, performance, and reliability considerations", V. Subramanian, 2002 Topical Research Conference on Reliability, Oct 2002.

85. ***invited*** "FinFET - quasi-planar double-gate MOSFET", S. H. Tang, L. Chang, N. Lindert, Y-K. Choi, W-C. Lee, X. Huang, V. Subramanian, J. Bokor, T-J. King, C. Hu, 20001 IEEE International Solid-State Circuits Conference Digest of Technical Papers, pp. 118-119, 437, 2001.

86. ***invited*** "3-D ICs with Multiple Si Layers: Performance Analysis, and Technology", K. Saraswat, K. Banerjee, A. Joshi, P. Kalavade, S. Souri, and V. Subramanian, *presented at* The Fifth International Symposium on Low and High Dielectric Constant Materials: Materials Science, Processing, and Reliability Issues, 197th meeting of the Electrochemical Society, Toronto, Ontario, Canada, May 14-18, 2000.

87. ***invited*** "Novel 3-D Structures", K. C. Saraswat, S. J. Souri, V. Subramanian, A. R. Joshi, and A. W. Wang, 1999 IEEE International SOI Conference Proceedings, pp. 54-55.

88. ***invited*** "Seeding Technology for High Performance TFTs", K. C. Saraswat and V. Subramanian, Proceedings of the Electronic Display Forum 98, EIAJ/SEMI, Yokohama, April 1998, pp. 2.7-2.15.

89. ***invited*** "A Low-Temperature Polycrystalline Si TFT Technology for Large-Area AMLCD Drivers", K. C. Saraswat, V. Subramanian, and S. Jurichich, Polycrystalline Thin Films III - Structure, Texture, Properties, and Applications, MRS Symposium Proceedings pp 439-449, 1997.

90. ***invited*** "A low temperature polycrystalline SiGe CMOS TFT technology for large area AMLCD drivers", K. C. Saraswat, S. Jurichich, T.-J. King, V. Subramanian, and A. Wang, Proceedings of Thin Film Transistor Technologies III, ECS Symposium, 1996, pp. 186-196.

Journal Papers

1. ***invited*** Gerd Grau and Vivek Subramanian, "Dimensional scaling of high-speed printed organic transistors enabling high-frequency operation", Flex. Print. Electron. 2020, Vol. 5 014013

2. ***invited*** William Scheideler and Vivek Subramanian, "Printed flexible and transparent electronics: enhancing low-temperature processed metal oxides with 0D and 1D nanomaterials", 2019 Nanotechnology 30 272001

3. R. Kumar, K. M. Johnson, N. X. Williams, V. Subramanian, "Scaling Printable Zn–Ag2O Batteries for Integrated Electronics", Adv. Energy Mater. 2019, 1803645.

4. William J. Scheideler, Matthew W. McPhail, Rajan Kumar, Jeremy Smith, and Vivek Subramanian, "Scalable, High-Performance Printed InOx Transistors Enabled by Ultraviolet-Annealed Printed High-k AlOx Gate Dielectrics", ACS Applied Materials & Interfaces 2018 10 (43), 37277-37286.

5. J. Smith, S. Chung, J. Jang, C. Biao, V. Subramanian, "Solution-processed complementary resistive switching arrays for associative memory", IEEE Transactions on Electron Devices 64 (10), pp 4310, 2017

6. A. Zeumault, V. Subramanian, "Use of high-k encapsulation to improve mobility in trap-limited metal oxide semiconductors", physica status solidi (b) 254 (10), 1700124, 2017

7. A. Zeumault, W. Scheideler, V. Subramanian, "Electrostatic tuning of spray-deposited ZnO for controlled mobility enhancement", Advanced Functional materials, 27 (30), pp. 1701021, 2017

8. W. J. Scheideler, R. Kumar, A. R. Zeumault, V. Subramanian, "Low-Temperature-Processed Printed Metal Oxide Transistors Based on Pure Aqueous Inks", Advanced Functional Materials 2017, 1606062.

9. Jaewon Jang, Vivek Subramanian, "Effect of electrode material on resistive switching memory behavior of solution-processed resistive switches: Realization of robust multi-level cells", Thin Solid Films, Volume 625, Pages 87-92, 1 March 2017.

10. S. Chung, M. A. U. Karim, H. J. Kwon, W. Scheideler and V. Subramanian, “A High-Speed Inkjet-Printed Microelectromechanical Relay With a Mechanically Enhanced Double-Clamped Channel-Beam,” Journal of Microelectromechanical Systems, vol. 26, no. 1, pp. 95-101, Feb. 2017.

11. G. Grau, E. J. Frazier, and V. Subramanian, “Printed unmanned aerial vehicles using paper-based electroactive polymer actuators and organic ion gel transistors”, Nature Microsystems & Nanoengineering, vol 2, pp. 16032, 2016

12. ***invited*** Gerd Grau, Jialiang Cen, Hongki Kang, Rungrot Kitsomboonloha, William J Scheideler, and Vivek Subramanian “Gravure-printed electronics: recent progress in tooling development, understanding of printing physics, and realization of printed devices”, IOP Journal of Flexible and Printed Electronics, vol. 1, No. 2, pp. 023002, 2016

13. Scheideler, William J., Jeremy Smith, Igal Deckman, Seungjun Chung, Ana Claudia Arias, and Vivek Subramanian. "A robust, gravure-printed, silver nanowire/metal oxide hybrid electrode for high-throughput patterned transparent conductors." Journal of Materials Chemistry C 4, no. 15 (2016): 3248-3255.

14. Karim, Muhammed Ahosan Ul, Seungjun Chung, Elad Alon, and Vivek Subramanian. "Fully Inkjet-Printed Stress-Tolerant Microelectromechanical Reed Relays for Large-Area Electronics." Advanced Electronic Materials (2016).

15. Khan, Yasser, Felippe J. Pavinatto, Monica C. Lin, Amy Liao, Sarah L. Swisher, Kaylee Mann, Vivek Subramanian, Michel M. Maharbiz, and Ana C. Arias. "Bioelectronic Interfaces: Inkjet-Printed Flexible Gold Electrode Arrays for Bioelectronic Interfaces (Adv. Funct. Mater. 7/2016)." Advanced Functional Materials 26, no. 7 (2016): 981-981.

16. Jang, Jaewon, Seungjun Chung, Hongki Kang, and Vivek Subramanian. "P-type CuO and Cu 2 O transistors derived from a Sol–Gel Copper (II) acetate monohydrate precursor." Thin Solid Films (2016).

17. Grau, Gerd, and Vivek Subramanian. "Fully High-Speed Gravure Printed, Low-Variability, High-Performance Organic Polymer Transistors with Sub-5 V Operation." Advanced Electronic Materials (2016).

18. Zeumault, Andre, and Vivek Subramanian. "Mobility Enhancement in Solution-Processed Transparent Conductive Oxide TFTs due to Electron Donation from Traps in High-k Gate Dielectrics." Advanced Functional Materials (2016).

19. Zeumault, Andre, William Scheideler, Gerd Grau, Jeremy Smith, and Vivek Subramanian. "Patterning of Solution-Processed, Indium-Free Oxide TFTs by Selective Spray Pyrolysis." Advanced Electronic Materials (2015).

20. Jang, Jaewon, Hongki Kang, Himamshu C. Nallan Chakravarthula, and Vivek Subramanian. "Fully Inkjet-Printed Transparent Oxide Thin Film Transistors Using a Fugitive Wettability Switch." Advanced Electronic Materials 1, no. 7 (2015).

21. Grau, Gerd, Rungrot Kitsomboonloha, Hongki Kang, and Vivek Subramanian. "High performance printed organic transistors using a novel scanned thermal annealing technology." Organic Electronics 20 (2015): 150-157.

22. Zeumault, Andre, and Vivek Subramanian. "Improved Technique for Quantifying the Bias-Dependent Mobility of Metal-Oxide Thin-Film Transistors." Electron Devices, IEEE Transactions on 62, no. 3 (2015): 855-861.

23. Swisher, Sarah L., Steven K. Volkman, and Vivek Subramanian. "Tailoring Indium Oxide Nanocrystal Synthesis Conditions for Air-Stable High-Performance Solution-Processed Thin-Film Transistors." ACS applied materials & interfaces 7, no. 19 (2015): 10069-10075.

24. Koo, Hyunmo, Wookyu Lee, Younchang Choi, Junfeng Sun, Jina Bak, Jinsoo Noh, Vivek Subramanian, Yasuo Azuma, Yutaka Majima, and Gyoujin Cho. "Scalability of carbon-nanotube-based thin film transistors for flexible electronic devices manufactured using an all roll-to-roll gravure printing system." Scientific reports 5 (2015).

25. “Perpendicular Magnetization Switching via Current induced Spin-Orbit Torques on Flexible Substrate”, O.J. Lee, L. You, J. Jang, V. Subramanian, S. Sahahuddin, Bulletin of the American Physical Society 60, 2015.

26. “High-Performance Inkjet-Printed Four-Terminal Microelectromechanical Relays and Inverters”, Seungjun Chung, Muhammed Ahosan Ul Karim, Hyuk-Jun Kwon, and Vivek Subramanian, Nano Letters, 15 (5), pp 3261–3266, 2015.

27. ***Invited*** Subramanian, Vivek, Jialiang Cen, Alejandro de la Fuente Vornbrock, Gerd Grau, Hongki Kang, Rungrot Kitsomboonloha, Daniel Soltman, and Huai-Yuan Tseng. "High-Speed Printing of Transistors: From Inks to Devices." Proceedings of the IEEE 103, no. 4 (2015): 567-582.

28. Scheideler, William J., Jaewon Jang, Muhammed Ahosan Ul Karim, Rungrot Kitsomboonloha, Andre Zeumault, and Vivek Subramanian. "Gravure-Printed Sol–Gels on Flexible Glass: A Scalable Route to Additively Patterned Transparent Conductors." ACS applied materials & interfaces 7, no. 23 (2015): 12679-12687.

29. Lee, OukJae, Long You, Jaewon Jang, Vivek Subramanian, and Sayeef Salahuddin. "Flexible spin-orbit torque devices." Applied Physics Letters 107, no. 25 (2015): 252401.

30. Kitsomboonloha, Rungrot, Hongki Kang, Gerd Grau, William Scheideler, and Vivek Subramanian. "MHz-Range Fully Printed High-Performance Thin-Film Transistors by Using High-Resolution Gravure-Printed Lines." Advanced Electronic Materials 1, no. 12 (2015).

31. Swisher, Sarah L., Monica C. Lin, Amy Liao, Elisabeth J. Leeflang, Yasser Khan, Felippe J. Pavinatto, Kaylee Mann et al. "Impedance sensing device enables early detection of pressure ulcers in vivo." Nature communications 6 (2015).

32. "A Stencil Printed, High Energy Density Silver Oxide Battery Using a Novel Photopolymerizable Poly(acrylic acid) Separator", K. Braam and V. Subramanian, Advanced Materials, Vol. 27, 689-694, 2015

33. "Megahertz-class printed high mobility organic thin-film transistors and inverters on plastic using attoliter-scale high-speed gravure-printed sub-5μm gate electrodes", H. Kang, R. Kitsomboonloha, K. Ulmer, L. Stecker, G. Grau, J. Jang, V. Subramanian, Organic Electronics, vol. 15, 3639-3647, 2014.

34. "Exploitation of the coffee-ring effect to realize mechanically enhanced inkjet-printed microelectromechanical relays with U-bar-shaped cantilevers", S Chung, MAU Karim, M Spencer, HJ Kwon, CP Grigoropoulos, E Alon, V. Subramanian, Applied Physics Letters 105 (26), 261901, 2014.

35. "Printed Transistors on Paper: Towards Smart Consumer Product Packaging", G. Grau, R. Kitsomboonloha, S. L. Swisher, H. Kang, and V. Subramanian, Advanced Functional Materials, Vol. 24, 5067-5074, 2014.

36. "Cell Filling in Gavure Printing for Printed Electronics, J. Cen, R. Kitsomboonloha, and V. Subramanian, vol. 30, 13716-13726, 2014.

37. "Systematic Design of Jettable Nanoparticle-based inkjet inks: Rheology, Acoustics, and Jettability", H. C. Nallan, J. A. Sadie, R. Kitsomboonloha, S. K. Volkman, and V. Subramanian, Langmuir, vol. 30, 13470-13477, 2014.

38. "Three-dimensional Inkjet-printed Interconnects using Functional Metallic Nanoparticle Inks", J. A. Sadie, V. Subramanian, Advanced Functional Materials, vol. 24, 6834-6842, 2014.

39. "Electrical Characteristics of multilayer MoS_2 transistors at real operating temperatures with different ambient conditions", H-J. Kwon, J. Jang, S. Kim, V. Subramanian, and C. P. Grigoropoulos, Applied Physics Letters, vol. 105, 15205, 2014.

40. "Lubrication-related residue as a fundamental process scaling limit to gravure printed electronics", R. Kitsomboonloha and V. Subramanian, Langmuir, vol. 30, 3612-3624, 2014.

41. "Roll-to-roll gravure with nanomaterials for printing smart packaging", M. Jung, J. Kim, H. Koo, W. Lee, V. Subramanian, G. Cho, Journal of Nanoscience and Nanotechnology, vol. 14, 1303-1317, 2014.

42. "Measurement and analysis of 1/f noise under switched bias in organic thin film transistors", H. Kang and V. Subramanian, Applied Physics Letters, 104, 023301, 2014.

43. "A new switching device for printed electronics: Inkjet-printed Microelectromechanical Relay", E. S. Park, Y. Chen, T. J. K. Liu, and V. Subramanian, Nano Letters, 13 (11), 5355-5360, 2013.

44. "Inkjet printing of precisely defined features using contact-angle hysteresis", Dan Soltman, Ben Smith, S.J.S. Morris, Vivek Subramanian, Journal of Colloid and Interface Science, Volume 400, Pages 135–139, 2013

45. "Transparent High-Performance Thin Film Transistors from Solution-Processed SnO2/ZrO2 Gel-like Precursors", J. Jang, R. Kitsomboonloha, S. L. Swisher, E. S. Park, H. Kang, and V. Subramanian, Advanced Materials, 25 (7), pp. 1042-1047, 2013.

46. "Femtoliter-Scale Patterning by High-Speed, Highly Scaled Inverse Gravure Printing", R Kitsomboonloha, SJS Morris, X Rong, V Subramanian, Langmuir 28 (48), 16711-16723, 2012

47. "Resistance Switching Characteristics of Solid Electrolyte Chalcogenide Ag2Se Nanoparticles for Flexible Nonvolatile Memory Applications", J. Jang, F. Pan, K. Braam, and V. Subramanian, Advanced Materials, 24, pp. 3573-3576, 2012

48. "High-Performance Printed Transistors Realized Using Femtoliter Gravure-Printed Sub-10 μm Metallic Nanoparticle Patterns and Highly Uniform Polymer Dielectric and Semiconductor Layers", H. Kang, R. Kitsomboonloha, J. Jang, and V. Subramanian, Advanced Materials, 24, pp. 3065–3069, 2012

49. "All Printed Edge-Triggered Register Using Single Walled Carbon Nanotube-Based Thin Film Transistor" J. Noh, M. Jung, K. Jung, G. Lee, S. Lim, D. Kim, V. Subramanian, G. Cho, Journal of Nanoscience and Nanotechnology, 12, pp. pp. 4261-4264, 2012

50. “Effect of sintering conditions on mixed ionic-electronic conducting properties of silver sulfide nanoparticles”. Shong Yin, Kazuya Terabe, Michael F. Toney, and Vivek Subramanian, J. Appl. Phys. 111, 053530 (2012)

51. “Characterization and optimization of a printed, primary silver-zinc battery”, Kyle Braam, Steven K. Volkman, Vivek Subramanian, Journal of Power Sources, vol. 199, pp. 367-372, 2012.

52. “Mechanistic Studies on Sintering of Silver Nanoparticles”, Steven K. Volkman, Shong Yin, Teymur Bakhishev, Kanan Puntambekar, Vivek Subramanian, Michael F. Toney, Chemistry of Materials, vol. 23, pp 4634–4640, 2011.

53. “Fully Gravure-Printed D Flip-Flop on Plastic Foils Using Single-Walled Carbon-Nanotube-Based TFTs”, J. Noh, M. Jung, K. Jung, G. Lee, J. Kim, S. Lim, D. Kim, Y. Choi, Y. Kim, V. Subramanian, G. Cho, Electron Device Letters, IEEE , vol.32, pp.638-640, 2011

54. “Measurement, analysis, and modeling of 1/f noise in pentacene thin film transistors”, H. Kang, L. Jagannathan, V. Subramanian, Applied Physics Letters, vol., 99, pp 062106-062108, 2011.

55. “A Detailed Study of the Forming Stage of an Electrochemical Resistive Switching Memory by KMC Simulation”, F. Pan, S. Yin, V. Subramanian, IEEE Electron Device Letters, IEEE , vol.32, pp.949-951, 2011

56. “High-speed organic transistors fabricated using a novel hybrid-printing technique”, H-Y. Tseng, B. Purushothaman, J. Anthony, V. Subramanian, Organic Electronics, Vol. 12, pp. 1120-1125, 2011.

57. “AM Radio Circuit Using Printed Electronic Components”, J. Noh, J. Kim, N. Lim, J. Kim, V. Subramanian, G. Cho, Journal of Nanoscience and Nanotechnology, Volume 11, pp. 4384-4388, 2011

58. “All Inkjet-Printed, Fully Self-Aligned Circuits for Low-Cost Applications”, H-Y. Tseng and V. Subramanian, Organic Electronics, Vol. 12, pp. 249-256, 2011

59. “Modeling of printed single walled carbon nanotube thin film transistors for attaining optimized clock signals”, Jinsoo Noh, Minhun Jung, Kyunghwan Jung, Soyeon Lim, Gwangyong Lee, Vivek Subramanian, Ashley D. Leonard, James Tour, and Gyoujin Cho, J. Appl. Phys. 108, pp. 102811, 2010

60. “Fully gravure and ink-jet printed high speed pBTTT organic thin film transistors”, Alejandro de la Fuente Vornbrock, Donovan Sung, Hongki Kang, Rungrot Kitsomboonloha, Vivek Subramanian, Organic Electronics, 11, pp. 2037-2044, 2010

61. “Scalability of Roll-to-Roll Gravure-Printed Electrodes on Plastic Foils”, Jinsoo Noh, Dongsun Yeom, Chaemin Lim, Hwajin Cha, Jukyung Han, Junseok Kim, Yongsu Park, Vivek Subramanian, Gyoujin Cho, IEEE Transactions on Electronics Packaging Manufacturing, vol. 33, pp. 275 – 283, 2010

62. “Methodology for inkjet printing partially wetting films”, D. Soltman, B. Smith, H. Kang, S. Morris, and V. Subramanian, Langmuir, 26, pp. 15686-15693, 2010

63. “Hydrostatic optimization of inkjet-printed films”, H. Kang, D. Soltman, and V. Subramanian, Langmuir, 26, pp 11568–11573, 2010

64. ***Invited*** “Printed Electronics: The Challenges Involved in Printing Devices, Interconnects, and Contacts”, J. Perelaer, P. J. Smith, D. Mager, D. Soltman, S. K. Volkman, V. Subramanian, J. G. Korvink, U. S. Schubert, J. Mat. Chem., J. Mater. Chem., 20, pp. 8446-8453, 2010

65. “Quantification of Thin Film Crystallographic Orientation Using X-ray Diffraction with an Area Detector”, Jessy L. Baker, Leslie H. Jimison, Stefan Mannsfeld, Steven Volkman, Shong Yin, Vivek Subramanian, Alberto Salleo, A. Paul Alivisatos and Michael F. Toney, Langmuir, 2010, 26 (11), pp 9146–9151

66. “Thickness Changes in Polythiophene Gas Sensors Exposed to Vapor”, F. Liao, M.F. Toney, and V. Subramanian, Sensors and Actuators B, 148, pp. 74-80, 2010

67. “Physical Discrimination of Amine Vapor Mixtures Using Polythiophene Gas Sensor Arrays”, F. Liao, S. Yin, M.F. Toney, V. Subramanian, Sensors and Actuators B, 150, pp. 254-263, 2010

68. “Solution-Processable alpha-omega-Distyryl Oligothiophene Semiconductors with Enhanced Environmental Stability”, C. E. Mauldin, K. Puntambekar, A. R. Murphy, F. Liao, V. Subramanian, J.M.J. Fréchet, D.M. DeLongchamp, D.A. Fischer, D.A. M.F. Toney, Chemistry of Materials, vol. 21, 4831—4835, 2009.

69. ***invited*** “Solution-processed Zinc Oxide Transistors for Low-Cost electronics Applications”, V. Subramanian, T. Bakhishev, D. R. Redinger, and S. K. Volkman, IEEE Journal of Display Technology, Vol. 5 , pp. 525 – 530, 2009

70. “Investigation of Gold Nanoparticle Inks for Low-Temperature Lead-Free Packaging Technology”, T. Bakhishev and V. Subramanian, Journal of Electronic Materials, vol. 38, pp. 2720, 2009.

71. “Label-free low-cost disposable DNA hybridization detection systems using organic TFTs”, Biosensors and Bioelectronics, vol. 25, pp. 972, 2010.

72. “DNA detection using organic thin film transistors: Optimization of DNA immobilization and sensor sensitivity”, Lakshmi Jagannathan, Vivek Subramanian, Biosensors and Bioelectronics, vol. 25, pp. 288, 2009.

73. “First-Principles Studies of the Dynamics of [2]Rotaxane Molecular Switches”, Kinyip Phoa, J. B. Neaton, Vivek Subramanian, Nano Letters, 9, pp. 3225-3229, 2009.

74. “Patternable polymer bulk heterojunction photovoltaic cells on plastic by rotogravure printing”, Jau M. Ding, Alejandro de la Fuente Vornbrock, Ching Ting and Vivek Subramanian,, Solar Energy and Materials, 93, pp. 459-464, 2009.

75. “Scaling and Optimization of Gravure-Printed Nanoparticle Lines for Printed Electronics”, D. C. Sung, A. de la Fuente Vornbrock, V. Subramanian, IEEE Transactions on Components and Packaging Technologies, 33, pp. 105 – 114, 2010.

76. “Selective Growth of Zinc Oxide Nanorods on Inket printed seed patterns”, R. Kitsomboonloha, S. Baruah, M. T. Z. Myint, V. Subramanian, and J. Dutta, “ Journal of Crystal Growth, 311, pp. 2352-2358, 2009

77. “Inkjet printed line morphologies and temperature control of the coffee ring effect”, Dan Soltman and Vivek Subramanian, Langmuir, vol 24(5), pp. 2224-2231, 2008.

78. “High-Performance Chemical-Bath-Deposited Zinc Oxide Thin-Film Transistors”, D. Redinger and V. Subramanian, IEEE Transactions on Electron Devices, 54, pp. 1301-1307, 2007.

79. “DNA hybridization detection with organic thin film transistors: Toward fast and disposable DNA microarray chips”, Qintao Zhang and Vivek Subramanian, Biosensors and Bioelectronics, 22, pp. 3182-3187, 2007.

80. “Performance recovery and optimization of poly(3-hexylthiophene) transistors by thermal cycling”, B. A. Mattis, P. C. Chang, and V. Subramanian, Synthetic Metals, 156, pp. 1241-1248, 2006.

81. “Printable polythiophene gas sensor array for low-cost electronic noses”, Josephine B. Chang, Vincent Liu, Vivek Subramanian, Kevin Sivula, Christine Luscombe, Amanda Murphy, Jinsong Liu, and Jean M. J. Fréchet J. Appl. Phys. 100, 014506 (2006)

82. “Effect of active layer thickness on bias stress effect in pentacene thin-film transistors”, Josephine B. Chang and Vivek Subramanian Appl. Phys. Lett. 88, 233513 (2006)

83. “Correlating molecular design to microstructure in thermally convertible oligothiophenes: the effect of branched versus linear end groups”, D. M. DeLongchamp, Y. Jung, D. A. Fischer, E. K. Lin, P. Chang, V. Subramanian, A. R., Murphy, J. M. J. Frechet., Journal of Physical Chemistry B, vol.110, no.22, 8 June 2006, pp. 10645-50.

84. “Inkjetted Crystalline Single-Monolayer Oligothiophene OTFTs”, P. C. Chang,, S. E. Molesa, A. R. Murphy, J. M. J. Fréchet, and V. Subramamian, IEEE Transactions on Electron Devices, vol. 53, pp. 594-600, 2006.

85. ***selected for cover:*** “Direct correlation of organic semiconductor film structure to field-effect mobility”, D. M. DeLongchamp, S. Sambasivan, D. A. Fischer, E. K. Lin, P. Chang, A. R. Murphy, J. M. J. Frechet, V. Subramanian, Advanced Materials, vol. 17, 2340-344, 2005.

86. “Self-Assembly, Molecular Ordering, and Charge Mobility in Solution-Processed Ultrathin Oligothiophene Films”, A. R. Murphy, P. C. Chang, P. VanDyke, J. Liu, J. M. J. Fréchet, V. Subramanian, D. M. DeLongchamp, S. Sambasivan, D. A. Fische, E. K. Lin, Chem. Mater., vol. 17, pp. 6033-41, 2005.

87. “Printed organic transistors for ultra-low-cost RFID applications”, V. Subramanian, P.C. Chang, J. B. Lee, S. E. Molesa, S. K. Volkman, IEEE Transactions on Components & Packaging Technologies, vol. 28, pp. 742-727, 2005.

88. ***invited*** “Progress towards development of all-printed RFID tags: Materials, Processes, and Devices”, Vivek Subramanian, Jean M. J. Fréchet , Paul C. Chang, Daniel Huang, Josephine B. Lee, Steven E. Molesa, Amanda R. Murphy, David R. Redinger, and Steven K. Volkman, Proceedings of the IEEE, vol. 93, pp. 1330-1338, 2005.

89. “10-nm channel length pentacene transistors”, Josephine Lee, Paul Chang, Alex Liddle, and Vivek Subramanian, IEEE Transactions on Electron Devices, vol. 52, pp. 1874-1879, 2005.

90. “Organic TFTs as gas sensors for electronic nose applications”, F. Liao, C. Chen, and V. Subramanian, Sensors and Actuators B-Chemical. Vol. 107, pp. 849-855, 2005.

91. “Nanoscale device isolation of organic transistors via electron-beam lithography”, Brian A. Mattis, Yunan Pei, and Vivek Subramanian, Appl. Phys. Lett., vol. 86, pp. 769-772, 2005.

92. “Weave Patterned Organic Transistors on Fiber for E-Textiles”, Josephine B. Lee and Vivek Subramanian, IEEE Transactions on Electron Devices, vol. 62, pp. 269, 2005.

93. “An ink-jet-deposited passive component process for RFID”, D. Redinger, R. Farshchi, and V. Subramanian, IEEE Transactions on Electron Devices, vol. 51, pp. 1978, 2004.

94. “Film Morphology and Thin Film Transistor Performance of Solution Processed Oligothiophenes”, Paul C. Chang, Josephine Lee, Daniel Huang, Vivek Subramanian, Amanda R. Murphy, and Jean M. J. Fréchet,„ J. Chem. Mat., vol. 16, pp. 4783, 2004.

95. “Organic Thin Film Transistors from a Soluble Oligothiophene Derivative Containing Thermally Removable Solubilizing Groups”, Amanda R. Murphy, Jean M. J. Frechet, Paul Chang, Josephine Lee,and Vivek Subramanian, J. Am. Chem. Soc. vol. 126, pp. 1596, 2004.

96. “Plastic-compatible low-resistance printable gold nanoparticle conductors for flexible electronics”, D. Huang, F. Liao, S. Molesa, D. Redinger, and V. Subramanian, Journal of the electrochemical society, Vol. 150, pp. 412, 2003.

97. “Observation of dopant-mediated intermixing at Ge/Si Interface”, H. Takeuchi, P. Ranade, V. Subramanian, and T-J. King, Applied Physics Letters, Vol. 80, pp. 3706-3708, 2002.

98. “A novel elevated source/drain PMOSFET formed by Ge-B/Si Intermixing”, P. Ranade, H. Takeuchi, V. Subramanian, and T-J. King, IEEE Electron Device Letters, Vol. 23, pp. 218-220, 2002.

99. “Design and Fabrication of 50 nm Ultra-Thin Body P-MOSFETs with a Silicon-Germanium Heterostructure Channel". Y-C. Yeo, V. Subramanian, J. Kedzierski, P. Xuan, T-J. King, J. Bokor, and C. Hu, IEEE Transactions on Electron Devices, 49, pp. 279 –286, 2002 (IEEE Paul Rappaport Award for best paper in an IEEE Electron Device Society Journal).

100. “Observation of Boron and Arsenic Mediated Interdiffusion Across Germanium/Silicon Interfaces”, P. Ranade, H. Takeuchi, V. Subramanian and T.-J. King, Electrochemical and Solid-State Letters, Vol. 5, no. 2, pp. G5-G7, 2002.

101. “Sub-50nm P-Channel FinFET”, X. Huang, W-C. Lee, C. Kuo, D. Hisamoto, L. Chang, J. Kedzierski, E. Anderson, H. Takeuchi, Y-K. Choi, K. Asano, V. Subramanian, T-J. King, J. Bokor, and C. Hu, IEEE Transactions on Electron Devices, Vol. 48, pp. 880-886, 2001.

102. “A 20 nm gate-length ultra-thin body p-MOSFET with silicide source/drain.” J. Kedzierski, P. Xuan, V. Subramanian, E. Anderson, J. Bokor, T.-J. King, and C. Hu, Superlattices and Microstructures, Vol. 28, pp.445-452, 2000.

103. “Ultrathin-body SOI MOSFET for deep-sub-tenth micron era”, Y-K. Choi, K. Asano, N. Lindert, V. Subramanian, T-J. King, J. Bokor, C. Hu , IEEE Electron Device Letters , Vol. 21, pp. 254-255, 2000.

104. “Nanoscale Ultra-Thin-Body Silicon-on-Insulator P-MOSFET with a SiGe/Si Heterostructure Channel”, Y. C. Yeo, V. Subramanian, J. Kedzierski, P. Xuan, T-J. King, J. Bokor, and C. Hu, IEEE Electron Device Letters, Vol. 21, pp. 161-163, 2000.

105. “Low-leakage Germanium-seeded Laterally-crystallized Single-grain 100nm TFTs for Vertical Integration Applications”, V. Subramanian, M. Toita, N. R. Ibrahim, S. J. Souri and K. C. Saraswat, IEEE Electron Device Letters, Vol. 20, pp. 341-343, 1999.

106. “High Performance Germanium-Seeded Laterally Crystallized TFTs for Vertical Device Integration”, V. Subramanian and K. C. Saraswat, IEEE Transactions on Electron Devices. Vol. 18, pp. 1934-1939, 1998.

107. “Optimization of Silicon-Germanium TFTs through the control of amorphous precursor characteristics”, V. Subramanian and K. C. Saraswat, IEEE Transactions on Electron Devices, vol. 45, pp. 1690-1695, 1998.

108. “Controlled Two-Step Solid Phase Crystallization for High Performance Polysilicon TFTs”, V. Subramanian, P. Dankoski, L. Degertekin, B. T. Khuri-Yakub, and K. C. Saraswat, IEEE Electron Device. Letters, vol. 18, pp. 378-81, 1997

109. “In-Situ Monitoring of Crystallinity and Temperature During Rapid Thermal Crystallization of Silicon on Glass”, V. Subramanian, L. Degertekin, P. Dankoski, B. T. Khuri-Yakub, and K. C. Saraswat, Journal of the Electrochemical Society, vol. 144, 1997, pp. 2216-2221.

110. “The Effect of Ionizing Radiation Damage on Transconductance of Short Channel Insulated Gate Field Effect Transistors”, Subramanian & Bhattacharya, Japanese Journal of Applied Physics I, vol. 34 (1995), pp. 1809

111. “Chemical Contamination of Thin Oxides and Native Silicon for use in Modern Device Processing”, Subramanian et al, International Journal of Electronics, vol. 78 (1995), pp. 519

Conference Presentations

1. R. Kumar, E. Kedzie, B. D. McCloskey, and V. Subramanian, “Characterizing Zn Corrosion in Printed Zn-Air batteries Via Operando Dems, XRD, and XAS”, Electrochemical Conference on Energy and the Environment: Bioelectrochemistry and Energy Storage, MA2019-04 July 21-26, 2019, Glasgow, Scotland
2. Carlos Biaou, Matt McPhail, Vivek Subramanian and Oscar Dubon, “Comprehensive Multifactorial Studies on the Degradation of Perovskite Solar Cells in Operation”, 2019 Spring Materials Research Society Meeting, Phoenix, AZ, April 22-26, 2019.
3. Rajan Kumar, Jessica E. Nichols, Bryan D. McCloskey, and Vivek Subramanian, “Low-Temperature-Processing of Printed Cathodes for Aqueous Metal-Air Batteries”, ECS AiMES 2018 Meeting, September 30, 2018 - October 4, 2018, Cancun, Mexico
4. N. Deka and V. Subramanian, "First demonstration of vacuum-sealed fully integrated BEOL-compatible field emission devices for Si integrated high voltage applications," 2018 76th Device Research Conference (DRC), Santa Barbara, CA, 2018, pp. 1-2.
5. “Inkjet-printed MEM relays for active solar cell routing”, S Patel, WJ Scheideler, MAU Karim, V Subramanian, Micro Electro Mechanical Systems (MEMS), 2018 IEEE, 616-619
6. “Back-channel engineering of ultrathin printed indium oxide transistors for carbon dioxide sensing”, Y. Kobayashi, W. Scheideler, V. Subramanian, 2017 Materials Research Society Fall Meeting, Boston, MA, Nov 28, 2017.
7. “Morphological Control of Gravure Printed Perovskite Films”, M. McPhail and V. Subramanian, 2017 Materials Research Society Fall meeting, Boston, MA, Nov 29, 2017.
8. “Improving high-speed nanomaterial printing with sub-process-decoupled gravure printer design”, W. Scheideler, V. Subramanian, ASME 2017 Conference on Smart Materials, Adaptive Structures, and Intelligent Systems, Snowbird, UT, Sept 18-20, 2017
9. “Development of a printed cathode and catalyst layer for printed zinc-air batteries, R. Kumar, N. Williams, and V. Subramanian, 232nd ECS Meeting, National Harbor, MD, Oct 1-5, 2017.
10. “UV-annealing-enhanced stability in high-performance printed InOx transistors, W. Scheideler, V. Subramanian, 2017 IEEE Electron Devices Technology and Manufacturing Conference (EDTM), Toyama, Japan, Feb 28-Mar 2, 2017.
11. “Inkjet-printed Four-Terminal Microelectromechanical Relays for 3-Dimensional Logic Applications” S. Cheung, M. Karim, H-J Kwon, T. Lee, and V. Subramanian, 2017 Spring Meeting of the Materials Research Society, Pheonix, AZ, April 17-21, 2017.
12. “Fluid mechanical proximity effects in high-resolution gravure printing for printed electronics”, G Grau, WJ Scheideler, V Subramanian, 69th Annual Meeting of the APS Division of Fluid Dynamics, Portland, OR, Nov 20-22, 2016
13. “Systematic Ink Design and Solubility Enhancement via Genetic Algorithm for Nanoparticle-based Inkjet Inks”, J. Sadie, H. Nallan, S. Volkman, V. Subramanian, NIP & Digital Fabrication Conference (Vol. 2015, No. 1, pp. 439-442). Society for Imaging Science and Technology.
14. M. Ahosan Ul Karim, S. Chung, E. Alon, V. Subramanian, “Stress-tolerant fully inkjet-printed Reed Relays”, IEEE International Conference on Solid-State Sensors, Actuators and Microsystems (TRANSDUCERS) (pp. 568-571), 2015.
15. “High-resolution gravure printed lines: proximity effects and design rules”, G. Grau, W. J. Scheideler, V. Subramanian, SPIE Organic Photonics+ Electronics (pp. 95690B-95690B). International Society for Optics and Photonics, 2015
16. Grau, Gerd, Rungrot Kitsomboonloha, and Vivek Subramanian. "Fabrication of a high-resolution roll for gravure printing of 2μm features." In SPIE Organic Photonics+ Electronics, pp. 95680M-95680M. International Society for Optics and Photonics, 2015.
17. Zeumault, Andre, and Vivek Subramanian. "Interpretation of subthreshold swing and threshold voltage in solution-processed zinc oxide TFTs." In Device Research Conference (DRC), 2015 73rd Annual, pp. 179-180. IEEE, 2015.
18. Zeumault, Andre, and Vivek Subramanian. "Anomalous process temperature scaling behavior of sol-gel ZrO x gate dielectrics: Mobility enhancement in ZnO TFTs." In Device Research Conference (DRC), 2015 73rd Annual, pp. 203-204. IEEE, 2015.

19. Scheideler, William J., Andre Zeumault, and Vivek Subramanian. "Engineering high-k La x Zr 1− x O y dielectrics for high-performance fully-solution-processed transparent transistors." In Device Research Conference (DRC), 2015 73rd Annual, pp. 205-206. IEEE, 2015.

20. "Fully Printed Transient Silver-Zinc Primary Battery", Nishita Deka, Kyle Braam, Vivek Subramanian, 2015 Spring Meeting of the Materials Research Society, San Francisco, CA, April 6-10, 2015.

21. "Perpendicular Magnetization Switching via Current induced Spin-Orbit Torques on Flexible Substrate", OukJae Lee, Long You, JaeWon Jang, Vivek Subramanian, Sayeef Salahuddin. 2015 Spring Meeting of the Materials Research Society, San Francisco, CA, April 6-10, 2015.

22. "Direct Patterning of Sol-Gel-Enhanced Silver Nanowire Electrodes by Gravure Printing", William Joseph Scheideler, Vivek Subramanian, 2015 Spring Meeting of the Materials Research Society, San Francisco, CA, April 6-10, 2015.

23. "Development of Oxidation-Resistant Cu/Ag Alloyed Particles for Realization of Low-Resistance, Low-Cost Printed Conductors", Steven K Volkman, Vivek Subramanian, 2015 Spring Meeting of the Materials Research Society, San Francisco, CA, April 6-10, 2015.

24. "Perpendicular Magnetization Switching via Current induced Spin-Orbit Torques on Flexible Substrate", OukJae Lee, Long You, Jaewon Jang, Vivek Subramanian, Sayeef Salahuddin, APS Bulletin of the American Physical Society. APS March Meeting 2015 Volume 60, Number 2. San Antonio, TX, March 2–6, 2015

25. "Gravure-Printing Transparent Sol-Gel Conductors on Flexible Glass Substrates", William Joseph Scheideler, Jaewon Jang, Vivek Subramanian, 2014 Fall Meeting of the Materials Research Society, Boston, MA, Nov 30 – Dec 6, 2014.

26. "High performance printed organic transistors using a novel scanned thermal annealing technology," G. Grau, R. Kitsomboonloha, H. Kang, and V. Subramanian, LOPE-C, Munich, 2014.

27. "High-Performance Organic TFTs using High-Resolution Gravure Printed Electrodes", R. Kitsomboonloha, H. Kang, V. Subramanian, 2013 Fall Meeting of the Materials Research Society, Boston, Ma, Dec 1-6, 2013

28. "Effect of Substrate Roughness on the Performance of Printed OTFTs on Paper Substrates", G. Grau and V. Subramanian, 2013 Fall Meeting of the Materials Research Society, Boston, Ma, Dec 1-6, 2013.

29. "Simulation and Experimental Characterization of Cell Filling During Highly-Scaled Gravure Printing for Printed Electronics Applications", A. Cen, R. Kitsomboonloha, and V. Subramanian, 2013 Fall Meeting of the Materials Research Society, Boston, Ma, Dec 1-6, 2013.

30. ***Best paper award*** "Droplet-on-demand Inkjet-Filled TSVs as a pathway to cost-efficient chip stacking", J. Sadie, N. Quack, M. Wu, and V. Subramanian, IMAPS 2013 - 46th International Symposium on Microelectronics, Orlando, FL, Sept 30 – Oct 3, 2013.

31. "Through silicon vias and thermocompression bonding using inkjet-printed gold nanoparticles for heterogeneous MEMS Integration", N. Quack, J. Sadie, V. Subramanian, and M. C. Wu, The 17th International Conference on Solid-State Sensors, Actuators and Microsystems, Barcelona, Spain, June 16-20, 2013.

32. "Micro-relay reliability improvement by inkjet-printed microshell encapsulation", Yenhao Chen, Eung Seok Park, I-Ru Chen, Louis Hutin, Vivek Subramanian, Tsu-Jae King Liu, The 17th International Conference on Solid-State Sensors, Actuators and Microsystems, Barcelona, Spain, June 16-20, 2013.

33. "Understanding the Enhanced Mobility of Transparent Metal-Oxide Semiconductor Thin-Film Transistors Utilizing High-k Dielectrics" Andre Zeumault, Jaewon Jang, Vivek Subramanian, 2013 Large Area, Organic and Printed Electronics Conference (LOPE-C), Munich, Germany, June 11-13, 2013.

34. "High Performance Solution-Processed Thin-Film Transistors Based on In2O3 Nanocrystals: Investigating Effects of Annealing Conditions and Gate Dielectric", Sarah L. Swisher, Steve Volkman, and Vivek Subramanian, 2013 Large Area, Organic and Printed Electronics Conference (LOPE-C), Munich, Germany, June 11-13, 2013.

35. "Printed Transistors on Paper: Towards Smart Consumer Product Packaging", Gerd Grau, Rungrot Kitsomboonloha, Sarah Swisher, Hongki Kang and Vivek Subramanian, 2013 Large Area, Organic and Printed Electronics Conference (LOPE-C), Munich, Germany, June 11-13, 2013.

36. "Inkjetted Inorganic Transistors using a Sol-gel Processed SnO2 Semiconductor and Sb-doped SnO2 Electrodes", Jaewon Jang, Eung Seok Park, Hongki Kang and Vivek Subramanian, Materials Research Society Fall 2012 Meeting, Boston, MA, Nov 25-30, 2012

37. ***Best Paper Award*** "Demonstration of Inkjet Printed Nanoparticle-based Inks for Solder Bump Replacement", Jacob Sadie, Steven Volkman, and Vivek Subramanian, 45th International Symposium on Microelectronics (IMAPS 2012), San Diego, CA, September 9 - 13, 2012

38. "Experimental study of the residue film in direct gravure printing of electronics", Rungrot Kitsomboonloha, Umut Ceyhan, SJS Morris, Vivek Subramanian, 65th Annual Meeting of the APS Division of Fluid Dynamics, Volume 57, Number 17, San Diego, California, November 18–20, 2012

39. "Lubrication analysis of the nanometric coating film deposited during gravure printing", Umut Ceyhan, Rungrot Kitsomboonloha, SJS Morris, Vivek Subramanian, 65th Annual Meeting of the APS Division of Fluid Dynamics, Volume 57, Number 17, San Diego, California, November 18–20, 2012

40. "A Simple Model of Highly Scaled Gravure Printing", R. Kitsomboonloha, S. Morris and V. Subramanian, 2012 Large Area Organic and Printed Electronics Conference (LOPE-C), Munich, Germany, July 2012

41. "Development and characterization of an air-stable printed silver-zinc battery", K. Braam, S. K. Volkman, and V. Subramanian, 2012 Large Area Organic and Printed Electronics Conference (LOPE-C), Munich, Germany, July 2012.

42. "A very reliable multilevel YSZ resistive switching memory", F. Pan, J. Jang, and V. Subramanian, 70th Annual Device Research Conference (DRC), 18-20 June 2012, pp. 217 - 218

43. "High performance solution-processed thin-film transistors based on In2O3 nanocrystals", S. L. Swisher, S. Volkman, K. Braam, J. Jang, V. Subramanian, 70th Annual Device Research Conference (DRC), 18-20 June 2012, pp. 241 - 242

44. "A Mixed-Signal EEG Interface Circuit For Use In First Year Electronics Courses,", V. Lee, J. Monski, W. Williams, B. Muthuswamy, T. Swiontek, M. Maharbiz, V. Subramanian, F. Kovac, Proceedings of the 2012 IEEE International Symposium on Circuits and Systems (ISCAS), pp. 2689 – 2692, May 2012.

45. "A novel Yittrium Stabilized Zirconia based resistive switching memory", Feng Pan, Jaewon Jang, Vivek Subramanian, 2012 Spring Materials Research Meeting.

46. "Resistance Switching Memory Device with Ag2Se Nano-particle Aqueous Ink", Jaewon Jang, Feng Pan, Kyle Braam and Vivek Subramanian, 2012 Spring Materials Research Meeting.

47. "Highly-Scaled Gravure Printed organic TFTs with 10μm channel length on Plastic with 300 kHz operation", Hongki Kang, Rungrot Kitsomboonloha, Jaewon Jang, and Vivek Subramanian, 2012 Spring Materials Research Meeting.

48. "Inkjet-Printed Microshell Encapsulation: A New Zero-Level Packaging Technology", Eung Seok Park, Jaeseok Jeon, Vivek Subramanian, and Tsu-Jae King Liu, The 25th International Conference on Micro Electro Mechanical Systems, Paris, France, January 29 – February 2, pp. 257-230,2012.

49. "Inkjet-Printed Micro-Electro-Mechanical Switches", Eung Seok Park, Yenhao Chen, Tsu-Jae King Liu, and Vivek Subramanian, 2011 International Electron Device Meeting, 29.2.1-29.2.4, 2011.

50. "A New Candidate for High Performance Transparent Electronic Circuits: Sol-gel Based SnO2/ZrO2 Thin Film Transistors", Jaewon Jang, Rungrot Kitsomboonloha, and Vivek Subramanian, 2011 International Electron Device Meeting, 14.7.1-14.7.3, 2011

51. "Measurement, analysis, and modeling of 1/f noise in pentacene TFTs ", H. Kang and V. Subramanian, 2011 Large Area, Organic, and Printed Electronic Convention (LOPE-C), Frankfurt, Germany, June 2011.

52. "Inkjet Printed Heaters and Resistive Temperature Detectors for Biological Microfluidic Applications", Lakshmi Jagannathan, Samantha Cronier, Walter Li, Dwight Williams, Vivek Subramanian, 2011 Large Area, Organic,and Printed Electronic Convention (LOPE-C), Frankfurt, Germany, June 2011

53. "A comprehensive simulation study on metal conducting filament formation in resistive switching memories", F. Pan, S. Yin, and V. Subramanian, 3rd International Memory Workshop, May 22nd-25th, Monterey, CA, 2011.

54. "Rotational optical alignment for array based free space board-to-board optical interconnect with zero power hold", J. Chou, Y. Kyoungsik, T. Bakhishev, D. Horsley, T. Walmsley, S. Mathai, M. Tan, S.Y. Wang, V. Subramanian, M. Wu, 2010 IEEE 23rd International Conference on Micro Electro Mechanical Systems (MEMS), , pp.807-810, 24-28 Jan. 2010

55. "Electrical Characterization of close-packed ZnSe Nanoparticle Films", J. Jang, V. Subramanian, Materials Research Society Fall Meeting, December, 2010

56. "Synthesis, growth, and phase transitions in iron sulfide nanoparticles", J. Jang, V. Subramanian, Materials Research Society Fall Meeting, December 2010

57. “Methodology for Inkjet Printing Partially Wetting Films”, D. Soltman, B. Smith, H. Kang, S. Morris, and V. Subramanian, IS&T Digital Fabrication conference, Austin, TX, Sept. 19-23, 2010.

58. “A Kinetic Monte Carlo study on the dynamic Switching properties of Electrochemical Metallization RRAMs during the SET Process”, F. Pan, V. Subramanian, The International Conference on Simulation of Semiconductor Processes and Devices (SISPAD), Bologna, Italy, Sept 6 – 8, 2010.

59. “A 2D Kinetic Monte Carlo simulation of resistive switching and filament formation in electrochemical RRAMs”, F. Pan and V. Subramanian, 2010 IEEE Device Research Conference.

60. “Highly-scale gravure-printed pBTTT organic field-effect transistors: Device characteristics and Bias Stability Analysis”, R. Kitsomboonloha, A. de la Fuente and V. Subramanian, 2010 Large Area Organic, and Printed Electronics Convention (LOPE-C), Frankfurt, Germany, June 2010.

61. “Downscaling of all inkjet printed, fully self-aligned organic circuits”, H-Y. Tseng and V. Subramanian, 2010 Large Area Organic, and Printed Electronics Convention (LOPE-C), Frankfurt, Germany, June 2010.

62. “Methodology for two dimensional pattern generation in inkjet printing”, D. Soltman and V. Subramanian, 2010 Large Area Organic, and Printed Electronics Convention (LOPE-C), Frankfurt, Germany, June 2010.

63. “Solution-Processed Non-volatile Filament Memory Based on ZnO Nanoparticle Films”, T. Bakhishev and V. Subramanian, 2010 Large Area Organic, and Printed Electronics Convention (LOPE-C), Frankfurt, Germany, June 2010.

64. “Printable Ag2O Cathodes for Silver-Zinc Batteries”, K. Braam, S. K. Volkman, and V. Subramanian, 2010 Spring meeting of the Materials Research Society, San Francisco, CA, April 2010.

65. “Ink-Jet Printed Conductors Based on Reduced Graphene Oxide”, T. Bakhishev, J. T. Robinson, P. E. Sheehan, Z. Wei and V. Subramanian, 2010 Spring meeting of the Materials Research Society, San Francisco, CA, April 2010.

66. “Hydrostatic concerns in inkjet-printed films”, H. Kang, D. Soltman, and V. Subramanian, 2010 Spring meeting of the Materials Research Society, San Francisco, CA, April 2010.

67. “Dielectric Breakdown and Kinetic Monte Carlo Simulation of Metal Filament Retention RESET Processes for Resistive Switches “, F. Pan and V. Subramanian, 2010 Spring meeting of the Materials Research Society, San Francisco, CA, April 2010.

68. “Considerations for pattern generation in inkjet-printed electronics”, Dan Soltman, Hongki Kang, Vivek Subramanian, SPIE Advanced Lithography, San Jose, CA, February, 2010

69. “All Inkjet Printed Self-Aligned Transistors and Circuits Applications”, Huai-Yuan Tseng and Vivek Subramanian, 2009 International Electron Device Meeting, Baltimore, MD., Dec, 2009

70. “Printed detection and resonant circuit for AM radio”, Jinsoo Noh; Namsoo Lim; Jaeyoung Kim; Subramanian, V.; Gyoujin Cho; IEEE International Symposium on Assembly and Manufacturing, pp.167-170, 17-20 Nov. 2009

71. “Optimization of inkjet-based process modules for printed transistor circuits”, Huai-Yuan Tseng, Shong Yin, Vivek Subramanian, Digifab, Louisville, KY, October 2009

72. “All Inkjet Printed Self-Aligned Transistors for Low Cost RFID Applications”, Huai-Yuan Tseng, Vivek Subramanian, 2009 IEEE Device Research Conference

73. “Printing and scaling of metallic traces and capacitors using a laboratory-scale rotogravure press”, Alejandro de la Fuente Vornbrock, Jau M. Ding, Donovan Sung, Huai-Yuan Tseng, Vivek Subramanian, 2009 Flexible Electronics and Display Conference, Phoenix, AZ, Feb 2-5, 2009.

74. “Effect of Pentacene Film Formation on Detection Behavior of Organic Transistor DNA Microarrays:, Lakshmi Jagannathan and Vivek Subramanian, Materials Research Society Fall Meeting, Boston, MA, Dec 1-4, 2008

75. “Microstructure of Pentacene Films from a Pentacene Precursor”, Daniel C Huang, Shong Yin, Kanan Puntambekar, Mike Toney and Vivek Subramanian, Materials Research Society Fall Meeting, Boston, MA, Dec 1-4, 2008

76. “Solution Processed Silver Sulfide Filament Memories”, Shong Yin and Vivek Subramanian, Materials Research Society Fall Meeting, Boston, MA, Dec 1-4, 2008

77. “The Dielectric-Integrated Monolayer Field Effect Transistor (DI-mFET)”, Kinyip Phoa and Vivek Subramanian, 2008 Semiconductor Research Corporation TechCon, Austin, TX, Nov 3-4, 2008.

78. “Pentacene Characterization for Optimum DNA Immobilization”, Lakshmi Jagannathan, Vivek Subramanian, 2008 Semiconductor Research Corporation TechCon, Austin, TX, Nov 3-4, 2008

79. “Effect of Pentacene Film Formation on Detection Behavior of Organic Transistor DNA Microarrays”, Lakshmi Jagannathan and Vivek Subramanian, Materials Research Society Fall Meeting, Boston, MA, Dec 1-4, 2008.

80. “Microstructure of Pentacene Films from a Pentacene Precursor”, Daniel C Huang, Shong Yin, Kanan Puntambekar, Mike Toney and Vivek Subramanian, Materials Research Society Fall Meeting, Boston, MA, Dec 1-4, 2008

81. “Experimental and Theoretical Studies for the Optimization of Polythiophene Gas Sensor Array”, F. Liao, V. Subramanian, 214th Meeting of The Electrochemical Society, Honolulu, HI, Oct 12-17, 2008.

82. “A Novel Solder Based on Metallic Nanoparticle Inks for Low-Temperature Packaging Technology”, T. Bakhishev and V. Subramanian, 2009 TMS Annual Meeting & Exhibition, San Francisco, CA, Feb 15-19, 2009

83. “Label-free low-cost disposable DNA hybridization detection systems using organic TFTs”, Qintao Zhang, Vivek Subramanian, 2007 IEEE International Electron Device Meeting, Washington DC, Dec 10-12, 2007.

84. “Printable DNA sensor using organic transistors”, Qintao Zhang and Vivek Subramanian, Transducers 2007, Lyon, France, 3EH5.P, 2007.

85. “Organic Transistors of Molecular Integrated Semiconductor-insulator Monolayer Films Using a Room Temperature Self-assembly Process”, Kanan Puntambekar, Kinyip Phoa, Vivek Subramanian, Amanda Murphy, Clayton Mauldin, Jean M. J. Frechét, Dean M. DeLongchamp, Daniel Fischer and Michael F. Toney, Materials Research Society Spring 2007 Meeting, O11.4, 2007.

86. “Stacked Low-Power Field-Programmable Antifuse Memories for RFID on Plastic”, B. Mattis, V. Subramanian, 2006 International Electron Device Meeting, 2006, 11.7

87. “A field-programmable antifuse memory for RFID on plastic”, B. Mattis and V. Subramanian, 2006 IEEE Device Research Conference, June 2006.

88. “Iodine-doped pentacene schottky diodes for high-frequency RFID rectification”, D. Huang and V. Subramanian, 2006 IEEE Device Research Conference, June 2006.

89. “Low-Voltage Inkjetted Organic Transistors for Printed RFID and Display Applications”, S. E. Molesa, A. de la Fuente Vornbrock, P. C. Chang, V. Subramanian, University of California Berkeley, Berkeley, CA, IEEE International Electron Device Meeting Technical Digest, pp. 5.4.1-5.4.4, 2005.

90. “Monolayer Formation in Oligothiophene Based OTFTs”, Paul Chang, Amanda R. Murphy, Jean M. J. Frechet and Vivek Subramanian, 2005 Materials Research Society Fall Symposium, Paper M7.7, Boston MA, December, 2005.

91. “A novel high-Q printed inductor technology for RFID applications”, David Redinger and Vivek Subramanian, 2005 Materials Research Society Fall Symposim, Paper M8.7, Boston MA, December 2005.

92. “Solution-processed ZnO nanowire-network thin film transistors for transparent electronics”, Teymur Bakhishev, Steven K Volkman and Vivek Subramanian, 2005 Materials Research Society Fall Symposium, Paper DD5.5, Boston MA, December, 2005.

93. “Polythiophene Thin-film Transistor Array for Gas Sensing”, J. B. Lee, M. Heeney, S. Tierney, I. McCulloch, A. Murphy, J. Liu, J. Frechet, and V. Subramanian, 63rd IEEE Device Research Conference Digest, Vol 1, pp. 147-148, 2005.

94. “Measuring Structure and Order Development in Organic Semiconductor Films with Soft X-Ray Spectroscopy”, D. M. DeLongchamp, E. K. Lin, D. Fischer, S. Sambasivan, B. M. Vogel, J. M. J. Frechet, V. Subramanian, and A. R. Murphy, 2005 Annual AIChE Meeting, Cincinnati, OH, Oct 31 – Nov1, 2005.

95. “A high-performance all-inkjetted organic transistor technology”, Steven E. Molesa, Steven K. Volkman, David R. Redinger, Alejandro de la Fuente Vornbrock, and Vivek Subramanian, 2004 IEEE International Electron Device Meeting Technical Digest, pp. 1072, 2004.

96. “A novel transparent air-stable printable n-type semiconductor technology using ZnO nanoparticles”, Steven K. Volkman, Steven E. Molesa, Josephine B. Lee, Brian A. Mattis, Alejandro de la Fuente Vornbrock, Teymur Bakhishev, and Vivek Subramanian, 2004 IEEE International Electron Device meeting Technical Digest, pp. 769, 2004.

97. “Structure and order development in organic semiconductor films”, Dean M DeLongchamp, Erin Jablonski, Sharadha Sambasivan, Daniel Fischer, Eric K Lin, Steven Volkman, Paul Chang, Vivek Subramanian, 2004 Annual AIChE Meeting, Austin, TX, Nov 7-12, 2004.

98. ***Best paper award*** "Single-monolayer inkjetted oligothiophene organic TFTs exhibiting high performance and low leakage", P. C. Chang,, S. E. Molesa, A. R. Murphy, J. M. J. Fréchet, and V. Subramanian, 62nd IEEE Device Research Conference Conference Digest, Pages 183 - 184 vol.1, 2004.

99. "High-performance inkjet-printed pentacene transistors for ultra-low-cost RFID applications.", Steven Molesa, Mark Chew, David Redinger, Steven K Volkman, and Vivek Subramanian, 2004 Mat. Res. Soc. Spring Meeting

100. "Ink-Jetted Silver/Copper Conductors for Printed RFID Applications", Steven K. Volkman, Yunan Pei, David Redinger, Shong Yin, and Vivek Subramanian, Flexible Electronics 2004—Materials and Device Technology, edited by Norbert Fruehauf, Babu R. Chalamala, Bruce E. Gnade, and Jin Jang (Mater. Res. Soc. Symp. Proc. 814, Warrendale, PA , 2004), I7.8

101. "The role of film thickness in organic thin film transistor gas sensors", Christopher Chen, Frank Liao, and Vivek Subramanian, 2004 Mat. Res. Soc. Spring Meeting.

102. "Organic TFT Gas Sensors for Electronic Nose Applications", Frank Liao, Chris Chen, and Vivek Subramanian, 2004 Mat. Res. Soc. Spring Meeting.

103. "10nm organic FETs: scaling phenomena and characterization", Josephine Lee, Paul Chang, Alex Liddle, and Vivek Subramanian, 2004 Mat. Res. Soc. Spring Meeting.

104. "Nanoscale Patterning of Organic and Molecular Electron Devices through Radiation-induced Film Modification", Brian Alexander Mattis, Yunan Pei and Vivek Subramanian, 2004 Mat. Res. Soc. Spring Meeting.

105. "Crystalline Organic Semiconducting Thin Films Cast From a Novel Thermolytic Thiophene Oligomer", Paul C. Chang, Amanda R. Murphy, Josephine B. Lee, Jean M.J. Fréchet, and Vivek Subramanian, Flexible Electronics 2004—Materials and Device Technology, edited by Norbert Fruehauf, Babu R. Chalamala, Bruce E. Gnade, and Jin Jang (Mater. Res. Soc. Symp. Proc. 814, Warrendale, PA , 2004), I12.4.

106. "Measurements of the transient photoconductivity of single crystals of pentacene", C. Weber, M. Langner, J. Orenstein, T. Le, V. Subramanian, V. Butko, A. Ramirez, American Physical Society, Annual APS March Meeting 2003, March 3-7, 2003, , abstract #Y16.015

107. "Organic transistors on fibers: A first step towards electronic textiles", Josephine B. Lee and Vivek Subramanian, IEEE International Electron Device Meeting Technical Digest, pp. 8.3.1, 2003.

108. "Inkjetted Passive Components on Plastic Substrate for RFID", D. Redinger, R. Farshchi, and V. Subramanian, 2003 IEEE Device Research Conference Conference Digest, pp. 187-188, 2003.

109. "Effect of Thermal Cycling on performance of poly(3-hexyl)thiophene transistors", B. Mattis, P. Chang, and V. Subramanian, Proceedings of the Materials Research Society Spring 2003 meeting, Symposium: Organic and Polymeric Materials and Devices, Editors: Paul W.M. Blom, Neil C. Greenham, Christos D. Dimitrakopoulos, C. Daniel Frisbie, MRS Proceedings Volume 771, L10.35, 2003.

110. "High-quality inkjet-printed multilevel interconnects and inductive components on plastic for ultra-low-cost RFID applications", S. Molesa, D. Redinger, D. Huang, and V. Subramanian, Proceedings of the Materials Research Society Spring 2003 meeting, Symposium H: Flexible Electronics--Materials and Device Technology, Editors: Norbert Fruehauf, Babu R. Chalamala, Bruce E. Gnade, Jin Jang, MRS Proceedings Volume 769, H8.3, 2003.

111. "Inkjetted organic transistors using a novel pentacene precursor", S. Volkman, S. Molesa, B. Mattis, P. C. Chang, and V. Subramanian, Proceedings of the Materials Research Society Spring 2003 meeting, Symposium H: Flexible Electronics--Materials and Device Technology, Editors: Norbert Fruehauf, Babu R. Chalamala, Bruce E. Gnade, Jin Jang, MRS Proceedings Volume 769, H11.7, 2003.

112. "Flexonics", J. Canny, J. Risner, and V. Subramanian, presented at The Fifth International Workshop on Algorithmic Foundations of Robotics, 2002.

113. "Inkjetted gold conductors for electronics on plastics", Daniel C. Huang, Frank Liao, and Vivek Subramanian, presented at Materials Research Society Spring 2002 meeting.

114. "Applications of Printing Technology in Organic Electronics and Display Fabrication", V. Subramanian, presented at the Half Moon Bay Maskless Lithography Workshop, DARPA/SRC, Half Moon Bay, CA, Nov 9-10, 2000.

115. "A 20 nm Gate-Length Ultra-Thin Body p-MOSFET with Silicide Source/Drain", J. Kedzierski, P. Xuan, V. Subramanian, E. Anderson, J. Bokor, T.-J. King, and C. Hu, presented at the Silicon Nanolectronics Workshop 2000.

116. "60nm Planarized Ultra-thin Body Solid Phase Epitaxy MOS-FETs", P. Xuan, J. Kedzierski, V. Subramanian, J. Bokor, T-J. King, C. Hu, 58th Annual Device Research Conference Digest, Pages 67 – 68, 2000.

117. "High performance 200nm single-grain TFTs fabricated using a self-aligned germanium seeding technology", P. Kalavade, A. R. Joshi, V. Subramanian and K. C. Saraswat, presented at the 2000 Materials Research Society Spring Symposium.

118. "Nanoscale SiGe-Channel Ultra-Thin-Body Silicon-on-Insulator P-MOSFETs", Y-C. Yeo, V. Subramanian, J. Kedzierski, P. Xuan, T-J. King, J. Bokor, and C. Hu, presented at the 1999 International Semiconductor Device Research Symposium.

119. "Ultra-thin body SOI MOSFET for Deep-sub-tenth Micron Era", Y-K. Choi, K. Asano, N. Lindert, V. Subramanian, T-J. King, J. Bokor and C. Hu, 1999 IEEE International Electron Device Meeting Technical Digest, pp. 919-921, 1999.

120. "Sub 50-nm FinFET: PMOS", X. Huang, W-C. Lee, C. Kuo, D. Hisamoto, L. Chang, J. Kedzierski, E. Anderson, H. Takeuchi, Y-K. Choi, K. Asano, V. Subramanian, T-J. King, J. Bokor and C. Hu, 1999 IEEE International Electron Device Meeting Technical Digest, pp. 67-70, 1999.

121. "A bulk-Si-compatible ultrathin-body SOI technology for sub-100nm MOSFETs", V. Subramanian, J. Kedzierski, N. Lindert, H. Tam, Y. Su, J. McHale, K. Cao, T-J. King, J. Bokor, and C. Hu, Proceedings of the 57th Annual Device Research Conference, pp. 28-29, 1999.

122. "Process issues for deep-submicron electron beam lithography at the Stanford Nanofabrication Facility", V. Subramanian and M. King, Electron Beam Lithography for Nanostructure Fabrication Workshop, Cornell University, Ithaca, NY, January 14-15, 1999.

123. "Laterally Crystallized Polysilicon TFTs Using Patterned Light Absorption Masks", V. Subramanian and K. C. Saraswat, Proceedings of the 55th Annual Device Research Conference, 1997, pp. 54-55.

124. "A Novel Technique for 3-D Integration: Ge-seeded Laterally Crystallized TFTs", V. Subramanian and K. C. Saraswat, 1997 Symposium on VLSI technology Digest of Technical Papers, 1997, pp. 97-98.

125. "Response surface characterization of the deposition of LPCVD SiGe for solid-phase crystallized poly-TFTs", V. Subramanian, K. C. Saraswat, H. Hovagimian, and J. Mehlhaff , Proceedings of the Second International Workshop in Statistical Metrology, 1997, pp. 94-97.

126. "Design and Characterization of SiGe TFT Devices and Process using Stanford's Test Chip Design Environment", M. V. Kumar, V. Subramanian, K. C. Saraswat, J. D. Plummer, and W. Lukaszek, Proceedings of the 1997 IEEE International Conference on Microelectronic Test Structures, pp. 143-145.

127. "Response surface optimization for high-performance solid-phase crystallized silicon-germanium thin film transistors", V. Subramanian, K. C. Saraswat, H. Hovagimian, and J. Mehlhaff, Proceedings of the SPIE - The International Society for Optical Engineering, vol.3014, p. 127-32, 1997.

128. "Optimization and Modeling of Silicon-Germanium Thin Film Transistors for AMLCD Applications using a Plackett-Burman Experimental Design V. Subramanian, K. C. Saraswat, H. Hovagimian, and J. Mehlhaff, First International Workshop on Statistical Metrology, Honolulu, Hawaii, June 9, 1996

129. "Accelerated Breakdown in Thin Oxide Films due to Interfacial Stress and Carrier Depletion", V. Subramanian, N. Bhat, and K. C. Saraswat, Materials Reliability in Microelectronics VI, MRS Symposium proceedings, 1996, pp. 323-328

130. "A Novel Technique for In-Situ Monitoring of Crystallinity and Temperature during Rapid Thermal Annealing of Thin Si/Si-Ge films on Quartz/Glass", V. Subramanian, L. Degertekin, P. Dankoski, B. T. Khuri-Yakub, and K. C. Saraswat, Flat Panel Display Materials II, MRS Symposium, pp.267-72, 1996.