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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
11/338,007	01/23/2006	James A. Cooper	3220-79132	4085
23643 7590 04/04/2007 BARNES & THORNBURG LLP 11 SOUTH MERIDIAN INDIANAPOLIS, IN 46204			EXAMINER PATTON, PAUL E	
			ART UNIT	PAPER NUMBER
			2822	
SHORTENED STATUTORY PERIOD OF RESPONSE		MAIL DATE	DELIVERY MODE	
3 MONTHS		04/04/2007	PAPER	

**Please find below and/or attached an Office communication concerning this application or proceeding.**

If NO period for reply is specified above, the maximum statutory period will apply and will expire 6 MONTHS from the mailing date of this communication.

**Office Action Summary**

Application No.

11/338,007

Applicant(s)

COOPER ET AL.

Examiner

Paul E. Patton

Art Unit

2822

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

- 1) ☒ Responsive to communication(s) filed on 23 January 2006.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

- 4) ☒ Claim(s) 1-23 is/are pending in the application.
- 4a) Of the above claim(s) \_\_\_\_\_ is/are withdrawn from consideration.
- 5) ☐ Claim(s) \_\_\_\_\_ is/are allowed.
- 6) ☒ Claim(s) 1-23 is/are rejected.
- 7) ☐ Claim(s) \_\_\_\_\_ is/are objected to.
- 8) ☐ Claim(s) \_\_\_\_\_ are subject to restriction and/or election requirement.

**Application Papers**

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☒ The drawing(s) filed on 23 January 2006 is/are: a) ☒ accepted or b) ☐ objected to by the Examiner.  
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).  
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☒ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

**Priority under 35 U.S.C. § 119**

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some \* c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
  2. ☐ Certified copies of the priority documents have been received in Application No. \_\_\_\_\_.
  3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

\* See the attached detailed Office action for a list of the certified copies not received.

**Attachment(s)**

- |  |   |
|--|---|
| 1) <input checked="" type="checkbox"/> Notice of References Cited (PTO-892)          | 4) <input type="checkbox"/> Interview Summary (PTO-413)           |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948) | Paper No(s)/Mail Date. _____                                      |
| 3) <input type="checkbox"/> Information Disclosure Statement(s) (PTO/SB/08)          | 5) <input type="checkbox"/> Notice of Informal Patent Application |
| Paper No(s)/Mail Date _____  | 6) <input type="checkbox"/> Other: _____                          |

## **DETAILED ACTION**

### ***Oath/Declaration***

1. The oath or declaration is defective. A new oath or declaration in compliance with 37 CFR 1.67(a) identifying this application by application number and filing date is required. See MPEP §§ 602.01 and 602.02.

The oath or declaration is defective because: the signature of the second inventor is lacking.

### ***Claim Rejections - 35 USC § 102***

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

3. Claims 1, 3, 4, 9, 10 12, 13 and 15 are rejected under 35 U.S.C. 102(b) as being anticipated by Ono et al., (US 2003/0227052 A1) Ono.
4. As to claims 1,3,4,9,12, and 13, Ono discloses and shows (Fig 1), a double implanted MOS field effect transistor comprising a semiconductor substrate (10) having a first concentration of first type impurities (n+); a drift semiconductor layer (50) formed on a front side of the semiconductor substrate and having a second concentration of first type impurities less than the first concentration of first type impurities (n-); a first source region (20); a second source region (20); and a JFET region (40) defined between the first source region and the second source region, the JFET region having a third concentration of first type impurities that is greater than the second concentration

of first type impurities (n) and having a width (L) less than about 3 micrometers and a width of about one micrometer. (Paragraphs [0039] & [0041]).

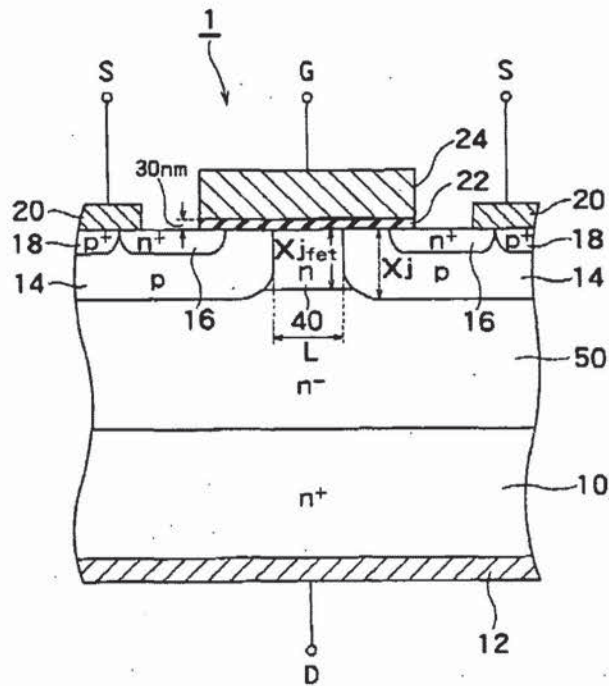


FIG. 1

5. As to claims 10 and 15, Ono shows (Fig 12) a plurality of base contact regions (18) formed in each of the first and second source regions (16), the base contact regions being smaller than the first and second source regions.





6. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

7. Claim 2 is rejected under 35 U.S.C. 103(a) as being unpatentable over Ono in view of Kumar et al., (USPAT 6,573,534.B1) Kumar.

8. Ono does not disclose that the semiconductor substrate is a silicon-carbide substrate.

9. Kumar is related to a similar MOS FET structure and discloses that the substrate is a silicon-carbide substrate (Column 1, line 40).

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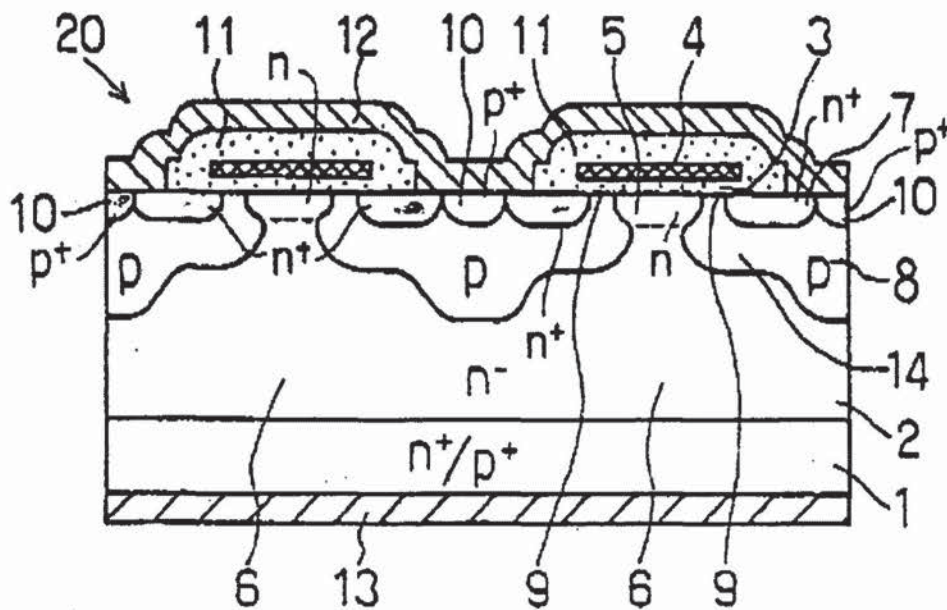
10. Kumar is evidence that a person of ordinary skill in the art would find a reason, suggestion or motivation to use a silicon-carbide substrate.

11. Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Ono by using a silicon-carbide substrate for advantages such as higher breakdown voltage and lower ON resistance according to the teachings of Kumar (Column 1, lines 27-30).

12. Claims 5 and 14 are rejected under 35 U.S.C. 103(a) as being unpatentable over Ono in view of Tokura et al., (USPAT 5,545,908).

13. Ono does not disclose that the concentration of first type impurities associated with the JFET region is at least one order of magnitude greater than the concentration of first type impurities associated with the drift region.

14. Tokura is related to a similar MOSFET structure and discloses and shows (Tokura, Fig 1) that the doping level at the JFET region (5) is  $8 \times 10^{16} \text{ cm}^{-3}$  whereas the doping level of the drift region (2) is  $5 \times 10^{15} \text{ cm}^{-3}$ . (Tokura, Column 10, lines 29-33 & Column 11, lines 54-58). Note that Tokura does not label the region between the two p doped wells on opposite sides of the gate as a JFET. However the structure in this device as well as Ono will form a parasitic JFET due to the arrangement of the layers. (Ono, Paragraph [0040]).



Tokura, Fig 1

15. Tokura is evidence that a person of ordinary skill in the art would find a reason, suggestion or motivation to have the concentration of the JFET region at least an order of magnitude greater than the concentration of the drift region.

16. Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Ono by having the concentration of the JFET region at least an order of magnitude greater than the concentration of the drift region for advantages such as reduced ON resistance according to the teachings of Tokura (Column 5, lines 60-66 & Column 8, lines 33-34).

17. Claims 6-8 and 17-21 are rejected under 35 U.S.C. 103(a) as being unpatentable over Ono in view of Zeng et al., (USPAT 6,137,139) Zeng.

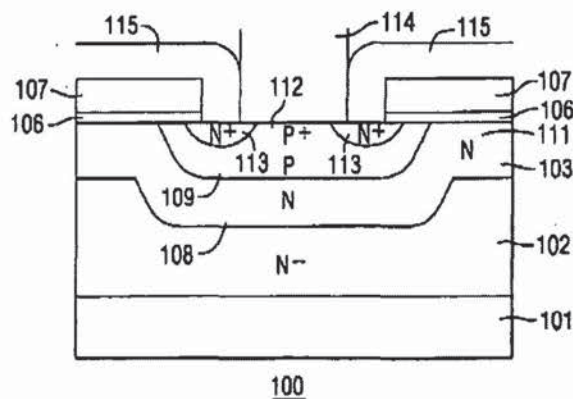
18. As to claims 6-8, Ono shows (Ono, Fig 1) the JFET region is formed directly below the gate structure and between the base doped wells formed on either side of the



gate. As noted above the parasitic JFET is a consequence of the lateral gate-source arrangement of a vertical MOSFET and would be above the current spreading layer and the drift region shown by Zeng.

19. Ono does not explicitly disclose that a current spreading layer is formed on a front side of the drift semiconductor layer; and wherein the concentration of impurities of the first type is greater than the concentration of impurities of the first type in the drift region by at least one order of magnitude.

20. Zeng discloses and shows (Fig 2C) a current spreading layer (103) formed on a front side of the drift semiconductor layer (102) wherein the concentration of impurities of the first type is greater than the concentration of impurities of the first type in the drift region by at least one order of magnitude (Zeng, Column 2, lines 64-67 & Column 3, lines 4-7).



**FIG. 2C**

21. Zeng is evidence that a person of ordinary skill in the art would find a reason, suggestion or motivation to have a current spreading layer formed on a front side of the drift semiconductor layer; and wherein the concentration of impurities of the first type is



greater than the concentration of impurities of the first type in the drift region by at least one order of magnitude.

22. Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Ono to have a current spreading layer formed on a front side of the drift semiconductor layer; and wherein the concentration of impurities of the first type is greater than the concentration of impurities of the first type in the drift region by at least one order of magnitude for advantages such as reduced on-resistance without degrading device ruggedness and reliability according to the teachings of Zeng (Column 4, lines 32-39).

23. As to claim 17, Ono discloses and shows (Ono, Fig 1), a double implanted MOS field effect transistor comprising a semiconductor substrate (10) a drift semiconductor layer (50) formed on a front side of the semiconductor substrate; a first source region (20); a second source region (20); and a JFET region (40) defined between the first source region and the second source region.

24. Ono does not disclose or show a current spreading semiconductor layer formed on a front side of the drift semiconductor layer.

25. Zeng discloses and shows (Fig 2C) a current spreading layer (103) formed on a front side of the drift semiconductor layer (102).

26. Ono shows (Ono, Fig 1) the JFET region is formed directly below the gate structure and between the base doped wells formed on either side of the gate. As noted above the parasitic JFET is a consequence of the lateral gate-source arrangement of a vertical MOSFET and would be above the current spreading layer and the drift region shown by Zeng.

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27. Zeng is evidence that a person of ordinary skill in the art would find a reason, suggestion or motivation to have a current spreading layer formed on a front side of the drift semiconductor layer.

28. Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Ono to have a current spreading layer formed on a front side of the drift semiconductor for advantages such as reduced on-resistance without degrading device ruggedness and reliability according to the teachings of Zeng (Column 4, lines 32-39)..

29. As to claims 18 and 19, Ono does not disclose a current spreading semiconductor layer having a first concentration of first type impurities and the drift semiconductor layer has a second concentration of first type impurities, the first concentration of first type impurities being greater than the second concentration by at least one order of magnitude.

30. Zeng discloses a current spreading layer wherein the concentration of impurities of the first type is greater than the concentration of impurities of the first type in the drift region by at least one order of magnitude (Zeng, Column 2, lines 64-67 & Column 3, lines 4-7).

31. Zeng is evidence that a person of ordinary skill in the art would find a reason, suggestion or motivation to have a current spreading layer wherein the concentration of impurities of the first type is greater than the concentration of impurities of the first type in the drift region by at least one order of magnitude.

32. Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Ono to have a current spreading layer wherein



the concentration of impurities of the first type is greater than the concentration of impurities of the first type in the drift region by at least one order of magnitude for advantages such as reduced on-resistance without degrading device ruggedness and reliability according to the teachings of Zeng (Column 4, lines 32-39).

33. As to claim 20, Ono as modified by Zeng discloses the JFET region has a width of about three micrometers or less (Ono, Paragraph [0041]).

34. As to claim 21, Ono as modified by Zeng shows (Fig 12) a plurality of base contact regions (18) formed in each of the first and second source regions (16), the base contact regions being smaller than the first and second source regions.

35. Claims 11 and 16 are rejected under 35 U.S.C. 103(a) as being unpatentable over Ono in view of Kobayashi et al., (US2003/0052329 A1) Kobayashi.

36. As to claims 11 and 16, Ono does not explicitly disclose a plurality of source regions and a plurality of base contact regions, wherein the plurality of source regions and the plurality of base contact regions, form alternating strips of N-type doped regions and P-type doped regions, the alternating strips being substantially orthogonal to respective source electrodes formed over the first and second source regions.

37. Kobayashi shows (Fig 18) a plurality of source regions and a plurality of base contact regions, wherein the plurality of source regions (15) and the plurality of base contact regions (13), form alternating strips of N-type doped regions and P-type doped regions, the alternating strips (17) being substantially orthogonal to respective source electrodes formed over the first and second source regions.



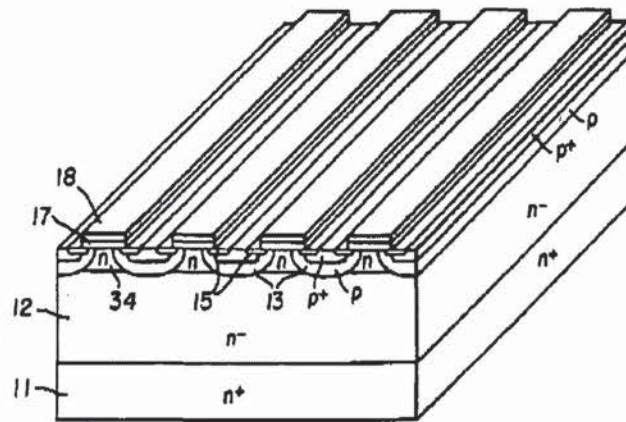


FIG. 18

38. Kobayashi is evidence that a person of ordinary skill in the art would find a reason, suggestion or motivation to form a plurality of source regions and a plurality of base contact regions, wherein the plurality of source regions and the plurality of base contact regions, form alternating strips of N-type doped regions and P-type doped regions, the alternating strips being substantially orthogonal to respective source electrodes formed over the first and second source regions.

39. Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Ono to form a plurality of source regions and a plurality of base contact regions, wherein the plurality of source regions and the plurality of base contact regions, form alternating strips of N-type doped regions and P-type doped regions, the alternating strips being substantially orthogonal to respective source electrodes formed over the first and second source regions for advantages such as reduced electric field strength according to the teachings of Kobayashi (Paragraph [0034]).

40. Claim 22 is rejected under 35 U.S.C. 103(a) as being unpatentable over Ono in view of Zeng and further in view of Kobayashi.

41. Ono as modified by Zeng does not explicitly disclose a plurality of source regions and a plurality of base contact regions, wherein the plurality of source regions and the plurality of base contact regions, form alternating strips of N-type doped regions and P-type doped regions, the alternating strips being substantially orthogonal to respective source electrodes formed over the first and second source regions.

42. Kobayashi shows (Fig 18) a plurality of source regions and a plurality of base contact regions, wherein the plurality of source regions (15) and the plurality of base contact regions (13), form alternating strips of N-type doped regions and P-type doped regions, the alternating strips (17) being substantially orthogonal to respective source electrodes formed over the first and second source regions.

43. Kobayashi is evidence that a person of ordinary skill in the art would find a reason, suggestion or motivation to form a plurality of source regions and a plurality of base contact regions, wherein the plurality of source regions and the plurality of base contact regions, form alternating strips of N-type doped regions and P-type doped regions, the alternating strips being substantially orthogonal to respective source electrodes formed over the first and second source regions.

44. Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Ono as modified by Zeng to form a plurality of source regions and a plurality of base contact regions, wherein the plurality of source regions and the plurality of base contact regions, form alternating strips of N-type doped regions and P-type doped regions, the alternating strips being substantially orthogonal



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to respective source electrodes formed over the first and second source regions for advantages such as reduced electric field strength according to the teachings of Kobayashi (Paragraph [0034]).

45. Claim 23 is rejected under 35 U.S.C. 103(a) as being unpatentable over Ono in view of Zeng and further in view of Tokura and Kumar.

46. Ono discloses and shows (Fig 1), a double implanted MOS field effect transistor comprising a semiconductor substrate (10) having a first concentration of first type impurities (n+); a drift semiconductor layer (50) formed on a front side of the semiconductor substrate and having a second concentration of first type impurities less than the first concentration of first type impurities (n-); a first source region (20); a second source region (20); and a JFET region (40) defined between the first source region and the second source region, the JFET region having a fourth concentration of first type impurities that is greater than the second concentration of first type impurities (n) and having a width (L) less than about 3 micrometers and a width of about one micrometer. (Paragraphs [0039] & [0041]).

47. Ono does not disclose that the semiconductor substrate is silicon-carbide.

48. Kumar discloses that the substrate is a silicon-carbide substrate (Column 1, line 40).

49. Kumar is evidence that a person of ordinary skill in the art would find a reason, suggestion or motivation to use a silicon-carbide substrate.

50. Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Ono by using a silicon-carbide substrate for



advantages such as higher breakdown voltage and lower ON resistance according to the teachings of Kumar (Column 1, lines 27-30).

51. Furthermore, Ono as modified by Kumar does not explicitly disclose that a current spreading layer is formed on a front side of the drift semiconductor layer; and wherein the concentration of impurities of the first type is greater than the concentration of impurities of the first type in the drift region.

52. Zeng discloses and shows (Fig 2C) a current spreading layer (103) formed on a front side of the drift semiconductor layer (102) wherein the concentration of impurities of the first type is greater than the concentration of impurities of the first type in the drift region (Zeng, Column 2, lines 64-67 & Column 3, lines 4-7).

53. Zeng is evidence that a person of ordinary skill in the art would find a reason, suggestion or motivation to have a current spreading layer formed on a front side of the drift semiconductor layer; and wherein the concentration of impurities of the first type is greater than the concentration of impurities of the first type in the drift region .

54. Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Ono as modified by Kumar to have a current spreading layer formed on a front side of the drift semiconductor layer; and wherein the concentration of impurities of the first type is greater than the concentration of impurities of the first type in the drift region for advantages such as reduced on-resistance without degrading device ruggedness and reliability according to the teachings of Zeng (Column 4, lines 32-39).

55. Lastly, Ono as modified by Kumar and Zeng does not disclose that the concentration of first type impurities associated with the JFET region is greater than the concentration of first type impurities associated with the drift region.

56. Tokura is related to a similar MOSFET structure and discloses and shows (Tokura, Fig 1) that the doping level at the JFET region (5) is  $8 \times 10^{16} \text{ cm}^{-3}$  whereas the doping level of the drift region (2) is  $5 \times 10^{15} \text{ cm}^{-3}$ . (Tokura, Column 10, lines 29-33 & Column 11, lines 54-58). Note that Tokura does not label the region between the two p-doped wells on opposite sides of the gate as a JFET. However the structure in this device as well as Ono will form a parasitic JFET due to the arrangement of the layers. (Ono, Paragraph [0040]).

57. Tokura is evidence that a person of ordinary skill in the art would find a reason, suggestion or motivation to have the concentration of the JFET region greater than the concentration of the drift region.

58. Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Ono as modified by Kumar and Zeng by having the concentration of the JFET region at least an order of magnitude greater than the concentration of the drift region for advantages such as reduced ON resistance according to the teachings of Tokura (Column 5, lines 60-66 & Column 8, lines 33-34).


**Conclusion**

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Paul E. Patton whose telephone number is 571-272-9762. The examiner can normally be reached on 7:00 - 5:30 Monday through Thursday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Zandra Smith can be reached on 571-272-2429. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

PEP

  
Zandra V. Smith  
Supervisory Patent Examiner  
30 March 2007

Paul E Patton  
Examiner  
Art Unit 2822



<b>Notice of References Cited</b>	Application/Control No. 11/338,007	Applicant(s)/Patent Under Reexamination COOPER ET AL.	
	Examiner Paul E. Patton	Art Unit 2822	Page 1 of 1

**U.S. PATENT DOCUMENTS**

*		Document Number Country Code-Number-Kind Code	Date MM-YYYY	Name	Classification
*	A	US-2003/0227052	12-2003	Ono et al.	257/341
*	B	US-5,545,908	08-1996	Tokura et al.	257/341
*	C	US-6,573,534 B1	06-2003	Kumar et al.	257/77
*	D	US-2003/0052329 A1	03-2003	Kobayashi et al.	257/135
*	E	US-6,137,139	10-2000	Zeng et al.	257/342
*	F	US-6,552,391 B2	04-2003	Zeng et al.	257/342
*	G	US-2003/0205829 A1	11-2003	Boden, Milton J. JR.	257/921
	H	US-			
	I	US-			
	J	US-			
	K	US-			
	L	US-			
	M	US-			

**FOREIGN PATENT DOCUMENTS**

*		Document Number Country Code-Number-Kind Code	Date MM-YYYY	Country	Name	Classification
	N					
	O					
	P					
	Q					
	R					
	S					
	T					

**NON-PATENT DOCUMENTS**

*		Include as applicable: Author, Title Date, Publisher, Edition or Volume, Pertinent Pages)
	U	
	V	
	W	
	X	

\*A copy of this reference is not being furnished with this Office action. (See MPEP § 707.05(a).)  
Dates in MM-YYYY format are publication dates. Classifications may be US or foreign.



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Bib Data Sheet

CONFIRMATION NO. 4085

<b>SERIAL NUMBER</b> 11/338,007	<b>FILING OR 371(c) DATE</b> 01/23/2006 <b>RULE</b>	<b>CLASS</b> 257	<b>GROUP ART UNIT</b> 2809	<b>ATTORNEY DOCKET NO.</b> 3220-79132
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## APPLICANTS

James A. Cooper, West Lafayette, IN;  
 Asmita Saha, West Lafayette, IN;

## \*\* CONTINUING DATA \*\*\*\*\*

This appln claims benefit of 60/646,152 01/21/2005

## \*\* FOREIGN APPLICATIONS \*\*\*\*\*

## IF REQUIRED, FOREIGN FILING LICENSE GRANTED \*\*

03/01/2006

Foreign Priority claimed <input type="checkbox"/> yes <input checked="" type="checkbox"/> no	<b>STATE OR COUNTRY</b> IN	<b>SHEETS DRAWING</b> 4	<b>TOTAL CLAIMS</b> 23	<b>INDEPENDENT CLAIMS</b> 4
35 USC 119 (a-d) conditions met <input type="checkbox"/> yes <input checked="" type="checkbox"/> no <input type="checkbox"/> Met after Allowance				
Verified and Acknowledged Examiner's Signature <i>[Signature]</i> Initials <i>[Initials]</i>				


## ADDRESS

23643

## TITLE

High-voltage power semiconductor device

<b>FILING FEE RECEIVED</b> 1480	FEES: Authority has been given in Paper No. _____ to charge/credit DEPOSIT ACCOUNT No. _____ for following:	<input type="checkbox"/> All Fees <input type="checkbox"/> 1.16 Fees ( Filing ) <input type="checkbox"/> 1.17 Fees ( Processing Ext. of time ) <input type="checkbox"/> 1.18 Fees ( Issue ) <input type="checkbox"/> Other _____ <input type="checkbox"/> Credit
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<b>Index of Claims</b> 	<b>Application/Control No.</b> 11338007	<b>Applicant(s)/Patent Under Reexamination</b> COOPER ET AL.
	<b>Examiner</b> Patton, Paul E	<b>Art Unit</b> 2822

✓	<b>Rejected</b>
=	<b>Allowed</b>


-	<b>Cancelled</b>
÷	<b>Restricted</b>

N	<b>Non-Elected</b>
I	<b>Interference</b>

A	<b>Appeal</b>
O	<b>Objected</b>

<input type="checkbox"/> Claims renumbered in the same order as presented by applicant			<input type="checkbox"/> CPA			<input type="checkbox"/> T.D.			<input type="checkbox"/> R.1.47		
CLAIM		DATE									
Final	Original	03/26/2007									
	1	✓									
	2	✓									
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	4	✓									
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	23	✓									



<b>Search Notes</b> 	<b>Application/Control No.</b> 11338007	<b>Applicant(s)/Patent Under Reexamination</b> COOPER ET AL.
	<b>Examiner</b> Patton, Paul E	<b>Art Unit</b> 2822

SEARCHED			
Class	Subclass	Date	Examiner
257	263, 256, 341, 342, 335, 339, 350, 263,	3/22/2007	PEP
438	142, 156, 176, 186, 197, 268	3/22/2007	PEP

SEARCH NOTES		
Search Notes	Date	Examiner
Search history attached	2/26/2007	PEP

INTERFERENCE SEARCH			
Class	Subclass	Date	Examiner