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11 South Meridian Street  
Indianapolis, Indiana 46204**IN THE UNITED STATES PATENT AND TRADEMARK OFFICE**

Group: 2822  
Confirmation No.: 4085  
Application No.: 11/338,007  
Invention: HIGH-VOLTAGE POWER  
SEMICONDUCTOR DEVICE  
Applicant: James A. Cooper et al.  
Filed: January 23, 2006  
Attorney  
Docket: 3220-79132  
Examiner: Patton, Paul E.

Certificate Under 37 CFR 1.8(a)

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on August 6, 2007

(Signature)

Glen M. Kellett  
(Printed Name)AMENDMENT AND REPLY

MAIL STOP AMENDMENT  
Commissioner for Patents  
P. O. Box 1450  
Alexandria, VA 22313-1450

Sir:

In response to the Office Action dated April 4, 2007, please consider the  
following:

**Amendments to the Claims** are reflected in the listing of claims which begins on  
page 2 of this paper.

**Remarks** begin on page 8 of this paper.

### AMENDMENTS TO THE CLAIMS

This listing of claims replaces all prior versions and listings of the claims in this application:

1. (Currently Amended) A metal-oxide semiconductor field-effect transistor comprising:

a semiconductor silicone-carbide substrate having a first concentration of first type impurities;

a drift semiconductor layer formed on a front side of the semiconductor substrate and having a second concentration of first type impurities less than the first concentration of first type impurities;

a current spreading semiconductor layer formed on a front side of the drift semiconductor layer;

a first source region;

a second source region; and

a JFET region formed on a front side of the current spreading semiconductor layer and defined between the first source region and the second source region, the JFET region having a third concentration of first type impurities that is greater than the second concentration of first type impurities.

2. (Cancelled)

3. (Original) The metal-oxide semiconductor field-effect transistor of claim 1, wherein the JFET region has a width of less than about three micrometers.

4. (Original) The metal-oxide semiconductor field-effect transistor of claim 3, wherein the JFET region has a width of about one micrometer.

5. (Original) The metal-oxide semiconductor field-effect transistor of claim 1, wherein the third concentration of first type impurities is at least one order of magnitude greater than the second concentration of first type impurities.

6. (Cancelled)

7. (Currently Amended) The metal-oxide semiconductor field-effect transistor of claim ~~6~~ 1, wherein the current spreading semiconductor layer has a fourth concentration of first type impurities that is greater than the second concentration of first type impurities.

8. (Original) The metal-oxide semiconductor field-effect transistor of claim 7, wherein the fourth concentration of first type impurities is at least one order of magnitude greater than the second concentration of first type impurities.

9. (Currently Amended) The metal-oxide semiconductor field-effect transistor of claim ~~6~~ 8, wherein the JFET region has a width of about one micrometer.

10. (Original) The metal-oxide semiconductor field-effect transistor of claim 1, further comprising a plurality of base contact regions formed in each of the first and the second source regions, the base contact regions being smaller than the first and second source regions.

11. (Original) The metal-oxide semiconductor field-effect transistor of claim 1, further comprising a plurality of source regions and a plurality of base contact regions, wherein the plurality of source regions and the plurality of base contact regions form alternating strips of N-type doped regions and P-type doped regions, the alternating strips being substantially orthogonal to respective source electrodes formed over the first and the second source regions.

12. (Currently Amended) A double-implanted metal-oxide semiconductor field-effect transistor comprising:

a ~~semiconductor~~ silicone-carbide substrate;

a drift semiconductor layer formed on a front side of the semiconductor substrate;

a first source region;

a plurality of first base contact regions defined in the first source region, each of the plurality of first base contact regions being spaced apart from each other;

a second source region; ~~and~~

a plurality of second base contact regions defined in the second source region, each of the plurality of second base contact regions being spaced apart from each other; and

a JFET region defined between the first source region and the second source region, the JFET region having a width less than about three micrometers.

13. (Original) The double-implanted metal-oxide semiconductor field-effect transistor of claim 12, wherein the JFET region has a width of about one micrometer.



14. (Original) The double-implanted metal-oxide semiconductor field-effect transistor of claim 12, wherein the JFET region has a first concentration of first type impurities and the drift semiconductor layer has a second concentration of first type impurities, the first concentration of first type impurities being greater than the second concentration of first type impurities.

15-16. (Cancelled)

17. (Currently Amended) A double-implanted metal-oxide semiconductor field-effect transistor comprising:

a semiconductor substrate;

a drift semiconductor layer formed on a front side of the semiconductor substrate;

a current spreading semiconductor layer formed on a front side of the drift semiconductor layer;

~~a first source region;~~

~~a second source region; and~~

a plurality of first and second source regions;

a plurality of base contact regions; and

a JFET region defined between the plurality of first source region regions and the plurality of second source region regions, the JFET region being formed on a front side of the current spreading semiconductor layer,

wherein the plurality of first and second source regions and the plurality of base contact regions form alternating strips of N-type doped regions and P-type doped regions, the alternating strips being substantially orthogonal to respective source electrodes formed over the first and the second source regions.

18. (Original) The double-implanted metal-oxide semiconductor field-effect transistor of claim 17, wherein the current spreading semiconductor layer has a first concentration of first type impurities and the drift semiconductor layer has a second concentration of first type impurities, the first concentration of first type impurities being greater than the second concentration of first type impurities.

19. (Original) The double-implanted metal-oxide semiconductor field-effect transistor of claim 18, wherein the first concentration of first type impurities is at least one order of magnitude greater than the second concentration of first type impurities.

20. (Original) The double-implanted metal-oxide semiconductor field-effect transistor of claim 17, wherein the JFET region has a width of about three micrometers or less.

21-22. (Cancelled)

23. (Original) A vertical double-implanted metal-oxide semiconductor field-effect transistor comprising:

a silicon-carbide substrate having a first concentration of first type impurities;

a drift semiconductor layer epitaxially formed on a front side of the silicon-carbide substrate and having a second concentration of first type impurities less than the first concentration of first type impurities;

a current spreading semiconductor layer epitaxially formed on a front side of the drift layer, the current spreading semiconductor layer having a third concentration of first type impurities greater than the second concentration of first type impurities;

a first source region;

a second source region; and

a JFET region defined between the first source region and the second source region and formed on a front side of the current spreading semiconductor layer, the JFET region having a width less than about three micrometers and a fourth concentration of first type impurities greater than the second concentration of first type impurities.

### REMARKS

The Office Action dated April 4, 2007 has been carefully reviewed. Claims 1-23 stand rejected in the 4/4/2007 Office Action. Additionally, the declaration filed on May 18, 2006 is found defective in the 4/4/2007 Office Action. By this amendment, claims 2, 6, 15, 16, 21, and 22 are cancelled without prejudice. Claims 1, 7, 9, 12, and 17 are amended.

### DECLARATION

The Examiner found the declaration filed on May 18, 2006 to be defective because the signature of the second named inventor, Ms. Asmita Saha, was lacking. Applicants file herewith a new declaration signed by the second named inventor, Ms. Asmita Saha. A copy of the originally filed declaration, which is signed by the first named inventor, Mr. James A. Cooper, is also included for the convenience of the Office.

### SECTION 102(e) REJECTION OF INDEPENDENT CLAIM 1

The Examiner rejected independent claim 1 under 35 U.S.C. §102(e) as being anticipated by U.S. Patent Publication No. 2003/0227052 A1 to Ono et al. (hereinafter "Ono"). This claim has been amended to include the subject matter of dependent claims 2 and 6. Claims 2 and 6 have been cancelled. Regarding claim 2, the Examiner rejected this claim under 35 U.S.C. §103(a) as being unpatentable over Ono in view of U.S. Patent No. 6,573,534 B1 to Kumar et al. (hereinafter "Kumar"). Regarding claim 6, the Examiner rejected this claim under 35 U.S.C. §103(a) as being unpatentable over Ono in view of U.S. Patent No. 6,137,139 to Zeng et al. (hereinafter "Zeng").

The Combination of Ono, Kumar, and/or Zeng fails to Render Amended Claim 1  
Obvious



Claim 1 has been amended to recite "a silicone-carbide substrate having a first concentration of first type impurities" and "a current spreading semiconductor layer formed on a front side of the drift semiconductor layer." In forming the rejection of claim 1, the Examiner bases his rejection on Ono, but concedes that "Ono does not disclose that the semiconductor substrate is a silicon-carbide substrate." The Examiner relies on Kumar to overcome this deficiency of Ono. The Examiner asserts:

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Ono by using a silicon-carbide substrate for advantages such as higher breakdown voltage and lower ON resistance according to the teachings of Kumar (Column 1, lines 27-30). 4/4/2007 Office Action, Paragraph 11, Page 5.

Applicants strongly disagree. As noted by the Examiner, Ono and Zeng are directed toward MOSFET devices having silicon substrates, while Kumar is directed toward silicon-carbide MOSFET devices. Although the Examiner asserts that modifying Ono to include a silicon-carbide is an obvious modification, such an assertion ignores the technical aspects of silicon-carbide MOSFET devices. Silicon-carbide MOSFET devices are often used for high-power applications. In such applications, a high blocking voltage is desirable. For example, Kumar teaches:

It is an object of the present invention to provide a SiC MOS transistor which makes full use of the characteristics of SiC in order to obtain even lower ON resistance and *higher breakdown voltage* than conventional SiC MOS transistors. Kumar, Col 1, ll. 31-35, emphasis added.

Unlike silicon MOSFET devices, the blocking voltage of silicon-carbide MOSFET devices is limited by gate oxide failure rather than semiconductor breakdown. Gate oxide failure can be caused by the magnetic field of the gate oxide having an excessive strength. As noted in Paragraph [0028] of Applicants' present patent application, the use of a JFET region and/or a current spreading layer in a silicon-carbide substrate reduces the blocking voltage of the

device due to an increased strength of the gate oxide magnetic field. As such, it would not be obvious to one of ordinary skill in the art to use the features of Ono or Zeng with a silicon-carbide substrate because such features would reduce the blocking voltage of the device and likely render the device inoperable for its intended purpose (i.e., high power applications). Thus, it is clear that no one of ordinary skill in the art would combine Ono or Zeng with Kumar in the manner proposed by the Examiner. As such, amended claim 1 is believed to be in condition for allowance and such action is respectfully requested.

Discussion Re: Claims 3-4 and 7-11

Claims 3-4 and 7-11 include claim 1 as a base claim. As such, the rejection of claims 3-4 and 7-11 should be withdrawn for the reasons hereinbefore discussed with regard to amended claim 1. In light of the reasons for withdrawal of the rejection of claim 1, any arguments specific to claims 3-4 and 7-11 are held in abeyance without prejudice or admission to any assertion made by the Examiner in order to expedite prosecution. Claims 7 and 9 have been amended for consistency.

SECTION 102(e) REJECTION OF INDEPENDENT CLAIM 12

The Examiner rejected independent claim 12 under 35 U.S.C. §102(e) as being anticipated by Ono. Claim 12 has been amended to recite:

12. A double-implanted metal-oxide semiconductor field-effect transistor comprising:  
a silicone-carbide substrate;  
a drift semiconductor layer formed on a front side of the semiconductor substrate;  
a first source region;  
a plurality of first base contact regions defined in the first source region, each of the plurality of first base contact regions being spaced apart from each other;  
a second source region;  
a plurality of second base contact regions defined in the second source region, each of the plurality of second base contact regions being spaced apart from each other; and



a JFET region defined between the first source region and the second source region, the JFET region having a width less than about three micrometers.

Anticipation exists only if all the elements of the claimed invention are present in a product or process disclosed, expressly or inherently, in a single prior art reference. *Hazeltine Corp. v. RCA Corp.*, 468 U.S. 1228 (1984). Ono fails to disclose or teach each and every element of amended claim 12. Accordingly, amended claim 12 is believed to be in condition for allowance and such action is respectfully requested.

Discussion Re: Claims 13 and 14

Claims 13 and 14 include claim 12 as a base claim. As such, the rejection of claims 13 and 14 should be withdrawn for the reasons hereinbefore discussed with regard to amended claim 12. In light of the reasons for withdrawal of the rejection of claim 12, any arguments specific to claims 13 and 14 are held in abeyance without prejudice or admission to any assertion made by the Examiner in order to expedite prosecution.

SECTION 103(a) REJECTION OF INDEPENDENT CLAIM 17

The Examiner rejected claim 17 under 35 U.S.C. §103(a) as being unpatentable over Ono in view of Zeng. Claim 17 has been amended to include the subject matter of claim 22. In regard to claim 22, the Examiner rejected this claim under 35 U.S.C. §103(a) as being unpatentable over Ono in view of Zeng and further in view of U.S. Patent Publication Serial No. 2003/0052329 to Kobayashi et al. (hereinafter "Kobayashi"). In support of this rejection, the Examiner asserts that:

Kobayashi shows (Fig 18) a plurality of source regions and a plurality of base contact regions, wherein the plurality of base contact regions (13), form alternating strips of N-type doped regions and P-type doped regions, *the alternating strips (17) being substantially orthogonal to respective source electrodes formed over the first and second source regions.* 4/4/2007 Office Action, Paragraph 37, Page 10, emphasis added.

Applicants disagree. First, reference numeral 13 of Kobayashi points to a well region (13) and reference numeral 17 of Kobayashi points to a gate insulation film (17). Applicants assume the Examiner meant to refer to the contact region 21 and the source region 15 of Kobayashi, respectively. Regardless, Kobayashi simply fails to teach such a configuration. Rather, it is clear from a review of FIGS. 17 and 18 of Kobayashi that the source electrode 19 (see FIG. 17) is oriented in a **parallel configuration** (i.e., non-orthogonal) relative to the source region 15 and the contact region 21. Therefore, for at least this reason, the combination of Ono, Zeng, and Kobayashi fails to render amended claim 17 obvious. As such, claim 17 is believed to be in condition for allowance and such action is respectfully requested.

Discussion Re: Claims 18-20

Claims 18-20 include claim 17 as a base claim. As such, the rejection of claims 18-20 should be withdrawn for the reasons hereinbefore discussed with regard to amended claim 17. In light of the reasons for withdrawal of the rejection of claim 17, any arguments specific to claims 18-20 are held in abeyance without prejudice or admission to any assertion made by the Examiner in order to expedite prosecution.

SECTION 103(a) REJECTION OF INDEPENDENT CLAIM 23

The Examiner rejected claim 32 under 35 U.S.C. §103(a) as being unpatentable over Ono in view of Zeng in further view of Tokura and in further view of Kumar. In forming this rejection, the Examiner concedes that "Ono does not disclose that the semiconductor substrate is silicon-carbide." The Examiner again relies on Kumar to overcome this deficiency of Ono. The Examiner asserts:

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Ono by using a silicon-carbide substrate for advantages such as higher breakdown voltage and lower ON resistance according to the teachings of Kumar. 4/4/2007 Office Action, Page 13-14, Paragraph 50.



However, for all of the reasons provided above in regard to independent claim 1, it would not be obvious to one of ordinary skill to modify the teaching of Ono in the manner suggested by the Examiner. For at last this reason, the combination of Ono, Zeng, Tokura, and Kumar fails to render claim 23 obvious. As such, claim 23 is believed to be in condition for allowance and such action is respectfully requested.

### CONCLUSION

In view of the foregoing, it is submitted that this application is in a condition for allowance. Action to that end is hereby solicited. If there are any questions or comments that would speed prosecution of this application, the Examiner is invited to call the undersigned at (317) 261-7959.

It is respectfully requested that this paper be considered as a petition for a two-month extension of time extending the deadline of this response to August 4, 2007. The Commissioner is hereby authorized to charge the fee of \$450.00 for this two-month extension of time, and any shortages or overpayments of fees, to the Account of Barnes & Thornburg, Deposit Account No. 10-0435 with reference to file 3220-79132.

Respectfully submitted,

BARNES & THORNBURG LLP



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