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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
11/338,007	01/23/2006	James A. Cooper	3220-79132	4085

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BARNES & THORNBURG LLP
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EXAMINER	
PATTON, PAUL E	

ART UNIT	PAPER NUMBER
2822	

MAIL DATE	DELIVERY MODE
10/12/2007	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	11/338,007	COOPER ET AL.	
	Examiner	Art Unit	
	Paul E. Patton	2822	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *06 August 2007*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1,3-5,7-14,17-20 and 23* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1,3-5,7-14,17-20 and 23* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Amendment

1. Acknowledgement is made of Amendment filed August 6, 2007

Claim Objections

2. Claims 1 and 12 are objected to because of the following informalities: The claims refer to "a silicone-carbide substrate" which should read – a silicon-carbide substrate—.

Appropriate correction is required.

Claim Rejections - 35 USC § 103

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

2. Claims 1, 3, 4, 7 – 10, 12, and 13 are rejected under 35 U.S.C. 103(a) as being unpatentable over Ono et al., (US 2003/0227052 A1) Ono in view of Kumar et al., (USPAT 6,573,534.B1) Kumar and further in view of Zeng et al., (USPAT 6,137,139) Zeng.

3. As to claims 1,3,4,9,12, and 13, Ono discloses and shows (Fig 1), a double implanted MOS field effect transistor comprising a semiconductor substrate (10) having a first concentration of first type impurities (n+); a drift semiconductor layer (50) formed on a front side of the semiconductor substrate and having a second concentration of first type impurities less that the first concentration of first type impurities (n-); a first

source region (20); a second source region (20); and a JFET region (40) defined between the first source region and the second source region, the JFET region having a third concentration of first type impurities that is greater than the second concentration of first type impurities (n) and having a width (L) less than about 3 micrometers and a width of about one micrometer. (Paragraphs [0039] & [0041]).

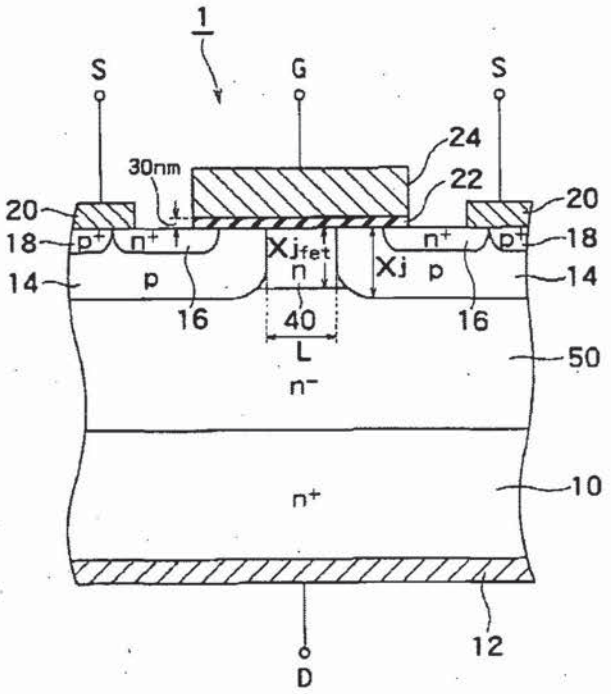


FIG. 1

4. Ono does not disclose that the semiconductor substrate is a silicon-carbide substrate.

5. Kumar is related to a similar MOS FET structure and discloses that the substrate is a silicon-carbide substrate (Column 1, line 40).

6. Kumar is evidence that a person of ordinary skill in the art would find a reason, suggestion or motivation to use a silicon-carbide substrate.

7. Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Ono by using a silicon-carbide substrate for advantages such as higher breakdown voltage and lower ON resistance according to the teachings of Kumar (Column 1, lines 27-30).

8. Ono shows (Ono, Fig 1) the JFET region is formed directly below the gate structure and between the base doped wells formed on either side of the gate. As noted above the parasitic JFET is a consequence of the lateral gate-source arrangement of a vertical MOSFET and would be above the current spreading layer and the drift region shown by Zeng.

9. Ono as modified by Kumar does not explicitly disclose that a current spreading layer is formed on a front side of the drift semiconductor layer; and wherein the concentration of impurities of the first type is greater that the concentration of impurities of the first type in the drift region by at least one order of magnitude.

10. Zeng discloses and shows (Fig 2C) a current spreading layer (103) formed on a front side of the drift semiconductor layer (102) wherein the concentration of impurities of the first type is greater that the concentration of impurities of the first type in the drift region by at least one order of magnitude (Zeng, Column 2, lines 64-67 & Column 3, lines 4-7).

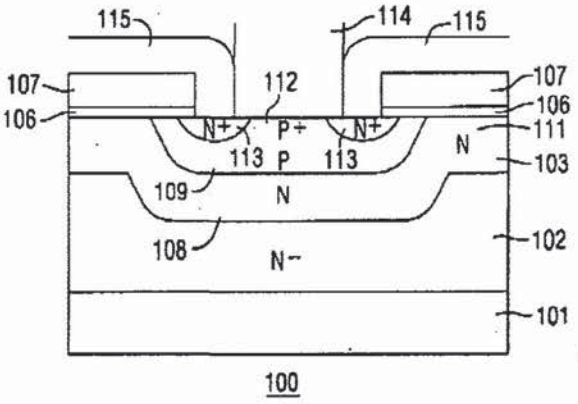


FIG. 2C

11. Zeng is evidence that a person of ordinary skill in the art would find a reason, suggestion or motivation to have a current spreading layer formed on a front side of the drift semiconductor layer; and wherein the concentration of impurities of the first type is greater that the concentration of impurities of the first type in the drift region by at least one order of magnitude.

12. Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Ono to have a current spreading layer formed on a front side of the drift semiconductor layer; and wherein the concentration of impurities of the first type is greater that the concentration of impurities of the first type in the drift region by at least one order of magnitude for advantages such as reduced on-resistance without degrading device ruggedness and reliability according to the teachings of Zeng (Column 4, lines 32-39).

13. As to claims 7 and 8, Ono as modified by Kumar and Zeng discloses and shows (Fig 2C) a current spreading layer (103) formed on a front side of the drift semiconductor layer (102) wherein the concentration of impurities of the first type is

greater that the concentration of impurities of the first type in the drift region by at least one order of magnitude (Zeng, Column 2, lines 64-67 & Column 3, lines 4-7).

14. As to claim 10, Ono as modified by Kumar and Zeng shows (Ono, Fig 12) a plurality of base contact regions (18) formed in each of the first and second source regions (16), the base contact regions being smaller that the first and second source regions.

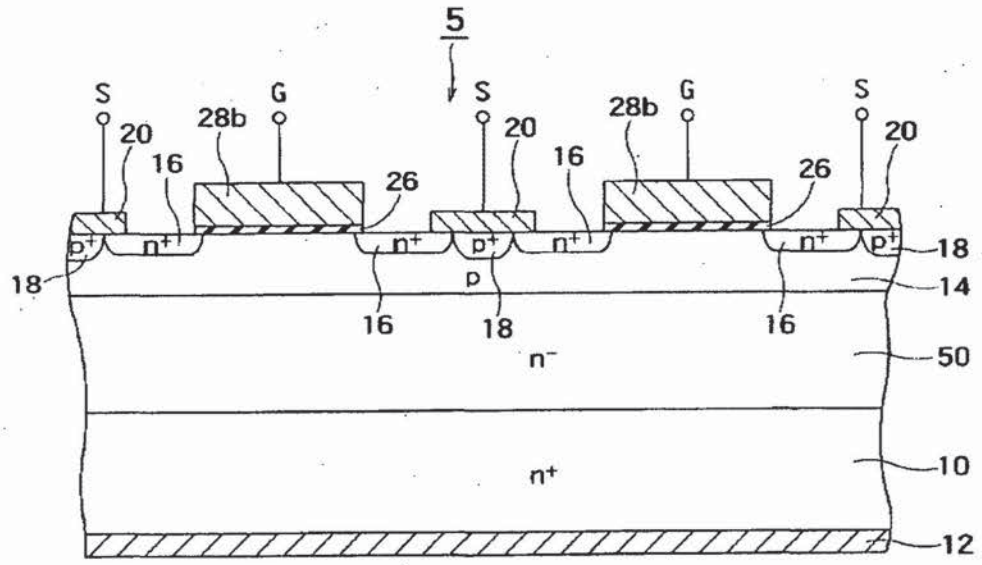


FIG. 12

15. Claims 11, and 17-20 are rejected under 35 U.S.C. 103(a) as being unpatentable over Ono in view of Kumar and Zeng and further in view of Kobayashi et al., (US2003/0052329 A1) Kobayashi.

16. As to claim 11, Ono as modified by Kumar and Zeng does not explicitly disclose a plurality of source regions and a plurality of base contact regions, wherein the plurality of source regions and the plurality of base contact regions, form alternating strips of N-

type doped regions and P-type doped regions, the alternating strips being substantially orthogonal to respective source electrodes formed over the first and second source regions.

17. Kobayashi shows (Fig 18) a plurality of source regions and a plurality of base contact regions, wherein the plurality of source regions (15) and the plurality of base contact regions (21), form alternating strips of N-type doped regions and P-type doped regions, the alternating strips (17) being substantially orthogonal to respective source electrodes formed over the first and second source regions.

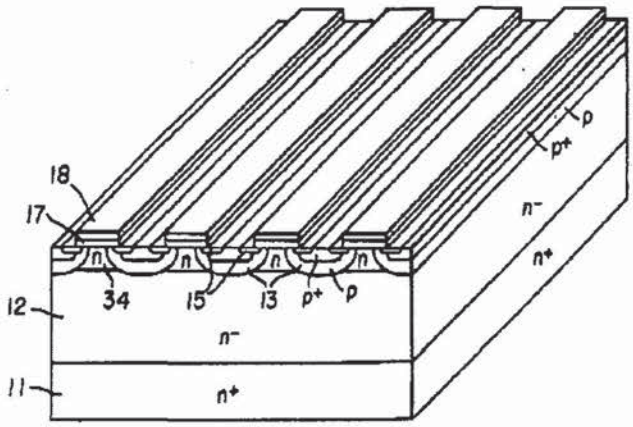


FIG. 18

18. Kobayashi is evidence that a person of ordinary skill in the art would find a reason, suggestion or motivation to form a plurality of source regions and a plurality of base contact regions, wherein the plurality of source regions and the plurality of base contact regions, form alternating strips of N-type doped regions and P-type doped regions, the alternating strips being substantially orthogonal to respective source electrodes formed over the first and second source regions.

19. Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Ono, Kumar and Zeng to form a plurality of source regions and a plurality of base contact regions, wherein the plurality of source regions and the plurality of base contact regions, form alternating strips of N-type doped regions and P-type doped regions, the alternating strips being substantially orthogonal to respective source electrodes formed over the first and second source regions for advantages such as reduced electric field strength according to the teachings of Kobayashi (Paragraph [0034]).

20. As to claim 17, Ono as modified by Kumar, Zeng and Kobayashi discloses and shows (Ono, Fig 1), a double implanted MOS field effect transistor comprising a semiconductor substrate (10) a drift semiconductor layer (50) formed on a front side of the semiconductor substrate; a first source region (20); a second source region (20); and a JFET Further, Zeng discloses and shows (Fig 2C) a current spreading layer (103) formed on a front side of the drift semiconductor layer (102). Ono shows (Ono, Fig 1) the JFET region is formed directly below the gate structure and between the base doped wells formed on either side of the gate. As noted above the parasitic JFET is a consequence of the lateral gate-source arrangement of a vertical MOSFET and would be above the current spreading layer and the drift region shown by Zeng. Further, Kobayashi shows (Fig 18) a plurality of source regions and a plurality of base contact regions, wherein the plurality of source regions (15) and the plurality of base contact regions (21), form alternating strips of N-type doped regions and P-type doped regions,

the alternating strips (17) being substantially orthogonal to respective source electrodes formed over the first and second source regions.

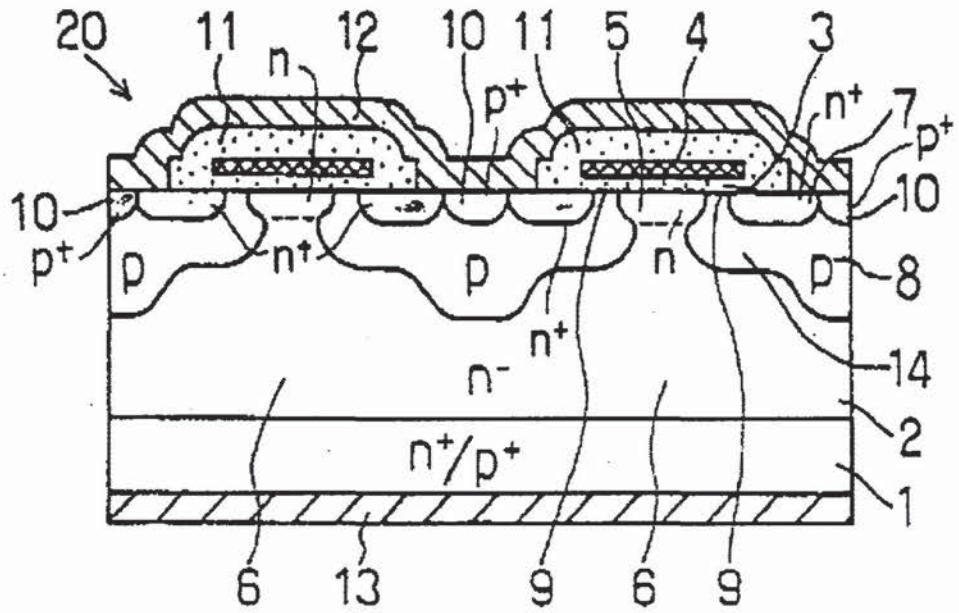
21. As to claims18 and 19, Ono as modified by Kumar, Zeng and Kobayashi discloses a current spreading layer wherein the concentration of impurities of the first type is greater that the concentration of impurities of the first type in the drift region by at least one order of magnitude (Zeng, Column 2, lines 64-67 & Column 3, lines 4-7).

22. As to claim 20, Ono as modified by Kumar, Zeng and Kobayashi discloses the JFET region has a width of about three micrometers or less (Ono, Paragraph [0041]).

23. Claims 5, 14 and 23 are rejected under 35 U.S.C. 103(a) as being unpatentable over Ono in view of Kumar and Zeng and further in view of Tokura et al., (USPAT 5,545,908).

24. Ono as modified by Kumar and Zeng does not disclose that the concentration of first type impurities associated with the JFET region is at least one order of magnitude greater that the concentration of first type impurities associated with the drift region.

25. Tokura is related to a similar MOSFET structure and discloses and shows (Tokura, Fig 1) that the doping level at the JFET region (5) is 8E16 cm^{-3} whereas the doping level of the drift region (2) is 5E15 cm^{-3} .(Tokura, Column 10, lines 29-33 & Column 11, lines 54-58). Note that Tokura does not label the region between the two p doped wells on opposite sides of the gate as a JFET. However the structure in this device as well as Ono will form a parasitic JFET due to the arrangement of the layers. (Ono, Paragraph [0040]).



Tokura, Fig 1

26. Tokura is evidence that a person of ordinary skill in the art would find a reason, suggestion or motivation to have the concentration of the JFET region at least an order of magnitude greater that the concentration of the drift region.

27. Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Ono by having the concentration of the JFET region at least an order of magnitude greater that the concentration of the drift region for advantages such as reduced ON resistance according to the teachings of Tokura (Column 5,lines 60-66 & Column 8, lines 33-34).

28. As to claim 23, Ono as modified by Kumar, Zeng, and Tokura discloses and shows (Fig 1), a double implanted MOS field effect transistor comprising a semiconductor substrate (10) having a first concentration of first type impurities (n+); a

drift semiconductor layer (50) formed on a front side of the semiconductor substrate and having a second concentration of first type impurities less that the first concentration of first type impurities (n-); a first source region (20); a second source region (20); and a JFET region (40) defined between the first source region and the second source region, the JFET region having a fourth concentration of first type impurities that is greater than the second concentration of first type impurities (n) and having a width (L) less than about 3 micrometers and a width of about one micrometer. (Paragraphs [0039] & [0041]).

Kumar discloses that the substrate is a silicon-carbide substrate (Column 1, line 40). Zeng discloses and shows (Fig 2C) a current spreading layer (103) formed on a front side of the drift semiconductor layer (102) wherein the concentration of impurities of the first type is greater that the concentration of impurities of the first type in the drift region (Zeng, Column 2, lines 64-67 & Column 3, lines 4-7). Lastly, Tokura discloses and shows (Tokura, Fig 1) that the doping level at the JFET region (5) is 8E16 cm^{-3} whereas the doping level of the drift region (2) is 5E15 cm^{-3}.(Tokura, Column 10, lines 29-33 & Column 11, lines 54-58). Note that Tokura does not label the region between the two p-doped wells on opposite sides of the gate as a JFET. However the structure in this device as well as Ono will form a parasitic JFET due to the arrangement of the layers. (Ono, Paragraph [0040]).

Response to Arguments

29. In regard to the discussion of claim 1 as amended, the applicant argues that the combination of Ono, Kumar and Zeng does not render claim 1 obvious. However, the

argument seems to contradict the assertion in that forming a DMOS transistor using silicon carbide rather than silicon does, indeed, improve breakdown voltage and reduce ON resistance as is known in the art. In the instant case Ono and Zeng disclose the structure of the DMOS device and Kumar teaches the alternative of silicon-carbide with its known advantages. Hence, one of ordinary skill would indeed consider whether their particular problem would call for silicon-carbide.

30. It is further noted that applicant asserts that silicon-carbide devices are limited by gate oxide failure due to a magnetic field. This is a strange assertion, since it is very well known that the gate oxide would fail due to an electric field intensity not a magnetic field.

31. As to the discussion of the use of a current spreading layer, it is very well known in the art that current spreading layers are employed to counteract current "crowding" in DMOS devices which is a well known performance limiter and failure mode.

32. As to the discussion of claim 12, the same points that apply to claim 1 are relevant here as well. Claim 12 is obvious over the cited references.

33. As to claim 17, this claim is rejected on the same basis as before. While it is true that Kobayashi has a drawing with limited detail, The format claimed of the individual devices laid out in strips is very well known in the art for power transistors. Further, the source contacts would inherently be laid out orthogonal from the strip direction as can be also inferred from figure 12 of Tokura.

34. In like manner, claim 23 is obvious on the same basis as claim 1.

Conclusion

35. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Paul E. Patton whose telephone number is 571-272-9762. The examiner can normally be reached on 7:00 - 5:30 Monday through Thursday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Zandra Smith can be reached on 571-272-2429. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

Paul E Patton
Examiner
Art Unit 2822

PEP

Zandra V. Smith
Supervisory Patent Examiner
10 Oct. 2007

Notice of References Cited	Application/Control No. 11/338,007	Applicant(s)/Patent Under Reexamination COOPER ET AL.	
	Examiner Paul E. Patton	Art Unit 2822	Page 1 of 1

U.S. PATENT DOCUMENTS

*		Document Number Country Code-Number-Kind Code	Date MM-YYYY	Name	Classification
*	A	US-2003/0227052 A1	12-2003	Ono et al.	257/341
*	B	US-5,545,908	08-1996	Tokura et al.	257/341
*	C	US-6,573,534 B1	06-2003	Kumar et al.	257/77
*	D	US-2003/0052329 A1	03-2003	Kobayashi et al.	257/135
*	E	US-5,137,139	08-1992	Ruscello, Lorenzo	198/460.1
*	F	US-6,552,391 B2	04-2003	Zeng et al.	257/342
*	G	US-2003/0205829 A1	11-2003	Boden, Milton J. JR.	257/921
	H	US-			
	I	US-			
	J	US-			
	K	US-			
	L	US-			
	M	US-			

FOREIGN PATENT DOCUMENTS

*		Document Number Country Code-Number-Kind Code	Date MM-YYYY	Country	Name	Classification
	N					
	O					
	P					
	Q					
	R					
	S					
	T					

NON-PATENT DOCUMENTS

*		Include as applicable: Author, Title Date, Publisher, Edition or Volume, Pertinent Pages)
	U	
	V	
	W	
	X	

*A copy of this reference is not being furnished with this Office action. (See MPEP § 707.05(a).)
Dates in MM-YYYY format are publication dates. Classifications may be US or foreign.

Index of Claims	Application/Control No.	Applicant(s)/Patent Under Reexamination
	11338007	COOPER ET AL.
	Examiner	Art Unit
	Patton, Paul E	2822

✓	Rejected	-	Cancelled	N	Non-Elected	A	Appeal
=	Allowed	÷	Restricted	I	Interference	O	Objected

☐ Claims renumbered in the same order as presented by applicant ☐ CPA ☐ T.D. ☐ R.1.47

CLAIM		DATE								
Final	Original	03/26/2007	10/02/2007							
	1	✓	✓							
	2	✓	-							
	3	✓	✓							
	4	✓	✓							
	5	✓	✓							
	6	✓	-							
	7	✓	✓							
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	21	✓	-							
	22	✓	-							
	23	✓	✓							

Search Notes	Application/Control No.	Applicant(s)/Patent Under Reexamination
	11338007	COOPER ET AL.
	Examiner	Art Unit
	Patton, Paul E	2822

SEARCHED			
Class	Subclass	Date	Examiner
257	263, 256, 341, 342, 335, 339, 350, 263,	3/22/2007	PEP
438	142, 156, 176, 186, 197, 268	3/22/2007	PEP

SEARCH NOTES		
Search Notes	Date	Examiner
Search history attached	2/26/2007	PEP
Updated Search	10/2/2007	PEP
Consult with M. Prenty	10/2/2007	PEP

INTERFERENCE SEARCH			
Class	Subclass	Date	Examiner