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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.	
11/338,007	01/23/2006	James A. Cooper	3220-79132	4085	
	7590 06/25/2008 IORNBURG LLP		EXAM	INER	
11 SOUTH ME	RIDIAN		PATTON,	PAUL E	
INDIANAPOLI	IS, IN 46204		ART UNIT PAPER NUMBER		
			2822		
			MAIL DATE	DELIVERY MODE	
			06/25/2008	PAPER	

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

		Application No.	Applicant(s)			
	000	11/338,007	COOPER ET AL.			
	Office Action Summary	Examiner	Art Unit			
		PAUL E. PATTON	2822			
Period fo	The MAILING DATE of this communication app or Reply	pears on the cover sheet with the c	orrespondence address			
A SH WHIC - Exter after - If NC - Failu Any	ORTENED STATUTORY PERIOD FOR REPLY CHEVER IS LONGER, FROM THE MAILING DON'S INSTRUCTION OF THE MAILING OF THE MAIL	ATE OF THIS COMMUNICATION 36(a). In no event, however, may a reply be tim vill apply and will expire SIX (6) MONTHS from , cause the application to become ABANDONEI	Lely filed the mailing date of this communication. (35 U.S.C. § 133).			
Status						
1)⊠ 2a)□ 3)□	Responsive to communication(s) filed on <u>12 M</u> This action is FINAL . 2b) This Since this application is in condition for allowar closed in accordance with the practice under E	action is non-final. nce except for formal matters, pro				
Dispositi	on of Claims					
5) \(\times \) 6) \(\times \) 7) \(\times \) 8) \(\times \)	Claim(s) 1,3-5,7-14,17-20 and 23 is/are pendir 4a) Of the above claim(s) is/are withdraw Claim(s) 12-14 and 17-20 is/are allowed. Claim(s) 1,3-5 and 7-10 is/are rejected. Claim(s) 11 is/are objected to. Claim(s) are subject to restriction and/o	wn from consideration.				
Applicati	on Papers					
10)□	The specification is objected to by the Examine The drawing(s) filed on is/are: a) accomplicant may not request that any objection to the Replacement drawing sheet(s) including the correct The oath or declaration is objected to by the Examine	epted or b) objected to by the Eddrawing(s) be held in abeyance. See ion is required if the drawing(s) is obj	ected to. See 37 CFR 1.121(d).			
Priority ι	ınder 35 U.S.C. § 119					
12) Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f). a) All b) Some * c) None of: 1. Certified copies of the priority documents have been received. 2. Certified copies of the priority documents have been received in Application No 3. Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)). * See the attached detailed Office action for a list of the certified copies not received.						
Attachmen	t(s)					
1) Notic	e of References Cited (PTO-892)	4) Interview Summary				
3) 🔲 Inform	e of Draftsperson's Patent Drawing Review (PTO-948) mation Disclosure Statement(s) (PTO/SB/08) r No(s)/Mail Date	Paper No(s)/Mail Da 5) Notice of Informal P 6) Other:				

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DETAILED ACTION

Response to Amendment

- Acknowledgement is made of Amendment filed March 12, 2008.
- 2. Applicant's arguments regarding claims 1, 3-5, 7-10 and 23 have been fully considered but they are not persuasive. Applicant's argument asserts that examiner has not presented reasonable arguments for combining the references to Ono, Kumar and Zeng. However, examiner believes that the rationale stated in the previous office action clearly presents such a rationale. Further, applicant argues that the combination of these elements *might* render such a device inoperative. However, absent documentary evidence this assertion is not convincing.
- 3. The rejections of dependent claim 11 and claims 12-14 and 17-20 have been withdrawn.

Claim Rejections - 35 USC § 103

- 4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:
 - (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.
- 5. Claims 1, 3, 4, and 7 10, are rejected under 35 U.S.C. 103(a) as being unpatentable over Ono et al., (US 2003/0227052 A1) Ono in view of Kumar et al., (USPAT 6,573,534.B1) Kumar and further in view of Zeng et al., (USPAT 6,137,139) Zeng.

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6. As to claims 1,3,4, and 9, Ono discloses and shows (Fig 1), a double implanted MOS field effect transistor comprising a semiconductor substrate (10) having a first concentration of first type impurities (n+); a drift semiconductor layer (50) formed on a front side of the semiconductor substrate and having a second concentration of first type impurities less that the first concentration of first type impurities (n-); a first source region (20); a second source region (20); and a JFET region (40) defined between the first source region and the second source region, the JFET region having a third concentration of first type impurities that is greater than the second concentration of first type impurities (n) and having a width (L) less than about 3 micrometers and a width of about one micrometer. (Paragraphs [0039] & [0041]).

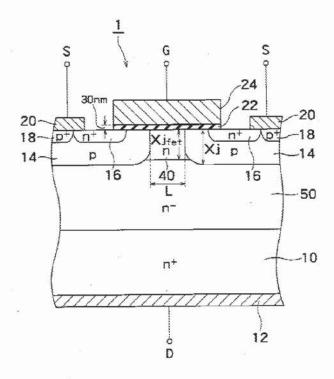


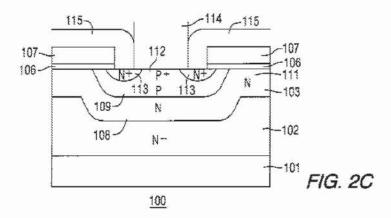
FIG. 1

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 Ono does not disclose that the semiconductor substrate is a silicon-carbide substrate.

- 8. Kumar is related to a similar MOS FET structure and discloses that the substrate is a silicon-carbide substrate (Column 1, line 40).
- Kumar is evidence that a person of ordinary skill in the art would find a reason,
 suggestion or motivation to use a silicon-carbide substrate.
- 10. Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Ono by using a silicon-carbide substrate for advantages such as higher breakdown voltage and lower ON resistance according to the teachings of Kumar (Column 1, lines 27-30).
- 11. Ono shows (Ono, Fig 1) the JFET region is formed directly below the gate structure and between the base doped wells formed on either side of the gate. As noted above the parasitic JFET is a consequence of the lateral gate-source arrangement of a vertical MOSFET and would be above the current spreading layer and the drift region shown by Zeng.
- 12. One as modified by Kumar does not explicitly disclose that a current spreading layer is formed on a front side of the drift semiconductor layer; and wherein the concentration of impurities of the first type is greater that the concentration of impurities of the first type in the drift region by at least one order of magnitude.
- 13. Zeng discloses and shows (Fig 2C) a current spreading layer (103) formed on a front side of the drift semiconductor layer (102) wherein the concentration of impurities of the first type is greater that the concentration of impurities of the first type in the drift

region by at least one order of magnitude (Zeng, Column 2, lines 64-67 & Column 3, lines 4-7).



- 14. Zeng is evidence that a person of ordinary skill in the art would find a reason, suggestion or motivation to have a current spreading layer formed on a front side of the drift semiconductor layer; and wherein the concentration of impurities of the first type is greater that the concentration of impurities of the first type in the drift region by at least one order of magnitude.
- 15. Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Ono to have a current spreading layer formed on a front side of the drift semiconductor layer; and wherein the concentration of impurities of the first type is greater that the concentration of impurities of the first type in the drift region by at least one order of magnitude for advantages such as reduced on-resistance without degrading device ruggedness and reliability according to the teachings of Zeng (Column 4, lines 32-39).

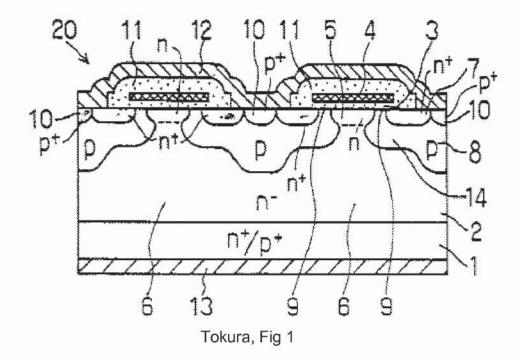
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16. As to claims 7 and 8, Ono as modified by Kumar and Zeng discloses and shows (Fig 2C) a current spreading layer (103) formed on a front side of the drift semiconductor layer (102) wherein the concentration of impurities of the first type is greater that the concentration of impurities of the first type in the drift region by at least one order of magnitude (Zeng, Column 2, lines 64-67 & Column 3, lines 4-7).

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- 17. As to claim 10, Ono as modified by Kumar and Zeng shows (Ono, Fig 12) a plurality of base contact regions (18) formed in each of the first and second source regions (16), the base contact regions being smaller that the first and second source regions.
- 18. Claims 5 and 23 are rejected under 35 U.S.C. 103(a) as being unpatentable over Ono in view of Kumar and Zeng and further in view of Tokura et al., (USPAT 5,545,908).
- 19. One as modified by Kumar and Zeng does not disclose that the concentration of first type impurities associated with the JFET region is at least one order of magnitude greater that the concentration of first type impurities associated with the drift region.
- 20. Tokura is related to a similar MOSFET structure and discloses and shows (Tokura, Fig 1) that the doping level at the JFET region (5) is 8E16 cm⁻³ whereas the doping level of the drift region (2) is 5E15 cm⁻³. (Tokura, Column 10, lines 29-33 & Column 11, lines 54-58). Note that Tokura does not label the region between the two p doped wells on opposite sides of the gate as a JFET. However the structure in this device as well as Ono will form a parasitic JFET due to the arrangement of the layers. (Ono, Paragraph [0040]).



- 21. Tokura is evidence that a person of ordinary skill in the art would find a reason, suggestion or motivation to have the concentration of the JFET region at least an order of magnitude greater that the concentration of the drift region.
- 22. Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Ono by having the concentration of the JFET region at least an order of magnitude greater that the concentration of the drift region for advantages such as reduced ON resistance according to the teachings of Tokura (Column 5,lines 60-66 & Column 8, lines 33-34).
- 23. As to claim 23, Ono as modified by Kumar, Zeng, and Tokura discloses and shows (Fig 1), a double implanted MOS field effect transistor comprising a semiconductor substrate (10) having a first concentration of first type impurities (n+); a

drift semiconductor layer (50) formed on a front side of the semiconductor substrate and having a second concentration of first type impurities less that the first concentration of first type impurities (n-); a first source region (20); a second source region (20); and a JFET region (40) defined between the first source region and the second source region, the JFET region having a fourth concentration of first type impurities that is greater than the second concentration of first type impurities (n) and having a width (L) less than about 3 micrometers and a width of about one micrometer. (Paragraphs [0039] & [0041]).

Kumar discloses that the substrate is a silicon-carbide substrate (Column 1, line 40). Zeng discloses and shows (Fig 2C) a current spreading layer (103) formed on a front side of the drift semiconductor layer (102) wherein the concentration of impurities of the first type is greater that the concentration of impurities of the first type in the drift region (Zeng, Column 2, lines 64-67 & Column 3, lines 4-7). Lastly, Tokura discloses and shows (Tokura, Fig 1) that the doping level at the JFET region (5) is 8E16 cm⁻³ whereas the doping level of the drift region (2) is 5E15 cm⁻³ .(Tokura, Column 10, lines 29-33 & Column 11, lines 54-58). Note that Tokura does not label the region between the two p-doped wells on opposite sides of the gate as a JFET. However the structure in this device as well as Ono will form a parasitic JFET due to the arrangement of the layers. (Ono, Paragraph [0040]).

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Allowable Subject Matter

24. Claim 11 is objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

- 25. Claims 12-14 and 17-20 are allowed.
- 26. The following is a statement of reasons for the indication of allowable subject matter: The prior art of record, taken alone or in combination fails to anticipate or render obvious the plurality of source regions and the plurality of base contact regions form alternating strips of N-type doped regions and P-type doped regions, the alternating strips being substantially orthogonal to respective source electrodes formed over the first and the second source regions as recited in independent claim 17 along with all its other limitations and dependent claim 11.
- 27. As to claim 12, the prior art of record taken alone or in combination fails to anticipate or render obvious a first source electrode formed over the first source region, the first source electrode defining a longitudinal axis; a plurality of first base contact regions defined in the first source region, each of the plurality of first base contact regions being spaced apart from each other in a direction parallel to the longitudinal axis defined by the first source electrode; a second source region; a second source electrode formed over the second source region, the second source electrode defining a longitudinal axis; a plurality of second base contact regions defined in the second source region, each of the plurality of second base contact regions being spaced apart

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fro each other in a direction parallel to the longitudinal axis defined by the second source electrode, along with all the other limitations of claim 12.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to PAUL E. PATTON whose telephone number is (571)272-9762. The examiner can normally be reached on 7:00 - 5:30 Monday through Thursday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Zandra Smith can be reached on 571-272-2429. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

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Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/Zandra V. Smith/ Supervisory Patent Examiner, Art Unit 2822 Paul E Patton Examiner Art Unit 2822

/P. E. P./ Examiner, Art Unit 2822

	Application/Control No.	Applicant(s)/Patent Under Reexamination
Index of Claims	11338007	COOPER ET AL.
	Examiner	Art Unit
	Patton, Paul E	2822

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=	Allowed	. k	÷ Restricted I		1	Interference		0	Objected	
	☐ Claims renumbered in the same order as presented by a			plicant		□ СРА] T.D.		R.1.47	
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	1	✓	✓	✓						
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	3	✓	✓	√						
	4	✓	√	Y						
	5	✓	✓	✓:						
	6	✓						2		
	7	✓	✓	✓						
	8	✓	✓	1						
	9	✓	✓	V						
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	11	✓	✓	0						
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	13	✓	✓	=						

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U.S. Patent and Trademark Office Part of Paper No.: 20080530

EAST Search History

Ref#	Hits	Search Query	DBs	Default Operator	Plurals	Time Stamp
L21	5095	((257/263) or (257/256) or (257/341) or (257/342) or (257/335) or (257/339) or (257/350)).CCLS.	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2008/05/30 10:55
L22	3980	((438/142) or (438/156) or (438/176) or (438/186) or (438/197) or (438/268)).CCLS.	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2008/05/30 10:55
L23	8894	L21 L22	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2008/05/30 10:55
L24	8029	@ad<"20060123" and L23	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2008/05/30 10:55
L25	1642	24 and (parallel strip longitud\$4) same source	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2008/05/30 10:56
L26	448	24 and (parallel strip longitud\$4) same (source near3 electrode)	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2008/05/30 10:57
S1	1393	((Cooper near (James J)) (Saha near (Asmita A))). in.	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2007/03/22 10:54

S2	380394	"257".clas.	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2007/03/22 09:01
S3	7	S1 and S2	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2007/03/22 09:01
S4	4717	((257/263) or (257/256) or (257/341) or (257/342) or (257/335) or (257/339) or (257/350)).OCLS.	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2007/03/22 10:55
S5	3327	((438/142) or (438/156) or (438/176) or (438/186) or (438/197) or (438/268)).CCLS.	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2007/03/22 10:56
S6	7886	S4 S5	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2007/03/22 11:03
S7	156976	MOSFET ("metal oxide semiconductor")	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2007/03/22 11:04
S8	5305	DMOS	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2007/03/22 11:04
S9	304	Double adj implant	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2007/03/22 11:04

S10	57449	power same (FET "Field effect")	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2007/03/22 11:06
S11	8478	JFET ("Junction Field Effect")	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2007/03/22 11:07
S12	3533	current near spread\$3	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2007/03/23 10:28
S13	10361	Drift near5 (layer region)	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2007/03/22 11:10
S14	0	S6 and S7 and S9 and S10 and S11 and S12 and S13	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2007/03/22 11:12
S15	20	S7 and S12 and S13 and S6	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2007/03/22 11:13
S16	80	S7 and S12 and S13	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2007/03/22 11:34
S17	0	S16 and S9	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2007/03/22 11:14

S18	180117	siC (Silicon adj carbide)	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2007/03/22 11:35
S19	548	S11 and S13 and S7	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2007/03/22 14:11
S20	202	S19 and S6	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2007/03/23 12:53
S21	1125	257/341.ccls.	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2007/03/22 15:36
S22	145	S21 and S11	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2007/03/22 15:36
S23	16	S21 and S12	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2007/03/22 15:58
S24	49	S6 and S12	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2007/03/22 16:11
S25	628	S6 and S18	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2007/03/22 16:12

S26	92	S21 and S18	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2007/03/22 16:12
S27	1121	current near spread\$3 near5 layer	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2007/03/23 10:29
S28	1125	257/341.ccls.	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2007/03/23 10:29
S29	6	S27 and S28	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2007/03/23 10:32
S30	4717	((257/263) or (257/256) or (257/341) or (257/342) or (257/335) or (257/339) or (257/350)).OCLS.	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2007/03/23 10:32
S31	3327	((438/142) or (438/156) or (438/176) or (438/186) or (438/197) or (438/268)).CCLS.	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2007/03/23 10:32
S32	7886	S30 S31	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2007/03/23 10:32
S33	12	S27 and S32	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2007/03/23 10:32

S34	156976	MOSFET ("metal oxide semiconductor")	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2007/03/23 12:47
S35	8478	JFET ("Junction Field Effect")	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2007/03/23 12:47
S36	10361	Drift near5 (layer region)	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2007/03/23 12:47
S37	548	S35 and S36 and S34	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2007/03/23 12:47
S38	202	S37 and S32	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2007/03/23 12:47
S39	195	S38 and dop\$3	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2007/03/23 14:03
S40	187432	S34 amd S36 and (dop\$3 concentrat\$3 dos\$3)	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2007/03/23 14:06
S41	4013	S40 and S32	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2007/03/23 14:07

S42	436	S41 and S35	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2007/03/23 15:25
S43	4	S42 and S27	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2007/03/23 15:25
S44	5	S42 and current near5 spread	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2007/03/23 15:27
S45	36	S41 and current near5 spread	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2007/03/26 08:21
S46	2	("5688725").PN.	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2007/03/23 15:50
S47	5	("4941026" "5341011" "5424231" "5532179" "5558313").PN.	US-PGPUB; USPAT; USOCR	OR	ON	2007/03/26 08:12
S48	2	("4941026").PN.	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2007/03/26 08:12
S49	4717	((257/263) or (257/256) or (257/341) or (257/342) or (257/335) or (257/339) or (257/350)).OCLS.	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2007/03/26 08:21
S50	3327	((438/142) or (438/156) or (438/176) or (438/186) or (438/197) or (438/268)).OCLS.	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2007/03/26 08:21

S51	7886	S49 S50	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2007/03/26 08:21
S52	157110	MOSFET ("metal oxide semiconductor")	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2007/03/26 08:21
S53	10368	Drift near5 (layer region)	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2007/03/26 08:21
S54	187573	S52 amd S53 and (dop\$3 concentrat\$3 dos\$3)	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2007/03/26 08:21
S55	4013	S54 and S51	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2007/03/26 08:21
S56	72	S55 and current near5 spread\$3	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2007/03/26 08:22

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Search Notes



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Applicant(s)/Patent Under Reexamination

COOPER ET AL.

Examiner

Patton, Paul E

Art Unit

2822

SEARCHED

Class	Subclass	Date	Examiner
257	263, 256, 341, 342, 335, 339, 350, 263,	3/22/2007	PEP
438	142, 156, 176, 186, 197, 268	3/22/2007	PEP

SEARCH NOTES

Search Notes	Date	Examiner
Search history attached	2/26/2007	PEP
Updated Search	10/2/2007	PEP
Consult with M. Prenty	10/2/2007	PEP
Consult with M. Prenty	5/30/2008	PEP
Updated search	5/30/2008	PEP

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Class	Subclass	Date	Examiner		

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