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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

<i>Group:</i>	2822	}	
		}	
<i>Confirmation No.:</i>	4085	}	
		}	
<i>Application No.:</i>	11/338,007	}	
		}	
<i>Invention:</i>	HIGH-VOLTAGE POWER SEMICONDUCTOR DEVICE	}	DATED:
		}	
<i>Applicant:</i>	James A. Cooper et al.	}	AUGUST 22, 2008
		}	
<i>Filed:</i>	January 23, 2006	}	
		}	
<i>Attorney</i>		}	
<i>Docket:</i>	3220-79132	}	
		}	
<i>Examiner:</i>	Patton, Paul E.	}	

RESPONSE TO OFFICE ACTION

MAIL STOP AF
Commissioner for Patents
P. O. Box 1450
Alexandria, VA 22313-1450

Sir:

In response to the Office Action dated June 25, 2008, Applicants submit the following:

Amendments to the Claims, which begin on page 2 of this paper; and

Remarks, which begin on page 7 of this paper.

CLAIMS AS PENDING

1. (Currently Amended) A metal-oxide semiconductor field-effect transistor comprising:

a silicon-carbide substrate having a first concentration of first type impurities;

a drift semiconductor layer formed on a front side of the semiconductor substrate and having a second concentration of first type impurities less than the first concentration of first type impurities;

a current spreading semiconductor layer formed on a front side of the drift semiconductor layer;

a first source region;

a second source region; and

a JFET region formed on a front side of the current spreading semiconductor layer and defined between the first source region and the second source region, the JFET region having a third concentration of first type impurities that is greater than the second concentration of first type impurities;

a plurality of source regions; and

a plurality of base contact regions,

wherein the plurality of source regions and the plurality of base contact regions form alternating strips of N-type doped regions and P-type doped regions, the alternating strips being substantially orthogonal to respective source electrodes formed over the first and the second source regions.

2. (Cancelled)

3. (Original) The metal-oxide semiconductor field-effect transistor of claim 1, wherein the JFET region has a width of less than about three micrometers.

4. (Original) The metal-oxide semiconductor field-effect transistor of claim 3, wherein the JFET region has a width of about one micrometer.

5. (Original) The metal-oxide semiconductor field-effect transistor of claim 1, wherein the third concentration of first type impurities is at least one order of magnitude greater than the second concentration of first type impurities.

6. (Cancelled)

7. (Previously Presented) The metal-oxide semiconductor field-effect transistor of claim 1, wherein the current spreading semiconductor layer has a fourth concentration of first type impurities that is greater than the second concentration of first type impurities.

8. (Original) The metal-oxide semiconductor field-effect transistor of claim 7, wherein the fourth concentration of first type impurities is at least one order of magnitude greater than the second concentration of first type impurities.

9. (Previously Presented) The metal-oxide semiconductor field-effect transistor of claim 8, wherein the JFET region has a width of about one micrometer.

10. (Original) The metal-oxide semiconductor field-effect transistor of claim 1, further comprising a plurality of base contact regions formed in each of the first and the second source regions, the base contact regions being smaller than the first and second source regions.

11. (Cancelled)

12. (Previously Presented) A double-implanted metal-oxide semiconductor field-effect transistor comprising:

a silicon-carbide substrate;

a drift semiconductor layer formed on a front side of the semiconductor substrate;

a first source region;

a first source electrode formed over the first source region, the first source electrode defining a longitudinal axis;

a plurality of first base contact regions defined in the first source region, each of the plurality of first base contact regions being spaced apart from each other in a direction parallel to the longitudinal axis defined by the first source electrode;

a second source region;

a second source electrode formed over the second source region, the second source electrode defining a longitudinal axis;

a plurality of second base contact regions defined in the second source region, each of the plurality of second base contact regions being spaced apart from each other in a direction parallel to the longitudinal axis defined by the second source electrode; and

a JFET region defined between the first source region and the second source region, the JFET region having a width less than about three micrometers.

13. (Original) The double-implanted metal-oxide semiconductor field-effect transistor of claim 12, wherein the JFET region has a width of about one micrometer.

14. (Original) The double-implanted metal-oxide semiconductor field-effect transistor of claim 12, wherein the JFET region has a first concentration of first type impurities and the drift semiconductor layer has a second concentration of first type impurities, the first concentration of first type impurities being greater than the second concentration of first type impurities.

15-16. (Cancelled)

17. (Previously Presented) A double-implanted metal-oxide semiconductor field-effect transistor comprising:

a semiconductor substrate;

a drift semiconductor layer formed on a front side of the semiconductor substrate;

a current spreading semiconductor layer formed on a front side of the drift semiconductor layer;

a plurality of first and second source regions;

a plurality of base contact regions; and

a JFET region defined between the plurality of first source regions and the plurality of second source regions, the JFET region being formed on a front side of the current spreading semiconductor layer,

wherein the plurality of first and second source regions and the plurality of base contact regions form alternating strips of N-type doped regions and P-type doped regions, each of the alternating strips defining a longitudinal axis that is substantially orthogonal to a longitudinal axis defined by respective source electrodes formed over the first and the second source regions.

18. (Original) The double-implanted metal-oxide semiconductor field-effect transistor of claim 17, wherein the current spreading semiconductor layer has a first concentration of first type impurities and the drift semiconductor layer has a second concentration of first type impurities, the first concentration of first type impurities being greater than the second concentration of first type impurities.

19. (Original) The double-implanted metal-oxide semiconductor field-effect transistor of claim 18, wherein the first concentration of first type impurities is at least one order of magnitude greater than the second concentration of first type impurities.

20. (Original) The double-implanted metal-oxide semiconductor field-effect transistor of claim 17, wherein the JFET region has a width of about three micrometers or less.

21-23. (Cancelled)

REMARKS

Applicants thank the Examiner for consideration of the present application. This response is filed in response to the Office Action, dated June 25, 2008, to place this application in condition for allowance as suggested by the Examiner. In the 06/25/08 Final Office Action, the Examiner rejected claims 1, 3-5, and 7-10. The Examiner objected to claim 11, but indicated that this claim would be allowable if rewritten to include all the limitations of the base claim. Applicants note with appreciation the Examiner's indication that claims 12-14 and claims 17-20 are in condition for allowance. By this amendment, claim 1 is amended and claims 11 and 23 are cancelled.

DISCUSSION: Independent Claim 1

Claim 1 has been amended to include each element of claim 11. As such, claim 1 is believed to be in condition for allowance and such action is respectfully requested. In addition, claims 1, 3-5, and 7-10 each include claim 1 as a base claim. Accordingly, each of claims 1, 3-5, 7-10 is also believed to be in condition for allowance and such action is respectfully requested.

CONCLUSION

In view of the foregoing, it is submitted that this application is in a condition for allowance. Action to that end is hereby solicited. If there are any questions or comments that would speed prosecution of this application, the Examiner is invited to call the undersigned at (317) 261-7959.

It is respectfully requested that, if necessary to effect a timely response, this paper be considered as a Petition for an Extension of Time sufficient to effect a timely response. The

Commissioner is hereby authorized to charge the fee for such Petition and any shortage of fees, and credit any overpayment of fees, to the Account of Barnes & Thornburg, Deposit Account No. 10-0435 with reference to file 3220-79132.

Respectfully submitted,

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