

SiC Power-Switching Devices—The Second Electronics Revolution?

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Invited Paper

Silicon carbide (SiC) offers significant advantages for power-switching devices because the critical field for avalanche breakdown is about ten times higher than in silicon. SiC power devices have made remarkable progress in the past five years, demonstrating currents in excess of 100 A and blocking voltages in excess of 19 000 V. In this paper, we describe the latest progress in three classes of SiC devices: diodes (p-i-n and Schottky), transistors (junction field-effect transistor, metal-oxide-semiconductor field-effect transistor, bipolar junction transistor), and thyristors (gate turn-off).

Keywords—Bipolar junction transistors (BJTs), gate turn-off (GTO), junction field-effect transistors (JFETs), metal-oxide-semiconductor field-effect transistor (MOSFETs), p-i-n diodes, power-switching devices, power transistors, Schottky barrier diodes (SBDs), silicon carbide, thyristors, wide bandgap semiconductors.

I. INTRODUCTION

It is now widely recognized that silicon power-switching devices are reaching their theoretical limits of performance, as established by fundamental material parameters such as the critical field for avalanche breakdown [1]. It is also recognized that several other semiconductors, particularly silicon carbide (SiC), have electronic parameters that would enable dramatic improvements in performance [1]. The commercial availability of single-crystal SiC wafers in the early 1990s led to a resurgence of activity in the development of SiC electronic devices. Over the past decade, a plethora of new SiC-based power-switching devices have been demonstrated, and many of the most optimistic performance predictions have been experimentally confirmed. However, there

is a significant difference between demonstrating prototype devices and establishing an economically viable commercial product. Silicon has proven to be an extremely difficult material to displace, largely because of economic factors, and it remains to be seen whether SiC can accomplish what other semiconductor materials have failed to do.

From a purely technical standpoint, SiC brings significant new challenges, both in materials science and device design. One of the unique features of SiC is its high thermal stability compared to silicon. This is both a blessing and a curse—a blessing because of improved reliability and higher temperature capability, a curse because many of the typical fabrication processes either do not occur at all in SiC or require extremely high temperatures. The most challenging aspect of the thermal stability is the fact that SiC does not melt, but instead gradually sublimates at temperatures above 2000 K. This makes it impossible to form large single-crystal ingots by pulling a seed crystal from a melt, as in the Czochralski process that produces 200–300-mm diameter silicon ingots. Instead, SiC crystals are formed by a modified sublimation process that is presently limited to 100-mm diameter ingots. The process is expensive and difficult and SiC wafer costs are astronomical compared to silicon. Even so, the performance advantages of SiC power devices are so great that the higher cost of the starting material can still be offset in certain cases, allowing SiC to compete directly with silicon in specialized device markets.

The evolution of SiC power-switching technology can be divided into three phases: prototype device demonstration, device scale-up, and commercial production. Device scale-up in this context refers to the attempt to build devices of sufficient area that the absolute currents are competitive with silicon. Many types of SiC power devices are well along in the prototype demonstration phase and several have demonstrated performance measures far superior to silicon. These include rectifiers with blocking voltages above 19 kV [2], power metal-oxide-semiconductor field-effect transistors (MOSFETs) [3], and bipolar junction transistors (BJTs) [4] with performance figures 100 times higher than

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in silicon, and gate turn-off (GTO) thyristors blocking over 3 kV and switching over 60 kW [5]. Several of these devices are in the scale-up phase, with terminal currents in excess of 100 A already demonstrated in single-device packaged rectifiers [6]. One class of device, the Schottky diode, is now in limited commercial production [7].

In this paper, we will review recent progress and assess the current status of SiC power devices in three categories: 1) diodes; 2) transistors; and 3) thyristors.

II. DIODES

A. Schottky Barrier Diodes

SiC Schottky barrier diodes (SBDs) or metal–semiconductor diodes [8], [44], [45] are attractive because they provide rectification without significant switching loss. Switching loss occurs when a diode switches from the conducting state to the blocking state. In p–i–n diodes [8], [44], [45], the on-state current is comprised of both holes and electrons injected into the lightly doped “i” region. These carriers must be removed before the diode can turn off. This gives rise to a reverse recovery transient, where a large reverse current flows as carriers are extracted from the “i” region of the diode. Schottky diodes are metal/semiconductor junctions, and conduction current in these devices consists only of electrons injected from the n-type semiconductor into the metal. Since no holes are injected into the semiconductor, there is no stored charge and no reverse recovery transient, so the SBD turns off very rapidly. The reverse current transient of the p–i–n diode causes power dissipation in other components of the switching system, typically a switching transistor, and this switching loss is attributed to the diode since the current transient is caused by the diode. Substitution of an SBD in place of a p–i–n diode effectively eliminates the switching loss.

Although Schottky diodes are desirable because of their low switching loss, it is not feasible to build high voltage SBDs in silicon. This is because of the relatively low barrier heights between common metals and silicon. The bandgap energy of silicon is 1.12 eV and the barrier heights of metal contacts to silicon are typically less than 0.5 eV. Under large reverse bias, the barrier is further reduced by Schottky barrier lowering. Since electron injection from the metal into the semiconductor increases exponentially as barrier height is reduced, a very large reverse current is observed in silicon SBDs at modest reverse voltages. Such is not the case with SiC because it is easy to fabricate SBDs with barrier heights as high as 1.5 eV. Since the reverse current depends exponentially on barrier height, the reverse leakage in SiC SBDs is orders of magnitude lower than in silicon, even at high voltages. Indeed, SBDs with blocking voltages up to 5 kV have recently been demonstrated in SiC [9].

Fig. 1 shows the cross section of a typical SBD in SiC. A lightly doped n-type blocking layer is grown by chemical vapor deposition on an n+ 4H-SiC substrate that is misoriented about 8° off the normal to the (0001) silicon face. This misorientation creates periodic steps along the surface that expose the polytype stacking sequence, creating

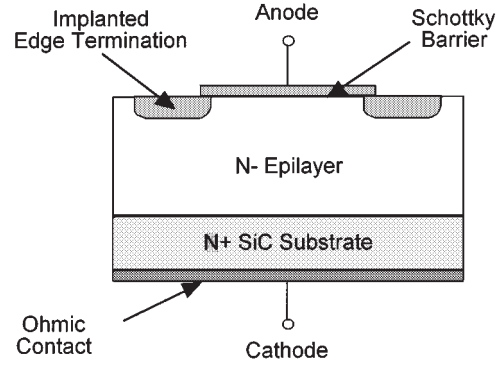


Fig. 1. Cross section of a SBD on SiC. Lightly-doped n-type epilayer is designed to withstand the desired blocking voltage.

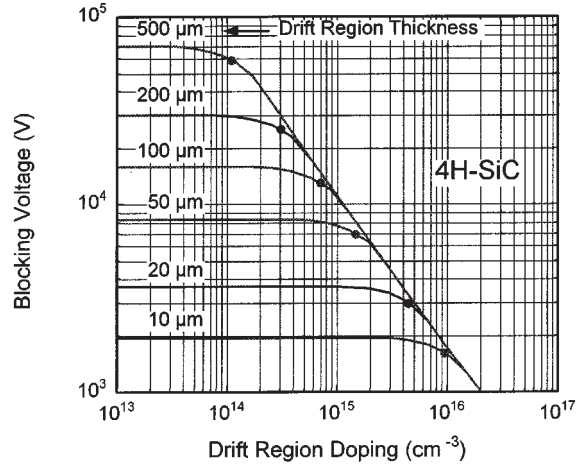


Fig. 2. Blocking voltage of a 4H-SiC epilayer as a function of doping and thickness. Points indicate designs that provide the optimal V_B^2/R_{ON} figure of merit for each thickness.

a template that preserves the polytype information during epigrowth. The doping and thickness of the epilayer are chosen to achieve the desired blocking voltage. Fig. 2 shows the blocking voltage of a 4H-SiC epilayer as a function of doping and thickness. The circles on each curve denote the doping that maximizes a performance figure of merit (FOM) given by the square of the blocking voltage divided by the specific on-resistance V_B^2/R_{ON} . The theoretical maximum value for this FOM under optimum punchthrough conditions is

$$\left. \frac{V_B^2}{R_{ON}} \right|_{MAX} = \mu_N \epsilon_S \left(\frac{2E_C}{3} \right)^3 \quad (1)$$

where μ_N is the electron mobility parallel to the c axis, ϵ_S is the semiconductor dielectric constant, and E_C is the critical field for avalanche breakdown. The theoretical maximum for this FOM is about 4 MW/cm² for silicon and 4000 MW/cm² for 4H-SiC (E_C in SiC is approximately ten times higher than in silicon).

The Schottky junction on the top surface of the blocking layer is formed by implanting an edge termination ring at the surface, then depositing the Schottky metal. The edge termination ring is needed to prevent field crowding at the periphery of the metal in the blocking state, which would

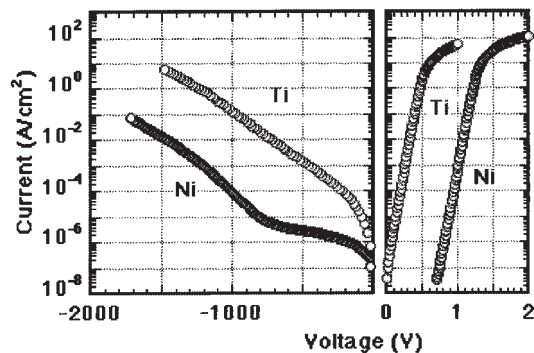


Fig. 3. Forward and reverse I - V characteristics of Ni and Ti Schottky diodes on a $13\text{-}\mu\text{m}$ -thick n-type 4H-SiC epilayer using RTE edge termination. Since Ti has a lower barrier height to SiC, the forward and reverse currents at a given voltage are higher for the Ti diode than for the Ni diode.

significantly reduce the blocking voltage. Two types of edge termination rings are currently in use: a resistive termination extension (RTE) [10] and a junction termination extension (JTE) [11]. The RTE is usually formed using a p-type dopant, either aluminum or boron, but it can also be a species that creates a highly damaged resistive layer at the surface [12]. In the case of a p-type dopant, the implant is annealed at a temperature sufficient to repair most of the lattice damage, but insufficient to fully activate the dopant. As a result, the RTE layer contains a high density of deep traps. This resistive layer permits a small lateral leakage current to flow in the blocking state, resulting in a lateral potential drop that reduces field crowding. Fig. 3 shows static current-voltage (I - V) characteristics of SiC Schottky diodes formed using Ni and Ti on the same blocking epilayer [13]. Both diodes use the same RTE edge termination. The ledge in reverse leakage current observed in the Ni diode at small reverse voltage is due to lateral current flow in the RTE layer. At higher reverse voltages for the Ni diode and at all reverse voltages for the Ti diode, emission over the Schottky barrier dominates the RTE current. The alternative termination technique, JTE [11], utilizes a fully activated p-type implant. The total dose in the JTE layer is selected so that the layer will be fully depleted before the peak field is high enough to cause avalanche breakdown. The exposed acceptor charge in the JTE layer terminates electric field lines that would otherwise extend to the edge of the Schottky metal, thereby reducing field crowding at the metal edge.

The I - V characteristics of the SBD in both the forward and reverse directions are strongly dependent upon the metal/semiconductor barrier height Φ_{BN} , as shown in Fig. 3. The barrier height for Ti on n-type 4H-SiC is approximately 0.8 eV, whereas for Ni it is approximately 1.4 eV. As a result, the Ti diode conducts at a lower forward voltage, but allows a much larger reverse current than the Ni diode. As a general rule, it is desirable to keep the reverse current density below about 1 mA/cm^2 at the maximum specified reverse voltage. Using this criterion, we could operate the Ni diode up to about 1200-V reverse bias, but the Ti diode could only be used to about 500 V. For this reason,

the Ni diode provides the best overall compromise between forward and reverse characteristics.

The saturation of the I - V characteristics at high forward currents is due to the series resistance of the n-type blocking layer, which in this case is $13\text{-}\mu\text{m}$ thick and doped $3.5 \times 10^{15}\text{ cm}^{-3}$. At a forward voltage of 2 V, the Ni diode will carry 100 A/cm^2 , while the Ti diode will carry slightly higher current. The blocking voltages of the two diodes are 1700 and 1500 V, respectively.

B. p - i - n Junction Diodes

As the desired blocking voltage increases, the n-type blocking layer must become thicker and more lightly doped, as indicated in Fig. 2. This leads to increased on-state resistance, reducing the maximum forward current density. Inverting (1) gives an expression for on-resistance as a function of blocking voltage

$$R_{ON} = \frac{V_B^2}{\mu_N \epsilon_S} \left(\frac{3}{2EC} \right)^3. \quad (2)$$

Strictly speaking, (1) and (2) apply only to *unipolar* devices such as the Schottky diode and the MOSFET. In *bipolar* devices such as the p - i - n diode, BJT, insulated-gate bipolar transistor (IGBT), and GTO, the injection of minority carriers into the blocking layer is accompanied by a corresponding increase in the density of majority carriers to maintain charge neutrality [8], [44], [45]. These additional carriers increase the conductivity of the region (conductivity modulation) and the on-resistance is lower than given by (2). This represents a major advantage of p - i - n diodes over SBDs at high blocking voltages.

The advantage of lower on-resistance is partially offset by the higher junction voltage required to achieve the same current density in a p - i - n diode compared to an SBD. As is well known, the diffusion current in a p - n diode scales as the square of the intrinsic carrier concentration n_i [8], [44], [45]. Because of the wider bandgap of 4H-SiC, n_i is approximately 18 orders of magnitude lower than in silicon. This requires a greater reduction of the built-in potential barrier to achieve the same current density, and typical junction voltage drops in a forward-biased SiC p - i - n diode are on the order of 3 V. In contrast, the lower barrier height of a typical SBD on SiC requires a junction voltage drop only on the order of 1 V. The total on-state power dissipation of a diode is the sum of the junction drop and the drop across the on-state resistance of the blocking layer. The p - i - n diode has lower on-resistance, but higher junction drop as compared to the SBD. As blocking voltage is increased, the on-resistance of the blocking layer eventually becomes the dominant resistance, giving the p - i - n diode an advantage over the SBD.

Because of carriers stored in the " i " layer in the on-state, SiC p - i - n diodes exhibit a reverse recovery transient, as discussed above, leading to a switching power dissipation that is proportional to frequency [8], [44], [45]. This switching loss is essentially absent in the SBD. As a result, the SBD becomes favored over the p - i - n as switching frequency

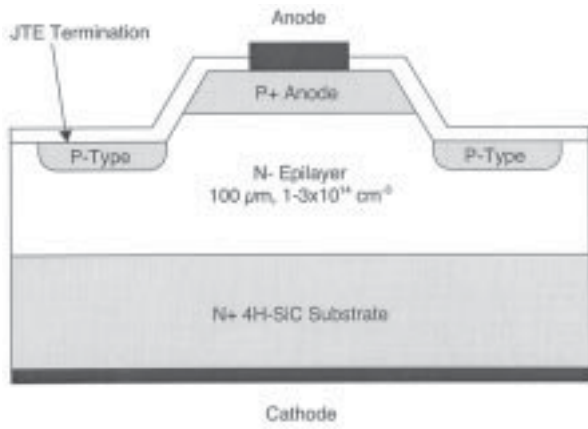


Fig. 4. Cross section of an epitaxial mesa-isolated p-i-n diode in SiC. Edge termination is provided by an implanted p-type JTE ring.

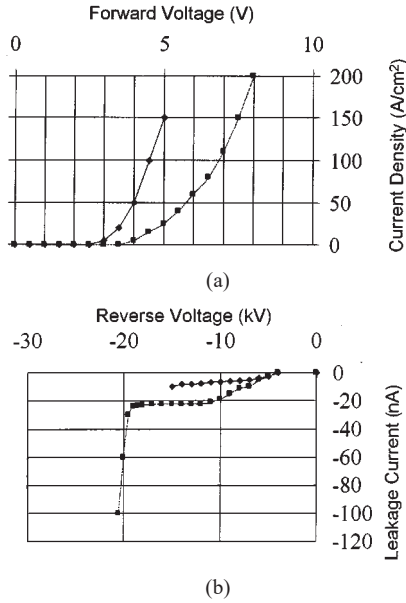


Fig. 5. Forward and reverse I - V characteristics of a mesa-isolated JTE-terminated p-i-n diode on a 200- μ m 4H-SiC epilayer. Reverse blocking voltage of 19 kV is the highest reported for any semiconductor device to date.

is increased. To summarize, the SiC SBD is desirable for high-frequency switching systems due to its low switching loss, but the SiC p-i-n becomes more competitive at higher blocking voltages due to conductivity modulation which leads to lower on-resistance. Even though SiC p-i-n diodes exhibit greater switching loss than SiC SBDs, their switching loss is still small compared to silicon p-i-n diodes due to the thinner blocking layer required to support a given blocking voltage in SiC.

Fig. 4 shows the cross section of a high-voltage p-i-n diode in SiC [14]. The p+ anode is formed during epigrowth, and selectively removed using reactive ion etching (RIE). A p-type JTE ring is implanted, and ohmic contacts are established to the anode and substrate. P-type ohmic contacts are typically pure Al or an Al/Ti alloy; n-type ohmic contacts utilize Ni. Contacts are annealed at 850 °C–1000 °C, forming an Al-rich p+ surface layer in the case of p-type contacts or a Ni-silicide layer in the case of n-type contacts. Fig. 5

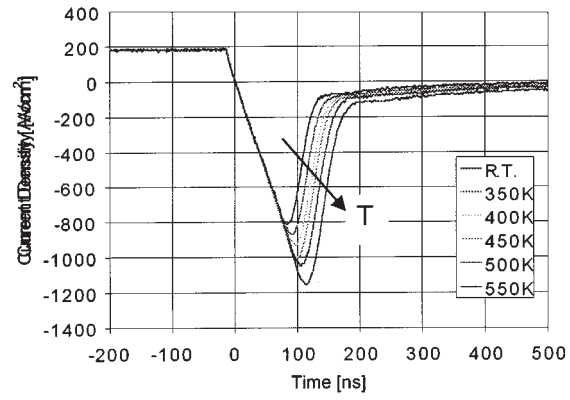


Fig. 6. Turn-off transients of an 8.6-kV SiC p-i-n diode as a function of temperature.

shows the static I - V characteristics of a SiC p-i-n diode on a 200- μ m blocking layer doped $8 \times 10^{13} \text{ cm}^{-3}$ [2]. This diode blocks over 19 kV, the highest voltage of any semiconductor device reported to date. Forward drop is 6.5 V at 100 A/cm².

Fig. 6 shows the measured reverse recovery transient of an 8.6 kV SiC p-i-n diode on a 100- μ m blocking layer [15]. The area under the current transient corresponds to the charge stored in the blocking layer under forward bias, and is simply given by the product of the forward current density and the ambipolar lifetime $Q_S = J_{ON} \tau_A$. In SiC, as in silicon, the carrier lifetime increases approximately as the square of temperature [16], leading to increased stored charge and longer reverse recovery transients as temperature is increased.

III. TRANSISTORS

A. General Discussion

The first SiC power transistors were vertical trench U-shape MOSFETs (UMOSFETs) reported by Cree Research in 1992 [17]. Since that time, a wide variety of SiC power transistors have been developed, including planar double-implanted MOSFETs (DMOSFETs) [18], junction FETs (JFETs) [19], BJTs [4], and IGBTs [20]. As with diodes, transistors are classified as either unipolar or bipolar. In unipolar transistors such as MOSFETs and JFETs, conduction involves only one type of carrier, typically electrons, and the blocking layer is not subject to conductivity modulation [8], [44], [45]. Unipolar devices obey the on-resistance blocking-voltage relations given by (1) and (2). In addition, both JFETs and MOSFETs have high input impedance, greatly simplifying the design of control circuits. The BJT, as a bipolar device, offers lower on-resistance due to conductivity modulation of the blocking layer, but requires substantial input (base) current. This places demands on control circuits and introduces additional power dissipation in the device.

As a bipolar device, the IGBT would also conductivity modulate its blocking layer and its insulated gate would provide a high input impedance, simplifying drive requirements [8], [44], [45]. Unfortunately, the IGBT has an odd number of p-n junctions in the primary current path. This places one

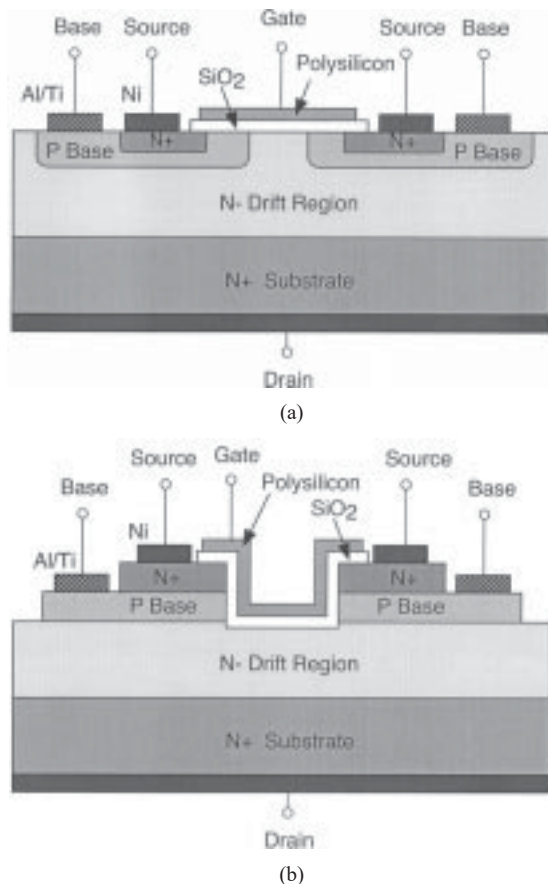


Fig. 7. Cross sections of (a) DMOS and (b) UMOS power transistors in SiC. DMOS structure is planar, but requires ion implantation and high-temperature implant activation. Trench-gate UMOS structure occupies less area and can be made without ion implantation, but suffers from field crowding at the trench corners.

junction voltage drop (≈ 3 V) in series with the resistive drop across the blocking layer, which adds to the power dissipation. In addition, n-channel IGBTs require p-type SiC substrates, which have high resistivity due to the low ionization fraction of the deep acceptor impurities (ionization energy around 200 MeV). This series substrate resistance is typically larger than the resistance of the blocking layer, negating any advantages from conductivity modulation. Finally, the IGBT exhibits substantial switching loss due to stored charge. For these reasons, the IGBT has so far not been a competitive device in SiC.

In the sections that follow, we first discuss unipolar transistors (MOSFETs and JFETs) and then turn our attention to BJTs.

B. Metal–Oxide–Semiconductor Field-Effect Transistors

Fig. 7 illustrates the two basic designs used for power MOSFETs in SiC. The UMOS design, in its most basic form, requires no ion implantation or implant annealing steps, and historically was the first power MOSFET realized in SiC [17]. The UMOSFET suffers from several practical problems, however. First, the MOS channel lies along the vertical sidewalls of a trench formed by RIE. Depending upon the precise crystal alignment, this sidewall may approximate the

(11 $\bar{2}$ 0) or the (1 $\bar{1}$ 00) crystal planes, or may lie along an intermediate direction. Current flow in the channel is parallel to the c axis of the crystal and carriers must cross alternating silicon and carbon planes of the crystal. The a -axis MOS interface includes bonds between oxygen atoms and both silicon and carbon surface atoms, giving rise to new and as-yet poorly understood electrical characteristics (interface traps and interface charges). Surface roughness due to RIE damage is present, but not yet fully quantified. All these factors contribute to a lower inversion layer mobility on these surfaces.

The sharp geometry of the trench corners in the UMOSFET give rise to two-dimensional field crowding in the blocking state, resulting in high fields in the oxide. This is especially critical in SiC, for the following reason. Since the critical field for avalanche breakdown in SiC is approximately ten times higher than in silicon, the peak surface fields in the semiconductor can reach values in the range of 2–3 MV/cm without initiating semiconductor breakdown. By Gauss' Law, the field in the oxide is some 2.5 times higher than the field in the adjacent SiC. This can bring the oxide field to 5–7 MV/cm, very close to the breakdown field of the oxide. With a two to three times enhancement in field at the trench corners, oxide breakdown occurs. Oxide breakdown at the trench corners thus becomes the factor limiting blocking voltage of SiC UMOSFETs.

All the trench problems mentioned above are avoided by the planar DMOS geometry [18]. In silicon the p-type base and n+ source regions of DMOSFETs are formed by double diffusion of p- and n-type dopants through a single oxide window, but this process is impractical in SiC due to the small diffusion coefficients for impurities in the material. Instead, the DMOS structure is formed in SiC using a double ion implantation with two separate implantation masks. Inversion carriers flow along the (0001) silicon plane, a surface that has not been roughened by RIE. However, the DMOSFET is not without its own problems. Activation of the implants that form the base and source regions requires annealing at temperatures in excess of 1500 °C. Depending upon the precise annealing conditions (time, temperature, and ambient), this anneal can create surface roughness through a process called *step bunching* [21], [22]. This surface roughness has been shown to severely degrade channel mobility in subsequently formed MOSFETs [23].

Inversion layer mobility is degraded in both UMOSFET and DMOSFETs, albeit through different mechanisms. However, several groups have shown that incorporating an n-type counterdoped layer along the oxide/semiconductor interface restores the channel mobility in both types of transistors. One version of this structure, known as an accumulation-channel FET or “ACCUFET,” was demonstrated in the DMOS geometry by Shenoy *et al.* [24] and in the UMOS geometry by Hara *et al.* [25]. More recently, counterdoped channels have been used in high-performance UMOSFETs by Tan *et al.* [3] and in high-performance DMOSFETs by Agarwal *et al.* [26].

Perhaps the most advanced UMOSFET to date is the trench-oxide-protected UMOSFET developed by Tan *et al.* in 1998 [3]. This device, shown in Fig. 8, incorporates two new features that protect the trench oxide from high fields

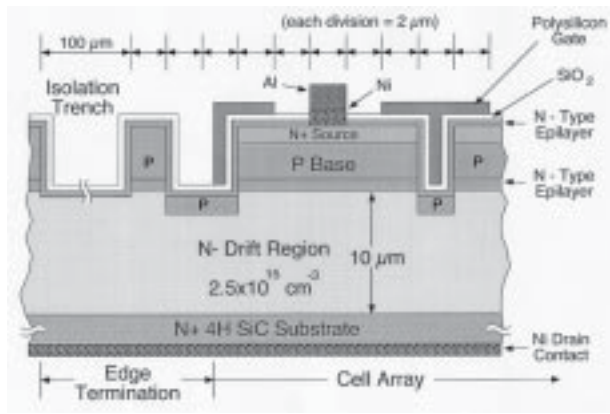


Fig. 8. Trench-oxide-protected UMOFET introduced in 1998. The p-type region in the bottom of each trench protects the gate oxide from high electric fields in the blocking state and the thin n-type epilayer beneath the p-type base prevents pinchoff of the channel in the conducting state.

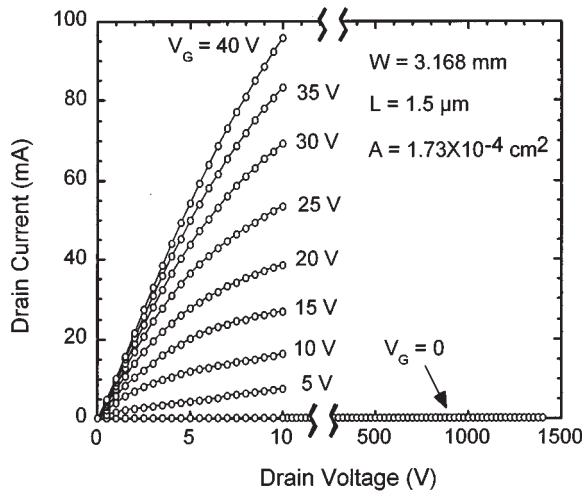


Fig. 9. Static I - V characteristics of the UMOFET of Fig. 8. Specific on-resistance is $15.7 \text{ m}\Omega\text{cm}^2$, as determined from the linear region of the plot. Blocking voltage is 1400 V at $V_G = 0$.

and enhance lateral current spreading into the blocking layer. The first feature is a self-aligned p-type implant in the bottom of the gate trench. Since this layer is grounded (not shown in the figure) and doped high enough that it will not fully deplete, it effectively shields the trench oxide from high fields in the blocking state, both along the trench bottom and at the trench corners. The second feature is a thin n-type current spreading layer formed between the blocking layer and the p-type base during epigrowth. This layer fully depletes in the blocking state, having negligible effect on the blocking voltage. In the on-state, it prevents JFET pinchoff between the p-type trench implant and the p-type base and provides a low-resistance path into the blocking layer, thereby eliminating current crowding at the trench corners. For higher channel mobility, the device of Fig. 8 also incorporates a counterdoped channel layer formed by epigrowth after trench etch. Fig. 9 shows the static I - V characteristics of this device on a $10\text{-}\mu\text{m}$ blocking layer. The blocking voltage of 1400 V is approximately 72% of the theoretical plane-junction blocking voltage for this blocking

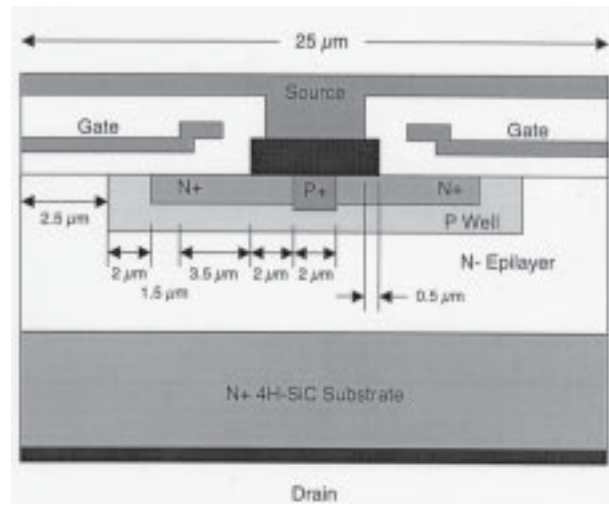


Fig. 10. Cross section of a counter-doped DMOSFET. In this device, a thin n-type surface layer is formed by ion implantation in order to improve the surface mobility.

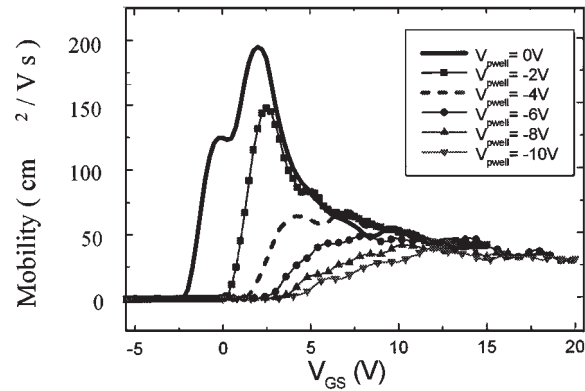


Fig. 11. Electron surface mobility of the counter-doped DMOSFET as a function of gate voltage for several values of base-to-source (back gate) bias. Back gate bias of 4 V shifts the threshold voltage positive and the resulting surface mobility is greater than $50 \text{ cm}^2/\text{V}\cdot\text{s}$ for a wide range of gate voltages.

layer and the specific on-resistance of $15.7 \text{ m}\Omega\text{cm}^2$ results in a V_{DS}^2/R_{ON} FOM of $125 \text{ MW}/\text{cm}^2$, 25 times higher than the theoretical limit for silicon MOSFETs.

Fig. 10 shows a counterdoped 4H-SiC DMOSFET developed by Agarwal *et al.* [26]. In this device, a thin n-type surface layer is introduced by ion implantation to improve the surface mobility. The surface layer in this particular device is doped slightly heavier than optimum, producing a depletion-mode (normally on) device. However, enhancement mode operation can be demonstrated by reverse biasing the base-source junction, thereby increasing the threshold voltage. Fig. 11 shows measured channel mobility for several values of base-to-source bias. The device becomes enhancement mode for base voltages above 2 V and at zero bias the peak channel mobility is $195 \text{ cm}^2/\text{V}\cdot\text{s}$, a very attractive value for channels in ion implanted base regions in SiC. Fig. 12 shows the on-state I - V characteristics at zero base voltage (depletion mode), demonstrating a maximum drain current of 10 A in an area of 0.105 cm^2 ($3.3 \times 3.3 \text{ mm}^2$). A blocking voltage of 350 V is obtained in the $3.3 \times 3.3 \text{ mm}^2$

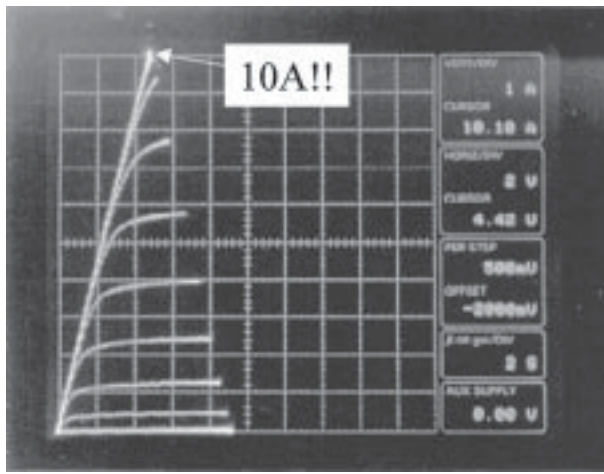


Fig. 12. On-state I - V characteristics of the counter-doped DMOSFET of Fig. 10. Active area is $3.3 \times 3.3 \text{ mm}^2$, producing a maximum current of 10 A.

device, and 1950 V in a smaller $0.75 \times 0.75 \text{ mm}^2$ device, utilizing a $25\text{-}\mu\text{m}$ blocking layer.

An interesting variant of the counterdoped DMOSFET is the static induction-injected accumulated FET (SIAFET) reported by Takayama *et al.* [27]. This device is similar in cross section to the counterdoped DMOSFET of Fig. 10, but the n-type surface channel is formed by subsequent epigrowth after implantation of the p-type base region. In the SIAFET mode of operation, the base is used as a second gate (JFET gate) and is driven into forward conduction in the on-state. This has two beneficial effects. First, it allows the lateral spacing between base regions to be reduced without fear of pinch-off, since the base is forward biased in the on-state. This reduces the overall area of the device and provides increased protection for the gate oxide in the blocking state. Second, injection from the forward biased base may conductivity modulate the n-type surface channel and JFET regions, further reducing on-resistance. SIAFETs on $75\text{-}\mu\text{m}$ blocking layers have demonstrated blocking voltages as high as 6100 V using JTE termination. With the MOS gate at 20 V and the JFET gate at 7.5 V, the 6-kV device exhibited an on-resistance of $732 \text{ m}\Omega\text{cm}^2$, for a V_B^2/R_{ON} FOM of 51 MW/cm^2 . The JFET gate current under these conditions was $845 \text{ }\mu\text{A}$. This represents a drain current to gate current ratio of approximately 11. Significantly higher "betas" (~ 150) could be obtained at lower JFET gate biases, albeit with higher on-resistance.

In all SiC MOSFETs produced to date, the inversion layer electron mobility is much lower than would normally be expected based on the bulk mobility of electrons in the material. Inversion layer mobilities in silicon MOSFETs typically range from about 750 to $500 \text{ cm}^2/\text{V}\cdot\text{s}$ as the device is biased from weak inversion into strong inversion. In 4H-SiC MOSFETs, mobilities have until recently been measured in the single digits. This is surprising, since the bulk mobility of electrons in lightly doped 4H-SiC is as high as $1000 \text{ cm}^2/\text{V}\cdot\text{s}$, not significantly below that of silicon. Work is currently underway to improve the channel mobility of SiC power MOSFETs. We pointed out earlier that high-temperature implant

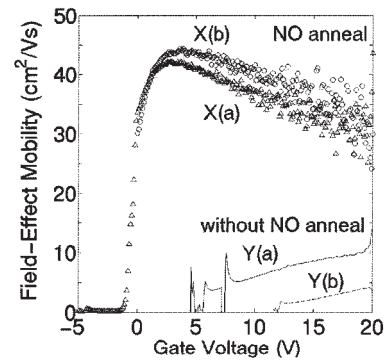


Fig. 13. Electron inversion layer mobility on p-type 4H-SiC epilayers that have been exposed to a 1400°C activation anneal for the source/drain implants. Gate oxides are thermally grown at 1150°C in wet O_2 and subject to a 950°C reoxidation anneal in wet O_2 . Lower curves did not receive a postoxidation anneal in NO, while the upper curves received the NO anneal. Curves with suffix (b) are measured *before* the 850°C ohmic contact anneal, while curves with suffix (a) are measured *after* the ohmic contact anneal. Improvement in mobility due to the NO anneal is dramatic.

annealing can introduce surface roughness in DMOSFETs and RIE can introduce surface roughness in UMOSFETs and both of these effects reduce surface mobility. However, the mobility is also low in planar epitaxial MOSFETs that experience neither high temperature implant anneals or RIE. It has recently been discovered that although the density of interface states is relatively low in the lower half of the bandgap on SiC, it rises exponentially in the upper half of the bandgap, approaching $10^{14} \text{ eV}^{-1} \text{ cm}^{-2}$ near the conduction band edge [28], [29]. This effect is especially apparent in the 4H polytype, owing to its larger bandgap. These interface states exert two deleterious effects on mobility. First, they trap a significant fraction of the charge induced at the interface by the applied gate voltage, removing these carriers from the inversion layer. Second, these trapped charges act as Coulomb scattering centers, reducing the mobility of the few electrons that remain in the inversion layer.

One of the most promising recent developments is the use of a nitric oxide (NO) anneal following gate oxidation. Work performed at Auburn and Vanderbilt Universities [30] and confirmed by measurements at Purdue University [31] indicates that the NO anneal reduces the density of interface states in the upper half of the bandgap in 4H-SiC by an order of magnitude. Moreover, the inversion layer mobility of epitaxial MOSFETs is increased significantly [32], [33], as illustrated in Fig. 13. In this figure, the two lower curves represent inversion layer field-effect mobility of samples without a postoxidation NO anneal (measured before and after the ohmic contact anneal), while the two upper curves show the mobility on identically processed samples from the same wafer that received a postoxidation NO anneal. Field-effect mobilities as high as $45 \text{ cm}^2/\text{V}\cdot\text{s}$ are observed.

These new results are encouraging and will dramatically reduce the on-resistance if they can be successfully transferred to power MOSFETs. However, it is not yet clear whether the NO anneal will be effective in power MOSFETs, since the inversion channel in DMOSFETs lies in an ion implanted region, while the inversion channel in UMOSFETs

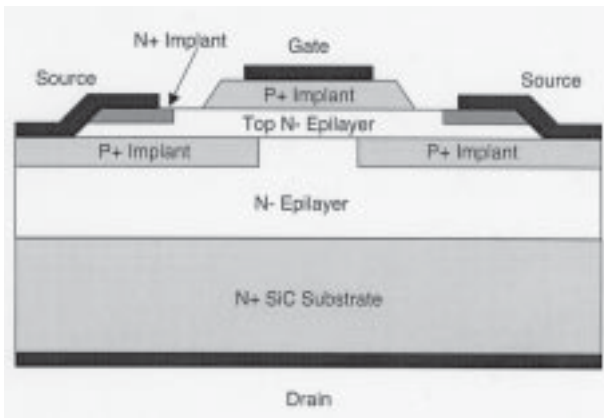


Fig. 14. Cross section of a vertical JFET in SiC. The p-type buried gate is formed by ion implantation, followed by epigrowth of the n-type channel and the p-type top gate. Top gate is patterned by RIE and n-type source regions are formed by a second ion implantation. Alternatively, both the top gate and source can be formed by separate ion implantations.

lies along the vertical sidewall of a trench formed by etching. Work is currently underway to investigate these issues.

C. Junction Field-Effect Transistors

JFETs offer high input impedance (although not as high as the MOSFET) without a critical gate oxide. This avoids several current material science issues peculiar to MOSFETs, including channel mobility, oxide breakdown, and long-term reliability of the oxide. The JFET fabrication process is simpler than for MOSFETs, and JFETs can operate at junction temperatures above 250 °C, the practical upper limit for MOSFETs [34]. However, JFETs are normally depletion-mode (normally-on) devices, and the gate must be maintained at a negative voltage to keep the device off. Most power control systems require enhancement-mode (normally off) devices so that the system will fail in a “safe” condition should control power be interrupted. One way to circumvent this problem is to connect a depletion-mode JFET in a cascode configuration with an enhancement-mode control device such as a silicon power MOSFET [35]. In this configuration, the SiC JFET blocks the high voltage, while the silicon MOSFET in series with the JFET provides normally off current control and high input impedance.

Fig. 14 shows the cross section of a vertical JFET as typically realized in SiC [19]. In this device, the p-type buried gate is formed in selected areas by ion implantation following epigrowth of the n-type blocking layer. The n-type channel layer is grown in a second epigrowth operation and the top gate and n-type source regions are formed on the top surface by selective ion implantation.

The first high-performance SiC power JFETs were reported by Siemens in 1999 [19]. These depletion mode (normally on) devices are intended for use with a cascode MOSFET, as described above. The buried gate is permanently connected to the source, keeping it at ground potential. These devices block 1800 V at a specific on-resistance of 24 mΩcm², for a V_B^2/R_{ON} FOM of 135 MW/cm², slightly higher than the best MOSFET reported to date.

Recently, Kansai Electric Power Co. and Cree, Inc. reported the first enhancement-mode SiC JFETs [36]. In the Kansai/Cree devices, the buried gate is connected to the top gate, providing a gating effect from both sides of the channel. JFETs on a 50-μm blocking layer block 4.4 kV. With the gate forward biased by 2.6 V, the specific on-resistance is 121 mΩcm², for a V_B^2/R_{ON} FOM of 164 MW/cm², the highest yet reported for any SiC FET. Similar JFETs on a 75-μm blocking layer block 5.5 kV with an on-resistance of 218 mΩcm² for an FOM of 139 mΩcm², comparable to the lower voltage Siemens device.

D. Bipolar Junction Transistors

The silicon BJT was the first true power device, but it was gradually replaced by the silicon power MOSFET and IGBT. At the present time, BJTs are no longer considered competitive in silicon. There are two main reasons for this. First, BJTs are current-controlled devices with low input impedance, requiring substantial input drive current (base current). This complicates drive circuits and leads to increased power dissipation in the device. Second, silicon BJTs are subject to an avalanche effect known as “second breakdown” that can quickly lead to destruction. The critical current density for the onset of second breakdown is proportional to the doping of the collector drift region [37]. For a nonpunchthrough design, the doping of the drift region is proportional to the square of the critical field. Since the critical field for avalanche breakdown in SiC is ten times higher than in silicon, the drift region doping for a given blocking voltage is 100 times higher than in silicon. This means the critical current density for second breakdown in SiC is also 100 times higher than in silicon, thereby making second breakdown a nonissue in SiC [37]. The higher critical field holds other advantages for SiC BJTs: for a given blocking voltage, both the collector and base are narrower in SiC than in silicon. The narrower base leads to higher current gain (beta), while the narrower collector enables faster switching. Thus, the BJT is once again an attractive power device in SiC.

The SiC BJT offers interesting tradeoffs compared to SiC MOSFETs. From a practical point of view, BJTs avoid many of the troublesome issues associated with the gate oxide in MOSFETs. These include oxide breakdown under high fields, oxide reliability at high temperatures and high fields, and low inversion layer mobility at the oxide/semiconductor interface. Since they do not have a critical gate oxide, BJTs can be operated at higher junction temperatures than MOSFETs, which are limited to ~250 °C and below by oxide reliability considerations [34]. In many ways, SiC BJTs are easier to fabricate than SiC power MOSFETs and, thus, should have higher manufacturing yield. From a performance standpoint, BJTs offer lower on-resistance than MOSFETs because they have no channel resistance, and the drift region resistance is lower than given by (2) due to conductivity modulation. Since the BJT has an even number of p-n junctions in the current path, both of which are strongly forward biased in the on-state, their junction drops cancel almost completely, resulting in no additional power

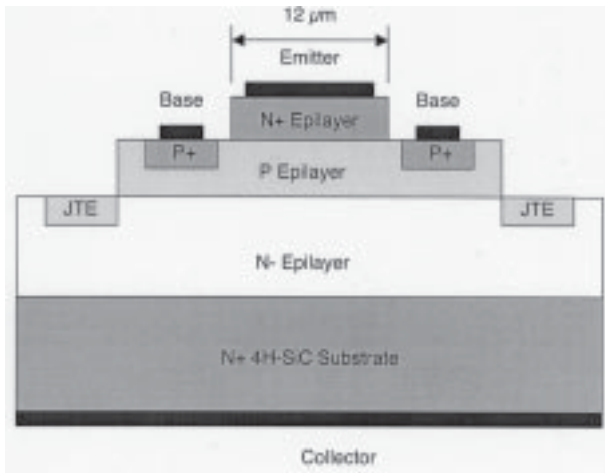


Fig. 15. Cross section of an epitaxial-emitter SiC BJT. Emitter and base regions are patterned by RIE and the base contact and JTE regions are formed by ion implantation.

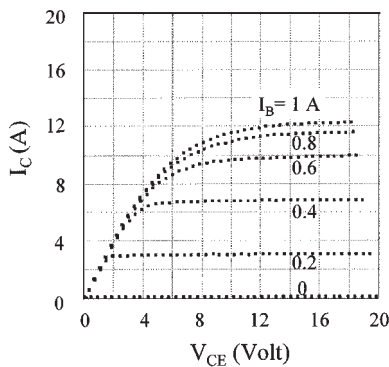


Fig. 16. On-state I - V characteristics of a $1.0 \times 1.4 \text{ mm}^2$ SiC BJT on a $20\text{-}\mu\text{m}$ blocking layer. Common-emitter current gain is 20 and the open-base blocking voltage is 1800 V. Specific on-resistance is $7 \text{ m}\Omega\text{cm}^2$, leading to a V_B^2/R_{ON} figure of merit of 463 MW/cm^2 , the highest yet reported for any SiC power device.

dissipation. The main disadvantage of the BJT relative to the MOSFET remains the high input (base) drive current required in the on-state. This base current can account for substantial power dissipation in the device, since it flows through the E-B junction, which has a voltage drop of approximately 3 V in the on-state. For this reason, as well as for input circuit considerations, it is desirable to maximize beta in the BJT.

Fig. 15 shows the cross section of an epitaxial-emitter SiC BJT fabricated on a $20\text{-}\mu\text{m}$ blocking layer doped $2.5 \times 10^{15} \text{ cm}^{-3}$ [4]. The $0.75\text{-}\mu\text{m}$ -thick emitter and $1.0\text{-}\mu\text{m}$ -thick base are defined by RIE and the base contact region and JTE termination are formed by ion implantation. Fig. 16 shows on-state characteristics of a $1.0 \times 1.4 \text{ mm}^2$ device with a cell pitch of $23 \text{ }\mu\text{m}$. The common emitter current gain (beta) is 20 and a maximum collector current of 3.8 A (271 A/cm^2) is obtained at a base current of 250 mA . Blocking voltage is 1800 V with the base open (BV_{CEO}), and 2200 V with base shorted to emitter (BV_{CBS}). This is about 71% of the theoretical plane-junction breakdown voltage for the collector epilayer used. The specific on-resistance is $7 \text{ m}\Omega\text{cm}^2$, resulting in a V_B^2/R_{ON} FOM of 463 MW/cm^2 . This is the

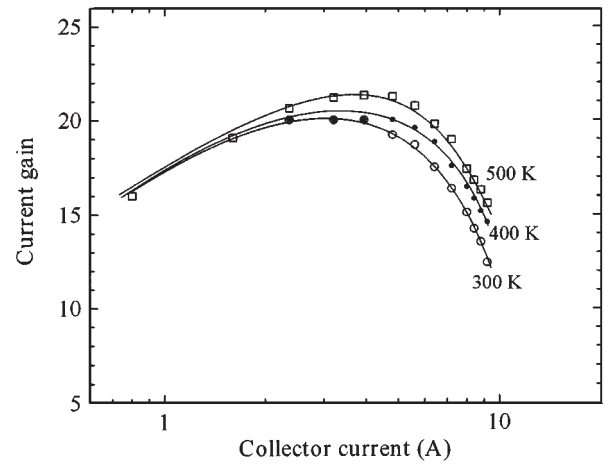


Fig. 17. Current gain as a function of collector current for the BJT of Fig. 16. Beta increases slightly with temperature due to increases in minority carrier lifetime, leading to higher base transport factor.

highest FOM of any SiC power device reported to date and almost four times higher than the best SiC MOSFET [3]. The on-resistance is close to the theoretical value for a nonconductivity-modulated drift region of this thickness and doping, as given by (2).

The current gain increases monotonically with temperature, as shown in Fig. 17. This is the result of two competing effects. First, acceptors in the p-type base have high ionization energies and are not fully ionized at room temperature. As temperature is raised, more of the acceptors become ionized, contributing holes to the valence band. This increases the apparent base doping and reduces emitter injection efficiency, reducing beta. However, the minority carrier lifetime in the base increases with temperature, as mentioned earlier. This increases the base transport factor, increasing beta. In the devices shown here, the second effect is dominant, leading to a positive temperature coefficient of current gain (beta).

A positive temperature coefficient of beta might be a cause for concern if devices are connected in parallel, since the hottest device would tend to “hog” the current, potentially leading to thermal runaway. However, in these devices, the net on-resistance is dominated by the collector drift region, not by the intrinsic BJT. For this reason, the on-resistance is actually insensitive to beta and exhibits a positive temperature coefficient due to increased scattering in the drift region, which reduces the carrier mobility. This will allow multiple BJTs to be connected in parallel to form modules, without fear of thermal runaway.

E. Comparison of Transistor Performance

Fig. 18 summarizes the blocking voltage and specific on-resistance of the leading MOSFETs, JFETs, and BJTs reported in recent years. The diagonal lines represent loci of constant V_B^2/R_{ON} . Equation (1) gives the theoretical maximum FOM for unipolar devices (MOSFETs and JFETs) in 4H-SiC as 4000 MW/cm^2 , indicated by the double diagonal line in the figure. We should note that is not strictly correct to include the BJT in this type of plot for two reasons. First, the

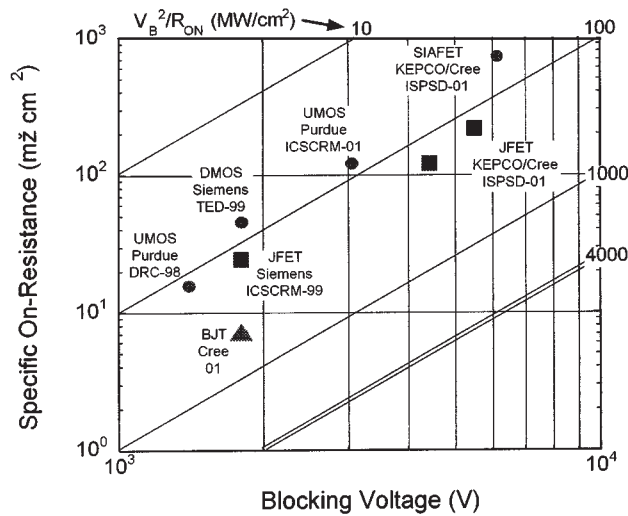


Fig. 18. Specific on-resistance and blocking voltage of MOSFETs, JFETs, and BJTs in SiC. Diagonal lines represent loci of constant V_B^2/R_{ON} . The theoretical maximum V_B^2/R_{ON} for conventional silicon MOSFETs is about 4 MW/cm² and all the SiC devices exceed this value by a wide margin. Theoretical limit for 4H-SiC is about 4000 MW/cm², leaving significant room for further progress in SiC switching devices.

BJT can achieve on-resistances lower than given by (2) due to conductivity modulation of the drift region. The degree of conductivity modulation depends, among other things, on the current density at which the BJT is operated, so that quoting a specific value for on-resistance is not meaningful. Second, the on-state power dissipation of unipolar devices is directly proportional to on-resistance ($P_{ON} = J_{ON}^2 R_{ON}$), but the power dissipation of the BJT contains an additional term that accounts for dissipation due to the base current. Thus, the BJT dissipates more power than would be indicated by simply considering the on-resistance. In the case of the Cree BJT, however, the base current power dissipation is small compared to that due to the on-resistance, making it reasonable to include the BJT in this figure. One notes that the BJT has slightly higher FOM than the best MOSFETs or JFETs reported to date, but all three types of SiC transistors far exceed the best silicon MOSFETs, including the recently introduced superjunction MOSFETs [38], [39]. In addition, there is significant room for further progress before reaching the theoretical limit for 4H-SiC.

IV. THYRISTORS

Large-area silicon thyristors are being manufactured today with single devices on a 100-mm-diameter wafer with current handling capability of 1000 A and blocking voltages approaching 10 000 V. These devices are being used in high-voltage direct-current transmission systems. At present, no other device type can match the performance of thyristors, and their application to very high power systems is expected to continue in the foreseeable future. The GTO thyristor has also been developed over the past 30 years. Their main advantages over thyristors have been the higher switching speed and the ability to turn off the current without

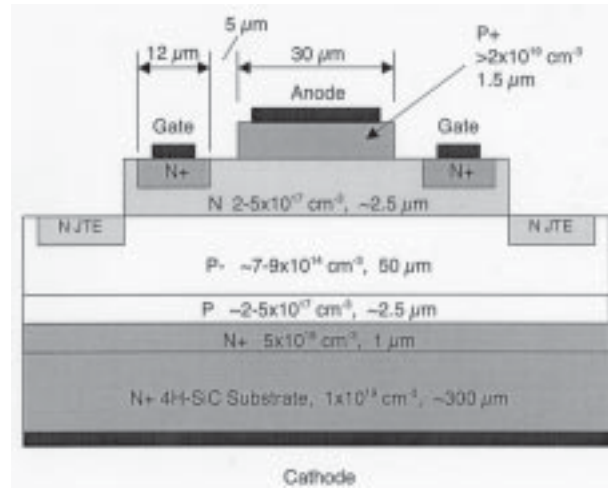


Fig. 19. Cross-sectional view of the thyristor structure.

reversal of the anode to cathode voltage. These attributes have led to the use of GTOs in high power inverter systems.

Thyristors made from SiC have been pursued over the last several years because of the potential for lower forward drop, faster switching, higher blocking voltage, and higher operating temperature compared to silicon-based thyristors. The first symmetrical (blocking in both directions) thyristors were demonstrated by Cree [40]. These early devices blocked 700 V with a rated current of 6 A at a forward drop of 3.9 V. The devices were made on n+ 4H-SiC substrates resulting in a np-np structure, which is inverse of the conventional p-n-p-n structure used in silicon technology. This is necessary in SiC due to the high resistance of the p+ substrates. Subsequently, other researchers have built on this early work and have produced asymmetrical (blocking in only one direction) n-p-n-p devices [41]–[43]. The limitations on epilayer thickness and the device footprint have generally limited these results to 1000 V blocking and several amps.

Recently, remarkable progress has been made in 4H-SiC based GTO thyristors. 4H-SiC GTO thyristors with 3.1-kV forward-blocking capability and up to 12 A of forward current were successfully demonstrated [5].

A cross-sectional view of the thyristor structure is shown in Fig. 19. Five epilayers are grown on 380-μm-thick 8° off-axis 4H-SiC n-type substrates with resistivity of 0.02 Ω·cm. The blocking p-(base) layer is 50-μm thick, doped to around 7×10^{14} cm⁻³. The p+ buffer layer reduces the spreading of the depletion layer under forward bias, thus, making the device asymmetrical. The high injection efficiency of the p+ (anode)-n(base) junction is provided by very heavy doping of the p+ layer to 1×10^{19} cm⁻³.

The 2×2 mm² GTO thyristors are packaged with 15 ribbon bonds on each of the anode and gate pads, as shown in Fig. 20. These packaged devices are tested with the gate terminal floating at room temperature for blocking voltage measurements. To prevent arcing in air, the package is immersed in Fluorinert during the measurement. The I - V characteristics of a 2×2 mm² device measured using a Tektronix 371 curve tracer is shown in Fig. 21. In this measurement, the anode is grounded and the cathode is biased negatively with

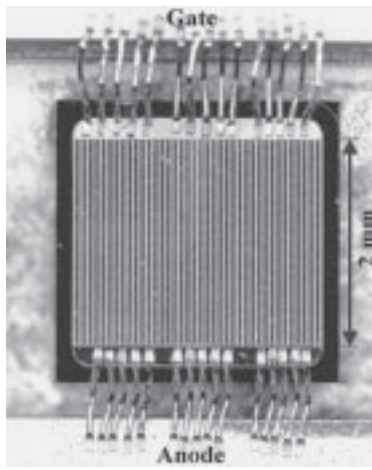


Fig. 20. Photograph of a packaged $2 \times 2 \text{ mm}^2$ interdigitated GTO thyristor.

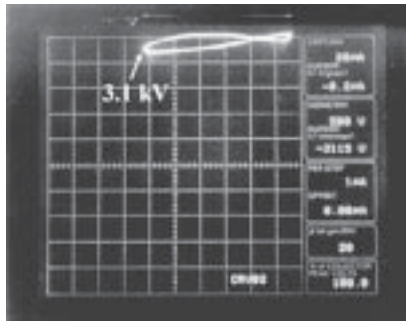


Fig. 21. Forward blocking characteristics of the $2 \times 2 \text{ mm}^2$ GTO of Fig. 20 measured at room temperature in Fluorinert. Device exhibits a forward blocking voltage of 3.1 kV.

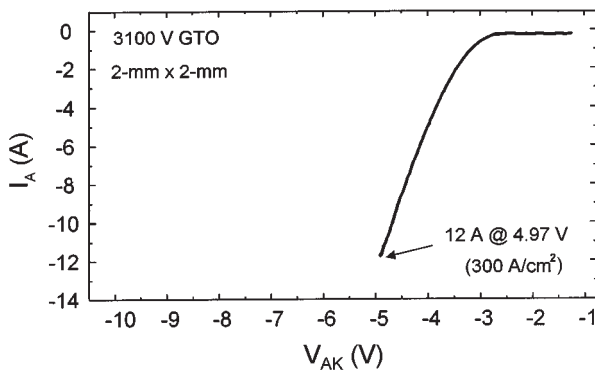
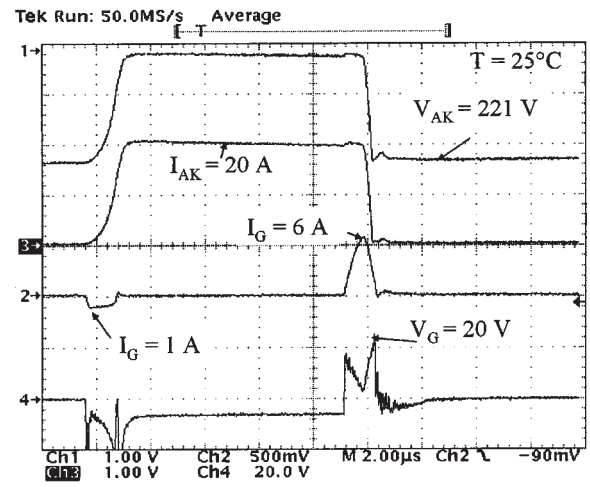
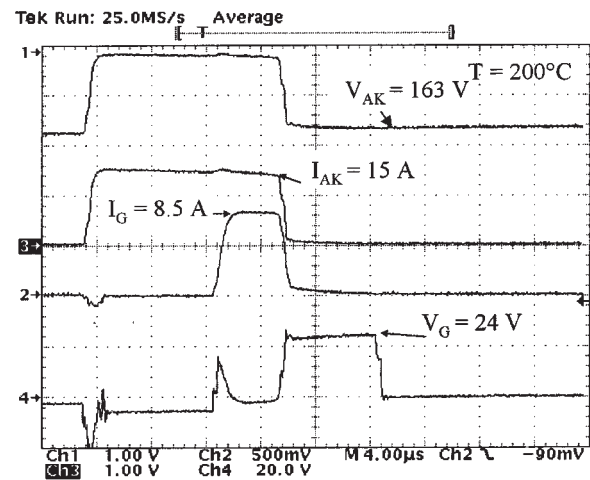


Fig. 22. Forward characteristics of the $2 \times 2 \text{ mm}^2$ GTO thyristor of Fig. 20 measured at room temperature. Anode is grounded and the gate current is 300 mA.

respect to the anode. Fig. 21 indicates that the blocking voltage of this device is at least 3100 V, which, in this case, is limited by the capability of the Tektronix 371 curve tracer. The device can be turned on by forward biasing the anode-to-gate p-n junction. Room-temperature forward characteristics for this device, measured using a Tektronix 370 A curve tracer, are shown in Fig. 22. To minimize the effects of voltage drop in the wires connecting the package to the curve tracer, Kelvin measurements with four wires



(a)



(b)

Fig. 23. Turn-on and turn-off characteristics of the $2 \times 2 \text{ mm}^2$ packaged device (a) at room temperature and (b) at 200 °C.

are performed. The devices show a forward current of 12 A (300 A/cm^2 —normalized to the cathode area) with a voltage drop of 4.97 V.

Fig. 23(a) and (b) show the turn-on and turn-off characteristics of the packaged $2 \times 2 \text{ mm}^2$ GTO at room temperature and at 200 °C. At room temperature, a $1.2\text{-}\mu\text{s}$ long gate pulse of 1 A is applied to turn on the device with 221 V across the anode-to-cathode terminals. The series resistance in the anode to cathode circuit is adjusted between 10–11 Ω to obtain an anode-cathode current $I_{AK} \sim 20 \text{ A}$. The device is turned off by reverse-biasing the gate-anode p-n junction with a 6-A $1.2\text{-}\mu\text{s}$ pulse. The resulting fall time is about 300 ns at a turn-off gain of 3.3. As the device is heated to 200 °C, the lifetimes of the electrons and holes in SiC increase. This results in an increased conductivity modulation of the $50\text{-}\mu\text{m}$ drift layer. This makes it difficult to turn off the device without an increased gate current. Fig. 23(b) shows that at 200 °C, the maximum anode-to-cathode current that can be turned off is about 15 A and required a 8.5-A $6\text{-}\mu\text{s}$

gate pulse (turn-off gain ~ 1.75). The storage time in the device is about 5 μ s at 200 °C, while it is less than 200 ns at room temperature.

V. CONCLUSION

Over the past five years, progress in SiC power-switching devices has been rapid. Several devices have now demonstrated performance figures that far exceed comparable silicon devices and, unlike silicon, the theoretical performance limits for SiC do not impose any near-term constraints on continued progress.

SiC wafers are now commercially available in 75-mm diameters with micropipe densities below 10 cm⁻². This permits high-yield fabrication of transistors and diodes with 20-A capability as single devices and 100 A or higher capability in modules. SiC wafers will continue to increase in size and improve in quality in coming years.

SiC power devices will first appear in specialized commercial applications where silicon parts cannot effectively compete. One such application is freewheeling rectifiers in motor control circuits, where SiC Schottky or p-i-n diodes will displace conventional silicon p-i-n diodes. Substitution of SiC diodes in these systems provides significant systems advantages due to greatly reduced switching losses. Further into the future, SiC transistors and thyristors will begin to displace silicon IGBTs. It is not clear at this point whether these SiC transistors will be MOSFETs, JFETs, or BJTs. JFETs and BJTs have fewer materials issues and are easier to fabricate than SiC MOSFETs, but MOSFETs ultimately offer the greatest advantages over silicon IGBTs because of their high input impedance and low dynamic power dissipation. More development work is needed to bring SiC MOSFETs to their full potential, and the success of this development will determine whether or when SiC MOSFETs enter the commercial marketplace.

REFERENCES

- [1] B. J. Baliga, "Power semiconductor device figure of merit for high-frequency applications," *IEEE Electron Device Lett.*, vol. 10, p. 455, Oct. 1989.
- [2] Y. Sugawara, D. Takayama, K. Asano, R. Singh, J. Palmour, and T. Hayashi, "12-19kV 4H-SiC p-i-n diodes with low power loss," in *Proc. 13th Int. Symp. Power Semiconductor Devices and ICs*, Osaka, Japan, June 4-7, 2001, pp. 27-30.
- [3] J. Tan, J. A. Cooper, Jr., and M. R. Melloch, "High-voltage accumulation-layer UMOSFETs in 4H-SiC," *IEEE Electron Device Lett.*, vol. 19, pp. 487-489, Dec. 1998.
- [4] S.-H. Ryu, A. K. Agarwal, R. Singh, and J. W. Palmour, "1800 V n-p-n bipolar junction transistors in 4H-SiC," *IEEE Electron Device Lett.*, vol. 22, pp. 124-126, Mar. 2001.
- [5] —, "3100-V asymmetrical gate turn-Off (GTO) thyristors in 4H-SiC," *IEEE Electron Device Lett.*, vol. 22, pp. 127-129, Mar. 2001.
- [6] H. Lendenmann, N. Johansson, D. Mou, M. Frischholz, B. Åstrand, P. Isberg, and C. Ovren, "Operation of a 2500V 150A Si-IGBT/SiC Diode Module," *Mater. Sci. Forum*, vol. 338-342, pp. 1423-1426, 2000.
- [7] Infineon Technologies, "SDP04S60, SPD04S60, SDP06S60, SDB06S60, SDP10S30, SDB10S30, and SDB20S30 preliminary data sheets," Jan. 2001.
- [8] S. K. Gandhi, *Semiconductor Power Devices*. New York: Wiley, 1977.
- [9] H. M. McGlothlin, D. T. Morissette, J. A. Cooper, Jr., and M. R. Melloch, "4 kV silicon carbide Schottky diodes for high-frequency switching applications," in *Proc. IEEE Device Research Conf.*, Santa Barbara, CA, June 1999, pp. 42-43.
- [10] A. Itoh, T. Kimoto, and H. Matsunami, "Excellent reverse blocking characteristics of high-voltage 4H-SiC Schottky rectifiers with boron-implanted edge termination," *IEEE Electron Device Lett.*, vol. 17, pp. 139-141, Mar. 1996.
- [11] V. A. K. Temple, "Junction termination extension (JTE), a new technique for increasing avalanche breakdown voltage and controlling surface electric fields in p-n junctions," in *IEDM Tech. Dig.*, 1977, pp. 423-426.
- [12] D. Alok, B. J. Baliga, M. Kothandaraman, and P. K. McLarty, "Argon implanted SiC device edge termination: Modeling, analysis, and experimental results," in *Proceedings of the Sixth International Conference on Silicon Carbide and Related Materials*, ser. 142. Bristol, U.K.: Inst. of Physics, 1996, pp. 565-568.
- [13] K. J. Schoen, J. M. Woodall, J. A. Cooper, Jr., and M. R. Melloch, "Design considerations and experimental characterization of high voltage SiC Schottky barrier rectifiers," *IEEE Trans. Electron Devices*, vol. 45, pp. 1595-1604, July 1998.
- [14] Y. Sugawara, K. Asano, R. Singh, and J. W. Palmour, "6.2kV 4H-SiC p-i-n diode with low forward voltage drop," *Mater. Sci. Forum*, vol. 338-342, pp. 1371-1374, 2000.
- [15] R. Singh and J. W. Palmour, "High temperature characteristics of 8.6 kV 4H-SiC p-i-n diode," presented at the Fifth Int. High Temperature Electronics Conf., Albuquerque, NM, 2000.
- [16] A. Udall and E. Velmer, "Measurement of charge carrier lifetime temperature-dependence in 4H-SiC power devices," *Mater. Sci. Forum*, vol. 338-342, pp. 781-784, 2000.
- [17] J. W. Palmour, J. A. Edmond, H. S. Kong, and C. H. Carter, Jr., "6H-silicon carbide power devices for aerospace applications," in *Proc. 28th Intersociety Energy Conversion Energy Conf.*, 1993, pp. 1.249-1.254.
- [18] J. N. Shenoy, J. A. Cooper, Jr., and M. R. Melloch, "High-voltage double-implanted power MOSFETs in 6H-SiC," *IEEE Electron Device Lett.*, vol. 18, pp. 93-95, Mar. 1997.
- [19] P. Friedrichs, H. Mitlehner, R. Kalschmidt, U. Weinert, W. Bartsch, C. Hecht, K. O. Dohnke, B. Weis, and D. Stephani, "Static and dynamic characteristics of 4H-SiC JFETs designed for different blocking categories," *Mater. Sci. Forum*, vol. 338-342, pp. 1243-1246, 2000.
- [20] R. Singh, S.-H. Ryu, and J. W. Palmour, "High temperature, high current, p-channel UMOS 4H-SiC IGBT," in *Proc. IEEE Device Research Conf.*, Santa Barbara, CA, June 1999, pp. 46-47.
- [21] M. A. Capano, S.-H. Ryu, M. R. Melloch, and J. A. Cooper, Jr., "Dopant activation and surface morphology of ion implanted 4H- and 6H-silicon carbide," *J. Electron. Mater.*, vol. 27, no. 4, pp. 370-376, Apr. 1998.
- [22] M. A. Capano, S. Ryu, J. A. Cooper, Jr., M. R. Melloch, K. Rottner, S. Karlsson, N. Nordell, A. Powell, and D. E. Walker, Jr., "Surface roughening in ion implanted 4H-silicon carbide," *J. Electron. Mater.*, vol. 28, no. 3, pp. 214-218, Mar. 1999.
- [23] M. K. Das, J. A. Cooper, Jr., M. R. Melloch, and M. A. Capano, "Inversion channel mobility in 4H- and 6H-SiC MOSFETs," in *Proc. Semiconductor Interface Specialists Conf.*, San Diego, CA, Dec. 1998.
- [24] P. M. Shenoy and B. J. Baliga, "The planar 6H-SiC ACCUFET: A new high-voltage power MOSFET structure," *IEEE Electron Device Lett.*, vol. 18, p. 589, Dec. 1997.
- [25] K. Hara, "Vital issues for SiC power devices," in *Mater. Sci. Forum*, 1998, vol. 264-268, pp. 901-906.
- [26] A. Agarwal, S.-H. Ryu, M. Das, L. A. Lipkin, J. W. Palmour, and N. Saks, "Large area 4H-SiC power MOSFETs," in *Proc. Int. Symp. Power Semiconductor Devices and ICs*, 2001, pp. 183-186.
- [27] D. Takayama, Y. Sugawara, T. Hayashi, R. Singh, J. W. Palmour, S. Ryu, and K. Asano, "Static and dynamic characteristics of 4-6 kV 4H-SiC SIAFETs," in *Proc. 13th Int. Symp. Power Semiconductor Devices and ICs*, Osaka, Japan, June 2001, pp. 41-44.
- [28] V. V. Afanas'ev, M. Bassler, G. Pensl, and M. Schulz, "Intrinsic SiC/SiO₂ interface states," *Phys. Stat. Sol. (a)*, vol. 162, pp. 321-337, 1997.
- [29] M. K. Das, B. S. Um, and J. A. Cooper, Jr., "Anomalous high density of interface states near the conduction band in SiO₂/4H-SiC MOS devices," *Mater. Sci. Forum*, vol. 338-342, pp. 1069-1072, 2000.

- [30] G. Y. Chung, C. C. Tin, J. R. Williams, K. McDonald, M. Di Ventra, S. T. Pantelides, L. C. Feldman, and R. A. Weller, "Effect of nitric oxide annealing on the interface trap densities near the band edges in the 4H polytype of silicon carbide," *Appl. Phys. Lett.*, vol. 76, no. 27, pp. 1713–1715, Mar. 2000.
- [31] B. S. Um, J. A. Cooper, Jr., unpublished.
- [32] G. Y. Chung, C. C. Tin, J. R. Williams, K. McDonald, R. K. Chanana, R. A. Weller, S. T. Pantelides, L. C. Feldman, O. W. Holland, M. K. Das, and J. W. Palmour, "Improved inversion channel mobility for 4H-SiC MOSFETs following high temperature anneals in nitric oxide," *IEEE Electron Device Lett.*, vol. 22, pp. 176–178, Apr. 2001.
- [33] C.-Y. Lu, J. A. Cooper, Jr., G. Y. Chung, J. R. Williams, K. McDonald, and L. C. Feldman, "Effect of process variations on 4H silicon carbide MOSFET mobility," *Mater. Sci. Forum*, vol. 389–393, pp. 997–980, 2001.
- [34] M. M. Maranowski and J. A. Cooper, Jr., "Time-dependent-dielectric-breakdown measurements of thermal oxides on N-type 6H-SiC," *IEEE Trans. Electron Devices*, vol. 46, pp. 520–524, Mar. 1999.
- [35] B. J. Baliga, "Prospects for development of SiC power devices," in *Proceedings of the Sixth International Conference on Silicon Carbide and Related Materials*, ser. 142. Bristol, U.K.: Inst. of Physics, 1996, pp. 1–6.
- [36] K. Asano, Y. Sugawara, S. Ryu, J. Palmour, T. Hayashi, and D. Takayama, "5.5kV normally-off low RonS 4H-SiC SEJFET," in *Proc. 13th Int. Symp. Power Semiconductor Devices and ICs*, Osaka, Japan, June 2001.
- [37] A. Q. Huang and B. Zhang, "Comparing SiC switching power devices: MOSFET, n-p-n transistor, and GTO thyristor," *Solid-State Electron.*, vol. 44, pp. 325–340, 2000.
- [38] T. Fujihira, "Theory of semiconductor superjunction devices," *Jpn. J. Appl. Phys.*, vol. 36, pp. 6254–6262, 1997.
- [39] *Cool MOS—The competitive advantage for your high-voltage applications*, Siemens Microelectronics, 1998.
- [40] J. W. Palmour, R. Singh, L. A. Lipkin, and D. G. Waltz, "4H silicon carbide high temperature power devices," in *Proc. 3rd Int. High Temperature Electronics Conf.*, vol. 2, Albuquerque, NM, 1996, p. XVI-9.
- [41] A. K. Agarwal, J. B. Casady, L. B. Rowland, S. Seshadri, R. R. Siergiej, W. F. Valek, and C. D. Brandt, "700-V asymmetrical 4H-SiC gate turn-off thyristors (GTOs)," *IEEE Electron Device Lett.*, vol. 18, p. 518, Nov. 1997.
- [42] J. B. Casady, A. K. Agarwal, L. B. Rowland, R. R. Siergiej, S. Seshadri, S. Mani, J. Barrows, D. Piccone, P. A. Sanger, and C. D. Brandt, "4H-SiC gate turn-off (GTO) thyristor development," *Mater. Sci. Forum*, vol. 264–268, pp. 1069–1072, 1998.
- [43] B. Li, L. Cao, and J. H. Zhao, "High current density 800V 4H-SiC gate turn-off thyristors," *IEEE Electron Device Lett.*, vol. 20, p. 219, May 1999.
- [44] S. M. Sze, *Physics of Semiconductor Devices*, 2nd ed. New York: Wiley, 1981.
- [45] B. J. Baliga, *Power Semiconductor Devices*. Boston, MA: PWS, 1996.



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