Status and Prospects for SiC Power MOSFETs

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***Abstract*—SiC electronic device technology has made rapid progress during the past decade. In this paper, we review the evolution of SiC power MOSFETs between 1992 and the present, discuss the current status of device development, identify the critical fabrication issues, and assess the prospects for continued progress and eventual commercialization.**

***Index Terms*—Metal-oxide semiconductor field effect transistors (MOSFETs), power devices, silicon carbide.**

I. Introduction

IT WAS recognized in the late 1980s that power switching devices in silicon were approaching their theoretical limits [1] and that these limits could be significantly extended by fabricating power devices in materials with higher breakdown electric fields, such as silicon carbide (SiC) or semiconducting diamond. For vertically oriented majority carrier devices, the theoretical minimum value of the resistance-area product under optimum punchthrough conditions is

$$R_{SP} = \left(\frac{3}{2}\right)^3 \frac{V_B^2}{\mu_N \varepsilon_S E_C^3} = \frac{3.375 V_B^2}{\mu_N \varepsilon_S E_C^3} \tag{1}$$

where R_{SP} is the specific resistance in Ω-cm^2, μ_N is the electron mobility perpendicular to the surface, ε_S is the permittivity of the semiconductor, E_C is the critical field for avalanche breakdown perpendicular to the surface, and V_B is the designed blocking voltage of the drift region. Although it varies with doping, the critical field E_C in SiC is almost an order of magnitude higher than in silicon. Even allowing for the lower electron mobility, the specific resistance in SiC at a given blocking voltage is about $400\times$ lower than in silicon. At a time when silicon devices are approaching their theoretical limits of performance, such a large improvement is quite significant.

Semiconducting diamond faces several material problems that make implementation of MOSFETs impractical at the present time, but the situation in SiC is much more promising. Commercially available as single crystal wafers since 1990, SiC is the only known compound semiconductor whose native oxide is SiO_2. This makes it an ideal candidate for high-performance power MOSFETs.

SiC is a hexagonal crystal, and the lack of cubic symmetry causes the electron mobility, electron saturation velocity, impact ionization coefficients, thermal oxidation rates, and MOS interface properties all to be anisotropic. The SiC lattice consists of alternating planes of silicon and carbon atoms, and the stacking sequence of these planes defines different *polytypes* of the material, identified by the repeat distance of the stacking sequence (e.g., 3C, 4H, 6H, 15R, etc.). The lattice constant in the basal plane is virtually identical for all polytypes, but important electrical properties such as the bandgap energy, electron mobility, and critical field differ significantly between polytypes. SiC crystals are also polar, so that each wafer has a silicon-terminated face (0001) and a carbon-terminated face ($000\bar{1}$). Oxidation rates and MOS properties are significantly different on the silicon- and carbon-faces of the wafer, and most device fabrication is performed on the (0001) silicon face.

The high thermal and chemical stability of SiC makes certain types of fabrication operations difficult. For example, diffusion coefficients for dopant atoms are extremely low at the temperatures typically used for silicon device processing, and for this reason selective doping of SiC is accomplished by ion implantation. Implant activation typically requires annealing at temperatures between 1000 and 1700 °C. Oxidation rates are lower than in silicon. Chemical etching is impractical owing to the high chemical stability of SiC, and selective etching is accomplished by reactive ion etching (RIE) using flourinated gasses such as NF_3 or SF_6. These factors pose challenges in the fabrication of SiC devices and limit the types of device structures that can be realized in the material. This will become apparent in the discussions of specific device structures below.

II. Experimental Results

A. Early MOSFETs

The first MOSFETs in SiC were reported in the late 1980s [2]–[4] and the first power MOSFETs in 1994 [5]. The power devices were vertical trench MOSFETs, or UMOSFETs, as illustrated in Fig. 1(a). UMOSFETs are attractive because the base and source regions can be formed epitaxially, without the need for ion implantation and associated high-temperature annealing. In UMOSFETs, the MOS channel is formed on the sidewalls of trenches created by RIE. As a result, the MOS interface lies on the "a-axis" surface of the crystal, typically on the $(1\bar{1}00)$ or $(11\bar{2}0)$ planes. Unlike the (0001) silicon face, these a-axis surfaces expose an equal number of silicon and carbon atoms at the interface. Little is known about the oxide-semiconductor bonding on these surfaces, particularly the role of carbon bonds, but the MOS interface is generally thought to be inferior to interfaces formed on the (0001) silicon face, where only silicon atoms are present [6]. However, this conclusion is not firmly established, and one group has reported excellent electron mobility along the $(11\bar{2}0)$ interface [7].

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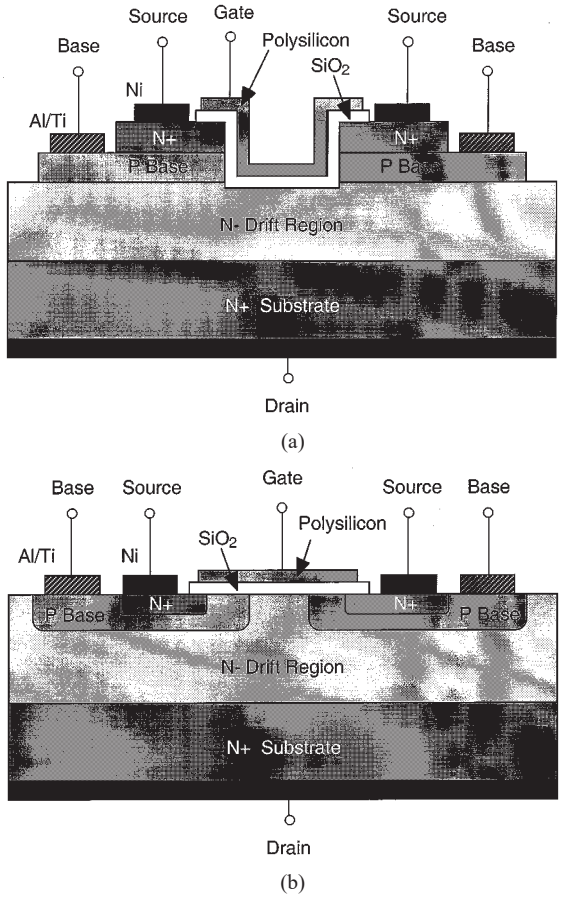

Fig. 1. (a) Cross section of a trench-gate UMOSFET, typical of those made in SiC between 1992 and 1998. Note that the source can be formed either by epitaxy or implantation. (b) Cross section of a planar DMOSFET, typical of those made in SiC since 1996. The base and source are formed by nonself-aligned ion implantation.

Another disadvantage of the UMOS geometry becomes apparent when one considers the peak electric fields in the device. At the onset of avalanche breakdown, the electric field at the p-n junction in SiC is almost 10× higher than in silicon, owing to the higher critical field of the material. At the MOS interface, the field in the oxide exceeds the semiconductor field by the ratio of the dielectric constants, a factor of 2.5. This places the field in the oxide at around 5 MV/cm, a value dangerously close to oxide breakdown. The geometry of the trench corner further increases the oxide field due to field crowding, resulting in local oxide failure. By 1995, UMOSFETs fabricated on the carbon face of SiC had achieved blocking voltages about 260 V [8], limited by oxide breakdown at the trench corners. Further progress was only made after major modifications to the MOSFET geometry, as described in Sections II-B and II-D.

The specific resistance R_{SP} of UMOSFETs produced between 1992 and 1995 was in the range of 10–50 mΩ-cm^2, higher than the theoretical minimum predicted by (1) for those blocking voltages. In these devices, as in all SiC power MOSFETs reported to date, the specific resistance is dominated by the MOSFET channel and not by the drift region. This, in effect, prevents designers from taking full advantage of the higher critical field of SiC, as promised by equation (1). The issue of MOSFET channel resistance and MOS inversion layer mobility will be discussed more fully in Section III.

B. DMOSFETs

An obvious way to avoid the problem with oxide breakdown at the trench corners is to eliminate the trenches. This was accomplished in 1996 with the introduction of planar double-implanted DMOSFETs [9], shown in Fig. 1(b). Since impurity diffusion is impractical in SiC, the base and source regions are formed by successive ion implantation using aluminum or boron for the p-type base and nitrogen for the n^+ source. Because p-type implant anneals are conducted at temperatures between 1600 and 1700 °C, self-aligned implant processes using polysilicon gates are not practical in SiC, and realignment tolerances must be allowed between the base, source, and gate features. However, in spite of these drawbacks, the elimination of the trench corners resulted in a 3× improvement in device blocking voltage, to 760 V.

A useful figure of merit to compare device performance is the ratio V_B^2/R_{SP}. This follows naturally from (1), which represents the ideal situation in which the resistance is dominated by the drift region and there is no two-dimensional (2-D) field crowding. In such a case, V_B^2/R_{SP} has a theoretical maximum value of $(\mu_N \varepsilon_S E_C^3)/3.375$, a quantity that depends only upon fundamental material parameters. Any real device will have a V_B^2/R_{SP} value below the theoretical maximum. Thus, V_B^2/R_{SP} becomes a useful measure of the ideality of a given experimental device.

In addition to the resistance of the MOS inversion layer, the specific resistance of the DMOSFET also includes the resistance of the JFET region between the implanted p-base regions. This introduces a tradeoff in the design: As the spacing between base regions is increased to reduce the JFET resistance, the area of the device also increases, increasing R_{SP}. In addition, as the spacing increases, and the effectiveness of the base regions in terminating the electric field in the blocking state diminishes, increasing the field in the oxide and lowering the blocking voltage. The optimum base spacing can be defined as that value that maximizes the value of V_B^2/R_{SP} for the DMOSFET.

The DMOSFET geometry offers many advantages in SiC, and several groups have reported novel DMOS variations. The most notable of these are the accumulation-channel DMOSFET developed at North Carolina State University, Raleigh, in 1997 [10], the triple-implanted DMOSFET reported by Siemens in 1998 [11], and the static induction accumulation FET (SIAFET) developed by Kansai Electric Power Company (KEPCO) and Cree, Inc., Durham, NC, in 2000 [12]. The accumulation-channel DMOSFET is formed by burying the p-base beneath the surface, leaving a thin n-type region adjacent to the oxide-semiconductor interface. This increases the effective MOS channel mobility, reducing R_{SP}. The North Carolina State device exhibited a blocking voltage of 350 V, specific resistance of 18 mΩ-cm^2, and V_B^2/R_{SP} of 6.8 MW/cm^2. The triple-implanted 6H-SiC DMOSFET reported by Siemens exhibited a blocking voltage of 1800 V, specific resistance of 46 mΩ-cm^2, and V_B^2/R_{SP} of 70 MW/cm^2.

The SIAFET developed by KEPCO and Cree is structurally similar to the accumulation-channel DMOSFET, but each cell of the device contains a channel-terminating p^+ surface contact that plays an important role in both blocking and on-state

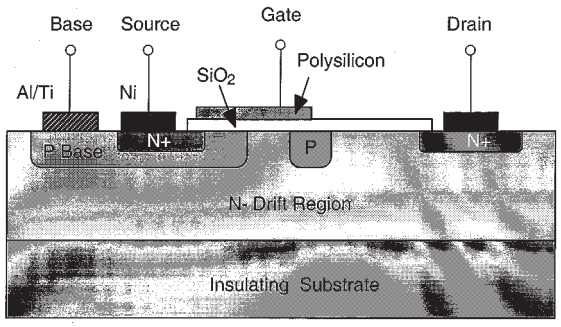

Fig. 2. Cross section of a lateral DMOSFET on an insulating substrate, first introduced in SiC in 1997.

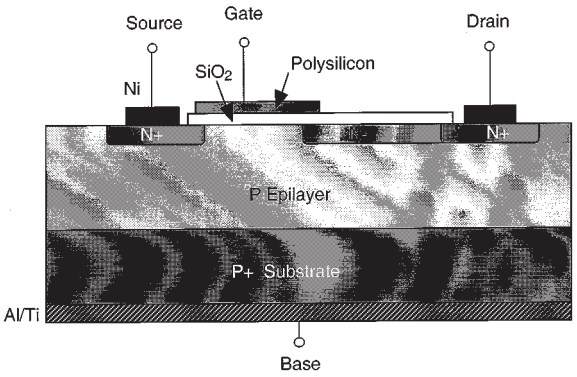

Fig. 3. Cross section of a lateral RESURF DMOSFET on a p-type substrate.

operation. In the on-state, the p^+ surface contact and buried p-base are forward biased relative to the channel, reducing the lateral depletion of the JFET region between the buried p-base regions and conductivity modulating both the channel and JFET regions. This makes it possible to design the device with a smaller JFET gap than would otherwise be the case, providing increased protection to the gate oxide in the blocking state. At the present time the SIAFET holds the record for MOSFET blocking voltage, 6.1 kV, with a specific resistance of 732 mΩ-cm^2 and a V_B^2/R_{SP} of 51 MW/cm^2 [12]. For comparison, the theoretical maximum V_B^2/R_{SP} for *silicon* power MOSFETs is only about 4 MW/cm^2.

C. LDMOSFETs

SiC lateral DMOSFETs were introduced in 1997 [13] to enable blocking voltages higher than permitted by the thickness of the epilayers available at that time. The basic geometry, Fig. 2, consists of an n-type epilayer on an insulating SiC substrate. As in the conventional DMOSFET, the p-base and n^+ source are formed by ion implantation. The source implant step is also used to form a drain contact on the top surface, allowing the drift region to extend laterally along the surface instead of vertically. The original LDMOSFET [13] exhibited a blocking voltage of 2600 V, 3$\times$ higher than that of vertical devices available at the time.

The LDMOSFET requires a large surface area to accommodate the lateral drift region, but this can be minimized by employing reduced-surface-field (RESURF) design techniques [14]. In the RESURF technique, an n-type drift region is implanted into a p-type epilayer, as illustrated in Fig. 3. In the blocking state, the drift region depletes before reaching avalanche breakdown, and field lines from donor atoms in the depleted drift region extend vertically, terminating on acceptor atoms in the underlying p-type epilayer. Since field lines are oriented vertically and not horizontally, there is very little field taper from source to drain. Thus, the lateral field remains almost constant along the drift region, and an arbitrarily high blocking voltage can be achieved simply by moving the drain further from the source. In practice, the blocking voltage is limited by vertical breakdown between the drain and the underlying p-type epilayer. If field crowding at the ends are ignored and a constant lateral field is assumed along the drift region, the specific resistance of a RESURF LDMOSFET is approximately 4$\times$ *lower* than given by (1) for a vertical device of the same blocking voltage [15]. However, in practice it is very difficult to achieve a constant lateral field along the drift region, and RESURF devices have so far not proven competitive with vertical MOSFETs in SiC. In addition, RESURF devices are much more sensitive to the surface charge in the oxide above the active SiC layer, a particularly difficult problem in SiC.

D. Advanced UMOSFETs

In our discussion of early UMOSFETs, we noted that their blocking voltage was limited by oxide breakdown at the trench corners. A number of attempts were made to alleviate this problem by tapering the sidewalls or rounding the corners using proprietary processing techniques. A notable example is the UMOSFET reported by Denso Corp., Japan, in 1997 [16]. This device utilizes rounded trench corners and incorporates an n-type epilayer grown subsequent to trench etch, forming the first accumulation-channel UMOSFET. This UMOSFET exhibited a blocking voltage of 450 V, specific resistance of 10.9 mΩ-cm^2, and V_B^2/R_{SP} of 18.6 MW/cm^2.

In 1998, Purdue University reported a SiC accumulation-channel UMOSFET with new structural features that shielded the trench oxide from high electric fields in the blocking state [17]. A cross section of this device is shown in Fig. 4. The new features consist of a p-type region formed in the trench bottom by self-aligned ion implantation, and a thin n-type epilayer incorporated between the n-drift region and the p-type base. The p-type trench implant is grounded, and shields the trench oxide from high electric fields in the blocking state. The n-type epilayer prevents JFET pinch-off between the trench implant and the base, and promotes lateral current spreading in the on-state, eliminating current crowding at the trench corners. The device also incorporates an n-type epilayer grown after the trench etch and implant steps, as in the Denso device. The Purdue UMOSFET exhibited a blocking voltage of 1400 V, specific resistance of 15.7 mΩ-cm^2, and V_B^2/R_{SP} of 125 MW/cm^2, about 25$\times$ higher than the theoretical limit for conventional silicon MOSFETs.

E. Comparison of Devices

Fig. 5 shows specific resistance and blocking voltage for the leading SiC power MOSFETs reported to date. Diagonal lines in the figure represent the theoretical limits given by (1) using parameters for silicon and 4H-SiC, respectively. As seen, a number

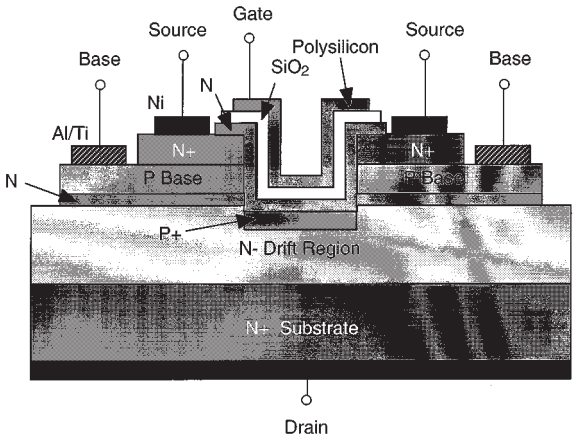

Fig. 4. Cross section of an advanced accumulation-channel UMOSFET introduced in 1998. New features include a p^+ region at the bottom of the trench to protect the oxide from high fields in the blocking state, an n-type layer below the base to prevent JFET pinchoff of the channel and promote lateral current spreading, and an n-type epilayer grown on the trench sidewalls to form an accumulation channel at the MOS interface.

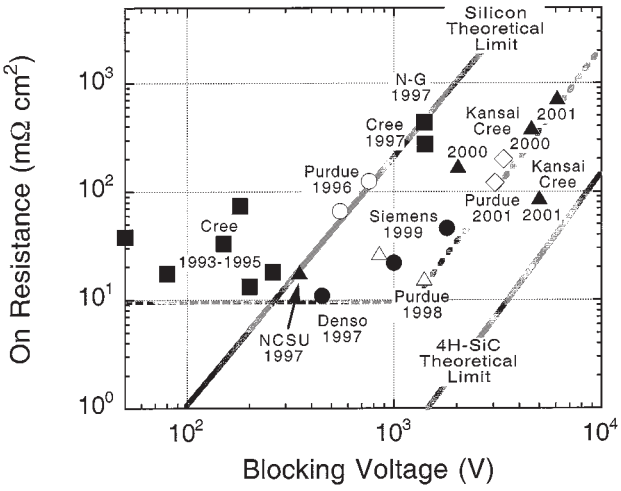

Fig. 5. On resistance and blocking voltage of representative SiC MOSFETs fabricated between 1992 and the present. Solid diagonal lines represent the theoretical limits for silicon and 4H-SiC given by (1), and the dashed line represents the current state-of-the-art in SiC.

of SiC power MOSFETs exceed the theoretical limit for silicon MOSFETs by a wide margin, but so far none come close to the theoretical limit for 4H-SiC. This is because the specific resistance in these devices is dominated by the MOSFET channel, and not by the drift region. Examination of the figure reveals that little progress has been made in reducing the specific resistance over the past eight years. We will discuss the device physics underlying this problem in Section III.

In spite of the lingering problems with MOS channel resistance, overall progress has been impressive. Blocking voltage has increased at the average rate of 75% per year over the past seven years, as shown in Fig. 6. The hot-wall epigrowth technique [18], [19] makes it feasible to obtain drift regions up to 200 μm thick, which should enable blocking voltages of about 20 kV (PiN diodes have already demonstrated blocking voltages of 19.3 kV [20].) Work is currently underway to improve our understanding of the SiC/SiO_2 interface and increase the MOS channel mobility. This is expected to push the performance much closer to the theoretical limits predicted by (1).

III. MOSFET Processing Issues

A. Effect of Implant Activation Annealing on Inversion Layer Mobility

Since diffusion is impractical in SiC, selective doping must be accomplished by ion implantation. Activation of implanted dopants requires annealing at temperatures between 1000 and 1700 °C, depending upon the implant species and polytype [21], [22]. At the higher temperatures, surface degradation occurs due to loss of silicon from the surface and an associated phenomenon known as step bunching [23]. Step bunching arises as a result of the intentional miscut angle of the substrate needed to preserve the polytype stacking sequence during epigrowth, typically 3.5° for 6H-SiC and 8° for 4H-SiC. At the higher annealing temperatures, the surface atoms become mobile, and the surface seeks to minimize its energy by reducing the number of steps. This results in fewer but higher steps, a phenomenon known as step bunching. The inversion layer mobility of MOSFETs fabricated on step-bunched surfaces can be extremely low, often less than 1 cm^2/Vs. Experiments at various institutions [24] indicate that annealing in a silicon-rich ambient significantly improves surface morphology. However, even if visually smooth surfaces are maintained during the anneal, the MOSFET inversion layer mobility can still be quite low [25], and research in this area is continuing.

B. Effect of Interface States on Inversion Layer Mobility

From 1992 to 1997, SiC MOS research focussed on reducing the density of interface states on p-type SiC, since this is the material on which n-channel MOSFETs are made. Due to the wide bandgap of SiC, however, conventional MOS measurement techniques can only probe the lower half of the bandgap on p-type substrates. Through a series of incremental improvements [26]–[28], the average interface state density D_{IT} in the lower half of the bandgap was reduced from 6×10^{11} eV^{-1} cm^{-2} in 1992 to around 1.5×10^{11} eV^{-1} cm^{-2} in 1996. In the best devices, the interface state density decreases into the mid-10^{10} eV^{-1} cm^{-2} range near midgap [29]. At these levels, it was felt that interface state density had little impact on MOSFET performance. However, in 1997 Afanasev and co-workers [30] reported internal photoemission (IPE) measurements of interface state density in the upper-half of the bandgap that show D_{IT} rising exponentially toward the conduction band, reaching levels above 10^{13} eV^{-1} cm^{-2} near the band edge. These measurements have since been confirmed by other groups [31], [32] using MOS admittance measurements on n-type substrates. Fig. 7 shows interface state density measured on both p-type and n-type SiC samples using the AC conductance technique.

An exponentially increasing interface state density in the upper half of the bandgap can be highly detrimental to the inversion layer mobility in MOSFETs because of two effects [31], [33], [34]. First, a substantial fraction of the electron charge induced at the interface will be held in traps, and

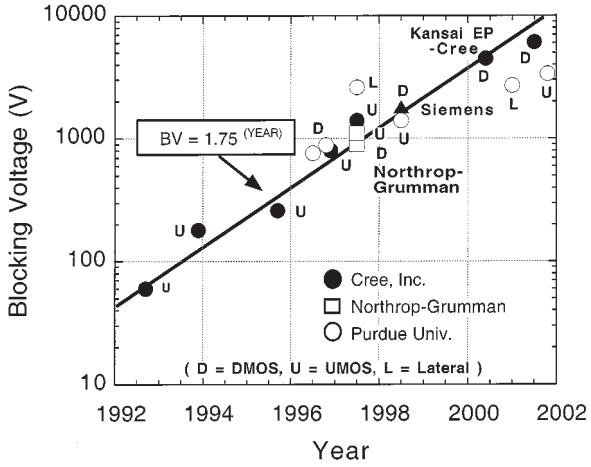

Fig. 6. Best reported blocking voltage versus year for SiC MOSFETs. Blocking voltage has increased at about 75% per year since 1992.

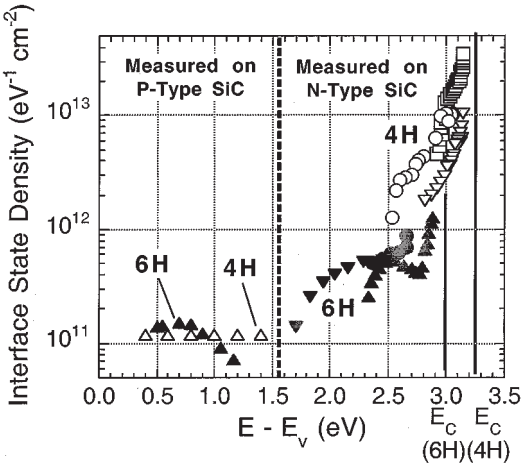

Fig. 7. Interface state density for thermally grown SiO_2 on 4H-SiC (open symbols) and 6H-SiC (solid symbols), as measured by the hi–lo technique (triangles) and the ac conductance technique (circles and squares). Data in the upper half of the bandgap are measured on n-type epilayers, and data in the lower half are measured on p-type epilayers. Although the interface state density appears similar on the two polytypes, the wider bandgap of 4H-SiC allows the interface state density to reach much higher levels near the conduction band.

these carriers are not available for conduction. Second, the trapped electrons give rise to strong Coulomb scattering of the remaining mobile electrons, reducing their mobility. The combined effect can easily account for the observed low inversion layer mobilities in both 4H and 6H polytypes. Work is underway to reduce the interface state density in the upper half of the bandgap, and significant progress has been achieved using post-oxidation annealing in nitric oxide (NO) [35], [36]. It has recently been demonstrated that this anneal can lead to higher inversion layer mobilities [37], [38], but the picture is still not totally clear and the results have yet to be transferred to high voltage power MOSFETs.

C. Oxide Reliability Considerations

As discussed earlier, the higher critical field of SiC means that the surface electric fields in SiC MOSFETs can be up to 10× higher than in silicon devices. This places greater stress on the gate oxide, and raises concerns about oxide reliability, especially at elevated temperatures. The concern is heightened because the conduction band offset between SiO_2 and SiC is lower than between SiO_2 and silicon. The most severe degradation occurs when electrons are injected from the SiC into the oxide, as will occur in an n-channel MOSFET in the conducting state. Only a limited amount of work has been performed on SiC oxide reliability [39], but these studies suggest that acceptable reliability can be maintained if the oxide electric field is kept below about 4 MV/cm and the temperature below 150 °C. Higher temperatures can be tolerated if the oxide field is further reduced. Unfortunately, it appears that long term operation of SiC MOS devices above 200–250 °C will not be feasible.

IV. Summary and Conclusions

SiC MOSFETs have achieved blocking voltages of 6.1 kV and performance figures-of-merit 70× higher than the theoretical limit for silicon MOSFETs. Blocking voltages have increased at an average rate of 75% per year for the past eight years. In spite of this progress, SiC MOSFETs are not yet economically competitive with silicon devices, and therefore are not yet ready for commercialization.

Two aspects of SiC MOSFET development require further improvement. First, inversion layer mobility needs to be increased. This will require minimizing surface degradation due to implant anneals while reducing interface state density, possibly using post-oxidation annealing techniques now under investigation. The incorporation of accumulation-channel surface layers or buried channel implants may provide an alternate route around the mobility limitations. Second, device size needs to be increased to provide absolute currents in the tens of amps instead of fractions of an amp, and a manufacturable process must be developed that can produce high performance devices with good yield at an acceptable cost. This requires improvements in SiC material quality, increases in wafer size, and reductions in wafer cost, topics addressed by an accompanying paper in this issue [40].

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