

10 A, 2.4 kV Power DiMOSFETs in 4H-SiC

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Abstract—We report the characteristics of large area ($3.3 \times 3.3 \text{ mm}^2$) high-voltage 4H-SiC DiMOSFETs. The MOSFETs show a peak MOS channel mobility of $22 \text{ cm}^2/\text{V}\cdot\text{s}$ and a threshold voltage of 8.5 V at room temperature. The DiMOSFETs exhibit an on-resistance of $42 \text{ m}\Omega\cdot\text{cm}^2$ at room temperature and $85 \text{ m}\Omega\cdot\text{cm}^2$ at 200°C . Stable avalanche characteristics at approximately 2.4 kV are observed. An on-current of 10 A is measured on a 0.103 cm^2 device. High switching speed is also demonstrated. This suggests that the devices are capable of high-voltage, high-frequency, low-loss switching applications.

Index Terms—Avalanche, fast switching, high voltage, MOSFET, NO anneal, silicon carbide.

I. INTRODUCTION

VERY HIGH critical field ($\sim 2 \text{ MV/cm}$) and good bulk electron mobility ($\sim 800 \text{ cm}^2/\text{V}\cdot\text{s}$) make 4H-silicon carbide very attractive for high-speed unipolar switching devices for blocking voltages ranging from 600 V to 3000 V [1], [2]. At such high voltages, conventional silicon devices typically utilize conductivity modulation in the drift layer, resulting in slower switching speeds. Several exploratory devices, such as vertical MOSFETs [3]–[7] and vertical JFETs [8], [9] have been demonstrated in SiC. However, none of the devices reported to date demonstrated reasonable current ratings and normally off characteristics. In this letter, we present results from our latest 4H-SiC DiMOSFETs (double-implanted MOSFETs) [3], [10] with active areas of up to 0.103 cm^2 . The 0.103 cm^2 device exhibits a specific on-resistance of $42 \text{ m}\Omega\cdot\text{cm}^2$, a drain current of 10 A at a forward drop of 7.2 V, and a blocking voltage of around 2.4 kV.

II. DEVICE DESIGN AND FABRICATION

A simplified schematic cross section of a DiMOSFET cell is shown in Fig. 1. The MOS channel length, defined by the p-well and n^+ implants, is $1.5 \mu\text{m}$. Electrons flow laterally from n^+ source through an MOS channel on the implanted p-well, then flow vertically through the JFET region formed by two adjacent p-well regions, and then through the lightly doped n^- drift region into the drain. The cell pitch is $16 \mu\text{m}$, and packing density of the gate periphery is 1250 cm/cm^2 . A $20 \mu\text{m}$ thick

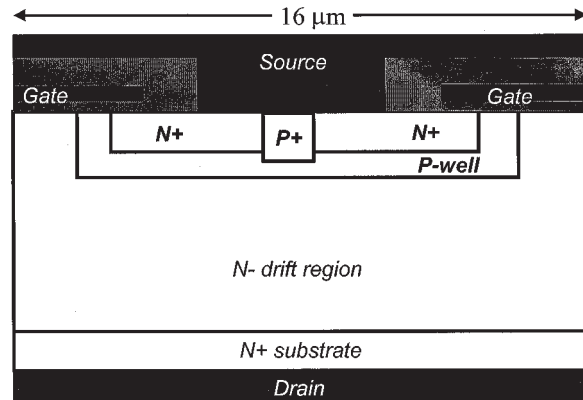


Fig. 1. Simplified cross-sectional view of a DiMOSFET cell.

drift layer with a doping concentration of $2.5 \times 10^{15} \text{ cm}^{-3}$ was chosen for a 2000 V blocking voltage design.

P-wells, with a surface concentration of around $1 \times 10^{16} \text{ cm}^{-3}$, were formed by aluminum implantation. N^+ source regions were then formed by a heavy-dose nitrogen implantation. A heavy dose aluminum implantation formed p^+ contacts to the p-wells, as well as the floating guard rings to terminate the edges. All the implants were activated at around 1600°C in Ar. A $2\text{-}\mu\text{m}$ -thick oxide layer was then deposited and patterned as the field oxide followed by a gate oxidation. $500\text{-}\text{\AA}$ -thick gate oxide was thermally grown at 1200°C in dry O_2 , then annealed in NO at Auburn University, Auburn, AL, as described in [11]. Then, a $0.25 \mu\text{m}$ thick Molybdenum layer was sputtered and patterned as gate metal. The gate was then metallized with a $0.25\text{-}\mu\text{m}$ -thick Ni/Au layer to reduce the gate resistance further. The contacts to source, drain, and p^+ regions were formed with alloyed Ni. A PECVD oxide layer was then deposited as an inter-metallic dielectric, and via holes were opened. Finally, a $2\text{-}\mu\text{m}$ -thick Ti/Pt/Au layer was e-beam evaporated and lifted off as the final metal layer.

III. EXPERIMENTAL RESULTS

Fig. 2 shows the effective MOS channel mobility (μ_{eff}) and threshold voltage (V_{TH}) measured on a lateral test MOSFET with a W/L of $200 \mu\text{m}/200 \mu\text{m}$. A peak mobility of $22 \text{ cm}^2/\text{Vs}$ and a V_{TH} of 8.5 V are measured at room temperature. At 200°C , the peak mobility increases to $27 \text{ cm}^2/\text{Vs}$ and the V_{TH} shifts to 5.5 V. This suggests that the MOS channel is still severely affected by interface traps [12]. Fig. 3(a) shows the on-state characteristics of a $3.3 \text{ mm} \times 3.3 \text{ mm}$ (active area = 0.103 cm^2) DiMOSFET at room temperature, measured using a Tektronix 370 curve tracer. The device is normally off, and shows an on-current of 10 A (97 A/cm^2)

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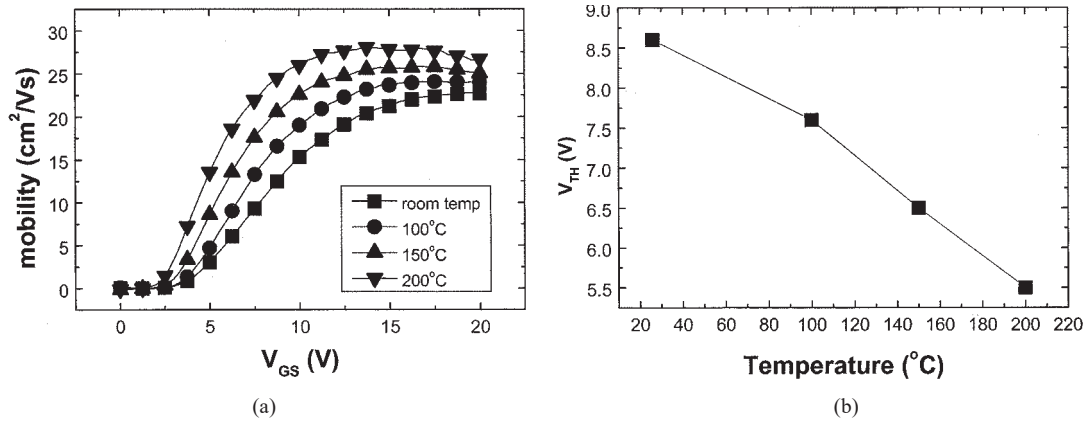


Fig. 2. (a) Effective MOS channel mobility and (b) threshold voltage extracted from a 200 $\mu\text{m}/200 \mu\text{m}$ 4H-SiC test MOSFET. V_{DS} was fixed at 50 mV.

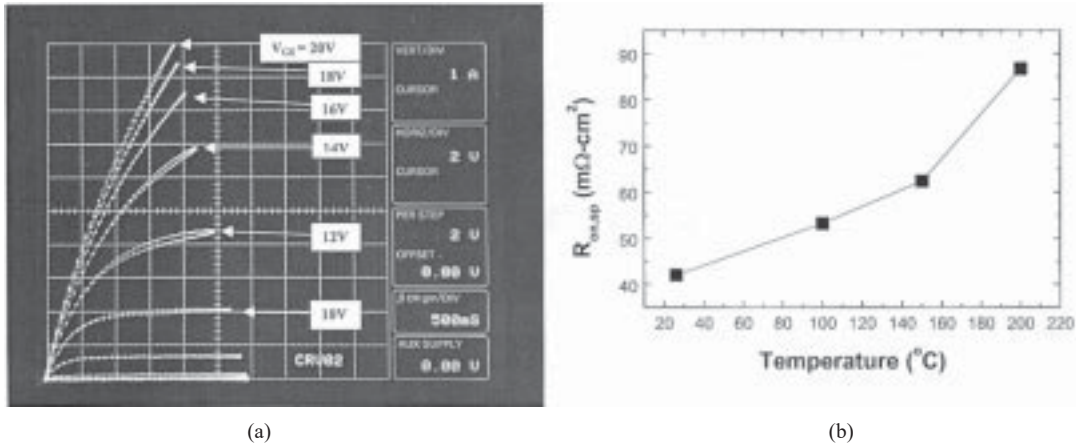


Fig. 3. (a) On-state current-voltage $I-V$ characteristics of a 0.103 cm² 4H-SiC DiMOSFET. (b) Specific on-resistance of a 4H-SiC DiMOSFET as a function of temperature.

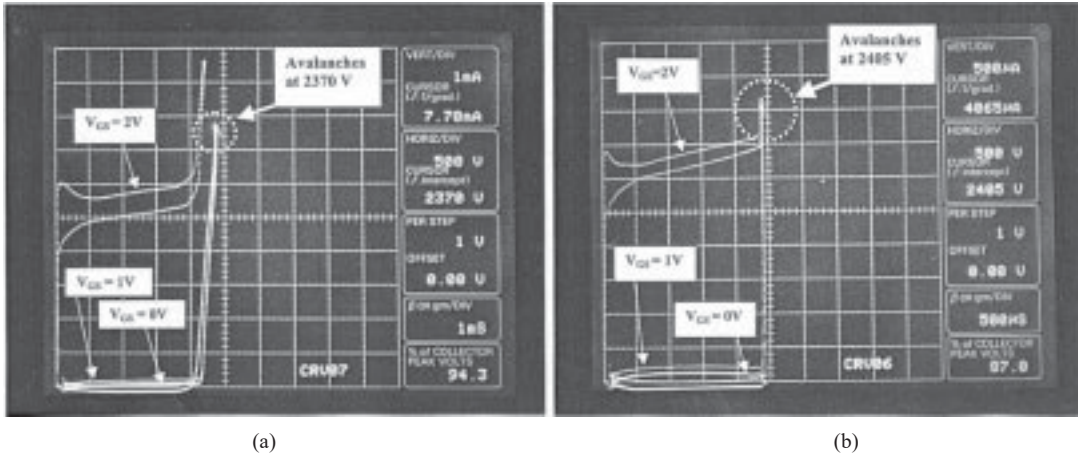


Fig. 4. (a) Blocking characteristics of a 0.103 cm² 4H-SiC DiMOSFET. (b) Blocking characteristics of a 0.0387 cm² 4H-SiC DiMOSFET. Both measurements were done at room temperature, and the devices were immersed in Fluorinert™ oil.

at a forward drop of around 7.2 V. Specific on-resistance, $R_{on,sp}$, measured with $V_{GS} = 20$ V and $V_{DS} = 1$ V at room temperature, is around 42 mΩ·cm². The specific on-resistance is very dependent on the gate bias, and high gate voltages were required to turn the devices fully on, indicating that the on-resistance is dominated by the MOS channel resistance at room temperature. This suggests that further improvement in the μ_{eff} is necessary to reduce the on-resistance. A higher μ_{eff} is also expected to result in improved long-term reliability

of the device because a lower gate bias (with less stress on the gate dielectric) can be used to fully turn on the device. Fig. 3(b) shows $R_{on,sp}$ as a function of temperature. The $R_{on,sp}$ value increases with temperature despite the increase in μ_{eff} and the negative shift in V_{TH} , due to decrease in electron mobility in the drift layer. This enables easy paralleling of these devices.

Fig. 4(a) shows the blocking capability of the same device at room temperature, measured using a Tektronix 371 curve tracer. The measurement was done in Fluorinert™ oil. The

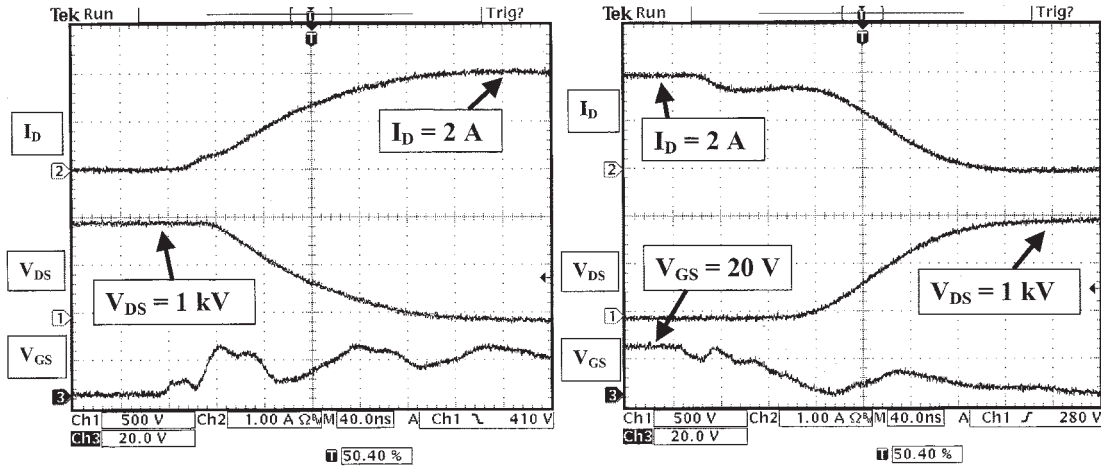


Fig. 5. Room temperature dynamic characteristics of a 0.0387 cm^2 4H-SiC DiMOSFET. A supply voltage of 1000 V, a 500Ω resistive load, and a 50Ω gate resistor were used for the measurement. The switching frequency of the gate drive was 100 kHz. (a) Turn-on transients and (b) turn-off transients.

device starts showing some leakage current at a V_{DS} of 2100 V, then avalanches at a V_{DS} of 2370 V. This blocking voltage is approximately 75% of the ideal parallel plate blocking voltage of the epilayer (3100 V), assuming a critical electric field (E_c) of 2 MV/cm. The blocking characteristics of a smaller (0.0387 cm^2) device placed adjacent to the device are shown in Fig. 4(b). Since the area of this device is smaller, it contains less material defects, and no significant leakage current is observed until it reaches avalanche conditions. None of the curves ($V_{GS} = 0 \text{ V}, 1 \text{ V}, 2 \text{ V}$) in Fig. 4(b) show signs of early breakdown until V_{DS} reaches 2405 V, at which point the device shows avalanche breakdown. The avalanche was powered up to 4 mA ($=0.1 \text{ A/cm}^2$), which corresponds to a power density of about 240 W/cm^2 .

Fig. 5 shows dynamic characteristics of a —packaged 0.0387 cm^2 device at room temperature. A supply voltage of 1000 V, a 500Ω resistive load, a 50Ω gate resistor, and a 100 kHz gate pulse were used for this measurement. The device switches 2 A of drain current (about 52 A/cm^2) with a turn-on delay, $t_{d(on)}$, of 40 ns, a rise time, t_r , of 140 ns, a turn-off delay, $t_{d(off)}$, of 100 ns, and a fall time, t_f , of 120 ns. This shows that these DiMOSFETs are suitable for low loss, high speed power switching applications.

IV. CONCLUSION

The 2.4 kV DiMOSFETs in 4H-SiC have been successfully fabricated. The devices have an MOS channel mobility of $22 \text{ cm}^2/\text{V}\cdot\text{s}$ and a threshold voltage of 8.5 V. The DiMOSFETs exhibit an on-resistance of $42 \text{ m}\Omega\cdot\text{cm}^2$ at 27°C , which increases with the temperature. The on-resistance is dominated by the MOS channel resistance, which suggests that further improvement in the MOS channel mobility is necessary to improve the device performance. A blocking voltage of around 2.4 kV is observed, and an on-current of 10 A is measured from a 0.103 cm^2 device. Dynamic measurement of these devices showed a turn-on time ($t_{d(on)} + t_r$) of 180 ns and a turn-off time ($t_{d(off)} + t_f$) of 220 ns when controlling a current density of 52 A/cm^2 with a 1000 V supply voltage. The excellent blocking

capability and fast switching speed of the devices suggest that these devices will enable high-voltage, high-frequency, and low-loss power switching applications.

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