International Journal of High Speed Electronics and Systems
Vol. 14, No. 3 (2004) 879–883

World Scientific
www.worldscientific.com

2 KV 4H-SiC DMOSFETS FOR LOW LOSS, HIGH FREQUENCY SWITCHING APPLICATIONS

SEI-HYUNG RYU, SUMI KRISHNASWAMI, MRINAL DAS,
JAMES RICHMOND, ANANT AGARWAL, AND JOHN PALMOUR

Cree, Inc., 4600 Silicon Drive, Durham, NC 27703, USA

JAMES SCOFIELD

Air Force Research Laboratory, Wright-Patterson Airforce Base, OH 45433, USA

Due to the high critical field in 4H-SiC, the drain charge and switching loss densities in a SiC power device are approximately 10X higher than that of a silicon device. However, for the same voltage and resistance ratings, the device area is much smaller for the 4H-SiC device. Therefore, the total drain charge and switching losses are much lower for the 4H-SiC power device. A 2.3 kV, 13.5 mΩ-cm2 4H-SiC power DMOSFET with a device area of 2.1 mm x 2.1 mm has been demonstrated. The device showed a stable avalanche at a drain bias of 2.3 kV, and an on-current of 5 A with a VGS of 20 V and a VDS of 2.6 V. Approximately an order of magnitude lower parasitic capacitance values, as compared to those of commercially available silicon power MOSFETs, were measured for the 4H-SiC power DMOSFET. This suggests that the 4H-SiC DMOSFET can provide an order of magnitude improvement in switching performance in high speed switching applications.

1 Introduction

The high critical field (E_c) of 4H-SiC enables Power MOSFETs in 4H-SiC using drift layers with 10% of the thickness and 100 times the doping concentration as compared to silicon devices with comparable blocking voltages (BV). Therefore, the drift layer charge per unit area for a 4H-SiC MOSFET is expected to be a factor of 10 greater than that of a silicon MOSFET with the same BV. However, the device area for a 4H-SiC MOSFET is expected to be a factor of 100 smaller than that of a silicon MOSFET with comparable voltage and on-resistance ratings due to the reduction in drift layer resistance. Therefore, the total drift layer charge for a 4H-SiC MOSFET is a factor of 10 smaller than that of a silicon device, and a 10X improvement in switching characteristics over silicon devices are expected for 4H-SiC devices [1]. In this paper, characteristics of our 2.3 kV 4H-SiC DMOSFETs are presented, and its internal capacitances, which are an indicator of switching speeds, are compared to those of commercially available silicon MOSFETs.

2 Switching Characteristics of Power Switches

Turn-on and turn-off transients of power switches can be viewed as charging and discharging operations of parasitic capacitances. Simplified diagrams of power MOSFET turn-on and turn-off transients are given in Fig. 1. During the turn-off transient, the drain capacitances, C_{GD} and C_{DS}, are charged by the load current. The charge stored in the drain capacitance can be obtained by calculating the depletion charge in the drift layer using critical field (E_C) and Gauss's law,

(a) (b)

Figure 1. Simple diagrams of (a) turn-off and (b) turn-on transients of a power switch.

$$Q_D = A \cdot \varepsilon \cdot E_C . \tag{1}$$

where A is the device area, including the edge termination structure. The load current (I_D) determines the charging rate. Therefore, the voltage rise time (t_r) can be given as:

$$t_r = Q_D / I_D = A \cdot \varepsilon \cdot E_C / I_D \tag{2}$$

During the turn-on transient, the charge stored in the drain capacitance is discharged through the switch. The turn-on time, or voltage fall time (t_f), is determined by the transconductance of the switch, and does not depend on the load current. The t_f can be substantially reduced by using low resistance gate drives, i.e., gate drives with higher current capabilities. However, t_r is determined by the parasitic capacitances and external load current, and cannot be reduced by using stronger gate drives. The switching time is generally determined by t_r, which is proportional to drain charge.

The switching power loss can be estimated by multiplying the stored energy by switching frequency.

$$P_{sw} = A \cdot f \cdot \int_0^{V_{DD}} C \cdot V \cdot dV = A \cdot f \cdot (1/3) \cdot \varepsilon \cdot E_C \cdot V_{DD} \tag{3}$$ [2,3]

It is shown in Eqs. (1) and (3) that the drain charge and switching loss per unit area is directly proportional to E_C. Since E_C in 4H-SiC is approximately 10 times higher than that of silicon, the drain charge and switching loss per unit area are also 10 times higher in 4H-SiC. However, the drift layer of a 4H-SiC device is 10X thinner, and 100X higher doped than that of a silicon device with the same blocking voltage. The electron mobility in 4H-SiC is approximately 70% of that of silicon. Hence, the specific on-resistance of a 4H-SiC device can be theoretically calculated to be a factor of 700 smaller than that of a silicon device. The device area for the same blocking voltage and the same on-resistance will be a factor of 700 smaller for 4H-SiC devices. Therefore, from Eqs. (2) and (3), the drain

charge and switching loss can be 70X smaller for the 4H-SiC device when compared to a silicon device with the same on-resistance and blocking voltage ratings.

3 Experimental

A simplified cross-section of a 4H-SiC power DMOSFET is shown in Fig. 2. The DMOSFET structure is preferred in 4H-SiC because it is an MOS controlled planar structure. Also, the implanted p-wells shield the MOS gate region from high electric fields.

A 15 μm thick, 5.5 x 10^{15} cm^{-3} doped n-type epilayer was grown on an n^+, 4H-SiC substrate as the drift layer for the device. P-wells, 0.7 μm deep, were formed via aluminum ion implantation, after which 0.3 μm deep n^+ source regions were formed by nitrogen implantation. The MOS gate length, defined by these two implants, was 0.5 μm. A heavy dose aluminum implantation formed p^+ contacts to the p-wells as well as the floating guard rings. A 1 μm thick oxide layer was then deposited and patterned as the field oxide. Approximately 600 Å thick gate oxide layer was thermally grown at 1200°C in dry O_2, then nitrided in N_2O. A degenerately doped polysilicon layer was deposited and patterned as the gate electrode. An LPCVD oxide layer (1 μm thick) was then deposited as an inter-metallic dielectric layer, and via holes were opened. The source and drain ohmic contacts were formed with alloyed Ni. Finally, an aluminum overlayer was deposited and etched to form electrodes.

Figure 3 shows the I_D-V_{GS} characteristics of a 150 μm / 150 μm test MOSFET, built on a p-well adjacent to the power DMOSFET. A V_{DS} of 50 mV was used for the measurement. A peak effective channel mobility of 17 cm^2/Vs was extracted from the first derivative of the IV curve, and a threshold voltage of 8 V was extracted from the linear portion of the IV curve.

Figure 4(a) shows the room temperature on-state characteristics of a 4H-SiC power DMOSFET. The active area of this device is 2.78x10^{-2} cm^2, and the total chip size is 2.1 mm x 2.1 mm. The threshold voltage extracted from saturation region is approximately 4 V, which is significantly lower than the value measured from the 150 μm long test MOSFET. With a gate bias of 20 V (E_{OX} = 3.3 MV/cm), the device showed an on-current of 5 A at a forward drop of 2.6 V. The specific on- resistance measured was 13.5 mΩ-cm^2. The off-state characteristics are shown in Fig. 4(b). The device is normally-off, and showed stable avalanche behavior at a V_{DS} of 2.3 kV. The theoretical parallel plate electric field is approximately 2.1 MV/cm at this voltage. It is shown that reducing the channel length down to 0.5 μm does not affect the breakdown voltage.

The internal capacitances of the 4H-SiC DMOSFET are compared to those of commercially available silicon power MOSFETs in Table 1. When compared to a conventional 1200 V silicon MOSFET [4], a factor of 9 reduction in all capacitance values (normalized in on-resistance only) is shown. The advantages in input and reverse transfer capacitances reduce when the comparison is made to the charge compensated MOSFETs [5]. However, there still is a factor of 8 difference in output capacitance, which determines the switching time and losses, between the 2.3 kV 4H-SiC DMOSFET and the 800 V CoolMOS transistor. This suggests that the 4H-SiC DMOSFETs can have

a significant advantage over silicon devices in high speed power switching applications, regardless of the device structure.

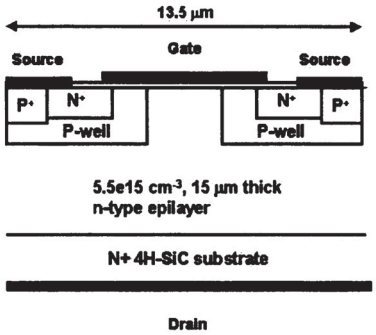

Fig. 2. Simplified 4H-SiC DMOSFET cross-section.

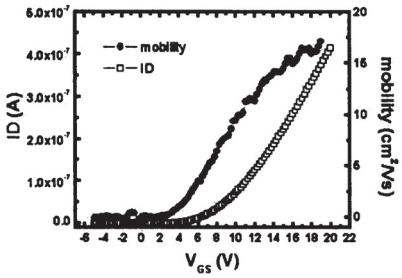

Fig. 3. I_D vs. V_{GS} characteristics measured from a 150 μm / 150 μm FATFET.

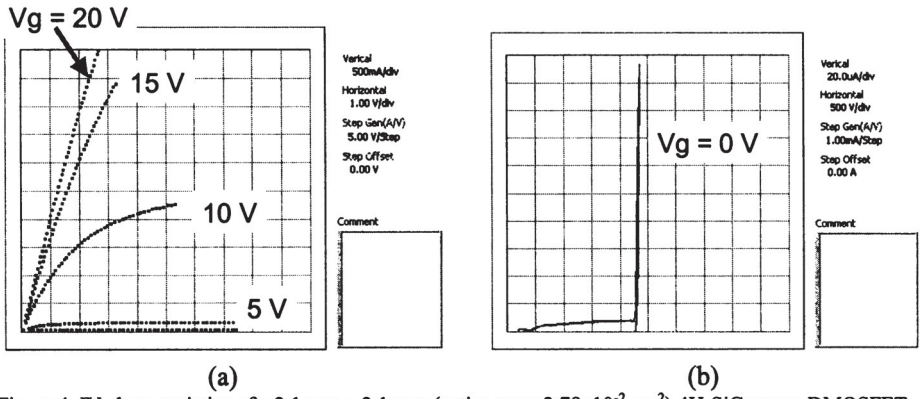

Figure 4. IV characteristics of a 2.1 mm x 2.1 mm (active area: 2.78×10^{-2} cm^2) 4H-SiC power DMOSFET. (a) on-state, and (b) off-state.

4 Summary

4H-SiC power DMOSFETs are suggested for high speed power switching applications. The drain charge and switching loss per unit area of a 4H-SiC device are approximately 10 times higher than those of a comparable silicon device. However, the total drain charge and switching loss for the 4H-SiC device are expected to be much smaller due to the very small chip size, which, in theory, can be a factor or 700 smaller than that of the silicon device. A 2.3 kV, 13.5 mΩ-cm2 4H-SiC power DMOSFET is demonstrated. The internal capacitances of the 4H-SiC DMOSFETs were compared to those of commercial silicon power MOSFETs, a 9X improvement in all capacitance values were achieved when compared to a 1200 V conventionalsilicon MOSFET, and an 8X improvement in output capacitance value was observed when compared to a 800 V charge compensated silicon MOSFET. This suggests that 4H-SiC power DMOSFETs will result in at least an order of magnitude improvement over silicon devices in switching characteristics.

Table 1. Comparison of internal capacitances of Power MOSFETs in Si and SiC.

	APT Power MOS 7 [4] (APT1201R4BLL)	Infineon CoolMOS [5] (SPP11N80C3)	Cree SiC DMOSFET
Vdss	1200V	800V	2300V
Ron	1.4 Ω	0.45 Ω	0.48 Ω (Vg = 20V)
Input capacitance	2030 pF*	1600 pF*	377.64 pF*
Output Capacitance	309 pF*	800 pF*	100.2 pF*
Reverse Transfer capacitance	60 pF*	40 pF*	18.52 pF*

*measured at VGS = 0 V, VDS = 25 V, 1 MHz

Acknowledgement

This work is supported in part by AFRL TIA # FA8650-04-2-2410, monitored by Dr. J. Scofield.

References

1. S. Ryu et al.,: MRS Proc. Vol. 764 (2003), p.C2.7.1
2. K. Adachi et al.,: Mat. Sci. Forum Vols. 457 – 460 (2004), p. 1233.
3. Q. Huang.: IEEE EDL, Vol. 25, No. 5 (2004), p. 298.
4. http://www.advancedpower.com/
5. http://www.infineon.com/cmc_upload/documents/085/068/SPP_A11N80C3.pdf