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PATENT APPLICATION
TRANSMITTAL**

(Only for new nonprovisional applications under 37 CFR 1.53(b))

Attorney Docket No.

3220-79132

First Inventor

James A. Cooper

Title

HIGH-VOLTAGE POWER SEMICONDUCTOR
DEVICE

Express Mail Label No.

EV446882016US

APPLICATION ELEMENTS

See MPEP chapter 600 concerning utility patent application contents.

1. ☒ **Fee Transmittal Form** (e.g., PTO/SB/17)
(Submit an original and a duplicate for fee processing)
2. ☐ **Applicant claims small entity status.**
See 37 CFR 1.27.
3. ☒ **Specification** [Total Pages 22]
Both the claims and abstract must start on a new page
(For information on the preferred arrangement, see MPEP
608.01(a))
4. ☒ **Drawing(s)** (35 U.S.C. 113) [Total Sheets 4]
5. Oath or Declaration (unsigned) [Total Sheets 3]
a. ☐ Newly executed (original or copy)
b. ☐ Copy from a prior application (37 CFR 1.63(d))
(for continuation/divisional with Box 18 completed)
i. ☐ **DELETION OF INVENTOR(S)**
Signed statement attached deleting inventor(s)
name in the prior application, see 37 CFR
1.63(d)(2) and 1.33(b).
6. ☐ **Application Data Sheet.** See 37 CFR 1.76
7. ☐ **CD-ROM or CD-R** in duplicate, large table or Computer
Program (Appendix)
☐ Landscape Table on CD
8. **Nucleotide and/or Amino Acid Sequence Submission**
(if applicable, items a. - c. are required)
a. **Computer Readable Form (CRF)**
i. ☐ Computer Readable Form (CRF)
ii. ☐ Transfer Request (37 CFR 1.821(e))
b. **Specification Sequence Listing on:**
i. ☐ CD-ROM or CD-R (2 copies); or
ii. ☐ Paper
c. ☐ Statements verifying identity of above copies

ADDRESS TO:

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9. ☐ **Assignment Papers** (cover sheet & document(s))
Name of Assignee _____
10. ☐ **37 CFR 3.73(b) Statement** ☐ **Power of Attorney**
(when there is an assignee)
11. ☐ **English Translation Document** (if applicable)
12. ☐ **Information Disclosure Statement** (PTO/SB/08 or PTO-1449)
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publications, & other information
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(b)(2)(B)(i). Applicant must attach form PTO/SB/35
or equivalent.
17. ☒ **Other:** Application Title Page (1 Page)

18. If a CONTINUING APPLICATION, check appropriate box, and supply the requisite information below and in the first sentence of the specification following the title, or in an Application Data Sheet under 37 CFR 1.76:

☐ Continuation ☐ Divisional ☐ Continuation-in-part (CIP) of prior application No.: _____

Prior application information:

Examiner _____

Art Unit: _____

19. CORRESPONDENCE ADDRESS

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Name
(Print/Type)

Bradford C. Addison

Date

January 23, 2006

Registration No.
(Attorney/Agent)

41486

This collection of information is required by 37 CFR 1.53(b). The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.11 and 1.14. This collection is estimated to take 12 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.

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STMicroelectronics v. Purdue, IPR2022-00252
Page 1

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Effective on 12/08/2004.
 Fees pursuant to the Consolidated Appropriations Act, 2005 (H.R. 4818).

FEE TRANSMITTAL for FY 2005

☐ Applicant claims small entity status. See 37 CFR 1.27

TOTAL AMOUNT OF PAYMENT (\$) \$1,350.00

Complete if Known

Application Number	Unknown
Filing Date	Herewith
First Named Inventor	James A. Cooper et al.
Examiner Name	Unknown
Art Unit	Unknown
Attorney Docket No.	3220-79132

METHOD OF PAYMENT (check all that apply)

☐ Check ☐ Credit Card ☐ Money Order ☐ None ☐ Other (please identify): _____

☒ Deposit Account Deposit Account Number: 10-0435 Deposit Account Name: Barnes & Thornburg LLP

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FEE CALCULATION

1. BASIC FILING, SEARCH, AND EXAMINATION FEES

Application Type	FILING FEES		SEARCH FEES		EXAMINATION FEES		Fees Paid(\$)
	Fee (\$)	Small Entity Fee (\$)	Fee (\$)	Small Entity Fee (\$)	Fee (\$)	Small Entity Fee (\$)	
Utility	300	150	500	250	200	100	\$1,000.00
Design	200	100	100	50	130	65	
Plant	200	100	300	150	160	80	
Reissue	300	150	500	250	600	300	
Provisional	200	100	0	0	0	0	

2. EXCESS CLAIM FEES

Fee Description	Fee (\$)	Small Entity Fee (\$)
Each claim over 20 (including Reissues)	50	25
Each independent claim over 3 (including Reissues)	200	100
Multiple dependent claims	360	180

Total Claims 23 - 20 or HP = 3 x \$50.00 = \$150.00

HP = highest number of total claims paid for, if greater than 20.

Indep. Claims 4 - 3 or HP = 1 x \$200.00 = \$200.00

HP = highest number of independent claims paid for, if greater than 3.

3. APPLICATION SIZE FEE

If the specification and drawings exceed 100 sheets of paper (excluding electronically filed sequence or computer listing under 37 CFR 1.52(e)), the application size fee due is \$250 (\$125 for small entity) for each additional 50 sheets or fraction thereof. See 35 U.S.C. 41(a)(1)(G) and 37 CFR 1.16(s).


Total Sheets 27 - 100 = 0 / 50 0 (round up to a whole number) x \$250.00 = \$0.00

4. OTHER FEE(S)

Non-English specification, \$130 fee (no small entity discount)

Other (e.g., late filing surcharge): _____

SUBMITTED BY

Signature		Registration No. (Attorney/Agent)	41486	Telephone	317-231-7253
Name (Print/Type)	Bradford G. Addison			Date	January 23, 2006

This collection of information is required by 37 CFR 1.136. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 30 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.

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BARNES & THORNBURG LLP

11 South Meridian Street
Indianapolis, IN 46204
(317) 236-1313
(317) 231-7433 Fax

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<i>Confirmation No.:</i>	Unknown	}
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<i>Application No.:</i>	Unknown	}
		}
<i>Invention:</i>	HIGH-VOLTAGE POWER SEMICONDUCTOR DEVICE	}
		}
<i>Applicant:</i>	James A. Cooper et al.	}
		}
<i>Filed:</i>	Herewith	}
		}
<i>Attorney</i>		}
<i>Docket:</i>	3220-79132	}
		}
<i>Examiner:</i>	Unknown	}

CERTIFICATE UNDER 37 C.F.R. § 1.10

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I hereby certify that this correspondence is being deposited with the United States Postal Service as Express Mail, in an envelope addressed to the Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450, on January 23, 2006. The Express Mail mailing label number is EV446882016US.

Respectfully submitted,
BARNES & THORNBURG LLP



Glen M. Kellett

BGA/GMK/kim
Indianapolis, IN
(317) 231-7253

UTILITY PATENT APPLICATION

of

James A. Cooper

and

Asmita Saha

for

HIGH-VOLTAGE POWER SEMICONDUCTOR DEVICE

Attorney Docket 3220-79132

Purdue 64281.00.US

HIGH-VOLTAGE POWER SEMICONDUCTOR DEVICE

[0001] This patent application claims priority to and the benefit of U.S. Provisional Patent Application Serial No. 60/646,152 entitled “Optimized Vertical Power DMOSFETs in Silicon Carbide” which was filed on January 21, 2005, the disclosure of which is expressly incorporated herein by reference

TECHNICAL FIELD

[0002] The present disclosure relates generally to semiconductor devices, and more particularly to semiconductor devices for high-voltage power applications.

BACKGROUND

[0003] One design consideration in the fabrication of semiconductor devices, such as metal-oxide semiconductor field-effect transistors (MOSFETs), for high-voltage power applications is the blocking voltage of the semiconductor device. The blocking voltage is defined as the drain-to-source voltage of the semiconductor device at which avalanche breakdown occurs and/or the strength of the magnetic field of the gate oxide at which the gate oxide fails. As such, for high-voltage power applications, a high blocking voltage is generally desirable. Another design consideration in such applications is the specific on-resistance of the semiconductor device (i.e., the product of the resistance of the device between the source and drain when the device is in an on-state and the area of the device, typically measured in $\text{m}\Omega\text{-cm}^2$). As the specific on-resistance of the device decreases, the efficiency of the semiconductor device may be improved. However, the typical fabrication techniques for reducing the specific on-resistance of high-voltage power semiconductor devices may also reduce the blocking voltage of the device.

SUMMARY

[0004] A metal-oxide semiconductor field-effect transistor (MOSFET) may include a semiconductor substrate. The semiconductor substrate may have a first concentration of first type impurities such as, for example, N-type impurities. The semiconductor substrate may be formed from a silicon carbide material. The MOSFET may include a drift semiconductor layer formed on a front side of the semiconductor substrate. The drift semiconductor layer may be so formed by epitaxially growing the drift semiconductor layer on the front side of the semiconductor substrate. The drift semiconductor layer may have a second concentration of first type impurities less than the first concentration of first type impurities. For example, the drift semiconductor layer may have a concentration of first type impurities of about $1 \times 10^{16} \text{ cm}^{-3}$ or less. The MOSFET may also include a first source region, a second source region, and a junction field-effect transistor (JFET) region defined therebetween. The JFET region may be defined, for example, under a gate electrode of the MOSFET. The JFET region may have a third concentration of first type impurities that is greater than the second concentration of first type impurities. For example, the third concentration of first type impurities may be at least one order of magnitude greater than the second concentration of first type impurities. In one particular embodiment, the JFET region may have a concentration of first type impurities of about $1 \times 10^{17} \text{ cm}^{-3}$ or greater. The JFET region may have a width less than about three micrometers. For example, the JFET may have a width of about one micrometer.

[0005] The MOSFET may also include a current spreading semiconductor layer formed on a front side of the drift semiconductor layer and, in some embodiments, under other base layers. The current spreading semiconductor layer may be so formed by, for

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example, epitaxially growing the current spreading semiconductor layer formed on a front side of the drift semiconductor layer. The current spreading semiconductor layer may have a fourth concentration of first type impurities greater than the second concentration of first type. For example, the fourth concentration of first type impurities may be at least one order of magnitude greater than the second concentration of first type impurities. In one particular embodiment, the current spreading semiconductor layer may have a concentration of first type impurities of about $1 \times 10^{17} \text{ cm}^{-3}$ or greater.

[0006] The MOSFET may further comprise a plurality of base contact regions formed in each of the first and the second source regions. The base contact regions being smaller than the first and second source regions. Alternatively, the MOSFET may further include a plurality of source regions and a plurality of base contact regions. The plurality of source regions and the plurality of base contact regions may form alternating strips of N-type doped regions and P-type doped regions. The alternating strips being substantially orthogonal to respective source electrodes formed over the first and the second source regions. The MOSFET may be a double-implanted MOSFET (DMOSFET). For example, the MOSFET may be a vertical DMOSFET.

[0007] A double-implanted metal-oxide semiconductor field-effect transistor (DMOSFET) may include a semiconductor substrate. The semiconductor substrate may be formed from silicon-carbide. The DMOSFET may include a drift semiconductor layer formed on a front side of the semiconductor substrate. The drift semiconductor layer may be so formed by epitaxially growing the drift semiconductor on the front side of the semiconductor substrate. The drift semiconductor layer may have a concentration of first type impurities less than a concentration of first type impurities of the semiconductor substrate. The DMOSFET may also include a first source region, a second source region, and a JFET region defined therebetween. The JFET region may

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have a concentration of first type impurities that is greater than the concentration of first type impurities of the drift semiconductor layer. For example, the concentration of first type impurities of the JFET region may be at least one order of magnitude greater than the concentration of first type impurities of the drift semiconductor layer. The JFET region may also have a width less than about three micrometers. For example, the JFET may have a width of about one micrometer. Each of the first and the second source regions may include an N-type doped region having a plurality of smaller P-type regions formed therein. The plurality of smaller P-type regions may be formed, for example, under a source electrode. Alternatively, each of the first and the second source regions may include alternating strips of N-type doped regions and P-type doped regions. The alternating strips of doped regions may be substantially orthogonal with respect to the JFET region and/or to a source electrode(s) formed above the source regions.

[0008] Additionally, the DMOSFET may include a current spreading semiconductor layer. The current spreading semiconductor layer may be formed on a front side of the drift semiconductor layer and the JFET region may be formed on a front side of the current spreading semiconductor layer. The current spreading semiconductor layer may be so formed by epitaxially growing the current spreading semiconductor layer. The current spreading semiconductor layer may include a concentration of first type impurities that is greater than the concentration of first type impurities of the drift semiconductor layer. For example, the current spreading semiconductor layer may be a concentration of first type impurities that is at least one order of magnitude greater than the concentration of first type impurities of the drift semiconductor layer.

[0009] A vertical double-implanted metal-oxide semiconductor field-effect transistor (vertical DMOSFET) may include a silicon-carbide substrate. The silicon-carbide substrate may have a first concentration of first type impurities such as, for

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example, N-type impurities. The vertical DMOSFET may also include a drift semiconductor layer epitaxially formed on a front side of the silicon-carbide substrate. The drift semiconductor layer may have a second concentration of first type impurities less than the first concentration of first type impurities of the silicon-carbide substrate. The vertical DMOSFET may further include a current spreading semiconductor layer epitaxially formed on a front side of the drift layer. The current spreading layer may have a third concentration of first type impurities greater than the second concentration of first type impurities of the drift semiconductor layer. The vertical DMOSFET may also include a first source region, a second source region, and a junction field-effect transistor (JFET) region defined therebetween. The JFET may be formed on a front side of the current spreading semiconductor layer. The JFET region may have a width of about one micrometer. The JFET region may also have a fourth concentration of first type impurities greater than the second concentration of first type impurities of the drift semiconductor layer. The DMOSFET may further comprise a plurality of base contact regions formed in each of the first and the second source regions. The base contact regions being smaller than the first and second source regions. Alternatively, the DMOSFET may further include a plurality of source regions and a plurality of base contact regions. The plurality of source regions and the plurality of base contact regions may form alternating strips of N-type doped regions and P-type doped regions. The alternating strips being substantially orthogonal to respective source electrodes formed over the first and the second source regions.

[0010] The above and other features of the present disclosure, which alone or in any combination may comprise patentable subject matter, will become apparent from the following description and the attached drawings.

BRIEF DESCRIPTION OF THE DRAWINGS

[0011] The detailed description particularly refers to the following figures, in which:

[0012] FIG. 1 is a diagrammatic cross-sectional view of one embodiment of a semiconductor device;

[0013] FIG. 2 is a plan view of a portion of the semiconductor device of FIG. 1;

[0014] FIG. 3 is a plan view of another embodiment of the semiconductor device of FIG. 1; and

[0015] FIG. 4 is a plan view of yet another embodiment of the semiconductor device of FIG. 1.

DETAILED DESCRIPTION OF THE DRAWINGS

[0016] While the concepts of the present disclosure are susceptible to various modifications and alternative forms, specific exemplary embodiments thereof have been shown by way of example in the drawings and will herein be described in detail. It should be understood, however, that there is no intent to limit the concepts of the present disclosure to the particular forms disclosed, but on the contrary, the intention is to cover all modifications, equivalents, and alternatives falling within the spirit and scope of the invention as defined by the appended claims.

[0017] Referring to FIG. 1, a high-voltage power semiconductor device 10 includes a substrate 12 and a number of semiconductor layers successively formed on the substrate 12. Illustratively, the semiconductor device 10 is a vertical double-implanted metal-oxide semiconductor field-effect transistor (DMOSFET). However, in other embodiments, the semiconductor device 10 may be embodied as other types of MOSFET devices. The substrate 12 is illustratively formed from silicon-carbide and

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doped with an N-type impurity to an “N+” concentration. In some embodiments, the dopant impurities are incorporated into the substrate 12 during the manufacturing of the silicon-carbide wafer from which the substrate 12 is formed. However, in other embodiments, the substrate 12 may be doped with the N-type impurities at a later step in the fabrication process using any suitable doping technique such as, for example, ion implantation or diffusion.

[0018] The semiconductor device 10 includes a drift semiconductor layer 14 formed on a front side 16 of the substrate 12. It should be appreciated, however, that one or more “buffer layers” may also be formed between the drift layer 14 and the substrate 12. As such, as used herein the term “formed on a front side of the substrate/layer” is intended to mean formed on a top surface of the substrate/layer and/or formed on the front side of the substrate/layer with respect to the top surface of the substrate/layer with a number of intervening “buffer” layers. Similarly, as used herein, the term “formed on a back side of the substrate/layer” is intended to mean formed on a bottom surface of the substrate/layer and/or formed on the back side of the substrate/layer with respect to the bottom surface with a number of intervening “buffer layers”.

[0019] In the illustrative embodiment, the drift layer 14 is formed on the front side 16 by epitaxially growing the drift layer 14 on the surface 16. The drift layer 14 may be epitaxially grown on the surface 16 by, for example, a chemical vapor deposition process. The drift layer 14 is also illustratively formed from silicon-carbide and doped with N-type impurities to an “N-” concentration. Illustratively, the drift layer 14 is so doped during the formation of the drift layer 14. The blocking voltage of the semiconductor device 10 is determined, in part, on the thickness 18 and the doping concentration of the drift layer 14. To achieve a desired blocking voltage, these two variables may be modified. For example, the thickness 18 of the drift layer 14 may be

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increased and/or the doping concentration of the drift layer 14 may be decreased to thereby increase the blocking voltage of the semiconductor device 10. However, when the thickness 18 and/or the doping concentration of the drift layer 14 are decreased, the specific on-resistance of the semiconductor device 10 may be increased as a result thereof. Accordingly, the design process of the semiconductor device 10 may include reiterative design steps of the drift layer 14 and other layers or regions of the device 10 to achieve the desired block voltage while maintaining (or reducing) the specific on-resistance of the semiconductor device 10 as discussed in more detail below.

[0020] In one particular embodiment, the semiconductor device 10 has a blocking voltage of about 1000 volts. In such embodiments, the drift layer 14 has a thickness 18 of about 6 micrometers and an N-type doping concentration of about $1 \times 10^{16} \text{ cm}^{-3}$. However, in other embodiments, drift layers 14 having alternative thicknesses and doping concentrations may be used depending upon the application and design parameters, such as the desired blocking voltage, of the semiconductor device 10.

[0021] The semiconductor device 10 also includes a current spreading semiconductor layer 20 formed on a front side 22 of the drift layer 14. In the illustrative embodiment, the current spreading layer 20 is formed on the front side 22 by epitaxially growing (e.g., via chemical vapor deposition) the current spreading layer 20 on the front side 22 to a thickness 24. The current spreading layer 20 is illustratively formed from silicon-carbide and is doped with N-type impurities to an "N" concentration. The current spreading layer 20 may be so doped during the formation of the layer 20 or subsequently thereafter using any suitable doping technique such as, for example, an ion implantation or diffusion process. The current spreading layer 20 is doped to an N-type impurity concentration that is greater than the concentration of the N-type impurities of the drift layer 14. For example, the current spreading layer 20 may be doped to an N-type

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impurity concentration that is one order of magnitude or greater than the doping concentration of the drift layer 14. In one particular embodiment, the drift layer 14 has a doping concentration of about $1 \times 10^{16} \text{ cm}^{-3}$ and the current spreading layer 20 has a doping concentration of about $1 \times 10^{17} \text{ cm}^{-3}$ and a thickness 24 of about 0.4 micrometers.

[0022] The semiconductor device 10 also includes two doped semiconductor wells or base regions 26, 28 formed above the current spreading layer 20 and a junction field-effect transistor (JFET) region 30 formed between the wells 26, 28. It should be appreciated that the semiconductor 10 illustrated in FIG. 1 may be a single “transistor cell” and that a completely fabricated transistor device may include any number of semiconductor devices 10. As such, the following description is in regard to but one semiconductor device 10 with the understanding that the description is application to all semiconductor devices 10 that form a fabricated transistor device. For example, the fabricated transistor device may include any number of doped semiconductor wells 26, 28 depending on the number of semiconductor devices 10 included therein. Additionally, it should be appreciated that in some embodiments, the number of semiconductor devices 10 so included in the fabricated transistor device may be arranged in a hexagonal cellular array rather than in an interdigitated finger array.

[0023] In the illustrative embodiment, the wells 26, 28 are doped with a P-type impurity to a “P” concentration whereas the JFET region 30 is doped with N-type impurities to an “N” concentration. As such, the JFET region 30 is doped to an N-type impurity concentration that is greater than the concentration of N-type impurities of the drift layer 14. For example, the JFET region 30 may be doped to an N-type impurity concentration that is one order of magnitude or greater than the doping concentration of the drift layer 14. In one particular embodiment, the drift layer 14 has a doping

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concentration of about $1 \times 10^{16} \text{ cm}^{-3}$ and the JFET region 30 has a doping concentration of about $1 \times 10^{17} \text{ cm}^{-3}$.

[0024] It should be appreciated that in some embodiments, the JFET region 30 and the current spreading layer 20 have similar doping concentrations. In such embodiments, the wells 26, 28 and the JFET region 30 may be formed by growing an extra-thick current spreading layer 20 and forming the “P” wells 26, 28 using a suitable incorporation process such as an ion implantation process. The doping of the current spreading layer 20 and the JFET region 30 may be performed during the growth process or may be performed subsequently thereafter using, for example, an ion implantation or diffusion process.

[0025] Alternatively, in other embodiments, after the current spreading layer 20 is formed on the front side 22 of the drift layer 12, an additional epitaxial layer may be formed on a front side 34 of the current spreading layer 20. In such embodiments, the wells 26, 28 may be formed by, for example, implanting the wells 26, 28 in the additional epitaxial layer using an ion implantation process. The remaining region of the additional epitaxial layer between the wells 26, 28 forms the JFET region 30. The JFET region 30 may be doped, either during fabrication of the additional epitaxial layer or subsequently thereafter, to a doping concentration similar to the doping concentration of the current spreading layer 20. Alternatively, in some embodiments, the JFET region 30 may be doped to a concentration of impurities that is different than the doping concentration of the current spreading layer 20, but still greater than the doping concentration of the drift layer 14. Such a doping concentration of the JFET region 30 may be achieved by doping the additional epitaxial layer to the desired concentration.

[0026] By forming a JFET region 30 with a doping concentration that is greater than the doping concentration of the drift layer 14, the specific on-resistance of the

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semiconductor device 10 may be reduced compared to a MOSFET device having JFET regions and drift layers of substantially equal impurity concentrations. In some embodiments, the JFET region 30 is also fabricated to have a short width 36 relative to a typical DMOSFET device, which may reduce the specific on-resistance of the semiconductor device 10. For example, in some embodiments, the JFET region 30 has a width 36 that is about three micrometers or less. In one particular embodiment, the JFET region 30 has a width 36 of about one micrometer.

[0027] Additionally, by forming the current spreading layer 20, the specific on-resistance of the semiconductor device 10 may also be reduced compared to a MOSFET device without a current spreading layer. Because the doping concentration of the current spreading layer 20 is greater than the doping concentration of the underlying drift layer 14, current tends to flow downwardly from the JFET region 30 and laterally through the current spreading layer 20 before subsequently flowing down through the upper portion of the lower doped drift layer 14. Because the current tends to flow laterally through the current spreading layer 20, the current density of the semiconductor device 10 through the lower doped drift layer 14 may be reduced thereby reducing the specific on-resistance of the semiconductor device 10.

[0028] It should be appreciated, however, that the increased doping concentration of the JFET region 30 and the current spreading layer 20 may tend to reduce the blocking voltage of the semiconductor device 10. Conversely, the shorter width 36 of the JFET region 30 compared to typical semiconductor device may tend to increase the blocking voltage of the semiconductor device 10 because such a configuration may reduce the magnetic field in the gate oxide layer above the JFET region 30. As discussed above, the doping concentration and thickness 18 of the drift layer 14 may be modified to achieve the desired blocking voltage of the semiconductor device 10. In this way, the design of

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the semiconductor device 10 involves a number of parameters that may affect or be interdependent upon each other. As such, the design process of the semiconductor device 10 may include a number of reiterative steps of selecting a width 36 and a doping concentration for the JFET region 30, selecting a doping concentration and a thickness for the current spreading layer 20, selecting a doping concentration and a thickness 18 for the drift layer 14, and/or selecting values for other parameters to achieve the desired characteristics of the semiconductor device 10.

[0029] As illustrated in FIG. 1, the semiconductor device 10 also includes source regions 46, 48 defined in the “P” wells 26, 28, respectively. The source regions 46, 48 are doped with N-type impurities to a “N+” concentration. The semiconductor 10 also includes base electrode regions 42, 44. The base electrode regions 42, 44 are doped with P-type impurities to a “P+” concentration. The regions 42, 44, 46, 48 may be doped using any suitable doping technique such as, for example, an ion implantation process or the like. A source metallic electrode 50, 52 is formed over the source regions 46, 48, respectively. In some embodiments, the source electrodes 50, 52 are coupled together to form a unitary source electrode. Additionally, in some embodiments, the source electrodes are formed from two or more metallic materials such that one metallic material is coupled with the source regions 46, 48 and a second metallic material is coupled with the base contact regions 42, 44.

[0030] The semiconductor device 10 also includes a gate metallic electrode 54 formed on a dielectric layer 56, such as an oxide, over the JFET region 30. The gate electrode 54 and dielectric layer 56 also extend over portions of the source regions 46, 48. The semiconductor device 10 further includes a drain metallic electrode 58 coupled to a bottom surface 60 of the substrate 12. The semiconductor device 10 may be

-13-

electrically coupled with other electrical devices, sources, or the like via the electrodes 50, 52, 54, 58.

[0031] At some point during the design process, the specific on-resistance contribution of a JFET region of a MOSFET device is reduced to a point whereat the source resistance of the device becomes one of the dominating contributions to the specific on-resistance of the device. The source resistance of a device is the resistance between the source electrodes and the inner portions of the source regions. As illustrated in FIG. 2, in one embodiment, the source regions 46, 48 of the semiconductor device 10 and the base contact regions 42, 44 are formed in the “P-” wells 26, 28 such that portions of the source regions 46, 48 and the base contact regions 42, 44 lie under the source electrodes 50, 52, respectively. Note that the outer edges of the source electrodes 50, 52 have been removed in FIG. 2 for clarity. As illustrated, the source regions 46, 48 and the base contact regions 42, 44 extend longitudinally with and substantially parallel to the source electrodes 50, 52 and the JFET region 30.

[0032] Because of semiconductor manufacturing process variations, such a topological configuration as illustrated in FIG. 2 can result in an undesirable source resistance if the source regions 46, 48 are misaligned with respect to the base contact regions 42, 44 and/or the source regions 46, 48 are misaligned with respect to the source electrodes 50, 52. For example, with respect to the source region 46, if the source electrode 50 is inadvertently formed more toward the direction of arrow 128 and/or the source region 46 is inadvertently formed more toward the direction of arrow 130, the source electrode 50 may not adequately cover the source region 46 and thereby cause the source resistance of the semiconductor device 10 to be increased due to the misalignment.

[0033] Referring now to FIG. 3, to reduce the likelihood of misalignment between the source electrodes and the source regions, in some embodiments, the

-14-

semiconductor device 10 is fabricated to have source regions 154, 156 that each include a plurality of base contact regions 158, 160 formed in source regions 154, 156, respectively. As shown in FIG. 3, the base contact regions 158, 160 are embodied as small “islands” or regions within the larger source regions 154, 156. The base contact regions 158, 160 are formed to be located in a central location under the source metallic electrodes 50, 52 with areas of source regions 154, 156 spaced between each base contact regions 158, 160. Note that the outer edges of the source electrodes 50, 52 have been removed in FIG. 3 for clarity. Because the source regions 154, 156 form a greater portion of the area under the source electrodes 50, 52, the tolerance to manufacturing variability of the semiconductor device 10 may be increased. That is, even if the source electrodes 50, 52 are slightly misaligned with respect to the source regions 154, 156, the source resistance of the semiconductor device 10 is not substantially increased because a substantial portion of the source regions 154, 156 would remain aligned with the respective source electrode 50, 52.

[0034] Referring now to FIG. 4, in another embodiment, the semiconductor device 10 is fabricated to have source regions 188, 190 and base contact regions 184, 186 embodied as strips. The strips alternate between source regions 188, 190 and base contact regions 184, 186. The strips of source regions 188, 190 and base contact regions 184, 186 are orientated such that they are substantially orthogonal to the source electrodes 50, 52 and the JFET region 30. That is, a portion of each of the source regions 188, 190 and base contact regions 184, 186 is positioned under the respective source electrode 50, 52. Because the source regions 188, 190 and base contact regions 184, 186 are configured substantially orthogonal to the source electrodes 50, 52, if any one or more of the source electrodes 50, 52 are fabricated to be slightly misaligned (e.g., the source electrode 50, 52 is closer to or farther away from the gate electrode 54), a substantial

-15-

portion of each source regions 188, 190 and base contact regions 184, 186 would remain under the respective source electrode. As such, the source resistance of the semiconductor device 10 is not substantially increased when the source electrodes 50, 52 and/or the source regions 188, 190 are slightly misaligned during fabrication of the device 10.

[0035] It should be appreciated that the semiconductor 10 may be fabricated using any one of a number of fabrication techniques. For example, in one embodiment, the semiconductor 10 may be fabricated using any one of the semiconductor fabrication methods described in U.S. Utility Patent Application Serial No. XX/XXX,XXX entitled "Method for Fabricating a Semiconductor Device," which was filed on January XX, 2006 by James A. Cooper et al., the disclosure of which is expressly incorporated herein by reference.

[0036] While the disclosure has been illustrated and described in detail in the drawings and foregoing description, such an illustration and description is to be considered as exemplary and not restrictive in character, it being understood that only illustrative embodiments have been shown and described and that all changes and modifications that come within the spirit of the disclosure are desired to be protected.

[0037] There are a plurality of advantages of the present disclosure arising from the various features of the device described herein. It will be noted that alternative embodiments of the device of the present disclosure may not include all of the features described yet still benefit from at least some of the advantages of such features. Those of ordinary skill in the art may readily devise their own implementations of the device that incorporate one or more of the features of the present invention and fall within the spirit and scope of the present disclosure as defined by the appended claims.

CLAIMS

1. A metal-oxide semiconductor field-effect transistor comprising:
a semiconductor substrate having a first concentration of first type impurities;
a drift semiconductor layer formed on a front side of the semiconductor substrate and having a second concentration of first type impurities less than the first concentration of first type impurities;
a first source region;
a second source region; and
a JFET region defined between the first source region and the second source region, the JFET region having a third concentration of first type impurities that is greater than the second concentration of first type impurities.
2. The metal-oxide semiconductor field-effect transistor of claim 1, wherein the substrate is a silicon-carbide substrate.
3. The metal-oxide semiconductor field-effect transistor of claim 1, wherein the JFET region has a width of less than about three micrometers.
4. The metal-oxide semiconductor field-effect transistor of claim 3, wherein the JFET region has a width of about one micrometer.
5. The metal-oxide semiconductor field-effect transistor of claim 1, wherein the third concentration of first type impurities is at least one order of magnitude greater than the second concentration of first type impurities.

-17-

6. The metal-oxide semiconductor field-effect transistor of claim 1, further comprising a current spreading semiconductor layer formed on a front side of the drift semiconductor layer, wherein the JFET region is formed on a front side of the current spreading semiconductor layer.

7. The metal-oxide semiconductor field-effect transistor of claim 6, wherein the current spreading semiconductor layer has a fourth concentration of first type impurities that is greater than the second concentration of first type impurities.

8. The metal-oxide semiconductor field-effect transistor of claim 7, wherein the fourth concentration of first type impurities is at least one order of magnitude greater than the second concentration of first type impurities.

9. The metal-oxide semiconductor field-effect transistor of claim 6, wherein the JFET region has a width of about one micrometer.

10. The metal-oxide semiconductor field-effect transistor of claim 1, further comprising a plurality of base contact regions formed in each of the first and the second source regions, the base contact regions being smaller than the first and second source regions.

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11. The metal-oxide semiconductor field-effect transistor of claim 1, further comprising a plurality of source regions and a plurality of base contact regions, wherein the plurality of source regions and the plurality of base contact regions form alternating strips of N-type doped regions and P-type doped regions, the alternating strips being substantially orthogonal to respective source electrodes formed over the first and the second source regions.

12. A double-implanted metal-oxide semiconductor field-effect transistor comprising:

a semiconductor substrate;

a drift semiconductor layer formed on a front side of the semiconductor substrate;

a first source region;

a second source region; and

a JFET region defined between the first source region and the second source region, the JFET region having a width less than about three micrometers.

13. The double-implanted metal-oxide semiconductor field-effect transistor of claim 12, wherein the JFET region has a width of about one micrometer.

14. The double-implanted metal-oxide semiconductor field-effect transistor of claim 12, wherein the JFET region has a first concentration of first type impurities and the drift semiconductor layer has a second concentration of first type impurities, the first concentration of first type impurities being greater than the second concentration of first type impurities.

-19-

15. The double-implanted metal-oxide semiconductor field-effect transistor of claim 12, further comprising a plurality of base contact regions formed in each of the first and the second source regions, the base contact regions being smaller than the first and second source regions.

16. The double-implanted metal-oxide semiconductor field-effect transistor of claim 12, further comprising a plurality of source regions and a plurality of base contact regions, wherein the plurality of source regions and the plurality of base contact regions form alternating strips of N-type doped regions and P-type doped regions, the alternating strips being substantially orthogonal to respective source electrodes formed over the first and the second source regions.

17. A double-implanted metal-oxide semiconductor field-effect transistor comprising:

- a semiconductor substrate;

- a drift semiconductor layer formed on a front side of the semiconductor substrate;

- a current spreading semiconductor layer formed on a front side of the drift semiconductor layer;

- a first source region;

- a second source region; and

- a JFET region defined between the first source region and the second source region, the JFET region being formed on a front side of the current spreading semiconductor layer.

18. The double-implanted metal-oxide semiconductor field-effect transistor of claim 17, wherein the current spreading semiconductor layer has a first concentration of first type impurities and the drift semiconductor layer has a second concentration of first type impurities, the first concentration of first type impurities being greater than the second concentration of first type impurities.

19. The double-implanted metal-oxide semiconductor field-effect transistor of claim 18, wherein the first concentration of first type impurities is at least one order of magnitude greater than the second concentration of first type impurities.

20. The double-implanted metal-oxide semiconductor field-effect transistor of claim 17, wherein the JFET region has a width of about three micrometers or less.

21. The double-implanted metal-oxide semiconductor field-effect transistor of claim 17, further comprising a plurality of base contact regions formed in each of the first and the second source regions, the base contact regions being smaller than the first and second source regions.

22. The double-implanted metal-oxide semiconductor field-effect transistor of claim 17, further comprising a plurality of source regions and a plurality of base contact regions, wherein the plurality of source regions and the plurality of base contact regions form alternating strips of N-type doped regions and P-type doped regions, the alternating strips being substantially orthogonal to respective source electrodes formed over the first and the second source regions.

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23. A vertical double-implanted metal-oxide semiconductor field-effect transistor comprising:

a silicon-carbide substrate having a first concentration of first type impurities;

a drift semiconductor layer epitaxially formed on a front side of the silicon-carbide substrate and having a second concentration of first type impurities less than the first concentration of first type impurities;

a current spreading semiconductor layer epitaxially formed on a front side of the drift layer, the current spreading semiconductor layer having a third concentration of first type impurities greater than the second concentration of first type impurities;

a first source region;

a second source region; and

a JFET region defined between the first source region and the second source region and formed on a front side of the current spreading semiconductor layer, the JFET region having a width less than about three micrometers and a fourth concentration of first type impurities greater than the second concentration of first type impurities.

ABSTRACT OF THE DISCLOSURE

A semiconductor device, such as a metal-oxide semiconductor field-effect transistor, includes a semiconductor substrate, a drift layer formed on the substrate, a first and a second source region, and a JFET region defined between the first and the second source regions. The JFET region may have a short width and/or a higher concentration of impurities than the drift layer. The semiconductor device may also include a current spreading layer formed on the drift layer. The current spreading layer may also have a higher concentration of impurities than the drift layer.

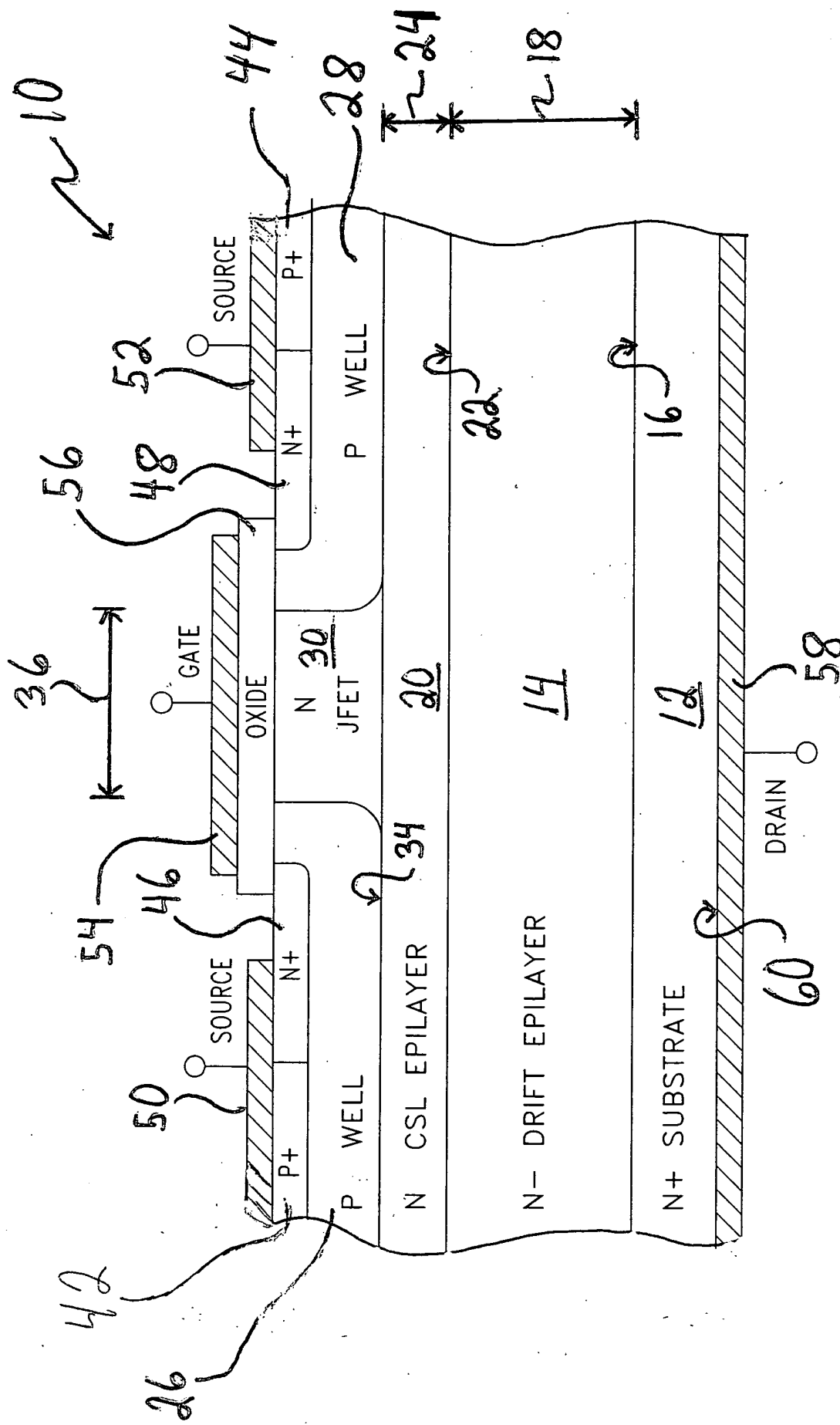


Fig. 1

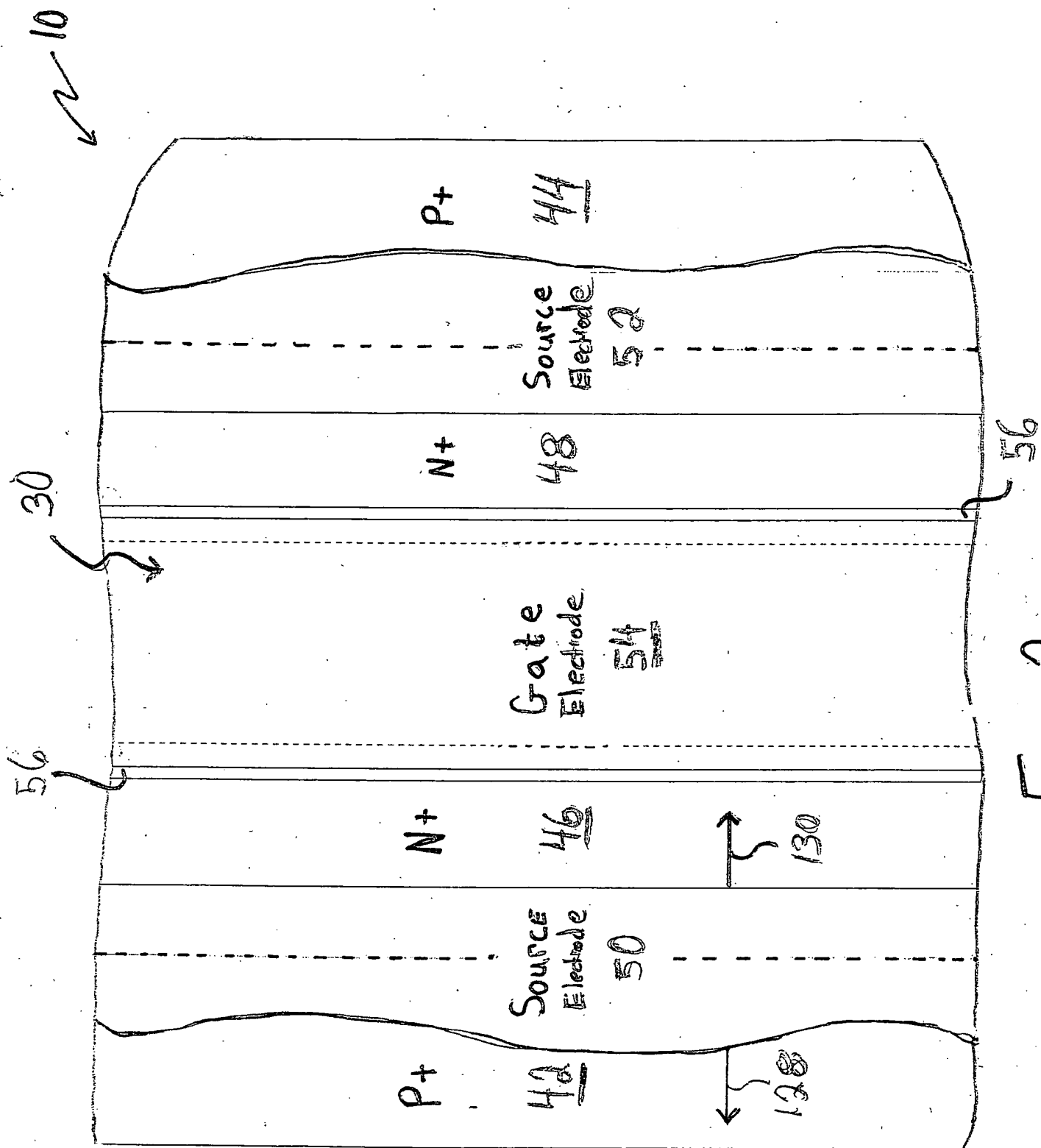
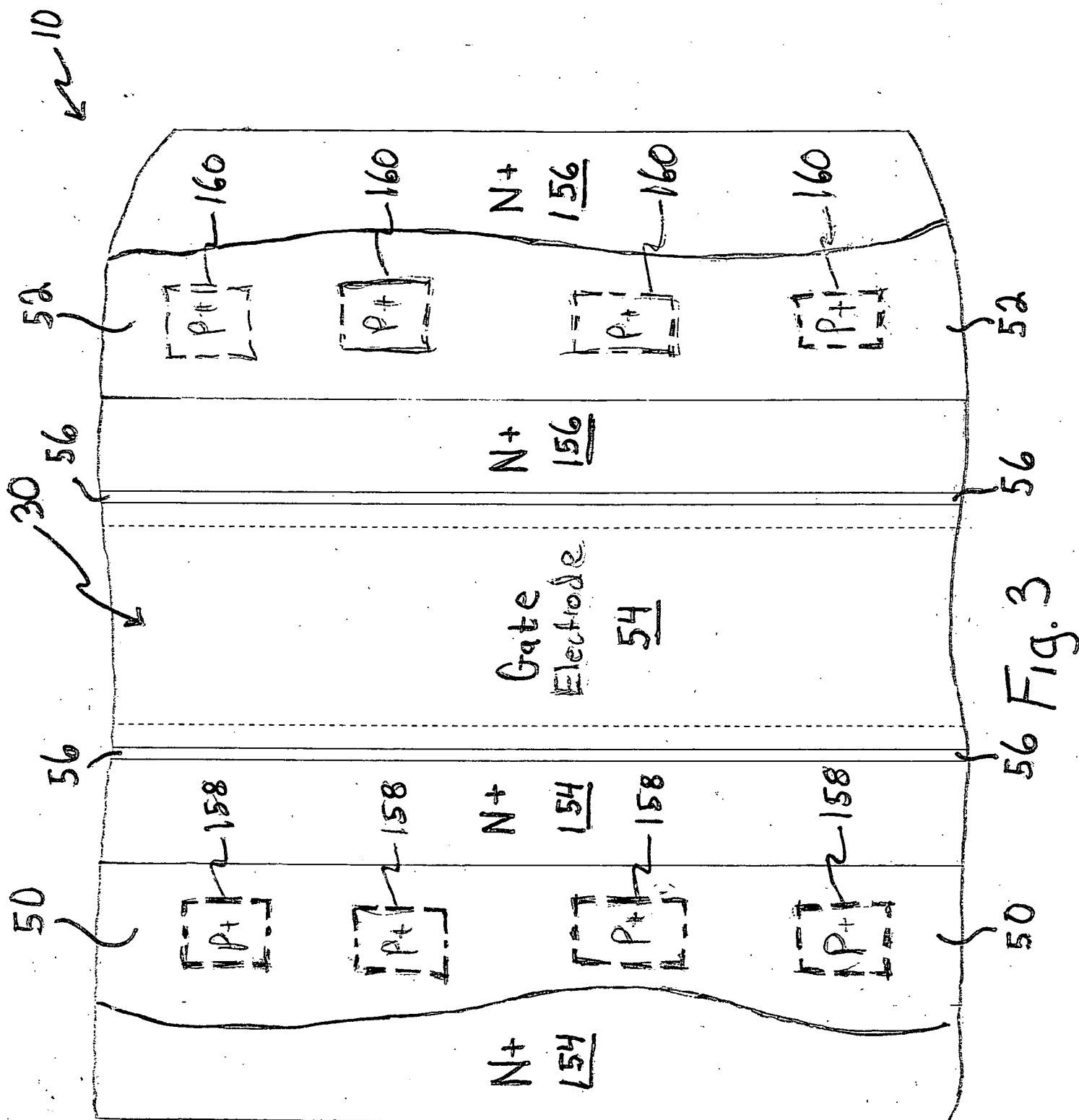
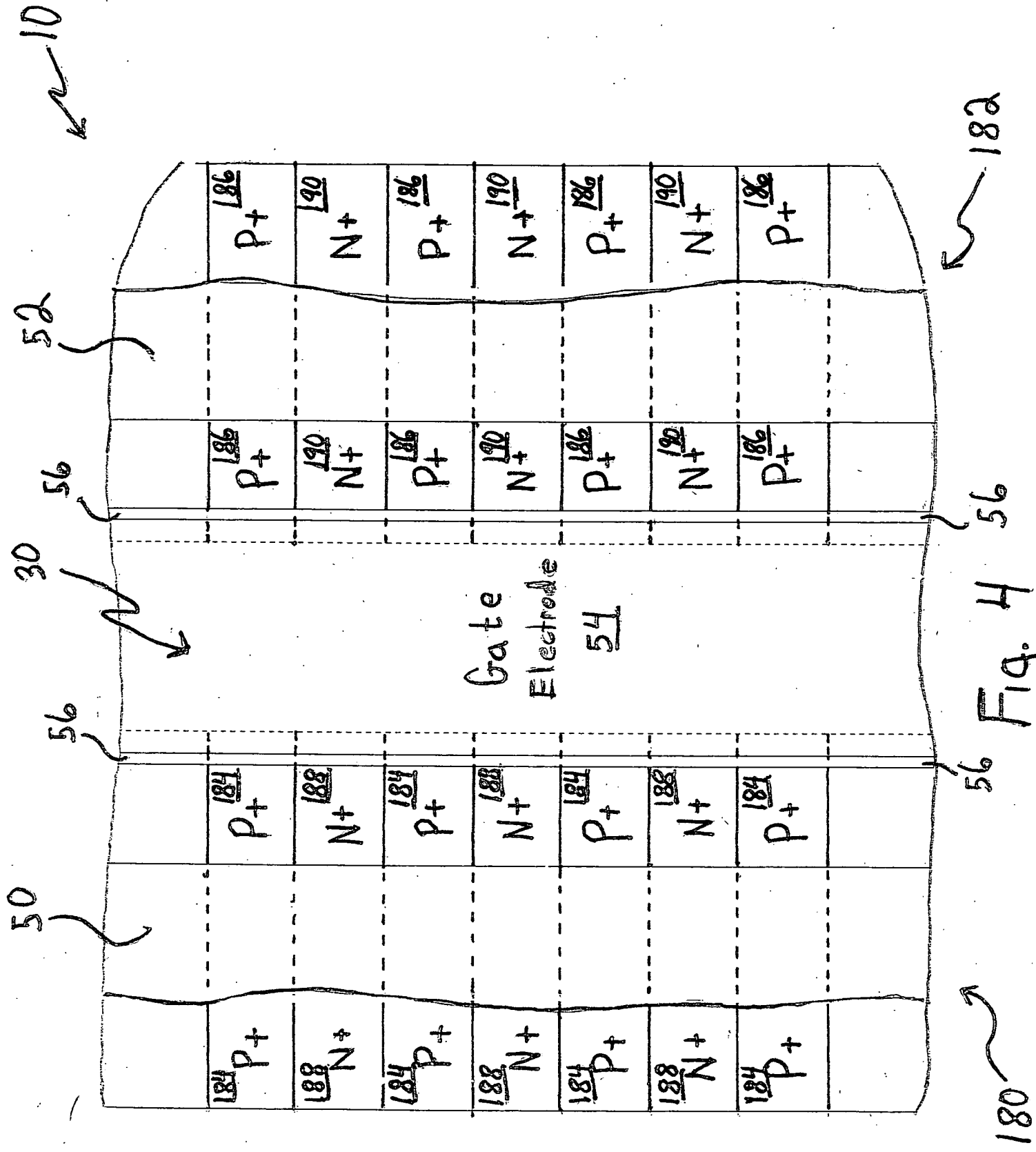


Fig. 2





Docket No.
3220-79132

Declaration For Patent Application

English Language Declaration

As a below named inventor, I hereby declare that:

My residence, post office address and citizenship are as stated below next to my name,

I believe I am the original, first and sole inventor (if only one name is listed below) or an original, first and joint inventor (if plural names are listed below) of the subject matter which is claimed and for which a patent is sought on the invention entitled

HIGH-VOLTAGE POWER SEMICONDUCTOR DEVICE

the specification of which

(check one)

☒ is attached hereto.

☐ was filed on _____ as United States Application No. or PCT International Application Number _____ and was amended on _____

(if applicable)

I hereby state that I have reviewed and understand the contents of the above identified specification, including the claims, as amended by any amendment referred to above.

I acknowledge the duty to disclose information which is material to patentability as defined in 37 CFR 1.56, including for continuation-in-part applications, material information which became available between the filing date of the prior applications and the national or PCT international filing date of the continuation-in-part application.

I hereby claim foreign priority benefits under 35 U.S.C. 119(a)-(d) or (f), or 365(b) of any foreign application(s) for patent, inventor's or plant breeder's rights certificate(s), or 365(a) of any PCT International application which designated at least one country other than the United States of America, listed below and have also identified below, by checking the box, any foreign application for patent or inventor's or plant breeder's rights certificate(s), or any PCT international application having a filing date before that of the application on which priority is claimed.

Prior Foreign Application(s)

Priority Claimed

(Number) (Country) (Day/Month/Year Filed)

☒

(Number) (Country) (Day/Month/Year Filed)

☒

(Number) (Country) (Day/Month/Year Filed)

☒

I hereby claim the benefit under 35 U.S.C. Section 119(e) of any United States provisional application(s) listed below:

60/646,152

(Application Serial No.)

1/21/05

(Filing Date)

(Application Serial No.)

(Filing Date)

(Application Serial No.)

(Filing Date)

I hereby claim the benefit under 35 U. S. C. Section 120 of any United States application(s), or Section 365(c) of any PCT International application designating the United States, listed below and, insofar as the subject matter of each of the claims of this application is not disclosed in the prior United States or PCT International application in the manner provided by the first paragraph of 35 U.S.C. Section 112, I acknowledge the duty to disclose to the United States Patent and Trademark Office all information known to me to be material to patentability as defined in Title 37, CFR Section 1.56 which became available between the filing date of the prior application and the national or PCT International filing date of this application:

(Application Serial No.)

(Filing Date)

(Status)
(patented, pending, abandoned)

(Application Serial No.)

(Filing Date)

(Status)
(patented, pending, abandoned)

(Application Serial No.)

(Filing Date)

(Status)
(patented, pending, abandoned)

I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code and that such willful false statements may jeopardize the validity of the application or any patent issued thereon.

Full name of sole or first inventor James A. Cooper	
Sole or first inventor's signature	Date
Residence 511 Kerber Road, West Lafayette, IN 47906-9433	
Citizenship USA	
Post Office Address 511 Kerber Road, West Lafayette, IN 47906-9433	

Full name of second inventor, if any Asmita Saha	
Second inventor's signature	Date
Residence	
Citizenship	
Post Office Address	

Full name of third inventor, if any	
Third inventor's signature	Date
Residence	
Citizenship	
Post Office Address	

Full name of fourth inventor, if any	
Fourth inventor's signature	Date
Residence	
Citizenship	
Post Office Address	

Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it displays a valid OMB control number.

PATENT APPLICATION FEE DETERMINATION RECORD

Substitute for Form PTO-875 Effective December 8, 2004

Application or Docket Number

11338007

APPLICATION AS FILED - PART I

(Column 1)

(Column 2)

SMALL ENTITY

OR

OTHER THAN SMALL ENTITY

FOR	NUMBER FILED	NUMBER EXTRA
BASIC FEE (37 CFR 1.16(a), (b), or (c))	N/A	N/A
SEARCH FEE (37 CFR 1.16(k), (l), or (m))	N/A	N/A
EXAMINATION FEE (37 CFR 1.16(d), (p), or (q))	N/A	N/A
TOTAL CLAIMS (37 CFR 1.16(i))	23 minus 20 =	3
INDEPENDENT CLAIMS (37 CFR 1.16(h))	4 minus 3 =	1
APPLICATION SIZE FEE (37 CFR 1.16(e))	If the specification and drawings exceed 100 sheets of paper, the application size fee due is \$250 (\$125 for small entity) for each additional 50 sheets or fraction thereof. See 35 U.S.C. 41(a)(1)(G) and 37 CFR 1.16(s).	
MULTIPLE DEPENDENT CLAIM PRESENT (37 CFR 1.16(j))		

RATE (\$)	FEE (\$)
N/A	150.00
N/A	250
N/A	100
X\$ 25 =	
X100 =	
+180=	
TOTAL	

RATE (\$)	FEE (\$)
N/A	300.00
N/A	500
N/A	200
X\$50 =	150
X200 =	200
+360=	
TOTAL	1350

* If the difference in column 1 is less than zero, enter "0" in column 2.

APPLICATION AS AMENDED - PART II

(Column 1)

(Column 2)

(Column 3)

SMALL ENTITY

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OTHER THAN SMALL ENTITY

AMENDMENT A		CLAIMS REMAINING AFTER AMENDMENT		HIGHEST NUMBER PREVIOUSLY PAID FOR	PRESENT EXTRA
	Total (37 CFR 1.16(i))	*	Minus	**	=
	Independent (37 CFR 1.16(h))	*	Minus	***	=
	Application Size Fee (37 CFR 1.16(s))				
FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))					

RATE (\$)	ADDITIONAL FEE (\$)
X\$ 25 =	
X100 =	
+180=	
TOTAL ADD'L FEE	

RATE (\$)	ADDITIONAL FEE (\$)
X\$50 =	
X200 =	
+360=	
TOTAL ADD'L FEE	

(Column 1)

(Column 2)

(Column 3)

AMENDMENT B		CLAIMS REMAINING AFTER AMENDMENT		HIGHEST NUMBER PREVIOUSLY PAID FOR	PRESENT EXTRA
	Total (37 CFR 1.16(i))	*	Minus	**	=
	Independent (37 CFR 1.16(h))	*	Minus	***	=
	Application Size Fee (37 CFR 1.16(s))				
FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))					

RATE (\$)	ADDITIONAL FEE (\$)
X\$ 25 =	
X100 =	
+180=	
TOTAL ADD'L FEE	

RATE (\$)	ADDITIONAL FEE (\$)
X\$50 =	
X200 =	
+360=	
TOTAL ADD'L FEE	

* If the entry in column 1 is less than the entry in column 2, write "0" in column 3.

** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 20, enter "20".

*** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 3, enter "3".

The "Highest Number Previously Paid For" (Total or Independent) is the highest number found in the appropriate box in column 1.

This collection of information is required by 37 CFR 1.16. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 12 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.

PATENT APPLICATION SERIAL NO _____

U.S. DEPARTMENT OF COMMERCE
PATENT AND TRADEMARK OFFICE
FEE RECORD SHEET

01/26/2006 HMARZII 00000023 100435 11338007

01 FC:1011	300.00 DA
02 FC:1111	500.00 DA
03 FC:1311	200.00 DA
04 FC:1201	200.00 DA
05 FC:1202	150.00 DA

PTO-1556

(5/87)



UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
 United States Patent and Trademark Office
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 P.O. Box 1450
 Alexandria, Virginia 22313-1450
 www.uspto.gov

APPLICATION NUMBER	FILING OR 371 (c) DATE	FIRST NAMED APPLICANT	ATTORNEY DOCKET NUMBER
11/338,007	01/23/2006	James A. Cooper	3220-79132

23643
 BARNES & THORNBURG
 11 SOUTH MERIDIAN
 INDIANAPOLIS, IN 46204

CONFIRMATION NO. 4085
FORMALITIES
LETTER

Date Mailed: 03/01/2006

NOTICE TO FILE MISSING PARTS OF NONPROVISIONAL APPLICATION

FILED UNDER 37 CFR 1.53(b)

Filing Date Granted

Items Required To Avoid Abandonment:

An application number and filing date have been accorded to this application. The item(s) indicated below, however, are missing. Applicant is given **TWO MONTHS** from the date of this Notice within which to file all required items and pay any fees required below to avoid abandonment. Extensions of time may be obtained by filing a petition accompanied by the extension fee under the provisions of 37 CFR 1.136(a).

- The oath or declaration is unsigned.

The applicant needs to satisfy supplemental fees problems indicated below.

The required item(s) identified below must be timely submitted to avoid abandonment:

- To avoid abandonment, a surcharge (for late submission of filing fee, search fee, examination fee or oath or declaration) as set forth in 37 CFR 1.16(f) of \$130 for a non-small entity, must be submitted with the missing items identified in this letter.

SUMMARY OF FEES DUE:

Total additional fee(s) required for this application is **\$130** for a Large Entity

- **\$130** Surcharge.

Items Required To Avoid Processing Delays:

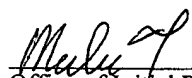
The item(s) indicated below are also required and should be submitted with any reply to this notice to avoid further processing delays.

- A new oath or declaration, identifying this application number is required. The oath or declaration does not comply with 37 CFR 1.63 in that it:
- does not identify the residence (e.g., city and either state or foreign country) of each inventor.

- does not identify the complete mailing or post office address of each inventor.

Replies should be mailed to: Mail Stop Missing Parts
Commissioner for Patents
P.O. Box 1450
Alexandria VA 22313-1450

*A copy of this notice **MUST** be returned with the reply.*

A handwritten signature in cursive script, appearing to read "M. L. G.", is written over a horizontal line.

Office of Initial Patent Examination (571) 272-4000, or 1-800-PTO-9199, or 1-800-972-6382
PART 3 - OFFICE COPY

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BARNES & THORNBURG LLP



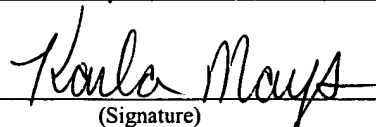
IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Customer No. 23643
Group: 2811
Confirmation No.: 4085
Application No.: 11/338,007
Invention: HIGH-VOLTAGE POWER SEMICONDUCTOR DEVICE
Inventor: James A. Cooper et al.
Filed: January 23, 2006
Attorney
Docket: 3220-79132
Examiner: Unknown

Certificate Under 37 CFR 1.8(a)

I hereby certify that this correspondence is being deposited with the United States Postal Service with sufficient postage as first class mail in an envelope addressed to Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450

on 4/10/06


(Signature)

Karla Mays
(Printed Name)

PRELIMINARY AMENDMENT UNDER 37 C. F. R. §1.115(a)

Mail Stop Amendment
Commissioner for Patents
P. O. Box 1450
Alexandria, VA 22313-1450

Dear Sirs:

Preliminary to the examination of the above-identified national patent application, claiming priority to U.S. Provisional Patent Application No. 60/646,152, Applicants request entry of the amendment to the specification indicated below.

IN THE SPECIFICATION:

Under 37 C.F.R. § 1.121(b) please insert the following after the Title on page 1:

This invention was made with support from DARPA/MTO Grant No. N00014-02-1-0628; the government may have certain rights in this invention.

REMARKS

Applicants do not believe that any fees are due with this Preliminary Amendment; however, the Commissioner is authorized to charge any fees that may be due with this amendment to the deposit account of Barnes & Thornburg account No. 10-0435, with reference to our matter No. 3220-79132.

Respectfully submitted,

BARNES & THORNBURG



Bradford G. Addison
Registration No. 41,486
Attorney for Applicants

BGA/gmk
Indianapolis, IN
(317) 231-7253

Under the Paperwork Reduction Act of 1995, no person is required to respond to a collection of information unless it displays a valid OMB control number.

PATENT APPLICATION FEE DETERMINATION RECORD

Substitute for Form PTO-875 Effective December 8, 2004

Application or DocId Number

11338007

APPLICATION AS FILED - PART I

(Column 1)

(Column 2)

SMALL ENTITY

OR

OTHER THAN SMALL ENTITY

FOR	NUMBER FILED	NUMBER EXTRA
BASIC FEE (37 CFR 1.18(a), (d), or (e))	N/A	N/A
SEARCH FEE (37 CFR 1.18(a), (d), or (e))	N/A	N/A
EXAMINATION FEE (37 CFR 1.18(a), (d), or (e))	N/A	N/A
TOTAL CLAIMS (37 CFR 1.18(b))	23 minus 20 =	
INDEPENDENT CLAIMS (37 CFR 1.18(b))	4 minus 3 =	
APPLICATION SIZE FEE (37 CFR 1.16(a))	If the specification and drawings exceed 100 sheets of paper, the application size fee due is \$250 (\$125 for small entity) for each additional 50 sheets or fraction thereof. See 35 U.S.C. 41(a)(1)(G) and 37 CFR 1.16(s).	

RATE (\$)	FEE (\$)
N/A	150.00
N/A	\$250
N/A	\$100
X\$ 25	
X100	
+180=	
TOTAL	

RATE (\$)	FEE (\$)
N/A	300.00
N/A	\$500
N/A	\$200
X\$50	150
X200	200
+360=	
TOTAL	1350

MULTIPLE DEPENDENT CLAIM PRESENT (37 CFR 1.16(d))

* If the difference in column 1 is less than zero, enter "0" in column 2.

APPLICATION AS AMENDED - PART II

(Column 1)

(Column 2)

(Column 3)

SMALL ENTITY

OR

OTHER THAN SMALL ENTITY

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Total (37 CFR 1.16(b))	23	Minus 23	
Independent (37 CFR 1.16(b))	4	Minus 4	
Application Size Fee (37 CFR 1.16(s))			
FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(d))			

RATE (\$)	ADDITIONAL FEE (\$)
X\$ 25	
X100	
+180=	
TOTAL ADD'L FEE	

RATE (\$)	ADDITIONAL FEE (\$)
X\$50	
X200	
+360=	
TOTAL ADD'L FEE	

AMENDMENT B	CLAIMS REMAINING AFTER AMENDMENT	HIGHEST NUMBER PREVIOUSLY PAID FOR	PRESENT EXTRA
Total (37 CFR 1.16(b))		Minus	
Independent (37 CFR 1.16(b))		Minus	
Application Size Fee (37 CFR 1.16(s))			
FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(d))			

RATE (\$)	ADDITIONAL FEE (\$)
X\$ 25	
X100	
+180=	
TOTAL ADD'L FEE	

RATE (\$)	ADDITIONAL FEE (\$)
X\$50	
X200	
+360=	
TOTAL ADD'L FEE	

- * If the entry in column 1 is less than the entry in column 2, write "0" in column 3.
- ** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 20, enter "20".
- *** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 3, enter "3".

The "Highest Number Previously Paid For" (Total or Independent) is the highest number found in the appropriate box in column 1.

This collection of information is required by 37 CFR 1.16. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 12 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.

If you need assistance in completing the form, call 1-800-PTO-9199 and select option 2.

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If more than 150 claims or 10 actions
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BARNES & THORNBURG LLP

11 South Meridian Street
Indianapolis, Indiana 46204
(317) 236-1313
(317) 231-7433 Fax

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Customer No.: 23643 }
 }
Group: 2811 }
 }
Confirmation No.: 4085 }
 }
Application No.: 11/338,007 }
 }
Invention: HIGH-VOLTAGE POWER }
 SEMICONDUCTOR DEVICE }
 }
Applicant: James A. Cooper et al. }
 }
Filed: January 23, 2006 }
 }
Attorney }
Docket: 3220-79132 }
 }
Examiner: Unknown }

DATED: MAY 18, 2006

RESPONSE TO NOTICE TO FILE MISSING PARTS - FILING DATE GRANTED

Mail Stop Missing Parts
Commissioner for Patents
P. O. Box 1450
Alexandria, VA 22313-1450

Sir:

In response to the Notice to File Missing Parts of Application -- Filing Date
Granted dated March 1, 2006, Applicants submit herewith:

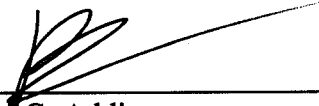
- (1) a Request for One-Month Extension of Time;
- (2) an executed Declaration; and
- (3) a copy of the Notice to File Missing Parts of Nonprovisional Application--
Filing Date Granted.

Applicants hereby authorize the Commissioner to charge the total amount of
\$250.00 to cover the cost of the one-month extension (\$120.00) and the declaration surcharge
(\$130.00) to our Deposit Account No. 10-0435.

The Commissioner is hereby authorized to charge any additional fees which may be required, or credit any overpayments, to Deposit Account No. 10-0435, with reference to our file number 3220-79132.

Respectfully submitted,

BARNES & THORNBURG LLP



Bradford G. Addison
Attorney Reg. No. 41,486

BGA/GMK/kim
Indianapolis, IN
(317) 231-7253



UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
 United States Patent and Trademark Office
 Address: COMMISSIONER FOR PATENTS
 P.O. Box 1450
 Alexandria, Virginia 22313-1450
 www.uspto.gov

APPLICATION NUMBER	FILING OR 371 (c) DATE	FIRST NAMED APPLICANT	ATTORNEY DOCKET NUMBER
11/338,007	01/23/2006	James A. Cooper	3220-79132

23643
 BARNES & THORNBURG
 11 SOUTH MERIDIAN
 INDIANAPOLIS, IN 46204

CONFIRMATION NO. 4085
FORMALITIES
LETTER

Date Mailed: 03/01/2006

NOTICE TO FILE MISSING PARTS OF NONPROVISIONAL APPLICATION

FILED UNDER 37 CFR 1.53(b)

Filing Date Granted

Items Required To Avoid Abandonment:

An application number and filing date have been accorded to this application. The item(s) indicated below, however, are missing. Applicant is given **TWO MONTHS** from the date of this Notice within which to file all required items and pay any fees required below to avoid abandonment. Extensions of time may be obtained by filing a petition accompanied by the extension fee under the provisions of 37 CFR 1.136(a).

- The oath or declaration is unsigned.

The applicant needs to satisfy supplemental fees problems indicated below.

The required item(s) identified below must be timely submitted to avoid abandonment:

- To avoid abandonment, a surcharge (for late submission of filing fee, search fee, examination fee or oath or declaration) as set forth in 37 CFR 1.16(f) of \$130 for a non-small entity, must be submitted with the missing items identified in this letter.

SUMMARY OF FEES DUE:

Total additional fee(s) required for this application is **\$130** for a Large Entity

- **\$130** Surcharge.

Items Required To Avoid Processing Delays:

The item(s) indicated below are also required and should be submitted with any reply to this notice to avoid further processing delays.

- A new oath or declaration, identifying this application number is required. The oath or declaration does not comply with 37 CFR 1.63 in that it:
- does not identify the residence (e.g., city and either state or foreign country) of each inventor.

- does not identify the complete mailing or post office address of each inventor.

Replies should be mailed to: Mail Stop Missing Parts
Commissioner for Patents
P.O. Box 1450
Alexandria VA 22313-1450

*A copy of this notice **MUST** be returned with the reply.*

Mulu T

Office of Initial Patent Examination (571) 272-4000, or 1-800-PTO-9199, or 1-800-972-6382
PART 2 - COPY TO BE RETURNED WITH RESPONSE

Docket No.
3220-79132

Declaration For Patent Application

English Language Declaration

As a below named inventor, I hereby declare that:

My residence, post office address and citizenship are as stated below next to my name,

I believe I am the original, first and sole inventor (if only one name is listed below) or an original, first and joint inventor (if plural names are listed below) of the subject matter which is claimed and for which a patent is sought on the invention entitled

HIGH-VOLTAGE POWER SEMICONDUCTOR DEVICE

the specification of which

(check one)

☐ is attached hereto.

☒ was filed on January 23, 2006 as United States Application No. or PCT International Application Number 11/338,007

and was amended on _____

(if applicable)

I hereby state that I have reviewed and understand the contents of the above identified specification, including the claims, as amended by any amendment referred to above.

I acknowledge the duty to disclose information which is material to patentability as defined in 37 CFR 1.56, including for continuation-in-part applications, material information which became available between the filing date of the prior applications and the national or PCT international filing date of the continuation-in-part application.

I hereby claim foreign priority benefits under 35 U.S.C. 119(a)-(d) or (f), or 365(b) of any foreign application(s) for patent, inventor's or plant breeder's rights certificate(s), or 365(a) of any PCT International application which designated at least one country other than the United States of America, listed below and have also identified below, by checking the box, any foreign application for patent or inventor's or plant breeder's rights certificate(s), or any PCT international application having a filing date before that of the application on which priority is claimed.

Prior Foreign Application(s)

Priority Claimed

(Number) _____	(Country) _____	(Day/Month/Year Filed) _____	<input type="checkbox"/>
(Number) _____	(Country) _____	(Day/Month/Year Filed) _____	<input type="checkbox"/>
(Number) _____	(Country) _____	(Day/Month/Year Filed) _____	<input type="checkbox"/>

I hereby claim the benefit under 35 U.S.C. Section 119(e) of any United States provisional application(s) listed below:

60/646,152	1/21/05
(Application Serial No.)	(Filing Date)

_____ (Application Serial No.) _____ (Filing Date)

(Application Serial No.) _____ (Filing Date) _____

I hereby claim the benefit under 35 U. S. C. Section 120 of any United States application(s), or Section 365(c) of any PCT International application designating the United States, listed below and, insofar as the subject matter of each of the claims of this application is not disclosed in the prior United States or PCT International application in the manner provided by the first paragraph of 35 U.S.C. Section 112, I acknowledge the duty to disclose to the United States Patent and Trademark Office all information known to me to be material to patentability as defined in Title 37, CFR Section 1.56 which became available between the filing date of the prior application and the national or PCT International filing date of this application:

(Application Serial No.)	(Filing Date)	(Status) (patented, pending, abandoned)

(Application Serial No.)	(Filing Date)	(Status) (patented, pending, abandoned)
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(Application Serial No.)	(Filing Date)	(Status) (patented, pending, abandoned)
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I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code and that such willful false statements may jeopardize the validity of the application or any patent issued thereon.

Full name of sole or first inventor James A. Cooper	5-2-06
Sole or first inventor's signature <i>James A. Cooper</i>	Date
Residence 511 Kerber Road, West Lafayette, IN 47906-9433	
Citizenship USA	
Post Office Address 511 Kerber Road, West Lafayette, IN 47906-9433	

Full name of second inventor, if any Asmita Saha	
Second inventor's signature 411, NORTH SALISBURY ST. AP A, WEST LAFAYETTE, IN 47906.	Date
Residence INDIAN	
Citizenship 411, NORTH SALISBURY ST. AP A, WEST LAFAYETTE, IN 47906	
Post Office Address	

Full name of third inventor, if any	
Third inventor's signature	Date
Residence	
Citizenship	
Post Office Address	

Full name of fourth inventor, if any	
Fourth inventor's signature	Date
Residence	
Citizenship	
Post Office Address	

Electronic Patent Application Fee Transmittal

Application Number:	11338007			
Filing Date:	23-Jan-2006			
Title of Invention:	High-voltage power semiconductor device			
First Named Inventor:	James A. Cooper			
Filer:	Bradford G. Addison/Karla Mays			
Attorney Docket Number:	3220-79132			
Filed as Large Entity				
Utility Filing Fees				
Description	Fee Code	Quantity	Amount	Sub-Total in USD(\$)
Basic Filing:				
Pages:				
Claims:				
Miscellaneous-Filing:				
Late filing fee or oath or declaration	1051	1	130	130
Petition:				
Patent-Appeals-and-Interference:				
Post-Allowance-and-Post-Issuance:				
Extension-of-Time:				

Description	Fee Code	Quantity	Amount	Sub-Total in USD(\$)
Extension - 1 month with \$0 paid	1251	1	120	120
Miscellaneous:				
Total in USD (\$)				250

Electronic Acknowledgement Receipt

EFS ID:	1051440
Application Number:	11338007
Confirmation Number:	4085
Title of Invention:	High-voltage power semiconductor device
First Named Inventor:	James A. Cooper
Customer Number:	23643
Filer:	Bradford G. Addison/Karla Mays
Filer Authorized By:	Bradford G. Addison
Attorney Docket Number:	3220-79132
Receipt Date:	18-MAY-2006
Filing Date:	23-JAN-2006
Time Stamp:	17:22:05
Application Type:	Utility
International Application Number:	

Payment information:

Submitted with Payment	yes
Payment was successfully received in RAM	\$ 250
RAM confirmation Number	214
Deposit Account	100435
The Director of the USPTO is hereby authorized to charge indicated fees and credit any overpayment as follows: Charge any Additional Fees required under 37 C.F.R. Section 1.16 and 1.17	

File Listing:

Document Number	Document Description	File Name	File Size(Bytes)	Multi Part	Pages				
1		79132.pdf	276534	yes	8				
	Multipart Description								
	Doc Desc		Start	End					
	Authorization for Extension of Time all replies		1	1					
	Applicant Response to Pre-Exam Formalities Notice		2	5					
	Oath or Declaration filed		6	8					
Warnings:									
Information:									
2	Fee Worksheet (PTO-875)	fee-info.pdf	8305	no	2				
Warnings:									
Information:									
Total Files Size (in bytes):			284839						
<p>This Acknowledgement Receipt evidences receipt on the noted date by the USPTO of the indicated documents, characterized by the applicant, and including page counts, where applicable. It serves as evidence of receipt similar to a Post Card, as described in MPEP 503.</p> <p><u>New Applications Under 35 U.S.C. 111</u> If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application.</p> <p><u>National Stage of an International Application under 35 U.S.C. 371</u> If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.</p>									

BARNES & THORNBURG LLP

11 South Meridian Street
Indianapolis, IN 46204
(317) 236-1313
(317) 231-7433 Fax

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

<i>Customer No.:</i>	23643	}
		}
<i>Group:</i>	2811	}
		}
<i>Confirmation No.:</i>	4085	}
		}
<i>Application No.:</i>	11/338,007	}
		}
<i>Invention:</i>	HIGH-VOLTAGE POWER SEMICONDUCTOR DEVICE	}
		}
<i>Applicant:</i>	James A. Cooper et al.	}
		}
<i>Filed:</i>	January 23, 2006	}
		}
<i>Attorney</i>		}
<i>Docket:</i>	3220-79132	}
		}
<i>Examiner:</i>	Unknown	}

DATED: AUGUST 3, 2006

SUBMISSION OF POWER OF ATTORNEY TO PROSECUTE APPLICATIONS BEFORE THE USPTO AND STATEMENT UNDER 37 CFR 3.73(B)

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

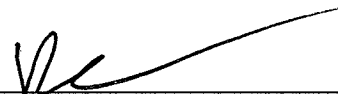
Sir:

Applicants submit for the above-identified application the following: (1) Power of Attorney to Prosecute Applications Before the USPTO (Form PTO/SB/80), and (2) a Statement Under 37 CFR 3.73(b) (Form PTO/SB/96) indicating reel and frame number of an assignment recorded in the above-captioned matter.

Please charge any fees that may be due in connection with this submission to our
Deposit Account No. 10-0435.

Respectfully submitted,

BARNES & THORNBURG LLP

A handwritten signature in black ink, appearing to read 'B. Addison', is written over a horizontal line.

Bradford G. Addison
Attorney Reg. No. 41,486

BGA/GMK/kim
Indianapolis, IN
(317) 231-7253

BARNES & THORNBURG LLP

11 South Meridian Street
Indianapolis, IN 46204
(317) 236-1313
(317) 231-7433 Fax

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

<i>Customer No.:</i>	23643	}	
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<i>Group:</i>	2811	}	
		}	
<i>Confirmation No.:</i>	4085	}	
		}	
<i>Application No.:</i>	11/338,007	}	
		}	
<i>Invention:</i>	HIGH-VOLTAGE POWER SEMICONDUCTOR DEVICE	}	DATED: AUGUST 3, 2006
		}	
<i>Applicant:</i>	James A. Cooper et al.	}	
		}	
<i>Filed:</i>	January 23, 2006	}	
		}	
<i>Attorney</i>		}	
<i>Docket:</i>	3220-79132	}	
		}	
<i>Examiner:</i>	Unknown	}	

SUBMISSION OF POWER OF ATTORNEY TO PROSECUTE APPLICATIONS BEFORE THE USPTO AND STATEMENT UNDER 37 CFR 3.73(B)

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

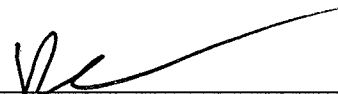
Sir:

Applicants submit for the above-identified application the following: (1) Power of Attorney to Prosecute Applications Before the USPTO (Form PTO/SB/80), and (2) a Statement Under 37 CFR 3.73(b) (Form PTO/SB/96) indicating reel and frame number of an assignment recorded in the above-captioned matter.

Please charge any fees that may be due in connection with this submission to our
Deposit Account No. 10-0435.

Respectfully submitted,

BARNES & THORNBURG LLP

A handwritten signature in black ink, appearing to read 'B. Addison', is written over a horizontal line.

Bradford G. Addison
Attorney Reg. No. 41,486

BGA/GMK/kim
Indianapolis, IN
(317) 231-7253

STATEMENT UNDER 37 CFR 3.73(b)Applicant/Patent Owner: James A. Cooper et al./Purdue Research FoundationApplication No./Patent No./Control No.: 11/338,007 Filed/Issue Date: January 23, 2006Entitled: **HIGH-VOLTAGE POWER SEMICONDUCTOR DEVICE**Purdue Research Foundation, a corporation

(Name of Assignee)

(Type of Assignee, e.g., corporation, partnership, university, government agency, etc.)

states that it is:

1. ☒ the assignee of the entire right, title, and interest; or
2. ☐ an assignee of less than the entire right, title and interest
The extent (by percentage) of its ownership interest is _____ %

in the patent application/patent identified above by virtue of either:

- A. ☒ An assignment from the inventor(s) of the patent application/patent identified above. The assignment was recorded in the United States Patent and Trademark Office at 017637, Frame 0557, or a true copy of the original is attached.

OR

- B. ☐ A chain of title from the inventor(s), of the patent application/patent identified above, to the current assignee as follows:

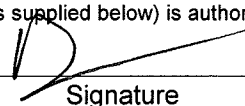
1. From: _____ To: _____
The document was recorded in the United States Patent and Trademark Office at
Reel _____, Frame _____, or for which a copy thereof is attached.
2. From: _____ To: _____
The document was recorded in the United States Patent and Trademark Office at
Reel _____, Frame _____, or for which a copy thereof is attached.
3. From: _____ To: _____
The document was recorded in the United States Patent and Trademark Office at
Reel _____, Frame _____, or for which a copy thereof is attached.

- ☐ Additional documents in the chain of title are listed on a supplemental sheet.

As required by 37 CFR 3.73(b)(1)(i), the documentary evidence of the chain of title from the original owner to the assignee was, or concurrently is being, submitted for recordation pursuant to 37 CFR 3.11.

[NOTE: A separate copy (i.e., a true copy of the original assignment document(s)) must be submitted to Assignment Division in accordance with 37 CFR Part 3, to record the assignment in the records of the USPTO. See MPEP 302.08]

The undersigned (whose title is supplied below) is authorized to act on behalf of the assignee.


Signature

Bradford G. Addison

Printed or Typed Name

Attorney

Title

8/3/06
Date

(317) 231-7253

Telephone number

Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it displays a valid OMB control number.

POWER OF ATTORNEY TO PROSECUTE APPLICATIONS BEFORE THE USPTO

I hereby appoint:



Practitioners associated with the Customer Number:

23643

OR



Practitioner(s) named below (if more than ten patent practitioners are to be named, then a customer number must be used):

Name	Registration Number

as attorney(s) or agent(s) to represent the undersigned before the United States Patent and Trademark Office (USPTO) in connection with any and all patent applications assigned only to the undersigned according to the USPTO assignment records or assignment documents attached to this form in accordance with 37 CFR 3.73(b).

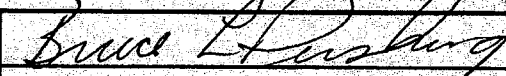
Assignee Name and Address:

Purdue Research Foundation
3000 Kent Avenue
West Lafayette, Indiana 47906

A copy of this form, together with a statement under 37 CFR 3.73(b) (Form PTO/SB/96 or equivalent) is required to be filed in each application in which this form is used. The statement under 37 CFR 3.73(b) may be completed by one of the practitioners appointed in this form if the appointed practitioner is authorized to act on behalf of the assignee, and must identify the application in which this Power of Attorney is to be filed.

SIGNATURE of Assignee of Record

The individual whose signature and title is supplied below is authorized to act on behalf of the assignee

Signature		Date	October 19, 2004
Name	Bruce L. Pershing	Telephone	(765) 496-7712
Title	Investment Officer and Corporate Secretary		

This collection of information is required by 37 CFR 1.31 and 1.33. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.11 and 1.14. This collection is estimated to take 3 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

If you need assistance in completing the form, call 1-800-PTO-9199 and select option 2.

Electronic Acknowledgement Receipt

EFS ID:	1139035
Application Number:	11338007
Confirmation Number:	4085
Title of Invention:	High-voltage power semiconductor device
First Named Inventor:	James A. Cooper
Customer Number:	23643
Filer:	Bradford G. Addison/Karla Mays
Filer Authorized By:	Bradford G. Addison
Attorney Docket Number:	3220-79132
Receipt Date:	03-AUG-2006
Filing Date:	23-JAN-2006
Time Stamp:	10:30:06
Application Type:	Utility
International Application Number:	

Payment information:

Submitted with Payment	no
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File Listing:

Document Number	Document Description	File Name	File Size(Bytes)	Multi Part	Pages
1		79132.PDF	429603	yes	4

	Multipart Description		
	Doc Desc	Start	End
	Transmittal to TC	1	2
	Assignee showing of ownership per 37 CFR 3.73(b).	3	3
	Power of Attorney (may include Associate POA)	4	4
Warnings:			
Information:			
Total Files Size (in bytes):		429603	
<p>This Acknowledgement Receipt evidences receipt on the noted date by the USPTO of the indicated documents, characterized by the applicant, and including page counts, where applicable. It serves as evidence of receipt similar to a Post Card, as described in MPEP 503.</p> <p><u>New Applications Under 35 U.S.C. 111</u> If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application.</p> <p><u>National Stage of an International Application under 35 U.S.C. 371</u> If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.</p>			

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PATENT APPLICATION FEE DETERMINATION RECORD

Substitute for Form PTO-875 Effective December 8, 2004

Application or DocId Number

11338007

APPLICATION AS FILED - PART I

(Column 1)

(Column 2)

SMALL ENTITY

OR

OTHER THAN SMALL ENTITY

FOR	NUMBER FILED	NUMBER EXTRA
BASIC FEE (37 CFR 1.16(a), (b), or (c))	N/A	N/A
SEARCH FEE (37 CFR 1.16(d), (e), or (f))	N/A	N/A
EXAMINATION FEE (37 CFR 1.16(g), (h), or (i))	N/A	N/A
TOTAL CLAIMS (37 CFR 1.16(j))	23 minus 20 =	3
INDEPENDENT CLAIMS (37 CFR 1.16(k))	4 minus 3 =	1
APPLICATION SIZE FEE (37 CFR 1.16(l))	If the specification and drawings exceed 100 sheets of paper, the application size fee due is \$250 (\$125 for small entity) for each additional 50 sheets or fraction thereof. See 35 U.S.C. 41(a)(1)(G) and 37 CFR 1.16(s).	
MULTIPLE DEPENDENT CLAIM PRESENT (37 CFR 1.16(m))		

RATE (\$)	FEE (\$)
N/A	150.00
N/A	\$250
N/A	\$100
X\$ 25 =	
X100 =	
+180=	
TOTAL	

RATE (\$)	FEE (\$)
N/A	300.00
N/A	\$500
N/A	\$200
X\$50 =	150
X200 =	200
+360=	
TOTAL	1350

* If the difference in column 1 is less than zero, enter "0" in column 2.

APPLICATION AS AMENDED - PART II

(Column 1)

(Column 2)

(Column 3)

SMALL ENTITY

OR

OTHER THAN SMALL ENTITY

AMENDMENT A	CLAIMS REMAINING AFTER AMENDMENT	HIGHEST NUMBER PREVIOUSLY PAID FOR	PRESENT EXTRA
Total (37 CFR 1.16(j))	23	Minus 23	=
Independent (37 CFR 1.16(k))	4	Minus 4	=
Application Size Fee (37 CFR 1.16(s))			
FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(m))			

RATE (\$)	ADDITIONAL FEE (\$)
X\$ 25 =	
X100 =	
+180=	
TOTAL ADD'L FEE	

RATE (\$)	ADDITIONAL FEE (\$)
X\$50 =	
X200 =	
+360=	
TOTAL ADD'L FEE	

AMENDMENT B	CLAIMS REMAINING AFTER AMENDMENT	HIGHEST NUMBER PREVIOUSLY PAID FOR	PRESENT EXTRA
Total (37 CFR 1.16(j))		Minus	=
Independent (37 CFR 1.16(k))		Minus	=
Application Size Fee (37 CFR 1.16(s))			
FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(m))			

RATE (\$)	ADDITIONAL FEE (\$)
X\$ 25 =	
X100 =	
+180=	
TOTAL ADD'L FEE	

RATE (\$)	ADDITIONAL FEE (\$)
X\$50 =	
X200 =	
+360=	
TOTAL ADD'L FEE	

- * If the entry in column 1 is less than the entry in column 2, write "0" in column 3.
- ** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 20, enter "20".
- *** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 3, enter "3".

The "Highest Number Previously Paid For" (Total or Independent) is the highest number found in the appropriate box in column 1.

This collection of information is required by 37 CFR 1.16. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 12 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.

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EAST Search History

Ref #	Hits	Search Query	DBs	Default Operator	Plurals	Time Stamp
S1	1393	((Cooper near (James J)) (Saha near (Asmita A))).in.	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2007/03/22 10:54
S2	380394	"257".clas.	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2007/03/22 09:01
S3	7	S1 and S2	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2007/03/22 09:01
S4	4717	((257/263) or (257/256) or (257/341) or (257/342) or (257/335) or (257/339) or (257/350)).CCLS.	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2007/03/22 10:55
S5	3327	((438/142) or (438/156) or (438/176) or (438/186) or (438/197) or (438/268)).CCLS.	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2007/03/22 10:56
S6	7886	S4 S5	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2007/03/22 11:03
S7	156976	MOSFET ("metal oxide semiconductor")	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2007/03/22 11:04
S8	5305	DMOS	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2007/03/22 11:04

EAST Search History

S9	304	Double adj implant	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2007/03/22 11:04
S10	57449	power same (FET "Field effect")	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2007/03/22 11:06
S11	8478	JFET ("Junction Field Effect")	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2007/03/22 11:07
S12	3533	current near spread\$3	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2007/03/23 10:28
S13	10361	Drift near5 (layer region)	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2007/03/22 11:10
S14	0	S6 and S7 and S9 and S10 and S11 and S12 and S13	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2007/03/22 11:12
S15	20	S7 and S12 and S13 and S6	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2007/03/22 11:13
S16	80	S7 and S12 and S13	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2007/03/22 11:34

EAST Search History

S17	0	S16 and S9	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2007/03/22 11:14
S18	180117	siC (Silicon adj carbide)	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2007/03/22 11:35
S19	548	S11 and S13 and S7	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2007/03/22 14:11
S20	202	S19 and S6	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2007/03/23 12:53
S21	1125	257/341.ccls.	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2007/03/22 15:36
S22	145	S21 and S11	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2007/03/22 15:36
S23	16	S21 and S12	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2007/03/22 15:58
S24	49	S6 and S12	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2007/03/22 16:11

EAST Search History

S25	628	S6 and S18	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2007/03/22 16:12
S26	92	S21 and S18	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2007/03/22 16:12
S27	1121	current near spread\$3 near5 layer	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2007/03/23 10:29
S28	1125	257/341.ccls.	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2007/03/23 10:29
S29	6	S27 and S28	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2007/03/23 10:32
S30	4717	((257/263) or (257/256) or (257/341) or (257/342) or (257/335) or (257/339) or (257/350)).CCLS.	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2007/03/23 10:32
S31	3327	((438/142) or (438/156) or (438/176) or (438/186) or (438/197) or (438/268)).CCLS.	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2007/03/23 10:32
S32	7886	S30 S31	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2007/03/23 10:32

EAST Search History

S33	12	S27 and S32	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2007/03/23 10:32
S34	156976	MOSFET ("metal oxide semiconductor")	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2007/03/23 12:47
S35	8478	JFET ("Junction Field Effect")	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2007/03/23 12:47
S36	10361	Drift near5 (layer region)	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2007/03/23 12:47
S37	548	S35 and S36 and S34	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2007/03/23 12:47
S38	202	S37 and S32	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2007/03/23 12:47
S39	195	S38 and dop\$3	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2007/03/23 14:03
S40	187432	S34 amd S36 and (dop\$3 concentrat\$3 dos\$3)	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2007/03/23 14:06

EAST Search History

S41	4013	S40 and S32	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2007/03/23 14:07
S42	436	S41 and S35	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2007/03/23 15:25
S43	4	S42 and S27	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2007/03/23 15:25
S44	5	S42 and current near5 spread	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2007/03/23 15:27
S45	36	S41 and current near5 spread	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2007/03/26 08:21
S46	2	("5688725").PN.	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2007/03/23 15:50
S47	5	("4941026" "5341011" "5424231" "5532179" "5558313").PN.	US-PGPUB; USPAT; USOCR	OR	ON	2007/03/26 08:12
S48	2	("4941026").PN.	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2007/03/26 08:12
S49	4717	((257/263) or (257/256) or (257/341) or (257/342) or (257/335) or (257/339) or (257/350)).CCLS.	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2007/03/26 08:21

EAST Search History

S50	3327	((438/142) or (438/156) or (438/176) or (438/186) or (438/197) or (438/268)).CCLS.	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2007/03/26 08:21
S51	7886	S49 S50	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2007/03/26 08:21
S52	157110	MOSFET ("metal oxide semiconductor")	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2007/03/26 08:21
S53	10368	Drift near5 (layer region)	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2007/03/26 08:21
S54	187573	S52 amd S53 and (dop\$3 concentrat\$3 dos\$3)	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2007/03/26 08:21
S55	4013	S54 and S51	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2007/03/26 08:21
S56	72	S55 and current near5 spread\$3	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2007/03/26 08:22



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11A

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
11/338,007	01/23/2006	James A. Cooper	3220-79132	4085

23643 7590 04/04/2007
BARNES & THORNBURG LLP
11 SOUTH MERIDIAN
INDIANAPOLIS, IN 46204

EXAMINER

PATTON, PAUL E

ART UNIT	PAPER NUMBER
----------	--------------

2822

SHORTENED STATUTORY PERIOD OF RESPONSE	MAIL DATE	DELIVERY MODE
3 MONTHS	04/04/2007	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

If NO period for reply is specified above, the maximum statutory period will apply and will expire 6 MONTHS from the mailing date of this communication.

DETAILED ACTION

Oath/Declaration

1. The oath or declaration is defective. A new oath or declaration in compliance with 37 CFR 1.67(a) identifying this application by application number and filing date is required. See MPEP §§ 602.01 and 602.02.

The oath or declaration is defective because: the signature of the second inventor is lacking.

Claim Rejections - 35 USC § 102

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

3. Claims 1, 3, 4, 9, 10 12, 13 and 15 are rejected under 35 U.S.C. 102(b) as being anticipated by Ono et al., (US 2003/0227052 A1) Ono.
4. As to claims 1,3,4,9,12, and 13, Ono discloses and shows (Fig 1), a double implanted MOS field effect transistor comprising a semiconductor substrate (10) having a first concentration of first type impurities (n+); a drift semiconductor layer (50) formed on a front side of the semiconductor substrate and having a second concentration of first type impurities less than the first concentration of first type impurities (n-); a first source region (20); a second source region (20); and a JFET region (40) defined between the first source region and the second source region, the JFET region having a third concentration of first type impurities that is greater than the second concentration

of first type impurities (n) and having a width (L) less than about 3 micrometers and a width of about one micrometer. (Paragraphs [0039] & [0041]).

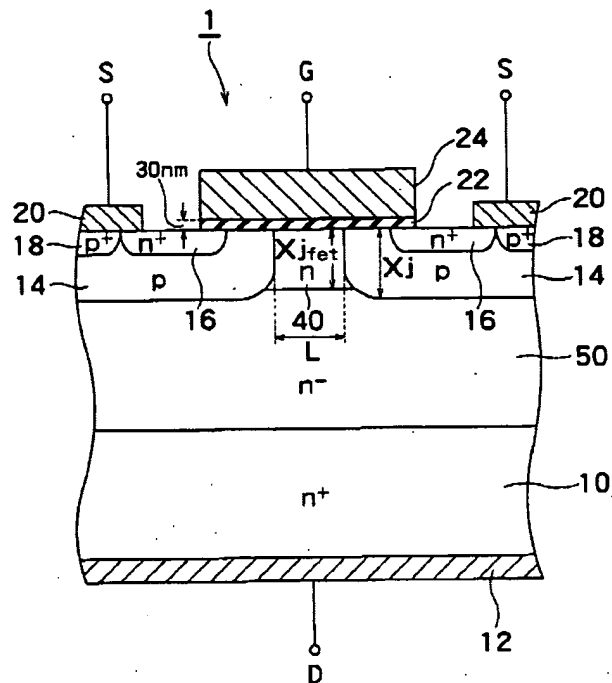


FIG. 1

5. As to claims 10 and 15, Ono shows (Fig 12) a plurality of base contact regions (18) formed in each of the first and second source regions (16), the base contact regions being smaller than the first and second source regions.

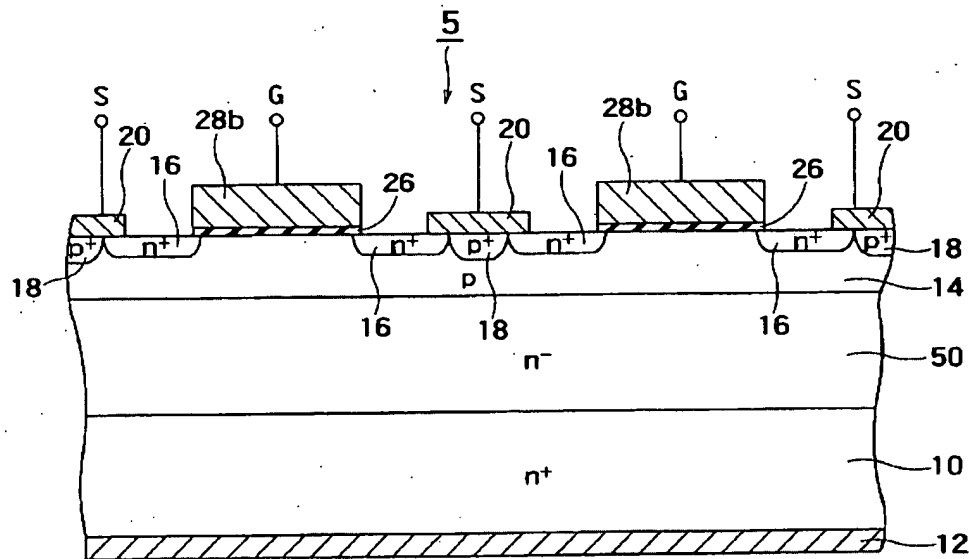


FIG. 12

Claim Rejections - 35 USC § 103

6. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

7. Claim 2 is rejected under 35 U.S.C. 103(a) as being unpatentable over Ono in view of Kumar et al., (USPAT 6,573,534.B1) Kumar.

8. Ono does not disclose that the semiconductor substrate is a silicon-carbide substrate.

9. Kumar is related to a similar MOS FET structure and discloses that the substrate is a silicon-carbide substrate (Column 1, line 40).

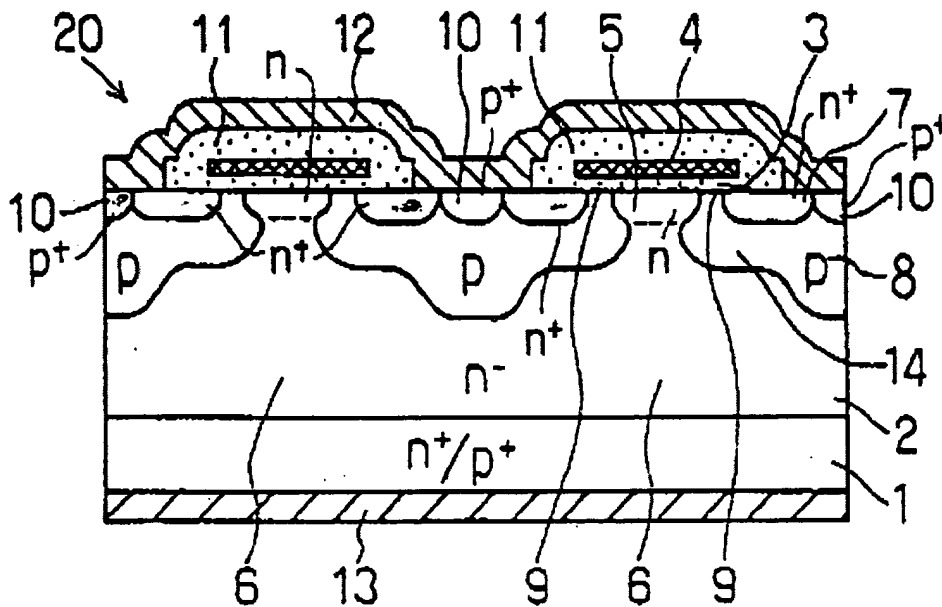
10. Kumar is evidence that a person of ordinary skill in the art would find a reason, suggestion or motivation to use a silicon-carbide substrate.

11. Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Ono by using a silicon-carbide substrate for advantages such as higher breakdown voltage and lower ON resistance according to the teachings of Kumar (Column 1, lines 27-30).

12. Claims 5 and 14 are rejected under 35 U.S.C. 103(a) as being unpatentable over Ono in view of Tokura et al., (USPAT 5,545,908).

13. Ono does not disclose that the concentration of first type impurities associated with the JFET region is at least one order of magnitude greater than the concentration of first type impurities associated with the drift region.

14. Tokura is related to a similar MOSFET structure and discloses and shows (Tokura, Fig 1) that the doping level at the JFET region (5) is $8 \times 10^{16} \text{ cm}^{-3}$ whereas the doping level of the drift region (2) is $5 \times 10^{15} \text{ cm}^{-3}$. (Tokura, Column 10, lines 29-33 & Column 11, lines 54-58). Note that Tokura does not label the region between the two p doped wells on opposite sides of the gate as a JFET. However the structure in this device as well as Ono will form a parasitic JFET due to the arrangement of the layers. (Ono, Paragraph [0040]).



Tokura, Fig 1

15. Tokura is evidence that a person of ordinary skill in the art would find a reason, suggestion or motivation to have the concentration of the JFET region at least an order of magnitude greater than the concentration of the drift region.

16. Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Ono by having the concentration of the JFET region at least an order of magnitude greater than the concentration of the drift region for advantages such as reduced ON resistance according to the teachings of Tokura (Column 5, lines 60-66 & Column 8, lines 33-34).

17. Claims 6-8 and 17-21 are rejected under 35 U.S.C. 103(a) as being unpatentable over Ono in view of Zeng et al., (USPAT 6,137,139) Zeng.

18. As to claims 6-8, Ono shows (Ono, Fig 1) the JFET region is formed directly below the gate structure and between the base doped wells formed on either side of the

20. Zeng discloses and shows (Fig 2C) a current spreading layer (103) formed on a front side of the drift semiconductor layer (102) wherein the concentration of impurities of the first type is greater than the concentration of impurities of the first type in the drift region by at least one order of magnitude (Zeng, Column 2, lines 64-67 & Column 3, lines 4-7).



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greater than the concentration of impurities of the first type in the drift region by at least one order of magnitude.

22. Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Ono to have a current spreading layer formed on a front side of the drift semiconductor layer; and wherein the concentration of impurities of the first type is greater than the concentration of impurities of the first type in the drift region by at least one order of magnitude for advantages such as reduced on-resistance without degrading device ruggedness and reliability according to the teachings of Zeng (Column 4, lines 32-39).

23. As to claim 17, Ono discloses and shows (Ono, Fig. 1), a double implanted MOS field effect transistor comprising a semiconductor substrate (10) a drift semiconductor layer (50) formed on a front side of the semiconductor substrate; a first source region (20); a second source region (20); and a JFET region (40) defined between the first source region and the second source region.

24. Ono does not disclose or show a current spreading semiconductor layer formed on a front side of the drift semiconductor layer.

25. Zeng discloses and shows (Fig. 2C) a current spreading layer (103) formed on a front side of the drift semiconductor layer (102).

26. Ono shows (Ono, Fig. 1) the JFET region is formed directly below the gate structure and between the base doped wells formed on either side of the gate. As noted above the parasitic JFET is a consequence of the lateral gate-source arrangement of a vertical MOSFET and would be above the current spreading layer and the drift region shown by Zeng.

Art Unit: 2822

27. Zeng is evidence that a person of ordinary skill in the art would find a reason, suggestion or motivation to have a current spreading layer formed on a front side of the drift semiconductor layer.

28. Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Ono to have a current spreading layer formed on a front side of the drift semiconductor for advantages such as reduced on-resistance without degrading device ruggedness and reliability according to the teachings of Zeng (Column 4, lines 32-39)..

29. As to claims 18 and 19, Ono does not disclose a current spreading semiconductor layer having a first concentration of first type impurities and the drift semiconductor layer has a second concentration of first type impurities, the first concentration of first type impurities being greater than the second concentration by at least one order of magnitude.

30. Zeng discloses a current spreading layer wherein the concentration of impurities of the first type is greater than the concentration of impurities of the first type in the drift region by at least one order of magnitude (Zeng, Column 2, lines 64-67 & Column 3, lines 4-7).

31. Zeng is evidence that a person of ordinary skill in the art would find a reason, suggestion or motivation to have a current spreading layer wherein the concentration of impurities of the first type is greater than the concentration of impurities of the first type in the drift region by at least one order of magnitude.

32. Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Ono to have a current spreading layer wherein

the concentration of impurities of the first type is greater than the concentration of impurities of the first type in the drift region by at least one order of magnitude for advantages such as reduced on-resistance without degrading device ruggedness and reliability according to the teachings of Zeng (Column 4, lines 32-39).

33. As to claim 20, Ono as modified by Zeng discloses the JFET region has a width of about three micrometers or less (Ono, Paragraph [0041]).

34. As to claim 21, Ono as modified by Zeng shows (Fig 12) a plurality of base contact regions (18) formed in each of the first and second source regions (16), the base contact regions being smaller than the first and second source regions.

35. Claims 11 and 16 are rejected under 35 U.S.C. 103(a) as being unpatentable over Ono in view of Kobayashi et al., (US2003/0052329 A1) Kobayashi.

36. As to claims 11 and 16, Ono does not explicitly disclose a plurality of source regions and a plurality of base contact regions, wherein the plurality of source regions and the plurality of base contact regions, form alternating strips of N-type doped regions and P-type doped regions, the alternating strips being substantially orthogonal to respective source electrodes formed over the first and second source regions.

37. Kobayashi shows (Fig 18) a plurality of source regions and a plurality of base contact regions, wherein the plurality of source regions (15) and the plurality of base contact regions (13), form alternating strips of N-type doped regions and P-type doped regions, the alternating strips (17) being substantially orthogonal to respective source electrodes formed over the first and second source regions.

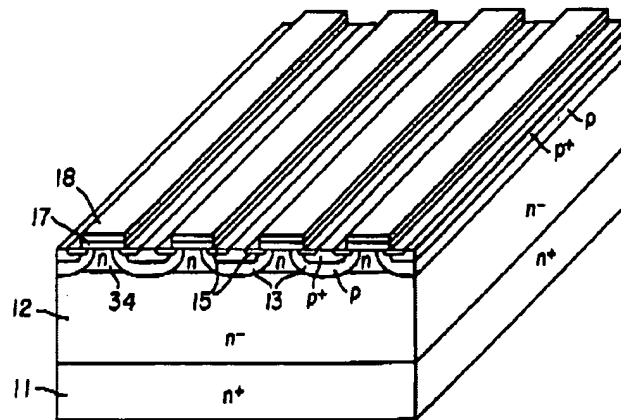


FIG. 18

38. Kobayashi is evidence that a person of ordinary skill in the art would find a reason, suggestion or motivation to form a plurality of source regions and a plurality of base contact regions, wherein the plurality of source regions and the plurality of base contact regions, form alternating strips of N-type doped regions and P-type doped regions, the alternating strips being substantially orthogonal to respective source electrodes formed over the first and second source regions.

39. Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Ono to form a plurality of source regions and a plurality of base contact regions, wherein the plurality of source regions and the plurality of base contact regions, form alternating strips of N-type doped regions and P-type doped regions, the alternating strips being substantially orthogonal to respective source electrodes formed over the first and second source regions for advantages such as reduced electric field strength according to the teachings of Kobayashi (Paragraph [0034]).

40. Claim 22 is rejected under 35 U.S.C. 103(a) as being unpatentable over Ono in view of Zeng and further in view of Kobayashi.

41. Ono as modified by Zeng does not explicitly disclose a plurality of source regions and a plurality of base contact regions, wherein the plurality of source regions and the plurality of base contact regions, form alternating strips of N-type doped regions and P-type doped regions, the alternating strips being substantially orthogonal to respective source electrodes formed over the first and second source regions.

42. Kobayashi shows (Fig 18) a plurality of source regions and a plurality of base contact regions, wherein the plurality of source regions (15) and the plurality of base contact regions (13), form alternating strips of N-type doped regions and P-type doped regions, the alternating strips (17) being substantially orthogonal to respective source electrodes formed over the first and second source regions.

43. Kobayashi is evidence that a person of ordinary skill in the art would find a reason, suggestion or motivation to form a plurality of source regions and a plurality of base contact regions, wherein the plurality of source regions and the plurality of base contact regions, form alternating strips of N-type doped regions and P-type doped regions, the alternating strips being substantially orthogonal to respective source electrodes formed over the first and second source regions.

44. Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Ono as modified by Zeng to form a plurality of source regions and a plurality of base contact regions, wherein the plurality of source regions and the plurality of base contact regions, form alternating strips of N-type doped regions and P-type doped regions, the alternating strips being substantially orthogonal

Art Unit: 2822

to respective source electrodes formed over the first and second source regions for advantages such as reduced electric field strength according to the teachings of Kobayashi (Paragraph [0034]).

45. Claim 23 is rejected under 35 U.S.C. 103(a) as being unpatentable over Ono in view of Zeng and further in view of Tokura and Kumar.

46. Ono discloses and shows (Fig 1), a double implanted MOS field effect transistor comprising a semiconductor substrate (10) having a first concentration of first type impurities (n+); a drift semiconductor layer (50) formed on a front side of the semiconductor substrate and having a second concentration of first type impurities less than the first concentration of first type impurities (n-); a first source region (20); a second source region (20); and a JFET region (40) defined between the first source region and the second source region, the JFET region having a fourth concentration of first type impurities that is greater than the second concentration of first type impurities (n) and having a width (L) less than about 3 micrometers and a width of about one micrometer. (Paragraphs [0039] & [0041]).

47. Ono does not disclose that the semiconductor substrate is silicon-carbide.

48. Kumar discloses that the substrate is a silicon-carbide substrate (Column 1, line 40).

49. Kumar is evidence that a person of ordinary skill in the art would find a reason, suggestion or motivation to use a silicon-carbide substrate.

50. Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Ono by using a silicon-carbide substrate for

advantages such as higher breakdown voltage and lower ON resistance according to the teachings of Kumar (Column 1, lines 27-30).

51. Furthermore, Ono as modified by Kumar does not explicitly disclose that a current spreading layer is formed on a front side of the drift semiconductor layer; and wherein the concentration of impurities of the first type is greater than the concentration of impurities of the first type in the drift region.

52. Zeng discloses and shows (Fig 2C) a current spreading layer (103) formed on a front side of the drift semiconductor layer (102) wherein the concentration of impurities of the first type is greater than the concentration of impurities of the first type in the drift region (Zeng, Column 2, lines 64-67 & Column 3, lines 4-7).

53. Zeng is evidence that a person of ordinary skill in the art would find a reason, suggestion or motivation to have a current spreading layer formed on a front side of the drift semiconductor layer; and wherein the concentration of impurities of the first type is greater than the concentration of impurities of the first type in the drift region.

54. Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Ono as modified by Kumar to have a current spreading layer formed on a front side of the drift semiconductor layer; and wherein the concentration of impurities of the first type is greater than the concentration of impurities of the first type in the drift region for advantages such as reduced on-resistance without degrading device ruggedness and reliability according to the teachings of Zeng (Column 4, lines 32-39).

55. Lastly, Ono as modified by Kumar and Zeng does not disclose that the concentration of first type impurities associated with the JFET region is greater than the concentration of first type impurities associated with the drift region.

56. Tokura is related to a similar MOSFET structure and discloses and shows (Tokura, Fig 1) that the doping level at the JFET region (5) is $8 \times 10^{16} \text{ cm}^{-3}$ whereas the doping level of the drift region (2) is $5 \times 10^{15} \text{ cm}^{-3}$. (Tokura, Column 10, lines 29-33 & Column 11, lines 54-58). Note that Tokura does not label the region between the two p-doped wells on opposite sides of the gate as a JFET. However the structure in this device as well as Ono will form a parasitic JFET due to the arrangement of the layers. (Ono, Paragraph [0040]).

57. Tokura is evidence that a person of ordinary skill in the art would find a reason, suggestion or motivation to have the concentration of the JFET region greater than the concentration of the drift region.

58. Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Ono as modified by Kumar and Zeng by having the concentration of the JFET region at least an order of magnitude greater than the concentration of the drift region for advantages such as reduced ON resistance according to the teachings of Tokura (Column 5, lines 60-66 & Column 8, lines 33-34).


Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Paul E. Patton whose telephone number is 571-272-9762. The examiner can normally be reached on 7:00 - 5:30 Monday through Thursday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Zandra Smith can be reached on 571-272-2429. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

PEP


Zandra V. Smith
Supervisory Patent Examiner
30 March 2007

Paul E Patton
Examiner
Art Unit 2822

Notice of References Cited	Application/Control No. 11/338,007	Applicant(s)/Patent Under Reexamination COOPER ET AL.	
	Examiner Paul E. Patton	Art Unit 2822	Page 1 of 1

U.S. PATENT DOCUMENTS

*		Document Number Country Code-Number-Kind Code	Date MM-YYYY	Name	Classification
*	A	US-2003/0227052	12-2003	Ono et al.	257/341
*	B	US-5,545,908	08-1996	Tokura et al.	257/341
*	C	US-6,573,534 B1	06-2003	Kumar et al.	257/77
*	D	US-2003/0052329 A1	03-2003	Kobayashi et al.	257/135
*	E	US-6,137,139	10-2000	Zeng et al.	257/342
*	F	US-6,552,391 B2	04-2003	Zeng et al.	257/342
*	G	US-2003/0205829 A1	11-2003	Boden, Milton J. JR.	257/921
	H	US-			
	I	US-			
	J	US-			
	K	US-			
	L	US-			
	M	US-			

FOREIGN PATENT DOCUMENTS

*		Document Number Country Code-Number-Kind Code	Date MM-YYYY	Country	Name	Classification
	N					
	O					
	P					
	Q					
	R					
	S					
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NON-PATENT DOCUMENTS

*		Include as applicable: Author, Title Date, Publisher, Edition or Volume, Pertinent Pages)
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	V	
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	X	

*A copy of this reference is not being furnished with this Office action. (See MPEP § 707.05(a).)
Dates in MM-YYYY format are publication dates. Classifications may be US or foreign.



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Bib Data Sheet

CONFIRMATION NO. 4085

SERIAL NUMBER 11/338,007	FILING OR 371(c) DATE 01/23/2006 RULE	CLASS 257	GROUP ART UNIT 2809	ATTORNEY DOCKET NO. 3220-79132
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APPLICANTS

James A. Cooper, West Lafayette, IN;
 Asmita Saha, West Lafayette, IN;

** CONTINUING DATA *****

This appln claims benefit of 60/646,152 01/21/2005

** FOREIGN APPLICATIONS *****

IF REQUIRED, FOREIGN FILING LICENSE GRANTED **
 03/01/2006

Foreign Priority claimed <input type="checkbox"/> yes <input checked="" type="checkbox"/> no	STATE OR COUNTRY IN	SHEETS DRAWING 4	TOTAL CLAIMS 23	INDEPENDENT CLAIMS 4
35 USC 119 (a-d) conditions met <input type="checkbox"/> yes <input checked="" type="checkbox"/> no <input type="checkbox"/> Met after Allowance				
Verified and Acknowledged Examiner's Signature: <i>Paul B. Vetter</i> Initials: <i>PBP</i>				


ADDRESS

23643

TITLE

High-voltage power semiconductor device

FILING FEE RECEIVED 1480	FEES: Authority has been given in Paper No. _____ to charge/credit DEPOSIT ACCOUNT No. _____ for following:	<input type="checkbox"/> All Fees
		<input type="checkbox"/> 1.16 Fees (Filing)
		<input type="checkbox"/> 1.17 Fees (Processing Ext. of time)
		<input type="checkbox"/> 1.18 Fees (Issue)
		<input type="checkbox"/> Other _____
		<input type="checkbox"/> Credit

Index of Claims 	Application/Control No. 11338007	Applicant(s)/Patent Under Reexamination COOPER ET AL.
	Examiner Patton, Paul E	Art Unit 2822


✓	Rejected
=	Allowed

-	Cancelled
÷	Restricted

N	Non-Elected
I	Interference

A	Appeal
O	Objected

<input type="checkbox"/> Claims renumbered in the same order as presented by applicant		<input type="checkbox"/> CPA	<input type="checkbox"/> T.D.	<input type="checkbox"/> R.1.47						
CLAIM		DATE								
Final	Original	03/26/2007								
	1	✓								
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Search Notes 	Application/Control No. 11338007	Applicant(s)/Patent Under Reexamination COOPER ET AL.
	Examiner Patton, Paul E	Art Unit 2822

SEARCHED			
Class	Subclass	Date	Examiner
257	263, 256, 341, 342, 335, 339, 350, 263,	3/22/2007	PEP
438	142, 156, 176, 186, 197, 268	3/22/2007	PEP

SEARCH NOTES		
Search Notes	Date	Examiner
Search history attached	2/26/2007	PEP

INTERFERENCE SEARCH			
Class	Subclass	Date	Examiner

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AUG 6 - 2007

BARNES & THORNBURG LLP

11 South Meridian Street
Indianapolis, Indiana 46204**IN THE UNITED STATES PATENT AND TRADEMARK OFFICE**

Group: 2822
Confirmation No.: 4085
Application No.: 11/338,007
Invention: HIGH-VOLTAGE POWER
SEMICONDUCTOR DEVICE
Applicant: James A. Cooper et al.
Filed: January 23, 2006
Attorney
Docket: 3220-79132
Examiner: Patton, Paul E.

Certificate Under 37 CFR 1.8(a)

I hereby certify that this correspondence is being
facsimile transmitted to the United States Patent
and Trademark Office, fax number (571) 273-
8300

on August 6, 2007

(Signature)

Glen M. Kellett
(Printed Name)AMENDMENT AND REPLY

MAIL STOP AMENDMENT
Commissioner for Patents
P. O. Box 1450
Alexandria, VA 22313-1450

Sir:

In response to the Office Action dated April 4, 2007, please consider the
following:

Amendments to the Claims are reflected in the listing of claims which begins on
page 2 of this paper.

Remarks begin on page 8 of this paper.

AMENDMENTS TO THE CLAIMS

This listing of claims replaces all prior versions and listings of the claims in this application:

1. (Currently Amended) A metal-oxide semiconductor field-effect transistor comprising:

a semiconductor silicone-carbide substrate having a first concentration of first type impurities;

a drift semiconductor layer formed on a front side of the semiconductor substrate and having a second concentration of first type impurities less than the first concentration of first type impurities;

a current spreading semiconductor layer formed on a front side of the drift semiconductor layer;

a first source region;

a second source region; and

a JFET region formed on a front side of the current spreading semiconductor layer and defined between the first source region and the second source region, the JFET region having a third concentration of first type impurities that is greater than the second concentration of first type impurities.

2. (Cancelled)

3. (Original) The metal-oxide semiconductor field-effect transistor of claim 1, wherein the JFET region has a width of less than about three micrometers.

4. (Original) The metal-oxide semiconductor field-effect transistor of claim 3, wherein the JFET region has a width of about one micrometer.

5. (Original) The metal-oxide semiconductor field-effect transistor of claim 1, wherein the third concentration of first type impurities is at least one order of magnitude greater than the second concentration of first type impurities.

6. (Cancelled)

7. (Currently Amended) The metal-oxide semiconductor field-effect transistor of claim ~~6~~ 1, wherein the current spreading semiconductor layer has a fourth concentration of first type impurities that is greater than the second concentration of first type impurities.

8. (Original) The metal-oxide semiconductor field-effect transistor of claim 7, wherein the fourth concentration of first type impurities is at least one order of magnitude greater than the second concentration of first type impurities.

9. (Currently Amended) The metal-oxide semiconductor field-effect transistor of claim ~~6~~ 8, wherein the JFET region has a width of about one micrometer.

10. (Original) The metal-oxide semiconductor field-effect transistor of claim 1, further comprising a plurality of base contact regions formed in each of the first and the second source regions, the base contact regions being smaller than the first and second source regions.

11. (Original) The metal-oxide semiconductor field-effect transistor of claim 1, further comprising a plurality of source regions and a plurality of base contact regions, wherein the plurality of source regions and the plurality of base contact regions form alternating strips of N-type doped regions and P-type doped regions, the alternating strips being substantially orthogonal to respective source electrodes formed over the first and the second source regions.

12. (Currently Amended) A double-implanted metal-oxide semiconductor field-effect transistor comprising:

a ~~semiconductor~~ silicone-carbide substrate;

a drift semiconductor layer formed on a front side of the semiconductor substrate;

a first source region;

a plurality of first base contact regions defined in the first source region, each of the plurality of first base contact regions being spaced apart from each other;

a second source region; ~~and~~

a plurality of second base contact regions defined in the second source region, each of the plurality of second base contact regions being spaced apart from each other; and

a JFET region defined between the first source region and the second source region, the JFET region having a width less than about three micrometers.

13. (Original) The double-implanted metal-oxide semiconductor field-effect transistor of claim 12, wherein the JFET region has a width of about one micrometer.

14. (Original) The double-implanted metal-oxide semiconductor field-effect transistor of claim 12, wherein the JFET region has a first concentration of first type impurities and the drift semiconductor layer has a second concentration of first type impurities, the first concentration of first type impurities being greater than the second concentration of first type impurities.

15-16. (Cancelled)

17. (Currently Amended) A double-implanted metal-oxide semiconductor field-effect transistor comprising:

a semiconductor substrate;

a drift semiconductor layer formed on a front side of the semiconductor substrate;

a current spreading semiconductor layer formed on a front side of the drift semiconductor layer;

~~a first source region;~~

~~a second source region; and~~

a plurality of first and second source regions;

a plurality of base contact regions; and

a JFET region defined between the plurality of first source region regions and the plurality of second source region regions, the JFET region being formed on a front side of the current spreading semiconductor layer,

wherein the plurality of first and second source regions and the plurality of base contact regions form alternating strips of N-type doped regions and P-type doped regions, the alternating strips being substantially orthogonal to respective source electrodes formed over the first and the second source regions.

18. (Original) The double-implanted metal-oxide semiconductor field-effect transistor of claim 17, wherein the current spreading semiconductor layer has a first concentration of first type impurities and the drift semiconductor layer has a second concentration of first type impurities, the first concentration of first type impurities being greater than the second concentration of first type impurities.

19. (Original) The double-implanted metal-oxide semiconductor field-effect transistor of claim 18, wherein the first concentration of first type impurities is at least one order of magnitude greater than the second concentration of first type impurities.

20. (Original) The double-implanted metal-oxide semiconductor field-effect transistor of claim 17, wherein the JFET region has a width of about three micrometers or less.

21-22. (Cancelled)

23. (Original) A vertical double-implanted metal-oxide semiconductor field-effect transistor comprising:

a silicon-carbide substrate having a first concentration of first type impurities;

a drift semiconductor layer epitaxially formed on a front side of the silicon-carbide substrate and having a second concentration of first type impurities less than the first concentration of first type impurities;

a current spreading semiconductor layer epitaxially formed on a front side of the drift layer, the current spreading semiconductor layer having a third concentration of first type impurities greater than the second concentration of first type impurities;

a first source region;

a second source region; and

a JFET region defined between the first source region and the second source region and formed on a front side of the current spreading semiconductor layer, the JFET region having a width less than about three micrometers and a fourth concentration of first type impurities greater than the second concentration of first type impurities.

REMARKS

The Office Action dated April 4, 2007 has been carefully reviewed. Claims 1-23 stand rejected in the 4/4/2007 Office Action. Additionally, the declaration filed on May 18, 2006 is found defective in the 4/4/2007 Office Action. By this amendment, claims 2, 6, 15, 16, 21, and 22 are cancelled without prejudice. Claims 1, 7, 9, 12, and 17 are amended.

DECLARATION

The Examiner found the declaration filed on May 18, 2006 to be defective because the signature of the second named inventor, Ms. Asmita Saha, was lacking. Applicants file herewith a new declaration signed by the second named inventor, Ms. Asmita Saha. A copy of the originally filed declaration, which is signed by the first named inventor, Mr. James A. Cooper, is also included for the convenience of the Office.

SECTION 102(e) REJECTION OF INDEPENDENT CLAIM 1

The Examiner rejected independent claim 1 under 35 U.S.C. §102(e) as being anticipated by U.S. Patent Publication No. 2003/0227052 A1 to Ono et al. (hereinafter "Ono"). This claim has been amended to include the subject matter of dependent claims 2 and 6. Claims 2 and 6 have been cancelled. Regarding claim 2, the Examiner rejected this claim under 35 U.S.C. §103(a) as being unpatentable over Ono in view of U.S. Patent No. 6,573,534 B1 to Kumar et al. (hereinafter "Kumar"). Regarding claim 6, the Examiner rejected this claim under 35 U.S.C. §103(a) as being unpatentable over Ono in view of U.S. Patent No. 6,137,139 to Zeng et al. (hereinafter "Zeng").

The Combination of Ono, Kumar, and/or Zeng fails to Render Amended Claim 1
Obvious

Claim 1 has been amended to recite “a silicone-carbide substrate having a first concentration of first type impurities” and “a current spreading semiconductor layer formed on a front side of the drift semiconductor layer.” In forming the rejection of claim 1, the Examiner bases his rejection on Ono, but concedes that “Ono does not disclose that the semiconductor substrate is a silicon-carbide substrate.” The Examiner relies on Kumar to overcome this deficiency of Ono. The Examiner asserts:

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Ono by using a silicon-carbide substrate for advantages such as higher breakdown voltage and lower ON resistance according to the teachings of Kumar (Column 1, lines 27-30). 4/4/2007 Office Action, Paragraph 11, Page 5.

Applicants strongly disagree. As noted by the Examiner, Ono and Zeng are directed toward MOSFET devices having silicon substrates, while Kumar is directed toward silicon-carbide MOSFET devices. Although the Examiner asserts that modifying Ono to include a silicon-carbide is an obvious modification, such an assertion ignores the technical aspects of silicon-carbide MOSFET devices. Silicon-carbide MOSFET devices are often used for high-power applications. In such applications, a high blocking voltage is desirable. For example, Kumar teaches:

It is an object of the present invention to provide a SiC MOS transistor which makes full use of the characteristics of SiC in order to obtain even lower ON resistance and *higher breakdown voltage* than conventional SiC MOS transistors. Kumar, Col 1, ll. 31-35, emphasis added.

Unlike silicon MOSFET devices, the blocking voltage of silicon-carbide MOSFET devices is limited by gate oxide failure rather than semiconductor breakdown. Gate oxide failure can be caused by the magnetic field of the gate oxide having an excessive strength. As noted in Paragraph [0028] of Applicants' present patent application, the use of a JFET region and/or a current spreading layer in a silicon-carbide substrate reduces the blocking voltage of the

device due to an increased strength of the gate oxide magnetic field. As such, it would not be obvious to one of ordinary skill in the art to use the features of Ono or Zeng with a silicon-carbide substrate because such features would reduce the blocking voltage of the device and likely render the device inoperable for its intended purpose (i.e., high power applications). Thus, it is clear that no one of ordinary skill in the art would combine Ono or Zeng with Kumar in the manner proposed by the Examiner. As such, amended claim 1 is believed to be in condition for allowance and such action is respectfully requested.

Discussion Re: Claims 3-4 and 7-11

Claims 3-4 and 7-11 include claim 1 as a base claim. As such, the rejection of claims 3-4 and 7-11 should be withdrawn for the reasons hereinbefore discussed with regard to amended claim 1. In light of the reasons for withdrawal of the rejection of claim 1, any arguments specific to claims 3-4 and 7-11 are held in abeyance without prejudice or admission to any assertion made by the Examiner in order to expedite prosecution. Claims 7 and 9 have been amended for consistency.

SECTION 102(e) REJECTION OF INDEPENDENT CLAIM 12

The Examiner rejected independent claim 12 under 35 U.S.C. §102(e) as being anticipated by Ono. Claim 12 has been amended to recite:

12. A double-implanted metal-oxide semiconductor field-effect transistor comprising:
a silicone-carbide substrate;
a drift semiconductor layer formed on a front side of the semiconductor substrate;
a first source region;
a plurality of first base contact regions defined in the first source region, each of the plurality of first base contact regions being spaced apart from each other;
a second source region;
a plurality of second base contact regions defined in the second source region, each of the plurality of second base contact regions being spaced apart from each other; and

a JFET region defined between the first source region and the second source region, the JFET region having a width less than about three micrometers.

Anticipation exists only if all the elements of the claimed invention are present in a product or process disclosed, expressly or inherently, in a single prior art reference. *Hazeltine Corp. v. RCA Corp.*, 468 U.S. 1228 (1984). Ono fails to disclose or teach each and every element of amended claim 12. Accordingly, amended claim 12 is believed to be in condition for allowance and such action is respectfully requested.

Discussion Re: Claims 13 and 14

Claims 13 and 14 include claim 12 as a base claim. As such, the rejection of claims 13 and 14 should be withdrawn for the reasons hereinbefore discussed with regard to amended claim 12. In light of the reasons for withdrawal of the rejection of claim 12, any arguments specific to claims 13 and 14 are held in abeyance without prejudice or admission to any assertion made by the Examiner in order to expedite prosecution.

SECTION 103(a) REJECTION OF INDEPENDENT CLAIM 17

The Examiner rejected claim 17 under 35 U.S.C. §103(a) as being unpatentable over Ono in view of Zeng. Claim 17 has been amended to include the subject matter of claim 22. In regard to claim 22, the Examiner rejected this claim under 35 U.S.C. §103(a) as being unpatentable over Ono in view of Zeng and further in view of U.S. Patent Publication Serial No. 2003/0052329 to Kobayashi et al. (hereinafter "Kobayashi"). In support of this rejection, the Examiner asserts that:

Kobayashi shows (Fig 18) a plurality of source regions and a plurality of base contact regions, wherein the plurality of base contact regions (13), form alternating strips of N-type doped regions and P-type doped regions, *the alternating strips (17) being substantially orthogonal to respective source electrodes formed over the first and second source regions.* 4/4/2007 Office Action, Paragraph 37, Page 10, emphasis added.

Applicants disagree. First, reference numeral 13 of Kobayashi points to a well region (13) and reference numeral 17 of Kobayashi points to a gate insulation film (17). Applicants assume the Examiner meant to refer to the contact region 21 and the source region 15 of Kobayashi, respectively. Regardless, Kobayashi simply fails to teach such a configuration. Rather, it is clear from a review of FIGS. 17 and 18 of Kobayashi that the source electrode 19 (see FIG. 17) is oriented in a **parallel configuration** (i.e., non-orthogonal) relative to the source region 15 and the contact region 21. Therefore, for at least this reason, the combination of Ono, Zeng, and Kobayashi fails to render amended claim 17 obvious. As such, claim 17 is believed to be in condition for allowance and such action is respectfully requested.

Discussion Re: Claims 18-20

Claims 18-20 include claim 17 as a base claim. As such, the rejection of claims 18-20 should be withdrawn for the reasons hereinbefore discussed with regard to amended claim 17. In light of the reasons for withdrawal of the rejection of claim 17, any arguments specific to claims 18-20 are held in abeyance without prejudice or admission to any assertion made by the Examiner in order to expedite prosecution.

SECTION 103(a) REJECTION OF INDEPENDENT CLAIM 23

The Examiner rejected claim 32 under 35 U.S.C. §103(a) as being unpatentable over Ono in view of Zeng in further view of Tokura and in further view of Kumar. In forming this rejection, the Examiner concedes that "Ono does not disclose that the semiconductor substrate is silicon-carbide." The Examiner again relies on Kumar to overcome this deficiency of Ono. The Examiner asserts:

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Ono by using a silicon-carbide substrate for advantages such as higher breakdown voltage and lower ON resistance according to the teachings of Kumar. 4/4/2007 Office Action, Page 13-14, Paragraph 50.

However, for all of the reasons provided above in regard to independent claim 1, it would not be obvious to one of ordinary skill to modify the teaching of Ono in the manner suggested by the Examiner. For at last this reason, the combination of Ono, Zeng, Tokura, and Kumar fails to render claim 23 obvious. As such, claim 23 is believed to be in condition for allowance and such action is respectfully requested.

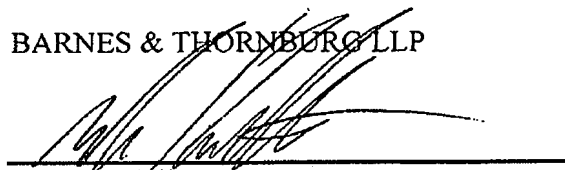
CONCLUSION

In view of the foregoing, it is submitted that this application is in a condition for allowance. Action to that end is hereby solicited. If there are any questions or comments that would speed prosecution of this application, the Examiner is invited to call the undersigned at (317) 261-7959.

It is respectfully requested that this paper be considered as a petition for a two-month extension of time extending the deadline of this response to August 4, 2007. The Commissioner is hereby authorized to charge the fee of \$450.00 for this two-month extension of time, and any shortages or overpayments of fees, to the Account of Barnes & Thornburg, Deposit Account No. 10-0435 with reference to file 3220-79132.

Respectfully submitted,

BARNES & THORNBURG LLP



Glen M. Kellett
Registration No. 60,202
Barnes & Thornburg
11 South Meridian Street
Indianapolis, Indiana 46204-3535
Telephone: (317) 261-7959
Fax: (317) 231-7433

INDS02 GKELLETT 911490v1

AUG 06 2007

Express Mail Label No.

Page 1 of 2

Docket No.
3220-79132

Declaration For Patent Application

English Language Declaration

As a below named inventor, I hereby declare that:

My residence, post office address and citizenship are as stated below next to my name,

I believe I am the original, first and sole inventor (if only one name is listed below) or an original, first and joint inventor (if plural names are listed below) of the subject matter which is claimed and for which a patent is sought on the invention entitled

HIGH-VOLTAGE POWER SEMICONDUCTOR DEVICE

the specification of which

(check one)

☐ Is attached hereto.

☒ was filed on January 23, 2006 as United States Application No. or PCT International Application Number 11/338,007 and was amended on _____

(if applicable)

I hereby state that I have reviewed and understand the contents of the above identified specification, including the claims, as amended by any amendment referred to above.

I acknowledge the duty to disclose information which is material to patentability as defined in 37 CFR 1.56, including for continuation-in-part applications, material information which became available between the filing date of the prior applications and the national or PCT International filing date of the continuation-in-part application.

I hereby claim foreign priority benefits under 35 U.S.C. 119(a)-(d) or (f), or 365(b) of any foreign application(s) for patent, inventor's or plant breeder's rights certificate(s), or 365(a) of any PCT International application which designated at least one country other than the United States of America, listed below and have also identified below, by checking the box, any foreign application for patent or inventor's or plant breeder's rights certificate(s), or any PCT international application having a filing date before that of the application on which priority is claimed.

Prior Foreign Application(s)

Priority Claimed

(Number) _____ (Country) _____ (Day/Month/Year Filed) _____

☐

(Number) _____ (Country) _____ (Day/Month/Year Filed) _____

☐

(Number) _____ (Country) _____ (Day/Month/Year Filed) _____

☐

Page 3 of 3

Full name of sole or first inventor James A. Cooper	Date
Sole or first inventor's signature	
Residence 511 Kerber Road, West Lafayette, IN 47906-9433	
Citizenship USA	
Post Office Address 511 Kerber Road, West Lafayette, IN 47906-9433	

Full name of second inventor, if any Asmita Saha	Date
Second inventor's signature <i>Asmita Saha</i>	08/03/07
Residence 7162, NE Rontler Way, Ap # 2522, Hillsboro, OR 97124	
Citizenship INDIAN	
Post Office Address 7162, NE Rontler Way, Ap # 2522, Hillsboro, OR 97124	

Full name of third inventor, if any	Date
Third inventor's signature	
Residence	
Citizenship	
Post Office Address	

Full name of fourth inventor, if any	Date
Fourth inventor's signature	
Residence	
Citizenship	
Post Office Address	

Express Mail Label No.

Page 1 of 3

Docket No.
3220-79132

Declaration For Patent Application

English Language Declaration

As a below named inventor, I hereby declare that:

My residence, post office address and citizenship are as stated below next to my name,

I believe I am the original, first and sole inventor (if only one name is listed below) or an original, first and joint inventor (if plural names are listed below) of the subject matter which is claimed and for which a patent is sought on the invention entitled

HIGH-VOLTAGE POWER SEMICONDUCTOR DEVICE

the specification of which

(check one)

☐ is attached hereto.

☒ was filed on January 23, 2006 as United States Application No. or PCT International

Application Number 11/338,007

and was amended on _____

(if applicable)

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I hereby claim foreign priority benefits under 35 U.S.C. 119(a)-(d) or (f), or 365(b) of any foreign application(s) for patent, inventor's or plant breeder's rights certificate(s), or 365(a) of any PCT International application which designated at least one country other than the United States of America, listed below and have also identified below, by checking the box, any foreign application for patent or inventor's or plant breeder's rights certificate(s), or any PCT international application having a filing date before that of the application on which priority is claimed.

Prior Foreign Application(s)

Priority Claimed

_____ (Number)	_____ (Country)	_____ (Day/Month/Year Filed)	<input type="checkbox"/>
_____ (Number)	_____ (Country)	_____ (Day/Month/Year Filed)	<input type="checkbox"/>
_____ (Number)	_____ (Country)	_____ (Day/Month/Year Filed)	<input type="checkbox"/>

I hereby claim the benefit under 35 U.S.C. Section 119(e) of any United States provisional application(s) listed below:

<u>60/646,152</u>	<u>1/21/05</u>
(Application Serial No.)	(Filing Date)

(Application Serial No.)	(Filing Date)
--------------------------	---------------

(Application Serial No.) _____ (Filing Date) _____

I hereby claim the benefit under 35 U. S. C. Section 120 of any United States application(s), or Section 365(c) of any PCT International application designating the United States, listed below and, insofar as the subject matter of each of the claims of this application is not disclosed in the prior United States or PCT International application in the manner provided by the first paragraph of 35 U.S.C. Section 112, I acknowledge the duty to disclose to the United States Patent and Trademark Office all information known to me to be material to patentability as defined in Title 37, CFR Section 1.56 which became available between the filing date of the prior application and the national or PCT International filing date of this application:

(Application Serial No.)	(Filing Date)	(Status) (patented, pending, abandoned)

(Application Serial No.)	(Filing Date)	(Status) (patented, pending, abandoned)
--------------------------	---------------	--

(Application Serial No.)	(Filing Date)	(Status) (patented, pending, abandoned)
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I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code and that such willful false statements may jeopardize the validity of the application or any patent issued thereon.

Page 3 of 3

Full name of sole or first inventor James A. Cooper	Date 5-2-06
Sole or first inventor's signature <i>James A. Cooper</i>	
Residence 511 Kerber Road, West Lafayette, IN 47906-9433	
Citizenship USA	
Post Office Address 511 Kerber Road, West Lafayette, IN 47906-9433	

Full name of second inventor, if any Asmita Saha	Date
Second inventor's signature 411, NORTH SALISBURY ST. AP A, WEST LAFAYETTE, IN 47906	
Residence INDIAN	
Citizenship 411, NORTH SALISBURY ST. AP A, WEST LAFAYETTE, IN 47906	
Post Office Address	

Full name of third inventor, if any	Date
Third inventor's signature	
Residence	
Citizenship	
Post Office Address	

Full name of fourth inventor, if any	Date
Fourth inventor's signature	
Residence	
Citizenship	
Post Office Address	

AUG 6 - 2007

BARNES & THORNBURG LLP

btlaw.com

11 South Meridian Street
Indianapolis, Indiana 46204-3535
(317) 236-1313

Fax Number: (317) 231-7433

FAX COVER SHEET

NAME	COMPANY NAME	TELECOPY NO.
TO: Commissioner for Patents	U.S. Patent and Trademark Office	(571) 273-8300

FROM: Glen M. Kellett

DIRECT DIAL: (317) 261-7959

E-MAIL: gkellett@btlaw.com

DATE: August 8, 2007

TIME SENDING: _____

NUMBER OF PAGES (INCLUDING THIS COVER SHEET): 20If you have difficulty receiving this Fax, please call Barnes & Thornburg at 317-231-7557 and ask for Cortney Drew

Faxed: August 8, 2007
Applicant: James A. Cooper
Invention: **HIGH-VOLTAGE POWER SEMICONDUCTOR DEVICE**
Serial No.: 11/338,007
Filed: January 23, 2006
Docket: 3220-79132

☒ Response to Office Action (13 pages)
☒ Declaration signed by Inventor Asmita Saha (3 pages)
☒ Copy of Declaration signed by Inventor James A. Cooper (3 pages)

Response once received:

CLIENT# 3220
MATTER# 79131

☐ Original to follow by mail
☒ Original will not follow by mail

CONFIDENTIALITY NOTICE: This message is for the exclusive use of the individual or entity to which it is addressed and is confidential. If you are not the addressee or an employee or agent of the addressee responsible for delivering it to the addressee, please do not read, use, disclose, copy or distribute this message and do not take any action in reliance upon it. If you have received this message in error, please notify us immediately by telephone (collect) to arrange for its return. We do not intend to waive any attorney-client or work product privilege by the transmission of this message.

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Route to: Cortney Drew

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United States Patent and Trademark Office
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PATENT APPLICATION FEE DETERMINATION RECORD

Substitute for Form PTO-975 Effective December 8, 2004

Application or Docket Number

11338007

APPLICATION AS FILED - PART I

(Column 1)

(Column 2)

SMALL ENTITY

OR

OTHER THAN SMALL ENTITY

FOR	NUMBER FILED	NUMBER EXTRA
BASIC FEE (37 CFR 1.16(a), (b), or (c))	N/A	N/A
SEARCH FEE (37 CFR 1.16(d), (e), or (f))	N/A	N/A
EXAMINATION FEE (37 CFR 1.16(g), (h), or (i))	N/A	N/A
TOTAL CLAIMS (37 CFR 1.16(j))	23 minus 20 =	3
INDEPENDENT CLAIMS (37 CFR 1.16(k))	4 minus 3 =	1
APPLICATION SIZE FEE (37 CFR 1.16(l))	If the specification and drawings exceed 100 sheets of paper, the application size fee due is \$250 (\$125 for small entity) for each additional 50 sheets or fraction thereof. See 35 U.S.C. 41(a)(1)(G) and 37 CFR 1.16(s).	
MULTIPLE DEPENDENT CLAIM PRESENT (37 CFR 1.16(m))		

RATE (\$)	FEE (\$)
N/A	150.00
N/A	\$250
N/A	\$100
X\$ 25 =	
X100 =	
+180=	
TOTAL	

RATE (\$)	FEE (\$)
N/A	300.00
N/A	\$500
N/A	\$200
X\$50 =	150
X200 =	200
+360=	
TOTAL	1350

* If the difference in column 1 is less than zero, enter "0" in column 2.

APPLICATION AS AMENDED - PART II

(Column 1)

(Column 2)

(Column 3)

SMALL ENTITY

OR

OTHER THAN SMALL ENTITY

AMENDMENT A	CLAIMS REMAINING AFTER AMENDMENT	HIGHEST NUMBER PREVIOUSLY PAID FOR	PRESENT EXTRA
Total (37 CFR 1.16(j))	23	23	
Independent (37 CFR 1.16(k))	4	4	
Application Size Fee (37 CFR 1.16(s))			
FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(m))			

RATE (\$)	ADDITIONAL FEE (\$)
X\$ 25 =	
X100 =	
+180=	
TOTAL ADD'L FEE	

RATE (\$)	ADDITIONAL FEE (\$)
X\$50 =	
X200 =	
+360=	
TOTAL ADD'L FEE	

8-6-07

(Column 1)

(Column 2)

(Column 3)

AMENDMENT B	CLAIMS REMAINING AFTER AMENDMENT	HIGHEST NUMBER PREVIOUSLY PAID FOR	PRESENT EXTRA
Total (37 CFR 1.16(j))	17	23	
Independent (37 CFR 1.16(k))	4	4	
Application Size Fee (37 CFR 1.16(s))			
FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(m))			

RATE (\$)	ADDITIONAL FEE (\$)
X\$ 25 =	
X100 =	
+180=	
TOTAL ADD'L FEE	

RATE (\$)	ADDITIONAL FEE (\$)
X\$50 =	
X200 =	
+360=	
TOTAL ADD'L FEE	

* If the entry in column 1 is less than the entry in column 2, write "0" in column 3.

** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 20, enter "20".

*** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 3, enter "3".

The "Highest Number Previously Paid For" (Total or Independent) is the highest number found in the appropriate box in column 1.

This collection of information is required by 37 CFR 1.16. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 12 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.

If you need assistance in completing the form, call 1-800-PTO-9199 and select option 2.

EAST Search History

Ref #	Hits	Search Query	DBs	Default Operator	Plurals	Time Stamp
S1	1393	((Cooper near (James J)) (Saha near (Asmita A))).in.	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2007/03/22 10:54
S2	380394	"257".clas.	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2007/03/22 09:01
S3	7	S1 and S2	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2007/03/22 09:01
S4	4717	((257/263) or (257/256) or (257/341) or (257/342) or (257/335) or (257/339) or (257/350)).CCLS.	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2007/03/22 10:55
S5	3327	((438/142) or (438/156) or (438/176) or (438/186) or (438/197) or (438/268)).CCLS.	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2007/03/22 10:56
S6	7886	S4 S5	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2007/03/22 11:03
S7	156976	MOSFET ("metal oxide semiconductor")	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2007/03/22 11:04
S8	5305	DMOS	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2007/03/22 11:04

EAST Search History

S9	304	Double adj implant	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2007/03/22 11:04
S10	57449	power same (FET "Field effect")	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2007/03/22 11:06
S11	8478	JFET ("Junction Field Effect")	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2007/03/22 11:07
S12	3533	current near spread\$3	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2007/03/23 10:28
S13	10361	Drift near5 (layer region)	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2007/03/22 11:10
S14	0	S6 and S7 and S9 and S10 and S11 and S12 and S13	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2007/03/22 11:12
S15	20	S7 and S12 and S13 and S6	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2007/03/22 11:13
S16	80	S7 and S12 and S13	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2007/03/22 11:34

EAST Search History

S17	0	S16 and S9	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2007/03/22 11:14
S18	180117	siC (Silicon adj carbide)	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2007/03/22 11:35
S19	548	S11 and S13 and S7	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2007/03/22 14:11
S20	202	S19 and S6	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2007/03/23 12:53
S21	1125	257/341.ccls.	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2007/03/22 15:36
S22	145	S21 and S11	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2007/03/22 15:36
S23	16	S21 and S12	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2007/03/22 15:58
S24	49	S6 and S12	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2007/03/22 16:11

EAST Search History

S25	628	S6 and S18	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2007/03/22 16:12
S26	92	S21 and S18	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2007/03/22 16:12
S27	1121	current near spread\$3 near5 layer	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2007/03/23 10:29
S28	1125	257/341.ccls.	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2007/03/23 10:29
S29	6	S27 and S28	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2007/03/23 10:32
S30	4717	((257/263) or (257/256) or (257/341) or (257/342) or (257/335) or (257/339) or (257/350)).CCLS.	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2007/03/23 10:32
S31	3327	((438/142) or (438/156) or (438/176) or (438/186) or (438/197) or (438/268)).CCLS.	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2007/03/23 10:32
S32	7886	S30 S31	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2007/03/23 10:32

EAST Search History

S33	12	S27 and S32	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2007/03/23 10:32
S34	156976	MOSFET ("metal oxide semiconductor")	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2007/03/23 12:47
S35	8478	JFET ("Junction Field Effect")	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2007/03/23 12:47
S36	10361	Drift near5 (layer region)	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2007/03/23 12:47
S37	548	S35 and S36 and S34	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2007/03/23 12:47
S38	202	S37 and S32	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2007/03/23 12:47
S39	195	S38 and dop\$3	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2007/03/23 14:03
S40	187432	S34 amd S36 and (dop\$3 concentrat\$3 dos\$3)	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2007/03/23 14:06

EAST Search History

S41	4013	S40 and S32	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2007/03/23 14:07
S42	436	S41 and S35	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2007/03/23 15:25
S43	4	S42 and S27	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2007/03/23 15:25
S44	5	S42 and current near5 spread	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2007/03/23 15:27
S45	36	S41 and current near5 spread	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2007/03/26 08:21
S46	2	("5688725").PN.	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2007/03/23 15:50
S47	5	("4941026" "5341011" "5424231" "5532179" "5558313").PN.	US-PGPUB; USPAT; USOCR	OR	ON	2007/03/26 08:12
S48	2	("4941026").PN.	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2007/03/26 08:12
S49	4717	((257/263) or (257/256) or (257/341) or (257/342) or (257/335) or (257/339) or (257/350)).CCLS.	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2007/03/26 08:21

EAST Search History

S50	3327	((438/142) or (438/156) or (438/176) or (438/186) or (438/197) or (438/268)).CCLS.	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2007/03/26 08:21
S51	7886	S49 S50	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2007/03/26 08:21
S52	157110	MOSFET ("metal oxide semiconductor")	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2007/03/26 08:21
S53	10368	Drift near5 (layer region)	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2007/03/26 08:21
S54	187573	S52 amd S53 and (dop\$3 concentrat\$3 dos\$3)	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2007/03/26 08:21
S55	4013	S54 and S51	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2007/03/26 08:21
S56	72	S55 and current near5 spread\$3	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2007/03/26 08:22



UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
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Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
11/338,007	01/23/2006	James A. Cooper	3220-79132	4085

23643 7590 10/12/2007
BARNES & THORNBURG LLP
11 SOUTH MERIDIAN
INDIANAPOLIS, IN 46204

EXAMINER

PATTON, PAUL E

ART UNIT	PAPER NUMBER
----------	--------------

2822

MAIL DATE	DELIVERY MODE
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10/12/2007

PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No. 11/338,007	Applicant(s) COOPER ET AL.	
	Examiner Paul E. Patton	Art Unit 2822	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 06 August 2007.
- 2a) ☒ This action is **FINAL**. 2b) ☐ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1,3-5,7-14,17-20 and 23 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 1,3-5,7-14,17-20 and 23 is/are rejected.
- 7) ☐ Claim(s) _____ is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on _____ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some * c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. _____.
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- | | |
|--|---|
| 1) <input checked="" type="checkbox"/> Notice of References Cited (PTO-892) | 4) <input type="checkbox"/> Interview Summary (PTO-413)
Paper No(s)/Mail Date. _____ |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948) | 5) <input type="checkbox"/> Notice of Informal Patent Application |
| 3) <input type="checkbox"/> Information Disclosure Statement(s) (PTO/SB/08)
Paper No(s)/Mail Date _____ | 6) <input type="checkbox"/> Other: _____ |

DETAILED ACTION

Amendment

1. Acknowledgement is made of Amendment filed August 6, 2007

Claim Objections

2. Claims 1 and 12 are objected to because of the following informalities: The claims refer to "a silicone-carbide substrate" which should read – a silicon-carbide substrate—.

Appropriate correction is required.

Claim Rejections - 35 USC § 103

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

2. Claims 1, 3, 4, 7 – 10, 12, and 13 are rejected under 35 U.S.C. 103(a) as being unpatentable over Ono et al., (US 2003/0227052 A1) Ono in view of Kumar et al., (USPAT 6,573,534.B1) Kumar and further in view of Zeng et al., (USPAT 6,137,139) Zeng.

3. As to claims 1,3,4,9,12, and 13, Ono discloses and shows (Fig 1), a double implanted MOS field effect transistor comprising a semiconductor substrate (10) having a first concentration of first type impurities (n+); a drift semiconductor layer (50) formed on a front side of the semiconductor substrate and having a second concentration of first type impurities less than the first concentration of first type impurities (n-); a first

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source region (20); a second source region (20); and a JFET region (40) defined between the first source region and the second source region, the JFET region having a third concentration of first type impurities that is greater than the second concentration of first type impurities (n) and having a width (L) less than about 3 micrometers and a width of about one micrometer. (Paragraphs [0039] & [0041]).

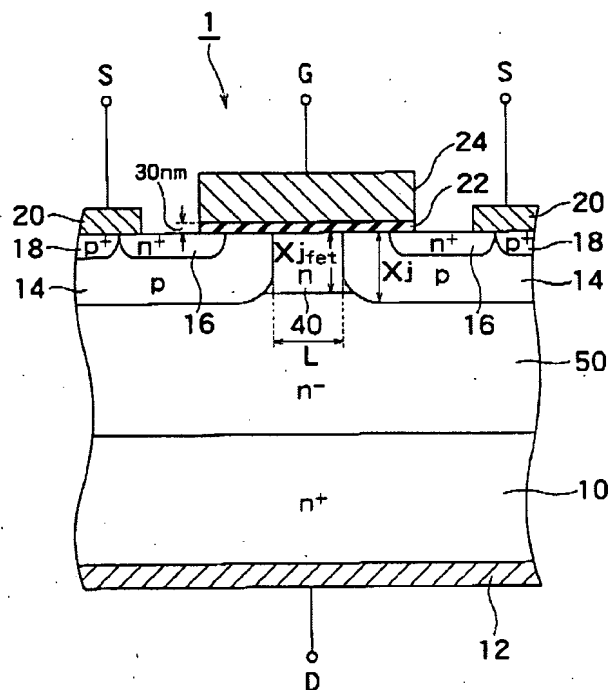


FIG. 1

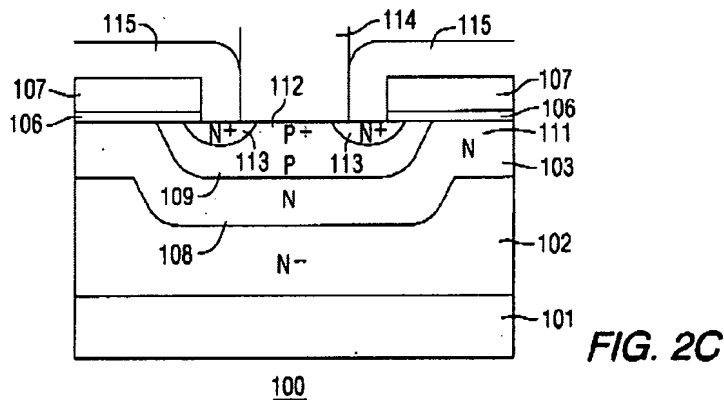
4. Ono does not disclose that the semiconductor substrate is a silicon-carbide substrate.
5. Kumar is related to a similar MOS FET structure and discloses that the substrate is a silicon-carbide substrate (Column 1, line 40).
6. Kumar is evidence that a person of ordinary skill in the art would find a reason, suggestion or motivation to use a silicon-carbide substrate.

7. Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Ono by using a silicon-carbide substrate for advantages such as higher breakdown voltage and lower ON resistance according to the teachings of Kumar (Column 1, lines 27-30).

8. Ono shows (Ono, Fig 1) the JFET region is formed directly below the gate structure and between the base doped wells formed on either side of the gate. As noted above the parasitic JFET is a consequence of the lateral gate-source arrangement of a vertical MOSFET and would be above the current spreading layer and the drift region shown by Zeng.

9. Ono as modified by Kumar does not explicitly disclose that a current spreading layer is formed on a front side of the drift semiconductor layer; and wherein the concentration of impurities of the first type is greater than the concentration of impurities of the first type in the drift region by at least one order of magnitude.

10. Zeng discloses and shows (Fig 2C) a current spreading layer (103) formed on a front side of the drift semiconductor layer (102) wherein the concentration of impurities of the first type is greater than the concentration of impurities of the first type in the drift region by at least one order of magnitude (Zeng, Column 2, lines 64-67 & Column 3, lines 4-7).



11. Zeng is evidence that a person of ordinary skill in the art would find a reason, suggestion or motivation to have a current spreading layer formed on a front side of the drift semiconductor layer; and wherein the concentration of impurities of the first type is greater than the concentration of impurities of the first type in the drift region by at least one order of magnitude.

12. Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Ono to have a current spreading layer formed on a front side of the drift semiconductor layer; and wherein the concentration of impurities of the first type is greater than the concentration of impurities of the first type in the drift region by at least one order of magnitude for advantages such as reduced on-resistance without degrading device ruggedness and reliability according to the teachings of Zeng (Column 4, lines 32-39).

13. As to claims 7 and 8, Ono as modified by Kumar and Zeng discloses and shows (Fig 2C) a current spreading layer (103) formed on a front side of the drift semiconductor layer (102) wherein the concentration of impurities of the first type is

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greater than the concentration of impurities of the first type in the drift region by at least one order of magnitude (Zeng, Column 2, lines 64-67 & Column 3, lines 4-7).

14. As to claim 10, Ono as modified by Kumar and Zeng shows (Ono, Fig 12) a plurality of base contact regions (18) formed in each of the first and second source regions (16), the base contact regions being smaller than the first and second source regions.

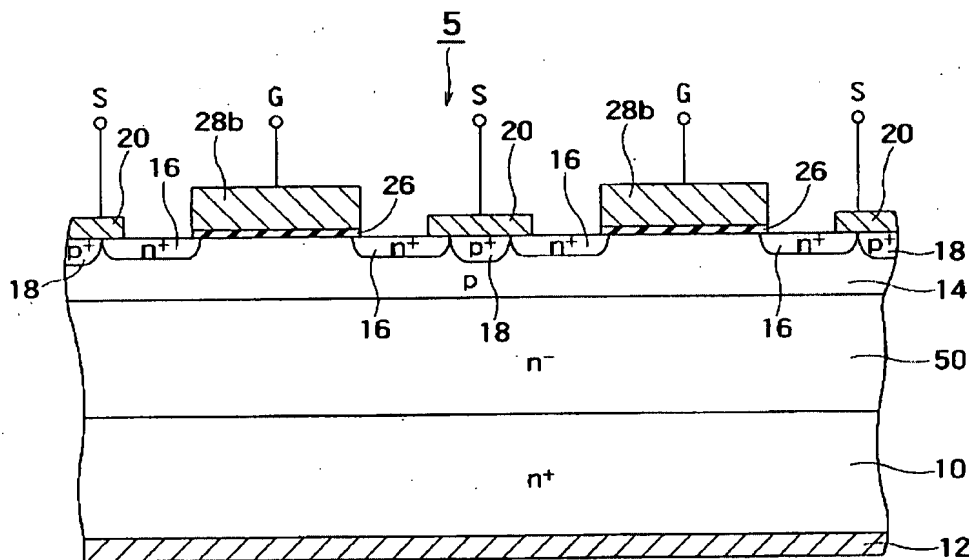


FIG. 12

15. Claims 11, and 17-20 are rejected under 35 U.S.C. 103(a) as being unpatentable over Ono in view of Kumar and Zeng and further in view of Kobayashi et al., (US2003/0052329 A1) Kobayashi.

16. As to claim 11, Ono as modified by Kumar and Zeng does not explicitly disclose a plurality of source regions and a plurality of base contact regions, wherein the plurality of source regions and the plurality of base contact regions, form alternating strips of N-

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type doped regions and P-type doped regions, the alternating strips being substantially orthogonal to respective source electrodes formed over the first and second source regions.

17. Kobayashi shows (Fig 18) a plurality of source regions and a plurality of base contact regions, wherein the plurality of source regions (15) and the plurality of base contact regions (21), form alternating strips of N-type doped regions and P-type doped regions, the alternating strips (17) being substantially orthogonal to respective source electrodes formed over the first and second source regions.

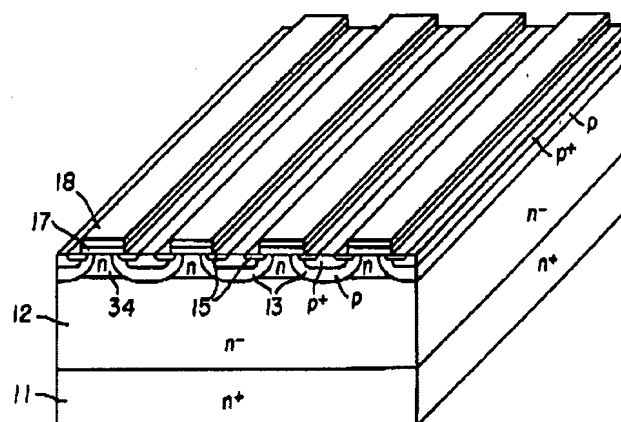


FIG. 18

18. Kobayashi is evidence that a person of ordinary skill in the art would find a reason, suggestion or motivation to form a plurality of source regions and a plurality of base contact regions, wherein the plurality of source regions and the plurality of base contact regions, form alternating strips of N-type doped regions and P-type doped regions, the alternating strips being substantially orthogonal to respective source electrodes formed over the first and second source regions.

19. Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Ono, Kumar and Zeng to form a plurality of source regions and a plurality of base contact regions, wherein the plurality of source regions and the plurality of base contact regions, form alternating strips of N-type doped regions and P-type doped regions, the alternating strips being substantially orthogonal to respective source electrodes formed over the first and second source regions for advantages such as reduced electric field strength according to the teachings of Kobayashi (Paragraph [0034]).

20. As to claim 17, Ono as modified by Kumar, Zeng and Kobayashi discloses and shows (Ono, Fig 1), a double implanted MOS field effect transistor comprising a semiconductor substrate (10) a drift semiconductor layer (50) formed on a front side of the semiconductor substrate; a first source region (20); a second source region (20); and a JFET. Further, Zeng discloses and shows (Fig 2C) a current spreading layer (103) formed on a front side of the drift semiconductor layer (102). Ono shows (Ono, Fig 1) the JFET region is formed directly below the gate structure and between the base doped wells formed on either side of the gate. As noted above the parasitic JFET is a consequence of the lateral gate-source arrangement of a vertical MOSFET and would be above the current spreading layer and the drift region shown by Zeng. Further, Kobayashi shows (Fig 18) a plurality of source regions and a plurality of base contact regions, wherein the plurality of source regions (15) and the plurality of base contact regions (21), form alternating strips of N-type doped regions and P-type doped regions,

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the alternating strips (17) being substantially orthogonal to respective source electrodes formed over the first and second source regions.

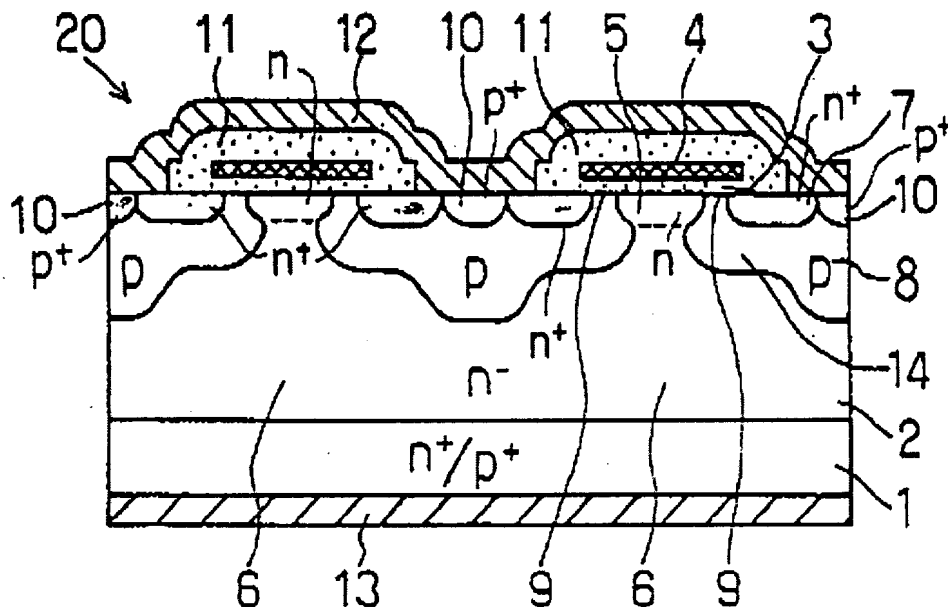
21. As to claims 18 and 19, Ono as modified by Kumar, Zeng and Kobayashi discloses a current spreading layer wherein the concentration of impurities of the first type is greater than the concentration of impurities of the first type in the drift region by at least one order of magnitude (Zeng, Column 2, lines 64-67 & Column 3, lines 4-7).

22. As to claim 20, Ono as modified by Kumar, Zeng and Kobayashi discloses the JFET region has a width of about three micrometers or less (Ono, Paragraph [0041]).

23. Claims 5, 14 and 23 are rejected under 35 U.S.C. 103(a) as being unpatentable over Ono in view of Kumar and Zeng and further in view of Tokura et al., (USPAT 5,545,908).

24. Ono as modified by Kumar and Zeng does not disclose that the concentration of first type impurities associated with the JFET region is at least one order of magnitude greater than the concentration of first type impurities associated with the drift region.

25. Tokura is related to a similar MOSFET structure and discloses and shows (Tokura, Fig 1) that the doping level at the JFET region (5) is $8 \times 10^{16} \text{ cm}^{-3}$ whereas the doping level of the drift region (2) is $5 \times 10^{15} \text{ cm}^{-3}$. (Tokura, Column 10, lines 29-33 & Column 11, lines 54-58). Note that Tokura does not label the region between the two p doped wells on opposite sides of the gate as a JFET. However the structure in this device as well as Ono will form a parasitic JFET due to the arrangement of the layers. (Ono, Paragraph [0040]).



Tokura, Fig 1

26. Tokura is evidence that a person of ordinary skill in the art would find a reason, suggestion or motivation to have the concentration of the JFET region at least an order of magnitude greater than the concentration of the drift region.

27. Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Ono by having the concentration of the JFET region at least an order of magnitude greater than the concentration of the drift region for advantages such as reduced ON resistance according to the teachings of Tokura (Column 5, lines 60-66 & Column 8, lines 33-34).

28. As to claim 23, Ono as modified by Kumar, Zeng, and Tokura discloses and shows (Fig 1), a double implanted MOS field effect transistor comprising a semiconductor substrate (10) having a first concentration of first type impurities (n+); a

drift semiconductor layer (50) formed on a front side of the semiconductor substrate and having a second concentration of first type impurities less than the first concentration of first type impurities (n-); a first source region (20); a second source region (20); and a JFET region (40) defined between the first source region and the second source region, the JFET region having a fourth concentration of first type impurities that is greater than the second concentration of first type impurities (n) and having a width (L) less than about 3 micrometers and a width of about one micrometer. (Paragraphs [0039] & [0041]).

Kumar discloses that the substrate is a silicon-carbide substrate (Column 1, line 40). Zeng discloses and shows (Fig 2C) a current spreading layer (103) formed on a front side of the drift semiconductor layer (102) wherein the concentration of impurities of the first type is greater than the concentration of impurities of the first type in the drift region (Zeng, Column 2, lines 64-67 & Column 3, lines 4-7). Lastly, Tokura discloses and shows (Tokura, Fig 1) that the doping level at the JFET region (5) is $8E16 \text{ cm}^{-3}$ whereas the doping level of the drift region (2) is $5E15 \text{ cm}^{-3}$. (Tokura, Column 10, lines 29-33 & Column 11, lines 54-58). Note that Tokura does not label the region between the two p-doped wells on opposite sides of the gate as a JFET. However the structure in this device as well as Ono will form a parasitic JFET due to the arrangement of the layers. (Ono, Paragraph [0040]).

Response to Arguments

29. In regard to the discussion of claim 1 as amended, the applicant argues that the combination of Ono, Kumar and Zeng does not render claim 1 obvious. However, the

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argument seems to contradict the assertion in that forming a DMOS transistor using silicon carbide rather than silicon does, indeed, improve breakdown voltage and reduce ON resistance as is known in the art. In the instant case Ono and Zeng disclose the structure of the DMOS device and Kumar teaches the alternative of silicon-carbide with its known advantages. Hence, one of ordinary skill would indeed consider whether their particular problem would call for silicon-carbide.

30. It is further noted that applicant asserts that silicon-carbide devices are limited by gate oxide failure due to a magnetic field. This is a strange assertion, since it is very well known that the gate oxide would fail due to an electric field intensity not a magnetic field.

31. As to the discussion of the use of a current spreading layer, it is very well known in the art that current spreading layers are employed to counteract current "crowding" in DMOS devices which is a well known performance limiter and failure mode.

32. As to the discussion of claim 12, the same points that apply to claim 1 are relevant here as well. Claim 12 is obvious over the cited references.

33. As to claim 17, this claim is rejected on the same basis as before. While it is true that Kobayashi has a drawing with limited detail, The format claimed of the individual devices laid out in strips is very well known in the art for power transistors. Further, the source contacts would inherently be laid out orthogonal from the strip direction as can be also inferred from figure 12 of Tokura.

34. In like manner, claim 23 is obvious on the same basis as claim 1.

Conclusion

35. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire **THREE MONTHS** from the mailing date of this action. In the event a first reply is filed within **TWO MONTHS** of the mailing date of this final action and the advisory action is not mailed until after the end of the **THREE-MONTH** shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than **SIX MONTHS** from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Paul E. Patton whose telephone number is 571-272-9762. The examiner can normally be reached on 7:00 - 5:30 Monday through Thursday.

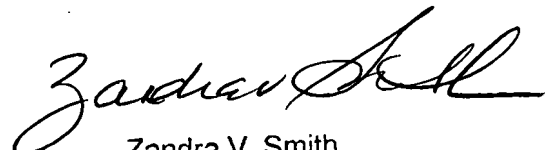
Art Unit: 2822

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Zandra Smith can be reached on 571-272-2429. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

Paul E Patton
Examiner
Art Unit 2822


PEP


Zandra V. Smith
Supervisory Patent Examiner
10 Oct. 2007

Notice of References Cited	Application/Control No. 11/338,007		Applicant(s)/Patent Under Reexamination COOPER ET AL.	
	Examiner Paul E. Patton		Art Unit 2822	Page 1 of 1

U.S. PATENT DOCUMENTS

*		Document Number Country Code-Number-Kind Code	Date MM-YYYY	Name	Classification
*	A	US-2003/0227052 A1	12-2003	Ono et al.	257/341
*	B	US-5,545,908	08-1996	Tokura et al.	257/341
*	C	US-6,573,534 B1	06-2003	Kumar et al.	257/77
*	D	US-2003/0052329 A1	03-2003	Kobayashi et al.	257/135
*	E	US-5,137,139	08-1992	Ruscello, Lorenzo	198/460.1
*	F	US-6,552,391 B2	04-2003	Zeng et al.	257/342
*	G	US-2003/0205829 A1	11-2003	Boden, Milton J. JR.	257/921
	H	US-			
	I	US-			
	J	US-			
	K	US-			
	L	US-			
	M	US-			


FOREIGN PATENT DOCUMENTS

*		Document Number Country Code-Number-Kind Code	Date MM-YYYY	Country	Name	Classification
	N					
	O					
	P					
	Q					
	R					
	S					
	T					

NON-PATENT DOCUMENTS

*		Include as applicable: Author, Title Date, Publisher, Edition or Volume, Pertinent Pages)
	U	
	V	
	W	
	X	

*A copy of this reference is not being furnished with this Office action. (See MPEP § 707.05(a).)
Dates in MM-YYYY format are publication dates. Classifications may be US or foreign.

Index of Claims 	Application/Control No. 11338007	Applicant(s)/Patent Under Reexamination COOPER ET AL.
	Examiner Patton, Paul E	Art Unit 2822


✓	Rejected
=	Allowed

-	Cancelled
÷	Restricted

N	Non-Elected
I	Interference

A	Appeal
O	Objected

<input type="checkbox"/> Claims renumbered in the same order as presented by applicant		<input type="checkbox"/> CPA		<input type="checkbox"/> T.D.		<input type="checkbox"/> R.1.47			
CLAIM		DATE							
Final	Original	03/26/2007	10/02/2007						
	1	✓	✓						
	2	✓	-						
	3	✓	✓						
	4	✓	✓						
	5	✓	✓						
	6	✓	-						
	7	✓	✓						
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	18	✓	✓						
	19	✓	✓						
	20	✓	✓						
	21	✓	-						
	22	✓	-						
	23	✓	✓						

Search Notes 	Application/Control No. 11338007	Applicant(s)/Patent Under Reexamination COOPER ET AL.
	Examiner Patton, Paul E	Art Unit 2822

SEARCHED			
Class	Subclass	Date	Examiner
257	263, 256, 341, 342, 335, 339, 350, 263,	3/22/2007	PEP
438	142, 156, 176, 186, 197, 268	3/22/2007	PEP

SEARCH NOTES		
Search Notes	Date	Examiner
Search history attached	2/26/2007	PEP
Updated Search	10/2/2007	PEP
Consult with M. Prenty	10/2/2007	PEP

INTERFERENCE SEARCH			
Class	Subclass	Date	Examiner

REQUEST FOR CONTINUED EXAMINATION(RCE)TRANSMITTAL (Submitted Only via EFS-Web)

Application Number	11/338,007	Filing Date	2006-01-23	Docket Number (if applicable)	3220-79132	Art Unit	2822
First Named Inventor	James A. Cooper			Examiner Name	Patton, Paul E.		

This is a Request for Continued Examination (RCE) under 37 CFR 1.114 of the above-identified application.

Request for Continued Examination (RCE) practice under 37 CFR 1.114 does not apply to any utility or plant application filed prior to June 8, 1995, or to any design application. The Instruction Sheet for this form is located at WWW.USPTO.GOV

SUBMISSION REQUIRED UNDER 37 CFR 1.114

Note: If the RCE is proper, any previously filed unentered amendments and amendments enclosed with the RCE will be entered in the order in which they were filed unless applicant instructs otherwise. If applicant does not wish to have any previously filed unentered amendment(s) entered, applicant must request non-entry of such amendment(s).

☐ Previously submitted. If a final Office action is outstanding, any amendments filed after the final Office action may be considered as a submission even if this box is not checked.

☐ Consider the arguments in the Appeal Brief or Reply Brief previously filed on _____

☐ Other _____

☒ Enclosed

☒ Amendment/Reply

☐ Information Disclosure Statement (IDS)

☐ Affidavit(s)/ Declaration(s)

☐ Other _____

MISCELLANEOUS

☐ Suspension of action on the above-identified application is requested under 37 CFR 1.103(c) for a period of months _____
(Period of suspension shall not exceed 3 months; Fee under 37 CFR 1.17(i) required)

☐ Other _____

FEES

The RCE fee under 37 CFR 1.17(e) is required by 37 CFR 1.114 when the RCE is filed.

☒ The Director is hereby authorized to charge any underpayment of fees, or credit any overpayments, to
Deposit Account No 100435

SIGNATURE OF APPLICANT, ATTORNEY, OR AGENT REQUIRED

☒ Patent Practitioner Signature

☐ Applicant Signature

Signature of Registered U.S. Patent Practitioner			
Signature	/Glen Kellett/	Date (YYYY-MM-DD)	2008-03-12
Name	Glen M. Kellett	Registration Number	60202

This collection of information is required by 37 CFR 1.114. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.11 and 1.14. This collection is estimated to take 12 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450.

If you need assistance in completing the form, call 1-800-PTO-9199 and select option 2.

Privacy Act Statement

The Privacy Act of 1974 (P.L. 93-579) requires that you be given certain information in connection with your submission of the attached form related to a patent application or patent. Accordingly, pursuant to the requirements of the Act, please be advised that: (1) the general authority for the collection of this information is 35 U.S.C. 2(b)(2); (2) furnishing of the information solicited is voluntary; and (3) the principal purpose for which the information is used by the U.S. Patent and Trademark Office is to process and/or examine your submission related to a patent application or patent. If you do not furnish the requested information, the U.S. Patent and Trademark Office may not be able to process and/or examine your submission, which may result in termination of proceedings or abandonment of the application or expiration of the patent.

The information provided by you in this form will be subject to the following routine uses:

1. The information on this form will be treated confidentially to the extent allowed under the Freedom of Information Act (5 U.S.C. 552) and the Privacy Act (5 U.S.C. 552a). Records from this system of records may be disclosed to the Department of Justice to determine whether the Freedom of Information Act requires disclosure of these records.
2. A record from this system of records may be disclosed, as a routine use, in the course of presenting evidence to a court, magistrate, or administrative tribunal, including disclosures to opposing counsel in the course of settlement negotiations.
3. A record in this system of records may be disclosed, as a routine use, to a Member of Congress submitting a request involving an individual, to whom the record pertains, when the individual has requested assistance from the Member with respect to the subject matter of the record.
4. A record in this system of records may be disclosed, as a routine use, to a contractor of the Agency having need for the information in order to perform a contract. Recipients of information shall be required to comply with the requirements of the Privacy Act of 1974, as amended, pursuant to 5 U.S.C. 552a(m).
5. A record related to an International Application filed under the Patent Cooperation Treaty in this system of records may be disclosed, as a routine use, to the International Bureau of the World Intellectual Property Organization, pursuant to the Patent Cooperation Treaty.
6. A record in this system of records may be disclosed, as a routine use, to another federal agency for purposes of National Security review (35 U.S.C. 181) and for review pursuant to the Atomic Energy Act (42 U.S.C. 218(c)).
7. A record from this system of records may be disclosed, as a routine use, to the Administrator, General Services, or his/her designee, during an inspection of records conducted by GSA as part of that agency's responsibility to recommend improvements in records management practices and programs, under authority of 44 U.S.C. 2904 and 2906. Such disclosure shall be made in accordance with the GSA regulations governing inspection of records for this purpose, and any other relevant (i.e., GSA or Commerce) directive. Such disclosure shall not be used to make determinations about individuals.
8. A record from this system of records may be disclosed, as a routine use, to the public after either publication of the application pursuant to 35 U.S.C. 122(b) or issuance of a patent pursuant to 35 U.S.C. 151. Further, a record may be disclosed, subject to the limitations of 37 CFR 1.14, as a routine use, to the public if the record was filed in an application which became abandoned or in which the proceedings were terminated and which application is referenced by either a published application, an application open to public inspections or an issued patent.
9. A record from this system of records may be disclosed, as a routine use, to a Federal, State, or local law enforcement agency, if the USPTO becomes aware of a violation or potential violation of law or regulation.

Electronic Patent Application Fee Transmittal

Application Number:	11338007			
Filing Date:	23-Jan-2006			
Title of Invention:	High-voltage power semiconductor device			
First Named Inventor/Applicant Name:	James A. Cooper			
Filer:	Glen Madison Kellett			
Attorney Docket Number:	3220-79132			
Filed as Large Entity				
Utility Filing Fees				
Description	Fee Code	Quantity	Amount	Sub-Total in USD(\$)
Basic Filing:				
Pages:				
Claims:				
Miscellaneous-Filing:				
Petition:				
Patent-Appeals-and-Interference:				
Post-Allowance-and-Post-Issuance:				
Extension-of-Time:				
Extension - 2 months with \$0 paid	1252	1	460	460

Description	Fee Code	Quantity	Amount	Sub-Total in USD(\$)
Miscellaneous:				
Request for continued examination	1801	1	810	810
Total in USD (\$)				1270

Electronic Acknowledgement Receipt

EFS ID:	2991186
Application Number:	11338007
International Application Number:	
Confirmation Number:	4085
Title of Invention:	High-voltage power semiconductor device
First Named Inventor/Applicant Name:	James A. Cooper
Customer Number:	23643
Filer:	Glen Madison Kellett
Filer Authorized By:	
Attorney Docket Number:	3220-79132
Receipt Date:	12-MAR-2008
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Application Type:	Utility under 35 USC 111(a)

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Submitted with Payment	yes
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Payment was successfully received in RAM	\$ 1270
RAM confirmation Number	4514
Deposit Account	100435
Authorized User	

The Director of the USPTO is hereby authorized to charge indicated fees and credit any overpayment as follows:

Charge any Additional Fees required under 37 C.F.R. Section 1.21 (Miscellaneous fees and charges)

File Listing:					
Document Number	Document Description	File Name	File Size(Bytes) /Message Digest	Multi Part /.zip	Pages (if appl.)
1	Amendment Submitted/Entered with Filing of CPA/RCE	Amendment.pdf	645644 94b52dc230bcb838b0e82e21b87e5a780d16abb3	no	15
Warnings:					
Information:					
2	Request for Continued Examination (RCE)	RCE.pdf	626286 aa095ad63b36dcca6619add368cf9afaf d8126a4	no	3
Warnings:					
Information:					
3	Fee Worksheet (PTO-06)	fee-info.pdf	8297 0ae2a03a39bb9dcf6d16e092f0069d712b47f6ee	no	2
Warnings:					
Information:					
Total Files Size (in bytes):			1280227		
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BARNES & THORNBURG LLP

11 South Meridian Street
Indianapolis, Indiana 46204

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

<i>Group:</i>	2822	}	
		}	
<i>Confirmation No.:</i>	4085	}	
		}	
<i>Application No.:</i>	11/338,007	}	
		}	
<i>Invention:</i>	HIGH-VOLTAGE POWER SEMICONDUCTOR DEVICE	}	ELECTRONICALLY SUBMITTED ON: MARCH 12, 2008
		}	
<i>Applicant:</i>	James A. Cooper et al.	}	
		}	
<i>Filed:</i>	January 23, 2006	}	
		}	
<i>Attorney</i>		}	
<i>Docket:</i>	3220-79132	}	
		}	
<i>Examiner:</i>	Patton, Paul E.	}	

RESPONSE TO ACCOMPANY REQUEST FOR CONTINUED EXAMINATION

MAIL STOP RCE
Commissioner for Patents
P. O. Box 1450
Alexandria, VA 22313-1450

Sir:

In response to the Office Action dated October 12, 2007, and contemporaneously with the filing of a Request for Continued Examination, Applicants submit the following:

Amendments to the Claims are reflected in the listing of claims which begins on page 2 of this paper.

Remarks begin on page 7 of this paper.

AMENDMENTS TO THE CLAIMS

This listing of claims replaces all prior versions and listings of the claims in this application:

1. (Currently Amended) A metal-oxide semiconductor field-effect transistor comprising:

a ~~silicone-carbide~~ silicon-carbide substrate having a first concentration of first type impurities;

a drift semiconductor layer formed on a front side of the semiconductor substrate and having a second concentration of first type impurities less than the first concentration of first type impurities;

a current spreading semiconductor layer formed on a front side of the drift semiconductor layer;

a first source region;

a second source region; and

a JFET region formed on a front side of the current spreading semiconductor layer and defined between the first source region and the second source region, the JFET region having a third concentration of first type impurities that is greater than the second concentration of first type impurities.

2. (Cancelled)

3. (Original) The metal-oxide semiconductor field-effect transistor of claim 1, wherein the JFET region has a width of less than about three micrometers.

4. (Original) The metal-oxide semiconductor field-effect transistor of claim 3, wherein the JFET region has a width of about one micrometer.

5. (Original) The metal-oxide semiconductor field-effect transistor of claim 1, wherein the third concentration of first type impurities is at least one order of magnitude greater than the second concentration of first type impurities.

6. (Cancelled)

7. (Previously Presented) The metal-oxide semiconductor field-effect transistor of claim 1, wherein the current spreading semiconductor layer has a fourth concentration of first type impurities that is greater than the second concentration of first type impurities.

8. (Original) The metal-oxide semiconductor field-effect transistor of claim 7, wherein the fourth concentration of first type impurities is at least one order of magnitude greater than the second concentration of first type impurities.

9. (Previously Presented) The metal-oxide semiconductor field-effect transistor of claim 8, wherein the JFET region has a width of about one micrometer.

10. (Original) The metal-oxide semiconductor field-effect transistor of claim 1, further comprising a plurality of base contact regions formed in each of the first and the second source regions, the base contact regions being smaller than the first and second source regions.

11. (Original) The metal-oxide semiconductor field-effect transistor of claim 1, further comprising a plurality of source regions and a plurality of base contact regions, wherein the plurality of source regions and the plurality of base contact regions form alternating strips of N-type doped regions and P-type doped regions, the alternating strips being substantially orthogonal to respective source electrodes formed over the first and the second source regions.

12. (Currently Amended) A double-implanted metal-oxide semiconductor field-effect transistor comprising:

a ~~silicon-carbide~~ silicon-carbide substrate;

a drift semiconductor layer formed on a front side of the semiconductor substrate;

a first source region;

a first source electrode formed over the first source region, the first source electrode defining a longitudinal axis;

a plurality of first base contact regions defined in the first source region, each of the plurality of first base contact regions being spaced apart from each other in a direction parallel to the longitudinal axis defined by the first source electrode;

a second source region;

a second source electrode formed over the second source region, the second source electrode defining a longitudinal axis;

a plurality of second base contact regions defined in the second source region, each of the plurality of second base contact regions being spaced apart from each other in a direction parallel to the longitudinal axis defined by the second source electrode; and

a JFET region defined between the first source region and the second source region, the JFET region having a width less than about three micrometers.

13. (Original) The double-implanted metal-oxide semiconductor field-effect transistor of claim 12, wherein the JFET region has a width of about one micrometer.

14. (Original) The double-implanted metal-oxide semiconductor field-effect transistor of claim 12, wherein the JFET region has a first concentration of first type impurities and the drift semiconductor layer has a second concentration of first type impurities, the first concentration of first type impurities being greater than the second concentration of first type impurities.

15-16. (Cancelled)

17. (Currently Amended) A double-implanted metal-oxide semiconductor field-effect transistor comprising:

- a semiconductor substrate;
- a drift semiconductor layer formed on a front side of the semiconductor substrate;
- a current spreading semiconductor layer formed on a front side of the drift semiconductor layer;
- a plurality of first and second source regions;
- a plurality of base contact regions; and
- a JFET region defined between the plurality of first source regions and the plurality of second source regions, the JFET region being formed on a front side of the current spreading semiconductor layer,

wherein the plurality of first and second source regions and the plurality of base contact regions form alternating strips of N-type doped regions and P-type doped regions, each of the alternating strips defining a longitudinal axis that is ~~being~~ substantially orthogonal to a longitudinal axis defined by respective source electrodes formed over the first and the second source regions.

18. (Original) The double-implanted metal-oxide semiconductor field-effect transistor of claim 17, wherein the current spreading semiconductor layer has a first concentration of first type impurities and the drift semiconductor layer has a second concentration of first type impurities, the first concentration of first type impurities being greater than the second concentration of first type impurities.

19. (Original) The double-implanted metal-oxide semiconductor field-effect transistor of claim 18, wherein the first concentration of first type impurities is at least one order of magnitude greater than the second concentration of first type impurities.

20. (Original) The double-implanted metal-oxide semiconductor field-effect transistor of claim 17, wherein the JFET region has a width of about three micrometers or less.

21-22. (Cancelled)

23. (Original) A vertical double-implanted metal-oxide semiconductor field-effect transistor comprising:

- a silicon-carbide substrate having a first concentration of first type impurities;

- a drift semiconductor layer epitaxially formed on a front side of the silicon-carbide substrate and having a second concentration of first type impurities less than the first concentration of first type impurities;

- a current spreading semiconductor layer epitaxially formed on a front side of the drift layer, the current spreading semiconductor layer having a third concentration of first type impurities greater than the second concentration of first type impurities;

- a first source region;

- a second source region; and

- a JFET region defined between the first source region and the second source region and formed on a front side of the current spreading semiconductor layer, the JFET region having a width less than about three micrometers and a fourth concentration of first type impurities greater than the second concentration of first type impurities.

REMARKS

The Office Action dated October 12, 2007 has been carefully reviewed. Claims 1, 3-5, 7-14, 17-20, and 23 are pending in this application. Claims 1, 3-5, 7-14, 17-20, and 23 stand rejected in the 10/12/2007 Office Action. By this amendment, claims 1, 12, and 17 are amended.

35 U.S.C. §103(a) REJECTIONS

The Examiner rejected claims 1, 3, 4, 7-10, 12, and 13 as being unpatentable over Ono (U.S. Patent Publication No. 2003/0227052 A1) in view of Kumar (U.S. Patent No. 6,573,534 B1) in further view of Zeng (U.S. Patent No. 6,137,139). The Examiner rejected claims 11 and 17-29 as being unpatentable over Ono in view of Kumar in further view of Zeng and in further view of Kobayashi (U.S. Patent Publication Serial No. 2003/0052329). The Examiner rejected claims 5, 14, and 23 as being unpatentable over Ono in view of Kumar in further view of Zeng and in further view of Tokura (U.S. Patent No. 5,545,908).

Discussion: Independent Claim 1 - Ono, Kumar, & Zeng

In support of the rejection of claim 1, the Examiner concedes that "Ono does not disclose that the semiconductor substrate is a silicon-carbide substrate." (10/12/2007 Office Action, page 3, paragraph 4). The Examiner relies on Kumar to overcome this deficiency of Ono and states that Kumar "discloses that the substrate is a silicon-carbide substrate." (10/12/2007 Office Action, page 3, paragraph 5). The Examiner also concedes that "Ono as modified by Kumar does not explicitly disclose that a current spreading layer is formed on a front side of the drift semiconductor layers; and where the concentration of impurities of the first type is greater than [sic] the concentration of impurities of the first type in the drift region by at least one order of magnitude." (10/12/2007 Office Action, page 4, paragraph 9). The Examiner relies on Zeng to overcome this deficiency of Ono and Kumar. In an attempt to establish a reason to combine the teachings of Ono, Kumar, and Zeng, the Examiner argues that:

[I]t would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Ono by using as silicon-carbide substrate for advantages such as higher breakdown voltage and lower ON resistance

according to the teachings of Kumar (Column 1, lines 27-30). . . .

[i]t would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Ono to have a current spreading layer formed on a front side of the drift semiconductor layer; and wherein the concentration of impurities of the first type is greater than [sic] the concentration of impurities of the first type in the drift region by at least one order of magnitude for advantages such as reduced on-resistance without degrading device ruggedness and reliability according to the teachings of Zeng (Column 4, lines 32039). (10/12/2007 Office Action, page 4, paragraph 7 and page 5, paragraph 12)

Applicants respectfully traverse these rejections. As discussed in detail below, Applicants believe that no rational reason exists why one of ordinary skill in the art would combine Ono, Kumar, and Zeng in the manner described. Applicants assert that no such reason exists because the proposed combination would render the device of Ono unsatisfactory or inoperable for its intended purpose. Thus, Ono, Kumar, and Zeng teach away from the proposed combination and cannot support a finding of obviousness.

I. References Teach Away from Proposed Combination

Applicants assert that no rational reason exists to combine Ono, Kumar, and Zeng in the manner described by the Examiner because the cited references teach away from the proposed combination. The Supreme Court recently emphasized the “principle that when the prior art teaches away from combining certain known elements, discovery of a successful means of combining them is more likely to be nonobvious.” KSR Int’l v. Teleflex, Inc., 127 S.Ct. 1727, 1740 (citing U.S. v. Adams, 383 U.S. 39, 51-52 (1966)). According to the Federal Circuit, the prior art effectively teaches away when an examiner’s proposed modification of prior art renders the prior art invention “inoperable for its intended purpose.” In re Gordon, 733 F.2d 900, 902 (Fed. Cir. 1984). “If proposed modification would render the prior art invention being modified unsatisfactory for its intended purpose, then there is no suggestion or motivation to make the proposed modification.” (see MPEP §2141.01.V)

The semiconductor device of Ono would be rendered unsatisfactory or inoperable for its intended purpose if modified to include the structures of Zeng and Kumar as proposed by

the Examiner. As noted by the Examiner, Ono and Zeng are directed toward MOSFET devices having silicon substrates, while Kumar is directed toward silicon-carbide MOSFET devices. Although the Examiner asserts that modifying Ono to include a silicon-carbide is an obvious modification, such an assertion ignores the technical aspects of silicon-carbide MOSFET devices. Silicon-carbide MOSFET devices are often used for high-power applications. In such applications, a high blocking voltage is desirable. For example, Kumar teaches:

It is an object of the present invention to provide a SiC MOS transistor which makes full use of the characteristics of SiC in order to obtain even lower ON resistance and *higher breakdown voltage* than conventional SiC MOS transistors. Kumar, Col 1, ll. 31-35, emphasis added.

Unlike silicon MOSFET devices, the blocking voltage of silicon-carbide MOSFET devices is limited by gate oxide failure rather than semiconductor breakdown. Gate oxide failure can be caused by the electric field of the gate oxide having an excessive strength. As noted in Paragraph [0028] of Applicants' present patent application, the use of a JFET region and a current spreading layer in a silicon-carbide substrate reduces the blocking voltage of the device due to an increased strength of the gate oxide electric field. As such, it would not be obvious to one of ordinary skill in the art to incorporate a JFET region as taught in Ono and a current spreading layer as taught in Zeng with a silicon-carbide substrate because such features would reduce the blocking voltage of the device and likely render the device inoperable for its intended purpose. For example, such modification to the power MOSFET 1 of Ono would render the device unsatisfactory or inoperable for its intended purpose as a power device due to a reduced blocking voltage. Applicants, however, have discovered various methods and structures, such as increasing the thickness of the drift layer, wherein a JFET region and a current spreading layer may be incorporated in a silicon-carbide substrate while maintaining a high blocking voltage (see, e.g., Paragraph [0028] of Applicants' present patent application).

For at least the reasons provided above, there simply is no motivation combine Ono, Kumar, and Zeng in the manner proposed by the Examiner because such a modification would render the resultant device unsatisfactory in operation. As such, amended claim 1 is believed to be in condition for allowance and such action is respectfully requested.

Discussion Re: Claims 3-4 and 7-11

Claims 3-4 and 7-11 include claim 1 as a base claim. As such, the rejection of claims 3-4 and 7-11 should be withdrawn for the reasons hereinbefore discussed with regard to amended claim 1. In light of the reasons for withdrawal of the rejection of claim 1, any arguments specific to claims 3-4 and 7-11 are held in abeyance without prejudice or admission to any assertion made by the Examiner in order to expedite prosecution.

Discussion: Independent Claim 12 - Ono, Kumar, & Zeng

The Examiner appears to reject claim 12 as being unpatentable over the combination of Ono, Kumar, and Zeng. For the reasons provided below, the rejection of claim 12 is traversed.

I. Examiner Has Failed to Provide Explanation Of Rejection

The Examiner has failed to provide an explicit rejection of claim 12. Applicants respectfully request that the Examiner point with particularity to those sections of Ono, Kumar, and/or Zeng wherein the Examiner believes each element of claim 12 is disclosed as required by 37 C.F.R. §1.104(c)(2):

In rejecting claims for want of novelty or for obviousness, the examiner must cite the best references at his or her command. When a reference is complex or shows or describes inventions other than that claimed by the applicant, the particular part relied on must be designated as nearly as practicable. The pertinence of each reference, if not apparent, must be clearly explained and each rejected claim specified.

II. Combination Fails To Disclose Each Element Of Claim 12

Applicants believe that no reference of record discloses each and every element of amended claim 12. Claim 12 has been amended to further clearly define the claimed invention. In particular, claim 12 has been amended to recite:

12. A double-implanted metal-oxide semiconductor field-effect transistor comprising:
a silicon-carbide substrate;

a drift semiconductor layer formed on a front side of the semiconductor substrate;
a first source region;
a first source electrode formed over the first source region, the first source electrode defining a longitudinal axis;
a plurality of first base contact regions defined in the first source region, each of the plurality of first base contact regions being spaced apart from each other in a direction parallel to the longitudinal axis defined by the first source electrode;
a second source region;
a second source electrode formed over the second source region, the second source electrode defining a longitudinal axis;
a plurality of second base contact regions defined in the second source region, each of the plurality of second base contact regions being spaced apart from each other in a direction parallel to the longitudinal axis defined by the second source electrode; and
a JFET region defined between the first source region and the second source region, the JFET region having a width less than about three micrometers.

None of the references of record individually or in combination disclose such a device. For example, neither Ono, Kumar, nor Zeng disclose the particular configuration of base contact regions and source regions as claimed.

III. References Teach Away from Proposed Combination

The Examiner rejected claim 12 as unpatentable over the combination of Ono, Kumar, and Zeng. As such, all the arguments provided above in regard to claim 1 apply with equal force to claim 12. Accordingly, for at least the reasons provided herein, amended claim 12 is believed to be in condition for allowance and such action is respectfully requested.

Discussion Re: Claims 13 and 14

Claims 13 and 14 include claim 12 as a base claim. As such, the rejection of claims 13 and 14 should be withdrawn for the reasons hereinbefore discussed with regard to amended claim 12. In light of the reasons for withdrawal of the rejection of claim 12, any arguments specific to claims 13 and 14 are held in abeyance without prejudice or admission to any assertion made by the Examiner in order to expedite prosecution.

Discussion: Independent Claim 17 - Ono, Kumar, Zeng, & Kobayashi

The Examiner maintains his rejection of claim 17 based on the combination of Ono, Kumar, Zeng, and Kobayshi. In support of this rejection, the Examiner asserts that:

Kobayashi shows (Fig 18) a plurality of source regions and a plurality of base contact regions, wherein the plurality of base contact regions (13), form alternating strips of N-type doped regions and P-type doped regions, *the alternating strips (17) being substantially orthogonal to respective source electrodes formed over the first and second source regions.* (10/12/2007 Office Action, Page 8, Paragraph 20, emphasis added).

The Examiner later expounds upon this rejection:

As to claim 17, this claim is rejected on the same basis as before. While it is true that Kobayashi has a drawing with limited detail, [t]he format claimed of the individual devices laid out in strips is very well known in the art of power transistors. Further, the source contacts would inherently be laid out orthogonal from the strip direction as can be also inferred from figure 12 of Tokura. (10/12/2007 Office Action, Page 12, Paragraph 33).

Applicants disagree. First, Kobayashi fails to disclose the particular structure relied on by the Examiner. Second, the Examiner appears to be taking improper Official Notice regarding the configuration of power transistors. Third, the Examiner improperly argues that the claimed configuration is inherent in the cited reference. Thus, for at least these reasons, the Examiner's rejection of claim 17 is improper and should be withdrawn.

I. Kobayshi Fails To Disclose The Structure Relied On By Examiner

Again, Applicants point out that reference numeral 13 of Kobayashi points to a well region (13) and reference numeral 17 of Kobayashi points to a gate insulation film (17). Applicants assume the Examiner meant to refer to the contact region 21 and the source region 15 of Kobayashi, respectively. Regardless, Kobayashi simply fails to teach "a plurality of source regions and a plurality of base contact regions, wherein the plurality of base contact regions (13), form alternating strips of N-type doped regions and P-type doped regions, the alternating strips (17) being substantially orthogonal to respective source electrodes formed over the first and second source regions" as asserted by the Examiner. Rather, it is clear from a review of FIGS.

17 and 18 of Kobayashi that the source electrode 19 (see FIG. 17) is oriented in a **parallel configuration** (i.e., non-orthogonal) relative to the source region 15 and the contact region 21.

However, to further clearly define the invention of claim 17, Applicants have amended claim 17 to recite:

wherein the plurality of first and second source regions and the plurality of base contact regions form alternating strips of N-type doped regions and P-type doped regions, each of the alternating strips defining a longitudinal axis that is substantially orthogonal to a longitudinal axis defined by respective source electrodes formed over the first and the second source regions

Neither Kobayashi nor any other reference of record teaches such a structure. If the Examiner upholds his rejection of claim 17 based on Kobayashi, Applicants respectfully request the Examiner point with particularity to the figure(s) and associated description of Kobayashi wherein such an element is disclosed.

II. Official Notice is Improper

The Examiner appears to take official notice that “[t]he format claimed of the individual devices laid out in strips is very well known in the art of power transistors.” However, such official notice is improper because such a configuration is clearly not well known and the Examiner has failed to provide a technical line of reasoning supporting the official notice (see MPEP §2144.03.A and §2144.03.B). Applicants specifically challenge such an official notice because the claimed configuration of “wherein the plurality of first and second source regions and the plurality of base contact regions form alternating strips of N-type doped regions and P-type doped regions, each of the alternating strips defining a longitudinal axis that is substantially orthogonal to a longitudinal axis defined by respective source electrodes formed over the first and the second source regions” is not common knowledge, being rather an invention of the Applicants.

II. Claimed Configuration Is Not Inherent

The Examiner argues that “the source contacts would inherently be laid out orthogonal from the strip direction as can be also inferred from figure 12 of Tokura.” “Inherency, however, may not be established by probabilities or possibilities. The mere fact that

a certain thing may result from a given set of circumstances is not sufficient.” *Hansgird v. Kemmer*, 102 F.2d 212, 40 U.S.P.Q. 665, 667 (C.C.P.A. 1939); *In re Oelrich and Divigard*, 666 F.2d 578, 212 U.S.P.Q. 323, 326 C.C.P.A. 1981). Accordingly, it cannot be said that the source contacts of Kobayashi must be orthogonal to the strip direction of the base and source regions. Applicants note that Figure 12 of Tokura is of no help either. As such, the device configuration of claim 17 is neither inherent nor obvious in light of the teachings of Kobayashi, Tokura, nor any other reference of record. For at least the reasons provided above, amended claim 17 is believed to be in condition for allowance and such action is respectfully requested.

Discussion Re: Claims 18-20

Claims 18-20 include claim 17 as a base claim. As such, the rejection of claims 18-20 should be withdrawn for the reasons hereinbefore discussed with regard to amended claim 17. In light of the reasons for withdrawal of the rejection of claim 17, any arguments specific to claims 18-20 are held in abeyance without prejudice or admission to any assertion made by the Examiner in order to expedite prosecution.

Discussion: Independent Claim 23 - Ono, Kumar, Zeng, & Tokura

The Examiner rejected claim 23 as unpatentable over the combination of Ono, Kumar, Zeng, and Tokura. As such, for all the reasons provided above in regard to independent claim 1, it would not be obvious to one of ordinary skill to combine the teachings of Ono, Kumar, and Zeng in the manner proposed by the Examiner. For at last this reason, the combination of Ono, Zeng, Tokura, and Kumar fails to render claim 23 obvious. As such, claim 23 is believed to be in condition for allowance and such action is respectfully requested.

CONCLUSION

In view of the foregoing, it is submitted that this application is in a condition for allowance. Action to that end is hereby solicited. If there are any questions or comments that would speed prosecution of this application, the Examiner is invited to call the undersigned at (317) 261-7959.

It is respectfully requested that this paper be considered as a petition for a two-month extension of time extending the deadline of this response to March 12, 2008. The Commissioner is hereby authorized to charge the fee of \$460.00 for this two-month extension of time, and any shortages or overpayments of fees, to the Account of Barnes & Thornburg, Deposit Account No. 10-0435 with reference to file 3220-79132.

Respectfully submitted,

BARNES & THORNBURG LLP

A handwritten signature in black ink, appearing to read 'Glen M. Kellett', is written over a horizontal line.

Glen M. Kellett
Registration No. 60,202
Barnes & Thornburg
11 South Meridian Street
Indianapolis, Indiana 46204-3535
Telephone: (317) 261-7959
Fax: (317) 231-7433

Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it displays a valid OMB control number.

PATENT APPLICATION FEE DETERMINATION RECORD Substitute for Form PTO-875					Application or Docket Number 11/338,007		Filing Date 01/23/2006		<input type="checkbox"/> To be Mailed	
APPLICATION AS FILED – PART I										
(Column 1)			(Column 2)		SMALL ENTITY <input type="checkbox"/> OR		OTHER THAN SMALL ENTITY			
FOR	NUMBER FILED	NUMBER EXTRA	RATE (\$)	FEE (\$)	OR	RATE (\$)	FEE (\$)			
<input type="checkbox"/> BASIC FEE (37 CFR 1.16(a), (b), or (c))	N/A	N/A	N/A			N/A				
<input type="checkbox"/> SEARCH FEE (37 CFR 1.16(k), (l), or (m))	N/A	N/A	N/A			N/A				
<input type="checkbox"/> EXAMINATION FEE (37 CFR 1.16(o), (p), or (q))	N/A	N/A	N/A			N/A				
TOTAL CLAIMS (37 CFR 1.16(i))	minus 20 =	*	X \$	=		X \$	=			
INDEPENDENT CLAIMS (37 CFR 1.16(h))	minus 3 =	*	X \$	=		X \$	=			
<input type="checkbox"/> APPLICATION SIZE FEE (37 CFR 1.16(s))	If the specification and drawings exceed 100 sheets of paper, the application size fee due is \$250 (\$125 for small entity) for each additional 50 sheets or fraction thereof. See 35 U.S.C. 41(a)(1)(G) and 37 CFR 1.16(s).									
<input type="checkbox"/> MULTIPLE DEPENDENT CLAIM PRESENT (37 CFR 1.16(j))										
* If the difference in column 1 is less than zero, enter "0" in column 2.			TOTAL			TOTAL				
APPLICATION AS AMENDED – PART II										
(Column 1)		(Column 2)		(Column 3)		SMALL ENTITY OR		OTHER THAN SMALL ENTITY		
AMENDMENT	03/12/2008	CLAIMS REMAINING AFTER AMENDMENT		HIGHEST NUMBER PREVIOUSLY PAID FOR	PRESENT EXTRA	RATE (\$)	ADDITIONAL FEE (\$)	OR	RATE (\$)	ADDITIONAL FEE (\$)
	Total (37 CFR 1.16(i))	* 17	Minus	** 23	= 0	X \$	=		X \$50=	0
	Independent (37 CFR 1.16(h))	* 4	Minus	***4	= 0	X \$	=		X \$210=	0
	<input type="checkbox"/> Application Size Fee (37 CFR 1.16(s))									
	<input type="checkbox"/> FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))									
						TOTAL ADD'L FEE			OR	TOTAL ADD'L FEE
(Column 1)		(Column 2)		(Column 3)		SMALL ENTITY OR		OTHER THAN SMALL ENTITY		
AMENDMENT	Total (37 CFR 1.16(i))	*	Minus	**	=	RATE (\$)	ADDITIONAL FEE (\$)		RATE (\$)	ADDITIONAL FEE (\$)
	Independent (37 CFR 1.16(h))	*	Minus	***	=	X \$	=		X \$	=
	<input type="checkbox"/> Application Size Fee (37 CFR 1.16(s))									
	<input type="checkbox"/> FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))									
						TOTAL ADD'L FEE			OR	TOTAL ADD'L FEE
<p>* If the entry in column 1 is less than the entry in column 2, write "0" in column 3.</p> <p>** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 20, enter "20".</p> <p>*** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 3, enter "3".</p> <p>The "Highest Number Previously Paid For" (Total or Independent) is the highest number found in the appropriate box in column 1.</p>										

Legal Instrument Examiner:
/JERMAINE D. MINOR/

This collection of information is required by 37 CFR 1.16. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 12 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

If you need assistance in completing the form, call 1-800-PTO-9199 and select option 2.



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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
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11/338,007

01/23/2006

James A. Cooper

3220-79132

4085

23643 7590 06/25/2008

BARNES & THORNBURG LLP
11 SOUTH MERIDIAN
INDIANAPOLIS, IN 46204

EXAMINER

PATTON, PAUL E

ART UNIT

PAPER NUMBER

2822

MAIL DATE

DELIVERY MODE

06/25/2008

PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No. 11/338,007	Applicant(s) COOPER ET AL.	
	Examiner PAUL E. PATTON	Art Unit 2822	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 12 March 2008.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1,3-5,7-14,17-20 and 23 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☒ Claim(s) 12-14 and 17-20 is/are allowed.
- 6) ☒ Claim(s) 1,3-5 and 7-10 is/are rejected.
- 7) ☐ Claim(s) 11 is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on _____ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some * c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
 2. ☐ Certified copies of the priority documents have been received in Application No. _____.
 3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- | | |
|--|---|
| 1) <input type="checkbox"/> Notice of References Cited (PTO-892) | 4) <input type="checkbox"/> Interview Summary (PTO-413) |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948) | Paper No(s)/Mail Date. _____ |
| 3) <input type="checkbox"/> Information Disclosure Statement(s) (PTO/SB/08) | 5) <input type="checkbox"/> Notice of Informal Patent Application |
| Paper No(s)/Mail Date _____ | 6) <input type="checkbox"/> Other: _____ |

DETAILED ACTION

Response to Amendment

1. Acknowledgement is made of Amendment filed March 12, 2008.
2. Applicant's arguments regarding claims 1, 3-5, 7-10 and 23 have been fully considered but they are not persuasive. Applicant's argument asserts that examiner has not presented reasonable arguments for combining the references to Ono, Kumar and Zeng. However, examiner believes that the rationale stated in the previous office action clearly presents such a rationale. Further, applicant argues that the combination of these elements *might* render such a device inoperative. However, absent documentary evidence this assertion is not convincing.
3. The rejections of dependent claim 11 and claims 12-14 and 17-20 have been withdrawn.

Claim Rejections - 35 USC § 103

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.
5. Claims 1, 3, 4, and 7 – 10, are rejected under 35 U.S.C. 103(a) as being unpatentable over Ono et al., (US 2003/0227052 A1) Ono in view of Kumar et al., (USPAT 6,573,534.B1) Kumar and further in view of Zeng et al., (USPAT 6,137,139) Zeng.

Art Unit: 2822

6. As to claims 1,3,4, and 9, Ono discloses and shows (Fig 1), a double implanted MOS field effect transistor comprising a semiconductor substrate (10) having a first concentration of first type impurities (n^+); a drift semiconductor layer (50) formed on a front side of the semiconductor substrate and having a second concentration of first type impurities less than the first concentration of first type impurities (n^-); a first source region (20); a second source region (20); and a JFET region (40) defined between the first source region and the second source region, the JFET region having a third concentration of first type impurities that is greater than the second concentration of first type impurities (n) and having a width (L) less than about 3 micrometers and a width of about one micrometer. (Paragraphs [0039] & [0041]).

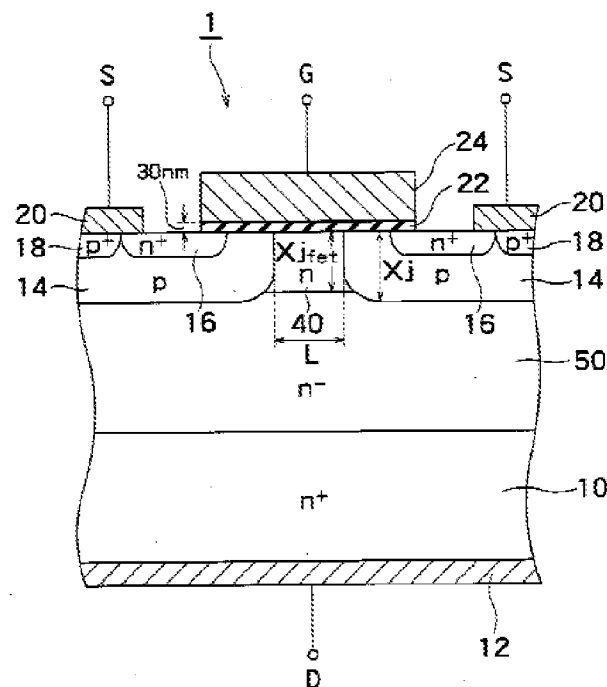
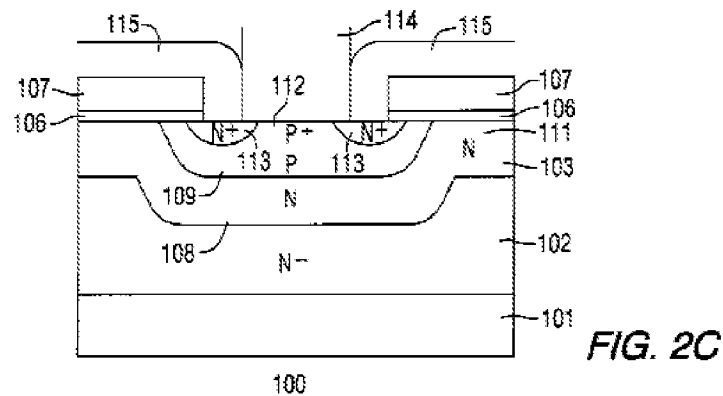


FIG. 1

7. Ono does not disclose that the semiconductor substrate is a silicon-carbide substrate.
8. Kumar is related to a similar MOS FET structure and discloses that the substrate is a silicon-carbide substrate (Column 1, line 40).
9. Kumar is evidence that a person of ordinary skill in the art would find a reason, suggestion or motivation to use a silicon-carbide substrate.
10. Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Ono by using a silicon-carbide substrate for advantages such as higher breakdown voltage and lower ON resistance according to the teachings of Kumar (Column 1, lines 27-30).
11. Ono shows (Ono, Fig 1) the JFET region is formed directly below the gate structure and between the base doped wells formed on either side of the gate. As noted above the parasitic JFET is a consequence of the lateral gate-source arrangement of a vertical MOSFET and would be above the current spreading layer and the drift region shown by Zeng.
12. Ono as modified by Kumar does not explicitly disclose that a current spreading layer is formed on a front side of the drift semiconductor layer; and wherein the concentration of impurities of the first type is greater than the concentration of impurities of the first type in the drift region by at least one order of magnitude.
13. Zeng discloses and shows (Fig 2C) a current spreading layer (103) formed on a front side of the drift semiconductor layer (102) wherein the concentration of impurities of the first type is greater than the concentration of impurities of the first type in the drift

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region by at least one order of magnitude (Zeng, Column 2, lines 64-67 & Column 3, lines 4-7).



14. Zeng is evidence that a person of ordinary skill in the art would find a reason, suggestion or motivation to have a current spreading layer formed on a front side of the drift semiconductor layer; and wherein the concentration of impurities of the first type is greater than the concentration of impurities of the first type in the drift region by at least one order of magnitude.

15. Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Ono to have a current spreading layer formed on a front side of the drift semiconductor layer; and wherein the concentration of impurities of the first type is greater than the concentration of impurities of the first type in the drift region by at least one order of magnitude for advantages such as reduced on-resistance without degrading device ruggedness and reliability according to the teachings of Zeng (Column 4, lines 32-39).

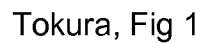
16. As to claims 7 and 8, Ono as modified by Kumar and Zeng discloses and shows (Fig 2C) a current spreading layer (103) formed on a front side of the drift semiconductor layer (102) wherein the concentration of impurities of the first type is greater than the concentration of impurities of the first type in the drift region by at least one order of magnitude (Zeng, Column 2, lines 64-67 & Column 3, lines 4-7).

17. As to claim 10, Ono as modified by Kumar and Zeng shows (Ono, Fig 12) a plurality of base contact regions (18) formed in each of the first and second source regions (16), the base contact regions being smaller than the first and second source regions.

18. Claims 5 and 23 are rejected under 35 U.S.C. 103(a) as being unpatentable over Ono in view of Kumar and Zeng and further in view of Tokura et al., (USPAT 5,545,908).

19. Ono as modified by Kumar and Zeng does not disclose that the concentration of first type impurities associated with the JFET region is at least one order of magnitude greater than the concentration of first type impurities associated with the drift region.

20. Tokura is related to a similar MOSFET structure and discloses and shows (Tokura, Fig 1) that the doping level at the JFET region (5) is $8 \times 10^{16} \text{ cm}^{-3}$ whereas the doping level of the drift region (2) is $5 \times 10^{15} \text{ cm}^{-3}$. (Tokura, Column 10, lines 29-33 & Column 11, lines 54-58). Note that Tokura does not label the region between the two p doped wells on opposite sides of the gate as a JFET. However the structure in this device as well as Ono will form a parasitic JFET due to the arrangement of the layers. (Ono, Paragraph [0040]).



22. Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Ono by having the concentration of the JFET region at least an order of magnitude greater than the concentration of the drift region for advantages such as reduced ON resistance according to the teachings of Tokura (Column 5, lines 60-66 & Column 8, lines 33-34).

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drift semiconductor layer (50) formed on a front side of the semiconductor substrate and having a second concentration of first type impurities less than the first concentration of first type impurities (n-); a first source region (20); a second source region (20); and a JFET region (40) defined between the first source region and the second source region, the JFET region having a fourth concentration of first type impurities that is greater than the second concentration of first type impurities (n) and having a width (L) less than about 3 micrometers and a width of about one micrometer. (Paragraphs [0039] & [0041]).

Kumar discloses that the substrate is a silicon-carbide substrate (Column 1, line 40). Zeng discloses and shows (Fig 2C) a current spreading layer (103) formed on a front side of the drift semiconductor layer (102) wherein the concentration of impurities of the first type is greater than the concentration of impurities of the first type in the drift region (Zeng, Column 2, lines 64-67 & Column 3, lines 4-7). Lastly, Tokura discloses and shows (Tokura, Fig 1) that the doping level at the JFET region (5) is $8 \times 10^{16} \text{ cm}^{-3}$ whereas the doping level of the drift region (2) is $5 \times 10^{15} \text{ cm}^{-3}$. (Tokura, Column 10, lines 29-33 & Column 11, lines 54-58). Note that Tokura does not label the region between the two p-doped wells on opposite sides of the gate as a JFET. However the structure in this device as well as Ono will form a parasitic JFET due to the arrangement of the layers. (Ono, Paragraph [0040]).

Allowable Subject Matter

24. Claim 11 is objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

25. Claims 12-14 and 17-20 are allowed.

26. The following is a statement of reasons for the indication of allowable subject matter: The prior art of record, taken alone or in combination fails to anticipate or render obvious the plurality of source regions and the plurality of base contact regions form alternating strips of N-type doped regions and P-type doped regions, the alternating strips being substantially orthogonal to respective source electrodes formed over the first and the second source regions as recited in independent claim 17 along with all its other limitations and dependent claim 11.

27. As to claim 12, the prior art of record taken alone or in combination fails to anticipate or render obvious a first source electrode formed over the first source region, the first source electrode defining a longitudinal axis; a plurality of first base contact regions defined in the first source region, each of the plurality of first base contact regions being spaced apart from each other in a direction parallel to the longitudinal axis defined by the first source electrode; a second source region; a second source electrode formed over the second source region, the second source electrode defining a longitudinal axis; a plurality of second base contact regions defined in the second source region, each of the plurality of second base contact regions being spaced apart

fro each other in a direction parallel to the longitudinal axis defined by the second source electrode, along with all the other limitations of claim 12.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to PAUL E. PATTON whose telephone number is (571)272-9762. The examiner can normally be reached on 7:00 - 5:30 Monday through Thursday.


If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Zandra Smith can be reached on 571-272-2429. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/Zandra V. Smith/
Supervisory Patent Examiner, Art Unit 2822

Paul E Patton
Examiner
Art Unit 2822

/P. E. P./
Examiner, Art Unit 2822

<i>Index of Claims</i> 	Application/Control No. 11338007	Applicant(s)/Patent Under Reexamination COOPER ET AL.
	Examiner Patton, Paul E	Art Unit 2822

✓	Rejected	-	Cancelled	N	Non-Elected	A	Appeal
=	Allowed	÷	Restricted	I	Interference	O	Objected

<input type="checkbox"/> Claims renumbered in the same order as presented by applicant		<input type="checkbox"/> CPA		<input type="checkbox"/> T.D.		<input type="checkbox"/> R.1.47			
CLAIM		DATE							
Final	Original	03/26/2007	10/02/2007	05/30/2008					
	1	✓	✓	✓					
	2	✓	-	-					
	3	✓	✓	✓					
	4	✓	✓	✓					
	5	✓	✓	✓					
	6	✓	-						
	7	✓	✓	✓					
	8	✓	✓	✓					
	9	✓	✓	✓					
	10	✓	✓	✓					
	11	✓	✓	O					
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	23	✓	✓	✓					

EAST Search History

Ref #	Hits	Search Query	DBs	Default Operator	Plurals	Time Stamp
L21	5095	((257/263) or (257/256) or (257/341) or (257/342) or (257/335) or (257/339) or (257/350)).CCLS.	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2008/05/30 10:55
L22	3980	((438/142) or (438/156) or (438/176) or (438/186) or (438/197) or (438/268)).CCLS.	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2008/05/30 10:55
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L24	8029	@ad<"20060123" and L23	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2008/05/30 10:55
L25	1642	24 and (parallel strip longitud\$4) same source	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2008/05/30 10:56
L26	448	24 and (parallel strip longitud\$4) same (source near3 electrode)	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2008/05/30 10:57
S1	1393	((Cooper near (James J)) (Saha near (Asmita A))). in.	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2007/03/22 10:54

S2	380394	"257".clas.	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2007/03/22 09:01
S3	7	S1 and S2	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2007/03/22 09:01
S4	4717	((257/263) or (257/256) or (257/341) or (257/342) or (257/335) or (257/339) or (257/350)).CCLS.	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2007/03/22 10:55
S5	3327	((438/142) or (438/156) or (438/176) or (438/186) or (438/197) or (438/268)).CCLS.	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2007/03/22 10:56
S6	7886	S4 S5	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2007/03/22 11:03
S7	156976	MOSFET ("metal oxide semiconductor")	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2007/03/22 11:04
S8	5305	DMOS	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2007/03/22 11:04
S9	304	Double adj implant	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2007/03/22 11:04

S10	57449	power same (FET "Field effect")	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2007/03/22 11:06
S11	8478	JFET ("Junction Field Effect")	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2007/03/22 11:07
S12	3533	current near spread\$3	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2007/03/23 10:28
S13	10361	Drift near5 (layer region)	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2007/03/22 11:10
S14	0	S6 and S7 and S9 and S10 and S11 and S12 and S13	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2007/03/22 11:12
S15	20	S7 and S12 and S13 and S6	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2007/03/22 11:13
S16	80	S7 and S12 and S13	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2007/03/22 11:34
S17	0	S16 and S9	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2007/03/22 11:14

S18	180117	siC (Silicon adj carbide)	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2007/03/22 11:35
S19	548	S11 and S13 and S7	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2007/03/22 14:11
S20	202	S19 and S6	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2007/03/23 12:53
S21	1125	257/341.ccls.	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2007/03/22 15:36
S22	145	S21 and S11	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2007/03/22 15:36
S23	16	S21 and S12	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2007/03/22 15:58
S24	49	S6 and S12	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2007/03/22 16:11
S25	628	S6 and S18	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2007/03/22 16:12

S26	92	S21 and S18	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2007/03/22 16:12
S27	1121	current near spread\$3 near5 layer	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2007/03/23 10:29
S28	1125	257/341.ccls.	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2007/03/23 10:29
S29	6	S27 and S28	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2007/03/23 10:32
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S31	3327	((438/142) or (438/156) or (438/176) or (438/186) or (438/197) or (438/268)).CCLS.	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2007/03/23 10:32
S32	7886	S30 S31	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2007/03/23 10:32
S33	12	S27 and S32	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2007/03/23 10:32


S34	156976	MOSFET ("metal oxide semiconductor")	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2007/03/23 12:47
S35	8478	JFET ("Junction Field Effect")	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2007/03/23 12:47
S36	10361	Drift near5 (layer region)	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2007/03/23 12:47
S37	548	S35 and S36 and S34	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2007/03/23 12:47
S38	202	S37 and S32	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2007/03/23 12:47
S39	195	S38 and dop\$3	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2007/03/23 14:03
S40	187432	S34 amd S36 and (dop\$3 concentrat\$3 dos\$3)	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2007/03/23 14:06
S41	4013	S40 and S32	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2007/03/23 14:07

S42	436	S41 and S35	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2007/03/23 15:25
S43	4	S42 and S27	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2007/03/23 15:25
S44	5	S42 and current near5 spread	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2007/03/23 15:27
S45	36	S41 and current near5 spread	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2007/03/26 08:21
S46	2	("5688725").PN.	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2007/03/23 15:50
S47	5	("4941026" "5341011" "5424231" "5532179" "5558313").PN.	US-PGPUB; USPAT; USOCR	OR	ON	2007/03/26 08:12
S48	2	("4941026").PN.	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2007/03/26 08:12
S49	4717	((257/263) or (257/256) or (257/341) or (257/342) or (257/335) or (257/339) or (257/350)).CCLS.	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2007/03/26 08:21
S50	3327	((438/142) or (438/156) or (438/176) or (438/186) or (438/197) or (438/268)).CCLS.	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2007/03/26 08:21

S51	7886	S49 S50	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2007/03/26 08:21
S52	157110	MOSFET ("metal oxide semiconductor")	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2007/03/26 08:21
S53	10368	Drift near5 (layer region)	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2007/03/26 08:21
S54	187573	S52 amd S53 and (dop\$3 concentrat\$3 dos\$3)	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2007/03/26 08:21
S55	4013	S54 and S51	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2007/03/26 08:21
S56	72	S55 and current near5 spread\$3	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2007/03/26 08:22

5/ 30/ 2008 6:27:01 PM

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Search Notes 	Application/Control No. 11338007	Applicant(s)/Patent Under Reexamination COOPER ET AL.
	Examiner Patton, Paul E	Art Unit 2822

SEARCHED			
Class	Subclass	Date	Examiner
257	263, 256, 341, 342, 335, 339, 350, 263,	3/22/2007	PEP
438	142, 156, 176, 186, 197, 268	3/22/2007	PEP

SEARCH NOTES		
Search Notes	Date	Examiner
Search history attached	2/26/2007	PEP
Updated Search	10/2/2007	PEP
Consult with M. Prenty	10/2/2007	PEP
Consult with M. Prenty	5/30/2008	PEP
Updated search	5/30/2008	PEP

INTERFERENCE SEARCH			
Class	Subclass	Date	Examiner

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

<i>Group:</i>	2822	}	
		}	
<i>Confirmation No.:</i>	4085	}	
		}	
<i>Application No.:</i>	11/338,007	}	
		}	
<i>Invention:</i>	HIGH-VOLTAGE POWER SEMICONDUCTOR DEVICE	}	DATED:
		}	
<i>Applicant:</i>	James A. Cooper et al.	}	AUGUST 22, 2008
		}	
<i>Filed:</i>	January 23, 2006	}	
		}	
<i>Attorney</i>		}	
<i>Docket:</i>	3220-79132	}	
		}	
<i>Examiner:</i>	Patton, Paul E.	}	

RESPONSE TO OFFICE ACTION

MAIL STOP AF
Commissioner for Patents
P. O. Box 1450
Alexandria, VA 22313-1450

Sir:

In response to the Office Action dated June 25, 2008, Applicants submit the following:

Amendments to the Claims, which begin on page 2 of this paper; and

Remarks, which begin on page 7 of this paper.

CLAIMS AS PENDING

1. (Currently Amended) A metal-oxide semiconductor field-effect transistor comprising:

a silicon-carbide substrate having a first concentration of first type impurities;

a drift semiconductor layer formed on a front side of the semiconductor substrate and having a second concentration of first type impurities less than the first concentration of first type impurities;

a current spreading semiconductor layer formed on a front side of the drift semiconductor layer;

a first source region;

a second source region; and

a JFET region formed on a front side of the current spreading semiconductor layer and defined between the first source region and the second source region, the JFET region having a third concentration of first type impurities that is greater than the second concentration of first type impurities;

a plurality of source regions; and

a plurality of base contact regions,

wherein the plurality of source regions and the plurality of base contact regions form alternating strips of N-type doped regions and P-type doped regions, the alternating strips being substantially orthogonal to respective source electrodes formed over the first and the second source regions.

2. (Cancelled)

3. (Original) The metal-oxide semiconductor field-effect transistor of claim 1, wherein the JFET region has a width of less than about three micrometers.

4. (Original) The metal-oxide semiconductor field-effect transistor of claim 3, wherein the JFET region has a width of about one micrometer.

5. (Original) The metal-oxide semiconductor field-effect transistor of claim 1, wherein the third concentration of first type impurities is at least one order of magnitude greater than the second concentration of first type impurities.

6. (Cancelled)

7. (Previously Presented) The metal-oxide semiconductor field-effect transistor of claim 1, wherein the current spreading semiconductor layer has a fourth concentration of first type impurities that is greater than the second concentration of first type impurities.

8. (Original) The metal-oxide semiconductor field-effect transistor of claim 7, wherein the fourth concentration of first type impurities is at least one order of magnitude greater than the second concentration of first type impurities.

9. (Previously Presented) The metal-oxide semiconductor field-effect transistor of claim 8, wherein the JFET region has a width of about one micrometer.

10. (Original) The metal-oxide semiconductor field-effect transistor of claim 1, further comprising a plurality of base contact regions formed in each of the first and the second source regions, the base contact regions being smaller than the first and second source regions.

11. (Cancelled)

12. (Previously Presented) A double-implanted metal-oxide semiconductor field-effect transistor comprising:

a silicon-carbide substrate;

a drift semiconductor layer formed on a front side of the semiconductor substrate;

a first source region;

a first source electrode formed over the first source region, the first source electrode defining a longitudinal axis;

a plurality of first base contact regions defined in the first source region, each of the plurality of first base contact regions being spaced apart from each other in a direction parallel to the longitudinal axis defined by the first source electrode;

a second source region;

a second source electrode formed over the second source region, the second source electrode defining a longitudinal axis;

a plurality of second base contact regions defined in the second source region, each of the plurality of second base contact regions being spaced apart from each other in a direction parallel to the longitudinal axis defined by the second source electrode; and

a JFET region defined between the first source region and the second source region, the JFET region having a width less than about three micrometers.

13. (Original) The double-implanted metal-oxide semiconductor field-effect transistor of claim 12, wherein the JFET region has a width of about one micrometer.

14. (Original) The double-implanted metal-oxide semiconductor field-effect transistor of claim 12, wherein the JFET region has a first concentration of first type impurities and the drift semiconductor layer has a second concentration of first type impurities, the first concentration of first type impurities being greater than the second concentration of first type impurities.

15-16. (Cancelled)

17. (Previously Presented) A double-implanted metal-oxide semiconductor field-effect transistor comprising:

a semiconductor substrate;

a drift semiconductor layer formed on a front side of the semiconductor substrate;

a current spreading semiconductor layer formed on a front side of the drift semiconductor layer;

a plurality of first and second source regions;

a plurality of base contact regions; and

a JFET region defined between the plurality of first source regions and the plurality of second source regions, the JFET region being formed on a front side of the current spreading semiconductor layer,

wherein the plurality of first and second source regions and the plurality of base contact regions form alternating strips of N-type doped regions and P-type doped regions, each of the alternating strips defining a longitudinal axis that is substantially orthogonal to a longitudinal axis defined by respective source electrodes formed over the first and the second source regions.

18. (Original) The double-implanted metal-oxide semiconductor field-effect transistor of claim 17, wherein the current spreading semiconductor layer has a first concentration of first type impurities and the drift semiconductor layer has a second concentration of first type impurities, the first concentration of first type impurities being greater than the second concentration of first type impurities.

19. (Original) The double-implanted metal-oxide semiconductor field-effect transistor of claim 18, wherein the first concentration of first type impurities is at least one order of magnitude greater than the second concentration of first type impurities.

20. (Original) The double-implanted metal-oxide semiconductor field-effect transistor of claim 17, wherein the JFET region has a width of about three micrometers or less.

21-23. (Cancelled)

REMARKS

Applicants thank the Examiner for consideration of the present application. This response is filed in response to the Office Action, dated June 25, 2008, to place this application in condition for allowance as suggested by the Examiner. In the 06/25/08 Final Office Action, the Examiner rejected claims 1, 3-5, and 7-10. The Examiner objected to claim 11, but indicated that this claim would be allowable if rewritten to include all the limitations of the base claim. Applicants note with appreciation the Examiner's indication that claims 12-14 and claims 17-20 are in condition for allowance. By this amendment, claim 1 is amended and claims 11 and 23 are cancelled.

DISCUSSION: Independent Claim 1

Claim 1 has been amended to include each element of claim 11. As such, claim 1 is believed to be in condition for allowance and such action is respectfully requested. In addition, claims 1, 3-5, and 7-10 each include claim 1 as a base claim. Accordingly, each of claims 1, 3-5, 7-10 is also believed to be in condition for allowance and such action is respectfully requested.

CONCLUSION

In view of the foregoing, it is submitted that this application is in a condition for allowance. Action to that end is hereby solicited. If there are any questions or comments that would speed prosecution of this application, the Examiner is invited to call the undersigned at (317) 261-7959.

It is respectfully requested that, if necessary to effect a timely response, this paper be considered as a Petition for an Extension of Time sufficient to effect a timely response. The

Commissioner is hereby authorized to charge the fee for such Petition and any shortage of fees, and credit any overpayment of fees, to the Account of Barnes & Thornburg, Deposit Account No. 10-0435 with reference to file 3220-79132.

Respectfully submitted,

BARNES & THORNBURG LLP



Glen M. Kellett
Registration No. 60,202
Barnes & Thornburg
11 South Meridian Street
Indianapolis, Indiana 46204-3535
Telephone: (317) 261-7959
Fax: (317) 231-7433

Electronic Acknowledgement Receipt

EFS ID:	3826562
Application Number:	11338007
International Application Number:	
Confirmation Number:	4085
Title of Invention:	High-voltage power semiconductor device
First Named Inventor/Applicant Name:	James A. Cooper
Customer Number:	23643
Filer:	Glen Madison Kellett
Filer Authorized By:	
Attorney Docket Number:	3220-79132
Receipt Date:	22-AUG-2008
Filing Date:	23-JAN-2006
Time Stamp:	16:26:42
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	no
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File Listing:

Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1	Amendment - After Non-Final Rejection	Response.pdf	226875 a3cc8616bcc296493636340871e6c418f8718bca	no	9

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If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application.

National Stage of an International Application under 35 U.S.C. 371

If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.

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If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.

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PATENT APPLICATION FEE DETERMINATION RECORD Substitute for Form PTO-875					Application or Docket Number 11/338,007		Filing Date 01/23/2006		<input type="checkbox"/> To be Mailed	
APPLICATION AS FILED – PART I										
(Column 1)			(Column 2)		SMALL ENTITY <input type="checkbox"/> OR		OTHER THAN SMALL ENTITY			
FOR	NUMBER FILED	NUMBER EXTRA	RATE (\$)	FEE (\$)	OR	RATE (\$)	FEE (\$)			
<input type="checkbox"/> BASIC FEE (37 CFR 1.16(a), (b), or (c))	N/A	N/A	N/A			N/A				
<input type="checkbox"/> SEARCH FEE (37 CFR 1.16(k), (l), or (m))	N/A	N/A	N/A			N/A				
<input type="checkbox"/> EXAMINATION FEE (37 CFR 1.16(o), (p), or (q))	N/A	N/A	N/A			N/A				
TOTAL CLAIMS (37 CFR 1.16(i))	minus 20 =	*	X \$	=		X \$	=			
INDEPENDENT CLAIMS (37 CFR 1.16(h))	minus 3 =	*	X \$	=		X \$	=			
<input type="checkbox"/> APPLICATION SIZE FEE (37 CFR 1.16(s))	If the specification and drawings exceed 100 sheets of paper, the application size fee due is \$250 (\$125 for small entity) for each additional 50 sheets or fraction thereof. See 35 U.S.C. 41(a)(1)(G) and 37 CFR 1.16(s).									
<input type="checkbox"/> MULTIPLE DEPENDENT CLAIM PRESENT (37 CFR 1.16(j))										
* If the difference in column 1 is less than zero, enter "0" in column 2.			TOTAL			TOTAL				
APPLICATION AS AMENDED – PART II										
(Column 1)		(Column 2)		(Column 3)		SMALL ENTITY OR		OTHER THAN SMALL ENTITY		
AMENDMENT	08/22/2008	CLAIMS REMAINING AFTER AMENDMENT		HIGHEST NUMBER PREVIOUSLY PAID FOR	PRESENT EXTRA	RATE (\$)	ADDITIONAL FEE (\$)	OR	RATE (\$)	ADDITIONAL FEE (\$)
	Total (37 CFR 1.16(i))	* 15	Minus	** 20	= 0	X \$	=		X \$50=	0
	Independent (37 CFR 1.16(h))	* 3	Minus	***4	= 0	X \$	=		X \$210=	0
	<input type="checkbox"/> Application Size Fee (37 CFR 1.16(s))									
	<input type="checkbox"/> FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))									
						TOTAL ADD'L FEE			OR	TOTAL ADD'L FEE
(Column 1)		(Column 2)		(Column 3)		SMALL ENTITY OR		OTHER THAN SMALL ENTITY		
AMENDMENT		CLAIMS REMAINING AFTER AMENDMENT		HIGHEST NUMBER PREVIOUSLY PAID FOR	PRESENT EXTRA	RATE (\$)	ADDITIONAL FEE (\$)	OR	RATE (\$)	ADDITIONAL FEE (\$)
	Total (37 CFR 1.16(i))	*	Minus	**	=	X \$	=		X \$	=
	Independent (37 CFR 1.16(h))	*	Minus	***	=	X \$	=		X \$	=
	<input type="checkbox"/> Application Size Fee (37 CFR 1.16(s))									
	<input type="checkbox"/> FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))									
						TOTAL ADD'L FEE			OR	TOTAL ADD'L FEE
<p>* If the entry in column 1 is less than the entry in column 2, write "0" in column 3.</p> <p>** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 20, enter "20".</p> <p>*** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 3, enter "3".</p> <p>The "Highest Number Previously Paid For" (Total or Independent) is the highest number found in the appropriate box in column 1.</p>										

Legal Instrument Examiner:
/MARSHA R. RICHARDS/

This collection of information is required by 37 CFR 1.16. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 12 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

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23643 7590 12/17/2008

BARNES & THORNBURG LLP
11 SOUTH MERIDIAN
INDIANAPOLIS, IN 46204

EXAMINER

PATTON, PAUL E

ART UNIT

PAPER NUMBER

2822

DATE MAILED: 12/17/2008

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
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11/338,007

01/23/2006

James A. Cooper

3220-79132

4085

TITLE OF INVENTION: HIGH-VOLTAGE POWER SEMICONDUCTOR DEVICE

APPLN. TYPE	SMALL ENTITY	ISSUE FEE DUE	PUBLICATION FEE DUE	PREV. PAID ISSUE FEE	TOTAL FEE(S) DUE	DATE DUE
nonprovisional	NO	\$1510	\$300	\$0	\$1810	03/17/2009

THE APPLICATION IDENTIFIED ABOVE HAS BEEN EXAMINED AND IS ALLOWED FOR ISSUANCE AS A PATENT. PROSECUTION ON THE MERITS IS CLOSED. THIS NOTICE OF ALLOWANCE IS NOT A GRANT OF PATENT RIGHTS. THIS APPLICATION IS SUBJECT TO WITHDRAWAL FROM ISSUE AT THE INITIATIVE OF THE OFFICE OR UPON PETITION BY THE APPLICANT. SEE 37 CFR 1.313 AND MPEP 1308.

THE ISSUE FEE AND PUBLICATION FEE (IF REQUIRED) MUST BE PAID WITHIN THREE MONTHS FROM THE MAILING DATE OF THIS NOTICE OR THIS APPLICATION SHALL BE REGARDED AS ABANDONED. THIS STATUTORY PERIOD CANNOT BE EXTENDED. SEE 35 U.S.C. 151. THE ISSUE FEE DUE INDICATED ABOVE DOES NOT REFLECT A CREDIT FOR ANY PREVIOUSLY PAID ISSUE FEE IN THIS APPLICATION. IF AN ISSUE FEE HAS PREVIOUSLY BEEN PAID IN THIS APPLICATION (AS SHOWN ABOVE), THE RETURN OF PART B OF THIS FORM WILL BE CONSIDERED A REQUEST TO REAPPLY THE PREVIOUSLY PAID ISSUE FEE TOWARD THE ISSUE FEE NOW DUE.

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A. If the status is the same, pay the TOTAL FEE(S) DUE shown above.

B. If the status above is to be removed, check box 5b on Part B - Fee(s) Transmittal and pay the PUBLICATION FEE (if required) and twice the amount of the ISSUE FEE shown above, or

If the SMALL ENTITY is shown as NO:

A. Pay TOTAL FEE(S) DUE shown above, or

B. If applicant claimed SMALL ENTITY status before, or is now claiming SMALL ENTITY status, check box 5a on Part B - Fee(s) Transmittal and pay the PUBLICATION FEE (if required) and 1/2 the ISSUE FEE shown above.

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23643 7590 12/17/2008

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(Depositor's name)
(Signature)
(Date)

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
-----------------	-------------	----------------------	---------------------	------------------

11/338,007 01/23/2006 James A. Cooper 3220-79132 4085

TITLE OF INVENTION: HIGH-VOLTAGE POWER SEMICONDUCTOR DEVICE

APPLN. TYPE	SMALL ENTITY	ISSUE FEE DUE	PUBLICATION FEE DUE	PREV. PAID ISSUE FEE	TOTAL FEE(S) DUE	DATE DUE
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nonprovisional NO \$1510 \$300 \$0 \$1810 03/17/2009

EXAMINER	ART UNIT	CLASS-SUBCLASS
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PATTON, PAUL E 2822 257-341000

1. Change of correspondence address or indication of "Fee Address" (37 CFR 1.363).

- ☐ Change of correspondence address (or Change of Correspondence Address form PTO/SB/122) attached.
- ☐ "Fee Address" indication (or "Fee Address" Indication form PTO/SB/47; Rev 03-02 or more recent) attached. **Use of a Customer Number is required.**

2. For printing on the patent front page, list

- (1) the names of up to 3 registered patent attorneys or agents OR, alternatively, 1 _____
- (2) the name of a single firm (having as a member a registered attorney or agent) and the names of up to 2 registered patent attorneys or agents. If no name is listed, no name will be printed. 2 _____
- 3 _____

3. ASSIGNEE NAME AND RESIDENCE DATA TO BE PRINTED ON THE PATENT (print or type)

PLEASE NOTE: Unless an assignee is identified below, no assignee data will appear on the patent. If an assignee is identified below, the document has been filed for recordation as set forth in 37 CFR 3.11. Completion of this form is NOT a substitute for filing an assignment.

(A) NAME OF ASSIGNEE (B) RESIDENCE: (CITY and STATE OR COUNTRY)

Please check the appropriate assignee category or categories (will not be printed on the patent) : ☐ Individual ☐ Corporation or other private group entity ☐ Government

4a. The following fee(s) are submitted:

- ☐ Issue Fee
- ☐ Publication Fee (No small entity discount permitted)
- ☐ Advance Order - # of Copies _____

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- ☐ A check is enclosed.
- ☐ Payment by credit card. Form PTO-2038 is attached.
- ☐ The Director is hereby authorized to charge the required fee(s), any deficiency, or credit any overpayment, to Deposit Account Number _____ (enclose an extra copy of this form).

5. Change in Entity Status (from status indicated above)

- ☐ a. Applicant claims SMALL ENTITY status. See 37 CFR 1.27. ☐ b. Applicant is no longer claiming SMALL ENTITY status. See 37 CFR 1.27(g)(2).

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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
11/338,007	01/23/2006	James A. Cooper	3220-79132	4085
23643	7590	12/17/2008	EXAMINER	
BARNES & THORNBURG LLP 11 SOUTH MERIDIAN INDIANAPOLIS, IN 46204			PATTON, PAUL E	
			ART UNIT	PAPER NUMBER
			2822	
DATE MAILED: 12/17/2008				

Determination of Patent Term Adjustment under 35 U.S.C. 154 (b) (application filed on or after May 29, 2000)

The Patent Term Adjustment to date is 0 day(s). If the issue fee is paid on the date that is three months after the mailing date of this notice and the patent issues on the Tuesday before the date that is 28 weeks (six and a half months) after the mailing date of this notice, the Patent Term Adjustment will be 0 day(s).

If a Continued Prosecution Application (CPA) was filed in the above-identified application, the filing date that determines Patent Term Adjustment is the filing date of the most recent CPA.

Applicant will be able to obtain more detailed information by accessing the Patent Application Information Retrieval (PAIR) WEB site (<http://pair.uspto.gov>).

Any questions regarding the Patent Term Extension or Adjustment determination should be directed to the Office of Patent Legal Administration at (571)-272-7702. Questions relating to issue and publication fee payments should be directed to the Customer Service Center of the Office of Patent Publication at 1-(888)-786-0101 or (571)-272-4200.

Notice of Allowability	Application No.	Applicant(s)	
	11/338,007	COOPER ET AL.	
	Examiner	Art Unit	
	PAUL E. PATTON	2822	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address--

All claims being allowable, PROSECUTION ON THE MERITS IS (OR REMAINS) CLOSED in this application. If not included herewith (or previously mailed), a Notice of Allowance (PTOL-85) or other appropriate communication will be mailed in due course. **THIS NOTICE OF ALLOWABILITY IS NOT A GRANT OF PATENT RIGHTS.** This application is subject to withdrawal from issue at the initiative of the Office or upon petition by the applicant. See 37 CFR 1.313 and MPEP 1308.

1. ☒ This communication is responsive to amendment filed August 22, 2008..
2. ☒ The allowed claim(s) is/are 1,3-5,7-10,12-14 and 17-20.
3. ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
 - a) ☐ All b) ☐ Some* c) ☐ None of the:
 1. ☐ Certified copies of the priority documents have been received.
 2. ☐ Certified copies of the priority documents have been received in Application No. ____.
 3. ☐ Copies of the certified copies of the priority documents have been received in this national stage application from the International Bureau (PCT Rule 17.2(a)).
 - * Certified copies not received: ____.

Applicant has THREE MONTHS FROM THE "MAILING DATE" of this communication to file a reply complying with the requirements noted below. Failure to timely comply will result in ABANDONMENT of this application.

THIS THREE-MONTH PERIOD IS NOT EXTENDABLE.

4. ☐ A SUBSTITUTE OATH OR DECLARATION must be submitted. Note the attached EXAMINER'S AMENDMENT or NOTICE OF INFORMAL PATENT APPLICATION (PTO-152) which gives reason(s) why the oath or declaration is deficient.
5. ☐ CORRECTED DRAWINGS (as "replacement sheets") must be submitted.
 - (a) ☐ including changes required by the Notice of Draftsperson's Patent Drawing Review (PTO-948) attached
 - 1) ☐ hereto or 2) ☐ to Paper No./Mail Date ____.
 - (b) ☐ including changes required by the attached Examiner's Amendment / Comment or in the Office action of Paper No./Mail Date ____.

Identifying indicia such as the application number (see 37 CFR 1.84(c)) should be written on the drawings in the front (not the back) of each sheet. Replacement sheet(s) should be labeled as such in the header according to 37 CFR 1.121(d).
6. ☐ DEPOSIT OF and/or INFORMATION about the deposit of BIOLOGICAL MATERIAL must be submitted. Note the attached Examiner's comment regarding REQUIREMENT FOR THE DEPOSIT OF BIOLOGICAL MATERIAL.

Attachment(s)

- | | |
|--|--|
| <ol style="list-style-type: none"> 1. <input type="checkbox"/> Notice of References Cited (PTO-892) 2. <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948) 3. <input type="checkbox"/> Information Disclosure Statements (PTO/SB/08),
Paper No./Mail Date ____ 4. <input type="checkbox"/> Examiner's Comment Regarding Requirement for Deposit
of Biological Material | <ol style="list-style-type: none"> 5. <input type="checkbox"/> Notice of Informal Patent Application 6. <input type="checkbox"/> Interview Summary (PTO-413),
Paper No./Mail Date ____. 7. <input type="checkbox"/> Examiner's Amendment/Comment 8. <input checked="" type="checkbox"/> Examiner's Statement of Reasons for Allowance 9. <input type="checkbox"/> Other ____. |
|--|--|

DETAILED ACTION

Response to Amendment

1. Acknowledgement is made of Amendment filed August 22, 2008.

Allowable Subject Matter

2. Claims 1, 3-5, 7-10, 12-14 and 17-20 are allowed.
3. The following is an examiner's statement of reasons for allowance: The prior art of record taken alone or in combination fails to anticipate or render obvious a plurality of source regions and a plurality of base contact regions forming alternating strips of N-type doped regions and P-type doped regions, the alternating strips being substantially orthogonal to respective source electrodes formed over the first and the second source regions along with all the other limitations as recited in independent claims 1 and 17; or a first source electrode formed over the first source region, the first source electrode defining a longitudinal axis; a plurality of first base contact regions defined in the first source region, each of the plurality of first base contact regions being spaced apart from each other in a direction parallel to the longitudinal axis defined by the first source electrode; a second source region; a second source electrode formed over the second source region, the second source electrode defining a longitudinal axis; a plurality of second base contact regions defined in the second source region, each of the plurality of second base contact regions being spaced apart from each other in a direction parallel to the longitudinal axis defined by the second source electrode, along with all the other limitations of claim 12..

Any comments considered necessary by applicant must be submitted no later than the payment of the issue fee and, to avoid processing delays, should preferably accompany the issue fee. Such submissions should be clearly labeled "Comments on Statement of Reasons for Allowance."

Any inquiry concerning this communication or earlier communications from the examiner should be directed to PAUL E. PATTON whose telephone number is (571)272-9762. The examiner can normally be reached on 7:00 - 5:30 Monday through Thursday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Zandra Smith can be reached on 571-272-2429. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.


/Zandra V. Smith/
Supervisory Patent Examiner, Art Unit 2822

Paul E Patton
Examiner
Art Unit 2822

Application/Control Number: 11/338,007
Art Unit: 2822

Page 4

/P. E. P./
Examiner, Art Unit 2822

Search Notes 	Application/Control No. 11338007	Applicant(s)/Patent Under Reexamination COOPER ET AL.
	Examiner Patton, Paul E	Art Unit 2822

SEARCHED			
Class	Subclass	Date	Examiner
257	263, 256, 341, 342, 335, 339, 350, 263,	3/22/2007	PEP
438	142, 156, 176, 186, 197, 268	3/22/2007	PEP

SEARCH NOTES		
Search Notes	Date	Examiner
Search history attached	2/26/2007	PEP
Updated Search	10/2/2007	PEP
Consult with M. Prenty	10/2/2007	PEP
Consult with M. Prenty	5/30/2008	PEP
Updated search	5/30/2008	PEP
Updated Search	11/25/2008	PEP
Consult with M. Prenty	11/25/2008	PEP

INTERFERENCE SEARCH			
Class	Subclass	Date	Examiner
257	ALL	11/25/2008	PEP

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BIB DATA SHEET

CONFIRMATION NO. 4085

SERIAL NUMBER 11/338,007	FILING or 371(c) DATE 01/23/2006 RULE	CLASS 257	GROUP ART UNIT 2822	ATTORNEY DOCKET NO. 3220-79132		
APPLICANTS James A. Cooper, West Lafayette, IN; Asmita Saha, West Lafayette, IN; ** CONTINUING DATA ***** This appln claims benefit of 60/646,152 01/21/2005 ** FOREIGN APPLICATIONS ***** ** IF REQUIRED, FOREIGN FILING LICENSE GRANTED ** 03/01/2006						
Foreign Priority claimed <input type="checkbox"/> Yes <input checked="" type="checkbox"/> No 35 USC 119(a-d) conditions met <input type="checkbox"/> Yes <input checked="" type="checkbox"/> No Verified and Acknowledged <u>/PAUL E PATTON/</u> Examiner's Signature		<input type="checkbox"/> Met after Allowance PEP Initials	STATE OR COUNTRY IN	SHEETS DRAWINGS 4	TOTAL CLAIMS 23	INDEPENDENT CLAIMS 4
ADDRESS BARNES & THORNBURG LLP 11 SOUTH MERIDIAN INDIANAPOLIS, IN 46204 UNITED STATES						
TITLE High-voltage power semiconductor device						
FILING FEE RECEIVED 1480	FEES: Authority has been given in Paper No. _____ to charge/credit DEPOSIT ACCOUNT No. _____ for following:		<input type="checkbox"/> All Fees			
			<input type="checkbox"/> 1.16 Fees (Filing)			
			<input type="checkbox"/> 1.17 Fees (Processing Ext. of time)			
			<input type="checkbox"/> 1.18 Fees (Issue)			
			<input type="checkbox"/> Other _____			
			<input type="checkbox"/> Credit			

EAST Search History

Ref #	Hits	Search Query	DBs	Default Operator	Plurals	Time Stamp
L1	5225	((257/263) or (257/256) or (257/341) or (257/342) or (257/335) or (257/339) or (257/350)).CCLS.	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2008/11/25 16:26
L2	4227	((438/142) or (438/156) or (438/176) or (438/186) or (438/197) or (438/268)).CCLS.	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2008/11/25 16:26
L3	9258	L1 L2	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2008/11/25 16:26
L4	196068	MOSFET ("metal oxide semiconductor")	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2008/11/25 16:26
L5	12566	Drift near5 (layer region)	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2008/11/25 16:26
L6	230967	L4 amd L5 and (dop\$3 concentrat\$3 dos\$3)	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2008/11/25 16:26
L7	4805	L6 and L3	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2008/11/25 16:26

L8	87	L7 and current near5 spread\$3	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2008/11/25 16:26
L9	0	(metal and oxide and field and effect and transistor and silicon and carbide and concentration and impurities and drift and layer and formed and front and side and current and spreading and first and source and second and region and jfet and defined and between and third and alternating and strips and orthogonal and respective).clm. and "257".clas.	US-PGPUB	OR	ON	2008/11/25 17:20
S1	1393	((Cooper near (James J)) (Saha near (Asmita A))). in.	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2007/03/22 10:54
S2	380394	"257".clas.	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2007/03/22 09:01
S3	7	S1 and S2	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2007/03/22 09:01
S4	4717	((257/263) or (257/256) or (257/341) or (257/342) or (257/335) or (257/339) or (257/350)).CCLS.	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2007/03/22 10:55
S5	3327	((438/142) or (438/156) or (438/176) or (438/186) or (438/197) or (438/268)).CCLS.	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2007/03/22 10:56

S6	7886	S4 S5	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2007/03/22 11:03
S7	156976	MOSFET ("metal oxide semiconductor")	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2007/03/22 11:04
S8	5305	DMOS	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2007/03/22 11:04
S9	304	Double adj implant	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2007/03/22 11:04
S10	57449	power same (FET "Field effect")	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2007/03/22 11:06
S11	8478	JFET ("Junction Field Effect")	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2007/03/22 11:07
S12	3533	current near spread\$3	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2007/03/23 10:28
S13	10361	Drift near5 (layer region)	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2007/03/22 11:10

S14	0	S6 and S7 and S9 and S10 and S11 and S12 and S13	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2007/03/22 11:12
S15	20	S7 and S12 and S13 and S6	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2007/03/22 11:13
S16	80	S7 and S12 and S13	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2007/03/22 11:34
S17	0	S16 and S9	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2007/03/22 11:14
S18	180117	siC (Silicon adj carbide)	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2007/03/22 11:35
S19	548	S11 and S13 and S7	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2007/03/22 14:11
S20	202	S19 and S6	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2007/03/23 12:53
S21	1125	257/341.ccls.	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2007/03/22 15:36

S22	145	S21 and S11	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2007/03/22 15:36
S23	16	S21 and S12	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2007/03/22 15:58
S24	49	S6 and S12	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2007/03/22 16:11
S25	628	S6 and S18	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2007/03/22 16:12
S26	92	S21 and S18	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2007/03/22 16:12
S27	1121	current near spread\$3 near5 layer	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2007/03/23 10:29
S28	1125	257/341.ccls.	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2007/03/23 10:29
S29	6	S27 and S28	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2007/03/23 10:32

S30	4717	((257/263) or (257/256) or (257/341) or (257/342) or (257/335) or (257/339) or (257/350)).CCLS.	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2007/03/23 10:32
S31	3327	((438/142) or (438/156) or (438/176) or (438/186) or (438/197) or (438/268)).CCLS.	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2007/03/23 10:32
S32	7886	S30 S31	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2007/03/23 10:32
S33	12	S27 and S32	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2007/03/23 10:32
S34	156976	MOSFET ("metal oxide semiconductor")	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2007/03/23 12:47
S35	8478	JFET ("Junction Field Effect")	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2007/03/23 12:47
S36	10361	Drift near5 (layer region)	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2007/03/23 12:47
S37	548	S35 and S36 and S34	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2007/03/23 12:47

S38	202	S37 and S32	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2007/03/23 12:47
S39	195	S38 and dop\$3	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2007/03/23 14:03
S40	187432	S34 amd S36 and (dop\$3 concentrat\$3 dos\$3)	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2007/03/23 14:06
S41	4013	S40 and S32	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2007/03/23 14:07
S42	436	S41 and S35	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2007/03/23 15:25
S43	4	S42 and S27	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2007/03/23 15:25
S44	5	S42 and current near5 spread	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2007/03/23 15:27
S45	36	S41 and current near5 spread	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2007/03/26 08:21

S46	2	("5688725").PN.	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2007/03/23 15:50
S47	5	("4941026" "5341011" "5424231" "5532179" "5558313").PN.	US-PGPUB; USPAT; USOCR	OR	ON	2007/03/26 08:12
S48	2	("4941026").PN.	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2007/03/26 08:12
S49	4717	((257/263) or (257/256) or (257/341) or (257/342) or (257/335) or (257/339) or (257/350)).CCLS.	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2007/03/26 08:21
S50	3327	((438/142) or (438/156) or (438/176) or (438/186) or (438/197) or (438/268)).CCLS.	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2007/03/26 08:21
S51	7886	S49 S50	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2007/03/26 08:21
S52	157110	MOSFET ("metal oxide semiconductor")	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2007/03/26 08:21
S53	10368	Drift near5 (layer region)	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2007/03/26 08:21
S54	187573	S52 amd S53 and (dop\$3 concentrat\$3 dos\$3)	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2007/03/26 08:21

S55	4013	S54 and S51	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2007/03/26 08:21
S56	72	S55 and current near5 spread\$3	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2007/03/26 08:22
S57	5095	((257/263) or (257/256) or (257/341) or (257/342) or (257/335) or (257/339) or (257/350)).CCLS.	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2008/05/30 10:55
S58	3980	((438/142) or (438/156) or (438/176) or (438/186) or (438/197) or (438/268)).CCLS.	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2008/05/30 10:55
S59	8894	S57 S58	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2008/05/30 10:55
S60	8029	@ad< "20060123" and S59	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2008/05/30 10:55
S61	1642	S60 and (parallel strip longitud\$4) same source	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2008/05/30 10:56
S62	448	S60 and (parallel strip longitud\$4) same (source near3 electrode)	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2008/05/30 10:57

11/ 25/ 2008 5:20:37 PM

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ART B - FEE(S) TRANSMITTAL

Complete and send this form, together with applicable fee(s), to: **Mail** **Mail Stop ISSUE FEE**
Commissioner for Patents
P.O. Box 1450
Alexandria, Virginia 22313-1450
 or **Fax** **(571)-273-2885**

INSTRUCTIONS: This form should be used for transmitting the ISSUE FEE and PUBLICATION FEE (if required). Blocks 1 through 5 should be completed where appropriate. All further correspondence including the Patent, advance orders and notification of maintenance fees will be mailed to the current correspondence address as indicated unless corrected below or directed otherwise in Block 1, by (a) specifying a new correspondence address; and/or (b) indicating a separate "FEE ADDRESS" for maintenance fee notifications.

CURRENT CORRESPONDENCE ADDRESS (Note: Use Block 1 for any change of address)

23643 7590 12/17/2008

BARNES & THORNBURG LLP
11 SOUTH MERIDIAN
INDIANAPOLIS, IN 46204

Note: A certificate of mailing can only be used for domestic mailings of the Fee(s) Transmittal. This certificate cannot be used for any other accompanying papers. Each additional paper, such as an assignment or formal drawing, must have its own certificate of mailing or transmission.

Certificate of Mailing or Transmission

I hereby certify that this Fee(s) Transmittal is being deposited with the United States Postal Service with sufficient postage for first class mail in an envelope addressed to the Mail Stop ISSUE FEE address above, or being facsimile transmitted to the USPTO (571) 273-2885, on the date indicated below.

(Depositor's name)
(Signature)
(Date)

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
11/338,007	01/23/2006	James A. Cooper	3220-79132	4085

TITLE OF INVENTION: HIGH-VOLTAGE POWER SEMICONDUCTOR DEVICE

APPLN. TYPE	SMALL ENTITY	ISSUE FEE DUE	PUBLICATION FEE DUE	PREV. PAID ISSUE FEE	TOTAL FEE(S) DUE	DATE DUE
nonprovisional	NO	\$1510	\$300	\$0	\$1810	03/17/2009

EXAMINER	ART UNIT	CLASS-SUBCLASS
PATTON, PAULE	2822	257-341000

1. Change of correspondence address or indication of "Fee Address" (37 CFR 1.363).
☐ Change of correspondence address (or Change of Correspondence Address form PTO/SB/122) attached.
☐ "Fee Address" indication (or "Fee Address" Indication form PTO/SB/47; Rev 03-02 or more recent) attached. Use of a Customer Number is required.

2. For printing on the patent front page, list
 (1) the names of up to 3 registered patent attorneys or agents OR, alternatively,
 (2) the name of a single firm (having as a member a registered attorney or agent) and the names of up to 2 registered patent attorneys or agents. If no name is listed, no name will be printed.

1 Barnes & Thornburg LLP
 2 _____
 3 _____

3. ASSIGNEE NAME AND RESIDENCE DATA TO BE PRINTED ON THE PATENT (print or type)

PLEASE NOTE: Unless an assignee is identified below, no assignee data will appear on the patent. If an assignee is identified below, the document has been filed for recordation as set forth in 37 CFR 3.11. Completion of this form is NOT a substitute for filing an assignment.

(A) NAME OF ASSIGNEE

(B) RESIDENCE: (CITY and STATE OR COUNTRY)

Purdue Research Foundation

West Lafayette, IN

Please check the appropriate assignee category or categories (will not be printed on the patent): ☐ Individual ☒ Corporation or other private group entity ☐ Government

4a. The following fee(s) are submitted:

☒ Issue Fee
☒ Publication Fee (No small entity discount permitted)
☐ Advance Order - # of Copies _____

4b. Payment of Fee(s): (Please first reapply any previously paid issue fee shown above)

☐ A check is enclosed.
☐ Payment by credit card. Form PTO-2038 is attached.
☒ The Director is hereby authorized to charge the required fee(s), any deficiency, or credit any overpayment, to Deposit Account Number 100435 (enclose an extra copy of this form).

5. Change in Entity Status (from status indicated above)

☐ a. Applicant claims SMALL ENTITY status. See 37 CFR 1.27.

☐ b. Applicant is no longer claiming SMALL ENTITY status. See 37 CFR 1.27(g)(2).

NOTE: The Issue Fee and Publication Fee (if required) will not be accepted from anyone other than the applicant; a registered attorney or agent; or the assignee or other party in interest as shown by the records of the United States Patent and Trademark Office.

Authorized Signature [Signature]

Date January 23, 2009

Typed or printed name Glen M. Kellett

Registration No. 60202

This collection of information is required by 37 CFR 1.311. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 12 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, Virginia 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, Virginia 22313-1450.

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Electronic Patent Application Fee Transmittal

Application Number:	11338007			
Filing Date:	23-Jan-2006			
Title of Invention:	HIGH-VOLTAGE POWER SEMICONDUCTOR DEVICE			
First Named Inventor/Applicant Name:	James A. Cooper			
Filer:	Glen Madison Kellett/Cortney Drew			
Attorney Docket Number:	3220-79132			
Filed as Large Entity				
Utility under 35 USC 111(a) Filing Fees				
Description	Fee Code	Quantity	Amount	Sub-Total in USD(\$)
Basic Filing:				
Pages:				
Claims:				
Miscellaneous-Filing:				
Petition:				
Patent-Appeals-and-Interference:				
Post-Allowance-and-Post-Issuance:				
Utility Appl issue fee	1501	1	1510	1510
Publ. Fee- early, voluntary, or normal	1504	1	300	300

Description	Fee Code	Quantity	Amount	Sub-Total in USD(\$)
Extension-of-Time:				
Miscellaneous:				
Total in USD (\$)				1810

Electronic Acknowledgement Receipt

EFS ID:	4663270
Application Number:	11338007
International Application Number:	
Confirmation Number:	4085
Title of Invention:	HIGH-VOLTAGE POWER SEMICONDUCTOR DEVICE
First Named Inventor/Applicant Name:	James A. Cooper
Customer Number:	23643
Filer:	Glen Madison Kellett/Cortney Drew
Filer Authorized By:	Glen Madison Kellett
Attorney Docket Number:	3220-79132
Receipt Date:	23-JAN-2009
Filing Date:	23-JAN-2006
Time Stamp:	11:26:16
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	yes
Payment Type	Deposit Account
Payment was successfully received in RAM	\$ 1810
RAM confirmation Number	6804
Deposit Account	100435
Authorized User	

The Director of the USPTO is hereby authorized to charge indicated fees and credit any overpayment as follows:

Charge any Additional Fees required under 37 C.F.R. Section 1.16 (National application filing, search, and examination fees)

Charge any Additional Fees required under 37 C.F.R. Section 1.17 (Patent application and reexamination processing fees)

Charge any Additional Fees required under 37 C.F.R. Section 1.19 (Document supply fees)

Charge any Additional Fees required under 37 C.F.R. Section 1.20 (Post Issuance fees)

Charge any Additional Fees required under 37 C.F.R. Section 1.21 (Miscellaneous fees and charges)

File Listing:

Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1	Issue Fee Payment (PTO-85B)	Issue_Fee.pdf	113710	no	1
			6ccee97a0c1e3e88445e84c6856141145ee315b4		

Warnings:

Information:

2	Fee Worksheet (PTO-06)	fee-info.pdf	32146	no	2
			d578a3b9c9ad85604735e742332075be678737ed		

Warnings:

Information:

Total Files Size (in bytes):			145856
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This Acknowledgement Receipt evidences receipt on the noted date by the USPTO of the indicated documents, characterized by the applicant, and including page counts, where applicable. It serves as evidence of receipt similar to a Post Card, as described in MPEP 503.

New Applications Under 35 U.S.C. 111

If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application.

National Stage of an International Application under 35 U.S.C. 371

If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.

New International Application Filed with the USPTO as a Receiving Office

If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.



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APPLICATION NO.	ISSUE DATE	PATENT NO.	ATTORNEY DOCKET NO.	CONFIRMATION NO.
11/338,007	03/03/2009	7498633	3220-79132	4085

23643 7590 02/11/2009
BARNES & THORNBURG LLP
11 SOUTH MERIDIAN
INDIANAPOLIS, IN 46204

ISSUE NOTIFICATION

The projected patent number and issue date are specified above.

Determination of Patent Term Adjustment under 35 U.S.C. 154 (b) (application filed on or after May 29, 2000)

The Patent Term Adjustment is 0 day(s). Any patent to issue from the above-identified application will include an indication of the adjustment on the front page.

If a Continued Prosecution Application (CPA) was filed in the above-identified application, the filing date that determines Patent Term Adjustment is the filing date of the most recent CPA.

Applicant will be able to obtain more detailed information by accessing the Patent Application Information Retrieval (PAIR) WEB site (<http://pair.uspto.gov>).

Any questions regarding the Patent Term Extension or Adjustment determination should be directed to the Office of Patent Legal Administration at (571)-272-7702. Questions relating to issue and publication fee payments should be directed to the Customer Service Center of the Office of Patent Publication at (571)-272-4200.

APPLICANT(s) (Please see PAIR WEB site <http://pair.uspto.gov> for additional applicants):

James A. Cooper, West Lafayette, IN;
Asmita Saha, West Lafayette, IN;

AO 120 (Rev. 08/10)

TO: Mail Stop 8 Director of the U.S. Patent and Trademark Office P.O. Box 1450 Alexandria, VA 22313-1450	REPORT ON THE FILING OR DETERMINATION OF AN ACTION REGARDING A PATENT OR TRADEMARK
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In Compliance with 35 U.S.C. § 290 and/or 15 U.S.C. § 1116 you are hereby advised that a court action has been
 filed in the U.S. District Court Western District of Texas on the following

☐ Trademarks or ☒ Patents. (☐ the patent action involves 35 U.S.C. § 292.):

DOCKET NO. 6:21-cv-00727	DATE FILED 7/14/2021	U.S. DISTRICT COURT Western District of Texas
PLAINTIFF The Trustees of Purdue University		DEFENDANT STMicroelectronics N.V. and STMicroelectronics, Inc.
PATENT OR TRADEMARK NO.	DATE OF PATENT OR TRADEMARK	HOLDER OF PATENT OR TRADEMARK
1 7,498,633	3/3/2009	The Trustees of Purdue University
2 8,035,112	10/11/2011	The Trustees of Purdue University
3		
4		
5		

In the above—entitled case, the following patent(s)/ trademark(s) have been included:

DATE INCLUDED	INCLUDED BY <input type="checkbox"/> Amendment <input type="checkbox"/> Answer <input type="checkbox"/> Cross Bill <input type="checkbox"/> Other Pleading	
PATENT OR TRADEMARK NO.	DATE OF PATENT OR TRADEMARK	HOLDER OF PATENT OR TRADEMARK
1		
2		
3		
4		
5		

In the above—entitled case, the following decision has been rendered or judgement issued:

DECISION/JUDGEMENT

CLERK	(BY) DEPUTY CLERK	DATE
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Copy 1—Upon initiation of action, mail this copy to Director Copy 3—Upon termination of action, mail this copy to Director
 Copy 2—Upon filing document adding patent(s), mail this copy to Director Copy 4—Case file copy