IN THE UNITED STATES DISTRICT COURT
FOR THE WESTERN DISTRICT OF TEXAS
WACO DIVISION

THE TRUSTEES OF PURDUE UNIVERSITY, Plaintiff, vs. STMICROELECTRONICS N.V., STMICROELECTRONICS INTERNATIONAL N.V., AND STMICROELECTRONICS, INC. Defendants.	CASE NO. 6:21–CV–727-ADA JURY TRIAL DEMANDED

DEFENDANTS' PRELIMINARY INVALIDITY CONTENTIONS

I. INTRODUCTION

Pursuant to the Court's Scheduling Order [ECF 45], Defendants STMicroelectronics N.V. and STMicroelectronics, Inc.[1] hereby serve these Preliminary Invalidity Contentions on Plaintiff, The Trustees of Purdue University ("Plaintiff" or "Purdue"), regarding the Asserted Claims of U.S. Patent Nos. 7,498,633 ("the '633 Patent") and 8,035,112 ("the '112 Patent") (collectively, the "Asserted Patents").

Plaintiff purports to assert the following claims of the Asserted Patents against Defendants in this case (collectively, the "Asserted Claims"):

Patent	Asserted Claims
the '633 Patent	Claim 9
the '112 Patent	claims 1, 6, 7, 10, 11, and 12

Defendants hereby provide their disclosures pertaining only to the Asserted Claims identified by Plaintiff in its Infringement Contentions. To the extent Plaintiff later attempts to assert additional claims against any Defendant, such Defendant reserves the right to amend its Invalidity Contentions and contend that any additional claims are also invalid. Defendants' Invalidity Contentions are not an admission of validity as to any other claims of the Asserted Patents.

Defendants' preliminary invalidity contentions are based on information reasonably available at this time with respect to the Asserted Claim(s), and are necessarily preliminary and may require subsequent amendment, modification, and/or supplementation.

Defendants reserve the right to amend, modify, and/or supplement these invalidity contentions based on, among other things, amendments, modifications, or supplements to

[1] STMicroelectronics N.V. is not subject to the Court's jurisdiction, as detailed in its Motion to Dismiss [ECF 38]. And STMicroelectronics International N.V. has not yet been served in this case and therefore is not properly before the Court and not subject to the Court's jurisdiction.

Plaintiff's Infringement Contentions, further investigation, third-party discovery, fact or expert discovery, and/or evaluation of the scope and content of the prior art (including, for example, the prior art from all other cases in which Plaintiff asserts one or more of the Asserted Patents), disclosure of the parties' claim constructions, an order construing the Asserted Claims, new developments in the case, or any other basis contemplated by the Federal Rules of Civil Procedure, the Court's Local Rules, and any other applicable order entered by the Court.

Moreover, general fact discovery has not yet opened, and Defendants have not obtained deposition testimony from any of the named inventors of the Asserted Patents or any third party, including, without limitation, deposition of any third party whose products or technologies are identified by Plaintiff in its Infringement Contentions. Defendants expect discovery will reveal additional prior art, including related disclosures and corresponding evidence for many of the prior art references identified herein. As such, Defendants have not yet completed their investigation, discovery, or analysis of matters relating to the validity or enforceability of the Asserted Claim(s), including, without limitation, invalidity due to on-sale statutory bars, public use statutory bars, improper inventorship, or unenforceability due to inequitable conduct. The disclosures herein are not and should not be construed as a statement that no other persons have discoverable information, that no other documents, data compilations, and/or tangible things exist that any Defendant may use to support its claims or defenses, or that no other legal theories or factual bases will be pursued. Accordingly, Defendants reserve the right to amend, modify, and/or supplement these invalidity contentions as additional information is discovered, identified, or otherwise appreciated, including testimony about the scope and content of the prior art and the claimed inventions.

These Preliminary Invalidity Contentions are based on Defendants' present understanding of Plaintiff's Infringement Contentions served on such Defendants on October 25, 2021. Nothing in these Preliminary Invalidity Contentions should be regarded as conceding that Plaintiff's infringement contentions are legally or factually adequate or as necessarily reflecting the proper interpretation of the claims or an interpretation of the claims that any Defendant agrees with or proposes. Defendants dispute Plaintiff's apparent claim interpretations and will identify claim constructions for specific claim terms under the scheduling order governing this case. To the extent additional information regarding Plaintiff's infringement contentions becomes available, Defendants anticipate that they will provide corresponding invalidity contentions correlating Plaintiff's interpretation of the claims with the prior art and such Defendant may thus amend their invalidity contentions accordingly as applicable to the claims asserted by Plaintiff against such Defendant.

Nothing in these invalidity contentions shall be treated as an admission that any of Defendants' accused products meets any limitation of the Asserted Claims. Each Defendant denies that it infringes any claim of the Asserted Patents. To the extent that any prior art reference identified by Defendants contains a claim element that is the same as or similar to an element in an accused product, inclusion of that reference in Defendants' invalidity contentions shall not be deemed a waiver of any claim construction or non-infringement position. Any use of these invalidity contentions to support any allegation of infringement would be misleading, false and wrong as a matter of law and fact.

The Court has not yet construed the Asserted Claims. Defendants reserve the right to identify other prior art or to supplement their invalidity disclosures and contentions because Defendants' positions on invalidity of certain claims may depend on how those claims are

construed by the Court. Defendants' Preliminary Invalidity Contentions are based, at least in part, on their present understanding of the claim constructions Plaintiff appears to be using—based on Plaintiff's Infringement Contentions—whether or not Defendants agree with such claim constructions. Further, to the extent that these Preliminary Invalidity Contentions reflect constructions of claim terms that may be consistent with or implicit in Plaintiff's Infringement Contentions, no inference is intended or should be drawn that Defendants agree with such claim construction(s) and contentions. Defendants make no explicit expression of any position respecting claim construction in these Preliminary Invalidity Contentions. Any statement herein describing or tending to describe any claim element is provided for the purpose of understanding the relevant prior art and not for claim construction. Defendants expressly reserve the right to (1) propose any claim construction that they consider appropriate, and (2) contest any claim construction they consider inappropriate.

Defendants hereby reserve the right to incorporate by reference the testimony of any fact witnesses who are deposed, who provide declarations, or who otherwise testify in this case. Defendants also reserve the right to incorporate by reference the reports and testimony of Defendants' expert witnesses regarding invalidity of the Asserted Patents. Defendants further incorporate by reference any Invalidity Contentions served by other entities accused of infringing the Asserted Patents.

Nothing in these contentions constitutes an admission concerning the priority dates, conception date or reduction to practice of the Asserted Claims of the Asserted Patents. Defendants further reserve the right to seek discovery regarding any alleged conception and reduction to practice dates, as appropriate, and to demonstrate earlier invention by other parties under 35 U.S.C. § 102(g). Defendants further reserve the right to take discovery on the issues of

improper inventorship and/or derivation under 35 U.S.C. § 102(f), public use and/or the on-sale bar under 35 U.S.C. § 102(b), and/or applicants' failure to comply with 35 U.S.C. § 112. Defendants therefore reserve all rights to further supplement or amend these Preliminary Invalidity Contentions if and when further information becomes available.

II. IDENTIFICATION OF PRIOR ART

The concepts disclosed and claimed in each of the Asserted Patents are not new and had been disclosed, and actively practiced by others prior to the claimed invention date. The prior art includes various documents, products, patents, inventions, and systems that separately and together render the Asserted Claims invalid. In addition, as described in more detail below, claims of certain of the Asserted Patents are invalid under 35 U.S.C. § 112.

Defendants assert that the prior art listed in Exhibits 633-A1 through 633-An, 633-B1 through 633Bn, and 633-X, and Exhibits 112-A1 through 112-An, 112-B1 through 112-Bn, and 112-X individually, or in combination, invalidate(s) the Asserted Claims.[2] Defendants identify patents, publications and systems as prior art under 35 U.S.C. §§102 (a), (b), (e), (g) and/or §103 (collectively referred to herein as "prior art references") and reserve the right to identify additional patents, publications and systems as prior art as investigations continue.

In these contentions, Defendants identify exemplary elements of prior art references that anticipate or render obvious the elements of the Asserted Claims and/or show the state of the art in the relevant timeframe. Although Defendants have identified at least one citation per element for each prior art reference, each and every disclosure of the same or similar elements in said prior art reference is not necessarily identified. In an effort to focus the issues, and for the sake of concision, Defendants identify exemplary portions of the cited references. Of course, a person

[2] Exhibits 633-An, 633-Bn, 112-An and 112-Bn refer to the highest numbered such Exhibit that Defendants have or may provide.

of ordinary skill in the art would generally read a prior art reference as a whole and in the context of other publications, literature, and general knowledge in the field. To understand and interpret any specific statement or disclosure in a prior art reference, a person of ordinary skill in the art would rely upon other information including other publications and general scientific or engineering knowledge. Defendants therefore rely on all disclosures set forth in the prior art references and reserve the right to rely upon other portions of the prior art references not specifically cited herein as well as the right to rely on other patents, publications and expert testimony to provide context, demonstrate the general state of the art and the knowledge of one of ordinary skill in the art at the time the purported inventions of the Asserted Patents were made, and to aid understanding and interpretation of the identified portions and to provide information relating to the motivation to modify and/or combine references with either the knowledge of a person of skill in the art or with other references.

Defendants also incorporate by reference and reserve the right to rely upon patents, applications, publications, reports and other public materials or products in the same family as or otherwise related to the prior art references listed herein, even if not expressly disclosed in these contentions. Defendants further reserve the right to rely upon other prior art references, other publications, and the testimony of experts to establish that the alleged inventions would have been obvious to a person of ordinary skill in the art at the time of invention, including on the basis of modifying or combining certain cited references. Defendants also reserve the right to rely upon any admissions or omissions relating to prior art in the Asserted Patents or the prosecution history of the Asserted Patents.

Where Defendants identify a particular figure in a prior art reference, that identification encompasses the caption and description of the figure as well as any text relating to the figure in

addition to the figure itself. Similarly, where an identified portion of text refers to a figure or other material, that identification includes the referenced figure or other material as well regardless of whether the reference figure or other material is expressly presented in the claim chart.

Although certain elements of the Asserted Claims have been correlated to certain prior art disclosures, some of the elements may require construction and through that may be determined to be indefinite, not enabled, or otherwise fail to comply with section 112. As such, Defendants do not concede that the elements are adequately disclosed or delineated in the Asserted Patents merely because they have been correlated to specific prior art disclosures.

Defendants reserve all rights to further supplement or modify these Preliminary Invalidity Contentions, including the prior art disclosed and stated grounds of invalidity, pursuant to the Federal Rules of Civil Procedure and local rules. In addition, Defendants reserve the right to prove the invalidity of the Asserted Claims on bases other than those required to be disclosed in these disclosures and contentions. Defendants also expressly reserve the right to amend and/or supplement their Invalidity Contentions should this case be transferred to another district where different local and/or patent rules are operative.

For purposes of these Preliminary Invalidity Contentions, Defendants identify prior art references and provide element-by-element claim charts based, in part, on the apparent claim constructions advanced by Plaintiff in its Infringement Contentions. Nothing stated herein shall be treated as an admission or suggestion that Defendants agree with Plaintiff regarding either the scope of any of the Asserted Claims or the claim constructions advanced in Plaintiff's Infringement Contentions. Moreover, nothing in these Preliminary Invalidity Contentions shall

be treated as an admission that any of Defendants' accused technology meets any limitations of the Asserted Claims.

Defendants provide disclosures and related documents pertaining only to the Asserted Claims as identified by Plaintiff in its Infringement Contentions. Defendants will supplement their document production should they later find additional responsive documents. To the extent multiple limitations of the Asserted Claim(s) are construed to have similar meanings, or encompass similar features or functions, all prior art identified in Defendants' Preliminary Invalidity Contentions for each such limitation shall be deemed to apply to all such similar limitations.

To the extent that they constitute prior art, Defendants reserve the right to rely upon foreign counterparts of any U.S. patents or patent applications identified in Defendants' Preliminary Invalidity Contentions; U.S. counterparts of foreign patents and foreign patent applications identified in Defendants' Preliminary Invalidity Contentions; U.S. and foreign patents and patent applications corresponding to articles and publications identified in Defendants' Preliminary Invalidity Contentions; and any systems, products, techniques, or prior inventions that relate to any references identified in Defendants' Preliminary Invalidity Contentions.

Defendants may also rely upon inventor admissions concerning the scope of the prior art relevant to the Asserted Patents found in, among other places, the prosecution history of the Asserted Patents and any related patents, patent application, and/or reexaminations or post-grant proceedings.

A. Identification of Anticipating Prior Art

Each of the Asserted Claims is anticipated by at least the prior art listed in the tables below. The claim charts attached in the following Exhibits demonstrate where each limitation of

the anticipated claims is found in certain of the references listed below, either expressly or inherently in the larger context of the passage, or inherently as the reference as a whole is understood by a person having ordinary skill in the art. At least the following are prior art under one or more sections of 35 U.S.C. § 102:

1. Anticipating Prior Art to the '633 Patent

The following patents, publications, and systems are prior art to the Asserted Claim of the '633 Patent.

Exhibit	Patent or Patent Pub. No. / Title / Author	Filing, Priority, or Pub. Date[3]	Short Cite
633-A1	US 2002/0038891A1 (U.S. 6,956,238)	July 24, 2001	Ryu
633-A2	US 2004/0119076A1 (US 7,221,010)	Oct. 20, 2003	Ryu-2
633-A3	US 6,639,273	Oct. 28, 2003	Ueno
633-A4	US 6,316,791	Nov. 3, 2001	Schörner
633-A5	JP2001-144288	May 25, 2001	Kataoka
633-B1	US 6,413,822	July 2, 2002	Williams
633-B2	US 5,317,184	May 31, 1994	Rexer
633-B3	US 7,091,558 (EP03425099)	Jan. 23, 2004	Frisina
633-B4	US 6,054,737	Apr. 24, 2000	Magri'
633-B5	EP0022001A1 (FR7916902)	Jan. 7, 1981	Tonnel
633-B6	US 6,204,533	Mar. 20, 2001	Williams-2
633-B7	B. Jayant Baliga, Modern Power Devices, John Wiley & Sons, Inc., 1987	Feb. 27, 1987	Baliga

[3] For each reference, a filing or priority or other relevant date is identified to which the reference is entitled for prior art purposes. This may be the publication date, filing date or 102(e) date of the reference or of an earlier application to which the reference claims priority. Publications or issue dates of the same reference may provide additional priority dates and Defendants reserve the right to rely on all applicable priority dates. Throughout these Preliminary Invalidity Contentions, Defendants reserve the right to revise any of these dates as new information is obtained and to rely on all priority documents associated with a reference to establish the effective prior art date. Defendants also reserve the right to rely on any priority document or patent family member for the listed patents for invalidity prior art purposes because the grounds for invalidity for any family member or priority document will be apparent from the disclosures in these contentions.

Exhibit	Patent or Patent Pub. No. / Title / Author	Filing, Priority, or Pub. Date[3]	Short Cite
633-B8	G. Belverde et al., “A low-voltage MOSFET with small on-resistance: an extended characterization in high-efficiency power converter applications," Conference Record of the 2001 IEEE Industry Applications Conference. 36th IAS Annual Meeting (Cat. No.01CH37248), 2001, pp. 635-640 vol.1	2001	Belverde
633-B9	US 6,388,280	May 14, 2002	Hatade

Exhibit	System Prior Art	Short Cite
633-B10	STMicroelectronics MDmesh Products includes at least products made with any of the MDx0, MDx1, MDx2, MDx5, MDx7, MDx9, MDxB and MDxN dies (including at least the dies and products listed in Exhibits 633-B10(a) through 633-B10(h)).	MD Mesh Products
633-B10(a)	STMicroelectronics MDmesh MDx0 Products includes all products made with any of the MDx0 dies (including at least die MD50 and MD60).	MDmesh MDx0 Products
633-B10(b)	STMicroelectronics MDmesh MDx1 Products includes all products made with any of the MDx1 dies (including at least die MD61).	MDmesh MDx1 Products
633-B10(c)	STMicroelectronics MDmesh MDx2 Products includes all products made with of the MDx2 dies (including at least die MD62).	MDmesh MDx2 Products
633-B10(d)	STMicroelectronics MDmesh MDx5 Products includes all products made with any of the MDx5 dies (including at least die MD55 and die MD65 and at least products STP12NM50, STB12NM50FP, and STB12NM50).	MDmesh MDx5 Products
633-B10(e)	STMicroelectronics MDmesh MDx7 Products includes all products made with any of the MDx7 dies (including at least Die MD57).	MDmesh MDx7 Products
633-B10(f)	STMicroelectronics MDmesh MDx9 Products includes all products made with any of the MDx9 dies (including at least Die MD59 and die MD69 and at least product STW45NM50).	MDmesh MDx9 Products
633-B10(g)	STMicroelectronics MDmesh MDxB Products includes all products made with any of the MDxB dies (including at least die MD5B and die MD6B).	MDmesh MDxB Products
633-B10(h)	STMicroelectronics MDmesh MDxN Products includes all products made with any of the MDxN dies (including at least die MD5N and die MD6N).	MDmesh MDxN Products

Exhibit	System Prior Art	Short Cite
633-B11	STMicroelectronics PP26 Products includes all products made with the PP26 die (including at least product IRFP250).	PP26 Products
633-B12	STMicroelectronics EZ67 Products including all products made with the EZ67 die (including at least products STP13NK60Z/FP, STB13NK60Z, STB13NK60Z-1, STW13NK60Z).	EZ67 Products

2. Anticipating Prior Art to the '112 Patent

The following patents, publications, and systems are prior art to the Asserted Claims of the '112 Patent.

Exhibit	Patent or Patent Pub. No. / Title / Author	Filing, Priority, or Pub. Date[4]	Short Cite
112-A1	US 7,645,658	Oct. 23, 2007	Nakamura
112-A2	US 2005/0093000A1	May 5, 2005	Tanimoto
112-A3	US 2006/0027833A1	Feb. 9, 2006	Tanimoto2
112-A4	US 6,639,273	Oct. 28, 2003	Ueno
112-A5	US 6,238,980	May 29, 2001	Ueno2
112-A6	JP 2001-144288	May 25, 2001	Kataoka
112-A7	JP 2004-311815	Nov. 4, 2004	Kosugi
112-A8	US 7,598,567	Nov. 3, 2006	Hefner
112-A9	US 2005/0230686A1	Oct. 20, 2005	Kojima
112-A10	US 7,622,741 (WO2005/083796)	Feb. 25, 2005	Miura
112-A11	D. Peters et al, "4H-SiC Power MOSFET Blocking 1200V with a Gate Technology Compatible with Industrial Applications," Materials Science Forum Vols 433-436 (2003) pp 769-772.	Sep. 15, 2003	Peters

[4] For each reference, a filing or priority or other relevant date is identified to which the reference is entitled for prior art purposes. This may be the publication date, filing date or 102(e) date of the reference or of an earlier application to which the reference claims priority. Publications or issue dates of the same reference may provide additional priority dates and Defendants reserve the right to rely on all applicable priority dates. Throughout these Preliminary Invalidity Contentions, Defendants reserve the right to revise any of these dates as new information is obtained and to rely on all priority documents associated with a reference to establish the effective prior art date. Defendants also reserve the right to rely on any priority document or patent family member for the listed patents for invalidity prior art purposes because the grounds for invalidity for any family member or priority document will be apparent from the disclosures in these contentions.

Exhibit	Patent or Patent Pub. No. / Title / Author	Filing, Priority, or Pub. Date[4]	Short Cite
112-A12	Agarwal et al, "SiC Power Devices – An Overview," Mat. Res. Soc. Symp. Proc. Vol. 815 © 2004.	2004	Agarwal
112-A13	US 8,133,787	Feb. 26, 2008	Endo
112-A14	US 7,772,058	Jan. 30, 2008	Tanimoto3
112-A15	A. Agarwal, "Large_area_4H-SiC_power_MOSFETs," Proceedings of 2001 International Symposium on Power Semiconductor Devices & ICs, Osaka"	2001	Agarwal2
112-B1	EP0022001A1 (FR7916902)	Jan. 7, 1981	Tonnel
112-B2	US 6,054,737	Apr. 24, 2000	Magri'
112-B3	US 5,317,184	May 31, 1994	Rexer
112-B4	G. Belverde et al., "A low-voltage MOSFET with small on-resistance: an extended characterization in high-efficiency power converter applications," Conference Record of the 2001 IEEE Industry Applications Conference. 36th IAS Annual Meeting (Cat. No.01CH37248), 2001, pp. 635-640 vol.1	2001	Belverde
112-B5	US 6,388,280	May 14, 2002	Hatade

Exhibit	System Prior Art	Short Cite
112-B6	STMicroelectronics MDmesh Products includes at least products made with any of the MDx0, MDx1, MDx2, MDx5, MDx7, MDx9, MDxB and MDxN dies (including at least the dies and products listed in Exhibits 112-B6(a) through 112-B6(h)).	MD Mesh Products
112-B6(a)	STMicroelectronics MDmesh MDx0 Products includes all products made with any of the MDx0 dies (including at least die MD50 and MD60).	MDmesh MDx0 Products
112-B6(b)	STMicroelectronics MDmesh MDx1 Products includes all products made with any of the MDx1 dies (including at least die MD61).	MDmesh MDx1 Products
112-B6(c)	STMicroelectronics MDmesh MDx2 Products includes all products made with of the MDx2 dies (including at least die MD62).	MDmesh MDx2 Products
112-B6(d)	STMicroelectronics MDmesh MDx5 Products includes all products made with any of the MDx5 dies (including at least die MD55 and die MD65 and at least products STP12NM50, STB12NM50FP, and STB12NM50).	MDmesh MDx5 Products

Exhibit	System Prior Art	Short Cite
112-B6(e)	STMicroelectronics MDmesh MDx7 Products includes all products made with any of the MDx7 dies (including at least Die MD57).	MDmesh MDx7 Products
112-B6(f)	STMicroelectronics MDmesh MDx9 Products includes all products made with any of the MDx9 dies (including at least Die MD59 and die MD69 and at least product STW45NM50).	MDmesh MDx9 Products
112-B6(g)	STMicroelectronics MDmesh MDxB Products includes all products made with any of the MDxB dies (including at least die MD5B and die MD6B).	MDmesh MDxB Products
112-B6(h)	STMicroelectronics MDmesh MDxN Products includes all products made with any of the MDxN dies (including at least die MD5N and die MD6N).	MDmesh MDxN Products
112-B7	STMicroelectronics PP26 Products includes all products made with the PP26 die (including at least product IRFP250).	PP26 Products
112-B8	STMicroelectronics EZ67 Products including all products made with the EZ67 die (including at least products STP13NK60Z/FP, STB13NK60Z, STB13NK60Z-1, STW13NK60Z).	EZ67 Products

On information and belief, each listed document or item became prior art at least as early as the dates set forth herein.

B. Invalidity Due to Obviousness

The attached claim charts in:

Exhibits 633-A1 through 633-An and 633-B1 through 633-Bn in combination with one or more of each other or in combination with one or more of the references cited in claim chart of Exhibit 633-X, demonstrate that each prior art reference disclosed in the preceding sections, either alone or in combination with other prior art, and/or in combination with the knowledge of one skilled in the art, also renders the Asserted Claim of the ’633 Patent invalid as obvious; and

Exhibits 112-A1 through 112-An and 112-B1 though 112-Bn in combination with one or more of each other or in combination with one or more of the references cited in claim chart of Exhibit 112-X, demonstrate that each prior art reference disclosed in the preceding sections,

either alone or in combination with other prior art, and/or in combination with the knowledge of one skilled in the art, also renders the Asserted Claims of the '112 Patent invalid as obvious.

As set forth more fully below, Defendants assert that each prior art reference may be read in light of or combined with (1) information known to persons skilled in the art at the time of the alleged invention, (2) any of the other anticipatory prior art references, and/or (3) any of the additional prior art identified above and in the charts attached hereto. In addition, Defendants incorporate by reference each and every prior art reference of record in the prosecution of the Asserted Patents and related applications, including the statements made therein by the applicant, as well as the prior art discussed in the specification.

The Supreme Court, in *KSR International Co. v. Teleflex Inc., et al.*, 550 U.S. 398 (2007), held that a claimed invention can be obvious even if there is no explicit teaching, suggestion, or motivation for combining the prior art to produce that invention. In summary, *KSR* holds that patents that are based on new combinations of elements or components already known in a technical field may be found to be obvious. Specifically, the Court in *KSR* rejected a rigid application of the "teaching, suggestion, or motivation [to combine]" test. *KSR*, 550 U.S. at 418-19. "In determining whether the subject matter of patent claim is obvious, neither the particular motivation nor the avowed purpose of the patentee controls. What matters is the objective reach of the claim." *Id*. at 419-20. "Under the correct analysis, any need or problem known in the field of endeavor at the time of invention and addressed by the patent can provide a reason for combining the elements in the manner claimed." *Id*. at 420. In particular, in *KSR*, the Supreme Court emphasized the principle that "[t]he combination of familiar elements according to known methods is likely to be obvious when it does no more than yield predictable results." *Id*. at 416.

A key inquiry is whether the "improvement is more than the predictable use of prior art elements according to their established functions." *Id.* at 417.

The rationale to combine or modify prior art references is significantly stronger when the references seek to solve the same problem, come from the same field, and correspond well to each other. *In re Inland Steel Co.*, 265 F.3d 1354, 1362 (Fed. Cir. 2001). The Federal Circuit has held that two references may be combined as invalidating art under similar circumstances, namely "[the prior art] focus[es] on the same problem that the . . . patent addresses. . . . Moreover, both [prior art references] come from the same field . . . . Finally, the solutions to the identified problems found in the two references correspond well." *Id.* at 1364.

The Asserted Claims of each of the Asserted Patents would have been obvious to a person of ordinary skill at the time of the alleged invention. Specifically, for the reasons set forth below, a person of ordinary skill at the time of the alleged inventions had reason to and would have been motivated to combine or modify one or more of the references listed and charted in the attached Exhibits to arrive at the claimed inventions.

In addition to any prior art combinations disclosed below, Defendants will rely on any other combination of any prior art references disclosed herein, including to any prior art references disclosed in the prosecution history of the Asserted Patents. Plaintiff has not identified what elements or combinations it alleges were not known to one of ordinary skill in the art at the time of invention. Therefore, for any claim limitation that Plaintiff alleges is not disclosed in a particular prior art reference, Defendants reserve the right to assert that any such limitation is either inherent in the disclosed reference or obvious to one of ordinary skill in the art at the time in light of the same, or that the limitation disclosed in another one or more of the references disclose above and in combination would have rendered the asserted claim obvious.

The references cited, either alone or in combination, herein indicate that at a minimum, the Asserted Claims would have been obvious to one of ordinary skill in the art at the relevant time. However, to the extent it is determined that any one or more references do not disclose any particular element, that element was well-known in the art and one of ordinary skill in the art would have found it obvious to incorporate that feature based on at least the teaching of other prior art references, known techniques to improved similar systems, design incentives, or the general knowledge of one of ordinary skill in the art to obtain predictable results with reasonable expectations of success.

Defendants identify at least the following additional prior art references that either alone or in combination with any of the anticipatory prior art references (identified above), the knowledge of a person having ordinary skill in the art, and/or other prior art renders the Asserted Claims invalid as obvious under 35 U.S.C. § 103:

1. Additional Prior Art That Renders Obvious the Claims of the '633 Patent

Exhibit	Patent or Pub. No. / Title / Autor	Filing or Priority Date	Short Cite
633-X	US 2002/0030191A1	Mar. 14, 2002	Das
633-X	US 6,136,727	Oct. 24, 2000	Ueno-3
633-X	US 5,323,022	Jun. 21, 1994	Glass
633-X	Peters, "4H-SiC Power MOSFET Blocking 1200V with a Gate Technology Compatible with Industrial Applications," Materials Science Forum Vols 433-436 (2003) pp 769-772.	2003	Peters
633-X	US 5,233,215	Aug. 3, 1993	Baliga3
633-X	US 6,107,142	Aug. 22, 2000	Suvorov
633-X	US 5,510,281	Apr. 23, 1996	Ghezzo
633-X	US 5,111,253	May 5, 1992	Korman
633-X	US 2004/0119076A1	Oct. 30, 2003	Ryu-2

Exhibit	Patent or Pub. No. / Title / Autor	Filing or Priority Date	Short Cite
633-X	S.M. Sze, "Physics of Semiconductor Devices," 2nd Ed., John Wiley and Sons, 1981.	1981	Sze
633-X	P. G. Neudeck, “Progress in Silicon Carbide Semiconductor Electronics Technology,” Journal of Electronic Materials, Vol. 24, No. 4, 1995.	1995	Neudeck
633-X	M. Bhatnagar et al., “Comparison of 6H-SiC, 3C-SiC, and Si for Power Devices,” IEEE Transactions on Electron Devices, Vol. 40, No. 3. March 1993, p. 645.	Mar. 1993	Bhatnagar
633-X	Cooper et al., “SiC Power-Switching Devices—The Second Electronics Revolution?” Proceedings of the IEEE, Vol. 90, No. 6, June 2002 at 956.	Jun. 2002	SiC Power-Switching Devices
633-X	J. A. Cooper et al, “Status and Prospects for SiC Power MOSFETs,” IEEE Transactions on Electron Devices, Vol. 49, No. 4, April 2002 at 658.	Mar. 1997	Status and Prospects
633-X	Shenoy et al., “High-Voltage Double-Implanted Power MOSFET’s in 6H-SiC,” IEEE Electron Device Letters, Vol. 18, No. 3, March 1997, at 93.	Apr. 2002	Shenoy
633-X	Ryu et al., “Design and Process Issues for Silicon Carbide Power DiMOSFETS 2001,” Mat. Res. Soc. Symp. Vol. 640 © 2001.	2001	Design and Process
633-X	Grant, “Power MOSFETs Theory and Applications,” John Wiley & Sons 1989.	1989	Grant
633-X	R. W. Coen et al., “A High-Performance Planar Power MOSFET,” IEEE Trans on Elec. Dev. Vol., ED-27, No. 2, Feb. 1980	Feb. 1980	Coen
633-X	Saint, “IC Layout Basics,” McGraw-Hill 2001.	2001	Saint
633-X	Final Technical Report, N00014-01-1-0072, “Development of SiC Power MOSFETs with Low On-Resistance for Military and Commercial Applications”	2003	ADA414680
633-X	J.B. Casady et al., “Fabrication Procedures and Characterization of 6H-SiC MESFETs for USE in High Temperature Electronics,” 1995 Proceedings. 45th Electronic Components and Technology Conference, 1995, pp. 261-265, IEEE doi 10.1109/ECTC.1995.514395	1995	Casady

Exhibit	Patent or Pub. No. / Title / Autor	Filing or Priority Date	Short Cite
633-X	J.B. Casady et al., "Silicon Carbide Power MOSFET Technology," Compound Semiconductors 1997. Proceedings of the IEEE Twenty-Fourth International Symposium on Compound Semiconductors. IEEE doi 10.1109/ISCS.1998.711654	1997	Casady2
633-X	V.R. Vathulya, "A Novel 6H-SiC Power DMOSFET with Implanted P-Well Spacer," IEEE Electron Device Letters, VOL. 20, NO. 7, July 1999, P. 354	2001	Vathulya
633-X	A. Agarwal et al., "Large area 4H-SiC power MOSFETs," Proceedings of the 13th International Symposium on Power Semiconductor Devices & ICs. IPSD '01 (IEEE Cat. No.01CH37216), 2001, pp. 183-186, doi 10.1109/ISPSD.2001.934585	2001	Agarwal2
633-X	S. Ryu et al, "4H-SIC DMOSFETs for High Frequency Power Switching Applications," Mat. Res. Soc. Symp. Proc. Vol. 764 © 2003 Materials Research Society, MRS Online Proceedings Library (OPL) , Volume 764: Symposium C – New Applications for Wide-Bandgap Semiconductors , 2003 , C2.7 DOI https://doi.org/10.1557/PROC-764-C2.7	2003	Ryu-3
633-X	S. Ryu et al., "10A, 2.4kV Power DiMOSFET in 4H-SiC," IEEE Electron Device Letters, VOL. 23, NO. 6, June 2002	2002	Ryu-6
633-X	S. Ryu et al, "10-kV, 123-m-ohm-cm2 4H-SiC Power MOSFETs," IEEE Electron Device Letters, Vol. 25, No. 8, p. 556, Aug. 2004	Aug. 2004	Ryu-7
633-X	Admissions / admitted prior art in U.S. Pat. No. 7,498,633	Before the invention of the '633 Patent claims	Cooper '633

The following table shows exemplary combinations that render claim 9 of the '633 Patent obvious. Specific examples of this obviousness are set forth below. The identification of primary references, secondary references, and obviousness combinations is not intended to be exhaustive—there are many possible combinations of the references that one of ordinary skill in the art would have been motivated to make—and it is not practical to provide details of all such possible combinations:

One of the Following Primary References	In Combination with One or More of the Following References
• Ryu (Ex. 633-A1) • Ryu-2 (Ex. 633-A2) • Ueno (Ex. 633-A3) • Schörner (Ex. 633-A4) • Kataoka (Ex. 633-A5) • Williams (Ex. 633-B1) • Rexer (Ex. 633-B2) • Frisina (Ex. 633-B3) • Magri' (Ex. 633-B4) • Tonnel (Ex. 633-B5) • Williams-2 (Ex. 633-B6) • Baliga (Ex. 633-B7) • Belverde (Ex. 633-B8) • Hatade (Ex. 633-B9) • MDmesh Products (Ex. 633-B10, including Exs. 633-B10(a) - 633-B10(h)) • PP26 Products (Ex. 633-B11) • EZ67 Products (Ex. 633-B12)	• Any one or more of the '633 Patent "Primary" references – i.e., references identified in Exhibits 633-A1 through 633-An and 633-B1 through 633-Bn. • Any one or more of the references cited in Exhibit 633-X, i.e.: o Das o Ueno-3 o Glass o Peters o Baliga3 o Suvorov o Ghezzo o Korman o Ryu-2 o Sze o Neudeck o Bhatnagar o SiC Power-Switching Devices o Status and Prospects o Shenoy o Design and Process o Grant o Coen o Saint o ADA414680 o Casady o Casady2 o Vathulya o Agarwal2 o Ryu-3 o Ryu-6 o Ryu-7 o Applicants' admissions / admitted prior art in '633 Patent

As explained below, one of ordinary skill in the art would have found it obvious and would have been motivated to make the combinations listed.

The ’633 patent is directed to a semiconductor device such as a “vertical double-implanted metal-oxide semiconductor field-effect transistor,” MOSFET or DMOSFET. *See e.g.*, ’633 Patent at Abstract, 1:12-14, 3:7–8, 4:4-9, claim 9, Figure 1. And a particular issue addressed in the ’633 Patent and asserted claims is the shape or layout of the device for providing electrical connections between the source regions and base (i.e., body) of the device. *See e.g.,* 7:57–59, Figure 3.

Ryu is analogous art to the ’633 Patent because, among other things, it is in the same field of endeavor of the ’633 Patent and because Ryu is pertinent to the particular problem sought to be solved by the inventor in the ’633 Patent. Specifically, like the ’633 Patent, Ryu is directed to the configuration or layout of a vertical MOSFET formed in a silicon carbide substrate. Because of the matter with which Ryu deals, it logically would have commended itself to an inventor’s attention in considering the problem of how to configure the shape layout of a vertical MOSFET formed in silicon carbide and, in particular, the shape or layout of the device for providing electrical connections between the source regions and base (i.e., body) of the device.

Ryu-2 is analogous art to the ’633 Patent because, among other things, it is in the same field of endeavor of the ’633 Patent and because Ryu-2 is pertinent to the particular problem sought to be solved by the inventor in the ’633 Patent. Specifically, like the ’633 Patent, Ryu-2 is directed to the configuration or layout of a vertical MOSFET formed in a silicon carbide substrate. Because of the matter with which Ryu-2 deals, it logically would have commended itself to an inventor’s attention in considering the problem of how to configure the shape layout

of a vertical MOSFET formed in silicon carbide and, in particular, the shape or layout of the device for providing electrical connections between the source regions and base (i.e., body) of the device.

Ueno is analogous art to the ’633 Patent because, among other things, it is in the same field of endeavor of the ’633 Patent and because Ueno is pertinent to the particular problem sought to be solved by the inventor in the ’633 Patent. Specifically, like the ’633 Patent, Ueno is directed to the configuration or layout of a vertical MOSFET formed in a silicon carbide substrate. Because of the matter with which Ueno deals, it logically would have commended itself to an inventor’s attention in considering the problem of how to configure the shape layout of a vertical MOSFET formed in silicon carbide and, in particular, the shape or layout of the device for providing electrical connections between the source regions and base (i.e., body) of the device.

Schörner is analogous art to the ’633 Patent because, among other things, it is in the same field of endeavor of the ’633 Patent and because Schörner is pertinent to the particular problem sought to be solved by the inventor in the ’633 Patent. Specifically, like the ’633 Patent, Schörner is directed to the configuration or layout of a vertical MOSFET formed in a silicon carbide substrate. Because of the matter with which Schörner deals, it logically would have commended itself to an inventor’s attention in considering the problem of how to configure the shape layout of a vertical MOSFET formed in silicon carbide and, in particular, the shape or layout of the device for providing electrical connections between the source regions and base (i.e., body) of the device.

Kataoka is analogous art to the ’633 Patent because, among other things, it is in the same field of endeavor of the ’633 Patent and because Kataoka is pertinent to the particular problem

sought to be solved by the inventor in the ’633 Patent. Specifically, like the ’633 Patent, Kataoka is directed to the configuration or layout of a vertical MOSFET formed in a silicon carbide substrate. Because of the matter with which Kataoka deals, it logically would have commended itself to an inventor’s attention in considering the problem of how to configure the shape layout of a vertical MOSFET formed in silicon carbide and, in particular, the shape or layout of the device for providing electrical connections between the source regions and base (i.e., body) of the device.

Williams is analogous art to the ’633 Patent because, among other things, it is in the same field of endeavor of the ’633 Patent and because Williams is pertinent to the particular problem sought to be solved by the inventor in the ’633 Patent. Specifically, like the ’633 Patent, Williams is directed to the configuration or layout of a vertical MOSFET and in particular addresses the shape or layout of the device for providing electrical connections between the source regions and base (i.e., body) of the device. Because of the matter with which Williams deals, it logically would have commended itself to an inventor’s attention in considering the problem of how to configure the shape layout of a vertical MOSFET formed in silicon carbide and, in particular, the shape or layout of the device for providing electrical connections between the source regions and base (i.e., body) of the device.

Rexer is analogous art to the ’633 Patent because, among other things, it is in the same field of endeavor of the ’633 Patent and because Rexer is pertinent to the particular problem sought to be solved by the inventor in the ’633 Patent. Specifically, like the ’633 Patent, Rexer is directed to the configuration or layout of a vertical MOSFET and in particular addresses the shape or layout of the device for providing electrical connections between the source regions and base (i.e., body) of the device. Because of the matter with which Rexer deals, it logically would

have commended itself to an inventor's attention in considering the problem of how to configure the shape layout of a vertical MOSFET formed in silicon carbide and, in particular, the shape or layout of the device for providing electrical connections between the source regions and base (i.e., body) of the device.

Frisina is analogous art to the '633 Patent because, among other things, it is in the same field of endeavor of the '633 Patent and because Frisina is pertinent to the particular problem sought to be solved by the inventor in the '633 Patent. Specifically, like the '633 Patent, Frisina is directed to the configuration or layout of a vertical MOSFET and in particular addresses the shape or layout of the device for providing electrical connections between the source regions and base (i.e., body) of the device. Because of the matter with which Frisina deals, it logically would have commended itself to an inventor's attention in considering the problem of how to configure the shape layout of a vertical MOSFET formed in silicon carbide and, in particular, the shape or layout of the device for providing electrical connections between the source regions and base (i.e., body) of the device.

Magri' is analogous art to the '633 Patent because, among other things, it is in the same field of endeavor of the '633 Patent and because Magri' is pertinent to the particular problem sought to be solved by the inventor in the '633 Patent. Specifically, like the '633 Patent, Magri' is directed to the configuration or layout of a vertical MOSFET and in particular addresses the shape or layout of the device for providing electrical connections between the source regions and base (i.e., body) of the device. Because of the matter with which Magri' deals, it logically would have commended itself to an inventor's attention in considering the problem of how to configure the shape layout of a vertical MOSFET formed in silicon carbide and, in particular, the shape or

layout of the device for providing electrical connections between the source regions and base (i.e., body) of the device.

Tonnel is analogous art to the ’633 Patent because, among other things, it is in the same field of endeavor of the ’633 Patent and because Tonnel is pertinent to the particular problem sought to be solved by the inventor in the ’633 Patent. Specifically, like the ’633 Patent, Tonnel is directed to the configuration or layout of a vertical MOSFET and in particular addresses the shape or layout of the device for providing electrical connections between the source regions and base (i.e., body) of the device. Because of the matter with which Tonnel deals, it logically would have commended itself to an inventor’s attention in considering the problem of how to configure the shape layout of a vertical MOSFET formed in silicon carbide and, in particular, the shape or layout of the device for providing electrical connections between the source regions and base (i.e., body) of the device.

Williams-2 is analogous art to the ’633 Patent because, among other things, it is in the same field of endeavor of the ’633 Patent and because Williams-2 is pertinent to the particular problem sought to be solved by the inventor in the ’633 Patent. Specifically, like the ’633 Patent, Williams-2 is directed to the configuration or layout of a vertical MOSFET and in particular addresses the shape or layout of the device for providing electrical connections between the source regions and base (i.e., body) of the device. Because of the matter with which Williams-2 deals, it logically would have commended itself to an inventor’s attention in considering the problem of how to configure the shape layout of a vertical MOSFET formed in silicon carbide and, in particular, the shape or layout of the device for providing electrical connections between the source regions and base (i.e., body) of the device.

Baliga is analogous art to the ’633 Patent because, among other things, it is in the same field of endeavor of the ’633 Patent and because Baliga is pertinent to the particular problem sought to be solved by the inventor in the ’633 Patent. Specifically, like the ’633 Patent, Baliga is directed to the configuration or layout of a vertical MOSFET and in particular addresses the shape or layout of the device for providing electrical connections between the source regions and base (i.e., body) of the device. Because of the matter with which Baliga deals, it logically would have commended itself to an inventor’s attention in considering the problem of how to configure the shape layout of a vertical MOSFET formed in silicon carbide and, in particular, the shape or layout of the device for providing electrical connections between the source regions and base (i.e., body) of the device.

Belverde is analogous art to the ’633 Patent because, among other things, it is in the same field of endeavor of the ’633 Patent and because Belverde is pertinent to the particular problem sought to be solved by the inventor in the ’633 Patent. Specifically, like the ’633 Patent, Belverde is directed to the configuration or layout of a vertical MOSFET and in particular addresses the shape or layout of the device for providing electrical connections between the source regions and base (i.e., body) of the device. Because of the matter with which Belverde deals, it logically would have commended itself to an inventor’s attention in considering the problem of how to configure the shape layout of a vertical MOSFET formed in silicon carbide and, in particular, the shape or layout of the device for providing electrical connections between the source regions and base (i.e., body) of the device.

Hatade is analogous art to the ’633 Patent because, among other things, it is in the same field of endeavor of the ’633 Patent and because Hatade is pertinent to the particular problem sought to be solved by the inventor in the ’633 Patent. Specifically, like the ’633 Patent, Hatade

is directed to the configuration or layout of a vertical MOSFET and in particular addresses the shape or layout of the device for providing electrical connections between the source regions and base (i.e., body) of the device. Because of the matter with which Hatade deals, it logically would have commended itself to an inventor's attention in considering the problem of how to configure the shape layout of a vertical MOSFET formed in silicon carbide and, in particular, the shape or layout of the device for providing electrical connections between the source regions and base (i.e., body) of the device.

The MDmesh Products (including MDx0, MDx1, MDx2, MDx5, MDx9, MDxB, MDxN) are analogous art to the '633 Patent because, among other things, they are in the same field of endeavor of the '633 Patent and because the MDmesh Products are pertinent to the particular problem sought to be solved by the inventor in the '633 Patent. Specifically, like the '633 Patent, the MDmesh Products are directed to the configuration or layout of a vertical MOSFET and in particular addresses the shape or layout of the device for providing electrical connections between the source regions and base (i.e., body) of the device. Because of the matter with which the MDmesh Products deal, they logically would have commended themselves to an inventor's attention in considering the problem of how to configure the shape layout of a vertical MOSFET formed in silicon carbide and, in particular, the shape or layout of the device for providing electrical connections between the source regions and base (i.e., body) of the device.

The PP26 Products are analogous art to the '633 Patent because, among other things, they are in the same field of endeavor of the '633 Patent and because the PP26 Products are pertinent to the particular problem sought to be solved by the inventor in the '633 Patent. Specifically, like the '633 Patent, the PP26Products are directed to the configuration or layout of a vertical MOSFET and in particular addresses the shape or layout of the device for providing electrical

connections between the source regions and base (i.e., body) of the device. Because of the matter with which the PP26 Products deal, they logically would have commended themselves to an inventor's attention in considering the problem of how to configure the shape layout of a vertical MOSFET formed in silicon carbide and, in particular, the shape or layout of the device for providing electrical connections between the source regions and base (i.e., body) of the device.

The EZ67 Products are analogous art to the '633 Patent because, among other things, they are in the same field of endeavor of the '633 Patent and because the EZ67 Products are pertinent to the particular problem sought to be solved by the inventor in the '633 Patent. Specifically, like the '633 Patent, the EZ67 Products are directed to the configuration or layout of a vertical MOSFET and in particular addresses the shape or layout of the device for providing electrical connections between the source regions and base (i.e., body) of the device. Because of the matter with which the EZ67 Products deal, they logically would have commended themselves to an inventor's attention in considering the problem of how to configure the shape layout of a vertical MOSFET formed in silicon carbide and, in particular, the shape or layout of the device for providing electrical connections between the source regions and base (i.e., body) of the device.

Das is analogous art to the '633 Patent because, among other things, it is in the same field of endeavor of the '633 Patent, double-diffused or double-implanted MOSFETs, and because Das is pertinent to the application of MOSFET structures in silicon carbide substrate material, which is one of the issues that concerns the '633 Patent. Because of the matter with which Das deals, it logically would have commended itself to an inventor's attention in considering the

problem of forming vertical DMOSFETs in silicon carbide and considering the configuration and elements of the device.

Ueno-3 is analogous art to the ’633 Patent because, among other things, it is in the same field of endeavor of the ’633 Patent, MOSFETs, and because Ueno-3 is pertinent to the application of MOSFET structures in silicon carbide substrate material, which is one of the issues that concerns the ’633 Patent. Because of the matter with which Ueno-3 deals, it logically would have commended itself to an inventor’s attention in considering the problem of forming vertical DMOSFETs in silicon carbide and considering the configuration and elements of the device.

Glass is analogous art to the ’633 Patent because, among other things, it is in the same field of endeavor of the ’633 Patent, MOSFETs, and because Glass is pertinent to the application of MOSFET structures in silicon carbide substrate material and the formation of contacts in silicon carbide, which are issues that concern the ’633 Patent. Because of the matter with which Glass deals, it logically would have commended itself to an inventor’s attention in considering the problem of forming vertical DMOSFETs in silicon carbide and considering the configuration and elements of the device.

Peters is analogous art to the ’633 Patent because, among other things, it is in the same field of endeavor of the ’633 Patent, vertical MOSFETs, and because Peters is pertinent to the application of MOSFET structures in silicon carbide substrate material, which is one of the issues that concerns the ’633 Patent. Because of the matter with which Peters deals, it logically would have commended itself to an inventor’s attention in considering the problem of forming vertical DMOSFETs in silicon carbide and considering the configuration and elements of the device.

Baliga3 is analogous art to the ’633 Patent because, among other things, it is in the same field of endeavor of the ’633 Patent, vertical MOSFETs, and because Baliga3 is pertinent to the application of MOSFET structures in silicon carbide substrate material, which is one of the issues that concerns the ’633 Patent. Because of the matter with which Baliga3 deals, it logically would have commended itself to an inventor’s attention in considering the problem of forming vertical DMOSFETs in silicon carbide and considering the configuration and elements of the device.

Suvorov is analogous art to the ’633 Patent because, among other things, it is in the same field of endeavor of the ’633 Patent, MOSFETs, and because Suvorov is pertinent to the application of MOSFET structures in silicon carbide substrate material, which is one of the issues that concerns the ’633 Patent. Because of the matter with which Suvorov deals, it logically would have commended itself to an inventor’s attention in considering the problem of forming vertical DMOSFETs in silicon carbide and considering the configuration and elements of the device.

Ghezzo is analogous art to the ’633 Patent because, among other things, it is in the same field of endeavor of the ’633 Patent, vertical MOSFETs, and because Ghezzo is pertinent to the application of MOSFET structures in silicon carbide substrate material, which is one of the issues that concerns the ’633 Patent. Because of the matter with which Ghezzo deals, it logically would have commended itself to an inventor’s attention in considering the problem of forming vertical DMOSFETs in silicon carbide and considering the configuration and elements of the device.

Korman is analogous art to the ’633 Patent because, among other things, it is in the same field of endeavor of the ’633 Patent, vertical MOSFETs, and because Korman is pertinent to

configuration of MOSFET structures including configuration of sources / source electrodes, which are issues that concern the ’633 Patent. Because of the matter with which Korman deals, it logically would have commended itself to an inventor’s attention in considering the problem of forming vertical DMOSFETs in silicon carbide and considering the configuration and elements of the device.

Ryu-2 is analogous art to the ’633 Patent because, among other things, it is in the same field of endeavor of the ’633 Patent, vertical MOSFETs, and because Ryu-2 is pertinent to the application of MOSFET structures in silicon carbide substrate material, which is one of the issues that concerns the ’633 Patent. Because of the matter with which Ryu-2 deals, it logically would have commended itself to an inventor’s attention in considering the problem of forming vertical DMOSFETs in silicon carbide and considering the configuration and elements of the device.

Sze is analogous art to the ’633 Patent because, among other things, it is in the same field of endeavor of the ’633 Patent, MOSFETs and structures used in semiconductors, and because Sze is pertinent to the application of MOSFET structures in various semiconductor substrate materials and the formation of contacts in semiconductors, which are issues that concern the ’633 Patent. Because of the matter with which Sze deals, it logically would have commended itself to an inventor’s attention in considering the problem of forming vertical DMOSFETs in silicon carbide and considering the configuration and elements of the device.

Neudeck is analogous art to the ’633 Patent because, among other things, it is in the same field of endeavor of the ’633 Patent, MOSFETs including vertical MOSFETs, and because Neudeck is pertinent to the application of MOSFET structures in silicon carbide substrate material, which is one of the issues that concerns the ’633 Patent. Because of the matter with

which Neudeck deals, it logically would have commended itself to an inventor's attention in considering the problem of forming vertical DMOSFETs in silicon carbide and considering the configuration and elements of the device.

Bhatnagar is analogous art to the '633 Patent because, among other things, it is in the same field of endeavor of the '633 Patent, vertical DMOSFETs, and because Bhatnagar is pertinent to the application of MOSFET structures in silicon carbide substrate material, which is one of the issues that concerns the '633 Patent. Because of the matter with which Bhatnagar deals, it logically would have commended itself to an inventor's attention in considering the problem of forming vertical DMOSFETs in silicon carbide and considering the configuration and elements of the device.

SiC Power-Switching Devices is analogous art to the '633 Patent because, among other things, it is in the same field of endeavor of the '633 Patent, vertical DMOSFETs, and because SiC Power-Switching Devices is pertinent to the application of MOSFET structures in silicon carbide substrate material, which is one of the issues that concerns the '633 Patent. Because of the matter with which SiC Power-Switching Devices deals, it logically would have commended itself to an inventor's attention in considering the problem of forming vertical DMOSFETs in silicon carbide and considering the configuration and elements of the device.

Status and Prospects is analogous art to the '633 Patent because, among other things, it is in the same field of endeavor of the '633 Patent, vertical DMOSFETs, and because Status and Prospects is pertinent to the application of MOSFET structures in silicon carbide substrate material, which is one of the issues that concerns the '633 Patent. Because of the matter with which Status and Prospects deals, it logically would have commended itself to an inventor's

attention in considering the problem of forming vertical DMOSFETs in silicon carbide and considering the configuration and elements of the device.

Shenoy is analogous art to the ’633 Patent because, among other things, it is in the same field of endeavor of the ’633 Patent, vertical DMOSFETs, and because Shenoy is pertinent to the application of MOSFET structures in silicon carbide substrate material, which is one of the issues that concerns the ’633 Patent. Because of the matter with which Shenoy deals, it logically would have commended itself to an inventor’s attention in considering the problem of forming vertical DMOSFETs in silicon carbide and considering the configuration and elements of the device.

Design and Process is analogous art to the ’633 Patent because, among other things, it is in the same field of endeavor of the ’633 Patent, vertical DMOSFETs, and because Design and Process is pertinent to the application of MOSFET structures in silicon carbide substrate material, which is one of the issues that concerns the ’633 Patent. Because of the matter with which Design and Process deals, it logically would have commended itself to an inventor’s attention in considering the problem of forming vertical DMOSFETs in silicon carbide and considering the configuration and elements of the device.

Grant is analogous art to the ’633 Patent because, among other things, it is in the same field of endeavor of the ’633 Patent, power MOSFETs, and because Grant is pertinent to the structure, elements and operation of power MOSFETs, which are issues that concern the ’633 Patent. Because of the matter with which Grant deals, it logically would have commended itself to an inventor’s attention in considering the problem of forming vertical DMOSFETs in silicon carbide and considering the configuration and elements of the device.

Coen is analogous art to the ’633 Patent because, among other things, it is in the same field of endeavor of the ’633 Patent, planar power MOSFETs, and because Coen is pertinent to the structure, elements and operation of power MOSFETs, which are issues that concern the ’633 Patent. Because of the matter with which Coen deals, it logically would have commended itself to an inventor’s attention in considering the problem of forming vertical DMOSFETs in silicon carbide and considering the configuration and elements of the device.

Saint is analogous art to the ’633 Patent because, among other things, it is in the same field of endeavor of the ’633 Patent, semiconductor device layout and operation, and because Saint is pertinent to configuration and operation of well and substrate ties especially with respect to avoiding activation of parasitic bipolar elements and latch up, which are issues that concern the ’633 Patent. Because of the matter with which Saint deals, it logically would have commended itself to an inventor’s attention in considering the problem of forming vertical DMOSFETs in silicon carbide and considering the configuration and elements of the device.

ADA414680 is analogous art to the ’633 Patent because, among other things, it is in the same field of endeavor of the ’633 Patent, vertical DMOSFETs, and because ADA414680 is pertinent to the application of MOSFET structures in silicon carbide substrate material, which is one of the issues that concerns the ’633 Patent. Because of the matter with which ADA414680 deals, it logically would have commended itself to an inventor’s attention in considering the problem of forming vertical DMOSFETs in silicon carbide and considering the configuration and elements of the device.

Casady is analogous art to the ’633 Patent because, among other things, it is in the same field of endeavor of the ’633 Patent, SiC FET structures, and because Casady is pertinent to fabrication of silicon carbide FET structures, which is one of the issues that concerns the ’633

Patent. Because of the matter with which Casady deals, it logically would have commended itself to an inventor's attention in considering the problem of forming vertical DMOSFETs in silicon carbide and considering the configuration and elements of the device.

Casady2 is analogous art to the '633 Patent because, among other things, it is in the same field of endeavor of the '633 Patent, vertical DiMOSFETs, and because Casady2 is pertinent to the application of MOSFET structures in silicon carbide substrate material, which is one of the issues that concerns the '633 Patent. Because of the matter with which Casady2 deals, it logically would have commended itself to an inventor's attention in considering the problem of forming vertical DMOSFETs in silicon carbide and considering the configuration and elements of the device.

Vathulya is analogous art to the '633 Patent because, among other things, it is in the same field of endeavor of the '633 Patent, vertical DiMOSFETs, and because Vathulya is pertinent to the application of MOSFET structures in silicon carbide substrate material including n+ doped JFET region, which is one of the issues that concerns the '633 Patent. Because of the matter with which Vathulya deals, it logically would have commended itself to an inventor's attention in considering the problem of forming vertical DMOSFETs in silicon carbide and considering the configuration and elements of the device.

Agarwal2 is analogous art to the '633 Patent because, among other things, it is in the same field of endeavor of the '633 Patent, vertical DiMOSFETs, and because the application of MOSFET structures in silicon carbide substrate material is pertinent to the application of MOSFET structures in silicon carbide substrate material, which is one of the issues that concerns the '633 Patent. Because of the matter with which the application of MOSFET structures in silicon carbide substrate material deals, it logically would have commended itself to an

inventor's attention in considering the problem of forming vertical DMOSFETs in silicon carbide and considering the configuration and elements of the device.

Ryu-3 is analogous art to the '633 Patent because, among other things, it is in the same field of endeavor of the '633 Patent, vertical DMOSFETs, and because Ryu-3 is pertinent to the application of MOSFET structures in silicon carbide substrate material, which is one of the issues that concerns the '633 Patent. Because of the matter with which Ryu-3 deals, it logically would have commended itself to an inventor's attention in considering the problem of forming vertical DMOSFETs in silicon carbide and considering the configuration and elements of the device.

Ryu-6 is analogous art to the '633 Patent because, among other things, it is in the same field of endeavor of the '633 Patent, vertical DMOSFETs, and because Ryu-6 is pertinent to the application of MOSFET structures in silicon carbide substrate material, which is one of the issues that concerns the '633 Patent. Because of the matter with which Ryu-6 deals, it logically would have commended itself to an inventor's attention in considering the problem of forming vertical DMOSFETs in silicon carbide and considering the configuration and elements of the device.

Ryu-7 is analogous art to the '633 Patent because, among other things, it is in the same field of endeavor of the '633 Patent, vertical DMOSFETs, and because Ryu-7 is pertinent to the application of MOSFET structures in silicon carbide substrate material, which is one of the issues that concerns the '633 Patent. Because of the matter with which Ryu-7 deals, it logically would have commended itself to an inventor's attention in considering the problem of forming vertical DMOSFETs in silicon carbide and considering the configuration and elements of the device.

The Asserted Claim of the ’633 Patent would have been obvious over any one of—or combination of—the primary references addressed in Exhibit 633-A1 through 633-An and Exhibit 633-B1 through Exhibit 633Bn alone or in combination with knowledge of one of ordinary skill in the art and/or in combination with one or more of the references addressed in Exhibit 633-X. Specifically, these combinations would have been obvious for a number of reasons including because all the claimed elements were known in the prior art, and one skilled in the art could have combined the elements as claimed by known methods with no change in their respective functions and the combination would yield nothing more than predictable results to improve a similar device in the same way.

For example, Ryu, Ryu-2, Ueno, Schörner, and Kataoka (addressed in Exhibits 633-A1 through 633-An) all address vertical MOSFETs expressly disclosed as being formed in a silicon carbide substrate. Many of these references depict a cross section view of the disclosed structure and a person of skill in the art would know that vertical channel MOSFETs are inherently three-dimensional devices and that there are a number of widely known layouts used in vertical channel power MOSFETs, including linear, square and hex cell unit cells and that a typical power MOSFET has many such unit cells arranged in an array. A person of skill in the art would know that a given cross section structure for a vertical MOSFET could be implemented in various three-dimensional unit cell configurations such as linear, square and hex cell unit cells. Likewise, a person of skill in the art would know that the so-called body or base of the MOSFET structure is typically tied to the source to prevent inadvertent activation of parasitic components that are inherent in the configuration, as most of these references expressly disclose, and that there are various known layout configurations for making body connections in vertical MOSFETs including the specific layout specified in the Asserted Claim of the ’633 Patent.

Collectively these references disclose that the configuration of the vertical MOSFET including substrate, drift layer, first and second source regions, JFET region, source electrodes and base contact regions formed in the source regions in the configuration claimed, were all known in the vertical MOSFET art. As a result, for example, to the extent Purdue alleges that any one primary prior art reference does not expressly disclose a particular structure, layout or configuration of the Asserted Claim, it would have been obvious to one of skill in the art that a known structure or configuration from another reference also known for use in or applicable to vertical MOSFETs could be combined in an overall vertical MOSFET structure that would yield nothing more than predicable results, and that it would be desirable to do so because a vertical power MOSFET could achieve reduced ON resistance and greater manufacturing alignment tolerance by increasing the source contact area and making periodic contact to the base region.

Similarly, Williams, Rexer, Frisina, Magri', Tonnel, Williams2, Baliga, Belverde, Hatade, the MDmesh Products, the PP26 Products, and the EZ67 Products, (addressed in Exhibits 633-B1 through 633-Bn) each disclose vertical MOSFET devices that expressly describe/disclose source and body regions where body connections are made periodically to the body at body regions spaced apart in the source region. To the extent some of these references disclose a vertical MOSFET nominally in a silicon substrate, a person of skill in the art would recognize, as was long known before the purported invention of the '633 patent, that the general unit cell cross section configuration of a vertical MOSFET can be the same regardless of whether the substrate is silicon or silicon carbide, and that implementing the structure in a silicon carbide substrate would take advantage of the well-known semiconductor characteristics of silicon carbide such as: wide bandgap, high thermal conductivity, high melting point, high electric field breakdown strength, low dielectric constant, and high saturated electron drift velocity. As a

result, for example, to the extent Bell alleges that any one reference does not expressly disclose a particular substrate type, it would have been obvious to one of skill in the art that as a known substrate type for vertical MOSFETs, use of a silicon carbide substrate could be combined in an overall vertical MOSFET structure of the reference that would yield nothing more than predicable results, and that it would be desirable to do so because a vertical power MOSFET using a silicon carbide substrate could achieve improved capabilities such as the capability to operate at higher temperatures, higher device densities, higher speeds, or higher power levels, as compared to some other semiconductor materials.

Similarly, one or more of the above referenced references (addressed in Exhibits 633-A1 through 633-An and Exhibits 633-B1 through 633-Bn) would be obvious to combine with one or more of Das, Ueno-3, Glass, Peters, Baliga3, Suvorov, Ghezzo, Korman, Ryu-2, Sze, Neudeck, Bhatanagar, SiC Power-Switching, Status and Prospects, Shenoy, Design and Process, Grant, Coen, Saint, ADA414680, Casady, Casady2, Vathulya, Agarwal2, Ryu-3, Ryu-6, Ryu-7 and applicants' admissions and admitted prior art in the '633 Patent (addressed in Exhibit 633-X). Each of these references addressed in Exhibit 633-X are reasonably pertinent to particular problems sought to be solved by the inventor in the '633 Patent. Each of these references are directed to various topics relevant to the issues in the '633 Patent including the application of MOSFET structures in various semiconductor substrate materials, the formation of contacts in silicon carbide, the configuration of MOSFET structures including configuration of sources / source electrodes, the structure, elements and operation of power MOSFETs generally, and the configuration and operation of well and substrate ties especially with respect to avoiding activation of parasitic bipolar elements and latch up. It would have been obvious to one of skill in the art that these more specific details about the application of MOSFET structures in various

semiconductor substrate materials, the formation of contacts in silicon carbide, the configuration of MOSFET structures including configuration of sources / source electrodes, the structure, elements and operation of power MOSFETs generally and the configuration and operation of well and substrate ties especially with respect to avoiding activation of parasitic bipolar elements and latch up are each known techniques and structures that could be combined in an overall vertical MOSFET structure that would yield nothing more than predicable results and that it would be desirable to do so because the application of MOSFET structures in various semiconductor substrate materials, the formation of contacts in silicon carbide, the configuration of MOSFET structures including configuration of sources / source electrodes, the structure, elements and operation of power MOSFETs generally and the configuration and operation of well and substrate ties especially with respect to avoiding activation of parasitic bipolar elements and latch up all relate to known structures and structural elements in semiconductors and MOSFETs, and a person of skill in the art would find it desirable in a vertical MOSFET design to include known structures to provide a vertical MOSFET in silicon carbide to achieve a device with improved capabilities such as the capability to operate at higher temperatures, higher device densities, higher speeds, or higher power levels, as compared to other semiconductor materials while also having reduced ON resistance and greater manufacturing alignment tolerance with a configuration that avoids unwanted activation of parasitic components in the device.

More specifically, as one example, a person of skill in the art would find it obvious to combine references such as Ryu and Williams to achieve a structure like that of the ’633 Patent. Ryu relates to “semiconductor devices . . . and, more particularly, to silicon carbide (SiC) metal-oxide semiconductor field effect transistors (MOSFETs).” See Ryu ¶3. Also, like the ’633

patent, Ryu discloses embodiments of SiC MOSFETs that "may reduce on-state resistance." Ryu at ¶¶39, 64, 65. Ryu expressly discloses a substrate (see e.g., Fig. 2A, element 10), drift layer (see e.g., Fig. 2A, element 12), a JFET region in a gap between p-wells (see e.g., gap element 21 in Fig. 2A). Ryu likewise discloses n+ source regions 24 formed in p-wells 20 and p+ base contact regions 22 and source electrodes 30 (see e.g., Fig. 2A). Ryu illustrates a cross section of a vertical MOSFET unit cell, and it is inherent that a vertical MOSFET is a three-dimensional structure. A person of skill in the art would recognize that the cross-section structure shown in Ryu Fig. 2A could be implemented in various three-dimensional unit cell configurations such as linear, square and hex cell unit cells. Likewise, a person of skill in the art would understand that reduced ON resistance and greater manufacturing alignment tolerance by increasing the source contact area and making periodic contact to the base region. A person of skill in the art would recognize that Williams teaches specific configurations of the source and base contact regions in a vertical MOSFET that may help to reduce ON resistance and provide greater manufacturing alignment tolerance with a configuration that avoids unwanted activation of parasitic components in the device. Like the '633 patent, Williams relates to vertical MOSFETs. See, e.g., Williams at 1:7–8, Figure 1. Williams notes that "[t]he primary design goal for a power MOSFET used as a switch is to achieve the lowest on-resistance by simultaneously minimizing each of its resistive constituents." *Id*., 1:50–52. One of these resistive constituents is the source contact resistance. *See id*., 1:33–37. Williams discloses "plan views of various source-body designs" in Figures 19A–19F—including plan views just like those of the '633 patent—to "achieve the lowest possible resistance" by maximizing the area of the N+ source regions and/or to "suppress parasitic bipolar turn-on, prevent snapback and ruggedize the device" (i.e., prevent unwanted activation of the parasitic bipolar transistor) by maximizing the contact of the P+ body

contact regions to the body region. *Id*., 10:17–18; 16:28–35. Like the '633 patent's source regions 154, 156 with "island" base contact regions 158, 160, Williams also discloses a continuous N+ source region with P+ body contact windows in Figure 19E. 10:23–24. Williams teaches that such a source-body design provides "better N+ contact resistance and less P+ contact area (less rugged)." 17:18–19. A person of skill in the art would have understood that, if fabricated as a linear cell, Ryu's cross-sectional view of its MOSFET would extend perpendicularly to the page. The linear cellular arrangement of Williams was well-known in the art, and as explained above, would have been an obvious design choice for Ryu's cellular structure. A person of skill in the art would have been motivated to implement Ryu's MOSFET according to Williams's teachings such that Ryu's MOSFET was formed using a linear cell structure having the source contacts 30 define and extend along a longitudinal axis. As explained above, Ryu and Williams are from the same field of endeavor. *See, e.g., Medtronic, Inc. v. Cardiac Pacemakers, Inc*., 721 F.2d 1563, 1574–75 (Fed. Cir. 1983); M.P.E.P. § 2141. Ryu discloses embodiments of vertical MOSFETs that "may reduce on-state resistance" compared to conventional vertical MOSFETs. Ryu at ¶¶6, 9, 39, Figure 1. Williams discloses structures for vertical MOSFETs that are used to reduce on-resistance. See, e.g., Williams at Figure 1, 8:15–16 ("reduce the on-resistance of the DMOSFET"), 16:31–32 ("achieve the lowest possible resistance"). Thus, both references are directed to vertical MOSFETs and aim at reducing on-resistance. Ryu ¶6 and Williams 1:7–8. A person of skill in the art would have been motivated to use Williams's teachings in Ryu. This is because Williams's and Ryu's MOSFETs share many common features. For example, both Williams's trench-gated vertical MOSFETs and Ryu's non-trench-gated vertical MOSFET include a parasitic BJT within the epilayer that could inadvertently be activated. For both Williams and Ryu, the solution to the potential problem

caused by this parasitic transistor is the same. Both Ryu and Williams prevent the parasitic BJT from activating by shorting the source to the body using a source electrode. A person of skill in the art would have recognized that features of Williams, such as Williams's well-known linear geometry, were applicable in Ryu. Accordingly, a person of skill in the art would have understood that the teachings of Williams were directly applicable to Ryu's SiC MOSFETs. Implementing Ryu's MOSFET in a linear cell structure such that Ryu's n+ regions 24 and, consequently, Ryu's source contacts 30 define and extend along a longitudinal axis as taught by Williams would have yielded expected, predictable results. This implementation of Ryu using a linear cellular structure would have been well within the knowledge and skillset of a person of skill in the art. A person of skill in the art would also have had a reasonable expectation of success. The combination of Ryu and Williams represents a straight-forward implementation of steps of the well-understood semiconductor fabrication processes to implement the shape and location of the structures, which a person of skill in the art would have been familiar with and been able to implement.

Further, to the extent Purdue argues that any claim limitation of the '633 Patent is not disclosed and rendered obvious by the combination of Ryu and Williams, it would be obvious to combine Ryu and Williams with one or more of the other prior art references listed herein, including, without limitation, the references addressed in Exhibit 633-X including, Das, Ueno-3, Glass, Peters, Baliga3, Suvorov, Ghezzo, Korman, Ryu-2, Sze, Neudeck, Bhatanagar, SiC Power-Switching, Status and Prospects, Shenoy, Design and Process, Grant, Coen, Saint, ADA414680, Casady, Casady2, Vathulya, Agarwal2, Ryu-3, Ryu-6, Ryu-7 and applicants' admissions and admitted prior art in the '633 Patent. Each of these references addressed in Exhibit 633-X are reasonably pertinent to particular problems sought to be solved by the inventor

in the ’633 Patent. Each of these references are directed to various topics relevant to the issues in the ’633 Patent including the application of MOSFET structures in various semiconductor substrate materials, the formation of contacts in silicon carbide, the configuration of MOSFET structures including configuration of sources / source electrodes, the structure, elements and operation of power MOSFETs generally, and the configuration and operation of well and substrate ties especially with respect to avoiding activation of parasitic bipolar elements and latch up.

Similarly, as a second example, a person of skill in the art would find it obvious to combine the MDmesh Products (charted in Exhibits 633-B10 and 633-B10(a) through 633-B10(h)), the PP26 Products (charted in Exhibit 633-B11), or the EZ67 Products (charted in Exhibit 633-B12), each of which disclose a vertical MOSFET device with a substrate and drift layer and sources and body regions formed in the substrate where body connections are made periodically to the body at body regions spaced apart in the source region along an axis aligned with the longitudinal direction of the source and a JFET region between the first source region and the second source region, with prior art such as Baliga or Ryu that teach that such MOSFET device structures can be and would be obvious to be implemented in silicon carbide by adapting some of the manufacturing techniques while utilizing the same configuration. Baliga teaches that conventional power MOSFETs, including silicon MOSFETs, “can be readily translated into silicon carbide using known manufacturing techniques.” *See* Baliga at 4:22–38. Ryu likewise discloses a silicon carbide MOSFET. *See* description of Ryu above and Ryu generally. Indeed, a person of skill in the art would know that the same structures can be implemented in both substrate material types as evidenced by references such as Hatade (“Furthermore, although a silicon substrate is typically used for the semiconductor substrate 1, the present invention can

also be executed for a semiconductor substrate using other semiconductor materials." Hatade at 11:23-26); Sze ("MOSFETs have been made with various semiconductors such as Ge,12 Si, and GaAs,13." Sze at 432.); Uneo-3 ("SiC is expected to be used in a wide range of applications in the future." Ueno-3 at 1:33-53); Neudeck ("Given the extreme usefulness and success of MOSFET-based electronics in silicon, it is naturally desirable to implement high-performance inversion channel MOSFETs in SiC." Neudeck at 285-6); Bhatanagar ("From the previous discussion, it is possible to conclude that the development of SiC Schottky rectifiers and power MOSFET's will provide devices which can deliver larger currents at very fast switching speed in power circuits with high breakdown voltages." Bhatanagar at 653-4); Glass ("One material for which great semiconductor potential has long been recognized is silicon carbide (SiC). Silicon carbide has well known advantageous semiconductor characteristics: a wide bandgap, a high thermal conductivity, a high melting point, a high electric field breakdown strength, a low dielectric constant, and a high saturated electron drift velocity. Taken together, these qualities potentially give electronic devices formed from silicon carbide the capability to operate at higher temperatures, higher device densities, higher speeds, higher power levels, and even under higher radiation densities, as compared to other semiconductor materials." Glass at 2:5-21); Peters ("A cell structure of the so called triple implanted vertical MOSFET [in SiC] is sketched in Fig. 1. One can easily imagine that structure, process and electrode materials are designed as close as possible to the well known silicon DMOS." Peters at 769); and Ghezzo ("An object of one embodiment of the invention is to provide a silicon carbide high voltage MOS power device having structural characteristics of a DMOS device. Because SiC has a higher critical electric field than silicon, the specific on-resistance of a SiC DMOS is expected to be significantly lower than that of a silicon DMOS with the same high voltage rating. A method of implementing

vertical power SiC transistor is to replace the conventional double-diffusion with an edge-shifted double ion implantation sequence to overcome the problem of very small dopant diffusivity in SiC. The channel is formed by successive ion implantation of an acceptor atom (such as boron or aluminum) and a donor atom (such as nitrogen or phosphorous) to form the base and source regions, respectively. These implants are edge-shifted and have different depths with junctions formed by using spacers which add a margin around an initial mask edge with the second implantation region being shifted from the first region." Ghezzo 1:50–67.), among others.

Ryu and Williams, as explained above, is one particular combination that a person of skill in the art would find obvious to make to reach the configuration of the '633 patent. The MDmesh Products, the PP26 Products or the EZ67 Products and Baliga (and similar prior art that teach the implementation of MOSFETs in silicon carbide) are other specific combinations that a person of skill in the art would find obvious to make to reach the configuration of the '633 patent.

For the same reasons as explained above for the example combination of Ryu and Williams, a person of skill in the art would find it obvious to combine any one or more of Ryu, Ryu-2, Ueno, Schörner, and Kataoka (addressed in Exhibits 633-A1 through 633-An), which each address vertical MOSFETs expressly disclosed as being formed in a silicon carbide substrate, with any one or more of Williams, Rexer, Frisina, Magri', Tonnel, Williams2, Baliga, Belverde, Hatade, the MDmesh Products, the PP26 Products, and the EZ67 Products (addressed in Exhibits 633-B1 through 633-Bn), which each disclose vertical MOSFET devices that expressly describe source and body regions where body connections are made periodically to the body at body regions spaced apart in the source region. Such combinations represent straight-forward implementation of steps of the well-understood semiconductor fabrication processes to

implement the shape and location of the structures, which a person of skill in the art would have been familiar with and been able to implement. Further, to the extent Purdue argues that any claim limitation of the '633 Patent is not disclosed and rendered obvious by the above combinations, it would be obvious for the reasons explained above to combine the above combinations with one or more of the references addressed in Exhibit 633-X including, Das, Ueno-3, Glass, Peters, Baliga3, Suvorov, Ghezzo, Korman, Ryu-2, Sze, Neudeck, Bhatanagar, SiC Power-Switching, Status and Prospects, Shenoy, Design and Process, Grant, Coen, Saint, ADA414680, Casady, Casady2, Vathulya, Agarwal2, Ryu-3, Ryu-6, Ryu-7 and applicants' admissions and admitted prior art in the '633 Patent, to make obvious the configuration of the '633 Patent.

Similarly, for the same reasons as explained above for the example combination of the MDmesh Products, the PP26 Products, or the EZ67 Products and Baliga (and similar art that teach the implementation of MOSFETs in silicon carbide), a person of skill in the art would find it obvious to combine any one or more of Williams, Rexer, Frisina, Magri', Tonnel, Williams2, Baliga, Belverde, Hatade, the MDmesh Products, the MDmesh Products, the PP26 Products, and the EZ67 Products with Baliga (or similar art that teach the implementation of vertical MOSFETs in silicon carbide with a substrate, drift layer, first and second sources, base contact regions and a source electrode such as Ryu, Ryu-2, Ueno, Schörner, Kataoka, Casady, Casady2, Vathulya, Agarwal2, Ryu-3, Ryu-6, and Ryu-7). Such combinations represent straight-forward implementation of steps of the well-understood semiconductor fabrication processes to implement the shape and location of the structures, which a person of skill in the art would have been familiar with and been able to implement. Further, to the extent Purdue argues that any claim limitation of the '633 Patent is not disclosed and rendered obvious by the above

combinations, it would be obvious for the reasons explained above to combine the above combinations with one or more of Das, Ueno-3, Glass, Peters, Baliga3, Suvorov, Ghezzo, Korman, Ryu-2, Sze, Neudeck, Bhatanagar, SiC Power-Switching, Status and Prospects, Shenoy, Design and Process, Grant, Coen, Saint, ADA414680, Casady, Casady2, Vathulya, Agarwal2, Ryu-3, Ryu-6, Ryu-7, and applicants' admissions and admitted prior art in the '633 Patent (addressed in Exhibit 633-X) to make obvious the configuration of the '633 Patent.

Accordingly, one of ordinary skill in the art would have been motivated to combine any of the references cited in Exhibits 633-A1 through 633-An and Exhibits 633-B1 through 633-Bn either with the knowledge of one skilled in the art or with other references in Exhibit 633-X in addition to such knowledge, and would have further recognized that combinations of these references would have improved similar systems and methods in the same way and address any problems that the '633 Patent sought to solve.

2. Additional Prior Art That Renders Obvious the Claims of the '112 Patent

The following table shows exemplary combinations that render claims 1, 6, 7, 10, 11 and 12 of the '112 Patent obvious. Specific examples of this obviousness are set forth below. The identification of primary references, secondary references, and obviousness combinations is not intended to be exhaustive—there are many possible combinations of the references that one of ordinary skill in the art would have been motivated to make—and it is not practical to provide details of all such possible combinations.

Exhibit	Patent or Pub. No. Title / Author	Filing or Priority Date	Short Cite
112-X	US 2002/0030191A1	Mar. 14, 2002	Das
112-X	US 6,136,727	Oct. 24, 2000	Ueno-3
112-X	US 5,323,022	Jun. 21, 1994	Glass
112-X	US 5,233,215	Aug. 3, 1993	Baliga3

Exhibit	Patent or Pub. No. Title / Author	Filing or Priority Date	Short Cite
112-X	US 5,510,281	Apr. 23, 1996	Ghezzo
112-X	US 5,317,184	May 31, 1994	Rexer
112-X	US 4,593,302	Jun. 3, 1986	Lidow
112-X	US 5,111,253	May 5, 1992	Korman
112-X	US 4,343,015	Aug. 3, 1982	Baliga2
112-X	US 3,475,234	Oct. 28, 1969	Kerwin
112-X	US 3,576,478	Apr. 27, 1971	Watkins
112-X	Peters, “4H-SiC Power MOSFET Blocking 1200V with a Gate Technology Compatible with Industrial Applications,” Materials Science Forum Vols 433-436 (2003) pp 769-772.	2003	Peters
112-X	US 6,107,142	Aug. 22, 2000	Suvorov
112-X	S.M. Sze, "Physics of Semiconductor Devices," 2nd Ed., John Wiley and Sons, 1981.	1981	Sze
112-X	P. G. Neudeck, “Progress in Silicon Carbide Semiconductor Electronics Technology,” Journal of Electronic Materials, Vol. 24, No. 4, 1995.	1995	Neudeck
112-X	M. Bhatnagar et al., “Comparison of 6H-SiC, 3C-SiC, and Si for Power Devices,” IEEE Transactions on Electron Devices, Vol. 40, No. 3. March 1993, p. 645.	Mar. 1993	Bhatanagar
112-X	Cooper et al., “SiC Power-Switching Devices—The Second Electronics Revolution?” Proceedings of the IEEE, Vol. 90, No. 6, June 2002 at 956.	Jun. 2002	SiC Power-Switching Devices
112-X	Shenoy et al., “High-Voltage Double-Implanted Power MOSFET’s in 6H-SiC,” IEEE Electron Device Letters, Vol. 18, No. 3, March 1997, at 93.	Apr. 2002	Shenoy
112-X	Y. Xiao et al., “Current Sensing Trench Power MOSFET for Automotive Applications,” Twentieth Annual IEEE Applied Power Electronics Conference and Exposition, 2005.	2005	Xiao
112-X	Shanfield, S. and Bay, S., 1984. Process characterization of PSG and BPSG plasma deposition. J. Electrochem. Soc, 131(9), pp.2202-2203.	1984	Shanfield
112-X	RCA Review - Kern, W. and Schnable, G.L., 1982. Device Applications. IIMBO, 43, p.423.	1982	Kern

Exhibit	Patent or Pub. No. Title / Author	Filing or Priority Date	Short Cite
112-X	S. Wolf and R. N. Tauber, "Silicon Processing for the VLSI Era – Vol 1., Lattice Press 1986.	1986	Wolf
112-X	P. Van Zant, "Microchip Fabrication – A Practical Guide to Semiconductor Processing," 1997, 3rd Ed., McGraw Hill 1997.	1997	Van Zant
112-X	S. P. Murarka et al, "Interlayer Dielectrics for Semiconductor Technologies" Elsevier 2003.	2003	Murarka
112-X	Grant, "Power MOSFETs Theory and Applications," John Wiley & Sons 1989.	1989	Grant
112-X	Baliga, "Modern Power Devices," John Wiley & Sons 1987.	1987	Baliga
112-X	R. W. Coen et al., "A High-Performance Planar Power MOSFET," IEEE Trans on Elec. Dev. Vol., ED-27, No. 2, Feb. 1980.	Feb. 1980	Coen
112-X	J.B. Casady et al., "Fabrication Procedures and Characterization of 6H-SiC MESFETs for USE in High Temperature Electronics," 1995 Proceedings. 45th Electronic Components and Technology Conference, 1995, pp. 261-265, IEEE doi 10.1109/ECTC.1995.514395	1995	Casady
112-X	J.B. Casady et al., "Silicon Carbide Power MOSFET Technology," Compound Semiconductors 1997. Proceedings of the IEEE Twenty-Fourth International Symposium on Compound Semiconductors. IEEE doi 10.1109/ISCS.1998.711654	1997	Casady2
112-X	V.R. Vathulya, "A Novel 6H-SiC Power DMOSFET with Implanted P-Well Spacer," IEEE Electron Device Letters, VOL. 20, NO. 7, July 1999, P. 354	2001	Vathulya
112-X	S. Ryu et al, "4H-SIC DMOSFETs for High Frequency Power Switching Applications," Mat. Res. Soc. Symp. Proc. Vol. 764 © 2003 Materials Research Society, MRS Online Proceedings Library (OPL) , Volume 764: Symposium C – New Applications for Wide-Bandgap Semiconductors , 2003 , C2.7 DOI https://doi.org/10.1557/PROC-764-C2.7	2003	Ryu-3
112-X	S. Ryu et al, "2 KV 4H-SiC DMOSFETS For Low Loss, High Frequency Switching Applications," International Journal of High Speed Electronics and Systems, Vol. 14, No. 03, pp. 879-883 (2004)	2004	Ryu-4

Exhibit	Patent or Pub. No. Title / Author	Filing or Priority Date	Short Cite
112-X	S. Ryu et al, "Development of 10 kV 4H-SiC Power DMOSFETs 2004," Materials Science Forum Vols. 457-460 (2004) pp 1385-1388	2004	Ryu-5
112-X	S. Ryu et al., "10A, 2.4kV Power DiMOSFET in 4H-SiC," IEEE Electron Device Letters, VOL. 23, NO. 6, June 2002	2002	Ryu-6
112-X	S. Ryu et al, "10-kV, 123-m-ohm-cm2 4H-SiC Power MOSFETs," IEEE Electron Device Letters, Vol. 25, No. 8, p. 556, Aug. 2004	Aug. 2004	Ryu-7
112-X	Admitted prior art in U.S. Pat. No. 8,035,112	Before the invention of the '112 Patent claims	Cooper '112 or "applicant's admitted prior art in US 8,035,112"

The following table shows exemplary combinations that render claims 1, 6, 7, 10, 11 and 12 of the '112 Patent obvious. Specific examples of this obviousness are set forth below. The identification of primary references, secondary references, and obviousness combinations is not intended to be exhaustive—there are many possible combinations of the references that one of ordinary skill in the art would have been motivated to make—and it is not practical to provide details of all such possible combinations:

One of the Following Primary References	In Combination with One or More of the Following References
• Nakamura (Ex. 112-A1) • Tanimoto (Ex. 112-A2) • Tanimoto2 (Ex. 112-A3) • Ueno (Ex. 112-A4) • Ueno2 (Ex. 112-A5) • Kataoka (Ex. 112-A6) • Kosugi (Ex. 112-A7) • Hefner (Ex. 112-A8) • Kojima (Ex. 112-A9) • Miura (Ex. 112-A10) • Peters (Ex. 112-A11)	• Any one or more of the '112 Patent "Primary" references – i.e., references identified in Exhibits 112-A1 through 112-An and 112-B1 through 112-Bn. • Any one or more of the references cited in Exhibit 112-X, i.e.: o Das o Ueno-3 o Glass o Baliga3 o Ghezzo o Rexer

One of the Following Primary References	In Combination with One or More of the Following References
• Agarwal (Ex. 112-A12) • Endo (Ex. 112-A13) • Tanimoto3 (Ex. 112-A14) • Agarwal2 (Ex. 112-A15) • Tonnel (Ex. 112-B1) • Magri' (Ex. 112-B2) • Rexer (Ex. 112-B3) • Belverde (Ex. 112-B4) • Hatade (Ex. 112-B5) • MDmesh Products (Ex. 112-B6, including Exs. 112-B6(a) – 112-B6(h)) • PP26 Products (Ex. 112-B7) • EZ67 Products (Ex. 112-B8)	○ Lidow ○ Korman ○ Baliga2 ○ Kerwin ○ Watkins ○ Peters ○ Suvorov ○ Sze ○ Neudeck ○ Bhatanagar ○ SiC Power-Switching Devices ○ Shenoy ○ Xiao ○ Shanfield ○ Kern ○ Wolf ○ Van Zant ○ Murarka ○ Grant ○ Baliga ○ Coen ○ Casady ○ Casady2 ○ Vathulya ○ Ryu-3 ○ Ryu-4 ○ Ryu-5 ○ Ryu-6 ○ Ryu-7 ○ Cooper '112 admissions and/or admitted prior art in US 8,035,112.

As explained below, one of ordinary skill in the art would have found it obvious and would have been motivated to make the combinations listed.

The ’112 patent is directed to semiconductor field effect transistors and to a semiconductor device such as vertical MOSFET structure or a silicon carbide power MOSFET. *See e.g.*, ’112 Patent at 1:44; 2:49-50, 3:60-63, claims 1, 6, Figure 3. And a particular aspect of the ’112 Patent and asserted claims, includes having both the tops and sides of the MOSFET gates covered with an insulating layer so that, for example, a metal deposited between the gates is insulated from the gates.

Nakamura is analogous art to the ’112 Patent because, among other things, it is in the same field of endeavor of the ’112 Patent and because Nakamura is pertinent to the particular problem sought to be solved by the inventor in the ’112 Patent. Specifically, like the ’112 Patent, Nakamura is directed to the configuration of a vertical MOSFET formed in a silicon carbide substrate and layers in that structure including the MOSFET gates and insulating and conductive layers over the gates. Because of the matter with which Nakamura deals, it logically would have commended itself to an inventor’s attention in considering the problem of how to configure a vertical MOSFET formed in silicon carbide and, in particular, the structure of the gates and insulating and conductive layers over the gates.

Tanimoto is analogous art to the ’112 Patent because, among other things, it is in the same field of endeavor of the ’112 Patent and because Tanimoto is pertinent to the particular problem sought to be solved by the inventor in the ’112 Patent. Specifically, like the ’112 Patent, Tanimoto is directed to the configuration of a vertical MOSFET formed in a silicon carbide substrate and layers in that structure including the MOSFET gates and insulating and conductive layers over the gates. Because of the matter with which Tanimoto deals, it logically would have commended itself to an inventor’s attention in considering the problem of how to

configure a vertical MOSFET formed in silicon carbide and, in particular, the structure of the gates and insulating and conductive layers over the gates.

Tanimoto2 is analogous art to the ’112 Patent because, among other things, it is in the same field of endeavor of the ’112 Patent and because Tanimoto2 is pertinent to the particular problem sought to be solved by the inventor in the ’112 Patent. Specifically, like the ’112 Patent, Tanimoto2 is directed to the configuration of a vertical MOSFET formed in a silicon carbide substrate and layers in that structure including the MOSFET gates and insulating and conductive layers over the gates. Because of the matter with which Tanimoto2 deals, it logically would have commended itself to an inventor’s attention in considering the problem of how to configure a vertical MOSFET formed in silicon carbide and, in particular, the structure of the gates and insulating and conductive layers over the gates.

Ueno is analogous art to the ’112 Patent because, among other things, it is in the same field of endeavor of the ’112 Patent and because Ueno is pertinent to the particular problem sought to be solved by the inventor in the ’112 Patent. Specifically, like the ’112 Patent, Ueno is directed to the configuration of a vertical MOSFET formed in a silicon carbide substrate and layers in that structure including the MOSFET gates and insulating and conductive layers over the gates. Because of the matter with which Ueno deals, it logically would have commended itself to an inventor’s attention in considering the problem of how to configure a vertical MOSFET formed in silicon carbide and, in particular, the structure of the gates and insulating and conductive layers over the gates.

Ueno2 is analogous art to the ’112 Patent because, among other things, it is in the same field of endeavor of the ’112 Patent and because Ueno2 is pertinent to the particular problem sought to be solved by the inventor in the ’112 Patent. Specifically, like the ’112 Patent, Ueno2

is directed to the configuration of a vertical MOSFET formed in a silicon carbide substrate and layers in that structure including the MOSFET gates and insulating and conductive layers over the gates. Because of the matter with which Ueno2 deals, it logically would have commended itself to an inventor's attention in considering the problem of how to configure a vertical MOSFET formed in silicon carbide and, in particular, the structure of the gates and insulating and conductive layers over the gates.

Kataoka is analogous art to the '112 Patent because, among other things, it is in the same field of endeavor of the '112 Patent and because Kataoka is pertinent to the particular problem sought to be solved by the inventor in the '112 Patent. Specifically, like the '112 Patent, Kataoka is directed to the configuration of a vertical MOSFET formed in a silicon carbide substrate and layers in that structure including the MOSFET gates and insulating and conductive layers over the gates. Because of the matter with which Kataoka deals, it logically would have commended itself to an inventor's attention in considering the problem of how to configure a vertical MOSFET formed in silicon carbide and, in particular, the structure of the gates and insulating and conductive layers over the gates.

Kosugi is analogous art to the '112 Patent because, among other things, it is in the same field of endeavor of the '112 Patent and because Kosugi is pertinent to the particular problem sought to be solved by the inventor in the '112 Patent. Specifically, like the '112 Patent, Kosugi is directed to the configuration of a vertical MOSFET formed in a silicon carbide substrate and layers in that structure including the MOSFET gates and insulating and conductive layers over the gates. Because of the matter with which Kosugi deals, it logically would have commended itself to an inventor's attention in considering the problem of how to configure a vertical

MOSFET formed in silicon carbide and, in particular, the structure of the gates and insulating and conductive layers over the gates.

Hefner is analogous art to the ’112 Patent because, among other things, it is in the same field of endeavor of the ’112 Patent and because Hefner is pertinent to the particular problem sought to be solved by the inventor in the ’112 Patent. Specifically, like the ’112 Patent, Hefner is directed to the configuration of a vertical MOSFET formed in a silicon carbide substrate and layers in that structure including the MOSFET gates and insulating and conductive layers over the gates. Because of the matter with which Hefner deals, it logically would have commended itself to an inventor’s attention in considering the problem of how to configure a vertical MOSFET formed in silicon carbide and, in particular, the structure of the gates and insulating and conductive layers over the gates.

Kojima is analogous art to the ’112 Patent because, among other things, it is in the same field of endeavor of the ’112 Patent and because Kojima is pertinent to the particular problem sought to be solved by the inventor in the ’112 Patent. Specifically, like the ’112 Patent, Kojima is directed to the configuration of a vertical MOSFET formed in a silicon carbide substrate and layers in that structure including the MOSFET gates and insulating and conductive layers over the gates. Because of the matter with which Kojima deals, it logically would have commended itself to an inventor’s attention in considering the problem of how to configure a vertical MOSFET formed in silicon carbide and, in particular, the structure of the gates and insulating and conductive layers over the gates.

Miura is analogous art to the ’112 Patent because, among other things, it is in the same field of endeavor of the ’112 Patent and because Miura is pertinent to the particular problem sought to be solved by the inventor in the ’112 Patent. Specifically, like the ’112 Patent, Miura

is directed to the configuration of a vertical MOSFET formed in a silicon carbide substrate and layers in that structure including the MOSFET gates and insulating and conductive layers over the gates. Because of the matter with which Miura deals, it logically would have commended itself to an inventor's attention in considering the problem of how to configure a vertical MOSFET formed in silicon carbide and, in particular, the structure of the gates and insulating and conductive layers over the gates.

Peters is analogous art to the '112 Patent because, among other things, it is in the same field of endeavor of the '112 Patent and because Peters is pertinent to the particular problem sought to be solved by the inventor in the '112 Patent. Specifically, like the '112 Patent, Peters is directed to the configuration of a vertical MOSFET formed in a silicon carbide substrate and layers in that structure including the MOSFET gates and insulating and conductive layers over the gates. Because of the matter with which Peters deals, it logically would have commended itself to an inventor's attention in considering the problem of how to configure a vertical MOSFET formed in silicon carbide and, in particular, the structure of the gates and insulating and conductive layers over the gates.

Agarwal is analogous art to the '112 Patent because, among other things, it is in the same field of endeavor of the '112 Patent and because Agarwal is pertinent to the particular problem sought to be solved by the inventor in the '112 Patent. Specifically, like the '112 Patent, Agarwal is directed to the configuration of a vertical MOSFET formed in a silicon carbide substrate and layers in that structure including the MOSFET gates and insulating and conductive layers over the gates. Because of the matter with which Agarwal deals, it logically would have commended itself to an inventor's attention in considering the problem of how to configure a

vertical MOSFET formed in silicon carbide and, in particular, the structure of the gates and insulating and conductive layers over the gates.

Endo is analogous art to the ’112 Patent because, among other things, it is in the same field of endeavor of the ’112 Patent and because Endo is pertinent to the particular problem sought to be solved by the inventor in the ’112 Patent. Specifically, like the ’112 Patent, Endo is directed to the configuration of a vertical MOSFET formed in a silicon carbide substrate and layers in that structure including the MOSFET gates and insulating and conductive layers over the gates. Because of the matter with which Endo deals, it logically would have commended itself to an inventor’s attention in considering the problem of how to configure a vertical MOSFET formed in silicon carbide and, in particular, the structure of the gates and insulating and conductive layers over the gates.

Tanimoto3 is analogous art to the ’112 Patent because, among other things, it is in the same field of endeavor of the ’112 Patent and because Tanimoto3 is pertinent to the particular problem sought to be solved by the inventor in the ’112 Patent. Specifically, like the ’112 Patent, Tanimoto3 is directed to the configuration of a vertical MOSFET formed in a silicon carbide substrate and layers in that structure including the MOSFET gates and insulating and conductive layers over the gates. Because of the matter with which Tanimoto3 deals, it logically would have commended itself to an inventor’s attention in considering the problem of how to configure a vertical MOSFET formed in silicon carbide and, in particular, the structure of the gates and insulating and conductive layers over the gates.

Agarwal2 is analogous art to the ’112 Patent because, among other things, it is in the same field of endeavor of the ’112 Patent and because Agarwal2 is pertinent to the particular problem sought to be solved by the inventor in the ’112 Patent. Specifically, like the ’112

Patent, Agarwal2 is directed to the configuration of a vertical MOSFET formed in a silicon carbide substrate and layers in that structure including the MOSFET gates and insulating and conductive layers over the gates. Because of the matter with which Agarwal2 deals, it logically would have commended itself to an inventor's attention in considering the problem of how to configure a vertical MOSFET formed in silicon carbide and, in particular, the structure of the gates and insulating and conductive layers over the gates.

Tonnel is analogous art to the '112 Patent because, among other things, it is in the same field of endeavor of the '112 Patent and because Tonnel is pertinent to the particular problem sought to be solved by the inventor in the '112 Patent. Specifically, like the '112 Patent, Tonnel is directed to the configuration of a vertical MOSFET and addresses the layers in that structure including the MOSFET gates and insulating and conductive layers over the gates. Because of the matter with which Tonnel deals, it logically would have commended itself to an inventor's attention in considering the problem of how to configure a vertical MOSFET formed in silicon carbide and, in particular, the structure of the gates and insulating and conductive layers over the gates.

Magri' is analogous art to the '112 Patent because, among other things, it is in the same field of endeavor of the '112 Patent and because Magri' is pertinent to the particular problem sought to be solved by the inventor in the '112 Patent. Specifically, like the '112 Patent, Magri' is directed to the configuration of a vertical MOSFET and addresses the layers in that structure including the MOSFET gates and insulating and conductive layers over the gates. Because of the matter with which Magri' deals, it logically would have commended itself to an inventor's attention in considering the problem of how to configure a vertical MOSFET formed in silicon

carbide and, in particular, the structure of the gates and insulating and conductive layers over the gates.

Rexer is analogous art to the ’112 Patent because, among other things, it is in the same field of endeavor of the ’112 Patent and because Rexer is pertinent to the particular problem sought to be solved by the inventor in the ’112 Patent. Specifically, like the ’112 Patent, Rexer is directed to the configuration of a vertical MOSFET and addresses the layers in that structure including the MOSFET gates and insulating and conductive layers over the gates. Because of the matter with which Rexer deals, it logically would have commended itself to an inventor’s attention in considering the problem of how to configure a vertical MOSFET formed in silicon carbide and, in particular, the structure of the gates and insulating and conductive layers over the gates.

Belverde is analogous art to the ’112 Patent because, among other things, it is in the same field of endeavor of the ’112 Patent and because Belverde is pertinent to the particular problem sought to be solved by the inventor in the ’112 Patent. Specifically, like the ’112 Patent, Belverde is directed to the configuration of a vertical MOSFET and addresses the layers in that structure including the MOSFET gates and insulating and conductive layers over the gates. Because of the matter with which Belverde deals, it logically would have commended itself to an inventor’s attention in considering the problem of how to configure a vertical MOSFET formed in silicon carbide and, in particular, the structure of the gates and insulating and conductive layers over the gates.

Hatade is analogous art to the ’112 Patent because, among other things, it is in the same field of endeavor of the ’112 Patent and because Hatade is pertinent to the particular problem sought to be solved by the inventor in the ’112 Patent. Specifically, like the ’112 Patent, Hatade

is directed to the configuration of a vertical MOSFET and addresses the layers in that structure including the MOSFET gates and insulating and conductive layers over the gates. Because of the matter with which Hatade deals, it logically would have commended itself to an inventor's attention in considering the problem of how to configure a vertical MOSFET formed in silicon carbide and, in particular, the structure of the gates and insulating and conductive layers over the gates.

The MDmesh Products (including MDx0, MDx1, MDx2, MDx5, MDx9, MDxB, MDxN) are analogous art to the '112 Patent because, among other things, they are in the same field of endeavor of the '112 Patent and because the MDmesh Products are pertinent to the particular problem sought to be solved by the inventor in the '112 Patent. Specifically, like the '112 Patent, the MDmesh Products are directed to the configuration of a vertical MOSFET and addresses the layers in that structure including the MOSFET gates and insulating and conductive layers over the gates. Because of the matter with which the MDmesh Products deal, they logically would have commended themselves to an inventor's attention in considering the problem of how to configure a vertical MOSFET formed in silicon carbide and, in particular, the structure of the gates and insulating and conductive layers over the gates.

The PP26 Products are analogous art to the '112 Patent because, among other things, they are in the same field of endeavor of the '112 Patent and because the PP26 Products are pertinent to the particular problem sought to be solved by the inventor in the '112 Patent. Specifically, like the '112 Patent, the PP26 Products are directed to the configuration of a vertical MOSFET and addresses the layers in that structure including the MOSFET gates and insulating and conductive layers over the gates. Because of the matter with which the PP26 Products deal, they logically would have commended themselves to an inventor's attention in considering the

problem of how to configure a vertical MOSFET formed in silicon carbide and, in particular, the structure of the gates and insulating and conductive layers over the gates.

The EZ67 Products are analogous art to the ’112 Patent because, among other things, they are in the same field of endeavor of the ’112 Patent and because the EZ67 Products are pertinent to the particular problem sought to be solved by the inventor in the ’112 Patent. Specifically, like the ’112 Patent, the EZ67 Products are directed to the configuration of a vertical MOSFET and addresses the layers in that structure including the MOSFET gates and insulating and conductive layers over the gates. Because of the matter with which the EZ67 Products deal, they logically would have commended themselves to an inventor’s attention in considering the problem of how to configure a vertical MOSFET formed in silicon carbide and, in particular, the structure of the gates and insulating and conductive layers over the gates.

Hatade is analogous art to the ’112 Patent because, among other things, it is in the same field of endeavor of the ’112 Patent, vertical MOSFETs, and because Hatade is pertinent to the application of MOSFET structures in various semiconductor substrate materials, which is one of the issues that concerns the ’112 Patent. Because of the matter with which Hatade deals, it logically would have commended itself to an inventor’s attention in considering the problem of how to configure a vertical MOSFET formed in silicon carbide and, in particular, the structure of the gates and insulating and conductive layers over the gates.

Das is analogous art to the ’112 Patent because, among other things, it is in the same field of endeavor of the ’112 Patent, double-diffused or double-implanted MOSFETs, and because Das is pertinent to the application of MOSFET structures in silicon carbide substrate material, which is one of the issues that concerns the ’112 Patent. Because of the matter with which Das deals, it logically would have commended itself to an inventor’s attention in considering the

problem of how to configure a vertical MOSFET formed in silicon carbide and, in particular, the structure of the gates and insulating and conductive layers over the gates.

Ueno-3 is analogous art to the ’112 Patent because, among other things, it is in the same field of endeavor of the ’112 Patent, MOSFETs, and because Ueno-3 is pertinent to the application of MOSFET structures in silicon carbide substrate material and the favorability of SIC in forming of thermal oxide, which is one of the issues that concerns the ’112 Patent. Because of the matter with which Ueno-3 deals, it logically would have commended itself to an inventor’s attention in considering the problem of how to configure a vertical MOSFET formed in silicon carbide and, in particular, the structure of the gates and insulating and conductive layers over the gates.

Glass is analogous art to the ’112 Patent because, among other things, it is in the same field of endeavor of the ’112 Patent, MOSFETs, and because Glass is pertinent to the application of MOSFET structures in silicon carbide substrate material and favorable semiconductor characteristics that motivate the use thereof, which is one of the issues that concerns the ’112 Patent. Because of the matter with which Glass deals, it logically would have commended itself to an inventor’s attention in considering the problem of how to configure a vertical MOSFET formed in silicon carbide and, in particular, the structure of the gates and insulating and conductive layers over the gates.

Baliga3 is analogous art to the ’112 Patent because, among other things, it is in the same field of endeavor of the ’112 Patent, vertical MOSFETs, and because Baliga3 is pertinent to the application of MOSFET structures in silicon carbide substrate material and the ability that DMOSFET or UMOSFET can be readily translated into silicon carbide using known manufacturing techniques, which is one of the issues that concerns the ’112 Patent. Because of

the matter with which Baliga3 deals, it logically would have commended itself to an inventor's attention in considering the problem of how to configure a vertical MOSFET formed in silicon carbide and, in particular, the structure of the gates and insulating and conductive layers over the gates.

Ghezzo is analogous art to the '112 Patent because, among other things, it is in the same field of endeavor of the '112 Patent, vertical MOSFETs, and because Ghezzo is pertinent to the application of MOSFET structures in silicon carbide substrate material, which is one of the issues that concerns the '112 Patent. Because of the matter with which Ghezzo deals, it logically would have commended itself to an inventor's attention in considering the problem of how to configure a vertical MOSFET formed in silicon carbide and, in particular, the structure of the gates and insulating and conductive layers over the gates.

Rexer is analogous art to the '112 Patent because, among other things, it is in the same field of endeavor of the '112 Patent, vertical MOSFETs, and because Rexer is pertinent to MOSFET structures including the structure of the gates and insulating and conductive layers over the gates, which is one of the issues that concerns the '112 Patent. Because of the matter with which Rexer deals, it logically would have commended itself to an inventor's attention in considering the problem of how to configure a vertical MOSFET formed in silicon carbide and, in particular, the structure of the gates and insulating and conductive layers over the gates.

Lidow is analogous art to the '112 Patent because, among other things, it is in the same field of endeavor of the '112 Patent, power MOSFETs, and because Lidow is pertinent to MOSFET structures including the structure of the gates and insulating and conductive layers over the gates, which is one of the issues that concerns the '112 Patent. Because of the matter with which Lidow deals, it logically would have commended itself to an inventor's attention in

considering the problem of how to configure a vertical MOSFET formed in silicon carbide and, in particular, the structure of the gates and insulating and conductive layers over the gates.

Korman is analogous art to the ’112 Patent because, among other things, it is in the same field of endeavor of the ’112 Patent, vertical MOSFETs, and because Korman is pertinent to configuration of MOSFET structures including the structure of sources, source electrodes with respect to the gates and insulating and conductive layers over the gates, which is one of the issues that concerns the ’112 Patent. Because of the matter with which Korman deals, it logically would have commended itself to an inventor’s attention in considering the problem of how to configure a vertical MOSFET formed in silicon carbide and, in particular, the structure of the gates and insulating and conductive layers over the gates.

Baliga2 is analogous art to the ’112 Patent because, among other things, it is in the same field of endeavor of the ’112 Patent, vertical channel FETs, and because Baliga2 is pertinent to configuration of MOSFET structures including the configuration of source contact metallization and gate metal, which is one of the issues that concerns the ’112 Patent. Because of the matter with which Baliga2 deals, it logically would have commended itself to an inventor’s attention in considering the problem of how to configure a vertical MOSFET formed in silicon carbide and, in particular, the structure of the gates and insulating and conductive layers over the gates.

Kerwin is analogous art to the ’112 Patent because, among other things, it is in the same field of endeavor of the ’112 Patent, MIS devices, and because Kerwin is pertinent to configuration of MIS devices and the necessity of the insulating layer of the gate electrode to overlap the source and drain when the gate is formed by a separate masking step, which is one of the issues that concerns the ’112 Patent. Because of the matter with which Kerwin deals, it logically would have commended itself to an inventor’s attention in considering the problem of

how to configure a vertical MOSFET formed in silicon carbide and, in particular, the structure of the gates and insulating and conductive layers over the gates.

Watkins is analogous art to the ’112 Patent because, among other things, it is in the same field of endeavor of the ’112 Patent, FET devices, and because Watkins is pertinent to configuration of MIS devices and the necessity of gate overlap when the gate is formed by a separate masking step, which is one of the issues that concerns the ’112 Patent. Because of the matter with which Watkins deals, it logically would have commended itself to an inventor’s attention in considering the problem of how to configure a vertical MOSFET formed in silicon carbide and, in particular, the structure of the gates and insulating and conductive layers over the gates.

Peters is analogous art to the ’112 Patent because, among other things, it is in the same field of endeavor of the ’112 Patent, MOSFETs, and because Peters is pertinent to the application of MOSFET structures in silicon carbide substrate material including the structure of the gates and insulating and conductive layers over the gates, which is one of the issues that concerns the ’112 Patent. Because of the matter with which Peters deals, it logically would have commended itself to an inventor’s attention in considering the problem of how to configure a vertical MOSFET formed in silicon carbide and, in particular, the structure of the gates and insulating and conductive layers over the gates.

Suvorov is analogous art to the ’112 Patent because, among other things, it is in the same field of endeavor of the ’112 Patent, MOSFETs, and because Suvorov is pertinent to the application of MOSFET structures in silicon carbide substrate material, which is one of the issues that concerns the ’112 Patent. Because of the matter with which Suvorov deals, it logically would have commended itself to an inventor’s attention in considering the problem of

how to configure a vertical MOSFET formed in silicon carbide and, in particular, the structure of the gates and insulating and conductive layers over the gates.

Sze is analogous art to the ’112 Patent because, among other things, it is in the same field of endeavor of the ’112 Patent, MOSFETs and structures used in semiconductors, and because Sze is pertinent to the application of MOSFET structures in various semiconductor substrate materials and the formation of oxides and insulating layers in semiconductor devices, which is one of the issues that concerns the ’112 Patent. Because of the matter with which Sze deals, it logically would have commended itself to an inventor’s attention in considering the problem of how to configure a vertical MOSFET formed in silicon carbide and, in particular, the structure of the gates and insulating and conductive layers over the gates.

Neudeck is analogous art to the ’112 Patent because, among other things, it is in the same field of endeavor of the ’112 Patent, MOSFETs including vertical MOSFETs, and because Neudeck is pertinent to the application of MOSFET structures in silicon carbide substrate material, which is one of the issues that concerns the ’112 Patent. Because of the matter with which Neudeck deals, it logically would have commended itself to an inventor’s attention in considering the problem of how to configure a vertical MOSFET formed in silicon carbide and, in particular, the structure of the gates and insulating and conductive layers over the gates.

Bhatanagar is analogous art to the ’112 Patent because, among other things, it is in the same field of endeavor of the ’112 Patent, vertical DMOSFETs, and because Bhatanagar is pertinent to the application of MOSFET structures in silicon carbide substrate material, which is one of the issues that concerns the ’112 Patent. Because of the matter with which Bhatanagar deals, it logically would have commended itself to an inventor’s attention in considering the

problem of how to configure a vertical MOSFET formed in silicon carbide and, in particular, the structure of the gates and insulating and conductive layers over the gates.

SiC Power-Switching Devices is analogous art to the ’112 Patent because, among other things, it is in the same field of endeavor of the ’112 Patent, vertical DMOSFETs, and because SiC Power-Switching Devices is pertinent to the application of MOSFET structures in silicon carbide substrate material, which is one of the issues that concerns the ’112 Patent. Because of the matter with which SiC Power-Switching Devices deals, it logically would have commended itself to an inventor’s attention in considering the problem of how to configure a vertical MOSFET formed in silicon carbide and, in particular, the structure of the gates and insulating and conductive layers over the gates.

Shenoy is analogous art to the ’112 Patent because, among other things, it is in the same field of endeavor of the ’112 Patent, vertical DMOSFETs, and because Shenoy is pertinent to the application of MOSFET structures in silicon carbide substrate material, which is one of the issues that concerns the ’112 Patent. Because of the matter with which Shenoy deals, it logically would have commended itself to an inventor’s attention in considering the problem of how to configure a vertical MOSFET formed in silicon carbide and, in particular, the structure of the gates and insulating and conductive layers over the gates.

Xiao is analogous art to the ’112 Patent because, among other things, it is in the same field of endeavor of the ’112 Patent, vertical power MOSFETs, and because Xiao is pertinent to MOSFET structures including the structure of the gates and insulating and conductive layers over the gates including source and gate contacts, which is one of the issues that concerns the ’112 Patent. Because of the matter with which Xiao deals, it logically would have commended itself to an inventor’s attention in considering the problem of how to configure a vertical

MOSFET formed in silicon carbide and, in particular, the structure of the gates and insulating and conductive layers over the gates.

Shanfield is analogous art to the ’112 Patent because, among other things, it is in the same field of endeavor of the ’112 Patent, MOS devices, and because Shanfield is pertinent to MOSFET structures including the structure of the gates and insulating layers over the gates, which is one of the issues that concerns the ’112 Patent. Because of the matter with which Shanfield deals, it logically would have commended itself to an inventor’s attention in considering the problem of how to configure a vertical MOSFET formed in silicon carbide and, in particular, the structure of the gates and insulating and conductive layers over the gates.

Kern is analogous art to the ’112 Patent because, among other things, it is in the same field of endeavor of the ’112 Patent, MOS devices, and because Kern is pertinent to device structures and use of borophosphosilicate glass (BPSG) films as deposited dielectrics in MOS devices and an example of a dielectric used in MOS devices, which is one of the issues that concerns the ’112 Patent. Because of the matter with which Kern deals, it logically would have commended itself to an inventor’s attention in considering the problem of how to configure a vertical MOSFET formed in silicon carbide and, in particular, the structure of the gates and insulating and conductive layers over the gates.

Wolf is analogous art to the ’112 Patent because, among other things, it is in the same field of endeavor of the ’112 Patent, semiconductor devices, and because Wolf is pertinent to insulating materials for semiconductors including thermal oxidation of polysilicon and CVD silicon dioxide, which is one of the issues that concerns the ’112 Patent. Because of the matter with which Wolf deals, it logically would have commended itself to an inventor’s attention in

considering the problem of how to configure a vertical MOSFET formed in silicon carbide and, in particular, the structure of the gates and insulating and conductive layers over the gates.

Van Zant is analogous art to the ’112 Patent because, among other things, it is in the same field of endeavor of the ’112 Patent, microchip devices, and because Van Zant is pertinent to deposition of metal layers and step coverage in semiconductor devices, which is one of the issues that concerns the ’112 Patent. Because of the matter with which Van Zant deals, it logically would have commended itself to an inventor’s attention in considering the problem of how to configure a vertical MOSFET formed in silicon carbide and, in particular, the structure of the gates and insulating and conductive layers over the gates.

Murarka is analogous art to the ’112 Patent because, among other things, it is in the same field of endeavor of the ’112 Patent, semiconductor devices, and because Murarka is pertinent to the structure and layers of semiconductor devices including insulating layers and types and compositions thereof., which is one of the issues that concerns the ’112 Patent. Because of the matter with which Murarka deals, it logically would have commended itself to an inventor’s attention in considering the problem of how to configure a vertical MOSFET formed in silicon carbide and, in particular, the structure of the gates and insulating and conductive layers over the gates.

Grant is analogous art to the ’112 Patent because, among other things, it is in the same field of endeavor of the ’112 Patent, power MOSFETs, and because Grant is pertinent to the structure, elements and operation of power MOSFETs including the structure of the layers over the device including source and gate contacts, which is one of the issues that concerns the ’112 Patent. Because of the matter with which Grant deals, it logically would have commended itself to an inventor’s attention in considering the problem of how to configure a vertical MOSFET

formed in silicon carbide and, in particular, the structure of the gates and insulating and conductive layers over the gates.

Baliga is analogous art to the ’112 Patent because, among other things, it is in the same field of endeavor of the ’112 Patent, vertical-channel power MOSFET structures, and because Baliga is pertinent to the structure, elements and operation of power MOSFETs including gate structures, which is one of the issues that concerns the ’112 Patent. Because of the matter with which Baliga deals, it logically would have commended itself to an inventor’s attention in considering the problem of how to configure a vertical MOSFET formed in silicon carbide and, in particular, the structure of the gates and insulating and conductive layers over the gates.

Coen is analogous art to the ’112 Patent because, among other things, it is in the same field of endeavor of the ’112 Patent, planar power MOSFETs, and because Coen is pertinent to the structure, elements and operation of power MOSFETs including the structure of the layers over the device including source and gate contacts, which is one of the issues that concerns the ’112 Patent. Because of the matter with which Coen deals, it logically would have commended itself to an inventor’s attention in considering the problem of how to configure a vertical MOSFET formed in silicon carbide and, in particular, the structure of the gates and insulating and conductive layers over the gates.

Casady is analogous art to the ’112 Patent because, among other things, it is in the same field of endeavor of the ’112 Patent, SiC FET structures, and because Casady is pertinent to fabrication of silicon carbide FET structures, which is one of the issues that concerns the ’112 Patent. Because of the matter with which Casady deals, it logically would have commended itself to an inventor’s attention in considering the problem of how to configure a vertical

MOSFET formed in silicon carbide and, in particular, the structure of the gates and insulating and conductive layers over the gates.

Casady2 is analogous art to the ’112 Patent because, among other things, it is in the same field of endeavor of the ’112 Patent, vertical DiMOSFETs, and because Casady2 is pertinent to the structure, elements and operation of power MOSFETs including gate and source contact structures, which is one of the issues that concerns the ’112 Patent. Because of the matter with which Casady2 deals, it logically would have commended itself to an inventor’s attention in considering the problem of how to configure a vertical MOSFET formed in silicon carbide and, in particular, the structure of the gates and insulating and conductive layers over the gates.

Vathulya is analogous art to the ’112 Patent because, among other things, it is in the same field of endeavor of the ’112 Patent, vertical DiMOSFETs, and because Vathulya is pertinent to the structure, elements and operation of power MOSFETs including doped JFET region, which is one of the issues that concerns the ’112 Patent. Because of the matter with which Vathulya deals, it logically would have commended itself to an inventor’s attention in considering the problem of how to configure a vertical MOSFET formed in silicon carbide and, in particular, the structure of the gates and insulating and conductive layers over the gates.

Ryu-3 is analogous art to the ’112 Patent because, among other things, it is in the same field of endeavor of the ’112 Patent, vertical DMOSFETs, and because Ryu-3 is pertinent to the structure, elements and operation of MOSFETs including gate and source contacts, which is one of the issues that concerns the ’112 Patent. Because of the matter with which Ryu-3 deals, it logically would have commended itself to an inventor’s attention in considering the problem of how to configure a vertical MOSFET formed in silicon carbide and, in particular, the structure of the gates and insulating and conductive layers over the gates.

Ryu-4 is analogous art to the ’112 Patent because, among other things, it is in the same field of endeavor of the ’112 Patent, vertical DMOSFETs, and because Ryu-4 is pertinent to the application of MOSFET structures in silicon carbide substrate material, which is one of the issues that concerns the ’112 Patent. Because of the matter with which Ryu-4 deals, it logically would have commended itself to an inventor’s attention in considering the problem of how to configure a vertical MOSFET formed in silicon carbide and, in particular, the structure of the gates and insulating and conductive layers over the gates.

Ryu-5 is analogous art to the ’112 Patent because, among other things, it is in the same field of endeavor of the ’112 Patent, vertical DMOSFETs, and because Ryu-5 is pertinent to the structure, elements and operation of power MOSFETs including the structure of the layers over the device including source and gate contacts, which is one of the issues that concerns the ’112 Patent. Because of the matter with which Ryu-5 deals, it logically would have commended itself to an inventor’s attention in considering the problem of how to configure a vertical MOSFET formed in silicon carbide and, in particular, the structure of the gates and insulating and conductive layers over the gates.

Ryu-6 is analogous art to the ’112 Patent because, among other things, it is in the same field of endeavor of the ’112 Patent, vertical DMOSFETs, and because Ryu-6 is pertinent to the structure, elements and operation of power MOSFETs including the structure of the layers over the device including source and gate contacts, which is one of the issues that concerns the ’112 Patent. Because of the matter with which Ryu-6 deals, it logically would have commended itself to an inventor’s attention in considering the problem of how to configure a vertical MOSFET formed in silicon carbide and, in particular, the structure of the gates and insulating and conductive layers over the gates.

Ryu-7 is analogous art to the ’112 Patent because, among other things, it is in the same field of endeavor of the ’112 Patent, vertical DMOSFETs, and because Ryu-7 is pertinent to the application of MOSFET structures in silicon carbide substrate material, which is one of the issues that concerns the ’112 Patent. Because of the matter with which Ryu-7 deals, it logically would have commended itself to an inventor’s attention in considering the problem of how to configure a vertical MOSFET formed in silicon carbide and, in particular, the structure of the gates and insulating and conductive layers over the gates.

The Asserted Claims of the ’112 Patent would have been obvious over any one of—or combination of—the primary references addressed in Exhibits 112-A1 through 112-An and Exhibits 112-B1 through 112-Bn alone or in combination with knowledge of one of ordinary skill in the art and/or in combination with one or more of the references addressed in Exhibit 112-X. Specifically, these combinations would have been obvious for a number of reasons including because all the claimed elements were known in the prior art, and one skilled in the art could have combined the elements as claimed by known methods with no change in their respective functions and the combination would yield nothing more than predictable results to improve a similar device in the same way.

For example, Nakamura, Tanimoto, Tanimoto2, Ueno, Ueno2, Kataoka, Kosugi, Hefner, Kojima, Miura, Peters, Agarwal, Endo, Tanimoto3 and Agarwal2 (addressed in Exhibits 112-A1 through 112-An) all address a silicon carbide vertical MOSFET with a substrate and drift layer, gates having both tops and sides covered with an insulating material, another insulating layer under the gate between the gate and the substrate, and a metal layer covering gates and areas between the gates. Many of these references depict a cross section view of the disclosed structure and a person of skill in the art would know that vertical channel MOSFETs are

inherently three-dimensional devices and that it was well known for a power MOSFET to comprise many unit cells all of which are covered with metal layer common source electrode. Likewise, a person of skill in the art would know the design considerations applicable in selecting a composition and thickness for the insulating layer over the top and sides of the gates and the composition and thickness of the insulating layer under the gates between the gate and substrate, and that there are well known approaches for providing external electrical connection to the source and gates including the specific layout specified in the Asserted Claims of the '112 Patent.

Collectively these references disclose that the configuration of the vertical MOSFET including a silicon carbide substrate and drift layer, gates having both tops and sides covered with an insulating material, another insulating layer under the gate between the gate and the substrate, and a metal layer covering gates and areas between the gates, in the configuration claimed, were all known in the vertical MOSFET art. As a result, for example, to the extent Purdue alleges that any one primary prior art reference does not expressly disclose a particular structure, layout, configuration or thickness of the Asserted Claim, it would have been obvious to one of skill in the art that a known structure, layout, configuration or thickness from another reference also known for use in or applicable to vertical MOSFETs could be combined in an overall vertical MOSFET structure that would yield nothing more than predicable results, and that it would be desirable and/or a mere matter of design choice to do so because a metal layer as a common source electrode provides low resistance and facilitates alignment with source regions.

Similarly, Tonnel, Magri', Rexer, Belverde, Hatade, the MDmesh Product, the PP26 Products, and the EZ67 Products (addressed in Exhibits 112-B1 through 112-Bn) each disclose

vertical MOSFET devices including a semiconductor substrate and drift layer, gates having both tops and sides covered with an insulating material, another insulating layer under the gate between the gate and the substrate, and a metal layer covering gates and areas between the gates. To the extent any of these references disclose a vertical MOSFET nominally in a silicon substrate, a person of skill in the art would recognize, as was long known before the purported invention of the '112 patent, that the general unit cell cross section configuration of a vertical MOSFET can be the same regardless of whether the substrate is silicon or silicon carbide, and that implementing the structure in a silicon carbide substrate would take advantage of the well-known semiconductor characteristics of silicon carbide such as: wide bandgap, high thermal conductivity, high melting point, high electric field breakdown strength, low dielectric constant, and high saturated electron drift velocity. As a result, for example, to the extent Bell alleges that any one reference does not expressly disclose a particular substrate type of the Asserted Claim, it would have been obvious to one of skill in the art that as a known substrate type for vertical MOSFETs, use of a silicon carbide substrate could be combined in an overall vertical MOSFET structure of the reference that would yield nothing more than predicable results, and that it would be desirable to do so because a vertical power MOSFET using a silicon carbide substrate could achieve improved capabilities such as the capability to operate at higher temperatures, higher device densities, higher speeds, or higher power levels, as compared to some other semiconductor materials.

Similarly, one or more of the above referenced references (addressed in Exhibits 112-A1 through 112-An and Exhibits 112-B1 through 112-Bn) would be obvious to combine with one or more of Das, Ueno-3, Glass, Peters, Baliga3, Ghezzo, Rexer, Lidow, Korman, Baliga2, Kerwin, Watkins, Peters, Suvorov, Sze, Neudeck, Bhatanagar, SiC Power-Switching, Shenoy, Xiao,

Shanfield, Kern, Wolf, Van Zant, Murarka, Grant, Baliga, Coen, Casady, Casady2, Vathulya, Ryu-3, Ryu-4, Ryu-5, Ryu-6, Ryu-7 and applicants' admissions and admitted prior art in the '112 Patent (addressed in Exhibit 112-X). Each of these references addressed in Exhibit 112-X are reasonably pertinent to particular problems sought to be solved by the inventor in the '112 Patent. Specifically, each of these references are directed to various topics relevant to the issues in the '112 Patent including the application of MOSFET structures in various semiconductor substrate materials including silicon carbide substrate material and the semiconductor characteristics that motivate the use thereof, the known ability of known DMOSFET structures to be translated into silicon carbide, structures of MOSFET devices including insulating layers under and over the gates and conductive layers over the gates, configuration of sources and the source electrode with respect to MOSFET gates and insulating layers over gates, the known practice of having the insulating layer / gate overlap the source when the gate is formed by a separate masking step, the use of various materials including insulating layers formed by thermal oxidation of silicon and deposited dielectrics including BPSG as insulating layers, deposited metal step coverage, and the structure and layers of semiconductor devices including insulating layers and the types and compositions of insulating materials. It would have been obvious to one of skill in the art that these more specific details about the application of MOSFET structures in various semiconductor substrate materials including silicon carbide substrate material and the semiconductor characteristics that motivate the use thereof, the known ability of known DMOSFET structures to be translated into silicon carbide, structures of MOSFET devices including insulating layers under and over the gates and conductive layers over the gates, configuration of sources and the source electrode with respect to MOSFET gates and insulating layers over gates, the known practice of having the insulating layer / gate overlap the source

when the gate is formed by a separate masking step, the use of various materials including insulating layers formed by thermal oxidation of silicon and deposited dielectrics including BPSG as insulating layers, deposited metal step coverage, and the structure and layers of semiconductor devices including insulating layers and the types and compositions of insulating materials are each known techniques and structures that could be combined in an overall vertical MOSFET structure that would yield nothing more than predicable results and that it would be desirable to do so because the application of MOSFET structures in various semiconductor substrate materials including silicon carbide substrate material and the semiconductor characteristics that motivate the use thereof, the known ability of known DMOSFET structures to be translated into silicon carbide, structures of MOSFET devices including insulating layers under and over the gates and conductive layers over the gates, configuration of sources and the source electrode with respect to MOSFET gates and insulating layers over gates, the known practice of having the insulating layer / gate overlap the source when the gate is formed by a separate masking step, the use of various materials including insulating layers formed by thermal oxidation of silicon and deposited dielectrics including BPSG as insulating layers, deposited metal step coverage, and the structure and layers of semiconductor devices including insulating layers and the types and compositions of insulating materials all relate to known structures and structural elements in semiconductors and MOSFETs, and a person of skill in the art would find it desirable in a vertical MOSFET design to include known structures to provide a vertical MOSFET in silicon carbide to achieve a device with improved capabilities such as the capability to operate at higher temperatures, higher device densities, higher speeds, or higher power levels, as compared to other semiconductor materials while also having greater manufacturing alignment tolerance.

More specifically, as one example, a person of skill in the art would find the Asserted Claims of the '112 Patent obvious over Ueno and/or would have found it obvious to combine references such as Ueno and Lidow to achieve a structure like that of the '112 Patent. Ueno relates to SiC vertical power MOSFETs. *See e.g.*, Ueno at 1:7–14, 4:44–50, Figure. 1. Ueno discloses at wafer on which a drift layer is grown on an "n+ drain layer or substrate 41a." *Id. at* 8:1–13, 8:54–55; Figure 1. Ueno also discloses that "a p base region 42 is formed in a surface layer of the n drift layer 41b, and an n+ source region 43 is formed within the p base region 42." *Id*., 8:2–4. Figure 1 of Ueno shows two source regions 43. Gates are formed—by patterning a polysilicon film "to provide the gate electrode layer[s] 46"—on gate oxide film 45 over the surface of the n drift layer 41b. *Id*., 8:6–10, 10:42–44, Figures 3c and 3d. A source electrode 47 is formed to be in contact with the n+ source regions 43. *Id.*, 8:10–11. An interlayer insulating film 49, in the form of a silicon oxide film, insulates each gate from the source electrode 47. *Id*., 8:13–16. The interlayer insulating film 49 is grown by subjecting the gates to thermal oxidation. *Id*., 10:42–47, Figures 3d–3f. Ueno discloses that "[t]he thickness of the gate oxide film [45] is 50 nm, . . . while the thickness of the interlayer insulating film 49 is 2 μm." *Id*., 8:29–32. As such, renders obvious each of the asserted claims of the '112 Patent. However, to the extent it is alleged that any limitation of any claim is not clearly disclosed, a person of skill in the art would have found it obvious to combine Ueno and Lidow. Lidow discloses a power MOSFET and specifically discloses N+ type source regions 26, polysilicon gates 40, 41, 42, oxide layer 30, silicon dioxide coating sections 45, 46, 47, and source electrode 50. Lidow at 5:13 ("N+ regions 26), 5:30 ("N+ type source rings 50), 5:37 ("polysilicon sections 40, 41 and 42"), 5:57 ("gate 40"), 5:23–26 ("an oxide layer . . . shown as the insulation layer 30"), 5:39–41 ("A silicon dioxide coating is then deposited atop the polysilicon grid 40 shown as coating sections 45, 46

and 47 . . ."), 5:44–46 ("the source electrode is shown as conductive coating 50 which may be of any desired material, such as aluminum"). Lidow discloses that the source electrode 50 is a conductor that extends over and between the silicon dioxide coating sections 45, 46, 47 and the polysilicon gates 40, 41, 42 and is in electrical contact with the N+ type source regions 26. Lidow at 5:58–59 ("the source region 26, which is connected to the conductor 50"). Lidow also discloses that the source electrode 50 is "deposited over the entire upper surface of the wafer." *Id*., 5:42–44. Lidow likewise illustrates in a plan view of the MOSFET device in Figure 1 where the source electrode 50 covers substantially the entire upper surface of the MOSFET device, except for a portion where a "gate connection pad 91 is electrically connected to a plurality of extending fingers 92, 93, 94 and 95 which . . . make electrical connection to the polysilicon gate . . ." and a portion thus provides access to the polysilicon gate. *See id*., 3:21–23, 6:14–19, 6:32–36; *see also id*., Figure 2.

A person of skill in the art would have been motivated to form Ueno's MOSFET according to and informed by Lidow's teachings such that Ueno's source electrode 47 extends over substantially its entire MOSFET structure except for at least one gate contact access portion, consistent with Ueno's disclosure that a "gate electrode" (i.e., "gate contact access point") is provided in its structure when the source electrode 47 is deposited and patterned. Ueno at 10:61–64 ("After forming the contact hole, an aluminum alloy film is deposited, and patterned, as shown in FIG.3(f), so as to provide the source electrode 47 and gate electrode (not illustrated)."). Ueno and Lidow are from the same field of endeavor. *See, e.g., Medtronic, Inc. v. Cardiac Pacemakers, Inc*., 721 F.2d 1563, 1574–75 (Fed. Cir. 1983); M.P.E.P. § 2141. Both references are directed to power MOSFETs. Ueno discloses "a method for manufacturing silicon carbide vertical MOS semiconductor devices having high breakdown voltage." Ueno at 4:45–46.

Lidow discloses "a novel configuration for the central high conductivity region disposed beneath the gate oxide of a high power MOSFET." Lidow at 1:23–25. Thus, both references are directed to power MOSFETs and aim at improving their characteristics. Ueno discloses a MOSFET in silicon-carbide and Lidow a MOSFET in silicon, but a person of skill in the art would know that the same structures can be implemented in both substrate material types. Indeed, Baliga teaches that conventional power MOSFETs, including silicon MOSFETs, "can be readily translated into silicon carbide using known manufacturing techniques." *See* Baliga at 4:22–38. Moreover, Ueno's MOSFET and Lidow's MOSFET share the same relevant semiconductor structure and features, as can be seen by the side-by-side comparison of Ueno Figure 1 with Lidow Figure 5. Accordingly, a person of skill in the art would have understood that the teachings of Lidow were directly applicable to Ueno's MOSFET in silicon carbide. To the extent Purdue argues that it is not implied, inherent or obvious in Ueno, implementing Ueno's source electrode 47 such that it extends over substantially Ueno's entire MOSFET structure except for Ueno's disclosed, but not illustrated, "gate electrode" in the manner such as that shown by Lidow would have yielded expected, predictable results. Ueno discloses its source electrode 47 extending over and between interlayer insulating film 49 and gates. *See* Ueno at Figure 1. Ueno also explains that a "gate electrode" is provided in its structure when the source electrode 47 is deposited and patterned. *Id.* at 10:61–64; *see also*, id., 1:40–42, 57–59 (explaining in a "unit cell of typical Si vertical MOSFET that has been generally used as a power semiconductor device" that a "gate electrode made of metal is held in contact with the gate electrode layer 16 at a portion that is not illustrated in the figure."). A person of skill in the art would also have had a reasonable expectation of success. The combination of Ueno and Lidow represents a straight-forward implementation of steps of the well-understood semiconductor fabrication processes to implement the shape and

location of the structures, which a person of skill in the art would have been familiar with and been able to implement. The reasons a person of skill in the art would have expected success parallel those that provide motivation for this combination—including because both Ueno and Lidow are directed to vertical power MOSFETs. See Ueno at 4:45–46, Figure 1; Lidow at 1:23–25, Figures 1–5. A person of skill in the art would have had a reasonable expectation of success in implementing Ueno's MOSFET electrodes per the teachings of Lidow. Indeed, Ueno did not provide details of how to implement its gate electrode because such structures were well known as illustrated by Lidow.

Further, to the extent Purdue argues that any claim limitation of the '112 Patent is not disclosed and rendered obvious by Ueno alone or the combination of Ueno and Lidow, it would be obvious to combine Ueno and Lidow with one or more of the other prior art references listed herein, including Das, Ueno-3, Glass, Peters, Baliga3, Ghezzo, Rexer, Lidow, Korman, Baliga2, Kerwin, Watkins, Peters, Suvorov, Sze, Neudeck, Bhatanagar, SiC Power-Switching, Shenoy, Xiao, Shanfield, Kern, Wolf, Van Zant, Murarka, Grant, Baliga, Coen, Casady, Casady2, Vathulya, Ryu-3, Ryu-4, Ryu-5, Ryu-6, Ryu-7, and applicants' admissions and admitted prior art in the '112 Patent (addressed in Exhibit 112-X). Each of these references addressed in Exhibit 112-X are reasonably pertinent to particular problems sought to be solved by the inventor in the '112 Patent. Each of these references are directed to various topics relevant to the issues in the '112 Patent including the application of MOSFET structures in various semiconductor substrate materials including silicon carbide substrate material and the semiconductor characteristics that motivate the use thereof, the known ability of known DMOSFET structures to be translated into silicon carbide, structures of MOSFET devices including insulating layers under and over the gates and conductive layers over the gates, configuration of sources and the source electrode

with respect to MOSFET gates and insulating layers over gates, the known practice of having the insulating layer / gate overlap the source when the gate is formed by a separate masking step, the use of various materials including insulating layers formed by thermal oxidation of silicon and deposited dielectrics including BPSG as insulating layers, deposited metal step coverage, and the structure and layers of semiconductor devices including insulating layers and the types and compositions of insulating materials.

Similarly, as a second example, a person of skill in the art would find it obvious to combine the MDmesh Products (charted in Exhibits 112-B6 and 112-B6(a) through 112-B6(h)), the PP26 products (charted in Exhibit 112-B7), or the EZ67 Products (charted in Exhibit 112-B8), each of which disclose a vertical MOSFET with a substrate and drift layer, gates having both tops and sides covered with an insulating material, another insulating layer under the gate between the gate and the substrate, and a metal layer covering gates and areas between the gates, and prior art such as Baliga or Ryu that teach that such MOSFET device structures can be and would be obvious to be implemented in silicon carbide by adapting some of the manufacturing techniques while utilizing the same configuration. Baliga teaches that conventional power MOSFETs, including silicon MOSFETs, "can be readily translated into silicon carbide using known manufacturing techniques." *See* Baliga at 4:22–38. Ryu likewise discloses a silicon carbide MOSFET. *See* description of Ryu above and Ryu generally. Indeed, a person of skill in the art would know that the same structures can be implemented in both substrate material types as evidenced by references such as Hatade ("Furthermore, although a silicon substrate is typically used for the semiconductor substrate 1, the present invention can also be executed for a semiconductor substrate using other semiconductor materials." Hatade at 11:23-26); Sze ("MOSFETs have been made with various semiconductors such as Ge,12 Si, and GaAs,13." Sze

at 432.); Uneo-3 ("SiC is expected to be used in a wide range of applications in the future." Ueno-3 at 1:33-53); Neudeck ("Given the extreme usefulness and success of MOSFET-based electronics in silicon, it is naturally desirable to implement high-performance inversion channel MOSFETs in SiC." Neudeck at 285-6); Bhatanagar ("From the previous discussion, it is possible to conclude that the development of SiC Schottky rectifiers and power MOSFET's will provide devices which can deliver larger currents at very fast switching speed in power circuits with high breakdown voltages." Bhatanagar at 653-4); Glass ("One material for which great semiconductor potential has long been recognized is silicon carbide (SiC). Silicon carbide has well known advantageous semiconductor characteristics: a wide bandgap, a high thermal conductivity, a high melting point, a high electric field breakdown strength, a low dielectric constant, and a high saturated electron drift velocity. Taken together, these qualities potentially give electronic devices formed from silicon carbide the capability to operate at higher temperatures, higher device densities, higher speeds, higher power levels, and even under higher radiation densities, as compared to other semiconductor materials." Glass at 2:5-21); Peters ("A cell structure of the so called triple implanted vertical MOSFET [in SiC] is sketched in Fig. 1. One can easily imagine that structure, process and electrode materials are designed as close as possible to the well known silicon DMOS." Peters at 769); and Ghezzo ("An object of one embodiment of the invention is to provide a silicon carbide high voltage MOS power device having structural characteristics of a DMOS device. Because SiC has a higher critical electric field than silicon, the specific on-resistance of a SiC DMOS is expected to be significantly lower than that of a silicon DMOS with the same high voltage rating. A method of implementing vertical power SiC transistor is to replace the conventional double-diffusion with an edge-shifted double ion implantation sequence to overcome the problem of very small dopant diffusivity in SiC. The

channel is formed by successive ion implantation of an acceptor atom (such as boron or aluminum) and a donor atom (such as nitrogen or phosphorous) to form the base and source regions, respectively. These implants are edge-shifted and have different depths with junctions formed by using spacers which add a margin around an initial mask edge with the second implantation region being shifted from the first region." Ghezzo 1:50–67.), among others.

As explained above, Ueno and Lidow is one particular combination that a person of skill in the art would find obvious to make to reach the configuration of the '112 patent. The MDmesh Products, the PP26 Products, or the EZ67 Products and Baliga (and similar art that teach the implementation of MOSFETs in silicon carbide) are other specific combinations that a person of skill in the art would find obvious to make to reach the configuration of the '112 patent.

For the same reasons as explained above for the example combination of Ueno and Lidow, a person of skill in the art would find it obvious to combine any one or more of Nakamura, Tanimoto, Tanimoto2, Ueno, Ueno2, Kataoka, Kosugi, Hefner, Kojima, Miura, Peters, Agarwal, Endo, Tanimoto3 and Agarwal2 (addressed in Exhibits 112-A1 through 112-An), which each address vertical MOSFETs expressly disclosed as being formed in a silicon carbide substrate, with any one or more of Tonnel, Magri', Rexer, Belverde, Hatade, the MDmesh Products, the PP26 Products, and the EZ67 Products (addressed in Exhibits 112-B1 through 112-Bn), which each disclose vertical MOSFET devices that expressly describe vertical MOSFETs formed in a silicon substrate having various types and thickness of insulating layers and source electrode configurations. Such combinations represent straight-forward implementation of steps of the well-understood semiconductor fabrication processes to implement the shape and location of the structures, which a person of skill in the art would have

been familiar with and been able to implement. Further, to the extent Purdue argues that any claim limitation of the '112 Patent is not disclosed and rendered obvious by the above combinations, it would be obvious for the reasons explained above to combine the above combinations with one or more of Das, Ueno-3, Glass, Peters, Baliga3, Ghezzo, Rexer, Lidow, Korman, Baliga2, Kerwin, Watkins, Peters, Suvorov, Sze, Neudeck, Bhatanagar, SiC Power-Switching, Shenoy, Xiao, Shanfield, Kern, Wolf, Van Zant, Murarka, Grant, Baliga, Coen, Casady, Casady2, Vathulya, Ryu-3, Ryu-4, Ryu-5, Ryu-6, Ryu-7, and applicants' admissions and admitted prior art in the '112 Patent (addressed in Exhibit 112-X) to make obvious the configuration of the '112 Patent.

Similarly, for the same reasons as explained above for the example combination of the MDmesh Products, the PP26 Products, or the EZ67 Products and Baliga (and similar art that teach the implementation of MOSFETs in silicon carbide), a person of skill in the art would find it obvious to combine any one or more of Tonnel, Magri', Rexer, Belverde, Hatade, the MDmesh Products, the MDmesh Products, the PP26 Products, and the EZ67 Products (addressed in Exhibits 112-B1 through 112-Bn) with Baliga (or similar art that teach the implementation of MOSFETs in silicon carbide). Such combinations represent straight-forward implementation of steps of the well-understood semiconductor fabrication processes to implement the shape and location of the structures, which a person of skill in the art would have been familiar with and been able to implement. Further, to the extent Purdue argues that any claim limitation of the '112 Patent is not disclosed and rendered obvious by the above combinations, it would be obvious for the reasons explained above to combine the above combinations with one or more of Hatade, Das, Ueno-3, Glass, Peters, Baliga3, Ghezzo, Rexer, Lidow, Korman, Baliga2, Kerwin, Watkins, Peters, Suvorov, Sze, Neudeck, Bhatanagar, SiC Power-Switching, Shenoy, Xiao,

Shanfield, Kern, Wolf, Van Zant, Murarka, Grant, Baliga, Coen, Casady, Casady2, Vathulya, Ryu-3, Ryu-4, Ryu-5, Ryu-6, Ryu-7, and applicants' admissions and admitted prior art in the '112 Patent (addressed in Exhibit 112-X) to make obvious the configuration of the '112 Patent.

Accordingly, one of ordinary skill in the art would have been motivated to combine any of the references cited in Exhibits 112-A1 through 112-An and Exhibits 112-B1 through 112-Bn either with the knowledge of one skilled in the art or with other references in Exhibit 112-X in addition to such knowledge, and would have further recognized that combinations of these references would have improved similar systems and methods in the same way and address any problems that the '112 Patent sought to solve.

C. Invalidity Under 35 U.S.C. § 112

The following terms of the Asserted Patents are deficient under one or more paragraphs of 35 U.S.C. §112:

- '633 Patent claim 9 – "less than about three micrometers"
- '112 Patent claim 1 – "a second, thicker oxide layer"
- '112 Patent claim 6 – "a gate oxide layer"

Defendants do not yet know what claim terms Purdue will contend require construction, what constructions Purdue may propose or what evidence Purdue may contend supports a claim term or a proposed construction. Accordingly, Defendants reserve the right during claim construction to contend that claim terms are invalid under one or more paragraphs of 35 U.S.C. § 112 in response information or arguments raised during claim construction.

III. ADDITIONAL PRIOR ART

In addition to the prior art references charted, Defendants may use other prior art, contemporaneous art or general information to show the state of the art and what a person of skill in the relevant art would know.

Defendants also incorporate here by reference all prior art cited in the Asserted Patents and all prior art cited in the prosecution histories of the Asserted Patents, reexaminations, inter partes or covered business method patent review proceedings, and any foreign counterparts.

IV. DOCUMENT PRODUCTION AND INSPECTION

Also in accordance with the Court's Scheduling Order [ECF 45], Defendants are producing technical documents regarding the accused products based on what Plaintiff has identified in its Infringement Contentions served on such Defendants on October 25, 2021. In addition, Defendants are making certain design files and documents available for inspection pursuant to Defendants' proposed Protective Order. Finally, Defendants are making ST Prior Art Products available for inspection. Such inspections of the design files and ST Prior Art products are available in the Dallas office of Holland & Knight at 1722 Routh Street, Suite 1500, Dallas, Texas 75201.

V. CONCLUSION

Defendants reserve the right to continue to supplement their Preliminary Invalidity Contentions as Defendants obtain additional documentation and/or other information during their continuing investigations and during the course of discovery.

Dated: January 14, 2022

Respectfully submitted:

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CERTIFICATE OF SERVICE

I hereby certify that on January 14, 2022, I caused the foregoing to be electronically served upon all counsel of record.

/s/ Justin S. Cohen
Justin S. Cohen