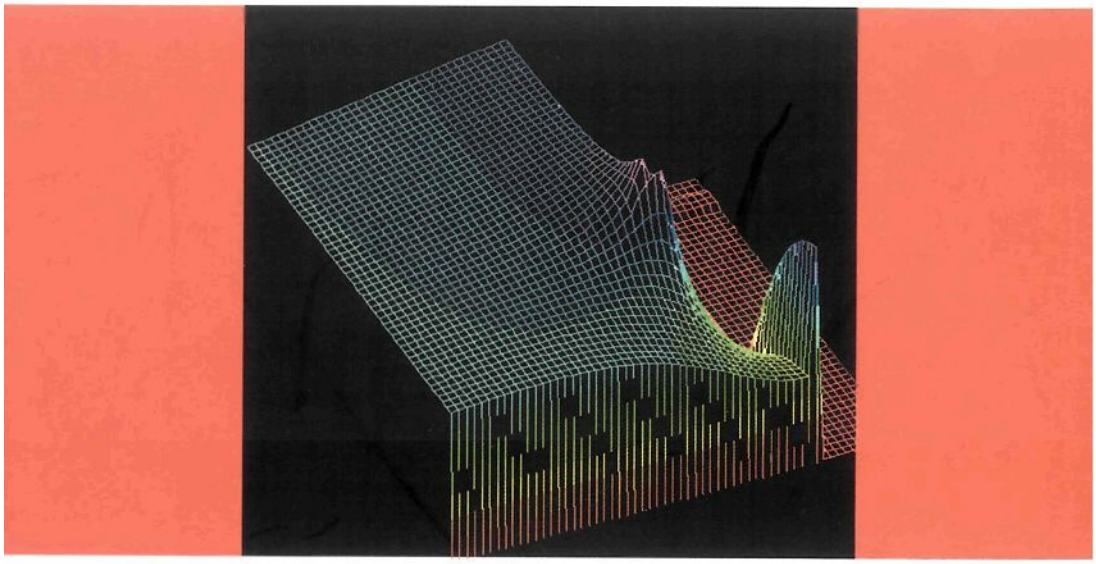

Silicon Carbide Power Devices

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Dedication

The author would like to dedicate this book to his family – his wife, Pratima and his sons, Avinash and Vinay - for their support of his commitment to create a world-wide effort on the development and commercialization of power devices based upon wide band-gap semiconductors.

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Preface

Power semiconductor devices are a key component of all power electronic systems. It is estimated that at least 50 percent of the electricity used in the world is controlled by power devices. With the wide spread use of electronics in the consumer, industrial, medical, and transportation sectors, power devices have a major impact on the economy because they determine the cost and efficiency of systems. After the initial replacement of vacuum tubes by solid state devices in the 1950s, semiconductor power devices have taken a dominant role with silicon serving as the base material.

Bipolar power devices, such as bipolar transistors and thyristors, were first developed in the 1950s. Their power ratings and switching frequency increased with advancements in the understanding of the operating physics and availability of more advanced lithography capability. The physics underlying the current conduction and switching speed of these devices has been described in several textbooks[1,2]. Since the thyristors were developed for high voltage DC transmission and electric locomotive drives, the emphasis was on increasing the voltage rating and current handling capability. The ability to use neutron transmutation doping to produce high resistivity n-type silicon with improved uniformity across large diameter wafers enabled increasing the blocking voltage of thyristors to over 5000 volts while being able to handle over 2000 amperes of current in a single device. Meanwhile, bipolar power transistors were developed with the goal of increasing the switching frequency in medium power systems. Unfortunately, the current gain of bipolar transistors becomes low when it is designed for high voltage operation at high current density. The popular solution to this problem, using the Darlington configuration, had the disadvantage of increasing the on-state voltage drop resulting in an increase in the power dissipation. In addition to the large control currents required for bipolar transistors, they suffered from second breakdown failure modes. These

issues produced a cumbersome design with snubber networks, which raised the cost and degraded the efficiency of the power control system.

In the 1970s, the power MOSFET product was first introduced by International Rectifier Corporation. Although initially hailed as a replacement for all bipolar power devices due to its high input impedance and fast switching speed, the power MOSFET has successfully cornered the market for low voltage (< 100 V) and high switching speed (> 100 kHz) applications but failed to make serious inroads in the high voltage arena. This is because the on-state resistance of power MOSFETs increases very rapidly with increase in the breakdown voltage. The resulting high conduction losses, even when using larger more expensive die, degrade the overall system efficiency.

In recognition of these issues, I proposed two new thrusts in 1979 for the power device field. The first was based upon the merging of MOS and bipolar device physics to create a new category of power devices[3]. My most successful innovation among MOS-Bipolar devices has been the *Insulated Gate Bipolar Transistor (IGBT).* Soon after commercial introduction in the early 1980s, the IGBT was adopted for all medium power electronics applications. Today, it is manufactured by more than a dozen companies around the world for consumer, industrial, medical, and other applications that benefit society. The triumph of the IGBT is associated with its huge power gain, high input impedance, wide safe operating area, and a switching speed that can be tailored for applications depending upon their operating frequency.

The second approach that I suggested in the early 1980s for enhancing the performance of power devices was to replace silicon with wide band gap semiconductors. The basis for this approach was an equation that I derived relating the on-resistance of the drift region in unipolar power devices to the basic properties of the semiconductor material. This equation has since been referred to as *Baliga's Figure of Merit (BFOM).* In addition to the expected reduction in the on-state resistance with higher carrier mobility, the equation predicts a reduction in on-resistance as the inverse of the cube of the breakdown electric field strength of the semiconductor material.

In the 1970s, there was a dearth of knowledge of the impact ionization coefficients of semiconductors. Consequently, an association of the breakdown electric field strength was made with the energy band gap of the semiconductor[4]. This led to the conclusion that wide band gap semiconductors offer the opportunity to greatly reduce the on-state resistance of the drift region in power devices. With a sufficiently low

on-state resistance, it became possible to postulate that unipolar power devices could be constructed from wide band gap semiconductors with lower on-state voltage drop than bipolar devices made out of silicon. Since unipolar devices exhibit much faster switching speed than bipolar devices because of the absence of minority carrier stored charge, wide band gap based power devices offered a much superior alternative to silicon bipolar devices for medium and high power applications. Device structures that were particularly suitable for development were identified as Schottky rectifiers to replace silicon P-i-N rectifiers, and power Field Effect Transistors to replace the bipolar transistors and thyristors prevalent in the 1970s.

The first attempt to develop wide band gap based power devices was undertaken at the General Electric Corporate Research and Development Center, Schenectady, NY, under my direction. The goal was to leverage a 13-fold reduction in specific on-resistance for the drift region predicted by the BFOM for Gallium Arsenide. A team of 10 scientists was assembled to tackle the difficult problems of the growth of high resistivity epitaxial layers, the fabrication of low resistivity ohmic contacts, low leakage Schottky contacts, and the passivation of the GaAs surface. This led to an enhanced understanding of the breakdown strength[5] for GaAs and the successful fabrication of high performance Schottky rectifiers[6] and MESFETs[7]. Experimental verification of the basic thesis of the analysis represented by BFOM was therefore demonstrated during this period. Commercial GaAs based Schottky rectifier products were subsequently introduced in the market by several companies.

In the later half of the 1980s, the technology for the growth of silicon carbide was developed with the culmination of commercial availability of wafers from CREE Research Corporation. Although data on the impact ionization coefficients of SiC was not available, early reports on the breakdown voltage of diodes enabled estimation of the breakdown electric field strength. Using these numbers in the BFOM predicted an impressive 100-200 fold reduction in the specific on-resistance of the drift region for SiC based unipolar devices. In 1988, I joined North Carolina State University and subsequently founded the *Power Semiconductor Research Center (PSRC)* - an industrial consortium – with the objective of exploring ideas to enhance power device performance. Within the first year of the inception of the program, SiC Schottky barrier rectifiers with breakdown voltage of 400 volts were successfully fabricated with on-state voltage drop of about 1

volt and no reverse recovery transients[8]. By improving the edge termination of these diodes, the breakdown voltage was found to increase to 1000 volts. With the availability of epitaxial SiC material with lower doping concentrations, SiC Schottky rectifiers with breakdown voltages over 2.5 kV have been fabricated at PSRC[9]. These results have motivated many other groups around the world to develop SiC based power rectifiers. In this regard, it has been my privilege to assist in the establishment of national programs to fund research on silicon carbide technology in the United States, Japan, and Switzerland-Sweden. Meanwhile, accurate measurements of the impact ionization coefficients for 6H-SiC and 4H-SiC in defect free regions were performed at PSRC using an electron beam excitation method[10]. Using these coefficients, a BFOM of over 1000 is predicted for SiC providing even greater motivation to develop power devices from this material.

Although the fabrication of high performance, high voltage Schottky rectifiers has been relatively straight-forward, the development of a suitable silicon carbide MOSFET structure has been more problematic. The existing silicon power D-MOSFET and U-MOSFET structures do not directly translate to suitable structures in silicon carbide. The interface between SiC and silicon dioxide, as a gate dielectric, needed extensive investigation due to the large density of traps that prevent the formation of high conductivity inversion layers. Even after overcoming this hurdle, the much higher electric field in the silicon dioxide when compared with silicon devices, resulting from the much larger electric field in the underlying SiC, leads to reliability problems. Fortunately, a structural innovation, called the ACCUFET, to overcome both problems was proposed and demonstrated at PSRC[11]. In this structure, a buried P^+ region is used to shield the gate region from the high electric field within the SiC drift region. This concept is applicable to devices that utilize either accumulation channels or inversion channels. Devices with low specific on-resistance have been demonstrated at PSRC using both 6H-SiC and 4H-SiC with epitaxial material capable of supporting over 5000 volts[12]. This device structure has been subsequently emulated by several groups around the world.

Although many papers have been published on silicon carbide device structures and process technology, no comprehensive book written by a single author is available that provides a unified treatment of silicon carbide power device structures. This book has been prepared to fill this gap. The emphasis in the book is on the physics of operation of the devices elucidated by extensive two-dimensional numerical analysis.

The simulations were done for 4H-SiC, rather than 6H-SiC, because its larger breakdown strength results in superior device performance. This analysis provides general guidelines for understanding the design and operation of the various device structures. For designs that may be pertinent to specific applications, the reader should refer to the papers published in the literature, the theses of my M.S. and Ph.D. students, as well as the work reported by other research groups. Comparison with silicon devices is provided to enable the reader to understand the benefits of silicon carbide devices.

In the introduction chapter, the desired characteristics of power devices are described with a broad introduction to potential applications. The second chapter provides the properties of silicon carbide that have relevance to the analysis and performance of power device structures. Issues pertinent to the fabrication of silicon carbide devices are reviewed here because the structures analyzed in the book have been constructed with these process limitations in mind. The third chapter discusses breakdown voltage, which is the most unique distinguishing characteristic for power devices, together with edge termination structures. This analysis is pertinent to all the device structures discussed in subsequent chapters of the book.

The fourth chapter provides a brief analysis of P-i-N rectifiers followed by a detailed analysis of the Schottky rectifier structure in chapter five. The sixth chapter introduces the concept and explains the benefits of shielding the Schottky contact. This approach is essential for mitigating the generation of high leakage current in silicon carbide Schottky rectifiers arising from Schottky barrier lowering and tunneling currents. The next chapter describes power JFET and MESFET structures with planar and trench gate regions. These normally-on structures can be used to construct the *Baliga-Pair* circuit[13], described in chapter eight, which has been shown to be ideally suitable for motor control applications. This represents a near term solution to taking advantage of the low specific on-resistance of the silicon carbide drift region while awaiting resolution of reliability issues with the gate oxide in silicon carbide power MOSFET structures.

Chapter nine provides a description of silicon carbide power MOSFET structures with emphasis on problems associated with simply replicating structures originally developed in silicon technology. Innovative approaches to prevent high electric field in the gate oxide of silicon carbide power MOSFETs are then discussed in chapter ten. In this chapter, accumulation-mode structures are shown to provide the

advantages of larger channel mobility and lower threshold voltage leading to a reduction in the specific on-resistance. In chapter eleven, issues with adopting the silicon UMOSFET structure to silicon carbide are enunciated followed by analysis of solutions to these problems in chapter twelve. Once again, methods for shielding the gate oxide are shown to enable reduction of the electric field in the gate oxide to acceptable levels. The shielding is also demonstrates to ameliorate the base reach-through problem allowing a reduction of the base width and hence the channel resistance contribution.

The application of the charge-coupling concept to silicon carbide is explored in chapter thirteen to reduce the resistance of the drift region. This approach is applicable to very high voltage structures with blocking voltage capability exceeding 3000 volts. In chapter fourteen, the operation of the integral diode within the silicon carbide power MOSFET structures is analyzed for utilization as a fly-back rectifier in motor control applications. A unique mode of current conduction in the silicon carbide power MOSFET in the third quadrant of operation is identified here which allows for a reduction of the on-state voltage drop of the integral diode.

Although the emphasis in this book has been on discrete vertical silicon carbide structures, for the sake of completeness, the fifteenth chapter describes high voltage lateral silicon carbide structures that are suitable for integration with CMOS circuits. In the concluding sixteenth chapter, the performance of silicon carbide devices is compared with that of silicon devices using a typical motor control application as an example to provide the reader with a perspective on the benefits of using silicon carbide devices. From an applications perspective, it is demonstrated that the replacement of the silicon P-i-N rectifier with the silicon carbide JBS rectifier provides a significant reduction in the power losses for the system as well as the stress experienced by the silicon IGBT. This approach is already becoming a commercially viable option due to the availability of silicon carbide Schottky rectifier products from several companies.

Throughout the book, experimental results are included whenever pertinent to each chapter. This provides a historical context and a brief summary of the state of the art for silicon carbide devices. Issues that must be addressed before commercialization of silicon carbide structures becomes viable are pointed out in these sections of the book.

I am hopeful that this book will be used for the teaching of courses on solid state devices and that it will make an essential reference for the power device industry. To facilitate this, analytical solutions are provided throughout the book that can be utilized to understand the underlying physics and model the structures. Comparison of the silicon carbide structures with their silicon counterparts is also included whenever pertinent to the discussion.

Ever since my identification of the benefits of utilizing wide band gap semiconductors for the development of superior power devices twenty-five years ago, it has been my mission to resolve issues that would impede their commercialization. I wish to thank the sponsors of the Power Semiconductor Research Center and the Office of Naval Research for supporting this mission during the last fifteen years. This has been essential to providing the resources required to create many breakthroughs in the silicon carbide technology which I hope will enable commercialization of the technology in the near future. I look forward to observing the benefits accrued to society by adopting the silicon carbide technology for conservation of fossil fuel usage resulting in reduced environmental pollution.

Prof. B. Jayant Baliga
2005

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Contents

Chapter 1

Introduction

The increasing dependence of modern society on electrical appliances for comfort, transportation, and healthcare has motivated great advances in power generation, power distribution and power management technologies. These advancements owe their allegiance to enhancements in the performance of power devices that regulate the flow of electricity. After the displacement of vacuum tubes by solid state devices in the 1950s, the industry relied upon silicon bipolar devices, such as bipolar power transistors and thyristors. Although the ratings of these devices grew rapidly to serve an ever broader system need, their fundamental limitations in terms of the cumbersome control and protection circuitry led to bulky and costly solutions. The advent of MOS technology for digital electronics enabled the creation of a new class of devices in the 1970s for power switching applications as well. These silicon power MOSFETs have found extensive use in high frequency applications with relatively low operating voltages (under 100 volts). The merger of MOS and bipolar physics enabled creation of yet another class of devices in the 1980s. The most successful innovation in this class of devices has been the Insulated Gate Bipolar transistor (IGBT). The high power density, simple interface, and ruggedness of the IGBT have made it the technology of choice for all medium and high power applications with perhaps the exception of high voltage DC transmission systems.

Power devices are required for systems that operate over a broad spectrum of power levels and frequencies. In Fig. 1.1, the applications for power devices are shown as a function of operating frequency. High power systems, such as HVDC power distribution and locomotive drives, requiring the control of megawatts of power operate at relatively low frequencies. As the operating frequency increases, the power ratings decrease for the devices with typical microwave devices handling about 100 watts. All of these applications are served by silicon devices. Thyristors are favored for the low frequency, high power applications,

IGBTs for the medium frequency and power applications, and power MOSFETs for the high frequency applications.

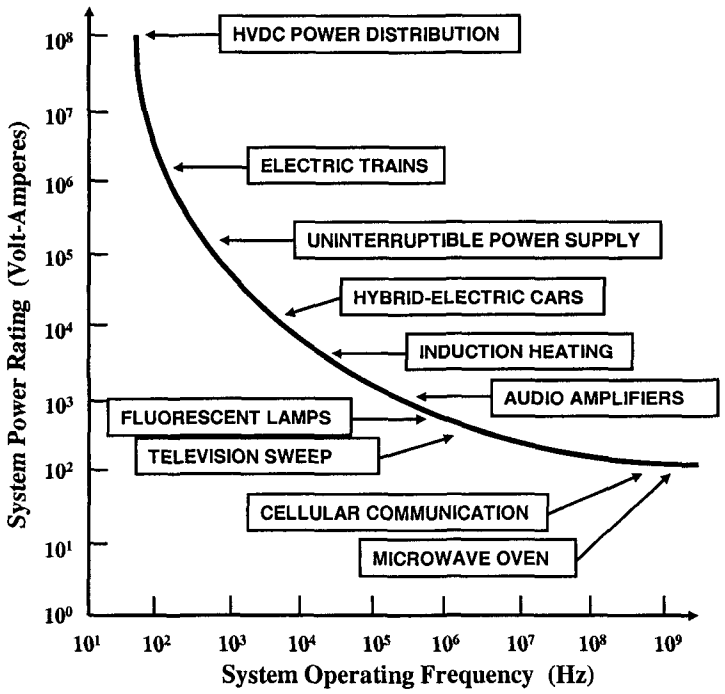

Fig. 1.1 Applications for Power Devices.

Another approach to classification of applications for power devices is in terms of their current and voltage handling requirements as shown in Fig. 1.2. On the high power end of the chart, thyristors are available that can individually handle over 6000 volts and 2000 amperes enabling the control of over 10 megawatts of power by a single monolithic device. These devices are suitable for the HVDC power transmission and locomotive drive (traction) applications. For the broad range of systems that require operating voltages between 300 volts and 3000 volts with significant current handling capability, the IGBT has been found to be the optimum solution. When the current requirements fall below 1 ampere, it is feasible to integrate multiple devices on a single monolithic chip to provide greater functionality for systems such as telecommunications and display drives. However, when the current exceeds a few amperes, it is more cost effective to use discrete power

MOSFETs with appropriate control ICs to serve applications such as automotive electronics and switch mode power supplies.

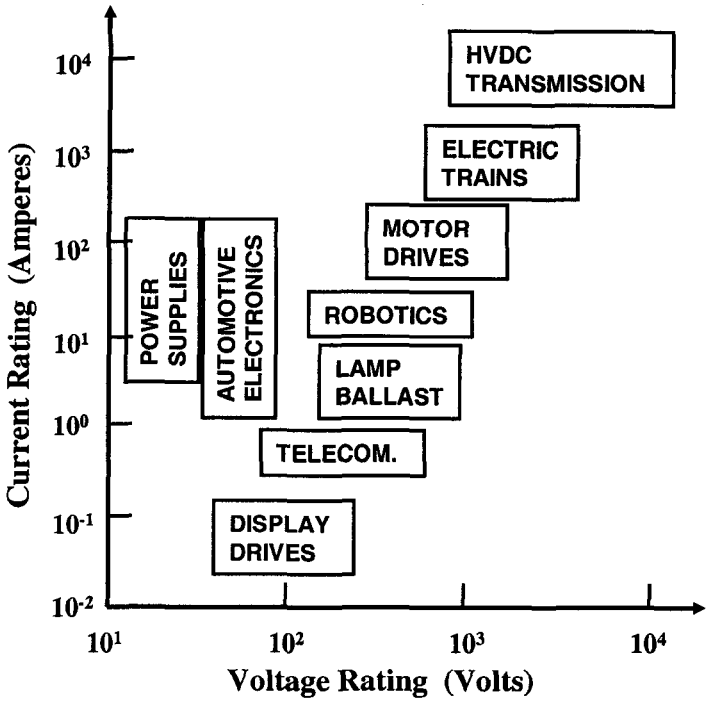

Fig. 1.2 System Ratings for Power Devices.

1.1 Ideal and Typical Power Device Characteristics

Although silicon power devices have served the industry for well over five decades, they cannot be considered to have ideal device characteristics. An ideal power rectifier should exhibit the *i-v* characteristics shown in Fig. 1.3. In the forward conduction mode, the first quadrant of operation the figure, it should be able to carry any amount of current with zero on-state voltage drop. In the reverse blocking mode, the third quadrant of operation in the figure, it should be able to hold off any value of voltage with zero leakage current. Further, the ideal rectifier should be able to switch between the on-state and the off-state with zero switching time. Actual silicon power rectifiers exhibit the *i-v* characteristics illustrated in Fig. 1.4. They have a finite voltage

drop (V_{ON}) when carrying current on the on-state leading to 'conduction' power loss. They also have a finite leakage current (I_{OFF}) when blocking voltage in the off-state creating power loss. In addition, the doping concentration and thickness of the drift region of the silicon device must be carefully chosen with a design target for the breakdown voltage (BV)[1]. The power dissipation in power devices increases when their voltage rating is increased due to an increase in the on-state voltage drop.

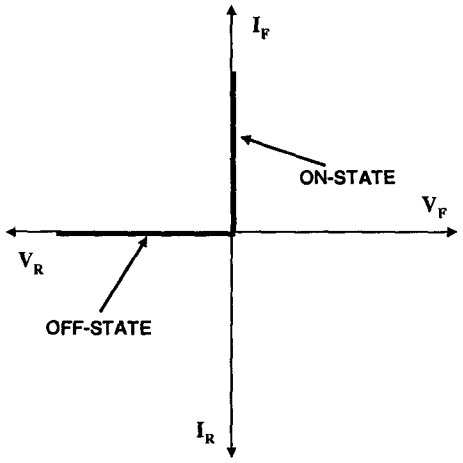

Fig. 1.3 Characteristics of an Ideal Power Rectifier.

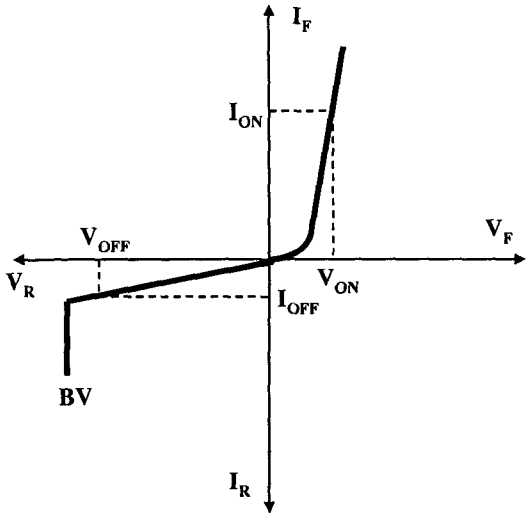

Fig. 1.4 Characteristics of a Typical Power Rectifier.

The *i-v* characteristics of an ideal power switch are illustrated in Fig. 1.5. As in the case of the ideal rectifier, the ideal transistor conducts current in the on-state with zero voltage drop and blocks voltage in the off-state with zero leakage current. In addition, the ideal device can operate with a high current and voltage in the active region with the forward current in this mode controlled by the applied gate bias. The spacing between the characteristics in the active region is uniform for an ideal transistor indicating a gain that is independent of the forward current and voltage.

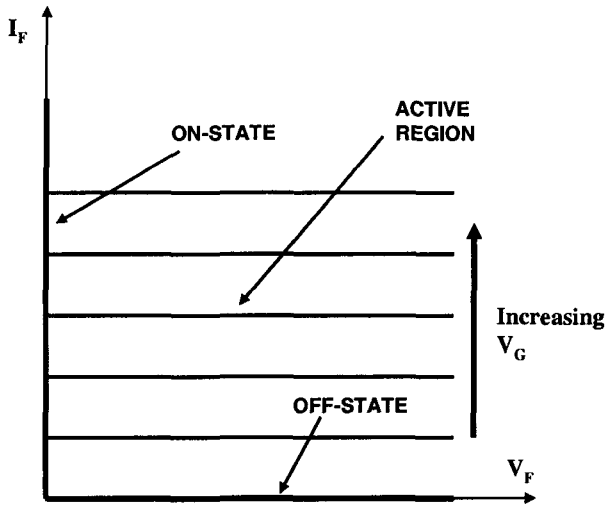

Fig. 1.5 Characteristics of an Ideal Transistor.

The *i-v* characteristics of a typical power switch are illustrated in Fig. 1.6. This device exhibits a finite resistance when carrying current in the on-state as well as a finite leakage current while operating in the off-state (not shown in the figure because its value is much lower than the on-state current levels). The breakdown voltage of a typical transistor is also finite as indicated in the figure with 'BV'. The typical transistor can operate with a high current and voltage in the active region. This current is controlled by the base current for a bipolar transistor while it is determined by a gate voltage for a MOSFET or IGBT (as indicated in the figure). It is preferable to have gate voltage controlled characteristics because the drive circuit can be integrated to reduce its cost. The spacing between the characteristics in the active region is non-uniform for a typical transistor with a square-law behavior for devices operating with

channel pinch-off in the current saturation mode[1]. Recently, devices operating under a new super-linear mode have been proposed and demonstrated for wireless base-station applications[2].

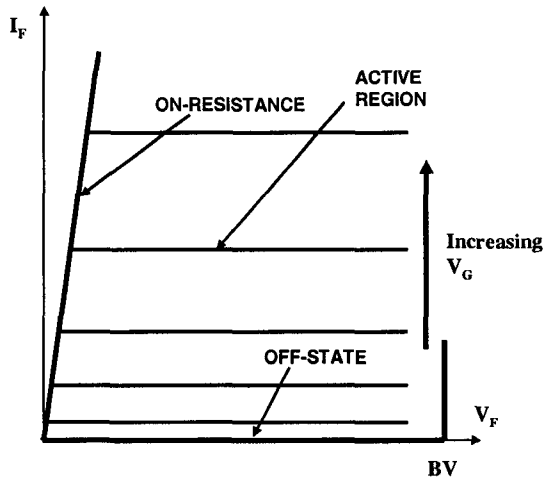

Fig. 1.6 Characteristics of a Typical Transistor.

1.2 Unipolar Power Devices

Bipolar power devices operate with the injection of minority carriers during on-state current flow. These carriers must be removed when the switching the device from the on-state to the off-state. This is accomplished by either charge removal via the gate drive current or via the electron-hole recombination process. These processes introduce significant power losses that degrade the power management efficiency. It is therefore preferable to utilize unipolar current conduction in a power device. The commonly used unipolar power diode structure is the Schottky rectifier that utilizes a metal-semiconductor barrier to produce current rectification. The high voltage Schottky rectifier structure also contains a drift region, as show in Fig. 1.7, which is designed to support the reverse blocking voltage. The resistance of the drift region increases rapidly with increasing blocking voltage capability as discussed later in this chapter. Silicon Schottky rectifiers are commercially available with blocking voltages of up to 100 volts. Beyond this value, the on-state voltage drop of silicon Schottky rectifiers becomes too large for practical

applications[1]. Silicon P-i-N rectifiers are favored for designs with larger breakdown voltages due to their lower on-state voltage drop despite their slower switching properties. As shown later in the book, silicon carbide Schottky rectifiers have much lower drift region resistance enabling design of very high voltage devices with low on-state voltage drop.

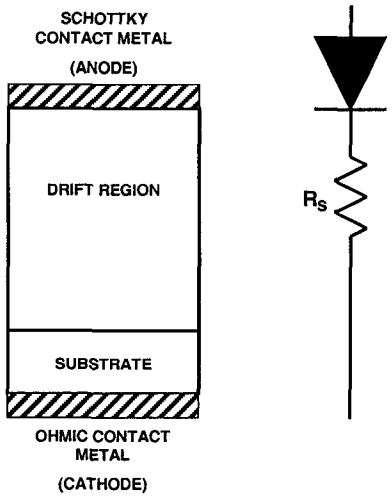

Fig. 1.7 The Power Schottky Rectifier Structure and its Equivalent Circuit.

The most commonly used unipolar power transistor is the silicon power Metal-Oxide-Semiconductor Field-Effect-Transistor or MOSFET. Although other structures, such as JFETs or SITs have been explored[3], they have not been popular for power electronic applications because of their normally-on behavior. The commercially available silicon power MOSFETs are based upon the structures shown in Fig. 1.8. The D-MOSFET was first commercially introduced in the 1970's and contains a 'planar-gate' structure. The P-base region and the N^+ source regions are self-aligned to the edge of the Polysilicon gate electrode by using ion-implantation of boron and phosphorus with their respective drive-in thermal cycles. The n-type channel is defined by the difference in the lateral extension of the junctions under the gate electrode. The device supports positive voltage applied to the drain across the P-base/N-drift region junction. The voltage blocking capability is determined by the doping and thickness of the drift region. Although low voltage (< 100 V) silicon power MOSFET have low on-resistances, the drift region

resistance increases rapidly with increasing blocking voltage limiting the performance of silicon power MOSFETs to below 200 volts. It is common-place to use the Insulated Gate Bipolar Transistors (IGBT) for higher voltage designs.

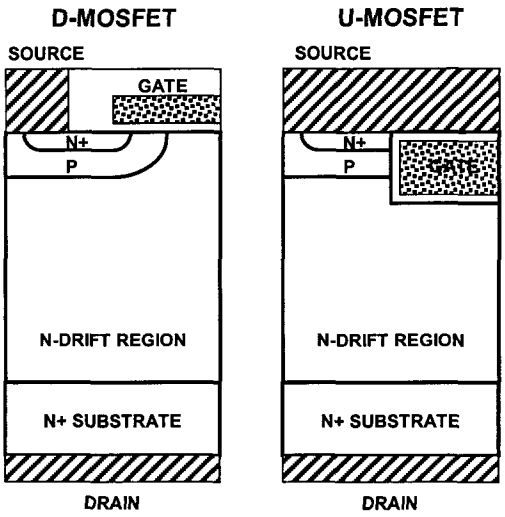

Fig. 1.8 Silicon Power MOSFET Structures.

The silicon U-MOSFET structure became commercially available in the 1990s. It has a gate structure embedded within a trench etched into the silicon surface. The N-type channel is formed on the side-wall of the trench at the surface of the P-base region. The channel length is determined by the difference in vertical extension of the P-base and N^+ source regions as controlled by the ion-implant energies and drive times for the dopants. The silicon U-MOSFET structure was developed to reduce the on-state resistance by elimination of the JFET component within the D-MOSFET structure[1].

1.3 Bipolar Power Devices

The commonly available silicon power bipolar devices are the bipolar transistor and the gate turn-off thyristor or GTO. These devices were originally developed in the 1950's and widely used for power switching applications until the 1970s when the availability of silicon power

MOSFETs and IGBTs supplanted them. The structures of the bipolar transistor and GTO are shown in Fig. 1.9. In both devices, injection of minority carriers into the drift region modulates its conductivity reducing the on-state voltage drop. However, this charge must be subsequently removed during switching resulting in high turn-off power losses. These devices require a large control (base or gate) current which must be implemented with discrete components leading to an expensive bulky system design.

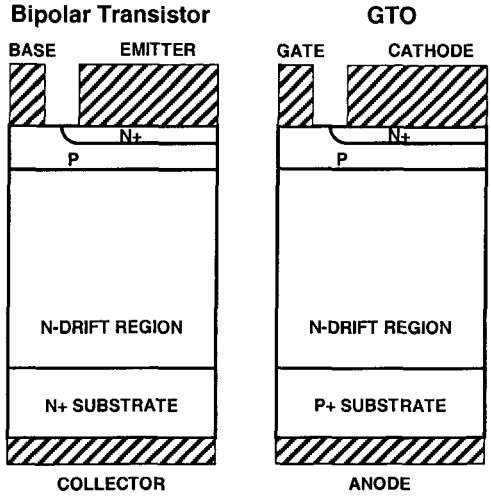

Fig. 1.9 Silicon Bipolar Device Structures.

Several groups have worked on the development of bipolar transistors[4,5,6,7] and GTOs[8,9] using silicon carbide. The large junction potential for silicon carbide results in a relatively high on-state voltage drop for these devices when compared with commercially available silicon devices. For this reason, the focus of this book is on unipolar silicon carbide structures.

1.4 MOS-Bipolar Power Devices

The most widely used silicon high voltage (>300 volt) device for power switching applications is the *Insulated Gate Bipolar Transistor* (IGBT)

which was developed in the 1980s by combining the physics of operation of bipolar transistors and MOSFETs[10]. The structure of the IGBT is deceptively similar to that for the power MOSFET as shown in Fig. 1.10 if viewed as a mere replacement of the N^+ substrate with a P^+ substrate. This substitution creates a four-layer parasitic thyristor which can latch up resulting in destructive failure due to loss of gate control. Fortunately the parasitic thyristor can be defeated by the addition of the P^+ region within the cell[1]. The benefit of the P^+ substrate is the injection of minority carriers into the N-drift region resulting in greatly reducing its resistance. This has enabled the development of high voltage IGBT products with high current carrying capability.

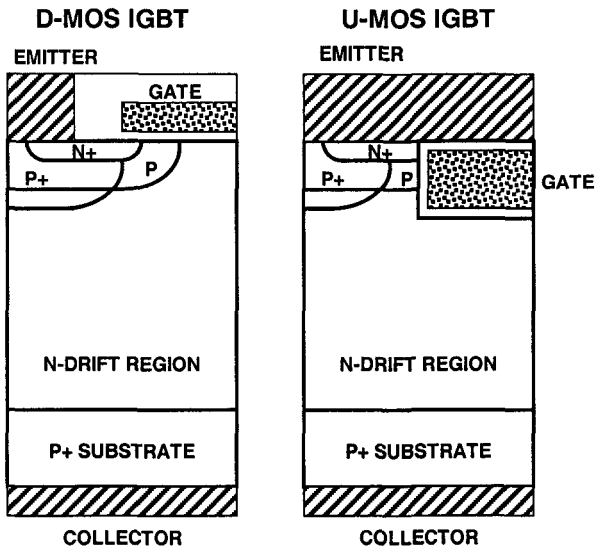

Fig. 1.10 IGBT Device Structures.

The development of the IGBT in silicon carbide has been analyzed and attempted by a few research groups[11,12,13]. The large junction potential and high resistance of the P^+ substrate for silicon carbide results in a relatively high on-state voltage drop for these devices when compared with commercially available silicon devices. Their switching speed is also compromised by the injected stored charge in the on-state. For these reasons, silicon carbide based IGBTs are not discussed in this book.

1.5 Ideal Drift Region for Unipolar Power Devices

The unipolar power devices discussed above all contain a drift region which is designed to support the blocking voltage. The properties (doping concentration and thickness) of the *ideal drift region* can be analyzed by assuming an abrupt junction profile with high doping concentration on one side and a low uniform doping concentration on the other side, while neglecting any junction curvature effects by assuming a parallel-plane configuration. The resistance of the ideal drift region can then be related to the basic properties of the semiconductor material[14].

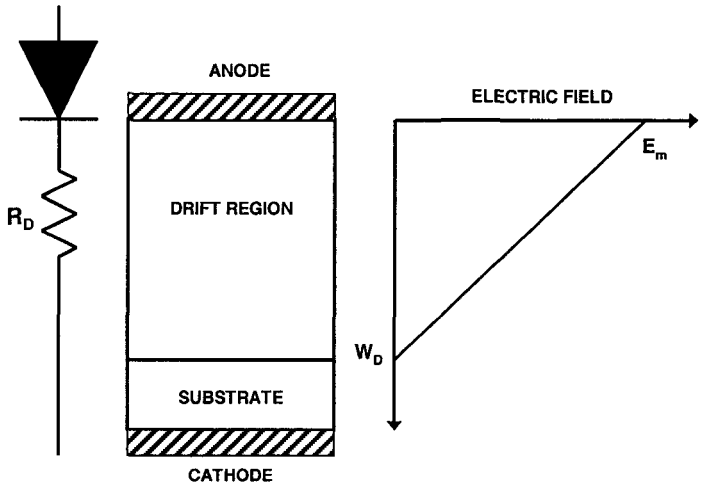

Fig. 1.11 The *Ideal Drift Region* and its Electric Field Distribution.

The solution of Poisson's equation leads to a triangular electric field distribution within a uniformly doped drift region[1] with the slope of the field profile being determined by the doping concentration. The maximum voltage that can be supported by the drift region is determined by the maximum electric field (E_m) reaching the critical electric field (E_c) for breakdown for the semiconductor material. The critical electric field for breakdown and the doping concentration then determine the maximum depletion width (W_D).

The specific resistance (resistance per unit area) of the ideal drift region is given by:

$$R_{on.sp} = \left(\frac{W_D}{q\mu_n N_D} \right) \quad [1.1]$$

Since this resistance was initially considered to be the lowest value achievable with silicon devices, it has historically been referred to as the *ideal specific on-resistance of the drift region.* More recent introduction of the charge-coupling concept, described later in this chapter, has enabled reducing the drift region resistance of silicon devices to below the values predicted by this equation. The depletion width under breakdown conditions is given by:

$$W_D = \frac{2BV}{E_C} \quad [1.2]$$

where BV is the desired breakdown voltage. The doping concentration in the drift region required to obtain this breakdown voltage is given by:

$$N_D = \frac{\varepsilon_S . E_C^2}{2.q.BV} \quad [1.3]$$

Combining these relationships, the specific resistance of the ideal drift region is obtained:

$$R_{on-ideal} = \frac{4BV^2}{\varepsilon_S \mu_n E_C^3} \quad [1.4]$$

The denominator of this equation ($\varepsilon_S.\mu_n.E_C^3$) is commonly referred to as *Baliga's Figure of Merit for Power Devices.* It is an indicator of the impact of the semiconductor material properties on the resistance of the drift region. The dependence of the drift region resistance on the mobility (assumed to be for electrons here because in general they have higher mobility values than for holes) of the carriers favors semiconductors such as Gallium Arsenide. However, the much stronger (cubic) dependence of the on-resistance on the critical electric field for breakdown favors wide band gap semiconductors such as silicon carbide. The critical electric field for breakdown is determined by the impact ionization coefficients for holes and electrons in semiconductors as discussed in the next chapter.

The change in the specific on-resistance for the drift region with critical electric field and mobility is shown in Fig. 1.12 for the case of a breakdown voltage of 1000 volts. The location of the properties for

silicon, gallium arsenide, and silicon carbide are shown in the figure by the points. The improvement in drift region resistance for GaAs in comparison with silicon is largely due to its much greater mobility for electrons. The improvement in drift region resistance for SiC in comparison with silicon is largely due to its much larger critical electric field for breakdown. Based upon these considerations, excellent high voltage Schottky rectifiers were developed from GaAs in the 1980s[15]. Much greater improvement in performance is clearly indicated for silicon carbide devices which is the subject of this book.

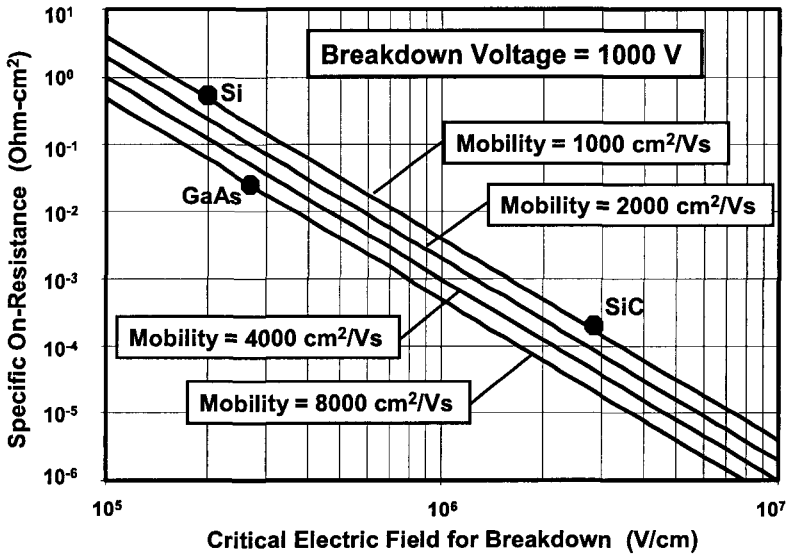

Fig. 1.12 Specific On-Resistance of the *Ideal Drift Region.*

1.6 Summary

The motivation for the development of silicon carbide unipolar devices has been reviewed in this chapter. Although excellent unipolar silicon Schottky rectifiers and power MOSFETs are commercially available with breakdown voltages below 200 volts, the resistance of their drift region increases rapidly at higher breakdown voltages producing significant power losses in applications. This problem can be overcome using silicon carbide based unipolar devices.

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Chapter 2

Material Properties and Technology

In the previous chapter, it was demonstrated the resistance of the drift region in unipolar vertical power devices is strongly dependent upon the fundamental properties of the semiconductor material. In this chapter, the measured properties for silicon carbide are reviewed and compared with those for silicon. These properties are then used to obtain other parameters (such as the built-in potential) which are relevant to the analysis of the performance of devices discussed in the rest of the book. The discussion is constrained to the 4H poly-type of silicon carbide because its properties are superior to those reported for the 6H poly-type. The parameters given in this chapter were used during two-dimensional numerical simulations to determine the characteristics of various devices discussed in this book. Data on the 6H poly-type is sometimes included to demonstrate the reasons that the 4H poly-type is preferred for power device structures. The 4H-SiC material is commercially available from several sources for the development and manufacturing of power devices because of its superior properties. Manufacturers are continually reducing the micropipe density in this material while increasing the diameter of commercially available wafers.

The second portion of this chapter provides a review of the technology developed for the fabrication of silicon carbide power devices. One of the advantages of silicon carbide is that, unlike gallium arsenide, its processing is compatible with silicon devices without the problem of contamination of production lines. It is advantageous to implement any available silicon process technologies, such as ion-implantation or reactive ion etching, to the fabrication of silicon carbide devices. This approach has been generally successful with the exception of the need to anneal the implants at much higher temperatures. Empirical studies performed on the oxidation and passivation of the silicon carbide surface, as well those on the formation of metal-contacts, are also reviewed in this portion of the chapter.

2.1 Fundamental Properties

This section provides a summary of the fundamental properties of silicon carbide[1,2,3] and compares them with those for silicon[4]. Only the properties for the 4H poly-type have been included here as discussed above. The basic properties of relevance to power devices are the energy band gap, the impact ionization coefficients, the dielectric constant, the thermal conductivity, the electron affinity, and the carrier mobility. Since the intrinsic carrier concentration and the built-in potential can be extracted by using this information, their values have also been computed and compared with those for silicon in this section.

Properties	Silicon	4H-SiC
Energy Band Gap (eV)	1.10	3.26
Relative Dielectric Constant	11.7	9.7
Thermal Conductivity (W/cm K)	1.5	3.7
Electron Affinity (eV)	4.05	3.7
Density of States Conduction Band (cm^{-3})	2.80×10^{19}	1.23×10^{19}
Density of States Valence Band (cm^{-3})	1.04×10^{19}	4.58×10^{18}

Fig. 2.1 Fundamental Material Properties.

2.1.1 Energy Band Gap

The energy band gap of silicon carbide is much larger than that for silicon allowing its classification as a wide band gap semiconductor. The band gap for 4H-SiC is 3.26 eV, which is 3 times larger than that for silicon. The band gap for 6H-SiC of 3.0 eV is slightly smaller. Since a larger band gap results in a smaller generation of carriers in the depletion regions of devices, it is favorable for reducing the leakage current of devices which utilize P-N junctions to support voltages. The larger band gap is also favorable for producing Metal-Semiconductor contacts with larger Schottky barrier heights. This enables reduction of the leakage current in Schottky rectifiers and MESFETs.

The intrinsic carrier concentration is determined by the thermal generation of electron hole pairs across the energy band gap of a semiconductor. Its value can be calculated by using the energy band gap (E_G) and the density of states in the conduction (N_C) and valence (N_V) bands:

$$n_i = \sqrt{n.p} = \sqrt{N_C.N_V}\, e^{-(E_G/2kT)} \qquad [2.1]$$

where k is Boltzmann's constant (1.38 x 10^{-23} J/°K) and T is the absolute temperature. For silicon, the intrinsic carrier concentration is given by:

$$n_i = 3.87x10^{16} T^{3/2} e^{-(7.02x10^3)/T} \qquad [2.2]$$

while that for 4H-SiC, it is given by:

$$n_i = 1.70x10^{16} T^{3/2} e^{-(2.08x10^4)/T} \qquad [2.3]$$

Using these equations, the intrinsic carrier concentration can be calculated as a function of temperature. The results are plotted in Fig. 2.2 and Fig. 2.3. The traditional method for making this plot is shown in Fig. 2.2 by using an inverse temperature scale for the x-axis. The additional Fig. 2.3 is provided here because it is easier to relate the value of the intrinsic carrier concentration to the temperature with it plotted on the x-axis. It is obvious that the intrinsic carrier concentration for silicon carbide is far smaller than for silicon due to the large difference in band gap energy. At room temperature (300°K), the intrinsic carrier concentration for silicon is 1.4 x 10^{10} cm^{-3} while that for 4H-SiC is only 6.7 x 10^{-11} cm^{-3}. This demonstrates that the bulk generation current is negligible for the determination of the leakage current in silicon carbide

devices. Surface generation currents may be much larger due to the presence of states within the band gap.

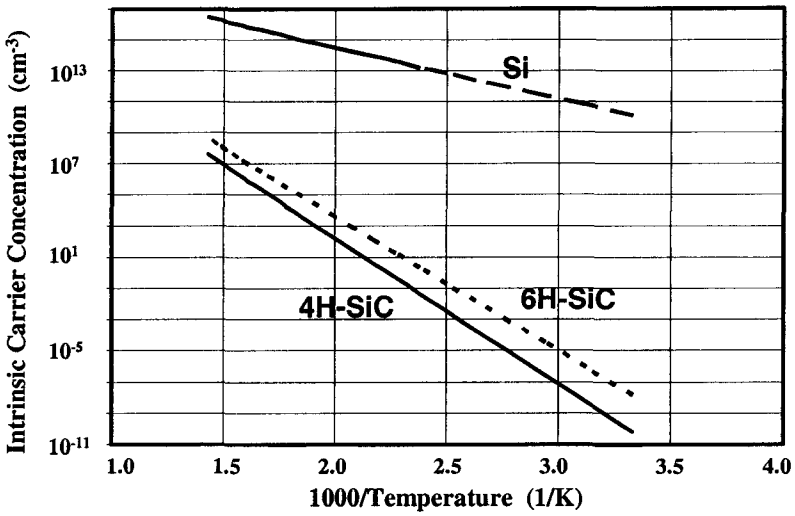

Fig. 2.2 Intrinsic Carrier Concentration.

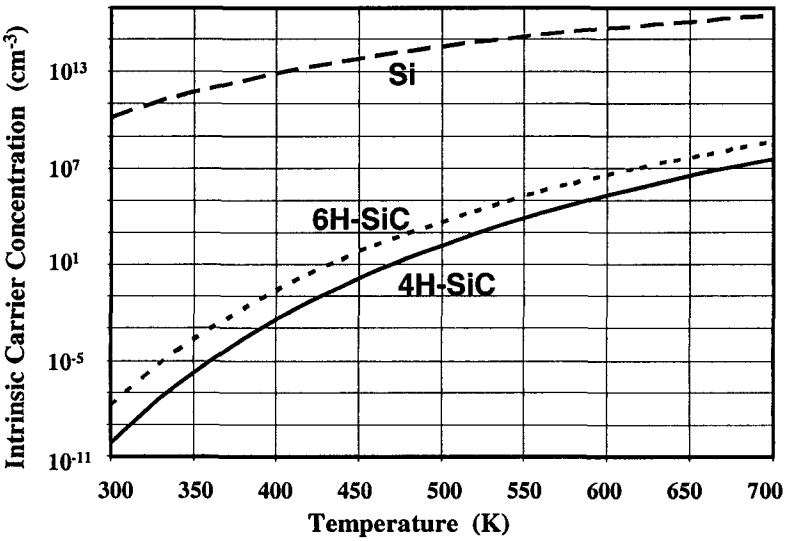

Fig. 2.3 Intrinsic Carrier Concentration.

For silicon, the intrinsic carrier concentration becomes equal to a typical doping concentration of 1 x 10^{15} cm^{-3} at a relatively low temperature of 540 °K or 267 °C. In contrast, the intrinsic carrier concentration for 4H-SiC is only 3.9 x 10^{7} cm^{-3} even at 700 °K or 427 °C. The development of mesoplasmas has been associated with the intrinsic carrier concentration becoming comparable to the doping concentration[5]. Mesoplasmas create current filaments that have very high current density leading to destructive failure in semiconductors. This is obviously much less likely in silicon carbide.

The built-in potential of P-N junctions can play an important role in determining the operation and design of power semiconductor devices. As an example, the built-in potential determines the zero-bias depletion width which is important for calculation of the on-resistance in power DMOSFETs. It has a strong impact on the on-state voltage drop in JBS rectifiers, and is an important parameter used for the design of normally-off accumulation mode MOSFETs. These structures are discussed in detail later in the book. The built-in voltage is given by:

$$V_{bi} = \frac{kT}{q} \ln\left(\frac{N_A^- . N_D^+}{n_i^2}\right) \qquad [2.4]$$

where N_A^- and N_D^+ are the ionized impurity concentrations on the two sides of an abrupt P-N junction. For silicon, their values are equal to the doping concentration because of the small dopant ionization energy levels. This does not apply to silicon carbide because of the much larger dopant ionization levels as discussed later in this chapter.

The calculated built-in potential is shown in Fig. 2.4 as a function of temperature for a typical operating range for power devices. In making the plots, the product ($N_A^-.N_D^+$) was assumed to be 10^{35} cm^{-6}. This would be applicable for a typical doping concentration of 1 x 10^{19} cm^{-3} on the heavily doped side of the junction and 1 x 10^{16} cm^{-3} on the lightly doped side of the junction. The built-in potential for silicon carbide is much larger than that for silicon due to the far smaller values for the intrinsic carrier concentration. This can be a disadvantage due to the larger zero bias depletion width for silicon carbide as shown later in the chapter. As an example, the larger zero bias depletion width consumes space within the D-MOSFET cell structure increasing the on-resistance by constricting the area through which current can flow. In contrast, the larger built-in potential for SiC and its associated larger zero bias depletion width can be taken advantage of in making innovative

device structures, such as the ACCUFET, that are tailored to the unique properties of SiC.

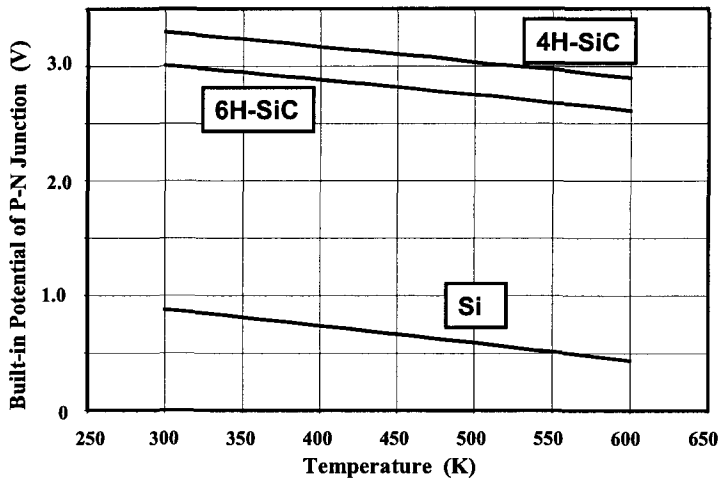

Fig. 2.4 Built-in Potential for a P-N Junction in Si and SiC.

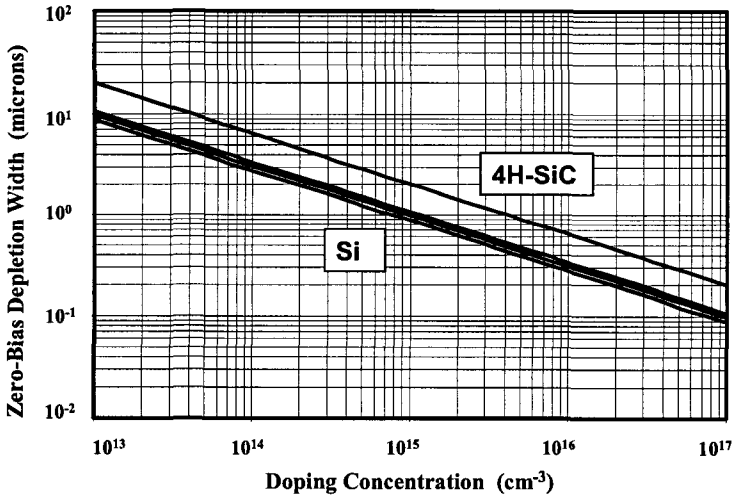

Fig. 2.5 Zero-Bias Depletion Width in Si and SiC.

The calculated zero bias depletion width is shown in Fig. 2.5 as a function of the doping concentration on the lightly doped side of the

abrupt P-N junction. For the case of silicon, three lines are given for 300°K, 400°K and 500°K with largest depletion width corresponding to the lowest temperature. For silicon carbide, the lines for these temperatures are very close to each other. For both silicon and silicon carbide, it can be seen that the zero bias depletion width can be substantial in size at low doping concentrations making it important to take this into account during device design and analysis. The zero bias depletion width for SiC is much (about 2x) larger than for silicon for the same doping concentration. However, it is worth noting that the doping concentration in SiC is also much greater for a given breakdown voltage than for silicon as discussed later in the chapter.

2.1.2 Impact Ionization Coefficients

The main advantage of wide band gap semiconductors for power device applications is the greater breakdown voltage capability of these materials. The higher breakdown voltage for these materials is associated with the reduced impact ionization coefficients at any given electric field when compared with silicon. The impact ionization coefficients for semiconductors is dictated by Chynoweth's Law[6,7]:

$$\alpha = a.e^{-b/E} \qquad [2.5]$$

where E is the electric field component in the direction of current flow. The parameters a and b are constants that depend upon the semiconductor material and the temperature. For silicon, the impact ionization rate is much larger for electrons than for holes. However, for silicon carbide the opposite has been found to hold true. For silicon, the impact ionization rates have been measured as a function of electric field and temperature[4,8,9]. The data can be modeled by using $a = 7 \times 10^5$ per cm and $b = 1.23 \times 10^6$ V/cm at room temperature[10].

The impact ionization coefficients for silicon carbide have been recently measured as a function of temperature by using an electron beam excitation method[11]. This method allowed extraction of impact ionization rates in defect free regions of the material by isolating diodes containing defects with an EBIC (Electron Beam Induced Current) image. This was important because substantially enhanced impact ionization rates were discovered when the measurements were conducted at defect sites[12]. For defect free material, the extracted values for the impact ionization coefficient parameters for holes in 4H-SiC were found to be:

$$a(4H-SiC) = 6.46x10^6 - 1.07x10^4 T \quad [2.6]$$

with

$$b(4H-SiC) = 1.75x10^7 \quad [2.7]$$

while for 6H-SiC:

$$a(6H-SiC) = 4.6x10^6 - 7.4x10^3 T \quad [2.8]$$

with

$$b(6H-SiC) = 1.5x10^7 \quad [2.9]$$

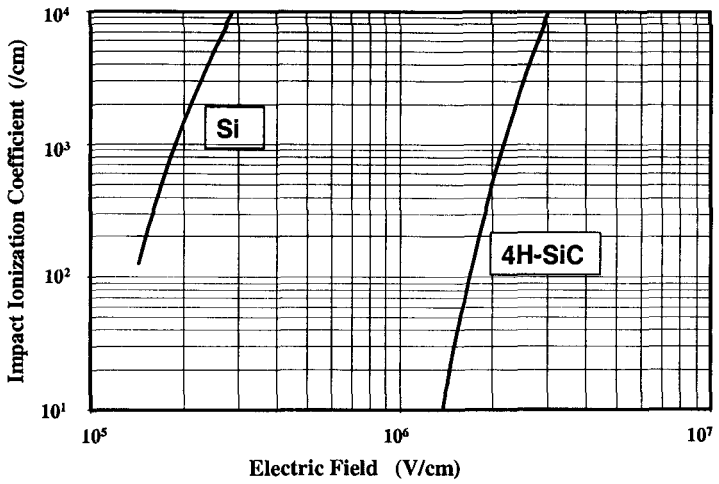

Fig. 2.6 Impact Ionization Coefficients in 4H-SiC and Silicon.

The impact ionization coefficients for 4H-SiC can be compared with those for silicon in Fig. 2.6. This behavior was incorporated in the analytical models used for two-dimensional numerical simulations of device structures discussed later in the book. It can be seen that the onset of significant generation of carriers by impact ionization occurs at much larger electric fields in 4H-SiC when compared with silicon. As a consequence, breakdown in 4H-SiC devices occurs when the electric fields are in the range of 2-3 x 10^6 V/cm – an order of magnitude larger than that for silicon. This implies a much larger critical electric field E_c

for breakdown for 4H-SiC resulting in a big increase in the *Baliga's Figure of Merit.* The critical electric field for breakdown is discussed in more detail in the next chapter.

2.1.3 Electron Mobility

The mobility for electrons is larger than that for holes in silicon carbide. It is therefore favorable to make unipolar devices using N-type drift regions rather than P-type drift regions. The conductivity of the drift region is given by:

$$\rho_n = \frac{1}{q\mu_n N_D} \qquad [2.10]$$

where μ_n by the mobility for electrons which is a function of doping concentration (N_D) and temperature (T).

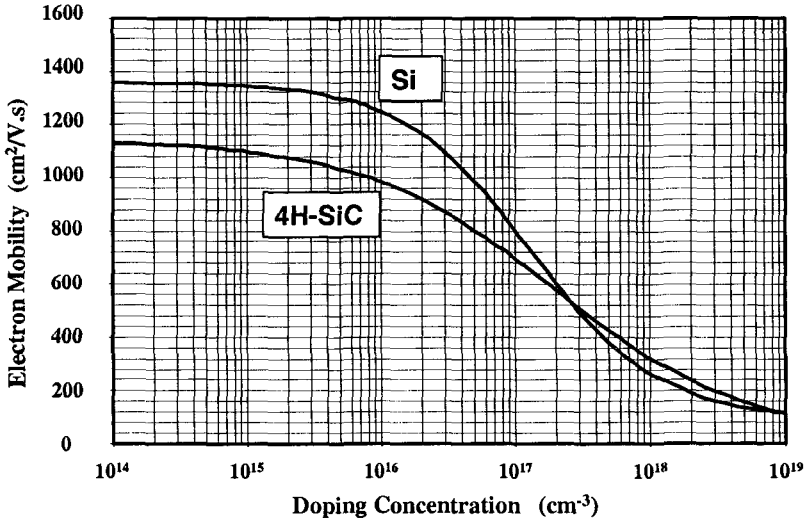

Fig. 2.7 Bulk Mobility for Electrons in 4H-SiC and Silicon.

For silicon, the measured data[13] for mobility of electrons at room temperature as a function of the doping concentration can be modeled by:

$$\mu_n(Si) = \frac{5.10x10^{18} + 92N_D^{0.91}}{3.75x10^{15} + N_D^{0.91}} \qquad [2.11]$$

For silicon carbide, the mobility of electrons at room temperature as a function of the doping concentration can be modeled by[3]:

$$\mu_n(4H - SiC) = \frac{4.05x10^{13} + 20N_D^{0.61}}{3.55x10^{10} + N_D^{0.61}} \qquad [2.12]$$

This behavior has also been theoretically modeled taking into account acoustic and polar optical phonon scattering as well as intervalley scattering[14]. The electron mobility at room temperature is plotted in Fig. 2.7 as a function of doping concentration for silicon and silicon carbide. In both cases, the mobility decreases with increasing doping due to enhanced Coulombic scattering of electrons by the ionized donors. This behavior was incorporated in the analytical models used for two-dimensional numerical simulations of device structures discussed later in the book.

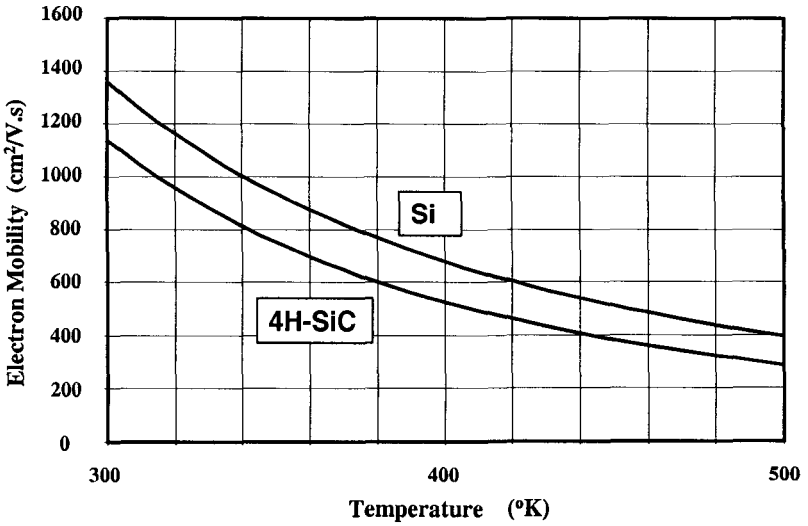

Fig. 2.8 Bulk Mobility for Electrons in 4H-SiC and Silicon.

The mobility decreases in semiconductors with increasing temperature due to enhanced phonon scattering. This holds true for

silicon and 4H-SiC as shown in Fig. 2.8. For silicon, the temperature dependence of the mobility at low doping concentrations can be modeled by[15]:

$$\mu_n(Si) = 1360\left(\frac{T}{300}\right)^{-2.42} \quad \text{[2.13]}$$

For 4H-SiC, the temperature dependence of the mobility at low doping concentrations can be modeled by[3]:

$$\mu_n(4H-SiC) = 1140\left(\frac{T}{300}\right)^{-2.70} \quad \text{[2.14]}$$

This behavior was also incorporated in the analytical models used for two-dimensional numerical simulations of device structures discussed later in the book. The variation of the mobility with temperature is shown in the above figure only up to 500 °K (227 °C). Although there is considerable interest in the performance of silicon carbide devices at much higher temperatures due to its wide band gap structure, the operation of devices above 500 °K is problematic due to degradation of the ohmic contacts and the surface passivation.

2.2 Other Properties Relevant to Power Devices

In this section, other properties for 4H-SiC are provided, which are required for the analysis of power device structures. These properties are compared with those for silicon whenever it is pertinent.

2.2.1 Donor and Acceptor Ionization Energy Levels

In silicon, the donor and acceptor ionization energy is small (50 meV) allowing the assumption that all the donors and acceptor impurities in the lattice are completely ionized at room temperature as well as at higher temperatures. This is not a valid assumption for silicon carbide due to the relatively larger ionization energies for donors and acceptors. The most commonly used donor in 4H-SiC is nitrogen which occupies Carbon sites in the lattice. Its ionization energy is reported to be about 100 meV[1]. To create p-type 4H-SiC, the most commonly used acceptor impurity is Aluminum with an ionization energy of about 200 meV[1]. At above room temperature, the ionized donor concentration is over ninety percent

allowing the approximation that the electron concentration is equal to the donor concentration when calculating the resistivity of drift regions.

2.2.2 Recombination Lifetimes

In silicon, high voltage devices are designed to operate with the injection of minority carriers into the drift region to reduce its resistivity by the conductivity modulation phenomenon[10]. The recombination of holes and electrons plays an important role in determining the switching speed of these structures. The recombination process can occur from band-to-band but is usually assisted by the presence of deep levels in the band gap. The deep levels can also produce leakage current during reverse blocking in power devices by the generation of carriers in the depletion region.

As already pointed out, for silicon carbide, it is appropriate to only consider unipolar devices for power switching applications. This is fortunate because the lifetime values reported for this material is relatively low (10^{-9} to 10^{-7} seconds)[3]. This is consistent with diffusion lengths of between 1 and 2 microns measured by using the EBIC technique[16]. It is likely that these low lifetime and diffusion lengths are associated with surface recombination. The performance of bipolar devices made from 4H-SiC, such as high voltage P-i-N rectifiers, indicates that higher values of bulk lifetime are applicable[17]. However, the large on-state voltage drop and slow switching speed of these devices makes them much less attractive for applications than unipolar devices.

2.2.3 Metal-Semiconductor Contacts

Contacts to power devices are made by using metal films deposited on the surface of its semiconductor layers. A common requirement is to make ohmic contacts to n-type and p-type regions. This can be achieved by using a metal-semiconductor contact with low barrier height and a high doping concentration in the semiconductor to promote tunneling current across the contact. For metal-semiconductor contacts with high doping level in the semiconductor, the contact resistance determined by the tunneling process is dependent upon the barrier height and the doping level[18]:

$$R_c = \exp\left[\frac{2\sqrt{\varepsilon_S m^*}}{h}\left(\frac{\phi_{bn}}{\sqrt{N_D}}\right)\right] \qquad [2.15]$$

In order to take full advantage of the low specific on-resistance of the drift region in silicon carbide devices, it is important to obtain a specific contact resistance that is several orders of magnitude smaller than that of the drift region. This is also necessary because the contact areas are often only a small fraction (less than 10 percent) of the active area of most power device structures. Typically, specific contact resistances of less than 1 x 10^{-5} ohm-cm^2 are desirable to n-type regions.

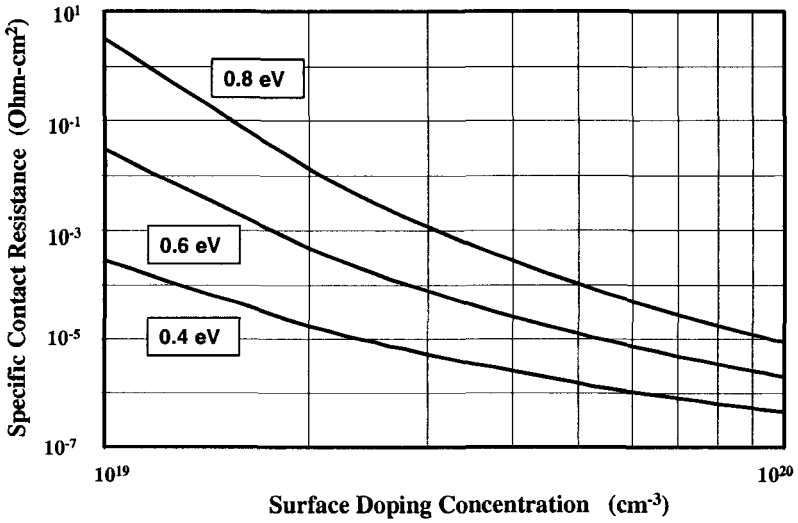

Fig. 2.9 Specific Resistance at Metal-Semiconductor Contacts.

The specific contact resistance calculated using the above formula is plotted in Fig. 2.9 as a function of the doping concentration using the barrier height as a parameter. Unfortunately, the barrier heights of metal contacts to silicon carbide tend to be large due to its wide band gap. From the figure, it can be concluded that a specific contact resistance of 1 x 10^{-5} ohm-cm^2 can be obtained for a doping concentration of 5 x 10^{19} cm^{-3} if the barrier height is 0.6 eV. Such high surface doping concentrations can be achieved for N-type 4H-SiC by using hot-implantation of nitrogen, phosphorus or arsenic followed by appropriate high temperature annealing[19]. Ohmic contacts with specific resistances of less than 10^{-6} Ohm-cm^2 have been reported to ion-implanted layers by using nickel and titanium[20].

Metal-semiconductor contacts can also be used to make Schottky barrier rectifiers with high breakdown voltages by using silicon carbide. In this case, it is advantageous to have a relatively large barrier height to reduce the leakage current. The commonly used metals for formation of Schottky barriers to 4H-SiC are Titanium and Nickel. The barrier heights measured for these contacts range from 1.10 to 1.25 eV for Titanium and 1.30 to 1.60 eV for Nickel[21,22,23]. The use of these metals to fabricate high voltage device structures is discussed in subsequent chapters of the book.

2.3 Fabrication Technology

Due to the substantial infrastructure available to fabricate silicon devices, it is advantageous to manufacture silicon carbide devices using the same technology platform. During the last fifteen years of research, it has been established that silicon carbide devices can be fabricated using the same equipment used for silicon devices in most instances. However, it has been found that much higher temperatures are needed for the annealing of ion implanted regions in silicon carbide to activate the dopants and remove the damage. In addition, the design of device structures in silicon carbide requires giving special consideration to the low diffusion coefficients for impurities. These unique issues are discussed in this section of the chapter.

2.3.1 *Diffusion Coefficients and Solubility of Dopants*

In silicon power devices, it is common-place to drive the dopants after ion-implantation to increase the junction depth. The widely used double-diffused (DMOS) process for silicon power MOSFETs utilizes the difference in the junction depth of the P-base and N^+ source regions to define the channel length without relying upon high resolution lithography to achieve sub-micron dimensions[10]. In silicon carbide, the diffusion coefficients are very small even at relatively high temperatures[1]. For nitrogen - the commonly used N-type dopant, the effective diffusion coefficient is reported as 5×10^{-12} cm^2/s even at 2450 °C. For aluminum - the commonly used P-type dopant, the effective diffusion coefficient is reported as 3×10^{-14} to 6×10^{-12} cm^2/s even at 1800 - 2000 °C. Due to the on-set of dissociation at these temperatures with attendant generation of defects, it is not practical to drive dopants in silicon carbide after ion implantation. The design of power device

structures in silicon carbide must take this limitation in process technology into account.

The solid solubility of dopants in silicon carbide has been reported to be comparable to that for dopants in silicon[1]. For nitrogen and aluminum, the solubility is in excess of 1 x 10^{20} cm^{-3}. Ion implanted nitrogen[24] and aluminum[25] doped layers have been formed with impurity concentrations ranging from 1 x 10^{19} cm^{-3} to 1 x 10^{20} cm^{-3}. These values are sufficient for the fabrication of most high voltage power device structures.

2.3.2 Ion Implantation and Annealing

A significant body of literature has developed on the ion implantation of impurities into silicon carbide and the subsequent annealing process to activate the dopants and remove lattice damage. The reader should refer to the proceeding of the conferences on 'Silicon Carbide and Related Materials' for an abundance of information on this topic.

Although room temperature ion implantation can be successful, it has been found that hot-implantation produces a higher degree of impurity activation and a smaller number of defects. The hot-implants are usually performed in the 500 °C range followed by anneals performed at between 1200 and 1600 °C. At above 1600 °C, degradation of the silicon carbide surface is observed due to sublimation or evaporation[19,25]. The surface degradation can be mitigated by using a graphite boat to host the implanted wafer with another silicon carbide wafer placed on top (proximity anneals)[26].

2.3.3 Gate Oxide Formation

Silicon bipolar power devices, such as the bipolar power transistor and the gate turn-off thyristor (GTO), were supplanted with MOS-gated devices in the 1980s. The silicon power MOSFET replaced the bipolar transistor for lower voltage (< 200 V) applications while the IGBT replaced bipolar transistors and GTOs for high voltage (>200V) applications. The main advantage of these MOS-gated device architectures was voltage controlled operation which greatly simplified the control circuit making it amenable to integration[10]. This feature must be extended to silicon carbide power devices to make them attractive from an applications perspective.

The issues that must be considered for the gate dielectric in MOS-gated silicon carbide devices are the quality of the oxide-semiconductor interface and the ability of the oxide to withstand higher electric fields than within silicon devices[27]. The quality of the oxide-semiconductor interface determines not only the channel mobility but impacts the threshold voltage of the devices. The electric field in the oxide is related to the electric field in the semiconductor by Gauss's Law:

$$E_{ox} = \frac{\varepsilon_{semi}}{\varepsilon_{ox}} E_{semi} \approx 3E_{semi} \qquad [2.16]$$

In silicon, the maximum electric field at breakdown is in the 3 x 10^5 V/cm range. Consequently, the maximum electric field in the oxide remains well below its breakdown field strength of 10^7 V/cm. In contrast, the maximum electric field for breakdown in silicon carbide is in the 3 x 10^6 V/cm range. Consequently, the electric field in the oxide can approach its breakdown strength and easily exceed a field of 3 x 10^6 V/cm, which is considered to be the threshold for reliable operation. One approach to overcome this problem is to use gate dielectric material with a larger permittivity[28,29]. In these references, it has been theoretically shown that the specific on-resistance can be reduced by an order of magnitude by using high dielectric constant gate material. A permittivity of about 15 (versus 3.85 for silicon dioxide) was found to be adequate for allowing full use of the high electric field strength for breakdown in silicon carbide without problems with unacceptably high oxide electric fields. One example of such a dielectric is zirconium oxide[30].

A second approach utilizes improved device structural architecture to screen the gate dielectric from the high electric fields within the silicon carbide. This is discussed in detail in the chapters on shielded planar and shielded trench gate MOSFETs in this book. Such devices can then be made using silicon dioxide whose properties are well understood. In this case, the silicon dioxide can be either grown by the thermal oxidation of silicon dioxide or by the formation of the oxide using chemical vapor deposition processes. Many studies on both of these techniques are available in the literature.

The thermal oxidation of SiC has been reviewed in the literature and the growth rate of the oxide has been compared with that on silicon surfaces[31]. Some selected data is shown in Fig. 2.10 to illustrate the much lower growth rate of thermal oxide on SiC when compared with silicon for both dry and wet oxidation conditions. The data shown in this figure

are for 6H-SiC but similar values are applicable to the 4H-SiC polytype[32]. It is obvious that a much higher temperature and longer time duration is required for the growth of oxides on silicon carbide. This oxide has been shown to be essentially silicon dioxide with no carbon incorporated in the film. The small amount of aluminum incorporated into the oxide, when grown on p-type SiC, has been found to have no adverse effect[33,34] on the MOS properties.

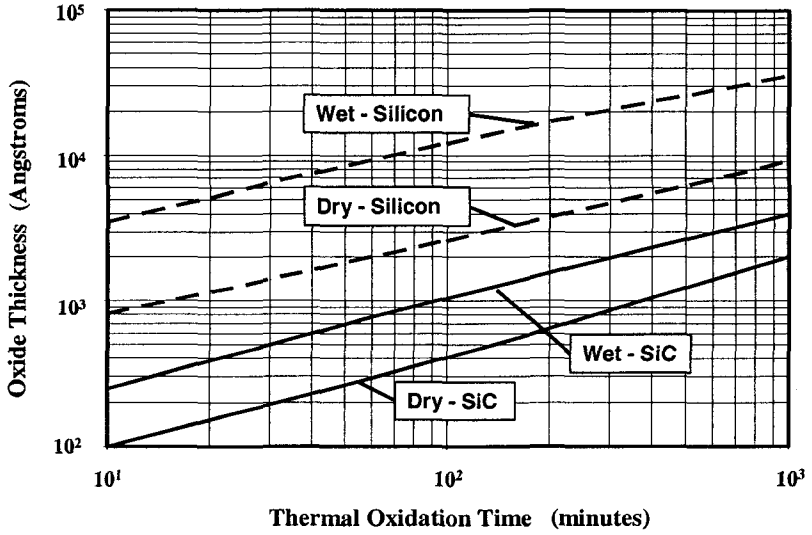

Fig. 2.10 Comparison of Thermal Oxidation of SiC with silicon at 1200 °C.

The gate dielectric produced with thermal oxidation of 6H-SiC has been found to be satisfactory for making MOSFETs with reasonable inversion layer mobility[35]. However, this method did not produce sufficiently high quality interfaces on 4H-SiC to make MOSFETs. It was discovered at PSRC that a low temperature oxide subjected to a wet nitrogen anneal enabled fabrication of n-channel inversion layer MOSFETs in 4H-SiC with an effective inversion layer mobility of 165 cm^2/Vs[36,37]. Although the gate oxide for these MOSFETs was unusually large (9000 angstroms), high performance MOSFETs with similar mobility values, were subsequently fabricated at PSRC using a gate oxide thickness of 850 angstroms[38]. At PSRC, an extensive evaluation of process conditions was performed to determine their impact on the inversion layer mobility. This work has been validated by other groups[39].

In addition, inversion layer mobility in the range of 50 cm^2/V-s has been reported on thermally grown oxides subjected to annealing in nitric oxide[31,40]. These experiments indicate that power MOSFETs with low specific on-resistance can be developed from 4H-SiC.

2.3.4 Reactive Ion Etching of Trenches

The first silicon power MOSFETs were manufactured using the Double-diffused or DMOS process to form a planar gate architecture[41]. Although these devices offered excellent input impedance and fast switching performance for low voltage (< 100 volt) applications, their on-resistance was found to be limited by the presence of a JFET region. The JFET region could be eliminated by adopting a trench gate or UMOS process[10]. The trench gate structure in the silicon power MOSFET is fabricated by using reactive ion etching. An equivalent process for silicon carbide was not developed until the mid 1990s. Until then, alternative methods such as etching with molten KOH solutions or the use of amorphization of selective SiC regions was explored[42].

Reactive ion etching is the most convenient process for formation of trenches in silicon carbide enabling the fabrication of devices with processes compatible with silicon device manufacturing technology. Many gas compositions have been tried for the formation of trenches in silicon carbide. For application to power devices, the trenches should have a nearly vertical profile with a slightly rounded bottom to reduce electric field enhancement. The trench surface must be smooth and free of damage in order to reduce interface states and obtain high mobility along the inversion channel formed on the trench sidewalls. Reactive ion etching using a SF_6/O_2 mixture has been found to produce trenches that meet these requirements[43]. Other reactive ion etching chemistries using fluorinated gases[44] have also been reported to produce trenches with vertical profiles and smooth surfaces.

2.4 Summary

The properties of silicon carbide relevant to power devices have been reviewed in this chapter. An improved knowledge of the impact ionization coefficients has allowed projection of very high performance for SiC based unipolar devices. The status of process technology for the fabrication of these unipolar devices has also been summarized here.

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Chapter 9

Planar Power MOSFETs

The planar power MOSFET was the first commercially successful unipolar switch developed using silicon technology[1] once the issues related to the metal-oxide-semiconductor interface had been resolved for CMOS technology. In order to reduce cost, the channel in these devices was created by the double diffusion (or D-MOS) process. In the DMOS process, the P-base and N^+ source regions are formed by ion implantations masked by a common edge defined by a refractory polysilicon gate electrode. A drive-in cycle is used after each ion implantation step to move the P-N junction in the lateral direction under the gate electrode. The separation between the N^+/P-base junction and the P-base/N-drift junction under the gate electrode defines the channel. Consequently, the channel length can be reduced to sub-micron dimensions without the need for high resolution lithography. This approach served the industry quite well from the 1970s into the 1990s with planar power MOSFETs still available for power electronic applications. In the 1990s, the industry borrowed the trench technology originally developed for DRAMs to introduce the UMOSFET structure for commercial applications[2]. This was important for the reduction of the channel and JFET components in the planar MOSFET structure designed for lower (< 30 volts) voltage applications. This UMOSFET structure has also been explored in silicon carbide as described in a subsequent chapter.

In silicon power MOSFETs, the on-resistance becomes dominated by the resistance of the drift region when the breakdown voltage exceeds 200 volts. At high breakdown voltages, the specific on-resistance for these devices becomes greater than 10^{-2} Ohm-cm^2, as shown in Fig. 3.6, leading to an on-state voltage drop of more than 1 volt at a typical on-state current density of 100 A/cm^2. For this reason, the Insulated Gate Bipolar Transistor (IGBT) was developed in the 1980s to serve medium and high power systems[2]. The superior performance of the

IGBT in high voltage applications relegated the silicon MOSFETs to applications with operating voltages below 100 volts. Novel silicon structures that utilize the charge-coupling concept have allowed extending the breakdown voltage of power MOSFETs to the 600 volt range[3]. However, their specific on-resistance is still quite large limiting their use to high operating frequencies where switching losses dominate.

In principle, the much lower resistance of the drift region in silicon carbide should enable development of power MOSFETs with very high breakdown voltages. These devices offer not only fast switching speed but also superior safe operating area when compared to high voltage silicon IGBTs. This allows reduction of both the switching loss and conduction loss components in power circuits[4]. Unfortunately, the power MOSFET structures developed in silicon cannot be directly utilized to form high performance silicon carbide devices. Firstly, the lack of significant diffusion of dopants in silicon carbide prevents the use of the silicon DMOS process. Secondly, a high electric field occurs in the gate oxide of the silicon carbide MOSFET exceeding its rupture strength leading to catastrophic failure of devices in the blocking mode at high voltages. Thirdly, when compared with silicon, the smaller band offset between the conduction band of silicon carbide and silicon dioxide can produce injection of hot carriers into the oxide leading to instability during operation. In addition, the quality of the oxide-semiconductor interface for silicon carbide must be improved to allow good control over the threshold voltage and the channel mobility.

This chapter begins with a review of the basic principles of operation of the planar MOSFET structure. A planar MOSFET structure formed by staggering the ion implantation of the P-base and N^+ source regions to create the channel is then described. Next, the problem of exacerbation of reach-through breakdown in silicon carbide is considered. Based upon fundamental considerations, the difference between the threshold voltage for silicon and silicon carbide structures is analyzed. The relatively high doping concentrations and large channel lengths required to prevent reach-through are shown to be serious limitations to obtaining low specific on-resistance in these devices. In addition, the much larger electric field in silicon carbide is shown to lead to a high electric field in the gate oxide. Structures designed to reduce the electric field at the gate oxide by using a shielding region are therefore essential to realization of practical silicon carbide MOSFETs even after the MOS interface quality is improved. These structures are described and analyzed in the next chapter. The results of the analysis of the planar

silicon carbide MOSFET structures by using two-dimensional numerical simulations are described in this chapter followed by the description of experimental results on relevant structures to define the state of the development effort on these devices.

9.1 Planar Power MOSFET Structure

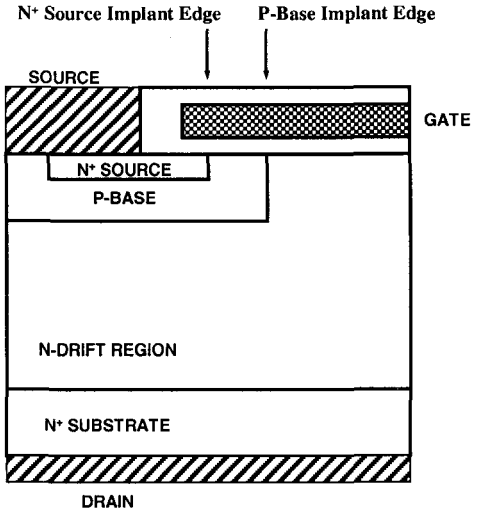

Fig. 9.1 The Planar Power MOSFET Structure.

The basic structure of the planar power MOSFET is shown in Fig. 9.1 together with the location of the ion implantation edges. In recognition of the low diffusion coefficients for dopants in silicon carbide, it was proposed[5] that the P-base and N^+ source ion implantations be staggered by using photoresist masks rather that be defined by the gate edge. It was also suggested that the P-base region be first amorphized to obtain a more uniform dopant distribution to suppress reach-through. This approach with staggered P-base and N^+ source implants was subsequently taken by several groups to fabricate high voltage devices[6]. These devices have been called DIMOSFETs because of the Double-Implant process used for their fabrication. The measured performance of these structures is discussed at the end of the chapter.

9.1.1 Planar Power MOSFET Structure: Blocking Characteristics

In the forward blocking mode of the planar power MOSFET, the voltage is supported by a depletion region formed on both sides of the P-base/N-drift junction. The maximum blocking voltage can be determined by the electric field at this junction becoming equal to the critical electric field for breakdown if the parasitic $N^+/P/N$ bipolar transistor is completely suppressed. This suppression is accomplished by short-circuiting the N^+ source and P-base regions using the source metal as shown on the upper left hand side of the cross-section. However, a large leakage current can occur when the depletion region in the P-base region reaches-through to the N^+ source region. The doping concentration and thickness of the P-base region must be designed to prevent the reach-through phenomenon from limiting the breakdown voltage.

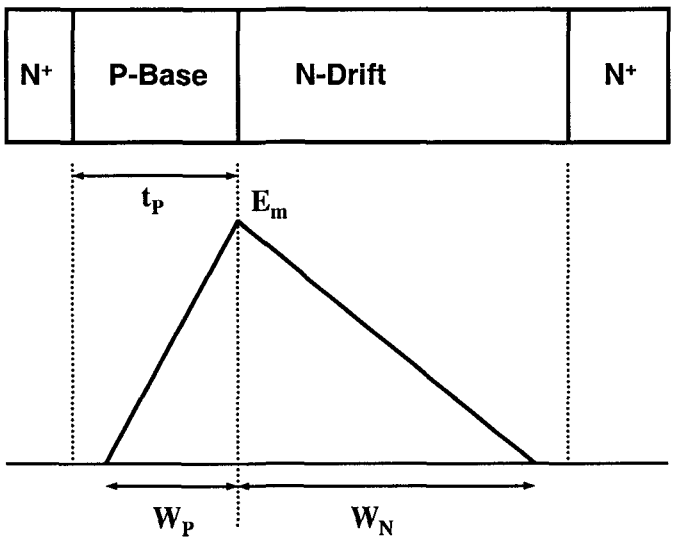

Fig. 9.2 Reach-Through in a Power MOSFET Structure.

The applied drain voltage is supported by the N-drift region and the P-base region with a triangular electric field distribution as shown in Fig. 9.2 if the doping is uniform on both sides. The maximum electric field occurs at the P-base/N-drift junction. The depletion width on the P-base side is related to the maximum electric field by:

$$W_P = \frac{\varepsilon_S E_m}{qN_A} \quad [9.1]$$

where N_A is the doping concentration in the P-base region. The minimum P-base thickness required to prevent reach-though limited breakdown can be obtained by assuming that the maximum electric field at the P-base/N-drift junction reaches the critical electric field for breakdown when the P-base region is completely depleted:

$$t_P = \frac{\varepsilon_S E_C}{qN_A} \quad [9.2]$$

where E_C is the critical electric field for breakdown in the semiconductor.

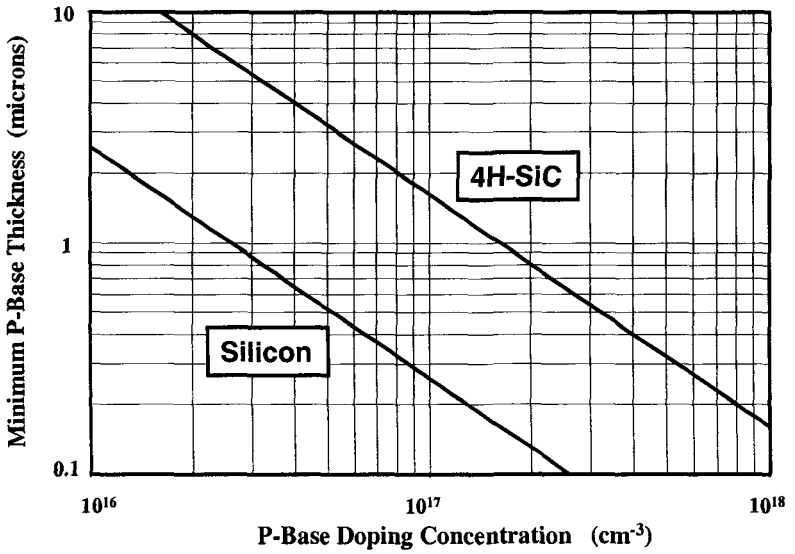

Fig. 9.3 Comparison of Minimum P-Base Thickness to prevent Reach-Through Breakdown in 4H-SiC and Silicon.

The calculated minimum P-base thickness for 4H-SiC power MOSFETs is compared with that for silicon in Fig. 9.3. At any given P-base doping concentration, the thickness for 4H-SiC is about six times larger than for silicon. This implies that the minimum channel length required for silicon carbide devices is much larger than for silicon devices resulting in a big increase in the on-resistance. The enhancement

of the on-resistance is compounded by the lower channel inversion layer mobility observed for silicon carbide.

The minimum thickness of the P-base region required to prevent reach-through breakdown decreases with increasing doping concentration as shown in Fig. 9.3. The typical P-base doping concentration for silicon power MOSFETs is 1 x 10^{17} cm^{-3} to obtain a threshold voltage between 1 and 2 volts for a gate oxide thickness of 500 to 1000 angstroms. At this doping level, the P-base thickness can be reduced to 0.5 microns without reach-through limiting the breakdown voltage. In contrast, for 4H-SiC, it is necessary to increase the P-base doping concentration to above 4 x 10^{17} cm^{-3} to prevent reach-through with a 0.5 micron P-base thickness. This higher doping concentration increases the threshold voltage as discussed in the next section.

The maximum blocking voltage capability of the power MOSFET structure is determined by the drift region doping concentration and thickness as already discussed in chapter 3. However, in the power MOSFET structure, a high electric field also develops in the gate oxide under forward blocking conditions. The electric field developed in the oxide is related to the electric field in the underlying semiconductor by Gausses Law:

$$E_{Oxide} = \left(\frac{\varepsilon_{Semi}}{\varepsilon_{Oxide}} \right) . E_{Semi} \qquad [9.3]$$

where ε_{Semi} and ε_{Oxide} are the dielectric constants of the semiconductor and the oxide and E_{Semi} is the electric field in the semiconductor. In the case of both silicon and silicon carbide, the electric field in the oxide is about 3 times larger than in the semiconductor. Since the maximum electric field in the silicon drift region remains below 3 x 10^5 V/cm, the electric field in the oxide does not exceed its reliability limit of about 3 x 10^6 V/cm. However, for 4H-SiC, the electric field in the oxide reaches a value of 9 x 10^6 V/cm when the field in the semiconductor reaches its breakdown strength. This value not only exceeds the reliability limit but can cause rupture of the oxide leading to catastrophic breakdown. It is therefore important to monitor the electric field in the gate oxide when designing and modeling the silicon carbide MOSFET structures. Novel structures[7] that shield the gate oxide from high electric field have also been proposed and demonstrated to resolve this problem. These structures will be discussed in the next chapter.

9.1.2 Planar Power MOSFET Structure: Forward Conduction

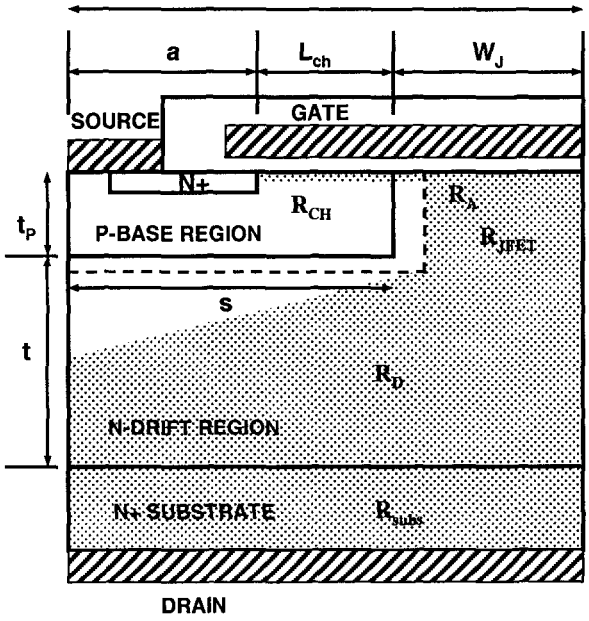

Fig. 9.4 Current Flow Path in the Planar 4H-SiC Power MOSFET.

Current flow between the drain and source can be induced by creating an inversion layer channel on the surface of the P-base region. The current path is illustrated in Fig. 9.4 by the dotted area. The current flows through the inversion layer channel formed due to the applied gate bias into the JFET region via the accumulation layer formed above it under the gate oxide. It then spreads into the N-drift region at a 45 degree angle and becomes uniform through the rest of the structure. The total on-resistance for the planar power MOSFET structure is determined by the resistance of these components in the current path:

$$R_{on,sp} = R_{CH} + R_A + R_{JFET} + R_D + R_{subs} \quad [9.4]$$

where R_{CH} is the channel resistance, R_A is the accumulation region resistance, R_{JFET} is the resistance of the JFET region, R_D is the resistance of the drift region after taking into account current spreading from the JFET region, and R_{subs} is the resistance of the N^+ substrate. These resistances can be analytically modeled by using the current flow pattern

indicated by the shaded regions in Fig. 9.4. In this figure, the depletion region boundaries have also been shown using dashed lines.

The specific channel resistance is given by:

$$R_{CH} = \frac{(L_{CH} \cdot p)}{\mu_{inv} C_{ox} (V_G - V_T)} \quad [9.5]$$

where L_{CH} is the channel length as shown in Fig. 9.4, μ_{inv} is the mobility for electrons in the inversion layer channel, C_{ox} is the specific capacitance of the gate oxide, V_G is the applied gate bias, and V_T is the threshold voltage. The specific capacitance can be obtained using:

$$C_{ox} = \frac{\varepsilon_{ox}}{t_{ox}} \quad [9.6]$$

where ε_{ox} is the dielectric constant for the gate oxide and t_{ox} is its thickness.

The specific resistance of the accumulation region is given by:

$$R_A = \frac{K(W_J - W_P)p}{\mu_a C_{ox} (V_G - V_T)} \quad [9.7]$$

where μ_a is the mobility for electrons in the accumulation layer, C_{ox} is the specific capacitance of the gate oxide, V_G is the applied gate bias, and V_T is the threshold voltage. The factor K is used to account for two-dimensional current spreading from the channel into the JFET region with a typical value of 0.6 for silicon devices. In this equation, W_P is the zero-bias depletion width at the P-base/N-drift junction. It can be determined using:

$$W_P = \sqrt{\frac{2\varepsilon_S V_{biP}}{qN_D}} \quad [9.8]$$

where the built-in potential V_{biP} for the P-N junction is typically 3.3 volts for 4H-SiC.

The specific JFET region resistance is given by:

$$R_{JFET} = \rho_D . t_P \left(\frac{p}{W_J - W_P} \right) \quad [9.9]$$

where t_p is the depth of the P-base region.

The drift region spreading resistance can be obtained by using:

$$R_D = \rho_D.p.\ln\left(\frac{p}{W_J - W_P}\right) + \rho_D.(t - s - W_P) \qquad [9.10]$$

where t is the thickness of the drift region below the P-base region and s is the width of the P-base region.

The contribution to the resistance from the N^+ substrate is given by:

$$R_{subs} = \rho_{subs}.t_{subs} \qquad [9.11]$$

where ρ_{subs} and t_{subs} are the resistivity and thickness of the substrate, respectively. A typical value for this contribution is 4×10^{-4} Ω-cm^2.

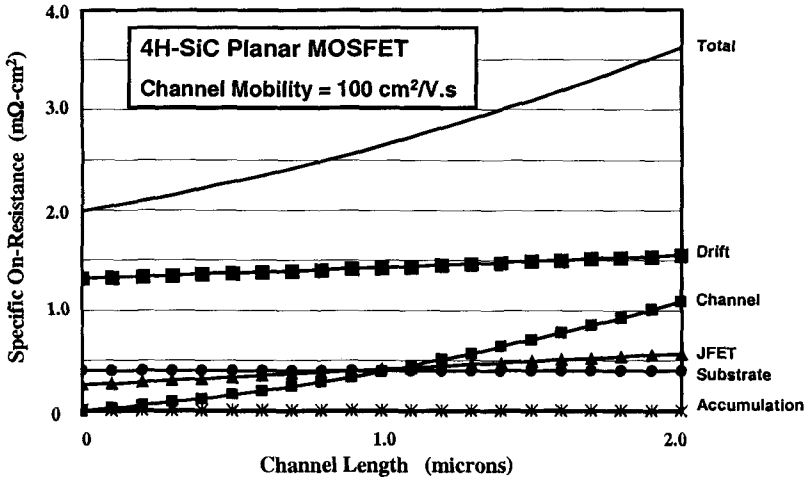

Fig. 9.5 On-Resistance Components for a 4H-SiC Planar MOSFET.

The specific on-resistances of 4H-SiC planar MOSFETs with a drift region doping concentration of 1×10^{16} cm^{-3} and thickness of 20 microns were modeled using the above analytical expressions. In all the devices, a gate oxide thickness of 0.1 microns was used. The dimension 'a' in the structure shown in Fig. 9.4 was kept at 1 micron. This value can be achieved using 0.5 micron design rules. The accumulation mobility was assumed to be twice the inversion layer mobility and a K-factor of 0.1 was used to provide correlation with the simulations. The P-

base was assumed to have a depth of 1 micron and the effective gate drive voltage ($V_G - V_T$) was assumed to be 20 volts. The various components of the on-resistance are shown in Fig. 9.5 when a channel inversion layer mobility of 100 cm^2/Vs was used. This magnitude of inversion layer mobility has been experimentally observed[8]. It can be seen that the drift region resistance is dominant under these conditions even for channel lengths of 2 microns. At a channel length of 1 micron, a total specific on-resistance of 2.7 $m\Omega\text{-}cm^2$ is obtained, which is about three times the ideal specific on-resistance. Although this is a good value for a device with the drift regions parameters used for the modeling, the breakdown voltage of the structure was determined to be well below its ideal parallel-plane case (3000 volts), as shown later under device simulations, due to the reach-through problem.

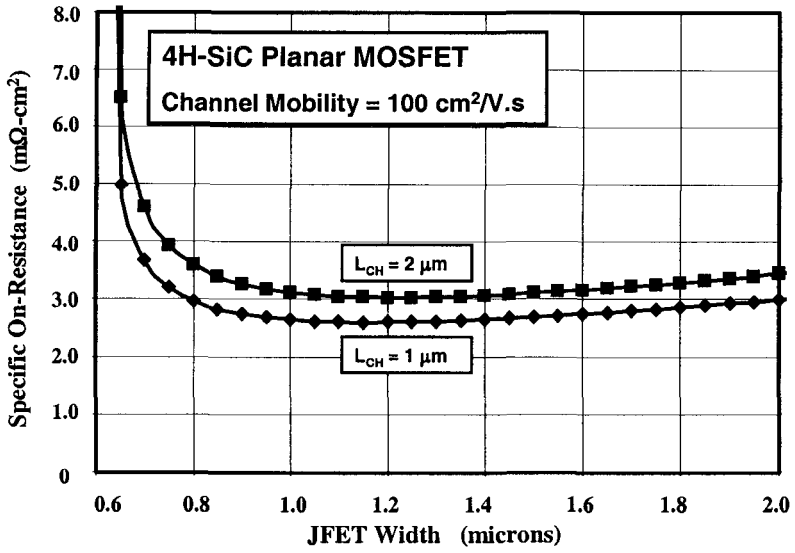

Fig. 9.6 Impact of JFET Width on the On-Resistance for a 4H-SiC Planar MOSFET.

The JFET width in the planar MOSFET structure must be optimized not only to obtain the lowest specific on-resistance but to also control the electric field at the gate oxide interface. The impact of changes to the JFET width on the specific on-resistance is shown in Fig. 9.6 for a structure with the same cell parameters that were given above. It can be observed that the specific on-resistance becomes very large when the JFET width is made smaller than about 0.7 microns. This occurs

because the zero bias depletion width for 4H-SiC P-N junctions is about 0.6 microns. When the JFET width approaches this value, the current becomes severely constricted resulting in a high specific on-resistance. As the JFET width is increased, the contribution from its resistance decreases rapidly. However, the increase in cell pitch enhances the specific resistance contributions from the channel resulting in an increase in the total specific on-resistance. A minimum specific on-resistance is observed to occur at a JFET width of about 1 micron.

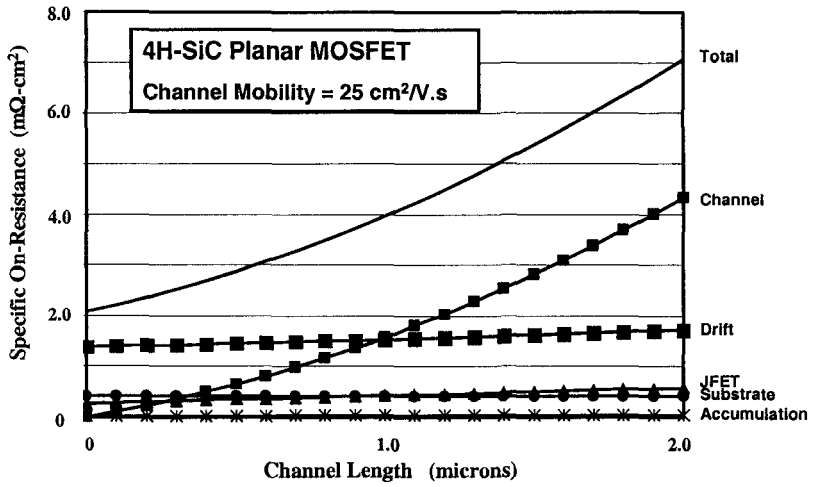

Fig. 9.7 On-Resistance Components for a 4H-SiC Planar MOSFET.

The above results are based upon using a channel mobility of 100 cm^2/Vs. However, most groups working on silicon carbide have reported much lower magnitudes for the inversion layer mobility in 4H-SiC structures[9]. Taking this into consideration, it is interesting to examine the impact of reducing the inversion layer mobility as depicted in Fig. 9.7 and 9.8 for the case of mobility values of 25 and 2.5 cm^2/Vs. With an inversion layer mobility of 25 cm^2/Vs, the channel contribution becomes comparable to the contribution from the drift region. This results in approximately doubling of the specific on-resistance to a value of 4 $m\Omega\text{-}cm^2$ for a channel length of 1 micron. When the inversion layer mobility is reduced to 2.5 cm^2/Vs, the channel resistance becomes dominant as shown in Fig. 9.8, with an increase in the specific on-resistance to a value of 18 $m\Omega\text{-}cm^2$ for a channel length of 1 micron.

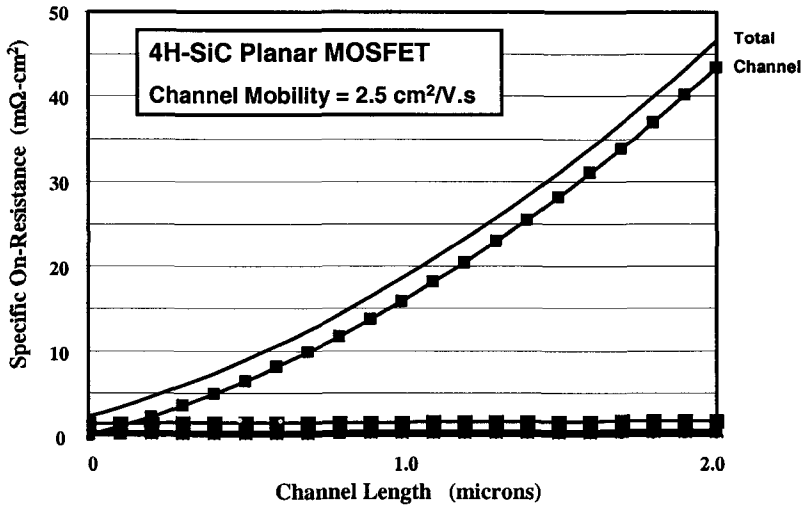

Fig. 9.8 On-Resistance Components for a 4H-SiC Planar MOSFET.

From the above discussion, it is obvious that the inversion layer mobility in the channel of the planar MOSFET has a significant impact on the specific on-resistance of the device. The relative magnitude of the channel mobility on the performance of the planar MOSFET depends upon the drift region resistance which is a function of the breakdown voltage of the device. In order to provide a better understanding of this, consider a 4H-SiC planar MOSFET with a JFET region whose doping concentration is held at 1 x 10^{16} cm^{-3} while the properties of the underlying drift region are adjusted to obtain the desired breakdown voltage. This approach for designing planar MOSFETs with enhanced doping in the JFET region is common practice in silicon technology[2]. The other cell parameters are maintained at the following values: parameter 'a' of 1 micron, P-base depth of 1 micron, gate oxide thickness of 0.1 microns, and channel length of 1 micron.

The specific on-resistance for the planar 4H-SiC MOSFETs is plotted in Fig. 9.9 as a function of the breakdown voltage for several cases of channel mobility. In performing this modeling, it is important to recognize that the thickness of the drift region (parameter 't' in Fig. 9.4) can become smaller than the cell parameter 's' at lower breakdown voltages (below 700 volts). Under these conditions, the current does not distribute at a 45 degree angle into the drift region from the JFET region.

Instead, the current flows from a cross-sectional width of ($W_J - W_P$) to a cross-section of ($t + W_J - W_P$). The drift region resistance for these cases can be modeled using:

$$R_D = \rho_D . p . \ln\left(\frac{t + W_J - W_P}{W_J - W_P}\right) \qquad [9.12]$$

In addition, the resistance contributed by the JFET region should be modeled using:

$$R_{JFET} = \rho_{JFET} . t_P \left(\frac{p}{W_J - W_P}\right) \qquad [9.13]$$

where ρ_{JFET} is the resistivity of the JFET region, which is different from the resistivity of the underlying drift region.

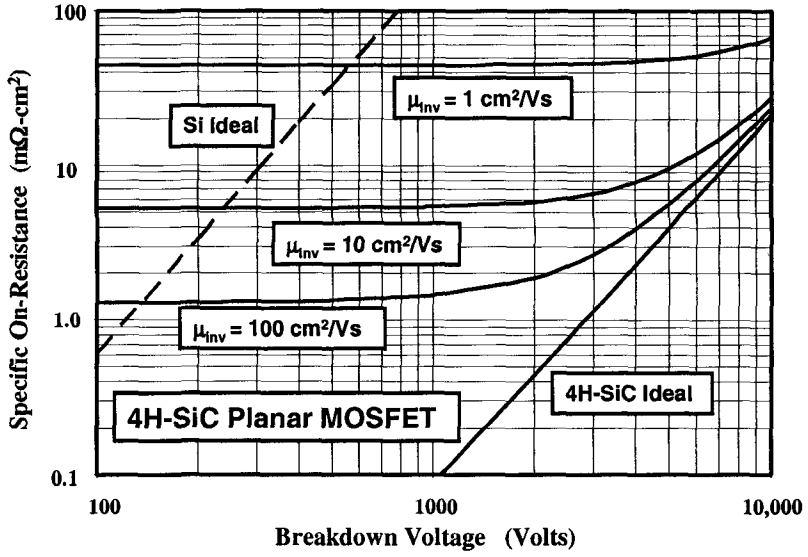

Fig. 9.9 Specific On-Resistance for 4H-SiC Planar MOSFETs.

From Fig. 9.9, it can be seen that the specific on-resistance of 4H-SiC planar MOSFETs approaches the ideal specific on-resistance when the breakdown voltage exceeds 5000 volts if a channel mobility of 100 cm^2/Vs is achieved. Even at this relatively high inversion layer

mobility for silicon carbide, the channel resistance limits the performance of the planar MOSFET when the breakdown voltage falls below 1000 volts. For a breakdown voltage of 1000 volts, the anticipated improvement in specific on-resistance over silicon devices is then about 100 times (as opposed to the 2000x improvement in the specific on-resistance of the drift region). When the inversion layer mobility is reduced to 10 cm^2/Vs, the degradation in performance extends to much larger breakdown voltages. This highlights the importance of developing process technology to achieve high inversion layer mobility in 4H-SiC structures. In comparison with silicon, whose ideal specific on-resistance is shown by the dashed line in Fig. 9.9, the 4H-SiC planar MOSFET can surpass the performance by an order of magnitude at breakdown voltages above 1000 volts if a channel mobility of at least 10 cm^2/Vs is obtained.

9.1.3 Planar Power MOSFET Structure: Threshold Voltage

The threshold voltage of the power MOSFET is an important design parameter from an application stand-point. A minimum threshold voltage must be maintained at above 1 volt for most system applications to provide immunity against inadvertent turn-on due to voltage spikes arising from noise. At the same time, a high threshold voltage is not desirable because the voltage available for creating the charge in the channel inversion layer is determined by $(V_G - V_T)$ where V_G is the applied gate bias voltage and V_T is the threshold voltage. Most power electronic systems designed for high voltage operation (the most suitable application area for silicon carbide devices) provide a gate drive voltage of only upto 10 volts. Based upon this criterion, the threshold voltage should be kept below 3 volts in order to obtain a low channel resistance contribution.

The threshold voltage can be modeled by defining it as the gate bias at which on-set of *strong inversion* begins to occur in the channel. This voltage can be determined using[10]:

$$V_{TH} = \frac{\sqrt{4\varepsilon_S kTN_A \ln(N_A / n_i)}}{C_{ox}} + \frac{2kT}{q}\ln\left(\frac{N_A}{n_i}\right) \qquad [9.14]$$

where N_A is the doping concentration of the P-base region, k is Boltzmann's constant, and T is the absolute temperature. The presence of positive fixed oxide charge shifts the threshold voltage in the negative direction by:

$$\Delta V_{TH} = \frac{Q_F}{C_{ox}} \qquad [9.15]$$

A further shift of the threshold voltage in the negative direction by 1 volt can be achieved by using heavily doped N-type polysilicon as the gate electrode as routinely done for silicon power MOSFETs.

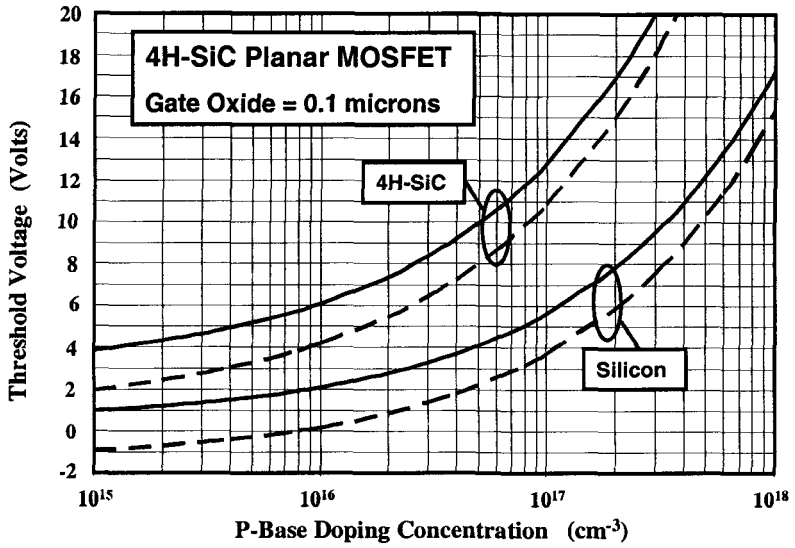

Fig. 9.10 Threshold Voltage of 4H-SiC Planar MOSFETs.

(Dashed lines include the impact of N^+ Polysilicon Gate and an Oxide Fixed Charge of 2×10^{11} cm^{-2})

The analytically calculated threshold voltage for 4H-SiC planar MOSFETs is shown in Fig. 9.10 for the case of a gate oxide thickness of 0.1 microns. The results obtained for a silicon power MOSFET with the same gate oxide thickness is also provided in this figure for comparison. In the case of silicon devices, a threshold voltage of about 3 volts is obtained for a P-base doping concentration of 1×10^{17} cm^{-3}. At this doping concentration, the depletion width in the P-base region for silicon devices is less than 0.5 microns, as shown earlier in Fig. 9.3, even when the electric field in the semiconductor approaches the critical electric field for breakdown. This allows the design of silicon power MOSFETs with channel lengths of below 0.5 microns without encountering reach-

through breakdown limitations. In contrast, a P-base doping concentration of about 3 x 10^{17} cm^{-3} is required in 4H-SiC (see Fig. 9.3) to keep the depletion width in the P-base region below 1 micron when the electric field in the semiconductor approaches the critical electric field for breakdown. At this doping concentration, the threshold voltage for the 4H-SiC MOSFET approaches 20 volts. The much larger threshold voltage for silicon carbide is physically related to its larger band gap as well as the higher P-base doping concentration required to suppress reach-through breakdown. This indicates a fundamental problem for achieving reasonable levels of threshold voltage in silicon carbide power MOSFETs if the conventional silicon structure is utilized. Innovative structures that shield the P-base region[7] can overcome this limitation as discussed in the next chapter.

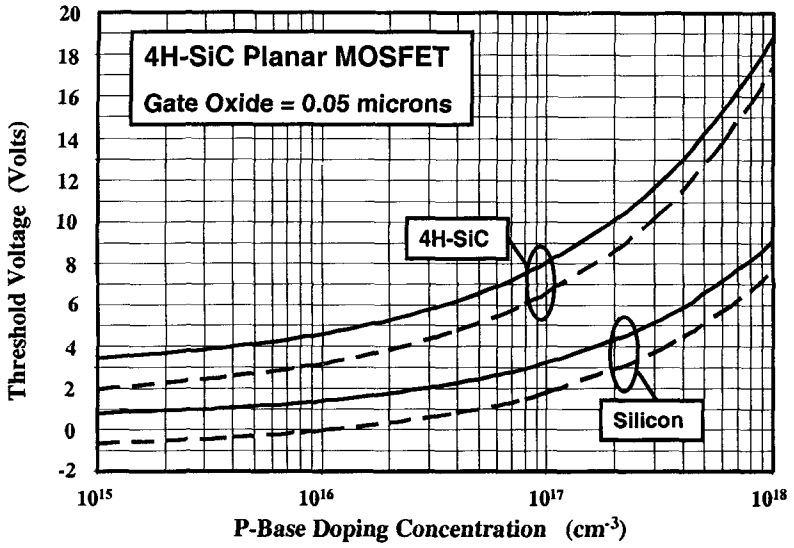

Fig. 9.11 Threshold Voltage of 4H-SiC Planar MOSFETs.

(Dashed lines include the impact of N^+ Polysilicon Gate and an Oxide Fixed Charge of 2 x 10^{11} cm^{-2})

The threshold voltage for a MOSFET can be reduced by decreasing the gate oxide thickness. If the gate oxide thickness is reduced to 0.05 microns, the threshold voltage for the silicon power MOSFET decreases to just below 2 volts as shown in Fig. 9.11. This is common practice for the design of low voltage silicon power MOSFETs that are

often driven with logic-level (5 volt) gate signals. In the case of the 4H-SiC MOSFET, the threshold voltage is reduced to 10 volts which is still too large from an applications stand-point. A further reduction of the threshold voltage is obtained by reducing the gate oxide thickness to 0.025 microns as shown in Fig. 9.12. For this gate oxide thickness, the threshold voltage for the silicon MOSFET drops below 1 volt indicating the need to increase the P-base doping concentration to 2 x 10^{17} cm^{-3}. For the case of 4H-SiC MOSFETs, a threshold voltage now becomes about 6 volts which is marginally acceptable. However, operation of very high voltage power MOSFETs with such thin gate oxides may create manufacturing and reliability issues when taking into account the high electric fields under the gate oxide in the semiconductor.

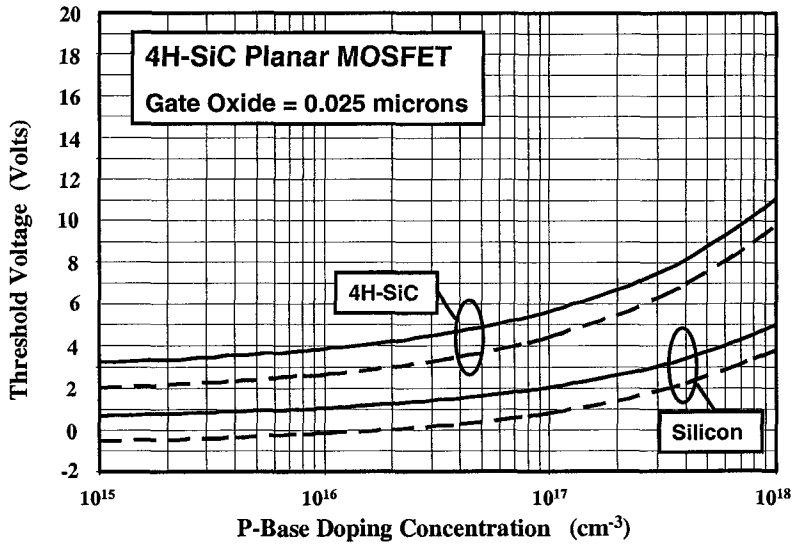

Fig. 9.12 Threshold Voltage of 4H-SiC Planar MOSFETs.

(Dashed lines include the impact of N^+ Polysilicon Gate and an Oxide Fixed Charge of 2 x 10^{11} cm^{-2})

The threshold voltage of power MOSFETs decreases with increasing temperature. This variation is shown in Fig. 9.13 for the case of 4H-SiC and silicon MOSFETs using a gate oxide thickness of 0.025 microns. It can be seen that there is a relatively small shift in the

threshold voltage with temperature. Consequently, this effect is not an important consideration during the design of 4H-SiC power MOSFETs.

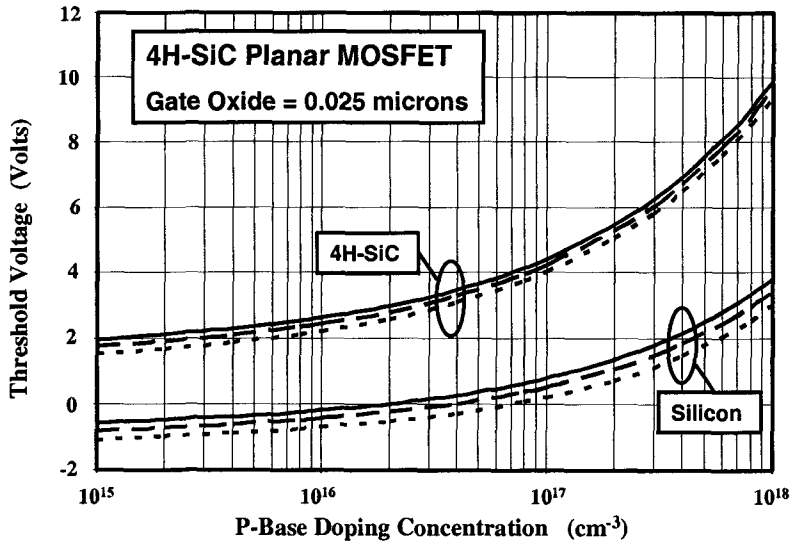

Fig. 9.13 Threshold Voltage of 4H-SiC Planar MOSFETs.
(Solid Line: 300 °K; Dashed Line: 400 °K; Dotted Line: 500 °K)

9.1.4 Planar MOSFET Structure: Threshold Voltage Simulations

In order to verify the predictions of the model for the threshold voltage for silicon carbide MOSFETs that was described in the previous section, two-dimensional numerical simulations were performed for a lateral MOSFET structure. This structure was designed with a long channel (10 microns) and uniform P-base doping concentration, as shown in Fig. 9.14, to allow extraction of the threshold voltage and the channel inversion layer mobility. Simulations performed with this structure using different P-base doping concentrations and gate oxide thickness values enables extraction of the dependence of the threshold voltage on these parameters.

The transfer characteristics obtained for the case of a gate oxide thickness of 0.05 microns, are shown in Fig. 9.15, for various P-base doping concentrations. The threshold voltage for various P-base doping concentrations was extracted by using a drain current level indicated by

the dashed line in the figure. The extracted threshold voltage is compared with the predictions of the analytical model in Fig. 9.16.

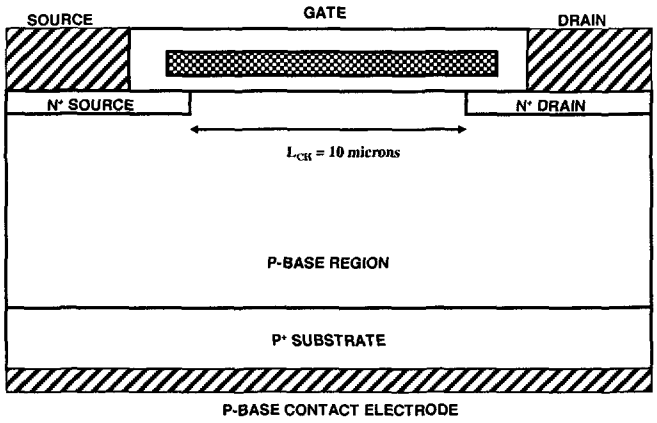

Fig. 9.14 The Planar Lateral 4H-SiC MOSFET Structure.

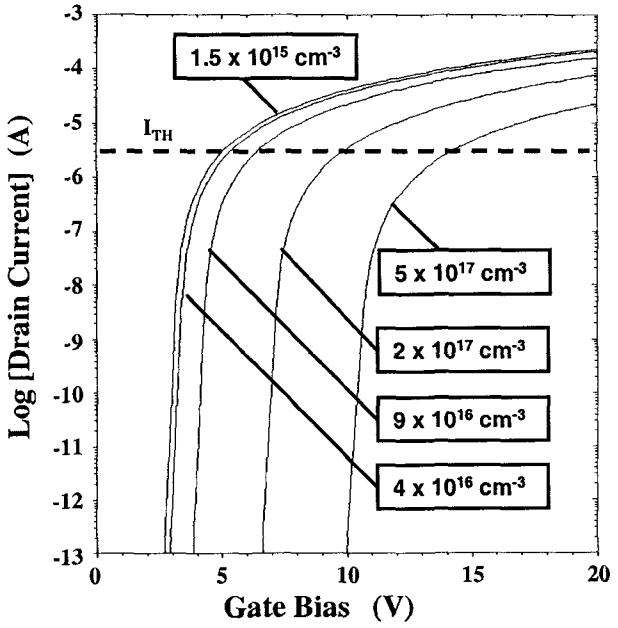

Fig. 9.15 Transfer Characteristics of the Planar Lateral 4H-SiC MOSFET Structure.

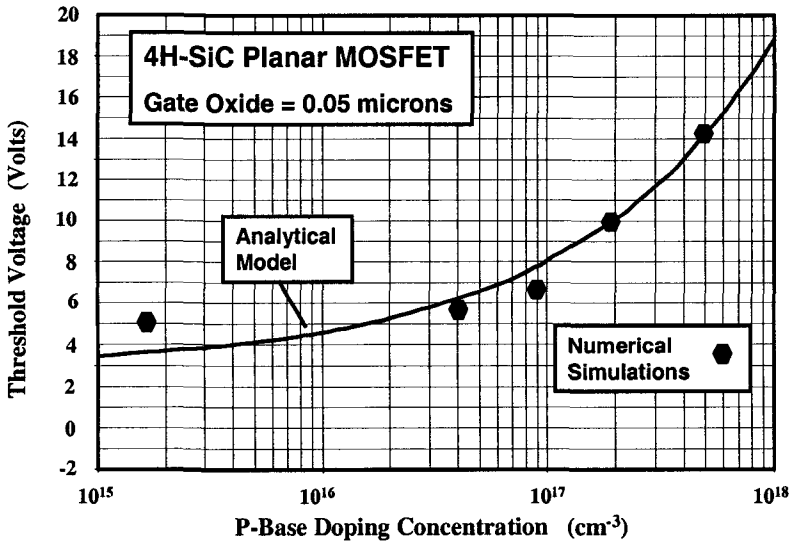

Fig. 9.16 Threshold Voltage of 4H-SiC Planar MOSFETs.

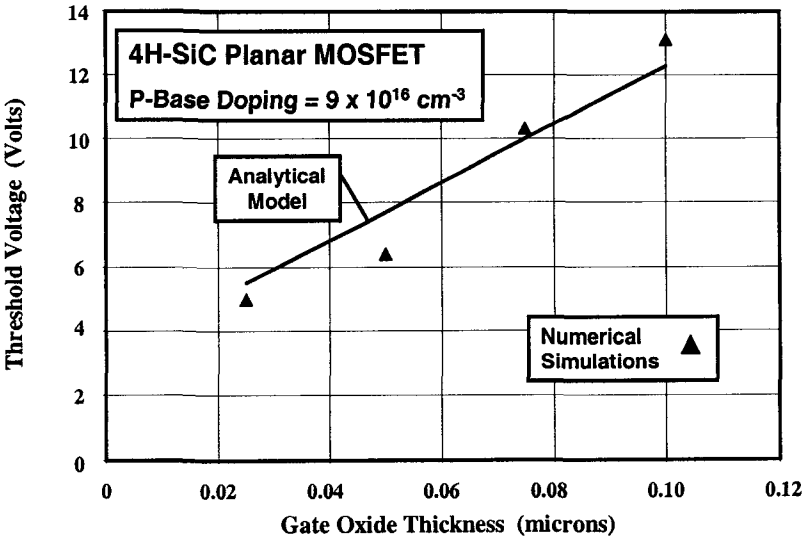

Fig. 9.17 Threshold Voltage of 4H-SiC Planar MOSFETs.

From Fig. 9.16, it can be seen that there is an excellent agreement between the threshold voltages predicted by the analytical model and the numerical simulations over a broad range of P-base doping concentrations. Note that no adjustment was made for the work function of the gate electrode or fixed oxide charge in both the simulations and in the analytical model. Numerical simulation of the lateral 4H-SiC MOSFET were also performed with various gate oxide thicknesses while maintaining a P-base doping concentration of 9 x 10^{16} cm^{-3}. The results of the threshold voltage extracted from these simulations are compared with those obtained using the analytical model in Fig. 9.17. Once again, the predictions of the analytical model are in good agreement with the simulations indicating that this model can be utilized for the design of silicon carbide MOSFETs.

9.1.5 Silicon Carbide MOSFET Structure: Hot Electron Injection

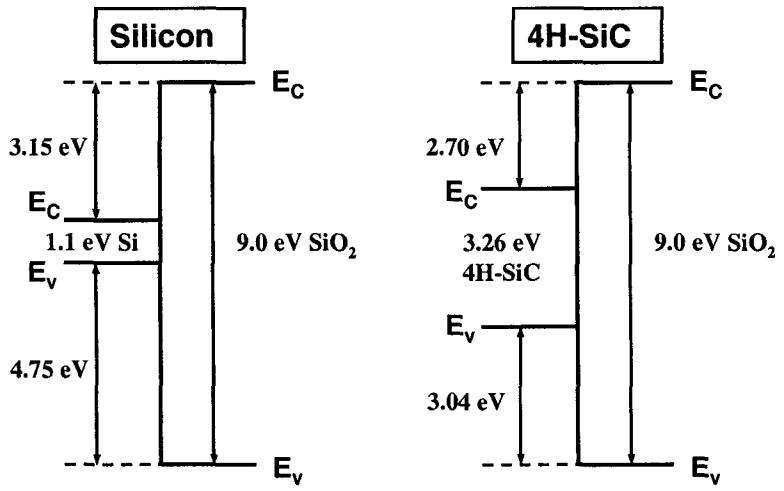

Fig. 9.18 Energy Band Offsets between Oxide and Semiconductors.

In any MOSFET structure, the injection of electrons into the gate oxide can occur when the electrons gain sufficient energy in the semiconductor to surmount the potential barrier between the semiconductor and the oxide. The energy band offsets between the semiconductor and silicon dioxide are shown in Fig. 9.18 for silicon and 4H-SiC for comparison purposes. Due to the larger band gap of 4H-SiC, the band offset between

the conduction band edges for the semiconductor and silicon dioxide is significantly smaller than for the case of silicon.

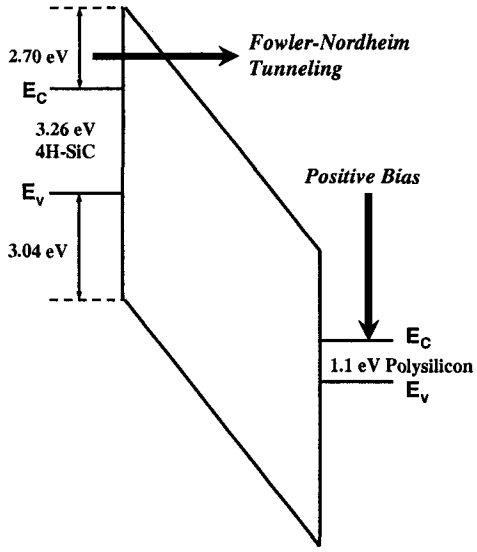

Fig. 9.19 Energy Band Diagram for the Polysilicon/Oxide/4H-SiC Structure.

The band diagram for the 4H-SiC silicon dioxide interface is shown in Fig. 9.19 when a positive bias is applied to the gate. This bias condition is typical for the on-state mode of operation in power MOSFETs. In this illustration, the gate was assumed to be formed using polysilicon. It can be seen that a narrow barrier is formed at the semiconductor-oxide interface which can be penetrated by the tunneling of electrons from the conduction band into the oxide. This produces a Fowler-Nordheim tunneling current that injects electrons into the oxide. This current has been observed in measurements reported on both 6H-SiC[11] and 4H-SiC[12] MOS-capacitors. The trapping of these electrons within the gate oxide can cause shifts in the threshold voltage of the MOSFET leading to reliability problems.

9.2 Planar Power MOSFET Structure: Numerical Simulations

In order to gain insight into the operation of the planar 4H-SiC power MOSFET structure, two-dimensional numerical simulations were

performed with a drift region doping concentration of 1 x 10^{16} cm^{-3} and thickness of 20 microns corresponding to a parallel-plane breakdown voltage of 3000 volts. The baseline device had a gate oxide thickness of 0.1 microns, which is typical for devices that have been fabricated and reported in the literature. The P-base region had a depth of 1 micron for all the structures with a doping concentration of 9 x 10^{16} cm^{-3}. The JFET width for the baseline device was 1 micron.

9.2.1 Planar Power MOSFET Structure: Blocking Characteristics

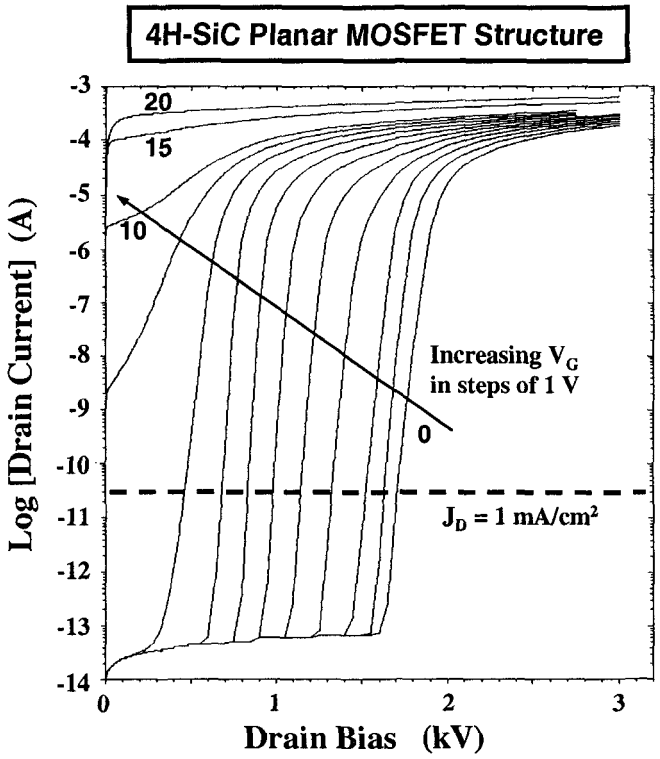

Fig. 9.20 Blocking Characteristics of the Planar 4H-SiC MOSFET Structure.

The blocking capability of the planar 4H-SiC power MOSFET was investigated by maintaining zero gate bias while increasing the drain voltage. It was found that the drain current begins to flow at a drain bias of about 1600 volts and then increases at an exponential rate as shown in

Fig. 9.20. In this figure, the drain current is also shown when various positive gate bias voltages are applied to the planar 4H-SiC power MOSFET structure. The exponential increase in the drain current with increasing drain bias voltage occurs for gate bias voltages of upto 8 volts. Thus, the exponential current-voltage relationship holds true as long as the gate bias is below the threshold voltage for the device. (The threshold voltage for this structure is about 10 volts as shown later in this section.) This behavior is associated with current flow due to the reach-through phenomenon.

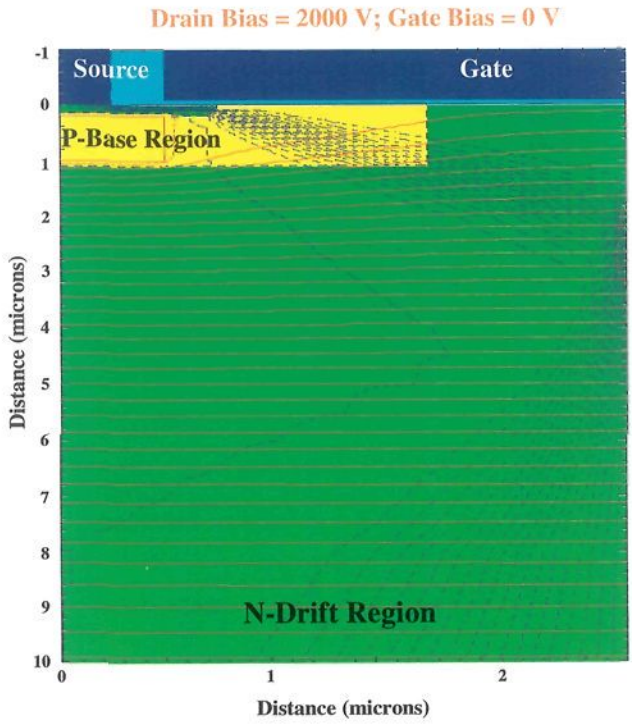

Fig. 9.21 Reach-Through Phenomenon in the Planar 4H-SiC Power MOSFET.

Reach-through breakdown in the planar 4H-SiC power MOSFET is induced when the depletion region extends through the P-base region. In order to illustrate this effect, the potential and current distributions within the planar 4H-SiC planar MOSFET structure are shown in Fig. 9.21 when a drain bias of 2000 volts is applied with zero gate bias. It can

be seen that the current flow (indicated by the dashed lines) occurs from the N^+ source region into the drift region through the P-base region. If the device had undergone breakdown due to impact ionization, the current flow would have occurred into the contact for the P-base region located on the left-hand edge of the structure and not through the N^+ source region.

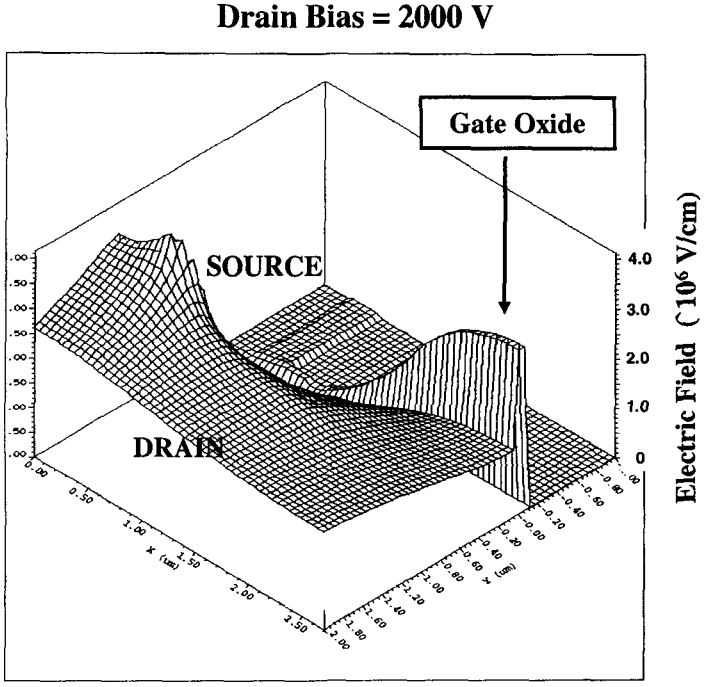

Fig. 9.22 Electric Field Distribution in the Planar 4H-SiC MOSFET Structure.

The above discussion illustrates one of the drawbacks of the planar power MOSFET structure when applied to silicon carbide. A second problem with this structure is associated with the high electric field generated at the gate oxide interface. This problem can be illustrated by examination of the electric field distribution within the planar 4H-SiC power MOSFET structure under voltage blocking conditions. A three-dimensional view of the electric field distribution is shown in Fig. 9.22 for a drain bias of 2000 volts including the portion of the structure containing the gate oxide. The field distribution shown in

this figure indicates that the electric field at the gate oxide is slightly suppressed by the presence of the JFET region. However, in spite of this field reduction, it can be seen that the electric field in the oxide has reached a magnitude of close to 3 x 10^6 V/cm. Such larger electric fields in the oxide can lead to reliability problems due to injection of hot electrons into the oxide.

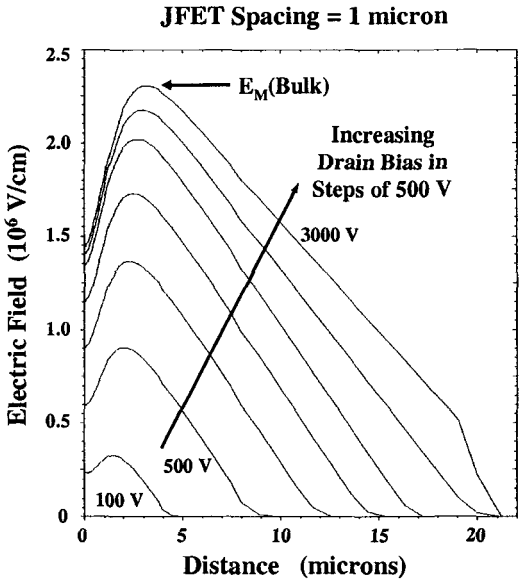

Fig. 9.23 Electric Field Distribution in the Planar 4H-SiC MOSFET Structure.

In the planar 4H-SiC power MOSFET structure, the largest electric field at the gate oxide interface occurs at the center of the JFET region. The behavior of this electric field with increasing drain bias is shown in Fig. 9.23 for the case of a JFET width of 1 micron. From this figure, it is apparent that there is some shielding of the gate oxide by the JFET region due to the formation of a potential barrier when this region becomes depleted at lower drain voltages. The maximum electric field occurs inside the semiconductor at a depth of about 3 microns. The electric field at the gate oxide interface is reduced to 60 percent of the bulk electric field. However, this is insufficient to keep the electric field in the gate oxide in the reliable operating regime. As previously discussed, the specific on-resistance for the planar MOSFET structure can be reduced by increasing the JFET width. However, the suppression

of the electric field at the gate oxide is almost completely lost when this is done as illustrated in Fig. 9.24 for the case of a JFET width of 3.3 microns.

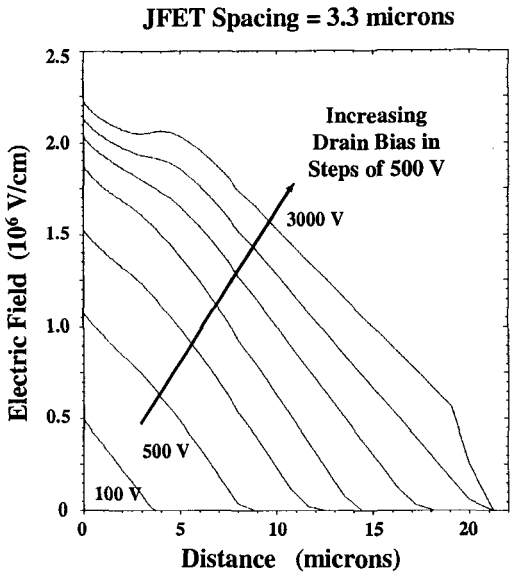

Fig. 9.24 Electric Field Distribution in the Planar 4H-SiC MOSFET Structure.

9.2.2 Planar Power MOSFET Structure: On-State Characteristics

The on-state voltage drop for the planar 4H-SiC power MOSFET structure is determined by its specific on-resistance. The on-resistance for the structure was extracted by performing numerical simulations with a gate bias of 20 volts. A relatively high gate bias was required because of the large threshold voltage of these devices as already discussed in previous sections of this chapter. As expected, the specific on-resistance was dependent upon the JFET region width and the channel inversion layer mobility.

The current distribution within the planar 4H-SiC power MOSFET structure is shown in Fig. 9.25 for the case of JFET widths of 1 and 8.3 microns. It can be seen that the current is constricted in the JFET region when its width is 1 micron. This phenomenon makes the JFET resistance contribution equal to the channel resistance contribution when the channel mobility is assumed to be 100 cm^2/Vs. When the JFET width

is increased, the JFET resistance decreases significantly and becomes a small fraction of the overall resistance of the device. However, the increase in cell pitch required to accommodate the larger JFET region produces an increase in the specific on-resistance of the structure. The current flow-lines shown in the lower part of Fig. 9.25 demonstrate that the current flow in the JFET region is occurring primarily near the edge of the channel. This justifies the use of a small value for the parameter 'K' in the analytical model for the accumulation region resistance.

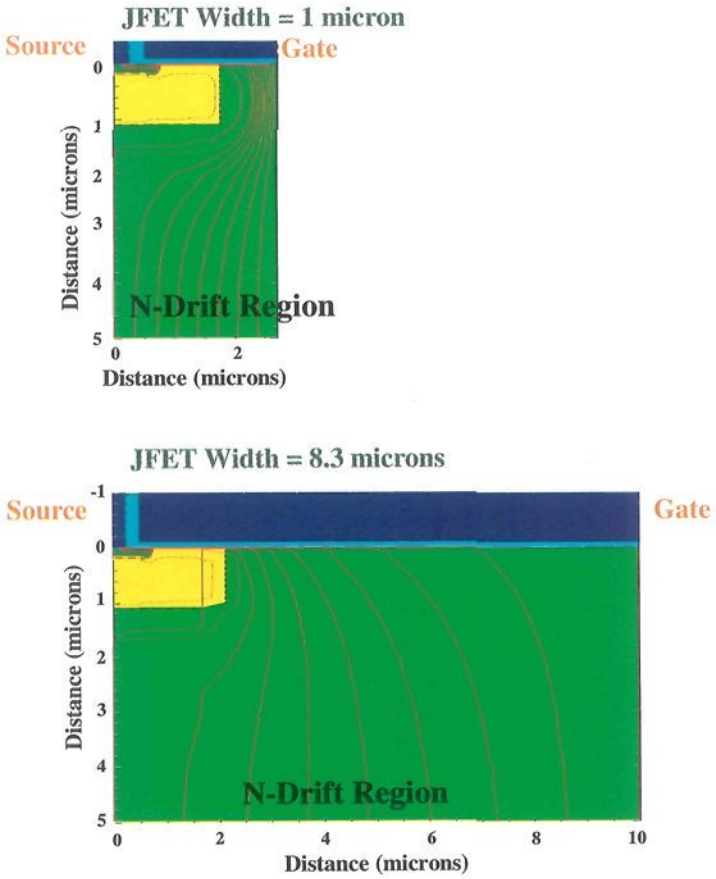

Fig. 9.25 On-State Current Distribution in the Planar 4H-SiC Power MOSFETs.

The simulations of the specific on-resistance were done for each of the structures with different values for the inversion layer mobility.

The specific on-resistance was obtained by using a drain bias of 1 volt and sweeping the gate bias to 20 volts to obtain the transfer characteristic. A drain bias of 1 volt was used for these simulations because the on-state voltage drop for these structures is typically in this range. A typical transfer characteristic obtained using this method is shown in Fig. 9.26 for the device with JFET width of 1 micron. From the transfer characteristics, it can be seen that the threshold voltage that determines the on-resistance is approximately 10 volts. This value is close to that calculated using the analytical model discussed in the previous section for the chosen P-base doping concentration of 9×10^{16} cm^{-3} and gate oxide thickness of 0.1 microns. The impact of changing the channel inversion layer mobility is also shown in this figure. As expected, there is a reduction in the drain current as the channel mobility is reduced.

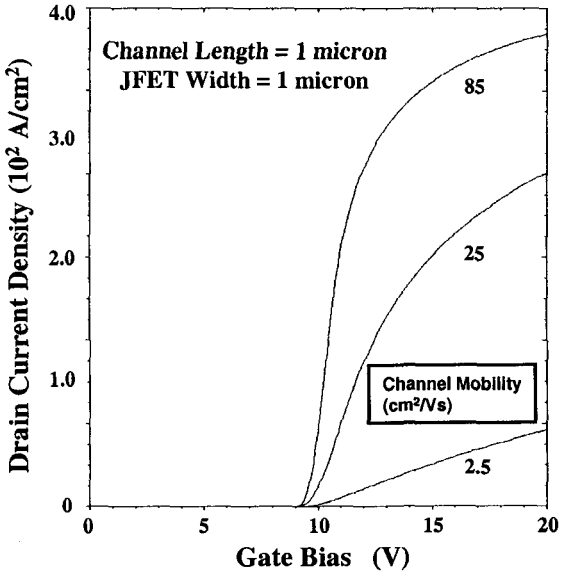

Fig. 9.26 Transfer Characteristics of the 4H-SiC Planar MOSFETs.

The specific on-resistances obtained from the on-state simulations are compared in Fig. 9.27 with the analytically calculated values obtained by using the model developed in the previous section. Three cases of JFET region width have been taken into consideration.

For the simulation cases, the channel mobility values were extracted from the *i-v* characteristics obtained for the lateral 4H-SiC MOSFET structure that was previously described (see Fig. 9.14) by using the same interface degradation factor as used during the simulation of the vertical 4H-SiC planar MOSFET structure. It can be seen that the predictions of the analytical model are in excellent agreement with the values obtained from the simulations in all cases. These results provide confidence in the ability to use the analytical model during the design of the planar 4H-SiC power MOSFET structure. From the figure, it can be concluded that a channel mobility of more than 50 cm^2/Vs is satisfactory for achieving a low specific on-resistance for a 2 kV planar 4H-SiC power MOSFET structure with JFET width of 1 micron. In addition, it can be concluded that there is no benefit to increasing the JFET width beyond 1 micron.

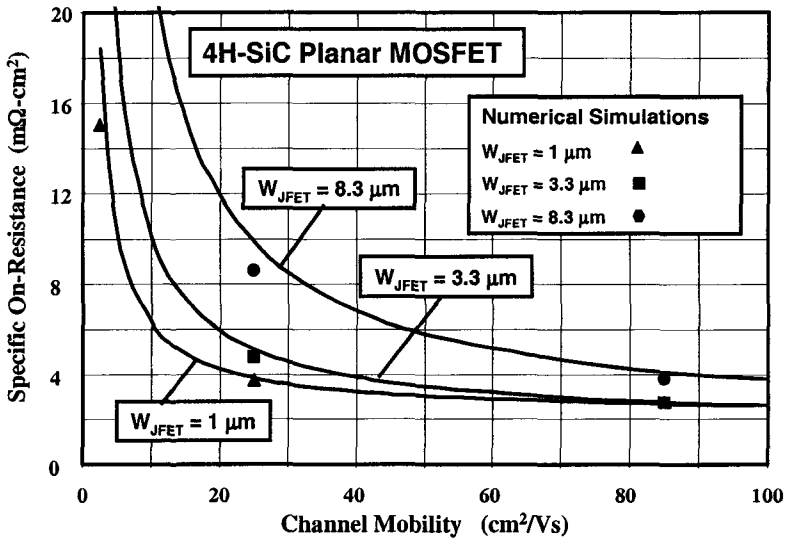

Fig. 9.27 Specific On-Resistance for the 4H-SiC Planar MOSFETs.

9.2.3 Planar Power MOSFET Structure: Output Characteristics

The output characteristics of the power MOSFET defines the region within which the device can operate during the switching transients in applications. The current-voltage loci during the transient must be chosen to remain within the boundary defined by the output characteristics. For a power MOSFET, one of the boundaries is defined by the on-resistance

and a second one by its breakdown voltage. These boundaries limit the maximum on-state current that can be tolerated by the device after taking into consideration the thermal impedance of the package and the maximum off-state voltage that can be impressed upon the device without excessive power dissipation due to leakage current. The gate controlled current saturation in power MOSFETs defines its third boundary. Here, the magnitude of the output resistance becomes important with a larger value preferred for providing greater control over the drain current by the applied gate bias voltage.

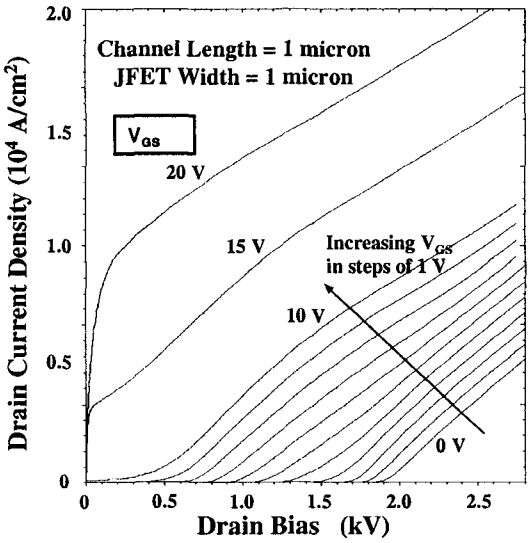

Fig. 9.28 Output Characteristics of a 4H-SiC Planar MOSFET.

The output characteristics for the 4H-SiC planar power MOSFET were analyzed by biasing the gate at various values and sweeping the drain voltage upto 2800 volts. The characteristics obtained for the structure with JFET width of 1 micron are shown in Fig. 9.28. It can be observed that significant current flow occurs when the drain bias exceeds 1900 volts for a zero gate bias voltage. This current flow is due to the reach-through breakdown problem discussed in the previous sections. The reach-through current also degrades the output resistance of the device at all positive gate bias voltages. Even further degradation of the output resistance and reduction of the maximum blocking voltage is

observed when the JFET width is increased as shown in Fig. 9.29. Consequently, the output characteristics observed for the 4H-SiC planar MOSFET structure are poor when compared with those described for the Baliga-Pair configuration in the previous chapter.

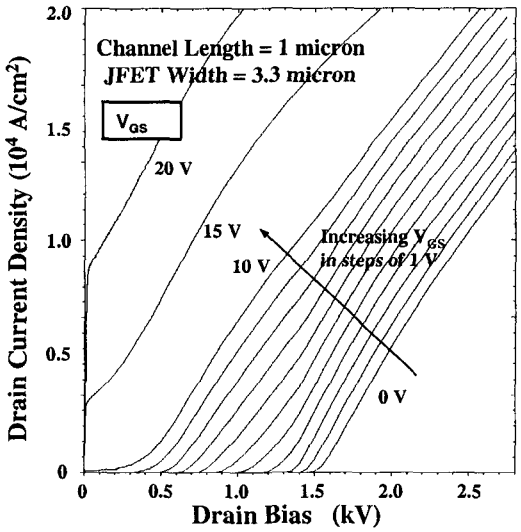

Fig. 9.29 Output Characteristics of a 4H-SiC Planar MOSFET.

9.3 Planar Power MOSFET: Experimental Results

The need to obtain a high quality interface between silicon carbide and the gate dielectric was identified as a challenging endeavor from the inception of interest in the development of unipolar transistors from this semiconductor material[13]. Initially, it was impossible to fabricate silicon carbide power MOSFETs with specific on-resistances below those reported for silicon devices until the interface was sufficiently improved to obtain adequate inversion layer mobility. Further, early work on planar MOSFETs did not sufficiently take into consideration the fundamental issues that have been discussed in the previous sections of this chapter dealing with the reach-through problem and the high electric field in the oxide. These issues are discussed here in the historical context of developing silicon carbide planar power MOSFET structures.

9.3.1 Silicon Carbide MOSFET: Inversion Layer Mobility

Early investigations of the interface between P-type silicon carbide and thermally grown oxide indicated a high density of interface states and positive charge in the oxide. Significant improvement in the interface quality was achieved for 6H-SiC by anneal the thermally grown oxide in a NO ambient[14] leading to a peak inversion layer mobility of 70 cm^2/Vs. However, the inversion layer mobility for 4H-SiC was reported[15] to be less than 1 cm^2/Vs.

In 1998, a break-through was achieved at PSRC[16] with the use of deposited oxides on 4H-SiC leading to a reported[17] record high inversion layer mobility of 165 cm^2/Vs. A detailed study[18] of the process steps responsible for producing the improved interface resulting in the high channel mobility was also undertaken at PSRC. This work produced the first observation of phonon scattering limited inversion layer mobility (which decreased with increasing temperature), and demonstrated that a wet oxide anneal of the deposited oxide was the critical step for producing the high inversion layer mobility. The process proposed and demonstrated at PSRC was subsequently reproduced by the sponsors[19] as well by other research groups[20]. These results indicate that it is possible to achieve sufficiently high inversion layer mobility in 4H-SiC power MOSFETs to obtain low specific on-resistance in high voltage structures.

The low inversion layer mobility observed in 4H-SiC MOSFETs fabricated using thermally grown gate oxides has been traced to the trapping of the carriers at interface states. Hall effect measurements performed on lateral MOSFETs have demonstrated that the effective Hall mobility for carriers in the inversion layer is high when the trapping effect is taken into consideration[21]. Due to the trapping effect, as recently as 2001, the measured effective mobility in 4H-SiC MOSFETs has been reported[22] to be less than 10 cm^2/V-s when thermal oxidation is used to form the gate oxide. In these devices, the effective mobility was found to increase with temperature which is a signature of trap dominated current conduction in the channel. By using NO ambient anneals of the thermally grown gate oxide, an improvement in the effective channel mobility to 30-35 cm^2/V-s was reported[23] in 2001.

In conclusion, process technology has been demonstrated to obtain sufficiently high inversion layer mobility on the surface of P-type 4H-SiC by using deposited silicon dioxide films. The quality of interface between thermally grown oxide and 4H-SiC remains inferior with significant progress being made towards its improvement.

9.3.2 The 4H-SiC Planar MOSFET: Experimental Results

As already mentioned earlier in the chapter, in recognition of the low diffusion coefficients for dopants in silicon carbide, it was proposed[5] that the P-base and N^+ source ion implantations for the planar silicon carbide power MOSFET be staggered by using photoresist masks rather that be defined by the gate edge as conventionally done for silicon devices. This idea was first successfully demonstrated[6] for 6H-SiC devices in 1997 under the DI-MOSFET moniker. The authors fabricated the devices using multiple energy boron implants to form a P-base region with a box profile at a depth of 1 micron. Devices were designed with channel length of 2 and 5 microns, and the JFET region width (W_J in Fig. 9.4) was varied from 2.5 to 15 microns. The channel inversion layer mobility was found to be about 20 cm^2/Vs for these 6H-SiC MOSFETs fabricated using a thermally grown oxide. The best specific on-resistance of 130 $m\Omega\text{-}cm^2$ was obtained for the smallest JFET width and channel length. The breakdown voltage of the device was found to be 760 volts as limited by reach-through as well as gate oxide rupture leading to catastrophic failure.

The DI-MOSFET structure was fabricated[9] from 4H-SiC more recently by using 25 micron thick epitaxial layers with doping concentration of $3 \times 10^{15}\ cm^{-3}$. In spite of using the previously discussed deposited oxide process[8], an inversion layer mobility of only 14 cm^2/Vs was observed. Due to the low channel mobility, the devices exhibited a relatively large specific on-resistance of 55 $m\Omega\text{-}cm^2$ even when a high gate bias of 25 volts was applied. The device was able to support nearly 2000 volts at zero gate bias. The authors associated the blocking voltage to be limited by open-base bipolar breakdown, namely, the reach-through problem discussed earlier in this chapter. This work was extended[24] to achieve a breakdown voltage of 2400 volts with a specific on-resistance of 42 $m\Omega\text{-}cm^2$ in large area (0.1 cm^2) device structures; as well as devices[25] with a breakdown voltage of 10 kV with a specific on-resistance of 236 $m\Omega\text{-}cm^2$.

9.4 Summary

The extension of the silicon power DMOSFET architecture to silicon carbide has been critically examined in this chapter. It has been shown

that the direct applicability of the structure to silicon carbide is hindered by the following issues:

(a) The lack of any significant diffusion of impurities in silicon carbide requires the staggering of the P-base and N^+ source ion implants with photoresist masking layers, which limits the minimum achievable channel length;

(b) The higher threshold voltage for silicon carbide when compared with silicon for the same doping concentration exacerbates the reach-through problem within the P-base region limiting the blocking voltage capability;

(c) The higher threshold voltage for silicon carbide MOSFETs increases the specific on-resistance due to the enhanced channel contribution;

(d) A high electric field develops at the gate oxide that can lead to catastrophic failure of the silicon carbide device well before the electric field in the semiconductor can reach the critical electric field for breakdown;

(e) The poor inversion layer mobility obtained with thermally grown oxide can limit the specific on-resistance to well above the capability of the drift region.

These limitations of the conventional DMOSFET structure can be overcome by shielding the P-base region as discussed in the next chapter.

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Chapter 10

Shielded Planar MOSFETs

In the previous chapter, it was demonstrated that the conventional silicon planar power DMOSFET structure is not satisfactory for utilization in silicon carbide due to a reach-through problem, a relatively high threshold voltage, a high electric field developed in the gate oxide, and the relatively low inversion layer mobility in the channel. All of these issues can be addressed in a satisfactory manner by shielding the channel from the high electric field developed in the drift region. The concept of shielding of the channel region was first proposed[1] at PSRC in the early 1990's with a U.S. patent issued in 1996. The shielding was accomplished by formation of either a P-type region under the channel or by creating a high resistivity conduction barrier region under the channel. The issue of low inversion layer channel mobility was addressed by utilizing an accumulation mode of operation. As discussed in this chapter, the accumulation mode is also attractive from the point of view of reducing the threshold voltage so as to enhance the channel conductivity.

This chapter begins with a review of the basic principles of operation of the shielded planar MOSFET structure. The impact of shielding on ameliorating the reach-through breakdown in silicon carbide is described. This shielding approach has more recently been used very effectively for improvement of even silicon low voltage planar power MOSFETs[2]. Based upon fundamental considerations, the difference between the threshold voltage for inversion and accumulation mode silicon carbide structures is then analyzed. The results of the analysis of the planar silicon carbide MOSFET structures by using two-dimensional numerical simulations are described in this chapter. It is shown that the shielding concept enables reduction of the electric field developed in the gate oxide as well leading to the possibility to fully utilize the breakdown field strength of the underlying semiconductor drift region. Experimental results on relevant structures are discussed at the end of this chapter to

define the state of the development effort on these devices. The shielded accumulation-mode MOSFET structures (named the ACCUFET) discussed in this chapter have the most promising characteristics for the development of monolithic power switches from silicon carbide.

10.1 Shielded Planar MOSFET Structure

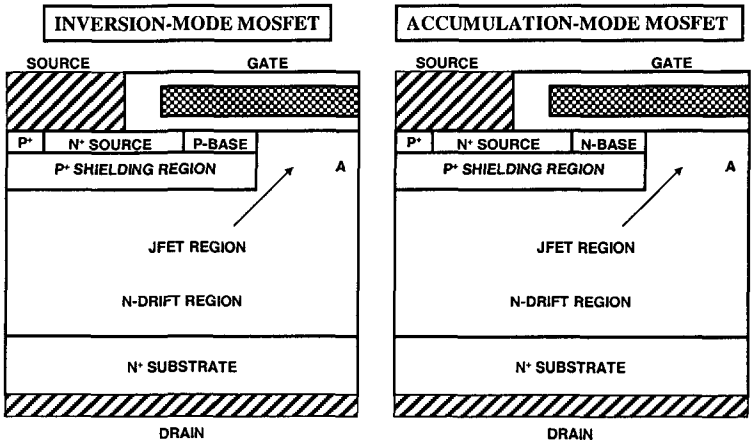

Fig. 10.1 Shielded Planar MOSFET Structures.

The basic structure of the shielded planar MOSFET is shown in Fig. 10.1 with either an inversion layer channel or an accumulation layer channel. In the case of the structure with the inversion layer channel, the P^+ shielding region extends under both the N^+ source region as well as under the P-base region. It could also extend beyond the edge of the P-base region. In the case of the structure with the accumulation layer channel, the P^+ shielding region extends under the N^+ source region and the N-base region located under the gate. This N-base region can be formed using an uncompensated portion of the N-type drift region or it can be created by adding N-type dopants with ion implantation to control its thickness and doping concentration.

The gap between the P^+ shielding regions is optimized to obtain a low specific on-resistance while simultaneously shielding the gate oxide interface from the high electric field in the drift region. In both structures shown above, a potential barrier is formed at location A after

the JFET region becomes depleted by the applied drain bias in the blocking mode. This barrier prevents the electric field from becoming large at the gate oxide interface. When a positive bias is applied to the gate electrode, an inversion layer or accumulation layer channel is formed in the structures enabling the conduction of drain current with a low specific on-resistance.

10.1.1 Shielded Planar MOSFET Structure: Blocking Mode

In the forward blocking mode of the shielded planar MOSFET structure, the voltage is supported by a depletion region formed on both sides of the P^+ region/N-drift junction. The maximum blocking voltage can be determined by the electric field at this junction becoming equal to the critical electric field for breakdown if the parasitic $N^+/P/N$ bipolar transistor is completely suppressed. This suppression is accomplished by short-circuiting the N^+ source and P^+ regions using the source metal as shown on the upper left hand side of the cross-section. This short circuit can be accomplished at a location orthogonal to the cell cross-section if desired to reduce the cell pitch while optimizing the specific on-resistance. If the doping concentration of the P^+ region is high, the reach-through breakdown problem discussed in the previous chapter is completely eliminated. In addition, the high doping concentration in the P^+ region promotes the depletion of the JFET region at lower drain voltages providing enhanced shielding of the channel and gate oxide.

With the shielding provided by the P^+ region, the minimum P-base thickness for 4H-SiC power MOSFETs is no longer constrained by the reach-through limitation. This enables reducing the channel length below the values associated with any particular doping concentration of the P-base region in Fig. 9.3. In addition, the opportunity to reduce the P-base doping concentration enables decreasing the threshold voltage. The smaller channel length and threshold voltage provide the benefits of reducing the channel resistance contribution.

In the case of the accumulation mode planar MOSFET structure, the presence of the sub-surface P^+ shielding region under the N-base region provides the potential required for *completely depleting* the N-base region if its doping concentration and thickness are appropriately chosen. This enables *normally-off operation* of the accumulation mode planar MOSFET with zero gate bias. It is worth pointing out that this mode of operation is fundamentally different that that of buried channel MOS devices[3]. Buried channel devices contain an un-depleted N-type

channel region that provides a current path for the drain current at zero gate bias. This region must be depleted by a negative gate bias creating a normally-on device structure.

In the accumulation-mode, planar MOSFET structure, the depletion of the N-base region is accompanied by the formation of the potential barrier for the flow of electrons through the channel. The channel potential barrier does not have to have a large magnitude because the depletion of the JFET region screens the channel from the drain bias as well.

The maximum blocking voltage capability of the shielded planar MOSFET structure is determined by the drift region doping concentration and thickness as already discussed in chapter 3. However, to fully utilize the high breakdown electric field strength available in silicon carbide, it is important to screen the gate oxide from the high field within the semiconductor. In the shielded planar MOSFET structure, this is achieved by the formation of a potential barrier at location A by the depletion of the JFET region at a low drain bias voltage.

10.1.2 Shielded Planar MOSFET Structure: Forward Conduction

In the shielded planar MOSFET structure, current flow between the drain and source can be induced by creating an inversion layer channel on the surface of the P-base region or an accumulation layer channel on the surface of the N-base region. The current path is similar to that already shown in Fig. 9.4 by the dotted area. The current flows through the channel formed due to the applied gate bias into the JFET region via the accumulation layer formed above it under the gate oxide. It then spreads into the N-drift region at a 45 degree angle and becomes uniform through the rest of the structure. The total on-resistance for the planar power MOSFET structure is determined by the resistance of these components in the current path:

$$R_{on,sp} = R_{CH} + R_A + R_{JFET} + R_D + R_{subs} \qquad [10.1]$$

where R_{CH} is the channel resistance, R_A is the accumulation region resistance, R_{JFET} is the resistance of the JFET region, R_D is the resistance of the drift region after taking into account current spreading from the JFET region, and R_{subs} is the resistance of the N^+ substrate. These resistances can be analytically modeled by using the current flow pattern indicated by the shaded regions in Fig. 9.4.

For the shielded planar MOSFET structure with the P-base region, the specific channel resistance is given by:

$$R_{CH} = \frac{(L_{CH} \cdot p)}{\mu_{inv} C_{ox} (V_G - V_T)} \quad [10.2]$$

where L_{CH} is the channel length as shown in Fig. 9.4, μ_{inv} is the mobility for electrons in the inversion layer channel, C_{ox} is the specific capacitance of the gate oxide, V_G is the applied gate bias, and V_T is the threshold voltage. For the shielded planar MOSFET structure with the N-base region, the specific channel resistance is given by:

$$R_{CH} = \frac{(L_{CH} \cdot p)}{\mu_a C_{ox} (V_G - V_T)} \quad [10.3]$$

where μ_a is the mobility for electrons in the accumulation layer channel. As discussed later in this chapter, much larger accumulation layer mobility has been experimentally observed in silicon carbide allowing reduction of the specific on-resistance. In addition, the threshold voltage for the accumulation mode is smaller than for the inversion mode allowing further improvement in the channel resistance contribution. The rest of the resistance components in the shielded planar MOSFET structure can be modeled by using the same equations provided in chapter 9.

The specific on-resistances of 4H-SiC shielded planar MOSFETs with a drift region doping concentration of 1 x 10^{16} cm^{-3} and thickness of 20 microns were modeled using the analytical expressions. For comparison of the inversion and accumulation mode structures, a gate oxide thickness of 0.1 microns was used. The dimension 'a' in the structure shown in Fig. 9.4 was kept at 1 micron. This value can be achieved using 0.5 micron design rules. The accumulation mobility was assumed to be 200 cm^2/Vs while an inversion layer mobility of 50 cm^2/Vs was used based upon typical values reported in the literature as discussed later in this chapter. A K-factor of 0.1 was used to provide correlation with the simulations. The P^+ region was assumed to have a depth of 1 micron and the effective gate drive voltage ($V_G - V_T$) was assumed to be 10 volts for the inversion mode structure versus 15 volts for the accumulation mode structure due to the difference between their threshold voltages. A channel length of 1 micron and a JFET width of 2 microns were used for these structures.

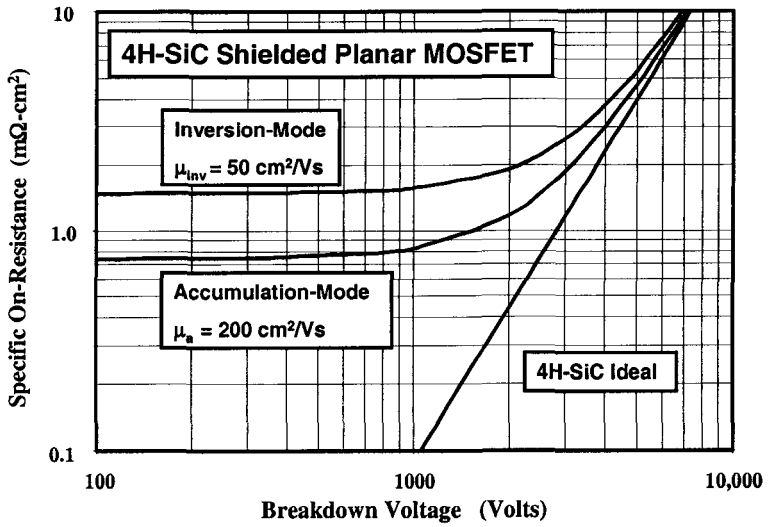

Fig. 10.2 On-Resistance for the 4H-SiC Shielded Planar MOSFETs.

The specific on-resistance for the shielded planar 4H-SiC MOSFETs is plotted in Fig. 10.2 as a function of the breakdown voltage. As discussed in the previous chapter, in performing this modeling, it is important to recognize that the thickness of the drift region (parameter 't' in Fig. 9.4) can become smaller than the cell parameter 's' at lower breakdown voltages (below 700 volts). Under these conditions, the current does not distribute at a 45 degree angle into the drift region from the JFET region. Instead, the current flows from a cross-sectional width of $(W_J - W_P)$ to a cross-section of $(t + W_J - W_P)$.

From Fig. 10.2, it can be seen that specific on-resistance of 4H-SiC shielded planar MOSFETs approaches the ideal specific on-resistance when the breakdown voltage exceeds 5000 volts because the drift region resistance becomes dominant. However, when the breakdown voltage falls below 1000 volts, the channel contribution becomes dominant. In this design regime, the advantage of using an accumulation channel becomes quite apparent. The accumulation-mode device has about 2x lower specific on-resistance. When compared with the planar MOSFET structure without the shielded channel (see Fig. 9.9), the difference in specific on-resistance does not appear to be very significant. However, as discussed in the previous chapter, the unshielded devices were able to support only about half the blocking

voltage capability of the drift region due to the reach-through breakdown problem. This limitation is not observed for the shielded planar MOSFET structure as will be shown in the section of this chapter dealing with simulated results.

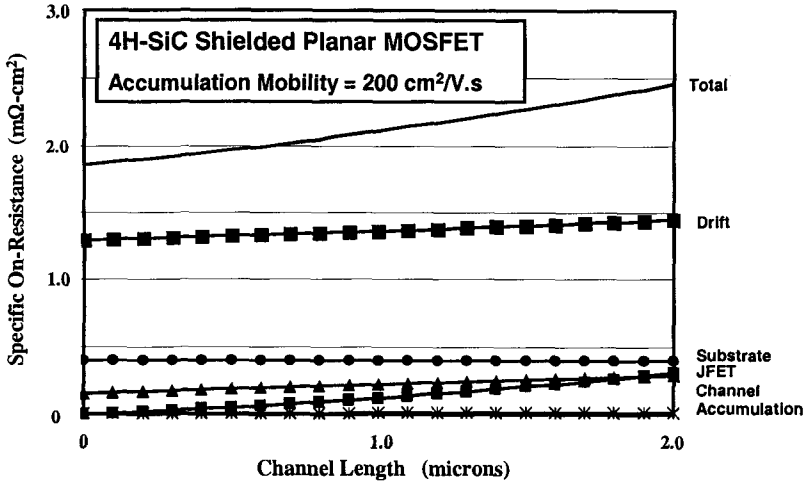

Fig. 10.3 Components of the On-Resistance for the 4H-SiC Shielded Planar MOSFET with Accumulation Channel.

In order to contrast the performance of the accumulation mode planar structure with the performance of the inversion mode structure described in the previous chapter, it is interesting to examine the components of the on-resistance for the accumulation-mode device. The various components of the on-resistance are shown in Fig. 10.3 when a channel accumulation layer mobility of 200 cm^2/Vs was used. This structure has a channel length of 1 micron, a JFET width of 1.5 microns, and a gate oxide thickness of 0.05 microns. A thinner gate oxide was chosen because of the shielding of the gate oxide in this structure. It can be seen that the drift region resistance is dominant under these conditions even for channel lengths of 2 microns. At a channel length of 1 micron, a total specific on-resistance of 2.1 $m\Omega\text{-}cm^2$ is obtained, which is about twice the ideal specific on-resistance. This is an excellent value for a device with the drift regions parameters used for the modeling providing a breakdown voltage of 3000 volts. It is worth pointing out that the contribution from the N^+ substrate is exceeding that from the channel for

this structure. This indicates the need to either reduce the substrate thickness or reduce its resistivity to bring the total specific on-resistance close to that of the drift region.

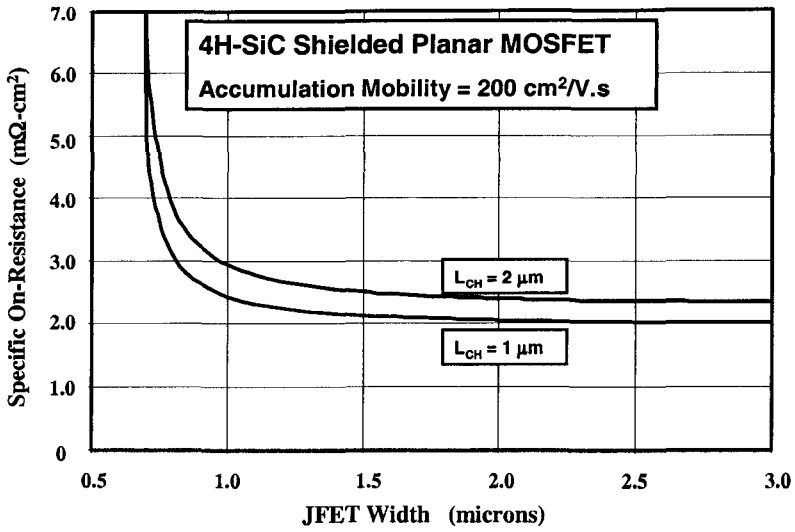

Fig. 10.4 Impact of JFET Width on the On-Resistance for the 4H-SiC Shielded Planar MOSFET with Accumulation Channel.

The JFET width in the planar MOSFET structure must be optimized not only to obtain the lowest specific on-resistance but to also control the electric field at the gate oxide interface. The impact of changes to the JFET width on the specific on-resistance for the accumulation-mode 4H-SiC shielded planar MOSFET structure is shown in Fig. 10.4 for a structure with the same cell parameters that were given above. It can be observed that the specific on-resistance becomes very large when the JFET width is made smaller than about 0.7 microns. This occurs because the zero bias depletion width for 4H-SiC P-N junctions is about 0.6 microns. When the JFET width approaches this value, the current becomes severely constricted resulting in a high specific on-resistance. As the JFET width is increased, the contribution from its resistance decreases rapidly. However, the increase in cell pitch enhances the specific resistance contributions from the channel resulting in a nearly constant total specific on-resistance. A minimum specific on-resistance is observed to occur at a JFET width of above 1.5 microns,

which is larger than the value for the planar MOSFETs discussed in the previous chapter. This is due to the larger mobility in the accumulation channel. In addition to the slightly lower specific on-resistance for this structure when compared with the planar MOSFET discussed in the previous chapter (see Fig. 9.6), the specific on-resistance is observed to be less sensitive to the channel length. This provides more latitude with regard to the design rules used for the fabrication of the accumulation mode device.

10.1.3 Shielded Planar MOSFET Structure: Threshold Voltage

As pointed out in the previous chapter, the threshold voltage of the power MOSFET is an important design parameter from an application stand-point. A minimum threshold voltage must be maintained at above 1 volt for most system applications to provide immunity against inadvertent turn-on due to voltage spikes arising from noise. At the same time, a high threshold voltage is not desirable because the voltage available for creating the charge in the channel is determined by (V_G – V_T) where V_G is the applied gate bias voltage and V_T is the threshold voltage. Most power electronic systems designed for high voltage operation (the most suitable application area for silicon carbide devices) provide a gate drive voltage of only upto 10 volts. Based upon this criterion, the threshold voltage should be kept below 3 volts in order to obtain a low channel resistance contribution.

For the inversion-mode shielded planar MOSFET, the threshold voltage can be modeled by defining it as the gate bias at which on-set of *strong inversion* begins to occur in the channel. This voltage can be determined using[4]:

$$V_{TH} = \frac{\sqrt{4\varepsilon_S kTN_A \ln(N_A / n_i)}}{C_{ox}} + \frac{2kT}{q}\ln\left(\frac{N_A}{n_i}\right) \qquad [10.4]$$

where N_A is the doping concentration of the P-base region, k is Boltzmann's constant, and T is the absolute temperature. The presence of positive fixed oxide charge shifts the threshold voltage in the negative direction by:

$$\Delta V_{TH} = \frac{Q_F}{C_{ox}} \qquad [10.5]$$

A further shift of the threshold voltage in the negative direction by 1 volt can be achieved by using heavily doped N-type polysilicon as the gate electrode as routinely done for silicon power MOSFETs.

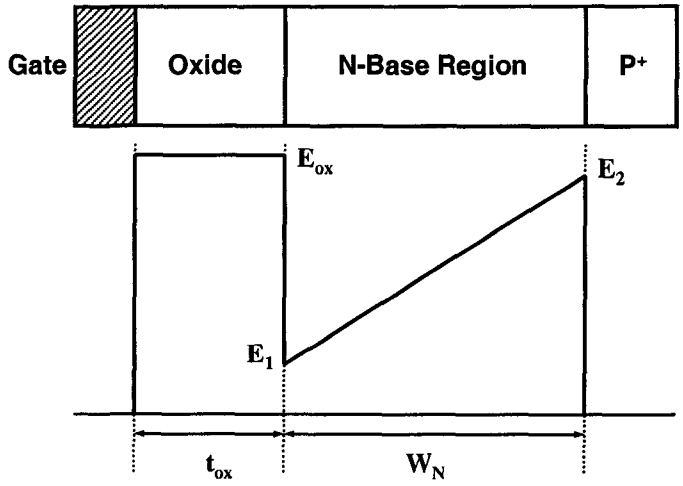

Fig. 10.5 Electric Field Profile in the Gate Region for the Accumulation-Mode MOSFET structure.

The band bending required to create a channel in the accumulation-mode planar MOSFET is much smaller than required for the inversion mode device. This provides the opportunity to reduce the threshold voltage while obtaining the desired normally-off device behavior. A model for the threshold voltage of accumulation-mode MOSFETs has been developed[5] using the electric field profile shown in Fig. 10.5 when the gate is biased at the threshold voltage. In this figure, the electric fields in the semiconductor and oxide are given by:

$$E_1 = \frac{V_{bi}}{W_N} - \frac{qN_D W_N}{2\varepsilon_S} \qquad [10.6]$$

$$E_2 = \frac{V_{bi}}{W_N} + \frac{qN_D W_N}{2\varepsilon_S} \qquad [10.7]$$

$$E_{ox} = \frac{\varepsilon_S}{\varepsilon_{ox}} E_1 \qquad [10.8]$$

Note that this model is based upon neglecting any voltage supported within the P^+ region under the assumption that it is very heavily doped. Using these electric fields, the threshold voltage is found to be given by:

$$V_{TH} = \phi_{MS} + \left(\frac{\varepsilon_S V_{bi}}{\varepsilon_{ox} W_N} - \frac{qN_D W_N}{2\varepsilon_{ox}} \right) t_{ox} \qquad [10.9]$$

The first term in this equation accounts for the work function difference between the gate material and the lightly doped N-Base region. The second term represents the effect of the built-in potential of the P^+/N junction that depletes the N-base region.

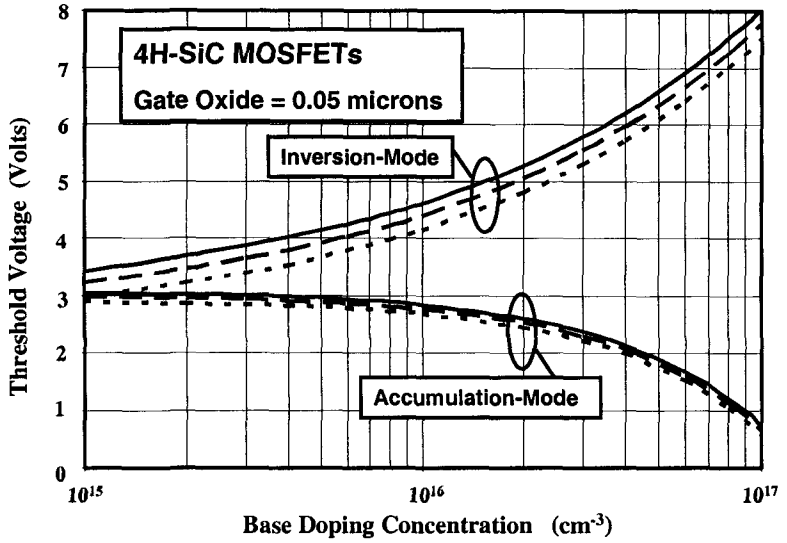

Fig. 10.6 Threshold Voltage of 4H-SiC Accumulation-Mode MOSFETs.

(Solid Line: 300°K; Dash Line: 400°K; Dotted Line: 500°K)

The analytically calculated threshold voltage for 4H-SiC accumulation-mode MOSFETs are provided in Fig. 10.6 for the case of a gate oxide thickness of 0.05 microns, and N-base thickness of 0.2 microns as a function of the N-base doping concentration with the inclusion of a metal-semiconductor work-function difference of 1 volt. For comparison purposes, the threshold voltage for the inversion-mode 4H-SiC MOSFET is also given in this figure for the same gate oxide

thickness. A strikingly obvious difference between the structures is a decrease in the threshold voltage for the accumulation-mode structure with increasing doping concentration in the N-base region. This occurs due to the declining influence of the P^+/N junction at the gate oxide interface when the doping concentration of the N-base region is increased. It can also be noted that the temperature dependence of the threshold voltage is smaller for the accumulation-mode structure. Of course, the most important benefit of the accumulation-mode is that lower threshold voltages can be achieved than in the inversion-mode structures. At an N-base doping concentration of 1 x 10^{16} cm^{-3}, the threshold voltage for the accumulation-mode structure is 2.8 volts. This will be reduced to just below 2 volts in the presence of typical fixed oxide charge in the 4H-SiC/oxide system.

10.1.4 Accumulation-Mode MOSFET Structure: Threshold Voltage Simulations

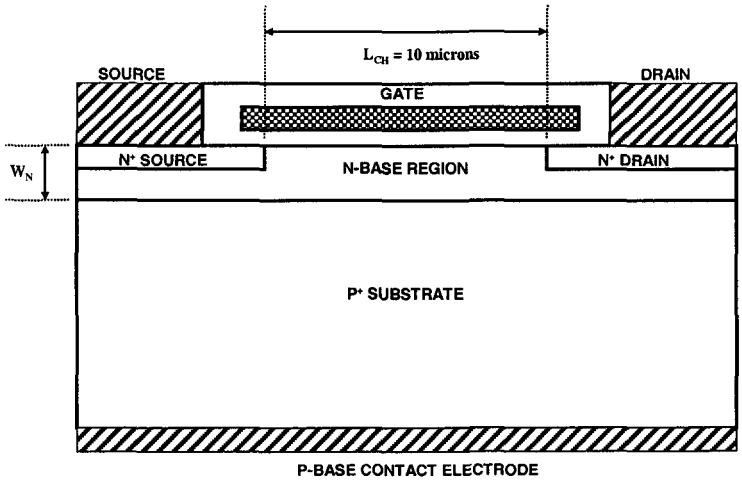

Fig. 10.7 The Planar Lateral Accumulation-Mode 4H-SiC MOSFET Structure.

In order to verify the predictions of the analytical model for the threshold voltage for silicon carbide accumulation-mode MOSFETs that was described in the previous section, two-dimensional numerical simulations were performed for a lateral MOSFET structure. This structure was designed with a long channel (10 microns) and uniform N-base doping concentration, as shown in Fig. 10.7, to allow extraction of the threshold

voltage and the channel accumulation layer mobility. Simulations performed with this structure using different N-base doping concentrations and gate oxide thickness values enables extraction of the dependence of the threshold voltage on these parameters. In addition, the impact of changing the thickness of the N-base region was examined.

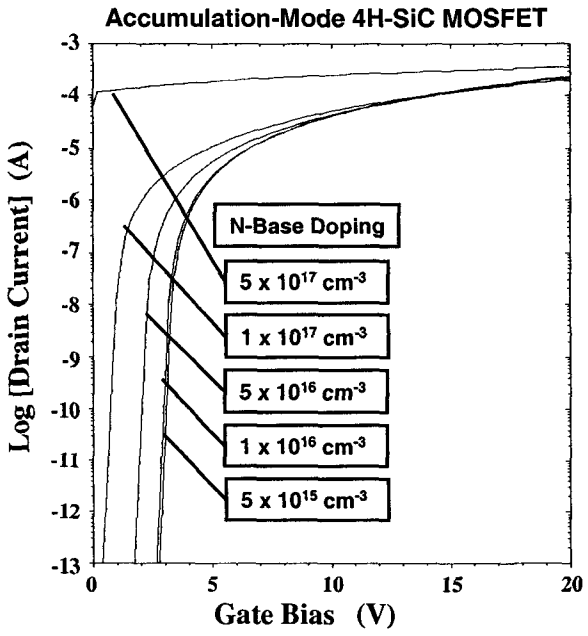

Fig. 10.8 Transfer Characteristics of the Planar Lateral Accumulation-Mode 4H-SiC MOSFET Structure.

The transfer characteristics obtained for the case of a gate oxide thickness of 0.05 microns and N-base thickness of 0.2 microns, are shown in Fig. 10.8, for various N-base doping concentrations. The threshold voltages for the different N-base doping concentrations were extracted by using a low drain current level (10^{-13} A/micron) because this defines the on-set of the formation of the accumulation layer. The extracted threshold voltage is compared with the predictions of the analytical model in Fig. 10.9. A good agreement is observed by using the model to compute the threshold voltage until it approaches a value close to zero. The threshold voltage predicted by the analytical model is larger than that obtained with the simulations at high doping concentration in

the N-base region. This occurs because the depletion region and voltage supported by the P^+ region were neglected when deriving the analytical model. For the P^+ region doping concentration of 1 x 10^{19} cm^{-3} used during the simulations, this assumption results in a deviation of about 0.3 volts in the analytically calculated threshold voltage at a N-base doping concentration of 1 x 10^{17} cm^{-3}. It is worth pointing out that when the doping concentration of the N-base region exceeds 1 x 10^{17} cm^{-3} (for a thickness of 0.2 microns), the built-in potential of the P^+/N junction becomes insufficient to completely deplete the N-base region. The threshold voltage then becomes negative indicting the presence of a conductive channel at zero gate bias.

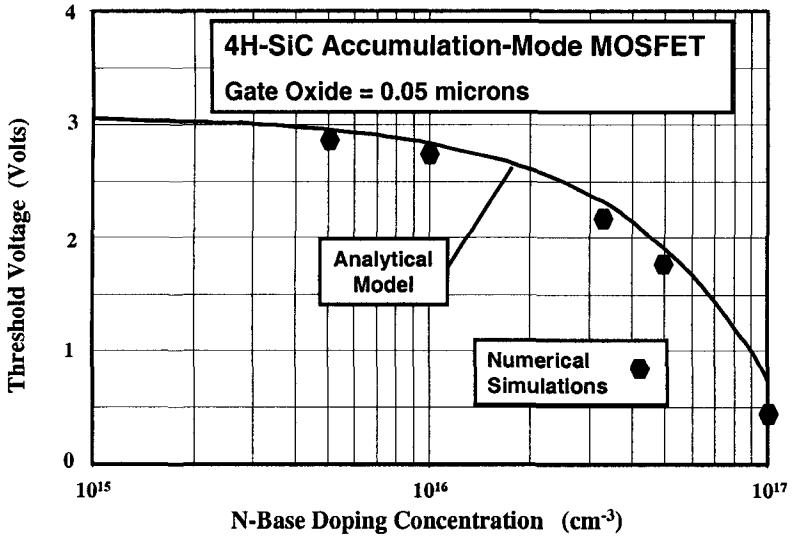

Fig. 10.9 Threshold Voltage of 4H-SiC Accumulation-Mode MOSFETs.

The thickness of the N-base region also has a strong influence on the threshold voltage of the accumulation-mode MOSFET. The results of simulations performed on the lateral accumulation-mode structure with various N-base widths are provided in Fig. 10.10 for the case of a gate oxide thickness of 0.05 microns and an N-base doping concentration of 1 x 10^{16} cm^{-3}. It can be observed that the threshold voltage decreases as the N-base width is increased eventually becoming less than zero for an N-base width of 1 micron. The threshold voltage extracted from these simulations is compared with the predictions of the analytical model in

Fig. 10.11. A good agreement is observed by using the model to compute the threshold voltage for N-base widths of 0.2 and 0.5 microns. However, the threshold voltage predicted by the analytical model is about 0.7 volts larger than that obtained with the simulations for the case of an N-base width of 0.1 microns. This deviation is again due to neglecting the depletion width and voltage supported by the P^+ region when deriving the analytical model. The contribution from this voltage becomes more significant as the width of the N-base region is reduced because it now supports a smaller fraction of the voltage across the gate structure.

The analytically predicted threshold voltage was also found to be larger than that obtained from the numerical simulations by about 0.7 volts when the width of the N-base region was increased to 1 micron. In this case, the N-base region is on the verge of being completely depleted according to the simulations. The influence of majority-carrier distribution tails[6] on the current transport at the gate oxide interface must now be taken into account, which is beyond the scope of the model. It is worth pointing out that a mobility degradation factor was not included during the simulations performed to extract the threshold voltage.

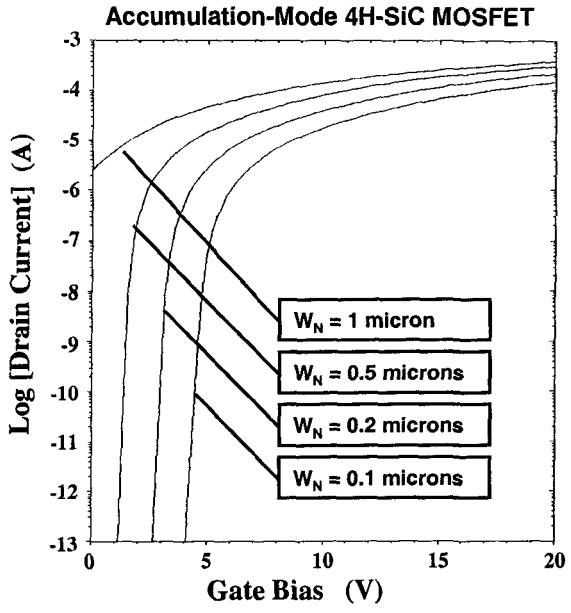

Fig. 10.10 Transfer Characteristics of the Planar Lateral Accumulation-Mode 4H-SiC MOSFET Structure.

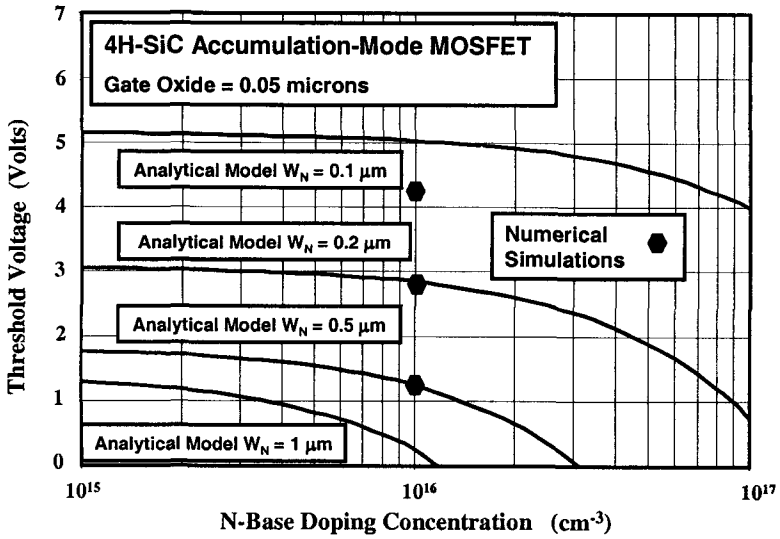

Fig. 10.11 Threshold Voltage of 4H-SiC Accumulation-Mode MOSFETs.

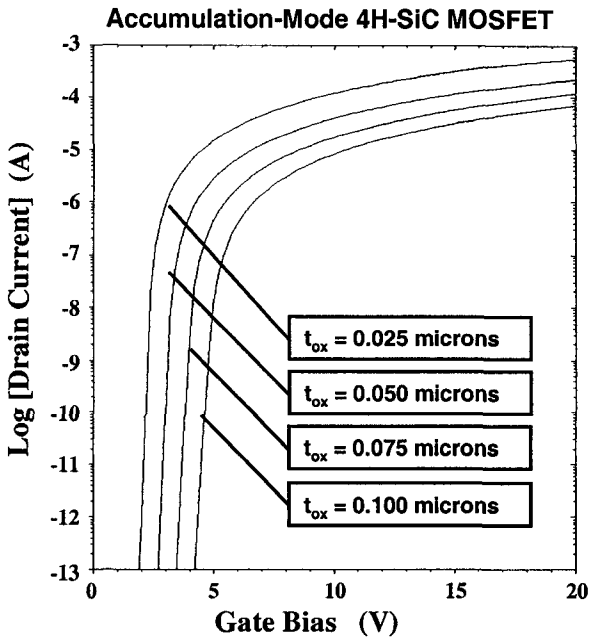

Fig. 10.12 Transfer Characteristics of the Planar Lateral Accumulation-Mode 4H-SiC MOSFET Structure.

As in the case of inversion-mode MOSFETs, the threshold voltage for the accumulation-mode MOSFETs depends upon the gate oxide thickness. This dependence is predicted by the second term for the analytical expression for the threshold voltage in Eq. [10.9]. The results of numerical simulations are shown in Fig. 10.12 for the case of an N-base doping concentration of 8.5 x 10^{15} cm^{-3} and thickness of 0.2 microns. The threshold voltage extracted from these simulations is compared with the analytically predicted values in Fig. 10.13. Once again, the predictions of the analytical model are in good agreement with the simulations indicating that this model can be utilized for the design of silicon carbide MOSFETs.

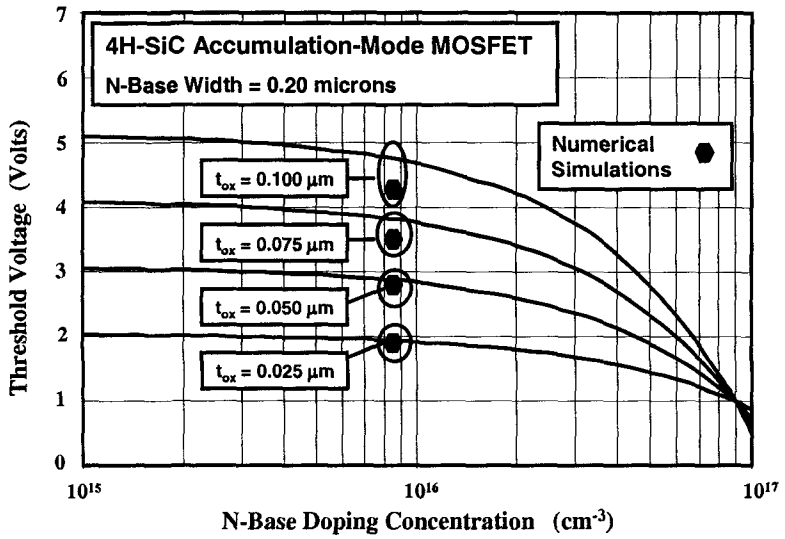

Fig. 10.13 Threshold Voltage of 4H-SiC Accumulation-Mode MOSFETs.

It is interesting to observe that the threshold voltage becomes independent of the gate oxide thickness in Fig. 10.13 for an N-base doping concentration of 9 x 10^{16} cm^{-3}. This behavior occurs due to the cancellation of the two parts in the second term in Eq. [10.9] under the condition:

$$N_D.W_N^2 = \frac{2.\varepsilon_S.V_{bi}}{q} \qquad [10.10]$$

This condition corresponds to the combination of N-base region doping concentration and thickness that is just completely depleted by the built-in potential of the P^+/N junction.

10.2 Planar Shielded Inversion-Mode MOSFET Structure: Numerical Simulations

In order to gain insight into the operation of the planar 4H-SiC shielded inversion-mode MOSFET structure, two-dimensional numerical simulations were performed with a drift region doping concentration of 1 x 10^{16} cm^{-3} and thickness of 20 microns corresponding to a parallel-plane breakdown voltage of 3000 volts. The baseline device had a gate oxide thickness of 0.04 microns and a P^+ region depth of 1 micron. The P-base region had a thickness of 0.2 microns with a doping concentration of 9 x 10^{16} cm^{-3}. The JFET width for the baseline device was 1.5 microns. The cell pitch for the structure, corresponding to the cross-section shown on the left-hand-side of Fig. 10.1, was 3.25 microns.

10.2.1 Planar Shielded Inversion-Mode MOSFET Structure: Blocking Characteristics

The blocking capability of the planar 4H-SiC shielded inversion-mode MOSFET was investigated by maintaining zero gate bias while increasing the drain voltage. It was found that the drain current remains below 1 x 10^{-13} amperes upto a drain bias of 3000 volts. This behavior is shown in Fig. 10.14 to contrast the characteristics of the shielded device with that shown earlier in Fig. 9.20 for the planar inversion-mode MOSFET without the shielding of the P-base region. Consequently, the shielding of the P-base region is very effective for preventing the reach-through breakdown problem allowing the device to operate upto the full capability of the drift region.

In this figure, the drain current is also shown when various positive gate bias voltages are applied to the planar 4H-SiC inversion-mode MOSFET structure. The on-set of drain current flow is observed when the gate bias exceeds 4 volts. Excellent drain current saturation under gate control is observed at all gate bias voltages upto the blocking voltage capability of the drift region. These characteristics indicate effective suppression of the reach-through phenomenon as well as the parasitic N-P-N bipolar transistor.

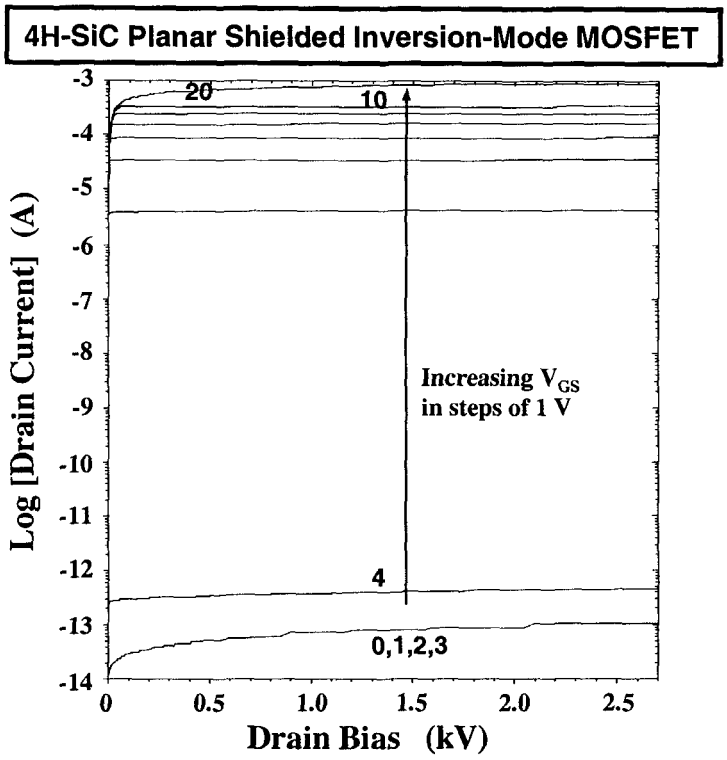

Fig. 10.14 Blocking Characteristics of the Planar 4H-SiC Shielded Inversion-Mode MOSFET Structure.

In the previous chapter, it was demonstrated that a high electric field is generated at the gate oxide interface in the planar 4H-SiC MOSFET structure when the shielding is ineffective. This problem can be mitigated with the P^+ region to shield the surface from the high electric fields developed in the drift region. A three-dimensional view of the electric field distribution is shown in Fig. 10.15 for a drain bias of 3000 volts with zero gate bias. The field distribution shown in this figure indicates that the electric field at the gate oxide is significantly suppressed by the presence of the P^+ region. At the maximum blocking capability of the drift region, the electric field at the gate oxide interface has reached a magnitude of 1.5×10^6 V/cm while the electric field in the bulk has reached a magnitude of 3×10^6 V/cm. A slight field enhancement is observed at the edge of the P^+ region at a depth of 1 micron below the semiconductor surface.

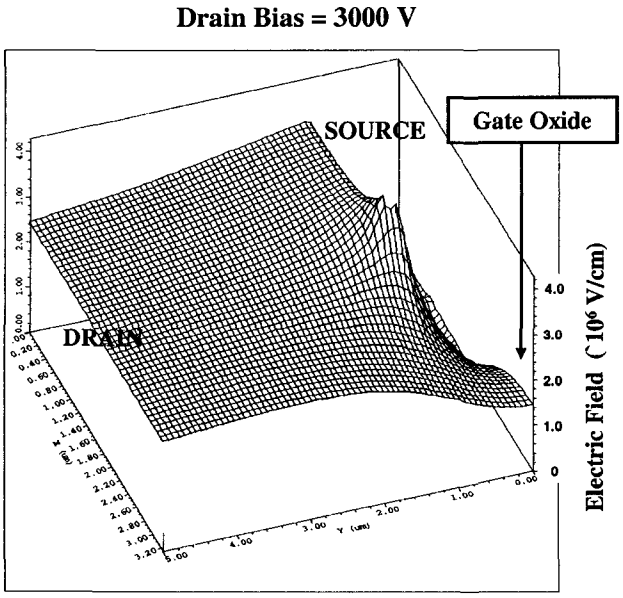

Fig. 10.15 Electric Field Distribution in the Planar 4H-SiC Shielded Inversion-Mode MOSFET Structure.

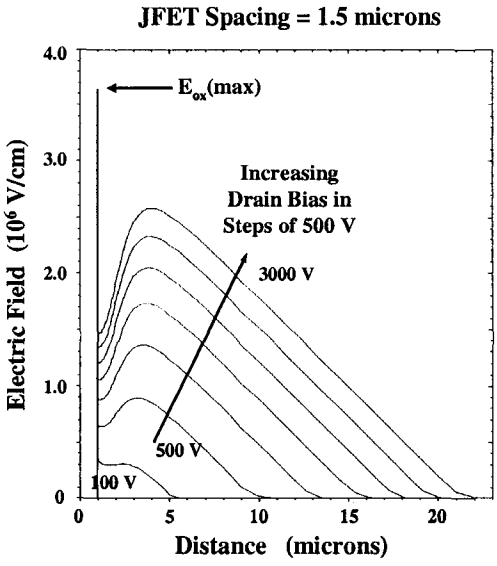

Fig. 10.16 Electric Field Distribution in the Planar 4H-SiC Shielded Inversion-Mode MOSFET Structure.

In the planar 4H-SiC shielded inversion-mode MOSFET structure, the largest electric field at the gate oxide interface occurs at the center of the JFET region. The behavior of this electric field with increasing drain bias is shown in Fig. 10.16 for the case of a JFET width of 1.5 microns. From this figure, it is apparent that there is considerable shielding of the gate oxide by the JFET region due to the formation of a potential barrier when this region becomes depleted at lower drain voltages. The maximum electric field occurs inside the semiconductor at a depth of about 4 microns. The electric field in the oxide reaches a magnitude of 3.5 x 10^6 V/cm at a drain bias of 3000 volts. The same magnitude for the electric field was observed in the unshielded structure for a smaller JFET width of 1 micron. This difference in behavior is due to the larger doping concentration of the P^+ shielding region when compared with P-base region. The high doping level in the P^+ region promotes the depletion of the JFET region setting up the same magnitude of the potential barrier at a larger JFET width.

10.2.2 Planar Shielded Inversion-Mode MOSFET Structure: On-State Characteristics

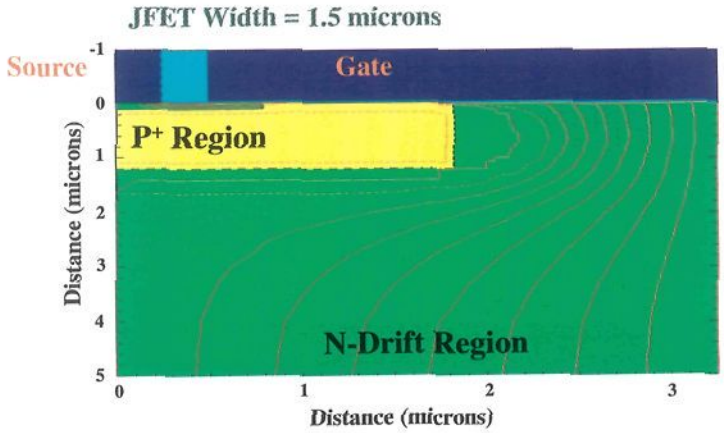

Fig. 10.17 On-State Current Distribution in the Planar 4H-SiC Shielded Inversion-Mode MOSFET Structure.

The on-resistance for the planar 4H-SiC shielded inversion-mode structure was extracted by performing numerical simulations with a gate bias of upto 20 volts. The current distribution within the structure is shown in Fig. 10.17 for the case of JFET width of 1.5 microns. It can be

seen that the current is not as severely constricted in the JFET region when compared with the current flow in the unshielded structure with JFET width of 1 micron (see top part of Fig. 9.25). Consequently, for the same magnitude of electric field reduction at the gate oxide interface, a lower contribution to the on-resistance can be obtained for the JFET region with the shielded structure.

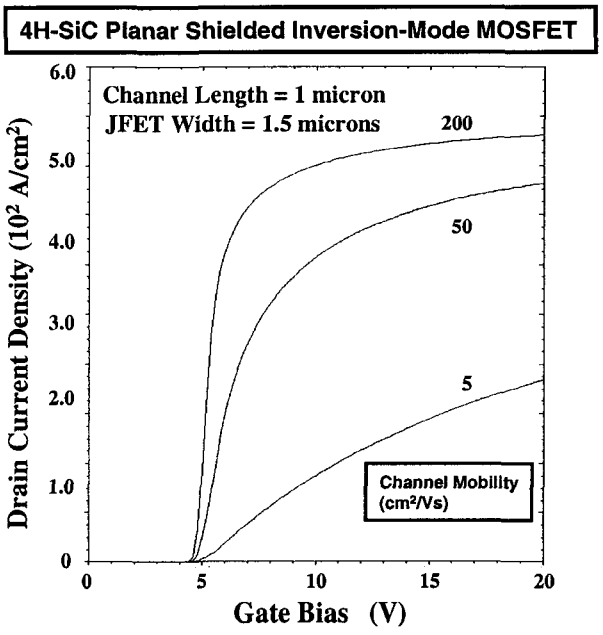

Fig. 10.18 Transfer Characteristics of the Planar 4H-SiC Shielded Inversion-Mode MOSFET Structures.

The simulations of the specific on-resistance of the planar 4H-SiC shielded inversion-mode MOSFET structure were performed with different values for the inversion layer mobility. The specific on-resistance was obtained by using a drain bias of 1 volt and sweeping the gate bias to 20 volts to obtain the transfer characteristic. A drain bias of 1 volt was used for these simulations because the on-state voltage drop for these structures is typically in this range. A typical transfer characteristic obtained using this method is shown in Fig. 10.18 for the device with JFET width of 1.5 microns. From the transfer characteristics, it can be seen that the threshold voltage that determines the on-resistance is approximately 5 volts, which is much lower than for the unshielded

device structure (see Fig. 9.26). This allows operating the device in the on-state with a gate bias of 10 volts. The impact of changing the channel inversion layer mobility is also shown in this figure. As expected, there is a reduction in the drain current as the channel mobility is reduced.

When the inversion layer mobility is assumed to be 200 cm^2/Vs, it can be noted from Fig. 10.18 that nearly the same drain current is obtained at a gate bias of 10 volts as at 20 volts. As discussed in the previous chapter, inversion layer effective mobility values as high as 165 cm^2/Vs have been experimentally obtained with even higher Hall mobility values reported in the literature. The simulation results indicate that it is possible to operate the planar 4H-SiC shielded inversion-mode MOSFET structure with a gate bias of 10 volts. The drain current is also observed to be larger than that observed in the unshielded structure. Consequently, the specific on-resistance for the shielded 4H-SiC inversion-mode MOSFET structure is found to be 2.4 $m\Omega\text{-}cm^2$ (after including a substrate contribution of 0.4 $m\Omega\text{-}cm^2$) compared with 2.8 $m\Omega\text{-}cm^2$ obtained for the unshielded structure. This value is in excellent agreement with the value obtained by using the analytical model for the specific on-resistance (see Fig. 10.2). Although the difference between the specific on-resistance for the shielded and unshielded structures is only 17 percent, it is worth pointing out the maximum blocking voltage capability for the shielded structure is twice that observed for the unshielded structure whose blocking capability was limited by the reach-through problem.

10.2.3 Planar Shielded Inversion-Mode MOSFET Structure: Output Characteristics

In a previous section, it was demonstrated that the shielding of the P-base region within the planar MOSFET structure suppresses the reach-through breakdown problem. The shielding effect can also be expected to improve the output characteristics of the power MOSFET structure. In addition, the elimination of the reach-through induced leakage current should improve the output resistance of the device. These factors indicate that the output characteristics for the shielded 4H-SiC inversion-mode MOSFET should be much superior to those observed for the unshielded device structure.

The output characteristics for the shielded 4H-SiC inversion-mode MOSFET structure were obtained by using two-dimensional numerical simulations with sweeping of the drain voltage at various gate

bias voltages. The results obtained for a structure with channel length of 1 micron, gate oxide thickness of 0.04 microns, and a JFET width of 1.5 microns are shown in Fig. 10.19. The device structure exhibits excellent drain current saturation for gate bias voltages upto 10 volts with a very high output resistance. The saturated drain current increases as the square of the gate bias voltage, which is typical for MOSFETs that operate with channel pinch-off. For the gate bias values of 15 and 20 volts, a pronounced quasi-saturation region is observed. However, when taking into consideration the very high drain current density obtained even for a gate bias of 10 volts, it is not necessary to operate the planar 4H-SiC shielded inversion-mode MOSFET with gate bias voltages above 10 volts.

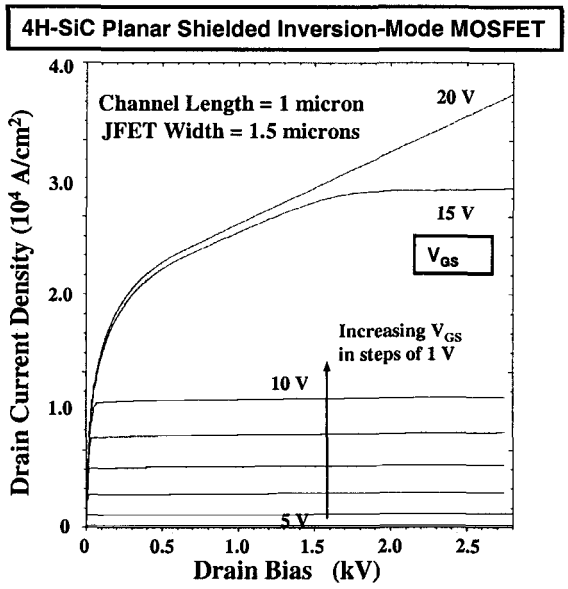

Fig. 10.19 Output Characteristics of a Planar 4H-SiC Shielded Inversion-Mode MOSFET structure.

10.3 Planar Shielded Accumulation-Mode MOSFET Structure: Numerical Simulations

In order to gain insight into the operation of the planar 4H-SiC shielded accumulation-mode MOSFET structure, two-dimensional numerical

simulations were performed with a drift region doping concentration of 1 x 10^{16} cm^{-3} and thickness of 20 microns corresponding to a parallel-plane breakdown voltage of 3000 volts. The baseline device had the same cell parameters as used for the inversion-mode structure, namely, a gate oxide thickness of 0.04 microns, a P^+ region depth of 1 micron, and a JFET width of 1.5 microns.. The N-base region had a thickness of 0.2 microns with a doping concentration of 8.5 x 10^{15} cm^{-3}. The cell pitch for the structure, corresponding to the cross-section shown on the right-hand-side of Fig. 10.1, was 3.25 microns.

10.3.1 Planar Shielded Accumulation-Mode MOSFET Structure: Blocking Characteristics

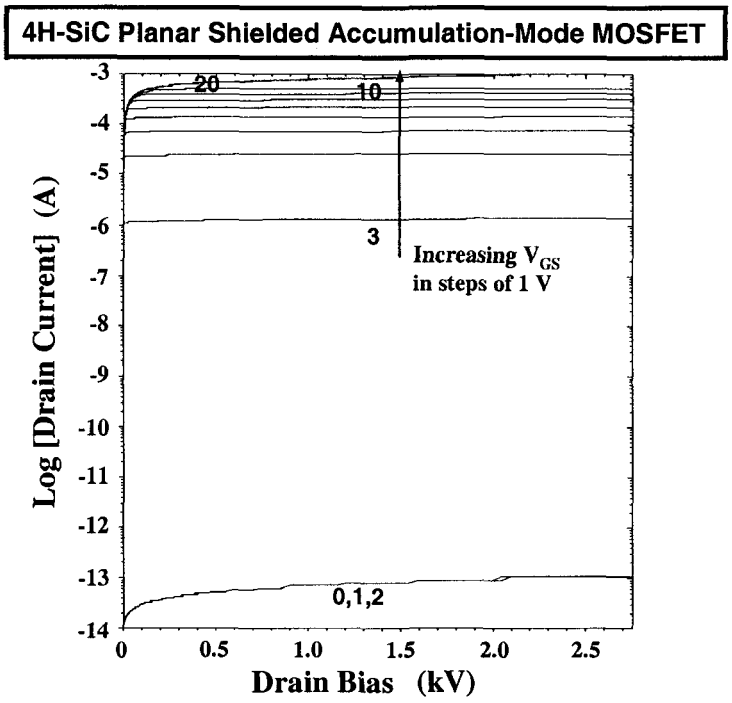

Fig. 10.20 Blocking Characteristics of the Planar 4H-SiC Shielded Accumulation-Mode MOSFET Structure.

The blocking capability of the planar 4H-SiC shielded accumulation-mode MOSFET was investigated by maintaining zero gate bias while increasing the drain voltage. It was found that the drain current remains

below 1 x 10^{-13} amperes upto a drain bias of 3000 volts. This behavior, shown in Fig. 10.20, demonstrates that the depletion of the N-base region by the built-in potential of P^+/N junction creates a potential barrier for electron transport through the channel. In addition, the shielding of the N-base region by the underlying P^+ region is very effective for preventing the reach-through breakdown problem allowing the device to operate upto the full capability of the drift region.

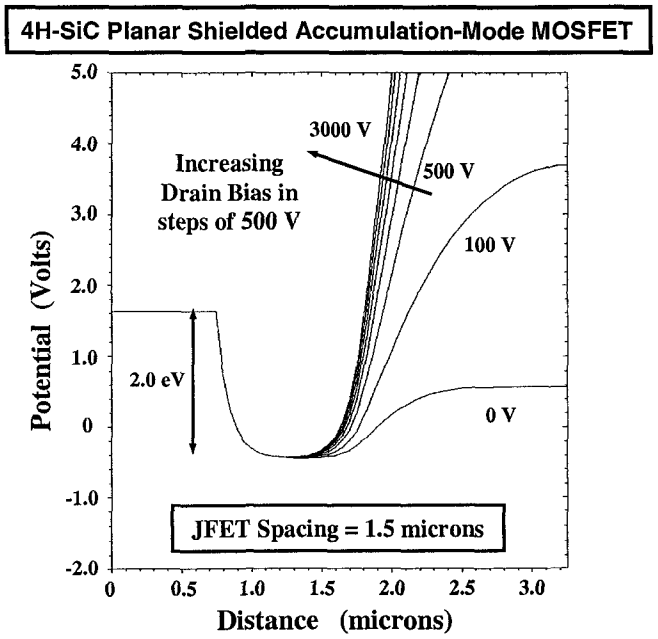

Fig. 10.21 Channel Potential Barrier in the Planar 4H-SiC Shielded Accumulation-Mode MOSFET Structure.

In order to understand the ability to suppress current flow in the accumulation-mode structure in the absence of the P-base region, it is instructive to examine the potential distribution along the channel. The variation of the potential along the channel is shown in Fig. 10.21 for the planar 4H-SiC shielded accumulation-mode MOSFET described above for various drain bias voltages when the gate bias voltage is held at zero volts. It can be seen that there is a potential barrier in the channel with a magnitude of 2 eV at zero drain bias. This barrier for the transport of electrons from the source to the drain is upheld even when the drain bias

is applied upto 3000 volts. This demonstrates the fundamental operating principle for creating a normally-off device with a depleted N-base region formed using the built-in potential of the P^+/N.

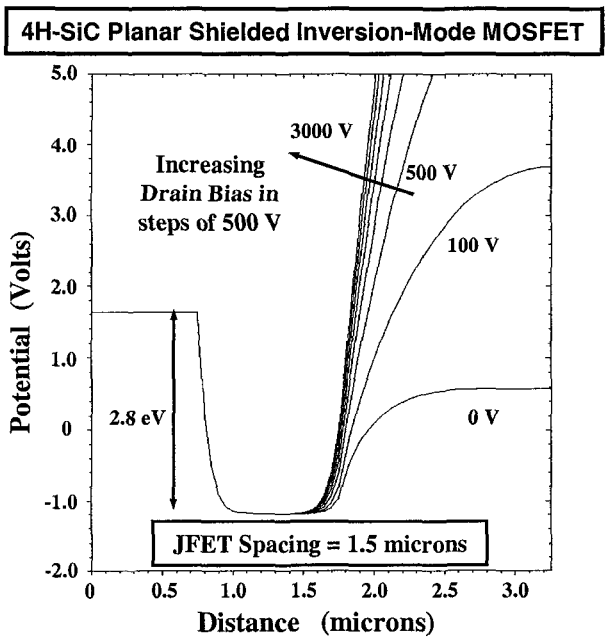

Fig. 10.22 Channel Potential Barrier in the Planar 4H-SiC Shielded Inversion-Mode MOSFET Structure.

For a better perspective on the operation of the accumulation-mode structure, the potential distribution along the channel is provided in Fig. 10.22 for the inversion-mode structure. From this figure, it can be seen that a potential barrier of 2.8 eV in magnitude is created due to the presence of the P-base region. This barrier is also retained intact when the drain bias voltage is increased to 3000 volts. By examining the potential distributions shown in the last two figures, it can be concluded that the accumulation-mode structure operates as well as the inversion-mode structure from the point of view of supporting high drain bias voltages with zero gate bias.

The normally-off feature can be preserved in the planar 4H-SiC shielded accumulation-mode MOSFET structure even when the channel length is reduced to 0.5 microns. The potential distribution along the

channel for this structure is shown in Fig. 10.23 for various drain bias voltages. It can be seen that, although the width of the barrier along the channel (x-direction in Fig. 10.23) is smaller than for the structure with the 1 micron channel length, the magnitude of the potential barrier for the transport of electrons from the source to the drain is still maintained at 2.0 eV. This is sufficient for obtained excellent blocking capability in the planar 4H-SiC shielded accumulation-mode MOSFET.

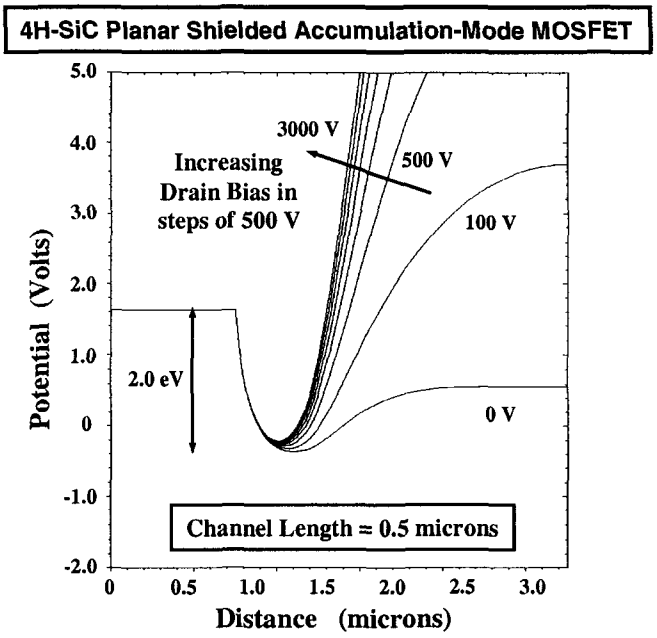

Fig. 10.23 Channel Potential Barrier in the Planar 4H-SiC Shielded Accumulation-Mode MOSFET Structure.

The blocking characteristic for the planar 4H-SiC shielded accumulation-mode MOSFET with channel length of 0.5 microns is shown in Fig. 10.24 together with traces obtained at various positive gate bias voltages. The device exhibits the same leakage current as the device with the longer channel length at zero gate bias. This demonstrates that the blocking voltage capability is preserved in the accumulation-mode structure even when the channel length is shortened to 0.5 microns. It is worth pointing out that an increased current is observed at a gate bias of 2 volts when the channel length is reduced to 0.5 microns. In addition, the traces for higher gate bias voltages are all shifted to larger drain current levels. This is, of course, related to the increase in the

transconductance of the MOSFET when the channel length is reduced. The change in the transconductance with channel length is similar to that observed in the conventional inversion-mode MOSFET structure.

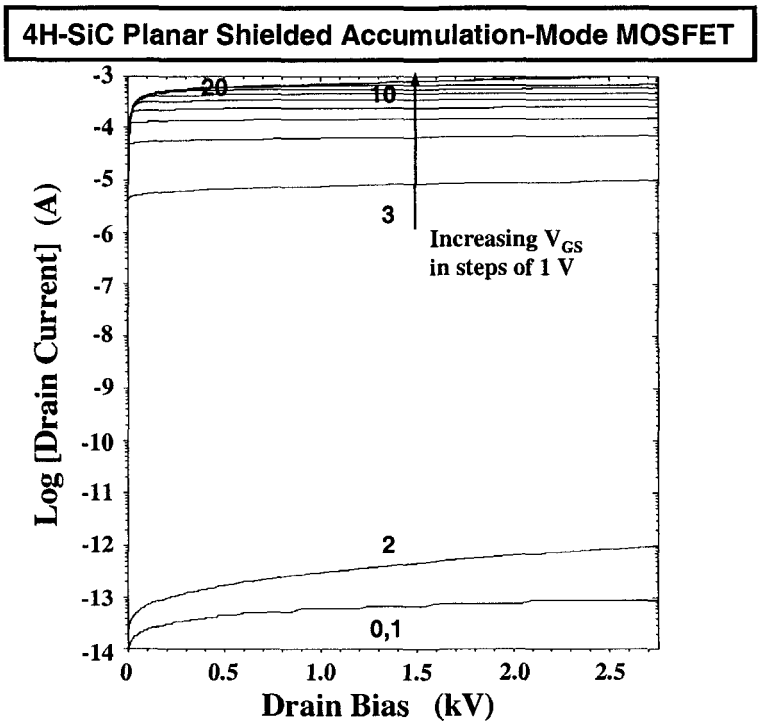

Fig. 10.24 Blocking Characteristics of the Planar 4H-SiC Shielded Accumulation-Mode MOSFET Structure.

As in the case of the inversion-mode structure, the P^+ region in the planar 4H-SiC shielded accumulation-mode MOSFET structure can isolate the surface under the gate oxide from the high electric fields developed in the drift region. In order to demonstrate this, a three-dimensional view of the electric field distribution is shown in Fig. 10.25 for this structure at a drain bias of 3000 volts with zero gate bias. The field distribution shown in this figure indicates that the electric field at the gate oxide is suppressed by the presence of the P^+ region to the same extent as for the inversion-mode structure. At the maximum blocking capability of the drift region, the electric field at the gate oxide interface has reached a magnitude of 1.5×10^6 V/cm while the electric field in the bulk has reached a magnitude of 3×10^6 V/cm.

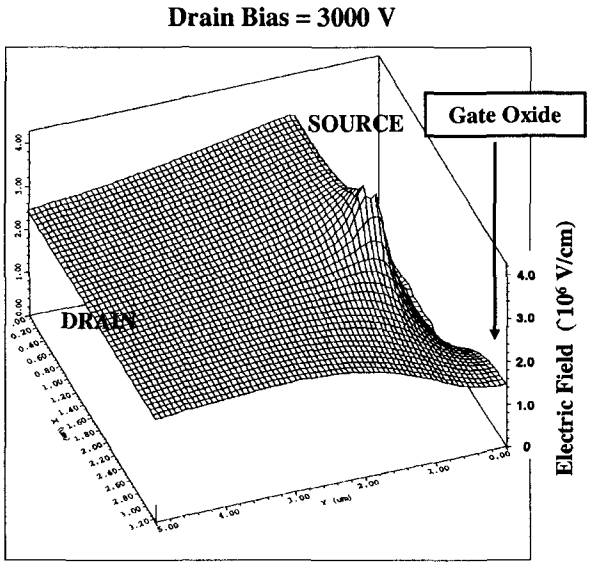

Fig. 10.25 Electric Field Distribution in the Planar 4H-SiC Shielded Accumulation-Mode MOSFET Structure.

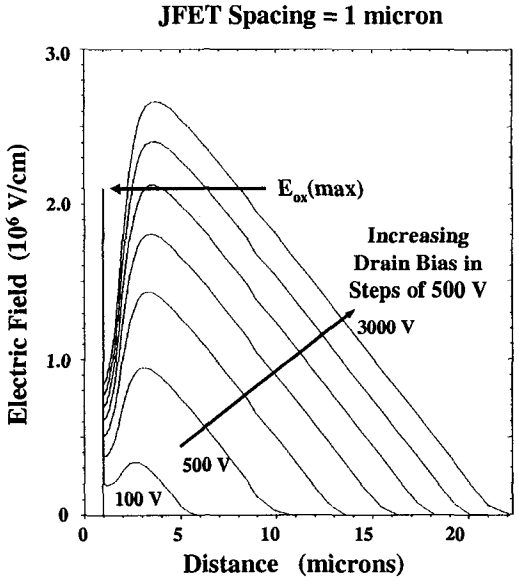

Fig. 10.26 Electric Field Distribution in the Planar 4H-SiC Shielded Accumulation-Mode MOSFET Structure.

In the planar 4H-SiC shielded accumulation-mode MOSFET structure, the largest electric field at the gate oxide interface occurs at the center of the JFET region. The behavior of this electric field with increasing drain bias was found to be identical to the profiles shown in Fig. 10.16 for the inversion-mode structure with the same JFET width of 1.5 microns. A further reduction of the electric field in the gate oxide can be achieved by reducing the width of the JFET region. In order to illustrate this, the electric field distribution is shown in Fig. 10.26 for the case of a planar 4H-SiC shielded accumulation-mode MOSFET structure with JFET width of 1 micron. It can be seen that the maximum electric field at the gate oxide interface is reduced to 8.5 x 10^5 V/cm resulting in a maximum electric field in the gate oxide of only 2.1 x 10^6 V/cm at a drain bias of 3000 volts. This value is sufficiently low for reliable operation of the structure especially due to the planar gate structure, where there are no localized electric field enhancements under the gate electrode.

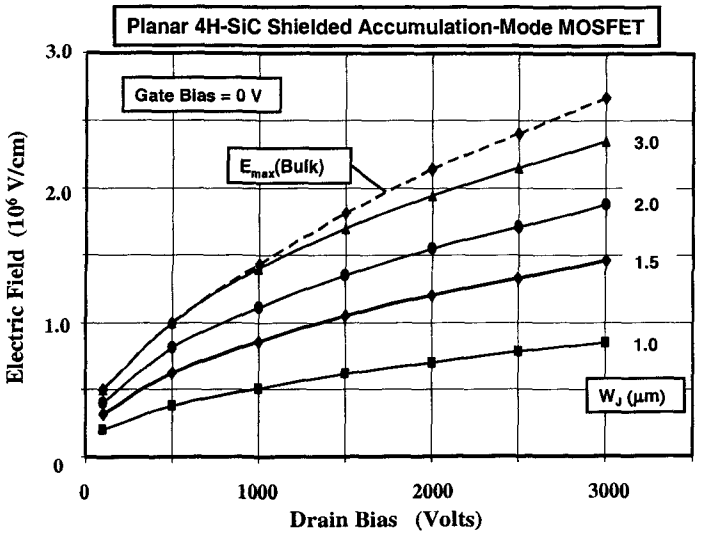

Fig. 10.27 Electric Field Suppression in the Planar 4H-SiC Shielded Accumulation-Mode MOSFET Structure.

The magnitude of the electric field developed in the vicinity of the gate oxide interface in the planar 4H-SiC shielded accumulation-mode MOSFET structure is dependent upon the width of the JFET region. The electric field at the gate oxide interface becomes smaller as

the JFET width is reduced as shown in Fig. 10.27. For the structure with a drift region doping concentration of 1 x 10^{16} cm^{-3}, the optimum spacing lies between 1 and 2 microns. The JFET width cannot be arbitrarily reduced because the resistance of the JFET region becomes very large when the width approaches the zero-bias depletion width of the P^+/N junction. For a drift region doping concentration of 1 x 10^{16} cm^{-3}, the zero-bias depletion width is approximately 0.6 microns. Consequently, using a JFET width of 1.5 microns provides adequate space in the JFET region for current flow as shown in the next section of the chapter.

10.3.2 Planar Shielded Accumulation-Mode MOSFET Structure: On-State Characteristics

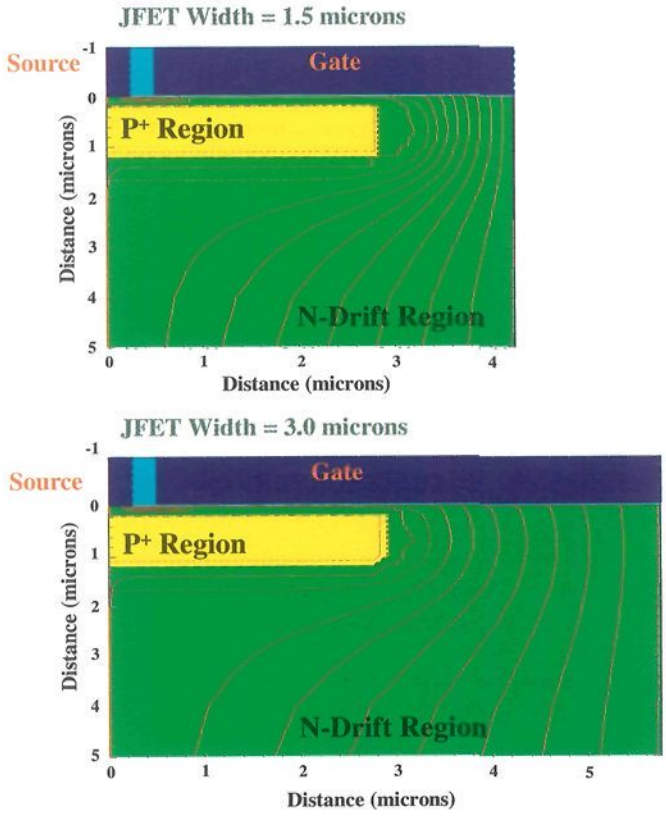

Fig. 10.28 On-State Current Distribution in the Planar 4H-SiC Shielded Accumulation-Mode MOSFET.

The on-resistance for the planar 4H-SiC shielded accumulation-mode structure was extracted by performing numerical simulations with a gate bias of 10 volts. The lower gate bias voltage, when compared with that used in the previous chapter for the unshielded inversion-mode structure, was chosen because of the smaller threshold voltage of these devices. A gate bias of 10 volts is a typical value for the available gate drive circuits used in medium and high power electronic systems. In addition, due to the improved channel resistance contribution, a channel length of 2 microns was also investigated because this provides greater margin when fabricating the devices.

The current distribution within the planar 4H-SiC shielded accumulation-mode MOSFET structure is shown in Fig. 10.28 for the case of JFET widths of 1.5 microns and 3 microns. These structures have a channel length of 2 microns. The absence of the P-type doping is apparent above the P^+ shielding region as is to be expected for an accumulation-mode structure. It can be seen that the current does not flow through the bulk of the N-base region and is confined to a channel formed below the gate oxide. This confirms the depletion of the N-base region by the built-in potential of the P^+/N junction, thus, preventing current flow through the bulk. In Fig. 10.28, the current is observed to flow from the accumulation layer channel into the JFET region and then spread into the drift region at a 45 degree angle. The current flow is not as severely constricted in the JFET region when the JFET width is increased from 1.5 to 3 microns.

Simulations to obtain the specific on-resistance of the planar 4H-SiC shielded accumulation-mode MOSFET structure were performed with different accumulation layer mobility values. The specific on-resistance was obtained by using a drain bias of 1 volt and sweeping the gate bias to 20 volts to obtain the transfer characteristic. A drain bias of 1 volt was used for these simulations because the on-state voltage drop for these structures is typically in this range. The specific on-resistance was computed by using the drain current extracted at a gate bias of 10 volts.

Typical transfer characteristics obtained using this method are shown in Fig. 10.29 for the device with JFET width of 1.5 microns and channel length of 1 micron. From the transfer characteristics, it can be seen that the threshold voltage that determines the on-resistance is approximately 3 volts, which is lower than for the shielded inversion-mode device structure (see Fig. 10.18). The impact of changing the channel accumulation mobility is shown in this figure. The mobility values chosen for these simulations extend to larger values because the

accumulation mobility measured in the literature is larger as discussed later in this chapter. As expected, there is a reduction in the drain current as the channel mobility is reduced.

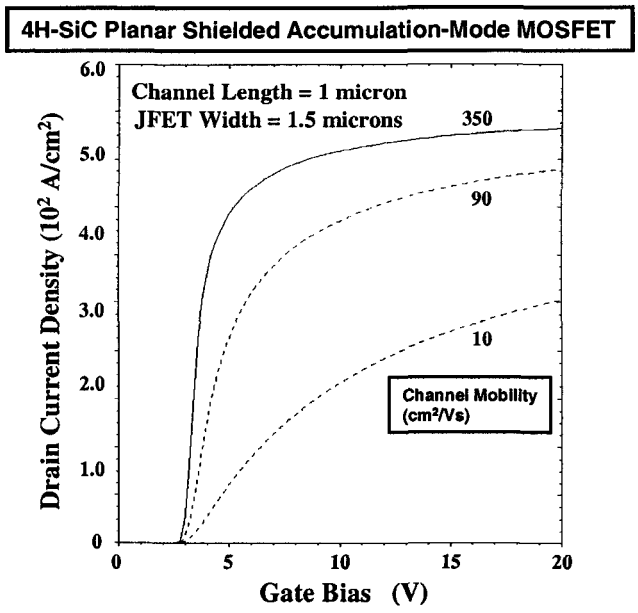

Fig. 10.29 Transfer Characteristics of the Planar 4H-SiC Shielded Accumulation-Mode MOSFETs.

When the accumulation layer mobility is assumed to be 350 cm^2/Vs, it can be noted from Fig. 10.29 that nearly the same drain current is obtained at a gate bias of 10 volts as at 20 volts. This demonstrates that it is possible to operate the planar 4H-SiC shielded accumulation-mode MOSFET structure with a gate bias of 10 volts. The specific on-resistance for the shielded 4H-SiC accumulation-mode MOSFET structure is found to be 2.4 $m\Omega\text{-}cm^2$ (after including a substrate contribution of 0.4 $m\Omega\text{-}cm^2$) which is the same as that obtained for the inversion-mode structure if an inversion layer mobility of 200 cm^2/Vs is assumed. This is because the channel resistance component for both structures becomes a small fraction of the total on-resistance for the 3 kV devices analyzed here. However, if the inversion layer mobility is low, as more commonly observed in the literature, the accumulation-mode structure will have a lower specific on-resistance. Thus, the

accumulation-mode structure provides an alternate approach to obtaining high performance MOSFETs in silicon carbide until consistently high inversion layer mobility can be reproducibly achieved when manufacturing these structures.

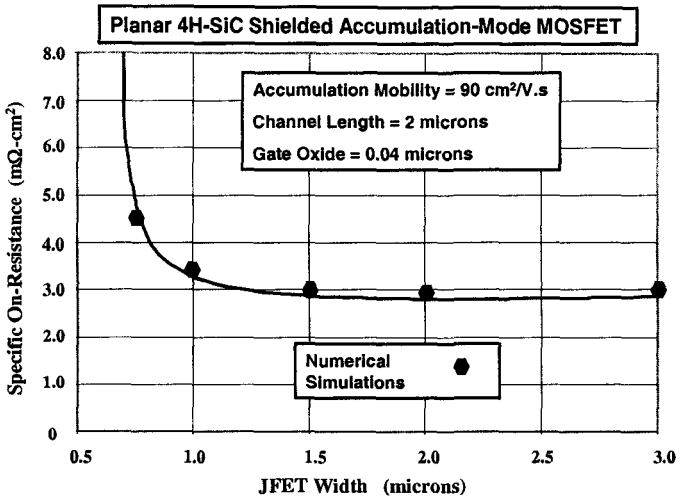

Fig. 10.30 Specific On-Resistances for the Planar 4H-SiC Shielded Accumulation-Mode MOSFETs.

The results of the specific on-resistance obtained from the simulations performed on planar 4H-SiC shielded accumulation-mode MOSFET structures with various JFET widths is shown in Fig. 10.30 together with the values obtained using the analytical model. These results are based upon using a channel mobility of 90 cm^2/Vs with a gate oxide thickness of 0.04 microns. A good agreement between the analytical model and the simulations provides further validation of the ability to predict specific on-resistance using the analytical model.

The optimization of the JFET width requires taking into consideration both the on-resistance and the electric field developed at the gate oxide interface. The relative changes in these parameters can be observed in Fig. 10.31 for the case of a device with channel length of 2 microns. A gate oxide thickness of 0.04 microns was used here with a channel mobility of 90 cm^2/V-s. It can be seen that the electric field in the semiconductor below the gate oxide can be reduced to less than 1 MV/cm when the JFET width is reduced to 1 micron with a degradation of the specific on-resistance by about 10 percent.

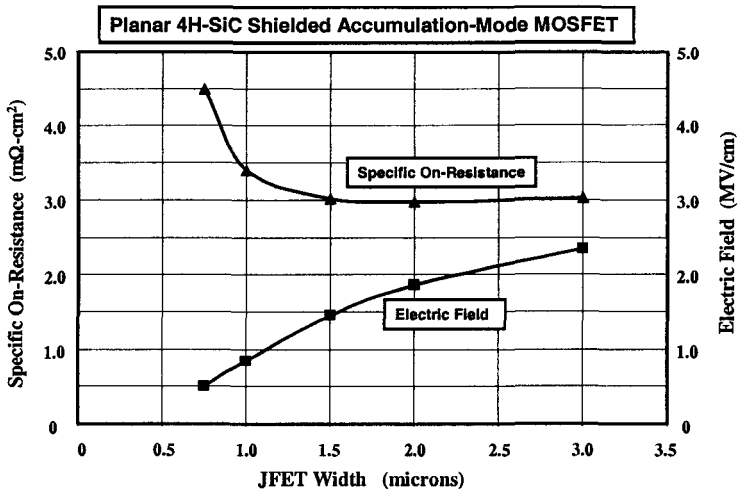

Fig. 10.31 Optimization of JFET Width in the Planar 4H-SiC Shielded Accumulation-Mode MOSFETs.

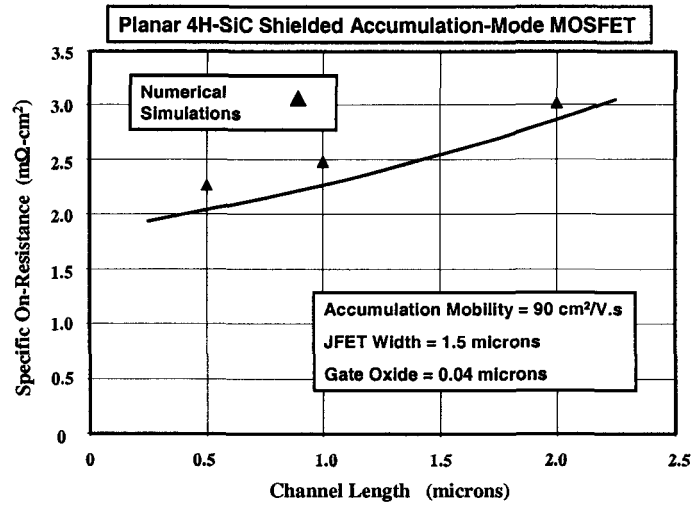

Fig. 10.32 Specific On-Resistances for the Planar 4H-SiC Shielded Accumulation-Mode MOSFETs.

As discussed in the earlier section, the planar 4H-SiC shielded accumulation-mode MOSFET structure was found to be capable of blocking high drain bias voltages even when the channel length is reduced to 0.5 microns. This creates the opportunity to reduce the

specific on-resistance by adjusting the channel length. The results of the specific on-resistance obtained from the simulations performed on planar 4H-SiC shielded accumulation-mode MOSFET structures with various channel lengths is shown in Fig. 10.32 together with the values obtained using the analytical model. These results are based upon using a channel mobility of 90 cm^2/Vs with a gate oxide thickness of 0.04 microns. A good agreement between the analytical model and the simulations provides further validation of the ability to predict specific on-resistance using the analytical model. With a channel length of 0.5 microns, the specific on-resistance for the planar 4H-SiC shielded accumulation-mode MOSFET structure is reduced to 2.3 mΩ-cm2, which is an extremely low value for a MOSFET capable of supporting 3000 volts.

10.3.3 Planar Shielded Accumulation-Mode MOSFET Structure: Output Characteristics

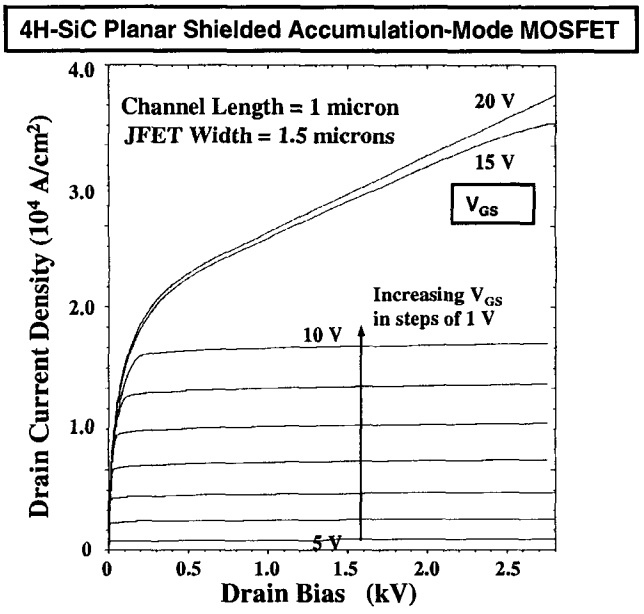

Fig. 10.33 Output Characteristics of a Planar 4H-SiC Shielded Accumulation-Mode MOSFET structure.

In a previous section, it was demonstrated that the shielding of the P-base region within the planar MOSFET structure suppresses the reach-through

breakdown problem. The shielding effect can also be expected to improve the output characteristics of the accumulation-mode power MOSFET structure because it suppresses the lowering of the potential barrier formed in the channel. With adequate suppression of channel current flow over the potential barrier, the drain current is controlled by the gate bias induced charge in the accumulation layer. The output characteristics for the shielded 4H-SiC accumulation-mode MOSFET should therefore be similar to those observed for the inversion-mode device.

The output characteristics for the shielded 4H-SiC accumulation-mode MOSFET structure were obtained by using two-dimensional numerical simulations with sweeping of the drain voltage at various gate bias voltages. The results obtained for a structure with channel length of 1 micron, gate oxide thickness of 0.04 microns, and a JFET width of 1.5 microns are shown in Fig. 10.33. The device structure exhibits excellent drain current saturation for gate bias voltages upto 10 volts with a very high output resistance. The saturated drain current increases as the square of the gate bias voltage, which is typical for MOSFETs that operate with channel pinch-off. For the gate bias values of 15 and 20 volts, a pronounced quasi-saturation region is observed similar to that for the inversion-mode structure. However, when taking into consideration the very high drain current density obtained even for a gate bias of 10 volts, it is not necessary to operate the planar 4H-SiC shielded accumulation-mode MOSFET with gate bias voltages above 10 volts. For the same gate bias voltage, the accumulation-mode structure exhibits a higher drain current than the inversion-mode structure due to its lower threshold voltage and increased channel mobility.

In the previous section, it was demonstrated that the channel length of the planar 4H-SiC shielded accumulation-mode MOSFET structure could be reduced to 0.5 microns without encountering a blocking problem. However, it is not obvious that current flow through the N-base region will not occur under the application of a positive gate bias. Any current flow through the N-base region will degrade the output resistance of the device. However, the output characteristics for the accumulation-mode structure with channel length of 0.5 microns, shown in Fig. 10.34, were found to be quite similar to those of longer channel devices in terms of the output resistance. This confirms the ability to support high voltages using a depleted N-base region without short channel effects. A slight increase in the transconductance for this structure is apparent as expected due to the reduced channel length.

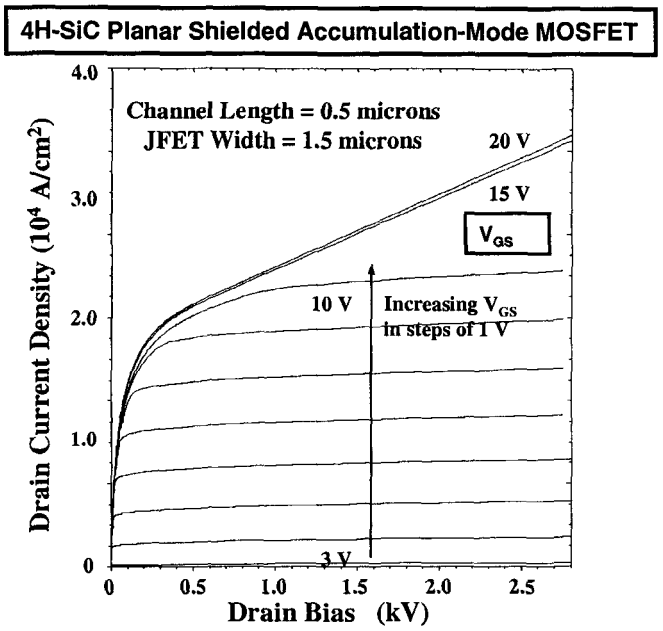

Fig. 10.34 Output Characteristics of a Planar 4H-SiC Shielded Accumulation-Mode MOSFET structure.

10.4 Planar Shielded MOSFET Structures: Experimental Results

As pointed out in the previous chapter, the need to obtain a high quality interface between silicon carbide and the gate dielectric was identified as a challenging endeavor from the inception of interest in the development of unipolar transistors from this semiconductor material[7]. Initially, it was impossible to fabricate silicon carbide power MOSFETs with specific on-resistances below those reported for silicon devices until the interface was sufficiently improved to obtain adequate inversion layer mobility. Even in recent years, poor inversion layer mobility values have been reported due to trapping of charge at the oxide-semiconductor interface. To overcome this technological barrier and to obtain a lower threshold voltage, the accumulation-mode structure was proposed[1]. This structure was also designed to shield the gate oxide from high electric fields in the semiconductor drift region. Experimental results on the shielded inversion-mode and accumulation-mode structures are discussed in this

section after reviewing results obtained on the accumulation layer mobility for 4H-SiC MOSFETs.

10.4.1 Silicon Carbide MOSFET: Accumulation Layer Mobility

Early investigations of the interface between P-type silicon carbide and thermally grown oxide indicated a high density of interface states and positive charge in the oxide. Significant improvement in the interface quality was achieved for 6H-SiC by anneal the thermally grown oxide in a NO ambient[8] leading to a peak inversion layer mobility of 70 cm^2/Vs. However, the inversion layer mobility for 4H-SiC was reported[9] to be less than 1 cm^2/Vs.

It has been established that the accumulation layer mobility is significantly greater than the inversion layer mobility in silicon MOSFET structures[10]. This encouraged the development of accumulation-mode MOSFETs in silicon carbide. The first planar accumulation-mode vertical power MOSFET structure, named the planar ACCUFET, was developed at PSRC using 6H-SiC as the semiconductor material[11]. The effective accumulation layer mobility extracted[12] from these structures was 120 cm^2/Vs for a structure fabricated using thermally grown gate oxide, which was considerably larger than the best inversion layer mobility (70 cm^2/Vs) reported[8] at that time.

More recently[13], the accumulation layer mobility has been measured in 4H-SiC MOSFETs using the Hall bar structure to differentiate between the effective mobility, which is limited by charge trapping, and the intrinsic mobility for free carriers in the channel. Note that the gate oxide process used for the fabrication of these MOSFETs was similar to that developed at PSRC[14] with the use of deposited oxides on 4H-SiC leading to a reported[15] record high inversion layer mobility of 165 cm^2/V-s. It was found that the accumulation mobility decreased from 350 cm^2/V-s in the weak accumulation regime of operation to 200 cm^2/V-s in the strong accumulation regime of operation. These results provided the justification for performing the simulations of the planar 4H-SiC shielded accumulation-mode MOSFET structures, as discussed in the previous section, using accumulation mobility values ranging upto 350 cm^2/V-s. However, the effective accumulation-layer mobility was found to be only 3-5 cm^2/V-s indicating substantial trapping of electrons at the gate oxide interface.

Better effective accumulation mobility values have been reported for 4H-SiC MOSFETs by using thermally grown oxide. In 1999, an

effective accumulation-layer mobility of 20-30 cm^2/V-s was reported[16] by using nitrogen ion implantation to form the N-base region. In 2001, a significantly larger accumulation-layer effective mobility of 200 cm^2/V-s was reported[17] by using a stacked gate oxide process. The stacked gate oxide consisted of a thermally grown layer with thickness of 0.02 microns followed by a NSG-CVD deposited layer with a thickness of 0.03 microns. These results have established the ability to obtain relatively high accumulation-layer mobility in 4H-SiC indicating the possibility for fabrication of high performance vertical power MOSFETs from this material.

The accumulation-mode power MOSFET structure was proposed to circumvent the problem of low inversion-layer mobility observed in 4H-SiC in the early studies with this material. However, in recent years, considerable progress has been made to improve upon the inversion-layer mobility. Exceptionally high inversion-layer mobility was achieved at PSRC by using a deposited oxide that was subsequently annealed in a wet oxidation ambient[14,15]. A detailed study[18] of the process steps responsible for producing the improved interface resulting in the high channel mobility was also undertaken at PSRC. This work produced the first observation of phonon scattering limited inversion layer mobility (which decreased with increasing temperature), and demonstrated that a wet oxide anneal of the deposited oxide was the critical step for producing the high inversion layer mobility. The process proposed and demonstrated at PSRC was subsequently reproduced by the sponsors[19] as well by other research groups[20]. These results indicate that it is possible to achieve sufficiently high inversion layer mobility in 4H-SiC power MOSFETs to obtain low specific on-resistance in high voltage structures.

The low inversion layer mobility observed in 4H-SiC MOSFETs fabricated using thermally grown gate oxides has been traced to the trapping of the carriers at interface states. Hall effect measurements performed on lateral MOSFETs have demonstrated that the effective Hall mobility for carriers in the inversion layer is high when the trapping effect is taken into consideration[21]. Due to the trapping effect, as recently as 2001, the measured effective mobility in 4H-SiC MOSFETs has been reported[22] to be less than 10 cm^2/V-s when thermal oxidation is used to form the gate oxide. In these devices, the effective mobility was found to increase with temperature which is a signature of trap dominated current conduction in the channel. By using NO ambient anneals of the thermally grown gate oxide, an improvement in the effective channel mobility to 30-35 cm^2/V-s has been reported[23] in 2001.

In summary, inversion-layer effective mobility values in the range of 30-35 cm^2/V-s have been observed in 4H-SiC MOSFETs while significantly larger effective accumulative-layer mobility values of 200 cm^2/V-s have been observed in this material. These values indicate that it is possible to develop high voltage 4H-SiC power MOSFETs using either the inversion-mode or accumulation-mode architecture if the base is shielded from the high electric field in the drift region. The accumulation-mode structure is favored for designs with low channel density where the channel contribution becomes a significant fraction of the total on-resistance.

10.4.2 The Planar 4H-SiC Inversion-Mode MOSFET Structure: Experimental Results

As already mentioned earlier in the previous chapter, in recognition of the low diffusion coefficients for dopants in silicon carbide, it was proposed[24] that the P-base and N^+ source ion implantations for the planar silicon carbide power MOSFET be staggered by using photoresist masks rather that be defined by the gate edge as conventionally done for silicon devices. The idea to incorporate a sub-surface P-type layer to shield the channel was also proposed at PSRC and subsequently patented[1]. This idea was first successfully demonstrated[25] for 6H-SiC devices in 1997 under the DI-MOSFET moniker. The authors fabricated the devices using multiple energy boron implants to form a P-base region with a box profile at a depth of 1 micron. The energy and dose for the implants was chosen to produce a retrograde doping profile on one of the wafers. This creates a low doped P-base region with an under-lying highly doped P^+ region that shields it from the high electric fields developed in the drift region. However, the devices with retrograded doping profile had inferior breakdown when compared with the box profile indicating that the design did not provide adequate shielding.

The concept of shielding the P-base region has also been reported[26] using a triple ion-implantation process to fabricate 6H-SiC vertical power MOSFETs. The ion-implant steps were designed to produce a low P-base surface concentration of 7×10^{16} cm^{-3} with the doping increasing to 1×10^{18} cm^{-3} at a depth of 0.4 microns. This profile enabled achieving a threshold voltage of 3 volts with a thermally grown gate oxide thickness of 0.036 microns. A breakdown voltage of 1800 volts was obtained for this device by using a drift region doping concentration of 6.5×10^{15} cm^{-3} and thickness of 15 microns. A specific

on-resistance of 82 mΩ-cm^2 was observed at a gate bias of 10 volts, which is an order of magnitude better than values that can be obtained with silicon technology. Good dynamic switching performance with ruggedness has been confirmed[27] for these MOSFETs.

Recently, a novel staggered implant process has been proposed to reduce the channel length and applied towards the fabrication of high voltage planar 4H-SiC MOSFETs[28]. In this process, oxidation of a sacrificial polysilicon layer is used to form a sidewall spacer that serves as a mask to stagger the P-base and N^+ source implants. The retrograde ion implant profile discussed earlier was also utilized for these devices to reduce the P-base doping concentration and suppress the reach-through problem. Planar 4H-SiC inversion-mode MOSFETs were successfully fabricated with breakdown voltage of 2 kV with a specific on-resistance of 27 mΩ-cm^2 at a gate bias of 20 volts.

10.4.3 The 4H-SiC Accumulation-Mode Planar MOSFET Structure: Experimental Results

The first planar shielded accumulation-mode MOSFET structure was fabricated[11] from 6H-SiC at PSRC in 1997. This device, named the planar ACCUFET, was conceived to circumvent the problems observed with obtaining high inversion layer mobility as well as to screen the channel and gate oxide from high electric fields developed in the drift region. The devices were fabricated using a drift region with doping concentration of 1 x 10^{16} cm^{-3} and thickness of 10 microns, corresponding to a breakdown voltage of 1500 volts. The sub-surface P^+ region used to shield the channel and gate oxide was formed by a single boron ion implant with energy of 380 keV and dose of 1 x 10^{14} cm^{-2}. This produced an N-base region with thickness of about 0.3 microns. The gate oxide with thickness of 0.0125 microns was formed using thermal oxidation followed by a re-oxidation anneal.

The un-terminated devices had a breakdown voltage of 350 volts. For the structure with cell pitch of 21 microns (channel length of 2.5 microns and JFET width of 4 microns), a specific on-resistance of 18 mΩ-cm^2 was measured at a gate bias of only 5 volts. This was possible because of the low threshold voltage (~ 1 volt) and high transconductance of the structure achieved with the small gate oxide thickness. The measured specific on-resistance was within 2.5 times the specific on-resistance of the drift region (8 mΩ-cm^2) despite the rather large cell pitch. In spite of the very thin gate oxide, no evidence of gate

rupture was observed in the blocking state due to the shielding by the P^+ region. The measured specific on-resistance for these MOSFETs is about 30 times smaller than that for silicon MOSFETs with blocking voltage capability of 1500 volts.

A detailed analysis[29] of the operation and design of the 6H-SiC ACCUFET was published in 1999. In this paper, it was pointed out that a trade-off between reducing the electric field at the gate oxide and minimizing the specific on-resistance must be performed. It was also found that the specific on-resistance for the ACCUFET increases with increasing temperature. This had not been previously observed in silicon carbide power MOSFETs because the channel conductance improved rapidly with temperature due to trap limited effective inversion-layer mobility. In contrast, the extracted accumulation-layer mobility was found to remain independent of temperature resulting in a positive temperature coefficient for the specific on-resistance due to increase in resistance of the bulk components.

The ACCUFET structure has also been successfully fabricated using 4H-SiC with high blocking voltage capability[30]. These devices were labeled SIAFETs even though the operating principle for the devices was acknowledged by the authors to be identical to that of ACCUFET structures. The authors achieved a blocking voltage capability of 4580 volts with normally-off operation at zero gate bias by using a drift region with a doping concentration of 5×10^{14} cm^{-3} and thickness of 75 microns. These devices exhibited a specific on-resistance of 1200 $m\Omega\text{-}cm^2$ in spite of using a gate bias of 40 volts because of a low accumulation-layer mobility of 0.5 $cm^2/V\text{-}s$. The specific on-resistance was found to reduce by a factor of 6 times by the application of a positive bias to the sub-surface P^+ region. Unfortunately, this entails a more complex package and gate drive circuit for the devices that departs from mainstream silicon technology. The performance of this structure, renamed SEMOSFET, has been extended[31] to a 5 kV blocking voltage capability with a specific on-resistance of 88 $m\Omega\text{-}cm^2$ in the presence of a positive bias of 2 volts applied to the buried P^+ region with 20 volts applied to the MOS-gate electrode. Since the bias applied to the buried P^+ region was less than the junction potential, these is no minority carrier injection from the P^+ region. Consequently, these devices exhibit very fast switching speeds with turn-on and turn-off times of less than 50 nanoseconds while operating at on-state voltage drops slightly less than that for a 4.5 kV IGBT.

10.5 Summary

In this chapter, it has been established that the incorporation of a sub-surface P^+ region into the planar MOSFET structure enables shielding the P-base region from reach-through limited breakdown and preventing high electric fields from developing across the gate oxide during the blocking mode. Since relatively low inversion layer mobility has been reported for 4H-SiC MOSFETs, an accumulation-mode structure was proposed with an N-base region that is completely depleted by the built-in potential of the underlying P^+/N junction. This structure takes advantage of the much larger accumulation mobility observed in semiconductors.

The operating principle of the planar shielded MOSFET structures has been reviewed in the chapter providing guidelines for the design of the structures. It has been demonstrated that the JFET width is a critical parameter that controls the electric field at the gate oxide interface as well as the specific on-resistance. Its optimization is important for obtaining high performance devices. In the case of the accumulation-mode structure, the appropriate combination of the doping concentration and thickness of the N-base region must be chosen to ensure that it is completely depleted by the built-in potential of the underlying P^+/N junction. With adequate shielding of the base region, it is found that short channel devices will support high blocking voltages limited only by the properties of the drift region. These devices have excellent safe-operating-area and fast switching speed. This technology has potential for use in systems operating at upto at least 5000 volts.

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Chapter 11

Trench-Gate Power MOSFETs

The silicon trench-gate power MOSFET was developed in the 1990s by borrowing the trench technology originally developed for DRAMs. Before the introduction of the trench-gate structure, it was found that the ability to reduce the specific on-resistance for silicon power MOSFETs was constrained by the poor channel density and the JFET region resistance[1]. Although the use of more advanced lithographic design rules enabled a steady reduction of the specific on-resistance in the 1970s and early 1980s, the improvements to the DMOSFET structure were saturating[2]. The trench-gate or UMOSFET structure enabled significant increase in the channel density and elimination of the JFET resistance contribution resulting in a major enhancement in low voltage (<50 volt) silicon power MOSFET performance. The first trench-gate devices[3,4] were fabricated in the mid-1980s and shown to have significantly lower specific on-resistance than the DMOSFET structure. However, problems with controlling the quality of the trench surface and oxide reliability problems needed to be solved before the introduction of commercial devices. Eventually, this technology overtook the planar DMOSFET technology in the 1990s and has now taken a dominant position in the industry for serving portable appliances, such as laptops, PDAs, etc.

In the silicon power DMOSFET structure, the channel and JFET resistances were found to become the dominant components when the breakdown voltage was reduced below 50 volts because of the low resistance of the drift region. Due to the much lower specific on-resistance for the drift region in silicon carbide, the channel and JFET contributions become dominant even when the breakdown voltage approaches 5000 volts, especially if the channel mobility is poor. This has motivated the development of the trench-gate architecture in silicon carbide. In addition, the P-base region for the trench-gate device could be fabricated using epitaxial growth which was at a more advanced state

than the ability to use ion implantation to create P-type layers in silicon carbide.

This chapter reviews the basic principles of operation of the trench-gate MOSFET structure. The specific on-resistance for this structure is shown to be significantly lower than that for the DMOSFET structure. However, the gate oxide in the UMOSFET structure is exposed to the very high electric field developed in the silicon carbide drift region during the blocking-mode. This is a major limitation to adopting the basic UMOSFET structure from silicon to silicon carbide. Consequently, structures designed to reduce the electric field at the gate oxide by using a shielding region are essential to realization of practical silicon carbide MOSFET structures[5]. These structures are described and analyzed in the next chapter. In this chapter, the results of the analysis of the basic trench-gate silicon carbide MOSFET structure by using two-dimensional numerical simulations are provided followed by the description of experimental results on relevant structures to define the state of the development effort on these devices.

11.1 Trench-Gate Power MOSFET Structure

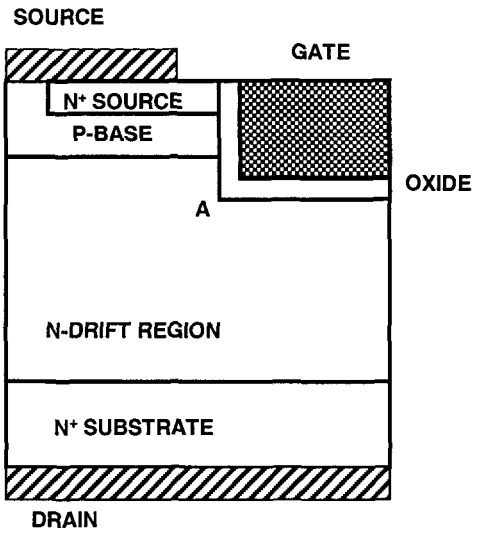

Fig. 11.1 The Trench-Gate Power MOSFET Structure.

The basic structure of the trench-gate power MOSFET is shown in Fig. 11.1. The structure can be fabricated by either the epitaxial growth of the P-base region over the drift region or by introducing the P-type dopants using ion-implantation. The first 4H-SiC UMOSFET structure was fabricated by the epitaxial growth of the P-base region due to problems with activation of P-type ion implanted dopants in silicon carbide[6]. However, this requires either removal of the P-type layer on the edges of the structure to form a mesa edge termination[6] or multiple trench-isolated guard rings[7]. The trench-gate structure was fabricated by using reactive-ion etching to form the U-shaped trenches. The gate oxide was then created by thermal oxidation followed by refilling the trench with polysilicon as done for silicon UMOSFET structures.

Note that the P-base region is short-circuited to the N^+ source region by the source metal. Although this is routinely done in silicon devices using a common ohmic contact metal for both the N^+ and P-type regions, this has been difficult to achieve in silicon carbide. It is usual to use different metals to form the ohmic contact to silicon carbide, typically with titanium for N-type regions and aluminum for P-type regions. In this case, it may be preferable to short circuit the source-base junction at a location orthogonal to the cross-section shown in the figure. This is also advantageous for reducing the cell pitch which results in a larger channel density.

11.1.1 Trench-Gate Power MOSFET Structure: Blocking Characteristics

When the trench-gate power MOSFET is operating in the forward blocking mode, the voltage is supported by a depletion region formed on both sides of the P-base/N-drift junction. The maximum blocking voltage can be determined by the electric field at this junction becoming equal to the critical electric field for breakdown if the parasitic N^+/P/N bipolar transistor is completely suppressed. This suppression is accomplished by short-circuiting the N^+ source and P-base regions using the source metal as shown on the upper left hand side of the cross-section. However, a large leakage current can occur when the depletion region in the P-base region reaches-through to the N^+ source region. The doping concentration and thickness of the P-base region must be designed to prevent the reach-through phenomenon from limiting the breakdown voltage. The physics governing the reach-through process is identical to that already described in chapter 9 for the planar MOSFET structure.

Consequently, the design rules provided earlier with the aid of Fig. 9.3 can be applied to the trench-gate structure as well. This implies that the minimum channel length required for the silicon carbide trench-gate devices is much larger than for silicon resulting in a substantial increase in the on-resistance. The degradation of the on-resistance is compounded by the lower channel inversion layer mobility observed for silicon carbide.

The minimum thickness of the P-base region required to prevent reach-through breakdown decreases with increasing doping concentration as shown in Fig. 9.3. For 4H-SiC, it is necessary to increase the P-base doping concentration to above 2 x 10^{17} cm^{-3} to prevent reach-through with a 1 micron P-base thickness. This higher doping concentration increases the threshold voltage as already discussed in chapter 9.

The maximum blocking voltage capability of the trench-gate MOSFET structure is determined by the drift region doping concentration and thickness as already discussed in chapter 3. However, in the trench-gate MOSFET structure, the gate extends into the drift region exposing the gate oxide to the high electric field developed in the drift region under forward blocking conditions. For 4H-SiC, the electric field in the oxide reaches a value of 9 x 10^6 V/cm when the field in the semiconductor reaches its breakdown strength. This value not only exceeds the reliability limit but can cause rupture of the oxide leading to catastrophic breakdown. The problem is exacerbated by electric field enhancement at the corners of the trenches at location A in the figure. Novel structures[5] that shield the gate oxide from high electric field have been proposed and demonstrated to resolve this problem. These structures are discussed in the next chapter.

11.1.2 Trench-Gate Power MOSFET Structure: Forward Conduction

Current flow between the drain and source can be induced by creating an inversion layer channel on the surface of the P-base region. The current path is illustrated in Fig. 11.2 by the dotted area. The current flows from the source region into the drift region through the inversion layer channel formed on the vertical side-walls of the trench due to the applied gate bias. It then spreads into the N-drift region from the bottom of the trench at a 45 degree angle and becomes uniform through the rest of the structure. The total on-resistance for the trench-gate power MOSFET

structure is determined by the resistance of these components in the current path:

$$R_{on,sp} = R_{CH} + R_D + R_{subs} \qquad [11.1]$$

where R_{CH} is the channel resistance, R_D is the resistance of the drift region after taking into account current spreading from the channel, and R_{subs} is the resistance of the N^+ substrate. These resistances can be analytically modeled by using the current flow pattern indicated by the shaded regions in Fig. 11.2.

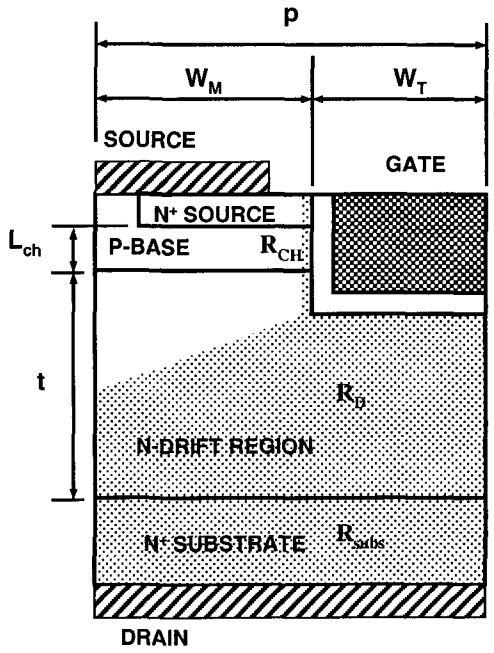

Fig. 11.2 Current Flow Path in the Trench-Gate 4H-SiC Power MOSFET.

The specific channel resistance is given by:

$$R_{CH} = \frac{(L_{CH} \cdot p)}{\mu_{inv} C_{ox} (V_G - V_T)} \qquad [11.2]$$

where L_{CH} is the channel length determined by the width of the P-base region as shown in Fig. 11.2, μ_{inv} is the mobility for electrons in the inversion layer channel, C_{ox} is the specific capacitance of the gate oxide,

V_G is the applied gate bias, and V_T is the threshold voltage. The specific capacitance can be obtained using:

$$C_{ox} = \frac{\varepsilon_{ox}}{t_{ox}} \qquad [11.3]$$

where ε_{ox} is the dielectric constant for the gate oxide and t_{ox} is its thickness.

The drift region spreading resistance can be obtained by using:

$$R_D = \rho_D . p . \ln\left(\frac{p}{W_T}\right) + \rho_D . (t - W_M) \qquad [11.4]$$

where t is the thickness of the drift region below the P- base region and W_T, W_M are the widths of the trench and mesa regions, respectively, as shown in the figure.

The contribution to the resistance from the N^+ substrate is given by:

$$R_{subs} = \rho_{subs} . t_{subs} \qquad [11.5]$$

where ρ_{subs} and t_{subs} are the resistivity and thickness of the substrate, respectively. A typical value for this contribution is 4×10^{-4} Ω-cm^2.

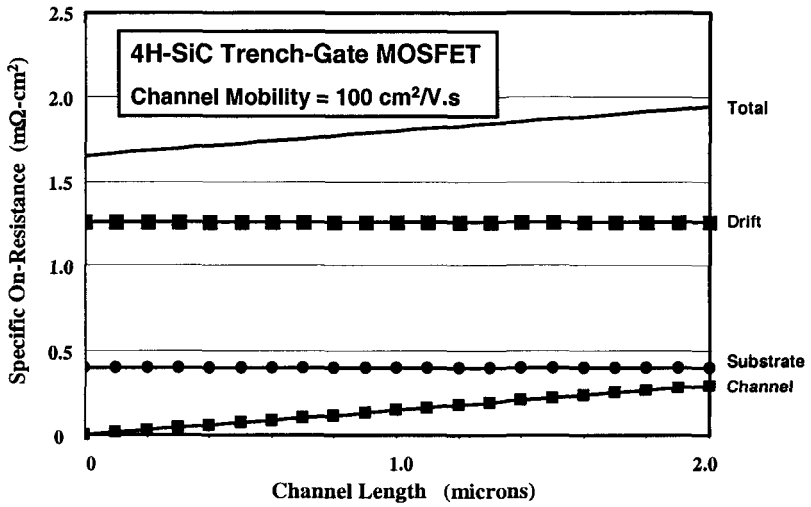

Fig. 11.3 On-Resistance Components for a 4H-SiC Trench-Gate MOSFET.

The specific on-resistances of 4H-SiC trench MOSFETs with a drift region doping concentration of 1 x 10^{16} cm^{-3} and thickness of 20 microns, capable of supporting 3000 volts, were modeled using the above analytical expressions. Since the trench-gate structure offers the opportunity to reduce the specific on-resistance with aggressive scaling, a gate oxide thickness of 0.05 microns was used. The mesa width (W_M) and trench width (W_T) for the structure shown in Fig. 11.2 were kept at 0.25 microns. These values can be achieved using 0.5 micron design rules. The effective gate drive voltage ($V_G - V_T$) was assumed to be 5 volts based upon a gate drive voltage of 10 volts and a threshold voltage of 5 volts. This threshold voltage is consistent with the model described in chapter 9 for the inversion-mode 4H-SiC MOSFET.

The various components of the on-resistance are shown in Fig. 11.3 when a channel inversion layer mobility of 100 cm^2/Vs was used. Inversion layer mobility values greater than this have been experimentally observed[8] in planar 4H-SiC MOSFET structures indicating the possibility to achieve them in trench gate devices as well. Note that only the channel resistance increases with increasing channel length. The other components are unaffected by the increase in channel length because the cell pitch remains unaltered. It can be seen that the drift region resistance is dominant here. At a channel length of 1 micron, a total specific on-resistance of 1.8 $m\Omega\text{-}cm^2$ is obtained, which is within two times the ideal specific on-resistance of the drift region.

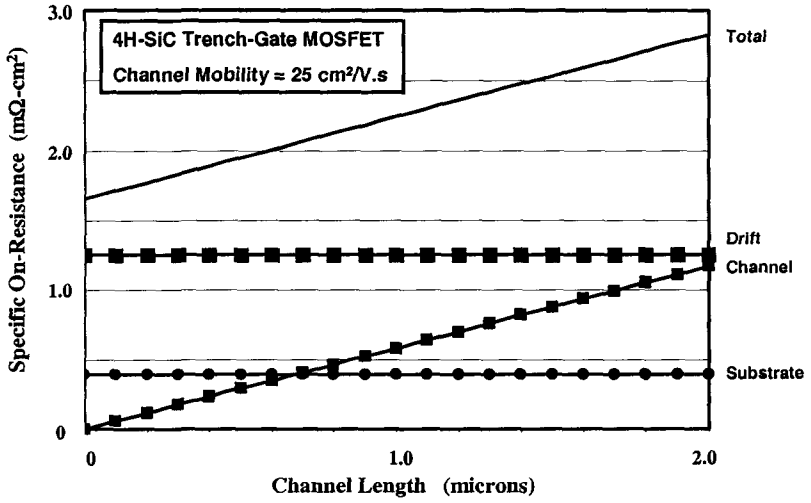

Fig. 11.4 On-Resistance Components for a 4H-SiC Trench-Gate MOSFET.

The above results are based upon using a channel mobility of 100 cm^2/Vs. Since most groups working on silicon carbide have reported much lower magnitudes for the inversion layer mobility in 4H-SiC structures[9], the impact of reducing the inversion layer mobility for the trench-gate MOSFET structure is depicted in Fig. 11.4 and 11.5 for the case of mobility values of 25 and 2.5 cm^2/Vs. With an inversion layer mobility of 25 cm^2/Vs, the channel contribution becomes comparable to the contribution from the drift region. This results in the specific on-resistance increasing to a value of 2.3 $m\Omega\text{-}cm^2$ for a channel length of 1 micron. When the inversion layer mobility is reduced to 2.5 cm^2/Vs, the channel resistance becomes dominant as shown in Fig. 11.5, with an increase in the specific on-resistance to a value of 7.5 $m\Omega\text{-}cm^2$ for a channel length of 1 micron.

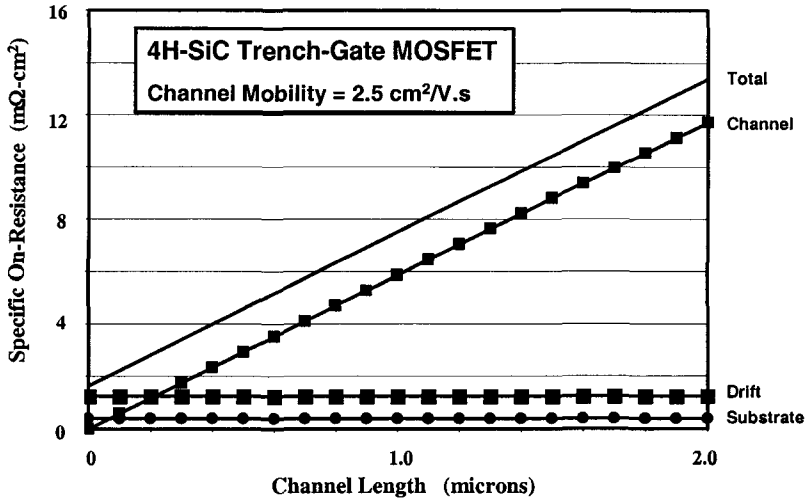

Fig. 11.5 On-Resistance Components for a 4H-SiC Trench-Gate MOSFET.

These results indicate that the channel resistance can become dominant even in the trench-gate MOSFET structure despite the high channel density if the inversion layer mobility is low. The relative contribution from the channel resistance in the trench-gate MOSFET structure depends upon the drift region resistance which is a function of the breakdown voltage of the device. In order to provide a better understanding of this, consider a 4H-SiC trench-gate MOSFET with a cell pitch of 0.5 microns (based upon 0.5 micron design rules), channel

length of 1 micron and gate oxide thickness of 0.1 microns, while the properties of the underlying drift region are adjusted to obtain the desired breakdown voltage. Since the threshold voltage for this oxide thickness is about 15 volts, the gate drive voltage was assumed to be 20 volts in this analysis. The specific on-resistance for this trench-gate 4H-SiC MOSFET structure is plotted in Fig. 11.6 as a function of the breakdown voltage using a channel mobility of 25 cm^2/V-s. In performing this modeling, it is important to recognize that the thickness of the drift region (parameter 't' in Fig. 11.2) can become smaller than the mesa width (W_M) at lower breakdown voltages (below 600 volts). Under these conditions, the current does not distribute at a 45 degree angle into the drift region from the bottom of the trench. Instead, the current flows from a cross-sectional width of (W_T) to a cross-section of ($p = W_M + W_P$). The drift region resistance for these cases can be modeled using:

$$R_D = \rho_D . p . \ln\left(\frac{p}{W_T}\right) \qquad [11.6]$$

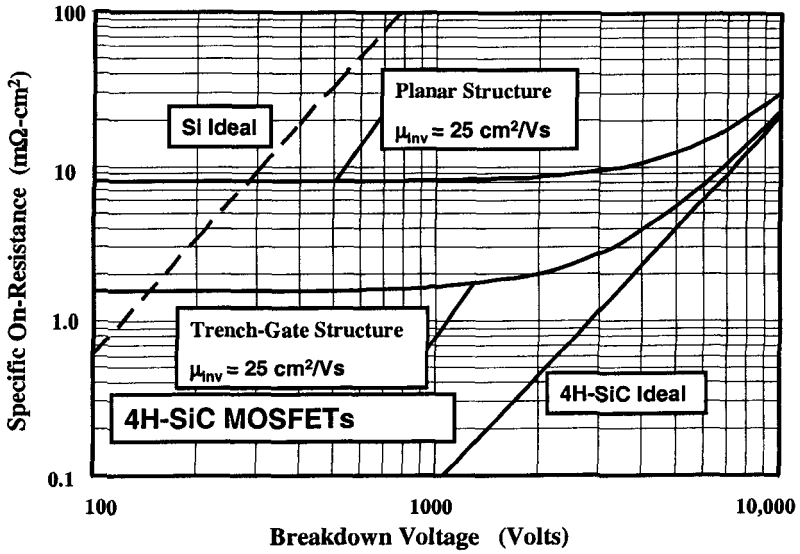

Fig. 11.6 Specific On-Resistance for 4H-SiC Trench-gate MOSFETs.

From Fig. 11.6, it can be concluded that the specific on-resistance of 4H-SiC trench-gate MOSFETs approaches the ideal specific on-resistance when the breakdown voltage exceeds 5000 volts even with a channel mobility of 25 cm^2/V-s. However, the channel resistance limits the performance of the trench-gate 4H-SiC MOSFET structure when the breakdown voltage falls below 1000 volts. For the case of a breakdown voltage of 1000 volts, the anticipated improvement in specific on-resistance over silicon power MOSFETs is then about 100 times (as opposed to the 2000x improvement in the specific on-resistance of the drift region). For a better perspective, the performance of the planar 4H-SiC inversion-mode MOSFET structure is also shown in the figure. The planar MOSFET analysis was based upon using the same channel length, gate oxide thickness, and channel mobility of 25 cm^2/V-s as the trench-gate structure. A cell-pitch of 3 microns was used for the planar structure based upon the same 0.5 micron design rules. It can be seen that the trench-gate structure offers a substantial (5-fold) reduction of the specific-on-resistance due to the higher channel density. These results highlight the need for development of aggressive processing techniques, like those routinely used for low voltage silicon power UMOSFET structures, to achieve a small cell pitch in the trench-gate 4H-SiC MOSFET structure.

The on-resistance model presented in this section was originally described[10] to highlight the importance of improving the channel inversion layer mobility for silicon carbide trench-gate MOSFETs. This model assumes that all the applied drain bias is supported within the N-drift region. For devices with lower breakdown voltages, the doping concentration in the N-drift layer becomes comparable to that for the P-base region. Consequently, a substantial fraction of the applied drain bias is supported within the P-base region as well. A model for the specific on-resistance that takes this into consideration indicates further reduction of the specific on-resistance[11]. However, the specific on-resistance of the trench-gate structure is still limited by the channel inversion layer mobility for devices designed to support 1000 volts.

11.1.3 Trench-Gate Power MOSFET Structure: Threshold Voltage

The threshold voltage of the trench-gate MOSFET structure is determined by the doping concentration of the P-base region along the sidewalls of the trench region. A minimum threshold voltage must be maintained at above 1 volt for most system applications to provide

immunity against inadvertent turn-on due to voltage spikes arising from noise. At the same time, a high threshold voltage is not desirable because the voltage available for creating the charge in the channel inversion layer is determined by $(V_G - V_T)$ where V_G is the applied gate bias voltage and V_T is the threshold voltage. Most power electronic systems designed for high voltage operation (the most suitable application area for silicon carbide devices) provide a gate drive voltage of only upto 10 volts. Based upon this criterion, the threshold voltage should be kept below 3 volts in order to obtain a low channel resistance contribution.

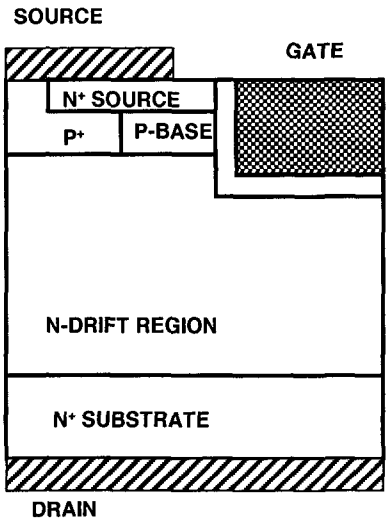

Fig. 11.7 Enhanced Trench-Gate Power MOSFET Structure.

The threshold voltage for the trench-gate inversion-mode MOSFET structure can be modeled using the same physics described in chapter 9 for the planar gate inversion-mode MOSFET structure. The threshold voltage for 4H-SiC devices can be obtained using the graphs provided in that chapter. Based upon that analysis, it is preferable to use a gate oxide thickness of 0.05 microns and a P-base doping concentration of 1×10^{17} cm^{-3} to obtain a threshold voltage of about 5 volts. However, the low P-base doping concentration can lead to a reach-through induced breakdown problem as discussed in chapter 9. A structural enhancement that can circumvent this problem is shown in Fig. 11.7. A P^+ region is incorporated into the trench-gate MOSFET structure under the source

region to suppress the extension of the depletion region in this portion of the cell structure. A relatively thin, lightly doped P-base region is formed adjacent to the trench sidewalls to determine the threshold voltage. It has been found (see simulation section in this chapter) that the presence of the P^+ region also suppresses reach-through within the adjacent P-base region allowing the structure to support high drain voltages upto the breakdown voltage capability of the drift region.

11.2 Trench-Gate Power MOSFET Structure: Numerical Simulations

In order to gain insight into the operation of the trench-gate 4H-SiC power MOSFET structure, two-dimensional numerical simulations were performed with a drift region doping concentration of 1×10^{16} cm^{-3} and thickness of 20 microns corresponding to a parallel-plane breakdown voltage of 3000 volts. The baseline device had a gate oxide thickness of 0.05 microns. The P^+ and P-base regions had a depth of 1 micron. The N^+ source region had a depth of 0.1 microns leading to a channel length of 0.9 microns. The mesa and trench width were chosen to be 0.5 microns. The P^+ region occupied half of the mesa width leaving the other half for the lightly doped P-base region with a doping concentration of 9×10^{16} cm^{-3}. This is compatible with a fabrication design rule of 0.5 microns. A trench depth of 1.5 microns was chosen to ensure that the gate electrode extended past the depth of the P-base region.

11.2.1 Trench-Gate Power MOSFET Structure: Blocking Characteristics

The blocking capability of the trench-gate 4H-SiC power MOSFET structure was investigated by maintaining zero gate bias while increasing the drain voltage. It was found that the device could sustain a drain bias of upto 3000 volts, as shown in Fig. 11.8, without any reach-through current despite the low P-base doping concentration. A low leakage current is observed for gate bias voltages ranging from 0 to 5 volts with current increasing at a gate bias of 6 volts. This indicates that the threshold voltage is about 5 volts. Unlike the planar 4H-SiC inversion-mode structure described in chapter 9, there is no reach-through induced current in the trench-gate device because of the incorporation of the P^+ region.

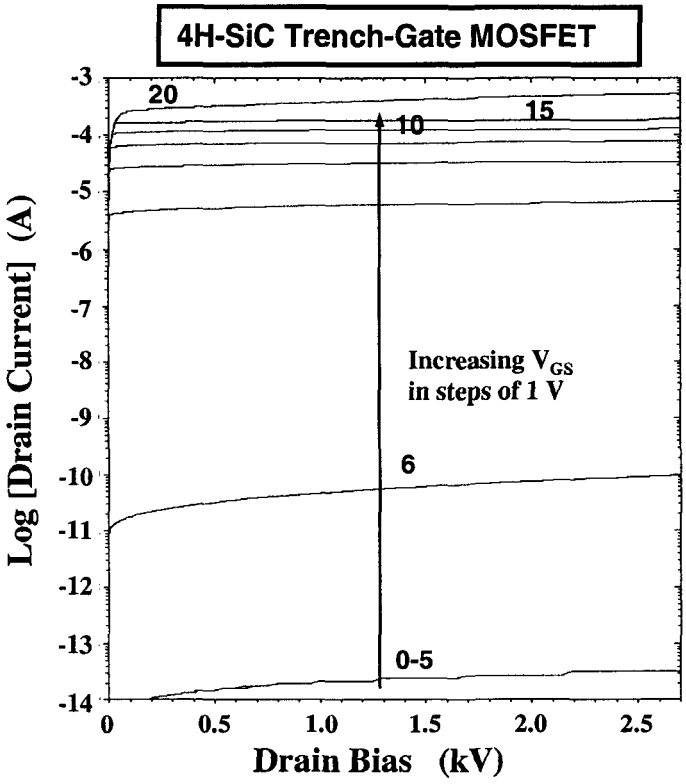

Fig. 11.8 Blocking Characteristics of the Trench-Gate 4H-SiC MOSFET Structure.

The potential distribution (solid-lines) within the upper portion of the trench-gate 4H-SiC MOSFET structure is shown in Fig. 11.9 at a drain bias of 3000 volts. It can be seen that there is a little electric field enhancement at the corner of the trench. Most notably, no potential lines are visible within the P-base region indicating that it is supporting less than 25 volts (the separation between the potential contours). This demonstrates that the presence of the P^+ region under the N^+ source region is suppressing the depletion of the more lightly doped P-base region. The current flow-lines observed under these voltage blocking conditions are also shown in the figure using dashed lines. It can be seen that the leakage current is collected at the contact to the P^+ region placed on the left-hand-side of the structure. Unlike in the case of the planar inversion-mode structure discussed in chapter 9 (see Fig. 9.21), there is

no current flow into the N^+ source region confirming that the reach-through phenomenon has been suppressed.

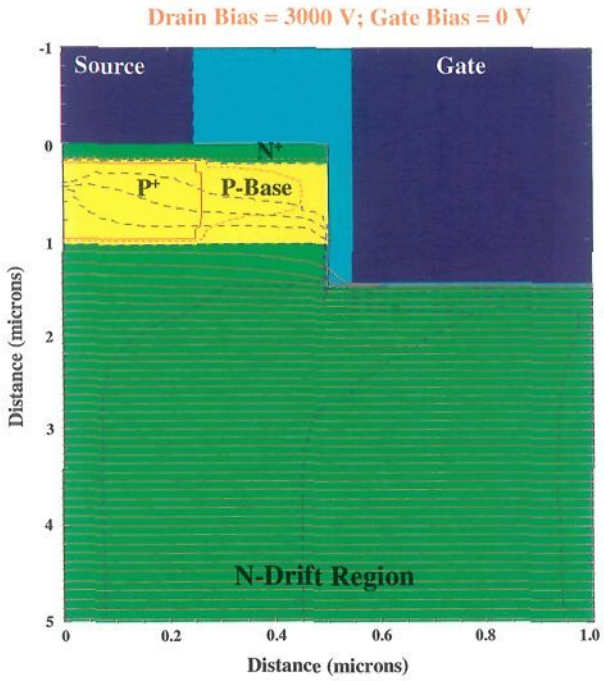

Fig. 11.9 Potential Distribution in the Trench-Gate 4H-SiC Power MOSFET.

A serious problem with the trench-gate silicon carbide MOSFET structure is associated with the high electric field generated at the gate oxide interface. In order for the channel to span the P-base region, it is necessary for the trench to penetrate through the P-base region into the N-drift region. This exposes the gate oxide located at the bottom of the trench to the high electric field developed in the silicon carbide drift region. The problem can be illustrated by examination of the electric field distribution within the trench-gate 4H-SiC power MOSFET structure under voltage blocking conditions. A three-dimensional view of the electric field distribution is shown in Fig. 11.10 for a drain bias of 1000 volts with zero bias applied to the gate electrode. The field distribution shown in this figure indicates that the electric field at the gate oxide has reached a magnitude of close to 1×10^7 V/cm. Consequently, the gate oxide will be prone to failure from rupture at a

drain bias that is just one-third of the breakdown voltage capability of the drift region. Gate oxide reliability problems can arise at much lower drain voltages indicating a serious limitation to operating the trench-gate 4H-SiC MOSFET structure in the blocking mode. Fortunately, this problem has been overcome using innovative structures[5] to shield the gate oxide that will be described in the next chapter.

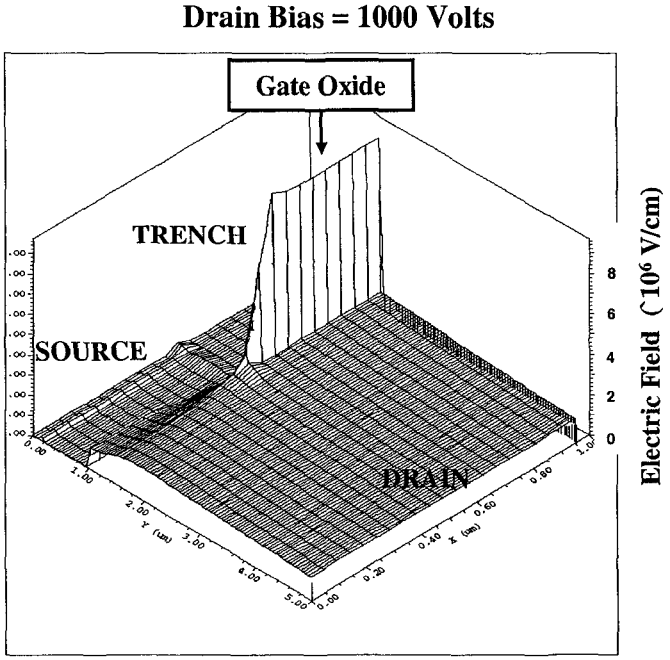

Fig. 11.10 Electric Field Distribution in the Trench-Gate 4H-SiC MOSFET Structure.

From Fig. 11.10, it can be seen that the largest electric field in the gate oxide in the trench-gate 4H-SiC power MOSFET structure occurs at the center of the trench region (x = 1 micron). The behavior of this electric field with increasing drain bias is shown in Fig. 11.11 for drain bias upto 1000 volts. It is obvious that the electric field in the oxide reaches its rupture strength at a drain bias of just 1000 volts. Meanwhile the maximum electric field in the bulk of the semiconductor occurs at the P^+/N junction at x = 0 microns. The development of this electric field is shown in Fig. 11.12, where it can be seen that the maximum electric field is far below the breakdown strength of 4H-SiC.

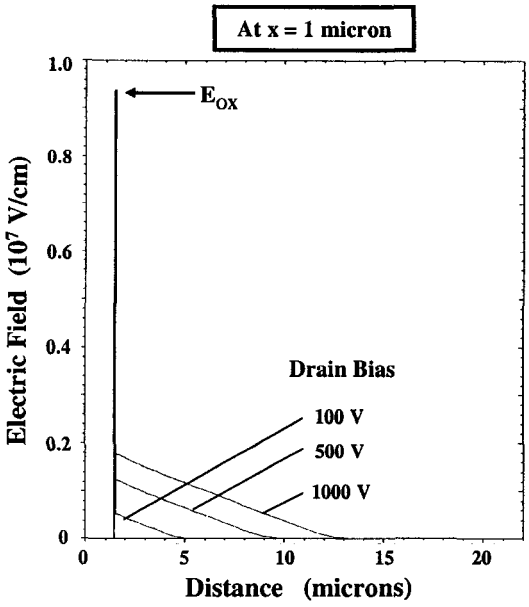

Fig. 11.11 Electric Field in the Trench-Gate 4H-SiC MOSFET Structure.

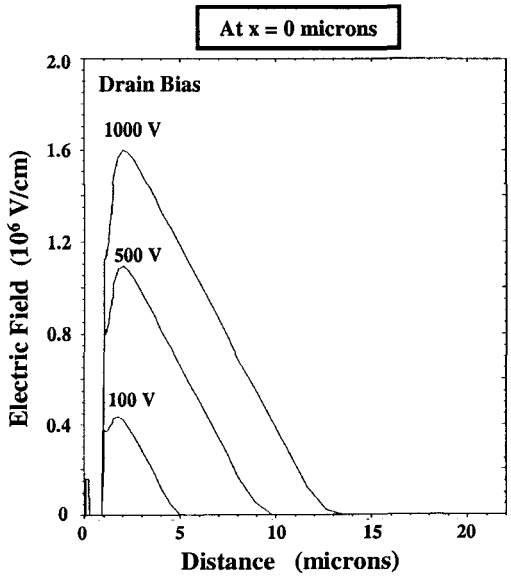

Fig. 11.12 Electric Field in the Trench-Gate 4H-SiC MOSFET Structure.

11.2.2 Trench-Gate Power MOSFET Structure: On-State Characteristics

The on-state voltage drop for the trench-gate 4H-SiC power MOSFET structure is determined by its specific on-resistance. The on-resistance for the structure was extracted by performing numerical simulations with a gate bias of 10 volts. The current distribution within the trench-gate 4H-SiC power MOSFET structure is shown in Fig. 11.13. It can be seen that the current flows through the channel and is then distributed from the bottom of the trench into the drift region. This is due to the formation of an accumulation region at the bottom of the trench because of the applied positive gate bias. The current is distributed into the drift region at a 45 degree angle and then becomes uniform from a depth of about 2 microns. This is consistent with the assumptions made in deriving the analytical model provided in the earlier section of this chapter.

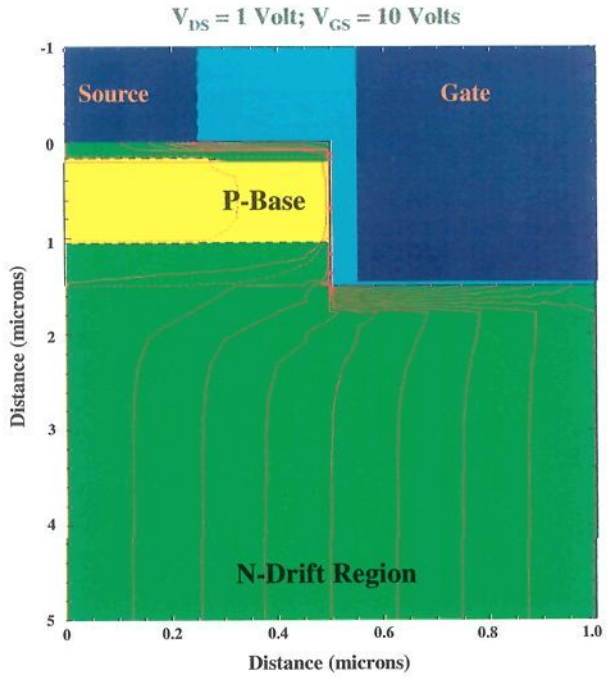

Fig. 11.13 On-State Current Distribution in the Trench-Gate 4H-SiC MOSFET.

The simulations of the specific on-resistance were done with different values for the channel inversion layer mobility. The specific on-resistance was obtained by using a drain bias of 1 volt and sweeping the gate bias to 20 volts to obtain the transfer characteristic. A drain bias of 1 volt was used for these simulations because the on-state voltage drop for these structures is typically in this range. The transfer characteristic obtained using this method is shown in Fig. 11.14 for the device with cell pitch of 1 micron. From the transfer characteristics, it can be seen that the threshold voltage that determines the on-resistance is approximately 5 volts (allowing operation of this device with a gate bias of 10 volts). This value is close to that calculated using the analytical model discussed in the previous chapter for the chosen P-base doping concentration of 9 x 10^{16} cm^{-3} and gate oxide thickness of 0.05 microns. The impact of changing the channel inversion layer mobility is also shown in this figure. As expected, there is a reduction in the drain current as the channel mobility is reduced.

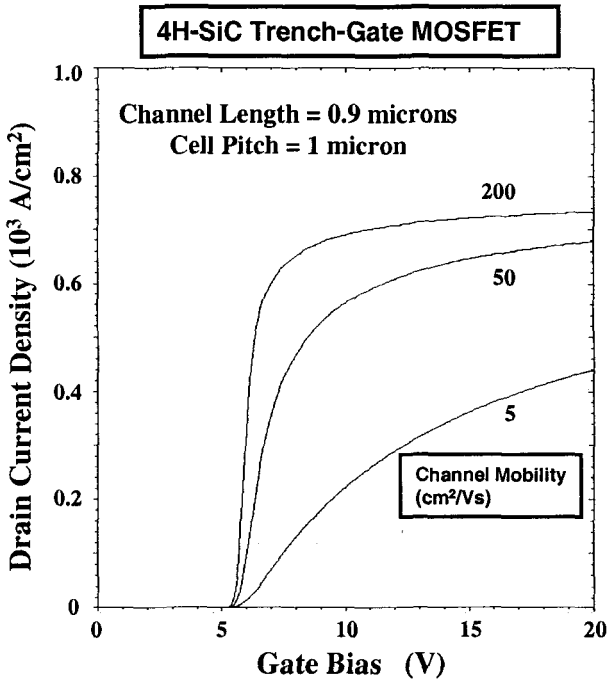

Fig. 11.14 Transfer Characteristics of the 4H-SiC Trench-Gate MOSFETs.

The specific on-resistances obtained from the on-state simulations are compared in Fig. 11.15 with the analytically calculated values obtained by using the model developed in the previous section. For the simulation cases, the channel mobility values were extracted from the *i-v* characteristics obtained for the lateral 4H-SiC MOSFET structure that was previously described in chapter 9 by using the same interface degradation factor as used during the simulation of the vertical 4H-SiC trench-gate MOSFET structure. It can be seen that the predictions of the analytical model are in excellent agreement with the values obtained from the simulations. These results provide confidence in the ability to use the analytical model during the design of the trench-gate 4H-SiC power MOSFET structure. From the figure, it can be concluded that a channel mobility of more than 50 cm^2/Vs is satisfactory for achieving a low specific on-resistance for a 3 kV trench-gate 4H-SiC power MOSFET structure with cell pitch of 1 micron.

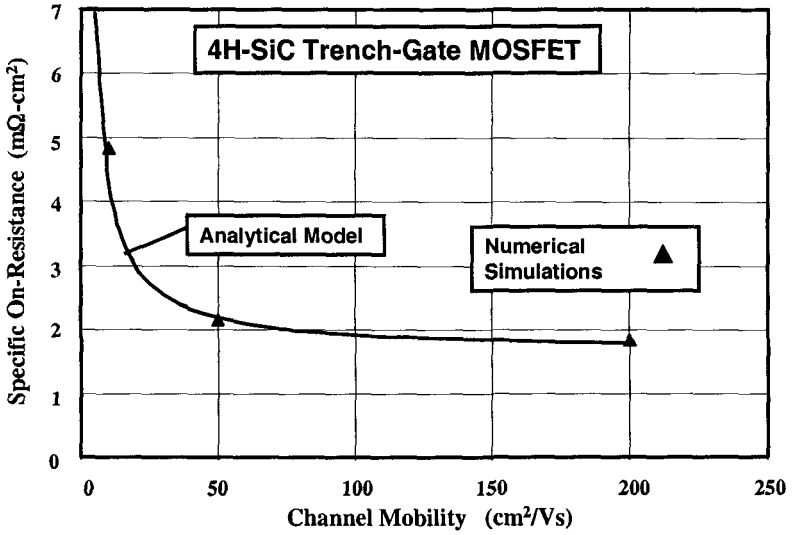

Fig. 11.15 Specific On-Resistance for the 4H-SiC Trench-Gate MOSFETs.

11.2.3 Trench-Gate Power MOSFET Structure: Output Characteristics

The output characteristics of the power MOSFET defines the region within which the device can operate during the switching transients in

applications. The current-voltage loci during the transient must be chosen to remain within the boundary defined by the output characteristics. The output characteristics for the 4H-SiC trench-gate power MOSFET structure were determined by biasing the gate at various values and sweeping the drain voltage upto 2800 volts. The characteristics obtained for the structure with cell pitch of 1 micron are shown in Fig. 11.16. The device exhibits excellent output characteristics upto a gate bias of 10 volts with high output resistance. However, it must be kept in mind that the electric field in the gate oxide reaches its rupture strength at a drain bias of 1000 volts. This is a serious limitation to the safe-operating-area for the trench-gate 4H-SiC structure.

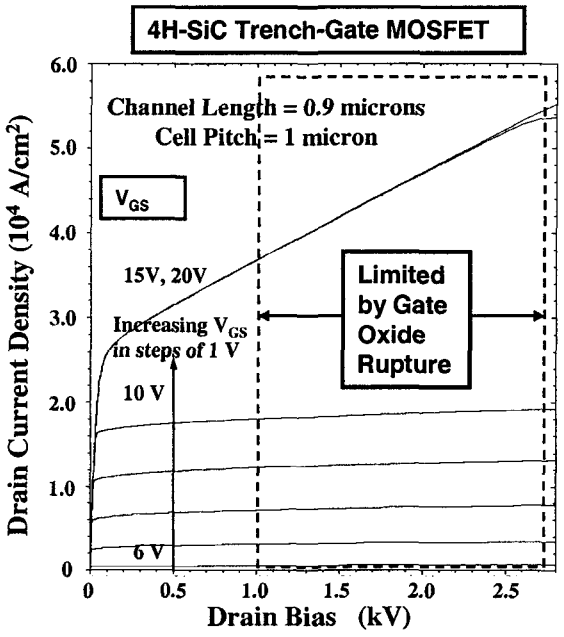

Fig. 11.16 Output Characteristics of a 4H-SiC Trench-Gate MOSFET.

11.3 Accumulation-Mode Trench-Gate Power MOSFET

With the recognition[10] of the difficulty for achieving high inversion layer mobility in silicon carbide especially along the sidewalls of trenches, an alternate device structure was proposed[12] based upon formation of a channel using an accumulation layer. This device structure, named the

accumulation-mode trench-gate MOSFET, is illustrated in Fig. 11.17. In this structure, the P-base region of the conventional trench-gate inversion-mode MOSFET is replaced with a very lightly doped N-type base region. The width of the N-base region (i.e. the mesa width) is designed to be completely depleted by the work-function difference between the gate and the semiconductor. This establishes a potential barrier for transport of electrons from the source to the drain allowing normally-off operation. The device can be switched to the on-state by the application of a positive gate bias, which creates an accumulation layer channel on the trench sidewalls. This channel provides the path for current flow between the source and drain electrodes. As discussed in the previous chapter, a larger accumulation layer mobility was anticipated along the trench sidewalls enabling reduction of the specific on-resistance.

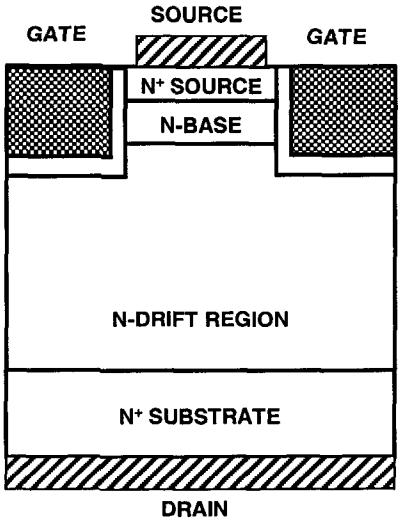

Fig. 11.17 Accumulation-Mode Trench-Gate Power MOSFET Structure.

One of the advantages of the accumulation-mode trench-gate MOSFET structure is the absence of P-N junctions in the path between the source and the drain. This eliminates the problems dealing with the parasitic P-N-P transistor within inversion-mode structures allowing reducing the mesa width to produce the desired normally-off behavior. The anti-parallel diode function can also be generated with the

accumulation-mode structure by application of a positive gate bias to create the channel when the structure operates in the third quadrant. This approach is similar to that used in silicon synchronous rectifiers using low voltage MOSFETs.

11.4 Trench-Gate Power MOSFET: High Permittivity Gate Insulator

As already discussed in a previous section of this chapter, a high electric field is developed in the gate oxide at the bottom of the trench in the silicon carbide UMOSFET structure. The electric field in the gate oxide can exceed its rupture strength at relatively low drain bias voltages limiting the blocking voltage capability of the trench-gate structure. The electric field in the oxide (E_{OX}) is related to the electric field in the underlying semiconductor (E_S) by Gausses Law:

$$E_{OX} = \left(\frac{\varepsilon_S}{\varepsilon_{OX}} \right) . E_S \qquad [11.7]$$

where ε_{OX} is the dielectric constant of the gate oxide and ε_S is the dielectric constant of the semiconductor. The relative dielectric constant (permittivity) for 4H-SiC is 9.7 while that for silicon dioxide is 3.85. Using these values, the electric field in the gate oxide is a factor of 2.5 times that in the semiconductor.

In recognition of this problem, it was proposed[13] that silicon dioxide be replaced by a gate insulator with high permittivity – preferably at least 10 times that of free space. With the increased dielectric constant for the gate insulator, the electric field developed in the gate dielectric would become closer to that developed in the semiconductor[14]. This implies that the maximum electric field in the gate dielectric can be reduced to 3 x 10^6 V/cm, which should be satisfactory for reliable operation. This approach can take advantage of the large effort being undertaken to develop high dielectric constant insulators for mainstream silicon DRAM chips.

A simple one-dimensional analysis of the metal-oxide-semiconductor structure provides interesting insight into the benefits of using high permittivity gate insulators in silicon carbide MOSFETs. Since the highest electric field occurs at the flat bottom of the trench

region in the UMOSFET structure, a one dimensional analysis is a reasonable approximation for analytical purposes.

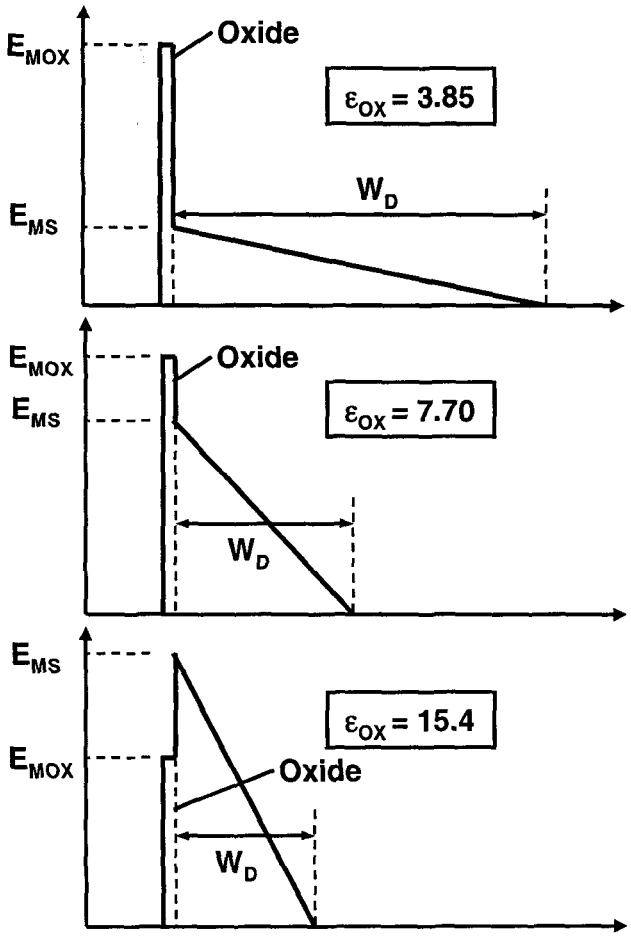

Fig. 11.18 Electric Field Distribution in the Gate Stack for the Trench-Gate Power MOSFET Structure.

The electric field profile in the MOS gate stack is illustrated in Fig. 11.18 for three cases of dielectric constants when it is supporting the same voltage (e.g. 3000 volts). In the first two cases with permittivity of 3.85 (corresponding to silicon dioxide) and 7.7 (corresponding to silicon nitride), it is assumed that the field distribution is constrained by reaching a maximum electric field of 3 x 10^6 V/cm in the gate oxide. This value was chosen based upon the maximum electric field in oxides

for reliable operation. Under this constraint, the maximum electric field in the silicon carbide becomes much lower than its breakdown field strength (1.2 x 10^6 V/cm for the permittivity of 3.85 and 2.4 x 10^6 V/cm for the permittivity of 7.7). However, when the permittivity is increased to 15.4, the electric field distribution becomes constrained by the maximum allowable electric field in the silicon carbide (3.3 x 10^6 V/cm for 4H-SiC at a doping concentration of about 1 x 10^{16} cm^{-3}). Under this limitation, the electric field in the oxide is reduced to about 2 x 10^6 V/cm for the permittivity of 15.4.

The changes in the electric field distribution have a strong impact on the doping concentration and thickness of the drift region required to support the drain bias (e.g. 3000 volts) as indicated in the figure. For the lower dielectric constants, a much thicker drift region with lower doping concentration (reflected in the smaller slope of the electric field profile in the semiconductor) is required because of the reduced maximum electric field, when compared with the properties of the ideal drift region. For the high dielectric constant case, the electric field in the semiconductor becomes identical to that for the ideal one-dimensional parallel plane abrupt junction. Thus, the specific on-resistance is equal to that for the ideal drift region only for the case of the high permittivity gate dielectric and much larger for the other cases.

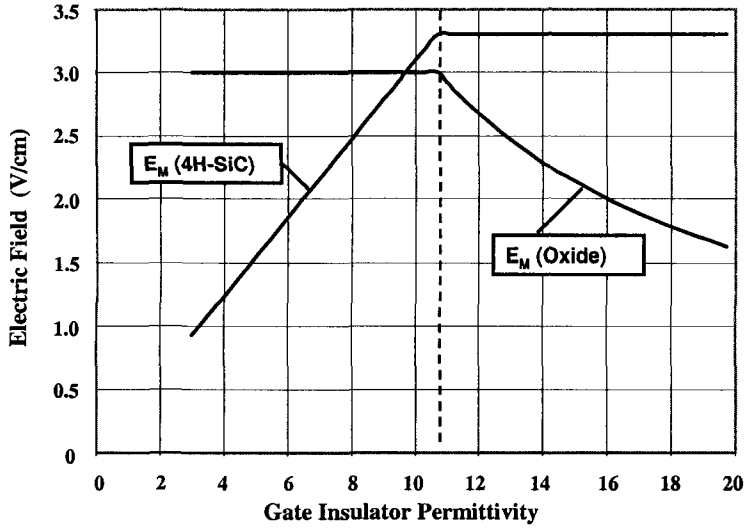

Fig. 11.19 Electric Field Distribution in the Gate Stack for the Trench-Gate Power MOSFET Structure.

In the above discussion, it was pointed out that the gate MOS stack operates in one of two regimes of operation – namely with the electric field constrained by a maximum allowable value in the gate insulator or by the electric field constrained by the maximum allowable value in the semiconductor. The results of the analytically calculated electric fields in the gate insulator and the semiconductor under these constraints are shown in Fig. 11.19. It can be seen that the transition occurs at a permittivity given by:

$$\varepsilon_{OX} = \left(\frac{E_{MS}(4H-SiC)}{E_{MOX}} \right) . \varepsilon_S \qquad [11.8]$$

where E_{MS}(4H-SiC) is the critical electric field for breakdown in 4H-SiC and E_{MOX} is the maximum electric field in the dielectric for reliable operation. For the values for these parameters described above, the transition occurs at a permittivity of 10.7. This is the minimum permittivity needed to reduce the specific on-resistance of the drift region to that for the ideal drift region.

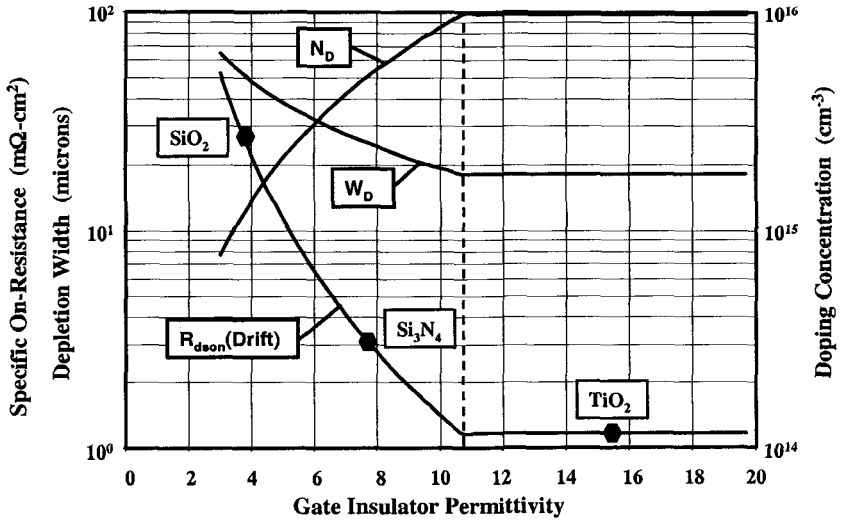

Fig. 11.20 Impact of Gate Insulator Permittivity for the Trench-Gate Power MOSFET Structure.

The permittivity of the gate insulator has a strong influence on the doping concentration and thickness of the drift region. This is shown in Fig. 11.20. The doping concentration of the drift region increases and its thickness decreases as the permittivity is increased upto a value of 10. This results in a drastic reduction of the specific on-resistance of the drift region. As examples, points are shown for selected insulators in the graph. In the case of the commonly used silicon dioxide gate insulator, the specific resistance of the drift region is degraded by a factor of 25 times. If silicon nitride is used as the gate insulator, the drift region resistance becomes only 3 times larger than the ideal case. With the use of a much higher dielectric constant of 15 with titanium dioxide as the insulator, the ideal drift region resistance can be obtained together with reduced electric field in the insulator.

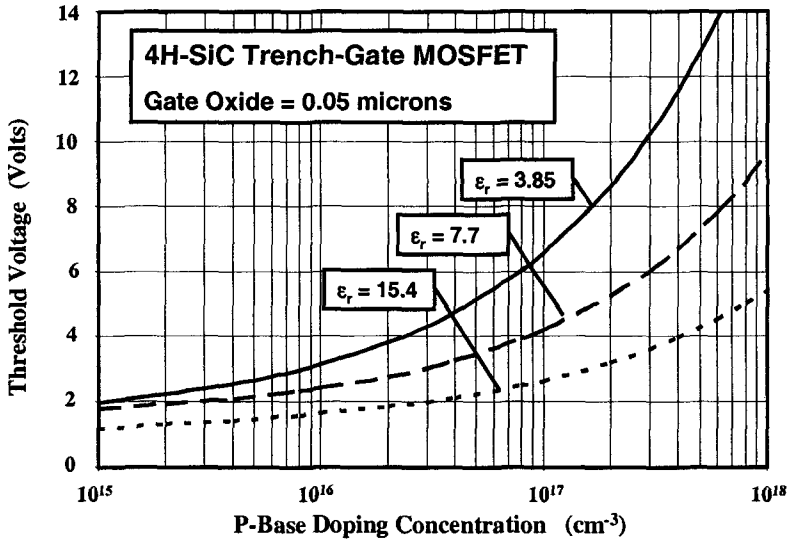

Fig. 11.21 Impact of Gate Insulator Permittivity on the Threshold Voltage of the Trench-Gate Power MOSFET Structure.

It is worth pointing out that a larger dielectric constant for the gate insulator is beneficial for achieving a lower threshold voltage with any given insulator thickness. This is shown in Fig. 11.21 for the case of a gate oxide thickness of 0.05 microns. The calculations of the threshold voltage were performed using the same assumptions regarding a work-function difference of 1 volt and the presence of a fixed oxide charge of

2 x 10^{11} cm^{-2} used in chapter 9 (see Fig. 9.11). At a P-base doping concentration of 3 x 10^{17} cm^{-3}, it can be seen that the threshold voltage is reduced from 10 volts for the silicon dioxide case (permittivity of 3.85) to 6 volts for the silicon nitride case (permittivity of 7.7), and even further to about 3 volts for a permittivity of 15.4. This is favorable for increasing the charge induced in the channel for an available gate bias of 10 volts in systems resulting in reducing the specific on-resistance.

The analysis described above highlights the benefits of using a gate insulator with high permittivity. It must be pointed out that the breakdown strength of insulators has been empirically found to reduce with increasing permittivity. Consequently, care must be taken to ensure that the gate insulator with high permittivity will operate in a reliable manner even when the electric field in it has been reduced. In addition, the band offset between the gate insulator and silicon carbide should be examined to make sure that the Fowler-Nordheim tunneling described in chapter 9 does not create instabilities.

11.5 Trench-Gate Power MOSFET: Experimental Results

The lack of significant diffusion of dopants in silicon carbide motivated the investigation of trench-gate structures before planar-gate structures. The need to obtain a high quality interface between silicon carbide and the gate dielectric was identified as a challenging endeavor from the inception of interest in the development of unipolar transistors from this semiconductor material[10,15]. In addition, the problem of high electric fields developed across the gate oxide, especially at the trench corners, was identified as a limitation to achieving high electric fields within the semiconductor[10]. These issues were indeed found to be a major limitation on the performance of the first trench-gate 4H-SiC power MOSFET structures.

The first reported[6] trench-gate power MOSFETs fabricated using 4H-SiC were limited to a blocking voltage of 260 volts due to rupture of the gate oxide. The specific on-resistance of 18 $m\Omega$-cm^2, measured at a gate bias of 22 volts, was inferior to that of silicon power MOSFETs because of a large cell pitch and low channel mobility (~ 10 cm^2/V-s).

Subsequently, a trench-gate 4H-SiC power MOSFET structure with breakdown voltage of 1100 volts was reported[16] by using a drift region with thickness of 12 microns and doping concentration of 1 x 10^{15} cm^{-3}. The low doping concentration in the drift region was required to

keep the maximum electric field in the silicon carbide to only 1 x 10^6 V/cm to prevent oxide rupture. This is consistent with the analysis in the previous section of this chapter. These devices exhibited a very high specific on-resistance (over 1 Ω-cm^2) at room temperature due to the poor channel mobility (~ 1.5 cm^2/V-s). The specific on-resistance reduced to about 180 mΩ-cm^2 (using data in Fig. 3 in the publication) due to an increase in the channel mobility. In these devices, a threshold voltage of 5 volts was obtained by using a low P-base doping concentration of 6.5 x 10^{16} cm^{-3} with a gate oxide thickness of 0.1 microns. However, this necessitated increasing the channel length to 4 microns to prevent reach-through problems. The large channel length, in conjunction with the poor channel mobility, was responsible for the poor (worse than silicon power MOSFETs) specific on-resistance of the devices.

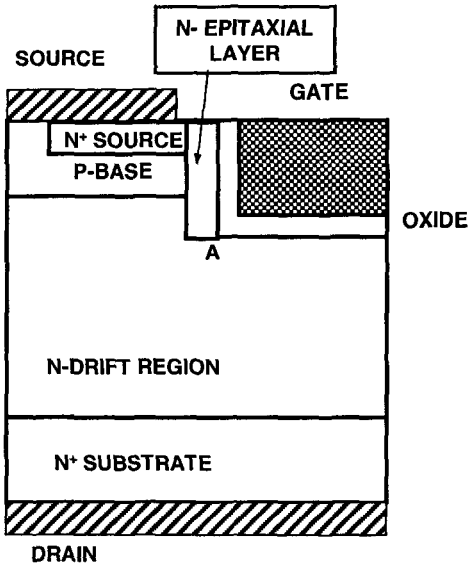

Fig. 11.22 Epitaxial-Channel Accumulation-Mode Trench-Gate Power MOSFET Structure.

In section 11.3, an accumulation-mode trench-gate MOSFET structure was described as an approach to reduce the specific on-resistance due to an increase in the channel mobility. An accumulation-mode structure that combines a trench-gate structure with a depleted N-base region located adjacent to a P-N junction (previously described in

chapter 10 as the shielded accumulation-mode planar MOSFET structure) has been proposed[17] and experimentally demonstrated. This structure, shown in Fig. 11.22, contains an N-base region that is epitaxially grown on the trench sidewall surface. The authors observed an accumulation layer mobility of 108 $cm^2/V\text{-}s$ for this structure resulting in a specific on-resistance of 11 $m\Omega\text{-}cm^2$ at a gate bias of 10 volts. The breakdown voltage of 500 volts for this structure is still limited by the development of high electric field in the gate oxide.

11.6 Summary

The trench-gate 4H-SiC vertical power MOSFET structure was the first approach explored by the silicon carbide community because the P-base region could be epitaxially grown rather than formed by ion implantation, which was a less mature technology. Although devices with breakdown voltages of upto 1100 volts have been fabricated, their performance was severely limited by the on-set of rupture of the gate oxide and the poor channel mobility. In order to overcome these problems, it is necessary to shield the gate oxide from the high electric field developed in the drift region. These device structures are discussed in the next chapter.

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Power semiconductor devices are widely used for the control and management of electrical energy. The improving performance of power devices has enabled cost reductions and efficiency increases resulting in lower fossil fuel usage and less environmental pollution. This book provides the first cohesive treatment of the physics and design of silicon carbide power devices with an emphasis on unipolar structures. It uses the results of extensive numerical simulations to elucidate the operating principles of these important devices.

About the Author

Professor Baliga is an internationally renowned scientist, prolific author of 12 books and over 500 publications. He has been granted more than 100 U.S. Patents. In recognition of his invention and commercialization of the Insulated Gate Bipolar Transistor (IGBT), Scientific American Magazine named him one of the 'Eight Heroes of the Semiconductor Revolution' in the 1997 special issue commemorating the Solid-State Century. He has received numerous IEEE awards and is an elected member of the National Academy of Engineering, the highest honor in the engineering profession.

Key Features

- The first tutorial treatment of silicon carbide power devices
- Uses rigorous analytical formulations to describe basic physical principles
- Describes the design and performance of Schottky rectifiers with trade-offs between the on-state and reverse blocking characteristics
- Analyzes numerous field effect transistors with emphasis on techniques for shielding the gate oxide
- Includes a thorough review of material properties

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