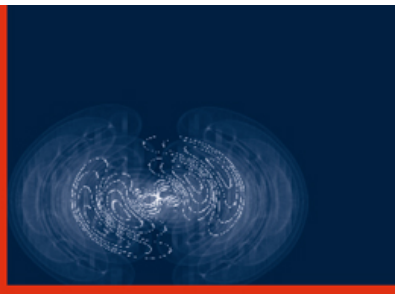

B. Jayant Baliga

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ISBN 978-1-4419-5916-4 e-ISBN 978-1-4419-5917-1
DOI 10.1007/978-1-4419-5917-1
Springer New York Heidelberg Dordrecht London

Library of Congress Control Number: 2010929769

Dedication

The author would like to dedicate this book to his wife, Pratima, for her unwavering support throughout his career devoted to the enhancement of the performance and understanding of power semiconductor devices.

Preface

With increased awareness of the adverse impact on the environment resulting from carbon emissions into the atmosphere, there is a growing demand for improving the efficiency of power electronic systems. Power semiconductor devices are recognized as a key component of all power electronic systems. It is estimated that at least 50 percent of the electricity used in the world is controlled by power devices. With the wide spread use of electronics in the consumer, industrial, medical, and transportation sectors, power devices have a major impact on the economy because they determine the cost and efficiency of systems. After the initial replacement of vacuum tubes by solid state devices in the 1950s, semiconductor power devices have taken a dominant role with silicon serving as the base material. These developments have been referred to as the *Second Electronic Revolution*.

In the 1970s, the power MOSFET product was first introduced by International Rectifier Corporation. Although initially hailed as a replacement for all bipolar power devices due to its high input impedance and fast switching speed, the silicon power MOSFET has successfully cornered the market for low voltage ($<$100 V) and high switching speed ($>$100 kHz) applications but failed to make serious inroads in the high voltage arena. This is because the on-state resistance of silicon power MOSFETs increases very rapidly with increase in the breakdown voltage. The resulting high conduction loss, even when using larger more expensive die, degrades the overall system efficiency.

The large on-state voltage drop for high voltage silicon power MOSFETs and the large drive current needed for silicon power bipolar transistors encouraged the development of the insulated gate bipolar transistor (IGBT) [1]. First commercialized in the early 1980s, the IGBT has become the dominant device used in all medium and high power electronic systems in the consumer, industrial, transportation, and military systems, and even found applications in the medical sector. The US Department of Energy has estimated that the implementation of IGBT-based variable speed drives for controlling motors is producing an energy savings of over 2 quadrillion btus per year, which is equivalent to 70 Giga-Watts of power. This energy savings eliminates the need for generating electricity from 70 coal-fired

power-plants resulting in reducing carbon dioxide emissions by over one-Trillion pounds each year.

With on-going investments in renewable energy sources such as wind and solar power that utilize power semiconductor device in inverters, it is anticipated that there will be an increasing need for technologists trained in the discipline of designing and manufacturing power semiconductor devices. My recently published textbook [2] provides a comprehensive analysis of the basic power rectifier and transistor structures. This textbook has been complemented with a monograph on "Advanced Power Rectifier Concepts" to familiarize students and engineering professionals with structures that exhibit improved performance attributes.

This monograph introduces the reader to advanced power MOSFET concepts that enable improvement of performance of these transistor structures. For the convenience of readers, analysis of the basic transistor structures, with the same voltage ratings as the novel device structures, have been included in the monograph to enable comparison of the performance. As in the case of the textbook, analytical expressions that describe the behavior of the advanced power MOSFET structures have been rigorously derived using the fundamental semiconductor Poisson's, continuity, and conduction equations in this monograph. The electrical characteristics of all the power MOSFETs discussed in this book can be computed using these analytical solutions as shown by typical examples provided in each section. In order to corroborate the validity of these analytical formulations, I have included the results of two-dimensional numerical simulations in each section of the book. The simulation results are also used to further elucidate the physics and point out two-dimensional effects whenever relevant. Due to increasing interest in the utilization of wide band-gap semiconductors for power devices, the book includes the analysis of silicon carbide structures.

In the first chapter, a broad introduction to potential applications for power devices is provided. The electrical characteristics for ideal power MOSFETs are then defined and compared with those for typical devices. The second and third chapters provide analyses of the planar DMOSFET structure and the trench-gate UMOSFET structure with 30-V blocking capability, which can be used as a benchmark for understanding the improvements achieved using the advanced device concepts. The analysis includes the on-resistance, the input capacitance, the gate charge, and the output characteristics.

The next four chapters are devoted to various advanced power MOSFET structures that allow improvement in the performance of devices with 30-V blocking capability. The fourth chapter discusses on the "Shielded Channel Planar Power MOSFET" structure, which allows a significant reduction in the gate charge while achieving a specific on-resistance close to that of the UMOSFET structure. The fifth chapter discusses the power CC-MOSFET structure, which utilizes the two-dimensional charge coupling effect to reduce the specific on-resistance by an order of magnitude. This structure is favorable for use as a synchronous rectifier in the sync-buck circuit topology used in voltage regulator modules for providing power to microprocessors in computers.

The next two chapters are devoted to high-voltage silicon device structures that utilize the charge-coupling concept to reduce the resistance of the drift region. In chapter six, the charge-coupling phenomenon is accomplished by using a graded doping profile in conjunction with an electrode embedded in an oxide coated trench to create the power GD-MOSFET structure. In chapter seven, the charge-coupling phenomenon is accomplished with adjacent p-type and n-type layers in the drift region to create the power SJ-MOSFET structure.

Chapter eight provides a detailed discussion of the body-diode within the various silicon power MOSFET structures. The body-diode can be used in place of the fly-back rectifier utilized in the H-bride circuit commonly used for motor control applications. It is demonstrated in this chapter that the judicious utilization of a Schottky contact within the power MOSFET cell structure can greatly improve the reverse recovery behavior of the body-diode.

Improvement in the performance of high voltage power MOSFET structures can also be achieved by replacing silicon with silicon carbide as the base material [3]. The much larger breakdown field strength for 4H-SiC allows increasing the doping concentration in the drift region by a factor of 200-times while shrinking the thickness of the drift region by one-order of magnitude. However, the silicon power MOSFET structure must be modified to shield the gate oxide from the much larger electric fields prevalent in silicon carbide to avoid rupture. In addition, the base region must be shielded to avoid reach-through breakdown. The on-resistance of these devices becomes limited by the channel resistance.

The final chapter provides a comparison of all the power MOSFET structures discussed in this book. The devices are first compared for the 30-V rating suitable for VRM applications and then with the 600-V rating suitable for motor control applications. In addition, the performance of all the devices is compared over a wide range of blocking voltages to provide a broader view.

I am hopeful that this monograph will be useful for researchers in academia and to product designers in the industry. It can also be used for the teaching of courses on solid state devices as a supplement to my textbook [2].

December, 2009 B. Jayant Baliga
Raleigh, NC

References

1. B.J. Baliga, “How the Super-Transistor Works”, Scientific American Magazine, Special Issue on ‘The Solid-State-Century’, pp. 34–41, January 22, 1988.
2. B.J. Baliga, “Fundamentals of Power Semiconductor Devices”, Springer Scientific, New York, 2008.
3. B.J. Baliga, “Silicon Carbide Power Devices”, World Scientific Press, Singapore, 2006.

Contents

Chapter 1
Introduction

Power devices are required for applications that operate over a broad spectrum of power levels as shown in Fig. 1.1 [1]. Based up on this figure, the applications can be broken down into several categories. The first category is applications that require low operating current (typically less than 1 A) levels. These applications, such as display drives, usually require a large number of transistors that must be capable of blocking up to 300 V. The small size of the low-current transistors allows their integration on a single chip with control circuits to provide a cost-effective solution.

The second category is applications where the operating voltage of the power circuit is relatively small (<100 V). Typical examples are automotive electronics and power supplies used in desktop computers and laptops. Silicon power MOSFET structures offer the best performance for these applications because of their low on-resistance and fast switching speed. This monograph describes a variety of power MOSFET structures that enable enhancement in their operating characteristics.

The third category is applications with high operating voltages (above 200 V). Typical examples are lamp ballasts, consumer appliances that utilize motors, and electric vehicle drives. The on-resistance of conventional silicon power MOSFET structures is too large to serve these applications. Consequently, these applications utilize silicon insulated gate bipolar transistors (IGBTs). The silicon IGBT combines the physics of the MOSFET structure with the physics of the bipolar transistor structure. Although the silicon IGBT has become ubiquitous for high voltage power electronic applications, silicon power MOSFETs that utilize two-dimensional charge coupling can be competitive with silicon IGBTs as shown in this monograph. In addition, power MOSFET structures built using silicon carbide as the base material have been shown to exhibit very promising characteristics for applications that require blocking voltages of up to 5,000 V [2]. Consequently, this monograph includes the discussion of the power MOSFET structures that are specially configured to obtain a high performance from silicon carbide.

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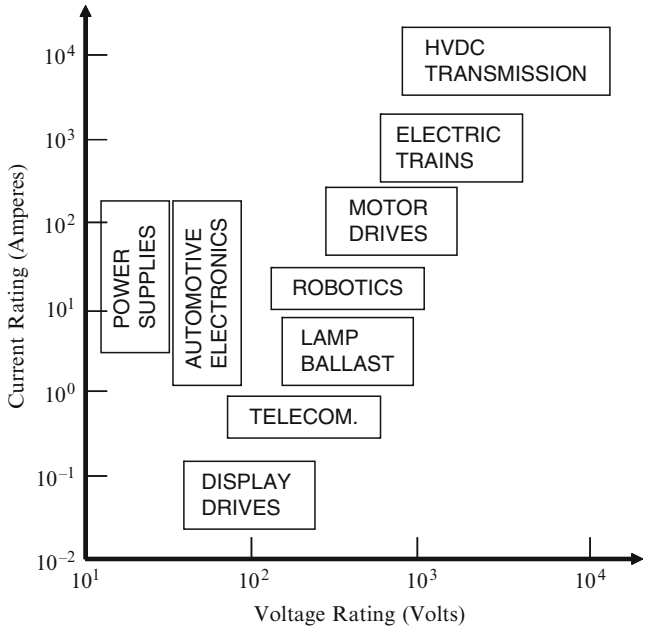

Fig. 1.1 Applications for power devices

1.1 Ideal Power Switching Waveforms

An ideal power device must be capable of controlling the flow of power to loads with zero power dissipation. The loads encountered in systems may be inductive in nature (such as motors and solenoids), resistive in nature (such as heaters and lamp filaments), or capacitive in nature (such as transducers and LCD displays). Most often, the power delivered to a load is controlled by turning-on a power switch on a periodic basis to generate pulses of current that can be regulated by a control circuit. The ideal waveforms for the power delivered through a power switch are shown in Fig. 1.2. During each switching cycle, the switch remains on for a time up to t_{ON} and maintains an off-state for the remainder of the period T. This produces pulses of current that flow through the circuit as controlled by the turning-on of power switches. For an ideal power switch, the voltage drop during the on-state is zero resulting in no power dissipation. Similarly, during the off-state, the (leakage) current in the ideal power switch is zero resulting in no power dissipation. In addition, it is assumed that the ideal power switch makes the transition between the on-state and off-state instantaneously resulting in no power loss as well.

Typical power MOSFET structures exhibit a finite voltage drop in the on-state and leakage current flow in the off-state. In addition, the power MOSFET structure exhibits power losses during the turn-on and turn-off transients. These power losses are related to their large terminal capacitances which must be charged

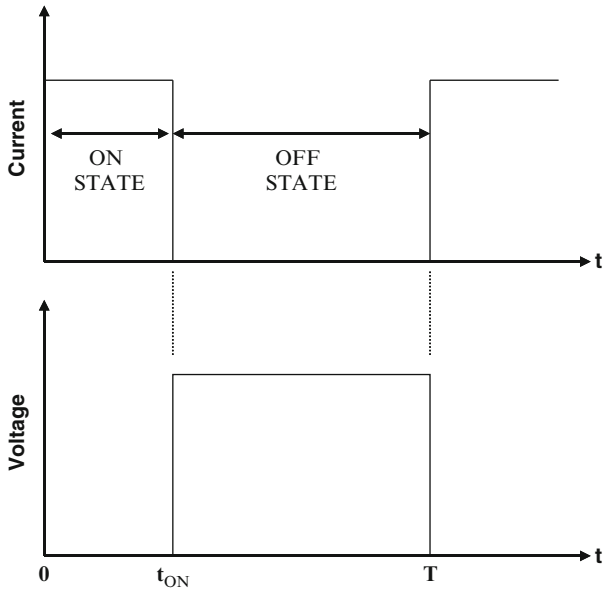

Fig. 1.2 Ideal switching waveforms for power delivery

and discharged during each operating cycle. The novel power MOSFET structures that are discussed in this monograph were created to reduce the on-resistance and capacitance.

1.2 Ideal and Typical Power MOSFET Characteristics

The *i*–*v* characteristics of an ideal power switch are illustrated in Fig. 1.3. The ideal transistor conducts current in the on-state with zero voltage drop and blocks voltage in the off-state with zero leakage current. In addition, the ideal device can operate with a high current and voltage in the active region with the saturated forward current in this mode controlled by the applied gate bias. The spacing between the characteristics in the active region is uniform for an ideal transistor indicating a gain (transconductance) that is independent of the forward current and voltage.

The *i*–*v* characteristics of a typical power MOSFET structure are illustrated in Fig. 1.4. This device exhibits a finite resistance when carrying current in the on-state as well as a finite leakage current while operating in the off-state (not shown in the figure because its value is much lower than the on-state current levels). The breakdown voltage of a typical transistor is also finite as indicated in the figure with 'BV'. The typical transistor can operate with a high current and voltage in the active region. This current is determined by a gate voltage for a MOSFET as indicated in the figure. It is desirable to have gate voltage controlled characteristics because the

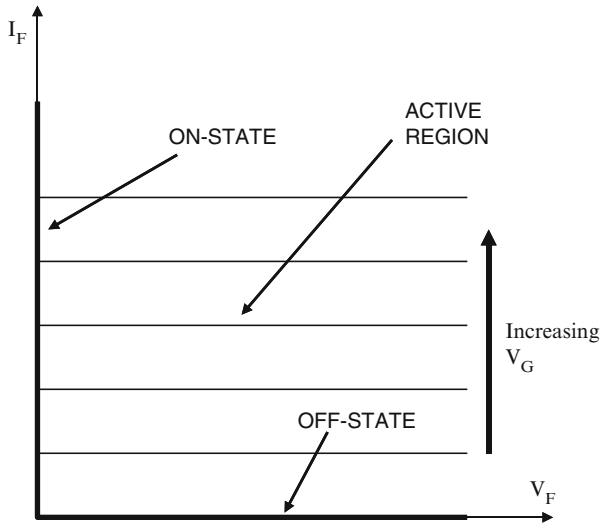

Fig. 1.3 Characteristics of an ideal power switch

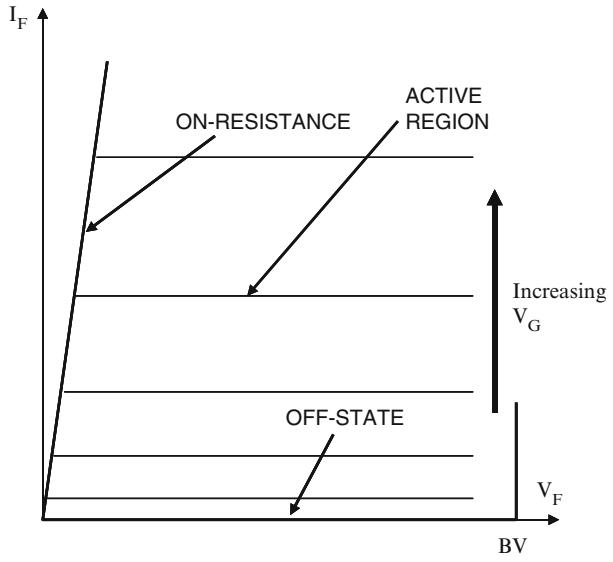

Fig. 1.4 Characteristics of a typical power MOSFET structure

drive circuit can be integrated to reduce its cost. The spacing between the characteristics in the active region is non-uniform for a typical MOSFET with a square-law behavior for devices operating with channel pinch-off in the current saturation mode. Recently, devices operating under a new super-linear mode have been proposed and demonstrated for wireless base-station applications [3]. These devices

exhibit an equal spacing between the saturated drain current characteristics as the gate voltage is increased. This is an ideal behavior when the transistor is used for the amplification of audio, video or cellular signals because it eliminates signal distortion that occurs with the characteristics shown in Fig. 1.4.

1.3 Typical Power MOSFET Structures

The most commonly used unipolar power transistor is the silicon power Metal-Oxide-Semiconductor Field-Effect-Transistor or MOSFET. Although other structures, such as JFETs or SITs have been explored [4], they have not been popular for power electronic applications because of their normally-on behavior. The commercially available silicon power MOSFETs are based upon the structures shown in Fig. 1.5. The D-MOSFET was first commercially introduced in the 1970s and contains a 'planar-gate' structure. The P-base region and the N^+ source regions are self-aligned to the edge of the polysilicon gate electrode by using ion-implantation of boron and phosphorus followed by their respective drive-in thermal cycles. The n-type channel is defined by the difference in the lateral extension of the junctions under the gate electrode. The device supports positive voltage applied to the drain across the P-base/N-drift region junction. The voltage blocking capability is determined by the doping and thickness of the N-drift region. Although low voltage silicon power MOSFETs have small on-resistances, the drift region resistance increases rapidly with

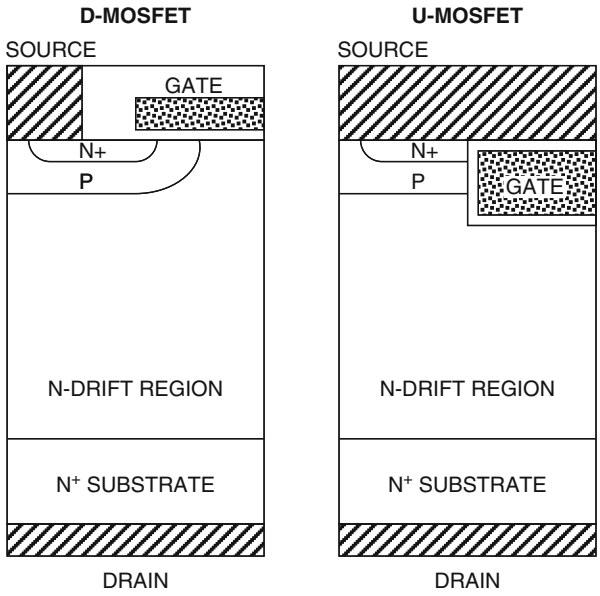

Fig. 1.5 Typical silicon power MOSFET structures

increasing blocking voltage limiting the performance of silicon power D-MOSFETs to below 200 V.

The silicon U-MOSFET structure became commercially available in the 1990s. It has a gate structure embedded within a trench etched into the silicon surface. The N-type channel is formed on the side-wall of the trench at the surface of the P-base region. The channel length is determined by the difference in vertical extension of the P-base and N^+ source regions as controlled by the ion-implant energies and drive times for the dopants. The silicon U-MOSFET structure was developed to reduce the on-state resistance by elimination of the JFET component within the D-MOSFET structure.

1.4 Ideal Drift Region for Unipolar Power Devices

The power MOSFET structures discussed above contain a drift region which is designed to support the blocking voltage. The properties (doping concentration and thickness) of the *ideal drift region* can be analyzed by assuming an abrupt junction profile with high doping concentration on one side and a low uniform doping concentration on the other side, while neglecting any junction curvature effects by assuming a parallel-plane configuration. The resistance of the ideal drift region can then be related to the basic properties of the semiconductor material [5].

A Schottky rectifier structure is illustrated in Fig. 1.6. The solution of Poisson's equation in the voltage blocking mode leads to a triangular electric field distribution, as shown in Fig. 1.6, within a uniformly doped drift region with the slope of the field profile being determined by the doping concentration. The same behavior for the electric field profile occurs in the vertical power MOSFET structures as well. The maximum voltage that can be supported by the drift region is determined by the

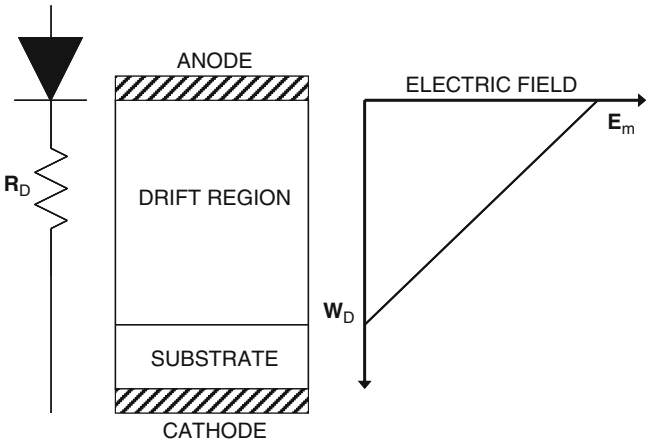

Fig. 1.6 The ideal drift region and its electric field distribution

maximum electric field (E_m) reaching the critical electric field (E_c) for breakdown for the semiconductor material. The critical electric field for breakdown and the doping concentration then determine the maximum depletion width (W_D).

The specific resistance (resistance per unit area) of the ideal drift region is given by:

$$R_{on.sp} = \left(\frac{W_D}{q\mu_n N_D}\right) \tag{1.1}$$

where N_D is the doping concentration of the drift region. Since this resistance was initially considered to be the lowest value achievable with silicon devices, it has historically been referred to as the *ideal specific on-resistance of the drift region*. More recent introduction of the charge-coupling concept, described later in this chapter, has enabled reducing the drift region resistance of silicon devices to below the values predicted by this equation. The depletion width under breakdown conditions is given by:

$$W_D = \frac{2BV}{E_C} \tag{1.2}$$

where BV is the desired breakdown voltage. The doping concentration in the drift region required to obtain this breakdown voltage is given by:

$$\mathrm{N_D} = \frac{\varepsilon_S \mathrm{E_C^2}}{2\mathrm{qBV}} \tag{1.3}$$

Combining these relationships, the specific resistance of the ideal drift region is obtained:

$$R_{on-ideal} = \frac{4BV^2}{\varepsilon_S \mu_n E_C^3} \tag{1.4}$$

The denominator of (1.4) $\left(\varepsilon_S\ \mu_n \mathrm{E_C^3}\right)$ is commonly referred to as *Baliga's Figure of Merit for Power Devices*. It is an indicator of the impact of the semiconductor material properties on the resistance of the drift region. The dependence of the drift region resistance on the mobility (assumed to be for electrons here because in general they have higher mobility values than for holes) of the carriers favors semiconductors such as Gallium Arsenide. However, the much stronger (cubic) dependence of the on-resistance on the critical electric field for breakdown favors wide band gap semiconductors such as silicon carbide [2]. The critical electric field for breakdown is determined by the impact ionization coefficients for holes and electrons in semiconductors.

As an example, the change in the specific on-resistance for the drift region with critical electric field and mobility is shown in Fig. 1.7 for the case of a breakdown

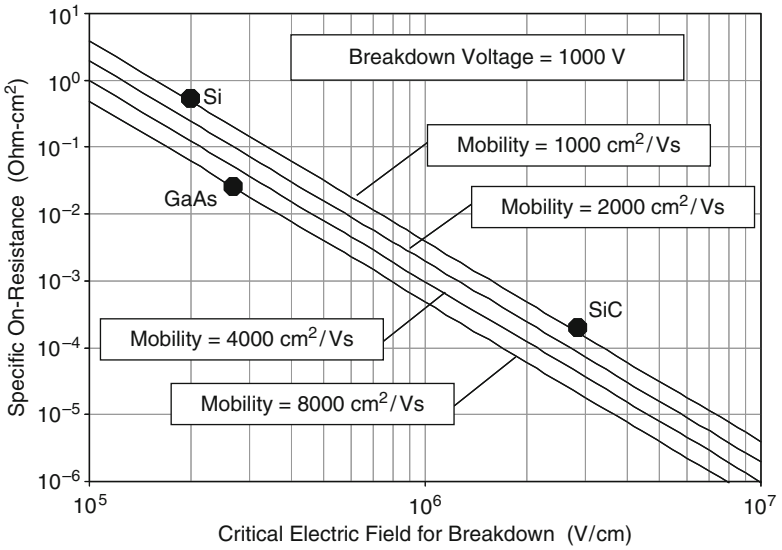

Fig. 1.7 Specific on-resistance of the *ideal drift region*

voltage of 1,000 V. The location of the properties for silicon, gallium arsenide, and silicon carbide are shown in the figure by the points. The improvement in drift region resistance for GaAs in comparison with silicon is largely due to its much greater mobility for electrons. The improvement in drift region resistance for SiC in comparison with silicon is largely due to its much larger critical electric field for breakdown. Based upon these considerations, excellent high voltage Schottky rectifiers were developed from GaAs in the 1980s [6] and from silicon carbide in the 1990s [7]. Interest in the development of power devices from wide-band-gap semiconductors, including silicon carbide and gallium nitride, continues to grow.

1.5 Charge-Coupled Structures: Ideal Specific On-Resistance

The depletion region extends in one-dimension from a junction or Schottky contact during the blocking mode for the conventional structure discussed in the previous section. In the charge coupled structure, the voltage blocking capability is enhanced by the extension of depletion layers in two-dimensions. This effect is created by the formation of a horizontal Schottky contact on the top surface as illustrated in Fig. 1.18 which promotes the extension of a depletion region along the vertical or y-direction. Concurrently, the presence of the vertical P-N junction created by the alternate N and P-type regions promotes the extension of a depletion region along the horizontal or x-direction. These depletion regions conspire to produce a two-dimensional charge coupling in the N-drift region

which alters the electric field profile. A similar phenomenon can be induced in the case of power MOSFET structures under the P-base region as discussed later in this monograph.

The optimization of the charge coupled structure requires proper choice of the doping concentration and thickness of the N and P-type regions. It has been found that the highest breakdown voltage occurs when the charge in these regions is given by:

$$Q_{optimum} = 2qN_D W_N = \varepsilon_S E_C \tag{1.5}$$

where q is the charge of an electron (1.6×10^{-19} C), N_D is the doping concentration of the N-Type drift region, W_N is the width of the N-type drift region as shown in Fig. 1.8, ε_S is the dielectric constant of the semiconductor, and E_C is the critical electric field for breakdown in the semiconductor. For silicon, the optimum charge is found to be 3.11×10^{-7} C/cm^2 based upon a critical electric field of 3×10^5 V/cm. The optimum charge is often represented as a dopant density per unit area, in which case it takes a value of about 2×10^{12}/cm^2 for silicon. A slightly lower value for the doping concentration in the drift region may be warranted as discussed later in this section of the chapter.

The specific on-resistance for the drift region in the charge coupled structures is given by:

$$R_{D,sp} = \rho_D t\left(\frac{p}{W_N}\right) \tag{1.6}$$

where ρ_D is the resistivity of the N-type drift region, t is the trench depth and p is the cell pitch. Here, the uniform electric field is assumed to be produced only along the

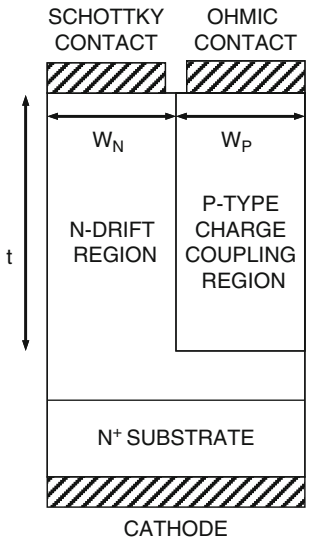

Fig. 1.8 Basic charge coupled Schottky diode structure

trench where the charge coupling occurs and the resistance of the remaining portion of the N-drift region is neglected. Using the relationship between the resistivity and the doping concentration, this equation can be written as:

$$R_{D,sp} = \frac{tp}{q\ \mu_N N_D W_N} \tag{1.7}$$

Combining this expression with (1.5):

$$R_{D,sp} = \frac{2tp}{\mu_N Q_{optimum}} \tag{1.8}$$

If the electric field along the trench, at the on-set of breakdown in the charge coupled device structure, is assumed to be uniform at a value equal to the critical electric field of the semiconductor:

$$t = \frac{BV}{E_C} \tag{1.9}$$

Using this expression, as well as the second part of (1.5), in (1.8) yields:

$$R_{D,sp} = \frac{2BVp}{\mu_N \varepsilon_S E_C^2} \tag{1.10}$$

This is a fundamental expression for the *ideal specific on-resistance of vertical charge coupled devices*. By comparison of this expression with that for the one dimensional case (see 1.4), it can be observed that the specific on-resistance for the charge coupled devices increases linearly with the breakdown voltage unlike the more rapid quadratic rate for the conventional drift region. In addition, it is worth pointing out that the specific on-resistance for the drift region in the charge coupled structure can be reduced by decreasing the pitch. This occurs because the doping concentration in the drift region increases when the pitch is reduced in order to maintain the same optimum charge. The larger doping concentration reduces the resistivity and hence the specific on-resistance.

However, the analysis of the specific on-resistance for the drift region in charge coupled device structures must be tempered by several considerations. Firstly, it must be recognized that the mobility will become smaller when the doping concentration becomes larger. Secondly, the critical electric field for breakdown becomes smaller for the charge coupled structures because the high electric field in the drift region extends over a larger distance producing enhanced impact ionization. If a critical electric field for breakdown in the drift region for charge coupled structures is reduced to 2×10^5 V/cm, an optimum charge of 2.07×10^{-7} C/cm^2, with a corresponding dopant density of about 1.3×10^{12}/cm^2, is more appropriate for silicon.

In designing the drift region for charge coupled structures, it is important to recognize that, unlike in the conventional one-dimensional case, the doping concentration of the drift region is dictated by the cell pitch and not the breakdown

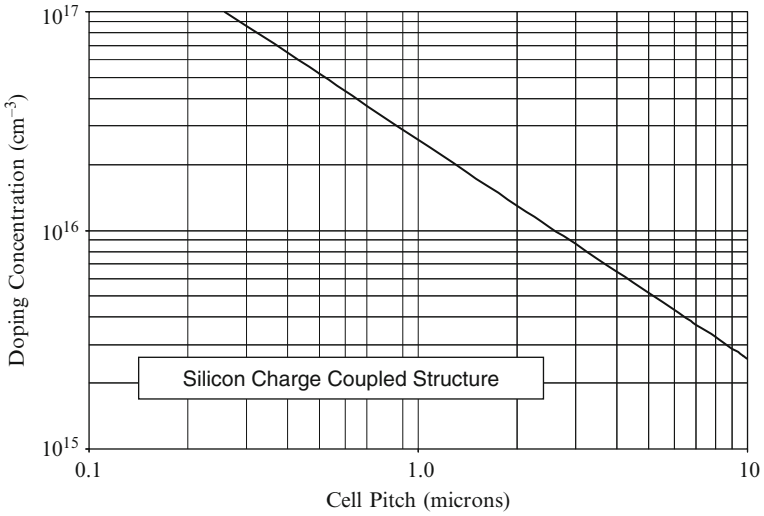

Fig. 1.9 Drift region doping concentration for the charge coupled structure

voltage. The breakdown voltage in the charge coupled structure is determined solely by the depth of the trench used to provide the charge coupling effect and is independent of the doping concentration of the N-drift region. In the case of silicon charge coupled devices, the doping concentration for the N-type drift region is provided in Fig. 1.9 for the case of equal widths for the N-type and P-type charge coupling regions. For a typical cell pitch of 1 μm, the doping concentration in the N-type drift region is about $2.5 \times 10^{16}/cm^3$ when a critical electric field of 2×10^5 V/cm is assumed.

It is interesting to compare the ideal specific on-resistance for the drift region in the silicon charge coupled structures to that for the one-dimensional parallel-plane case. This comparison is done in Fig. 1.10 using three values for the cell pitch in the case of the charge coupled structures. The doping concentration in the N-drift region increases when the cell pitch is reduced from 5 to 0.2 μm, as already shown in Fig. 1.9, leading to a decrease in the specific on-resistance. The resulting reduction of the mobility with increasing doping concentration was included during the calculation of the specific on-resistance in Fig. 1.10. There is a cross-over in the specific on-resistance for the two types of structures. For the cell pitch of 1 μm, the cross-over occurs at a breakdown voltage of about 50 V. The cross-over moves to a breakdown voltage of about 130 V when the cell pitch is increased to 5 μm, and to about 20 V if a smaller cell pitch of 0.2 μm is used. Consequently, the charge coupled structure is more attractive for reducing the specific on-resistance when the cell pitch is smaller. This entails a more complex process technology with higher attendant costs.

As a particular example, consider the case of silicon devices designed to support 200 V. In the case of the conventional structure with a one-dimensional junction,

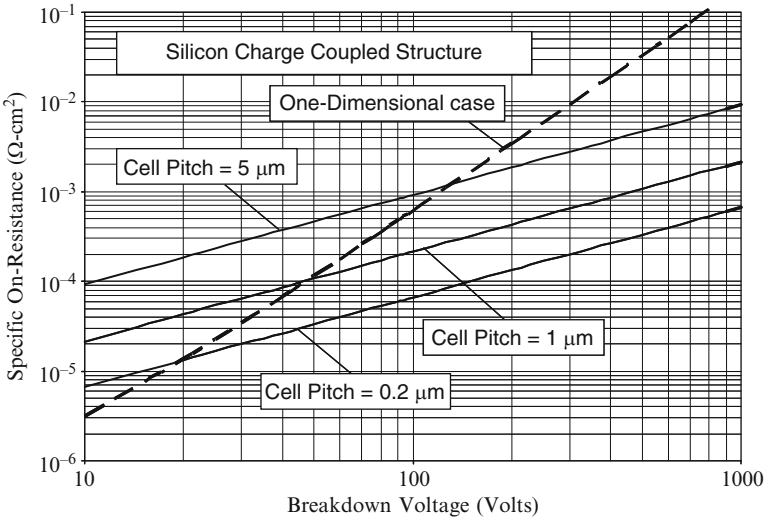

Fig. 1.10 Ideal specific on-resistance for the charge coupled structure. (*solid lines*: charge coupled structures; *dashed line*: one dimensional case)

the specific on-resistance of the drift region is found to be 3.4 mΩ cm^2 if a critical electric field for breakdown of 3×10^5 V/cm is used. In contrast, the specific on-resistance for the drift region of the charge coupled structure with a cell pitch of 1 μm is found to be only 0.43 mΩ cm^2 if a critical electric field for breakdown of 2×10^5 V/cm is used. In this calculation, a bulk mobility of 1,120 cm^2/V s was used corresponding to a doping concentration of 2.6×10^{16}/cm^3 in the N-type portion of the drift region. In this example, the drift region for the charge coupled structure would have a thickness of 10 μm when compared with 12.5 μm needed in the conventional structure.

1.6 Revised Breakdown Models for Silicon

In the textbook [1], the breakdown voltage for silicon devices was analyzed by using the Fulop's power law relating the impact ionization coefficient to the electric field. The Fulop's power law [8] for impact ionization in silicon is given by:

$$\alpha_B(\mathrm{Si}) = 1.80 \times 10^{-35} \mathrm{E}^7 \tag{1.11}$$

The values for the impact ionization coefficient obtained by using this equation are compared with the impact ionization coefficients measured for electrons and holes in silicon [9] as represented by Chynoweth's equation in Fig. 1.11. It can be observed that Fulop's power law falls between that for electrons and holes and

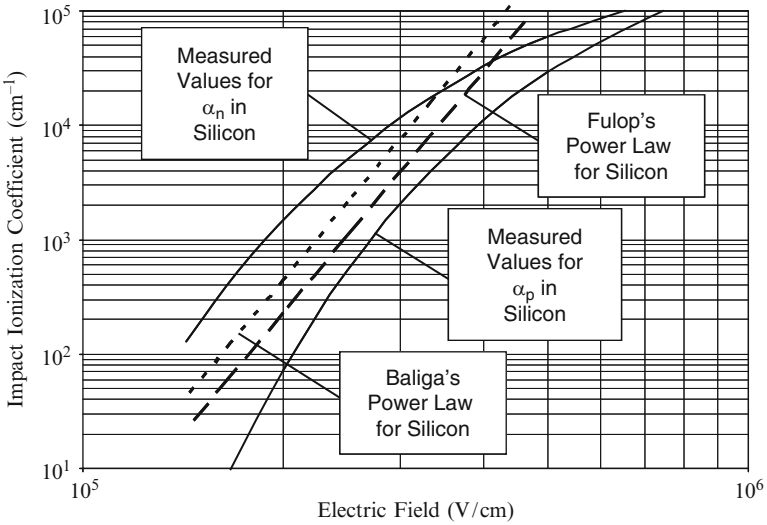

Fig. 1.11 Impact ionization coefficients for silicon

consequently underestimates the values for the impact ionization coefficients for electrons. This results in the prediction of larger breakdown voltages than in actual devices when performing the analytical calculations as pointed out in the textbook.

A better prediction of breakdown in silicon devices using analytical models can be achieved by improving the match between the power law and the measured data for impact ionization coefficients for electrons and holes in silicon. The proposed Baliga's power law for impact ionization in silicon is given by:

$$\alpha_B(\mathrm{Si}) = 3.507 \times 10^{-35} \mathrm{E}^7 \tag{1.12}$$

From Fig. 1.11, it can be observed that this equation provides a larger value for the impact ionization coefficients which will result in reducing the breakdown voltage.

In the case of one-dimensional parallel-plane junctions discussed in Chap. 3 of the textbook, the electric field takes a triangular distribution in the lightly doped side of the P-N junction given by:

$$\mathrm{E}(\mathrm{x}) = -\frac{\mathrm{qN_D}}{\varepsilon_S}(\mathrm{W_D} - \mathrm{x}) \tag{1.13}$$

where $\mathrm{W_D}$ is the depletion layer width, and $\mathrm{N_D}$ is the doping concentration on the lightly doped side of the junction. The breakdown voltage in this case is determined by the ionization integral becoming equal to unity:

$$\int_0^{W_D} \alpha dx = 1 \tag{1.14}$$

Substituting (1.12) into the above equation with the distribution given by (1.13), an expression for the depletion layer width at breakdown can be obtained:

$$W_{PP,B}(Si) = 2.404 \times 10^{10} N_D^{-7/8} \tag{1.15}$$

In contrast, the expression for the depletion layer width at breakdown obtained by using Fulop's power law is given by:

$$W_{PP,F}(Si) = 2.67 \times 10^{10} N_D^{-7/8} \tag{1.16}$$

The depletion layer widths at breakdown obtained for silicon devices by using the above equations can be compared in Fig. 1.12. The depletion layer widths computed using Baliga's power law are 11% smaller than those predicted by Fulop's power law.

The maximum electric field located at the P-N junction for the one-dimensional parallel-plane case is given by:

$$E_M = \frac{qN_D}{\varepsilon_S} W_D \tag{1.17}$$

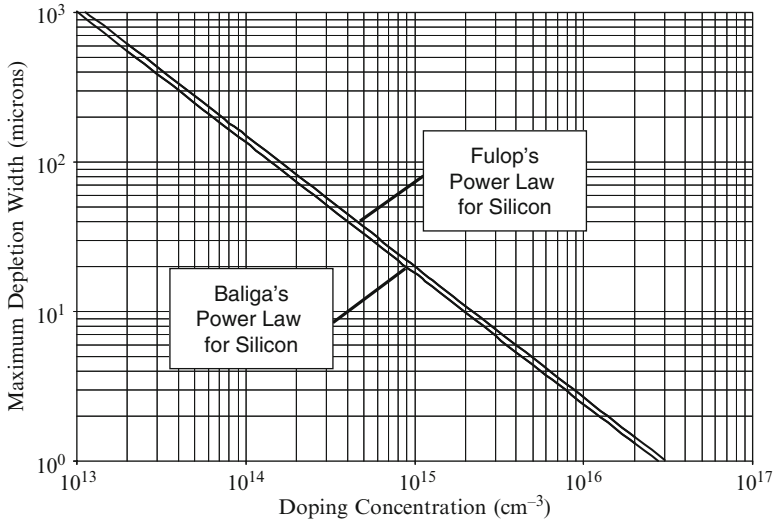

Fig. 1.12 Depletion layer width at breakdown in silicon for the one-dimensional parallel-plane junction

The critical electric field for breakdown of the one-dimensional parallel-plane junction can be obtained by substituting the depletion layer width at breakdown into this equation. In the case of Baliga's power law, the critical electric field for breakdown of the one-dimensional parallel-plane junction is given by:

$$E_{C,1D,B}(Si) = 3,700\ N_D^{1/8} \tag{1.18}$$

In contrast, in the case of Fulop's power law, the critical electric field for breakdown of the one-dimensional parallel-plane junction is given by:

$$E_{C,1D,F}(Si) = 4,010\ N_D^{1/8} \tag{1.19}$$

The critical electric fields for breakdown of the one-dimensional parallel-plane junction obtained for silicon devices by using the above equations can be compared in Fig. 1.13. The critical electric fields for breakdown of the one-dimensional parallel-plane junction computed using Baliga's power law are 8.4% smaller than those predicted by Fulop's power law.

The one-dimensional parallel-plane breakdown voltage for abrupt P-N junctions in silicon can be computed using the critical electric field and the depletion layer width at breakdown:

$$BV_{PP} = \frac{1}{2} E_{C,1D} W_{PP} \tag{1.20}$$

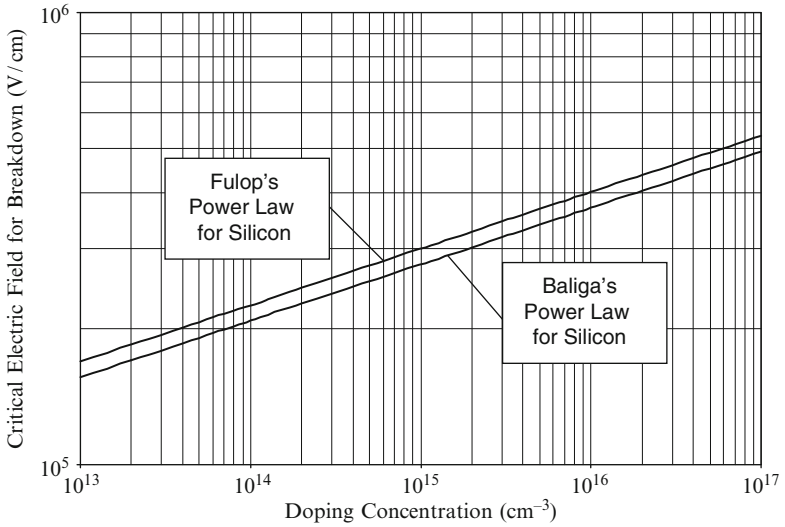

Fig. 1.13 Critical electric fields for breakdown in silicon for the one-dimensional parallel-plane junction

Using the equations derived above for the critical electric field and the depletion layer width at breakdown with Baliga's power law for the impact ionization coefficients, the breakdown voltage of the one-dimensional parallel-plane junction is given by:

$$BV_{PP,B}(Si) = 4.45 \times 10^{13} N_D^{-3/4} \tag{1.21}$$

In contrast, in the case of Fulop's power law, the breakdown voltage of the one-dimensional parallel-plane junction is given by:

$$BV_{PP,F}(Si) = 5.34 \times 10^{13} N_D^{-3/4} \tag{1.22}$$

The breakdown voltage of the one-dimensional parallel-plane junction obtained for silicon devices by using the above equations can be compared in Fig. 1.14. The breakdown voltages for the one-dimensional parallel-plane junction computed using Baliga's power law are 20% smaller than those predicted by Fulop's power law.

The ideal specific on-resistance is defined as the resistance per unit area for the drift region with the doping concentration and thickness corresponding to each breakdown voltage. This resistance can be computed using:

$$R_{on,sp}(Ideal) = \frac{W_{PP}}{q\,\mu_n N_D} \tag{1.23}$$

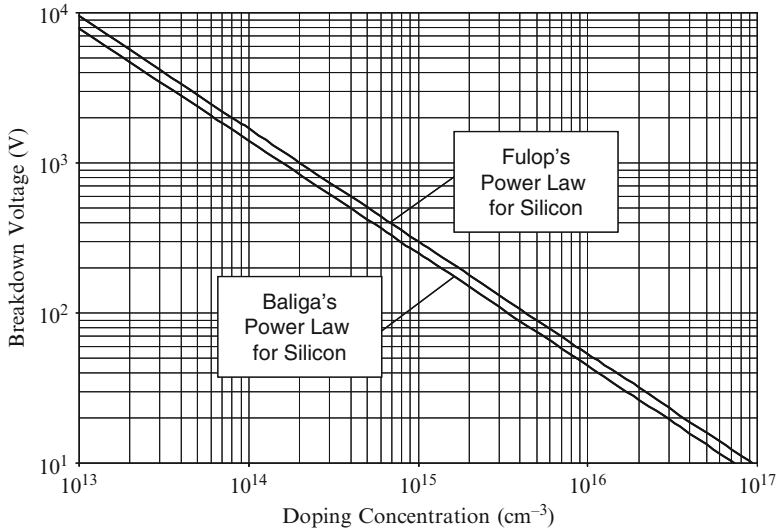

Fig. 1.14 One-dimensional parallel-plane breakdown voltages in silicon

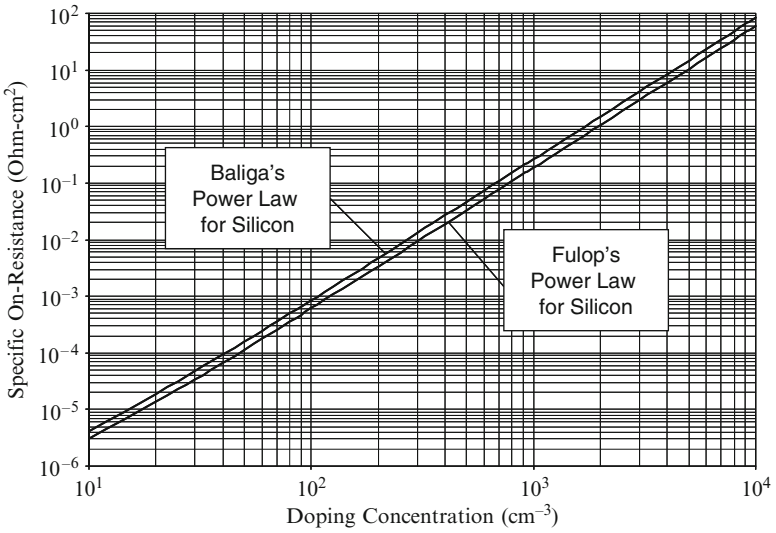

Fig. 1.15 Ideal specific on-resistances for silicon

It is important to include the dependence of the mobility on the doping concentration when computing the ideal specific on-resistance. The ideal specific on-resistance for silicon devices is slightly larger when the Baliga's power law for the impact ionization is utilized as compared with Fulop's power law as shown in Fig. 1.15. At breakdown voltages above 40 V, the mobility in silicon can be assumed to be independent of the doping concentration. The ideal specific on-resistance obtained by using Baliga's power law for the impact ionization coefficients is then given by:

$$R_{on,sp,B}(Si) = 8.37 \times 10^{-9} BV^{2.5} \tag{1.24}$$

In contrast, the ideal specific on-resistance obtained by using Fulop's power law for the impact ionization coefficients is given by:

$$R_{on,sp,F}(Si) = 5.93 \times 10^{-9} BV^{2.5} \tag{1.25}$$

The ideal specific on-resistances for silicon devices computed using Baliga's power law are 40% larger than those predicted by Fulop's power law.

The revised information provided above based up on using Baliga's power law for the impact ionization coefficients is intended to bring the analytical calculations of breakdown voltages in silicon devices more in line with the results of numerical simulations. This information can be used to compute the doping concentration and thickness of the drift region to achieve a desired breakdown voltage for power devices.

1.7 Typical Power MOSFET Applications

Power MOSFETs are used to control power flow to loads. Two typical examples for the application of high performance power MOSFETs are provided in this section to emphasize the characteristics of importance from an application standpoint. The first example is in the 'Sync-Buck' converter used to reduce the voltage from one DC level to another smaller value. This circuit is popular for providing power to microprocessors in computers and laptops. The second example is in variable speed motor drives. This application is popular for operating induction motors with variable loads leading to large gains in efficiency.

1.7.1 DC-DC Sync-Buck Converter

The sync-buck converter can be regarded as a DC-to-DC transformer because of its ability to reduce a DC input voltage to a smaller DC output voltage. As mentioned above, one popular application of the sync-buck converter is to provide power to various loads inside a computer from the back-plane DC power supply. The back-plane power supply has a typical voltage range of 17–20 V depending on the type of computer. Loads, such as disk drives require a DC voltage of 5–12 V. In contrast, integrated circuits in the computer, such as the microprocessor and graphics chips, require a lower DC voltage in the range of 1–2 V.

The commonly used sync-buck topology used for the DC-to-DC voltage conversion in computers is shown in Fig. 1.16. Due to the relatively low operating voltage in this circuit, a power MOSFET is typically used as the switch in the high-side location. When the transistor is turned on by the control circuit, current flows from the DC input source through the inductor to the load connected at the output terminals. When the transistor is switched off by the control circuit, the load current

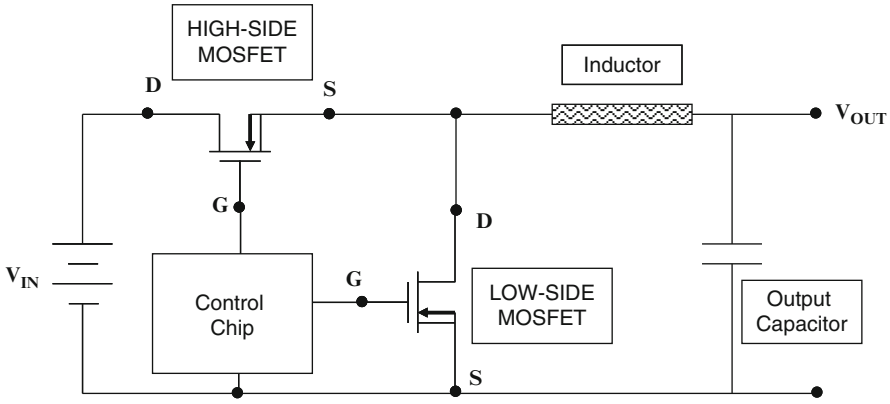

Fig. 1.16 Sync-buck DC-DC converter circuit

circulates through the MOSFET connected on the low-side and the inductor. The regulation of the DC output voltage can be achieved by adjusting the on-time of the transistor [10]. The switching waveforms for the high-side transistor are similar to those shown in Fig. 1.2. The waveforms for the low-side transistor are a complement of those for the high-side transistor. The efficiency of the sync-buck converter is determined by the on-resistance and switching speed of the two transistors.

The low-side MOSFET is also referred to as a synchronous rectifier. The current flow in the low-side MOSFET is in the opposite direction to the normal operation of power MOSFET devices. If the low-side power MOSFET is turned on by the control circuit, the current flow occurs with a voltage drop determined by the on-resistance of the MOSFET structure. This voltage drop is usually much smaller than the built-in potential of the junction between the P-base region and the N-drift region (called the body-diode of the MOSFET). However, if the low-side MOSFET is not turned-on, the current will flow through the body-diode. This not only increases power losses due to the high on-state voltage drop of the P-N junction, it also severely slows down the switching time due to the long reverse recovery time for the body-diode.

The high-side and low-side MOSFET devices cannot be simultaneously turned-on during circuit operation to avoid short-circuiting the input power source. This requires delaying the turn-on of the low-side transistor after the gate bias to the high-side transistor has been turned-off. During this delay-time interval, the current in the low-side MOSFET flows through its body-diode. This upsets high frequency operation of the circuit. One method to overcome this problem is to connect an external Schottky rectifier across the low-side switch. This has not been found to be an effective solution because of the inductance between the low-side MOSFET and the Schottky diode in the packages and circuit boards. An elegant solution to this problem is to integrate the Schottky rectifier into the power MOSFET structure. These MOSFET structures are also discussed in this monograph in Chap. 8.

1.7.2 Variable-Frequency Motor Drive

A significant increase in the efficiency for running motors can be achieved by using variable-frequency motor drives, in place of constant speed drives, with dampers to regulate the output. The most commonly used topology converts the constant frequency input AC power to a DC bus voltage and then use an inverter stage to produce the variable frequency output power [11]. The circuit diagram for a three-phase motor drive system is shown in Fig. 1.17. Six IGBTs are used with six fly-back rectifiers in the inverter stage to deliver the variable frequency power to the motor windings. A pulse-width-modulation (PWM) scheme is used to generate the variable frequency AC voltage waveform that is fed to the motor windings [12].

During each cycle of the PWM period, the current in the motor winding can be considered to remain approximately constant. This allows linearization of the waveforms for the current and voltage experienced by the IGBTs and the rectifiers. Typical waveforms for the transistor and the fly-back diode are illustrated in

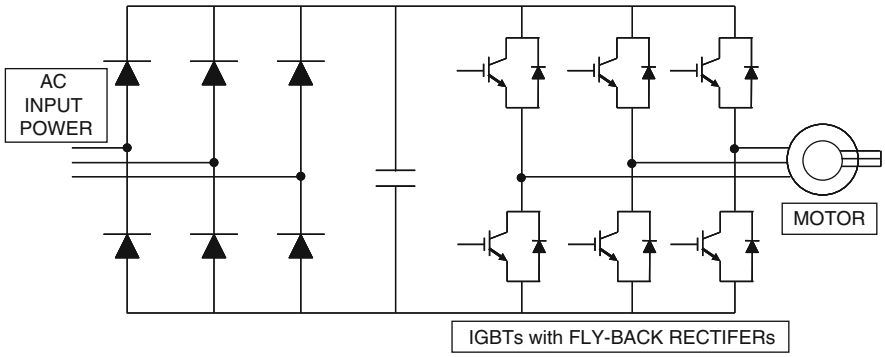

Fig. 1.17 Variable frequency motor drive circuit

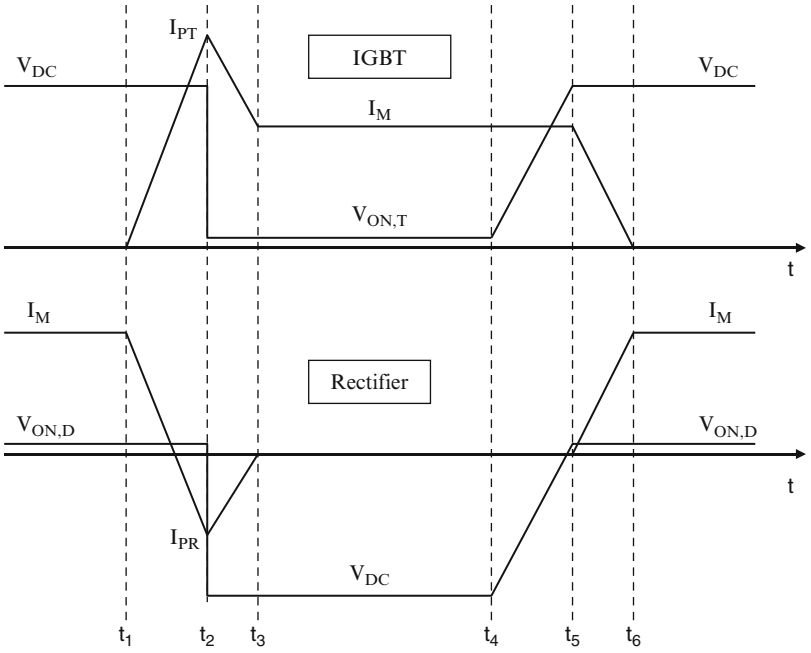

Fig. 1.18 Linearized waveforms for the PWM motor drive circuit

Fig. 1.18. The large reverse recovery current typically observed in silicon P-i-N rectifiers during the time interval from t_1 to t_3 produces high power dissipation not only in the diodes but also in the transistors [1]. This power loss can be eliminated by replacing the silicon P-i-N rectifiers with silicon carbide Schottky rectifiers.

With the availability of high voltage silicon carbide Schottky rectifiers, the power loss in the motor control application becomes dominated by the on-state and turn-off losses in the IGBTs [13]. The development of high performance power MOSFETs can reduce these power losses making the motor drive more efficient.

The on-resistances of the conventional silicon power MOSFET structures shown in Fig. 1.5 are too large for typical high voltage motor drive applications, such as for electric vehicles with a DC-bus voltage of 400 V, due to their high (600 V) blocking voltage capability. The on-resistance of silicon power MOSFETs can be reduced by using the charge coupling concept as discussed in this monograph. A reduction in the on-resistance can also be achieved by replacing silicon with silicon carbide based power MOSFET structures. Power MOSFET structures that are suitable for implementation in silicon carbide material are therefore also discussed in this monograph.

1.8 Summary

The desired characteristics for power MOSFET structures have been reviewed in this chapter. The characteristics of typical devices have been compared with those for the ideal case. The ability to reduce the on-resistance by using the two-dimensional charge coupling effect has been described. Improved analytical expressions for computation of the breakdown voltage in silicon devices have been derived using a proposed Baliga's power law for impact ionization coefficients. Typical applications for the power MOSFETs have also been discussed to highlight the device characteristics that are desired for the applications. Various power MOSFET structures are discussed in detail in subsequent chapters of this book.

References

1. B.J. Baliga, "Fundamentals of Power Semiconductor Devices", Springer Science, New York, 2008.
2. B.J. Baliga, "Silicon Carbide Power Devices", World Scientific Press, Singapore, 2005.
3. B.J. Baliga, "Silicon RF Power Devices", World Scientific Press, Singapore, 2005.
4. B.J. Baliga, "Modern Power Devices", Wiley, New York, 1987.
5. B.J. Baliga, "Semiconductors for High Voltage Vertical Channel Field Effect Transistors", Journal of Applied Physics, Vol. 53, pp. 1759–1764, 1982.
6. B.J. Baliga, et al, "Gallium Arsenide Schottky Power Rectifiers", IEEE Transactions on Electron Devices, Vol. ED-32, pp. 1130–1134, 1985.
7. M. Bhatnagar, P.M. McLarty, and B.J. Baliga, "Silicon Carbide High Voltage (400 V) Schottky Barrier Diodes", IEEE Electron Device Letters, Vol. EDL-13, pp. 501–503, 1992.
8. W. Fulop, "Calculation of Avalanche Breakdown in Silicon P-N Junctions", Solid State Electronics, Vol. 10, pp. 39–43, 1967.
9. R. Van Overstraeten and H. DeMan, "Measurements of the Ionization Rates in Diffused Silicon P-N Junctions", Solid State Electronics, Vol. 13, pp. 583–608, 1970.
10. N. Mohan, T.M. Undeland, and W.P. Robbins, "Power Electronics", pp. 164–172, Wiley, New York, 1995.
11. J.D. van Wyk, "Power Electronic Converters for Drives", pp. 81–137, in 'Power Electronics and Variable Frequency Drives', Edited by B.K. Bose, IEEE Press, New Jersey, 1997.
12. J. Holtz, "Pulse Width Modulation for Electronic Power Conversion", pp. 138–208, in 'Power Electronics and Variable Frequency Drives', Edited by B.K. Bose, IEEE Press, 1997.
13. B.J. Baliga, "Advanced Power Rectifier Concepts", Springer-Science, New York, 2009.

Chapter 2
D-MOSFET Structure

The first power MOSFET structure commercially introduced by the power semiconductor industry was the double-diffused or D-MOSFET structure. The channel length of this device could be reduced to sub-micron dimensions by controlling the diffusion depths of the P-base and N^+ source regions without resorting to expensive lithography tools [1]. The device fabrication process relied up on the available planar gate technology used to manufacture CMOS integrated circuits. These devices found applications in power electronic circuits that operated at low ($<$100 V) voltages. The fast switching speed and ruggedness of the D-MOSFET structure were significant advantages compared with the performance of the available bipolar power transistor.

The physics of operation of the power D-MOSFET structure has been analyzed in detail in the textbook [1]. In this chapter of the monograph, a brief description of the device operation is provided for completeness and for contrasting it to the advanced device structures that are discussed in later chapters. However, a detailed discussion of the characteristics of a device rated for blocking 30 V is provided here based up on the results of two-dimensional numerical simulations. These characteristics will be used as a bench-mark for comparison with the characteristics of the advanced power MOSFET structures described in other chapters.

2.1 The D-MOSFET Structure

A cross-section of the basic cell structure for the D-MOSFET structure is illustrated in Fig. 2.1. This device structure is fabricated by starting with an N-type epitaxial layer grown on a heavily doped N^+ substrate. The channel is formed by the difference in lateral extension of the P-base and N^+ source regions produced by their diffusion cycles. Both regions are self-aligned to the left-hand-side and right-hand-side of the gate region during ion-implantation to introduce the respective dopants. A refractory gate electrode, such as polysilicon, is required to allow diffusion of the dopants under the gate electrode at elevated temperatures.

B.J. Baliga, *Advanced Power MOSFET Concepts*,
DOI 10.1007/978-1-4419-5917-1_2,

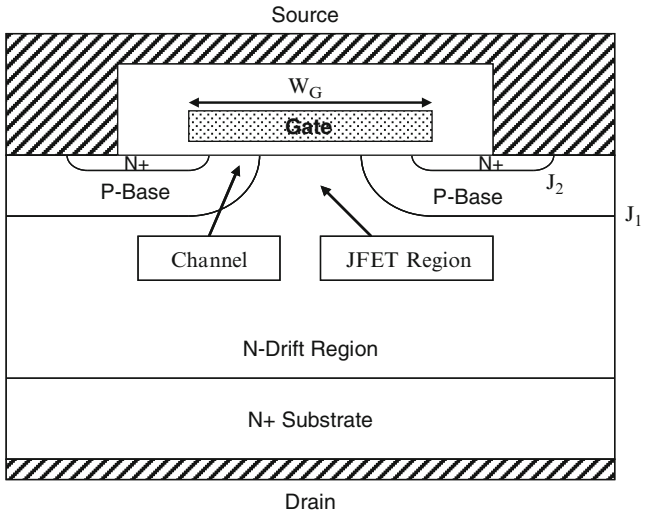

Fig. 2.1 The D-MOSFET structure

Without the application of a gate bias, a high voltage can be supported in the D-MOSFET structure when a positive bias is applied to the drain. In this case, junction J_1 formed between the P-Base region and the N-drift region becomes reverse biased. The voltage is supported mainly within the thick lightly doped N-drift region. Drain current flow in the D-MOSFET structure is induced by the application of a positive bias to the gate electrode. This produces an inversion layer at the surface of the P-base region under the gate electrode. This inversion layer channel provides a path for transport of electrons from the source to the drain when a positive drain voltage is applied.

After transport from the source region through the channel, the electrons enter the N-drift region at the upper surface of the device structure. They are then transported through a relatively narrow JFET region located between the adjacent P-base regions within the D-MOSFET structure. The constriction of the current flow through the JFET region substantially increases the internal resistance of the D-MOSFET structure. A careful optimization of the gate width (W_G) is required, in order to minimize the internal resistance for this structure as discussed in the textbook. In addition, it is customary to enhance the doping concentration in the JFET region to reduce the resistance to current flow through this portion of the device structure.

After being transported through the JFET region, the electrons enter the N-drift region below junction J_1. The current spreads from the relatively narrow JFET region to the entire width of the cell cross-section. This non-uniform current distribution within the drift region enhances its resistance making the internal resistance of the D-MOSFET structure larger than the ideal specific on-resistance of the drift region. The large internal resistance for the D-MOSFET structure has provided motivation for the development of the trench-gate power MOSFET

structure in the 1990s and the advanced power MOSFET structures discussed in this monograph.

2.2 Power D-MOSFET On-Resistance

The power D-MOSFET structure is shown in Fig. 2.2 with its internal resistance components. There are eight resistances that must be analyzed in order to obtain the total on-resistance between the source and drain electrodes when the device is turned-on. It is customary to analyze not only the resistance for a particular cell design but also the specific resistance for each of the components by multiplying the cell resistance with the cell area. The total on-resistance for the power MOSFET structure is obtained by the addition of all the resistances because they are considered to be in series in the current path between the source and the drain electrodes:

$$R_{ON} = R_{CS} + R_{N+} + R_{CH} + R_A + R_{JFET} + R_D + R_{SUB} + R_{CD} \tag{2.1}$$

Each of the resistances within the power D-MOSFET structure is analyzed below by using the procedure described in the textbook. In the textbook, it was demonstrated that the contributions from the source contact resistance (R_{CS}), the source resistance (R_{N+}), and the drain contact resistance (R_{CD}) are very small and will therefore be neglected in this and subsequent chapters.

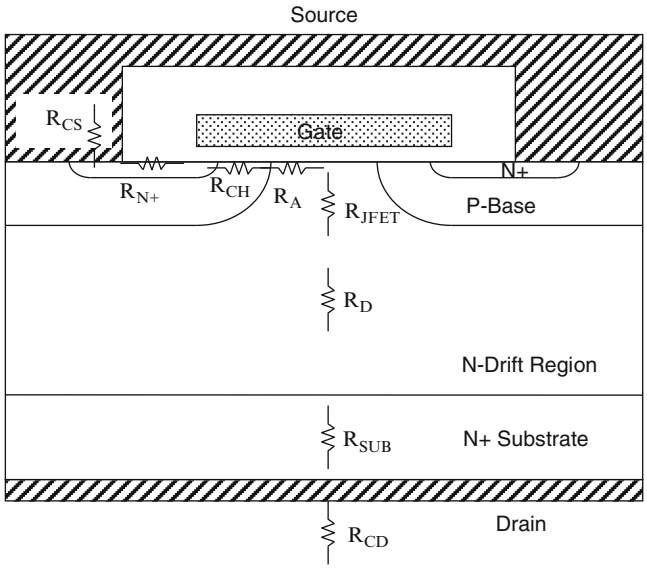

Fig. 2.2 Power D-MOSFET structure with its internal resistances

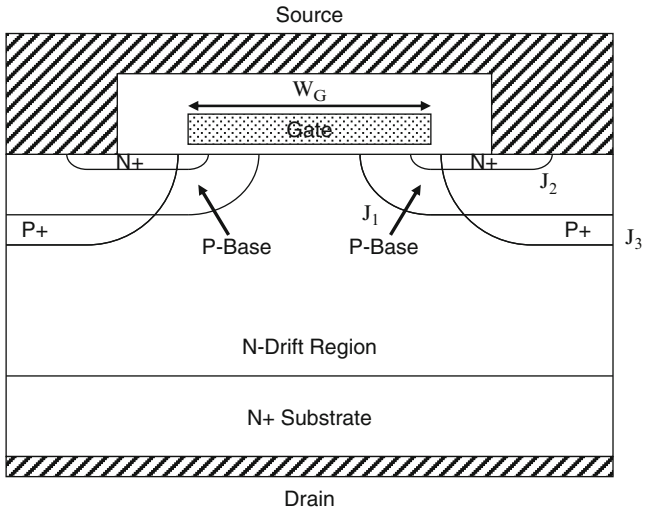

Fig. 2.3 Power D-MOSFET structure with deep P+ region

The on-resistance of the basic structure for the power D-MOSFET device has been analyzed in the textbook. Typical power D-MOSFET products include a deep P^+ region as illustrated in Fig. 2.3 to improve their ruggedness and safe-operating-area as discussed in the textbook. The analysis of the power D-MOSFET structure in this monograph includes the presence of this deep P^+ region. The blocking voltage for the device must be supported at the junction J_3 between the P^+ region and the N-drift region. The thickness of the N-drift region below the deep P^+ region must be sufficient to allow supporting the blocking voltage. This increases the on-resistance contribution from the drift region as discussed below.

A cross-section of the power D-MOSFET structure is illustrated in Fig. 2.4 with various dimensions that can be used for the analysis of the on-resistance components. Here, W_{Cell} is the pitch for the linear cell geometry analyzed in this section; W_G is the width of the gate electrode; W_{PW} is the width of the polysilicon window; W_C is the width of the contact window to the N^+ source and P-base regions; and W_S is the width of the photoresist mask used during the N^+ source ion-implantation. The junction depths of the P-base region and the deep P^+ region are x_{JP} and x_{JP+}, respectively.

In this monograph, the characteristics of advanced power MOSFET structures with 30-V blocking capability will be analyzed for power supply applications. For this voltage rating and the typical lithography design rules, the power D-MOSFET structure has a cell pitch (W_{CELL}) of 12 μm with a polysilicon gate width (W_G) of 8 μm. Typical junction depths for the N^+ source region, P-base region, and the P^+ region are 0.5, 1.5, and 2.5 μm, respectively. The doping concentration of the N-drift region required to achieve a 30-V blocking voltage capability, with an

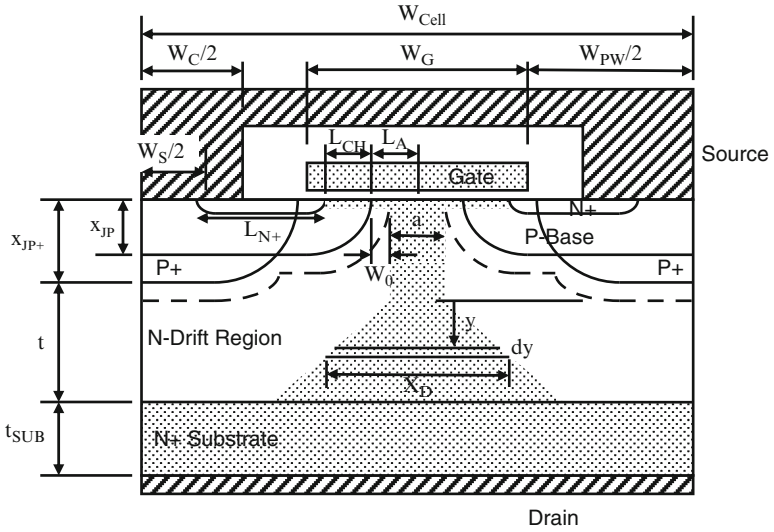

Fig. 2.4 Power D-MOSFET structure with current flow model A used for analysis of its internal resistances

80% reduction due to the edge termination, is $1.6 \times 10^{16}/\text{cm}^3$. The thickness of the N-drift region required below the deep P^+ region is 2.6 μm. It is worth pointing out that the entire blocking voltage is not supported within the N-drift region because of the graded doping profile of the P-base and the P^+ regions. This allows increasing the doping concentration and reducing the thickness of the N-drift region to achieve a smaller specific on-resistance for the D-MOSFET structure.

The current flow pattern in the power D-MOSFET structure is indicated by the shaded area in Fig. 2.4. In the first Model A for the specific on-resistance, it will be assumed that the JFET region extends to the bottom of the deep P^+ region. Consequently, this model assumes that there is current constriction by the deep P^+ regions. In the model, it is assumed that the current spreads at a 45° angle in the drift region and then becomes uniformly distributed when it enters the N^+ substrate. For the dimensions provided above for the D-MOSFET structure with 30-V blocking voltage capability, the current does not spread across the entire region below the windows in the gate electrode resulting in the current distribution shown in Fig. 2.4 by the shaded area.

An alternate Model B for the current distribution in the D-MOSFET structure is illustrated in Fig. 2.5. In this model, it is assumed that the junction formed by the P^+ regions (J_3) is too far from the current path in the JFET region to contribute to current constriction. The JFET current constriction is then assumed to be associated only with the junction (J_1) formed by the P-base region. The JFET region is then assumed to extend to the bottom of the P-base region as shown in the figure by the shaded area. This model produces a smaller contribution to the specific

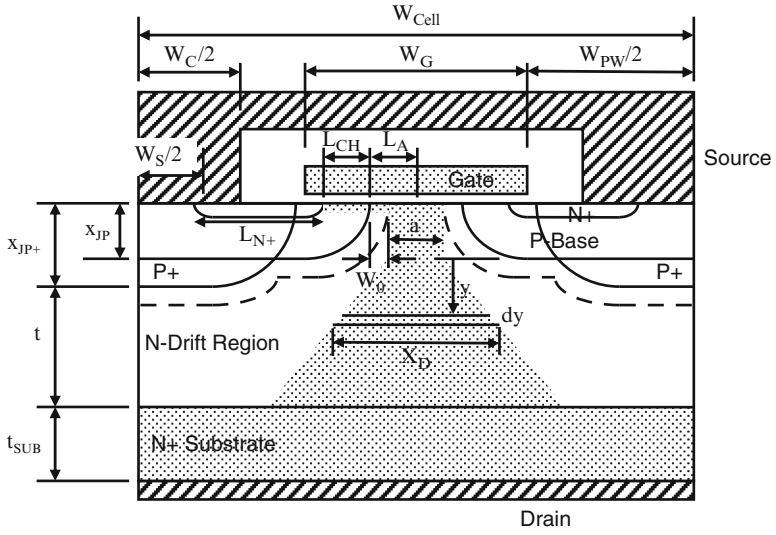

Fig. 2.5 Power D-MOSFET structure with current flow model B used for analysis of its internal resistances

on-resistance from the JFET region than Model A but the contribution from the drift region is enhanced.

2.2.1 Channel Resistance

The contribution to the specific on-resistance from the channel in the D-MOSFET structure is the same for models A and B. As derived in the textbook [1], the specific on-resistance contributed by the channel in the power D-MOSFET structure is given by:

$$R_{CH,SP} = \frac{L_{CH} W_{Cell}}{2\mu_{ni} C_{OX}(V_G - V_{TH})} \tag{2.2}$$

In the case of the 30-V power MOSFET structures used for power supply applications, it is customary to provide the on-resistance at a gate bias of 4.5 and 10 V. Assuming a gate oxide thickness is 500 Å, an inversion layer mobility of 450 cm^2/V s (to match the mobility used in the numerical simulations discussed later in this section), and a threshold voltage of 2 V in the above equation for the power D-MOSFET design with a cell width of 12 μm and gate electrode width of 8 μm, the specific resistance contributed by the channel at a gate bias of 4.5 V is found to be 0.784 mΩ cm^2. The specific on-resistance of the D-MOSFET structure is reduced to 0.245 mΩ cm^2 when the gate bias is increased to 10 V.

2.2.2 Accumulation Resistance

In the power MOSFET structure, the current flowing through the inversion channel enters the drift region at the edge of the P-base junction. The current then spreads from the edge of the P-base junction into the JFET region. The current spreading phenomenon is aided by the formation of an accumulation layer in the semiconductor below the gate oxide due to the positive gate bias applied to turn-on the device. The specific on-resistance contributed by the accumulation layer in the power D-MOSFET structure is given by [1]:

$$R_{A,SP} = K_A \frac{(W_G - 2x_{JP})W_{Cell}}{4\mu_{nA}C_{OX}(V_G - V_{TH})} \tag{2.3}$$

In writing this expression, a coefficient K_A has been introduced to account for the current spreading from the accumulation layer into the JFET region. A typical value for this coefficient is 0.6 based upon the current flow observed from numerical simulations of power D-MOSFET structures. The threshold voltage in the expression is for the on-set of formation of the accumulation layer. A zero threshold voltage will be assumed here when performing the analytical computations. Note that the junction depth of the P-base region (and not the P^+ region) defines the length of the accumulation region.

For the 30-V power D-MOSFET design with a cell width of 12 μm and gate width of 8 μm, the specific resistance contributed by the accumulation layer at a gate bias of 4.5 V is 0.294 mΩ cm^2 if the P-base junction depth (x_{JP}) is 1.5 μm and the gate oxide thickness is 500 Å. An accumulation layer mobility of 1,000 cm^2/V s was used in this calculation to match the mobility used in the numerical simulations (discussed later in this section). When the gate bias is increased to 10 V, the specific resistance contributed by the accumulation layer is reduced to 0.132 mΩ cm^2.

2.2.3 JFET Resistance

The electrons entering from the channel into the drift region are distributed into the JFET region via the accumulation layer formed under the gate electrode. The spreading of current in this region was accounted for by using a constant K_A of 0.6 for the accumulation layer resistance. Consequently, the current flow through the JFET region can be treated with a uniform current density. In the power D-MOSFET structure, the cross-sectional area for the JFET region increases with distance below the semiconductor surface due to the planar shape of the P-base junction. However, in order to simplify the analysis, a uniform cross-section for the current flow with a width 'a' will be assumed for the JFET region as illustrated by

the shaded area in Figs. 2.4 and 2.5. The width of the current flow is related to the device structural parameters:

$$a = (W_G - 2x_{JP} - 2W_0) \tag{2.4}$$

where W_0 is the zero-bias depletion width for the JFET region. The depletion region boundary is indicated in the figures with the dashed lines. In the models, it is assumed that no current can flow through the depleted region because all the free carriers have been swept out by the prevailing electric field across the junction. The zero-bias depletion width (W_0) in the JFET region can be computed by using the doping concentrations on both sides of the junction:

$$W_0 = \sqrt{\frac{2\varepsilon_S N_A V_{bi}}{qN_{DJ}(N_A + N_{DJ})}} \tag{2.5}$$

where N_A is the doping concentration in the P-base region and N_{DJ} is the doping concentration in the JFET region. In the above equation, the built-in potential is also related to the doping concentrations on both sides of the junction:

$$V_{bi} = \frac{kT}{q} \ln\left(\frac{N_A N_{DJ}}{n_i^2}\right) \tag{2.6}$$

In practical devices, the P-base region is diffused into the N-drift region producing a graded doping profile. However, these expressions based upon assuming a uniform doping concentration for the P-base region are adequate for analytical computations. It is common practice to enhance the doping concentration for the JFET region above that for the drift region. It is therefore appropriate to use the enhanced doping concentration (N_{DJ}) of the JFET region in the above expressions.

In Model A, the JFET region is assumed to extend to the bottom the P^+ region. The specific on-resistance contributed by the JFET region in the power D-MOSFET structure can then be obtained by using:

$$R_{JFET,SP} = \frac{\rho_{JFET} x_{JP+} W_{Cell}}{(W_G - 2x_{JP} - 2W_0)} \tag{2.7}$$

where ρ_{JFET} is the resistivity of the JFET region given by:

$$\rho_{JFET} = \frac{1}{q\mu_n N_{DJ}} \tag{2.8}$$

where μ_n is the bulk mobility appropriate to the doping level of the JFET region. Typical power D-MOSFET structures are fabricated by using a diffused JFET doping profile with its maximum concentration at the surface and a depth

approximately the same as the junction depth of the P-base region. In an analytical model, it is convenient to use an average doping concentration for the JFET region. The resistivity for the JFET region is found to be 0.269 Ω cm corresponding to an average JFET doping concentration of $2.0 \times 10^{16}/\text{cm}^3$. The zero-bias depletion width in the JFET region for this JFET doping concentration is 0.228 μm. For the 30-V power D-MOSFET design with a cell width of 12 μm and gate width of 8 μm, the specific resistance contributed by the JFET region is found to be 0.178 mΩ cm^2 based up on using the above parameters.

In Model B, the JFET region is assumed to extend to the bottom the P-base region. The specific on-resistance contributed by the JFET region in the power D-MOSFET structure can then be obtained by using:

$$R_{JFET,SP} = \frac{\rho_{JFET} x_{JP} W_{Cell}}{(W_G - 2x_{JP} - 2W_0)} \tag{2.9}$$

For the 30-V power D-MOSFET design with a cell width of 12 μm and gate width of 8 μm, the specific resistance contributed by the JFET region is found to be 0.107 mΩ cm^2 based up on using the same parameters as for Model A. It can be observed that the JFET resistance is smaller in Model B than for Model A due to the shorter path for current flow in the vertical direction.

2.2.4 Drift Region Resistance

The resistance contributed by the drift region in the power D-MOSFET structure is enhanced well above that for the ideal drift region due to current spreading from the JFET region. The cross-sectional area for the current flow in the drift region increases from the width 'a' of the JFET region as illustrated in Figs. 2.4 and 2.5 by the shaded area. Several models for this current spreading have been proposed in the literature [2]. The current distribution model used in this monograph is based up on a spreading angle of 45°.

In the case of Model A, the current spreads from the bottom of the P^+ region as shown in Fig. 2.4. The specific on-resistance contributed by the drift region in the power D-MOSFET structure with this model is given by:

$$R_{D,SP} = \frac{\rho_D W_{Cell}}{2} \ln\left[\frac{a + 2t}{a}\right] \tag{2.10}$$

For the parameters given above for this structure, the dimension 'a' in the equation is found to be 2.54 μm. For the 30-V power MOSFET design with a cell width of 12 μm and gate width of 8 μm, the specific resistance contributed by the drift region is then found to be 0.149 mΩ cm^2 by using a resistivity of the drift region of 0.325 Ω cm based upon a doping concentration of $1.6 \times 10^{16}/\text{cm}^3$.

In the case of Model B, the current spreads from the bottom of the P-base region as shown in Fig. 2.5. The specific on-resistance contributed by the drift region in the power D-MOSFET structure with this model is given by:

$$R_{D,SP} = \frac{\rho_D W_{Cell}}{2} \ln\left[\frac{a + 2[t+(x_{JP+} - x_{JP})]}{a}\right] \tag{2.11}$$

For the parameters given above for the 30-V power MOSFET design with a cell width of 12 μm and gate width of 8 μm, the specific resistance contributed by the drift region is then found to be 0.185 mΩ cm^2 by using a resistivity of the drift region of 0.325 Ω cm based upon a doping concentration of 1.6×10^{16}/cm^3. Consequently, the drift region resistance contribution is larger for Model B than for Model A.

2.2.5 N^+ Substrate Resistance

When the current reaches the bottom of the N-drift region, it is very quickly distributed throughout the heavily doped N^+ substrate. The current flow through the substrate can therefore be assumed to occur with a uniform cross-sectional area. Under this assumption, the specific resistance contributed by the N^+ substrate is given by:

$$R_{SUB,SP} = \rho_{SUB} t_{SUB} \tag{2.12}$$

where ρ_{SUB} and t_{SUB} are the resistivity and thickness of the N^+ substrate. The contribution from the N^+ substrate is therefore dependent up on the available technology for reducing its thickness and resistivity while maintaining good manufacturability. Since many manufacturers have reduced this contribution to well below that from the other resistance contributions, the substrate contribution will be assumed to be negligible in this monograph for all the power MOSFET structures.

2.2.6 Drain and Source Contact Resistance

During the initial development of power MOSFET products, the contact resistance to the source region was performed using aluminum metallization. This method resulted in relatively high contact resistance to the N^+ source region. With the advent of metal-silicides for ohmic contacts, the source contact resistance is now much smaller than the other resistance components and can be neglected for all the power MOSFET structures discussed in this monograph. The process technology for making contacts to the drain regions has also evolved to the state that this resistance can be neglected for power MOSFET structures.

2.2.7 Total On-Resistance

The total specific on-resistance for the power D-MOSFET structure can be computed by adding all the above components for the on-resistance. For the case of the 30-V power D-MOSFET design with a cell pitch (W_{Cell}) of 12 μm and gate width of 8 μm, the total specific on-resistance is found to be 1.405 mΩ cm^2 at a gate bias of 4.5 V and 0.704 mΩ cm^2 at a gate bias of 10 V by using Model A. For this cell design, the total specific on-resistance is found to be 1.370 mΩ cm^2 at a gate bias of 4.5 V and 0.669 mΩ cm^2 at a gate bias of 10 V by using Model B. Consequently, Model B predicts a smaller total specific on-resistance than Model A. The contributions from each of the components of the on-resistance are summarized in Figs. 2.6 and 2.7 for the two models.

The ideal specific on-resistance for a drift region is given by:

$$R_{IDEAL,SP} = \frac{W_{PP}}{q\,\mu_n N_D} \tag{2.13}$$

where W_{PP} is the parallel-plane depletion width at breakdown, N_D is the doping concentration of the drift region to sustain the blocking voltage, and μ_n is the mobility for electrons corresponding to this doping concentration. For the case of

Resistance	V_G = 4.5 V (mΩ-cm^2)	V_G = 10 V (mΩ-cm^2)
Channel ($R_{CH,SP}$)	0.784	0.245
Accumulation ($R_{A,SP}$)	0.294	0.132
JFET ($R_{JFET,SP}$)	0.178	0.178
Drift ($R_{D,SP}$)	0.149	0.149
Total ($R_{T,SP}$)	1.405	0.704

Fig. 2.6 On-resistance components within the 30-V power D-MOSFET structure using model A

Resistance	V_G = 4.5 V (mΩ-cm^2)	V_G = 10 V (mΩ-cm^2)
Channel ($R_{CH,SP}$)	0.784	0.245
Accumulation ($R_{A,SP}$)	0.294	0.132
JFET ($R_{JFET,SP}$)	0.107	0.107
Drift ($R_{D,SP}$)	0.185	0.185
Total ($R_{T,SP}$)	1.370	0.669

Fig. 2.7 On-resistance components within the 30-V power D-MOSFET structure using model B

a blocking voltage of 30 V, the depletion width and doping concentration are found to be $2.2 \times 10^{16}/cm^3$ and 1.4 μm, respectively. Using the electron mobility for this doping level, the ideal specific on-resistance is found to be 0.034 mΩ cm^2. Since the device is constrained by the impact of an 80% reduction of breakdown voltage due to the edge termination, it is worth computing the ideal specific on-resistance for this case for comparison with the device. For the case of a blocking voltage of 37.5 V, the depletion width and doping concentration are found to be $1.6 \times 10^{16}/cm^3$ and 1.8 μm, respectively. Using the electron mobility for this doping level, the ideal specific on-resistance is found to be 0.059 mΩ cm^2. It can be observed that the specific on-resistance for the D-MOSFET structure is far greater than these ideal specific on-resistances.

2.2.7.1 Simulation Results

The results of two-dimensional numerical simulations on the 30-V power D-MOSFET structure are described here to provide a more detailed understanding of the underlying device physics and operation. The structure used for the numerical simulations had a drift region thickness of 2.6 μm below the P^+ region with a doping concentration of $1.6 \times 10^{16}/cm^3$. The P-base region and N^+ source regions had depths of 1.7 and 0.7 μm, respectively. The doping concentration in the JFET region was enhanced by using an additional n-type doping concentration of $1 \times 10^{16}/cm^3$ with a depth of 1.5 μm. For the numerical simulations, half the cell (with a width of 6 μm) shown in Fig. 2.1 was utilized as a unit cell that is representative of the structure.

A three dimensional view of the doping distribution in the D-MOSFET structure is shown in Fig. 2.8 from the left hand edge of the structure to the center of the polysilicon gate region. The N^+ source and P-base regions are aligned to the gate edge, which is located at 2 μm from the left hand side. The structure also includes a P^+ region located at the left hand side to suppress the parasitic bipolar transistor. The enhancement of the doping in the N-drift region near the surface is due to the additional JFET doping.

The lateral doping profile taken along the surface under the gate electrode is shown in Fig. 2.9. From the profile, it can be observed that the doping concentration of the JFET region has been increased to $2.3 \times 10^{16}/cm^3$ due to the additional doping. The lateral extension of the P-base and N^+ source regions are 1.7 and 0.7 μm leading to a channel length of 1.0 μm. The surface concentration for the P-base region was chosen to obtain a maximum compensated P-type doping concentration in the channel of $1.0 \times 10^{17}/cm^3$.

The transfer characteristics for the D-MOSFET structure were obtained using numerical simulations with a drain bias of 0.1 V at 300 and 400°K. The resulting transfer characteristics are shown in Fig. 2.10. From this graph, a threshold voltage of 3.1 and 2.6 V can be extracted at 300 and 400°K, respectively. The threshold voltage decreases by 16% when the temperature increases. The specific on-resistance can be obtained from the transfer characteristics at any gate bias voltage.

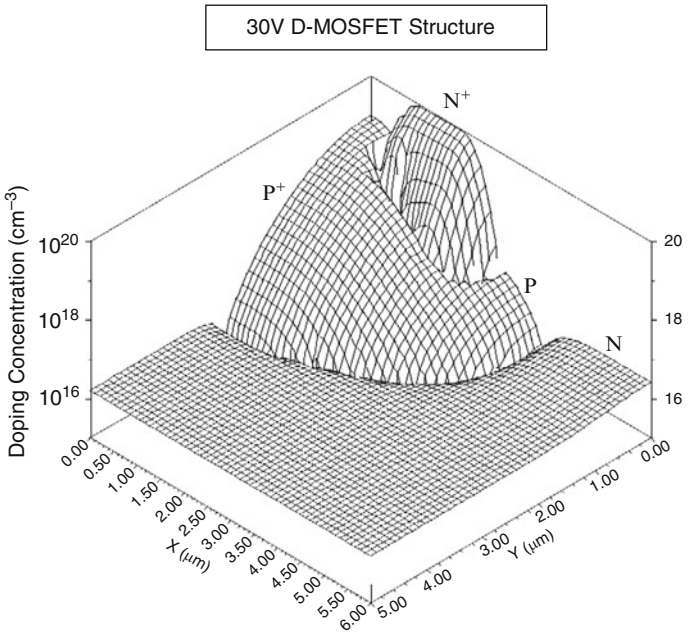

Fig. 2.8 Doping distribution for the D-MOSFET structure

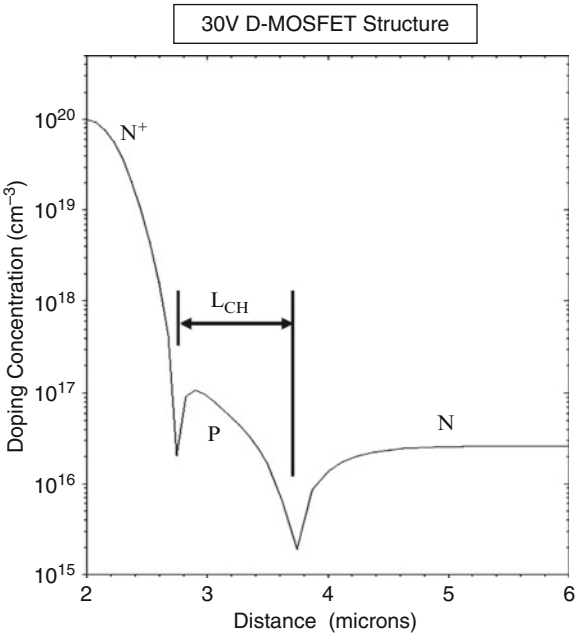

Fig. 2.9 Channel doping profile for the D-MOSFET structure

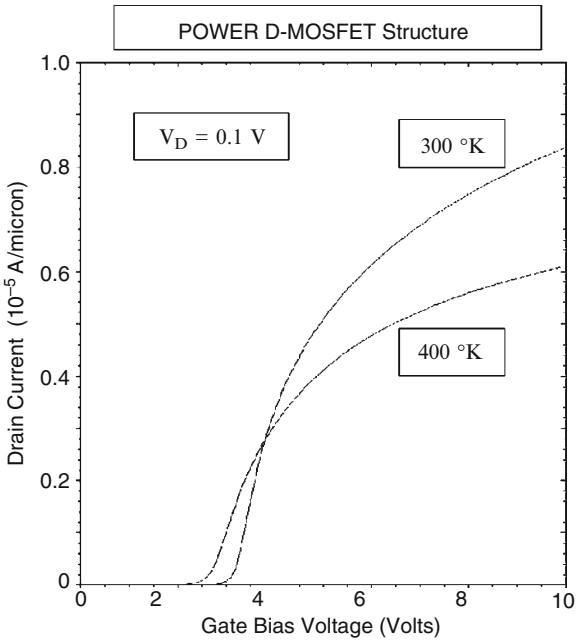

Fig. 2.10 Transfer characteristics of the D-MOSFET structure

For the case of a gate bias of 4.5 V and 300°K, the specific in-resistance is found to be 1.382 mΩ cm^2. For the case of a gate bias of 10 V and 300°K, the specific in-resistance is found to be 0.717 mΩ cm^2. These values are in close agreement with either the Model A or Model B for the current distribution within the D-MOSFET structure.

The on-state current flow pattern within the D-MOSFET structure at a small drain bias of 0.1 V and a gate bias of 4.5 V is shown in Fig. 2.11. In the figure, the depletion layer boundary is shown by the dotted lines and the junction boundary is delineated by the dashed line. The depletion layer width (W_0) in the JFET region is about 0.2 μm in good agreement with the value computed using the analytical model. It can be observed that the current flows from the channel and distributes into the JFET region via the accumulation layer. Within the JFET region, the cross-sectional area is approximately constant with a width (a/2) of 2.1 μm. From the figure, it can be seen that the current spreading from the JFET region begins at the depth of the P-base region rather than the deep P^+ region. This indicates that the Model B is more suitable than Model A for analysis of the on-resistance of the D-MOSFET structure. The current spreads from the JFET region to the drift region at a 45° angle as assumed in the models.

In order to compare the on-resistance values extracted from the numerical simulations with those predicted by the analytical models, it is necessary to extract the mobility in the inversion and accumulation layers within the simulated D-MOSFET structure. The channel and accumulation layer mobility were extracted

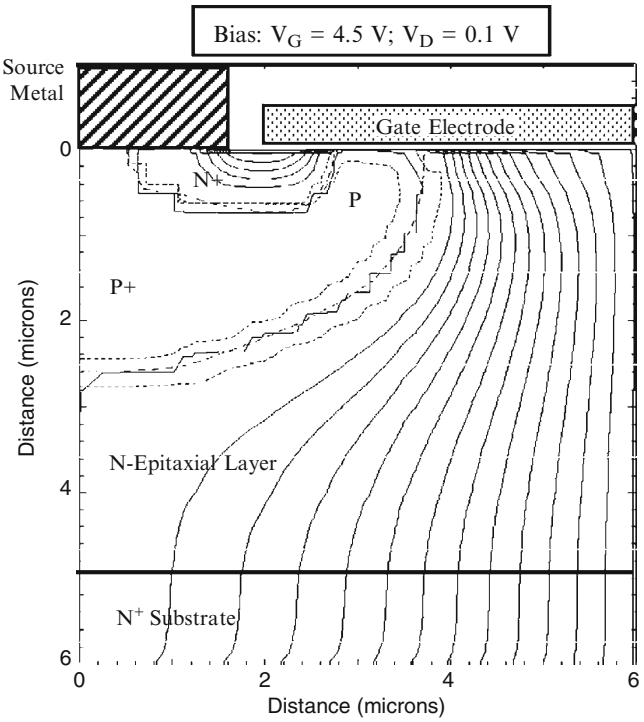

Fig. 2.11 Current distribution in the D-MOSFET structure

by simulation of a long channel lateral MOSFET structure with the same gate oxide thickness. The inversion layer mobility was found to be 450 cm^2/V s while that for the accumulation layer was found to be 1,000 cm^2/V s at a gate bias of 10 V. These values were consequently used in the analytical models when calculating the specific on-resistance.

2.3 Blocking Voltage

The power D-MOSFET structure must be designed to support a high voltage in the first quadrant when the drain bias voltage is positive. During operation in the blocking mode, the gate electrode is shorted to the source electrode by the external gate bias circuit. The application of a positive drain bias voltage produces a reverse bias across junction J_1 between the P-base region and the N-drift region, as well as across junction J_3 between the deep P^+ region and the N-drift region. Most of the applied voltage is supported across the N-drift region. The doping concentration of donors in the N-epitaxial drift region and its thickness must be chosen to attain the desired breakdown voltage. In devices designed to support low voltages (less than 50 V), the

doping concentration of the P-base region is comparable to the doping concentration of the N-drift region leading to a graded doping profile. Consequently, a significant fraction of the applied drain voltage is supported across a depletion region formed in the P-base region. The highest doping concentration in the P-base region is limited by the need to keep the threshold voltage around 2 V to achieve a low on-resistance at a gate bias of 4.5 V as discussed in the previous section.

For the allowable maximum P-base doping concentration, it is desirable to make the depth of the P-base region as small as possible to reduce the channel length in the power MOSFET structure. However, if the junction depth of the P-base region is made too small, the depletion region in the P-base region will reach through to the N^+ source region leading to a reduced breakdown voltage. In the power D-MOSFET structure, the gate region is not screened from the drain bias due to cylindrical shape of the planar junctions. This results in significant depletion of the P-base region making the channel length of this structure larger than that of the advanced power MOSFET structures discussed in this monograph.

2.3.1 Impact of Edge Termination

In practical devices, the maximum blocking voltage (BV) of the power MOSFET is invariably decided by the edge termination that surrounds the device cell structure. The most commonly used edge termination for power D-MOSFET devices is based up on floating field rings and field plates. The enhanced electric field at the edges limits the breakdown voltage to about 80% of the parallel-plane breakdown voltage (BV_{PP}):

$$BV_{PP} = \left(\frac{BV}{0.8}\right) \tag{2.14}$$

Consequently, the doping and thickness of the N-drift region must be chosen to achieve a parallel-plane breakdown voltage that is 25% larger than the blocking voltage for the device:

$$N_D = \left(\frac{4.45 \times 10^{13}}{BV_{PP}}\right)^{4/3} \tag{2.15}$$

A common design error that can occur is to make the thickness of the drift region below the P-N junction equal to the depletion width for the ideal parallel-plane junction with the above doping concentration. In actuality, the maximum depletion width is limited to that associated with the blocking voltage (BV) of the structure. The thickness of the drift region required below the P-N junction is therefore less than the depletion width for the ideal parallel-plane junction with the above doping concentration, and is given by:

$$t = W_D(BV) = \sqrt{\frac{2\varepsilon_S BV}{qN_D}} \tag{2.16}$$

The resistance of the drift region can be reduced by using this thickness rather than the maximum depletion width corresponding to the doping concentration given by (2.15).

2.3.2 *Impact of Graded Doping Profile*

For power MOSFET structures with low (less than 50 V) breakdown voltages, the doping concentration of the drift region is comparable to the doping concentration of the P-base region. This produces a graded doping profile for the junction J_1 between the P-base region and the N-drift region as illustrated in Fig. 2.12. In this figure, the concentrations of the donors and acceptors are shown by the solid lines while the dashed lines represent the net doping concentration after taking into account compensation near the junctions.

The electric field developed across junction J_1 during the blocking mode is also illustrated in Fig. 2.12. Due to the graded doping profile, the electric field extends on both sides of junction J_1. The electric field in the P-base region supports a portion of the applied positive drain voltage. This implies that the same breakdown voltage can be achieved with a larger doping concentration and a smaller thickness for the N-drift region. This improvement can be translated to increasing the breakdown

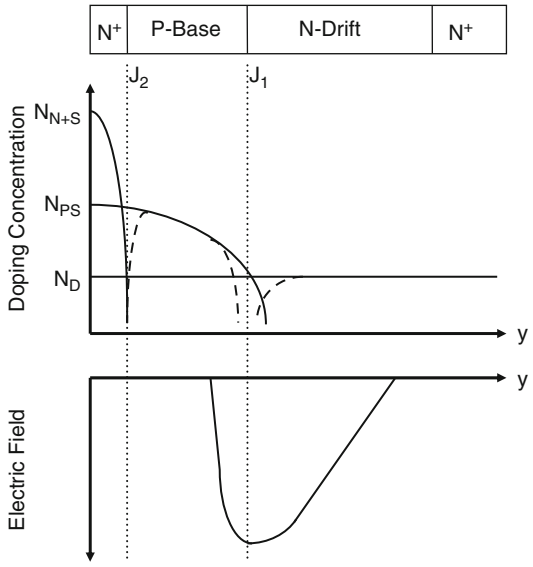

Fig. 2.12 Doping profile and electric field distribution for the power MOSFET structure

voltage at the edge termination if the P-base region is used at the edges of the power MOSFET structure. A reduction of the resistance for the power MOSFET structure can be achieved by taking into account the voltage supported within the P-base region. An improvement in the specific on-resistance of 20% can be achieved by taking into account the graded doping profile.

2.3.2.1 Simulation Results

The results of two-dimensional numerical simulations on the 30-V power D-MOSFET structure are described here to provide a more detailed understanding of the underlying device physics and operation during the blocking mode. The structure used for the numerical simulations had the same parameters as the structure described in the previous section. The blocking characteristic for the D-MOSFET cell structure is shown in Fig. 2.13 for 300°K. It can be observed that the cell is capable of supporting 42 V. This provides enough margin to achieve a device blocking voltage capability of slightly over 30 V after accounting for the reduction due to the edge termination.

It is instructive to examine the potential contours inside the power D-MOSFET structure when it is operating in the blocking mode. This allows determination of the voltage distribution within the structure and the penetration of the depletion

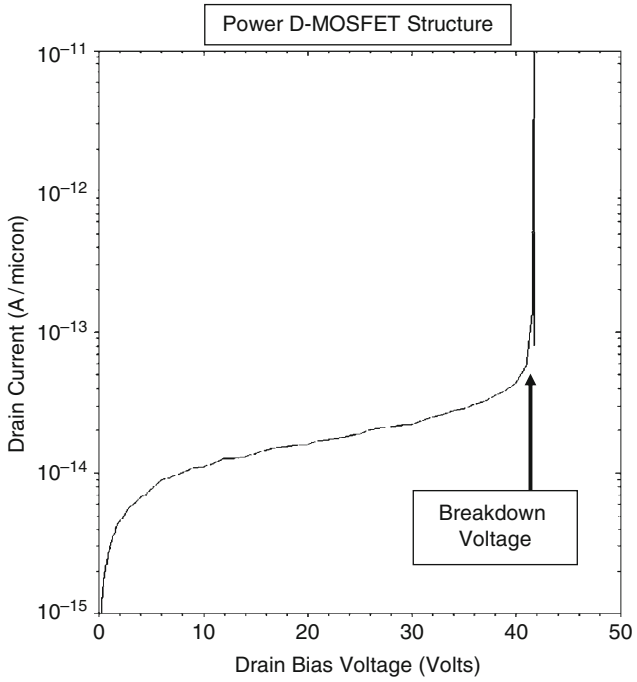

Fig. 2.13 Blocking characteristics for the D-MOSFET structure

region in the P-base region with increasing drain bias voltage. The potential contours for the D-MOSFET structure obtained using the numerical simulations with zero gate bias and various drain bias voltages are shown in Figs. 2.14–2.17. From these figures, it can be observed that the voltage distribution at the junction J_1 between the P-base region and the N-drift region is similar when proceeding from the surface towards the drain. This indicates that the surface region is not screened from the drain bias by the junctions. Consequently, the depletion region in the P-base region penetrates through a significant fraction of the P-base region when the drain bias is increased to 30 V. Any decrease in the doping concentration of the P-base region leads to reach-through breakdown limiting the ability to reduce the threshold voltage. The advanced power MOSFET structures discussed in subsequent chapters allow the screening of the semiconductor surface under the gate from the drain potential allowing the formation of shorter channel lengths to reduce the on-resistance.

It is insightful to also examine the electric field profile inside the power D-MOSFET structure when it is operating in the blocking mode. The electric field profile obtained through the junction between the deep P^+ region and the N-drift region is shown in Fig. 2.18. It can be observed that the maximum electric field occurs as expected at the junction at a depth of 2.6 μm from the surface. This figure demonstrates that a substantial portion of the voltage is supported inside the P^+ region due to its graded doping profile near the junction.

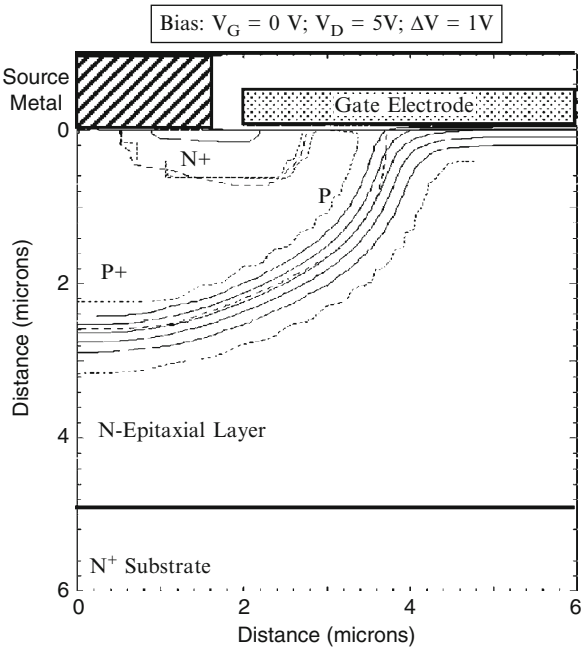

Fig. 2.14 Potential contours in the D-MOSFET structure

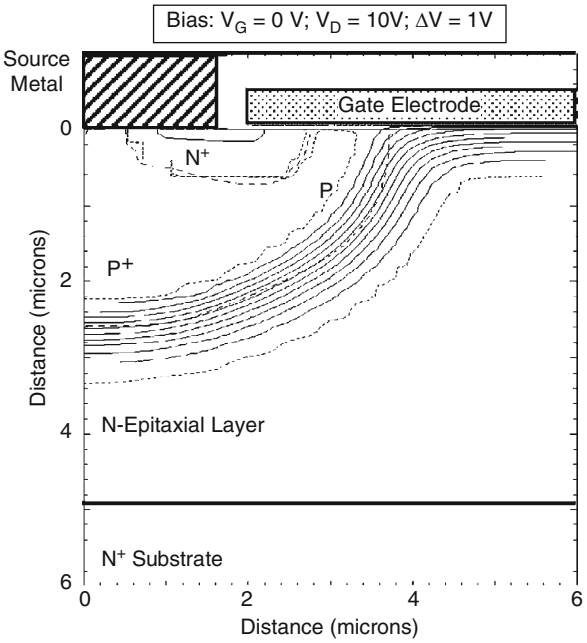

Fig. 2.15 Potential contours in the D-MOSFET structure

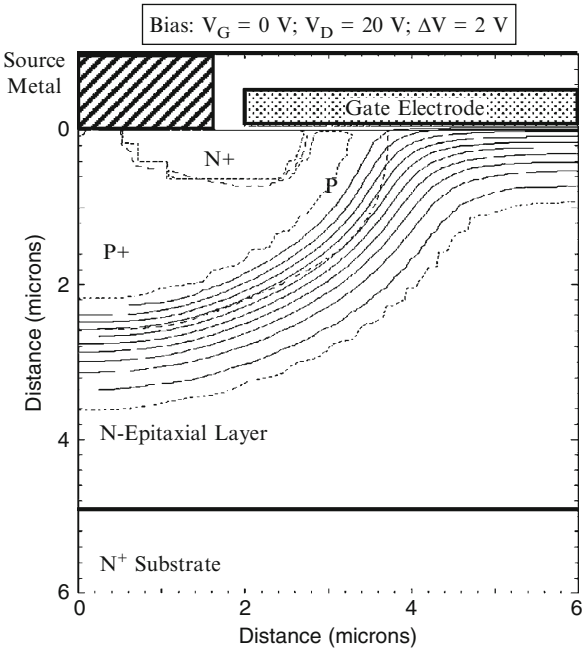

Fig. 2.16 Potential contours in the D-MOSFET structure

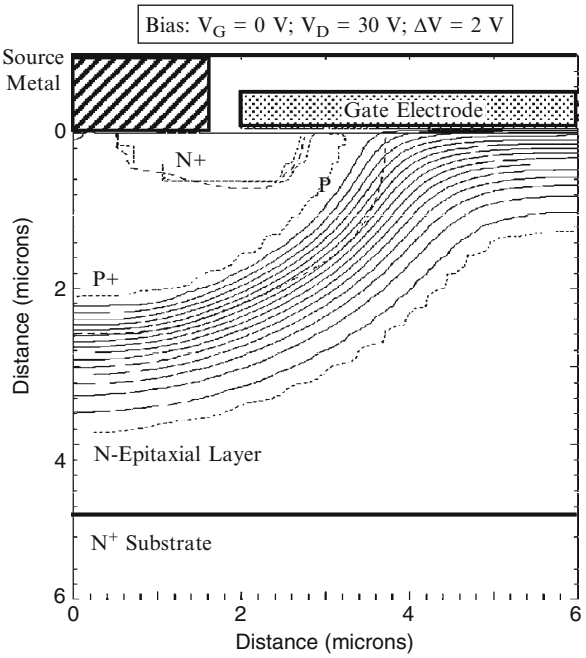

Fig. 2.17 Potential contours in the D-MOSFET structure

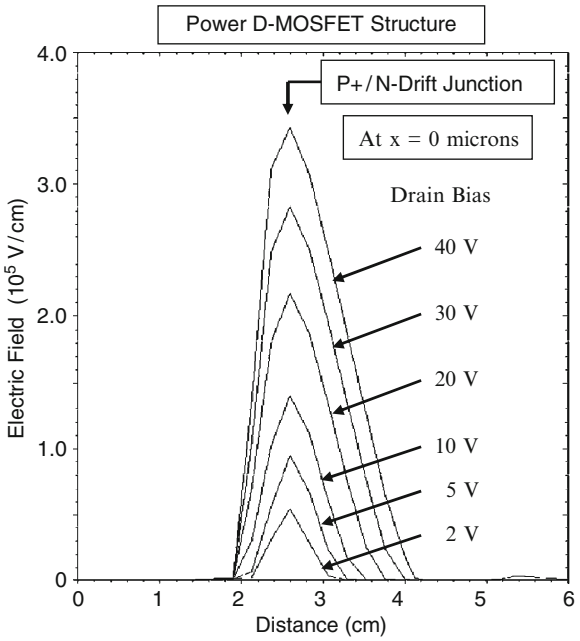

Fig. 2.18 Electric field distribution in the D-MOSFET structure

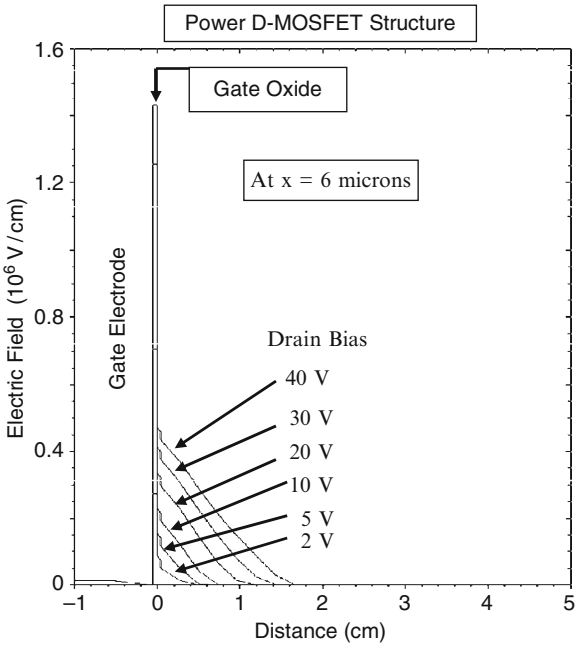

Fig. 2.19 Electric field distribution in the D-MOSFET structure

The doping concentration for the N-drift region can be increased while achieving the target blocking voltage capability due to this phenomenon. This allows reduction of the specific on-resistance for the power D-MOSFET structure.

The electric field profile taken through the middle of the gate electrode (at $\times = 6$ μm) is provided in Fig. 2.19. It can be observed that the electric field in the gate oxide is larger than in the semiconductor due to the difference in dielectric constant for the two materials. A change in the slope of the electric field profile can be observed close to the semiconductor surface due to the enhanced doping concentration arising from the JFET doping. The electric field in the oxide increases rapidly with increasing drain bias because the gate oxide is not shielded from the drain potential. The high electric field in the gate oxide in the blocking mode has been found to create reliability problems. The electric field in the gate oxide for the power D-MOSFET structure is just below the limit for reliable operation allowing stable device performance over long periods of time.

2.4 Output Characteristics

The output characteristics of the power D-MOSFET structure are important to the loci for the switching waveforms when it is operating in power circuits. The saturated drain current for the power MOSFET structure is given by:

$$I_{D,sat} = \frac{Z\mu_{ni}C_{OX}}{(L_{CH} - \Delta L_{CH})}(V_G - V_{TH})^2 \tag{2.17}$$

where ΔL_{CH} is reduction in the channel length due to depletion of the P-base region with increasing drain bias voltage. With sufficiently high doping concentration of the P-base region, the modulation of channel length can be made sufficiently small to ensure a high output resistance. The saturated drain current in the power D-MOSFET structure then increases as the square of the gate bias voltage.

2.4.1 Simulation Example

The output characteristics of the 30-V power D-MOSFET structure were obtained by using two-dimensional numerical simulations using various gate bias voltages. All the device parameters used for these numerical simulations are the same as those used in the previous sections. The output characteristics of the power D-MOSFET obtained using the simulations are shown in Fig. 2.20. The structure exhibits excellent current saturation with relatively flat output characteristics. The traces for increasing gate bias voltages are non-uniformly spaced due to the square-law behavior of the transfer characteristics.

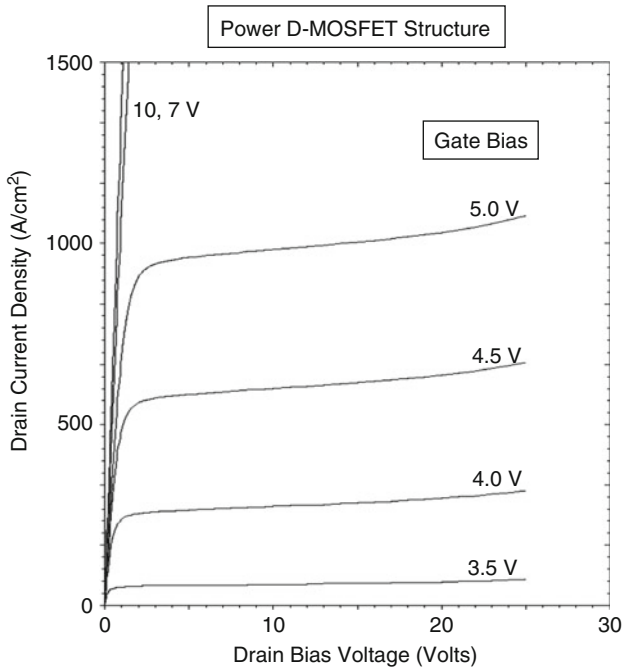

Fig. 2.20 Output characteristics for the power D-MOSFET structure

2.5 Device Capacitances

One of attractive features of all power MOSFET structures is unipolar current transport. The absence of minority carrier injection allows interruption of the current flow immediately after reduction of the gate bias below the threshold voltage. Although this implies a very fast switching speed for the power MOSFET structures, in practice the switching speed is limited by the device capacitances. The input drive signal for a power MOSFET structure is applied to the gate electrode, which is a part of a Metal-Oxide-Semiconductor sandwich. Due to the small thickness of the gate oxide and large device active area, the MOS sandwich comprises a significant capacitance. Analysis of this capacitance requires taking into account the formation of a depletion layer in the semiconductor under certain bias conditions. The rate at which the power MOSFET structure can be switched between the on- and off-states is determined by the rate at which the input capacitance can be charged or discharged. In addition, the capacitance between the drain and the gate electrodes has been found to play an important role in determining the drain current and voltage transitions during the switching event.

The capacitances within the power D-MOSFET structure have been analyzed in detail in the textbook [1]. The specific input (or gate) capacitance for the power D-MOSFET structure is given by:

$$C_{IN,SP} = C_{N+} + C_P + C_{SM} = \frac{2x_{JP}}{W_{Cell}}\left(\frac{\varepsilon_{OX}}{t_{OX}}\right) + \frac{W_G}{W_{Cell}}\left(\frac{\varepsilon_{OX}}{t_{IEOX}}\right) \tag{2.18}$$

where t_{OX} and t_{IEOX} are the thicknesses of the gate and inter-electrode oxides, respectively. For a 30-V power D-MOSFET structure with a cell pitch (W_{CELL} in Fig. 2.4) of 12 μm and gate electrode width of 8 μm, the input capacitance is found to be 22 nF/cm^2 for a gate oxide thickness of 500 Å and an inter-metal dielectric thickness of 5,000 Å.

The capacitance between the gate and drain electrodes (also called the reverse transfer capacitance) is determined by the width of the JFET region where the gate electrode overlaps the N-drift region. The MOS structure in this portion of the power D-MOSFET structure operates under deep depletion conditions when a positive voltage is applied to the drain. The gate-drain capacitance for the power D-MOSFET structure is given by:

$$C_{GD,SP} = \frac{(W_G - 2x_{PL})}{W_{Cell}}\left(\frac{C_{OX}C_{S,M}}{C_{OX} + C_{S,M}}\right) \tag{2.19}$$

where $C_{S,M}$ is the semiconductor capacitance under the gate oxide, which decreases with increasing drain bias voltage. The specific capacitance of the semiconductor depletion region can be obtained by computation of the depletion layer width.

The depletion layer width in the semiconductor under the gate oxide can be obtained using:

$$W_{D,MOS} = \frac{\varepsilon_S}{C_{OX}} \left\{ \sqrt{1 + \frac{2V_D C_{OX}^2}{q\varepsilon_S N_D}} - 1 \right\} \tag{2.20}$$

The specific capacitance for the semiconductor is then obtained using:

$$C_{S,M} = \frac{\varepsilon_S}{W_{D,MOS}} \tag{2.21}$$

The gate-drain (or reverse transfer) capacitance can be computed by using (2.19) with the above equations to determine the semiconductor capacitance as a function of the drain bias voltage.

The specific gate transfer capacitance obtained by using the above analytical formulae is shown in Fig. 2.21 for the case of a power D-MOSFET structure with 12 μm cell pitch, and polysilicon window of 8 μm. This structure has a gate oxide thickness of 500 Å and a lateral junction depth of 1.7 μm for the P-base region. The gate-drain (reverse transfer) capacitance decreases with increasing drain bias voltage due to the expansion of the depletion region in the semiconductor. At a drain bias of 20 V, the specific reverse transfer capacitance predicted by the analytical model is 3.0 nF/cm^2 for this design.

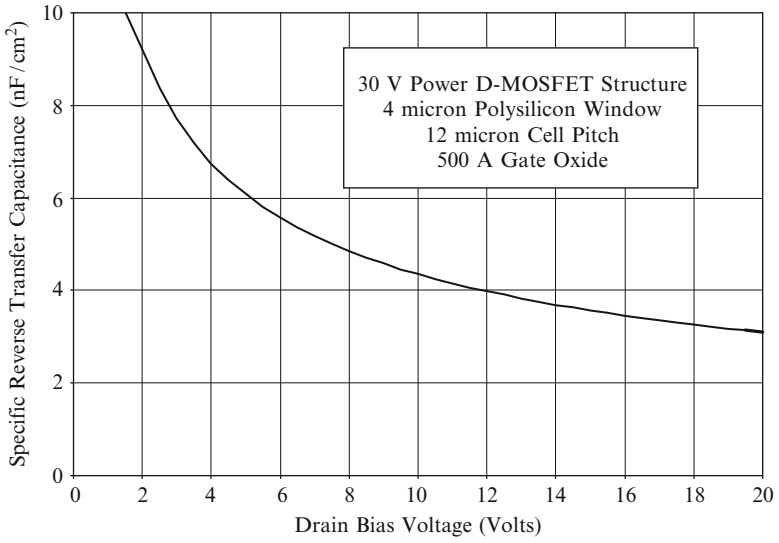

Fig. 2.21 Gate-drain capacitance for the power D-MOSFET structure

The output capacitance for the power D-MOSFET structure is associated with the capacitance of the junction between the P-base region and the N-drift region. The specific junction capacitance is given by [1]:

$$C_{S,J} = \frac{\varepsilon_S}{W_{D,J}} \tag{2.22}$$

where the depletion region thickness at the junction ($W_{D,J}$) is related to the drain bias voltage:

$$W_{D,J} = \sqrt{\frac{2\varepsilon_S(V_D + V_{bi})}{qN_D}} \tag{2.23}$$

This depletion layer width is larger than that under the gate oxide because all the applied drain voltage must be supported across the P-N junction. The specific output capacitance for the power D-MOSFET structure can then be obtained by assuming (Model A in the textbook) that the area of the junction within the cell is (W_{PW} + $2x_{PL}$)Z:

$$C_O = \left(\frac{W_{PW} + 2x_{PL}}{W_{Cell}}\right) C_{S,J} \tag{2.24}$$

where x_{PL} is the lateral extension of the P-base region under the gate electrode.

The output capacitance obtained by using the above analytical model is shown in Fig. 2.22 for the case of the 30-V power D-MOSFET structure with 12 μm cell pitch

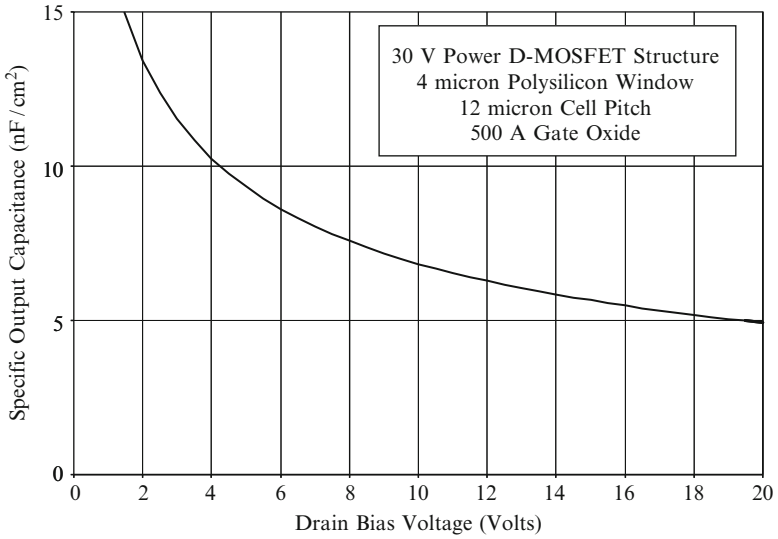

Fig. 2.22 Output capacitance for the power D-MOSFET structure

and polysilicon window of 8 μm. This structure has a gate oxide thickness of 500 Å and a lateral junction depth of 1.7 μm for the P-base region. A built-in potential of 0.8 V was assumed for the P-base/N-drift junction, and the drift region has a doping concentration of $1.6 \times 10^{16}/cm^3$. The specific output capacitance decreases with increasing drain bias voltage due to the expansion of the depletion region under the P-base region. At a drain bias of 20 V, the specific output capacitance predicted by the analytical model for this structure is 5 nF/cm^2.

2.5.1 Simulation Example

The capacitances of the 30-V power D-MOSFET structure were extracted using two-dimensional numerical simulations on the structure with device parameters described in the previous sections. The input capacitance was extracted by performing the numerical simulations with a small AC signal superposed on the DC gate bias voltage. The input capacitances obtained for the power D-MOSFET structure are shown in Fig. 2.23 at a drain bias of 20 V. The input capacitance is comprised of two components – the first is between the gate electrode and the source electrode (C_{GS}) while the second is between the gate electrode and the base electrode (C_{GB}). The total input capacitance can be obtained by the addition of these capacitances because they are in parallel and share a common contact

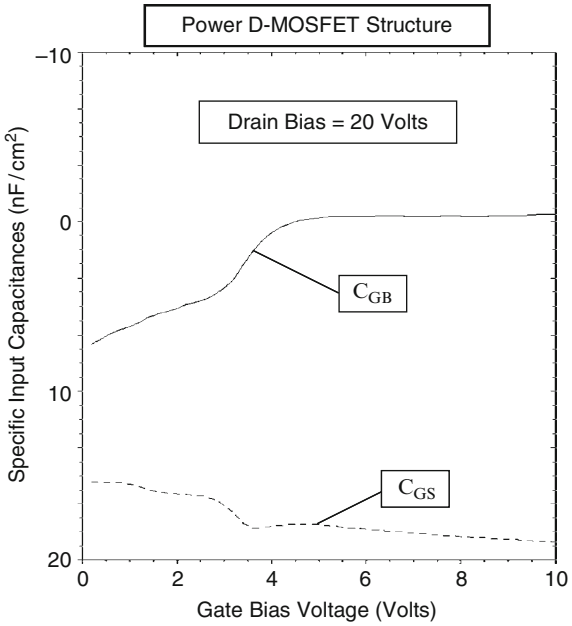

Fig. 2.23 Input capacitances for the D-MOSFET structure

electrode in the actual power D-MOSFET structure. From the figure, a total specific input capacitance of about 20 nF/cm^2 is observed which is approximately independent of the gate bias voltage. At gate bias voltages below the threshold voltage, there is significant coupling between the P-base region and the gate electrode leading to a large contribution to the input capacitance from this path. When the gate bias voltage exceeds the threshold voltage, the inversion layer screens the P-base region from the gate electrode and couples it with the N^+ source region. Consequently, the contribution from C_{GB} decreases to zero while that from C_{GS} increases as the gate bias voltage is increased. The specific input capacitance extracted from the numerical simulations is in excellent agreement with that calculated with the analytical model.

The drain-gate (reverse transfer) capacitance can be extracted by performing the numerical simulations with a small AC signal superposed on the DC drain bias voltage. The values obtained for the 30-V power D-MOSFET structure are shown in Fig. 2.24. The gate-to-drain and base-to-drain capacitances are shown in the figure for comparison. Both of these capacitances decrease with increasing drain bias voltage as expected from the analytical model. For this power D-MOSFET structure, the reverse transfer (gate-drain) capacitance is comparable in magnitude to the output (base-drain) capacitance. This implies a strong feedback path between the drain and the gate electrodes which is detrimental to the switching speed and power loss for the power D-MOSFET structure. The values for the reverse transfer and output capacitances obtained by using the analytical models are in excellent agreement with the simulation values.

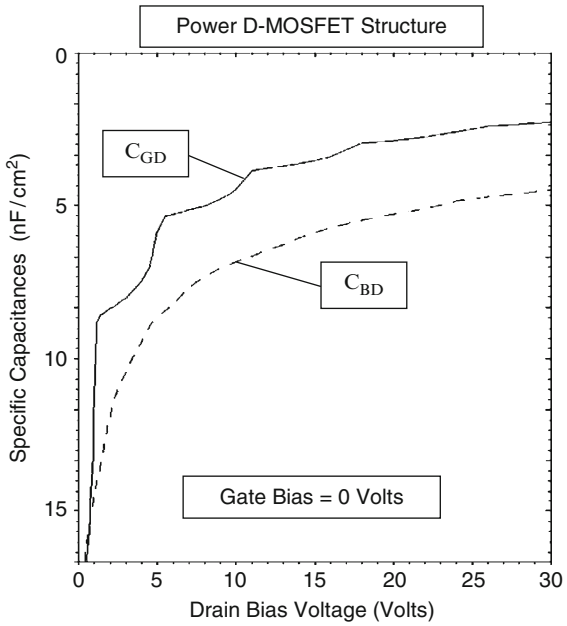

Fig. 2.24 Reverse transfer and output capacitances for the D-MOSFET structure

2.6 Gate Charge

It is standard practice in the industry to provide the gate charge for power MOSFET structures as a measure of their switching performance. The gate charge can be extracted by the application of a constant current source at the gate terminal while turning-on the power MOSFET structure from the blocking state. The linearized current and voltage waveforms observed during the turn-on process are illustrated in Fig. 6.98 in the textbook [1]. The various components for the gate charge are also defined in this figure. During the turn-on process, the gate current is used to charge the capacitances C_{GS} and C_{GD} shown in Fig. 6.97. The most significant gate charge components for assessing the performance of the power MOSFET structures are Q_{SW} (the gate switching charge), Q_{GD} (the gate-drain charge), and Q_G (the total gate charge). These components are given by [1]:

$$Q_{GD} = \frac{2K_G q\varepsilon_S N_D}{C_{OX}} \left[\sqrt{1 + \frac{2V_{DS}C_{OX}^2}{q\varepsilon_S N_D}} - \sqrt{1 + \frac{2V_{ON}C_{OX}^2}{q\varepsilon_S N_D}} \right] \tag{2.25}$$

$$Q_{SW} = [C_{GS} + C_{GD}(V_{DS})] \sqrt{\frac{J_{ON} W_{Cell} L_{CH}}{2\mu_{ni} C_{OX}}} + \frac{2K_G q\varepsilon_S N_D}{C_{OX}} \left[\sqrt{1 + \frac{2V_{DS}C_{OX}^2}{q\varepsilon_S N_D}} - \sqrt{1 + \frac{2V_{ON}C_{OX}^2}{q\varepsilon_S N_D}} \right] \tag{2.26}$$

$$Q_G = [C_{GS} + C_{GD}(V_{DS})]V_{GP} + \frac{2K_G q\varepsilon_S N_D}{C_{OX}} \left[\sqrt{1 + \frac{2V_{DS}C_{OX}^2}{q\varepsilon_S N_D}} - \sqrt{1 + \frac{2V_{ON}C_{OX}^2}{q\varepsilon_S N_D}} \right] + [C_{GS} + C_{GD}(V_{ON})](V_G - V_{GP}) \tag{2.27}$$

The gate charge values obtained for the 30-V power D-MOSFET structure by using the above equations are: $Q_{GD} = 216$ nC/cm^2; $Q_{SW} = 237$ nC/cm^2; and $Q_G = 592$ nC/cm^2. It can be concluded that the gate-drain charge (Q_{GD}) is the dominant portion (90%) of the gate switching charge (Q_{SW}).

Equations for the gate voltage, drain current, and drain voltage waveforms obtained by using the analytical model are provided in the textbook [1]. The waveforms obtained for the 30-V power D-MOSFET structure with 12 μm cell pitch and polysilicon gate width of 8 μm with a gate oxide thickness of 500 Å using these equations are provided in Fig. 2.25. A gate drive current density of 0.17 A/cm^2 was used to turn on the device from a steady-state blocking voltage of 20 V to match the results of two dimensional numerical simulations discussed below. The gate geometry factor (K_G) obtained for this structure using the structural dimensions is 0.38.

The gate voltage initially increases linearly with time. After reaching the threshold voltage, the drain current can be observed to increase in a non-linear manner

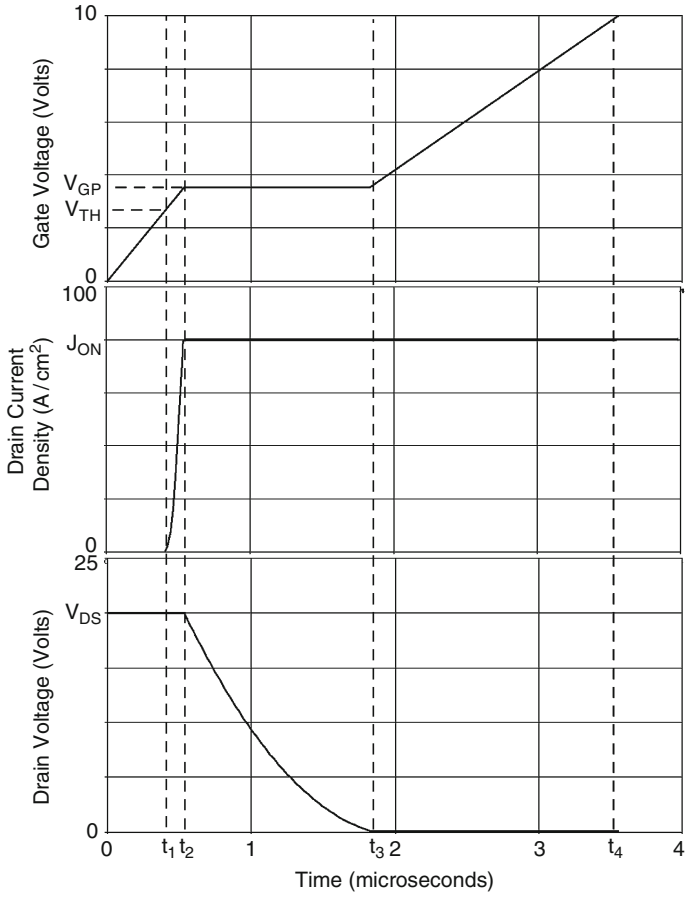

Fig. 2.25 Analytically computed waveforms for the 30-V power D-MOSFET structure

because the transconductance is a function of the gate bias voltage. The drain current density increases until it reaches an on-state current density of 80 A/cm^2. This transition occurs rapidly when compared with the time taken for the drain voltage to decrease during the next time interval. The on-state current density determines the gate plateau voltage which has a value of 3.54 V. During the gate voltage plateau phase, the drain voltage decreases in a non-linear manner until it reaches the on-state voltage drop. After this time, the gate voltage again increases but at a slower rate than during the initial turn-on phase.

2.6.1 Simulation Example

The gate charge for the 30-V power D-MOSFET structure was extracted by using the results of two-dimensional numerical simulations of the cell described in the

previous sections. The device was turned-on from blocking state with a drain bias of 20 V by driving it using a gate current of 1×10^{-8} A/μm (equivalent to 0.17 A/cm^2 for the area of 6×10^{-8} cm^2). Once the drain current density reached 80 A/cm^2, the drain current was held constant resulting in a reduction of the drain voltage. The gate plateau voltage for this drain current density was found to be 3.5 V. Once the drain voltage reached the on-state value corresponding to the gate plateau voltage, the gate voltage increased to the steady-state value of 10 V.

The gate charge waveforms obtained by using an input gate current density of 0.17 A/cm^2 when turning on the power D-MOSFET structure from a blocking state with drain bias of 20 V are shown in Fig. 2.26. The on-state current density is 80 A/cm^2 at a DC gate bias of 10 V at the end of the turn-on transient. The gate voltage increases at a constant rate at the beginning of the turn-on process as predicted by the analytical model. When the gate voltage reaches the threshold voltage, the drain current begins to increase. The drain current increases as

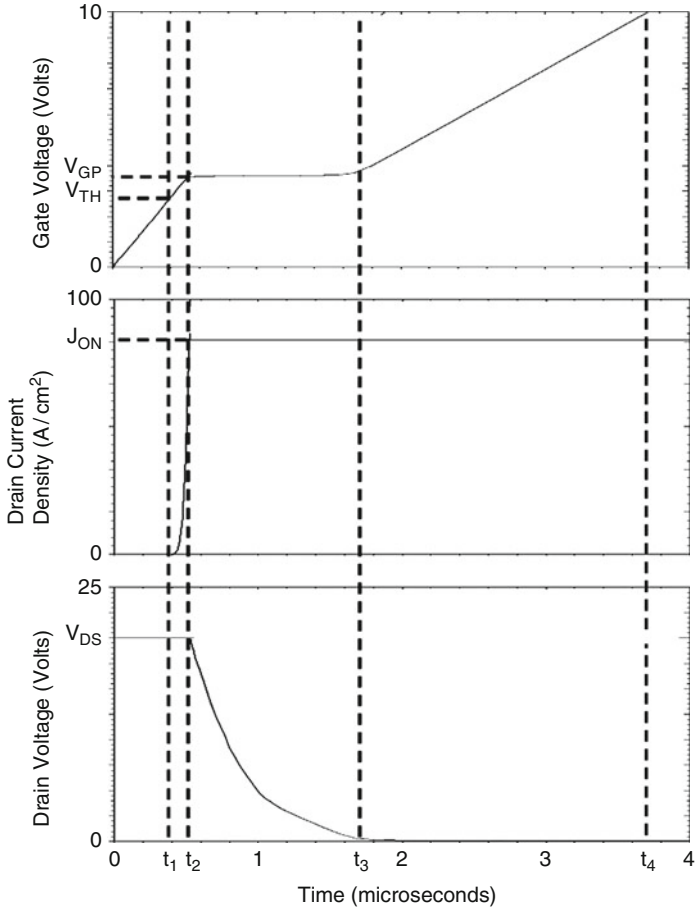

Fig. 2.26 Turn-on waveforms for the 30-V power D-MOSFET structure

Specific Gate Charge	Numerical Simulation (nC/cm^2)	Analytical Model (nC/cm^2)
Q_{GS1}	67	67.8
Q_{GS2}	20	21.1
Q_{GS}	87	88.8
Q_{GD}	200	216
Q_{SW}	220	237
Q_G	617	592

Fig. 2.27 Gate charge extracted from numerical simulations for the power D-MOSFET structure

predicted by the analytical model in a quadratic manner until it reaches the on-state current density of 80 A/cm^2.

Once the drain current reaches the on-state value, the gate voltage remains constant at the plateau voltage (V_{GP}). The plateau voltage for this structure is 3.5 V for the drain current density of 80 A/cm^2 as governed by the transconductance of the device. The drain voltage decreases during the plateau phase in a non-linear manner. After the end of the plateau phase, the gate voltage again increases until it reaches the gate supply voltage. Although the increase in gate voltage is non-linear at the beginning of this transition it becomes linear over most of the time after the plateau phase. The waveforms obtained using the analytical model (see Fig. 2.25) are very similar in shape and magnitude to those observed in the numerical simulations.

The values for the various components of the gate charge extracted from the numerical simulations are compared with those calculated by using the analytical model in Fig. 2.27. There is very good agreement between these values indicating that the analytical model is a good representation of the physics of turn-on for power D-MOSFET structure.

2.7 Device Figures of Merit

Significant power switching losses can arise from the charging and discharging of the large input capacitance in power MOSFET devices at high frequencies. The input capacitance (C_{IN}) of the power MOSFET structure must be charged to the gate supply voltage (V_{GS}) when turning on the device and then discharged to 0 V when turning off the device during each period of the operating cycle. The total power loss can be obtained by summing the on-state power dissipation for a duty cycle $\delta = t_{ON}/T$ and the switching power losses:

$$P_T = P_{ON} + P_{SW} = \delta R_{ON} I_{ON}^2 + C_{IN} V_{GS}^2 f \tag{2.28}$$

where R_{ON} is the on-resistance of the power MOSFET structure, I_{ON} is the on-state current, and f is the operating frequency. In writing this equation, the switching power losses due to the drain current and voltage transitions has been neglected. A minimum total power loss occurs for each power MOSFET structure at an optimum active area as shown in the textbook [1]. The on-state and switching power losses are equal at the optimum active area. The optimum active area at which the power dissipation is minimized is given by:

$$A_{OPT} = \sqrt{\frac{R_{ON,sp}}{C_{IN,sp}}}\left(\frac{I_{ON}}{V_{GS}}\right)\left(\sqrt{\frac{\delta}{f}}\right) \tag{2.29}$$

From the first term in this expression, a useful technology figure-of-merit can be defined:

$$FOM(A) = \frac{R_{ON,sp}}{C_{IN,sp}} \tag{2.30}$$

In the power electronics community, there is trend towards increasing the operating frequency for switch mode power supplies in order to reduce the size and weight of the magnetic components. The ability to migrate to higher operating frequencies in power conversion circuits is dependent on making enhancements to the power MOSFET technology. From the above equations, an expression for the minimum total power dissipation can be obtained [1]:

$$P_T(\min) = 2I_{ON}V_{GS}\sqrt{\delta R_{ON,sp}C_{IN,sp}f} \tag{2.31}$$

A second technology figure of merit related to the minimum power dissipation can be defined as:

$$FOM(B) = R_{ON,sp}C_{IN,sp} \tag{2.32}$$

In most applications for power MOSFET structures with high operating frequency, the switching losses associated with the drain current and voltage transitions become a dominant portion of the total power loss. The time period associated with the increase of the drain current and decrease of the drain voltage is determined by the charging of the device capacitances. It is therefore common practice in the industry to use the following figures-of-merit to compare the performance of power MOSFET products [1]:

$$FOM(C) = R_{ON,sp}Q_{GD,sp} \tag{2.33}$$

and

$$FOM(D) = R_{ON,sp}Q_{SW,sp} \tag{2.34}$$

Figures of Merit	V_G = 4.5 V	V_G = 10 V
FOM(A) ($\Omega^2cm^4s^{-1}$)	64,000	32,000
FOM(B) (ps)	30.9	15.5
FOM(C) (mΩ*nC)	303	152
FOM(D) (mΩ*nC)	333	167

Fig. 2.28 Figures of merit for the power D-MOSFET structure

Although FOM(D) encompasses both the drain current and voltage transitions, it is customary to use FOM(C) because the gate-drain charge tends to dominate in the switching gate charge. One advantage of using these expressions is that the figure-of-merit becomes independent of the active area of the power MOSFET device.

The figures of merit computed for the power D-MOSFET structure discussed in earlier sections of this chapter are provided in Fig. 2.28. The figure of merit usually used for comparison of device technologies in the literature is FOM(C). Most often, the value for this figure of merit at a gate bias of 4.5 V is utilized for selection of devices in the voltage regulator module application.

2.8 Discussion

The characteristics of the power D-MOSFET structure has been reviewed in this chapter. This structure has a relatively large specific on-resistance due to its high channel and JFET resistance contributions. Moreover, its reverse transfer charge is relatively large because of the open-junction structure below the gate region than overlaps the drift region. Since the power D-MOSFET structure was developed first from a historical perspective, it will be utilized as a bench mark for assessment of the performance of the improved device structures in subsequent chapters.

For purposes of comparison with the power MOSFET structures discussed in subsequent chapters, the analysis of the power DMOSFET structure is provided here for a broad range of blocking voltages. In this analysis, the power DMOSFET structure was assumed to have the following parameters: (a) N^+ source junction depth of 0.5 μm; (b) P-base junction depth of 1.5 μm; (c) P^+ region junction depth of 2.5 μm; (d) gate oxide thickness of 500 Å; (e) polysilicon window width of 4 μm; (f) JFET region doping concentration of $2 \times 10^{16}/cm^3$; (g) threshold voltage of 2 V; (h) gate drive voltage of 10 V; (i) inversion mobility of 450 cm^2/V s; (j) accumulation mobility of 1,000 cm^2/V s. The contributions from the contacts and the N^+ substrate were neglected during the analysis. The doping concentration and thickness of the drift region were determined under the assumption that the edge termination (in conjunction with the graded junction doping profiles) limits the breakdown voltage to 90% of the parallel-plane breakdown voltage. The device parameters pertinent to each blocking voltage are provided in Fig. 2.29. It can be

Blocking Voltage (V)	Drift Doping Concentration (cm^{-3})	Drift Region Thickness (microns)
30	1.6×10^{16}	3
60	6.0×10^{15}	5
100	3.0×10^{15}	8
200	1.2×10^{15}	17
300	6.8×10^{14}	26
600	2.7×10^{14}	58
1000	1.35×10^{14}	105

Fig. 2.29 Device parameters for the power D-MOSFET structures

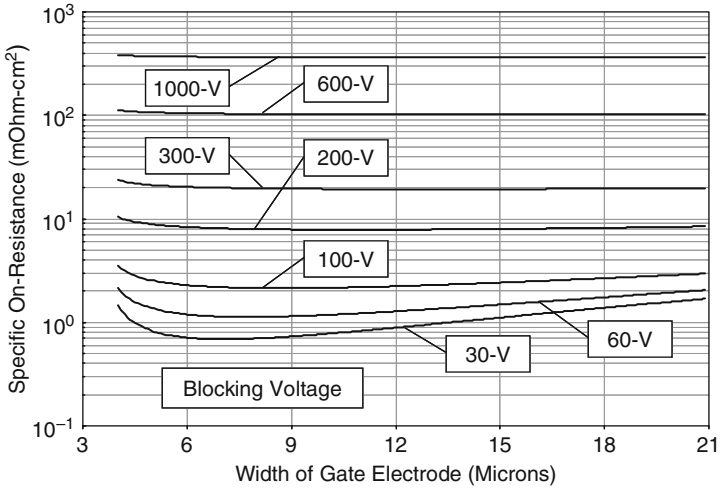

Fig. 2.30 Optimization of the specific on-resistance for the power D-MOSFET structures

observed that the doping concentration must be greatly reduced with increasing blocking voltage capability while simultaneously increasing the thickness of the drift region.

The gate electrode width was optimized for each breakdown voltage to achieve the minimum specific on-resistance in the power D-MOSFET structure. The specific on-resistance obtained by using the analytical model for the power DMOSFET structure as a function of the width of the gate electrode is shown in Fig. 2.30 for the case of various breakdown voltages. Note that a logarithmic scale has been used for the vertical axis because of the large range of values for the specific on-resistance. The single zone model (see Fig. 6.39 in the textbook) was used for the 30-V power D-MOSFET structure while the two zone model (see Fig. 6.41 in the textbook) was

Blocking Voltage (V)	Optimum Gate Width (microns)	Specific On-Resistance ($m\Omega$-cm^2)
30	7.0	0.687
60	7.7	1.13
100	8.7	2.14
200	10.8	7.85
300	12.7	19.4
600	17.0	102
1000	21.6	363

Fig. 2.31 Optimized specific on-resistance for the power D-MOSFET structures

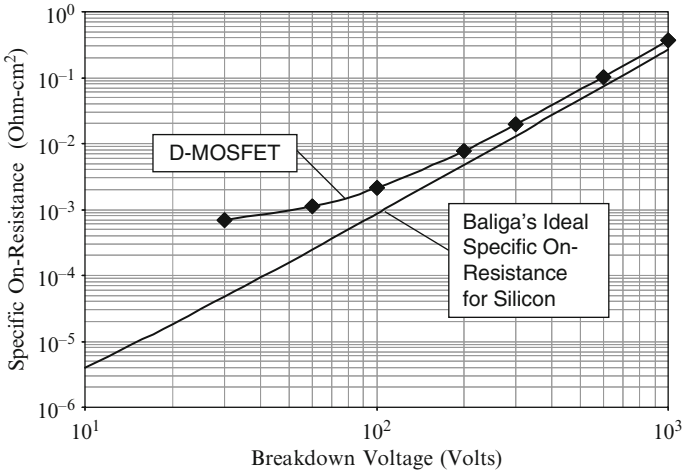

Fig. 2.32 Specific on-resistance for the power D-MOSFET structures

used for the rest of the higher voltage power D-MOSFET structures. From Fig. 2.30, it can be observed that the minimum specific on-resistance occurs at a larger optimum gate electrode width for the power D-MOSFET structures with larger blocking voltages. The optimum gate electrode width and minimum specific on-resistances for the power D-MOSFET structures are provided in Fig. 2.31. These values can be compared with the ideal specific on-resistance obtained by using Baliga's power law for the impact ionization coefficients in Fig. 2.32. From this figure, it can be concluded that the specific on-resistance for the D-MOSFET structure is always larger than the ideal specific on-resistance. For blocking voltages below 100 V, the specific on-resistance for the power D-MOSFET structure becomes substantially larger than the ideal case.

Blocking Voltage (V)	Drain Supply Voltage (Volts)	On-State Current Density (A/cm^2)	Specific Gate Transfer Charge (nC/cm^2)
30	20	1720	199
60	40	1110	203
100	67	652	211
200	133	402	223
300	200	276	226
600	400	137	230
1000	667	82.5	227

Fig. 2.33 Parameters used for gate transfer charge analysis for the power D-MOSFET structures

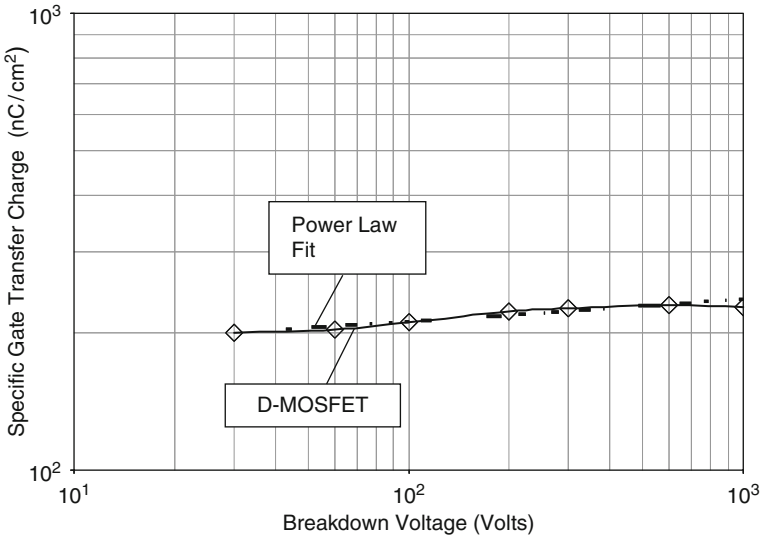

Fig. 2.34 Specific gate transfer charge for the power D-MOSFET structures

The specific gate transfer charge for the power D-MOSFET structures was obtained by using the analytical model (see 2.25). During this analysis, the devices were assumed to be operated at an on-state current density that results in a power dissipation of 100 W/cm^2 as determined by the specific on-resistance for each device. The on-state current density values are provided in Fig. 2.33. The drain supply voltage used for this analysis was chosen to be two-thirds of the breakdown voltage. The drain supply voltage values are also provided in Fig. 2.33.

The specific gate transfer charge values calculated by using the analytical model for the power D-MOSFET structure are given in Fig. 2.33 as a function of the breakdown voltage. These values are also plotted in Fig. 2.34 as a function of the

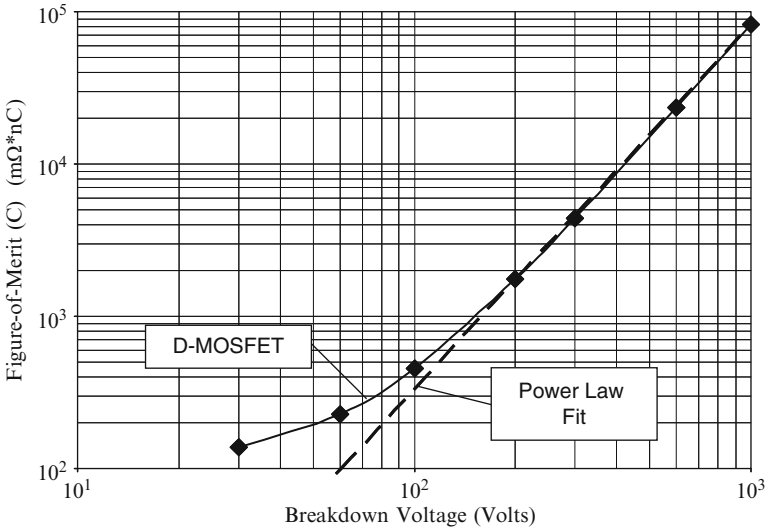

Fig. 2.35 Figure-of-merit (C) for the power D-MOSFET structures

breakdown voltage. It can be observed that the gate transfer charge increases gradually with increasing breakdown voltage. The specific gate transfer charge increases in a linear fashion on this log-log graph for breakdown voltages ranging from 120 to 1,000 V indicating a power law relationship. The power law relationship that fits the data is shown in the figure by the dashed line. The equation for this line is:

$$Q_{GD} = 2{,}350\ BV^{-0.575} \tag{2.35}$$

where the specific gate transfer charge has units of nC/cm^2.

The figure-of merit (C) – product of the specific on-resistance and the specific gate transfer charge – for the optimized power D-MODSFET structures was obtained by determining the gate transfer charge for the cell with the optimum gate width for each breakdown voltage using the analytical model (see 2.25). During this analysis, the devices were assumed to be operated at an on-state current density that results in a power dissipation of 100 W/cm^2 as determined by the specific on-resistance for each device. The resulting values for the FOM(C) are plotted in Fig. 2.35 as a function of the breakdown voltage of the power D-MOSFET structure. It can be observed that the FOM(C) increases in a linear fashion on this log-log graph for breakdown voltages above 200 V indicating a power law relationship. The power law relationship that fits the data is shown in the figure by the dashed line. The equation for this line is:

$$FOM(C) = R_{ON,sp}Q_{GD,sp} = 0.005423\ BV^{2.394} \tag{2.36}$$

where the FOM(C) has units of mΩ nC.

The values for the specific on-resistance, and FOM(C) provided here for the power D-MOSFET structure are useful as a benchmark to assess the performance of the power MOSFET structures that are discussed in subsequent chapters. Since the power D-MOSFET technology was developed in the 1970s, the manufacturing capability for these devices is mature leading to low device costs. Any advanced power MOSFET devices must provide substantial improvements in the specific on-resistance and FOM(C) in order to displace the power D-MOSFET structures in applications.

References

1. B.J. Baliga, "Fundamentals of Power Semiconductor Devices", Springer-Science, New York, 2008.
2. S.C. Sun and J.D. Plummer, "Modeling of the On-Resistance of LDMOS, VDMOS, and VMOS Power Transistors", IEEE Transactions on Electron Devices, Vol. ED-27, pp. 356–367, 1980.

Chapter 3
U-MOSFET Structure

As discussed in the previous chapter, the first power MOSFET structure commercially introduced by the power semiconductor industry was the double-diffused or D-MOSFET structure. The specific on-resistance of the D-MOSFET devices designed for low blocking voltages was found to be constrained by the significant channel resistance due to the low channel density and the JFET region contribution.

With the advent of trench technology developed for applications to the Dynamic Random Access Memories (DRAMs), the power device community developed the trench gate structure for power MOSFET devices. These devices are also called U-MOSFET structures because of the shape of the gate region. The specific on-resistance of the U-MOSFET structure is substantially smaller than that of the D-MOSFET structure because the channel density can be made larger by using a smaller cell pitch. Moreover, the U-MOSFET structure does not contain a JFET region allowing further reduction of the specific on-resistance. By the mid-1990s, most power device manufacturers were building their high performance power MOSFET devices with the trench gate architecture.

3.1 The U-MOSFET Structure

A cross-section of the basic cell structure for the U-MOSFET structure [1] is illustrated in Fig. 3.1. This device structure is fabricated by starting with an N-type epitaxial layer grown on a heavily doped N^+ substrate. The P-base region is then formed across the active area of the device by ion implantation of boron followed by a drive-in cycle. The N^+ source regions are then produced by ion implantation of phosphorus followed by its annealing process. A mask is required during the ion-implantation of the N^+ source regions to create the short between the N^+ source and P-base regions at the top of the mesa region. The trench is next formed by reactive ion etching using a mask aligned to the N^+ source mask to center it in relation to the shorts. The surface of the trench must be smooth and free of damage in order to obtain a good MOS interface with high channel inversion layer mobility.

B.J. Baliga, *Advanced Power MOSFET Concepts*,
DOI 10.1007/978-1-4419-5917-1_3, © Springer Science+Business Media, LLC 2010

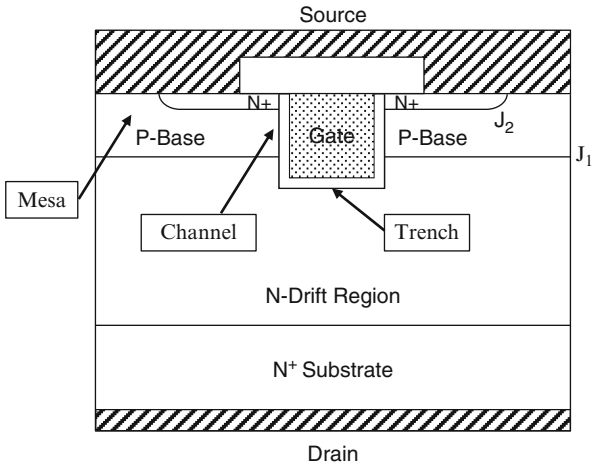

Fig. 3.1 The U-MOSFET structure

A high voltage can be supported in the U-MOSFET structure when a positive bias is applied to the drain without the application of a gate bias (i.e. with gate shorted to the source by the external drive circuit). In this case, junction J_1 formed between the P-Base region and the N-drift region becomes reverse biased. The voltage is supported mainly within the thick lightly doped N-drift region. Drain current flow in the U-MOSFET structure is induced by the application of a positive bias to the gate electrode. This produces an inversion layer at the surface of the P-base region under the gate electrode along the sidewalls of the trench. This inversion layer channel provides a path for transport of electrons from the source to the drain when a positive drain voltage is applied.

After transport from the source region through the channel, the electrons enter the N-drift region at the bottom of the trench. The accumulation layer formed at the bottom of the trench surface aids in the distribution of the carriers into the drift region. The current spreads from the bottom of the trench to the entire width of the cell cross-section. This non-uniform current distribution within the drift region enhances its resistance making the internal resistance of the U-MOSFET structure larger than the ideal specific on-resistance of the drift region.

The U-MOSFET cell pitch can be made much smaller than that for the D-MOSFET structure due to the process technology and the absence of the JFET region. The smaller cell pitch increases the channel density which reduces its contribution to the specific on-resistance. However, the electric field at the junction (J_1) between the P-base region and the N-drift region is large in the U-MOSFET structure. The large electric field at the junction promotes the extension of the depletion region into the P-base region. Consequently, the channel length in U-MOSFET devices must be made relatively large in order to suppress reach-through breakdown which increases the channel resistance.

The large electric field at the junction produces a large electric field in the gate oxide in the trenches especially at the corners in the U-MOSFET structure. This

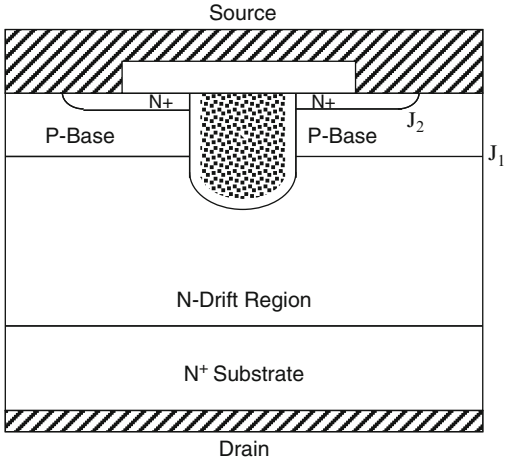

Fig. 3.2 The U-MOSFET structure with rounded trench bottom surface

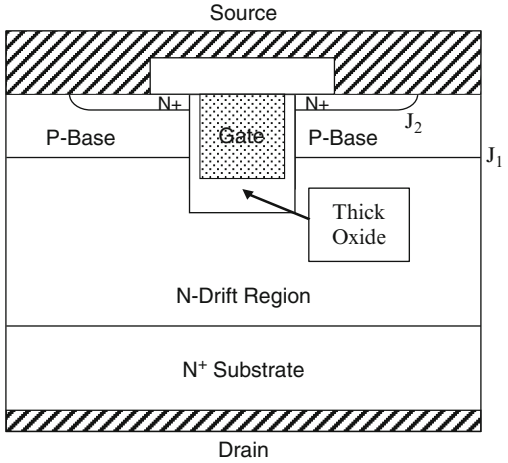

Fig. 3.3 The U-MOSFET structure with thicker oxide at the trench bottom surface

creates reliability concerns due to generation of hot-electrons. This problem has been addressed by the industry by the development of structures with rounded surfaces at the bottom of the trench [2] as illustrated in Fig. 3.2. In spite of this improvement, the electric field in the gate oxide is relatively large in the U-MOSFET structure. In addition, the reverse transfer capacitance for the power U-MOSFET structure is much greater than for the D-MOSFET structure. This capacitance can be reduced by selectively increasing the oxide thickness at the bottom of the trench surface as illustrated in Fig. 3.3 although this adds significant complexity to the device fabrication process [3–5].

3.2 Power U-MOSFET On-Resistance

The power U-MOSFET structure is shown in Fig. 3.4 with its internal resistance components [1]. The same internal resistances encountered in the power D-MOSFET structure are present in the power U-MOSFET structure with the exception of the JFET region resistance. The JFET region is eliminated within the power U-MOSFET structure because the trench extends beyond the bottom of the P-base region in order to form a channel connecting the N^+ source region with the N-drift region. The elimination of the JFET region allows a significant reduction of the overall specific on-resistance for the power U-MOSFET structure not only because its resistance is excluded but more importantly because the cell pitch can be made much smaller than that of the power D-MOSFET structure. A smaller cell pitch reduces the specific resistance contributions from the channel, accumulation and drift regions.

The total on-resistance for the power U-MOSFET structure is obtained by the addition of all the resistances because they are considered to be in series in the current path between the source and the drain electrodes:

$$R_{ON} = R_{CS} + R_{N+} + R_{CH} + R_A + R_D + R_{SUB} + R_{CD} \tag{3.1}$$

Each of the resistances within the power U-MOSFET structure is analyzed below. It is customary to utilize the linear cell surface topology for the power U-MOSFET structure because the trench surface can be oriented in the preferred direction most favorable for producing high quality etched surfaces.

A cross-section of the power U-MOSFET structure is illustrated in Fig. 3.5 with various dimensions that can be used for the analysis of the on-resistance components.

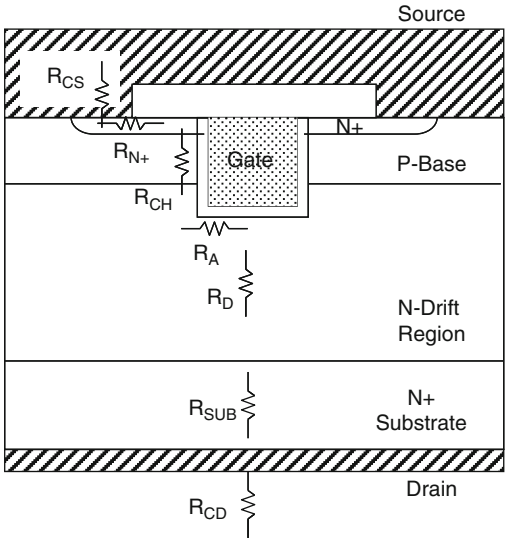

Fig. 3.4 Power U-MOSFET structure with its internal resistances

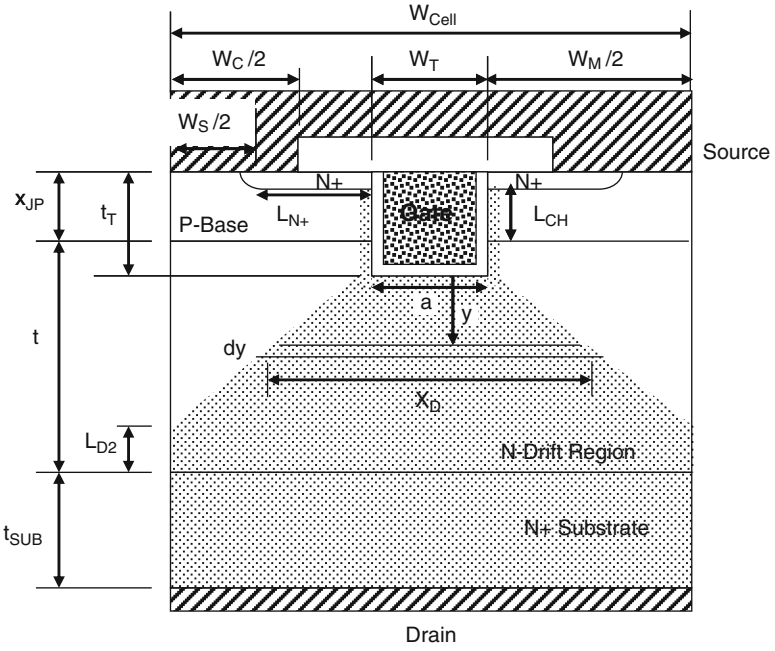

Fig. 3.5 Power U-MOSFET structure with current flow model used for analysis of its internal resistances

The edges of the masks used to define the boundary for the N^+ source ion implant and the contact window are also shown in the figure by the dimension W_S and W_C. These edges decide the area available within the structure for making contact to the N^+ source region. The position of the N^+ source definition mask also determines the length (L_{N+}) of the N^+ source region. In addition, the current flow pattern in the U-MOSFET structure is indicated by the shaded area in the figure. After entering the drift region, the current is assumed to spread from the trench bottom at a 45° angle. Since the mesa width is small, the current paths will usually overlap as illustrated in the figure. Consequently, the area for current transport varies for a portion of the drift region and then becomes uniform for the rest of the drift region.

In the textbook, it was demonstrated that the contributions from the source contact resistance (R_{CS}), the source resistance (R_{SN+}), and the drain contact resistance (R_{CD}) are very small for the U-MOSFET structure and will therefore be neglected in this chapter.

3.2.1 Channel Resistance

The power U-MOSFET structure shown in Fig. 3.5 contains channels formed on both of the vertical sidewalls of the trench gate structure. The specific on-resistance contributed by the channel in the power U-MOSFET structure is given by [1]:

$$R_{CH,SP} = \frac{L_{CH} W_{Cell}}{2\mu_{ni} C_{OX}(V_G - V_{TH})} \tag{3.2}$$

For the 30-V power U-MOSFET structure with a cell width of 3 μm, the specific resistance contributed by the channel at a gate bias of 4.5 V is 0.201 mΩ cm^2 if the channel length is 0.9 μm and the gate oxide thickness is 500 Å. For this structure, the specific resistance contributed by the channel at a gate bias of 10 V is 0.057 mΩ cm^2. These values are much smaller than the channel contributions within the power D-MOSFET structure. The reduction in the specific on-resistance contributed by the channel in the U-MOSFET structure is due to the increase in the channel density by a factor of four times.

3.2.2 Accumulation Resistance

In the power U-MOSFET structure, the current flowing through the inversion channel enters the drift region without encountering a JFET region. The current spreads from the edge of the P-base junction (J_1) along the surface of the trench due to the formation of an accumulation layer because of the positive gate bias. It is then distributed into the drift region. The specific on-resistance contributed by the accumulation layer in the power U-MOSFET structure is given by [1]:

$$R_{A,SP} = K_A \frac{L_A W_{Cell}}{2\mu_{nA} C_{OX}(V_G - V_{TH})} \tag{3.3}$$

In this equation, a coefficient K_A has been introduced to account for the current spreading from the accumulation layer into the drift region. A typical value for this coefficient is 0.6 based upon the current flow observed from numerical simulations of power U-MOSFET structures. The threshold voltage in the expression is for the on-set of formation of the accumulation layer, which will be assumed to zero in this section.

For the 30-V power U-MOSFET structure with a cell width of 3 μm, the specific resistance contributed by the accumulation layer at a gate bias of 4.5 V is 0.029 mΩ cm^2 if the P-base junction depth (x_{JP}) is 1 μm, the trench depth is 1.5 μm, and the gate oxide thickness is 500 Å. This value is an order of magnitude smaller than that for the power VD-MOSFET structure because the accumulation layer path (L_A) is only 1.0 μm in size and the cell pitch is much smaller for the U-MOSFET structure. The specific resistance contributed by the accumulation layer is reduced to 0.013 mΩ cm^2 when the gate bias is increased to 10 V.

3.2.3 Drift Region Resistance

The resistance contributed by the drift region in the power U-MOSFET structure is greater than that for the ideal drift region discussed earlier in the chapter due to

current spreading from the trench surface into the drift region. The cross-sectional area for the current flow in the drift region increases from the width 'a', which is the width of the trench for the U-MOSFET structure, as illustrated in Fig. 3.5 by the shaded area. The resistance of the drift region developed in this section is based upon the current flow pattern shown in this figure. In this pattern, it is assumed that the cross-section width (X_D) for current flow increases at a 45° angle from the bottom of the trench. It is also assumed that the width of the mesa region is sufficiently small when compared with the thickness of the drift region to allow the current flow paths to merge before the current reaches the N^+ substrate. The resistance of the drift region is now determined by two portions: a first portion with a cross-sectional area that increases with the depth and a second portion with a uniform cross-sectional area for the current flow.

The specific on-resistance contributed by the drift region in the power U-MOSFET structure is given by [1]:

$$R_{D,SP} = \frac{\rho_D W_{Cell}}{2} \ln\left[\frac{W_T + W_M}{W_T}\right] + \rho_D \left(t + x_{JP} - t_T - \frac{W_M}{2}\right) \tag{3.4}$$

For the 30-V power U-MOSFET structure constructed using a drift region with doping concentration of $1.6 \times 10^{16}/cm^3$, a trench width of 1 μm, and a cell width of 3 μm, the specific resistance contributed by the drift region calculated by using the above model is 0.106 mΩ cm^2. This is 50% smaller than the value for the 30-V power D-MOSFET structure.

3.2.4 Total On-Resistance

The total specific on-resistance for the power U-MOSFET structure can be computed by adding all the above components for the on-resistance. For the case of the 30-V power U-MOSFET design with a cell pitch (W_{Cell}) of 3 μm, trench width of 1 μm, a channel length of 0.9 μm and a threshold voltage of 2.3 V, the total specific on-resistance is found to be 0.336 and 0.176 mΩ cm^2 at gate bias of 4.5 and 10 V, respectively. The contributions from each of the components of the on-resistance are summarized in Fig. 3.6.

Resistance	V_G = 4.5 V (mΩ−cm^2)	V_G = 10 V (mΩ−cm^2)
Channel ($R_{CH, SP}$)	0.201	0.057
Accumulation ($R_{A, SP}$)	0.029	0.013
Drift ($R_{D, SP}$)	0.106	0.106
Total ($R_{T, SP}$)	0.336	0.176

Fig. 3.6 On-resistance components within the 30-V Power U-MOSFET structure

As discussed in Chap. 2, for the case of a blocking voltage of 30 V, the depletion width and doping concentration for the ideal drift region are found to be $2.2 \times 10^{16}/cm^3$ and 1.4 μm, respectively. Using the electron mobility for this doping level, the ideal specific on-resistance for this case is found to be 0.034 $m\Omega\ cm^2$. Since the device is usually constrained by the impact of an 80% reduction of breakdown voltage due to the edge termination, it is worth computing the ideal specific on-resistance for this case for comparison with the device. For the case of a blocking voltage of 37.5 V, the depletion width and doping concentration are found to be $1.6 \times 10^{16}/cm^3$ and 1.8 μm, respectively. Using the electron mobility for this doping level, the ideal specific on-resistance is found to be 0.059 $m\Omega\ cm^2$. It can be observed that the specific on-resistance for the U-MOSFET structure is only three times the ideal specific on-resistance for the blocking voltage of 37.5 V for a gate bias of 10 V. The specific on-resistance predicted by the analytical model is close to that reported for fabricated devices [2].

3.2.4.1 Simulation Results

The results of two-dimensional numerical simulations on the 30-V power U-MOSFET structure are described here to provide a more detailed understanding of the underlying device physics and operation. The structure used for the numerical simulations had a drift region thickness of 3 μm below the junction (J_1) between the P-base region and the N-drift region with a doping concentration of $1.6 \times 10^{16}/cm^3$. The P-base region and N^+ source regions had depths of 1.0 and 0.1 μm, respectively. For the numerical simulations, half the cell (with a width of 1.5 μm) shown in Fig. 3.1 was utilized as a unit cell that is representative of the structure. The gate oxide was assumed to 500 Å with a uniform thickness on the trench sidewalls and bottom surfaces. A three dimensional view of the doping distribution in the U-MOSFET structure is shown in Fig. 3.7. The short between the N^+ source and P-base region is placed in the center of the mesa region.

The channel doping profile taken vertically along the surface of the trench is shown in Fig. 3.8. The vertical extensions of the P-base and N^+ source regions are 1.0 and 0.1 μm leading to a channel length of 0.9 μm. The surface concentration for the P-base region was chosen to obtain a maximum compensated P-type doping concentration in the channel of $1.0 \times 10^{17}/cm^3$. This is sufficient to prevent reach-through breakdown while obtaining an acceptable threshold voltage for the gate oxide thickness of 500 Å.

The transfer characteristics for the U-MOSFET structure were obtained using numerical simulations with a drain bias of 0.1 V at 300 and 400°K. The resulting transfer characteristics are shown in Fig. 3.9. From this graph, a threshold voltage of 2.3 and 2.0 V can be extracted at 300 and 400°K, respectively. The threshold voltage decreases by 15% when the temperature increases as in the case of the D-MOSFET structure. The specific on-resistance can be obtained from the transfer characteristics at any gate bias voltage. For the case of a gate bias of 4.5 V and 300°K, the

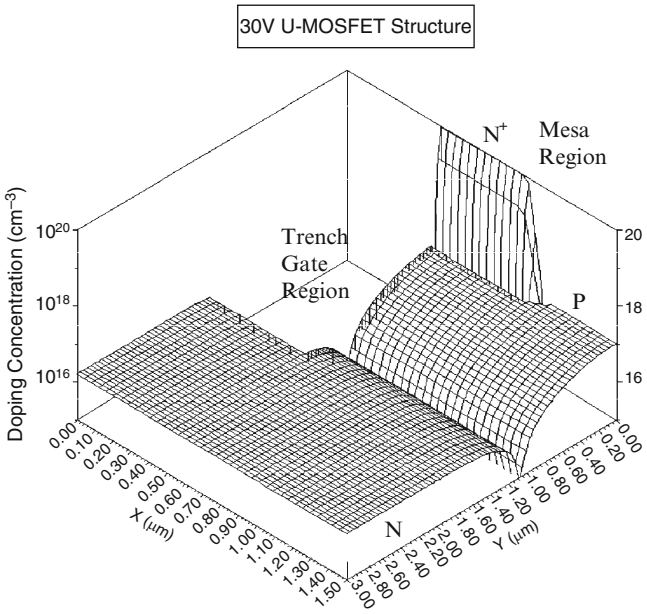

Fig. 3.7 Doping distribution for the U-MOSFET structure

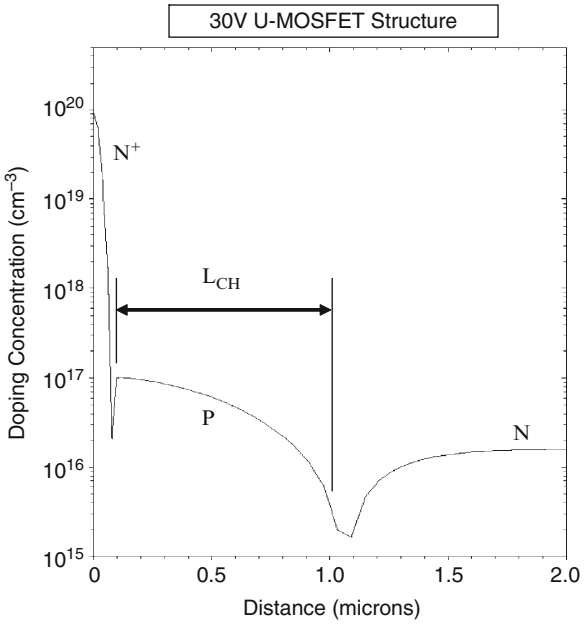

Fig. 3.8 Channel doping profile for the U-MOSFET structure

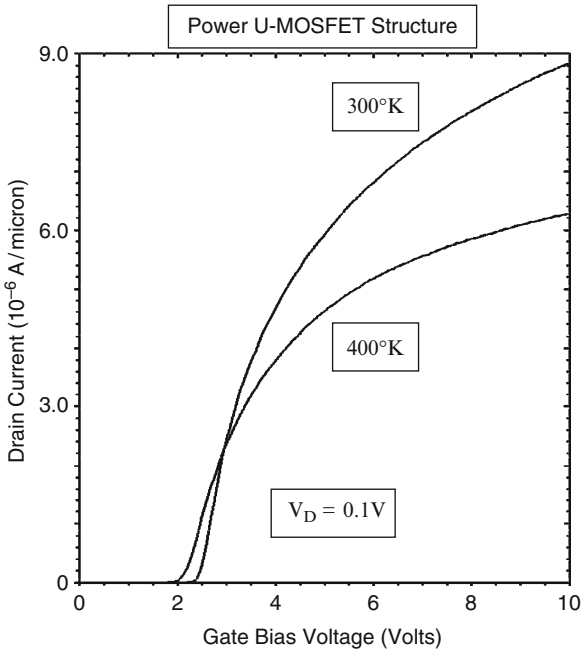

Fig. 3.9 Transfer characteristics of the U-MOSFET structure

specific in-resistance is found to be 0.280 mΩ cm^2, while for the case of a gate bias of 10 V and 300°K, the specific in-resistance is found to be 0.170 mΩ cm^2. These values are far smaller than those observed for the D-MOSFET structure. The specific on-resistance obtained using the analytical model is larger than those obtained from the numerical simulations for the gate bias of 4.5 V. This is associated with several assumption used in the analytical model. Firstly, the threshold voltage in the analytical model is assumed to be independent of the position along the channel. In the device structure used for the numerical simulations, the threshold voltage becomes smaller along the channel due to the reduced doping concentration of the P-base region near the drift region. This will reduce the channel resistance contribution for the device structure during the numerical simulations. Second, the current spreads from the channel into the drift region from the bottom of the P-base region rather than from the bottom of the trench.

The current spreading pattern in the U-MOSFET structure can be observed using the current flow-lines shown in Fig. 3.10 at a small drain bias of 0.1 V and a gate bias of 4.5 V. In the figure, the depletion layer boundary is shown by the dotted lines and the junction boundary is delineated by the dashed line. From this figure, it can be observed that the current spreading begins to occur from the junction between the P-base region and the N-drift region reducing the drift region resistance.

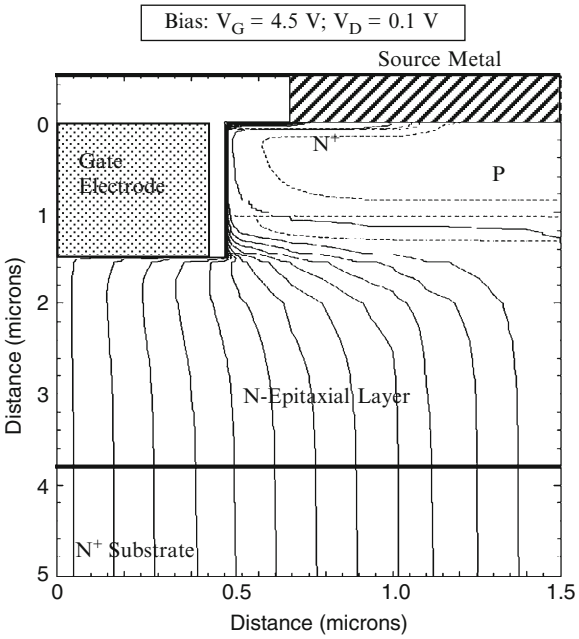

Fig. 3.10 Current distribution in the U-MOSFET structure

3.3 Blocking Voltage

The power U-MOSFET structure must be designed to support a high voltage in the first quadrant when the drain bias voltage is positive. During operation in the blocking mode, the gate electrode is shorted to the source electrode by the external gate bias circuit. The application of a positive drain bias voltage produces a reverse bias across junction J_1 between the P-base region and the N-drift region. Most of the applied voltage is supported across the N-drift region. The doping concentration of donors in the N-epitaxial drift region and its thickness are chosen to attain the desired breakdown voltage. In devices designed to support low voltages (less than 50 V), the doping concentration of the P-base region is comparable to the doping concentration of the N-drift region leading to a graded doping profile. Consequently, a significant fraction of the applied drain voltage is supported across a depletion region formed in the P-base region. The highest doping concentration in the P-base region is limited by the need to keep the threshold voltage around 2 V to achieve a low on-resistance at a gate bias of 4.5 V as discussed in the previous section.

For the allowable maximum P-base doping concentration, it is desirable to make the depth of the P-base region as small as possible to reduce the channel length in the power MOSFET structure. However, if the junction depth of the P-base region

is made too small, the depletion region in the P-base region will reach through to the N^+ source region leading to a reduced breakdown voltage. In the power U-MOSFET structure, significant depletion of the P-base region occurs making the channel length of this structure larger than that of the advanced power MOSFET structures discussed in this monograph.

3.3.1 Impact of Edge Termination

In practical devices, the maximum blocking voltage (BV) of the power MOSFET is invariably decided by the edge termination that surrounds the device cell structure. The most commonly used edge termination for power U-MOSFET devices is based up on floating field rings and field plates. The enhanced electric field at the edges limits the breakdown voltage to about 80% of the parallel-plane breakdown voltage (BV_{PP}). The doping and thickness for the N-drift region must be designed using the same approach described earlier in Sect. 2.3.1 for the D-MOSFET structure in order to minimize the resistance.

It is also important to shield the corners of the trenches at the edge termination to avoid a severe reduction in the breakdown voltage [6]. The most suitable option is to envelope the corners of the trenches at the edges with a deeper P^+ diffusion. This requires an additional process step during device fabrication.

3.3.2 Impact of Graded Doping Profile

For power MOSFET structures with low (less than 50 V) breakdown voltages, the doping concentration of the drift region is comparable to the doping concentration of the P-base region. This produces a graded doping profile for the junction J_1 between the P-base region and the N-drift region as illustrated in Fig. 2.12.

The electric field developed across junction J_1 during the blocking mode is also illustrated in Fig. 2.12. Due to the graded doping profile, the electric field extends on both sides of junction J_1. The electric field in the P-base region supports a portion of the applied positive drain voltage. This implies that the same breakdown voltage can be achieved with a larger doping concentration and a smaller thickness for the N-drift region. This improvement can be translated to increasing the breakdown voltage at the edge termination if the P-base region is used at the edges of the power MOSFET structure. A reduction of the resistance for the power MOSFET structure can be achieved by taking into account the voltage supported within the P-base region. An improvement in the specific on-resistance of 20% can be achieved by taking into account the graded doping profile.

3.3.2.1 Simulation Results

The results of two-dimensional numerical simulations on the 30 V power U-MOSFET structure are described here to provide a more detailed understanding of the underlying device physics and operation during the blocking mode. The structure used for the numerical simulations had the same parameters as the structure described in the previous section. The blocking characteristic for the U-MOSFET cell structure is shown in Fig. 3.11 for 300°K. It can be observed that the cell is capable of supporting 42 V. This provides enough margin to achieve a device blocking voltage capability of slightly over 30 V after accounting for the reduction due to the edge termination.

It is instructive to examine the potential contours inside the power U-MOSFET structure when it is operating in the blocking mode. This allows determination of the voltage distribution within the structure and the penetration of the depletion region in the P-base region with increasing drain bias voltage. The potential contours for the U-MOSFET structure obtained using the numerical simulations with zero gate bias and various drain bias voltages are shown in Fig. 3.12–3.15. From these figures, it can be observed that the depletion region in the P-base region penetrates through a significant fraction of the P-base region when the drain bias is increased to 30 V. Any decrease in the doping concentration of the P-base region leads to reach-through breakdown limiting the ability to reduce the threshold voltage.

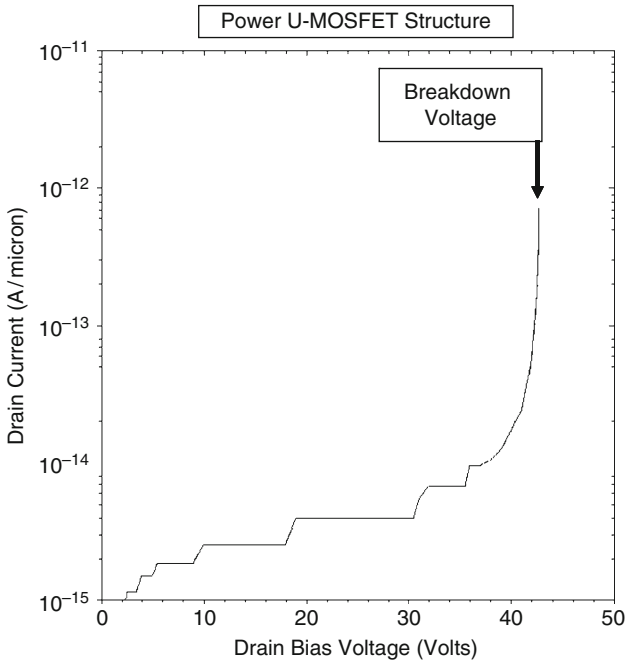

Fig. 3.11 Blocking characteristics for the D-MOSFET structure

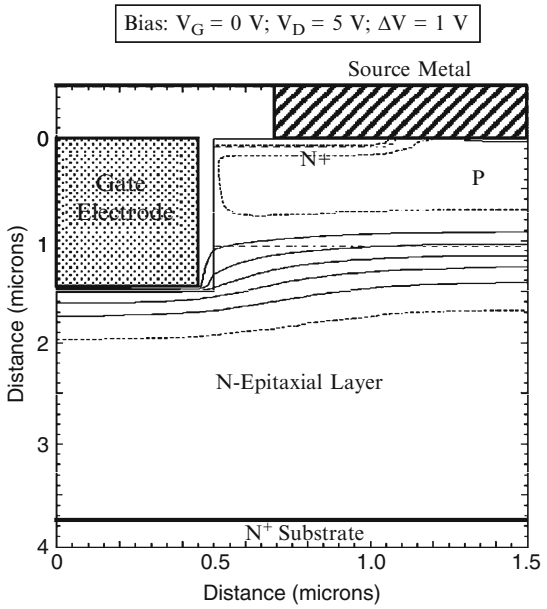

Fig. 3.12 Potential contours in the U-MOSFET structure

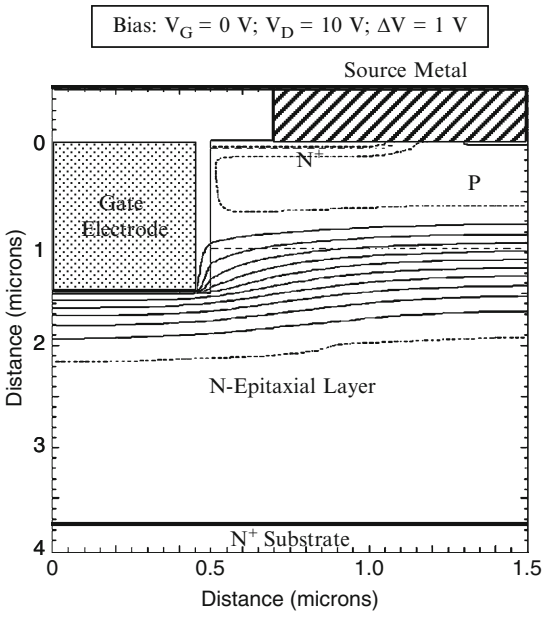

Fig. 3.13 Potential contours in the U-MOSFET structure

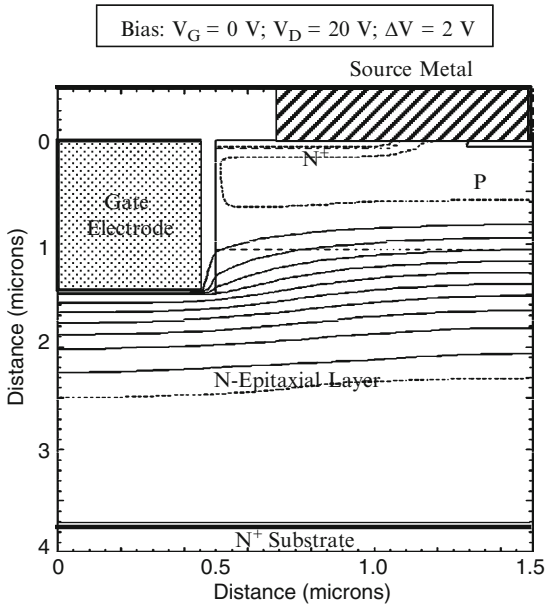

Fig. 3.14 Potential contours in the U-MOSFET structure

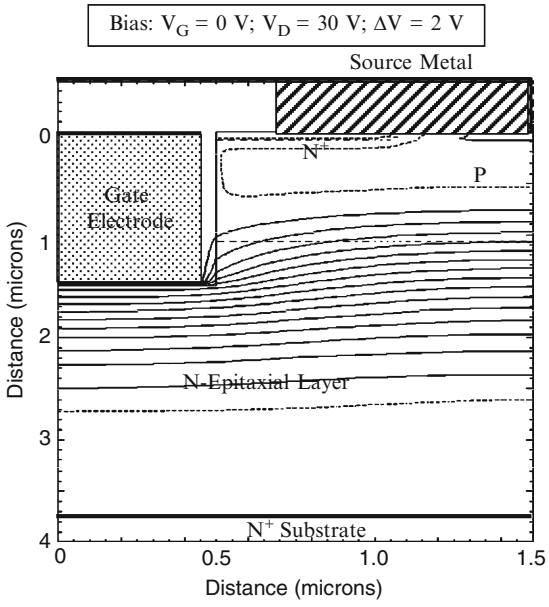

Fig. 3.15 Potential contours in the U-MOSFET structure

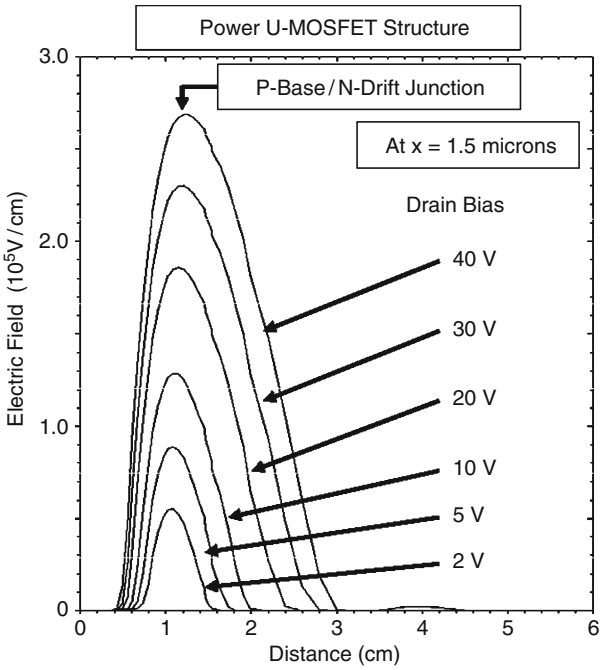

Fig. 3.16 Electric field distribution in the U-MOSFET structure

It is insightful to also examine the electric field profile inside the power U-MOSFET structure when it is operating in the blocking mode. The electric field profile obtained through the junction between the P-base region and the N-drift region is shown in Fig. 3.16. It can be observed that the maximum electric field occurs as expected at the junction at a depth of 1.0 μm from the surface. This figure demonstrates that a substantial portion of the voltage is supported inside the P-base region due to its graded doping profile near the junction. The doping concentration for the N-drift region can be increased while achieving the target blocking voltage capability due to this phenomenon. This allows reduction of the specific on-resistance for the power D-MOSFET structure.

The electric field profile taken through the middle of the gate electrode and the trench (at $\times = 0$ μm) is provided in Fig. 3.17. It can be observed that the electric field in the gate oxide is larger than in the semiconductor due to the difference in dielectric constant for the two materials. The electric field in the oxide increases rapidly with increasing drain bias because the gate oxide is not shielded from the drain potential. The electric field developed in the gate oxide at the bottom of the trench is twice as large as that observed in the D-MOSFET structure. The high electric field in the gate oxide in the blocking mode has been found to create reliability problems. The electric field in the gate oxide for this power U-MOSFET structure is above the limit for reliable operation over long periods of time.

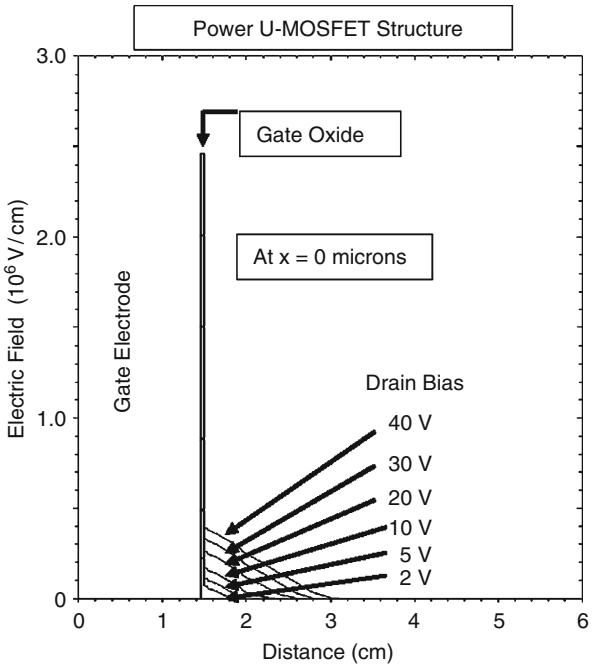

Fig. 3.17 Electric field distribution in the U-MOSFET structure

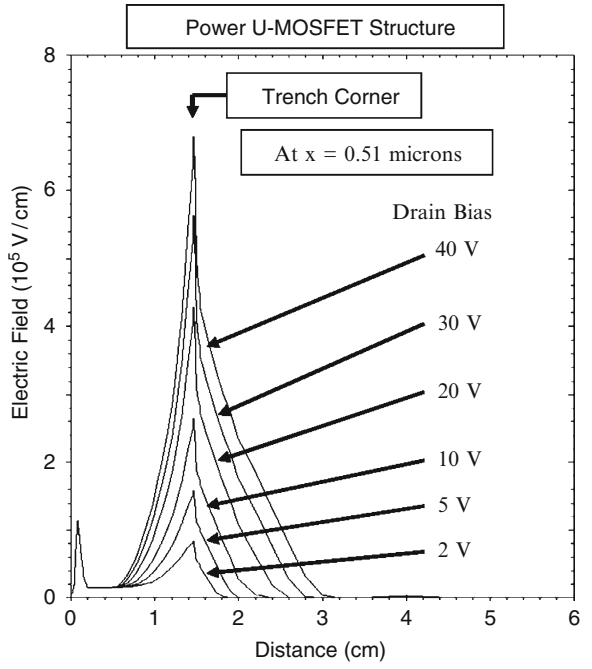

Fig. 3.18 Electric field distribution in the U-MOSFET structure

The electric field in the semiconductor and the gate oxide is enhanced by the sharp corner of the trench which extends into the drift region near the maximum electric field generated at the junction between the P-base region and the N-drift region. This can be observed in the electric field profiles taken along the vertical direction along the surface of the trench in the U-MOSFET structure. These electric field profiles are shown in Fig. 3.18 at various drain bias voltages. It can be observed that the electric field at the corner of the trench, located at 1.5 μm from the upper surface of the device, is greatly (more than two times) enhanced by the sharp corner of the trench. The high electric field produces hot-electrons in the vicinity of the channel which creates a shift in the threshold voltage during long term operation of the device.

3.4 Output Characteristics

The output characteristics of the power U-MOSFET structure are important to the loci for the switching waveforms when it is operating in power circuits. In the power MOSFET structure, the saturated drain current is given by:

$$I_{D,sat} = \frac{Z\mu_{ni}C_{OX}}{(L_{CH} - \Delta L_{CH})}(V_G - V_{TH})^2 \tag{3.5}$$

where ΔL_{CH} is reduction in the channel length due to depletion of the P-base region with increasing drain bias voltage. With sufficiently high doping concentration of the P-base region, the modulation of channel length can be made sufficiently small to ensure a high output resistance. The saturated drain current in the power U-MOSFET structure then increases as the square of the gate bias voltage.

3.4.1 Simulation Example

The output characteristics of the 30-V power U-MOSFET structure were obtained by using two-dimensional numerical simulations using various gate bias voltages. All the device parameters used for these numerical simulations are the same as those used in the previous sections. The output characteristics of the power U-MOSFET obtained using the simulations are shown in Fig. 3.19. The structure exhibits excellent current saturation with relatively flat output characteristics. At any gate bias voltage, the saturated drain current density for the U-MOSFET structure is much greater than that for the D-MOSFET structure due to the larger transconductance originating from a much greater channel density. The traces for increasing gate bias voltages are non-uniformly spaced due to the square-law behavior of the transfer characteristics.

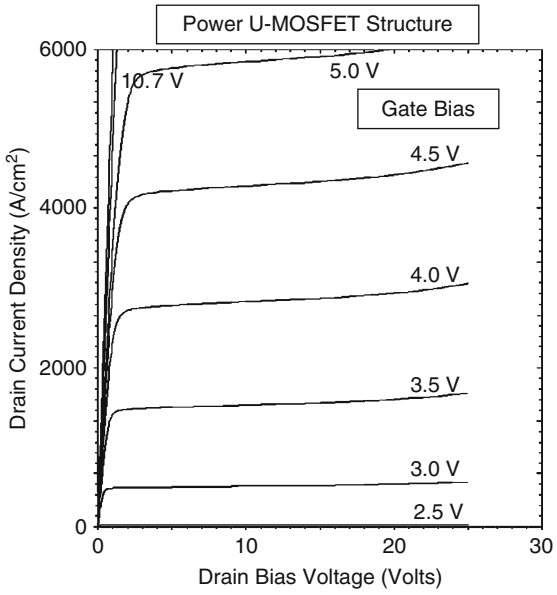

Fig. 3.19 Output characteristics for the power U-MOSFET structure

3.5 Device Capacitances

As discussed in the previous chapter for the D-MOSFET structure, the rate at which the power MOSFET structure can be switched between the on- and off-states is determined by the rate at which its input capacitance can be charged or discharged. In addition, the capacitance between the drain and the gate electrodes has been found to play an important role in determining the drain current and voltage transitions during the switching event.

The capacitances within the power U-MOSFET structure have been analyzed in detail in the textbook [1]. The specific input (or gate) capacitance for the power U-MOSFET structure is given by:

$$C_{IN,SP} = C_{N+} + C_P + C_{SM} = \frac{2x_{JP}}{W_{Cell}}\left(\frac{\varepsilon_{OX}}{t_{OX}}\right) + \frac{W_T}{W_{Cell}}\left(\frac{\varepsilon_{OX}}{t_{IEOX}}\right) \tag{3.6}$$

where t_{OX} and t_{IEOX} are the thicknesses of the gate and inter-electrode oxides, respectively. For a 30-V power U-MOSFET structure with a cell pitch (W_{CELL} in Fig. 3.5) of 3 μm and P-base junction depth width of 1.0 μm, the input capacitance is found to be 47 nF/cm^2 for a gate oxide thickness of 500 Å and an inter-metal dielectric thickness of 5,000 Å.

The capacitance between the gate and drain electrodes (also called the reverse transfer capacitance) is determined by the width of the trench where the gate electrode overlaps the N-drift region. The MOS structure in this portion of the

power U-MOSFET structure operates under deep depletion conditions when a positive voltage is applied to the drain. The gate-drain capacitance for the power U-MOSFET structure is given by [1]:

$$C_{GD,SP} = \left[\frac{W_T + 2(t_T - x_{JP})}{W_{Cell}}\right]\left(\frac{C_{OX}C_{S,M}}{C_{OX} + C_{S,M}}\right) \tag{3.7}$$

where $C_{S,M}$ is the semiconductor capacitance under the gate oxide, which decreases with increasing drain bias voltage. The specific capacitance of the semiconductor depletion region can be obtained by computation of the depletion layer width. The depletion layer width in the semiconductor under the gate oxide can be obtained using:

$$W_{D,MOS} = \frac{\varepsilon_S}{C_{OX}}\left\{\sqrt{1 + \frac{2V_D C_{OX}^2}{q\varepsilon_S N_D}} - 1\right\} \tag{3.8}$$

The specific capacitance for the semiconductor is then obtained using:

$$C_{S,M} = \frac{\varepsilon_S}{W_{D,MOS}} \tag{3.9}$$

The gate-drain (or reverse transfer) capacitance can be computed by using (3.7) with the above equations to determine the semiconductor capacitance as a function of the drain bias voltage.

The specific gate transfer capacitance obtained by using the above analytical formulae is shown in Fig. 3.20 for the case of a power U-MOSFET structure with 3 μm cell pitch, and trench width of 1 μm. This structure has a gate oxide thickness

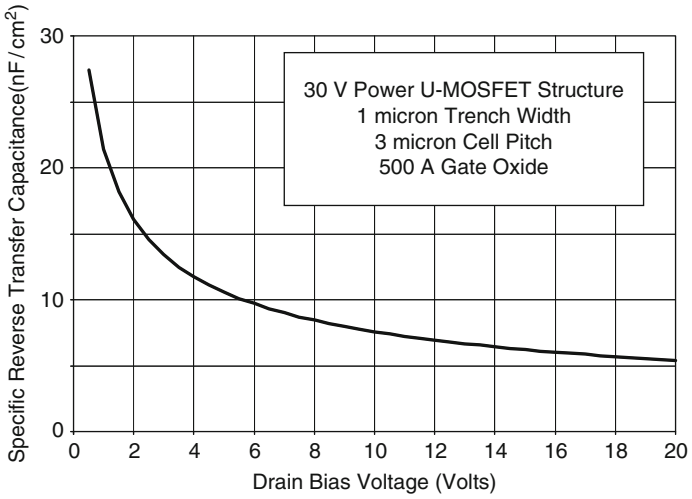

Fig. 3.20 Gate-drain capacitance for the power U-MOSFET structure

of 500 Å, a trench depth of 1.5 μm and P-base junction depth of 1.0 μm. The gate-drain (reverse transfer) capacitance decreases with increasing drain bias voltage due to the expansion of the depletion region in the semiconductor. At a drain bias of 20 V, the specific reverse transfer capacitance predicted by the analytical model is 5.4 nF/cm^2 for this design.

The output capacitance for the power U-MOSFET structure is associated with the capacitance of the junction between the P-base region and the N-drift region. The specific junction capacitance is given by [1]:

$$C_{S,J} = \frac{\varepsilon_S}{W_{D,J}} \tag{3.10}$$

where the depletion region thickness at the junction ($W_{D,J}$) is related to the drain bias voltage:

$$W_{D,J} = \sqrt{\frac{2\varepsilon_S(V_D + V_{bi})}{qN_D}} \tag{3.11}$$

This depletion layer width is larger than that under the gate oxide because all the applied drain voltage must be supported across the P-N junction. The specific output capacitance for the power U-MOSFET structure can then be obtained by using [1]:

$$C_O = \left[\frac{W_M - 2K_S(t_T - x_{JP} - t_{OX})}{W_{Cell}}\right] C_{S,J} \tag{3.12}$$

where x_{JP} is the junction depth of the P-base region.

The output capacitance obtained by using the above analytical model is shown in Fig. 3.21 for the case of the 30-V power U-MOSFET structure with 3 μm cell pitch and

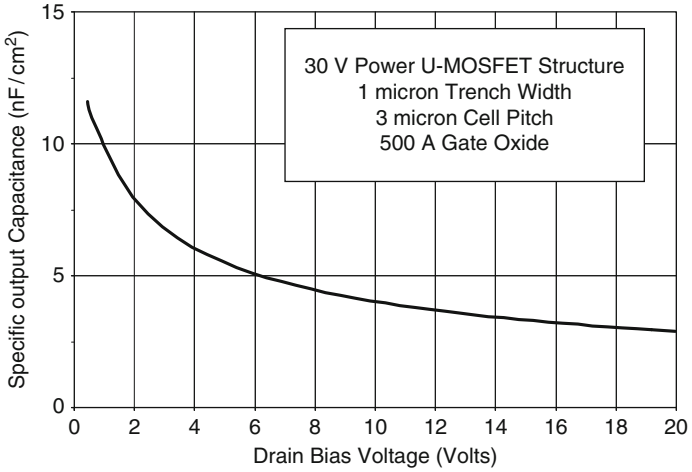

Fig. 3.21 Output capacitance for the power U-MOSFET structure

trench width of 1 μm. This structure has a gate oxide thickness of 500 Å and a junction depth of 1.0 μm for the P-base region. A built-in potential of 0.8 V was assumed for the P-base/N-drift junction, and the drift region has a doping concentration of $1.6 \times 10^{16}/cm^3$. The screening factor (K_S) was assumed to be 1. The specific output capacitance decreases with increasing drain bias voltage due to the expansion of the depletion region under the P-base region. At a drain bias of 20 V, the specific output capacitance predicted by the analytical model for this structure is 3 nF/cm^2.

3.5.1 Simulation Example

The capacitances of the 30-V power U-MOSFET structure were extracted using two-dimensional numerical simulations on the structure with device parameters described in the previous sections. The input capacitance was extracted by performing the numerical simulations with a small AC signal superposed on the DC gate bias voltage. The input capacitances obtained for the power U-MOSFET structure are shown in Fig. 3.22 at a drain bias of 0 V. The input capacitance is comprised of two components – the first is between the gate electrode and the source electrode (C_{GS}) while the second is between the gate electrode and the base electrode (C_{GB}). The total input capacitance can be obtained by the addition of

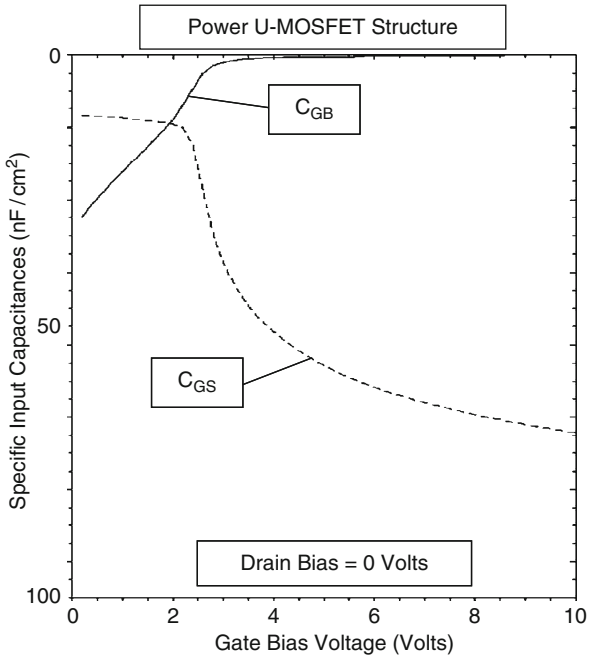

Fig. 3.22 Input capacitances for the U-MOSFET structure

these capacitances because they are in parallel and share a common contact electrode in the actual power U-MOSFET structure. From the figure, a total specific input capacitance of about 60 nF/cm^2 is observed which is approximately independent of the gate bias voltage. At gate bias voltages below the threshold voltage, there is significant coupling between the P-base region and the gate electrode leading to a large contribution to the input capacitance from this path. When the gate bias voltage exceeds the threshold voltage, the inversion layer screens the P-base region from the gate electrode and couples it with the N^+ source region. Consequently, the contribution from C_{GB} decreases to zero while that from C_{GS} increases as the gate bias voltage is increased. The specific input capacitance extracted from the numerical simulations is in excellent agreement with that calculated with the analytical model.

The drain-gate (reverse transfer) capacitance can be extracted by performing the numerical simulations with a small AC signal superposed on the DC drain bias voltage. The values obtained for the 30-V power U-MOSFET structure are shown in Fig. 3.23. The gate-to-drain and base-to-drain capacitances are shown in the figure for comparison. Both of these capacitances decrease with increasing drain bias voltage as expected from the analytical model. For this power U-MOSFET structure, the reverse transfer (gate-drain) capacitance is larger in magnitude than the output (base-drain) capacitance and much larger than that for the D-MOSFET

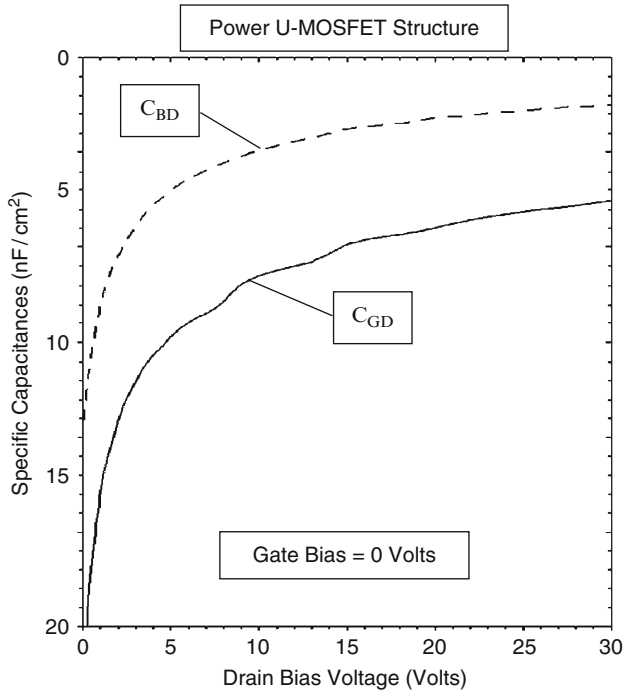

Fig. 3.23 Reverse transfer and output capacitances for the U-MOSFET structure

structure. This implies a strong feedback path between the drain and the gate electrodes which is detrimental to the switching speed and power loss for the power U-MOSFET structure. The values for the reverse transfer and output capacitances obtained by using the analytical models are in good agreement with the simulation values.

3.6 Gate Charge

As mentioned in the previous chapter, it is standard practice in the industry to provide the gate charge for power MOSFET structures as a measure of their switching performance. The gate charge can be extracted by the application of a constant current source at the gate terminal while turning-on the power MOSFET structure from the blocking state. The most significant gate charge components for assessing the performance of the power MOSFET structures are Q_{SW} (the gate switching charge), Q_{GD} (the gate-drain charge), and Q_G (the total gate charge). These components are given by [1]:

$$Q_{GD} = \frac{2K_G q\varepsilon_S N_D}{C_{OX}}\left[\sqrt{1+\frac{2V_{DS}C_{OX}^2}{q\varepsilon_S N_D}} - \sqrt{1+\frac{2V_{ON}C_{OX}^2}{q\varepsilon_S N_D}}\right] \tag{3.13}$$

$$\begin{aligned} Q_{SW} = {} & [C_{GS} + C_{GD}(V_{DS})]\sqrt{\frac{J_{ON}W_{Cell}L_{CH}}{2\,\mu_{ni}C_{OX}}} \\ & + \frac{2K_G q\varepsilon_S N_D}{C_{OX}}\left[\sqrt{1+\frac{2V_{DS}C_{OX}^2}{q\varepsilon_S N_D}} - \sqrt{1+\frac{2V_{ON}C_{OX}^2}{q\varepsilon_S N_D}}\right] \end{aligned} \tag{3.14}$$

$$\begin{aligned} Q_G = {} & [C_{GS} + C_{GD}(V_{DS})]V_{GP} \\ & + \frac{2K_G q\varepsilon_S N_D}{C_{OX}}\left[\sqrt{1+\frac{2V_{DS}C_{OX}^2}{q\varepsilon_S N_D}} - \sqrt{1+\frac{2V_{ON}C_{OX}^2}{q\varepsilon_S N_D}}\right] \\ & + [C_{GS} + C_{GD}(V_{ON})](V_G - V_{GP}) \end{aligned} \tag{3.15}$$

In these equations, the parameter K_G is given by [1]:

$$K_G = \left[\frac{W_T + 2(t_T - x_P - t_{OX})}{W_{Cell}}\right] \tag{3.16}$$

where t_{OX} is the gate oxide thickness. The gate geometry factor (K_G) obtained for this structure using the structural dimensions is 0.63.

The gate charge values obtained for the 30-V power U-MOSFET structure by using the above equations are: $Q_{GD} = 361$ nC/cm^2; $Q_{SW} = 376$ nC/cm^2; and $Q_G = 1{,}159$ nC/cm^2. It can be concluded that the gate-drain charge (Q_{GD}) is the dominant portion (90%) of the gate switching charge (Q_{SW}). The gate charge values for the power U-MOSFET structure are twice the values for the power D-MOSFET structure (see Chap. 2). Consequently, the improvement in the specific on-resistance achieved with the power U-MOSFET structure is offset by the much greater specific gate charge.

Equations for the gate voltage, drain current, and drain voltage waveforms obtained by using the analytical model are provided in the textbook [1]. The waveforms obtained for the 30-V power U-MOSFET structure with 3 μm cell pitch and trench width of 1 μm with a gate oxide thickness of 500 Å using these equations are provided in Fig. 3.24. A gate drive current density of 0.67 A/cm^2 was

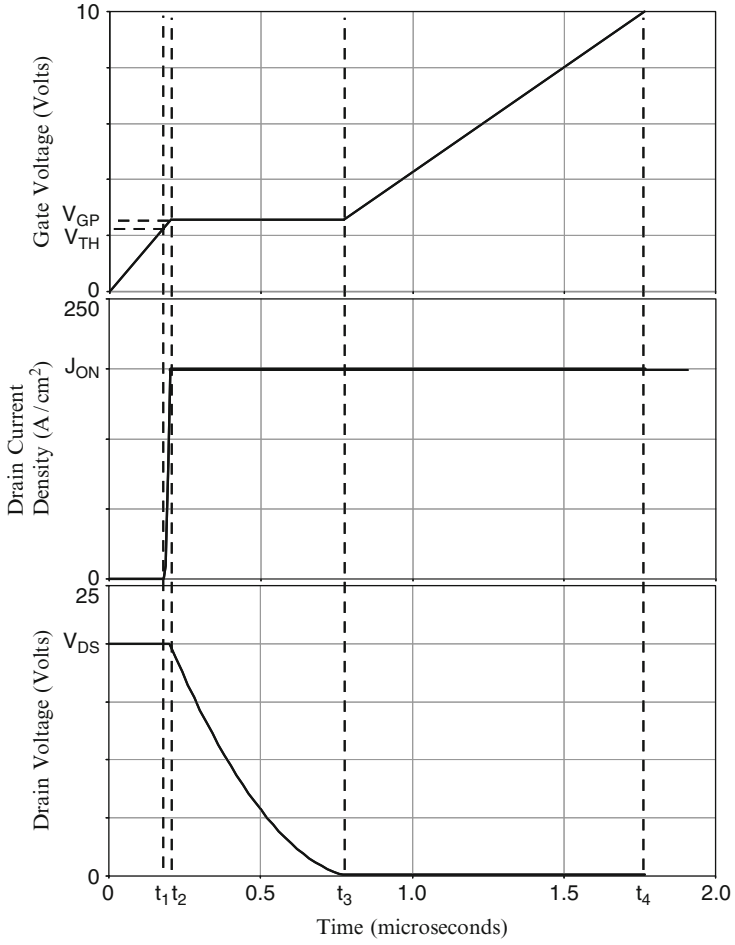

Fig. 3.24 Analytically computed waveforms for the 30-V power U-MOSFET structure

used to turn on the device from a steady-state blocking voltage of 20 V to match the results of two dimensional numerical simulations.

The gate voltage initially increases linearly with time. After reaching the threshold voltage, the drain current can be observed to increase in a non-linear manner because the transconductance is a function of the gate bias voltage until it reaches an on-state current density of 150 A/cm^2. This transition occurs rapidly when compared with the time taken for the drain voltage to decrease during the next time interval. The on-state current density determines the gate plateau voltage which has a value of 2.56 V. During the gate voltage plateau phase, the drain voltage decreases in a non-linear manner until it reaches the on-state voltage drop. After this time, the gate voltage again increases but at a slower rate than during the initial turn-on phase.

3.6.1 Simulation Example

The gate charge for the 30-V power U-MOSFET structure was extracted by using the results of two-dimensional numerical simulations of the cell described in the previous sections. The device was turned-on from blocking state with a drain bias of 20 V by driving it using a gate current of 1×10^{-8} A/μm (equivalent to 0.67 A/cm^2 for the area of 1.5×10^{-8} cm^2). Once the drain current density reached 150 A/cm^2, the drain current was held constant resulting in a reduction of the drain voltage. The gate plateau voltage for this drain current density was found to be 2.7 V. Once the drain voltage reached the on-state value corresponding to the gate plateau voltage, the gate voltage increased to the steady-state value of 10 V.

The gate charge waveforms obtained by using an input gate current density of 0.67 A/cm^2 when turning on the power U-MOSFET structure from a blocking state with drain bias of 20 V are shown in Fig. 3.25. The on-state current density is 150 A/cm^2 at a DC gate bias of 10 V at the end of the turn-on transient. The gate voltage increases at a constant rate at the beginning of the turn-on process as predicted by the analytical model. When the gate voltage reaches the threshold voltage, the drain current begins to increase. The drain current increases very rapidly as predicted by the analytical model until it reaches the on-state current density of 150 A/cm^2.

Once the drain current reaches the on-state value, the gate voltage remains constant at the plateau voltage (V_{GP}). The plateau voltage for this structure is 2.7 V for the drain current density of 150 A/cm^2 as governed by the transconductance of the device. The drain voltage decreases during the plateau phase in a non-linear manner. After the end of the plateau phase, the gate voltage again increases until it reaches the gate supply voltage. Although the increase in gate voltage is non-linear at the beginning of this transition it becomes linear over most of the time after the plateau phase. The waveforms obtained using the analytical model are very similar in shape and magnitude to those observed in the numerical simulations.

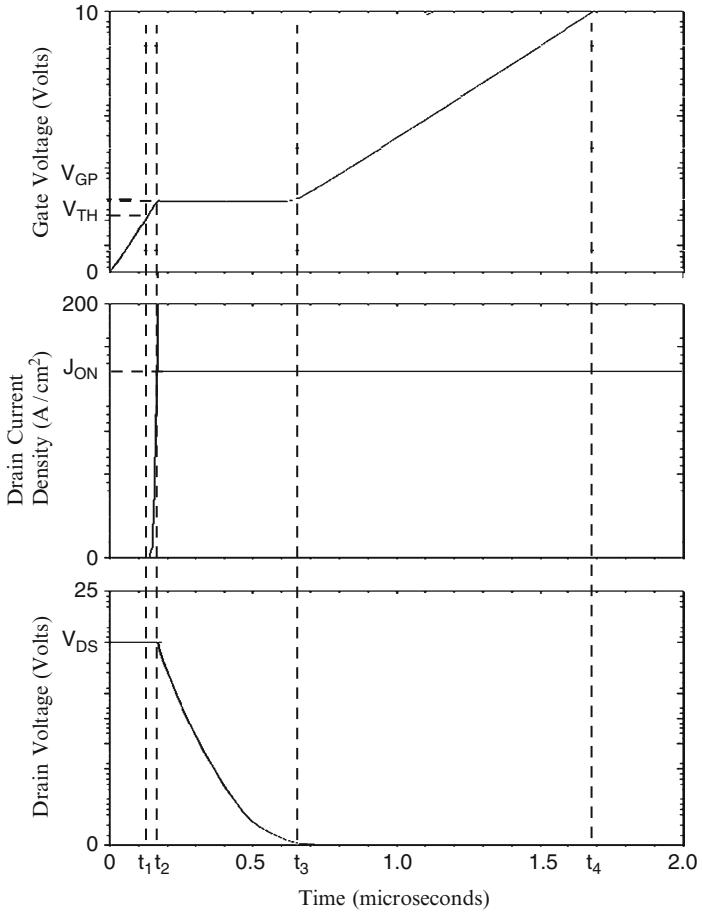

Fig. 3.25 Turn-on waveforms for the 30-V power U-MOSFET structure

Specific Gate Charge	Numerical Simulation (nC/cm^2)	Analytical Model (nC/cm^2)
Q_{GS1}	100	120
Q_{GS2}	13	13.5
Q_{GS}	113	133
Q_{GD}	326	361
Q_{SW}	339	376
Q_G	1127	1159

Fig. 3.26 Gate charge extracted from numerical simulations for the power U-MOSFET structure

The values for the various components of the gate charge extracted from the numerical simulations are compared with those calculated by using the analytical model in Fig. 3.26. There is good agreement between these values indicating that the analytical model is a reasonable representation of the physics of turn-on for power U-MOSFET structure.

3.7 Device Figures of Merit

Significant power switching losses can arise from the charging and discharging of the large input capacitance in power MOSFET devices at high frequencies. The input capacitance (C_{IN}) of the power MOSFET structure must be charged to the gate supply voltage (V_{GS}) when turning on the device and then discharged to 0 V when turning off the device during each period of the operating cycle. The total power loss can be obtained by summing the on-state power dissipation for a duty cycle $\delta = t_{ON}/T$ and the switching power losses:

$$P_T = P_{ON} + P_{SW} = \delta R_{ON} I_{ON}^2 + C_{IN} V_{GS}^2 f \tag{3.17}$$

where R_{ON} is the on-resistance of the power MOSFET structure, I_{ON} is the on-state current, and f is the operating frequency. In writing this equation, the switching power losses due to the drain current and voltage transitions has been neglected. A minimum total power loss occurs for each power MOSFET structure at an optimum active area as shown in the textbook [1]. The on-state and switching power losses are equal at the optimum active area. The optimum active area at which the power dissipation is minimized is given by:

$$A_{OPT} = \sqrt{\frac{R_{ON,sp}}{C_{IN,sp}}} \left(\frac{I_{ON}}{V_{GS}}\right) \left(\sqrt{\frac{\delta}{f}}\right) \tag{3.18}$$

From the first term in this expression, a useful technology figure-of-merit can be defined:

$$FOM(A) = \frac{R_{ON,sp}}{C_{IN,sp}} \tag{3.19}$$

In the power electronics community, there is trend towards increasing the operating frequency for switch mode power supplies in order to reduce the size and weight of the magnetic components. The ability to migrate to higher operating frequencies in power conversion circuits is dependent on making enhancements to the power MOSFET technology. From the above equations, an expression for the minimum total power dissipation can be obtained [1]:

$$P_T(\min) = 2 I_{ON} V_{GS} \sqrt{\delta R_{ON,sp} C_{IN,sp} f} \tag{3.20}$$

A second technology figure of merit related to the minimum power dissipation can be defined as:

$$FOM(B) = R_{ON,sp} C_{IN,sp} \tag{3.21}$$

In most applications for power MOSFET structures with high operating frequency, the switching losses associated with the drain current and voltage transitions become a dominant portion of the total power loss. The time period associated with the increase of the drain current and decrease of the drain voltage is determined by the charging of the device capacitances. It is therefore common practice in the industry to use the following figures-of-merit to compare the performance of power MOSFET products [1]:

$$FOM(C) = R_{ON,sp} Q_{GD,sp} \tag{3.22}$$

and

$$FOM(D) = R_{ON,sp} Q_{SW,sp} \tag{3.23}$$

Although FOM(D) encompasses both the drain current and voltage transitions, it is customary to use FOM(C) because the gate-drain charge tends to dominate in the switching gate charge. One advantage of using these expressions is that the figure-of-merit becomes independent of the active area of the power MOSFET device.

The figures of merit computed for the power U-MOSFET structure discussed in earlier sections of this chapter are provided in Fig. 3.27. The figure of merit usually used for comparison of device technologies in the literature is FOM(C). Most often, the value for this figure of merit at a gate bias of 4.5 V is utilized for selection of devices in the voltage regulator module application. In comparison with the power D-MOSFET structure (see Chap. 2), the power U-MOSFET structure has a FOM(C) at a gate bias of 4.5 V which is 2.4-times superior to the power D-MOSFET structure. In addition, the FOM(A) for the power U-MOSFET structure is a factor of nine times smaller than that for the power D-MOSFET structure. This implies a reduction in the active area by a factor of three times for the power U-MOSFET structure.

Figures of Merit	V_G = 4.5 V	V_G = 10 V
FOM(A) ($\Omega^2 cm^4 s^{-1}$)	7,085	3,720
FOM(B) (ps)	15.6	8.2
FOM(C) (mΩ*nC)	120	63
FOM(D) (mΩ*nC)	125	66

Fig. 3.27 Figures of merit for the power U-MOSFET structure

3.8 Thick Trench Bottom Oxide Structure

The power U-MOSFET structure discussed in the previous sections has a very low specific on-resistance due to the high channel density and the elimination of the JFET resistance. However, it has a large reverse transfer capacitance and reverse transfer gate charge that has an adverse impact on the switching performance. These disadvantages can be overcome by selectively increasing the thickness of the oxide at the bottom of the trench as illustrated in the device structure shown in Fig. 3.3 [3–5]. However, the thicker oxide at the bottom of the trenches increases the accumulation layer resistance. This produces an increase in the specific on-resistance for the power U-MOSFET structure.

3.8.1 On-Resistance

In the power U-MOSFET structure with the thick trench bottom oxide, only the accumulation layer resistance is impacted by the larger oxide thickness at the bottom of the trench. The specific on-resistance contributed by the accumulation layer in the power U-MOSFET structure with the thick oxide at the trench bottom can be obtained using:

$$R_{A,SP} = K_A \frac{L_A W_{Cell}}{2\mu_{nA} C_{OX,TB}(V_G - V_{TH})} \tag{3.24}$$

In this equation, the capacitance $C_{OX,TB}$ is the specific capacitance obtained using the thickness ($t_{OX,TB}$) of the trench bottom oxide. A typical trench bottom oxide thickness obtained by using the LOCOS process is 1,500 Å [3].

For the 30-V power U-MOSFET structure with a trench bottom oxide thickness of 1,500 Å and a cell width of 3 μm, the specific resistance contributed by the accumulation layer at a gate bias of 4.5 V increases to 0.087 mΩ cm^2 while the specific resistance contributed by the accumulation layer is increased to 0.039 mΩ cm^2 for the gate bias of 10 V. The total specific on-resistance for the power U-MOSFET structure with a trench bottom oxide thickness of 1,500 Å and a cell width of 3 μm then increases to 0.394 mΩ cm^2 for the gate bias of 4.5 V and 0.202 mΩ cm^2 for the gate bias of 10 V. This increase is about 15% over the power U-MOSFET structure without the thick oxide at the bottom of the trench.

3.8.2 Reverse Transfer Capacitance

The capacitance between the gate and drain electrodes (the reverse transfer capacitance) is determined by the width of the trench where the gate electrode overlaps the N-drift region. The oxide capacitance for the MOS structure in this portion of the

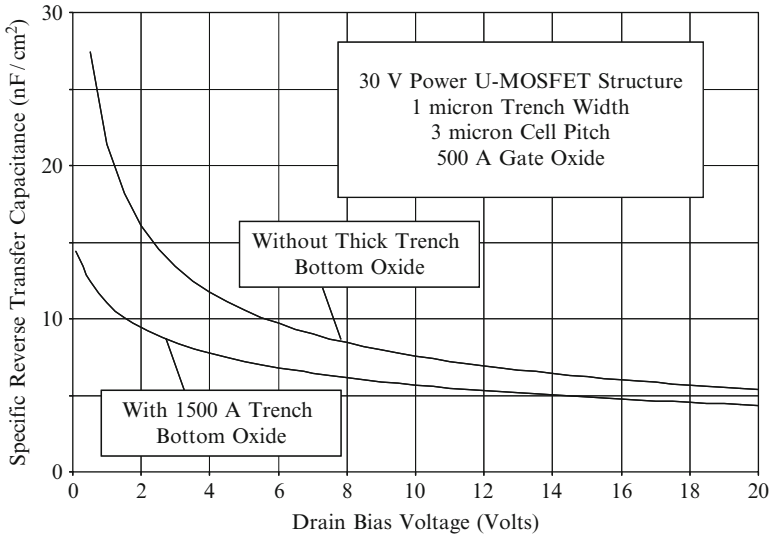

Fig. 3.28 Gate-drain capacitance for the power U-MOSFET structures

power U-MOSFET structure with the thick oxide at the bottom of the trench is reduced. The gate-drain capacitance for the power U-MOSFET structure with the thick oxide at the bottom of the trenches can be obtained using:

$$C_{GD,SP}=\left[\frac{W_T+2(t_T-x_{JP})}{W_{Cell}}\right]\left(\frac{C_{OX,TB}C_{S,M}}{C_{OX,TB}+C_{S,M}}\right) \tag{3.25}$$

where $C_{OX,TB}$ is the specific oxide capacitance for the thick oxide and $C_{S,M}$ is the semiconductor capacitance under the oxide, which decreases with increasing drain bias voltage. The specific capacitance of the semiconductor depletion region can be obtained by using the same formulae as in the previous U-MOSFET structure.

The specific gate transfer capacitance obtained by using the above analytical formula is shown in Fig. 3.28 for the case of a power U-MOSFET structure with 3 μm cell pitch, and trench width of 1 μm. This structure has a trench bottom oxide thickness of 1,500 Å, a trench depth of 1.5 μm and P-base junction depth of 1.0 μm. The gate-drain (reverse transfer) capacitance decreases with increasing drain bias voltage due to the expansion of the depletion region in the semiconductor. For purposes of comparison, this graph includes the reverse transfer capacitance for the power U-MOSFET structure with the gate oxide at the bottom of the trench. It can be observed that the reverse transfer capacitance is reduced by the thicker trench bottom oxide. The reduction is most effective at low drain bias voltages.

3.8.3 Gate Charge

As mentioned in the previous chapter, it is standard practice in the industry to provide the gate charge for power MOSFET structures as a measure of their switching performance. The most significant gate charge components for assessing the performance of the power MOSFET structures are Q_{SW} (the gate switching charge), Q_{GD} (the gate-drain charge), and Q_G (the total gate charge). These components for the power U-MOSFET structure with the thick trench bottom oxide are:

$$Q_{GD} = \frac{2K_G q\varepsilon_S N_D}{C_{OX,TB}} \left[\sqrt{1+\frac{2V_{DS}C_{OX,TB}^2}{q\varepsilon_S N_D}} - \sqrt{1+\frac{2V_{ON}C_{OX,TB}^2}{q\varepsilon_S N_D}} \right] \tag{3.26}$$

$$\begin{aligned} Q_{SW} = {} & [C_{GS} + C_{GD}(V_{DS})]\sqrt{\frac{J_{ON}W_{Cell}L_{CH}}{2\mu_{ni}C_{OX}}} \\ & + \frac{2K_G q\varepsilon_S N_D}{C_{OX,TB}} \left[\sqrt{1+\frac{2V_{DS}C_{OX,TB}^2}{q\varepsilon_S N_D}} - \sqrt{1+\frac{2V_{ON}C_{OX,TB}^2}{q\varepsilon_S N_D}} \right] \end{aligned} \tag{3.27}$$

$$\begin{aligned} Q_G = {} & [C_{GS} + C_{GD}(V_{DS})]V_{GP} \\ & + \frac{2K_G q\varepsilon_S N_D}{C_{OX,TB}} \left[\sqrt{1+\frac{2V_{DS}C_{OX,TB}^2}{q\varepsilon_S N_D}} - \sqrt{1+\frac{2V_{ON}C_{OX,TB}^2}{q\varepsilon_S N_D}} \right] \\ & + [C_{GS}+C_{GD}(V_{ON})](V_G - V_{GP}) \end{aligned} \tag{3.28}$$

In these equations, the parameter K_G is altered due to the thicker oxide at the trench bottom surface to:

$$K_G = \left[\frac{W_T + 2\left(t_T - x_P - t_{OX,TB}\right)}{W_{Cell}} \right] \tag{3.29}$$

where $t_{OX,TB}$ is the thickness of the trench bottom oxide.

The gate voltage waveform obtained for the power U-MOSFET structure with the thicker trench bottom oxide by using the analytical model is provided in Fig. 3.29 for the case of a gate current density of 0.67 A/cm^2. The time duration for the plateau in the gate voltage is reduced when compared with the structure without the thicker oxide at the trench bottom surface. The gate charge values obtained for the 30-V power U-MOSFET structure with a trench bottom oxide thickness of 1,500 Å by using the above equations are: $Q_{GD} = 258$ nC/cm^2; $Q_{SW} = 272$ nC/cm^2; and $Q_G = 849$ nC/cm^2. The gate-drain gate charge for the power U-MOSFET structure with the thick trench bottom oxide is reduced by 25%

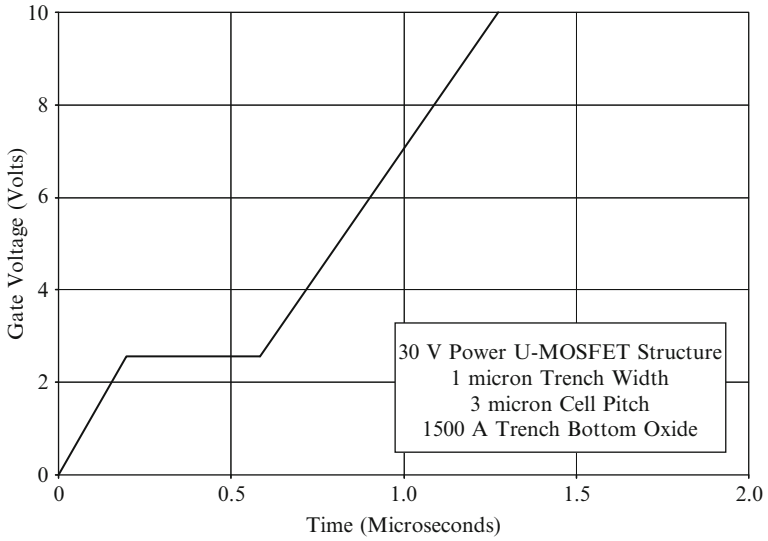

Fig. 3.29 Analytically computed gate voltage waveform for the 30-V power U-MOSFET structure with thick bottom oxide

compared with the previous power U-MOSFET structure. A greater reduction in the gate-drain charge has been achieved by not only increasing the oxide thickness at the bottom of the trench but by increasing the depth of the P-base region relative to the trench depth [3]. This approach has to be undertaken at the peril of increasing the on-resistance because of introducing a JFET effect in the U-MOSFET structure.

3.8.4 Device Figures-of-Merit

The figures of merit computed for the power U-MOSFET structure with the 1,500-Å thick oxide at the trench bottom by using the results of the analytical models are provided in Fig. 3.30. Only a modest 20% improvement in the figures-of-merit is predicted by the analytical models due to the increase in the on-resistance. However, larger improvements are observed with the simulations. Further, improved

Figures of Merit	V_G = 4.5 V	V_G = 10 V
FOM(C) (mΩ*nC)	101	52
FOM(D) (mΩ*nC)	107	55

Fig. 3.30 Figures of merit for the power U-MOSFET structure with 1,500-Å thick oxide at the bottom of the trench

figures of merit have been reported for fabricated devices by using more aggressive processing techniques such as increased P-base region depth and increase in the oxide thickness on the sidewalls of the trench only near the bottom surface.

3.8.4.1 Simulation Results

The results of two-dimensional numerical simulations on the 30-V power U-MOSFET structure with a thicker oxide at the bottom of the trench are described here to provide a more detailed understanding of the improvement in performance. The structure used for the numerical simulations had a drift region thickness of 3 μm below the junction (J_1) between the P-base region and the N-drift region with a doping concentration of $1.6 \times 10^{16}/cm^3$. The P-base region and N^+ source regions had depths of 1.0 and 0.1 μm, respectively. For the numerical simulations, half the cell (with a width of 1.5 μm) shown in Fig. 3.3 was utilized as a unit cell that is representative of the structure. The gate oxide was assumed to 500 Å on the trench sidewalls and 1,500 Å on the trench bottom surface. The doping concentration profiles for this U-MOSFET structure was kept identical to that of the structure with uniform oxide thickness in the trench.

The transfer characteristics for the U-MOSFET structure with thicker trench bottom oxide were obtained using numerical simulations with a drain bias of 0.1 V at 300 and 400°K. The resulting transfer characteristics are shown in Fig. 3.31. From this graph, a threshold voltage of 2.3 and 2.0 V can be extracted at 300 and 400°K, respectively – the same values as for the device without the thicker trench bottom oxide. The specific on-resistance can be obtained from the transfer characteristics at any gate bias voltage. For the case of a gate bias of 4.5 V and 300 °K, the specific in-resistance is found to be 0.284 mΩ cm^2, while for the case of a gate bias of 10 V and 300 °K, the specific in-resistance is found to be 0.172 mΩ cm^2. These values are very close to the values for the power U-MOSFET structure without the thick trench bottom oxide.

The specific on-resistance obtained using the analytical model indicates an increase in the specific on-resistance for the power U-MOSFET structure with the thick trench bottom oxide. This is associated with an increase in the contribution from the accumulation layer. As pointed out earlier for the power U-MOSFET structure with uniform oxide thickness, the current begins to spread into the drift region from the channel. This phenomenon ameliorates the impact of the thicker oxide at the bottom of the trench surface.

The current spreading pattern in the U-MOSFET structure with the thicker oxide on the trench bottom surface can be observed using the current flow-lines shown in Fig. 3.32 at a small drain bias of 0.1 V and a gate bias of 4.5 V. In the figure, the depletion layer boundary is shown by the dotted lines and the junction boundary is delineated by the dashed line. From this figure, it can be observed that the current spreading begins to occur from the junction between the P-base region and the N-drift region reducing the drift region resistance. Based up on these observations,

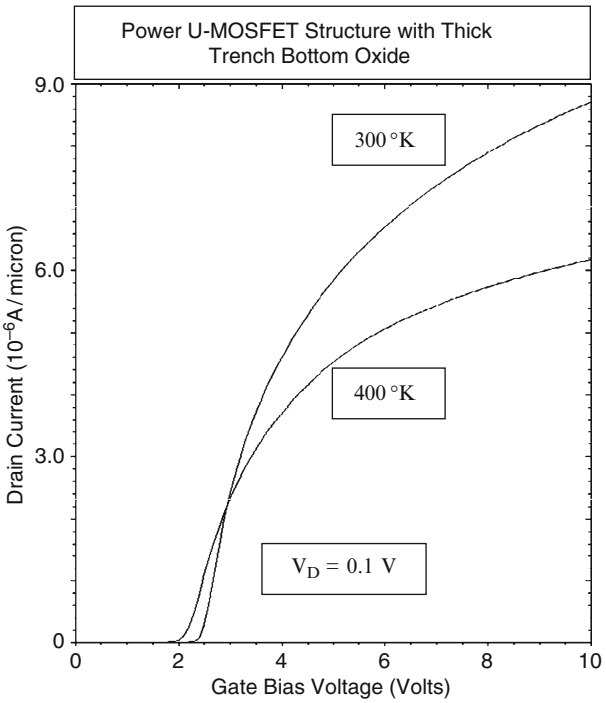

Fig. 3.31 Transfer characteristics of the U-MOSFET structure with thick trench bottom oxide

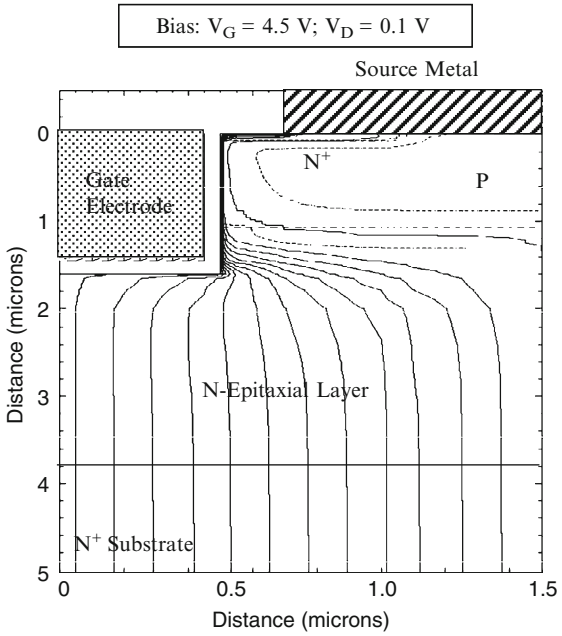

Fig. 3.32 Current distribution in the U-MOSFET structure with the thicker trench bottom oxide

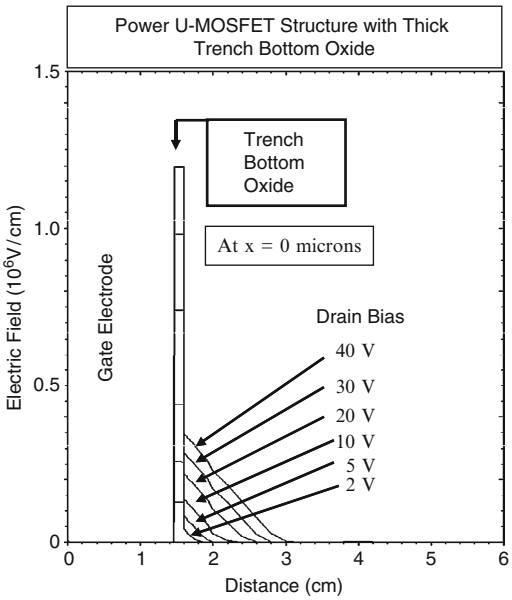

Fig. 3.33 Electric field distribution in the U-MOSFET structure with thicker trench bottom oxide

it can be concluded that the accumulation layer resistance can be neglected in the analytical model for the power U-MOSFET structure.

The electric field profile taken through the middle of the gate electrode and the trench (at $\times = 0$ μm) is provided in Fig. 3.33. It can be observed that the electric field in the trench bottom oxide is reduced to half that observed for the power U-MOSFET structure with uniform (500 Å) oxide thickness in the trench. The electric field in the oxide for the power U-MOSFET structure with the thicker oxide at the trench bottom is within the limit for reliable operation over long periods of time.

The drain-gate (reverse transfer) capacitance can be extracted by performing the numerical simulations with a small AC signal superposed on the DC drain bias voltage. The values obtained for the 30-V power U-MOSFET structure with thicker oxide at the trench bottom surface are shown in Fig. 3.34. The gate-to-drain and base-to-drain capacitances are shown in the figure for comparison. Both of these capacitances decrease with increasing drain bias voltage as expected from the analytical model. For this power U-MOSFET structure, the reverse transfer (gate-drain) capacitance is still larger in magnitude to the output (base-drain) capacitance and much larger that for the D-MOSFET structure. However, the reverse transfer capacitance is reduced when compared with the power U-MOSFET structure with uniform trench oxide thickness. The values for the reverse transfer and output capacitances obtained by using the analytical model for the power U-MOSFET structure with the thicker trench bottom oxide is in good agreement with the simulation values.

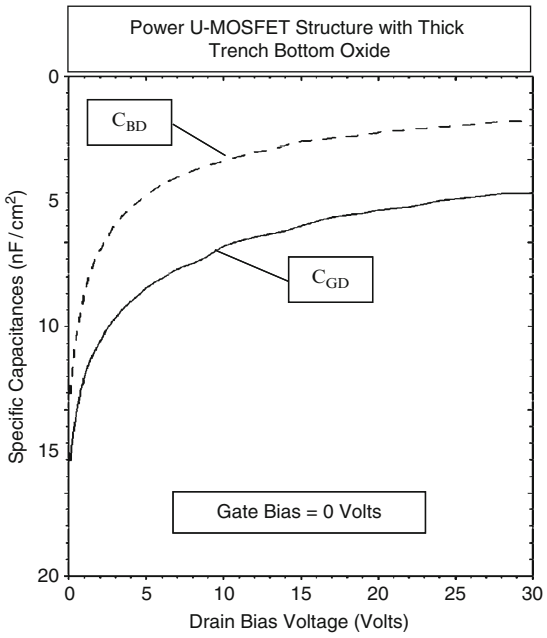

Fig. 3.34 Reverse transfer and output capacitances for the U-MOSFET structure with the thicker trench bottom oxide

The gate charge for the 30-V power U-MOSFET structure with thick trench bottom oxide was extracted by using the results of two-dimensional numerical simulations of the cell described above. The device was turned-on from blocking state with a drain bias of 20 V by driving it using a gate current of 1×10^{-8} A/μm (equivalent to 0.67 A/cm^2 for the area of 1.5×10^{-8} cm^2). Once the drain current density reached 150 A/cm^2, the drain current was held constant resulting in a reduction of the drain voltage. The gate plateau voltage for this drain current density was found to be 2.8 V. Once the drain voltage reached the on-state value corresponding to the gate plateau voltage, the gate voltage increased to the steady-state value of 10 V.

The gate charge waveforms obtained by using an input gate current density of 0.67 A/cm^2 when turning on the power U-MOSFET structure from a blocking state with drain bias of 20 V are shown in Fig. 3.35. The on-state current density is 150 A/cm^2 at a DC gate bias of 10 V at the end of the turn-on transient. The gate voltage increases at a constant rate at the beginning of the turn-on process as predicted by the analytical model. When the gate voltage reaches the threshold voltage, the drain current begins to increase. The drain current increases very rapidly as predicted by the analytical model until it reaches the on-state current density of 150 A/cm^2.

Once the drain current reaches the on-state value, the gate voltage remains constant at the plateau voltage (V_{GP}) (Fig. 3.35). The plateau voltage for this

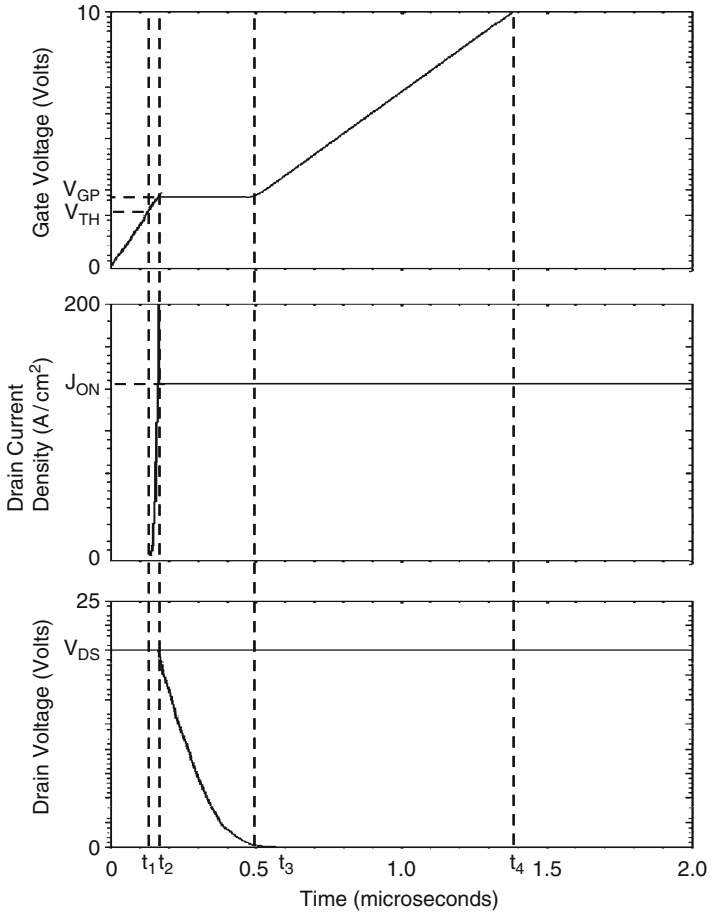

Fig. 3.35 Turn-on waveforms for the 30-V power U-MOSFET structure with thick trench bottom oxide

structure is 2.8 V for the drain current density of 150 A/cm^2 as governed by the transconductance of the device. The drain voltage decreases during the plateau phase in a non-linear manner. After the end of the plateau phase, the gate voltage again increases until it reaches the gate supply voltage. Although the increase in gate voltage is non-linear at the beginning of this transition it becomes linear over most of the time after the plateau phase. The waveforms obtained using the analytical model are very similar in shape and magnitude to those observed in the numerical simulations.

The values for the various components of the gate charge extracted from the numerical simulations are compared with those calculated by using the analytical model in Fig. 3.26. The analytical model predicts a 15% larger value for the gate transfer charge than observed in the simulations. There is good agreement

Specific Gate Charge	Numerical Simulation (nC/cm^2)	Analytical Model (nC/cm^2)
Q_{GS1}	100	118
Q_{GS2}	13	13.5
Q_{GS}	113	131
Q_{GD}	220	258
Q_{SW}	223	271
Q_G	927	849

Fig. 3.36 Gate charge extracted from numerical simulations for the power U-MOSFET structure with thick trench bottom oxide

between the values for the other gate charge components indicating that the analytical model is a good representation of the physics of turn-on for power U-MOSFET structure.

3.9 High Voltage Devices

The characteristics of a 600-V power U-MOSFET structure are described in this section for comparison with the performance of the power GD-MOSFET and power SJ-MOSFET structures that are discussed in later chapters. The analytical formulations presented in the previous sections for the power U-MOSFET structure are applicable for any breakdown voltage design when appropriate values for the device parameters are used during the computations. The values computed with the analytical models, provided in the last section of this chapter for devices with various blocking voltages, are in excellent agreement with the simulation results. This section will therefore focus on the results of two-dimensional numerical simulations for the 600-V power U-MOSFET structure.

3.9.1 Simulation Results

The breakdown voltage for the power U-MOSFET structure can be increased by reducing the doping concentration and increasing the width of the drift region. The same cell structure can be utilized for the higher breakdown voltage structures as used previously for the 30-V device. A doping concentration of $2.7 \times 10^{14}/cm^3$ and a thickness of 60 μm is appropriate for the drift region in the case of a breakdown voltage of 600 V. The doping profile used in the simulations of the 600-V power U-MOSFET structure is shown in Fig. 3.37.

The blocking characteristic for the 600-V power U-MOSFET cell structure is shown in Fig. 3.38 at 300°K. It can be observed that the blocking voltage exceeds

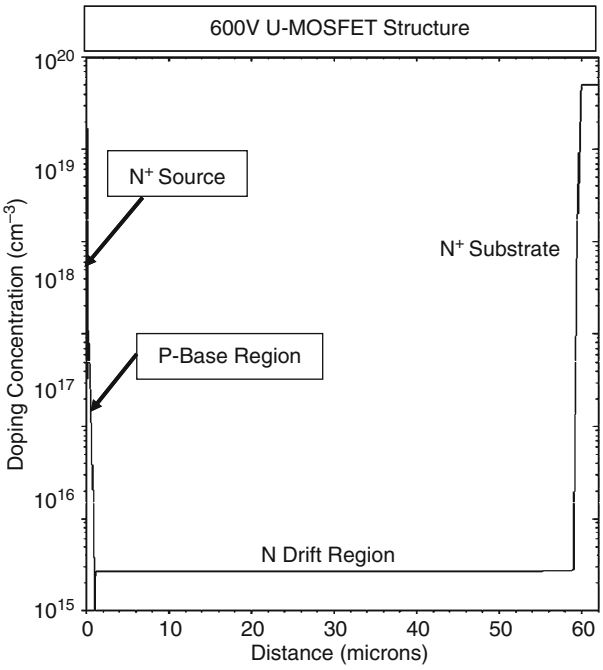

Fig. 3.37 Vertical doping profiles in the 600-V U-MOSFET structure

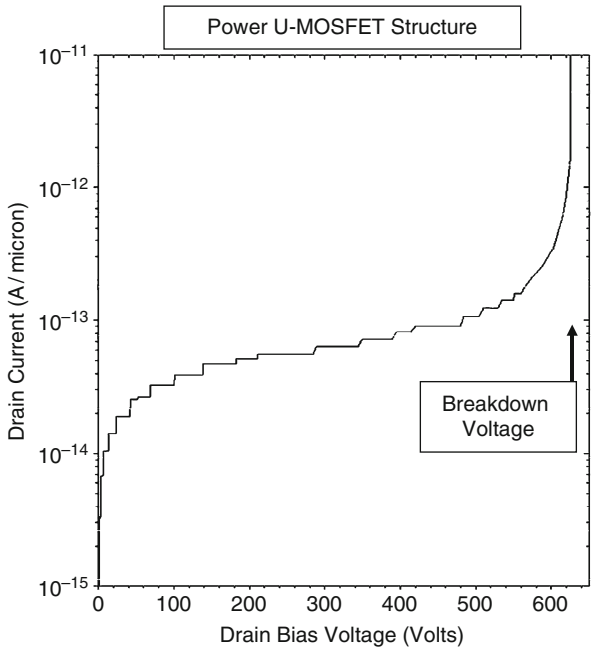

Fig. 3.38 Blocking characteristics for the 600-V U-MOSFET structure

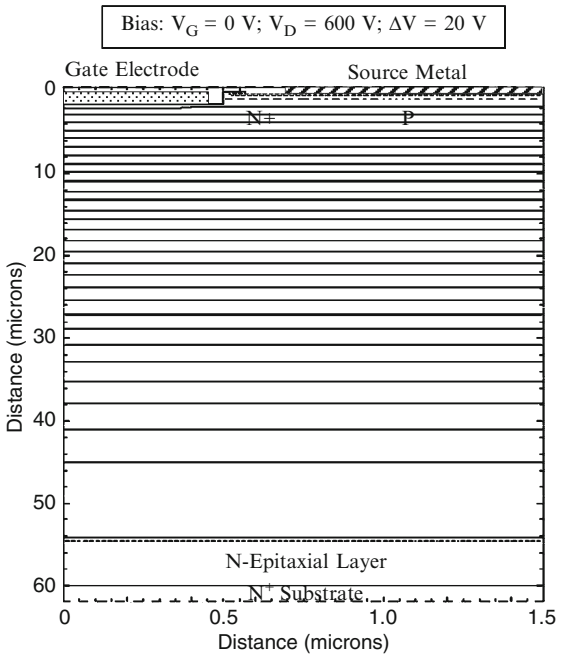

Fig. 3.39 Potential contours in the 600-V U-MOSFET structure

600 V for the chosen doping profile. For purposes of comparison with the high voltage power MOSFET structures in subsequent chapters, it is instructive to examine the potential contours inside the power 600-V U-MOSFET structure when it is operating in the blocking mode. The potential contours obtained using the numerical simulations with zero gate bias and a drain bias voltage of 600 V for the 600-V U-MOSFET structure are shown in Fig. 3.39. It can be observed that the potential lines are flat indicating nearly parallel-plane breakdown within the device cell structure. However, the potential lines are much closer together at the top of the structure when compared with the vicinity of the N^+ substrate indicating a non-uniform electric field distribution.

The electric field profiles along the vertical direction through the center of the mesa region are shown in Fig. 3.40 for the 600-V power U-MOSFET structure. The electric field has a triangular shape representative of a one-dimensional junction for all applied drain bias voltages. The electric field at the vicinity of the P-N junction is 2.1×10^5 V/cm at a drain bias of 600 V (just prior to breakdown). This magnitude of the electric field is in excellent agreement with the value for the critical electric field in the case of triangular electric field distribution predicted by the analytical model (see Fig. 1.13) for a 600-V device.

The transfer characteristics for the 600-V U-MOSFET structure were obtained using numerical simulations with a drain bias of 0.1 V at 300 and 400°K. The resulting transfer characteristics are shown in Fig. 3.41. The specific on-resistance

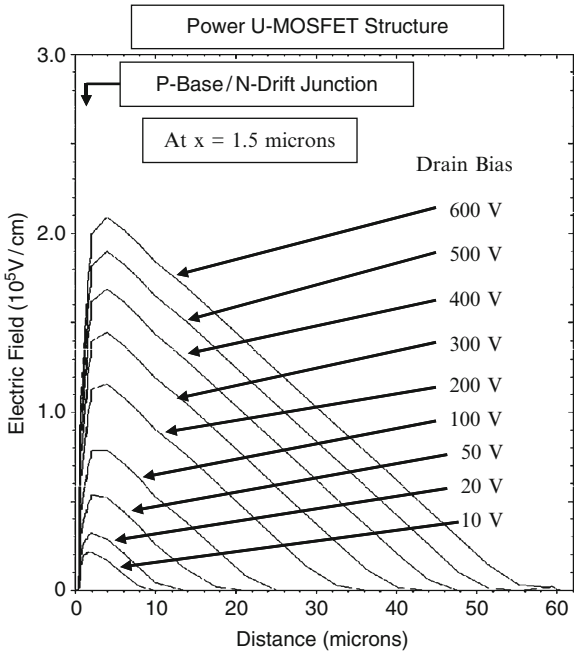

Fig. 3.40 Electric field profiles in the 600-V U-MOSFET structure

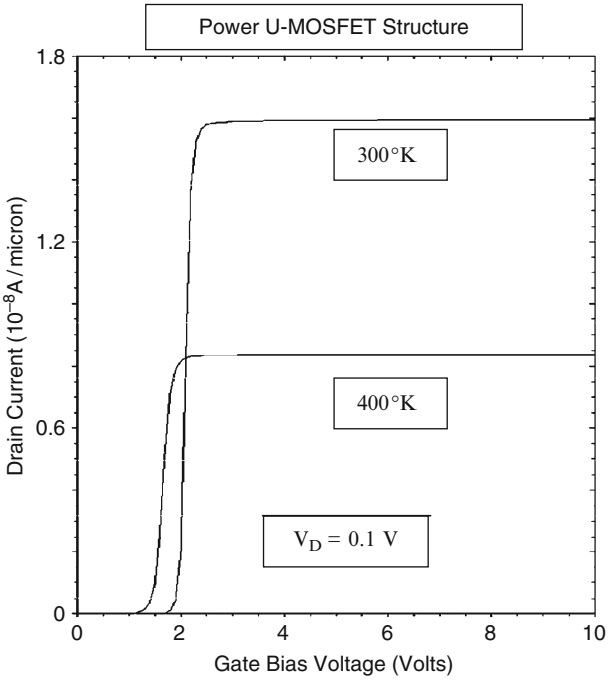

Fig. 3.41 Transfer characteristics of the 600-V U-MOSFET structure

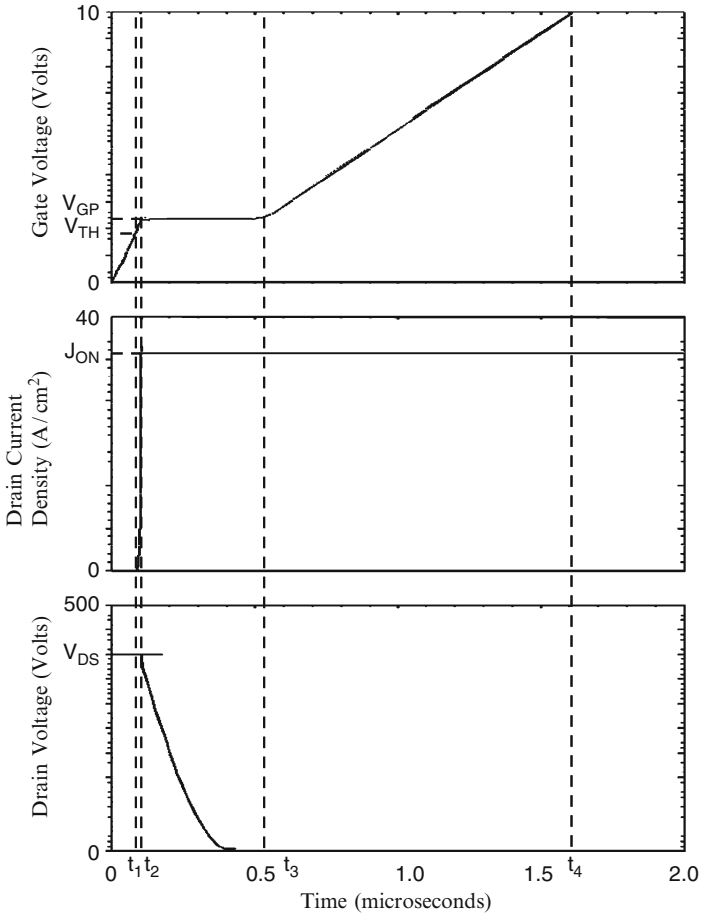

Fig. 3.42 Turn-on waveforms for the 600-V power GD-MOSFET structure

can be obtained from the transfer characteristics at any gate bias voltage. For the case of a gate bias of 10 V and 300°K, the specific in-resistance is found to be 94.1 mΩ cm^2. Since the ideal specific on-resistance for a 600 V device obtained using Baliga's power law for the impact ionization coefficients is 73.9 mΩ cm^2, the specific on-resistance of the power U-MOSFET structure approaches close to this ideal limit for silicon. One reason for this good performance is the low channel resistance contribution making the drift region resistance dominant as can be inferred from the very flat transfer characteristics at gate bias voltages above 3 V.

The gate charges for the 600-V power U-MOSFET structure were extracted by using the results of two-dimensional numerical simulations. The device was turned-on from blocking state with a drain bias of 400 V by using a gate current of 1×10^{-8} A/μm (equivalent to 0.67 A/cm^2 for the area of 1.5×10^{-8} cm^2). Once the drain current density reached the on-state value (34 A/cm^2) corresponding to a

on-state power dissipation of 100 W/cm^2, the drain current was held constant resulting in a reduction of the drain voltage. Once the drain voltage reached the on-state value corresponding to the gate plateau voltage, the gate voltage increased to the steady-state value of 10 V. The gate charge waveforms obtained by using the numerical simulations are shown in Fig. 3.42.

The values for the various components of the gate charge extracted from the numerical simulations for the 600-V power U-MOSFET structure are: $Q_{GS1} = 60$ nC/cm^2; $Q_{GS2} = 7$ nC/cm^2; $Q_{GD} = 267$ nC/cm^2; $Q_{SW} = 67$ nC/cm^2; and $Q_G = 1{,}070$ nC/cm^2. These values are smaller than those obtained for the 30-V power U-MOSFET structure because of the smaller doping concentration in the drift region for the 600-V device structure.

The Figure-of-Merit FOM(C) for the 600-V power U-MOSFET structure can be obtained using the results of the numerical simulations provided above. The Figure-of-Merit FOM(C) for the 600-V power U-MOSFET structure at a gate bias of 10 V is found to be 26,630 mΩ nC.

3.10 Inductive Load Turn-Off Characteristics

High voltage power MOSFET devices are often used for adjustable speed motor drives which behave as inductive loads. The basic half-bridge circuit utilized in these applications is shown in Fig. 10.1 of the textbook [1]. The waveforms for the current and voltage in the power switch are shown in Fig. 10.2 of the textbook. High power dissipation occurs during each turn-off event due to the simultaneous high current and voltage during the transient. This power loss is usually characterized as an energy loss per cycle.

The operation of a power MOSFET device in an inductive load circuit is illustrated in Fig. 3.43. The textbook provides a description of the basic operation of this circuit. After carrying the load current during its duty cycle, the power MOSFET device is switched off to transfer the current back to the free wheeling diode. Prior to the turn-off transient, the device is operating in its on-state because switch S_1 is closed and switch S_2 is open. These initial conditions are defined by: $v_G = V_{GS}$; $i_D = I_L$; and $v_D = V_{ON}(V_{GS})$. In order to initiate the turn-off process, switch S_1 is opened and switch S_2 is subsequently closed by the control circuit. The gate electrode of the power MOSFET device is then connected to the source via the gate resistance to discharge its capacitances. However, no changes in the drain current or voltage can occur until the gate voltage reaches the magnitude required to operate the power MOSFET device at a saturated drain current equal to the load current. (The small increase in the drain voltage, due to the increase in on-resistance resulting from the reduction of the gate bias voltage, has been neglected here). This gate plateau voltage is given by:

$$V_{GP} = V_{TH} + \sqrt{\frac{J_{D,ON} W_{Cell} L_{CH}}{\mu_{ni} C_{OX}}} \tag{3.30}$$

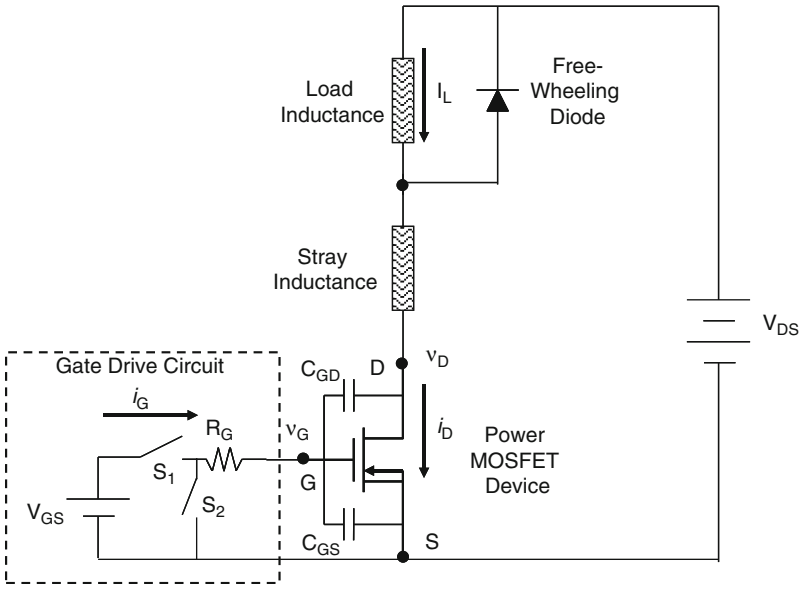

Fig. 3.43 Power MOSFET device operating in an inductive load circuit

where C_{OX} is the gate oxide capacitance. During this time interval, the gate-drain capacitance $C_{GD}(V_{ON})$ remains constant because the drain voltage is constant. Consequently, the time constant for discharging the gate of the power MOSFET device is $R_G*[C_{GS} + C_{GD}(V_{ON})]$ and the gate voltage decreases exponentially with time as given by:

$$v_G(t) = V_{GS}e^{-t/R_{G,SP}[C_{GS}+C_{GD}(V_{ON})]} \tag{3.31}$$

The time t_4 (using the notation from the textbook) for reaching the gate plateau voltage can be obtained by using this equation with (3.30) for the plateau voltage:

$$t_4 = R_{G,SP}[C_{GS} + C_{GD}(V_{ON})]\ln\left[\frac{V_{GS}}{V_{GP}}\right] \tag{3.32}$$

This time can be considered to a *turn-off delay time* before the drain voltage begins to increase after the turn-off is initiated by the control circuit.

The drain voltage begins to increase at time t_4 but the drain current remains constant at the load current I_L because the current cannot be transferred to the diode until the voltage at the drain of the MOSFET device exceeds the supply voltage V_{DS} by one diode drop to forward bias the diode. Since the drain current density is

constant, the gate voltage also remains constant at the gate plateau voltage. Consequently:

$$J_{GP} = \frac{V_{GP}}{R_{G,SP}} \tag{3.33}$$

Since all of the gate current is used to discharge the gate-drain capacitance during the plateau phase because there is no change in the voltage across the gate-source capacitance:

$$J_{GP} = C_{GD,SP}\frac{dv_D}{dt} \tag{3.34}$$

where $C_{GD,SP}$ is the specific gate transfer capacitance of the power MOSFET structure which is a function of the drain voltage. This voltage dependence of the gate transfer capacitance was not taken into account in the derivation provided in the textbook but is important to include here to allow comparison of the behavior of various power MOSFET structures.

The specific gate transfer capacitance of the power U-MOSFET structure can be taken into account by using the gate oxide capacitance, the semiconductor capacitance under the gate oxide and the relative area of the trench region:

$$C_{GD,SP} = \left(\frac{W_T}{W_{Cell}}\right)\left(\frac{C_{OX}C_{S,M}}{C_{OX} + C_{S,M}}\right) \tag{3.35}$$

where the specific semiconductor capacitance is given by:

$$C_{S,M} = \frac{\varepsilon_S}{W_{D,M}} \tag{3.36}$$

In this equation, the depletion width under the MOS gate region can be obtained by using:

$$W_{D,M} = \frac{\varepsilon_S}{C_{OX}}\left\{\sqrt{1 + \frac{2v_D(t)C_{OX}^2}{q\varepsilon_S N_D}} - 1\right\} \tag{3.37}$$

Combining the above relationships yields the following differential equation for the voltage increase phase of the turn-off transient:

$$dt = \left(\frac{W_T}{W_{Cell}}\right)\frac{C_{OX}}{J_{GP}}\frac{dv_D}{\sqrt{1 + \frac{2v_D(t)C_{OX}^2}{q\varepsilon_S N_D}}} \tag{3.38}$$

Integration of this equation yields:

$$(t - t_4) = \left(\frac{W_T}{W_{Cell}}\right)\frac{2q\varepsilon_S N_D}{J_{GP}C_{OX}}\left[\sqrt{1+\frac{2v_D(t)C_{OX}^2}{q\varepsilon_S N_D}}-\sqrt{1+\frac{2V_{ON}C_{OX}^2}{q\varepsilon_S N_D}}\right] \tag{3.39}$$

The voltage rise-time, i.e. the time taken for the voltage to increase from the on-state voltage drop (V_{ON}) to the drain supply voltage (V_{DS}) can be derived from the above expression:

$$t_{V,OFF} = \left(\frac{W_T}{W_{Cell}}\right)\frac{2q\varepsilon_S N_D}{J_{GP}C_{OX}}\left[\sqrt{1+\frac{2V_{DS}C_{OX}^2}{q\varepsilon_S N_D}} - \sqrt{1+\frac{2V_{ON}C_{OX}^2}{q\varepsilon_S N_D}}\right] \tag{3.40}$$

The voltage waveform during the rise-time can also be derived from (3.39):

$$v_D(t) = \frac{q\varepsilon_S N_D}{J_{GP}C_{OX}^2}\left\{\left[\sqrt{1+\frac{2V_{ON}C_{OX}^2}{q\varepsilon_S N_D}} + \left(\frac{W_{Cell}}{W_T}\right)\frac{J_{GP}C_{OX}}{2q\varepsilon_S N_D}t\right]^2 - 1\right\} \tag{3.41}$$

At the end of the plateau phase (at time t_5), the load current begins to transfer from the power MOSFET device to the free wheeling diode. Since the drain voltage remains constant, the gate-drain capacitance can also be assumed to remain constant during this phase. The current flowing through the gate resistance (R_G) discharges both the gate-drain and gate-source capacitances leading to an exponential fall in gate voltage from the plateau voltage:

$$v_G(t) = V_{GP}e^{-(t-t_5)/R_{G,SP}[C_{GS}+C_{GD}(V_{DS})]} \tag{3.42}$$

The drain current follows the gate voltage as given by:

$$J_D(t) = g_m[v_G(t) - V_{TH}] = \frac{\mu_{ni}C_{OX}}{2L_{CH}W_{Cell}}[v_G(t) - V_{TH}]^2 \tag{3.43}$$

The drain current decreases rapidly with time due to the exponential reduction of the gate voltage, as given by (3.42), during the current fall phase. The drain current becomes equal to zero when the gate voltage reaches the threshold voltage. The current fall time can therefore be obtained from (3.42):

$$t_{I,OFF} = R_{G,SP}[C_{GS} + C_{GD}(V_{DS})]\ln\left(\frac{V_{GP}}{V_{TH}}\right) \tag{3.44}$$

Specific capacitances should be used in this expression for computation of the current fall time. Beyond this point in time, the gate voltage decreases exponentially until it reaches zero. The time constant for this exponential decay is different from the initial phase due to the smaller gate-drain capacitance.

The largest power dissipation during the turn-off transient occurs during the drain voltage rise-time time interval ($t_{V,OFF}$). The turn-off energy loss per cycle can be obtained using:

$$E_{OFF} = \frac{1}{2} J_{ON} V_{DS} \left(t_{V,OFF} + t_{I,OFF} \right) \tag{3.45}$$

under the assumption that the drain current and voltage excursions are approximately linear with time.

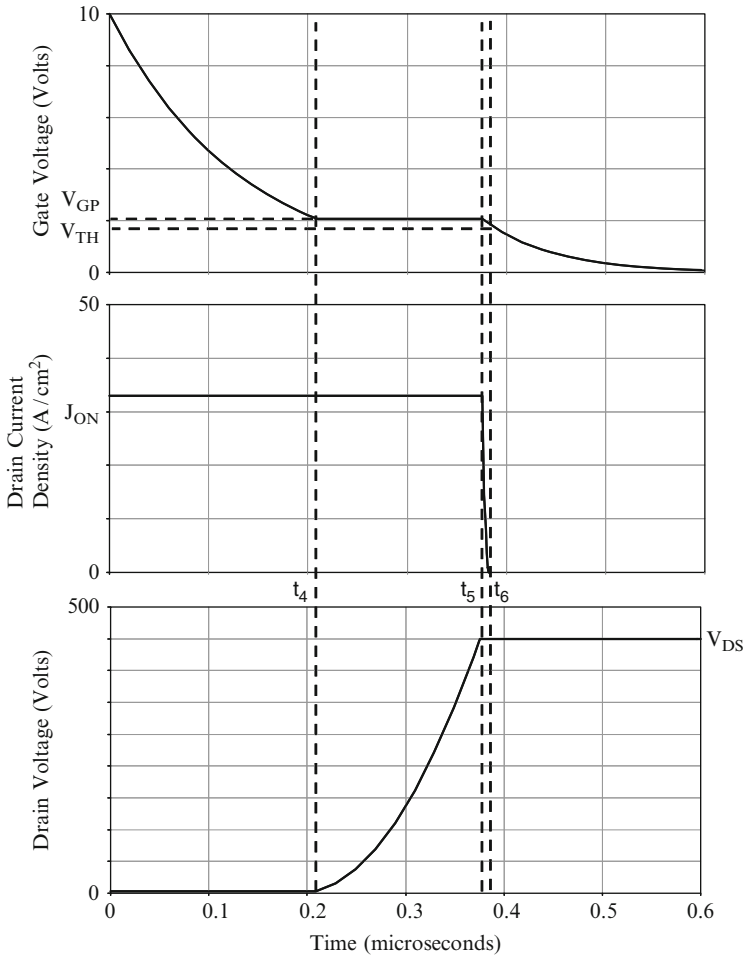

Fig. 3.44 Analytically computed turn-off waveforms for the 600-V power U-MOSFET structure

In the case of the 600-V power U-MOSFET structure, the typical drain supply voltage is 400 V. Using the specific on-resistance for this device of 94 mΩ cm^2 with an on-state power dissipation of 100 W/cm^2, the on-state current density is found to be 33 A/cm^2. The on-state voltage drop at this current density is 3.1 V. The device structure has a cell pitch of 3 μm with a mesa width of 2 μm, trench depth of 1.5 μm, and a gate oxide thickness of 500 Å. The drift region has a doping concentration of 2.7×10^{14}/cm^3 and thickness of 60 μm. The specific gate resistance used in the turn-off circuit was assumed to have a value of 1.5 Ω cm^2.

Using the above parameters, the specific gate reverse transfer capacitance computed by using (3.7) at the on-state voltage drop is 41.6 and 0.16 nF/cm^2 at the drain supply voltage. Using these values in (3.32), the time (t_4) to reach the gate plateau voltage is found to be 0.209 μs. Using these parameters in (3.40), the voltage rise-time is computed as 0.167 μs. Using these parameters in (3.44), the current fall-time is computed as 0.011 μs. It can be observed that the current fall time is much smaller than the voltage rise-time. The energy loss per cycle obtained by using these values for the voltage rise-time and current fall-time in (3.45) is 1.17 mJ/cm^2. The waveforms that can be generated by using the above equations are shown in Fig. 3.44.

3.10.1 Simulation Results

The results of two-dimensional numerical simulations on the turn-off of the 600-V power U-MOSFET structure are described below. The drain supply voltage was chosen as 400 V for the turn-off analysis. During the turn-off simulations, the gate voltage was reduced to zero with a gate resistance of 1×10^8 Ω μm for the 1.5 μm half-cell structure, which is equivalent to a specific gate resistance of 1.5 Ω cm^2. The current density was initially held constant at an on-state current density of 33 A/cm^2 allowing the drain voltage to rise to the drain supply voltage. The drain supply voltage was then held constant allowing the drain current density to reduce to zero.

The turn-off waveforms obtained for the 600-V power U-MOSFET structure by using the numerical simulations are shown in Fig. 3.45. The gate voltage initially reduces to the gate plateau voltage corresponding to the on-state current density. The drain voltage then increases from the on-state voltage drop to the drain supply voltage. After this, the drain current rapidly falls to zero. The drain voltage rise-time ($t_5 - t_4$) can be observed to be much greater than the drain current fall time ($t_6 - t_5$). The drain voltage rise-time obtained from the simulations of the power U-MOSFET structure is 0.185 μs and the drain current fall-time obtained from the simulations is 0.01 μs. The shape of the waveforms predicted by the analytical model (see Fig. 3.44) for the gate voltage, drain voltage and drain current are in good agreement with the simulation results. The numerical values predicted for the analytical model for the voltage rise-time and the drain fall-time are also in good agreement with those observed in the numerical simulations

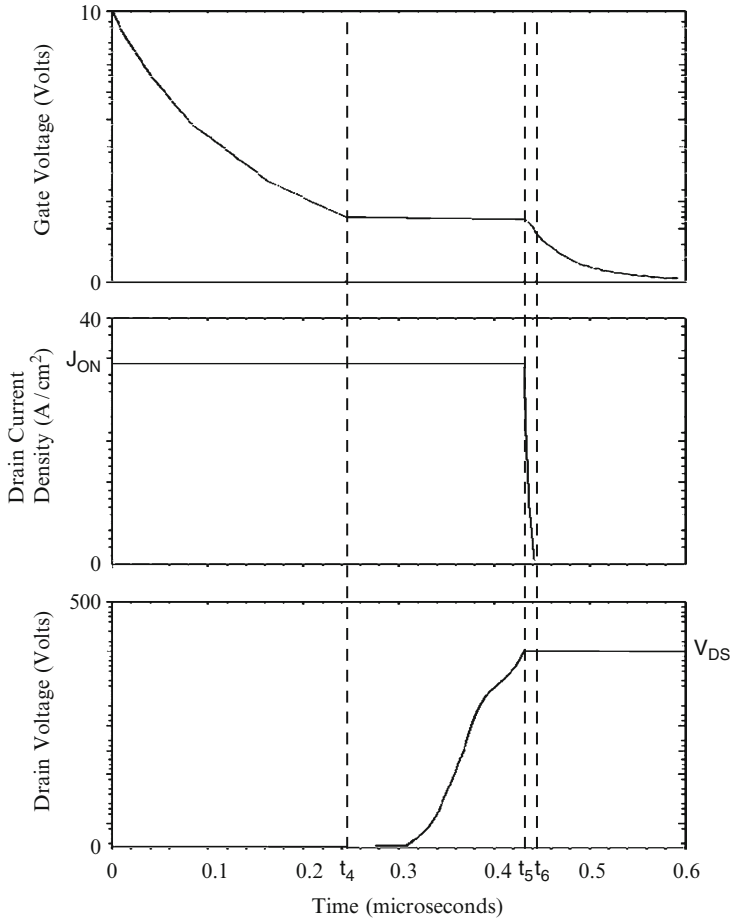

Fig. 3.45 Turn-off waveforms for the 600-V power U-MOSFET structure

allowing an accurate computation of the energy loss per cycle for the power U-MOSFET structure.

3.11 Discussion

The characteristics of the power U-MOSFET structure has been reviewed in this chapter. The specific on-resistance for this device structure is significantly reduced when compared with the power D-MOSFET structure due to its high channel density and the elimination of the JFET resistance contribution. The reduced specific on-resistance for the power U-MOSFET structure allows fabrication of devices with smaller active area to achieve the same absolute value for the on-resistance.

However, the reverse transfer capacitance and gate charge for the power U-MOSFET structure are twice as large as for the power D-MOSFET structure. Despite the larger capacitance and gate charge per unit area, the figures-of-merit for the power U-MOSFET structure are superior to those for the power D-MOSFET structure. Consequently, the power U-MOSFET structure has supplanted the power D-MOSFET structure in high frequency power circuits such as the voltage regulator modules for supply power to microprocessors.

The switching performance and figures-of-merit for the power U-MOSFET structure can be enhanced by the use of a thicker oxide on the trench bottom surface. The thicker oxide serves to reduce the gate-drain capacitance especially at low drain bias voltages. This leads to a smaller gate-transfer charge which is beneficial to achieving better figures-of-merit.

For purposes of comparison with the power D-MOSFET structures in the preceding chapter, the analysis of the power U-MOSFET structure is provided here for a broad range of blocking voltages. In this analysis, the power U-MOSFET structure was assumed to have the following parameters: (a) N^+ source junction depth of 0.1 μm; (b) P-base junction depth of 1.0 μm; (c) gate oxide thickness of 500 Å; (d) trench width of 1.0 μm; (e) mesa width of 2.0 μm; (f) threshold voltage of 2 V; (g) gate drive voltage of 10 V; (h) inversion mobility of 450 cm^2/V s; (i) accumulation mobility of 1,000 cm^2/V s. The contributions from the contacts and the N^+ substrate were neglected during the analysis. The doping concentration and thickness of the drift region were determined under the assumption that the edge termination (in conjunction with the graded junction doping profiles) limits the breakdown voltage to 90% of the parallel-plane breakdown voltage. The device parameters pertinent to each blocking voltage are provided in Fig. 3.46. These values are the same as those used for the analysis of the power D-MOSFET structure in Chap. 2. It can be observed that the doping concentration must be greatly reduced with increasing blocking voltage capability while simultaneously increasing the thickness of the drift region.

Blocking Voltage (V)	Drift Doping Concentration (cm^{-3})	Drift Region Thickness (microns)
30	1.6×10^{16}	3
60	6.0×10^{15}	5
100	3.0×10^{15}	8
200	1.2×10^{15}	17
300	6.8×10^{14}	26
600	2.7×10^{14}	58
1000	1.35×10^{14}	105

Fig. 3.46 Device parameters for the power U-MOSFET structures

Blocking Voltage (V)	Cell Pitch (microns)	Specific On-Resistance ($m\Omega$-cm^2)
30	3.0	0.171
60	3.0	0.525
100	3.0	1.43
200	3.0	6.92
300	3.0	18.2
600	3.0	100
1000	3.0	360

Fig. 3.47 Optimized specific on-resistance for the power U-MOSFET structures

In the power U-MOSFET structure, the smallest specific on-resistance is obtained when the trench and mesa width are minimized within the constraints of processing and lithography considerations. Consequently, a single device cell structure with a trench width of 1 μm and a mesa width of 2 μm (cell pitch of 3 μm) will be utilized here for the analysis of devices with various breakdown voltages. A two zone model for the resistance of the drift region was utilized for the analysis of the specific on-resistance. The specific on-resistances computed using the analytical model for the power U-MOSFET structures are provided in Fig. 3.47.

The specific on-resistance for the power U-MOSFET structure can be compared with the ideal specific on-resistance (obtained by using Baliga's power law for the impact ionization coefficients) in Fig. 3.48. From this figure, it can be concluded that the specific on-resistance for the U-MOSFET structure is always larger than the ideal specific on-resistance. For blocking voltages below 50 V, the specific on-resistance for the power U-MOSFET structure becomes substantially larger than the ideal case. At a blocking voltage of 30 V, the specific on-resistance is about three times larger than the ideal specific on-resistance obtained by using Baliga's power law for the impact ionization coefficients.

The specific gate transfer charge for the power U-MOSFET structures was obtained by using the analytical model (see 3.26). During this analysis, the devices were assumed to be operated at an on-state current density that results in a power dissipation of 100 W/cm^2 as determined by the specific on-resistance for each device. The on-state current density values are provided in Fig. 3.49. The drain supply voltage used for this analysis was chosen to be two-thirds of the breakdown voltage. The drain supply voltage values are also provided in Fig. 3.49.

The specific gate transfer charge values calculated by using the analytical model for the power U-MOSFET structure are given in Fig. 3.49 as a function of the breakdown voltage. These values are also plotted in Fig. 3.50 as a function of the breakdown voltage. It can be observed that the gate transfer charge decreases gradually with increasing breakdown voltage. The specific gate transfer charge decreases in a linear fashion on this log-log graph for breakdown voltages ranging

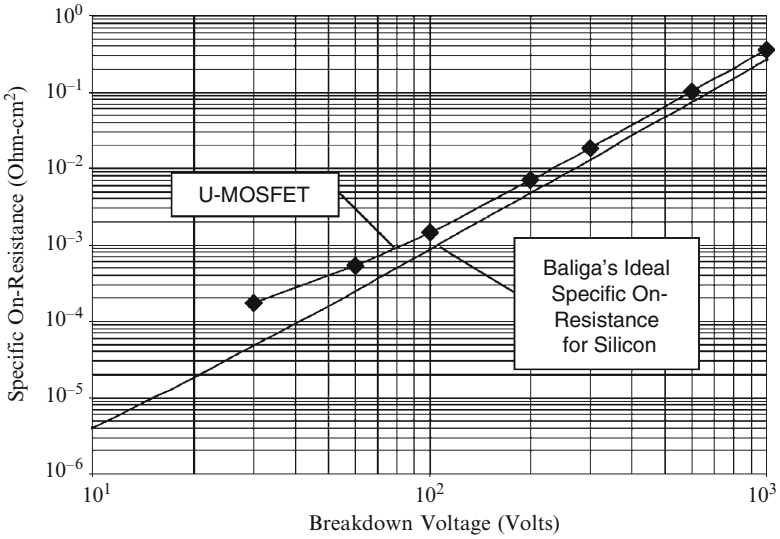

Fig. 3.48 Specific on-resistance for the power U-MOSFET structures

Blocking Voltage (V)	Drain Supply Voltage (Volts)	On-State Current Density (A / cm^2)	Specific Gate Transfer Charge (nC / cm^2)
30	20	765	356
60	40	436	325
100	80	264	300
200	133	120	269
300	200	74	247
600	400	32	218
1000	667	17	198

Fig. 3.49 Parameters used for gate transfer charge analysis for the power U-MOSFET structures

from 100 to 1,000 V indicating a power law relationship. The power law relationship that fits the data is shown in the figure by the dashed line. The equation for this line is:

$$Q_{GD} = \quad 689BV^{-0.18} \tag{3.46}$$

where the specific gate transfer charge has units of nC/cm^2.

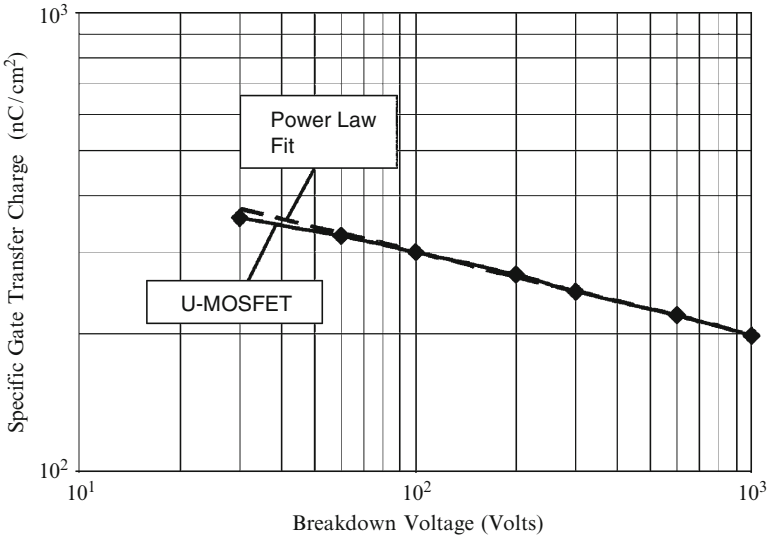

Fig. 3.50 Specific gate transfer charge for the power U-MOSFET structures

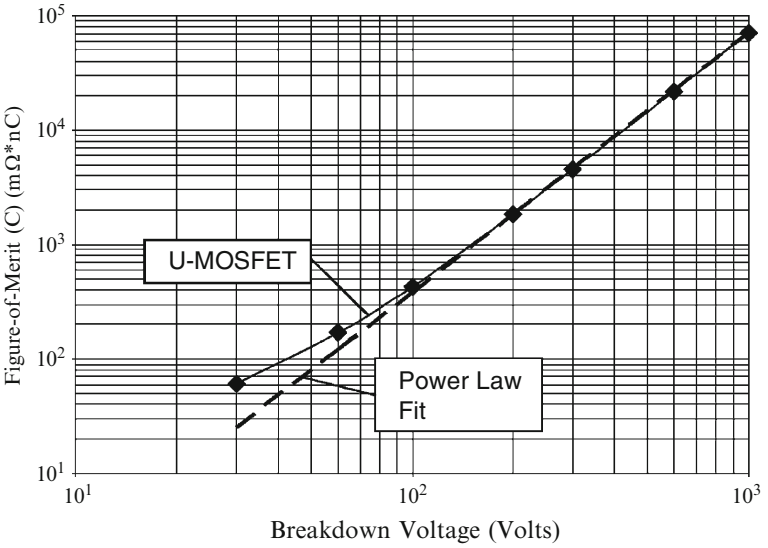

Fig. 3.51 Figure-of-merit (C) for the power U-MOSFET structures

The figure-of merit (C) – product of the specific on-resistance and the specific gate transfer charge – for the power U-MOSFET structures was obtained by using the specific gate transfer charge and specific on-resistance values provided above. During this analysis, the devices were assumed to be operated at an on-state

current density that results in a power dissipation of 100 W/cm^2 as determined by the specific on-resistance for each device. The resulting values for the FOM(C) are plotted in Fig. 3.51 as a function of the breakdown voltage of the power U-MOSFET structure. It can be observed that the FOM(C) increases in a linear fashion on this log-log graph for breakdown voltages above 100 V indicating a power law relationship. The power law relationship that fits the data is shown in the figure by the dashed line. The equation for this line is:

$$\text{FOM(C)} = R_{ON,sp}Q_{GD,sp} = 0.0113\ BV^{2.267} \tag{3.47}$$

where the FOM(C) has units of mΩ nC. The specific on-resistance and FOM(C) discussed here for the power U-MOSFET structure will be compared with those for the power D-MOSFET and other structures in the final chapter of the book.

References

1. B.J. Baliga, "Fundamentals of Power Semiconductor Devices", Springer-Science, New York, 2008.
2. J. Zeng, et al, "An Ultra-Dense Trench-Gated Power MOSFET Technology using a Self-Aligned Process", IEEE International Symposium on Power Semiconductor Devices, Abstract 7.3, pp. 147–150, 2001.
3. M. Darwish, et al, "A New Power W-Gated Trench MOSFET (WMOSFET) with High Switching Performance", IEEE International Symposium on Power Semiconductor Devices, Abstract 1.1, 2003, pp. 100–104.
4. T. Aoki, et al, "High Performance and Reliability Trench Gate Power MOSFET with Partially Thick Gate Oxide Film Structure", IEEE International Symposium on Power Semiconductor Devices, Abstract 6.3, pp. 85–88, 2006.
5. H. Wang, et al, "A 70V UMOS Technology with Trenched LOCOS Process to Reduce C_{gs}", IEEE International Symposium on Power Semiconductor Devices, Abstract P8-25, pp. 181–184, 2007.
6. N. Thapar and B. J. Baliga, "Influence of the Trench Corner Design on Edge Termination of UMOS Power Devices", Solid State Electronics, Vol. 41, pp. 1929–1936, 1997.

Chapter 4
SC-MOSFET Structure

As discussed in Chap. 2, the first power MOSFET structure commercially introduced by the power semiconductor industry was the D-MOSFET structure with the planar gate architecture. The fast switching speed and ruggedness of the D-MOSFET structure were significant advantages compared with the performance of the available bipolar power transistor. In order to reduce the specific on-resistance of the structure, the planar gate topology was replaced with a trench gate topology in the 1990s by creating the power U-MOSFET structure. The significant reduction of the specific on-resistance achieved using this approach has been described in Chap. 3. It has been found that the high input capacitance and large gate transfer charge for the power U-MOSFET structure offsets the benefits of the low specific on-resistance in high frequency applications such as the voltage-regulator-modules (VRMs) used to provide power to microprocessors.

Recently, significantly enhanced performance has been achieved in a planar gate power MOSFET structure by shielding the channel region from the drain. This shielded-channel power MOSFET structure (the SC-MOSFET) is the subject of this chapter. Although many aspects of operation of this device are similar to those already described for the power D-MOSFET structure, the SC-MOSFET structure contains a shielding junction with a unique JFET region doping profile to achieve a specific on-resistance close to that observed for the power U-MOSFET structure while also obtaining a reduced input capacitance and a very low gate transfer charge. This structure can be fabricated by using standard planar processes like the power D-MOSFET structure which reduces the complexity and cost in relation to the power U-MOSFET structure.

Commercially available power SC-MOSFET structures have been benchmarked against commercially available power U-MOSFET structure for the VRM applications and found to enable a significant improvement in efficiency for DC-to-DC power conversion at high frequencies. These devices are of interest for applications in laptops and servers where heat management becomes an important issue during operation.

B.J. Baliga, *Advanced Power MOSFET Concepts*,
DOI 10.1007/978-1-4419-5917-1_4,

4.1 The SC-MOSFET Structure

A cross-section of the basic cell structure for the SC-MOSFET structure [1] is illustrated in Fig. 4.1. This device structure is fabricated by starting with an N-type epitaxial layer grown on a heavily doped N^+ substrate. As in the case of the power D-MOSFET structure, the channel is formed by the difference in lateral extension of the P-base and N^+ source regions produced by their diffusion cycles. Both regions are self-aligned to the left-hand-side and right-hand-side of the gate region during ion-implantation to introduce the respective dopants. A refractory gate electrode, such as polysilicon, is required to allow diffusion of the dopants under the gate electrode at elevated temperatures. The unique aspect of the power SC-MOSFET structure is the addition of a P^+ screening region which is located at a larger depth than the P-base region.

In the power D-MOSFET structure, it is customary to choose the energy of the ion-implants for the dopants so that their highest concentration lies at the surface of the silicon. In contrast, a retrograde doping profile, with the peak doping concentration located below the silicon surface, is employed for the P^+ region and the JFET region in the power SC-MOSFET structure. In addition, the P^+ region is driven-in further than the P-base region so that it extends further under the gate electrode than the P-base region [2]. A relatively small spacing between the P^+ shielding regions is utilized in the power SC-MOSFET structure when compared with the power D-MOSFET structure to reduce the cell pitch to values comparable to those for the power U-MOSFET structure. In order to prevent a high JFET resistance, the doping concentration of the JFET region is enhanced by utilizing a n-type ion-implant with a relatively high doping

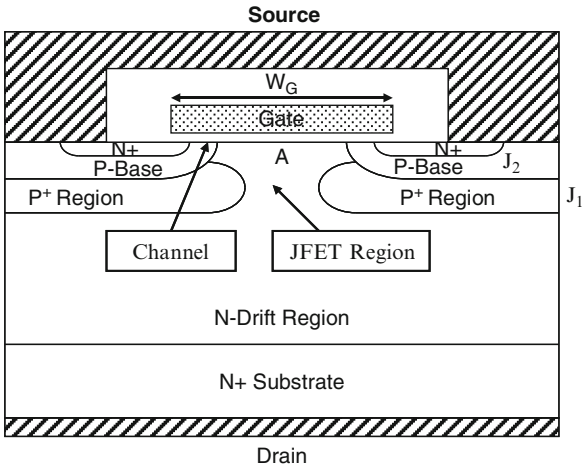

Fig. 4.1 The SC-MOSFET structure

concentration with its peak located at the same depth as the peak doping concentration of the P^+ shielding regions.

The physics of operation of the power SC-MOSFET structure is similar to that for the power D-MOSFET structure. Without the application of a gate bias, a high voltage can be supported in the SC-MOSFET structure when a positive bias is applied to the drain. In this case, junction J_1 formed between the P^+ shielding region and the N-drift region becomes reverse biased. The voltage is supported mainly within the thick lightly doped N-drift region. The space between the P^+ shielding regions and the doping concentration of the JFET region are designed so that a potential barrier forms between the P^+ shielding regions at a low drain bias voltage. The potential barrier shields the region under the gate oxide (marked A in Fig. 4.1) reducing the potential supported across the P-base region. This enables reduction of the channel length without encountering reach-through breakdown in the power SC-MOSFET structure. The channel length for the power SC-MOSFET structure can be made smaller than that for the power U-MOSFET structure producing a reduction in the specific on-resistance that compensates for the resistance contribution from the JFET region.

Drain current flow in the SC-MOSFET structure is induced by the application of a positive bias to the gate electrode. This produces an inversion layer at the surface of the P-base region under the gate electrode. The threshold voltage for the power SC-MOSFET structure can be controlled by adjusting the dose for the boron ion-implantation for the P-base region. The energy for the boron ion-implantation for the P-base region is chosen to maintain its peak concentration at the surface of the silicon. The inversion layer channel provides a path for transport of electrons from the source to the drain when a positive drain voltage is applied.

After transport from the source region through the channel, the electrons enter the N-drift region at the upper surface of the device structure. They are then transported through a relatively narrow JFET region located between the adjacent P^+ shielding regions within the SC-MOSFET structure. The constriction of the current flow through the JFET region increases the internal resistance of the SC-MOSFET structure. A careful optimization the retrograde doping concentration profile in the JFET region is necessary to reduce the resistance to current flow through this portion of the device structure.

After being transported through the JFET region, the electrons enter the N-drift region below junction J_1. The current spreads from the relatively narrow JFET region to the entire width of the cell cross-section. This non-uniform current distribution within the drift region enhances its resistance making the internal resistance of the SC-MOSFET structure larger than the ideal specific on-resistance of the drift region. The small cell-pitch for the power SC-MOSFET enables reducing the drift region resistance closer to that for the ideal case than for the power D-MOSFET structure. This requires utilizing a relatively smaller window between the polysilicon gate regions than in the case of the power D-MOSFET structure, which is possible because a separate mask is not required to define the ion-implantation boundary for the P^+ shielding regions in the power U-MOSFET structure.

4.2 Power SC-MOSFET On-Resistance

The components of the on-resistance for the power SC-MOSFET structure are the same as those already described for the power D-MOSFET structure. The total on-resistance for the power SC-MOSFET structure is obtained by the addition of all the eight resistances because they are considered to be in series in the current path between the source and the drain electrodes:

$$R_{ON} = R_{CS} + R_{N+} + R_{CH} + R_A + R_{JFET} + R_D + R_{SUB} + R_{CD} \tag{4.1}$$

Each of the resistances within the power SC-MOSFET structure are analyzed below by using the procedure described in the textbook [3]. In the textbook, it was demonstrated that the contributions from the source contact resistance (R_{CS}), the source resistance (R_{N+}), and the drain contact resistance (R_{CD}) are very small and will therefore be neglected in this chapter. As in the case of the power D-MOSFET and U-MOSFET structures, the substrate contribution will also be excluded for the comparison of devices.

A cross-section of the power SC-MOSFET structure is illustrated in Fig. 4.2 with various dimensions that can be used for the analysis of the on-resistance components. Here, W_{Cell} is the pitch for the linear cell geometry analyzed in this section; W_G is the width of the gate electrode; W_{PW} is the width of the polysilicon window; W_C is the width of the contact window to the N^+ source and P-base regions; and W_S

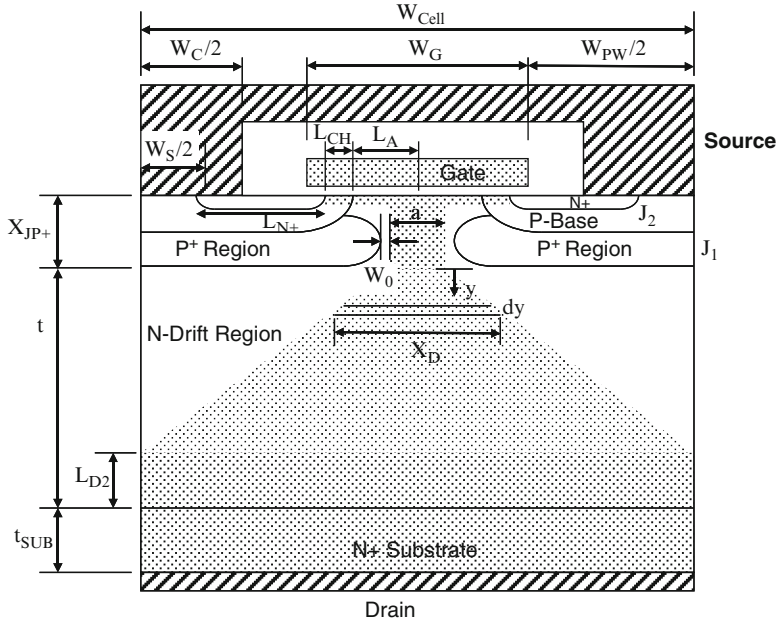

Fig. 4.2 Power SC-MOSFET structure with current flow model used for analysis of its internal resistances

is the width of the photoresist mask used during the N^+ source ion-implantation. The junction depths of the P-base region and the deep P^+ shielding region are x_{JP} and x_{JP+}, respectively.

In this monograph, the characteristics of power SC-MOSFET structure with 30-V blocking capability will be analyzed for power supply applications. For this voltage rating and the 1-μm lithography design rules, the power SC-MOSFET structure has a cell pitch (W_{CELL}) of 3 μm with a polysilicon gate width (W_G) of 1 μm. Typical junction depths for the N^+ source region and P-base region are 0.075 and 0.235 μm, respectively, leading to a channel length of only 0.16 μm. This short channel length is possible due to the shielding of the channel region in the power SC-MOSFET structure. The P^+ shielding region is formed by using high energy ion-implantation of boron leading to its peak concentration located below the surface at a depth of 0.3 μm. Due to the range of the ion-implantation and the subsequent diffusion during the annealing process, the vertical junction depth of the P^+ shielding region is typically 0.6 μm. In contrast, the lateral extension of the P^+ shielding region under the gate electrode is only 0.265 μm.

The doping concentration of the N-drift region required to achieve a 30-V blocking voltage capability, with an 80% reduction due to the edge termination, is $1.6 \times 10^{16}/cm^3$. The thickness of the N-drift region required below the P^+ shielding region is 2.6 μm. It is worth pointing out that the entire blocking voltage is not supported within the N-drift region because of the graded doping profile of the P^+ shielding region. This allows increasing the doping concentration and reducing the thickness of the N-drift region to achieve a smaller specific on-resistance for the D-MOSFET structure.

In the power SC-MOSFET structure, the energy for the ion-implantation of the P-type dopant (boron) for formation of the P^+ shielding region is chosen so that the peak doping concentration lies about 0.3 μm below the silicon surface. The polysilicon thickness must be sufficient to prevent the boron from penetration to the silicon surface during this process. The maximum concentration for the P^+ shielding region is limited to about $1 \times 10^{18}/cm^3$ to prevent significant contribution to the channel doping concentration. This is sufficient in magnitude to reduce the resistance of the base region for obtaining excellent ruggedness in the power SC-MOSFET structure because the P^+ shielding region extends below the entire length of the N^+ source region. The energy for the N-type dopant (phosphorus) used to form the JFET region is chosen so that its peak lies at the same depth as the P^+ shielding region. Its maximum doping concentration is chosen based upon a trade-off between reducing the JFET resistance contribution and shielding the P-base region from the drain potential.

The current flow pattern in the power SC-MOSFET structure is indicated by the shaded area in Fig. 4.2. In the model for the specific on-resistance, it will be assumed that the JFET region extends to the bottom of the P^+ shielding region. In the model, it is assumed that the current spreads at a 45° angle in the drift region. Due to the small size of the polysilicon window in the power SC-MOSFET structure, the current flow pattern overlaps for a part of the drift region similar to the case of the power U-MOSFET structure. The current is uniformly distributed in the N^+ substrate.

4.2.1 Channel Resistance

The contribution to the specific on-resistance from the channel in the SC-MOSFET structure is smaller than in the power D-MOSFET and U-MOSFET structures due to the shorter channel length. Based up on the analysis in the textbook [3] for the power D-MOSFET structure, the specific on-resistance contributed by the channel in the power SC-MOSFET structure is given by:

$$R_{CH,SP} = \frac{L_{CH} W_{Cell}}{2\mu_{ni} C_{OX}(V_G - V_{TH})} \tag{4.2}$$

In the case of the 30-V power MOSFET structures used for power supply applications, it is customary to provide the on-resistance at a gate bias of 4.5 and 10 V. Assuming a gate oxide thickness is 500 Å, an inversion layer mobility of 450 cm^2/V s (to match the mobility used in the numerical simulations discussed later in this section), and a threshold voltage of 2.5 V in the above equation for the power SC-MOSFET design with a cell width of 3 μm and gate electrode width of 1 μm, the specific resistance contributed by the channel at a gate bias of 4.5 V is found to be 0.039 mΩ cm^2. The specific on-resistance of the SC-MOSFET structure is reduced to 0.010 mΩ cm^2 when the gate bias is increased to 10 V. These values are much smaller than those for the power D-MOSFET and U-MOSFET structures due to the combination of a very short channel length and a small cell pitch.

4.2.2 Accumulation Resistance

In the power MOSFET structure, the current flowing through the inversion channel enters the drift region at the edge of the P-base junction. The current then spreads from the edge of the P-base junction into the JFET region. The current spreading phenomenon is aided by the formation of an accumulation layer in the semiconductor below the gate oxide due to the positive gate bias applied to turn-on the device. The specific on-resistance contributed by the accumulation layer in the power SC-MOSFET structure is given by the same formulation derived for the power D-MOSFET structure in the textbook [3]:

$$R_{A,SP} = K_A \frac{(W_G - 2x_{JP}) W_{Cell}}{4\mu_{nA} C_{OX}(V_G - V_{THA})} \tag{4.3}$$

In writing this expression, a coefficient K_A has been introduced to account for the current spreading from the accumulation layer into the JFET region. A typical value for this coefficient is 0.6 based upon the current flow observed from numerical simulations of power D-MOSFET structures. The threshold voltage (V_{THA}) in the

expression is for the on-set of formation of the accumulation layer. A zero threshold voltage will be assumed here when performing the analytical computations. Note that the junction depth of the P-base region (and not the P^+ region) defines the length of the accumulation region.

For the 30-V power SC-MOSFET design with a cell width of 3 μm and gate width of 1 μm, the specific resistance contributed by the accumulation layer at a gate bias of 4.5 V is 0.0078 mΩ cm^2 if the P-base junction depth (x_{JP}) is 0.235 μm and the gate oxide thickness is 500 Å. An accumulation layer mobility of 1,000 cm^2/V s was used in this calculation to match the mobility used in the numerical simulations (discussed later in this section). When the gate bias is increased to 10 V, the specific resistance contributed by the accumulation layer is reduced to 0.0035 mΩ cm^2. These values are also much smaller than those for the power D-MOSFET and U-MOSFET structures due to the combination of a short accumulation layer length and a small cell pitch.

4.2.3 JFET Resistance

The electrons entering from the channel into the drift region are distributed into the JFET region via the accumulation layer formed under the gate electrode. The spreading of current in this region was accounted for by using a constant K_A of 0.6 for the accumulation layer resistance. Consequently, the current flow through the JFET region can be treated with a uniform current density. In the power SC-MOSFET structure, the cross-sectional area for the JFET region is the smallest at the depth at which the P^+ shielding region has its highest concentration. Consequently, this width will be used for the analytical model in order to simplify the analysis by using a uniform cross-section for the current flow with a width 'a' for the JFET region as illustrated by the shaded area in Fig. 4.2. The width of the current flow is related to the device structural parameters:

$$a = (W_G - 2x_{JP+L} - 2W_0) \tag{4.4}$$

where W_0 is the zero-bias depletion width for the JFET region, and x_{JP+L} is the lateral extension of the P^+ shielding region under the gate electrode. The depletion region boundary is indicated in the figures with the dashed lines. In the models, it is assumed that no current can flow through the depleted region because all the free carriers have been swept out by the prevailing electric field across the junction. The zero-bias depletion width (W_0) in the JFET region can be computed by using the doping concentrations on both sides of the junction:

$$W_0 = \sqrt{\frac{2\varepsilon_S N_A V_{bi}}{qN_{DJ}(N_A + N_{DJ})}} \tag{4.5}$$

where N_A is the doping concentration in the P^+ shielding region and N_{DJ} is the doping concentration in the JFET region. In the above equation, the built-in

potential is also related to the doping concentrations on both sides of the junction:

$$V_{bi} = \frac{kT}{q} \ln\left(\frac{N_A N_{DJ}}{n_i^2}\right) \tag{4.6}$$

Since the JFET region is assumed to extend to the bottom the P^+ shielding region, the specific on-resistance contributed by the JFET region in the power SC-MOSFET structure can then be obtained by using:

$$R_{JFET,SP} = \frac{\rho_{JFET} x_{JP+} W_{Cell}}{(W_G - 2x_{JP+L} - 2W_0)} \tag{4.7}$$

where ρ_{JFET} is the resistivity of the JFET region given by:

$$\rho_{JFET} = \frac{1}{q\mu_n N_{DJ}} \tag{4.8}$$

where μ_n is the bulk mobility appropriate to the doping level of the JFET region. In the power SC-MOSFET structure, the JFET region has a retrograde doping profile with its maximum concentration (typically $1.5 \times 10^{17}/cm^3$) at the same depth as the P^+ shielding region. In an analytical model, it is convenient to use an average doping concentration for the JFET region which is slightly less than its peak doping concentration. The resistivity for the JFET region is then found to be 0.066 Ω cm corresponding to an average JFET doping concentration of $1.3 \times 10^{17}/cm^3$. The zero-bias depletion width in the JFET region for this JFET doping concentration is 0.0935 μm. For the 30-V power SC-MOSFET design with a cell width of 3 μm and gate width of 1 μm, the specific resistance contributed by the JFET region is found to be 0.042 mΩ cm^2 based up on using the above parameters. This value is much smaller than that for the power D-MOSFET structure due to the short cell pitch.

4.2.4 Drift Region Resistance

The resistance contributed by the drift region in the power SC-MOSFET structure is enhanced above that for the ideal drift region due to current spreading from the JFET region. The cross-sectional area for the current flow in the drift region increases from the width 'a' of the JFET region as illustrated in Fig. 4.2 at a spreading angle of 45°. Due to the small polysilicon window size in the power SC-MOSFET structure, the current paths overlap in the drift region.

The specific on-resistance contributed by the drift region in the power SC-MOSFET structure is given by the expression derived in the textbook [3] for high voltage D-MOSFET structures:

$$R_{D,SP} = \frac{\rho_D W_{Cell}}{2} \ln\left[\frac{W_{Cell}}{a}\right] + \rho_D \left(t - \frac{a}{2} - \frac{W_{Cell}}{2}\right) \tag{4.9}$$

For the parameters given above for this structure, the dimension 'a' in the equation is found to be 0.283 μm. For the 30-V power SC-MOSFET design with a cell width of 3 μm and gate width of 1 μm, the specific resistance contributed by the drift region is then found to be 0.1465 mΩ cm^2 by using a resistivity of the drift region of 0.325 Ω cm based upon a doping concentration of $1.6 \times 10^{16}/cm^3$.

4.2.5 Total On-Resistance

The total specific on-resistance for the power SC-MOSFET structure can be computed by adding all the above components for the on-resistance. For the case of the 30-V power SC-MOSFET design with a cell pitch (W_{Cell}) of 3 μm and gate width of 1 μm, the total specific on-resistance is found to be 0.235 mΩ cm^2 at a gate bias of 4.5 V and 0.202 mΩ cm^2 at a gate bias of 10 V by using the analytical model. The contributions from each of the components of the on-resistance are summarized in Fig. 4.3. The specific on-resistance for the power SC-MOSFET structure is found to be smaller than that for the power D-MOSFET and the U-MOSFET structures at a gate bias of 4.5 V.

The ideal specific on-resistance for a drift region is given by:

$$R_{IDEAL,SP} = \frac{W_{PP}}{q\mu_n N_D} \tag{4.10}$$

where W_{PP} is the parallel-plane depletion width at breakdown, N_D is the doping concentration of the drift region to sustain the blocking voltage, and μ_n is the mobility for electrons corresponding to this doping concentration. For the case of a blocking voltage of 30 V, the depletion width and doping concentration are found to be $2.2 \times 10^{16}/cm^3$ and 1.4 μm, respectively. Using the electron mobility for this doping level, the ideal specific on-resistance is found to be 0.034 mΩ cm^2. Since the device is constrained by the impact of an 80% reduction of breakdown voltage due to the edge termination, it is worth computing the ideal specific on-resistance for this case for comparison with the device. For the case of a blocking voltage of 37.5 V, the depletion width and doping concentration are found to be $1.6 \times 10^{16}/cm^3$ and 1.8 μm, respectively. Using the electron mobility for this doping level, the ideal

Resistance	V_G = 4.5 V (mΩ-cm^2)	V_G = 10 V (mΩ-cm^2)
Channel ($R_{CH,SP}$)	0.039	0.010
Accumulation ($R_{A,SP}$)	0.0078	0.0035
JFET ($R_{JFET,SP}$)	0.042	0.042
Drift ($R_{D,SP}$)	0.1465	0.1465
Total ($R_{T,SP}$)	0.235	0.202

Fig. 4.3 On-resistance components within the 30-V power SC-MOSFET structure

specific on-resistance is found to be 0.059 mΩ cm^2. In spite of its planar gate topology, the specific on-resistance for the SC-MOSFET structure is much closer to these ideal specific on-resistances than the power D-MOSFET and the U-MOSFET structures for the gate bias of 4.5 V.

4.2.5.1 Simulation Results

The results of two-dimensional numerical simulations on the 30-V power SC-MOSFET structure are described here to provide a more detailed understanding of the underlying device physics and operation. The structure used for the numerical simulations had a drift region thickness of 2.6 μm below the P^+ shielding region with a doping concentration of $1.6 \times 10^{16}/cm^3$. The P-base region and N^+ source regions had depths of 0.235 and 0.075 μm, respectively. The P^+ shielding region had a depth of 0.60 μm with its peak doping concentration located at 0.30 μm below the silicon surface. The doping concentration in the JFET region was enhanced by using a retrograde n-type doping profile with a peak concentration of $1.5 \times 10^{17}/cm^3$ with a depth of 0.3 μm. For the numerical simulations, half the cell (with a width of 1.5 μm) shown in Fig. 4.1 was utilized as a unit cell that is representative of the structure.

A three dimensional view of the doping distribution in the SC-MOSFET structure is shown in Fig. 4.4 from the left hand edge of the structure to the center of the

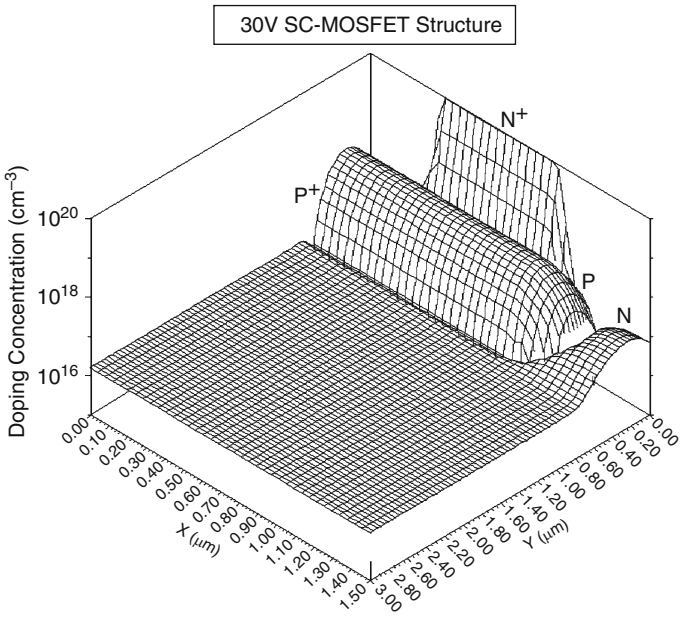

Fig. 4.4 Doping distribution for the SC-MOSFET structure

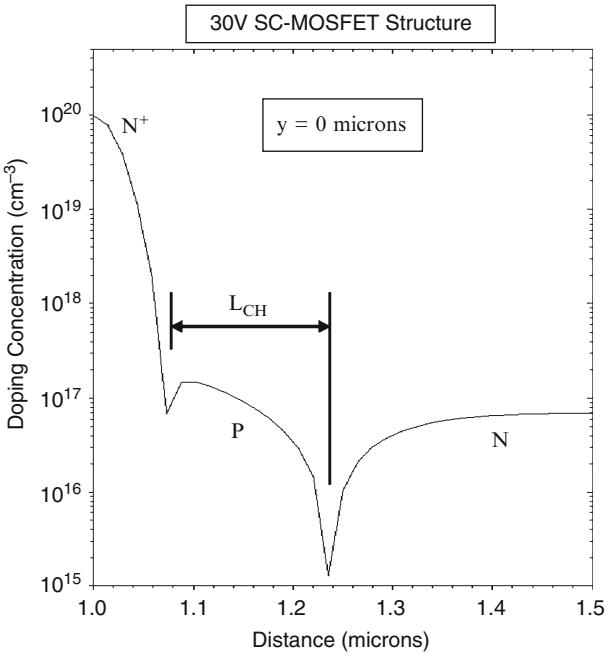

Fig. 4.5 Channel doping profile for the SC-MOSFET structure

polysilicon gate region. The N^+ source, P-base, and P^+ shielding regions are all aligned to the gate edge, which is located at 1 μm from the left hand side. The enhancement of the doping in the N-drift region near the surface is due to the additional JFET doping which can be observed to have a retrograde profile.

The lateral doping profile taken along the surface under the gate electrode is shown in Fig. 4.5. From the profile, it can be observed that the doping concentration of the JFET region has been increased to $7 \times 10^{16}/cm^3$ at the surface due to the additional doping from the N-type ion-implant. The lateral extensions of the P-base and N^+ source regions under the gate electrode are 0.235 and 0.075 μm leading to a channel length of only 0.16 μm. The surface concentration for the P-base region was chosen to obtain a maximum compensated P-type doping concentration in the channel of about $1.5 \times 10^{17}/cm^3$.

The vertical doping profile taken at two positions within the power SC-MOSFET structure are provided in Fig. 4.6. From the profile taken at $\times = 0$ μm in the middle of the polysilicon window (dashed line), it can be observed that the doping concentration of the P^+ shielding region has a maximum value of $9 \times 10^{17}/cm^3$ at a depth of 0.3 μm. The JFET region doping profile is shown by the solid line at the middle of the gate electrode ($\times = 1.5$ μm). It can be observed that the doping concentration of the JFET region has a maximum value of $1.5 \times 10^{17}/cm^3$ at a depth of 0.3 μm.

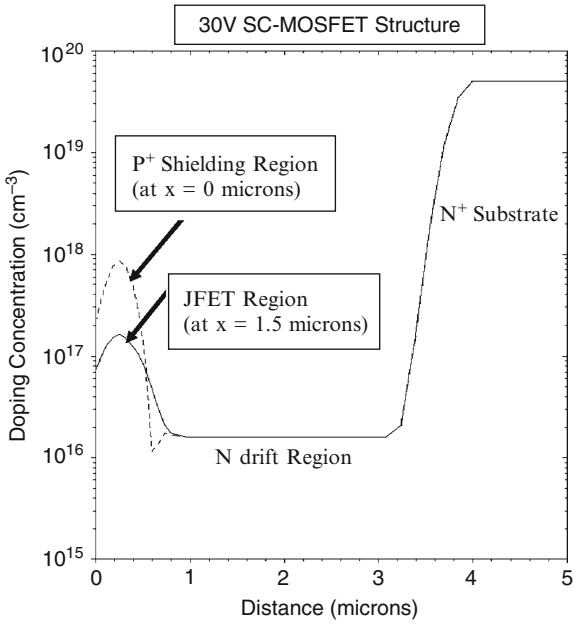

Fig. 4.6 Vertical doping profiles in the SC-MOSFET structure

In order to analyze the space between the P^+ shielding regions, the lateral doping profile under the gate electrode taken at a depth of 0.3 μm within the power SC-MOSFET structure is provided in Fig. 4.7. It can be observed that the P^+ shielding region extends to a distance of 0.265 μm from the edge of the gate electrode. This distance is larger than the extension of 0.235 μm by the P-base region from the edge of the gate electrode. The larger extension of the P^+ shielding region provides the desired shielding of the surface under the gate oxide from the drain potential.

The transfer characteristics for the SC-MOSFET structure were obtained using numerical simulations with a drain bias of 0.1 V at 300 and 400°K. The resulting transfer characteristics are shown in Fig. 4.8. From this graph, a threshold voltage of 2.5 and 2.0 V can be extracted at 300 and 400°K, respectively. The threshold voltage decreases by 20% when the temperature increases similar that observed for the power D-MOSFET structure. The specific on-resistance can be obtained from the transfer characteristics at any gate bias voltage. For the case of a gate bias of 4.5 V and 300°K, the specific in-resistance is found to be 0.242 mΩ cm^2. For the case of a gate bias of 10 V and 300°K, the specific in-resistance is found to be 0.212 mΩ cm^2. These values are in very close agreement with the results obtained from the analytical model.

The on-state current flow pattern within the SC-MOSFET structure at a small drain bias of 0.1 V and a gate bias of 4.5 V is shown in Fig. 4.9. In the figure, the

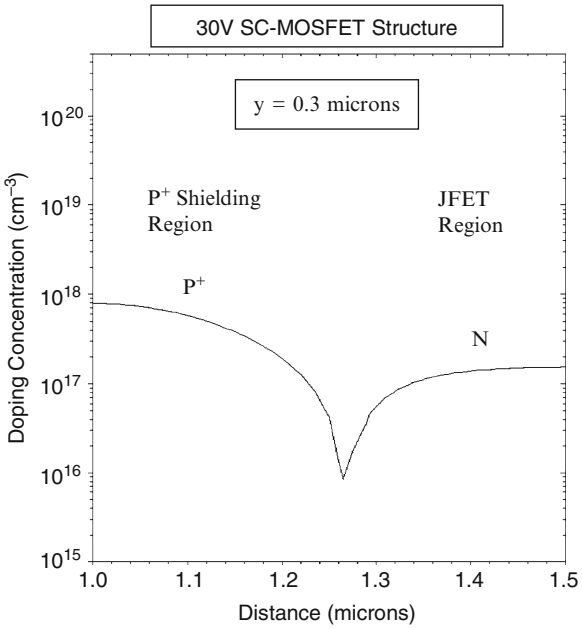

Fig. 4.7 Lateral doping profile in the SC-MOSFET structure

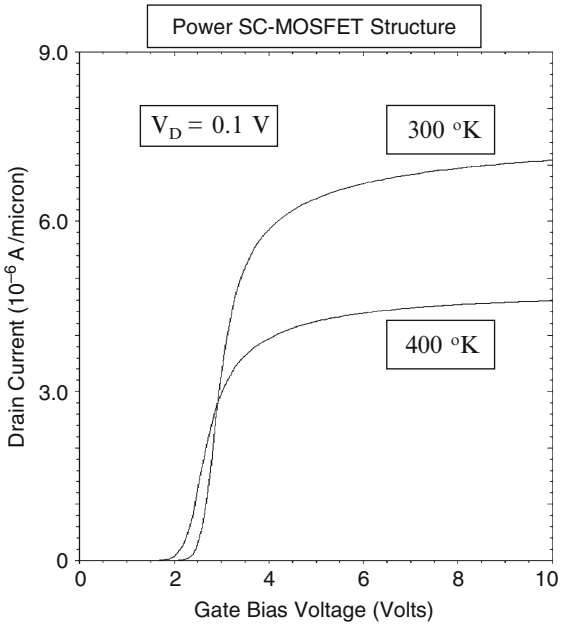

Fig. 4.8 Transfer characteristics of the SC-MOSFET structure

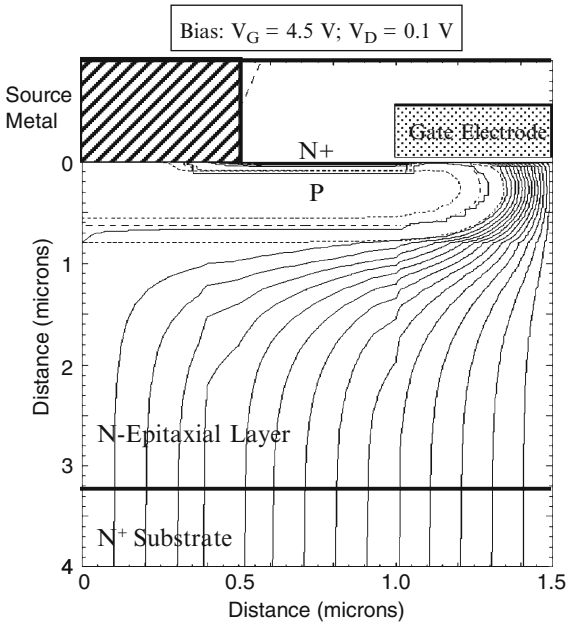

Fig. 4.9 Current distribution in the SC-MOSFET structure

depletion layer boundary is shown by the dotted lines and the junction boundary is delineated by the dashed line. The depletion layer width (W_0) in the JFET region is about 0.1 μm in good agreement with the value computed using the analytical model. It can be observed that the current flows from the channel and distributes into the JFET region via the accumulation layer. Within the JFET region, the cross-sectional area is approximately constant with a width (a/2) of 0.15 μm in good agreement with the assumptions used in the analytical model. From the figure, it can be seen that the current spreads from the JFET region to the drift region at a 45° angle as assumed in the models. Due to small polysilicon window size, the current flow becomes uniform at a depth of 2 μm for a portion of the drift region consistent with the analytical model.

In order to compare the on-resistance values extracted from the numerical simulations with those predicted by the analytical models, it is necessary to extract the mobility in the inversion and accumulation layers within the simulated D-MOSFET structure. The channel and accumulation layer mobility were extracted by simulation of a long channel lateral MOSFET structure with the same gate oxide thickness. The inversion layer mobility was found to be 450 cm^2/V s while that for the accumulation layer was found to be 1,000 cm^2/V s at a gate bias of 10 V. These values were consequently used in the analytical models when calculating the specific on-resistance.

4.3 Blocking Voltage

The power SC-MOSFET structure must be designed to support a high voltage in the first quadrant when the drain bias voltage is positive. During operation in the blocking mode, the gate electrode is shorted to the source electrode by the external gate bias circuit. The application of a positive drain bias voltage produces a reverse bias across junction J_1 between the P^+ shielding region and the N-drift region. Most of the applied voltage is supported across the N-drift region. The doping concentration of donors in the N-epitaxial drift region and its thickness must be chosen to attain the desired breakdown voltage. In the power D-MOSFET structure, the gate region is not screened from the drain bias due to cylindrical shape of the planar junctions. This results in significant depletion of the P-base region making the channel length of the structure large. In contrast, the P^+ shielding region in the power SC-MOSFET structure creates a potential barrier in the JFET region and screens the region under the gate electrode from the drain potential. The reduced potential at the upper surface allows reduction of the channel length without reach-through problems and also a reduces the electric field in the gate oxide enhancing the reliability.

4.3.1 Impact of Edge Termination

In practical devices, the maximum blocking voltage (BV) of the power MOSFET is invariably decided by the edge termination that surrounds the device cell structure. The most convenient edge termination for power SC-MOSFET devices is based up on floating field rings and field plates. With this design, the enhanced electric field at the edges limits the breakdown voltage to about 80% of the parallel-plane breakdown voltage (BV_{PP}):

$$BV_{PP} = \left(\frac{BV}{0.8}\right) \tag{4.11}$$

Consequently, the doping and thickness of the N-drift region must be chosen to achieve a parallel-plane breakdown voltage that is 25% larger than the blocking voltage for the device:

$$\mathrm{N_D} = \left(\frac{4.45 \times 10^{13}}{\mathrm{BV_{PP}}}\right)^{4/3} \tag{4.12}$$

The thickness of the drift region required below the P^+ shielding region is less than the depletion width for the ideal parallel-plane junction with the above doping concentration, and is given by:

$$t = W_D(BV) = \sqrt{\frac{2\varepsilon_S BV}{qN_D}} \tag{4.13}$$

The resistance of the drift region can be reduced by using this thickness rather than the maximum depletion width corresponding to the doping concentration given by (4.12).

4.3.1.1 Simulation Results

The results of two-dimensional numerical simulations on the 30-V power SC-MOSFET structure are described here to provide a more detailed understanding of the underlying device physics and operation during the blocking mode. The structure used for the numerical simulations had the same parameters as the structure described in the previous section. The blocking characteristic for the SC-MOSFET cell structure is shown in Fig. 4.10 at 300°K. It can be observed that the cell is capable of supporting 41 V. This provides enough margin to achieve a device blocking voltage capability of slightly over 30 V after accounting for the reduction due to the edge termination.

It is instructive to examine the potential contours inside the power SC-MOSFET structure when it is operating in the blocking mode. This allows determination of the voltage distribution within the structure and the penetration of the depletion region in the P-base region with increasing drain bias voltage. The potential contours for the SC-MOSFET structure obtained using the numerical simulations with zero gate bias and various drain bias voltages are shown in

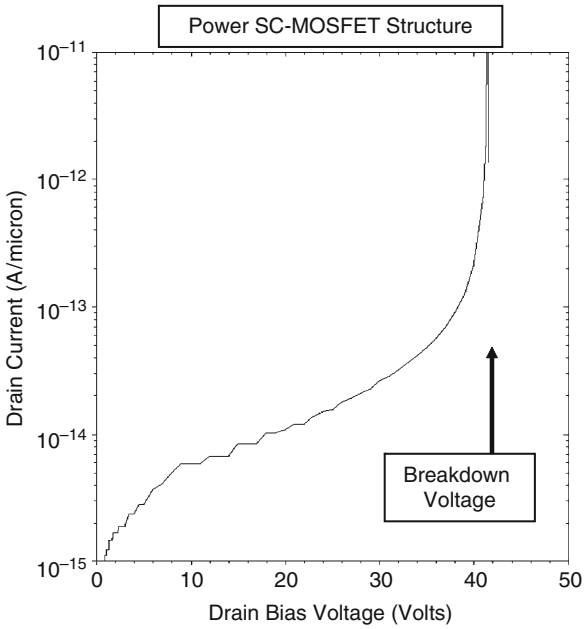

Fig. 4.10 Blocking characteristic for the SC-MOSFET structure

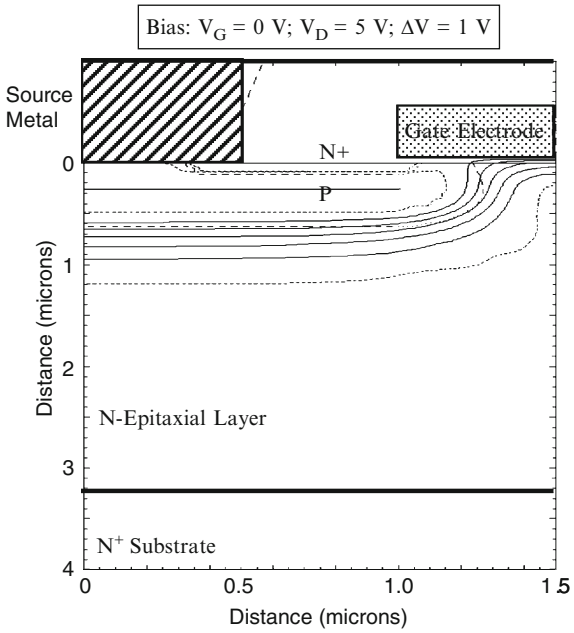

Fig. 4.11 Potential contours in the SC-MOSFET structure

Figs. 4.11–4.14. From these figures, it can be observed that the voltage distribution at the junction J_1 between the P^+ shielding region and the N-drift region changes when proceeding from the surface towards the drain. This indicates that the surface region is screened from the drain bias by the P^+ shielding region. Consequently, there is very little increase in the depletion of the P-base region when the drain bias is increased to 30 V. The screening phenomenon in the power SC-MOSFET structure allows utilization of a very short channel length which reduces the specific on-resistance.

It is insightful to also examine the electric field profile inside the power SC-MOSFET structure when it is operating in the blocking mode. The electric field profile obtained through the junction between the P^+ shielding region and the N- drift region is shown in Fig. 4.15. It can be observed that the maximum electric field occurs as expected at the junction at a depth of 0.6 μm from the surface.

The electric field profile taken through the middle of the gate electrode (at X = 1.5 μm) is provided in Fig. 4.16. It can be observed that the electric field exhibits a maximum below the surface at a depth of about 1 μm. This reduces the electric field at the surface under the gate oxide when compared with the power D-MOSFET and U-MOSFET structures. Further, the electric field in the gate oxide is much smaller than that observed in the power D-MOSFET and U-MOSFET structures. The low electric field in the gate oxide for the power SC-MOSFET structure indicates very reliable operation allowing stable device performance over long periods of time.

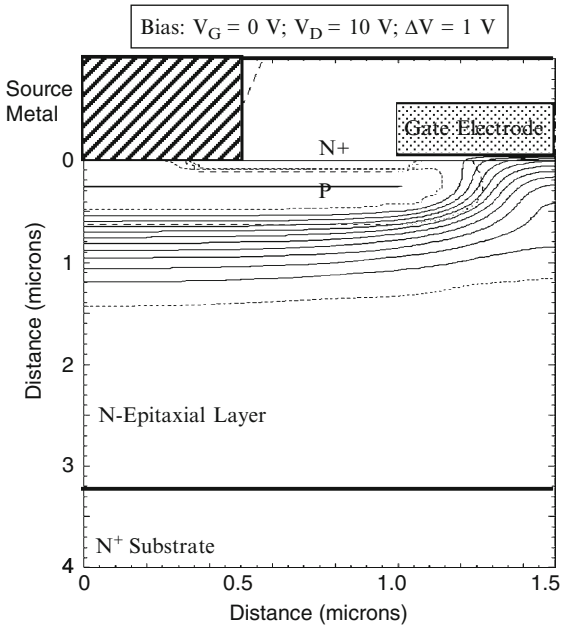

Fig. 4.12 Potential contours in the SC-MOSFET structure

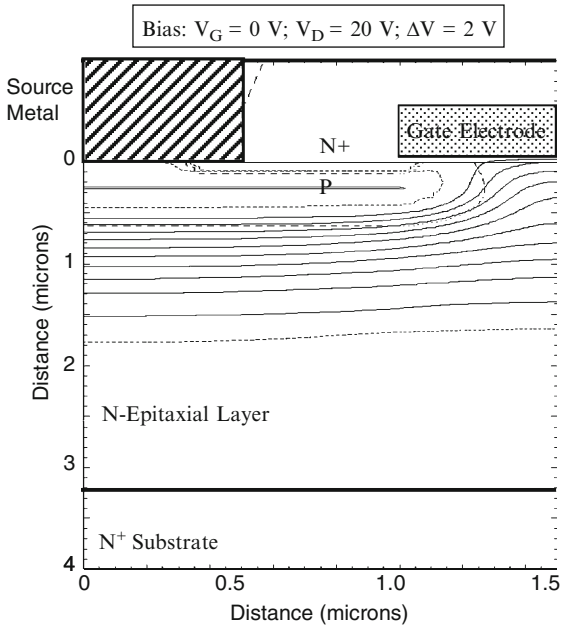

Fig. 4.13 Potential contours in the SC-MOSFET structure

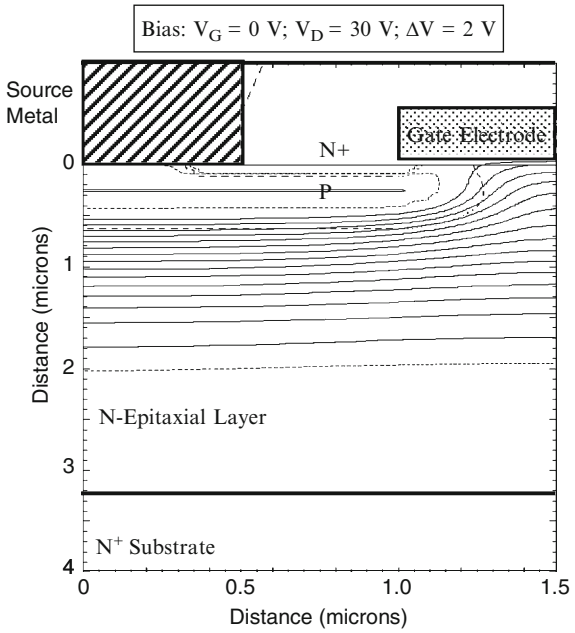

Fig. 4.14 Potential contours in the SC-MOSFET structure

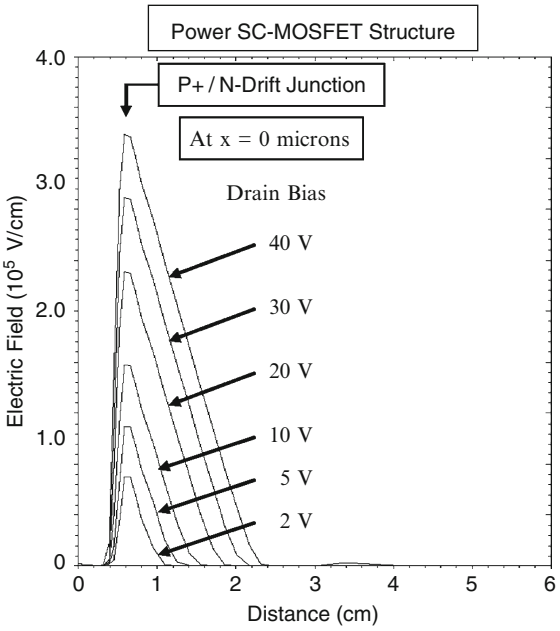

Fig. 4.15 Electric field distribution in the SC-MOSFET structure

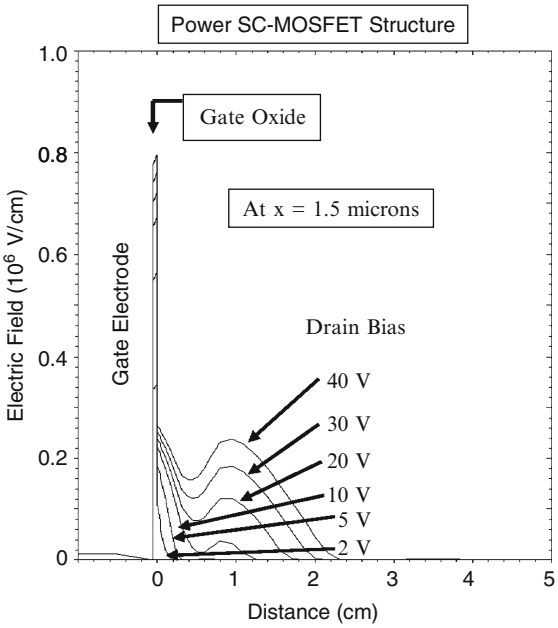

Fig. 4.16 Electric field distribution in the SC-MOSFET structure

4.4 Output Characteristics

The output characteristics of the power SC-MOSFET structure are important to the loci for the switching waveforms when it is operating in power circuits. Due to shielding of the P-base region, the power SC-MOSFET structure exhibits super-linear transfer characteristics [3]. The saturated drain current for the power SC-MOSFET structure is then given by:

$$I_{Dsat} = C_{ox}(V_G - V_T)\, v_{sat,n} Z \tag{4.14}$$

With sufficiently high doping concentration of the P-base region, the modulation of channel length can be made sufficiently small to ensure a high output resistance. In the power SC-MOSFET structure, the P^+ shielding region suppresses the depletion of the P-base region with increasing drain bias voltage. This is beneficial for obtaining a reasonable output resistance despite the very short channel length in the device. The short channel length in the power SC-MOSFET structure produces a high transconductance which is beneficial for reducing switching losses. The saturated drain current in the power SC-MOSFET structure increases linearly with the gate bias voltage.

4.4.1 Simulation Example

The output characteristics of the 30-V power SC-MOSFET structure were obtained by using two-dimensional numerical simulations using various gate bias voltages. All the device parameters used for these numerical simulations are the same as those used in the previous sections. The output characteristics of the power SC-MOSFET obtained using the simulations are shown in Fig. 4.17. The traces for increasing gate bias voltages are nearly uniformly spaced indicating super-linear [3] behavior of the transfer characteristics. When compared with the power D-MOSFET and U-MOSFET structures, the power SC-MOSFET structure exhibits a gradual transition from the on-state to the current saturation regime due to the voltage drop produced in the JFET region at high current densities.

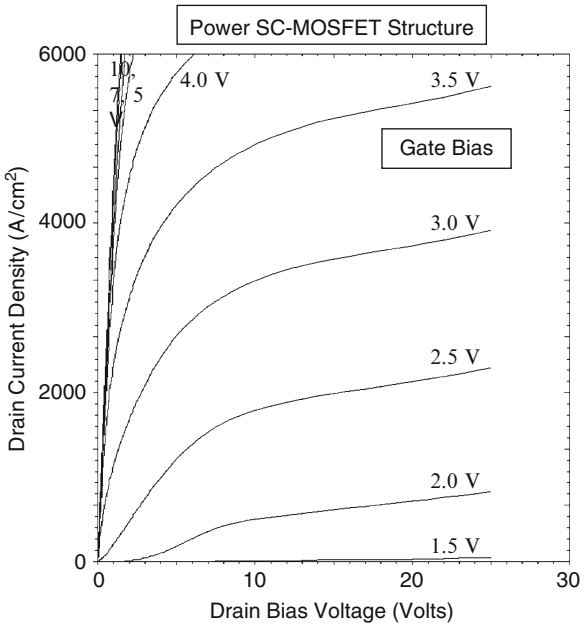

Fig. 4.17 Output characteristics for the power SC-MOSFET structure

4.5 Device Capacitances

For the power MOSFET structures, the switching speed is limited by the device capacitances in practical applications as previously discussed in Chap. 2. The rate at which the power MOSFET structure can be switched between the on- and off-states is determined by the rate at which the input capacitance can be charged or discharged. In addition, the capacitance between the drain and the gate electrodes

has been found to play an important role in determining the drain current and voltage transitions during the switching event.

The capacitances within the power SC-MOSFET structure can be analyzed using the same approach used in the textbook [3] for the power D-MOSFET structure. The specific input (or gate) capacitance for the power SC-MOSFET structure is given by:

$$C_{IN,SP} = C_{N+} + C_P + C_{SM} = \frac{2x_{JP}}{W_{Cell}}\left(\frac{\varepsilon_{OX}}{t_{OX}}\right) + \frac{W_G}{W_{Cell}}\left(\frac{\varepsilon_{OX}}{t_{IEOX}}\right) \tag{4.15}$$

where t_{OX} and t_{IEOX} are the thicknesses of the gate and inter-electrode oxides, respectively. The junction depth for the P-base region is much smaller in the power SC-MOSFET structure when compared with the power D-MOSFET structure resulting in a smaller input capacitance. For a 30-V power SC-MOSFET structure with a cell pitch (W_{CELL} in Fig. 4.2) of 3 μm and gate electrode width of 1 μm, the input capacitance is found to be 13 nF/cm^2 for a gate oxide thickness of 500 Å and an inter-metal dielectric thickness of 5,000 Å. This value is substantially smaller than 22 nF/cm^2 for the power D-MOSFET structure and 47 nF/cm^2 for the power U-MOSFET structure. This reduces the power requirements and losses in the gate drive circuit needed for the power SC-MOSFET structure.

The capacitance between the gate and drain electrodes (also called the reverse transfer capacitance) is determined by the width of the JFET region where the gate electrode overlaps the N-drift region. The MOS structure in this portion of the power SC-MOSFET structure operates under deep depletion conditions when a positive voltage is applied to the drain. As in the case of the power D-MOSFET structure, the gate-drain capacitance for the power SC-MOSFET structure is given by:

$$C_{GD,SP} = \frac{(W_G - 2x_{PL})}{W_{Cell}}\left(\frac{C_{OX}C_{S,M}}{C_{OX} + C_{S,M}}\right) \tag{4.16}$$

where $C_{S,M}$ is the semiconductor capacitance under the gate oxide, which decreases with increasing drain bias voltage. The specific capacitance of the semiconductor depletion region can be obtained by computation of the depletion layer width. The depletion layer width in the semiconductor under the gate oxide can be obtained using:

$$W_{D,MOS} = \frac{\varepsilon_S}{C_{OX}}\left\{\sqrt{1 + \frac{2V_D C_{OX}^2}{q\varepsilon_S N_{DJ}}} - 1\right\} \tag{4.17}$$

where N_{DJ} is the effective doping concentration of the semiconductor below the gate oxide for the retrograde doping profile. The specific capacitance for the semiconductor is then obtained using:

$$C_{S,M} = \frac{\varepsilon_S}{W_{D,MOS}} \tag{4.18}$$

The gate-drain (or reverse transfer) capacitance can be computed by using (4.18) with the above equations to determine the semiconductor capacitance as a function of the drain bias voltage.

However, in the case of the power SC-MOSFET structure, the above equation is only valid until the depletion region from the P^+ screening regions pinches-off the JFET region. Once this occurs, the gate-drain capacitance decreases drastically because the gate is screened from the drain. The drain voltage at which the JFET region is pinched-off is given by:

$$V_{P,JFET} = \frac{qN_{DJ,Peak}}{8\varepsilon_S}(W_G - 2x_{JP+L})^2 \tag{4.19}$$

where $N_{DJ,Peak}$ is the peak doping concentration for the retrograde doping profile.

For a typical power SC-MOSFET design with peak JFET region doping concentration ($N_{DJ,Peak}$) of $1.5 \times 10^{17}/cm^3$, gate width (W_G) of 1 μm, and P^+ screening region lateral junction depth of 0.265 μm, the JFET region pinch-off voltage is 6.4 V. The effective doping concentration for the JFET region in this case is $1.2 \times 10^{17}/cm^3$. After the JFET region is pinched-off, the gate-drain capacitance is determined by the edge of the depletion region located below the P^+ screening region. This distance below the gate oxide is given by:

$$W_S = x_{JP+} + \sqrt{\frac{2\varepsilon_S V_D}{qN_D}} \tag{4.20}$$

The specific capacitance for the semiconductor below the gate oxide can then be obtained using (4.18) with the width W_S. The specific gate transfer capacitance obtained by using the above analytical formulae is shown in Fig. 4.18 for the case of a power SC-MOSFET structure with 3 μm cell pitch, and polysilicon window of 2 μm. The gate-drain (reverse transfer) capacitance decreases gradually with increasing drain bias voltage due to the expansion of the depletion region in the semiconductor under the gate oxide until the drain bias reaches 6 V. Once the JFET region pinches-off at a drain bias of 6.3 V, the specific reverse transfer capacitance drops drastically which is beneficial for reducing the gate transfer charge. Despite this sharp reduction in the reverse transfer capacitance predicted by this model, the actual reverse transfer capacitance in devices is found to decrease to a much greater degree after the JFET region is pinched-off [4]. This effect can be accounted for by reducing the effective area for the gate region using a screening factor (K_S) as shown in Fig. 4.18.

The output capacitance for the power SC-MOSFET structure is associated with the capacitance of the junction between the P-base region and the N-drift region. Due to pinch-off of the JFET region with increasing drain bias voltage, it is necessary to examine the change in the depletion region boundary with applied voltage. The depletion layer boundary inside the power SC-MOSFET structure prior to the pinch-off of the JFET region is shown in Fig. 4.19 by the dashed lines. It can be observed that the depletion region has a vertical boundary inside the JFET

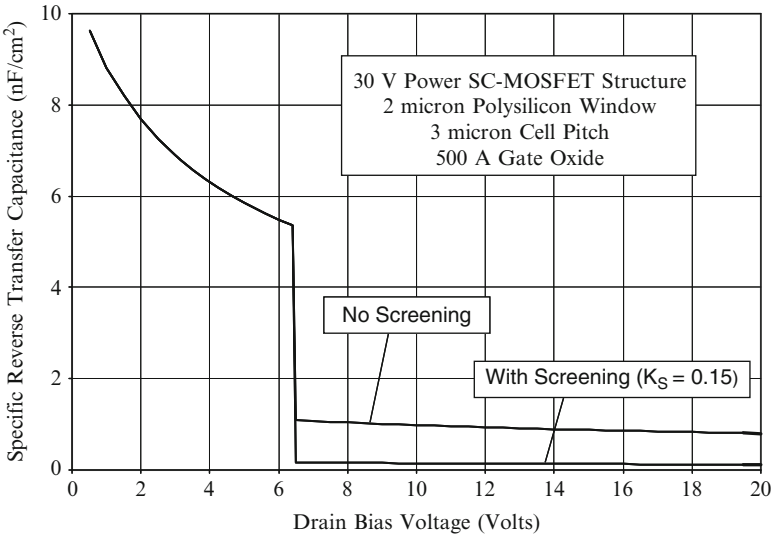

Fig. 4.18 Gate-drain capacitance for the power SC-MOSFET structure

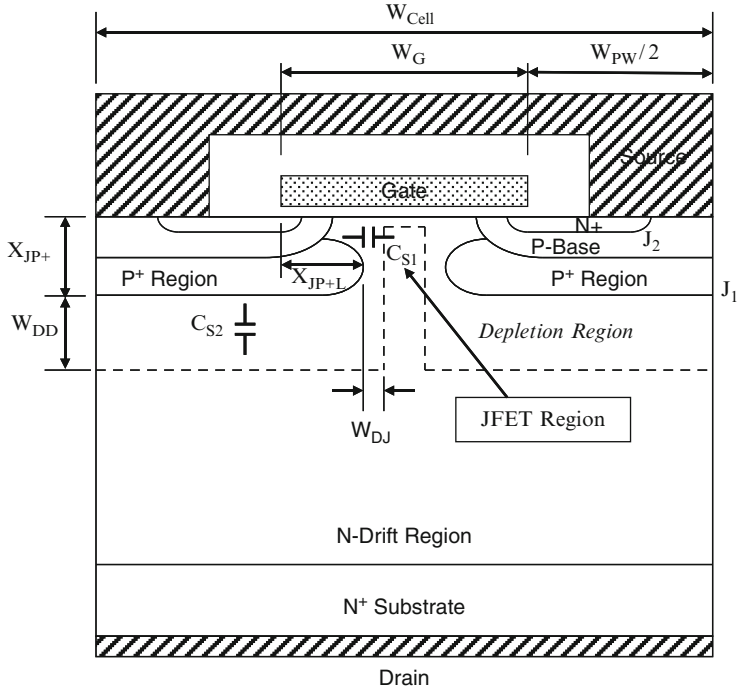

Fig. 4.19 Depletion region boundaries for determination of the output capacitance for the power SC-MOSFET structure

region and a horizontal boundary below the P^+ screening region. The capacitances associated with each of these regions are indicated in the figure as C_{S1} and C_{S2}. The specific junction capacitance associated with the JFET region is given by:

$$C_{S1,SP} = \frac{\varepsilon_S}{W_{DJ}} \left(\frac{2x_{JP+}}{W_{Cell}} \right) \tag{4.21}$$

where the depletion region thickness (W_{DJ}) in the JFET region is related to the drain bias voltage:

$$W_{DJ} = \sqrt{\frac{2\varepsilon_S (V_D + V_{bi})}{qN_{DJ}}} \tag{4.22}$$

where N_{DJ} is the average doping concentration of the JFET region. The specific junction capacitance associated with the bottom of the P^+ screening region is given by [3]:

$$C_{S2,SP} = \frac{\varepsilon_S}{W_{DD}} \left(\frac{W_{PW} + 2x_{JP+L}}{W_{Cell}} \right) \tag{4.23}$$

where the depletion region thickness (W_{DD}) in the drift region is related to the drain bias voltage:

$$W_{DD} = \sqrt{\frac{2\varepsilon_S (V_D + V_{bi})}{qN_D}} \tag{4.24}$$

where N_D is the doping concentration of the drift region.

The specific output capacitance for the power SC-MOSFET structure can then be obtained by combining the above values:

$$C_{O,SP} = C_{S1,SP} + C_{S2,SP} \tag{4.25}$$

The output capacitance obtained by using the above analytical model is shown in Fig. 4.20 for the case of the 30-V power SC-MOSFET structure with 3-μm cell pitch and polysilicon window of 2 μm. This structure has a gate oxide thickness of 500 Å and a lateral junction depth of 0.265 μm for the P^+ screening region. A built-in potential of 0.8 V was assumed for the P-base/N-drift junction, and the drift region has a doping concentration of $1.6 \times 10^{16}/cm^3$. An effective doping concentration of $1.2 \times 10^{17}/cm^3$ was assumed for the JFET region. The figure includes the contributions from the two components of the output capacitance. It can be observed that the specific output capacitance decreases with increasing drain bias voltage due to the expansion of the depletion region in the JFET region and under the P^+ screening region. At a drain bias of 6.4 V, the JFET region is pinched-off

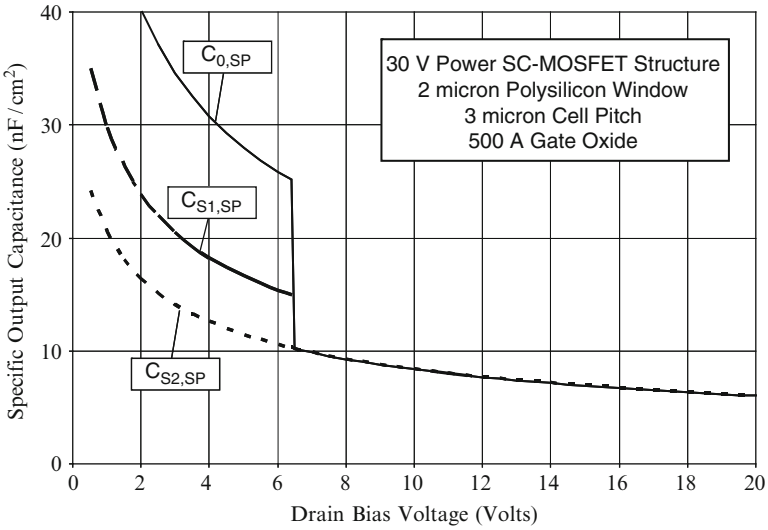

Fig. 4.20 Output capacitance for the power SC-MOSFET structure

resulting in the merging of the depletion regions in the JFET region. The output capacitance then reduces abruptly to that associated with the P^+ screening region. At a drain bias of 20 V, the specific output capacitance predicted by the analytical model for this structure is 6 nF/cm^2.

4.5.1 Simulation Example

The capacitances of the 30-V power SC-MOSFET structure were extracted using two-dimensional numerical simulations on the structure with device parameters described in the previous sections. The input capacitance was extracted by performing the numerical simulations with a small AC signal superposed on the DC gate bias voltage. The input capacitances obtained for the power SC-MOSFET structure are shown in Fig. 4.21 at a drain bias of 20 V. The input capacitance is comprised of two components – the first is between the gate electrode and the source electrode (C_{GS}) while the second is between the gate electrode and the base electrode (C_{GB}). The total input capacitance can be obtained by the addition of these capacitances because they are in parallel and share a common contact electrode in the actual power SC-MOSFET structure. From the figure, a total specific input capacitance of about 13 nF/cm^2 is observed at a gate bias of 4.5 V – close to that predicted by the analytical model.

The drain-gate (reverse transfer) capacitance can be extracted by performing the numerical simulations with a small AC signal superposed on the DC drain bias

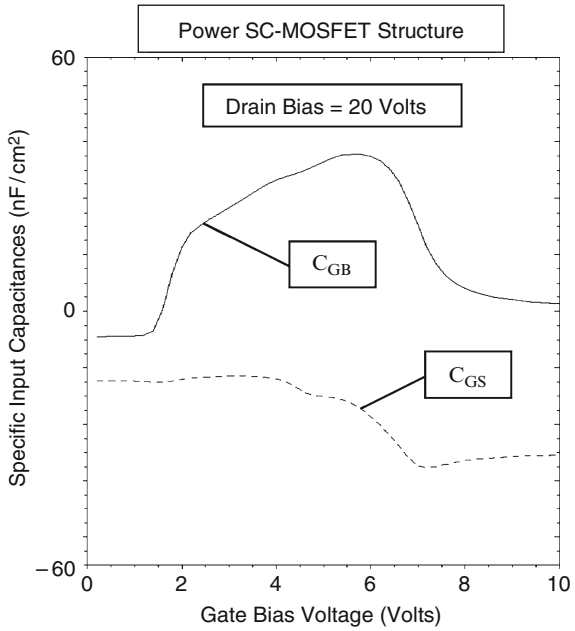

Fig. 4.21 Input capacitances for the SC-MOSFET structure

voltage. The values obtained for the 30-V power SC-MOSFET structure are shown in Fig. 4.22. The gate-to-drain and base-to-drain capacitances are shown in the figure for comparison. Both of these capacitances decrease with increasing drain bias voltage until about 7 V and then fall abruptly as expected from the analytical model based up on the pinch-off of the JFET region. It can be observed from this figure that the reverse transfer (gate-drain) capacitance becomes extremely small in magnitude when compared to the output (base-drain) capacitance for the power SC-MOSFET structure. This implies a greatly reduced feedback path between the drain and the gate electrodes which is beneficial to the switching speed and power loss for the power SC-MOSFET structure. The values for the reverse transfer and output capacitances obtained by using the analytical models are in good agreement with the simulation values. The reverse transfer capacitance for the power SC-MOSFET structure is also shown in Fig. 4.23 to provide a more detailed view of its small values at high drain bias voltages.

The extremely small reverse transfer capacitance for the power SC-MOSFET structure has been experimentally observed in the SSCFET products [4]. The datasheets also show the abrupt reduction of the reverse transfer and output capacitances after the drain bias increases beyond the pinch-off of the JFET region. The ten-times smaller ratio of the reverse transfer to the input capacitance for the SC-MOSFET structure when compared with the D-MOSFET and U-MOSFET structures provides strong immunity to [dV/dt] induced turn-on when the device is operated in VRM applications.

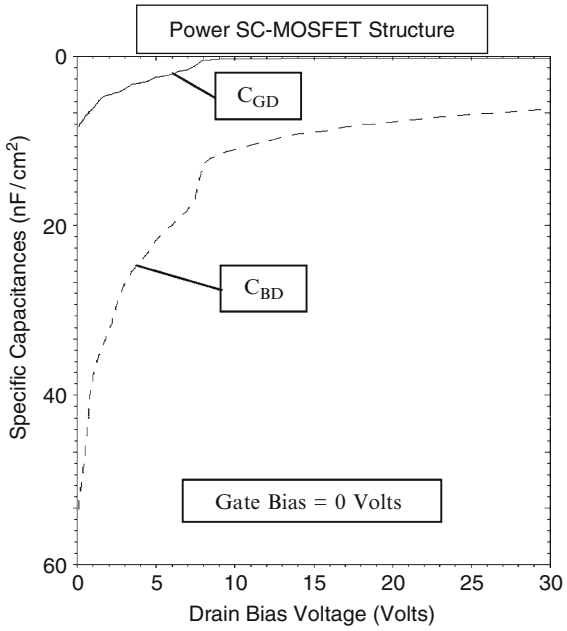

Fig. 4.22 Reverse transfer and output capacitances for the SC-MOSFET structure

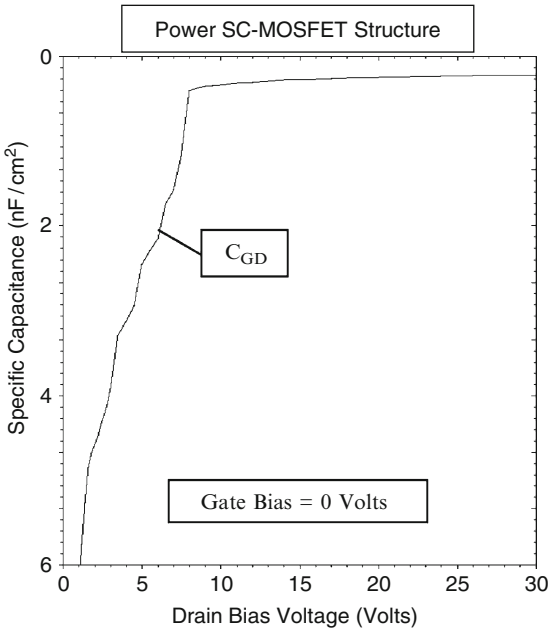

Fig. 4.23 Reverse transfer capacitance for the SC-MOSFET structure

4.6 Gate Charge

It is standard practice in the industry to provide the gate charge for power MOSFET structures as a measure of their switching performance. The gate charge can be extracted by the application of a constant current source at the gate terminal while turning-on the power MOSFET structure from the blocking state. The linearized current and voltage waveforms observed during the turn-on process are illustrated in Fig. 6.98 in the textbook [3]. The various components for the gate charge are also defined in this figure.

The gate charge components for the power SC-MOSFET structure are given by similar equations. However, adjustments must be made because the gate transfer capacitance for this device structure is close to zero during the transition from a drain bias of V_{DS} to the pinch-off voltage ($V_{P,JFET}$) for the JFET region. Due to the nearly zero gate transfer capacitance, an instantaneous drop in drain voltage from V_{DS} to $V_{P,JFET}$ can occur at the beginning of the gate plateau phase. After this, the gate transfer capacitance is given by (4.16) including the impact of the screening factor (K_S). The gate transfer charge corresponding to the transition where the drain voltage changes from $V_{P,JFET}$ to V_{ON} is given by:

$$Q_{GD} = \frac{2K_G q \varepsilon_S N_{DJ}}{C_{OX}} \left[\sqrt{1 + \frac{2V_{P,JFET} C_{OX}^2}{q\varepsilon_S N_{DJ}}} - \sqrt{1 + \frac{2V_{ON} C_{OX}^2}{q\varepsilon_S N_{DJ}}} \right] \tag{4.26}$$

The other components of the gate charge are similar to those already provided in the textbook:

$$Q_{SW} = Q_{GS2} + Q_{GD} \tag{4.27}$$

$$Q_G = [C_{GS} + C_{GD}(V_{DS})]V_{GP} + Q_{GD} + [C_{GS} + C_{GD}(V_{ON})](V_G - V_{GP}) \tag{4.28}$$

The gate charge values obtained for the 30-V power SC-MOSFET structure with source electrode in the trenches by using the above analytical equations are: $Q_{GD} = 90.4\ nC/cm^2$; $Q_{SW} = 92\ nC/cm^2$; and $Q_G = 333\ nC/cm^2$. The gate transfer charge for the power SC-MOSFET structure is much smaller than that for the power MOSFET structures discussed in the previous chapters. It can be concluded that the power SC-MOSFET structure is well suited for high frequency applications where both the specific on-resistance and switching losses must be optimized.

Equations for the gate voltage, drain current, and drain voltage waveforms obtained by using the analytical model are provided in the textbook [3]. However, the drain voltage waveform for the power SC-MOSFET structure must be reformulated because the gradual transition occurs from the pinch-off voltage for the JFET region to the on-state voltage drop. Due to the very small reverse transfer capacitance for the power SC-MOSFET structure at larger drain bias voltages, the drain

voltage first reduces abruptly from V_{DS} to $V_{P,JFET}$. After this, the drain voltage is determined by the gate transfer capacitance given by (4.16):

$$v_D(t) = \frac{q\varepsilon_S N_{DJ}}{2C_{OX}^2}\left\{\left[\sqrt{1+\frac{2V_{P,JFET}C_{Ox}^2}{q\varepsilon_S N_{DJ}}} - \frac{J_G C_{OX}(t-t_2)}{2K_G q\ \varepsilon_S N_{DJ}}\right]^2 - 1\right\} \tag{4.29}$$

from $t = t_2$ to $t = t_3$.

The waveforms obtained for the 30-V power SC-MOSFET structure – using 3-μm cell pitch, gate width of 1 μm, and a gate oxide thickness of 500 Å – using these equations are provided in Fig. 4.24. A gate drive current density of 0.67 A/cm^2 was

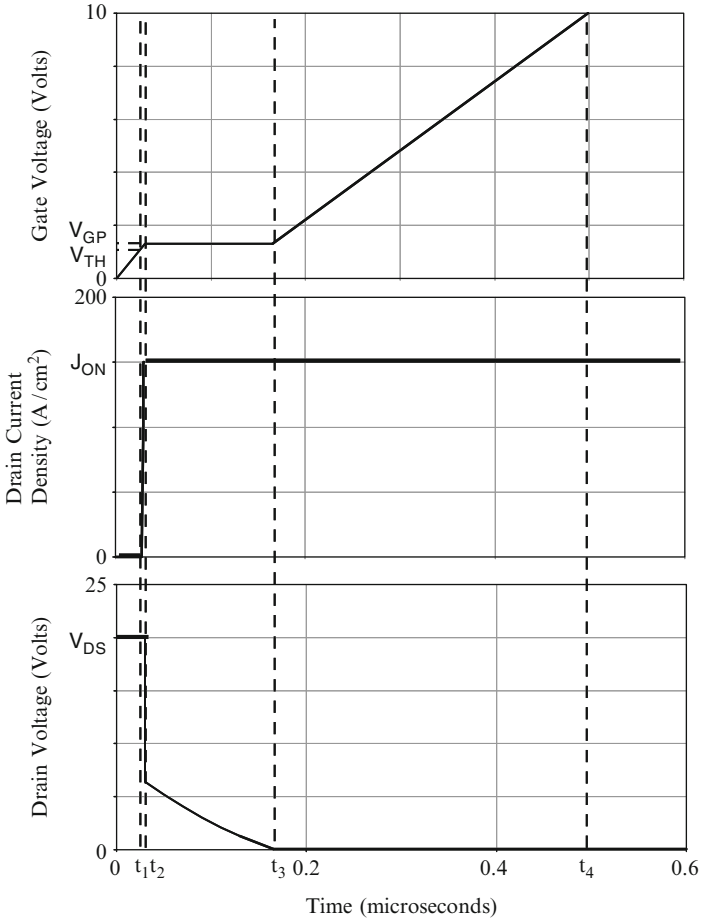

Fig. 4.24 Analytically computed waveforms for the 30-V power SC-MOSFET structure

used to turn on the device from a steady-state blocking voltage of 20 V to match the results of two dimensional numerical simulations discussed below. The specific input capacitance was assumed to be 15 nF/cm^2.

The gate voltage initially increases linearly with time. After reaching the threshold voltage, the drain current can be observed to increase very quickly because of the large transconductance for this device structure. The drain current density increases until it reaches an on-state current density of 150 A/cm^2. The on-state current density determines the gate plateau voltage which has a value of 1.31 V for a threshold voltage of 1.2 V at this drain bias. During the gate voltage plateau phase, the drain voltage drops abruptly from the drain supply voltage of 20 V to the JFET region depletion voltage of 6.4 V. The drain voltage then decreases in a non-linear manner until it reaches the on-state voltage drop. After this time, the gate voltage again increases but at a slower rate than during the initial turn-on phase due to the larger gate transfer capacitance.

4.6.1 Simulation Example

The gate charge for the 30-V power SC-MOSFET structure was extracted by using the results of two-dimensional numerical simulations of the cell described in the previous sections. The device was turned-on from blocking state with a drain bias of 20 V by driving it using a gate current of 1×10^{-8} A/μm (equivalent to 0.67 A/cm^2 for the area of 1.5×10^{-8} cm^2). Once the drain current density reached 150 A/cm^2, the drain current was held constant resulting in a reduction of the drain voltage. The gate plateau voltage for this drain current density was found to be 1.7 V. Once the drain voltage reached the on-state value corresponding to the gate plateau voltage, the gate voltage increased to the steady-state value of 10 V.

The gate charge waveforms obtained by using an input gate current density of 0.67 A/cm^2 when turning on the power SC-MOSFET structure from a blocking state with drain bias of 20 V are shown in Fig. 4.25. The on-state current density is 150 A/cm^2 at a DC gate bias of 10 V at the end of the turn-on transient. The gate voltage increases at a constant rate at the beginning of the turn-on process as predicted by the analytical model. When the gate voltage reaches the threshold voltage, the drain current begins to increase. The drain current increases very rapidly until it reaches the on-state current density of 150 A/cm^2.

Once the drain current reaches the on-state value, the gate voltage remains approximately constant at the plateau voltage (V_{GP}). The plateau voltage for this structure is 1.7 V for the drain current density of 150 A/cm^2 as governed by the transconductance of the device. The drain voltage drops abruptly from the supply voltage of 20 V of about 6.5 V (the JFET pinch-off voltage) as predicted by the analytical model. The drain voltage then decreases during the plateau phase in a non-linear manner. After the end of the plateau phase, the gate voltage again increases until it reaches the gate supply voltage. The waveforms obtained using

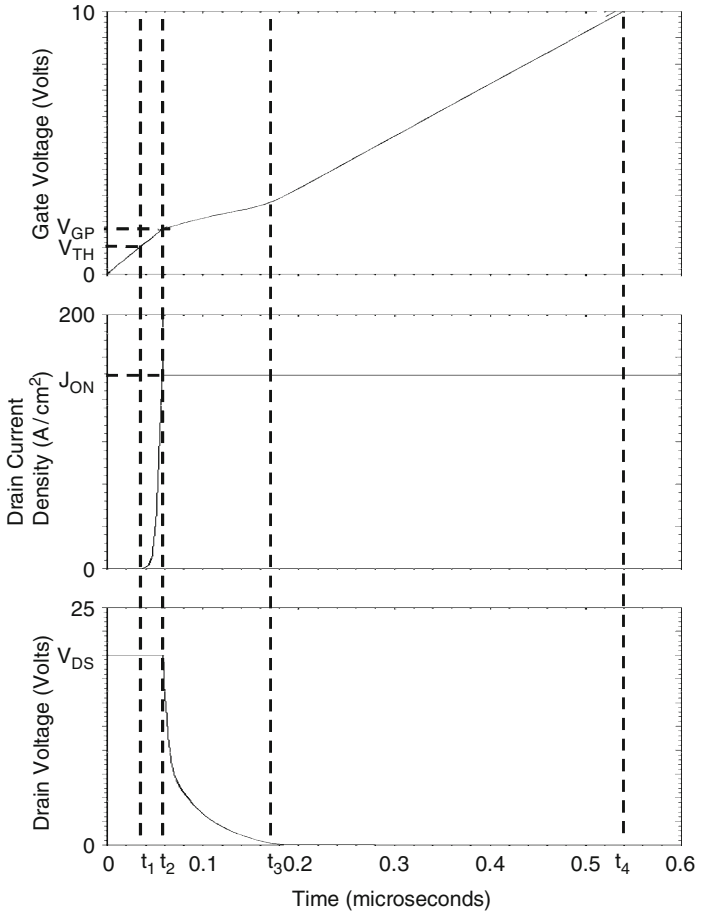

Fig. 4.25 Turn-on waveforms for the 30-V power SC-MOSFET structure

the numerical simulations show a significant increase in the gate voltage during the plateau phase of the waveform. This indicates a reduction of the transconductance of the SC-MOSFET structure as the drain voltage is decreasing from 20 V to the on-state voltage drop. This change in transconductance with drain bias is evident in the output characteristics previously shown in Fig. 4.17.

The values for the various components of the gate charge extracted from the numerical simulations are compared with those calculated by using the analytical model in Fig. 4.26. There is excellent agreement between these values indicating that the analytical model is a good representation of the physics of turn-on for power SC-MOSFET structure. It can be concluded from these gate charge values that the SC-MOSFET structure has much superior switching performance when compared with the D-MOSFET and U-MOSFET structures.

Specific Gate Charge	Numerical Simulation (nC/cm^2)	Analytical Model (nC/cm^2)
Q_{GS1}	23	18.1
Q_{GS2}	16	1.6
Q_{GS}	39	19.8
Q_{GD}	73	90.4
Q_{SW}	89	92.0
Q_G	360	332.7

Fig. 4.26 Gate charge extracted from numerical simulations for the power SC-MOSFET structure

4.7 Device Figures of Merit

Significant power switching losses can arise from the charging and discharging of the large input capacitance in power MOSFET devices at high frequencies. The input capacitance (C_{IN}) of the power MOSFET structure must be charged to the gate supply voltage (V_{GS}) when turning on the device and then discharged to 0 V when turning off the device during each period of the operating cycle. The total power loss can be obtained by summing the on-state power dissipation for a duty cycle $\delta = t_{ON}/T$ and the switching power losses:

$$P_T = P_{ON} + P_{SW} = \delta R_{ON} I_{ON}^2 + C_{IN} V_{GS}^2 f \tag{4.30}$$

where R_{ON} is the on-resistance of the power MOSFET structure, I_{ON} is the on-state current, and f is the operating frequency. In writing this equation, the switching power losses due to the drain current and voltage transitions has been neglected. A minimum total power loss occurs for each power MOSFET structure at an optimum active area as shown in the textbook [3]. The on-state and switching power losses are equal at the optimum active area. The optimum active area at which the power dissipation is minimized is given by:

$$A_{OPT} = \sqrt{\frac{R_{ON,sp}}{C_{IN,sp}}} \left(\frac{I_{ON}}{V_{GS}}\right) \left(\sqrt{\frac{\delta}{f}}\right) \tag{4.31}$$

From the first term in this expression, a useful technology figure-of-merit can be defined:

$$FOM(A) = \frac{R_{ON,sp}}{C_{IN,sp}} \tag{4.32}$$

In the power electronics community, there is trend towards increasing the operating frequency for switch mode power supplies in order to reduce the size and weight of the magnetic components. The ability to migrate to higher operating frequencies in power conversion circuits is dependent on making enhancements to the power MOSFET technology. From the above equations, an expression for the minimum total power dissipation can be obtained [3]:

$$P_T(\min) = 2I_{ON}V_{GS}\sqrt{\delta R_{ON,sp}C_{IN,sp}f} \tag{4.33}$$

A second technology figure of merit related to the minimum power dissipation can be defined as:

$$FOM(B) = R_{ON,sp}C_{IN,sp} \tag{4.34}$$

In most applications for power MOSFET structures with high operating frequency, the switching losses associated with the drain current and voltage transitions become a dominant portion of the total power loss. The time period associated with the increase of the drain current and decrease of the drain voltage is determined by the charging of the device capacitances. It is therefore common practice in the industry to use the following figures-of-merit to compare the performance of power MOSFET products [3]:

$$FOM(C) = R_{ON,sp}Q_{GD,sp} \tag{4.35}$$

and

$$FOM(D) = R_{ON,sp}Q_{SW,sp} \tag{4.36}$$

Although FOM(D) encompasses both the drain current and voltage transitions, it is customary to use FOM(C) because the gate-drain charge tends to dominate in the switching gate charge. One advantage of using these expressions is that the figure-of-merit becomes independent of the active area of the power MOSFET device.

The figures of merit computed for the power SC-MOSFET structure discussed in earlier sections of this chapter are provided in Fig. 4.27. The figure of merit usually

Figures of Merit	V_G = 4.5 V	V_G = 10 V
FOM(A) ($\Omega^2cm^4s^{-1}$)	18,080	15,500
FOM(B) (ps)	3.06	2.63
FOM(C) ($m\Omega^*nC$)	21.2	18.2
FOM(D) ($m\Omega^*nC$)	21.5	18.5

Fig. 4.27 Figures of merit for the power SC-MOSFET structure

used for comparison of device technologies in the literature is FOM(C). Most often, the value for this figure of merit at a gate bias of 4.5 V is utilized for selection of devices in the voltage regulator module application. In comparison with the power D-MOSFET structure (see Chap. 2), the power SC-MOSFET structure has a FOM (C) that is 14-times smaller. In comparison with the conventional power U-MOSFET structure (see Chap. 3), the power SC-MOSFET structure has a FOM(C) that is 5.7-times smaller. In comparison with the power U-MOSFET structure with thicker oxide at the trench bottom surface (see Chap. 3), the power SC-MOSFET structure has a FOM(C) that is 4.8-times smaller. Consequently, the power SC-MOSFET structure offers significant improvement in circuit performance while utilizing a simple planar fabrication process.

4.8 Discussion

The physics of operation and resulting electrical characteristics of the power SC-MOSFET structure have been described in this chapter. The specific on-resistance for this device structure is significantly reduced when compared with the power D-MOSFET structure due to its very short (shielded) channel length, enhanced doping concentration in the JFET region using a retrograde doping profile, and small cell pitch. The specific on-resistance for the power SC-MOSFET structure is comparable to that of the power U-MOSFET structure. In addition, the reverse transfer capacitance and gate charge for the power SC-MOSFET structure are much smaller than those for the power D-MOSFET and U-MOSFET structures. Consequently, the figure-of-merit FOM(C) for the power SC-MOSFET structure is superior to that for the power D-MOSFET and U-MOSFET structures. The commercially developed devices [4] have been found to exhibit the characteristics described in this chapter using analytical models and numerical simulations. They have been found to improve the efficiency of Voltage-Regulator-Modules by over 5% especially under higher operating frequencies.

For purposes of comparison with the power MOSFET structures discussed in subsequent chapters, the analysis of the power SC-MOSFET structure is provided here for a broad range of blocking voltages. In this analysis, the power SC-MOSFET structure was assumed to have the following parameters: (a) N^+ source junction depth of 0.075 μm; (b) P-base junction depth of 0.235 μm; (c) P^+ region junction depth of 0.6 μm; (d) gate oxide thickness of 500 Å; (e) polysilicon window width of 2 μm; (f) JFET region doping concentration of $1.3 \times 10^{17}/cm^3$; (g) threshold voltage of 2 V; (h) gate drive voltage of 10 V; (i) inversion mobility of 450 cm^2/V s; (j) accumulation mobility of 1,000 cm^2/V s. The contributions from the contacts and the N^+ substrate were neglected during the analysis. The doping concentration and thickness of the drift region were determined under the assumption that the edge termination (in conjunction with the graded junction doping profiles) limits the breakdown voltage to 90% of the parallel-plane breakdown voltage. The device parameters pertinent to each blocking voltage are provided in

Fig. 4.28. It can be observed that the doping concentration must be greatly reduced with increasing blocking voltage capability while simultaneously increasing the thickness of the drift region.

The gate electrode width was optimized for each breakdown voltage to achieve the minimum specific on-resistance in the power SC-MOSFET structure. The specific on-resistance obtained by using the analytical model for the power SC-MOSFET structure as a function of the width of the gate electrode is shown in Fig. 4.29 for the case of various breakdown voltages. Note that a logarithmic scale has been used for the vertical axis because of the large range of values for the specific on-resistance. The two zone model (see Fig. 6.41 in the textbook) was used

Blocking Voltage (V)	Drift Doping Concentration (cm^{-3})	Drift Region Thickness (microns)
30	1.6×10^{16}	3
60	6.0×10^{15}	5
100	3.0×10^{15}	8
200	1.2×10^{15}	17
300	6.8×10^{14}	26
600	2.7×10^{14}	58
1000	1.35×10^{14}	105

Fig. 4.28 Device parameters for the power SC-MOSFET structures

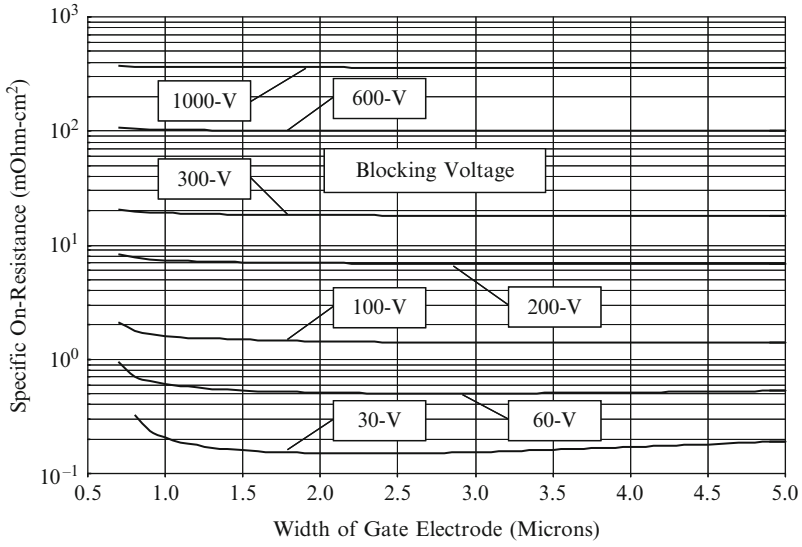

Fig. 4.29 Optimization of the specific on-resistance for the power SC-MOSFET structures

Blocking Voltage (V)	Optimum Gate Width (microns)	Specific On-Resistance (mΩ-cm^2)
30	2.2	0.149
60	2.8	0.503
100	3.5	1.40
200	4.8	6.83
300	5.9	18.0
600	8.2	99.6
1000	10.4	359

Fig. 4.30 Optimized specific on-resistance for the power SC-MOSFET structures

for all of the power SC-MOSFET structures because of the small width of the polysilicon window. From Fig. 4.29, it can be observed that the minimum specific on-resistance occurs at a larger optimum gate electrode width for the power SC-MOSFET structures with larger blocking voltages.

The optimum gate electrode width and minimum specific on-resistances for the power SC-MOSFET structures are provided in Fig. 4.30. The optimum gate electrode width for the power SC-MOSFET structures is much smaller than that for the power D-MOSFET structure due to the unique retrograde JFET region doping profile with much larger doping concentration. However, a small gate width (1 μm) is preferable for reducing the gate transfer charge. The specific on-resistance values for this case can be compared with the ideal specific on-resistance obtained by using Baliga's power law for the impact ionization coefficients in Fig. 4.31. From this figure, it can be concluded that the specific on-resistance for the SC-MOSFET structure is always larger than the ideal specific on-resistance. For blocking voltages below 60 V, the specific on-resistance for the power SC-MOSFET structure becomes substantially larger than the ideal case.

The specific gate transfer charge for the power SC-MOSFET structures was obtained by using the analytical model (see 4.26). During this analysis, the devices were assumed to be operated at an on-state current density that results in a power dissipation of 100 W/cm^2 as determined by the specific on-resistance for each device. The on-state current density values are provided in Fig. 4.32. The drain supply voltage used for this analysis was chosen to be two-thirds of the breakdown voltage. The drain supply voltage values are also provided in Fig. 4.32.

The specific gate transfer charge values calculated by using the analytical model for the power SC-MOSFET structure are given in Fig. 4.32 as a function of the breakdown voltage. These values are also plotted in Fig. 4.33 as a function of the breakdown voltage. It can be observed that the gate transfer charge decreases gradually with increasing breakdown voltage until a breakdown voltage of 300 V. The specific gate transfer charge then decreases drastically at higher breakdown voltages. This behavior occurs because the on-state voltage drop for the power SC-MOSFET begins to approach the pinch-off voltage for the JFET region as the

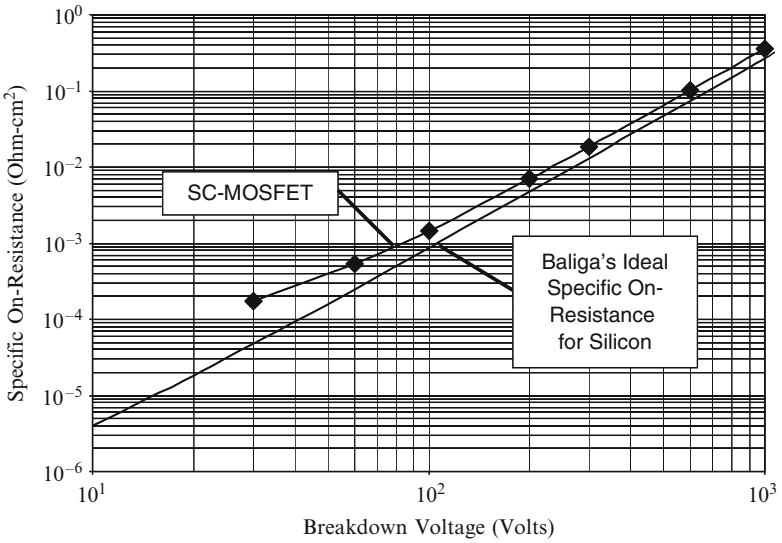

Fig. 4.31 Specific on-resistance for the power SC-MOSFET structures

Blocking Voltage (V)	Drain Supply Voltage (Volts)	On-State Current Density (A / cm^2)	Specific Gate Transfer Charge (nC / cm^2)
30	20	697	88
60	40	407	86
100	67	249	83
200	133	116	74
300	200	72.5	65
600	400	31.3	38
1000	667	16.6	3.8

Fig. 4.32 Parameters used for gate transfer charge analysis for the power SC-MOSFET structures

breakdown voltage is increased above 300 V. No power law fit is appropriate for this behavior.

The figure-of merit (C) – product of the specific on-resistance and the specific gate transfer charge – for the optimized power SC-MOSFET structures was obtained by determining the gate transfer charge for the cell with a gate width of 1 μm using the analytical model (see 4.26). During this analysis, the devices were assumed to be operated at an on-state current density that results in a power dissipation of 100 W/cm^2 as determined by the specific on-resistance for each

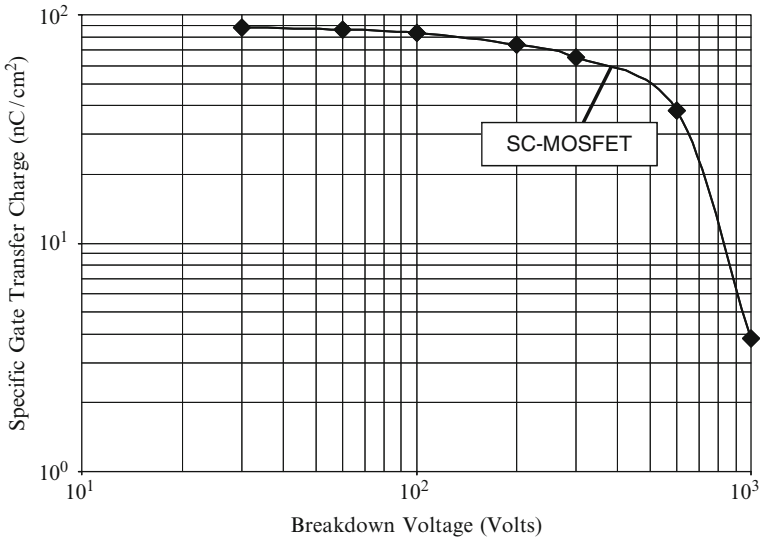

Fig. 4.33 Specific gate transfer charge for the power SC-MOSFET structures

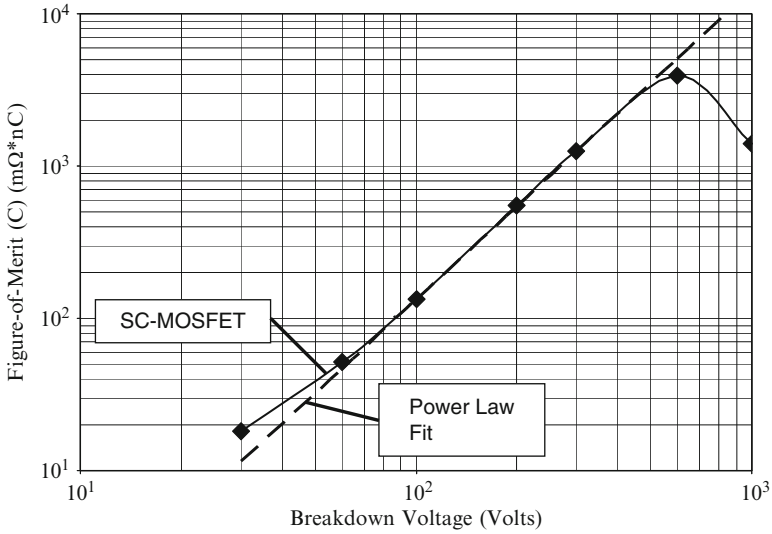

Fig. 4.34 Figure-of-merit (C) for the power SC-MOSFET structures

device. A gate width of 1 μm was used for the power SC-MOSFET structure, rather than the optimum gate width for achieving minimum specific on-resistance, because the device was developed for applications such as VRMs where low gate

charge (and consequently low FOM(C)) is required. The resulting values for the FOM(C) are plotted in Fig. 4.34 as a function of the breakdown voltage of the power SC-MOSFET structure. It can be observed that the FOM(C) increases in a linear fashion on this log-log graph for breakdown voltages ranging from 60 to 600 V indicating a power law relationship. The power law relationship that fits the data is shown in the figure by the dashed line. The equation for this line is:

$$\mathrm{FOM(C)} = \mathrm{R_{ON,sp}Q_{GD,sp}} = 0.01152\ \mathrm{BV}^{2.032} \tag{4.37}$$

where the FOM(C) has units of mΩ nC. The FOM(C) has a smaller value than predicted by the power law fit for the 1,000-V device because the on-state voltage drop at the operating current density is very close to the JFET pinch-off voltage.

References

1. B.J. Baliga and D. Girdhar, "Paradigm Shift in Planar Power MOSFET Technology", Power Electronics Technology Magazine, pp. 24–32, November 2003.
2. B.J. Baliga, "Power Semiconductor Devices having Laterally Extending Base Shielding Regions that Inhibit Base Reach-Through", U.S. Patent # 6,791,143, Issued September 14, 2004.
3. B.J. Baliga, "Fundamentals of Power Semiconductor Devices", Springer-Science, New York, 2008.
4. Silicon Semiconductor Corporation Datasheets, www.siliconsemi.com.

Chapter 9
SiC Planar MOSFET Structures

In Chap. 1, it was demonstrated that the specific on-resistance of power MOSFET devices can be greatly reduced by replacing silicon with wide band gap semiconductors. Among wide band gap semiconductors, the most progress with creating power MOSFET structures has been achieved using silicon carbide. Silicon carbide power device structures have been discussed in detail in a previous book [1]. In that book, it was shown that the conventional planar power D-MOSFET structure, developed and widely utilized for silicon, is not suitable for the development of silicon carbide devices. Two problems are encountered when utilizing the conventional power D-MOSFET structure for silicon carbide. The first problem is the much larger threshold voltage required to create an inversion layer in silicon carbide due to its much greater band gap. The doping concentration required in the P-base region to achieve a typical threshold voltage of 2 V is so low that the device cannot sustain a high blocking voltage due to reach-through of the depletion layer in the base region. The second problem is the very high electric field generated in the gate oxide because the electric field in the silicon carbide drift region under the gate is an order to magnitude larger than for silicon devices. This leads to rupture of the gate oxide at large blocking voltages.

For a planar power MOSFET structure, these issues can be addressed in a satisfactory manner by shielding the channel from the high electric field developed in the drift region. The concept of shielding of the channel region in a planar power MOSFET structure was first proposed [2] at PSRC in the early 1990s with a U.S. patent issued in 1996. The shielding was accomplished by formation of either a P^+ region under the channel or by creating a high resistivity conduction barrier region under the channel. The shielding approach also allowed the creation of a new power MOSFET structure called the ACCUFET where an accumulation layer is utilized to create the channel. The accumulation mode of operation allows achieving the desired typical threshold voltage and also provides a much larger channel mobility to reduce the channel resistance contribution.

In this chapter, the basic principles of operation of the shielded planar inversion-mode and accumulation-mode silicon carbide power MOSFET structures are described. The impact of shielding on ameliorating the reach-through breakdown

B.J. Baliga, *Advanced Power MOSFET Concepts*,
DOI 10.1007/978-1-4419-5917-1_9, © Springer Science+Business Media, LLC 2010

in silicon carbide is described. The difference between the threshold voltage for inversion and accumulation mode silicon carbide structures is then analyzed based up on fundamental considerations. The results of the analysis of the shielded planar silicon carbide MOSFET structures by using two-dimensional numerical simulations are described in this chapter as in the case of all the silicon devices. It is shown that the shielding concept also enables reduction of the electric field developed in the gate oxide leading to the possibility of fully utilizing the breakdown field strength of the underlying semiconductor drift region. The shielded accumulation-mode MOSFET structures (named the ACCUFET) discussed in this chapter have very promising characteristics for high voltage motor control applications.

9.1 Shielded Planar Inversion-Mode MOSFET Structure

The basic structure of the shielded planar inversion-mode power MOSFET structure is shown in Fig. 9.1. The structure contains a sub-surface P^+ shielding region which extends under both the N^+ source region and the P-base region. The P^+ shielding region is shown to extend beyond the edge of the P-base region in the figure. However, the P-base and the P^+ shielding region can also be formed by using a self-aligned ion-implantation process. The space between the P^+ shielding regions, indicated in the figure as the JFET region, is optimized to obtain a low specific on-resistance while simultaneously shielding the gate oxide interface and

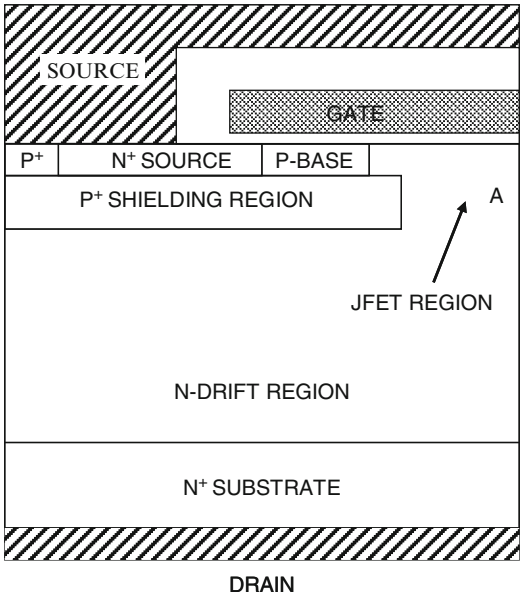

Fig. 9.1 Shielded planar inversion-mode power MOSFET structure

the P-base region from the high electric field in the drift region. A potential barrier is formed at location A after the JFET region becomes depleted by the applied drain bias in the blocking mode. This barrier prevents the electric field from becoming large at the gate oxide interface and at the P-base/N-drift junction. When a positive bias is applied to the gate electrode, an inversion layer channel is formed at the surface of the P-base region in the structure enabling the conduction of drain current with a low specific on-resistance. The specific on-resistance of the silicon carbide inversion-mode power MOSFET structure is limited by the channel resistance as described below.

9.1.1 Blocking Mode

In the forward blocking mode of the silicon carbide shielded planar inversion-mode power MOSFET structure, the voltage is supported by a depletion region formed on both sides of the P^+ region/N-drift junction. The maximum blocking voltage is determined by the electric field at this junction becoming equal to the critical electric field for breakdown if the parasitic $N^+/P/N$ bipolar transistor is completely suppressed. This suppression is accomplished by short-circuiting the N^+ source and P^+ regions using the source metal as shown on the upper left hand side of the cross-section. If the doping concentration of the P^+ region is large, the reach-through breakdown problem is completely eliminated. In addition, the high doping concentration in the P^+ region promotes the depletion of the JFET region at lower drain voltages providing enhanced shielding of the channel and gate oxide.

In the conventional power D-MOSFET structure, the minimum P-base thickness and doping concentration are constrained by the reach-through limitation. This does not occur in the silicon carbide shielded planar inversion-mode power MOSFET structure due to shielding of the P-base region from the drain potential by the P^+ shielding region. This allows reducing the channel length to less than 1 μm. In addition, the doping concentration of the P-base region can be reduced to achieve a desired threshold voltage without reach-through induced breakdown. The smaller channel length and threshold voltage reduce the channel resistance contribution.

As in the case of the planar silicon power D-MOSFET structure, the maximum blocking voltage capability of the silicon carbide shielded inversion-mode planar MOSFET structure is determined by the drift region doping concentration and thickness. However, to fully utilize the high breakdown electric field strength available in silicon carbide, it is necessary to screen the gate oxide from the high field within the semiconductor. In the shielded planar MOSFET structure, this is achieved by the formation of a potential barrier at location A by the depletion of the JFET region at a low drain bias voltage. The maximum electric field in the gate oxide can be made not only below its rupture strength but lower than values required for reliable operation over long time durations.

9.1.1.1 Simulation Results

The results of two-dimensional numerical simulations on the 600 V shielded 4H-SiC planar power MOSFET structure are described here to provide a more detailed understanding of the underlying device physics and operation during the blocking mode. The structure used for the numerical simulations had a drift region thickness of 4 μm below the P^+ shielding region with a doping concentration of 5×10^{16} cm^{-3}. The P^+ region extended from a depth of 0.2 to 1.0 μm with a doping concentration of 1×10^{19} cm^{-3}. The P-base and N^+ source regions were formed within the 0.2 μm of the N-drift region located above the P^+ region. The doping concentration of the P-base region was 5×10^{16} cm^{-3}. For the numerical simulations, the cell structure (with a width of 4 μm) illustrated in Fig. 9.1 was utilized as a unit cell that is representative of the structure. Due to high doping concentration in the drift region for the 600-V 4H-SiC devices, the doping concentration in the JFET region was not enhanced as is usually required for silicon devices.

A three dimensional view of the doping distribution in the 600 V shielded 4H-SiC planar power MOSFET structure is shown in Fig. 9.2 with the upper surface of the structure located on the right hand side in order to display the doping concentration in the vicinity of the channel. The highly doped P^+ shielding region is prominently located just below the surface. The P-base region can be observed to have a much lower doping concentration. The junction between the P-base region and N-JFET region is also visible.

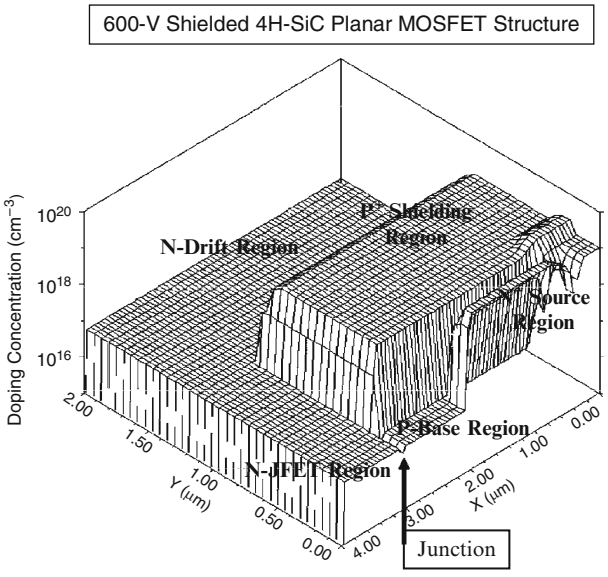

Fig. 9.2 Doping distribution in the shielded 4H-SiC planar power MOSFET structure

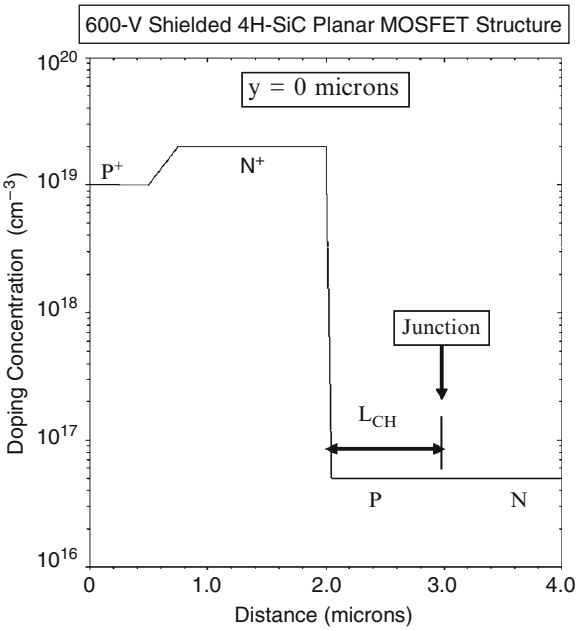

Fig. 9.3 Channel doping profile for the shielded 4H-SiC planar power MOSFET structure

The lateral doping profile taken along the surface of the 600 V shielded 4H-SiC planar power MOSFET structure is shown in Fig. 9.3. From the profile, it can be observed that the channel extends from 2 to 3 μm creating a channel length of 1 μm in the P-base region. The doping concentration of the JFET region is the same as that of the N-drift region. The N^+ source region and the P^+ contact region for shorting the source to the base region are visible on the left-hand-side. All the regions were defined with uniform doping with abrupt interfaces between them due to the low diffusion rates for dopants in 4H-SiC material.

The vertical doping profile taken at two positions within the 600 V shielded 4H-SiC planar power MOSFET structure are provided in Fig. 9.4. From the profile taken at x = 1 μm through the N^+ source region (solid line), it can be observed that the doping concentration of the P^+ shielding region has a maximum value of 1×10^{19} cm^{-3} at a depth ranging from 0.2 to 1.0 μm. The P-base region is located between the N^+ source region and the P^+ shielding region with a doping concentration of 5×10^{16} cm^{-3}. From the profile taken at x = 4 μm (dashed line), it can be observed that the JFET region has doping concentration of 5×10^{16} cm^{-3}.

The blocking characteristics for the 600 V shielded 4H-SiC planar power MOSFET structure were obtained by using zero gate bias. Due to the very small intrinsic concentration in 4H-SiC, no substantial leakage current is observed at room temperature. This also confirms that the reach-through of the P-base region has been suppressed by the P^+ shielding region. The potential contours within the

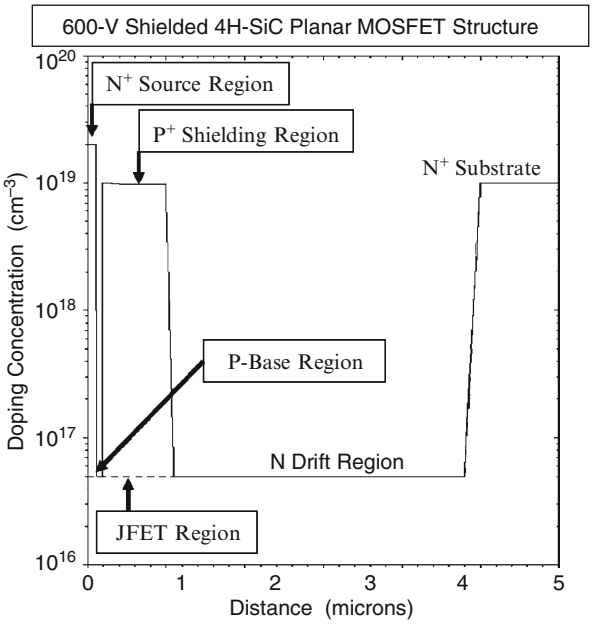

Fig. 9.4 Vertical doping profiles in the shielded 4H-SiC planar power MOSFET structure

shielded 4H-SiC planar power MOSFET structure at a drain bias of 600 V are provided in Fig. 9.5. It can be observed that the drain voltage is supported below the P^+ shielding region. The potential contours do not extend into the P-base region indicating that it is shielded from the drain potential by the P^+ shielding region. The potential contours are crowding at the edge of the P^+ shielding region indicating an enhanced electric field. This can be clearly observed in Fig. 9.6 which provides a three-dimensional view of the electric field distribution. In this figure, it can also be observed that the electric field in the JFET region, and most importantly at the surface under the gate oxide, has been greatly reduced by the presence of the P^+ shielding region.

It is insightful to examine the electric field profile in the JFET region within the 600 V shielded 4H-SiC planar power MOSFET structure when it is operating in the blocking mode. The electric field profiles obtained through the middle of the JFET region are shown in Fig. 9.7 at various drain bias voltages. It can be observed that the maximum electric field in the JFET region occurs at a depth of 1.5 μm from the surface. This reduces the electric field at the surface under the gate oxide to about one-third of the electric field in the bulk below the P^+ shielding region. Consequently, the electric field in the gate oxide is reduced to about 3×10^6 V/cm. The low electric field in the gate oxide for the 600 V shielded 4H-SiC planar power MOSFET structure prevents gate oxide rupture and allows stable device performance over long periods of time. An even further reduction of electric field in the

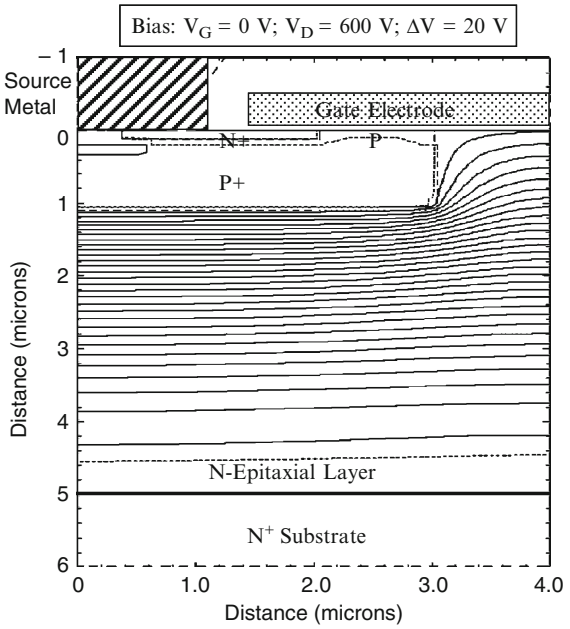

Fig. 9.5 Potential contours in the shielded 4H-SiC planar power MOSFET structure

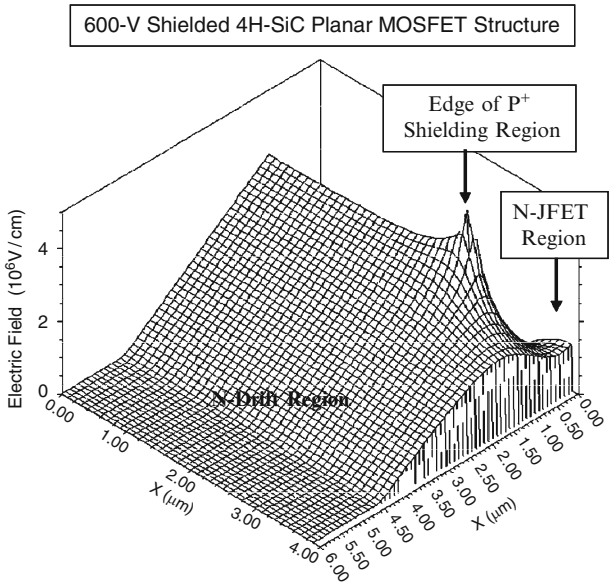

Fig. 9.6 Electric field distribution in the shielded 4H-SiC planar power MOSFET structure

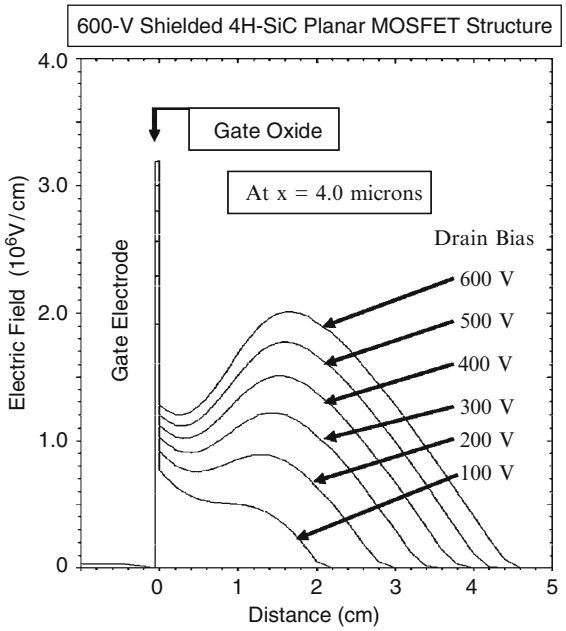

Fig. 9.7 Electric field distribution under the gate region in the shielded 4H-SiC planar power MOSFET structure

gate oxide can be achieved by reducing the width of the JFET region at the expense of a small increase in the on-resistance.

9.1.2 Threshold Voltage

The threshold voltage of the power MOSFET devices is an important design parameter from an application stand-point. A minimum threshold voltage must be maintained at above 1 V for most system applications to provide immunity against inadvertent turn-on due to voltage spikes arising from noise. At the same time, a high threshold voltage is not desirable because the voltage available for creating the charge in the channel is determined by $(V_G - V_{TH})$ where V_G is the applied gate bias voltage and V_{TH} is the threshold voltage. Most power electronic systems designed for high voltage operation (the most suitable application area for silicon carbide devices) provide a gate drive voltage of only up to 10 V. Based upon this criterion, the threshold voltage should be kept at 2 V in order to obtain a low channel resistance contribution.

For the inversion-mode shielded planar MOSFET structure, the threshold voltage can be modeled by defining it as the gate bias at which on-set of *strong inversion* begins to occur in the channel. This voltage can be determined using [3]

$$V_{TH} = \frac{\sqrt{4\varepsilon_S kTN_A \ln(N_A/n_i)}}{C_{ox}} + \frac{2kT}{q} \ln\left(\frac{N_A}{n_i}\right) \tag{9.1}$$

where N_A is the doping concentration of the P-base region, k is Boltzmann's constant, and T is the absolute temperature. The presence of positive fixed oxide charge shifts the threshold voltage in the negative direction by

$$\Delta V_{TH} = \frac{Q_F}{C_{ox}} \tag{9.2}$$

A further shift of the threshold voltage in the negative direction by 1 V can be achieved by using heavily doped N-type polysilicon as the gate electrode as routinely done for silicon power MOSFET structures.

The analytically calculated threshold voltage for 4H-SiC inversion-mode MOSFET structures are provided in Fig. 9.8 for the case of a gate oxide thickness of 0.05 μm as a function of the P-base doping concentration with the inclusion of a metal-semiconductor work-function difference of 1 V. It can be observed that the model predicts a threshold voltage of about 6.5 V even for a relatively low P-base doping concentration of 5×10^{16} cm^{-3}. It is difficult to reduce the threshold voltage below 3 V for the inversion-mode structure. This is one reason for the development of accumulation-mode power MOSFET structures for silicon carbide.

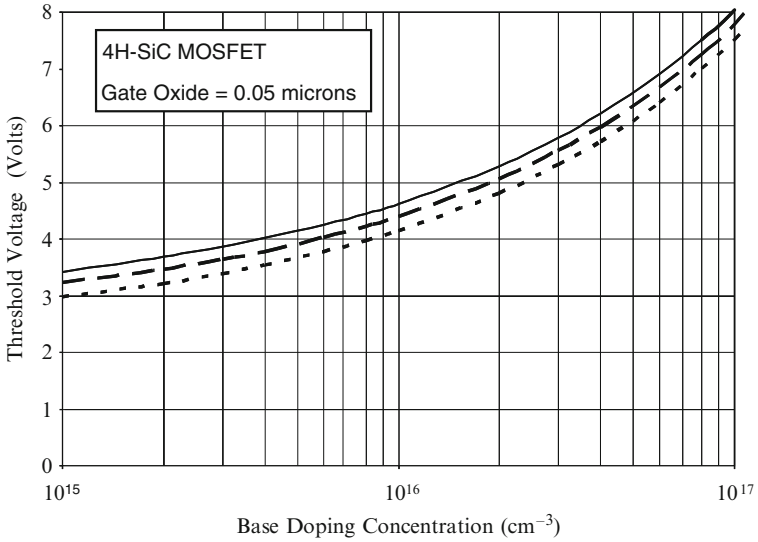

Fig. 9.8 Threshold voltage of 4H-SiC inversion-mode MOSFET structures (*solid line*: 300°K; *dash line*: 400°K; *dotted line*: 500°K)

9.1.3 On-State Resistance

In the silicon carbide shielded inversion-mode planar MOSFET structure, current flow between the drain and source can be induced by creating an inversion layer channel on the surface of the P-base region. The current flows through the channel formed due to the applied gate bias into the JFET region via the accumulation layer formed above it under the gate oxide. It then spreads into the N-drift region at a 45° angle and becomes uniform through the rest of the structure. The total on-resistance for the silicon carbide shielded inversion-mode planar SiC MOSFET structure is determined by the resistance of the components in the current path

$$R_{on,sp} = R_{CH} + R_A + R_{JFET} + R_D \tag{9.3}$$

where R_{CH} is the channel resistance, R_A is the accumulation region resistance, R_{JFET} is the resistance of the JFET region, R_D is the resistance of the drift region after taking into account current spreading from the JFET region. For consistency with previous chapters, the resistance of the N^+ substrate has been omitted in the above analysis even though the substrate contribution for 4H-SiC can be very large unless its thickness is reduced to below 50 μm. The resistances can be analytically modeled by using the current flow pattern indicated by the shaded regions in Fig. 9.9.

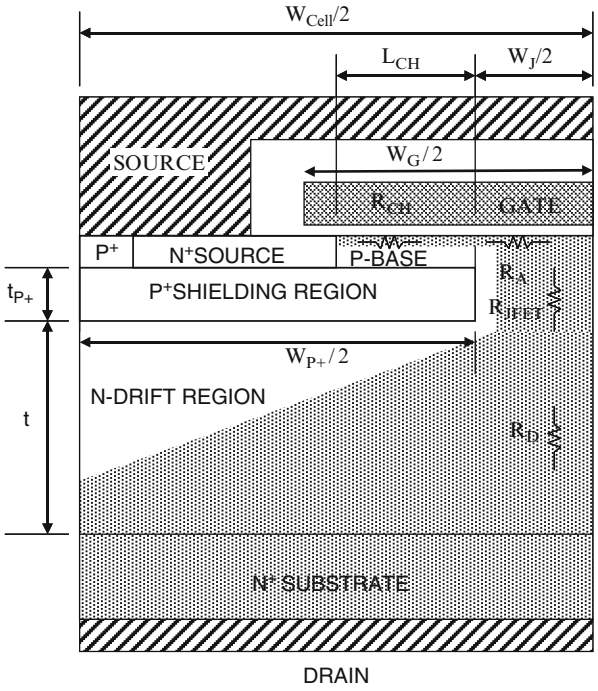

Fig. 9.9 Current path and resistances in the shielded planar SiC inversion-mode power MOSFET structure

9.1.3.1 Channel-Resistance

For the shielded planar SiC MOSFET structure with the P-base region, the specific channel resistance is given by

$$R_{CH} = \frac{(L_{CH} W_{Cell})}{2\ \mu_{inv} C_{ox} (V_G - V_{TH})} \tag{9.4}$$

where L_{CH} is the channel length as shown in Fig. 9.9, μ_{inv} is the mobility for electrons in the inversion layer channel, C_{ox} is the specific capacitance of the gate oxide, V_G is the applied gate bias, and V_{TH} is the threshold voltage. Although an inversion layer mobility of 165 cm^2/V-s has been observed in lateral MOSFET structures [4], the inversion layer mobility in high voltage 4H-SiC power MOSFET structure [5] is usually only 10–20 cm^2/V-s. The relatively low inversion layer mobility makes the channel resistance component dominant in the shielded planar SiC MOSFET structure.

In the case of the 600 V shielded planar 4H-SiC MOSFET structure, the cell width will be assumed to be 8 μm with a channel length of 1 μm. The threshold voltage for the inversion mode structure is 4.5 V despite the low doping concentration of 5×10^{16} cm^{-3} for the P-base region. Using a gate oxide thickness is 500 Å, and an inversion layer mobility of 12 cm^2/V-s in the above equation, the specific resistance contributed by the channel at a gate bias of 10 V is found to be 8.88 mΩ cm^2. This value is much larger than the ideal specific on-resistance of 0.0262 mΩ cm^2 for the drift region of a 600-V 4H-SiC device.

9.1.3.2 Accumulation-Resistance

In the shielded planar SiC MOSFET structure, the current flowing through the inversion channel enters the JFET region at the edge of the P-base junction. The current spreads downwards from the edge of the P-base junction into the JFET region. The current spreading phenomenon is aided by the formation of an accumulation layer in the semiconductor below the gate oxide due to the positive gate bias applied to turn-on the device. The specific on-resistance contributed by the accumulation layer in the shielded planar SiC MOSFET structure is given by

$$R_{A,SP} = K_A \frac{W_J W_{Cell}}{4\mu_{nA} C_{OX} (V_G - V_{TH})} \tag{9.5}$$

In writing this expression, a coefficient K_A has been introduced to account for the current spreading from the accumulation layer into the JFET region. A typical value for this coefficient is 0.6 based upon the current flow observed from numerical simulations of shielded planar SiC MOSFET structures. The threshold voltage in the expression is for the on-set of formation of the accumulation layer. A zero

threshold voltage will be assumed here when performing the analytical computations. Note that the width of the JFET region defines the length of the accumulation region.

In the case of n-channel 4H-SiC MOSFET structures, accumulation layer mobility values of 100–200 cm^2/V-s have been experimentally observed [6]. Using an accumulation layer mobility of 180 cm^2/V-s for the 600-V shielded planar SiC MOSFET structure with a cell width of 8 μm and JFET width of 2 μm, the specific resistance contributed by the accumulation layer at a gate bias of 10 V is found to be 0.196 mΩ cm^2 if the gate oxide thickness is 500 Å.

9.1.3.3 JFET-Resistance

The electrons entering from the channel into the drift region are distributed into the JFET region via the accumulation layer formed under the gate electrode. The spreading of current in this region was accounted for by using a constant K_A of 0.6 for the accumulation layer resistance. Consequently, the current flow through the JFET region can be treated with a uniform current density. In the shielded planar SiC MOSFET structure, the cross-sectional area for the JFET region is uniform with the width given by

$$a = (W_J - 2W_0) \tag{9.6}$$

where W_0 is the zero-bias depletion width for the JFET region. The zero-bias depletion width (W_0) in the JFET region can be computed by using its doping concentrations on both sides of the junction

$$W_0 = \sqrt{\frac{2\varepsilon_S V_{bi}}{qN_{DJ}}} \tag{9.7}$$

where N_{DJ} is the doping concentration in the JFET region. The built-in potential is also related to the doping concentrations on both sides of the junction

$$V_{bi} = \frac{kT}{q} \ln\left(\frac{N_A N_{DJ}}{n_i^2}\right) \tag{9.8}$$

where N_A is the doping concentration in the P^+ shielding region. Compared with silicon devices, the built-in potential for 4H-SiC is about 3-times larger.

The specific on-resistance contributed by the JFET region in the shielded planar SiC MOSFET structure can be obtained by using

$$R_{JFET,SP} = \frac{\rho_{JFET} t_{P+} W_{Cell}}{(W_J - 2W_0)} \tag{9.9}$$

where ρ_{JFET} is the resistivity of the JFET region given by

$$\rho_{JFET} = \frac{1}{q\mu_n N_{DJ}} \tag{9.10}$$

where μ_n is the bulk mobility appropriate to the doping level of the JFET region. In the case of the 600-V shielded planar 4H-SiC MOSFET structure with a doping concentration of 5×10^{16} cm^{-3} in the N-drift and JFET regions, the resistivity for the JFET region is found to be 0.156 Ω cm. The zero-bias depletion width in the JFET region for this JFET doping concentration is 0.254μm based up on a built-in potential of 3 V. For the 600-V shielded planar SiC MOSFET structure with a cell width of 8 μm and JFET width of 2 μm, the specific resistance contributed by the JFET region is found to be 0.067 mΩ cm^2 based up on using the above parameters with a P^+ region thickness (t_{P+}) of 0.8 μm.

9.1.3.4 Drift-Resistance

The resistance contributed by the drift region in the shielded planar SiC MOSFET structure is enhanced above that for the ideal drift region due to current spreading from the JFET region. The cross-sectional area for the current flow in the drift region increases from the width 'a' of the JFET region at a 45° angle as illustrated in Fig. 9.9 by the shaded area. For the 600-V shielded planar SiC MOSFET structure, the current paths in the drift region overlap at a depth of $W_{P+}/2$ from the bottom of the P^+ shielding region. The specific on-resistance contributed by the drift region with this model is given by

$$R_{D,SP} = \frac{\rho_D W_{Cell}}{2} \ln\left[\frac{a + W_{P+}}{a}\right] + \rho_D[t - (W_{P+}/2)] \tag{9.11}$$

For the parameters given above for this structure, the dimension 'a' in the equation is found to be 1.49 μm. For the 600-V shielded planar 4H-SiC MOSFET structure with a cell width of 8 μm and JFET width of 2 μm, the specific resistance contributed by the drift region is then found to be 0.117 mΩ cm^2 by using a resistivity of the drift region of 0.156 Ω cm (based upon a doping concentration of 5×10^{16} cm^{-3}) and a drift region thickness of 4 μm below the P^+ shielding region.

9.1.3.5 Total On-Resistance

The total specific on-resistance for the 600-V shielded planar 4H-SiC MOSFET structure with a cell width of 8 μm and JFET width of 2 μm is obtained by adding the above components of the resistances within the device structure. For a gate bias of 10 V, the total specific on-resistance is found to be 9.26 mΩ cm^2. The channel

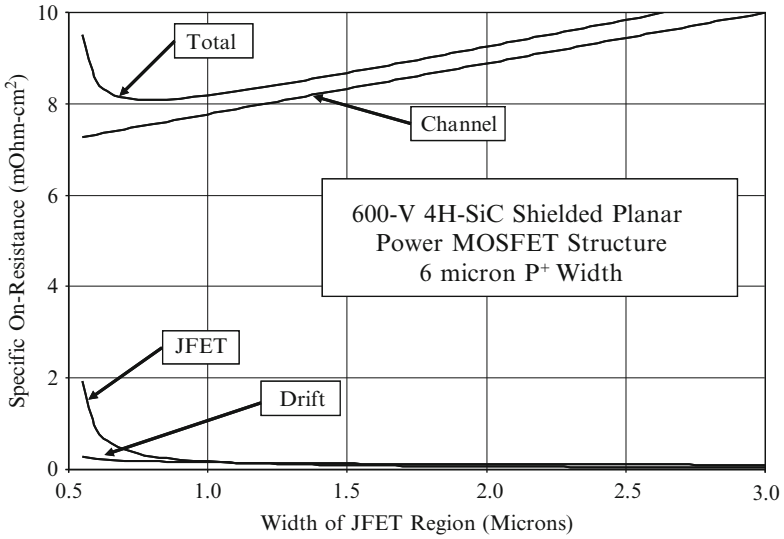

Fig. 9.10 On-resistance for the 600-V 4H-SiC shielded planar MOSFET structures

resistance constitutes 96% of the total specific on-resistance due to the poor mobility for the electrons in the inversion layer. The specific on-resistance for the 600-V shielded planar 4H-SiC MOSFET structure is an order of magnitude smaller than that for the silicon 600-V power D-MOSFET and U-MOSFET structures. However, specific on-resistances lower than those of the 600-V shielded planar 4H-SiC MOSFET structure can be obtained by using the silicon 600-V GD-MOSFET and SJ-MOSFET structures. Consequently, the 600-V shielded 4H-SiC power MOSFET structure is not competitive with the best silicon technology unless the channel mobility can be improved.

The impact of changing the width of the JFET region on the specific on-resistance of the shielded planar 4H-SiC MOSFET structure can be determined by using the above analytical model. The results obtained for the case of a 600-V device structure with a P^+ shielding region width of 6 μm are provided in Fig. 9.10. For this analysis, an inversion layer mobility of 12 cm^2/V-s was used. It can be observed that the specific on-resistance goes through a minimum as the width of the JFET region is increased. At very small widths for the JFET region, the resistance from the JFET region and the drift region become comparable to the channel contribution producing an increase in the total specific on-resistance. When the width of the JFET region is increased beyond 1 μm, the channel resistance becomes dominant producing a monotonic increase in the specific on-resistance. The increase in the specific on-resistance between a JFET width of 1 and 2 μm is relatively small. Consequently, this width can be optimized from the point of view of shielding the gate oxide and P-base region from the high electric fields in the drift region.

9.1.3.6 Impact of Breakdown Voltage

The specific on-resistance for the shielded planar 4H-SiC MOSFET structure is plotted in Fig. 9.11 as a function of the breakdown voltage by using the analytical model. In performing the modeling, it is important to recognize that the thickness of the drift region (parameter 't' in Fig. 9.9) can become smaller than half the width of the P^+ shielding region at lower breakdown voltages. Under these conditions, the current does not distribute across the entire drift region under the P^+ shielding region. The device parameters used for the plot are: channel inversion mobility of 12 cm^2/V-s; a fixed JFET doping concentration of 5×10^{16} cm^{-3}; a width of 6 μm for the P^+ shielding region; a width of 2 μm for the JFET region; a cell width of 8 μm; gate bias of 10 V; threshold voltage of 4.5 V; and a gate oxide thickness of 500 Å. From Fig. 9.11, it can be seen that specific on-resistance of 4H-SiC shielded planar MOSFET structure is limited by the channel resistance for breakdown voltages below 3,000 V due to the poor inversion layer mobility. The drift region resistance can be observed to be close to the ideal specific on-resistance over most the range of breakdown voltages. The total specific on-resistance of the 4H-SiC shielded planar MOSFET structure approaches that of the drift region only when the breakdown voltage exceeds 10,000 V.

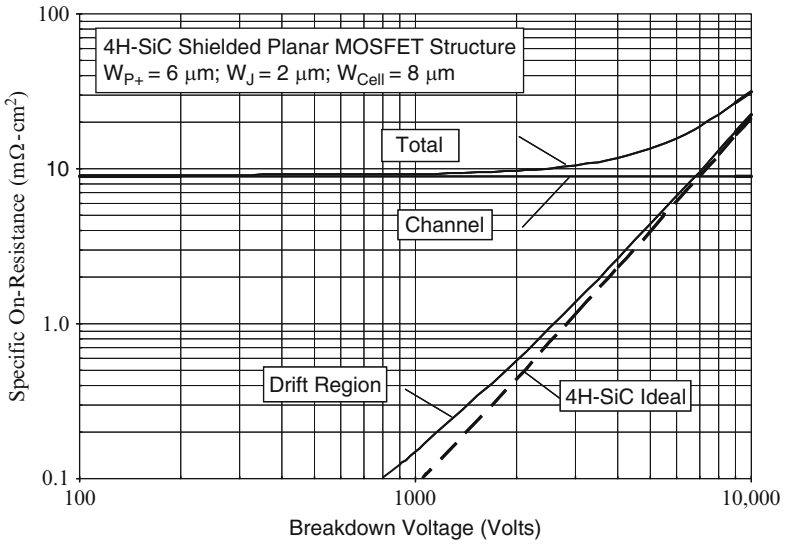

Fig. 9.11 Specific on-resistance for the 4H-SiC shielded planar MOSFET structure

9.1.3.7 Simulation Results

The transfer characteristic for the 600-V shielded 4H-SiC planar power MOSFET structure was obtained using numerical simulations with a drain bias of 0.1 V at

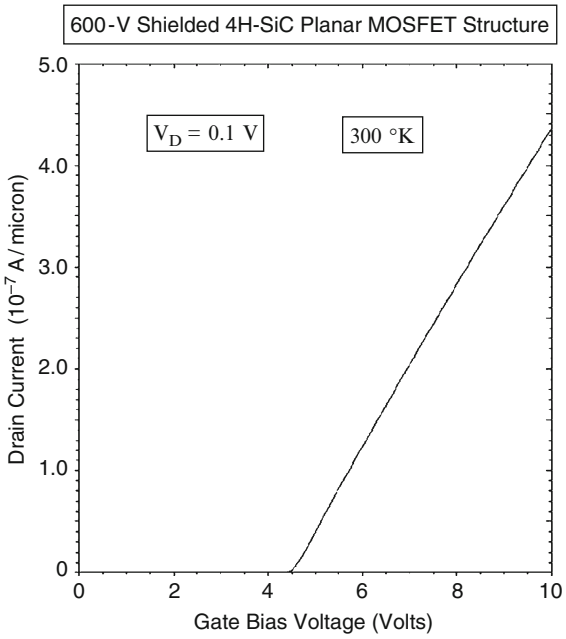

Fig. 9.12 Transfer characteristic of the shielded 4H-SiC planar power MOSFET structure

300°K. The device parameters for the structure used for the numerical simulations were provided in the Sect. 9.1.1. The channel mobility was degraded during the simulations to about 12 cm^2/V-s. The resulting transfer characteristic is shown in Fig. 9.12. From this graph, a threshold voltage of 4.5 can be extracted at 300°K. This demonstrates that the threshold voltage is relatively large for the inversion-mode 4H-SiC power MOSFET structure despite the low (5×10^{16} cm^{-3}) doping concentration for the P-base region. For the case of a gate bias of 10 V and 300°K, the specific on-resistance is found to be 9.17 mΩ cm^2 providing validation of the analytical model. The linear increase in drain current with gate voltage indicates that the channel resistance is dominant in the 600-V shielded 4H-SiC planar power MOSFET structure.

The on-state current flow pattern within the 600-V shielded 4H-SiC planar power MOSFET structure at a small drain bias of 0.1 V and a gate bias of 10 V is shown in Fig. 9.13. In the figure, the depletion layer boundary is shown by the dotted lines and the junction boundary is delineated by the dashed line. The depletion layer width (W_0) in the JFET region is about 0.25 μm in good agreement with the value computed using the analytical model. It can be observed that the current flows from the channel and distributes into the JFET region via the accumulation layer. Within the JFET region, the cross-sectional area is approximately constant with a width (a/2) of 0.75 μm. From the figure, it can be seen that the current spreads from the JFET region to the drift region at a

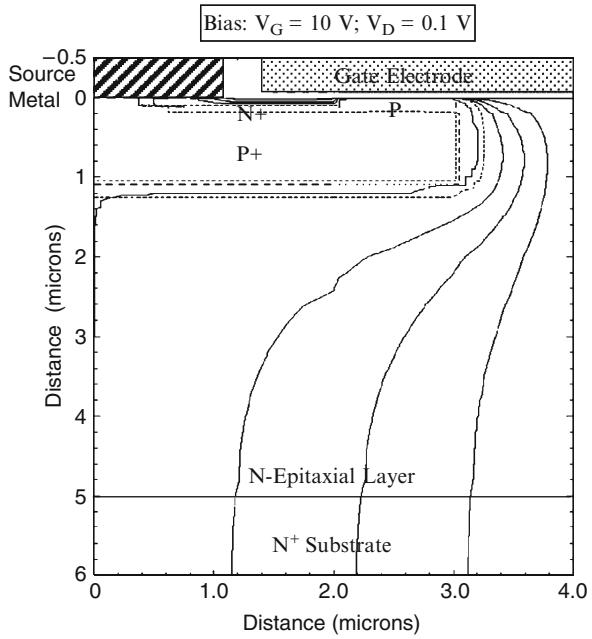

Fig. 9.13 Current distribution in the shielded 4H-SiC planar power MOSFET structure

45° angle as assumed in the model and becomes uniform for the last 1 μm of the drift region.

9.1.4 Capacitances

The capacitances within the shielded planar 4H-SiC MOSFET structure can be analytically modeled using the same approach as used for the power SC-MOSFET structure in Chap. 4. The specific input (or gate) capacitance for the shielded planar 4H-SiC MOSFET structure is given by

$$C_{IN,SP} = C_{N+} + C_P + C_{SM} = \frac{(W_G - W_J)}{W_{Cell}}\left(\frac{\varepsilon_{OX}}{t_{OX}}\right) + \frac{W_G}{W_{Cell}}\left(\frac{\varepsilon_{OX}}{t_{IEOX}}\right) \tag{9.12}$$

where t_{OX} and t_{IEOX} are the thicknesses of the gate and inter-electrode oxides, respectively. For a 600-V shielded planar 4H-SiC power MOSFET structure with a cell width (W_{CELL} in Fig. 9.9) of 8 μm, JFET region width of 2 μm, and gate electrode width of 5 μm, the specific input capacitance is found to be 30 nF cm^{-2} for a gate oxide thickness of 500 Å and an inter-metal dielectric thickness of 5,000 Å.

The capacitance between the gate and drain electrodes (also called the reverse transfer capacitance) is determined by the width of the JFET region where the gate electrode overlaps the N-drift region. The MOS structure in this portion of the shielded planar 4H-SiC power MOSFET structure operates under deep depletion conditions when a positive voltage is applied to the drain. As in the case of the power SC-MOSFET structure, the gate-drain capacitance for the shielded planar 4H-SiC MOSFET power structure is given by

$$C_{GD,SP} = \frac{(W_G - W_J)}{W_{Cell}} \left(\frac{C_{OX} C_{S,M}}{C_{OX} + C_{S,M}} \right) \tag{9.13}$$

where $C_{S,M}$ is the semiconductor capacitance under the gate oxide, which decreases with increasing drain bias voltage. The specific capacitance of the semiconductor depletion region can be obtained by computation of the depletion layer width. The depletion layer width in the semiconductor under the gate oxide can be obtained using

$$W_{D,MOS} = \frac{\varepsilon_S}{C_{OX}} \left\{ \sqrt{1 + \frac{2 V_D C_{OX}^2}{q\ \varepsilon_S N_{DJ}}} - 1 \right\} \tag{9.14}$$

where N_{DJ} is the doping concentration of the JFET region. The specific capacitance for the semiconductor is then obtained using

$$C_{S,M} = \frac{\varepsilon_S}{W_{D,MOS}} \tag{9.15}$$

The gate-drain (or reverse transfer) capacitance can be computed by using (9.13) with the above equations to determine the semiconductor capacitance as a function of the drain bias voltage.

However, as in the case of the power SC-MOSFET structure, the above equation is only valid until the depletion region from the P^+ shielding regions pinches-off the JFET region in the shielded planar 4H-SiC power MOSFET structure. The gate-drain capacitance then decreases at a different rate because the gate is screened from the drain. The drain voltage at which the JFET region is pinched-off is given by

$$V_{P,JFET} = \frac{q N_{DJ}}{8\ \varepsilon_S} W_J^2 \tag{9.16}$$

For the 600-V shielded planar 4H-SiC power MOSFET structure with JFET region doping concentration (N_{DJ}) of 5×10^{16} cm^{-3} and JFET width (W_J) of 2 μm, the JFET region pinch-off voltage is 46.5 V. After the JFET region is pinched-off, the

gate-drain capacitance is determined by the edge of the depletion region located below the P^+ shielding region. This distance below the gate oxide is given by

$$W_S = t_{P+} + \sqrt{\frac{2\varepsilon_S V_D}{qN_D}} \tag{9.17}$$

The specific capacitance for the semiconductor below the gate oxide can then be obtained using (9.15) with the width W_S.

The output capacitance for the shielded planar 4H-SiC power MOSFET structure is associated with the capacitance of the junction between the P^+ shielding region and the N-drift region. Due to pinch-off of the JFET region with increasing drain bias voltage, it is necessary to examine the change in the depletion region boundary with applied voltage. The depletion layer boundary inside the shielded planar 4H-SiC power MOSFET structure prior to the pinch-off of the JFET region is similar to that previously shown by the dashed lines in Fig. 4.19 for the power SC-MOSFET structure. It can be observed that the depletion region has a vertical boundary inside the JFET region and a horizontal boundary below the P^+ shielding region. The capacitances associated with each of these regions are indicated in the figure as C_{S1} and C_{S2}. The specific junction capacitance associated with the JFET region is given by

$$C_{S1,SP} = \frac{\varepsilon_S}{W_{DJ}}\left(\frac{2L_{P+}}{W_{Cell}}\right) \tag{9.18}$$

where the depletion region thickness (W_{DJ}) in the JFET region is related to the drain bias voltage

$$W_{DJ} = \sqrt{\frac{2\varepsilon_S(V_D + V_{bi})}{qN_{DJ}}} \tag{9.19}$$

The specific junction capacitance associated with the bottom of the P^+ shielding region is given by [1]

$$C_{S2,SP} = \frac{\varepsilon_S}{W_{DD}}\left(\frac{W_{P+}}{W_{Cell}}\right) \tag{9.20}$$

where the depletion region thickness (W_{DD}) in the drift region is related to the drain bias voltage

$$W_{DD} = \sqrt{\frac{2\varepsilon_S(V_D + V_{bi})}{qN_D}} \tag{9.21}$$

where N_D is the doping concentration of the drift region. The specific output capacitance for the shielded planar 4H-SiC power MOSFET structure can then be obtained by combining the above values

$$C_{O,SP} = C_{S1,SP} + C_{S2,SP} \tag{9.22}$$

9.1.5 Gate Charge

The gate charge components for the shielded planar 4H-SiC power MOSFET structure are given by similar equations to those derived in Chap. 4 for the power SC-MOSFET structure. The gate transfer capacitance for this device structure is small during the transition from a drain bias of V_{DS} to the pinch-off voltage ($V_{P,JFET}$) for the JFET region. Due to the small gate transfer capacitance, a more rapid drop in drain voltage occurs from V_{DS} to $V_{P,JFET}$ at the beginning of the gate plateau phase. If the screening effect is neglected, the gate transfer charge corresponding to the transition where the drain voltage changes from V_{DS} to V_{ON} is given by

$$Q_{GD} = \frac{2K_G q \varepsilon_S N_D}{C_{OX}} \left[\sqrt{1 + \frac{2V_{DS}C_{OX}^2}{q\ \varepsilon_S N_D}} - \sqrt{1 + \frac{2V_{ON}C_{GOX}^2}{q\ \varepsilon_S N_D}} \right] \tag{9.23}$$

where the parameter K_G is given by

$$K_G = \frac{(W_G - W_J)}{W_{Cell}} \tag{9.24}$$

The other components of the gate charge are similar to those already provided in the textbook [3]

$$Q_{SW} = Q_{GS2} + Q_{GD} \tag{9.25}$$

$$Q_G = [C_{GS} + C_{GD}(V_{DS})]V_{GP} + Q_{GD} + [C_{GS} + C_{GD}(V_{ON})](V_G - V_{GP}) \tag{9.26}$$

Equations for the gate voltage, drain current, and drain voltage waveforms for the shielded planar 4H-SiC power MOSFET structure are similar to those derived in Chap. 4 for the power SC-MOSFET structure. If the screening effect is neglected, the drain voltage is determined by the gate transfer capacitance given by (9.13)

$$v_D(t) = \frac{q\varepsilon_S N_D}{2C_{OX}^2} \left\{ \left[\sqrt{1 + \frac{2V_{DS}C_{Ox}^2}{q\ \varepsilon_S N_D}} - \frac{J_G C_{OX}(t - t_2)}{2K_G q\ \varepsilon_S N_D} \right]^2 - 1 \right\} \tag{9.27}$$

from $t = t_2$ to $t = t_3$.

9.1.5.1 Simulation Example

The gate charge for the 600-V shielded 4H-SiC planar power MOSFET structure was extracted by using the results of two-dimensional numerical simulations of the cell described in the previous sections. The device was turned-on from blocking state with a drain bias of 400 V by driving it using a gate current of 1×10^{-8} A/μm (equivalent to 0.25 A cm^{-2} for the area of 4×10^{-8} cm^2). Once the drain current density reached 125 A cm^{-2}, the drain current was held constant resulting in a reduction of the drain voltage. The gate plateau voltage for this drain current density was found to be 8.2 V due to the poor transconductance of the device as a result of the low inversion layer mobility. Once the drain voltage reached the on-state value corresponding to the gate plateau voltage, the gate voltage increased to the steady-state value of 10 V.

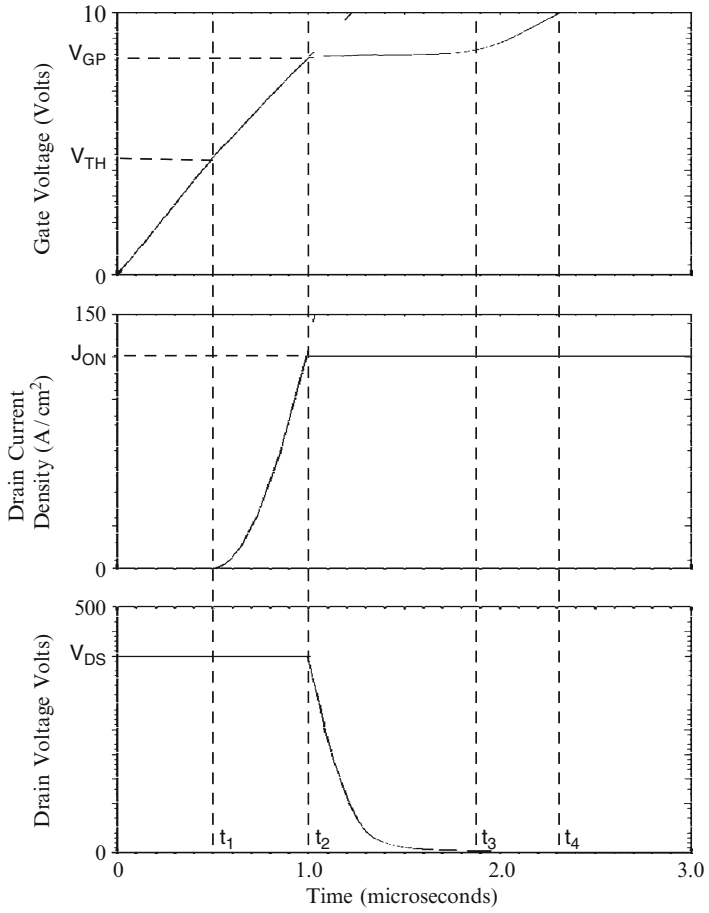

Fig. 9.14 Turn-on waveforms for the 600-V shielded 4H-SiC planar power MOSFET structure

Specific Gate Charge	Numerical Simulation (nC / cm^2)
Q_{GS1}	125
Q_{GS2}	125
Q_{GS}	250
Q_{GD}	200
Q_{SW}	325
Q_G	575

Fig. 9.15 Gate charge extracted from numerical simulations for the 600-V shielded 4H-SiC planar power MOSFET structure

The gate charge waveforms obtained by using an input gate current density of 0.25 A cm^{-2} when turning on the 600-V shielded 4H-SiC planar power MOSFET structure from a blocking state with drain bias of 400 V are shown in Fig. 9.14. The on-state current density is 125 A cm^{-2} at a DC gate bias of 10 V at the end of the turn-on transient. The gate voltage increases at a constant rate at the beginning of the turn-on process as predicted by the analytical model. When the gate voltage reaches the threshold voltage, the drain current begins to increase. The drain current increases relatively slowly until it reaches the on-state current density of 125 A cm^{-2} when compared with other high voltage silicon power MOSFET structures due to the low transconductance of the device.

Once the drain current reaches the on-state value, the gate voltage remains approximately constant at the plateau voltage (V_{GP}). The plateau voltage for this structure is a relatively large value of 8.2 V for the drain current density of 125 A cm^{-2} due to the poor transconductance of the device. The drain voltage drops rapidly from the supply voltage of 400 V of about 50 V (the JFET pinch-off voltage) as predicted by the analytical model. The drain voltage then decreases during the plateau phase in a non-linear manner. After the end of the plateau phase, the gate voltage again increases until it reaches the gate supply voltage.

The values for the various components of the gate charge extracted from the numerical simulations are provided in Fig. 9.15. The gate transfer charge for the 600-V shielded 4H-SiC planar power MOSFET structure is close to that of the 600-V D-MOSFET and U-MOSFET structures, and significantly larger than that of the 600-V power GD-MOSFET and SJ-MOSFET structures.

9.1.6 Device Figures of Merit

The figures of merit (defined in the previous chapters of the book) computed for the 600-V shielded planar 4H-SiC power MOSFET structure are provided in Fig. 9.16.

Figures of Merit	V_G = 10 V
FOM(A) ($\Omega^2cm^4s^{-1}$)	306, 667
FOM(B)(ps)	276
FOM(C) (mΩ*nC)	1840
FOM(D) (mΩ*nC)	2990

Fig. 9.16 Figures of merit for the 600-V 4H-SiC shielded planar MOSFET structures

The figure of merit usually used for comparison of device technologies in the literature is FOM(C). In comparison with the 600-V power D-MOSFET and U-MOSFET structures, the 600-V shielded planar 4H-SiC power MOSFET structure has a FOM(C) that is an order of magnitude smaller. However, in comparison with the 600-V power GD-MOSFET and SJ-MOSFET structures, the 600-V shielded planar 4H-SiC power MOSFET structure has a FOM(C) that is five-times larger. Consequently, 600-V shielded planar 4H-SiC power MOSFET structure offers significant improvement in circuit performance compared with the conventional silicon power MOSFET structures but is not competitive with the new silicon power MOSFET technology based up on the charge coupling concept. This conclusion is a consequence of the low inversion layer mobility.

9.1.7 Inductive Load Turn-Off Characteristics

As discussed in preceding chapters, high voltage power MOSFET devices are often used in adjustable speed motor drives which behave as inductive loads. The operation of the shielded planar 4H-SiC power MOSFET structure in an inductive load circuit can be analyzed using the same approach as used for the power SJ-MOSFET structure. The gate plateau voltage for the shielded planar 4H-SiC power MOSFET structure is given by

$$V_{GP} = V_{TH} + \sqrt{\frac{J_{D,ON} W_{Cell} L_{CH}}{\mu_{ni} C_{GOX}}} \tag{9.28}$$

where C_{GOX} is the gate oxide capacitance. The time constant for discharging the gate of the shielded planar 4H-SiC power MOSFET structure is $R_{G,SP}$* $[C_{GS} + C_{GD}(V_{ON})]$ and the gate voltage decreases exponentially with time as given by

$$v_G(t) = V_{GS} e^{-t/R_{G,SP}[C_{GS}+C_{GD}(V_{ON})]} \tag{9.29}$$

The time t_4 (using the notation from the textbook) for reaching the gate plateau voltage can be obtained by using this equation with (9.28) for the plateau voltage

$$t_4 = R_{G,SP}[C_{GS} + C_{GD}(V_{ON})]\ln\left[\frac{V_{GS}}{V_{GP}}\right] \tag{9.30}$$

This time can be considered to a *turn-off delay time* before the drain voltage begins to increase after the turn-off is initiated by the control circuit.

The drain voltage begins to increase at time t_4 but the drain current remains constant at the load current I_L because the current cannot be transferred to the diode until the voltage at the drain of the MOSFET device exceeds the supply voltage V_{DS} by one diode drop to forward bias the diode. Since the drain current density is constant, the gate voltage also remains constant at the gate plateau voltage. Consequently

$$J_{GP} = \frac{V_{GP}}{R_{G,SP}} \tag{9.31}$$

where $R_{G,SP}$ is the specific gate resistance. Since all the gate current is used to discharge the gate-drain capacitance during the plateau phase because there is no change in the voltage across the gate-source capacitance

$$J_{GP} = C_{GD,SP}\frac{dv_D}{dt} \tag{9.32}$$

where $C_{GD,SP}$ is the specific gate transfer capacitance of the power MOSFET structure which is a function of the drain voltage. This voltage dependence of the gate transfer capacitance was not taken into account in the derivation provided in the textbook but is important to include here to allow comparison of the behavior of various power MOSFET structures.

For simplicity of analysis, it will be assumed that any screening effect can be ignored. The gate transfer capacitance for the shielded planar 4H-SiC power MOSFET structure is then given by

$$C_{GD,SP} = \frac{(W_G - W_J)}{W_{Cell}}\left(\frac{C_{OX}C_{S,M}}{C_{OX} + C_{S,M}}\right) \tag{9.33}$$

Using this expression in (9.32) yields the following differential equation for the voltage increase phase of the turn-off transient

$$dt = \left(\frac{W_G - W_J}{W_{Cell}}\right)\frac{1}{J_{GP}}\left[\frac{C_{GOX}}{\sqrt{1 + \frac{2v_D(t)C_{GOX}^2}{q\,\varepsilon_S N_D}}}\right]dv_D \tag{9.34}$$

Integration of this equation yields

$$(t - t_4) = \left(\frac{W_G - W_J}{W_{Cell}}\right)\frac{4q\varepsilon_S N_D}{J_{GP}C_{GOX}}\left[\sqrt{1+\frac{2v_D(t)C_{GOX}^2}{q\ \varepsilon_S N_D}} - \sqrt{1+\frac{2V_{ON}C_{GOX}^2}{q\ \varepsilon_S N_D}}\right] \quad (9.35)$$

In the case of the shielded planar 4H-SiC power MOSFET structure, the drain voltage increases from the on-state voltage drop (V_{ON}) until it reaches the drain-supply voltage (V_{DS}). The voltage rise-time, i.e. the time taken for the voltage to increase from the on-state voltage drop (V_{ON}) to the drain supply voltage (V_{DS})

$$t_{V,OFF} = (t_5 - t_4) = \left(\frac{W_G - W_J}{W_{Cell}}\right)\frac{4q\varepsilon_S N_D}{J_{GP}C_{GOX}}\left[\sqrt{1+\frac{2V_{DS}C_{GOX}^2}{q\ \varepsilon_S N_D}} - \sqrt{1+\frac{2V_{ON}C_{GOX}^2}{q\ \varepsilon_S N_D}}\right] \quad (9.36)$$

A closed form solution for the rise in the drain voltage can be obtained from (9.35)

$$v_D(t) = \frac{q\varepsilon_S N_D}{2C_{GOX}^2}\left\{\left[\frac{J_{GP}C_{GOX}}{4q\ \varepsilon_S N_D}\left(\frac{W_{Cell}}{W_G - W_J}\right)(t - t_4) + \sqrt{1+\frac{2V_{ON}C_{GOX}^2}{q\ \varepsilon_S N_D}}\right]^2 - 1\right\} \quad (9.37)$$

This equation describes the increase in the drain voltage from the on-state voltage drop until it reaches the drain supply voltage. The drain voltage has an approximately quadratic shape as a function of the time after t_4.

At the end of the plateau phase (at time t_5), the load current begins to transfer from the power MOSFET device to the free wheeling diode. Since the drain voltage remains constant, the gate-drain capacitance can also be assumed to remain constant during this phase. The current flowing through the gate resistance (R_G) discharges both the gate-drain and gate-source capacitances leading to an exponential fall in gate voltage from the plateau voltage

$$v_G(t) = V_{GP}e^{-(t-t_5)/R_{G,SP}C_{GS}} \quad (9.38)$$

The drain current follows the gate voltage as given by

$$J_D(t) = g_m[v_G(t) - V_{TH}] = \frac{\mu_{ni}C_{OX}}{L_{CH}W_{Cell}}[v_G(t) - V_{TH}]^2 \quad (9.39)$$

The drain current decreases rapidly with time due to the exponential reduction of the gate voltage, as given by (9.38), during the current fall phase. The drain current

becomes equal to zero when the gate voltage reaches the threshold voltage. The current fall time can therefore be obtained from (9.38)

$$t_{I,OFF} = R_{G,SP} C_{GS} \ln\left(\frac{V_{GP}}{V_{TH}}\right) \tag{9.40}$$

Specific capacitances should be used in this expression for computation of the current fall time. Beyond this point in time, the gate voltage decreases exponentially until it reaches zero. The time constant for this exponential decay is different from the initial phase due to the smaller gate-drain capacitance.

The turn-off energy loss per cycle can be obtained using

$$E_{OFF} = \frac{1}{2} J_{ON} V_{DS} \left(t_{V,OFF} + t_{I,OFF}\right) \tag{9.41}$$

under the assumption that the drain current and voltage excursions are approximately linear with time. The energy loss during the voltage rise-time interval is comparable to the energy loss during the current fall-time interval for the shielded planar 4H-SiC power MOSFET structure.

9.1.7.1 Simulation Results

The results of two-dimensional numerical simulations on the turn-off of the 600 V shielded 4H-SiC planar power MOSFET structure are described here. The drain supply voltage was chosen as 400 V for the turn-off analysis. During the turn-off simulations, the gate voltage was reduced to zero with a gate resistance of 1×10^8 Ω μm for the 4 μm half-cell structure, which is equivalent to a specific gate resistance of 4 Ω cm^2. The current density was initially held constant at an on-state current density of 104 A cm^{-2} allowing the drain voltage to rise to the drain supply voltage. The drain voltage was then held constant allowing the drain current density to reduce to zero.

The turn-off waveforms obtained for the 600-V shielded 4H-SiC planar power MOSFET structure by using the numerical simulations are shown in Fig. 9.17. The gate voltage initially reduces to the gate plateau voltage corresponding to the on-state current density. The drain voltage then increases quadratically from the on-state voltage drop to the drain supply voltage as predicted by the analytical model. After this, the drain current reduces exponentially. The drain current fall time is much larger than observed for the silicon devices due to the poor transconductance of the shielded 4H-SiC planar power MOSFET structure. The drain voltage rise-time ($t_5 - t_4$) and the drain current fall time ($t_6 - t_5$) are comparable for the shielded 4H-SiC planar power MOSFET structure. The drain voltage rise-time obtained from the simulations of the 600-V shielded 4H-SiC planar power MOSFET structure is 0.13 μs and the drain current fall-time obtained from the simulations is 0.06 μs. The energy loss per cycle for the shielded 4H-SiC planar

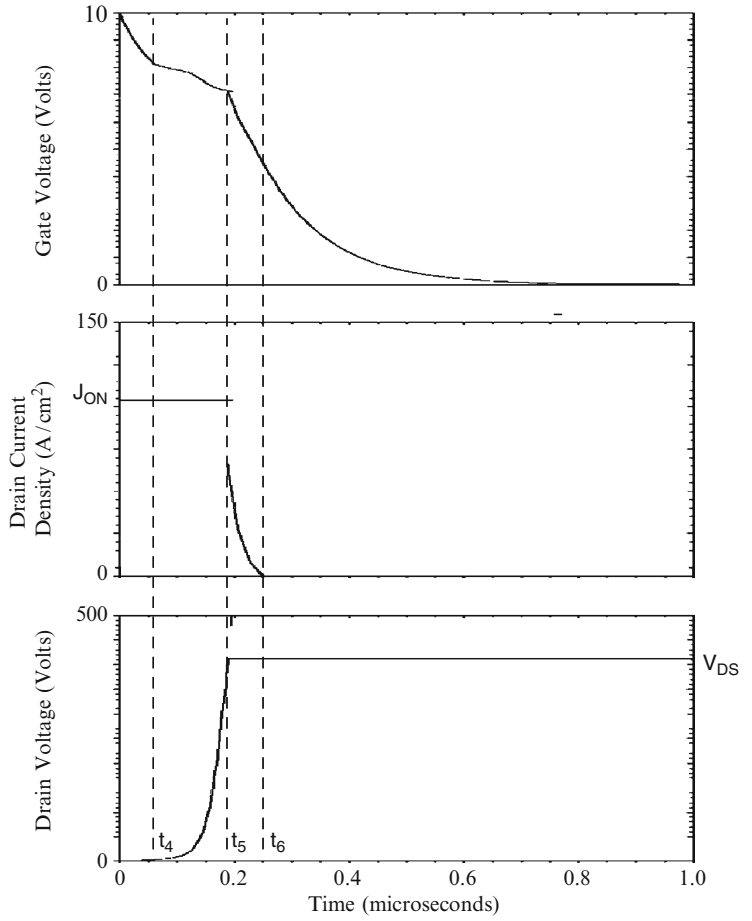

Fig. 9.17 Turn-off waveforms for the 600-V shielded 4H-SiC planar power MOSFET structure

power MOSFET structure computed by using the values from the simulations is 3.95 mJ cm^{-2}. This value is ten-times larger than that observed for the 600-V silicon power SJ-MOSFET structure and twice as large as that observed for the 600-V silicon power GD-MOSFET structure.

9.1.8 Body-Diode Characteristics

The shielded planar 4H-SiC power MOSFET structure has an internal body-diode formed between the P^+ shielding region and the N-drift region. The on-state voltage drop for this body diode is about 3 V compared with 1 V for silicon devices.

Large power loss occurs when the body diode is carrying current in the third quadrant for the shielded planar 4H-SiC power MOSFET structure. Consequently, it is necessary to connect a 4H-SiC Schottky rectifier in anti-parallel with the shielded planar 4H-SiC power MOSFET structure to carry the current in the third quadrant. The Schottky diode can be integrated into the shielded planar 4H-SiC power MOSFET structure. In this case, the P^+ shielding region can be utilized to protect the Schottky contact by forming a junction-barrier controlled Schottky (JBS) rectifier.

9.2 Shielded Planar ACCUFET Structure

The basic structure of the shielded planar ACCUFET structure is shown in Fig. 9.18. Unlike the shielded planar inversion-mode power MOSFET structure, there is no P-base region in this structure. Instead, a lightly doped N-base region is utilized. As in the case of the shielded planar inversion-mode power MOSFET structure, the structure contains a sub-surface P^+ shielding region which extends under both the N^+ source region and the N-base region. The extension of the P^+ shielding region beyond the edge of the N^+ source region defines the channel length. The doping concentration and thickness of the N-base region are chosen so that it is completely depleted by the built-in potential of the junction formed between the P^+ shielding region and the N-base region. This ensures normally-off operation where the device can support a large drain bias voltage when the gate bias voltage is zero.

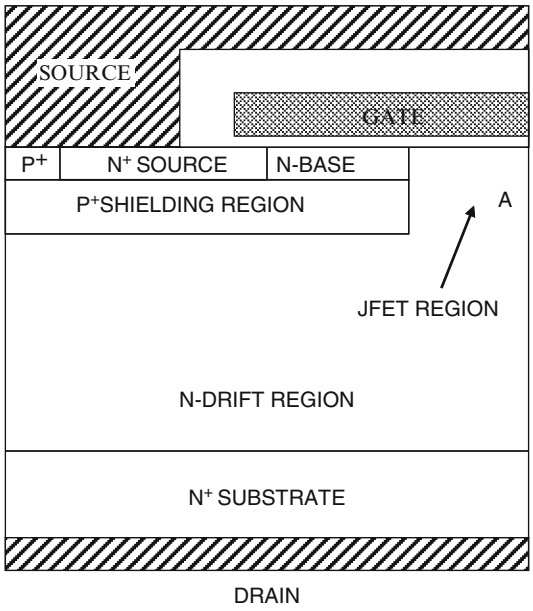

Fig. 9.18 Shielded planar accumulation-mode power MOSFET structure

The space between the P^+ shielding regions, indicated in the figure as the JFET region, is optimized to obtain a low specific on-resistance while simultaneously shielding the gate oxide interface and the N-base region from the high electric field in the drift region. A potential barrier is formed at location A after the JFET region becomes depleted by the applied drain bias in the blocking mode. This barrier prevents the electric field from becoming large at the gate oxide interface.

When a positive bias is applied to the gate electrode, an accumulation layer channel is formed at the surface of the N-base region in the shielded planar accumulation-mode power MOSFET structure enabling the conduction of drain current with a low specific on-resistance. The name for this device derives from the formation of the accumulation layer channel. The specific on-resistance for the shielded planar accumulation-mode power MOSFET structure is less than that for the inversion-mode structure because of a lower threshold voltage and a larger mobility for electrons in an accumulation layer. Since the specific on-resistance for the 4H-SiC planar power MOSFET structure was demonstrated to be limited by the channel resistance, a reduction of the channel resistance achieved with the shielded planar accumulation-mode power MOSFET structure creates devices with superior specific on-resistance.

9.2.1 Blocking Mode

In the forward blocking mode of the silicon carbide shielded planar accumulation-mode power MOSFET structure, the voltage is supported by a depletion region formed on both sides of the P^+ region/N-drift junction. The maximum blocking voltage is determined by the electric field at this junction becoming equal to the critical electric field for breakdown if the parasitic $N^+/P/N$ bipolar transistor is completely suppressed. This suppression is accomplished by short-circuiting the N^+ source and P^+ regions using the source metal as shown on the upper left hand side of the cross-section. If the doping concentration of the P^+ region is large, the reach-through breakdown problem is completely eliminated. In addition, the high doping concentration in the P^+ region promotes the depletion of the JFET region at lower drain voltages providing enhanced shielding of the channel and gate oxide.

In the silicon carbide planar accumulation-mode power MOSFET structure, shielding of the N-base region from the drain potential by the P^+ shielding region allows reducing the channel length to less than 1 μm. In addition, the doping concentration of the N-base region can be adjusted to achieve any desired threshold voltage. The smaller channel length and threshold voltage, as well as the larger mobility for electrons in an accumulation layer, reduce the channel resistance contribution.

As in the case of the planar silicon power D-MOSFET, the maximum blocking voltage capability of the silicon carbide shielded accumulation-mode planar

MOSFET structure is determined by the drift region doping concentration and thickness. However, to fully utilize the high breakdown electric field strength available in silicon carbide, it is necessary to screen the gate oxide from the high field within the semiconductor. In the shielded planar MOSFET structure, this is achieved by the formation of a potential barrier at location A by the depletion of the JFET region at a low drain bias voltage. The maximum electric field in the gate oxide can be made not only below its rupture strength but lower than values required for reliable operation over long time durations.

9.2.1.1 Simulation Results

The results of two-dimensional numerical simulations on the 600 V shielded 4H-SiC planar power ACCUFET structure are described here to provide a more detailed understanding of the underlying device physics and operation during the blocking mode. As in the case of the inversion-mode device structure, the 600-V ACCUFET structure used for the numerical simulations had a drift region thickness of 4 μm below the P^+ shielding region with a doping concentration of 5×10^{16} cm^{-3}. The P^+ region extended from a depth of 0.2 to 1.0 μm with a doping concentration of 1×10^{19} cm^{-3}. The N-base and N^+ source regions were formed within the 0.2 μm of the N-drift region located above the P^+ region. The doping concentration of the N-base region was kept at the same value as the drift region (5×10^{16} cm^{-3}). In general, the doping concentration for the N-base region can be adjusted independently by using the shallow ion-implantation of phosphorus. For the numerical simulations, the cell structure (with a width of 4 μm) illustrated in Fig. 9.18 was utilized as a unit cell that is representative of the structure. Due to high doping concentration in the drift region for the 600-V 4H-SiC devices, the doping concentration in the JFET region was not enhanced as is usually required for silicon devices.

A three dimensional view of the doping distribution in the 600 V shielded 4H-SiC planar power ACCUFET structure is shown in Fig. 9.19 with the upper surface of the structure located on the right hand side in order to display the doping concentration in the vicinity of the channel. The highly doped P^+ shielding region is prominently located just below the surface. The N-base region can be observed to have a much lower doping concentration. Unlike the inversion-mode device, there is no junction between the N-base region and N-JFET region.

The lateral doping profile taken along the surface of the 600 V shielded 4H-SiC planar power ACCUFET structure is shown in Fig. 9.20. The channel extends from 2 to 3 μm creating a channel length of 1 μm because the P^+ shielding region extends to 3 μm. The doping concentration of the JFET region is the same as that of the N-drift region. The N^+ source region and the P^+ contact region for shorting the source to the base region are visible on the left-hand-side. All the regions were defined with uniform doping with abrupt interfaces between them due to the low diffusion rates for dopants in 4H-SiC material. The vertical doping profile within the 600 V shielded 4H-SiC planar power ACCUFET structure is similar to that previously

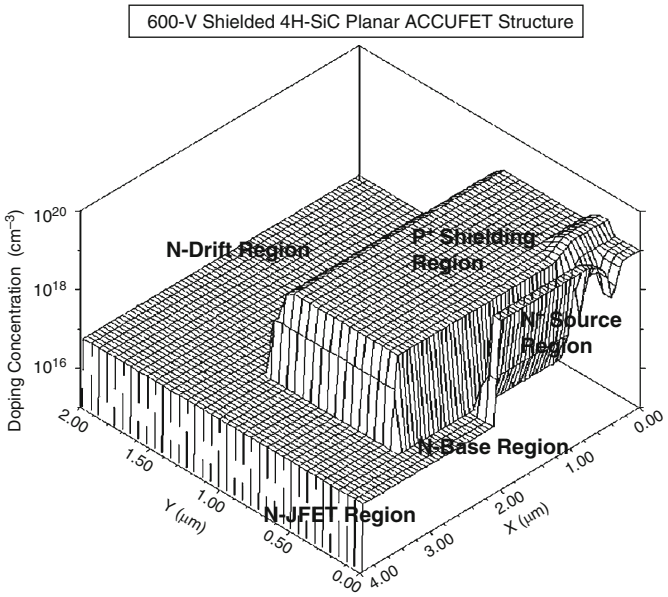

Fig. 9.19 Doping distribution in the shielded 4H-SiC planar power ACCUFET structure

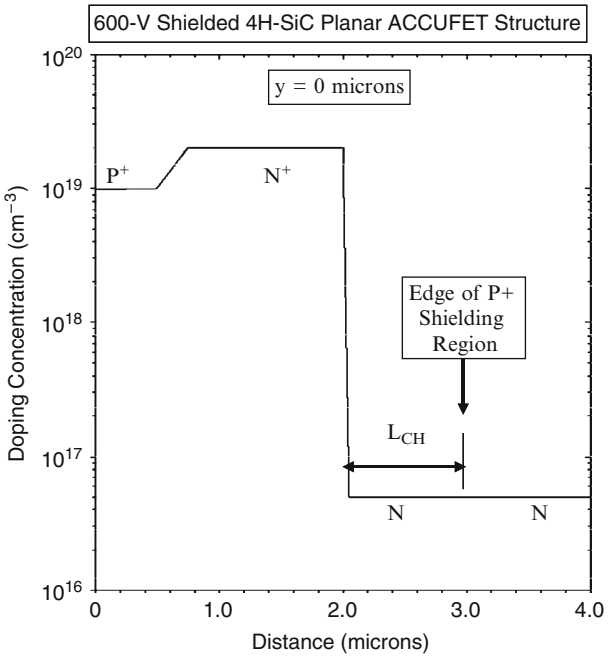

Fig. 9.20 Channel doping profile for the shielded 4H-SiC planar power ACCUFET structure

shown in Fig. 9.4. The N-base region is located between the N^+ source region and the P^+ shielding region with a doping concentration of 5×10^{16} cm^{-3} and thickness of 0.1 μm.

The blocking characteristics for the 600 V shielded 4H-SiC planar power ACCUFET structure were obtained by using zero gate bias. Due to the very small intrinsic concentration in 4H-SiC, no substantial leakage current is observed at room temperature. This also confirms that the bulk channel through of the N-base region has been suppressed due to its depletion by the P^+ shielding region. The potential contours within the shielded 4H-SiC planar power ACCUFET structure at a drain bias of 600 V are provided in Fig. 9.21. It can be observed that there is no junction between the base region and the JFET region in this structure. It can be observed that the drain voltage is supported below the P^+ shielding region. The potential contours do not extend into the N-base region indicating that it is shielded from the drain potential by the P^+ shielding region. The potential contours are crowding at the edge of the P^+ shielding region indicating an enhanced electric field. This can be clearly observed in Fig. 9.22 which provides a three-dimensional view of the electric field distribution. In this figure, it can also be observed that the electric field in the JFET region, and most importantly at the surface under the gate oxide, has been greatly reduced by the presence of the P^+ shielding region.

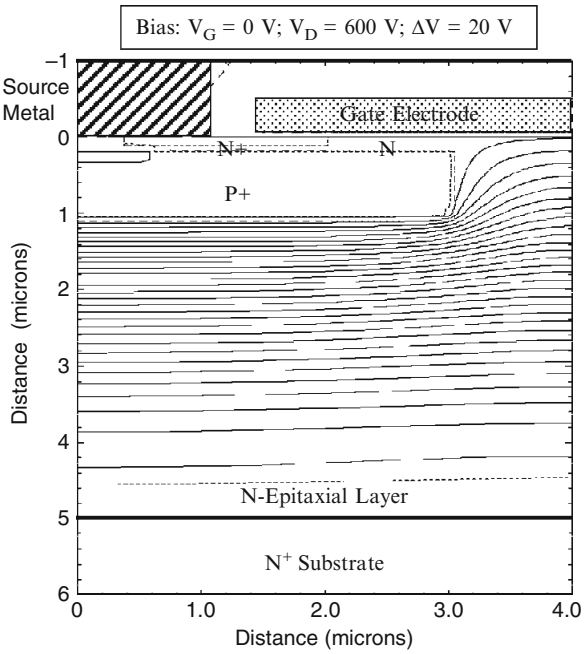

Fig. 9.21 Potential contours in the shielded 4H-SiC planar power ACCUFET structure

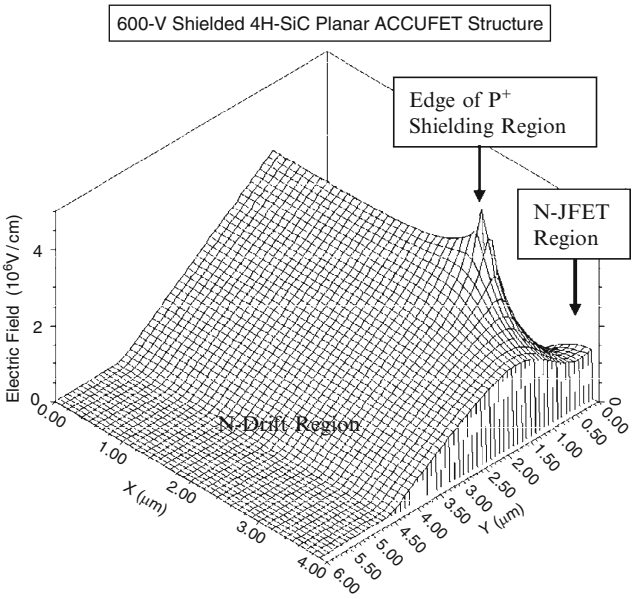

Fig. 9.22 Electric field distribution in the 600-V shielded 4H-SiC planar power ACCUFET structure

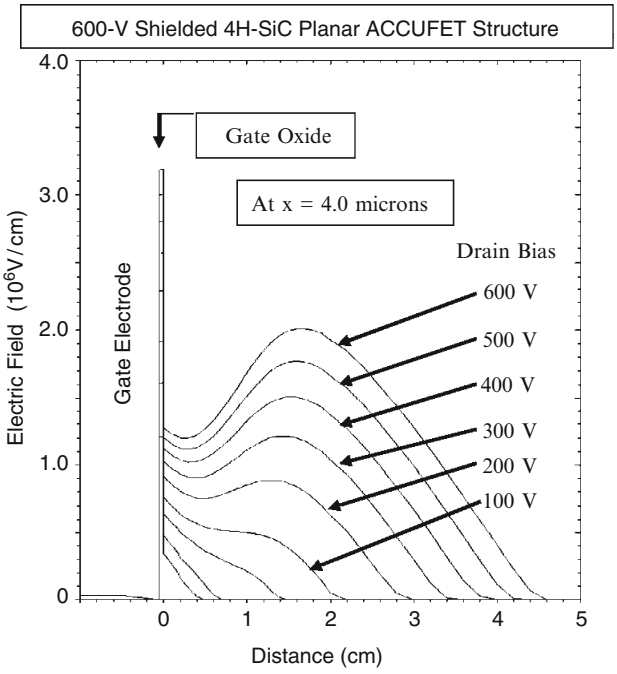

Fig. 9.23 Electric field distribution under the gate in the 600-V shielded 4H-SiC planar power ACCUFET structure

It is insightful to examine the electric field profile in the JFET region within the 600 V shielded 4H-SiC planar power ACCUFET structure when it is operating in the blocking mode. The electric field profiles obtained through the middle of the JFET region are shown in Fig. 9.23 at various drain bias voltages. It can be observed that the maximum electric field in the JFET region occurs at a depth of 1.5 μm from the surface. This reduces the electric field at the surface under the gate oxide to about one-third of the electric field in the bulk below the P^+ shielding region. Consequently, the electric field in the gate oxide is reduced to about 3×10^6 V/cm. The low electric field in the gate oxide for the 600 V shielded 4H-SiC planar power ACCUFET structure prevents gate oxide rupture and allows stable device performance over long periods of time. An even further reduction of electric field in the gate oxide can be achieved by reducing the width of the JFET region at the expense of an increase in the on-resistance.

The results of the numerical simulations on the blocking characteristics of the 600 V shielded 4H-SiC planar power ACCUFET structure demonstrate that the structure behaves in a similar manner to the inversion-mode device. This allows taking advantage of an accumulation-mode channel for reducing the channel resistance.

9.2.2 Threshold Voltage

As discussed in the previous section, the threshold voltage for high voltage power MOSFET devices must be kept at about 2 V in order to obtain a low channel resistance contribution. This is difficult to achieve with an inversion-mode channel in silicon carbide devices. The band bending required to create a channel in the accumulation-mode planar MOSFET is much smaller than required for the inversion mode device. This provides the opportunity to reduce the threshold voltage while obtaining the desired normally-off device behavior. A model for the threshold voltage of accumulation-mode MOSFET structures has been developed [7] using the electric field profile shown in Fig. 9.24 when the gate is biased at the threshold voltage.

In Fig. 9.24, the electric fields in the semiconductor and oxide are given by

$$E_1 = \frac{V_{bi}}{W_N} - \frac{qN_D W_N}{2\varepsilon_S} \tag{9.42}$$

$$E_2 = \frac{V_{bi}}{W_N} + \frac{qN_D W_N}{2\varepsilon_S} \tag{9.43}$$

$$E_{ox} = \frac{\varepsilon_S}{\varepsilon_{ox}} E_1 \tag{9.44}$$

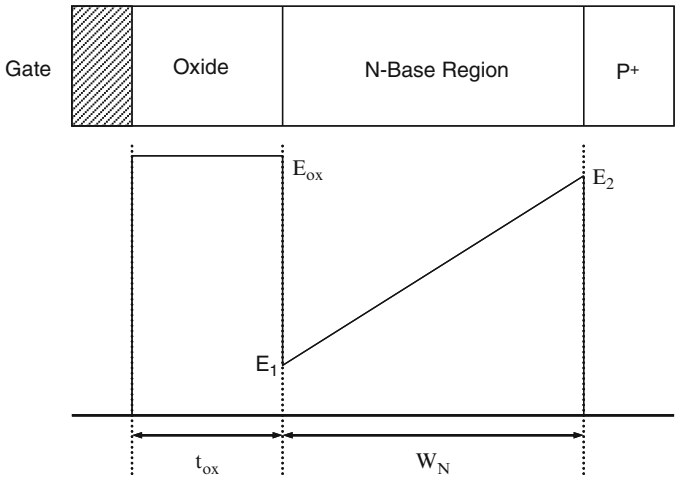

Fig. 9.24 Electric field profile for the accumulation-mode MOSFET structure

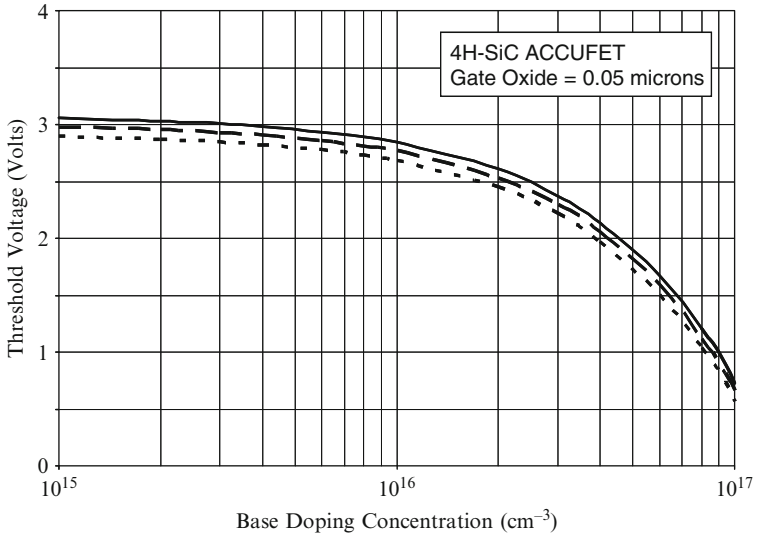

Fig. 9.25 Threshold voltage of the 4H-SiC ACCUFET structure (*solid line*: 300°K; *dash line*: 400°K; *dotted line*: 500°K)

Note that this model is based upon neglecting any voltage supported within the P^+ region under the assumption that it is very heavily doped. Using these electric fields, the threshold voltage is found to be given by

$$V_{TH} = \phi_{MS} + \left(\frac{\varepsilon_S V_{bi}}{\varepsilon_{ox} W_N} - \frac{q N_D W_N}{2\ \varepsilon_{ox}} \right) t_{ox} \tag{9.45}$$

The first term in this equation accounts for the work function difference between the gate material and the lightly doped N-base region. The second term represents the effect of the built-in potential of the P^+/N junction that depletes the N-base region.

The analytically calculated threshold voltage for 4H-SiC accumulation-mode MOSFET structure are provided in Fig. 9.25 for the case of a gate oxide thickness of 0.05 μm, and N-base thickness of 0.2 μm as a function of the N-base doping concentration with the inclusion of a metal-semiconductor work-function difference of 1 V. A strikingly obvious difference from the behavior of inversion-mode devices is a decrease in the threshold voltage for the accumulation-mode structure with increasing doping concentration in the N-base region. This occurs due to the declining influence of the built-in potential of the P^+/N junction at the gate oxide interface when the doping concentration of the N-base region is increased. Of course, the most important benefit of the accumulation-mode structure is that lower threshold voltages can be achieved than in the inversion-mode structures. For the chosen thickness of the N-base region, the desired threshold voltage of 2 V can be obtained for the accumulation-mode structure by using an N-base doping concentration of 5×10^{16} cm^{-3}.

9.2.3 On-State Resistance

The current flow path in the silicon carbide shielded accumulation-mode planar MOSFET structure is identical to that shown in Fig. 9.9 for the shielded inversion-mode planar MOSFET structure. The current flows through the channel formed due to the applied gate bias into the JFET region via the accumulation layer formed above it under the gate oxide. It then spreads into the N-drift region at a 45° angle and becomes uniform through the rest of the structure. The total on-resistance for the silicon carbide shielded accumulation-mode planar SiC MOSFET structure is determined by the resistance of the components in the current path

$$R_{on,sp} = R_{CH} + R_A + R_{JFET} + R_D \tag{9.46}$$

where R_{CH} is the channel resistance, R_A is the accumulation region resistance, R_{JFET} is the resistance of the JFET region, R_D is the resistance of the drift region after taking into account current spreading from the JFET region. For consistency with previous chapters, the resistance of the N^+ substrate has been omitted in the above analysis even though the substrate contribution for 4H-SiC can be very large unless its thickness is reduced to below 50 μm.

The resistances in the shielded accumulation-mode planar MOSFET structure can be analytically modeled by using the current flow pattern indicated by the shaded regions in Fig. 9.9. With the exception of the channel, all the other

resistance components are identical to those already provided for the shielded inversion-mode planar MOSFET structure in the previous section. Consequently, only the channel resistance component will be analyzed in this section for the shielded accumulation-mode planar MOSFET structure. The impact of the improved channel resistance on the total specific on-resistance of the shielded accumulation-mode planar MOSFET structure is also provided here.

9.2.3.1 Channel-Resistance

For the shielded accumulation-mode planar MOSFET structure with the N-base region, the specific channel resistance is given by

$$R_{CH} = \frac{(L_{CH} W_{Cell})}{2\ \mu_{acc} C_{ox} (V_G - V_{TH})} \tag{9.47}$$

where L_{CH} is the channel length as shown in Fig. 9.9, μ_{acc} is the mobility for electrons in the accumulation layer channel, C_{ox} is the specific capacitance of the gate oxide, V_G is the applied gate bias, and V_{TH} is the threshold voltage. Accumulation layer mobility values ranging from of 100 to 200 cm^2/V-s have been observed in lateral MOSFET structures [6]. The relatively high accumulation layer mobility, together with a smaller threshold voltage, reduces the channel resistance component in the shielded planar ACCUFET structure.

In the case of the 600 V shielded planar ACCUFET structure, the cell width will be assumed to be 8 μm with a channel length of 1 μm. The threshold voltage for the accumulation-mode structure is 2 V based up on using a doping concentration of 5×10^{16} cm^{-3} for the N-base region. Using a gate oxide thickness is 500 Å and an inversion layer mobility of 180 cm^2/V-s in the above equation, the specific resistance contributed by the channel at a gate bias of 10 V is found to be 0.407 mΩ cm^2. This value is an order of magnitude smaller than that for the inversion-mode structure.

9.2.3.2 Total On-Resistance

The total specific on-resistance for the 600-V shielded planar 4H-SiC ACCUFET structure with a cell width of 8 μm and JFET width of 2 μm is obtained by adding all the components of the resistances within the device structure. For a gate bias of 10 V, the total specific on-resistance is found to be 0.767 mΩ cm^2. The channel resistance constitutes only 53% of the total specific on-resistance due to the improved mobility for the electrons in the accumulation layer. The specific on-resistance for the 600-V shielded planar 4H-SiC ACCUFET structure is an order of magnitude smaller than that for 600-V shielded planar 4H-SiC MOSFET structure. Consequently, the specific on-resistance for the 600-V shielded planar

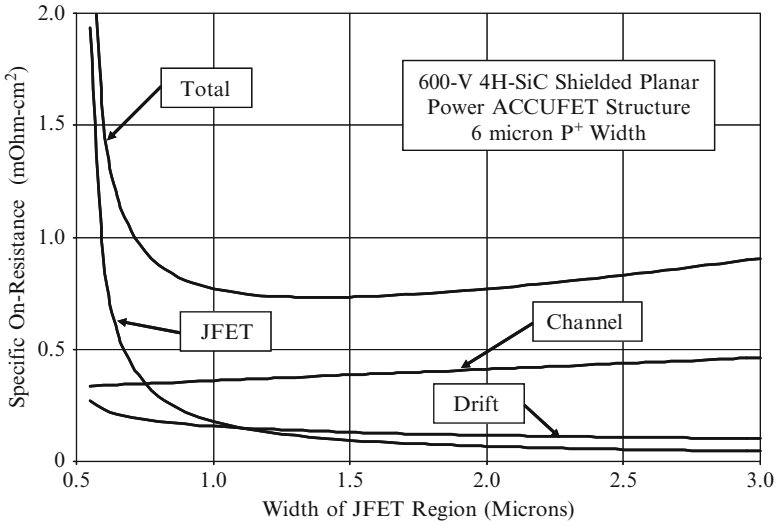

Fig. 9.26 On-resistance for the 600-V 4H-SiC shielded planar ACCUFET structures

4H-SiC ACCUFET structure is two orders of magnitude smaller than that for the silicon 600-V power D-MOSFET and U-MOSFET structures. Even compared with the silicon 600-V GD-MOSFET and SJ-MOSFET structures, the specific on-resistance for the 600-V shielded planar 4H-SiC ACCUFET structure is about five-times smaller. Consequently, the 600-V shielded planar 4H-SiC ACCUFET structure is superior to the best silicon technology because of the improved channel resistance.

The impact of changing the width of the JFET region on the specific on-resistance of the shielded planar 4H-SiC ACCUFET structure can be determined by using the above analytical model. The results obtained for the case of a 600-V device structure with a P^+ shielding region width of 6 μm are provided in Fig. 9.26. For this analysis, an accumulation layer mobility of 180 cm^2/V-s was used. It can be observed that the specific resistance of the channel is now comparable to those of the other components in the structure. The specific on-resistance goes through a minimum at a larger width of the JFET region when compared with the inversion-mode structure due to the larger channel mobility. The JFET width can be optimized between 1 and 2 μm from the point of view of shielding the gate oxide and N-base region from the high electric fields in the drift region.

9.2.3.3 Impact of Breakdown Voltage

The specific on-resistance for the shielded planar 4H-SiC MOSFET structure is plotted in Fig. 9.27 as a function of the breakdown voltage by using the analytical model. In performing the modeling, it is important to recognize that the thickness of

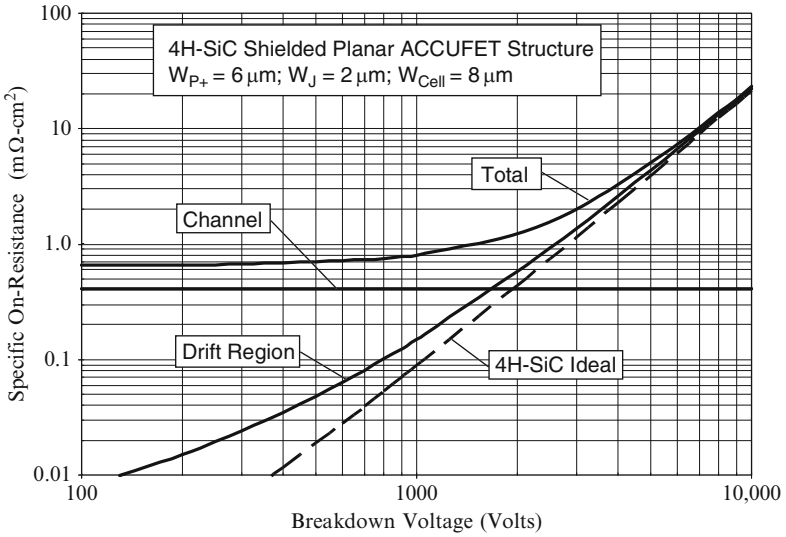

Fig. 9.27 Specific on-resistance for the 4H-SiC shielded planar ACCUFET structure

the drift region (parameter 't' in Fig. 9.9) can become smaller than half the width of the P^+ shielding region at lower breakdown voltages. Under these conditions, the current does not distribute across the entire drift region under the P^+ shielding region. The device parameters used for the plot are: channel inversion mobility of 180 cm^2/V-s; a fixed JFET doping concentration of 5×10^{16} cm^{-3}; a width of 6 μm for the P^+ shielding region; a width of 2 μm for the JFET region; a cell width of 8 μm; gate bias of 10 V; threshold voltage of 2 V; and a gate oxide thickness of 500 Å. From Fig. 9.27, it can be seen that specific on-resistance of 4H-SiC shielded planar ACCUFET structure is limited by the channel resistance for breakdown voltages below 1,000 V. However, the specific on-resistance obtained for the 4H-SiC shielded planar ACCUFET structure is an order of magnitude smaller than that for the 4H-SiC shielded planar MOSFET structure. The drift region resistance can be observed to be close to the ideal specific on-resistance when the breakdown voltage exceeds 1,000 V. The total specific on-resistance of the 4H-SiC shielded planar ACCUFET structure approaches that of the drift region only when the breakdown voltage exceeds 5,000 V.

9.2.3.4 Simulation Results

The results of two-dimensional numerical simulations on the 600-V shielded 4H-SiC planar power MOSFET structure are described here to provide a more detailed understanding of the underlying device physics and operation. The device parameters for the structure used for the numerical simulations were provided in the Sect. 9.2.1.

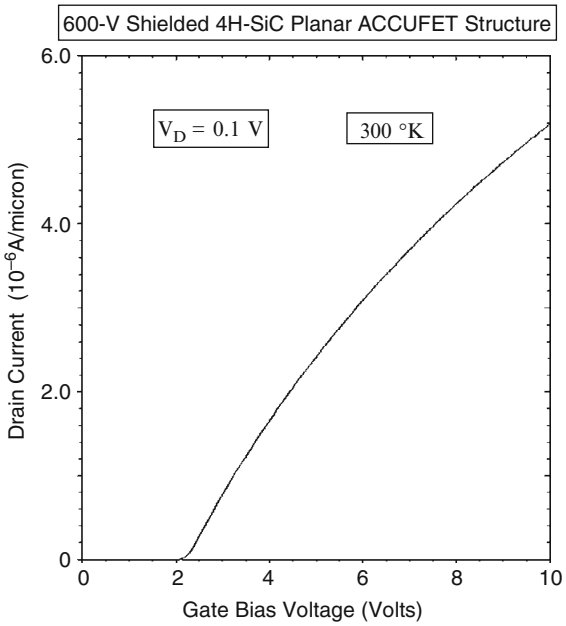

Fig. 9.28 Transfer characteristic of the shielded 4H-SiC planar power ACCUFET structure

The transfer characteristic for the 600-V shielded 4H-SiC planar power ACCUFET structure was obtained using numerical simulations with a drain bias of 0.1 V at 300°K. The channel mobility was adjusted during the simulations to 180 cm^2/V-s. The resulting transfer characteristic is shown in Fig. 9.28. From this graph, a threshold voltage of 2 can be extracted at 300°K. This demonstrates that an optimum threshold voltage can be obtained in the accumulation-mode 4H-SiC power MOSFET structure by proper choice of the doping concentration for the N-base region (5×10^{16} cm^{-3} in this case). The threshold voltage predicted by the analytical model (see Fig. 9.25) is in very good agreement with the value extracted from the numerical simulations. For the case of a gate bias of 10 V and 300°K, the specific in-resistance is found to be 0.772 mΩ cm^2 providing validation of the analytical model. The continuous increase in drain current with gate voltage indicates that the channel resistance is still dominant in the 600-V shielded 4H-SiC planar power ACCUFET structure even though the specific on-resistance has been greatly reduced.

The on-state current flow pattern within the 600-V shielded 4H-SiC planar power ACCUFET structure at a small drain bias of 0.1 V and a gate bias of 10 V is shown in Fig. 9.29. In the figure, the depletion layer boundary is shown by the dotted lines and the junction boundary is delineated by the dashed line. The depletion layer width (W_0) in the JFET region is about 0.25 μm in good agreement with the value computed using the analytical model. It can be observed from this

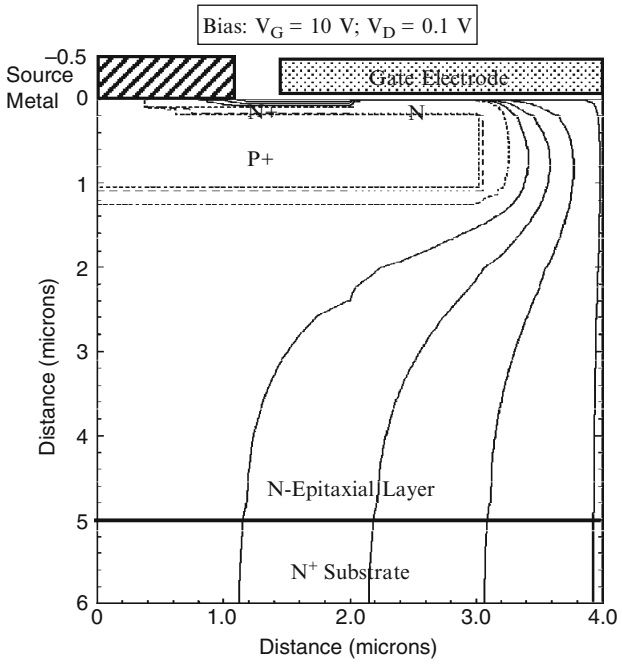

Fig. 9.29 Current distribution in the shielded 4H-SiC planar power ACCUFET structure

figure that the channel current is confined to a very thin accumulation layer formed at the surface. No current flows through the bulk portion of the N-base region demonstrating that the ACCUFET structure is not a bulk channel device. It can also be observed that the current flows from the channel and distributes into the JFET region via the accumulation layer. Within the JFET region, the cross-sectional area is approximately constant with a width (a/2) of 0.75 μm. From the figure, it can be seen that the current spreads from the JFET region to the drift region at a 45° angle as assumed in the model and becomes uniform for the last 1 μm of the drift region.

9.2.4 Capacitances

The capacitances within the shielded planar 4H-SiC ACCUFET structure can be analytically modeled using the same approach as used for the shielded planar 4H-SiC MOSFET structure. The specific input (or gate) capacitance for the shielded planar 4H-SiC ACCUFET structure is given by

$$C_{IN,SP} = C_{N+} + C_P + C_{SM} = \frac{(W_G - W_J)}{W_{Cell}}\left(\frac{\varepsilon_{OX}}{t_{OX}}\right) + \frac{W_G}{W_{Cell}}\left(\frac{\varepsilon_{OX}}{t_{IEOX}}\right) \tag{9.48}$$

where t_{OX} and t_{IEOX} are the thicknesses of the gate and inter-electrode oxides, respectively. For a 600-V shielded planar 4H-SiC power ACCUFET structure with a cell width (W_{CELL} in Fig. 9.9) of 8 μm, JFET region width of 2 μm, and gate electrode width of 5 μm, the specific input capacitance is found to be 30 nF cm^{-2} for a gate oxide thickness of 500 Å and an inter-metal dielectric thickness of 5,000 Å.

The capacitance between the gate and drain electrodes (also called the reverse transfer capacitance) is determined by the width of the JFET region where the gate electrode overlaps the N-drift region. The MOS structure in this portion of the shielded planar 4H-SiC power ACCUFET structure operates under deep depletion conditions when a positive voltage is applied to the drain. The gate-drain capacitance for the shielded planar 4H-SiC ACCUFET power structure is given by

$$C_{GD,SP} = \frac{(W_G - W_J)}{W_{Cell}} \left(\frac{C_{OX} C_{S,M}}{C_{OX} + C_{S,M}} \right) \tag{9.49}$$

where $C_{S,M}$ is the semiconductor capacitance under the gate oxide, which decreases with increasing drain bias voltage. The specific capacitance of the semiconductor depletion region can be obtained by computation of the depletion layer width. The depletion layer width in the semiconductor under the gate oxide can be obtained using

$$W_{D,MOS} = \frac{\varepsilon_S}{C_{OX}} \left\{ \sqrt{1 + \frac{2 V_D C_{OX}^2}{q\, \varepsilon_S N_{DJ}}} - 1 \right\} \tag{9.50}$$

where N_{DJ} is the doping concentration of the JFET region. The specific capacitance for the semiconductor is then obtained using

$$C_{S,M} = \frac{\varepsilon_S}{W_{D,MOS}} \tag{9.51}$$

The gate drain (or reverse transfer) capacitance can be computed by using (9.49) with the above equations until the JFET region is completely depleted. It then abruptly reduces to nearly zero.

The output capacitance for the shielded planar 4H-SiC power ACCUFET structure is associated with the capacitance of the junction between the P^+ shielding region and the N-drift region. Due to pinch-off of the JFET region with increasing drain bias voltage, it is necessary to examine the change in the depletion region boundary with applied voltage. The depletion layer boundary inside the shielded planar 4H-SiC power ACCUFET structure prior to the pinch-off of the JFET region is similar to that previously shown by the dashed lines in Fig. 4.19 for the power SC-MOSFET structure. It can be observed that the depletion region has a vertical boundary inside the JFET region and a horizontal boundary below the P^+ shielding region. The capacitances associated with each of these regions are indicated in the

figure as C_{S1} and C_{S2}. The specific junction capacitance associated with the JFET region is given by

$$C_{S1,SP} = \frac{\varepsilon_S}{W_{DJ}}\left(\frac{2L_{P+}}{W_{Cell}}\right) \tag{9.52}$$

where the depletion region thickness (W_{DJ}) in the JFET region is related to the drain bias voltage

$$W_{DJ} = \sqrt{\frac{2\varepsilon_S(V_D + V_{bi})}{qN_{DJ}}} \tag{9.53}$$

The specific junction capacitance associated with the bottom of the P^+ shielding region is given by [1]

$$C_{S2,SP} = \frac{\varepsilon_S}{W_{DD}}\left(\frac{W_{P+}}{W_{Cell}}\right) \tag{9.54}$$

where the depletion region thickness (W_{DD}) in the drift region is related to the drain bias voltage

$$W_{DD} = \sqrt{\frac{2\varepsilon_S(V_D + V_{bi})}{qN_D}} \tag{9.55}$$

where N_D is the doping concentration of the drift region. The specific output capacitance for the shielded planar 4H-SiC power ACCUFET structure can then be obtained by combining the above values

$$C_{O,SP} = C_{S1,SP} + C_{S2,SP} \tag{9.56}$$

9.2.5 Gate Charge

The gate charge components for the shielded planar 4H-SiC power ACCUFET structure are given by similar equations to those derived for the shielded planar 4H-SiC power MOSFET structure. If the screening effect is neglected, the gate transfer charge corresponding to the transition where the drain voltage changes from V_{DS} to V_{ON} is given by

$$Q_{GD} = \frac{2K_G q\varepsilon_S N_D}{C_{OX}}\left[\sqrt{1+\frac{2V_{DS}C_{OX}^2}{q\ \varepsilon_S N_D}} - \sqrt{1+\frac{2V_{ON}C_{GOX}^2}{q\ \varepsilon_S N_D}}\right] \tag{9.57}$$

where the parameter K_G is given by

$$K_G = \frac{(W_G - W_J)}{W_{Cell}} \tag{9.58}$$

The other components of the gate charge are similar to those already provided in the textbook [3]

$$Q_{SW} = Q_{GS2} + Q_{GD} \tag{9.59}$$

$$Q_G = [C_{GS} + C_{GD}(V_{DS})]V_{GP} + Q_{GD} + [C_{GS} + C_{GD}(V_{ON})](V_G - V_{GP}) \tag{9.60}$$

Equations for the gate voltage, drain current, and drain voltage waveforms for the shielded planar 4H-SiC power ACCUFET structure are similar to those derived in Chap. 4 for the power SC-MOSFET structure. If the screening effect is neglected, the drain voltage is determined by the gate transfer capacitance given by (9.49)

$$v_D(t) = \frac{q\varepsilon_S N_D}{2C_{OX}^2}\left\{\left[\sqrt{1 + \frac{2V_{DS}C_{Ox}^2}{q\ \varepsilon_S N_D}} - \frac{J_G C_{OX}(t - t_2)}{2K_G q\ \varepsilon_S N_D}\right]^2 - 1\right\} \tag{9.61}$$

from $t = t_2$ to $t = t_3$.

9.2.5.1 Simulation Example

The gate charge for the 600-V shielded 4H-SiC planar power ACCUFET structure was extracted by using the results of two-dimensional numerical simulations of the cell described in the previous sections. The device was turned-on from blocking state with a drain bias of 400 V by driving it using a gate current of 1×10^{-8} A/μm (equivalent to 0.25 A cm^{-2} for the area of 4×10^{-8} cm^2). Once the drain current density reached 320 A cm^{-2}, the drain current was held constant resulting in a reduction of the drain voltage. The gate plateau voltage for this drain current density was found to be 3.8 V due to the improved transconductance of the device as a result of the high accumulation layer mobility. Once the drain voltage reached the on-state value corresponding to the gate plateau voltage, the gate voltage increased to the steady-state value of 10 V.

The gate charge waveforms obtained by using an input gate current density of 0.25 A cm^{-2} when turning on the 600-V shielded 4H-SiC planar power MOSFET structure from a blocking state with drain bias of 400 V are shown in Fig. 9.30. The on-state current density is 320 A cm^{-2} at a DC gate bias of 10 V at the end of the turn-on transient. The gate voltage increases at a constant rate at the beginning of the turn-on process as predicted by the analytical model. When the gate voltage reaches the threshold voltage, the drain current begins to increase. The drain current

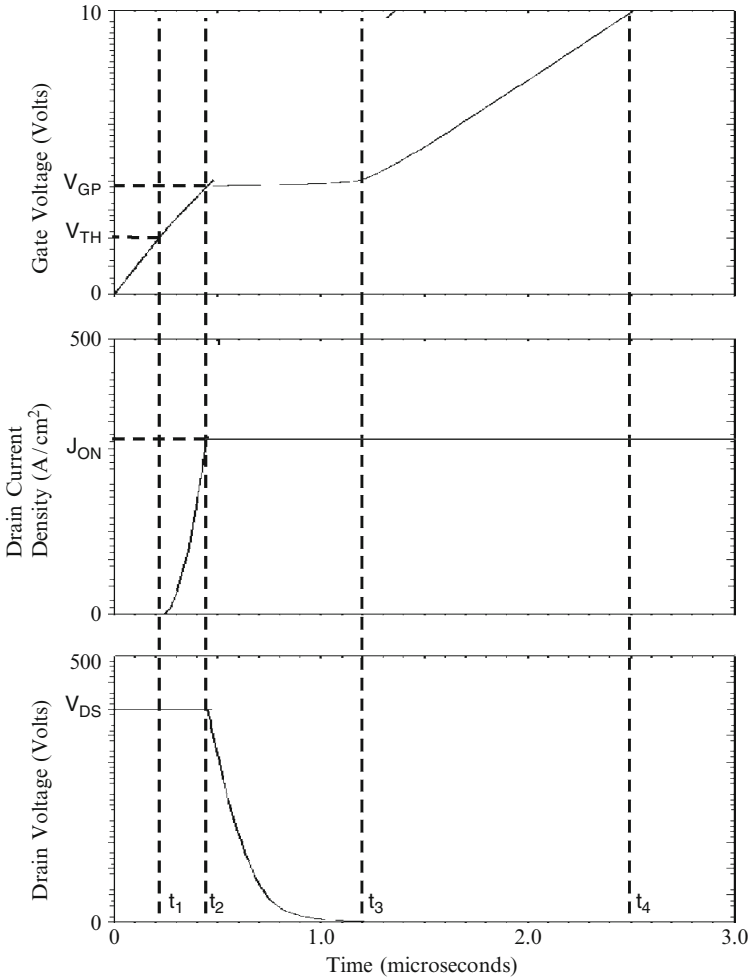

Fig. 9.30 Turn-on waveforms for the 600-V shielded 4H-SiC planar power ACCUFET structure

increases more rapidly than in the case of the inversion-mode structure until it reaches the on-state current density of 320 A cm^{-2} due to the improved transconductance of the device.

Once the drain current reaches the on-state value, the gate voltage remains approximately constant at the plateau voltage (V_{GP}). The plateau voltage for this structure is 3.8 V even for the larger drain current density of 320 A cm^{-2} due to the improved transconductance of the device. The drain voltage drops rapidly from the supply voltage of 400 V of about 50 V (the JFET pinch-off voltage) as predicted by the analytical model. The drain voltage then decreases during the plateau phase in a non-linear manner. After the end of the plateau phase, the gate voltage again increases until it reaches the gate supply voltage.

Specific Gate Charge	Numerical Simulation (nC/cm^2)
Q_{GS1}	53
Q_{GS2}	60
Q_{GS}	113
Q_{GD}	188
Q_{SW}	248
Q_G	625

Fig. 9.31 Gate charge extracted from numerical simulations for the 600-V shielded 4H-SiC planar power ACCUFET structure

The values for the various components of the gate charge extracted from the numerical simulations are provided in Fig. 9.31. These gate transfer charge for the 600-V shielded 4H-SiC planar power ACCUFET structure is close to that of the 600-V D-MOSFET and U-MOSFET structures, and slightly larger than that of the 600-V power GD-MOSFET and SJ-MOSFET structures.

9.2.6 Device Figures of Merit

The figures of merit (defined in the previous chapters of the book) computed for the 600-V shielded planar 4H-SiC power ACCUFET structure are provided in Fig. 9.32. The figure of merit usually used for comparison of device technologies in the literature is FOM(C). In comparison with the 600-V power D-MOSFET and U-MOSFET structures, the 600-V shielded planar 4H-SiC power ACCUFET structure has a FOM(C) that is 150-times smaller. Even in comparison with the 600-V power GD-MOSFET and SJ-MOSFET structures, the 600-V shielded planar 4H-SiC power ACCUFET structure has a FOM(C) that is three-times smaller. Consequently, 600-V shielded planar 4H-SiC power MOSFET structure offers significant improvement in circuit performance compared with the conventional power MOSFET structure and is superior to the new silicon power MOSFET technology based up on the charge coupling concept.

Figures of Merit	V_G = 10 V
FOM(A) ($\Omega^2cm^4s^{-1}$)	25,567
FOM(B)(ps)	23
FOM(C) (mΩ*nC)	144
FOM(D) (mΩ*nC)	190

Fig. 9.32 Figures of merit for the 600-V 4H-SiC shielded planar ACCUFET structures

9.2.7 Inductive Load Turn-Off Characteristics

As discussed in preceding chapters, high voltage power MOSFET devices are often used in adjustable speed motor drives which behave as inductive loads. The operation of the shielded planar 4H-SiC power ACCUFET structure in an inductive load circuit can be analyzed using the same approach as used for the shielded planar 4H-SiC power MOSFET structure. The gate plateau voltage for the shielded planar 4H-SiC power ACCUFET structure is given by

$$V_{GP} = V_{TH} + \sqrt{\frac{J_{D,ON} W_{Cell} L_{CH}}{\mu_{acc} C_{GOX}}} \tag{9.62}$$

where C_{GOX} is the gate oxide capacitance. The time constant for discharging the gate of the shielded planar 4H-SiC power ACCUFET structure is $R_{G,SP}$*[C_{GS} + $C_{GD}(V_{ON})$] and the gate voltage decreases exponentially with time as given by

$$v_G(t) = V_{GS} e^{-t/R_{G,SP}[C_{GS}+C_{GD}(V_{ON})]} \tag{9.63}$$

The time t_4 (using the notation from the textbook) for reaching the gate plateau voltage can be obtained by using this equation with (9.62) for the plateau voltage

$$t_4 = R_{G,SP}[C_{GS} + C_{GD}(V_{ON})] \ln\left[\frac{V_{GS}}{V_{GP}}\right] \tag{9.64}$$

This time can be considered to a *turn-off delay time* before the drain voltage begins to increase after the turn-off is initiated by the control circuit.

The drain voltage begins to increase at time t_4 but the drain current remains constant at the load current I_L because the current cannot be transferred to the diode until the voltage at the drain of the MOSFET device exceeds the supply voltage V_{DS} by one diode drop to forward bias the diode. Since the drain current density is constant, the gate voltage also remains constant at the gate plateau voltage. Consequently

$$J_{GP} = \frac{V_{GP}}{R_{G,SP}} \tag{9.65}$$

where $R_{G,SP}$ is the specific gate resistance. Since all the gate current is used to discharge the gate-drain capacitance during the plateau phase because there is no change in the voltage across the gate-source capacitance

$$J_{GP} = C_{GD,SP} \frac{dv_D}{dt} \tag{9.66}$$

where $C_{GD,SP}$ is the specific gate transfer capacitance of the power MOSFET structure which is a function of the drain voltage. This voltage dependence of the

gate transfer capacitance was not taken into account in the derivation provided in the textbook but is important to include here to allow comparison of the behavior of various power MOSFET structures.

For simplicity of analysis, it will be assumed that any screening effect can be ignored. The gate transfer capacitance for the shielded planar 4H-SiC power ACCUFET structure is then given by

$$C_{GD,SP} = \frac{(W_G - W_J)}{W_{Cell}} \left(\frac{C_{OX} C_{S,M}}{C_{OX} + C_{S,M}} \right) \tag{9.67}$$

Using this expression in (9.66) yields the following differential equation for the voltage increase phase of the turn-off transient

$$dt = \left(\frac{W_G - W_J}{W_{Cell}} \right) \frac{1}{J_{GP}} \left[\frac{C_{GOX}}{\sqrt{1 + \frac{2 v_D(t) C_{GOX}^2}{q \varepsilon_S N_D}}} \right] dv_D \tag{9.68}$$

Integration of this equation yields

$$(t - t_4) = \left(\frac{W_G - W_J}{W_{Cell}} \right) \frac{4q\varepsilon_S N_D}{J_{GP} C_{GOX}} \left[\sqrt{1 + \frac{2 v_D(t) C_{GOX}^2}{q \varepsilon_S N_D}} - \sqrt{1 + \frac{2 V_{ON} C_{GOX}^2}{q \varepsilon_S N_D}} \right] \tag{9.69}$$

In the case of the shielded planar 4H-SiC power ACCUFET structure, the drain voltage increases from the on-state voltage drop (V_{ON}) until it reaches the drain-supply voltage (V_{DS}). The voltage rise-time, i.e. the time taken for the voltage to increase from the on-state voltage drop (V_{ON}) to the drain supply voltage (V_{DS})

$$t_{V,OFF}(t_5 - t_4) = \left(\frac{W_G - W_J}{W_{Cell}} \right) \frac{4q\varepsilon_S N_D}{J_{GP} C_{GOX}} \left[\sqrt{1 + \frac{2 V_{DS} C_{GOX}^2}{q \varepsilon_S N_D}} - \sqrt{1 + \frac{2 V_{ON} C_{GOX}^2}{q \varepsilon_S N_D}} \right] \tag{9.70}$$

A closed form solution for the rise in the drain voltage can be obtained from (9.69)

$$v_D(t) = \frac{q\varepsilon_S N_D}{2 C_{GOX}^2} \left\{ \left[\frac{J_{GP} C_{GOX}}{4q \varepsilon_S N_D} \left(\frac{W_{Cell}}{W_G - W_J} \right) (t - t_4) + \sqrt{1 + \frac{2 V_{ON} C_{GOX}^2}{q \varepsilon_S N_D}} \right]^2 - 1 \right\} \tag{9.71}$$

This equation describes the increase in the drain voltage from the on-state voltage drop until it reaches the drain supply voltage. The drain voltage has an approximately quadratic shape as a function of the time after the time t_4.

At the end of the plateau phase (at time t_5), the load current begins to transfer from the power MOSFET device to the free wheeling diode. Since the drain voltage remains constant, the gate-drain capacitance can also be assumed to remain constant during this phase. The current flowing through the gate resistance (R_G) discharges both the gate-drain and gate-source capacitances leading to an exponential fall in gate voltage from the plateau voltage

$$v_G(t) = V_{GP} e^{-(t-t_5)/R_{G,SP}C_{GS}} \tag{9.72}$$

The drain current follows the gate voltage as given by

$$J_D(t) = g_m[v_G(t) - V_{TH}] = \frac{\mu_{ni} C_{OX}}{L_{CH} W_{Cell}} [v_G(t) - V_{TH}]^2 \tag{9.73}$$

The drain current decreases rapidly with time due to the exponential reduction of the gate voltage, as given by (9.72), during the current fall phase. The drain current becomes equal to zero when the gate voltage reaches the threshold voltage. The current fall time can therefore be obtained from (9.72)

$$t_{I,OFF} = R_{G,SP} C_{GS} \ln\left(\frac{V_{GP}}{V_{TH}}\right) \tag{9.74}$$

Specific capacitances should be used in this expression for computation of the current fall time. Beyond this point in time, the gate voltage decreases exponentially until it reaches zero. The time constant for this exponential decay is different from the initial phase due to the smaller (zero) gate-drain capacitance.

The turn-off energy loss per cycle can be obtained using

$$E_{OFF} = \frac{1}{2} J_{ON} V_{DS} \left(t_{V,OFF} + t_{I,OFF}\right) \tag{9.75}$$

under the assumption that the drain current and voltage excursions are approximately linear with time. The energy loss during the voltage rise-time interval is comparable to the energy loss during the current fall-time interval for the shielded planar 4H-SiC power MOSFET structure.

9.2.7.1 Simulation Results

The results of two-dimensional numerical simulations on the turn-off of the 600 V shielded 4H-SiC planar power MOSFET structure are described here. The drain

supply voltage was chosen as 400 V for the turn-off analysis. During the turn-off simulations, the gate voltage was reduced to zero with a gate resistance of $1 \times 10^8\ \Omega\ \mu m$ for the 4 μm half-cell structure, which is equivalent to a specific gate resistance of $4\ \Omega\ cm^2$. The current density was initially held constant at an on-state current density of 360 A cm^{-2} allowing the drain voltage to rise to the drain supply voltage. The drain supply voltage was then held constant allowing the drain current density to reduce to zero.

The turn-off waveforms obtained for the 600-V shielded 4H-SiC planar power ACCUFET structure by using the numerical simulations are shown in Fig. 9.33. The gate voltage initially reduces to the gate plateau voltage corresponding to the on-state current density. The drain voltage then increases quadratically from the on-

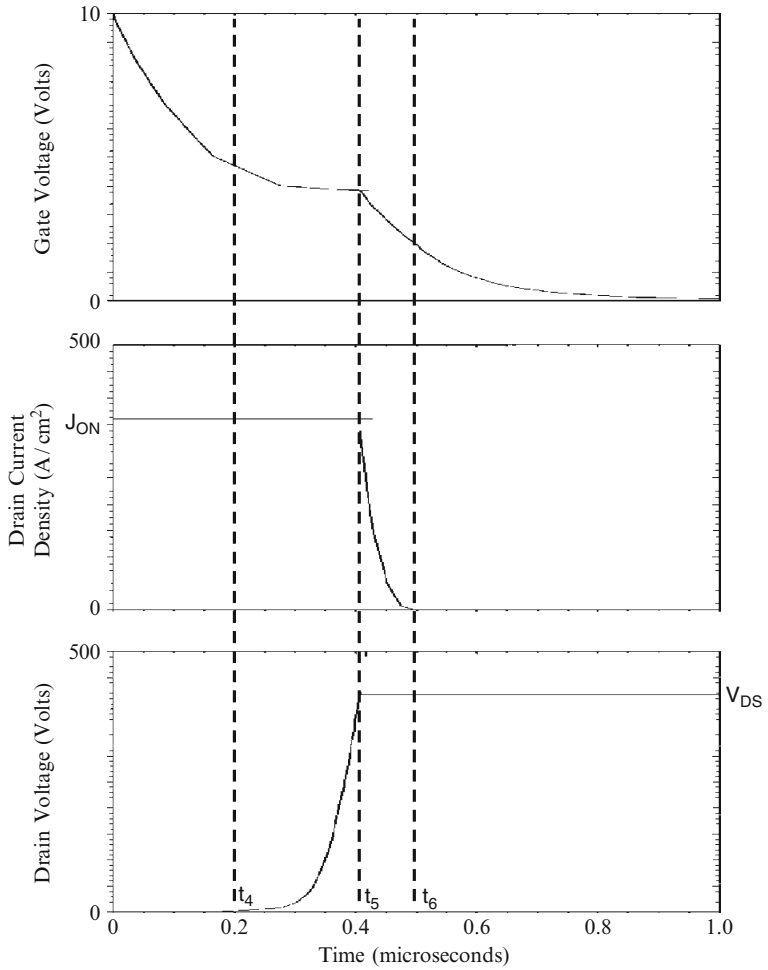

Fig. 9.33 Turn-off waveforms for the 600-V shielded 4H-SiC planar power ACCUFET structure

state voltage drop to the drain supply voltage as predicted by the analytical model to the drain supply voltage. After this, the drain current reduces exponentially. The drain voltage rise-time ($t_5 - t_4$) and the drain current fall time ($t_6 - t_5$) are comparable for the shielded 4H-SiC planar power ACCUFET structure. The drain voltage rise-time obtained from the simulations of the 600-V shielded 4H-SiC planar power ACCUFET structure is 0.21 μs and the drain current fall-time obtained from the simulations is 0.09 μs. The energy loss per cycle for the shielded 4H-SiC planar power MOSFET structure computed by using the values from the simulations is 21.6 mJ cm^{-2}. This value is much larger than that observed for the 600-V silicon power SJ-MOSFET structure and the 600-V silicon power GD-MOSFET structure.

9.2.8 Body-Diode Characteristics

The shielded planar 4H-SiC power ACCUFET structure has an internal body-diode formed between the P^+ shielding region and the N-drift region. The on-state voltage drop for this body diode is about 3 V compared with 1 V for silicon devices. A large power loss would occur when this body diode is carrying current in the third quadrant for the shielded planar 4H-SiC power ACCUFET structure. However, as the forward bias for the junction between the P^+ shielding region and the N-drift region increases, the depletion width in the N-base region, at its junction with the P^+ shielding region, shrinks. The reduction of the depletion region opens a bulk current conduction path in the N-base region which bypasses the junction. The on-state voltage drop for the current flow in the third quadrant for the shielded planar 4H-SiC power ACCUFET structure can therefore become smaller than the typical on-state voltage drop of 3 V for the P-N junction. The suppression of minority carrier injection by the junction due to the alternate current path also improves the reverse recovery performance of the 'body-diode'.

9.2.8.1 Simulation Results

The results of two-dimensional numerical simulations on the operation of the 600-V shielded 4H-SiC planar power ACCUFET structure in the third quadrant are described here to provide a more detailed understanding of the underlying device physics and operation. The device parameters for the structure used for the numerical simulations were provided in the Sect. 9.2.1.

The forward $i-v$ characteristic for the 'body-diode' in the 600-V shielded 4H-SiC planar power ACCUFET structure was obtained using numerical simulations with zero gate bias. A lifetime (τ_{n0} and τ_{p0}) of 1 μs was used for the simulations as representative of the quality of recent epitaxial layers. The resulting characteristic is shown in Fig. 9.34 by the solid line. For comparison purposes, the $i-v$ characteristic for the body-diode in the 600-V shielded 4H-SiC planar power MOSFET structure is also shown in the figure by the dashed line. It can be observed that the on-state

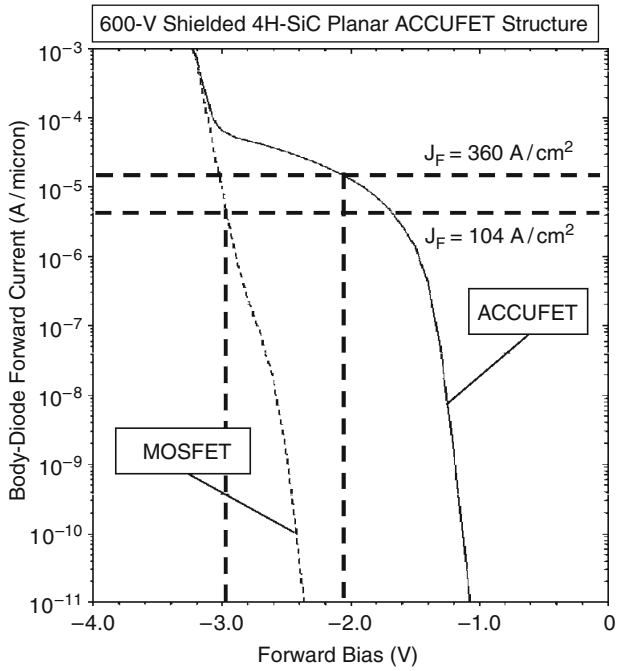

Fig. 9.34 Forward characteristic of the body-diode within the shielded 4H-SiC planar power ACCUFET structure

voltage drop for the body-diode in this device is 3 V at its on-state current density of 104 A cm^{-2}. From this graph, it can be observed that the $i-v$ characteristic for the 600-V shielded 4H-SiC planar power ACCUFET structure is shifted towards the right-hand-side. The on-state voltage drop at the on-state current density of 360 A cm^{-2} for this device is only 2.04 V. An inflection in the $i-v$ characteristics occurs when the drain bias exceed 3 V due to the on-set of current flow across the P-N junction in the 600-V shielded 4H-SiC planar power ACCUFET structure.

The hole concentration profile in the 600-V shielded 4H-SiC planar power ACCUFET structure is shown in Fig. 9.35 when the body diode is forward biased with a current density of 360 A cm^{-2}. A lifetime of 1 μs was used for these simulations. It can be observed that there are no holes injected into the N-type drift region under these conditions. In contrast, the injected hole concentration in the drift region for the 600-V shielded 4H-SiC planar power MOSFET structure was found to be approximately equal to the doping concentration. Based up on these results, it can be concluded that the injection of minority carriers is suppressed within the shielded 4H-SiC planar power ACCUFET structure. This is an unusual feature that is unique to the ACCUFET structure.

The current path for the 'body diode' in the 600-V shielded 4H-SiC planar power ACCUFET structure, when it is forward biased by a negative drain bias, is shown in Fig. 9.36. It can be observed that the current flow lines by-pass the junction between

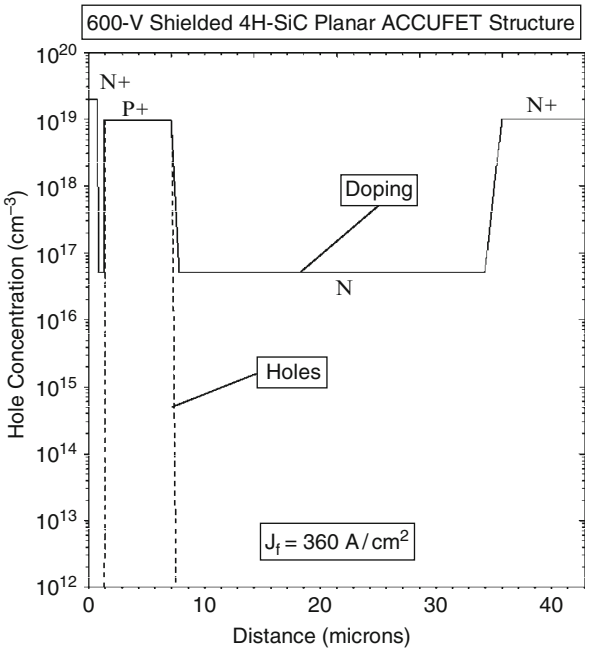

Fig. 9.35 Hole distribution in the 600-V shielded 4H-SiC planar power ACCUFET structure

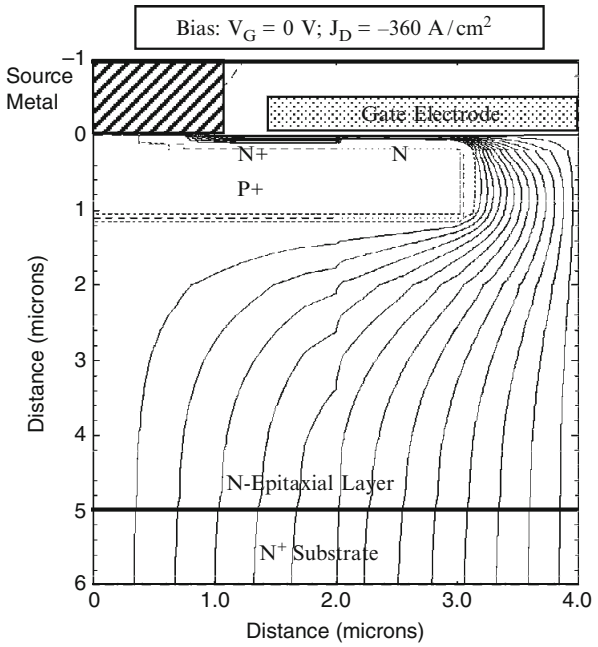

Fig. 9.36 Body diode current path within the 600-V shielded 4H-SiC planar power ACCUFET structure

the P^+ shielding region and the N-drift region. Instead, the current flows through the N-base region at the upper surface. In comparison with the on-state current flow during operation in the first quadrant (Fig. 9.29), the depletion width at the junction is much narrower and the current flow-lines spread down from the semiconductor surface. These features confirm the hypothesis that unipolar current flow occurs in the shielded 4H-SiC planar power ACCUFET structure through its N-base region during operation in the third quadrant.

The reverse recovery characteristic for the body diode in the 600-V shielded 4H-SiC planar power ACCUFET structure was obtained by initially forward biasing the body diode with an on-state current density of 360 A cm^{-2} corresponding with a on-state power dissipation of 100 W cm^{-2} based up on the specific on-resistance of this structure. For comparison purposes, the reverse recovery characteristic for the body-diode in the 600-V shielded 4H-SiC planar power MOSFET structure, with initially forward biasing the body diode with an on-state current density of 104 A cm^{-2} corresponding with a on-state power dissipation of 100 W cm^{-2} based up on its specific on-resistance, is also provided in the figure (dashed line). A lifetime of 1 μs was used for these simulations. For both structures, the drain current was ramped from negative to positive at a ramp rate of 3,300 A cm^{-2}-μs. The resulting waveforms for the drain current and drain voltage are shown in Figs. 9.37 and 9.38. It can be observed that the peak reverse recovery current

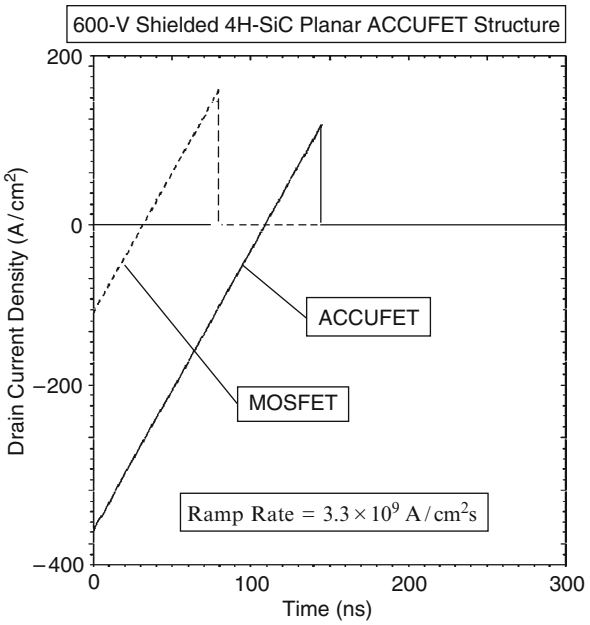

Fig. 9.37 Reverse recovery current of the body diode within the 600-V shielded 4H-SiC planar power ACCUFET structure

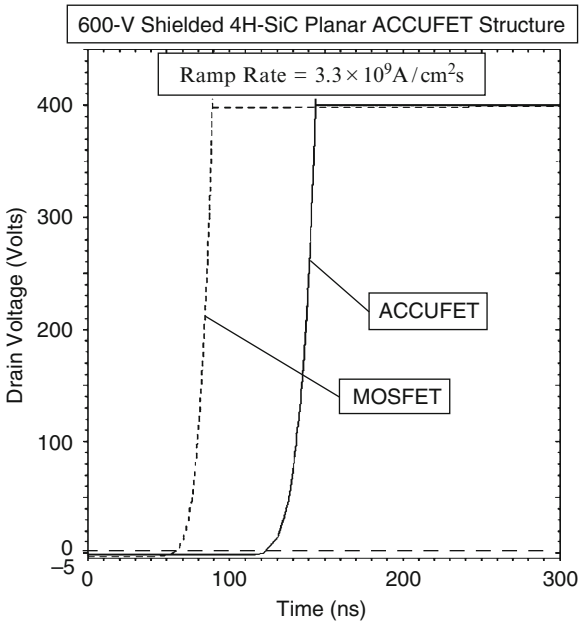

Fig. 9.38 Reverse recovery voltage of the body diode within the 600-V shielded 4H-SiC planar power ACCUFET structure

density (J_{PR}) for the 600-V shielded 4H-SiC planar power ACCUFET structure is 117 A cm^{-2}. This value is only one-third of the on-state current density. In contrast, the peak reverse recovery current density (J_{PR}) for the 600-V shielded 4H-SiC planar power MOSFET structure is 156 A cm^{-2}. This value is 1.5-times the on-state current density. Based up on these results, it is clear that the shielded 4H-SiC planar power ACCUFET structure has a much superior ($\sim$ five-times) integral diode.

9.3 Discussion

The characteristics of the 600-V shielded planar 4H-SiC power MOSFET structure have been reviewed in this chapter. It is demonstrated that the specific on-resistance of the device is dominated by the channel resistance if a typical channel inversion layer mobility of 10–20 cm^2/V-s is assumed. The resulting specific on-resistance, although an order of magnitude smaller than the conventional silicon power MOSFET structures, is not competitive with the silicon power MOSFET structures that utilize charge-coupling. Moreover, the P-N body-diode in the structure has a relatively large on-state voltage drop and poor reverse recovery characteristics.

In contrast, it is demonstrated that the specific on-resistance of the 600-V shielded planar 4H-SiC power ACCUFET structure is an order of magnitude smaller than that

of the inversion-mode structure. This is primarily due to the much larger mobility for electrons in an accumulation layer. The specific on-resistance for the 600-V shielded planar 4H-SiC power ACCUFET structure is found to be smaller than that obtained even for the silicon devices with charge-coupling.

A new mode of operation for current flow in the third quadrant is reported here for the first time for the shielded planar 4H-SiC power ACCUFET structure. This current flow occurs via the N-base region by-passing the P-N junction. Consequently, the on-state voltage drop of the 'body-diode' is reduced and minority carrier injection is completely suppressed. The reverse recovery characteristics for the 600-V shielded planar 4H-SiC power ACCUFET structure are much superior to those for the inversion-mode device.

The performance of the integral diode within the silicon carbide structures is summarized in Figs. 9.39 and 9.40 for the case of a lifetime of 1 μs in the drift region. The on-state voltage drop provided in the Fig. 9.39 is for the integral diode and in Fig. 9.40 for the MOSFET mode. From the information in the above figures, it can be concluded that the 600-V shielded planar 4H-SiC power ACCUFET structure offers the best performance. It has an exceptionally small specific on-resistance which allows operation at a high on-state current density. The chip area required to serve any application is proportionately reduced. The ratio of the peak reverse recovery current to the on-state current density for this device is much lower than for all of the 600-V power MOSFET structures discussed in the previous chapters. The figures-of-merit for the 600-V shielded planar 4H-SiC power ACCUFET structure are also an order of magnitude superior to those of the best silicon power MOSFET structures discussed in the previous chapters.

Device Structure	$R_{DSON,\,SP}$ ($m\Omega$-cm^2)	J_{ON} (A/cm^2)	V_{ON} (V)	J_{RR} (A/cm^2)	J_{RR}/J_{ON}	FOM(E) (V)
MOSFET	9.20	104	2.96	156	1.50	1.44
ACCUFET	0.77	360	2.04	117	0.325	0.091

Fig. 9.39 Integral diode parameters for the 600-V shielded 4H-SiC structures

Device Structure	$R_{DSON,SP}$ ($m\Omega$-cm^2)	J_{ON} (A/cm^2)	V_{ON} (V)	Q_{RR} ($\mu C/cm^2$)	Q_{RR}/J_{ON} (μs)	FOM(F) (nV-s)
MOSFET	9.20	104	0.96	3.69	0.0355	33.95
ACCUFET	0.77	360	0.28	2.08	0.0058	1.60

Fig. 9.40 Integral diode parameters for the 600-V shielded 4H-SiC structures

References

1. B.J. Baliga, “Silicon Carbide Power Devices”, World Scientific, Singapore, 2005.
2. B.J. Baliga, “Silicon Carbide Semiconductor Devices having Buried Silicon Carbide Conduction Barrier Layers Therein”, U. S. Patent 5,543,637, Issued August 6, 1996.
3. B.J. Baliga, “Fundamentals of Power Semiconductor Devices”, Springer-Science, New York, 2008.
4. S. Sridevan and B.J. Baliga, “Lateral N-channel Inversion Mode 4H-SiC MOSFETs”, IEEE Electron Device Letters, Vol. 19, pp. 228–230, 1998.
5. S.H. Ryu, et al., “10-kV 5-A 4H-SiC Power DMOSFET”, IEEE International Symposium on Power Semiconductor Devices, Abstract 7.2, pp. 265–268, 2006.
6. P.M. Shenoy and B.J. Baliga, “The Planar 6H-SiC ACCUFET”, IEEE Electron Device Letters, Vol. 18, pp. 589–591, 1997.
7. N. Thapar and B.J. Baliga, “Analytical Model for the Threshold Voltage of Accumulation Channel MOS-Gated Devices”, Solid State Electronics, Vol. 42, pp. 1975–1979, 1998.

About the Author

Professor Baliga is internationally recognized for his leadership in the area of power semiconductor devices. In addition to over 500 publications in international journals and conference digests, he has authored and edited 16 books ("*Power Transistors*", IEEE Press 1984; "*Epitaxial Silicon Technology*", Academic Press 1986; "*Modern Power Devices*", John Wiley 1987; "*High Voltage Integrated Circuits*", IEEE Press 1988; "*Solution Manual: Modern Power Devices*", John Wiley 1988; "*Proceedings of the 3rd Int. Symposium on Power Devices and ICs"*, IEEE Press 1991; "*Modern Power Devices*", Krieger Publishing Co. 1992; "*Proceedings of the 5th Int. Symposium on Power Devices and ICs"*, IEEE Press 1993; *"Power Semiconductor Devices*"; PWS Publishing Company 1995; *"Solution Manual: Power Semiconductor Devices*"; PWS Publishing Company 1996; *"Cryogenic Operation of Power Devices"*, Kluwer Press 1998; *"Silicon RF Power MOSFETs"*, World Scientific Publishing Company 2005; *"Silicon Carbide Power Devices"*, World Scientific Publishing Company 2006; "*Fundamentals of Power Semiconductor Devices*", Springer Science, 2008; "*Solution Manual: Fundamentals of Power Semiconductor Devices*", Springer Science, 2008; "*Advanced Power Rectifier Concepts*", Springer Science, 2009. In addition, he has contributed chapters to another twenty books. He holds 120 US Patents in the solid-state area. In 1995, one of his inventions was selected for the *B.F. Goodrich Collegiate Inventors Award* presented at the *Inventors Hall of Fame*.

Professor Baliga obtained his Bachelor of Technology degree in 1969 from the Indian Institute of Technology, Madras, India. He was the recipient of the *Philips India Medal* and the *Special Merit Medal (as Valedictorian)* at I.I.T, Madras. He obtained his Masters and Ph.D. degrees from Rensselaer Polytechnic Institute, Troy NY, in 1971 and 1974, respectively. His thesis work involved Gallium Arsenide diffusion mechanisms and pioneering work on the growth of InAs and GaInAs layers using Organometallic CVD techniques. At R.P.I., he was the recipient of the *IBM Fellowship* in 1972 and the *Allen B. Dumont Prize* in 1974.

From 1974 to 1988, Dr. Baliga performed research and directed a group of 40 scientists at the General Electric Research and Development Center in Schenectady, NY, in the area of Power Semiconductor Devices and High Voltage Integrated Circuits. During this time, he pioneered the concept of MOS-Bipolar functional integration to create a new family of discrete devices. He is the *inventor of the IGBT* which is now in production by many International Semiconductor companies. This invention is widely used around the globe for air-conditioning, home appliance (washing machines, refrigerators, mixers, etc) control, factory automation (robotics), medical systems (CAT scanners, uninterruptible power supplies), and electric street-cars/bullet-trains, as well as for the drive-train in electric and hybrid-electric cars under development for reducing urban pollution. The US Department of Energy has released a report that the variable speed motor drives enabled by IGBTs produce an energy savings of 2 quadrillion btus per year (equivalent to 70 Giga-Watts of power). The widespread adoption of Compact Fluorescent Lamps (CFLs) in place of incandescent lamps is producing an additional power savings of 30 Giga-Watts. The cumulative impact of these energy savings on the environment is a reduction in Carbon Dioxide emissions from Coal-Fired power plants by over One Trillion pounds per year. Most recently, the IGBT has enabled fabrication of very compact, light-weight, and inexpensive defibrillators used to resuscitate cardiac arrest victims. When installed in fire-trucks, paramedic vans, and on-board airlines, it is projected by the American Medical Association (AMA) to save 100,000 lives per year in the US. For this work, *Scientific American Magazine* named him one of the eight heroes of the semiconductor revolution in their 1997 special issue commemorating the Solid-State Century.

Dr. Baliga is also the originator of the concept of merging Schottky and p-n junction physics to create a new family of power rectifiers that are commercially available from various companies. In 1979, he theoretically demonstrated that the performance of power MOSFETs could be enhanced by several orders of magnitude by replacing silicon with other materials such as gallium arsenide and silicon carbide. This is forming the basis of a new generation of power devices in the twenty first Century.

In August 1988, Dr. Baliga joined the faculty of the Department of Electrical and Computer Engineering at North Carolina State University, Raleigh, North Carolina, as a Full Professor. At NCSU, in 1991 he established an international center called the *Power Semiconductor Research Center* (PSRC) for research in the area of power semiconductor devices and high voltage integrated circuits, and has served as its Founding Director. His research interests include the modeling of novel

device concepts, device fabrication technology, and the investigation of the impact of new materials, such as GaAs and Silicon Carbide, on power devices. In 1997, in recognition of his contributions to NCSU, he was given the highest university faculty rank of *Distinguished University Professor of Electrical Engineering*.

In 2008, Professor Baliga was a key member of an NCSU team – partnered with four other universities - that was successful in being granted an Engineering Research Center from the National Science Foundation for the development of micro-grids that allow integration of renewable energy sources. Within this program, he is responsible for the fundamental sciences platform and the development of power devices from wide-band-gap semiconductors for utility applications.

Professor Baliga has received numerous awards in recognition for his contributions to semiconductor devices. These include two *IR 100 awards* (1983, 1984), the *Dushman* and *Coolidge Awards* at GE (1983), and being selected among the *100 Brightest Young Scientists in America* by Science Digest Magazine (1984). He was elected *Fellow of the IEEE* in 1983 at the age of 35 for his contributions to power semiconductor devices. In 1984, he was given the *Applied Sciences Award* by the world famous sitar maestro Ravi Shankar at the Third Convention of Asians in North America. He received the 1991 *IEEE William E. Newell Award*, the highest honor given by the Power Electronics Society, followed by the 1993 *IEEE Morris E. Liebman Award* for his contributions to the emerging *Smart Power Technology*. In 1992, he was the first recipient of the BSS Society's *Pride of India Award*. At the age of 45, he was elected as Foreign Affiliate to the prestigious *National Academy of Engineering*, and was one of only four citizens of India to have the honor at that time (converted to regular Member in 2000 after taking US Citizenship). In 1998, the University of North Carolina system selected him for the *O. Max Gardner Award*, which recognizes the faculty member among the 16 constituent universities who has made the greatest contribution to the welfare of the human race. In December 1998, he received the *J.J. Ebers Award*, the highest recognition given by the IEEE Electron Devices Society for his technical contributions to the Solid-State area. In June 1999, he was honored at the Whitehall Palace in London with the *IEEE Lamme Medal*, one of the highest forms of recognition given by the IEEE Board of Governors, for his contributions to development of an apparatus/technology of benefit to society. In April 2000, he was honored by his Alma Mater as a *Distinguished Alumnus*. In November 2000, he received the *R.J. Reynolds Tobacco Company Award for Excellence in Teaching, Research, and Extension* for his contributions to the College of Engineering at North Carolina State University.

In 1999, Prof. Baliga founded a company, *Giant Semiconductor Corporation*, with seed investment from Centennial Venture Partners, to acquire an exclusive license for his patented technology from North Carolina State University with the goal of bringing his NCSU inventions to the marketplace. A company, *Micro-Ohm Corporation*, subsequently formed by him in 1999, has been successful in licensing the GD-TMBS power rectifier technology to several major semiconductor companies for world-wide distribution. These devices have application in power supplies, battery chargers, and automotive electronics. In June 2000, Prof. Baliga founded another company, *Silicon Wireless Corporation*, to commercialize a novel super-linear silicon

RF transistor that he invented for application in cellular base-stations and grew it to 41 employees. This company (renamed *Silicon Semiconductor Corporation*) is located at Research Triangle Park, NC. It received an investment of $10 Million from *Fairchild Semiconductor Corporation* in December 2000 to co-develop and market this technology. Based upon his additional inventions, this company has also produced a new generation of Power MOSFETs for delivering power to microprocessors in notebooks and servers. This technology was licensed by his company to Linear Technologies Corporation with transfer of the know-how and manufacturing process. Voltage Regulator Modules (VRMs) using his transistors are currently available in the market for powering microprocessor and graphics chips in laptops and servers.

Index