

VITA
9/26/2021

Name: James A. Cooper

Education:

<i>Degree</i>	<i>Date</i>	<i>School</i>
BSEE	1968	Mississippi State University
MSEE	1969	Stanford University
Ph.D.	1973	Purdue University

Thesis: *“A Unified Treatment of the Conductance, Capacitance, and Noise Due to Surface States at the SiO₂ -Si Interface”*

Thesis Advisor: Richard J. Schwartz

Professional and Honorary Society Memberships:

Institute of Electrical and Electronics Engineers (IEEE)

<i>Life Fellow</i>	<i>2012</i>
<i>Fellow</i>	<i>1993</i>
<i>Senior Member</i>	<i>1985 - 1992</i>
<i>Member</i>	<i>1973 - 1985</i>
<i>Student Member</i>	<i>1971 - 1973</i>
<i>Member</i>	<i>1969 - 1971</i>
<i>Student member</i>	<i>1966 – 1969</i>

Tau Beta Pi

Eta Kappa Nu

Phi Kappa Phi

Sigma Pi Sigma

Omicron Delta Kappa

Blue Key

Honors and Awards:

- [1] Elected Fellow of the IEEE, 1993 *“For time-of-flight studies of high-field transport at the silicon / silicon dioxide interface and demonstration of long-term charge storage in wide-bandgap semiconductors”*
- [2] Member of the Editorial Advisory Board of the *IEEE Proceedings*, 2004 – 2009.
- [3] Technical program co-chair, *International Conference on Silicon Carbide and Related Materials (ICSCRM 2017)*, Washington, DC, September 17-22, 2017.
- [4] Member, External Advisory Committee, Sandia National Laboratories IR&D project on ultra-wide-bandgap (UWBG) semiconductor technology, September 2017 – August 2018.
- [5] *Charles William Harrison Professor of Electrical and Computer Engineering*, Purdue University, February 8, 2002 – March 16, 2008.
- [6] *Jai N. Gupta Professor of Electrical and Computer Engineering*, Purdue University, March 17 2008 – October, 2014.
- [7] *Jai N. Gupta Professor Emeritus of Electrical and Computer Engineering*, Purdue University, January 2016 – present.
- [8] Chair, Dean’s Faculty Advisory Committee, College of Engineering, Purdue University, 2008 – 2010.

- [9] Founding Co-Director of the Birck Nanotechnology Center, Purdue University, November 30, 2001 – October 31, 2006; Interim Director of the BNC, March 1, 2010 – September 30, 2011.
- [10] Nominated for D. D. Ewing Undergraduate Teaching Award, Purdue University, 1992, 1993, 1994.
- [11] Nominated for Honeywell Teaching Award, Purdue University, 1994.
- [12] Recipient of the Hesselberth Award for Teaching Excellence, Purdue University, 2013.
- [13] Advisor to Best Student Paper, *Semiconductor Interface Specialists Conference*, San Diego, CA, December 3 - 5, 1998.
- [14] Advisor to Best Student Paper, *41ST Electronic Materials Conference*, Santa Barbara, CA, June 30 - July 2, 1999

Professional Experience:

- June 1968 – Aug. 1970
Staff Member Technical, Sandia National Laboratories, Albuquerque, NM
- Aug. 1970 – May 1972
Graduate Research Assistant and Graduate Teaching Assistant, School of Electrical Engineering, Purdue University, West Lafayette, IN
- June 1972 – May 1973
Staff Member Technical (Doctoral Support Program), Sandia National Laboratories, Albuquerque, NM (on leave at Purdue)
- June 1973 – Aug. 1983
Member of Technical Staff, Bell Laboratories, Murray Hill, NJ
- Aug. 1983 – Jan. 2017
Professor of Electrical and Computer Engineering, Purdue University, West Lafayette, IN
- Feb. 2015 – Present
President and Chairman, Sonrisa Research, Inc., Santa Fe, NM

Research Grants and Contracts Received (82):

- [1] 3-year Faculty Assistance Grant, McGraw-Edison, Aug. 1983 - Aug. 1986: **\$30,000** (sole P.I.).
- [2] Equipment Grant, AT&T Bell Laboratories, Feb. 17, 1984: **\$28,900** (sole P.I.).
- [3] “MBE Fabrication of Structures for the Study of Charge Storage and Transport at the AlGaAs/GaAs Interface,” NSF-MRL, July 1, 1984 - June 30, 1985: **\$23,381** (sole P.I.).
- [4] “A Study of the Long Term Retention of Minority Carriers at the AlGaAs/GaAs Interface,” National Science Foundation, Sept. 15, 1984 - Feb. 28, 1986: **\$213,904** (Cooper is P.I. and wrote the proposal; R. F. Pierret is faculty associate).
- [5] “Investigation of a New Concept in Semiconductor Microwave Oscillators,” Air Force Office of Scientific Research, May 1, 1985 - April 21, 1988: **\$ 258,787** (sole P.I.).
- [6] “Optoelectronics Center at Purdue University,” Indiana Corporation for Science and Technology, May 1, 1986 -- April 30, 1989: **\$2,477,659** (Cooper is P.I. and wrote the proposal; C. L. Chen, A. E. Kaplan, D. S. Elliott, M. S. Lundstrom, M. R. Melloch, R. F. Pierret, R. L. Gunshor, and L. A. Kolodziejski are faculty associates).
- [7] “GaAs Gate Dynamic Memory Technology,” Office of Naval Research, May 1, 1986 -- April 30, 1989: **\$272,928** (Cooper is P.I. and wrote the proposal; M. R. Melloch is faculty associate).
- [8] “Pseudomorphic Interfaces,” Office of Naval Research, June 1, 1987 - September 31, 1988: **\$250,000** (with R. L. Gunshor, M. R. Melloch, L. A. Kolodziejski, and R. F. Pierret).
- [9] Equipment Grant, AT&T Bell Laboratories, November 12, 1987: **\$25,000** (with M. R. Melloch).
- [10] “Continuation of Research on the Contiguous Domain Oscillator,” Air Force Office of Scientific Research, January 1, 1989 - April 30, 1990: **\$16,823** (sole P.I.).

- [11] "Development of a GaAs Dynamic Content Addressable Memory," North Carolina State University/Strategic Defense Initiative Organization, July 1, 1988 - December 31, 1990: **\$461,643** (Cooper is P.I. and wrote the proposal; M. R. Melloch and G. W. Neudeck are faculty associates).
- [12] "GaAs Gate Dynamic Memory Technology," Office of Naval Research, January 1, 1989 - December 31, 1991: **\$305,000** (Cooper is P.I. and wrote the proposal; M. R. Melloch is faculty associate).
- [13] "Optoelectronics Center at Purdue University," Indiana Corporation for Science and Technology, July 1, 1989--June 30, 1990: **\$600,000** (Cooper is P.I. and wrote the proposal; R. L. Gunshor, D. S. Elliott, C. L. Chen, M. S. Lundstrom, R. F. Pierret, J. L. Gray, G. W. Neudeck, and M. R. Melloch are faculty associates).
- [14] "Optoelectronics Center at Purdue University," Indiana Corporation for Science and Technology, July 1, 1990--June 30, 1991: **\$500,000** (Cooper is P.I. and wrote the proposal; R. L. Gunshor, D. S. Elliott, C. L. Chen, M. S. Lundstrom, R. F. Pierret, J. L. Gray, G. W. Neudeck, and M. R. Melloch are faculty associates).
- [15] "Optoelectronics Center at Purdue University," Indiana Corporation for Science and Technology, July 1, 1991--June 30, 1992: **\$350,000** (Cooper is P.I. and wrote the proposal; R. L. Gunshor, D. S. Elliott, C. L. Chen, M. S. Lundstrom, R. F. Pierret, J. L. Gray, G. W. Neudeck, and M. R. Melloch are faculty associates).
- [16] "Investigation and Development of a Transient Suppressor Diode," Allied-Signal Aerospace Corp., Bendix Engine Controls Div., South Bend, IN, August 15, 1990 -- August 14, 1991: **\$15,000 + \$15,000** matching funds from Indiana CST (sole P.I.).
- [17] "Renewed Funding for the Contiguous Domain Oscillator Project," Air Force Office of Scientific Research, July 1, 1991 -- June 30, 1992: **\$53,231** (sole P.I.).
- [18] "Development of a Novel Bipolar-FET (BiFET) Dynamic Content-Addressable Memory in GaAs," North Carolina State University / Strategic Defense Initiative Organization, April 1, 1991 -- March 31, 1993: **\$337,456** (Cooper is P.I. and wrote the proposal; M. R. Melloch is faculty associate). ** NOTE: This award was terminated after the first year and was replaced during the second and third years by award [22] below.
- [19] "Investigation of a Resistive Gate MESFET Oscillator," Purdue Research Foundation Grant, 1991 -- 1992: **\$9,000** (sole P.I.).
- [20] "Development of High-Temperature Optoelectronic Technology," Allied-Signal Corporation, Bendix Engine Controls Division, August 19, 1991 -- August 18, 1993: **\$144,699** (sole P.I.).
- [21] Optoelectronics Research Center Minigrant, January 1992: **\$7,450** (sole P.I.).
- [22] "Investigation of Novel Devices in Wide Bandgap Semiconductors," Strategic Defense Initiative Organization, May 1, 1992 -- April 30, 1994, **\$430,000** (Cooper is P.I. and wrote the proposal; M. R. Melloch is faculty associate). ** NOTE: This award replaced the last two years of award [18] above. (This represents a net gain of \$205,029).
- [23] "Investigation of a Resistive Gate MESFET Oscillator," Purdue Research Foundation Grant, 1992 -- 1993: **\$9,900** (sole P.I.).
- [24] Matching funds for Grant [20], Indiana BMT, October 1992, **\$25,000** (sole P.I.).
- [25] "Development of High-Speed Nonvolatile Semiconductor Memories in 6H Silicon Carbide," Cree Research / Strategic Defense Initiative Organization, March 29, 1993--March 28, 1994: **\$433,684** (Cooper is P.I. and wrote the proposal; M. R. Melloch is faculty associate).
- [26] Matching funds for Grant [25], Indiana BMT, July 1993, **\$25,000** (with M. R. Melloch).
- [27] "Engineering Research Equipment Grant: Chemical Vapor Deposition System," National Science Foundation, August 1993, **\$132,000** (with M. R. Melloch and J. M. Woodall).
- [28] "Development of Fabrication Technology for Power Devices in Silicon Carbide," Semiconductor Research Corporation, January 1, 1994 -- December 31, 1996, **\$225,000** (Cooper is P.I. and wrote the proposal; M. R. Melloch is faculty associate).
- [29] Matching funds for Grant [28], Indiana BMT, November 1994, **\$25,000** (with M. R. Melloch).
- [30] "Development of High-Speed Nonvolatile Semiconductor Memories in 6H Silicon Carbide," Cree Research / Ballistic Missile Defense Organization, May 26, 1994 -- May 25, 1996: **\$990,338** (Cooper is P.I. and wrote the proposal; M. R. Melloch is faculty associate).
- [31] "An Investigation of AlN and SiO₂ as Insulators for SiC Power MOSFET's," MellWood Laboratories, Inc./Office of Naval Research, January 1, 1995 -- December 31, 1995: **\$37,000** (sole P.I.).

- [32] "High-Field and High-Temperature Reliability of Gate Insulators for Silicon Carbide MIS Devices," AASERT grant, Ballistic Missile Defense Organization/Office of Naval Research, June 1, 1995 -- May 31, 1998: **\$160,000** (Cooper is P.I. and wrote the proposal; M. R. Melloch is faculty associate).
- [33] "An Investigation into the Feasibility of Processing Silicon Carbide Wafers on a Silicon Production Line," Delco Electronics, August 14, 1995 -- August 13, 1996: **\$45,859** (sole P.I.)
- [34] "Manufacturable Power Switching Devices", Office of Naval Research Multidisciplinary University Research Initiative (MURI), September 29, 1995 -- September 28, 2000: **\$10,450,000** (Cooper is P.I. and wrote the proposal; M. R. Melloch, J. M. Woodall and J. L. Gray are faculty associates. Includes four subcontracts: the University of Texas at Austin, \$2,168,956; Cree Research, Inc., \$1,447,886; Rensselaer Polytechnic Institute, \$980,087; and Howard University, \$1,228,728. The total funding for Purdue University is **\$4,624,343**.)
- [35] "An Investigation of High-Field Electron Transport in 6H and 4H Silicon Carbide," Space Power Institute, January 1, 1996 -- December 31, 1999, **\$202,969** (sole P.I.).
- [36] "Development of Stable High Temperature Contacts and Advanced MIS Structures for Wide Band Gap Materials," AASERT Grant, Office of Naval Research, June 1, 1996 -- May 31, 1999: **\$167,236** (Cooper is P.I.; J. M. Woodall is faculty associate and wrote the proposal).
- [37] "Time of Flight Instrumentation," DURIP Grant, Office of Naval Research, June 1, 1996 -- May 31, 1998: **\$163,650** (M. R. Melloch is P.I. and wrote the proposal; Cooper is faculty associate).
- [38] "Innovative Microwave Power Amplifier Consortium: IMPACT", Office of Naval Research Multidisciplinary University Research Initiative (MURI), August 31, 1996 -- August 30, 2001: **\$1,400,000** (Subcontract from UCSB, the prime contractor. Cooper is Purdue P.I. and assembled the Purdue proposal; M. R. Melloch and K. J. Webb are faculty associates.)
- [39] "GE/Purdue Collaboration on SiC Static Induction Transistor Fabrication," General Electric Corporate Research and Development, August 31, 1998 -- December 18, 1998: **\$25,000** (sole P.I.)
- [40] "General Electric SiC Microwave MESFET Design Study," General Electric Corporate Research and Development, February 15, 1999 -- December 15, 1999, **\$30,000** (Cooper is sole PI).
- [41] "A Proposal for a High-Temperature, Controlled-Ambient Annealing System for Silicon Carbide," DURIP Grant, Office of Naval Research, March 31, 1999 **\$192,000** (M. A. Capano is P.I. and wrote the proposal; Cooper is faculty associate).
- [42] "Exploratory Development of SiC Bipolar Transistors and GaN Heterojunction Bipolar Transistors for High-Power Switching Applications," Office of Naval Research (DARPA MegaWatt Program), July 1, 1999 -- June 30, 2002, **\$350,000** (Cooper is P.I. and wrote the proposal; M. R. Melloch and M. A. Capano are co-P.I.'s)
- [43] "SiC Power Devices." Gift from Rockwell Science Center, August 27, 1999, **\$25,000** (Cooper is sole recipient).
- [44] "Exploratory Study of Integrating SiC with Silicon," Lucent Technologies, January 1, 2000 -- June 30, 2001, **\$105,000** (Cooper is P.I. and wrote the proposal; M. R. Melloch and M. A. Capano are co-P.I.'s),
- [45] "Epitaxial Growth System for SiC and III-Nitride Semiconductors," DURIP Grant, Office of Naval Research, February, 2000 **\$300,000** (M. A. Capano is P.I. and wrote the proposal; Cooper is faculty associate).
- [46] "Investigation of Microwave Limiter Diodes in SiC," Technologies and Devices International, Inc., (STTR grant) June 1, 2000 -- October 15, 2000, **\$27,999** (J. A. Cooper is sole P.I.).
- [47] "Investigation of Jet Vapor Deposited (JVD) Silicon Oxide / Nitride / Oxide (ONO) Films as Gate Dielectrics for SiC and GaN Devices," Office of Naval Research, July 1, 2000 -- June 30, 2001, **\$295,000** (J. A. Cooper is sole P.I.).
- [48] "Center for Nanoscale Electronic / Biological Devices," Indiana 21st Century Research and Technology Fund, August 1, 2000 -- July 31, 2002, **\$1,480,093** (S. Datta is P.I. and wrote the proposal; J. A. Cooper, R. Bashir, and M. S. Lundstrom are faculty associates and thrust leaders; Cooper's thrust is allocated **\$332,661**)
- [49] "Expansion of Effort for an Exploratory Study of Integrating SiC with Silicon," Lucent Technologies, August 1, 2000 -- May 31, 2001, **\$66,937** (Cooper is P.I. and wrote the proposal; M. R. Melloch and M. A. Capano are co-P.I.'s),
- [50] "SiC Power Devices." Gift from Rockwell Science Center, September 27, 2000, **\$25,000** (Cooper is sole recipient).

- [51] "Development of SiC Power MOSFETs with Low On-Resistance for Military and Commercial Applications," Office of Naval Research, October 1, 2000 - September 30, 2001, **\$249,837** (J. A. Cooper is sole P.I.)
- [52] "Demonstration of Silicon Carbide Power Devices in Practical Power Conversion Systems," Office of Naval Research, October 1, 2000 - September 30, 2001, **\$299,159** (Cooper is P.I. and wrote the proposal; S. D. Sudhoff is co-P.I.)
- [53] "A Proposal on 3C-SiC Electrical Properties Evaluation," Dow Corning Corporation, October 1, 2000 - April 1, 2001, **\$56,235** (M. R. Melloch is P.I., J. A. Cooper and M. A. Capano are co-P.I.s).
- [54] "SiC Power Device Research," Gift from Silicon Power Corporation, April 4, 2001, **\$15,700** (Cooper is sole recipient).
- [55] "Development of SiC Power MOSFETs with Low On-Resistance for Military and Commercial Applications," Office of Naval Research, (RENEWAL of #51 above) October 1, 2001 - September 30, 2002, **\$196,085** (J. A. Cooper is sole P.I.)
- [56] "Demonstration of Silicon Carbide Power Devices in Practical Power Conversion Systems," Office of Naval Research, (RENEWAL of #52 above) October 1, 2001 - September 30, 2002, **\$300,000** (Cooper is P.I. and wrote the proposal; S. D. Sudhoff is co-P.I.)
- [57] "Cooper's Research," Fuji Electric Corporate R&D, Ltd. (Takashi Tsuji) September 1, 2001 - August 30, 2002 **\$7,500** (Cooper is sole P.I.)
- [58] "Development of Process Technologies for High Performance MOS-Based SiC Power Switching Devices," Defense Advanced Research Projects Agency, July 1, 2002 - December 31, 2003, **\$1,807,760** (J. A. Cooper is P.I. and wrote the proposal; M. A. Capano is faculty associate).
- [59] "Development of High-Voltage SiC Power MOSFETs with Ultra-Low Channel Resistance," Defense Advanced Research Projects Agency (subcontract to Cree, Inc.), July 1, 2002 - December 31, 2003, **\$87,500** (J. A. Cooper is sole P.I.)
- [60] "Heterogeneous Integration of Wide Bandgap Semiconductors with Silicon: Interfacing Silicon Nanoelectronics with the High-Voltage World," Defense Advanced Research Projects Agency (Thrust 2 of a proposal entitled "A Proposal to Support Innovative Nanotechnology-Related Research at Purdue," J. A. Cooper and R. J. Schwartz, P.I.'s) September 16, 2002 - September 15, 2004, **\$450,000** (M. A. Capano is P.I. and wrote the sub-proposal, Cooper is co-P.I. of sub-proposal)
- [61] "Demonstration of Silicon Carbide Power Devices in Practical Power Conversion Systems," Office of Naval Research, (RENEWAL of #56 above) October 1, 2002 - September 30, 2003, **\$300,000** (Cooper is P.I. and wrote the proposal; S. D. Sudhoff is co-P.I.)
- [62] "Investigation of the Feasibility of 3C Silicon Carbide Power Devices on Large Area Silicon Substrates," Office of Naval Research, December 1, 2002 - November 30, 2004, **\$342,597** (Cooper is P.I. and wrote the proposal; M. A. Capano is co-P.I.)
- [63] "Development of Process Technologies for High Performance MOS-Based SiC Power Switching Devices," Defense Advanced Research Projects Agency, January 1, 2004 - June 30, 2004, **\$534,506** (J. A. Cooper is P.I. and wrote the proposal; M. A. Capano is faculty associate).
- [64] "Development of High-Voltage SiC Power MOSFETs with Ultra-Low Channel Resistance," Defense Advanced Research Projects Agency (subcontract to Cree, Inc.), January 1, 2004 - June 30, 2004, **\$37,500** (J. A. Cooper is sole P.I.)
- [65] "Silicon Carbide Electronic Devices for Automotive Applications," Indiana 21ST Century Research and Technology Fund, August 20, 2004 - August 20, 2006, **\$1,097,873** (M. A. Capano is P.I. and wrote the proposal; J. A. Cooper is Co-P.I.)
- [66] "Development of Process Technologies for High Performance MOS-Based SiC Power Switching Devices," Defense Advanced Research Projects Agency, March 1, 2005 - September 30, 2006, **\$2,470,843** (J. A. Cooper is P.I. and wrote the proposal; M. A. Capano is faculty associate).
- [67] "SiC Integrated Power Electronics for Increased System Efficiency and Enhanced Survivability," Defense Advanced Research Projects Agency, April 1, 2005 - October 31, 2006, **\$800,000** (J. A. Cooper is sole P.I.)
- [68] "Reliable 4H-SiC MOSFET for Hybrid Electric Vehicle Power Systems," U. S. Army TARDEC, June 1, 2006 - May 31, 2008, **\$750,000** (J. A. Cooper is P.I. and wrote the proposal; P. Ye is faculty associate)
- [69] "Investigation of Graphene Nanoelectronics for Future Integrated Circuits," Intel Corporation, October 1, 2007 - September 30, 2008, **\$125,393** (J. A. Cooper is P.I. and wrote the proposal; J. Appenzeller, M. A. Capano, M. Qi, and P. Ye are faculty associates).

- [70] “Graphene Synthesis on Silicon,” Defense Advanced Research Projects Agency, May 1, 2008 – October 31, 2009, **\$400,000** (J. A. Cooper is P.I. and wrote the proposal; M. A. Capano and P. Ye are faculty associates).
- [71] “Investigation of Graphene Nanoelectronics for Future Integrated Circuits,” Intel Corporation, October 1, 2008 – September 30, 2009, **\$125,000** (J. A. Cooper is P.I. and wrote the proposal; J. Appenzeller and P. Ye are faculty associates).
- [72] P. Ye and J. A. Cooper, “Upgrading an Atomic Layer Deposition System for High-k Dielectric Integration on SiC and Graphene,” April 2009, **\$148,820** (P. Ye is P.I. and wrote the proposal. J. A. Cooper is faculty associate.)
- [73] “Investigation of Graphene Nanoelectronics for Future Integrated Circuits,” Intel Corporation, October 1, 2009 – September 30, 2010, **\$125,000** (J. A. Cooper is P.I. and wrote the proposal; J. Appenzeller and P. Ye are faculty associates).
- [74] “Investigation of Electrostatic Interface Smoothing in SiC MOS Devices to Increase Inversion Layer Mobility,” II-VI Foundation, July 1, 2009 – June 30, 2010, **\$106,076** (J. A. Cooper is sole P.I.).
- [75] “Investigation of Electrostatic Interface Smoothing in 4H-SiC,” Auburn University, March 12, 2009 – September 30, 2010, **\$46,427** (J. A. Cooper is sole P.I.).
- [76] “Investigation of Electrostatic Interface Smoothing in SiC MOS Devices to Increase Inversion Layer Mobility,” II-VI Foundation, July 1, 2010 – June 30, 2011, **\$99,285** (J. A. Cooper is sole P.I.).
- [77] “Investigation of Electrostatic Interface Smoothing in SiC MOS Devices to Increase Inversion Layer Mobility,” II-VI Foundation, July 1, 2011 – June 30, 2012, **\$99,822** (J. A. Cooper is sole P.I.).
- [78] “Investigation and Mitigation of Transport-Limiting Disorder at the SiO₂/SiC Interface,” II-VI Foundation, July 1, 2012 – June 30, 2013, **\$97,422** (J. A. Cooper is sole P.I.).
- [79] “SiO₂/4H-SiC Interface Optimization for Next Generation Power MOSFETs,” II-VI Foundation, July 1, 2013 – June 30, 2014, **\$91,000** (J. A. Cooper is sole P.I.).
- [80] “SiO₂/4H-SiC Interface Optimization for Next Generation Power MOSFETs,” II-VI Foundation, July 1, 2014 – June 30, 2015, **\$95,000** (J. A. Cooper is P.I., D. T. Morissette is co-P.I.).
- [81] “Revolutionary Innovation in SiC Power Devices,” Army Research Laboratory, July 17, 2015 – July 16, 2018, **\$3,029,347** (Contract awarded to Sonrisa Research, Inc., J. A. Cooper, President; Subcontract issued from Sonrisa to Purdue, **\$2,043,476**, D. T. Morissette is subcontract P.I.)
- [82] “Advanced SiC Trench MOSFETs: A Path to Record-Low $R_{on,sp}$ and Record-Low (\$/A),” PowerAmerica Institute, North Carolina State University, July 1, 2017 – June 30, 2018, **\$500,000** (Contract awarded to Sonrisa Research, Inc., J. A. Cooper, President; Subcontract issued from Sonrisa to Global Power Technologies Group, Lake Forest, CA, **\$444,046**, R. L. Woodin is subcontract P.I.). Subcontract funding includes \$250,046 in cost-share from Global Power Technologies Group.
- [83] “SiC Planar DMOSFETs and Power ICs with Enhanced Short-Circuit Withstand Time,” PowerAmerica Institute, North Carolina State University, July 1, 2018 – June 30, 2020, **\$330,877** (includes \$257,632 in cost-share) (Contract awarded to Sonrisa Research, Inc., J. A. Cooper, President; Subcontract issued from Sonrisa to X-FAB Texas, Lubbock, TX, **\$121,106**, J. Ransom is subcontract P.I.). Subcontract funding includes \$64,018 in cost-share from X-FAB Texas.
- [84] “A New Class of SiC Power MOSFETs With Record-Low Resistance,” ARPA-E, June 13, 2019 – June 12, 2022, **\$1,442,827** (includes \$73,545 in cost-share) (Contract awarded to Sonrisa Research, Inc., J. A. Cooper, President; Subcontract issued from Sonrisa to Purdue, **\$1,027,668**, D. T. Morissette is subcontract P.I.)
- [85] “Robust and Reliable SiC Power Devices and Power ICs,” Army Research Laboratory, August 16 2019 – August 15, 2020, **\$120,689** (Contract awarded to Sonrisa Research, Inc., J. A. Cooper, President; Subcontract issued from Sonrisa to Purdue, **\$120,689**, D. T. Morissette is subcontract P.I.)

Federal Proposals for the Birck Nanotechnology Center (5):

- [1] “A Proposal for Infrastructure to Support Nanotechnology Research at Purdue University,” 2002, Department of Energy, grant no. DE-DF02-02CH11126, **\$969,000** (J. A. Cooper, P.I.)
- [2] “A Proposal for Infrastructure to Support Nanotechnology Research at Purdue University,” 2002, Department of Housing and Urban Development, grant no. B-02-USP-IN-0230, **\$740,000** (J. A. Cooper, P.I.)

- [3] “A Proposal for Infrastructure to Support Nanotechnology Research at Purdue University,” 2002, National Aeronautics and Space Administration, grant no. NAG-2-1542, **\$3,000,000** (J. A. Cooper, P.I.)
- [4] “A Proposal to Support Innovative Nanotechnology-Related Research at Purdue University,” 2002, Defense Advanced Research Projects Agency, grant no. MDA972-02-1-0032, **\$1,800,000** (J. A. Cooper and R. J. Schwartz, P.I.s)
- [5] “A Proposal to Support Innovative Nanotechnology-Related Research at Purdue University,” 2003, Defense Advanced Research Projects Agency, grant no. MDA972-03-1-0020, **\$2,600,000** (J. A. Cooper and R. J. Schwartz, P.I.s)

Funding Summary (*total* funding of award, not Cooper’s share):

\$ 27,177,300	as P.I. of research proposals
\$ 3,927,659	as P.I. of Purdue Optoelectronics Research Center
<u>\$ 9,109,000</u>	as P.I. of Washington Projects for the Birck Nanotechnology Center
\$ 40,213,959	Total as P.I. (1983 – 2016, \$1.43 million/year)
<u>\$ 4,462,907</u>	as faculty associate on proposals written by others
\$ 44,676,866	Total funding through Purdue (1983 - 2016, \$1.4 million/year)
<u>\$ 5,423,740</u>	Funding to Sonrisa Research, Inc. (2015 - present)
\$ 50,100,606	Total research funding (1983 – present)

Professional Society Activities:

Technical Program Co-Chair, *International Conference on Silicon Carbide and Related Materials*, 2017.
 Member of Editorial Advisory Board, *IEEE Proceedings*, January 2004 – December 2009.
 Associate Guest Editor for Special Issue of *IEEE Transactions on Electron Devices*, 2008.
 Member of Steering Committee, *International Conference on Silicon Carbide and Related Materials*, 2005.
 Session Organizer, *Materials Research Society Fall Meeting*, Boston, MA, November 27 - December 1, 2000.
 Guest Editor for Special Issue of *IEEE Transactions on Electron Devices*, March 1999.
 Member of Program Committee, *IEEE Device Research Conference*, 1996 - 1999.
 Member of Program Committee, *Semiconductor Interface Specialists Conference*, 1997, 1998.
 Member of Program Committee, *24th International Symposium on Compound Semiconductors*, San Diego, CA, September 1997.
 Session Chairman, 1989 *IEEE Device Research Conference*, Boston, MA, June 1989.
 Member of Program Committee and Session Chairman, 1988 *IEEE International Electron Devices Meeting*, San Francisco, CA, Dec. 1988.
 Member of Program Committee and Session Chairman, 1987 *IEEE International Electron Devices Meeting*, Washington, DC, Dec. 1987.
 Associate Editor, *IEEE Transactions on Electron Devices*, March 1983 - March 1986
 Session Chairman, 1982 *IEEE Semiconductor Interface Specialists Conference*, San Diego, CA Dec. 1982

Ph.D. Thesis Supervision Completed (27):

<i>Name</i>	<i>Date</i>	<i>Thesis Title</i>
[1] Robert E. Beaty	Aug. 1988	“A Bias Tunable Monolithic Microwave Oscillator – The Contiguous Domain Oscillator”
[2] Qi-de Qian	Aug. 1988	“Electrical Behavior of an Inversion Layer at Al _x Ga _{1-x} As/GaAs Heterojunction”
[3] Yiwen Yin	May 1990	“Investigation of the MESFET Version Contiguous Domain Oscillator”
[4] Philip G. Neudeck	May 1991	“Development, Demonstration, and Device Physics of FET Accessed One-Transistor GaAs Dynamic Memory Technologies”
[5] John S. Kleine	May 1992	“Characterization of MODFET Dynamic Memory Cells”

[6] Hua Fu	Dec. 1992	“Characterization and Simulation of the Contiguous Domain Oscillator”
[7] Zicheng Gary Ling	May 1995	“The Development of a Vertically Integrated GaAs Bipolar/FET (BiFET) DRAM Cell”
[8] Weize Xie	Dec. 1995	“The Development of Nonvolatile Random Access Memory in 6H Silicon Carbide”
[9] Youlong Wang	May 1996	“Analysis and Optimization of Bipolar Nonvolatile Random Access Memory Cells in 6H Silicon Carbide”
[10] James (Nan-Hsi) Pan	Aug. 1996	“Development of Self-Aligned, Polysilicon Gate MOSFETs in 6H-Silicon Carbide”
[11] Michelle Mathur Maranowski	May 1998	“An Investigation into the Reliability of the Silicon Dioxide / Silicon Carbide Material System”
[12] Jian Tan	Aug. 1998	“An Optimized SiC Power UMOSFET”
[13] Mrinal Das	Dec. 1999	“Fundamental Studies of the Silicon Carbide MOS Structure”
[14] Andreas Prasadka	Dec. 1999	“High-Frequency, High-Power Static Induction Transistors in Silicon Carbide: Simulation and Fabrication”
[15] Dallas T. Morissette	May 2001	“Development of Robust Power Schottky Barrier Diodes in Silicon Carbide”
[16] Yu Li	Aug. 2001	“Modeling, Design, and Fabrication of High-Performance UMOSFETs in 4H-SiC for Power Switching Applications”
[17] Imran Ali Khan	Aug. 2002	“High Voltage UMOSFETs”
[18] Maherin Pauline Matin	Dec. 2002	“4H-SiC Power DMOSFETs”
[19] Chao-Yang Lu	Dec. 2003	“Design and Fabrication of High Performance UMOSFETs in 4H-SiC”
[20] Chih-Fang Huang	Dec. 2003	“Development of 4H-SiC BJTs for Power Electronic Applications”
[21] Asmita Saha	Dec. 2006	“SiC Short Channel Power DMOSFET: An Optimized Design”
[22] Yang Sui	May 2007	“Development of High Voltage P-Channel DMOS IGBTs in 4H-SiC”
[23] Xiaokun Wang	Aug. 2007	“Design and Fabrication of High-Voltage N-Channel DMOS IGBTs in 4H SiC”
[24] Jeong-Youb Lee	May 2008	“Development of a Basic SiC TTL IC Technology”
[25] Ginger Grace Walden	May 2009	“The Future of Silicon Carbide High Power Electronic Switches”
[26] Shakti Singh	May 2010	“High Performance TTL Bipolar Integrated Circuits in 4H-SiC”
[27] Steven Swandono	Aug. 2017	“Fundamental Studies of the Silicon Carbide MOS Interface”

M.S. Thesis Supervision Completed (10):

<i>Name</i>	<i>Date</i>	<i>Thesis Title</i>
[1] Ming Fang	Dec. 1985	“Fabrication and Characterization of Thin Metal Films”
[2] Qi-de Qian	May 1986	“Measurement of Minority Carrier Retention Time at Al _x Ga _{1-x} As/ GaAs Interface”
[3] John S. Kleine	Dec. 1986	“Rapid Thermal Annealing of Silicon Implanted Gallium Arsenide”
[4] Philip G. Neudeck	Dec. 1987	“Experiments in Interrupted Growth Molecular Beam Epitaxy Technology”
[5] Kai Chen	Dec. 1989	“Development of GaAs MODFET DCFL Circuits and Process Technology”

[6] Rahil Hasan	Dec. 1992	“Investigation and Development of a Transient Absorber Diode Using Gallium Arsenide”
[7] Jim Eun	Dec. 1992	“High Temperature Ohmic Contact Technology to n-Type GaAs”
[8] Jeffrey W. Sanders	Dec. 1993	“MOS Characterization of Thermally Oxidized Silicon Carbide (6H)”
[9] Maherin Pauline Martin	Dec. 1997	“Fabrication and Characterization of Silicon Carbide DMOS Transistors”
[10] Imran Ali Khan	May 1998	“Velocity-Field Measurements of Electrons in Silicon Carbide”

Ph. D. Thesis Graduates Supported by Sonrisa Research, Inc. (4):

<i>Name</i>	<i>Date</i>	<i>Thesis Title</i>
[1] Naeem Islam	Dec. 2020	“4H-SiC Vertical Tri-Gate Power MOSFETs Technology Development”
[2] Rahul Ramamurthy	July 2020	“Vertical Tri-Gate Metal-Oxide-Semiconductor Field-Effect Transistor in 4H-Silicon Carbide”
[3] Madan Sampath	July 2021	“Deeply-Scaled, Fully-Self-Aligned Trench MOSFETs in 4H-SiC”
[4] Monzurul Alam	August 2021	“The Design, Fabrication, and Characterization of Waffle-Substrate-Based <i>n</i> -Channel IGBTs in 4H-SiC”

Sabbatical Visitors and Visiting Scholars Hosted (6):

- [1] Prof. Kazuo Masaki, Sabbatical Visitor, September 1, 1995 – May 31, 1996
Department of Electrical Engineering
Anan College of Technology
Minobayasi, Anan, Tokushima 774, JAPAN
- [2] Prof. Kee Suk Nahm, Sabbatical Visitor, February 25, 2001 – February, 2003
School of Chemical Engineering and Technology
Chonbuk National University
Duckjin-Dong, Duckjin-Gu
Chonju 561-756, Republic of KOREA
- [3] Prof. Masataka Satoh, Sabbatical Visitor, April 3, 2001 – March 2002
Research Center of Ion Beam Technology
Hosei University
Koganei, Tokyo 184-8584, JAPAN
- [4] Mr. Takashi Tsuji, Visiting Scholar, August, 2001 – August, 2003
Corporate Research and Development
Fuji Electric Co.
2-2-1, Nagasaka, Yokosuka-City 240-0194 JAPAN
- [5] Mr. Tomohiro Tamaki, Visiting Scientist, September 2006 – November 2007
Renesas Technology Corporation
111, Nishiyokote-machi, Takasaki-shi

Gunma-ken, 370-0021, JAPAN

- [6] Mr. Hiroki Miyake, Visiting Scholar, September 2010 – November 2010
 Department of Electronic Science and Engineering
 Kyoto University
 A1-303 Kyotodaigaku-katsura, Nishikyo, Kyoto 615-8510, Japan

ECE Committee Activities:

Member, External Awards Committee	2008 – 2011
Chair, MN Area Committee	2007 – 2008
Member, Named Professor Committee	2007 – 2010
Member, Head's Advisory Committee	2001 – 2006
Member, Primary Committee	1983 - 2016
Member, Graduate Committee	1984 - 1987, 2000 - 2003
Member, Awards Committee	2000 - 2002
Chair, PDE Committee	1990 - 1992
Chair, Solid-State Area Committee	1989 - 1991
Member, PDE Committee	1989 - 1990

College of Engineering Committee Activities:

Chair, Deans Faculty Advisory Committee	2008 – 2010
Member, Dean's Faculty Advisory Committee	2004 – 2008
Engineering Faculty/Staff Grievance Committee	1989 – 1992

University-Wide Committee Activities:

University Committee on Research Integrity	2009 – 2011
President's Policy Advisory Group	2001
West Lafayette Campus Strategic Planning Task Force	2001

Other University-Wide Activities:

Co-Director of Birck Nanotechnology Center	October 2001 – October 31, 2006
Interim Director, Birck Nanotechnology Center	March 1, 2010 – September 30, 2011

Research Book Contributions and Books Published (6):

- [1] D. F. Nelson and J. A. Cooper, Jr., "High Field Surface Drift Velocities in Silicon," in *The Physics of Submicron Structures*, H. L. Grubin, K. Hess, G. J. Iafrate, and D. K. Ferry, eds., Plenum Publishing Co., 1984.
- [2] J. A. Cooper, Jr., D. F. Nelson, S. A. Schwartz, and K. K. Thornber, "Effects on Carrier Velocity at Interfaces," book chapter in *VLSI Electronics: Microstructure Science*, N. G. Einspruch and R. S. Bauer, eds., Vol. 10, pp. 323-361, Academic Press, 1985.
- [3] J. A. Cooper, Jr., "Recent Advances in GaAs Dynamic Memories," book chapter in *Advances in Electronics and Electron Physics*, P. W. Hawkes, ed., Vol. 86, pp. 1-79, Academic Press, 1993.
- [4] J. A. Cooper, Jr., "Nonvolatile Random Access Memories in Wide Bandgap Semiconductors," book chapter in *III-Nitrides*, J. I. Pankove and T. D. Moustakas, eds., in the series on *Semiconductors and Semimetals*, E. Weber and R. Willardson, eds., Vol. 50, pp. 473 - 491, Academic Press, 1997.

- [5] J. A. Cooper, Jr., "Silicon Carbide MOSFETs," book chapter in *Wide Energy Bandgap Electronic Devices*, F. Ren and J. C. Zolper, eds., World Scientific Publishing Co., 2003.
- [6] T. Kimoto and J. A. Cooper, *Fundamentals of Silicon Carbide Technology*, John Wiley & Sons, Singapore, 2014.

Serial Journal Articles (59):

- [1] J. A. Cooper, Jr., E. R. Ward, and R. J. Schwartz, "Surface States and Insulator Traps at the Si_3N_4 - GaAs Interface," *Solid State Electronics*, Vol. 15, pp. 1219-1227, Nov. 1972.
- [2] J. A. Cooper, Jr. and R. J. Schwartz, "The Effect of an Energy-Dependent Capture Cross Section on Data Interpretation Using the MOS Conductance Technique," *J. Applied Physics*, Vol. 44, pp. 5613-5614, Dec. 1973.
- [3] J. A. Cooper, Jr. and R. J. Schwartz, "Electrical Characteristics of the SiO_2 - Si Interface Near Midgap and in Weak Inversion," *Solid State Electronics*, Vol. 17, pp. 641-654, July 1974.
- [4] J. A. Cooper, Jr., "Limitations on the Performance of Field-Effect Devices for Logic Applications," (INVITED Paper), *Proceedings of the IEEE*, Vol. 69, pp. 226-231, Feb. 1981.
- [5] D. F. Nelson and J. A. Cooper, Jr., "High-Field Electron Velocities in Silicon Surface Inversion Layers," *Surface Science*, Vol. 113, pp. 267-272, 1982.
- [6] W. Fichtner, J. A. Cooper, Jr., A. R. Tretola, and D. Kahng, "A Novel Buried-Drain DMOSFET Structure," *IEEE Transactions on Electron Devices*, Vol. ED-29, pp. 1785, 1791, Nov. 1982.
- [7] J. A. Cooper, Jr., and D. F. Nelson, "High-Field Drift Velocity of Electrons at the SiO_2 - Si Interface as Determined by a Time-of-Flight Technique," *Journal of Applied Physics*, Vol. 54, pp. 1445-1456, March 1983.
- [8] M. R. Melloch, J. A. Cooper, Jr., and Q-D. Qian, "Investigation of Minority Carrier Hole Retention Behind AlAs and AlAs/GaAs Superlattice Barriers," *Journal of Vacuum Science and Technology*, Vol. B5, pp. 766-769, May-June 1987.
- [9] M. R. Melloch, C. P. McMahon, M. S. Lundstrom, J. A. Cooper, Jr., and Q-D. Qian, "Photocollection Efficiency of GaAs/AlAs/GaAs P^+ and N^+ Photodiodes," *Solar Cells*, Vol. 21, pp. 233-240, 1987.
- [10] J. S. Kleine, Q-D. Qian, J. A. Cooper, Jr., and M. R. Melloch, "Electron Emission from Direct Bandgap Heterojunction Capacitors," *IEEE Transactions on Electron Devices*, Vol. ED-36, pp. 289-299, February, 1989.
- [11] Q.D. Qian, M. R. Melloch, and J. A. Cooper, Jr., "Electrical Behavior of a Static Hole Inversion Layer at the i-AlAs/N-GaAs Heterojunction," *Journal of Applied Physics*, Vol. 65, pp. 3118-3126, April 15, 1989.
- [12] Q.-D. Qian, J. Qiu, J. L. Glenn, Jr., Sungki O, R. L. Gunshor, L. A. Kolodziejski, M. Kobayashi, N. Otsuka, M. R. Melloch, J. A. Cooper, Jr., M. Haggerott, T. Heyen, and A. V. Nurmikko, "II-VI/III-V Heterointerfaces: Epilayer-on-Epilayer Structures," *Journal of Crystal Growth*, Vol. 95, pp. 567-571, 1989.
- [13] Q. D. Qian, J. Qiu, M. Kobayashi, R. L. Gunshor, M. R. Melloch, and J. A. Cooper, Jr., "Electrical Characterization of an Epitaxial ZnSe/Epitaxial GaAs Heterointerface," *Journal of Vacuum Science and Technology*, July/August, 1989.
- [14] T. E. Dungan, P. G. Neudeck, M. R. Melloch, and J. A. Cooper, Jr., "One-Transistor GaAs MESFET- and JFET- Accessed Dynamic RAM Cells for High-Speed Medium Density Applications," *IEEE Transactions on Electron Devices*, Vol. ED-37, pp. 1599-1607, July, 1990.
- [15] T. B. Stellwag, M. R. Melloch, J. A. Cooper, Jr., S. T. Sheppard, and D. D. Nolte, "Increased Thermal Generation Rate in GaAs Due to Electron-Beam Metallization," *Journal of Applied Physics*, Vol. 71, pp. 4509-4514, 1 May, 1992.
- [16] H. Fu and J. A. Cooper, Jr., "Steady-State Modeling of Four-Terminal Resistive Gate MOSFET's," *IEEE Transactions on Electron Devices*, Vol. 40, pp. 1263-1269, July 1993.
- [17] T. S. Mayer, D. M. Fleetwood, D. E. Beutler, J. A. Cooper, Jr., and M. R. Melloch, "Unexpected Increase in the Thermal Generation Rate of Bulk GaAs Due to Electron-Beam Metallization," *IEEE Transactions on Nuclear Science*, Vol. 40, pp. 1293- , 1993.
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- [21] J. N. Shenoy, G. L. Chindalore, M. R. Melloch, J. A. Cooper, Jr., J. W. Palmour, and K. G. Irvine "Characterization and Optimization of the SiO₂/SiC MOS Interface," *Journal of Electronic Materials*, Vol. 24, pp. 303-309, April 1995.
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- [26] J. N. Pan, J. A. Cooper, Jr., and M. R. Melloch, "Activation of Nitrogen Implants in 6H-SiC," *Journal of Electronic Materials*, Vol. 26, No. 3, pp. 208-211, March 1997.
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- [45] D. T. Morisette and J. A. Cooper, Jr., "Theoretical Performance Comparison of SiC PiN and Schottky Diodes," *IEEE Transactions on Electron Devices*, Vol. 49, No. 9, pp. 1657-1664, September, 2002.
- [46] C.-Y. Lu, J. A. Cooper, Jr., T. Tsuji, G. Y. Chung, J. R. Williams, K. McDonald, and L. C. Feldman, "Effect of Process Variations and Ambient Temperature on Electron Mobility at the SiO₂/4H-SiC Interface," *IEEE Transactions on Electron Devices*, Vol. 50, No. 7, pp. 1582 – 1588, July, 2003.
- [47] K.-C. Chang, L. M. Porter, J. Bentley, C.-Y. Lu, and J. A. Cooper, Jr., "Electrical, Structural and Chemical Analysis of Silicon Carbide-Based Metal-Oxide-Semiconductor Field-Effect-Transistors," *Journal of Applied Physics*, Vol. 95, NO. 12, pp. 8252 – 8257, June 15, 2004.
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- [51] T. Tamaki, G. G. Walden, Y. Sui, and J. A. Cooper, "Optimization of On-State and Switching Performance for 15 – 20 kV 4H-SiC IGBTs," *IEEE Transactions on Electron Devices*, Vol. 55, No. 8, pp. 1920 – 1927, August, 2008.
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- [55] S. Singh and J. A. Cooper, "Bipolar Integrated Circuits in 4H-SiC," *IEEE Transactions on Electron Devices*, Vol. 58, No. 4, pp. 1084 – 1090, April 2011.
- [56] S. Swandono, A. Penumatcha, and J. A. Cooper, "Limitations of the MOS Hi-Lo CV Technique for MOS Interfaces with Large Time Constant Dispersion," *IEEE Transactions on Electron Devices*, Vol. 60, No. 3, pp. 923 – 926, March 2013.
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Serial Journal Correspondence or Letters (57):

- [1] J. A. Cooper, Jr. and D. F. Nelson, "Measurement of the High-Field Drift Velocity of Electrons in Inversion Layers on Silicon," *IEEE Electron Device Letters*, Vol. EDL-2, pp. 171, 173, July 1981.
- [2] K. K. Thornber, D. F. Nelson, and J. A. Cooper, Jr., "Cube-Root Broadening of Surface Charge Packets," *Applied Physics Letters*, Vol. 39, pp. 843-845, Nov. 15, 1981.
- [3] A. K. Sinha, J. A. Cooper, Jr., and H. J. Levinstein, "Speed Limitations Due to Interconnect Time Constants in VLSI Integrated Circuits," *IEEE Electron Device Letters*, Vol. EDL-3, pp. 90-92, April 1982.
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- [7] J. A. Cooper, Jr., "Power Law Broadening of Charge Packets at Semiconductor Interfaces," *Applied Physics Letters*, Vol. 44, pp. 243-245, Jan. 15, 1984.
- [8] J. A. Cooper, Jr. and K. K. Thornber, "Screened-Charge Transferred-Electron Oscillators," *IEEE Electron Device Letters*, Vol. EDL-6, pp. 50-53, Jan. 1985.
- [9] J. A. Cooper, Jr., Q-D. Qian, and M. R. Melloch, "Capacitance-Voltage and Current-Voltage Characteristics of Molecular Beam Epitaxially Grown P⁺-GaAs/AlAs/N-GaAs Heterostructures," *Applied Physics Letters*, Vol. 48, pp. 365-366, Feb. 3, 1986.
- [10] Q-D. Qian, M. R. Melloch, and J. A. Cooper, Jr., "Photosensitive Capacitance Voltage Characteristics of Molecular Beam Epitaxially Grown GaAs/AlGaAs/GaAs Heterostructures," *Applied Physics Letters*, Vol. 48, pp. 638-640, March 10, 1986.
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- [13] M. R. Melloch, Q-D. Qian, and J. A. Cooper, Jr., "Long Term Storage of Inversion Holes at a Superlattice/GaAs Interface," *Applied Physics Letters*, 49, 1471 (1986).
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- [153] S. Swandono, A. Penumatcha, and J. A. Cooper, "Electrical Evidence of Disorder at the SiO₂/4H-SiC Interface and its Effect on Electron Transport," *2012 IEEE Device Research Conference*, State College, PA, June 25 – 27, 2012.
- [154] J. A. Cooper, S. Swandono, and A. Penumatcha, "Interface State Time Constant Dispersion at the SiO₂/4H-SiC MOS Interface," *7th Annual SiC MOS Workshop*, College Park, MD, August 16 – 17, 2012.
- [155] J. A. Cooper, S. Swandono, and A. Penumatcha, "Origin of the Time Constant Dispersion at the SiO₂/4H-SiC MOS Interface," *Semiconductor Interface Specialist's Conference*, San Diego, CA, December 6 – 8, 2012.
- [156] J. A. Cooper, "Current Issues and Opportunities for SiC Power Electronics" [INVITED], *International Workshop on WBG Power Electronics 2013*, Hsinchu, Taiwan, April 8 – 9, 2013.
- [157] J. A. Cooper, "The Continuing Evolution of Silicon Carbide Power MOSFETs," [INVITED], *International Conference on Solid State Devices and Materials*, Tsukuba, Japan, September 8 – 11, 2014.
- [158] S. Swandono, D. T. Morisette, and J. A. Cooper, "Systemic Errors in the MOS Conductance Technique", *10th Annual SiC MOS Workshop*, College Park, MD, August 13 – 14, 2015.
- [159] J. A. Cooper, "Introduction to SiC Devices: Physics, Working Principles, Architectures," [INVITED], tutorial presentation at the *International Conference on Silicon Carbide and Related Materials*, Giardini Naxos, Italy, October 4 – 9, 2015.
- [160] J. A. Cooper, "Silicon Carbide Power MOSFETs: The Best is Yet to Come," [INVITED], *Materials Research Society Fall Symposium*, Boston, MA, November 2 – December 4, 2015.
- [161] S. Swandono, D. T. Morisette, and J. A. Cooper, "Errors Due to Nonlinear and Energy-Dependent Phenomena in the MOS AC Conductance Technique," *Semiconductor Interface Specialist's Conference*, Arlington, VA, December 2 – 5, 2015.
- [162] J. A. Cooper, "SiC Power MOSFETs: Device Physics and Design Optimization," [INVITED] tutorial presentation at the *European Conference on Silicon Carbide and Related Materials*, Halkidiki, Greece, September 25 – 29, 2016.
- [163] J. A. Cooper, "High-Voltage SiC Power Devices: Device Opportunities and Epigrowth Challenges," [INVITED] *18th U.S. Workshop on Organometallic Vapor Phase Epitaxy (OMVPE-18)*, Santa Fe, NM, July 30 - August 4, 2017.
- [164] J. A. Cooper, "SiO₂ / 4H-SiC Near-Interface Traps as Deduced from AC Conductance Measurements, *12th Annual SiC MOS Workshop*, College Park, MD, August 17 - 18, 2017.

- [165] J. A. Cooper, "Device Physics, Challenges, and Opportunities for SiC Power MOSFETs," [INVITED] tutorial presentation at the *TIA Summer School*, Tsukuba, Japan, August 25 – 28, 2017.
- [166] Md. M. Alam, D. T. Morisette, and J. A. Cooper, "Practical Design of 4H-SiC Superjunction Devices in the Presence of Charge Imbalance," *International Conference on Silicon Carbide and Related Materials (ICSCRM-2017)*, Washington, DC, September 17 - 22, 2017; *Materials Science Forum*, Vol. 924, pp. 563-567, 2018.
- [167] M. Sampath, D. T. Morisette, and J. A. Cooper, "Comparison of Single- and Double-Trench UMOSFETs in 4H-SiC," *International Conference on Silicon Carbide and Related Materials (ICSCRM-2017)*, Washington, DC, September 17 - 22, 2017; *Materials Science Forum*, Vol. 924, pp. 752-755, 2018.
- [168] J. A. Cooper, N. Islam, R. P. Ramamurthy, M. Sampath, and D. T. Morisette, "Vertical Tri-Gate Power MOSFETs in 4H-SiC," *International Conference on Silicon Carbide and Related Materials (ICSCRM-2017)*, Washington, DC, September 17 - 22, 2017; *Materials Science Forum*, Vol. 924, pp. 680-683, 2018.
- [169] J. A. Cooper and D. T. Morisette, "Thin Gate Oxides for Improved Device Performance," *13th Annual SiC MOS Workshop*, College Park, MD, August 16 - 17, 2018.
- [170] J. A. Cooper, "Progress is Impossible Without Change: Innovation as a Driver of SiC Technological Evolution," [PLENARY] *International Conference on Silicon Carbide and Related Materials (ICSCRM-2019)*, Kyoto, Japan, September 29 - October 4, 2019.
- [171] J. A. Cooper, D. T. Morisette, and M. Sampath, "Increased Short-Circuit Withstand Time and Reduced DIBL by Constant-Gate-Charge Scaling in SiC Power MOSFETs," *International Conference on Silicon Carbide and Related Materials (ICSCRM-2019)*, Kyoto, Japan, September 29 - October 4, 2019.
- [172] M. Sampath, A. Salemi, D. T. Morisette, and J. A. Cooper, "The IMOSFET: A Deeply-Scaled, Fully-Self-Aligned Trench MOSFET," *International Conference on Silicon Carbide and Related Materials (ICSCRM-2019)*, Kyoto, Japan, September 29 - October 4, 2019.
- [173] N. Opondo, J. A. Cooper, H. Liao, W. W. Chen, and D. T. Morisette, "The Waffle Substrate: A Novel Approach to Reducing Substrate Resistance in SiC Power Devices," *International Conference on Silicon Carbide and Related Materials (ICSCRM-2019)*, Kyoto, Japan, September 29 - October 4, 2019.
- [174] J. A. Cooper, "Evidence of a Transition Layer at the SiO₂/4H-SiC MOS Interface from AC Conductance Data," *International Conference on Silicon Carbide and Related Materials (ICSCRM-2019)*, Kyoto, Japan, September 29 - October 4, 2019.
- [175] M. Sampath, D. T. Morisette, and J. A. Cooper, "Constant-Gate-Charge Scaling for Increased Short-Circuit Withstand Time in SiC Power Devices," *International Reliability Physics Symposium*, Virtual Conference, April 28 - May 30, 2020.

Invited Lectures (43):

- [1] J. A. Cooper, Jr., "Dynamic Behavior of Electrons at Semiconductor Interfaces Under High-Field Conditions," Yale University, New Haven, CT, May 1984.
- [2] J. A. Cooper, Jr., "Dynamic Memory Elements for the High-Electron-Mobility-Transistor (HEMT) Technology," Kodak Research Laboratories, Rochester, NY, Sept. 1984.
- [3] J. A. Cooper, Jr., "One-Transistor Dynamic Memory Cells for GaAs Integrated Circuits," IBM T. J. Watson Research Center, Yorktown Heights, NY, Dec. 1984.
- [4] J. A. Cooper, Jr., "Observation of High Field Transport in Silicon Inversion Layers," Nippon Telegraph and Telephone Corp. Atsugi Electrical Communication Laboratories, Atsugi-shi, JAPAN, August 19, 1985.
- [5] J. A. Cooper, Jr., "Measurement of High Field Drift Velocity at Semiconductor Interfaces Using a Time-of-Flight Technique," Fujitsu Laboratories, Atsugi-shi, JAPAN, August 19, 1985.
- [6] J. A. Cooper, Jr., "High-Field Electron Transport at the Silicon-Silicon Dioxide Interface," Toshiba Research and Development Center, Kawasaki, JAPAN, August 20, 1985.
- [7] J. A. Cooper, Jr., "The High-Field Drift Velocity in Silicon Inversion Layers," Special Seminar, Kansai Branch of Japan Society of Applied Physics, Osaka, JAPAN, August 21, 1985.
- [8] J. A. Cooper, Jr. and M. R. Melloch, "One-Transistor Dynamic Memory Cells for GaAs Integrated Circuits," AT&T Bell Laboratories, Murray Hill, NJ, Sept. 1987.
- [9] J. A. Cooper, Jr. and M. R. Melloch, "Dynamic Storage of Majority and Minority Carriers in GaAs," Bell Communications Research, Inc., Red Bank, NJ, Sept. 1987.
- [10] J. A. Cooper, Jr., "Optoelectronics Research at Purdue University," Kodak Research Laboratories, Rochester, NY, March 1989.

- [11] J. A. Cooper, Jr., "A Resistive Gate MESFET Transferred Electron Oscillator," Wright Research and Development Center, WPAFB, Dayton, OH, Dec. 1989.
- [12] J. A. Cooper, Jr., "Development of High-Temperature Electronic and Optoelectronic Technology," Wright Research and Development Center, WPAFB, Dayton, OH, May 1991.
- [13] J. A. Cooper, Jr., "Recent Progress in Dynamic RAM Technology in GaAs," Kodak Research Laboratories, Rochester, NY, August 1991.
- [14] J. A. Cooper, Jr., "Dynamic RAM Technology in GaAs: Approaching Half-Day Storage Times at Room Temperature," Sandia National Laboratories, Albuquerque, NM, February, 1992.
- [15] J. A. Cooper, Jr., "Development of Nonvolatile Memories and UV Imagers in Silicon Carbide," NASA Langley Research Center, Hampton, VA, October 1992.
- [16] J. A. Cooper, Jr., "Silicon Carbide Electronic Devices," University of Illinois at Urbana-Champaign, Urbana, IL, April 14, 1994.
- [17] J. A. Cooper, Jr., "SiC Device Research at Purdue University," NASA Lewis Research Center, Cleveland, OH, November 10, 1994.
- [18] J. A. Cooper, Jr., "Silicon Carbide Device Technology," National Semiconductor, Santa Clara, CA, June 29, 1995.
- [19] J. A. Cooper, Jr., "MOS Research in SiC: A Status Report," Wright Laboratories, Dayton, OH, February 7, 1996.
- [20] J. A. Cooper, Jr., "Fabrication and Characterization of Double-Implanted, Planar Power MOSFETs in 6H-SiC," Motorola Phoenix Corporate Research Laboratories, Phoenix, AZ, June 21, 1996
- [21] J. A. Cooper, Jr., "Silicon Carbide: The Next Step Beyond Silicon?," Kodak Research Laboratories, Rochester, NY, July 24, 1996.
- [22] J. A. Cooper, Jr., "Silicon Carbide MOS Technology and MOS-Based Power Devices," Northrop-Grumman Science and Technology Center, Pittsburg, PA, August 16, 1996.
- [23] J. A. Cooper, Jr., "Silicon Carbide Electronics Technology: Promise, Prospects, and Practical Problems," Delco Electronics, Kokomo, IN, November 7, 1996.
- [24] J. A. Cooper, Jr., "SiC MOS Technology and MOS-Based Power Devices," Sherman Fairchild lecture, Lehigh University, Allentown, PA, May 1, 1997.
- [25] J. A. Cooper, Jr., "SiC Power Device Development: Past, Present, and Future," EPRI/DARPA Post Silicon Megawatt Electronics Initiative Review, Monterey, CA, January 12-13, 1999.
- [26] J. A. Cooper, Jr., "A Review of SiC MOS Research at Purdue University," Vanderbilt University, Nashville, TN, April 15, 1999.
- [27] J. A. Cooper, Jr., "Nanotechnology Overview and New Materials for Robust Electronics," Purdue Research Foundation Board of Trustees, May, 2000.
- [28] J. A. Cooper, Jr., "Status and Future of SiC Power Device Technology," ONR Advanced Electrical Power Systems Strategic Planning and Review Workshop," Ocean City, MD, October 4-5, 2000.
- [29] J. A. Cooper, Jr., "Nanotechnology: A New World of Opportunities for Purdue," Purdue University Board of Trustees, April 6, 2001.
- [30] J. A. Cooper, Jr., "Silicon Carbide Power Transistors: A Review of MOSFETs, JFETs, and BJTs," Naval Research Laboratory, Washington, DC, August 9, 2002.
- [31] J. A. Cooper, Jr., "Silicon Carbide: The Next Step Beyond Silicon?," IEEE Electron Devices Society Denver Section Meeting, Boulder, CO, April 2, 2004.
- [32] J. A. Cooper, "Graphene Nanoelectronics Research at Purdue University," Notre Dame University, South Bend, IN, February 1, 2008.
- [33] J. A. Cooper, "Fundamental Issues Limiting SiC Device Technology," *Energy Efficiency Through Wide Bandgap Electronics Workshop (EETWBE)*, Naval Research Laboratory, Washington, DC, January 7 – 9, 2009.
- [34] J. A. Cooper, "Performance Comparison of SiC Unipolar and Bipolar Devices for High-Voltage Power Switching Applications," Osaka University, Osaka, Japan, August 25, 2009.
- [35] J. A. Cooper, "SiC Power MOSFETs: Design, Fabrication, Characterization, and Optimization," Samsung Advanced Institute of Technology (SAIT), Gyeonggi-do, Yongin-si, Nongseo-dong 367, South Korea, November 28, 2011.
- [36] J. A. Cooper, "Silicon Carbide Power Devices: Physics, Design, and Performance," National Tsing-Hua University, Hsinchu, Taiwan, April 10, 2013.
- [37] J. A. Cooper, "The Past and Future History of Silicon Carbide Power MOSFETs," National Tsing-Hua University, Hsinchu, Taiwan, September 17, 2014.

- [38] J. A. Cooper, "Overview of SiC Power Device Technology," 2016 IEEE International Workshop on Wide Bandgap Semiconductor Power Electronics (IWWSPE), Xian, China, May 22, 2016.
- [39] J. A. Cooper, "Silicon Carbide Power Electronics: Challenges and Opportunities," Institute of Semiconductors, Chinese Academy of Sciences, Beijing, China, May 25, 2016.
- [40] J. A. Cooper, "Systematic Errors in Interface Analysis Using the MOS Conductance Technique", Symposium in Celebration of the 90th Birthday of Wolfgang J. (Jim) Choyke, Pittsburgh, PA, August 2, 2017.
- [41] J. A. Cooper, "SiC Power Devices: Physics, Current Status, and Future Trends," Workshop on Wide Bandgap Power Devices and Applications, Albuquerque, NM, October 30, 2017.
- [42] J. A. Cooper, "SiC Power MOSFETs: Structure, Physics, and Performance," Infineon Winter School, Villach, Austria, March 1, 2018.
- [43] J. A. Cooper, "Prospects for WBG Power Devices in the Electric Utility Grid", Enabling Advanced Power Electronics Technologies, Albuquerque, NM, July 17, 2018.

Technical Reports (21):

- [1] J. A. Cooper, Jr., "Effects of Ionizing Radiation on Monolithic MOS Inverters," SC-TM-70-339, Sandia Laboratories, June 1970.
- [2] J. A. Cooper, Jr. and R. J. Schwartz, "A Unified Treatment of the Conductance, Capacitance, and Noise due to Surface States at the SiO₂ - Si Interface," TR-EE-73-20, School of Electrical Engineering, Purdue University, August 1973.
- [3] J. A. Cooper, Jr. and A. M. Mohsen, "Design Considerations and Performance Predictions for Two-Phase Offset Charge Coupled Devices with Particular Reference to Their Use in Mass Memory," TM-74-2251-11, Bell Laboratories, April 12, 1974.
- [4] J. A. Cooper, Jr., "A Numerical Solution of the Two-Dimensional Poisson Equation for the Short-Channel IGFET with Non-Uniform Channel Doping," TM-78-2111-14, Bell Laboratories, Sept. 13, 1978.
- [5] S. M. Kang and J. A. Cooper, Jr., "Design of 3.5 μm CMOS Polycells," TM 79-1151-1, Bell Laboratories, Jan. 8, 1979.
- [6] J. A. Cooper, Jr., "Interconnect Capacitance in Integrated Circuits Under Design Rule Scaling," TM-79-1151-24, Aug. 27, 1979.
- [7] J. A. Cooper, Jr., D. V. Speeney, and T. T. Sheng, "A Polysilicon Source and Drain Recessed-Channel IGFET," TM-81-11151-3, Bell Laboratories, Jan 26, 1981.
- [8] J. A. Cooper, Jr. and M. G. Lamont, "Numerical Simulation of Surface Charge Transport in Silicon and GaAs," TM-83-11156-13, Bell Laboratories, July 18, 1983.
- [9] J. A. Cooper, Jr., "Power Law Broadening of Charge Packets at Semiconductor Interfaces," TM-83-11156-14, Bell Laboratories, July 18, 1983.
- (Several other Bell Laboratories Technical Memoranda are omitted here because they were subsequently published in the open literature.)**
- [10] Q-D. Qian, J. A. Cooper, Jr., and M. R. Melloch, "Measurement of Minority Carrier Retention Time at Al_xGa_{1-x}As / GaAs Interface," TR-EE 86-16, School of Electrical Engineering, Purdue University, June 1986.
- [11] J. S. Kleine and J. A. Cooper, Jr., "Rapid Thermal Annealing of Silicon Implanted Gallium Arsenide," TR-EE 86-43, School of Electrical Engineering, Purdue University, December 1986.
- [12] P. G. Neudeck, M. R. Melloch, and J. A. Cooper, Jr., "Experiments in Interrupted Growth Molecular Beam Epitaxy Technology," TR-EE 88-3, School of Electrical Engineering, Purdue University, January 1988.
- [13] M. R. Melloch, J. A. Cooper, Jr., T. E. Dungan, P. G. Neudeck, and J. W. Pabst, "GaAs Gate Dynamic Memory Technology," TR-EE 89-47, School of Electrical Engineering, Purdue University, August 1989.
- [14] K. Chen and J. A. Cooper, Jr., "Development of Process Technology for GaAs E/D MODFET Logic Circuits," TR-EE 89-57, School of Electrical Engineering, Purdue University, August 1989.
- [15] Y. Yin, J. A. Cooper, Jr., and H. Fu, "Investigation of a Resistive-Gate MESFET Contiguous Domain Oscillator," TR-EE 90-25, School of Electrical Engineering, Purdue University, April 1990.
- [16] P. G. Neudeck, J. A. Cooper, Jr., and M. R. Melloch, "Development, Demonstration, and Device Physics of FET-Accessed One-Transistor GaAs Dynamic Memory Technologies," TR-EE 91-21, School of Electrical Engineering, Purdue University, May 1991.

- [17] C. T. Gardner, J. A. Cooper, Jr., M. R. Melloch, J. W. Palmour, and C. H. Carter, Jr., "Electrical Characterization of NiPiN Structures in 6H-SiC," TR-EE-92-6, School of Electrical Engineering, Purdue University, January 1992.
- [18] J. A. Cooper, Jr., "Design Curves for Transient Heat Flow in Semiconductor Devices," TR-EE-92-9, School of Electrical Engineering, Purdue University, March 1992.
- [19] R. Hasan and J. A. Cooper, Jr., "Investigation and Development of a Transient Absorber Diode Using Gallium Arsenide," TR-EE 92-35, School of Electrical Engineering, Purdue University, September 1992.
- [20] J. Eun and J. A. Cooper, Jr., "High Temperature Ohmic Contact Technology to N-Type GaAs," TR-EE 93-7, School of Electrical Engineering, Purdue University, February 1993.
- [21] S. T. Sheppard, M. R. Melloch, and J. A. Cooper, Jr., "Development and Operation of Buried Channel Charge Coupled Devices in 6H Silicon Carbide," TR-ECE 96-8, School of Electrical and Computer Engineering, Purdue University, May 1996.

Issued Patents (21):

- [1] J. A. Cooper, Jr., "Apparatus and Method for Regenerating Charge," U.S. Patent #3,937,985, Feb. 10, 1976.
- [2] D. E. Blahut and J. A. Cooper, Jr., "Integrated Read Only Memory," U.S. Patent #4,139,907, Feb. 13, 1979.
- [3] D. E. Blahut and J. A. Cooper, Jr., "Programmable Logic Array," U.S. Patent #4,208,728, June 17, 1980.
- [4] J. A. Cooper, Jr. and R. H. Krambeck, "Multistage Logic Circuit Arrangement," U.S. Patent #4,291,247, Sept. 1981.
- [5] C. C. Chang, J. A. Cooper, Jr., D. Kahng, and S. P. Murarka, "Method of Fabricating MOS Field Effect Transistors," U.S. Patent #4,324,038, April 13, 1982.
- [6] J. A. Cooper, Jr., "Memory Cell for HEMT," U.S. Patent #4,635,083, January 6, 1987.
- [7] F. Capasso, J. A. Cooper, Jr., and K. K. Thornber, "Repeated Velocity Overshoot Semiconductor Device," U.S. Patent #4,719,496, January 12, 1988.
- [8] J. A. Cooper, Jr. and K. K. Thornber, "Transferred Electron Device," U.S. Patent #4,894,469, January 16, 1990.
- [9] J. A. Cooper, Jr., M. R. Melloch, and T. B. Stellwag, "Dynamic Random Access Memory Device," U.S. Patent #5,365,477, November 15, 1994.
- [10] J. A. Cooper, Jr., J. W. Palmour, C. H. Carter, Jr., "Nonvolatile Semiconductor Memories in SiC," U.S. Patent #5,465,249, November 7, 1995.
- [11] J. A. Cooper, Jr., "Structure for Increasing the Maximum Voltage of Silicon Carbide UMOS Power Transistors," U.S. Patent #6,180,958, January 30, 2001.
- [12] J. Henning, J. A. Cooper, Jr., K. J. Schoen, M. R. Melloch, and J. M. Woodall, "Dual-Metal-Trench Silicon Carbide Schottky Pinch Rectifier," U.S. Patent #6,362,495, March 26, 2002.
- [13] J. A. Cooper, Jr., M. R. Melloch, J. Shenoy, and J. Spitz, "Power Devices in Wide Bandgap Semiconductors," U.S. Patent #6,515,302, February 4, 2003.
- [14] J. A. Cooper, Jr. and A. Saha, "High-Voltage Power Semiconductor Device," U. S. Patent #7,498,633, March 3, 2009.
- [15] J. A. Cooper and A. Saha, "SiC Power DMOSFETs With Self-Aligned Source Contacts," U. S. Patent #8,035,112, October 11, 2011.
- [16] J. A. Cooper, Jr., and M. Matin, "Short-Channel Silicon Carbide Power MOSFET," U.S. Patent #8,133,789, March 13, 2012.
- [17] J. A. Cooper, Jr. and X. Wang, "Method for Fabricating a Semiconductor Device," U. S. Patent #8,343,841, January 1, 2013.
- [18] J. A. Cooper, Jr., and M. Matin, "Short-Channel Silicon Carbide Power MOSFET," U.S. Patent #8,476,697 B1, July 2, 2013.
- [19] J. A. Cooper, Jr., "Methods of Reducing the Electrical and Thermal Resistance of SiC Substrates and Devices Made Thereby," U.S. Patent # 9,780,206, October 2, 2017.
- [20] J. A. Cooper, "MOS-Based Power Semiconductor Device Having Increased Current Carrying Area and Method of Fabricating Same," U.S. Patent #9,997,599, June 12, 2018.
- [21] J. A. Cooper, "MOS-Based Power Semiconductor Device Having Increased Current Carrying Area and Method of Fabricating Same," U.S. Patent #11,145,721, October 12, 2021.

Pending Patent Applications (2):

- [1] J. A. Cooper, D. T. Morisette, and M. Sampath, "MOS devices with Increased Short Circuit Robustness," U.S. Non-Provisional Patent Application, submitted June 11, 2019.
- [2] A. Binder and J. A. Cooper, "Buried Field Shield in III-VI Compound Semiconductor Trench MOSFETs via Etch and Regrowth, Provisional Patent Application, submitted June 8, 2021.

Activities as a Referee:

Routinely referee papers for *IEEE Transactions on Electron Devices*, *IEEE Electron Device Letters*, *Journal of Applied Physics*, and *Applied Physics Letters*. Occasionally review proposals for the National Science Foundation.

Editorial Positions:

- [1] Member of Editorial Advisory Board, *IEEE Proceedings*, January 2004 – December 2009.
- [2] Associate Guest Editor, *Special Issue on Silicon Carbide*, *IEEE Transactions on Electron Devices*, 2008.
- [3] Guest Editor, *Special Issue on Silicon Carbide*, *IEEE Transactions on Electron Devices*, March 1999.
- [4] Associate Editor, *IEEE Transactions on Electron Devices*, March 1983 – March 1986.

Pending Publications (3):

- [1] R. P. Ramamurthy, N. Islam, M. Sampath, D. T. Morisette, and J. A. Cooper, "Design Optimization and Fabrication Technology for Tri-Gate Power MOSFETs in 4H-SiC," *in preparation*.
- [2] M. Sampath, D. T. Morisette, and J. A. Cooper, "Fabrication and Characterization of Deeply-Scaled, Fully-Self-Aligned Trench MOSFETs (IMOSFETs) in 4H-SiC," *in preparation*.
- [3] M. Sampath, D. T. Morisette, and J. A. Cooper, "Transient Switching Simulations of Deeply-Scaled, Fully-Self-Aligned Trench MOSFETs (IMOSFETs) in 4H-SiC," *in preparation*.

Other Activities:

- [1] Lecturer in Electrical Engineering and Computer Science, Columbia University, Fall 1978.
- [2] Visiting Lecturer in Electrical Engineering and Computer Science, Princeton University, Spring 1979.
- [3] Instructor, In-Hours Continuing Education Program, Bell Laboratories, Murray Hill, NJ, Fall 1974 and Spring 1980.
- [4] Faculty Advisor, Purdue Pilots, Inc. (student flying club), 1984 – 2011.
- [5] Founding Director, Purdue University Optoelectronics Center, 1986 - 1989.
- [6] Volunteer Pilot, AirLifeLine and Angel Flight Central (providing non-emergency transportation for medical patients), 1988 - 2008.
- [7] Member, Advisory Committee, Spring Mill Venture Partners LLC, September 22, 2003 – 2008.
- [8] In 1996, Cooper began a campaign to raise awareness of the need for new fabrication facilities for semiconductor research at Purdue. This movement gained widespread support within the university, leading to the \$58.3 million Birck Nanotechnology Center in Purdue's Discovery Park. From the Lilly Endowment, the Birck Center received an additional \$9 million in operating funds from August 1, 2001 – July 31, 2004 and \$750,000 in operating funds for FY 2005 – 2007. Cooper was a founding Co-Director of the Birck Nanotechnology Center, serving in this capacity from November 30, 2001 – October 31, 2006.
- [9] Mary Jo and Robert L. Kirk Interim Director of the Birck Nanotechnology Center, March 1, 2010 – September 30, 2011.
- [10] Founder and President of Sonrisa Research, Inc., a non-profit company conducting sponsored research for the government.

- [11] Member of the External Advisory Board, Ultra-Wide Bandgap Laboratory Directed Research and Development Grand Challenge, Sandia National Laboratories, Albuquerque, NM.
- [12] Consultant, Global Power Technologies Group (now SemiQ), Lake Forest, CA, 2014 – 2019.
- [13] Consultant, X-FAB Texas, Lubbock, TX, February 2015 - 2016.