

Filed on behalf of The Trustees of Purdue University

By: Michelle E. Armond

Douglas R. Wilson

Joseph Li

ARMOND WILSON LLP

4685 MacArthur Court, Suite 390

Newport Beach, CA 92660

Telephone: (949) 932-0778

Email: ipr@armondwilson.com

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

STMICROELECTRONICS, INC.

Petitioner,

v.

THE TRUSTEES OF PURDUE UNIVERSITY,

Patent Owner.

Case No. IPR2022-00252

U.S. Patent No. 7,498,633

PATENT OWNER'S PRELIMINARY RESPONSE

TABLE OF CONTENTS

I.	INTRODUCTION.....	1
II.	TECHNOLOGY OF THE '633 PATENT	5
A.	Silicon Planar and Trench Power MOSFETs.....	5
B.	Silicon Carbide.....	8
III.	BACKGROUND.....	9
A.	Co-Pending Litigation On The '633 Patent	9
B.	The Invention Of The '633 Patent	10
C.	U.S. Patent Application Publication No. 2004/0119076 (“Ryu”).....	14
D.	U.S. Patent No. 6,413,822 (“Williams”).....	14
IV.	LEVEL OF ORDINARY SKILL IN THE ART.....	15
V.	CLAIM CONSTRUCTION IS NOT NECESSARY TO DENY INSTITUTION HERE.....	18
VI.	THE BOARD SHOULD EXERCISE ITS DISCRETION TO DENY INSTITUTION DUE TO THE RISK OF DUPLICATIVE EFFORTS WITH THE DISTRICT COURT PROCEEDINGS AND THE CUMULATIVENESS OF THE ASSERTED REFERENCES.....	19
A.	The Board Should Deny Institution Under Section 314(a) Because The <i>Fintiv</i> Factors Support Denial.....	20
1.	Factor 1: Whether the Court granted a stay or evidence exists that one may be granted if a proceeding is instituted. ...	20
2.	Factor 2: The proximity of the Court’s trial date to the Board’s projected statutory deadline for a Final Written Decision.	21

3.	Factor 3: Investment in the parallel proceeding by the Court and the parties.	22
4.	Factor 4: Overlap between issues raised in the petition and in the parallel proceeding.	23
5.	Factor 5: Whether the petitioner and the defendant in the parallel proceeding are the same party.	24
6.	Factor 6: Other circumstances that impact the Board’s exercise of discretion, including the merits.	24
7.	None Of The <i>Fintiv</i> Factors Support Institution	26
B.	The Board Should Deny Institution Under Section 325(d) Because Petitioner Has Not Met Its Burden To Show Non-Cumulativeness Of Its References And Material Error By The Patent Office	26
1.	The Examiner Considered Numerous References During Prosecution Of The ’633 Patent	27
2.	Petitioner Fails To Show That Ryu and Williams Are Non-Cumulative Of Art Previously Considered By The Patent Office	30
3.	Petitioner Has Not Established The Patent Office Materially Erred In Allowing The Claims	32
VII.	THE PETITION’S CHALLENGE IS NOT REASONABLY LIKELY TO PREVAIL	32
A.	The Petition Fails To Show That The Combination Of Ryu And Williams Discloses Or Renders Obvious The Claimed JFET Region Width Limitations	33
1.	The Petition Fails To Show That Ryu Disclosed Or Rendered Obvious A JFET Region “Having A Width Less Than About Three Micrometers” As Required By Claim 9	34

2.	The Petition Fails To Show That Ryu Disclosed Or Rendered Obvious A JFET Region That “Has A Width Of About One Micrometer” As Required By Claim 10	39
B.	The Petition Fails To Show That It Would Have Been Obvious To Combine The Teachings Of Ryu And Williams To Arrive At The Claimed Invention.....	40
VIII.	CONCLUSION	43

TABLE OF AUTHORITIES

	Page No(s).
<i>Advanced Bionics, LLC v. MED-EL Elektromedizinische Geräte GmbH,</i> IPR2019-01469, 2020 WL 740292 (P.T.A.B. Feb. 13, 2020).....	27, 28, 31, 32
<i>Apple Inc. v. Fintiv, Inc.,</i> IPR2020-00019, 2020 WL 2126495 (P.T.A.B. Mar. 20, 2020).....	20, 24
<i>Apple Inc. v. Fintiv, Inc.,</i> IPR2020-00019, 2020 WL 2486683 (P.T.A.B. May 13, 2020)	21, 22, 23
<i>Atofina v. Great Lakes Chem. Corp.,</i> 441 F.3d 991 (Fed. Cir. 2006)	35, 36, 39
<i>Belden v. Berk-Tek LLC,</i> 805 F.3d 1064 (Fed. Cir. 2015)	42
<i>Cal. Inst. of Tech. v. Broadcom Ltd.,</i> 25 F.4th 976 (Fed. Cir. 2022)	25
<i>ClearValue, Inc. v. Pearl River Polymers, Inc.,</i> 668 F.3d 1340 (Fed. Cir. 2012)	36, 37
<i>Dynamic Drinkware, LLC v. Nat’l Graphics, Inc.,</i> 800 F.3d 1375 (Fed. Cir. 2015)	34
<i>Ecofasten Solar, LLC v. Unirac, Inc.,</i> IPR2021-01379, 2022 WL 443369 (P.T.A.B. Feb. 8, 2022).....	27
<i>Envtl. Designs, Ltd. v. Union Oil Co. of Cal.,</i> 713 F.2d 693 (Fed. Cir. 1983)	16
<i>Fitbit, Inc. v. Philips N. Am. LLC,</i> IPR2020-00828, 2020 WL 6470312 (P.T.A.B. Nov. 3, 2020).....	24
<i>Google LLC v. AGIS Software Dev., LLC,</i> IPR2020-00870, 2020 WL 6954675 (P.T.A.B. Nov. 25, 2020).....	22

STMicroelectronics v. The Trustees of Purdue Univ.
Patent No. 7,498,633 – IPR2022-00252

<i>Initiative for Meds., Access & Knowledge (I-MAK), Inc. v. Gilead Pharmasset LLC,</i> IPR2018-00390, 2018 WL 3493156 (P.T.A.B. July 19, 2018)	34, 35, 38
<i>KeyMe, LLC v. The Hillman Grp., Inc.,</i> IPR2020-01028, 2021 WL 129094 (P.T.A.B. Jan. 13, 2021)	24
<i>KSR Int’l Co. v. Teleflex Inc.,</i> 550 U.S. 398 (2007)	42
<i>In re Magnum Oil Tools Int’l, Ltd.,</i> 829 F.3d 1364 (Fed. Cir. 2016)	34
<i>Mylan Labs. Ltd. v. Janssen Pharmaceutica NV,</i> IPR2020-00440, 2020 WL 5580472 (P.T.A.B. Sept. 16, 2020)	21
<i>OSRAM Sylvania, Inc. v. Am. Induction Techs., Inc.,</i> 701 F.3d 698 (Fed. Cir. 2012)	35, 37, 38, 39
<i>Palo Alto Networks, Inc. v. Finjan, Inc.,</i> IPR2015-01979, 2017 WL 1040259 (P.T.A.B. Mar. 15, 2017)	42
<i>Realtime Data, LLC v. Iancu,</i> 912 F.3d 1368 (Fed. Cir. 2019)	19
<i>Samsung Elecs. Co., Ltd. v. Ancora Techs., Inc.,</i> IPR2020-01184, 2021 WL 42429 (P.T.A.B. Jan. 5, 2021)	22, 22, 25
<i>Vivid Techs., Inc. v. Am. Sci. & Eng’g, Inc.,</i> 200 F.3d 795 (Fed. Cir. 1999)	19
<i>Wasica Fin. GmbH v. Cont’l Auto. Sys., Inc.,</i> 853 F.3d 1272 (Fed. Cir. 2017)	38
<i>Xilinx, Inc. v. Analog Devices, Inc.,</i> IPR2021-00294, 2021 WL 2385526 (P.T.A.B. June 10, 2021)	31, 32

OTHER AUTHORITIES

35 U.S.C. § 103.....	28, 29
35 U.S.C. § 314.....	4, 19, 20, 26
35 U.S.C. § 325.....	4, 20, 26, 27, 32

TABLE OF EXHIBITS

Exhibit No.	Description
EX2001	File History of U.S. Patent No. 7,498,633
EX2002	Scheduling Order, <i>The Trustees of Purdue Univ. v. STMicroelectronics N.V. and STMicroelectronics, Inc.</i> , Case No. 6:21-cv-00727, Dkt. 45 (W.D. Tex. Nov. 22, 2021)
EX2003	Defendants' Preliminary Invalidity Contentions, <i>The Trustees of Purdue Univ. v. STMicroelectronics N.V. and STMicroelectronics, Inc.</i> , Case No. 6:21-cv-00727 (W.D. Tex. Jan. 14, 2022) (cover pleading)
EX2004	Excerpts from B. Jayant Baliga, SILICON CARBIDE POWER DEVICES (2005)
EX2005	Excerpts from B. Jayant Baliga, ADVANCED POWER MOSFET CONCEPTS (2010)
EX2006	Excerpts from Tsunenobu Kimoto and James A. Cooper, FUNDAMENTALS OF SILICON CARBIDE TECHNOLOGY (2014)
EX2007	Curriculum Vitae of James A. Cooper
EX2008	U.S. Patent App. Pub. No. 2003/0227052 A1 to Ono et al.
EX2009	U.S. Patent No. 6,573,534 to Kumar et al.
EX2010	U.S. Patent No. 6,137,139 to Zeng et al.
EX2011	U.S. Patent No. 5,545,908 to Tokura et al.
EX2012	STMicroelectronics, Inc.'s Opening Claim Construction Brief, <i>The Trustees of Purdue Univ. v. STMicroelectronics N.V. and STMicroelectronics, Inc.</i> , Case No. 6:21-cv-00727, Dkt. 66 (W.D. Tex. Feb. 21, 2022)
EX2013	Exhibit A to STMicroelectronics, Inc.'s Opening Claim Construction Brief, <i>The Trustees of Purdue Univ. v. STMicroelectronics N.V. and STMicroelectronics, Inc.</i> , Case No. 6:21-cv-00727, Dkt. 66-1 (W.D. Tex. Feb. 21, 2022)

STMicroelectronics v. The Trustees of Purdue Univ.
Patent No. 7,498,633 – IPR2022-00252

Exhibit No.	Description
EX2014	Plaintiff's Responsive Claim Construction Brief, <i>The Trustees of Purdue Univ. v. STMicroelectronics N.V. and STMicroelectronics, Inc.</i> , Case No. 6:21-cv-00727, Dkt. 70 (W.D. Tex. Mar. 14, 2022)
EX2015	STMicroelectronics, Inc.'s Reply Claim Construction Brief, <i>The Trustees of Purdue Univ. v. STMicroelectronics N.V. and STMicroelectronics, Inc.</i> , Case No. 6:21-cv-00727, Dkt. 74 (W.D. Tex. Mar. 28, 2022)
EX2016	Xu She, et al., <i>Review of Silicon Carbide Power Devices and Their Applications</i> , IEEE TRANSACTIONS ON INDUSTRIAL ELECTRONICS, vol. 64, no. 10 (Oct. 2017)
EX2017	IEEE Xplore profile page for Asmita Saha, https://ieeexplore.ieee.org/author/37284270100
EX2018	IEEE Xplore profile page for Sei-Hyung Ryu, https://ieeexplore.ieee.org/author/37274277600
EX2019	North Carolina State University profile page for Jayant Baliga, https://ece.ncsu.edu/people/bjbaliga/

Patent Owner The Trustees of Purdue University (“Purdue”) hereby submits its Preliminary Response to STMicroelectronics, Inc.’s (“ST”) petition for *inter partes* review of U.S. Patent No. 7,498,633 (“’633 Patent”).

I. INTRODUCTION

Professor James Cooper and his Ph.D. student Dr. Asmita Saha jointly invented the silicon carbide device described in the ’633 Patent at Professor Cooper’s cutting-edge silicon carbide research lab at Purdue University. After graduating with a master’s and Ph.D. from Stanford and Purdue, respectively, Professor Cooper was recruited to Bell Labs in 1973. EX2007 at 1-2. There, he was principal designer of Bell System’s first silicon-based CMOS microprocessor, which remains the dominant technology for most integrated circuits today.

Professor Cooper later returned to Purdue as a faculty member in Electrical and Computer Engineering, where he spent nearly 35 years at the helm of a large lab researching silicon carbide MOSFETs and related devices. *Id.* at 2. He is the founding Co-Director of Purdue’s Birck Nanotechnology Center. *Id.* During his tenure at Purdue, he served as major professor for 27 Ph.D. and 10 master’s thesis students, and his group has graduated many more, including Dr. Sei-Hyung Ryu, whose published application the Petition principally relies upon. *Id.* at 7-9.

Professor Cooper is an internationally recognized researcher in silicon carbide devices. Professor Cooper co-authored the definitive textbook on silicon carbide

STMicroelectronics v. The Trustees of Purdue Univ.
Patent No. 7,498,633 – IPR2022-00252

devices: FUNDAMENTALS OF SILICON CARBIDE TECHNOLOGY (Wiley 2014).

EX2006. His over 250 peer-reviewed publications have been cited thousands of times. EX2007 at 11-28.

His research lab has received over \$50,000,000 in government and industry support, including grants from Intel, Lucent, the National Science Foundation, NASA, DARPA, the U.S. Department of Energy, the U.S. Army, the Office of Naval Research, the Air Force Office of Scientific Research, and others. *Id.* at 2-7. His research has resulted in approximately 20 issued U.S. patents. *Id.* at 28. Among many others, Professor Cooper's lab has pioneered the following breakthroughs in silicon carbide semiconductors:

- first monolithic digital integrated circuits (1993)
- first planar DMOS power transistors (1996)
- first lateral DMOSFETs (1997)
- first oxide-protected UMOS power transistors (1998)
- first self-aligned short-channel DMOSFETs (2003)

The 2003 innovation became the basis for the first commercial silicon carbide power MOSFETs, and is the subject of the '633 Patent challenged here. In recognition of his considerable accomplishments and contributions to research on silicon carbide, Professor Cooper was elected a Life Fellow of the Institute of Electrical and Electronics Engineers (IEEE). *Id.* at 1.

The Petition is entirely premised on a fiction. Silicon is not silicon carbide. Decades of research were required to make silicon carbide MOSFETs commercially attainable. The conventional manufacturing techniques and designs for producing silicon MOSFETs do not readily translate to silicon carbide MOSFETs. The Petition pointedly ignores these technical challenges, selectively excerpting Baliga to incorrectly assert that conventional “DMOSFET [designs] can be readily translated into silicon carbide using known manufacturing techniques.” Paper 2 (“Pet.”) at 17 (citing EX1005 at 4:35-38). But, for example, Baliga itself recognized well-known diffusion fabrication techniques used in silicon semiconductors simply did not work in silicon carbide. *E.g.*, EX1005 at 4:38-47, 7:9-18. The disparate material properties of silicon carbide, such as the wider bandgap and different electrical field characteristics, posed significant design challenges in fabricating these devices. EX2016 at 8201-02. Baliga recognized “[t]he existing silicon power D-MOSFET and U-MOSFET structures do not directly translate to suitable structures in silicon carbide.” EX2004 at x.

If existing silicon MOSFET designs could be “readily translated into silicon carbide” DMOSFETs as Petitioner claims, it would have taken months to do it. It took decades. *See, e.g.*, EX2016 at 8194 (“The commercial SiC MOSFET was first released in 2011....”). Petitioner’s combining of disparate aspects of incompatible MOSFET designs fabricated from different substrates entirely ignores the

technological complexities of silicon carbide and is little more than a house of cards sitting atop impermissible hindsight.

The Board should deny institution for several reasons. First, proceeding here is a waste of the Board's and parties' resources. Petitioner asserted the identical references in co-pending litigation, and a jury will determine the validity of the '633 Patent before the Board is expected to render a Final Written Decision here, improperly affording Petitioner multiple bites at the apple to challenge validity of the same claims. As a result, none of the *Fintiv* factors favor institution. Additionally, over three office actions, the examiner thoroughly examined the claims and considered and evaluated numerous references with many of the same teachings as Petitioner's references. Petitioner does not meet its burden to show that its art is not cumulative or that the examiner materially erred in allowing the claims. The Board should exercise its discretion to deny institution under both 35 U.S.C. §§ 314(a) and 325(d).

Second, the Board should decline institution because Petitioner is unlikely to prevail on the merits. The Petition fails to show that the combination of Ryu and Williams discloses or renders obvious the claimed JFET region width limitations. The Petition ignores the criticality of the JFET region width as a parameter in planar MOSFET structures fabricated on a silicon carbide substrate. EX2004 at 303. Indeed, even Petitioner's own reference and expert confirm that the width of the

JFET region may depend on the desired blocking voltage and on-state resistance of the device, and that small variations in the JFET width can result in significant changes in the material properties of a device. EX1003 ¶ 44; EX2013 ¶ 41. Yet Petitioner offers no evidence (or even attorney argument) as to why Ryu’s disclosure of the JFET width range of 1-10 micrometers discloses with sufficient specificity the narrower range of 1-3 micrometers of Claim 9. Petitioner similarly offers no evidence or even argument to support Ryu’s alleged disclosure of the even narrower about 1 micrometer JFET width limitation of dependent Claim 10.

Finally, Petitioner’s proffered rationale for combining the incompatible MOSFET designs in the Ryu and Williams references is contradicted by Williams itself and is fatal to the Petition’s sole ground for all challenged claims. Thus, the Petition’s flaws further support denying institution.

For any of these reasons, the Board should not institute trial.

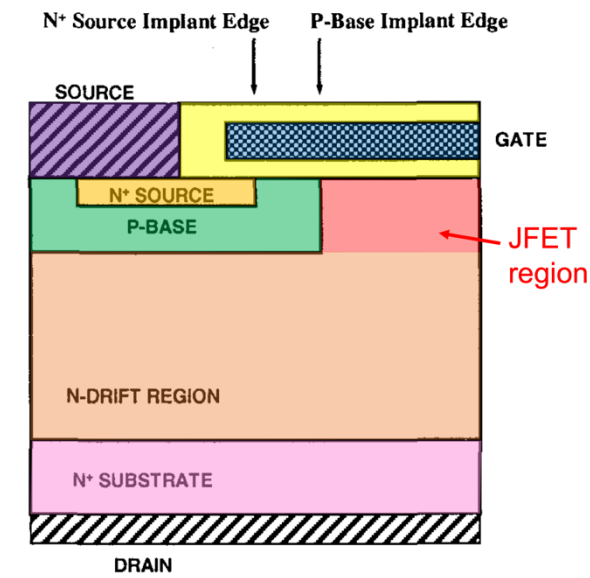
II. TECHNOLOGY OF THE ’633 PATENT

A. Silicon Planar and Trench Power MOSFETs

Efficient power electronic devices result in significant energy savings, increasing conservation of fossil fuels and mitigating environmental pollution. EX2005 at vii; EX2006 at xiii. In the early 1990s, most power MOSFETs were fabricated from a conventional silicon substrate. EX1005 at 4:22-23. These silicon MOSFETS performed best for “applications where the operating voltage of the

power circuit is relatively small (<100 V).” EX2005 at 1. But for “high operating voltages” required for “motors” and “electric vehicle drives,” “conventional silicon power MOSFET structures” with their high on-resistance simply do not work. *Id.*

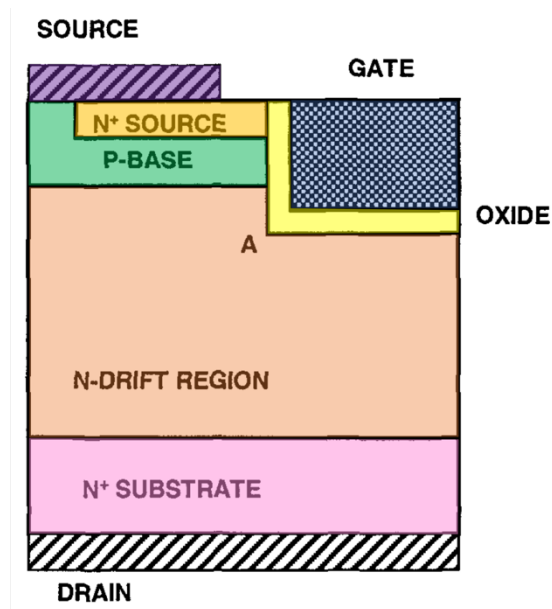
The channel in silicon planar power MOSFETs was created using the double diffusion (or D-MOS) fabrication process. EX2004 at 221. In the DMOS process, “the P-base and N^+ source regions are formed by ion implantations masked by a common edge defined by a refractory polysilicon gate electrode.” *Id.* The DMOSFET is a planar power MOSFET. EX2005 at 5 (“The D-MOSFET ... contains a ‘planar-gate’ structure.”). The basic structure of the planar power MOSFET is illustrated in the figure below.



EX2004 at 223 & Fig. 9.1 (annotated). The planar MOSFET structure includes a JFET region, shown above. *See, e.g.,* EX2005 at 24 & Fig. 2.1. The width of the JFET region in the planar MOSFET structure “must be optimized not only to obtain

the lowest specific on-resistance but to also control the electric field at the gate oxide interface.” EX2004 at 230.

In contrast to the planar power MOSFET, the silicon trench-gate power MOSFET or power UMOSFET was “developed in the 1990s by borrowing the trench technology originally developed for DRAM[]” memory devices. *Id.* at 307; *see also* EX2005 at 119 (“[T]he planar gate topology was replaced with a trench gate topology in the 1990s by creating the power U-MOSFET structure.”). The basic structure of the trench-gate power MOSFET or power UMOSFET in silicon is shown in the figure below.



EX2004 at 308 & Fig. 11.1 (annotated). “The JFET region is eliminated within the power U-MOSFET structure because the trench extends beyond the bottom of the

P-base region in order to form a channel connecting the N⁺ source region with the N-drift region.” EX2005 at 66.

Silicon DMOSFETs and UMOSFETs have different designs with different considerations related to their functionality and performance.

B. Silicon Carbide

In the early 1990s, researchers started looking to “power MOSFET structures built using silicon carbide” which had “very promising characteristics for applications that require blocking voltages of up to 5,000 V.” EX2005 at 1. Compared to silicon, silicon carbide with its wide-bandgap offered on-state resistance that was orders-of-magnitude lower at a given blocking voltage, higher thermal conductivity, and about a ten-times higher breakdown electric field strength. EX2006 at xiii; *see also* EX1005 at 4:27-31. Petitioner’s own cited reference explains that “[t]hese characteristics would allow silicon carbide power devices to operate at higher temperatures, higher power levels and with lower specific on resistance than conventional silicon based power devices.” EX1005 at 4:31-34. However, because of these very different material properties, harnessing the potential of silicon carbide MOSFETs remained elusive. The first commercial devices were not introduced until about 20 years later, in 2011. EX2016 at 8194.

Compared with other power devices, “the development of a suitable silicon carbide MOSFET structure has been more problematic” because the “existing silicon

power D-MOSFET and U-MOSFET structures do not directly translate to suitable structures in silicon carbide.” EX2004 at x. In other words, “the power MOSFET structures developed in silicon cannot be directly utilized to form high performance silicon carbide devices.” *Id.* at 222. Thus, development of suitable MOSFET designs in silicon carbide is uniquely difficult.

The width of the JFET region in a silicon carbide planar MOSFET is among those very important parameters that are difficult to optimize. In silicon carbide planar MOSFET structures, “the JFET width is a critical parameter” and “[i]ts optimization is important for obtaining high performance devices.” EX2004 at 303; *see also, e.g.*, EX2013 ¶ 41 (“In a 2002 article on silicon carbide MOSFETs, JFET widths between 2-5µm were evaluated by simulation and it was reported that ‘if the JFET gap is too small, specific on-resistance increases significantly.’”). “The optimization of the JFET width requires taking into consideration both the on-resistance and the electric field developed at the gate oxide interface.” EX2004 at 293.

III. BACKGROUND

A. Co-Pending Litigation On The ’633 Patent

In July and October 2021 respectively, Purdue filed suit asserting the ’633 Patent against ST and Wolfspeed. *The Trustees of Purdue Univ. v. STMicroelectronics N.V. and STMicroelectronics, Inc.*, No. 6:21-cv-00727

STMicroelectronics v. The Trustees of Purdue Univ.
Patent No. 7,498,633 – IPR2022-00252

(W.D. Tex.); *The Trustees of Purdue Univ. v. Wolfspeed, Inc.*, No. 1:21-cv-00840 (M.D.N.C.). The ST litigation is quickly advancing. By the time the Board is expected to issue its institution decision, the Court will have held a claim construction hearing and likely construed the claims. EX2002 at 3. Trial in the ST case is set for April 24, 2023. *Id.* at 5. No stay has been sought or entered in either of the co-pending district court actions.

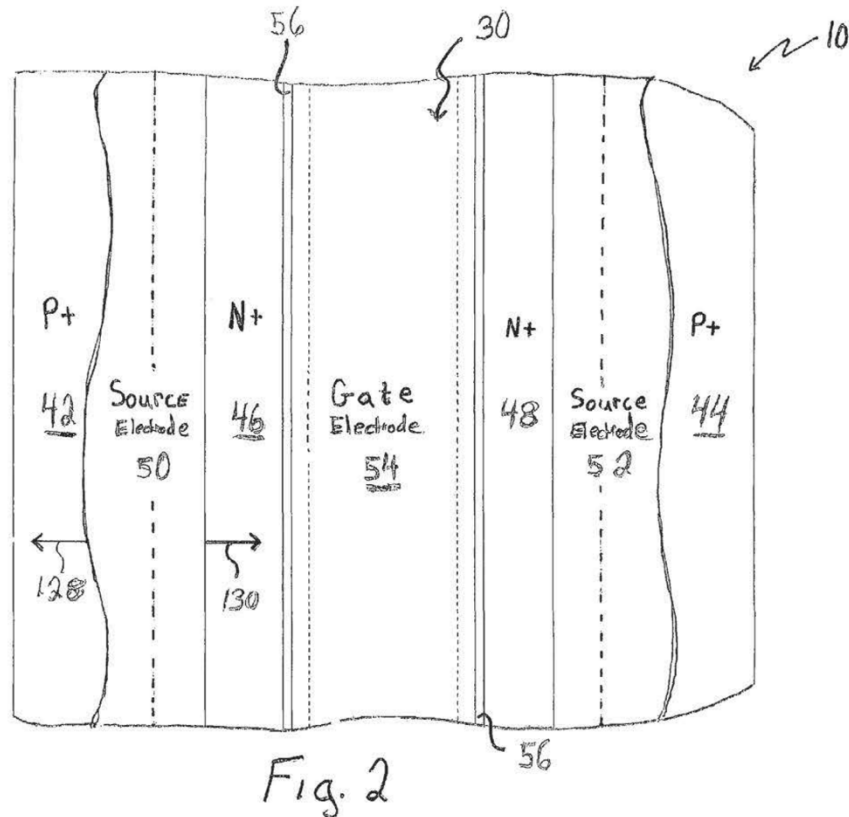
B. The Invention Of The '633 Patent

The '633 Patent introduced an important innovation to commercializing high-power silicon carbide DMOSFETs. The '633 Patent is titled “High-Voltage Power Semiconductor Device,” and describes semiconductor device designs for high-voltage power applications fabricated on a silicon carbide substrate. EX1001 at 1:12-14, 1:40-45.

The '633 Patent recognized the criticality of the width of the JFET region. It observed that “for high-voltage power applications, a high blocking voltage is generally desirable” and that “[a]s the specific on-resistance of the device decreases, the efficiency of the semiconductor device may be improved.” *Id.* at 1:25-27, 1:31-33. However, it also recognized that “the typical fabrication techniques for reducing the specific on-resistance of high-voltage power semiconductor devices may also reduce the blocking voltage of the device.” *Id.* at 1:33-36. Thus, the '633 Patent describes and claims a JFET region having a width “less than about three

micrometers.” *Id.* at 2:47-48, 10:7-8. The “short width 36 [of the JFET region 30] relative to a typical DMOSFET device... may reduce the specific on-resistance of the semiconductor device 10” and “may tend to increase the blocking voltage of the semiconductor device 10.” *Id.* at 6:21-24, 6:45-50.

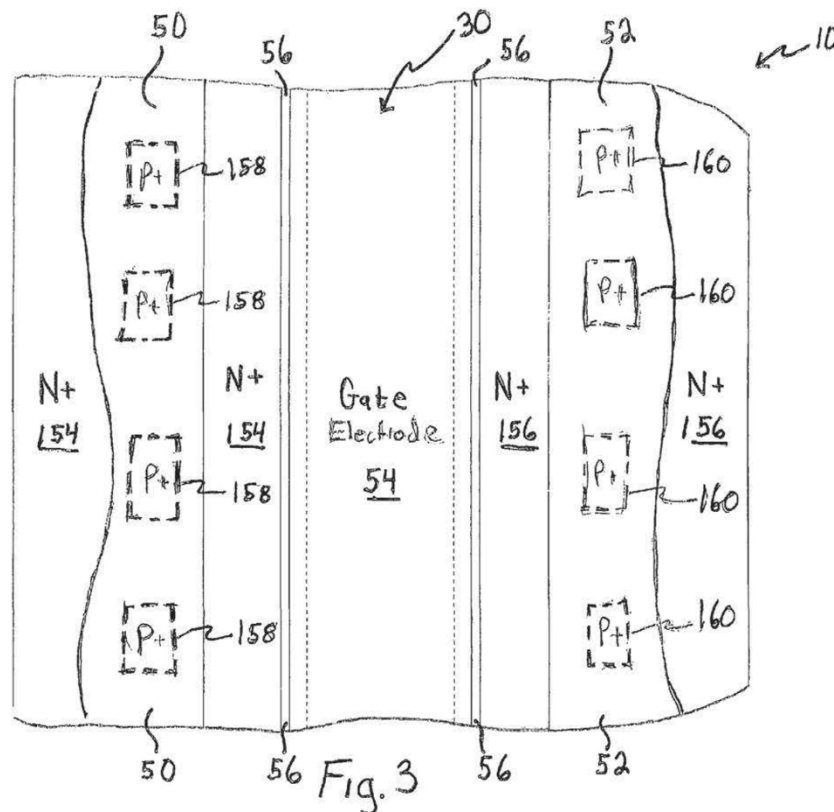
Another problem recognized by the ’633 Patent invention is that the reduction in specific on-resistance of the JFET region will ultimately lead to “the source resistance of the device becom[ing] one of the dominating contributions to the specific on-resistance of the device.” *Id.* at 7:22-28. The ’633 Patent explained that the typical parallel longitudinal overlap between base contact regions 42, 44; source regions 46, 48; and source electrodes 50, 52 as shown in Figure 2, reproduced below, “can result in an undesirable source resistance if the source regions 46, 48 are misaligned with respect to the base contact regions 42, 44 and/or the source regions 46, 48 are misaligned with respect to source electrodes 50, 42 [sic: 52].” *Id.* at 7:39-44.



EX1001 at Fig. 2.

The '633 Patent thus explained with reference to Figure 3, reproduced below, that “to reduce the likelihood of misalignment between the source electrodes and the source regions, ... the semiconductor device 10 is fabricated to have source regions 154, 156 that each include a plurality of base contact regions 158, 160 formed in source regions 154, 156, respectively.” *Id.* at 7:52-57. Figure 3 of the '633 Patent shows that “the base contact regions 158, 160 are embodied as small ‘islands’ or regions within the larger source regions 154, 156” and are “formed to be located in a central location under the source metallic electrodes 50, 52 with areas of source regions 154, 156 spaced between each base contact regions 158, 160.” *Id.* at 7:57-63.

As the '633 Patent explains, “even if the source electrodes 50, 52 are slightly misaligned with respect to the source regions 154, 156, the source resistance of the semiconductor device 10 is not substantially increased because a substantial portion of the source regions 154, 156 would remain aligned with the respective source electrode 50, 52.” *Id.* at 8:1-6.



EX1001 at Fig. 3.

In this IPR, Petitioner challenges the validity of only Claims 9-11 of the patent’s fifteen claims. *Id.* at 8:56-10:55; Pet. at 4.

C. U.S. Patent Application Publication No. 2004/0119076 (“Ryu”)

Petitioner primarily relies on Ryu to assert unpatentability of all challenged claims. Pet. at 4. However, as discussed in Section VI.B.2. *infra*, Ryu contains substantially similar disclosures to the Ono reference previously considered and relied upon by the examiner in multiple office actions during the original prosecution of the ’633 Patent. Ryu disclosed nothing about the configuration of a plurality of first and second base contact regions, much less their configuration relative to a first and a second electrode. *See generally* EX1003. Petitioner nonetheless asserts invalidity based on Ryu both here and in the co-pending litigation. EX2003 at 9.

D. U.S. Patent No. 6,413,822 (“Williams”)

Williams pertained to a different MOSFET structure on a fundamentally different substrate than the ’633 Patent. Williams is titled “Super-Self-Aligned Fabrication Process of Trench-Gate DMOS With Overlying Device Layer” and described a “trench MOSFET ... compris[ing] a semiconductor body having a trench formed therein.” EX1004 at 1, 7:46-48. Williams’ trench MOSFET was formed solely from silicon, not silicon carbide. *See, e.g., id.* at 11:53-56 (“The process describes a method to form a dense array of trench capacitors with access to the silicon on the backside or to the surface between the trenches without the need for a contact mask to contact the top of the silicon mesa regions.”). Williams discussed a “problem with existing conventional trench-gated vertical DMOS devices” that had

a significant effect on “low voltage devices.” *Id.* at 7:17-27. Williams is explicitly directed to low voltage MOSFETs. Petitioner argues invalidity based on Williams both here and in the co-pending litigation. EX2003 at 9.

IV. LEVEL OF ORDINARY SKILL IN THE ART

Petitioner asserts, incorrectly and without any support, that a “person of ordinary skill in the art (‘POSITA’) at the time of the earliest claimed priority date of the ’633 patent would have had the equivalent of a Bachelor’s degree in electrical engineering or a related subject and two or more years of experience in the field of semiconductor devices.” Pet. at 3.

Petitioner’s asserted level of skill in the art is absurdly low given the silicon carbide technology involved in the ’633 Patent. For example, despite the unique problems associated with silicon carbide devices, Petitioner’s proposed POSITA need not have had any experience with silicon carbide. *See id.* Petitioner completely overlooks the highly specialized and sophisticated nature of the materials and technology at issue, including the problems encountered in the art, and never addresses the level of skill of the inventors of the ’633 Patent or the authors of its relied-upon references.

“Factors that may be considered in determining level of ordinary skill in the art include: (1) the educational level of the inventor; (2) type of problems encountered in the art; (3) prior art solutions to those problems; (4) rapidity with

which innovations are made; (5) sophistication of the technology; and (6) educational level of active workers in the field.” *Envtl. Designs, Ltd. v. Union Oil Co. of Cal.*, 713 F.2d 693, 696 (Fed. Cir. 1983).

Based on the relevant factors, one of ordinary skill in the art at the time of the claimed invention would have had:

- a Master’s degree in electrical engineering or related subject with a concentration in design and fabrication of silicon carbide power semiconductor devices, or
- a Bachelor’s degree in electrical engineering or related subject, in addition to two years of experience in design and fabrication of silicon carbide power semiconductor devices.¹

Less work experience may be compensated by a higher level of relevant education, and vice versa, where “relevant” in either case must include design and fabrication of silicon carbide power semiconductor devices.

This level of ordinary skill is consistent with the specialized nature of the field of silicon carbide power semiconductor devices. This specialized field is

¹ Tellingly, Petitioner’s expert has not a single patent, publication, or presentation involving a silicon carbide power semiconductor device. *See* EX1002 at 101-120.

demonstrated, for example, by Dr. Baliga’s 2005 textbook, SILICON CARBIDE POWER DEVICES, which sought to “provide[] a unified treatment of silicon carbide power device structures.” EX2004 at x. The level of skill is also supported by the unique set of problems encountered in the field of silicon carbide power devices. Dr. Baliga explained in his textbook that “the development of a suitable silicon carbide MOSFET structure has been more problematic” and the “existing silicon power D-MOSFET and U-MOSFET structures do not directly translate to suitable structures in silicon carbide.” *Id.*

The educational level of the inventors and others in the field further support the level of ordinary skill in the art. Dr. Cooper received his Ph.D. in electrical engineering in 1973 and had been a professor of electrical and computer engineering at Purdue for nearly two decades at the time of the claimed invention. EX2007 at 1-2. His co-inventor, Dr. Saha, had a Master’s degree in electronics and electrical communication engineering in 1999 and was working towards completing her Ph.D. in electrical engineering when she jointly invented the ’633 Patent. EX2017 at 1.

The few others who were active in the highly specialized field of silicon carbide power devices had similar backgrounds. For example, the named inventor of Petitioner’s Ryu reference received his Ph.D. in electrical and computer engineering from Purdue in 1997, and Dr. Baliga, the named inventor and author of Petitioner’s EX1005 and EX1016 references, received his Ph.D. in electrical

engineering in 1974 and has been a distinguished university professor at North Carolina State University since 1997. EX2018 at 1; EX2019 at 1-2.

The background of the inventors and those in the field corroborate the proposed level of ordinary skill in the art at the time of the claimed invention.

V. CLAIM CONSTRUCTION IS NOT NECESSARY TO DENY INSTITUTION HERE

In the parallel Texas district court litigation, the parties dispute the construction of two terms. Specifically, the parties dispute the construction of “less than about three micrometers” in Claim 9 and whether the preamble of Claim 9 is limiting. The parties’ proposed constructions in the litigation are summarized below.

Claim Term	Patent Owner’s Proposed Construction	Petitioner’s Proposed Construction
Claim 9 preamble	The preamble is not limiting.	The preamble is limiting.
“less than about three micrometers” (Claim 9)	Plain and ordinary meaning; no construction necessary	Indefinite

EX2014 at 7, 10. In contrast to its litigation positions, Petitioner asserts in the Petition that “the Board need not construe any terms of the challenged claims” in this proceeding. Pet. at 38.

For purposes of denying institution and finding that Petitioner has not met its burden to show a reasonable likelihood of prevailing, Patent Owner believes the Board need not construe any terms of the challenged claims. *Realtime Data, LLC v. Iancu*, 912 F.3d 1368, 1375 (Fed. Cir. 2019) (“The Board is required to construe ‘only those terms... that are in controversy, and only to the extent necessary to resolve the controversy.’” (quoting *Vivid Techs., Inc. v. Am. Sci. & Eng’g, Inc.*, 200 F.3d 795, 803 (Fed. Cir. 1999))). Patent Owner reserves the right to assert additional claim construction positions should the Board institute IPR.

VI. THE BOARD SHOULD EXERCISE ITS DISCRETION TO DENY INSTITUTION DUE TO THE RISK OF DUPLICATIVE EFFORTS WITH THE DISTRICT COURT PROCEEDINGS AND THE CUMULATIVENESS OF THE ASSERTED REFERENCES

As a threshold matter, the Board should exercise its discretion to deny institution of *inter partes* review under 35 U.S.C. § 314(a) because the parallel Texas district court litigation is progressing and is set for trial first. The Texas litigation involves the same patent and asserted references and is scheduled for trial in April 2023, before any Final Written Decision is expected here. Conducting a validity trial after a jury will address patent validity is an inefficient use of resources, contravenes the broad effect of statutory IPR estoppel created by Congress by giving Petitioner two bites at the apple to challenge patent validity, and does not support institution under *Fintiv*.

The Board should also exercise its discretion to deny institution under 35 U.S.C. § 325(d) because the examiner expressly considered and evaluated numerous references with many of the same relevant teachings as Petitioner’s references. Petitioner improperly presents references which are missing key limitations, with no showing that the references here are different from the references the examiner considered or explanation of prior examiner error. The Petition provides no basis to second-guess the examiner’s conclusions.

A. The Board Should Deny Institution Under Section 314(a) Because The *Fintiv* Factors Support Denial

The accelerated schedule of the parallel pending litigation, and the weakness of Petitioner’s patentability challenge, each support denying institution under *Fintiv*. *See Apple Inc. v. Fintiv, Inc.*, IPR2020-00019, 2020 WL 2126495, at *2 (P.T.A.B. Mar. 20, 2020) (precedential). None of the *Fintiv* factors support instituting IPR.

1. Factor 1: Whether the Court granted a stay or evidence exists that one may be granted if a proceeding is instituted.

Under *Fintiv* factor 1, Petitioner admits that it has not sought a stay of the co-pending Western District of Texas district court action, asserting only that it “intends” to seek a stay. Pet. at 83. Moreover, even if Petitioner requests a stay, the Texas court is highly unlikely to grant it. *See, e.g., MV3 Partners, LLC v. Roku, Inc.*, No. 6:18-cv-00308-ADA, Dkt. 83 at 53 (W.D. Tex. July 22, 2019) (denying stay request brought after IPR institution and before claim construction hearing).

Here, the parties’ parallel litigation is further along than in *MV3 Partners* with a *Markman* hearing scheduled to take place well in advance of the institution decision deadline. EX2002 at 3.

Because the district court is unlikely to enter a stay, this factor weighs against institution. *See, e.g., Mylan Labs. Ltd. v. Janssen Pharmaceutica NV*, IPR2020-00440, 2020 WL 5580472, at *6 (P.T.A.B. Sept. 16, 2020) (*Fintiv* factor 1 “leans towards denial of institution” where the facts “indicate that no stay is likely to be entered”).

2. Factor 2: The proximity of the Court’s trial date to the Board’s projected statutory deadline for a Final Written Decision.

The district court trial is scheduled to begin on April 24, 2023 before the statutory deadline of any Final Written Decision in June 2023. EX2002 at 5. There is no reason to believe that the trial date will move. *See, e.g., Samsung Elecs. Co., Ltd. v. Ancora Techs., Inc.*, IPR2020-01184, 2021 WL 42429, at *5 (P.T.A.B. Jan. 5, 2021) (discretionary denial of petition: “Petitioner fails to provide sufficient evidence to show that the trial date has been changed or will be postponed. ... Judge Albright has stated that he ‘definitely intends to keep this case on track.’”). Indeed, the Board “generally take[s] courts’ trial schedules at face value absent some strong evidence to the contrary.” *Apple Inc. v. Fintiv, Inc.*, IPR2020-00019, 2020 WL 2486683, at *5 (P.T.A.B. May 13, 2020) (informative).

Petitioner speculates that the trial “may be postponed,” including due to delays resulting from the “uncertainty surrounding the COVID-19 pandemic.” Pet. at 84. But the district court has been consistently conducting civil trials, and pandemic court restrictions are widely lifting. Moreover, the Board consistently rejects such speculation regarding delays. *See, e.g., Samsung Elecs.*, 2021 WL 42429, at *5 (“Although we acknowledge the possibility of a Covid-19 related delay, we generally take courts’ trial schedules at face value absent some strong evidence to the contrary.”); *Google LLC v. AGIS Software Dev., LLC*, IPR2020-00870, 2020 WL 6954675, at *5 (P.T.A.B. Nov. 25, 2020) (“While we appreciate that the trial date is susceptible to change if and when the District Court determines good cause exists to do so, we decline to speculate whether such a contingency will occur.”).

The earlier district court trial date favors discretionary denial under *Fintiv* factor 2. *See Fintiv*, 2020 WL 2486683, at *5 (*Fintiv* factor 2 weighs in favor of discretionary denial where the “District Court trial is scheduled to begin two months before [the] deadline to reach a final decision”).

3. Factor 3: Investment in the parallel proceeding by the Court and the parties.

The co-pending district court case has been moving forward since July 2021. Infringement and invalidity contentions have been served; fact discovery is underway; and claim construction briefing and an April 29, 2022 *Markman* hearing

will be completed before the Board’s institution decision deadline. EX2002 at 1-3. Petitioner’s assertion that “[a]ll significant stages of litigation—including discovery, claim construction... remain in the future,” Pet. at 85, was inaccurate when made because non-party fact discovery opened a week before the petition was filed. EX2002 at 2. “Based on the level of investment and effort already expended on claim construction and invalidity contentions in the District Court,” *Fintiv* factor 3 weighs in favor of discretionary denial. *Fintiv*, 2020 WL 2486683, at *6.

4. Factor 4: Overlap between issues raised in the petition and in the parallel proceeding.

Petitioner’s invalidity contentions in the parallel litigation contradict Petitioner’s assertion that it “expects its invalidity positions in the district court case will diverge from the ground of unpatentability described in this Petition.” Pet. at 86. Petitioner’s invalidity contentions identify the same Ryu and Williams references relied upon in the Petition. EX2003 at 9. Thus, the issues of patentability in the Petition duplicate the patentability challenges that Petitioner has raised in the district court.

Despite the overlap in issues raised in the Petition and at the district court, Petitioner provided no stipulation to eliminate it, instead vaguely “reserv[ing] the right to enter a stipulation relating to the district court case that would prevent and/or reduce overlap with the requested IPR.” Pet. at 86. Because “Petitioner fails to

stipulate that it will not pursue in the district court any ground raised or that could have reasonably been raised in this proceeding,” its duplicative challenge should be rejected. *KeyMe, LLC v. The Hillman Grp., Inc.*, IPR2020-01028, 2021 WL 129094, at *6 (P.T.A.B. Jan. 13, 2021).

The overlap in invalidity challenges between the two proceedings supports denying institution under *Fintiv* factor 4. *See Fintiv*, 2020 WL 2126495, at *5.

5. Factor 5: Whether the petitioner and the defendant in the parallel proceeding are the same party.

Factor 5 also supports denial of institution. ST is both the Petitioner here and the defendant in the parallel Texas litigation. Petitioner does not dispute that *Fintiv* factor 5 favors discretionary denial. *See Pet.* at 86.

6. Factor 6: Other circumstances that impact the Board’s exercise of discretion, including the merits.

Petitioner’s patentability challenge is deeply flawed on the merits. As explained herein, the Petition’s relied-upon rationale for combining its two references, which lack teaching of key limitations, is refuted by the Petition’s own reference. Because Petitioner’s challenge lacks merit, *Fintiv* factor 6 heavily favors discretionary denial. *See, e.g., Fitbit, Inc. v. Philips N. Am. LLC*, IPR2020-00828, 2020 WL 6470312, at *9 (P.T.A.B. Nov. 3, 2020) (“[T]he merits of the proceeding weigh in favor of denying institution....”).

This challenge should be rejected outright because Petitioner seeks to evade the broad scope of statutory estoppel and improperly obtain two bites at the apple to challenge validity of the '633 Patent. Tellingly, Petitioner proffered no stipulation that validity will be exclusively decided at the PTAB. Because the validity of the '633 Patent will be decided by a jury before issuance of any Final Written Decision, Patent Owner will be unfairly denied the effects of statutory estoppel, which the Federal Circuit explained “applies not just to claims and grounds asserted in the petition and instituted for consideration by the Board, but to all grounds not stated in the petition but which reasonably could have been asserted against the claims included in the petition.” *Cal. Inst. of Tech. v. Broadcom Ltd.*, 25 F.4th 976, 991 (Fed. Cir. 2022).

In addition, given the obvious weakness of the Petition’s challenge, “[i]f the Board were to institute and Petitioner ultimately loses, it would not resolve validity challenges raised by unrelated third parties, including the defendants” in other district court proceedings. *Samsung Elecs.*, 2021 WL 42429, at *10. Petitioner’s *Fintiv* analysis deliberately ignores that, in addition to the Texas litigation, the '633 Patent is also involved in another parallel district court proceeding, *Trustees of Purdue Univ. v. Wolfspeed, Inc.*, No. 1:21-cv-00840 (M.D.N.C.). Indeed, co-defendant Wolfspeed subsequently filed its own IPR challenge to the '633 Patent.

IPR2022-00761. Instituting review here would lead to more than two duplicative proceedings addressing validity of the same patent.

7. None Of The *Fintiv* Factors Support Institution

The weight of the *Fintiv* factors supports the Board exercising its discretion to deny review under Section 314(a) here, thereby conserving the Board's and parties' resources and preventing multiple proceedings evaluating the same invalidity challenges that are set to be decided by a jury before the Board could conclude this IPR. The true motive of this IPR and the others is to drive up the costs of litigating infringement for Patent Owner, a public, non-profit university whose resources are limited. The funds expended in defending this IPR will reduce the resources available for Patent Owner's core mission of educating students, conducting fundamental research and maintaining the United States' technological supremacy in an important field of semiconductor technology.

B. The Board Should Deny Institution Under Section 325(d) Because Petitioner Has Not Met Its Burden To Show Non-Cumulativeness Of Its References And Material Error By The Patent Office

The Board should decline institution under 35 U.S.C. § 325(d) because, despite Petitioner bearing the burden to show non-cumulativeness, the Petition's sole ground relies on two references without any showing that they are not substantially the same as art previously considered by the examiner during the original prosecution of the '633 Patent or any showing of material error by the Patent Office.

STMicroelectronics v. The Trustees of Purdue Univ.
Patent No. 7,498,633 – IPR2022-00252

See, e.g., Ecofasten Solar, LLC v. Unirac, Inc., IPR2021-01379, 2022 WL 443369, at *16 (P.T.A.B. Feb. 8, 2022) (discretionary denial of petition: “Petitioner does not present any evidence or argument to persuade us that [the Petition’s references] are not the same or substantially the same as the prior art raised during the original prosecution or reexamination. Petitioner has the burden of proof to establish that it is entitled to the relief requested.”).

Section 325(d) provides that the Board may elect not to institute trial if “the same or substantially the same prior art or arguments previously were presented to the Office.” The Board applies a two-part framework: “(1) whether the same or substantially the same art previously was presented to the Office”; and, if so, (2) “whether the petitioner has demonstrated that the Office erred in a manner material to the patentability of challenged claims.” *Advanced Bionics, LLC v. MED-EL Elektromedizinische Geräte GmbH*, IPR2019-01469, 2020 WL 740292, at *3 (P.T.A.B. Feb. 13, 2020) (precedential).

1. The Examiner Considered Numerous References During Prosecution Of The ’633 Patent

Petitioner’s two-page selective recounting of the prosecution history glosses over the references already considered by the examiner during an extended examination of the claims spanning three office actions. The Petition entirely ignores the cumulateness of its references and their relied-upon teachings in the

Petition and fails to identify any material error by the Patent Office. *See* Pet. at 30-31. Under such circumstances, “the Director generally will exercise discretion not to institute *inter partes* review.” *Advanced Bionics*, 2020 WL 740292, at *3.

Indeed, during prosecution, the examiner thoroughly considered numerous references and properly allowed the claims. In a first Office Action, the examiner rejected pending Claims 12 and 13 (issued Claims 9 and 10) as being anticipated by U.S. Patent Publication No. 2003/0227052 A1 to Ono et al. (“Ono”). EX2001 at 72-73. The examiner also rejected pending Claim 14 (issued Claim 11) under 35 U.S.C. § 103 as being unpatentable over Ono in view of U.S. Patent No. 5,545,908 to Tokura et al. (“Tokura”). *Id.* at 75-76.

In response to the first Office Action, the applicant amended pending Claim 12 (issued Claim 9) to require a silicon-carbide substrate and also “a plurality of [first/second] base contact regions defined in the [first/second] source region, each of the plurality of [first/second] base contact regions being spaced apart from each other.” *Id.* at 94.

In a second Office Action, the examiner again rejected pending Claims 12 and 13 (issued Claims 9 and 10), this time under 35 U.S.C. § 103 as being unpatentable over Ono in view of U.S. Patent No. 6,573,534 to Kumar et al. (“Kumar”) and in further view of U.S. Patent No. 6,137,139 to Zeng et al. (“Zeng”). *Id.* at 122-125. The examiner also rejected pending Claim 14 (issued Claim 11)

under 35 U.S.C. § 103 as being unpatentable over Ono in view of Kumar and Zeng and in further view of Tokura. *Id.* at 129-30. The fact that the examiner was forced to find three and four reference combinations to make obviousness rejections—and no rejections were based on anticipation—shows that the examination was thorough and the search for prior art was both detailed and exhaustive.

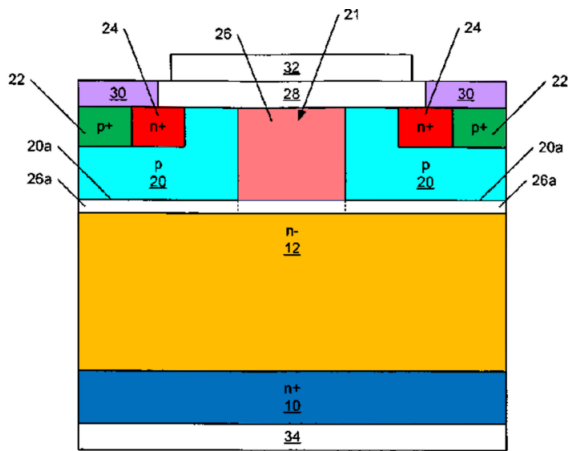
In response to the second Office Action, the applicant further amended pending Claim 12 (issued Claim 9) to require “a [first/second] source electrode formed over the [first/second] source region, the [first/second] source electrode defining a longitudinal axis” and to further clarify that “each of the plurality of [first/second] base contact regions” are “spaced apart from each other in a direction parallel to the longitudinal axis defined by the [first/second] source electrode.” *Id.* at 148. The applicant also argued that the examiner’s proposed art combination which included references (Ono and Zeng) “directed toward MOSFET devices having silicon substrates” and a reference (Kumar) “directed toward silicon-carbide MOSFET devices” “ignores the technical aspects of silicon-carbide MOSFET devices.” *Id.* at 151-155.

In a third Office Action, and in response to the applicant’s amendments, the examiner withdrew the rejections to pending Claims 12-14 (issued Claims 9-11) and allowed those claims. *Id.* at 162, 170. Regarding pending Claim 12, the examiner stated that the prior art “alone or in combination fails to anticipate or render obvious”

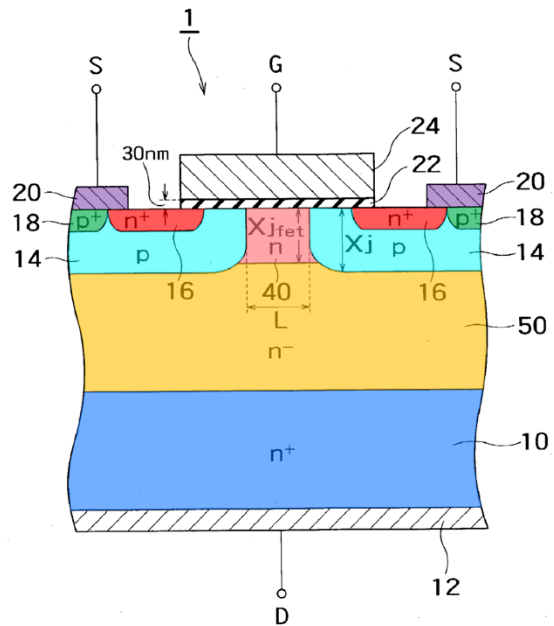
the first and second source electrode limitations and the plurality of first and second base contact regions limitations, along with the other limitations of Claim 12. *Id.* at 170-71. A Notice of Allowance subsequently issued indicating the allowance of Claims 12-14 and other claims. *Id.* at 199.

2. Petitioner Fails To Show That Ryu and Williams Are Non-Cumulative Of Art Previously Considered By The Patent Office

Petitioner provides no showing that the present Petition is not just a repeat of the original prosecution. As Petitioner acknowledges, the examiner initially rejected the challenged claims “over several prior art references” the Petition completely fails to identify, much less differentiate over the cited art. Pet. at 30. The examiner subsequently allowed the claims, finding that these references Ono (EX2008), Kumar (EX2009), and Zeng (EX2010) “alone or in combination fail[] to anticipate or render obvious” the limitations of pending Claim 12 (issued Claim 9). EX2001 at 170-71, 199. Petitioner never attempts to compare or contrast the teachings of the Petition’s references with those already considered in detail during prosecution. Even a cursory review of the Petition’s references and the art cited during prosecution reveals substantial similarities. For example, as shown in the side-by-side comparison below, Ryu’s planar MOSFET is identical to Ono’s planar MOSFET in relevant respects.



Petition's Proffered Reference
EX1003 (Ryu) at Fig. 2A (annotated
by Petitioner); Pet. at 36



Reference Cited by Examiner
EX2008 (Ono) at Fig. 1 (annotated)

Because Petitioner fails to show any material differences between the Petition's references and Ono, Kumar, Zeng, and Tokura considered during prosecution, the first prong of the *Advanced Bionics* framework is satisfied. *Advanced Bionics*, 2020 WL 740292, at *8; see also *Xilinx, Inc. v. Analog Devices, Inc.*, IPR2021-00294, 2021 WL 2385526, at *10 (P.T.A.B. June 10, 2021) (discretionary denial of petition: "Petitioner also does not compare or contrast the teachings of [the Petition's reference] relative to [the art considered during prosecution].").

3. Petitioner Has Not Established The Patent Office Materially Erred In Allowing The Claims

The Petition also provides no showing that “the Office erred in a manner material to the patentability of challenged claims.” *Advanced Bionics*, 2020 WL 740292, at *3.

Petitioner presents no new evidence, or even argument, suggesting that the Petition’s asserted references include teachings that were unavailable to the examiner when he allowed the claims. *See* Pet. at 30-31. Petitioner simply urges the Board to reach a different conclusion on the same facts, asserting only that the “Examiner did not have the benefit of *Ryu* and *Williams*, which are not of record.” *Id.* at 31. This is insufficient to meet Petitioner’s burden to show error. *See, e.g., Xilinx*, 2021 WL 2385526, at *10 (“Petitioner does not provide any indication that the Examiner’s prior art analysis in the prosecution history was error.”).

Because Petitioner fails to demonstrate non-cumulativeness or material error by the Office, the Board should exercise its discretion to deny institution under Section 325(d).

VII. THE PETITION’S CHALLENGE IS NOT REASONABLY LIKELY TO PREVAIL

The Board should additionally decline to institute trial because Petitioner fails to show a reasonable likelihood of prevailing on its sole ground. The Petition’s references lack teaching of key limitations, rendering Petitioner’s challenge doomed

to fail. Even setting aside their deficiencies, Petitioner cannot demonstrate a reasonable likelihood of prevailing because the Petition's asserted motivation to combine its two references is to any competent POSITA both deficient and fatally flawed.

A. The Petition Fails To Show That The Combination Of Ryu And Williams Discloses Or Renders Obvious The Claimed JFET Region Width Limitations

The Petition fails to show that Ryu and Williams teach or suggest all limitations of the challenged claims. For example, Claim 9 recites “a JFET region defined between the first source region and the second source region, the JFET region having a width less than about three micrometers.” EX1001 at 10:6-8. Claim 10, which depends from Claim 9, recites the further requirement that “the JFET region has a width of about one micrometer.” *Id.* at 10:9-11. The Petition's sole ground relies exclusively on Ryu to teach these limitations. Pet. at 78-81. But the Petition fails to show that Ryu disclosed or rendered obvious a JFET region “having a width less than about three micrometers” much less having “a width of about one micrometer.” The Board should deny institution because it is now too late for Petitioner to cure the Petition's deficiencies.

**1. The Petition Fails To Show That Ryu Disclosed Or
Rendered Obvious A JFET Region “Having A Width Less
Than About Three Micrometers” As Required By Claim 9**

Petitioner fails to meet its burden to show that Ryu disclosed or rendered obvious the claimed JFET region “having a width less than about three micrometers.” *See In re Magnum Oil Tools Int’l, Ltd.*, 829 F.3d 1364, 1375 (Fed. Cir. 2016) (“In an *inter partes* review, the burden of persuasion is on the petitioner to prove “unpatentability by a preponderance of the evidence,” 35 U.S.C. § 316(e), and that burden never shifts to the patentee.” (quoting *Dynamic Drinkware, LLC v. Nat’l Graphics, Inc.*, 800 F.3d 1375, 1378 (Fed. Cir. 2015))).

The only argument the Petition presents is the conclusory statement that “Ryu discloses that the JFET region 21 may have a width of less than about three micrometers because the recited width of ‘less than about three micrometers’ is disclosed with sufficient specificity by Ryu’s disclosure of a JFET width ‘from about 1 [micrometer] to about 10 [micrometers].’” Pet. at 80 (alterations in original). In support, the Petition cites the Subramanian declaration that merely repeats the conclusory argument verbatim without any additional explanation or analysis. *See id.* (citing EX1002 ¶ 138).

Petitioner fails to present any evidence or analysis supporting its assertion that the broader range of Ryu disclosed with “sufficient specificity” the narrower claimed range. *Initiative for Meds., Access & Knowledge (I-MAK), Inc. v. Gilead*

Pharmasset LLC, IPR2018-00390, 2018 WL 3493156, at *4 (P.T.A.B. July 19, 2018) (denying institution: “[T]he Petition contains no analysis tending to show that the broad percentage range disclosed in Ross ’645 teaches, ‘with sufficient specificity,’ the narrower range required by claim 1.” (internal citation omitted)). Thus, Petitioner cannot meet its burden to show invalidity.

The Petition is completely silent as to how Ryu’s broad range of “1 [micrometer] to about 10 [micrometers]” teaches “with sufficient specificity” the claimed range of “less than about three micrometers.” *Atofina v. Great Lakes Chem. Corp.*, 441 F.3d 991, 999 (Fed. Cir. 2006) (a reference’s broad range discloses a narrower claimed range only if the reference describes the claimed range “with sufficient specificity”). While a reference’s broad range can disclose a narrower claimed range in certain circumstances, “this inquiry necessarily includes a factual component.” *OSRAM Sylvania, Inc. v. Am. Induction Techs., Inc.*, 701 F.3d 698, 705 (Fed. Cir. 2012). In particular, “how one of ordinary skill in the art would understand the relative size of a genus or species in [the] particular technology is of critical importance.” *Id.* at 706.

In this case, the evidence of criticality of the JFET region width is overwhelming and uncontradicted. Ryu itself explains the criticality of the width of the JFET region:

[I]t may be difficult to control the precise gap between the p-wells 20 (the region which may be referred to as the JFET region 21) and/or the depth of the p-wells 20. ***If this gap is too high, the field in the gate oxide can become too high when the device is in the blocking state. However, if the gap is too narrow, the resistance of the JFET region 21 may become very high.*** Accordingly, gaps of from about 1 μm to about 10 μm are preferred. The particular gap utilized for a given device may depend upon the desired blocking voltage and on-state resistance of the device.

EX1003 ¶ 44 (emphasis added). Indeed, Petitioner’s own expert, Dr. Subramanian, confirmed Ryu’s observation, explaining: “In a 2002 article on silicon carbide MOSFETs, JFET widths between 2-5 μm were evaluated by simulation and it was reported that ‘if the JFET gap is too small, specific on-resistance increases significantly.’” EX2013 ¶ 41 (citation omitted). In other words, even within the smaller range of 2 to 5 micrometers, JFET width can cause a significant increase in specific on-resistance.

By describing the criticality of JFET width and making clear that despite the range provided, the “particular gap utilized for a given device may depend upon the desired blocking voltage and on-state resistance of the device,” (EX1003 ¶ 44), both Ryu and Dr. Subramanian expressly contradict Petitioner’s required showing that there is no “difference across the range.” *ClearValue, Inc. v. Pearl River Polymers, Inc.*, 668 F.3d 1340, 1345 (Fed. Cir. 2012) (distinguishing *Atofina* because “here,

there is no allegation of criticality or any evidence demonstrating any difference across the range”); *see also OSRAM Sylvania*, 701 F.3d at 705 (same). As a result, Petitioner’s reliance on *ClearValue* is misplaced. In any event, Petitioner made no effort to make its required showing, which is fatal to the Petition.

Ryu’s and Dr. Subramanian’s guidance as to the criticality of the JFET width are not alone. For example, in his text, SILICON CARBIDE POWER DEVICES, Dr. Baliga observes that for planar MOSFET structures, “the JFET width is a critical parameter” and “[i]ts optimization is important for obtaining high performance devices.” EX2004 at 303.

Moreover, Petitioner itself concedes that Ryu’s disclosed range represents a wide variation in silicon carbide devices. Petitioner asserts in the parallel litigation that a “POSITA would understand that JFET widths in a silicon carbide power MOSFET could *widely*” vary. EX2012 at 19 (emphasis added). To support that assertion, Petitioner cites a paragraph from a declaration of Dr. Subramanian in which he relies on a patent by Dr. Ryu to observe that “[i]n a patent issued around the time of the application for the ’633 Patent for a silicon carbide power MOSFET, JFET widths of 1-10 μ m were reported.” EX2013 ¶ 41. No actual working silicon carbide MOSFET products are disclosed where such a wide range is used because none exist. Petitioner even contradicts its required showing that there is no “difference across the range,” *ClearValue*, 668 F.3d at 1345, admitting in the parallel

litigation that “the JFET parameter here is intended to have an effect on the performance of the device” EX2015 at 7.

Additionally, the Petition presents no argument that the claimed width of “less than about three micrometers” would have been obvious. *See* Pet. at 80. Thus, Petitioner could not prevail on a theory that Claim 9’s JFET width range would have been obvious because it is not in the Petition. *See, e.g., I-MAK*, 2018 WL 3493156, at *5 (Petitioner not reasonably likely to prevail because “[t]he Petition does not provide a separate analysis of the obviousness challenge....”).

Moreover, Petitioner cannot cure the Petition’s deficiencies after institution. *See, e.g., Wasica Fin. GmbH v. Cont’l Auto. Sys., Inc.*, 853 F.3d 1272, 1285-86 (Fed. Cir. 2017) (rejecting Petitioner’s “attempts to cure the petition’s deficiencies in its subsequent briefing to the Board” where the “petition failed to set forth the necessary ‘factual components’ needed to advance this legal theory” (quoting *OSRAM Sylvania*, 701 F.3d at 705-06)).

Because the Petition fails to show that Ryu disclosed or rendered obvious the claimed width of “less than about three micrometers” required by all challenged claims, the Board should deny institution.

2. The Petition Fails To Show That Ryu Disclosed Or Rendered Obvious A JFET Region That “Has A Width Of About One Micrometer” As Required By Claim 10

Petitioner’s inadequate contentions for Claim 10 mimic those for Claim 9. *See* Pet. at 80-81. Accordingly, for at least the same reasons discussed with respect to Claim 9 in Section VII.A.1. *supra*, the Board should find Petitioner has failed to show a likelihood of establishing that Ryu disclosed or rendered obvious the additional requirement of Claim 10 that the claimed JFET region “has a width of about one micrometer.” Also, the disclosure of a range (*e.g.*, 1-10 micrometers) is not a disclosure of an endpoint of that range (*e.g.*, 1 micrometer). *See, e.g., Atofina*, 441 F.3d at 1000 (“[T]he disclosure of a range of 150 to 350 °C does not constitute a specific disclosure of the endpoints of that range, *i.e.*, 150 °C and 350 °C”).

In addition to failing to address the required factual inquiry, *see OSRAM Sylvania*, 701 F.3d at 706, and being insufficient as a matter of law, *see Atofina*, 441 F.3d at 1000, Petitioner’s contention that Ryu disclosed Claim 10’s more exacting requirement is particularly problematic. As mentioned above, Petitioner concedes that Ryu’s disclosure of a JFET width “from about 1 [micrometer] to about 10 [micrometers]” is a wide range. Moreover, compared with Claim 9, Claim 10 claims an even narrower range of “about one micrometer,” and Petitioner admits that “a POSITA would understand that the different selections of MOSFET parameters create design tradeoffs.” EX2012 at 19.

Despite Claim 10's narrow range and the overwhelming evidence from multiple sources including Petitioner's expert regarding the criticality of the claimed JFET width, Petitioner provides no additional explanation or analysis showing how Ryu's broad range discloses with sufficient specificity Claim 10's specific requirement that the JFET region "has a width of about one micrometer."

The Board should find no reasonable likelihood of success on Claim 10.

B. The Petition Fails To Show That It Would Have Been Obvious To Combine The Teachings Of Ryu And Williams To Arrive At The Claimed Invention

The Board should additionally deny institution because Petitioner cannot demonstrate a reasonable likelihood of prevailing based on the deficient motivation to combine Ryu and Williams asserted in the Petition.

The Petition does not assert that its primary reference, Ryu, disclosed "a plurality of [first/second] base contact regions defined in the [first/second] source region, each of the plurality of [first/second] base contact regions being spaced apart from each other in a direction parallel to the longitudinal axis defined by the [first/second] source electrode" as required by Claim 9. Instead, the Petition asserts that Williams disclosed these features. *See* Pet. at 63, 77. Specifically, the Petition relies on Williams' configuration of P⁺ contacts shown in Figure 19E. *See id.* at 63-64, 77.

However, the Petition’s rationale for combining Ryu with features from Williams is deeply flawed. According to the Petition, “a POSITA would have been motivated to use *Williams*’s teachings of multiple and periodic P+ body contact regions in *Ryu* to maximize the contact of the p+ regions and ruggedize *Ryu*’s MOSFET.” *Id.* at 69. But Williams’ Figure 19E, relied upon by Petitioner, does not maximize the contact of the P+ region or the ruggedness of a MOSFET. Williams explained that “[t]he window ... design[] of FIGS. 19E ... [has] similar geometric features to the corrugated and strapped corrugated design[] of FIG[]. 19A ..., but with better N+ contact resistance and *less P+ contact area (less rugged)*.” EX1004 at 17:15-19 (emphasis added). According to Williams, the design of Figure 19E maximizes N+ contact resistance at the expense of P+ contact area resulting in a “less rugged” design. In other words, Petitioner’s hindsight assertion that a POSITA would have looked to Williams’ Figure 19E to “maximize the contact of the p+ regions” is expressly refuted by Williams itself.

Petitioner’s additional formulations of this asserted motivation fare no better. Petitioner asserts that a POSITA would be motivated to use Williams’ Figure 19E embodiment in Ryu “because, as *Williams* teaches, such a configuration would help reduce on-resistance, while continuing to provide the needed connection between the n+ regions 24 and the p-wells 20 via the p+ regions 22 to ruggedize *Ryu*’s MOSFET against unwanted activation of the parasitic BJT.” Pet. at 70. But, as

noted *supra*, instead of promoting ruggedness, Williams instead taught that Figure 19E *sacrificed* ruggedness for better N+ contact resistance. EX1004 at 17:15-19. Thus, Figure 19E’s embodiment did not satisfy the motivation Petitioner provides, according to Williams itself.

Finally, Petitioner’s assertions that its proposed use of Williams’ Figure 19E in Ryu “would have been a simple substitution of one known element ... for another” and “would have been obvious to try” do not articulate motivations to combine. *See* Pet. at 71-72. Instead, these *ipse dixit* assertions merely articulate whether a POSITA could have made the asserted substitution, not whether a POSITA would have been motivated to make the asserted substitution. *Palo Alto Networks, Inc. v. Finjan, Inc.*, IPR2015-01979, 2017 WL 1040259, at *24 (P.T.A.B. Mar. 15, 2017) (“It is not enough to assert that the prior art provides two options and that it would have been predictable to implement either. An obviousness rationale generally requires some identification of ‘a design need or market pressure to solve a problem’ before looking at the ‘finite number of identified, predictable solutions.’” (quoting *KSR Int’l Co. v. Teleflex Inc.*, 550 U.S. 398, 421 (2007))); *see also Belden v. Berk-Tek LLC*, 805 F.3d 1064, 1073 (Fed. Cir. 2015) (“[O]bviousness concerns whether a skilled artisan not only *could have made* but *would have been motivated to make* the combinations or modifications of prior art to arrive at the claimed invention.”).

Taking the Petition’s asserted motivation to combine at face value, a proper reading of Williams would have led a POSITA to Williams’ Figure 19C, not Figure 19E, to increase ruggedness. In contrast to Williams’ Figure 19E embodiment, Williams disclosed that the “segmented N+ source design of FIG. 19C reduces the N+ contact and the channel perimeter further, compromising on-resistance *to achieve enhanced ruggedness.*” EX1004 at 16:63-65 (emphasis added). Even if Petitioner could change course now and rely on Figure 19C instead (it cannot), Figure 19C does not disclose the configuration of the “plurality of [first/second] base contact regions” required by Claim 9. Accordingly, either way, Petitioner cannot demonstrate a reasonable likelihood of prevailing on its obviousness challenge.

Because the Petition’s rationale for combining the teachings of Ryu and Williams in its sole ground is fatally flawed, the Board should deny institution.

VIII. CONCLUSION

For each of the foregoing reasons, Patent Owner respectfully requests that the Board deny institution.

ARMOND WILSON LLP

Dated: March 30, 2022

By: /Michelle E. Armond/

Michelle E. Armond (Reg. No. 53,954)

Douglas R. Wilson (Reg. No. 54,542)

Joseph Li (Reg. No. 74,998)

Attorneys for The Trustees of Purdue University

CERTIFICATE OF COMPLIANCE

Pursuant to 37 C.F.R. § 42.24(d), the undersigned certifies that foregoing **PATENT OWNER'S PRELIMINARY RESPONSE**, exclusive of the parts exempted as provided in 37 C.F.R. § 42.24, contains 8,996 words and therefore complies with the type-volume limitations of 37 C.F.R. § 42.24.

ARMOND WILSON LLP

Dated: March 30, 2022

By: /Michelle E. Armond/

Michelle E. Armond (Reg. No. 53,954)

Douglas R. Wilson (Reg. No. 54,542)

Joseph Li (Reg. No. 74,998)

Attorneys for The Trustees of Purdue University

CERTIFICATE OF SERVICE

The undersigned certifies that pursuant to 37 C.F.R. § 42.6(e), a true copy of the foregoing **PATENT OWNER'S PRELIMINARY RESPONSE** and **EXHIBITS 2001-2019** are being served electronically on March 30, 2022 to the following lead counsel for Petitioner to the following email addresses:

Richard Goldenberg
richard.goldenberg@wilmerhale.com

Gregory Lantier
gregory.lantier@wilmerhale.com

Scott Bertulli
scott.bertulli@wilmerhale.com

Trishan Efram
trishan.esram@wilmerhale.com

Wilmer Cutler Pickering Hale and Dorr LLP
60 State Street
Boston, MA 02109

ARMOND WILSON LLP

Dated: March 30, 2022

By: /Michelle E. Armond/

Michelle E. Armond (Reg. No. 53,954)

Douglas R. Wilson (Reg. No. 54,542)

Joseph Li (Reg. No. 74,998)

Attorneys for The Trustees of Purdue University