

UNITED STATES PATENT AND TRADEMARK OFFICE

PATENT TRIAL AND APPEAL BOARD

SAMSUNG ELECTRONICS CO., LTD.

Petitioner

v.

BISHOP DISPLAY TECH LLC

Patent Owner

Case No. IPR2022-00501

Patent No. 7,995,047

DECLARATION OF ALEX Z. KATTAMIS, PH.D., P.E.

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 - e. 10(d): “a plurality of voltage-current converting elements for generating an electric current in accordance with said reference voltage held in said voltage holding circuit;”162
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I. INTRODUCTION

1. My name is Alex Kattamis. I make this declaration based upon my own personal knowledge and, if called upon to testify, would testify competently to the matters contained herein.

2. I am over the age of 21 and am competent to make this declaration.

3. I have been retained by Baker Botts LLP on behalf of Samsung to provide technical assistance in the inter partes review of U.S. Patent No. 7,995,047, which I may abbreviate as **“the ’047 Patent”** or refer to as the **“Challenged Patent.”** This declaration is a statement of my opinions on issues related to the unpatentability of claims of the Challenged Patent.

4. I am a salaried employee of Exponent. Exponent charges \$495 per hour for my time plus expenses for work performed in connection with this project. I have received no additional compensation for work in this case, and my compensation does not depend upon the contents of this report, any testimony I may provide, or the ultimate outcome of the case.

II. EXPERIENCE AND QUALIFICATIONS

5. In formulating my opinions, I have relied upon my knowledge, training, and experience in the relevant art. My qualifications are stated more fully in my curriculum vitae, which has been provided as Appendix A. My CV also lists publications on which I am a named author and identifies parties on behalf of whom

I have previously provided expert testimony within the past four years. Here, I provide a brief summary of my qualifications.

6. I am a Senior Managing Engineer in Exponent's Electrical Engineering and Computer Science practice. I received my B.A. in Electrical Engineering from the University of Connecticut in 2002 and an M.A. and Ph.D. in Electrical Engineering from Princeton University in 2004 and 2007 respectively.

7. During my time at the University of Connecticut and through a grant from the National Science Foundation I designed and implemented devices for people with disabilities. This included the design and manufacture of analog and digital control systems for devices including go-karts and electronic lifts.

8. Before joining Princeton University, I worked as a design engineering intern at General Electric Industrial Systems. There I designed and implemented analog and digital circuits. This work included the implementation of current sense devices for feedback in power supplies

9. At Princeton University my research was focused on designing and fabricating pixel circuits on non-conventional substrates for driving liquid-crystal display (LCDs) and active-matrix organic light emitting diode displays (AMOLEDs).

10. Throughout my career at Exponent I have worked extensively on AMOLED and LCD displays including driver circuits, and thin-film transistor and pixel architectures.

11. I am a licensed Professional Engineer in the State of Connecticut, the State of Georgia, the Commonwealth of Massachusetts, the State of New Jersey, the State of New York, the Commonwealth of Pennsylvania, the State of Rhode Island, and in State of Texas. I am also designated a Model Law Engineer by the National Council of Examiners for Engineering.

12. I am a Senior Member of the Institute of Electrical and Electronics Engineers (IEEE), which is the world's largest technical professional organization dedicated to advancing technology for the benefit of humanity.

13. Therefore, based on my education, professional experience, scholarly books and publications, I am an expert in the relevant field of the Challenged Patent at issue here and have been an expert in this field since before the Challenged Patent was filed with the United States Patent and Trademark Office ("USPTO"). I am familiar with how a person having ordinary skill in the art would have understood and used the terminology found in the Challenged Patent at the time of its filing.

III. TASK SUMMARY AND MATERIALS REVIEWED

14. I have been asked to review the Challenged Patent and its prosecution history, to provide an understanding of the technology relevant to the Challenged

Patent, to review certain prior-art references, and analyze whether or not those references disclose or teach limitations of claims from the Challenged Patent. The opinions stated in this declaration are from the perspective of a person of ordinary skill in the art (POSITA).

IV. LIST OF EXHIBITS

15. In forming my opinions, I have reviewed the Challenged Patent, its prosecution history and referenced cited by the Examiner, the materials cited in the List of Exhibits, and the materials cited throughout my declaration.

Ex.	Description of Exhibits
1001	U.S. Patent No. 7,995,047 to Makoto Mizuki et al., entitled “Current Driving Device” (filed December 12, 2007 and issued August 9, 2011) (“ ’047 Patent ” or “ Challenged Patent ”)
1002	Declaration of Dr. Alex Kattamis in Support of Petition for <i>Inter Partes</i> Review of U.S. Patent No. 7,995,047, with CV attached as Appendix A (“ Kattamis Decl. ”)
1003	File History of U.S Patent No. 7,995,047 (App. No. 11/954,659) (“ ’047 Patent File History ”)
1004	M. Shimoda, K. Abe, H. Haga, H. Asada, H. Hayama, K. Iguchi, D. Iga, H. Imura, and S. Miyano, “An integrated poly-Si TFT current data driver with a data-line pre-charge function,” <i>Journal of the Society for Information Display</i> 11/3 (2003): 461-466 (“ Shimoda ”)
1005	U.S. Patent Publication No. 2006/0170629 to Jong-Hak Baek, entitled “Display Driver Circuit, Current Sample/Hold Circuit and Display Driving Method Using the Display Driver Circuit” (filed January 27, 2006 and published August 3, 2006) (“ Baek ”)

1006	U.S. Patent Publication No. 2005/0017765 to Kazuhiro Sasaki and Katsuhiko Morosawa, entitled ““Current Generation Supply Circuit and Display Device” (filed July 14, 2004 and published January 27, 2005 (“ Sasaki ”))
1007	John A. Camara, ELECTRICAL ENGINEERING REFERENCE MANUAL FOR THE ELECTRICAL AND COMPUTER PE EXAM, 6th ed. (Professional Publications, Inc.: 2002), ISBN: 1-888577-56-8 (“ Camara ”)
1008	Willem den Boer, ACTIVE MATRIX LIQUID CRYSTAL DISPLAYS, 1st ed. (Newnes: 2005), ISBN: 0-750678-13-5 (“ den Boer ”)
1009	M.K. Han, “AM backplane for AMOLED,” <i>Proc. Of ASID</i> 6 (Oct. 8-12, 2006): 53-58 (“ Han ”)
1010	B. Hekmatshoar, A. Kattamis et al., “A Novel TFT-OLED integration for OLED-independent pixel programming in amorphous-Si AMOLED pixels,” <i>Journal of the Society for Information Display</i> 16/1 (2008): 183-188.
1011	A. Kattamis et al., “Active-matrix organic light-emitting displays employing two thin-film-transistor a-Si:H pixels on flexible stainless-steel foil,” <i>Journal of the Society for Information Display</i> 15/7 (2007): 433-437.
1012	About the SID (dated June 16, 2004), available at: https://web.archive.org/web/20040616180753/http://www.sid.org/about/about.html
1013-1018	NOT USED
1019	Declaration of Dr. James L. Mullins sponsoring Exhibit 1004 and Exhibits 1020-1027 (“ Mullins Decl. ”)
1020	Copy of Shimoda owned by the Linda Hall Library
1021	Copy of Shimoda owned by the United States Library of Congress
1022	WorldCat entry for Journal of the Society for Information Display (Missouri)
1023	WorldCat entry for Journal of the Society for Information Display (Washington, DC)

1024	OPAC record from Linda Hall Library for Journal of the Society for Information Display
1025	OPAC record from United States Library of Congress for Journal of the Society for Information Display
1026	J.L. Sanford and F.R. Libsch, “V _t compensated voltage-data a-Si TFT AMOLED pixel circuits,” <i>Journal of the Society for Information Display</i> 11/1 (2004): 65-73 (“ Sanford ”)
1027	Y.-S. Son, S.-K. Kim, Y.-J. Jeon et al., “P-40: A Novel Data Driving Method and Circuits for AMOLED Displays,” <i>SID Symposium Digest of Technical Papers</i> 37 (2006): 343-346 (“ Son ”)

Other than the prosecution history, Ex. 1003, respectively, all citations to exhibits reference original page numbers found in the underlying document, and unless noted, all emphases have been added.

V. SUMMARY OF CONCLUSIONS AND GROUNDS FOR CHALLENGE OF '047 PATENT

16. After reviewing the materials identified in the List of Exhibits, I have concluded that each of Claims 1-4, 9, and 10 (“**Challenged Claims**”) of the '047 Patent would have been anticipated and/or obvious to a person of ordinary skill in the art, based on the following grounds.

Ground	'047 Patent Claims	Basis for Invalidity
1	1-4, 9	Anticipated by Shimoda (Ex. 1004)
2	1-4, 9	Obvious over Shimoda (Ex. 1004) in view of the knowledge of a POSITA
3	1-4, 9	Anticipated by Baek (Ex. 1005)
4	1-4, 9	Obvious over Baek (Ex. 1005) in view of the knowledge of a POSITA
5	10	Anticipated by Sasaki (Ex. 1006)

Ground	'047 Patent Claims	Basis for Invalidity
6	10	Obvious over Sasaki (Ex. 1006)

VI. UNDERSTANDING OF THE GOVERNING LAW

A. LEVEL OF ORDINARY SKILL IN THE ART

17. When analyzing a patent, I understand that it is important to identify the relevant art pertaining to the patent as well as the level of ordinary skill in that art at the time of the claimed invention. The “art” is the field of technology to which the patent is related.

18. I have been instructed by counsel that the person of ordinary skill in the art (“**POSITA**”) is a hypothetical person who is presumed to know the relevant prior art. I understand that the actual inventor’s skill is not determinative of the level of ordinary skill. I further understand that the factors that may be considered in determining the level of skill include: the types of problems encountered in the art; prior art solutions to those problems; rapidity with which innovations are made; sophistication of the technology; and educational level of active workers in the field. I understand that not all such factors may be present in every case, and one or more of them may predominate.

B. LEGAL STANDARD FOR CLAIM CONSTRUCTION

19. I understand that the first step in determining whether a patent claim would have been anticipated or obvious is to ascertain how a POSITA would have understood the claim terms.

20. I have been instructed by counsel on the law regarding claim construction and patent claims, and I understand that a patent may include two types of claims: independent claims and dependent claims. An independent claim stands alone and includes only the limitations it recites. A dependent claim can depend from an independent claim, or it can further depend from another dependent claim. I understand that a dependent claim includes all the limitations that it recites, in addition to all the limitations recited in the claim(s) from which it depends.

21. It is my understanding that in proceedings before the USPTO, the claims of a patent are to be construed under what is referred to as the “Phillips standard.” I understand that this means that claim terms of a patent are given the meaning the terms would have to a POSITA, in view of the description provided in the patent itself and the patent’s file history.

22. I understand that to determine how a person of ordinary skill would understand a claim term, one should look to those sources available that show what a person of skill in the art would have understood the disputed claim language to mean. I understand that, in construing a claim term, one looks primarily to the

intrinsic patent evidence, including the words of the claims themselves, the remainder of the patent, and the patent's prosecution history. I understand that extrinsic evidence, which is evidence external to the patent and the prosecution history, may also be useful in interpreting patent claims when the intrinsic evidence itself is insufficient.

23. I understand that words or terms should be given their ordinary and accepted meaning unless it appears that the inventors were using them to mean something else. In making this determination, the claims, the remainder of the patent, and the prosecution history are of paramount importance. Additionally, the patent and its prosecution history must be consulted to confirm whether the patentee has acted as its own lexicographer (i.e., provided its own special meaning to any disputed terms), or intentionally disclaimed, disavowed, or surrendered any claim scope.

24. In comparing the claims of the Challenged Patent to the prior art, I have considered the Challenged Patent and its file history in light of the understanding of a person of skill at the time of the alleged invention.

C. ANTICIPATION

25. It is my understanding that the claims of a patent are anticipated by a prior art reference if each and every element of the claim is found either explicitly or inherently in a single prior art reference. I understand that inherency requires a

showing that the missing descriptive matter in the claim is necessarily or implicitly present in the allegedly anticipating reference, and that it would have been so recognized by a POSITA. In addition, I understand that an enabling disclosure is a disclosure that allows a POSITA to make the invention without undue experimentation. Although anticipation typically involves the analysis of a single prior art reference, I understand that additional references may be used to show that the primary reference has enabling disclosure, to explain the meaning of a term used in the primary reference, and/or to show that a characteristic is inherent in the primary reference.

D. OBVIOUSNESS

26. I understand that the prior art may render a patent claim “obvious.” I understand that two or more prior art references (e.g., prior art articles, patents, or publications) that each disclose fewer than all elements of a patent claim may nevertheless be combined to render a patent claim obvious if the combination of the prior art collectively discloses all elements of the claim and one of ordinary skill in the art at the time would have been motivated to combine the prior art in such a way. I understand that this motivation to combine need not be explicit in any of the prior art, but may be inferred from the knowledge of one of ordinary skill in the art at the time the patent was filed. I also understand that one of ordinary skill in the art is not an automaton, but is a person having ordinary creativity. I further understand that

one or more prior art references, articles, patents or publications that disclose fewer than all of the elements of a patent claim may render a patent claim obvious if including the missing element would have been obvious to one of skill in the art (e.g., the missing element represents only an insubstantial difference over the prior art or a reconfiguration of a known system).

27. I understand that under the doctrine of obviousness, a claim may be invalid if the differences between the invention and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a POSITA to which the subject matter pertains.

28. To assess obviousness, I understand that I am to consider the scope and content of the prior art, the differences between the prior art and the claim, the level of ordinary skill in the art, and any secondary considerations to the extent they exist.

29. I understand that any evidence of secondary indicia of non-obviousness should be considered when evaluating whether a claimed invention would have been obvious to one of ordinary skill at the time of invention. These secondary indicia of non-obviousness may include, for example:

- a long felt but unmet need in the prior art that was satisfied by the claimed invention;
- commercial success of processes claimed by the patent;
- unexpected results achieved by the invention;

- praise of the invention by others skilled in the art;
- the taking of licenses under the patent by others; and
- deliberate copying of the invention.

I understand that there must be a nexus between any such secondary indicia and the claimed invention.

30. It is also my understanding that there are additional considerations that may be used as further guidance as to when the above factors will result in a finding that a claim is obvious, including the following:

- the claimed subject matter is simply a combination of prior art elements according to known methods to yield predictable results;
- the claimed subject matter is a simple substitution of one known element for another to obtain predictable results;
- the claimed subject matter uses known techniques to improve similar devices or methods in the same way;
- the claimed subject matter applies a known technique to a known device or method that is ready for improvement to yield predictable results;
- the claimed subject matter would have been “obvious to try” choosing from a finite number of identified, predictable solutions, with a reasonable expectation of success;
- there is known work in one field of endeavor that may prompt variations of it for use in either the same field or a different one based on design incentives or other market forces if the variations would have been predictable to a POSITA;
- there existed at the time of the invention a known problem for which there was an obvious solution encompassed by the patent’s claims; and

- there is some teaching, suggestion, or motivation in the prior art that would have led a POSITA to modify the prior art reference or to combine prior art reference teachings to arrive at the claimed subject matter.

31. Finally, I understand that a claim may be deemed invalid for obviousness in light of a single prior art reference, without the need to combine references, if the elements of the claim that are not found in the reference can be supplied by the knowledge or common sense of one of ordinary skill in the relevant art.

VII. OVERVIEW OF THE '047 PATENT

32. I have reviewed U.S. Patent No. 7,995,047 (“the '047 Patent”), which is entitled “Current Driving Device.” Ex. 1001.

A. PRIORITY DATE FOR CLAIMS OF THE '047 PATENT

33. I understand that the '047 Patent was filed on December 12, 2007, and that it was issued on August 9, 2011. The '047 Patent claims priority to an application filed in Japan on December 13, 2006. I understand that, regardless of whether the priority date of the '047 Patent is December 12, 2007 (corresponding to its U.S. filing date) or December 13, 2006 (corresponding to the filing date of the Japanese application), the references I rely on qualify as prior art.

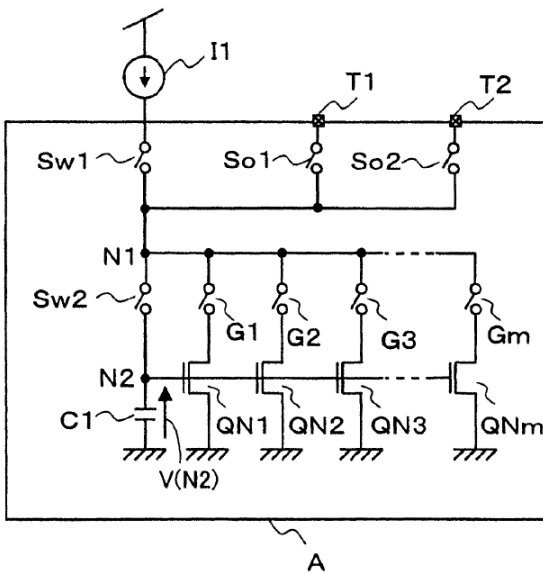
B. THE SUBJECT MATTER OF THE '047 PATENT

34. The '047 Patent is directed to a “current driving device” for use as a “driver for displays such as organic EL (Electro-luminescence) panels, LED panels, and the like.” Ex. 1001 ('047 Patent) 1:5-7.

35. As discussed in the “Background of the Invention” section, the '047 Patent recognizes a known problem in the prior art. For large screen displays with increasing definition, variations in electric currents “due to fabrication processes of each transistor, variations of gate voltages” and the “resistance of power supply wiring” cause non-uniformity in the display image. Ex. 1001 ('047 Patent) 1:17-20. The '047 Patent recognizes that, in order to ensure image uniformity “it is required for display drivers to improve the uniformity in the displayed images qualities through decreasing variations between output electric currents that are outputted from output terminals.” Ex. 1001 ('047 Patent) 1:13-16.

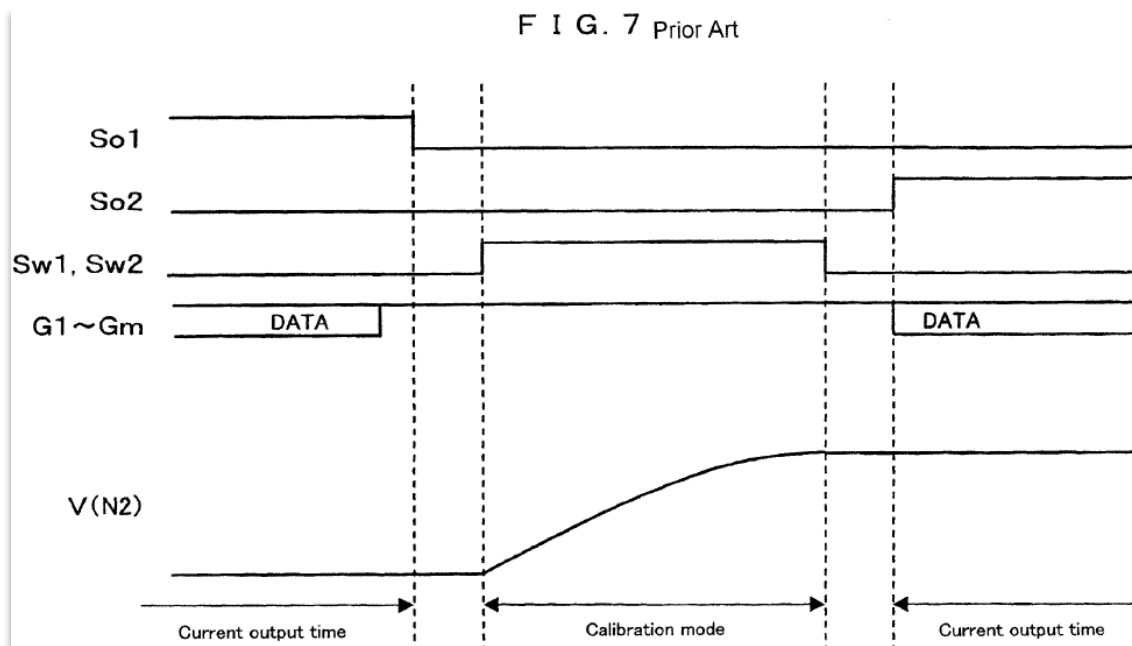
36. The '047 Patent discloses a known solution in the prior art for “decreasing such variations,” which includes the “current output part” as shown below in Figure 6A, further including “a calibration function and a current output function.” Ex. 1001 ('047 Patent) 1:33-39.

FIG. 6A Prior Art



As can be seen in the caption of the figures, Figure 6A is labeled with a caption that recognizes that it is “Prior Art.”

37. As shown in Figure 7, which is also labeled “Prior Art,” the ’047 Patent acknowledges that it was known in the prior art to have two modes of operation for the device shown in Figure 6A: “calibration mode” and “current output mode.”



Ex. 1001 ('047 Patent) at Fig. 7; 2:8-13.

38. During operation of the prior art “calibration mode,” the transistors are operated to allow “the electric current from the reference source I1 to flow through the transistors themselves. A voltage holding capacitance element C1 is charged to the above-described gate voltage.” Ex. 1001 ('047 Patent) 1:40-51. This calibration mode is comprised of a current supply mode. Ex. 1001 ('047 Patent) 1:37-39, *see also* Fig. 6A. As was known in the art, the '047 Patent recognizes that a purpose of charging a capacitor (e.g., voltage holding capacitance element C1) is to store a voltage to enable each QN1-QNm transistor to stay on while passing a desired amount of current such that combinations of currents from QN1-QNm are used to drive a pixel element.

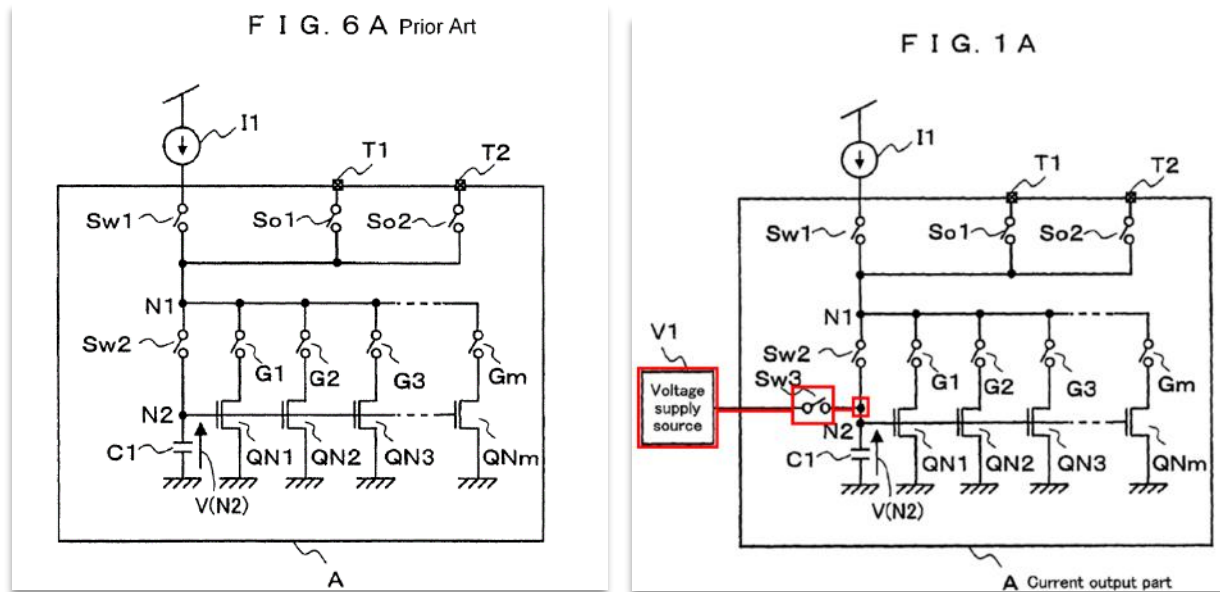
39. During operation of the prior art “current output mode ... [t]he voltage holding capacitance element C1 holds the voltage charged by the calibration ... [and] Nch transistors QN1-QNm output an electric current ... from one (in an [sic] conductive state) of the current output terminals T1 and T2, in accordance with the conduction state of the signal response switches G1-Gm.” Ex. 1001 (’047 Patent) 1:60-2:7, *see also id.* Fig. 6A.

40. Pixel luminance levels are determined by the bit depth or color depth of a particular display. For example, a display with 8 bits of data for blue sub-pixel has 256 potential luminance levels for the blue sub-pixel. Since the amount of light emitted (or luminance) by an organic electroluminescence diode or OLED is directly proportional to the current flowing through the device, there are 256 current values that are necessary to drive a blue sub-pixel.

41. The ’047 Patent describes how these 256 current values may be created using combinations of current output from QN1-QNm transistors that each output a set current. Therefore, the QN1-QNm transistors should be accurately set or calibrated by adequately charging C1 within a set amount of time such that they can output a desired current; otherwise, the color output of pixels will vary and reduce the display color quality. The appropriate charging of C1 to a particular voltage affects current flow through each transistor QN1-QNm, because C1 sets the gate voltage on the transistors which controls the current flow through the transistors.

42. Still in the “Background of the Invention” section, the ’047 Patent describes a known shortcoming with the two modes of operation, in that the ability of a reference current to charge the holding capacitive element “becomes insufficient when the current value of the reference current source I1 is very small.” Ex. 1001 (’047 Patent) 3:1-9, *see also* Fig. 6A. This means that it takes longer to charge the holding capacitor, which limits the speed at which the display screen can be refreshed. Furthermore, an incorrect voltage on the holding capacitor will cause the pixels to produce an incorrect luminance and color, because the current driver will output an inaccurate drive current. Overall, the display quality will be low if luminance and color cannot be reproduced accurately across millions of pixels in a flat panel display.

43. Thus, the ’047 Patent proposes a solution to these known problems, so that “a current driving device ... can perform calibration at a high speed and improve the non-uniformity of the output currents even when a reference current is very small and when there is a change in the reference current.” Ex. 1001 (’047 Patent) at 3:16-21. The ’047 Patent purports to improve upon the prior art (Fig. 6A) by including a voltage supply source, which was already known in the art as a “pre-charge circuit.” Figure 6A (admitted prior art) and Figure 1A of the ’047 Patent are shown side-by-side, with highlighting added to Figure 1A to show the additional components added.

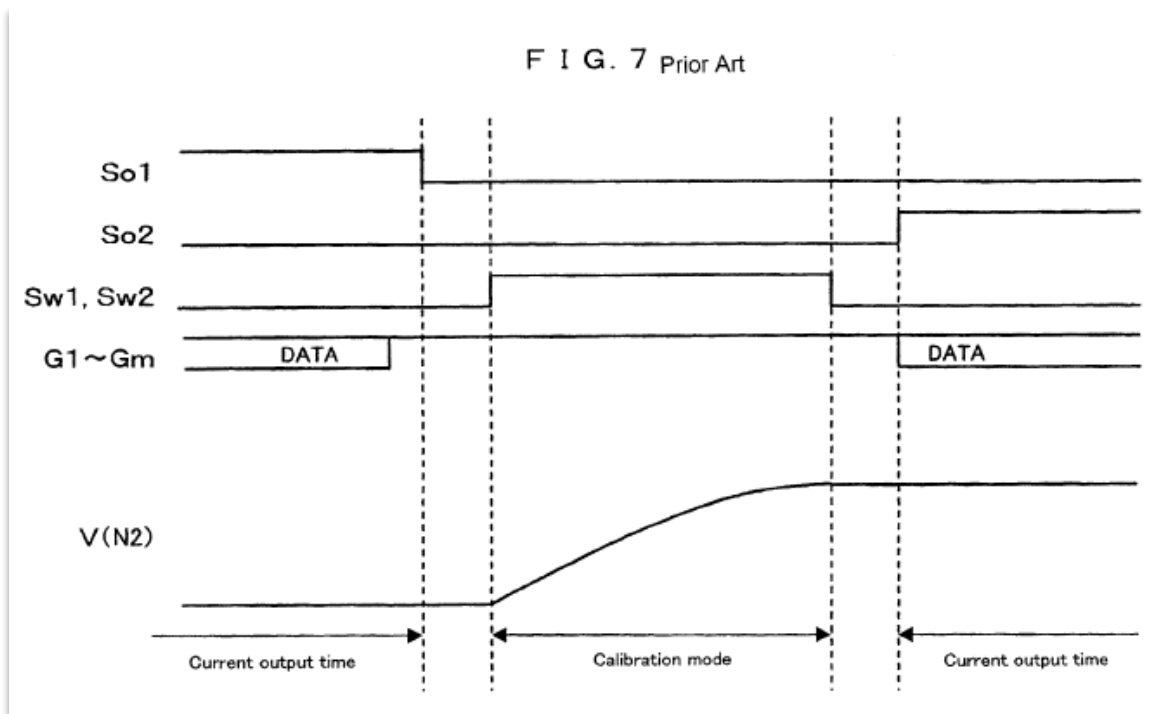


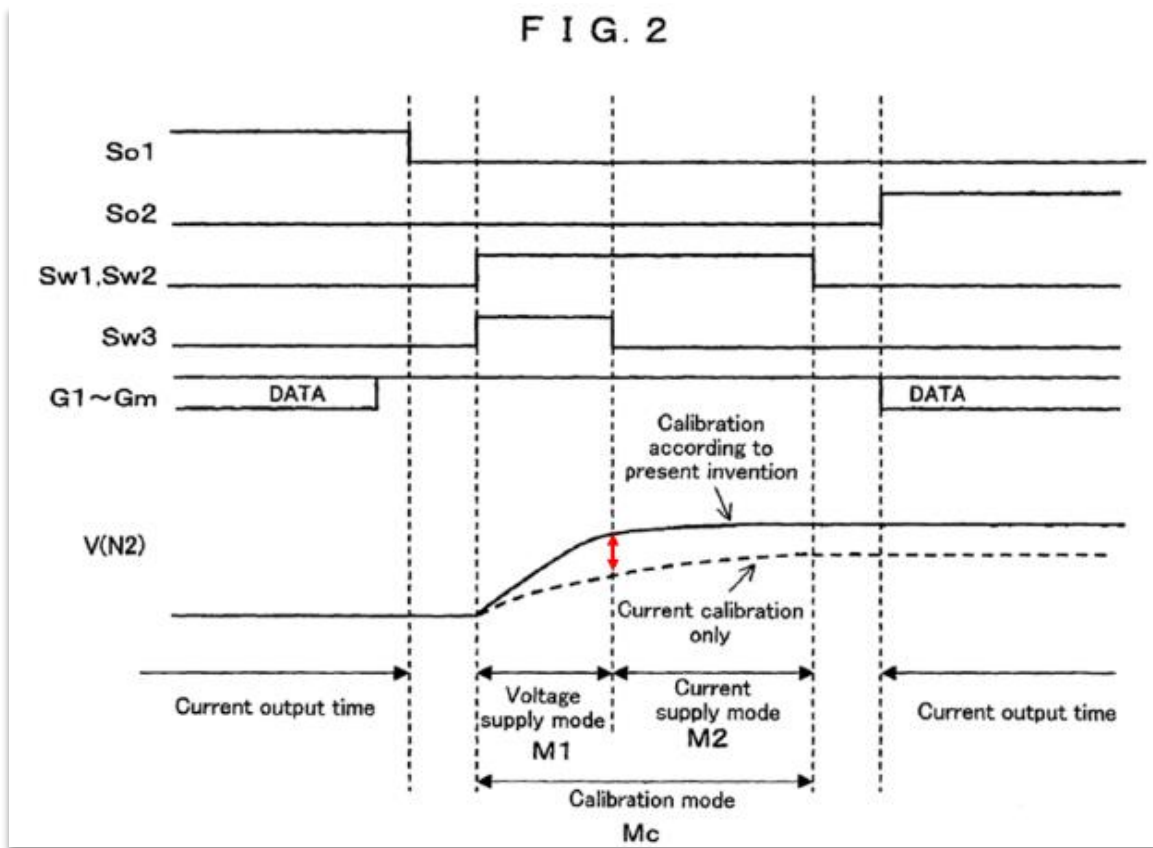
Ex. 1001 ('047 Patent) at Fig. 1, Fig. 6A (annotated). As can be seen, the only addition to the prior art circuit diagram is a voltage supply source (i.e., a pre-charge circuit) and a switch for connecting and disconnecting the voltage-supply source to the circuit ($Sw3$). As described in the substantive grounds, pre-charge circuits were also known in the prior art and were included in circuits to solve the same known problems discussed in the '047 Patent.

44. Along with the voltage supply source, the '047 Patent discloses an additional mode of operation referred to as a “voltage supply mode.” This voltage supply mode occurs prior to a current supply mode, and acts to pre-charge the capacitor ($C1$) to a certain level. Together the voltage supply mode and the current supply mode constitute the new “calibration mode” disclosed in the '047 Patent. Figure 2 of the '047 Patent discloses “three operation modes (the voltage supply

mode M1, the current supply mode M2, and the current output mode M3).” Ex. 1001 (’047 Patent) 9:32-34. This voltage supply mode is a pre-charging mode where a voltage source, as opposed to a current source, is used to charge capacitor C1. Accordingly, the ’047 Patent teaches a current driving device with a pre-charge function that reduces the time needed for charging a capacitor and thus “can perform calibration at a high speed and improve the non-uniformity of the output currents even when a reference current is very small.” Ex 1001 (’047 Patent) 3:19-22.

45. Figure 7 (admitted prior art) and Figure 2 of the ’047 Patent are shown side-by-side, with highlighting added to Figure 2 to show the increased rate at which the capacitor is charged by the voltage supply mode.





Ex. 1001 ('047 Patent) at Fig. 7, 2:8-13. But as I describe in the substantive grounds, charging the capacitor in two phases—voltage supply and current supply—was also known in the prior art.

C. THE CHALLENGED CLAIMS OF THE '047 PATENT

46. Claims 1-4, 9, and 10 of the '047 Patent ("Challenged Claims") are set forth below. I understand that claims 2, 3 and 9 depend from claim 1 and therefore include all of the limitations from claim 1. In the table below, some of the claim elements have been further sub-divided for ease of reference.

Claim Element	Claim Language from '047 Patent
1(pre)	1. A current driving device, comprising:
1(a)	a first voltage supply source for supplying a first voltage;
1(b)	a first current supply source for supplying a first electric current;
1(c)	a plurality of output terminals; and
1(d)(1)	a plurality of current output circuits for outputting an electric current in accordance with said first electric current, each of said current output circuits comprising
1(d)(2)	a current-voltage converting circuit, a voltage-current converting circuit, a voltage holding circuit having a terminal being connected to a reference voltage different from the first voltage, and at least one current output terminal, wherein:
1(e)	each of said current output circuits operates in three operation modes including a voltage supply mode, a current supply mode, and a current output mode,
1(f)	under said voltage supply mode, each of said current output circuits receives said first voltage from said first voltage supply source, and the first voltage is supplied to another terminal of said voltage holding circuit, and
1(g)	under said current supply mode, each of said current output circuits receives said first current from said first current supply source, and generates a second voltage by said current-voltage converting circuit, and the first current is supplied to said another terminal of said voltage holding circuit, and
1(h)	under said current output mode, each of said current output circuits outputs an output current according to said voltage held in said voltage holding circuit by said voltage-current converting circuit.
2	2. The current driving device according to claim 1, wherein: each of said output terminals is connected to said current output terminals provided to

Claim Element	Claim Language from '047 Patent
	said plurality of said current output circuits, and each of said plurality of current output circuits is connected in parallel to said first current supply source and said first voltage supply source used in common
3	3. The current driving device according to claim 1, wherein, in each of said current output circuits, said current-voltage converting circuit is actuated under said voltage supply mode.
4	4. The current driving device according to claim 1, wherein each of said current output circuits is configured to stop said current-voltage converting circuit under said voltage supply mode.
9	9. A current-driving-type display device, comprising said current driving device according to claim 1 mounted thereon so as to be driven by said current driving device.
10(pre)	10. A current driving device, comprising:
10(a)	a current input switch for controlling connection/disconnection states with respect to a current supply source;
10(b)	a voltage holding circuit for holding a reference voltage, which is charged by a flown current, the voltage holding circuit having a first terminal and a second terminal, the first terminal being connected to a fixed voltage;
10(c)	a calibration switch interposed between said current input switch and said voltage holding circuit;
10(d)	a plurality of voltage-current converting elements for generating an electric current in accordance with said reference voltage held in said voltage holding circuit;
10(e)	a plurality of signal response switches that are on/off controlled in accordance with inputted signals, each of said response switches being connected in series to a corresponding one of said voltage-current converting elements, and each of which being connected in parallel to said calibration switch;

Claim Element	Claim Language from '047 Patent
10(f)	a connection node provided between said current input switch and said calibration switch;
10(g)	a plurality of current output switches, each being interposed between the connection node and said plurality of current output terminals; and
10(h)	a high-speed switch for controlling connection/disconnection states of said voltage supply source with respect to the second terminal of said voltage holding circuit.

D. PROSECUTION HISTORY OF THE '047 PATENT

a. Originally Filed Claims on December 12, 2007

47. What ultimately issued as the '047 Patent was filed on December 12, 2007 in the USPTO as Application No. 11/954,659. The application was originally filed with ten claims: independent claim 1, dependent claims 2-9 (depending from claim 1), and independent claim 10. The text of the claims is copied below:

1. A current driving device, comprising:
a first voltage supply part for supplying a first voltage;
a first current supply part for supplying a first electric current;

a plurality of output terminals; and
a plurality of current output parts for outputting an electric current in accordance with said first electric current, each of said current output parts comprising a current-voltage converting function, a voltage-current converting function, a voltage holding part, and at least one current output terminal, wherein

said current output part takes three operation modes, i.e. a voltage supply mode, a current supply mode, and a current output mode,

under said voltage supply mode, said current output part receives said first voltage from said first voltage supply part and holds said voltage in said voltage holding part,

under said current supply mode, said current output part receives said first current from said first current supply part, and generates a second voltage by said current-voltage converting function and holds said voltage in said voltage holding part, and

under said current output mode, said current output part outputs an output current according to said voltage held in said voltage holding part by said voltage-current converting function.

2. The current driving device according to claim 1, wherein each of said output terminals is connected to said current output terminals provided to said plurality of said current output parts, and each of said plurality of current output parts is connected in parallel to said first current supply part and said first voltage supply part used in common.

3. The current driving device according to claim 1, wherein each of said current output parts actuates said current-voltage converting function under said voltage supply mode.

4. The current driving device according to claim 1, wherein each of said current output parts comprises a function of stopping said current-voltage converting function under said voltage supply mode.

5. The current driving device according to claims 1, further comprising

a second current supply part for supplying a second electric current that is proportional to said first electric current, and

a current-voltage converting part for generating said first voltage by receiving said second electric current, wherein

said first voltage supply part controls supplies of said first voltage generated by said current-voltage converting part to said current output parts.

6. The current driving device according to claim 5, wherein said current-voltage converting part comprises a switching part for short-circuiting a node at which said first voltage emerges to a reference voltage node.

7. The current driving device according to claims 1, further comprising a second voltage supply part with a larger voltage supply capacity than that of said first voltage supply part, wherein

the use of said first voltage supply part and the use of said second voltage supply part are switched in accordance with the number of said current output parts that take said voltage supply mode among said plurality of current output parts.

8. The current driving device according to claims 1, wherein

said first voltage supply part is constituted to be capable of changing its voltage supply capacity in accordance with the number of said current output parts that take said voltage supply mode among said plurality of current output parts.

9. A current-driving-type display device, comprising said current driving device according to claims 1 mounted thereon so as to be driven by said current driving device.

10. A current driving device, comprising:
a current input switch for controlling connection/

disconnection states with respect to a current supply part;
a voltage holding part for holding a reference voltage, which is charged by a flown current;

a calibration switch interposed between said current input switch and said voltage holding part;

a plurality of voltage-current converting elements for generating an electric current in accordance with said reference voltage held in said voltage holding part;

a plurality of signal response switches that are on/off controlled in accordance with inputted signals, said response switches being connected in series to each of said voltage-current converting elements, and each of which being connected in parallel to said calibration switch;

a plurality of current output switches, each being interposed between a connection node, which is provided between said current input switch and said calibration switch, and said plurality of current output terminals; and

a high-speeding switch for controlling connection/disconnection states of said voltage supply part with respect to said voltage holding part.

Ex. 1003 ('047 Patent File History, 12/12/2007 Original Claims) at 139-144.

b. USPTO Examiner Issues Office Action on December 8, 2010

48. The USPTO Examiner issued an office action on December 8, 2010. In that Office Action, the Examiner requested that corrected drawings be presented in which “Figures 6A, 6B, and 7-9 should be designated by a legend such as—Prior Art—because only that which is old is illustrated.” Ex. 1003 (’047 Patent File History, 12/8/2010 Office Action) at 49. The Examiner rejected claims 1-10 as anticipated by Date, U.S. Patent No. 7,466,166. The Examiner also rejected claims 1-10 as anticipated by Hashido, U.S. Patent No. 7,221,349.

c. Applicants Respond to Office Action on March 7, 2011

49. On March 7, 2011, the Applicants responded to the Examiner by agreeing that Figs. 6A, 6B, and 7-9 were in the prior art and changing the labels on those figures. Ex. 1003 (’047 Patent File History, 3/7/2011 Resp. to Office Action) at 35. The applicants amended the claims as follows:

1. (Currently Amended) A current driving device, comprising:
a first voltage supply [[part]] source for supplying a first voltage;
a first current supply [[part]] source for supplying a first electric current;
a plurality of output terminals; and
a plurality of current output [[parts]] circuits for outputting an electric current in accordance with said first electric current, each of said current output [[parts]] circuits comprising a current-voltage converting ~~function~~ circuit, a voltage-current converting ~~function~~ circuit, a voltage holding [[part]] circuit having a terminal being connected to a reference voltage different from the first voltage, and at least one current output terminal, wherein:

each of said current output ~~part takes~~ circuits operates in three operation modes [[, i.e.]] including a voltage supply mode, a current supply mode, and a current output mode,
under said voltage supply mode, each of said current output [[part]] circuits receives said first voltage from said first voltage supply [[part]] source, and ~~holds said voltage in the first voltage~~ is supplied to another terminal of said voltage holding [[part]] circuit,

under said current supply mode, each of said current output [[part]] circuits receives said first current from said first current supply [[part]] source, and generates a second voltage by said current-voltage converting ~~function~~ circuit, and ~~holds said voltage in the first current is supplied to~~ said another terminal of said voltage holding [[part]] circuit, and

under said current output mode, each of said current output [[part]] circuits outputs an output current according to said voltage held in said voltage holding [[part]] circuit by said voltage-current converting ~~function~~ circuit.

2. (Currently Amended) The current driving device according to claim 1, wherein:
each of said output terminals is connected to said current output terminals provided to said plurality of said current output [[parts]] circuits, and
each of said plurality of current output [[parts]] circuits is connected in parallel to said first current supply [[part]] source and said first voltage supply [[part]] source used in common.

3. (Currently Amended) The current driving device according to claim 1, wherein, in each of said current output [[parts]] circuits, ~~actuates~~ said current-voltage converting ~~function circuit~~ circuit is actuated under said voltage supply mode.

4. (Currently Amended) The current driving device according to claim 1, wherein each of said current output [[parts]] circuits is configured to stop ~~comprises a function of stopping~~ said current-voltage converting ~~function circuit~~ under said voltage supply mode.

5. (Currently Amended) The current driving device according to [[claims]] claim 1, further comprising:

a second current supply [[part]] source for supplying a second electric current that is proportional to said first electric current; [[.]] and

a second current-voltage converting [[part]] circuit for generating said first voltage by receiving said second electric current, wherein

said first voltage supply [[part]] source controls supplies of said first voltage generated by said second current-voltage converting [[part]] circuit to said current output [[parts]] circuits.

6. (Currently Amended) The current driving device according to claim 5, wherein said second current-voltage converting [[part]] circuit comprises a switching part for short-circuiting a node at which said first voltage emerges to a reference voltage node.

7. (Currently Amended) The current driving device according to [[claims]] claim 1, further comprising a second voltage supply [[part]] source with a larger voltage supply capacity than that of said first voltage supply [[part]] source, wherein

the use of said first voltage supply [[part]] source and the use of said second voltage supply [[part]] source are switched in accordance with the number of said current output [[parts]] circuits that [[take]] operate in said voltage supply mode among said plurality of current output [[parts]] circuits.

8. (Currently Amended) The current driving device according to [[claims]] claim 1, wherein said first voltage supply [[part]] source is configured to change ~~constituted to be capable of changing~~ its voltage supply capacity in accordance with the number of said current output [[parts]] circuits that [[take]] operate in said voltage supply mode among said plurality of current output [[parts]] circuits.

9. (Currently Amended) A current-driving-type display device, comprising said current driving device according to [[claims]] claim 1 mounted thereon so as to be driven by said current driving device.

10. (Currently Amended) A current driving device, comprising:
a current input switch for controlling connection/disconnection states with respect to a current supply [[part]] source;
a voltage holding [[part]] circuit for holding a reference voltage, which is charged by a flown current, the voltage holding circuit having a first terminal and a second terminal, the first terminal being connected to a fixed voltage;

a calibration switch interposed between said current input switch and said voltage holding ~~[[part]]~~ circuit;

a plurality of voltage-current converting elements for generating an electric current in accordance with said reference voltage held in said voltage holding ~~[[part]]~~ circuit;

a plurality of signal response switches that are on/off controlled in accordance with inputted signals, each of said response switches being connected in series to a corresponding one ~~[[each]]~~ of said voltage-current converting elements, and each of which being connected in parallel to said calibration switch;

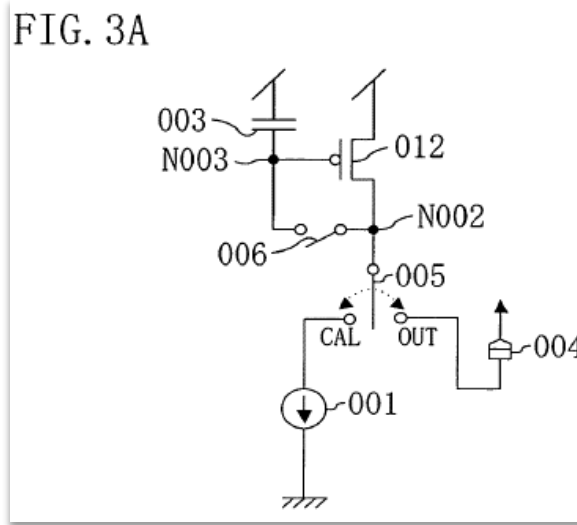
a connection node provided between said current input switch and said calibration switch;

a plurality of current output switches, each being interposed between ~~[[a]]~~ the connection node, ~~which is provided between said current input switch and said calibration switch~~, and said plurality of current output terminals; and

~~a high-speeding~~ high-speed switch for controlling connection/disconnection states of said voltage supply ~~[[part]]~~ source with respect to the second terminal of said voltage holding ~~[[part]]~~ circuit.

Ex. 1003 ('047 Patent File History, 3/7/2011 Resp. to Office Action) at 31-34. The Applicants also argued that the amended claims were different than what was disclosed in the prior art.

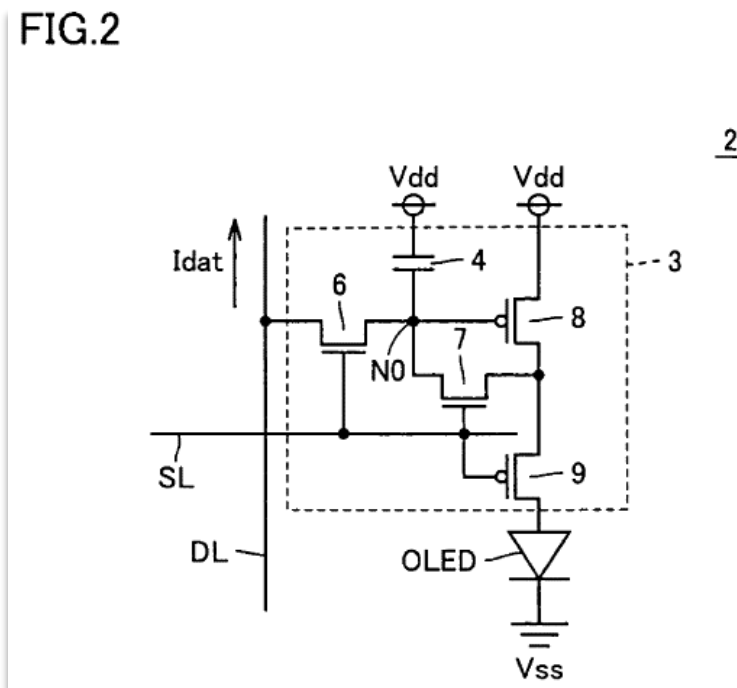
50. Regarding the Date reference, Applicants distinguished the claims from Figure 3A of Date, copied below:

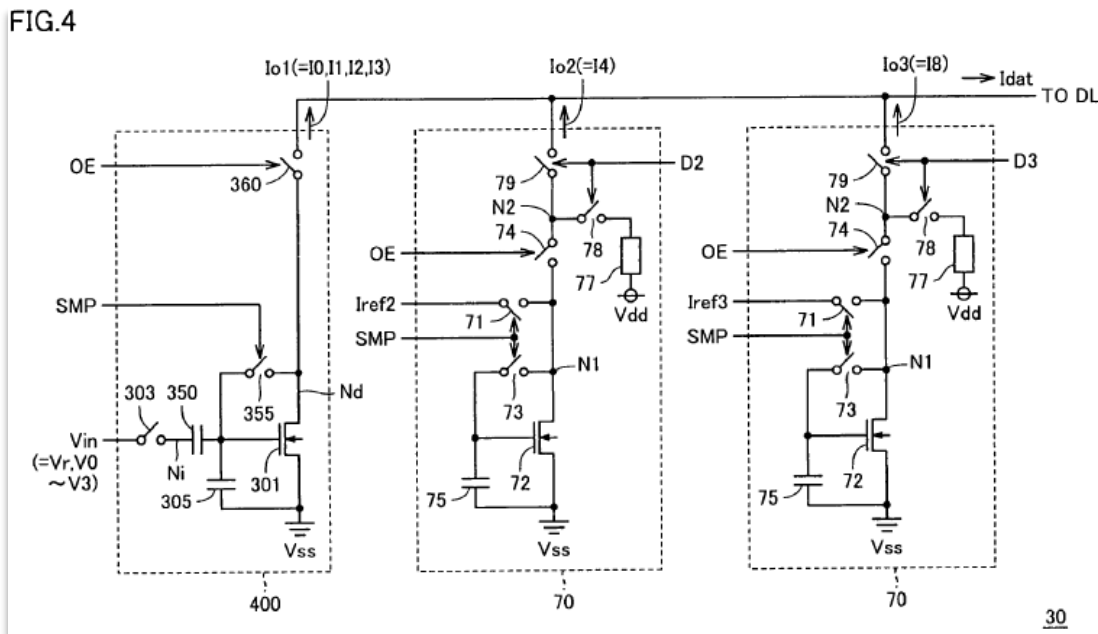


U.S. Patent No. 7,466,166 (Date) at Fig. 3. Applicants argued regarding Claim 1 that Date “fails to disclose that a voltage holding circuit has a terminal being connected to a reference voltage different from the first voltage, and under the voltage supply mode, the first voltage is supplied to another terminal of the voltage holding circuit.” In explaining Figure 3A of Date, Applicants argued that “the Examiner asserts that FIG. 3A of Date discloses the claimed first voltage supply part (source). It appears that the Examiner considers Vcc connected to capacitor 0003 as the claimed voltage holding part (circuit). However, it is clear that FIG. 3A fails to disclose that a voltage holding circuit (0003) has a terminal being connected to a reference voltage different from the first voltage (Vcc).” Regarding claim 10, Applicants argued “Date fails to disclose that the voltage holding circuit has a first terminal and a second terminal, the first terminal being connected to a fixed voltage, and the current driving device includes a high-speed switch for controlling

connection/disconnection states of **said voltage supply source with respect to the second terminal of said voltage holding circuit.**” Ex. 1003 ('047 Patent File History, 3/7/2011 Resp. to Office Action) at 37 (emphasis in original).

51. The Applicants distinguished the claims from Figure 2 and Figure 4 of Hashido, which are copied below:





U.S. Patent No. 7,221,349 (Hashido) at Figs. 2, 4. Applicants argued regarding claim 1 that “Hashido fails to disclose that a voltage holding circuit has a terminal being connected to a reference voltage different from the first voltage, and under the voltage supply mode, the first voltage is supplied to another terminal of the voltage holding circuit.” Applicants argued that capacitor 4 of Figure 2 does not correspond to the claimed voltage holding circuit, because Figure 2 fails to disclose that capacitor 4 “has a terminal being connected to a reference voltage has a terminal being connected to a reference voltage different from the first voltage (V_{DD}).” Regarding Figure 10, Applicants argued that Hashido fails to disclose that “the voltage holding circuit has a first terminal and a second terminal, the first terminal being connected to a fixed voltage, and the current driving device includes a high-

speed switch for controlling connection/disconnection states of **said voltage supply source with respect to the second terminal of said voltage holding circuit.**” Ex. 1003 (’047 Patent File History, 3/7/2011 Resp. to Office Action) at 38 (emphasis in original).

d. Notice of Allowance on May 31, 2011

52. On May 31, 2011 the USPTO issued a notice of allowance. The Examiner explained the reasons for allowance as follows:

1. Claims 1-10 are allowed.
2. The following is an examiner’s statement of reasons for allowance:

As argued by the Applicants in the Remarks, dated **March 7, 2011**, the cited references have failed to teach **“disclose that a voltage holding circuit has a terminal being connected to a reference voltage different from the first voltage, and under the voltage supply mode, the first voltage is supplied to another terminal of the voltage holding circuit”** in combination with other limitations of claim 1, and **“the voltage holding circuit has a first terminal and a second terminal, the first terminal being connected to a fixed voltage, and the current driving device includes a high-speed switch for controlling connection/disconnection states of said voltage supply source with respect to the second terminal of said voltage holding circuit”** in combination with other limitations of claim 10.

Ex. 1003 (’047 Patent File History, 5/31/2011 Notice of Allowance) at 13.

**VIII. LEVEL OF ORDINARY SKILL IN THE ART FOR THE '047
PATENT**

53. In the 2006-2007 timeframe, at the time the Challenged Patent was filed, I believe that a relevant person of ordinary skill in the art would have had an undergraduate degree in electrical engineering (or equivalent subject) together with two or three years of experience in designing circuits for driving light-emitting devices including organic light-emitting diodes, or a Ph.D. with experience in the same. This description is approximate, and a higher level of education or skill might make up for less experience, and vice-versa.

54. I believe that I would qualify as at least a person of ordinary skill in the art in the 2006-2007 timeframe, and that I have a sufficient level of knowledge, experience, and education to provide an opinion in the field of the Challenged Patent. I am familiar with what a person of ordinary skill in the art knew at that time because of my lengthy experience with engineering subjects of a similar nature to the concepts presented in the Challenged Patent. Additionally, at that time, I was familiar with the general subject material in the cited prior art in this Declaration.

IX. CLAIM CONSTRUCTION

55. In my opinion, and for the purposes of this declaration, I apply the ordinary and customary meaning of the claim terms of the Challenged Patent.

X. TECHNOLOGY BACKGROUND AND STATE OF THE ART FOR THE '047 PATENT

56. In the subsections below, I describe some of the basic principles of electrical engineering that would have been well-known to a POSITA in 2006-2007 timeframe, and long before.

A. EXEMPLARY REFERENCES CORROBORATING THE GENERAL ENGINEERING KNOWLEDGE

a. Camara Handbook (Ex. 1007)

57. As an example of general electrical engineering knowledge, Exhibit 1007 is the handbook published by in 2002, entitled “Electrical Engineering Reference Manual,” by John Camara (“**Camara**”). As implied by the title, this was a basic engineering reference manual that engineers used since 2002 to study for their Professional Engineer (PE) examinations. The cover of Camara states: “The most comprehensive resource available for the electrical PE exam.” Ex. 1007 (Camara). This handbook covers topics on the electrical and computer engineering professional engineering exam (including electric and electronic circuits), and it summarizes the level of knowledge one with a bachelor’s degree in electrical engineer would have possessed.

b. den Boer Text (Ex. 1008)

58. As an example of engineering knowledge pertaining to flat-panel displays, Exhibit 1008 is a textbook published in 2005, entitled “Active Matrix

Liquid Crystal Displays: Fundamentals and Applications,” by Willem den Boer (“**den Boer**”). This book memorializes the state of the art of flat-panel displays as of 2005, including liquid crystal displays and organic electroluminescence displays, and provides a perspective of the knowledge of one of ordinary skill. In this book, thin-film-transistors, drive electronics, and drive methods, including compensation methods used for high-speed performance, are discussed in terms of their development, solutions to problems associated with increases in display size, and the rapid developments in these technologies.

c. Han Article (Ex. 1009)

59. As an example of specific pixel circuit design general engineering knowledge pertaining to flat-panel display, Exhibit 1009 is a paper published by the Asian Society for Information Display (“ASID”) in 2006, entitled “AM backplane for AMOLED,” by Min-Koo Han et al. (“**Han**”). I am familiar with the Journal of the Society of Information Display (as discussed below in the context of Shimoda), and ASID is the Asian branch of the SID.

B. GENERAL DISPLAY BACKGROUND

60. It was known that the basic function of a display is to visually present information to a user. There are many flat panel display technologies, including liquid crystal displays (LCDs) and organic light-emitting diode (OLED) displays. To enable those displays, particularly active-matrix display technologies, switches

in the form of electronic transistors were well known, including a subcategory of transistors called thin-film transistors (TFT). Ex. 1008 (den Boer) p. 29-39 (§2.3-§2.6). It was known that an active-matrix display includes arrays of TFTs that worked with pixels, source (data) lines, and gate drivers. Ex. 1008 (den Boer) at 39-43 (§2.7). As an example, it was known that an HDTV could have “1080x1920 pixels.” Ex. 1008 (den Boer) at 176 (§6.6). It was further known that individual pixels would be comprised of three sub-pixels (e.g., red-green-blue). Ex. 1008 (den Boer) p. 3, 41, 144. Therefore, in such a known device, there would be 6,220,800 pixels ($1920 \times 1080 \times 3$) that are actively controlled to create an image.

61. It was also known to drive the pixels using a “TFT pixel array circuit (Fig. 2.17) [with] select buslines, data buslines, a TFT at each pixel, and a storage capacitor ... at each pixel.” Ex. 1018 (den Boer) at 39-40. The storage capacitor “acts as a buffer,” helping control gray level of pixels. Ex. 1018 (den Boer) at 27, 39. It was known that panels also include source drivers that use red-green-blue data to drive the columns of lines running vertically in the displays and provide the value of brightness required of each pixel. The gate or row drivers select the rows of lines running horizontally within the displays, and they turn on the switches within pixels of each row in a row-by-row succession. Ex. 1008 (den Boer) p. 93-98 (§4.2).

62. It was known that OLEDs are semiconducting devices comprised of organic materials that convert electrical energy to light, much like LEDs. In OLED

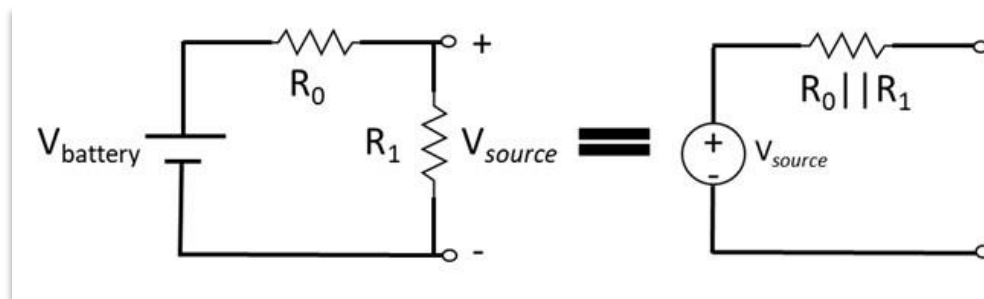
displays, the individual pixels comprise OLEDs that are current-driven devices, which means that a given OLED's brightness is set by a fixed current. Ex. 1009 (Han) p. 53 §1. It was known that a pixel's color and brightness are electronically adjusted by setting the current and therefore brightness of each pixel through the manipulation of TFT(s).

63. It was known that if any pixels had non-uniform characteristics, that could lead to dark dots, bright dots, and other undesirable characteristics in the display. However, it was known that flat-panel displays are made with motherglass, in which microelectronics circuits (including the TFTs) are fabricated across several square meters of surface, and variations in electronic characteristics or properties are inevitable. Ex. 1009 (Han) p. 53 (Introduction). Because of known variations in the electronic characteristics across the motherglass and variations in the characteristics of TFTs, it was known to use compensation and calibration to adjust for the variations. Ex. 1009 (Han) p. 53 at Abstract ("A number of TFT active matrix pixel circuits have been developed in order to compensate for TFT parameter variations"), Introduction ("Poly-Si TFT pixel circuit should compensate the non-uniform characteristics of the current, which originate from the inherent process variation of the crystal growth in polycrystalline film.").

C. BASIC CIRCUITS FOR DRIVING DISPLAYS

a. Voltage supply source / Voltage supply mode

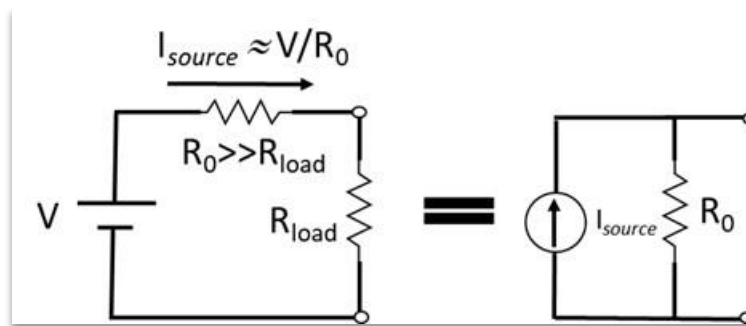
64. It was known that an ideal independent voltage source is modeled as a two-terminal device that has a fixed voltage across its terminals, regardless of the current through it or the load that it is driving. In a generic real-world application, voltage sources can be modeled as an ideal voltage source with internal resistance. Circuitry was well-known to provide voltage sources at various voltage levels to drive components (e.g., capacitors) within systems including drive electronics for flat panel displays. *See, e.g.,* Ex. 1007 (Camara) p. 26-4. A simple voltage source includes, for example, a battery with low internal resistance R_0 having an output voltage V_0 across R_1 that can be used to drive downstream circuits.



There are alternative means to create voltage sources using transistors, transformers, buffers, and repeaters, for example, and a POSITA would have the requisite experience to use and understand their role in circuitry.

b. Current supply source / Current supply mode

65. It was known that an ideal independent current source is modeled as a two-terminal device that delivers a fixed current flow through its terminals, regardless of the voltage across its terminals and the load that it drives. *See, e.g.,* Ex. 1007 (Camara) p. 26-4, 26-5. A simple current source includes, for example, a voltage source in series with a high resistance (R_0) that is much higher than the load resistance (R_{load}) such that the current (I_{source}) is essentially constant, as depicted below.

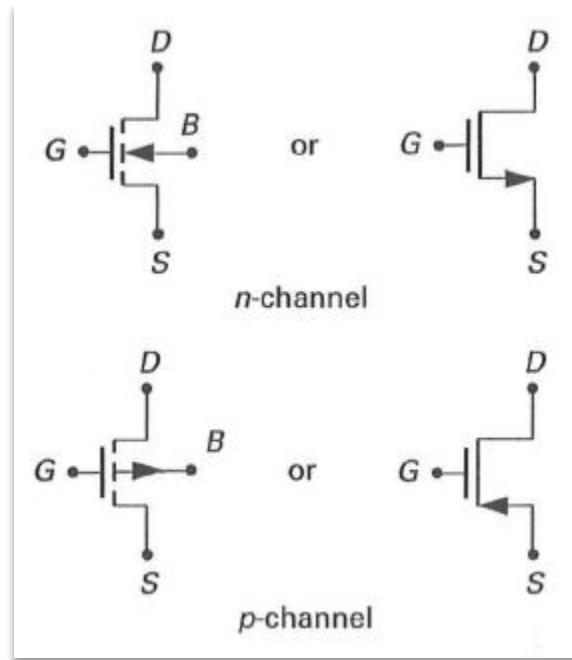


There are alternative means to create microelectronic current sources using transistors, diodes, and opamps (operational amplifiers), for example, and a POSITA would have the requisite experience to use and understand their role in circuitry.

c. Voltage-current converting circuit

66. It was known that the conversion of a voltage signal to a current signal can be accomplished with microelectronic devices that take a voltage input and produce a corresponding output current based on some transconductance of the

electronic device. A MOSFET was one known type of electronic device that can be configured to take an input voltage (V_G) on its gate terminal to produce an output current flowing between its drain and source terminals (I_D). *See, e.g.,* Ex. 1007 (Camara) p. 43-31. An example is shown below.



Ex. 1007 (Camara) p. 43-32 (Fig. 43.37(d)). It was known that other types of semiconductor devices can perform the same function, for example, a bipolar junction transistor. A POSITA would have the requisite experience to use and understand a MOSFET, which is a basic electronic device.

d. Capacitors

67. It was known that a capacitor is an electronic component that has the ability to store charge. Ex. 1007 (Camara) p. 27-9. It was also known to use

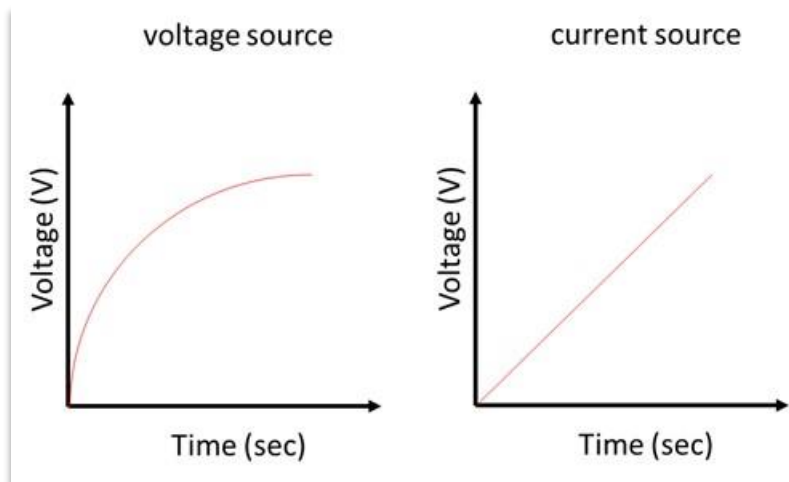
capacitors in pixel circuits, for example, as a buffer. Ex. 1018 (den Boer) at 27, 39.

When a capacitor is being charged, the time it takes for a capacitor to increase its stored charge depends on its resistance and capacitance. It was known that RC (resistance multiplied by capacitance) represents the time delay. Ex. 1007 (Camara) p. 30-2. A fundamental and well-known equation governs how a capacitor is charged and discharged,

$$I = C \frac{dV}{dt}$$

where the current (I) through a capacitor is equal to its capacitance (C) multiplied by the rate of change of the voltage across the capacitor $\frac{dV}{dt}$. Ex. 1007 (Camara) p. 29-4.

68. It was known that the voltage rise on a capacitor increases exponentially when the capacitor is driven by a voltage source; however, it was also known that a linear voltage rise is expected on a capacitor with a current source, as shown below. Ex. 1007 (Camara) p. 30-6, 30-7. Thus, voltage sources were known to charge the capacitor faster than current sources. A representative figure showing the charging of a capacitor with a voltage source and current source, respectively, is shown below.

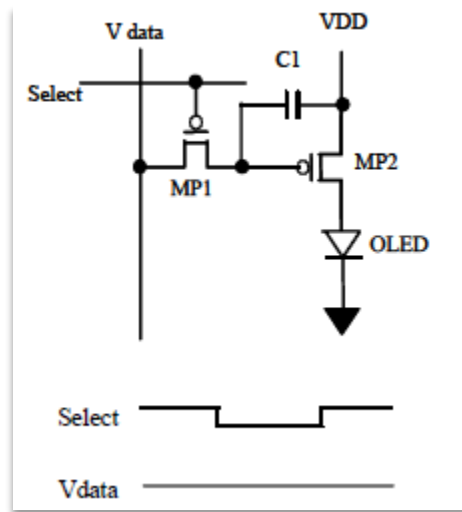


It was known that a small current may not be sufficient to charge a capacitor within a given amount of time (e.g., frame time), as compared to charging the same capacitor with a voltage source.

69. The use of a voltage source to charge the storage capacitor is one aspect of the purported invention of the '047 Patent. Ex. 1001 ('047 Patent) at 3:25. As described above, a POSITA would have been aware that different amounts of time are required to charge capacitors based on whether a current source (current programming) or a voltage source (voltage programming) is applied. A POSITA would have also known that a voltage source can be used to more quickly charge a storage capacitor based on the characteristics of a capacitor.

e. Voltage and Current Programming

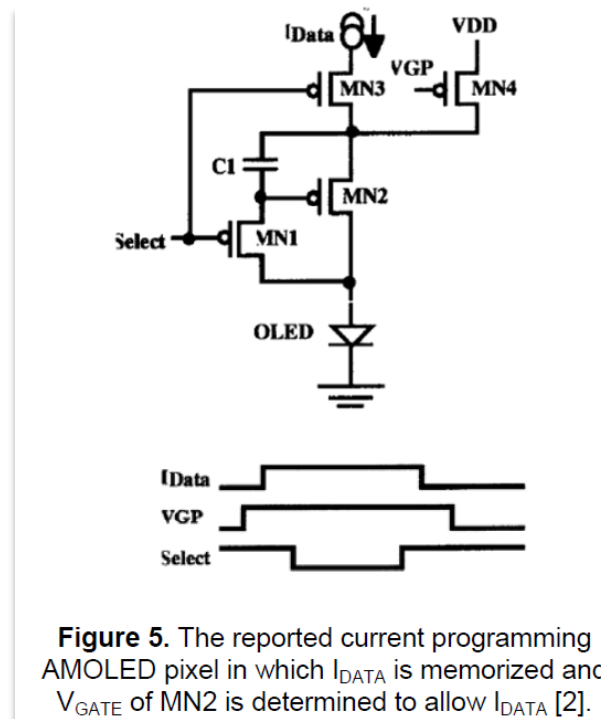
70. It was known that conventional OLED drivers relied on 2 TFTs as shown below.



Ex. 1009 (Han) at Fig. 1(a). In this configuration transistor MP2 drives the current for the OLED, and transistor MP1 is a switch that samples and holds the voltage on the storage capacitor C1. It was known that variations in TFT threshold voltage and series resistances change the current output to the OLED and therefore change the display brightness. For example, Figure 1(b) of Han reports “brightness non-uniformity (17%) of the conventional 2-TFT pixel.” Ex. 1009 (Han) p. 54. To compensate for this non-uniformity, current programming schemes have been developed.

71. It was known that in order to compensate for variation in TFT threshold voltage and mobility, current programming was used for driving OLEDs. Ex. 1009 (Han) p. 53 (“The current programming pixel circuits can compensate mobility variation as well as threshold voltage variation”). It was known that using current-programming, a current (as opposed to a voltage) is supplied to the pixel to charge a

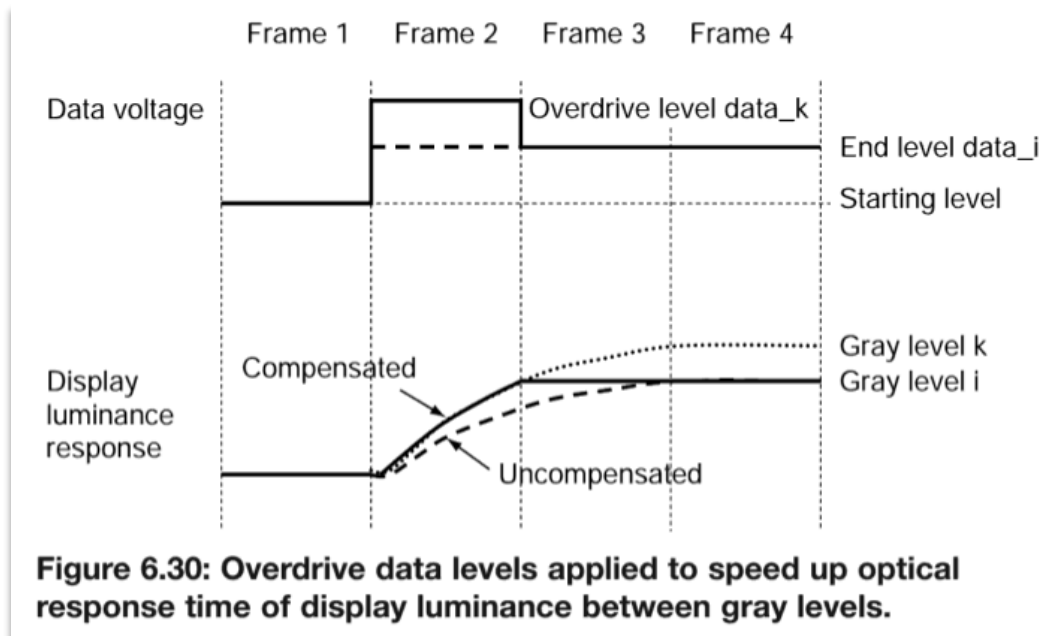
storage capacitor. A basic current-programming circuit (Fig. 5 of the Han) is shown below. In this circuit, the current I_{Data} charges capacitor C1 of the driving TFT until transistor MN2 can turn on. By using a current source I_{Data} to program the pixel, the current charging capacitor C1 remains constant even if there are variations in TFT threshold voltage or mobility.



Ex. 1009 (Han) at Fig. 5.

72. One known problem with current programming was that the rate at which a storage capacitor is charged can limit the speed of the display. For example, capacitance within flat panel display pixels provided a slowed response times for charging, and overvoltage compensation schemes were implemented to counter the

slow response time. In the example shown in Figure 6.30, uncompensated pixels with high capacitance were unable to attain the brightness level required within a frame of the image; hence, extra drive voltage was applied to enable a compensated response to attain the appropriate brightness level within the given amount of time.



Ex. 1008 (den Boer) p. 168 (Fig. 6.30).

73. The '047 Patent discloses that the ability of a small reference current to charge a holding capacitive element becomes insufficient when the current value of the reference current source is very small; hence, a voltage supply (pre-charge) is used to enable faster charging of the holding capacitor. The voltage supply is very similar to the compensation technique described in the den Boer §6.5.1.

With this method, however, the capacity for charging/discharging the voltage holding capacitance element C1 becomes insufficient when the

current value of the reference current source I1 is very small, so that it is difficult to charge the current of the Nch transistors QN1-QNm to accurately meet the value of the current from the reference current source I1 within the calibration period. FIG. 9 shows the state where the voltage holding capacitance element C1 is insufficiently charged because the reference current is very small.

Ex. 1001 ('047 Patent) at 3:1-9.

74. A POSITA, when faced with the issue of delays in capacitor charging, would have known that the use of a voltage source would allow for a quicker charge time. Furthermore, as described above, the topics of voltage supply sources, current supply sources, capacitor charging, voltage-current converting circuit, and current programming were all well-known to a POSITA.

XI. OVERVIEW OF THE PRIOR ART TO THE '047 PATENT

A. SHIMODA (EX. 1004)

a. Status of Shimoda as Prior Art

75. “Shimoda” refers to a publication by M. Shimoda and others entitled, “An integrated poly-Si TFT current data driver with a data-line pre-charge function.” Shimoda was published on pages 461-466 in volume 11 issue 3 of the Journal of the Society for Information Display (SID).

76. I am familiar with the Journal of the Society of Information Display (“SID”), in part because I have attended SID conferences and authored two articles

in the field of OLED displays that were published in the Journal of the SID. These include:

- B. Hekmatshoar, A. Kattamis et al., “A Novel TFT-OLED integration for OLED-independent pixel programming in amorphous-Si AMOLED pixels,” *Journal of the Society for Information Display* **16/1** (2008): 183-188 (Ex. 1010).
- A. Kattamis et al., “Active-matrix organic light-emitting displays employing two thin-film-transistor a-Si:H pixels on flexible stainless-steel foil,” *Journal of the Society for Information Display* **15/7** (2007): 433-437 (Ex. 1011).

The SID is perhaps the most well-known society in the field of electronic displays. As of June 16, 2004, the SID had “6000 members.”¹ Their conferences are generally attended by both people both from academia and from industry. The Journal of the SID would publish versions of such conference papers. For example, Shimoda states that it is a “Revised version of a paper presented at the 9th International Display Workshops (IDW '02) held December 4-6, 2002, in Hiroshima, Japan.” The Journal of the SID published the types of papers that a POSITA would have reviewed.

77. I understand from the declaration of Dr. James Mullins (Ex. 1019) that Shimoda was publicly accessible by 2004, if not sooner. This is well over one year

¹ Ex. 1012 (About the SID, dated June 16, 2004), available at:
<https://web.archive.org/web/20040616180753/http://www.sid.org/about/about.html>

before the earliest possible priority date of the '047 Patent. Accordingly, I understand that Shimoda qualifies as prior art to the '047 Patent.

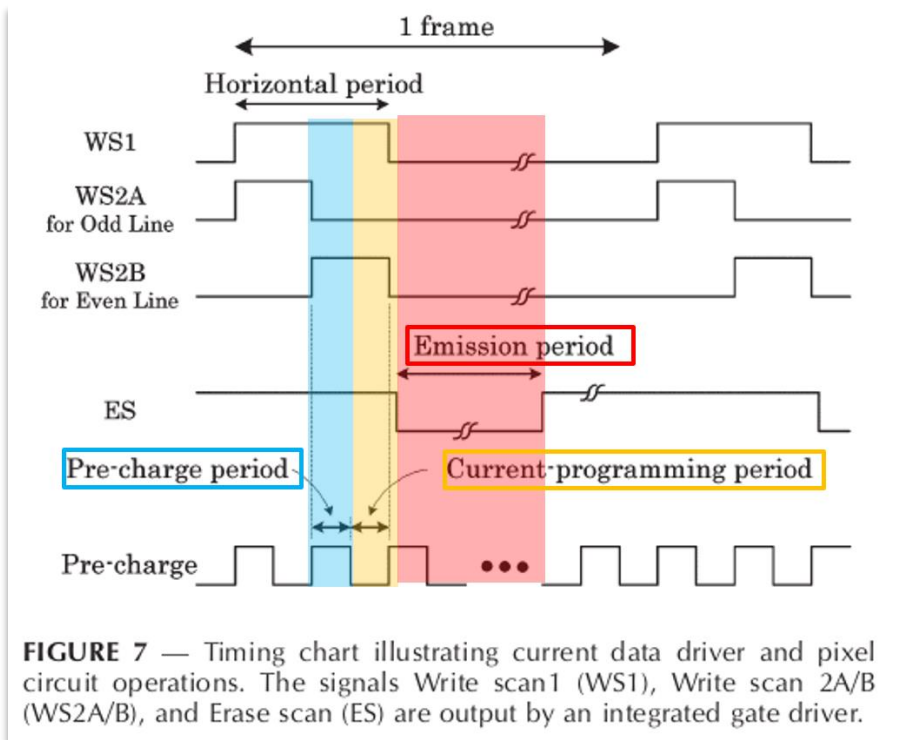
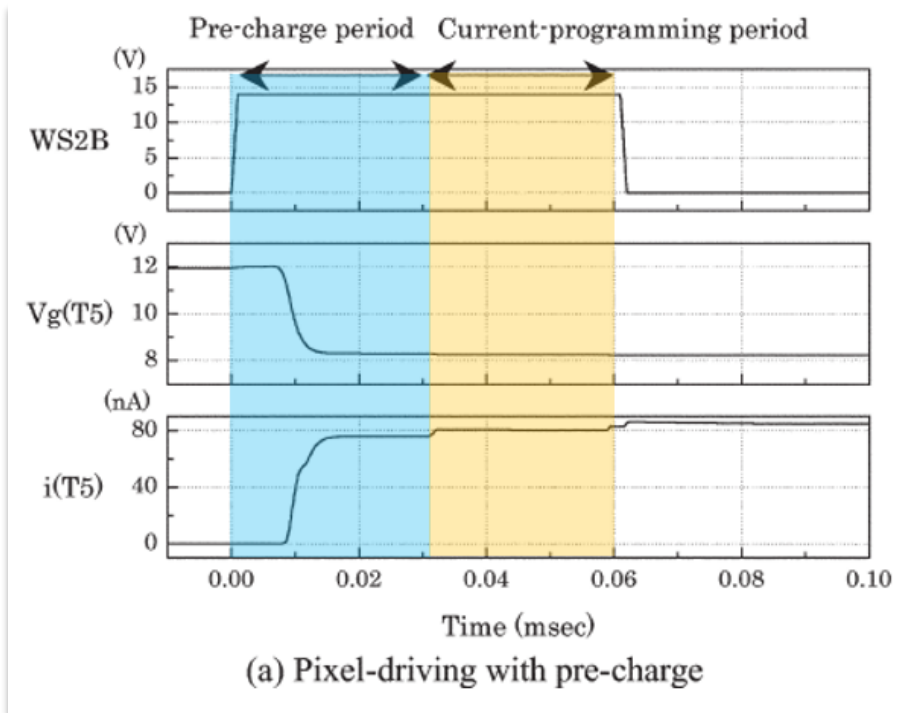
b. Overview of the Disclosure of Shimoda

78. Shimoda recognizes the same problem and offers a similar solution as the '047 Patent. Shimoda provides a solution to achieving “uniformity in the brightness of each pixel” of an organic LED (OLED) display. Ex. 1004 (Shimoda) §1. Shimoda recognizes that each pixel in an LED display is driven by a pixel circuit, and that the “brightness [of the pixel] is dependent on the current in the OLED that is driven by each pixel circuit.” Ex. 1004 (Shimoda) §1. Shimoda recognizes a known problem in the prior art that “non-uniformity in the current-voltage characteristics of the poly-Si TFTs [poly-silicon thin film transistors] that form part of the pixel circuit” leads to non-uniform current delivered the pixels. Ex. 1004 (Shimoda) §1.

79. Shimoda recognizes that a known prior-art solution to achieving uniform currents (and thus uniform brightness) was “a current-programming approach, which works to compensate for variations in both V_t [threshold voltage] and mobility in poly-Si TFTs, [is] effective in achieving good uniformity.” Ex. 1004 (Shimoda) §1. However, Shimoda recognizes that a conventional current driver suffers from serious drawbacks: “the lowness of its current for a dark gray scale means that (1) programming time will be relatively long and (2) a highly accurate

current data driver will be required.” Ex. 1004 (Shimoda) §1. To the extent an external driver is supplied, Shimoda asserts that “such drivers would increase programming time further because of the increase in high parasitic capacitance.” Ex. 1004 (Shimoda) §1. Thus, Shimoda seeks “to integrate high-accuracy current data drivers into the AMOLED display substrate itself.” Ex. 1004 (Shimoda) §1.

80. To solve this problem of non-uniform brightness, Shimoda teaches to increase the speed by which a capacitor can be charged with voltage during programming periods. Similar to the '047 Patent, Shimoda teaches adding to the current driving device a pre-charge circuit, which “pre-charges” the capacitor before the current-programming period. During a pre-charge period, the pre-charge circuit supplies a voltage to a pixel circuit, “rapidly pre-charg[ing] the voltage in the gate electrode of T5 so that a current roughly equivalent to the value of the current source flows through T5.” Ex. 1004 (Shimoda) §3.2. After the pre-charge period (annotated blue), a current-programming period (annotated yellow) compensates for any errors generated during the pre-charge period.



Ex. 1004, Figs. 7 and 8a (annotated).

81. Accordingly, Shimoda teaches a driving device with a pre-charge function that reduces the time needed for charging a capacitor and thus “helps achieve accurate current programming at low brightness,” solving the known problem identified in the ’047 Patent and offering a similar solution. Ex. 1004 (Shimoda) at Abstract.

B. BAEK (EX. 1005)

a. Status of Baek as Prior Art

82. “Baek” refers to United States Patent Application Publication No. 2006/0170629, entitled “Display Driver Circuit, Current Sample/Hold Circuit and Display Driving Method Using the Display Driver Circuit.” Baek names Jong-Hak Baek as the sole inventor and was assigned to Samsung Electronics Co., Ltd. Baek was filed in the United States on January 27, 2006 and published on August 3, 2006. Thus, Baek published more than one year before the earliest possible priority date of the ’047 Patent. Accordingly, I understand that Baek qualifies as prior art to the ’047 Patent.

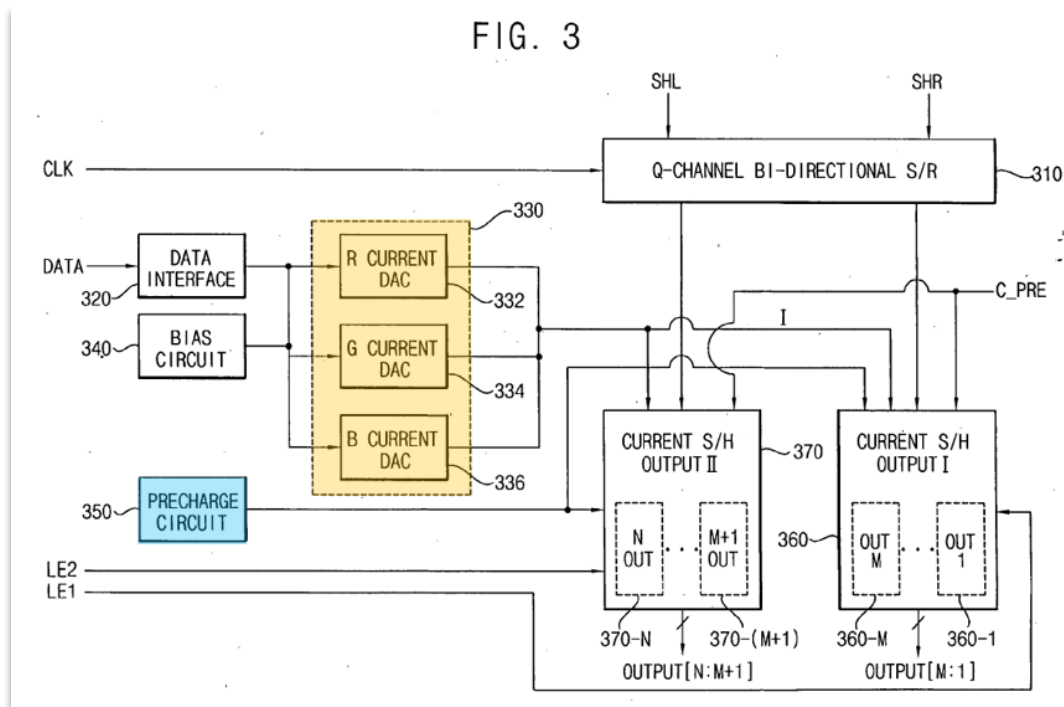
b. Overview of the Disclosure of Baek

83. The field of the invention in Baek includes “a display driver circuit for a flat display panel and a display driving method.” Ex. 1005 (Baek) ¶[0003]. The applications for the display driver circuit include liquid displays (LCD), plasma display panels (PDP), and organic light emitting diode (OLED) display. Ex. 1005

(Baek) ¶¶[0005], [0064]. Baek recognizes that in order to provide higher definition displays, “a number of bits for a gray level should be increased.” Ex. 1005 (Baek) ¶[0006]. Baek recognizes that “[a] conventional display driver circuit, which may include a digital-to-analog converter (DAC) corresponding to each one of the channels, may be limited in its function as the number of the gray-scale bits and the number of the channels increases.” Ex. 1005 (Baek) ¶[0007]. Examples of such conventional circuit include the ones described in the ’047 Patent. Ex. 1001 (the ’047 Patent) at 7:1-35; Fig. 1A. Baek further recognizes that for “larger scaled and higher definition panel[s],” the need exists for “performing faster sampling on an analog gray-scale signal, and ... reducing a mismatch between a sampling value and a holding value of the analog gray-scale signal.” Ex. 1005 (Baek) ¶[0019].

84. Baek discloses an LCD/OLED display driver circuit “capable of supporting an increased number of gray-scale bits and increased number of channels.” Ex. 1005 (Baek) ¶[0007]. This allows for “a display driver circuit with a smaller chip size capable of supporting a larger scaled and higher definition panel.” Ex. 1005 (Baek) ¶[0019]. To solve the above mentioned problems and to reduce charge time, Baek improves the conventional driving circuit by adding a pre-charge circuit to pre-charge each channel to reduce the charge time. Ex. 1005 (Baek) ¶[0026], ¶[0062].

85. As shown in the Figure 3 below, Baek discloses that a current digital-to-analog converter (DAC) 330 (annotated in gold) converts display data signals into analog currents, which are then supplied to current sample/hold (S/H) output circuits as reference currents. As suggested by its name, a current S/H output circuit samples and holds a reference current and later outputs the held reference current to a corresponding channel. Ex. 1005 (Baek) ¶¶[0045]-[0048].

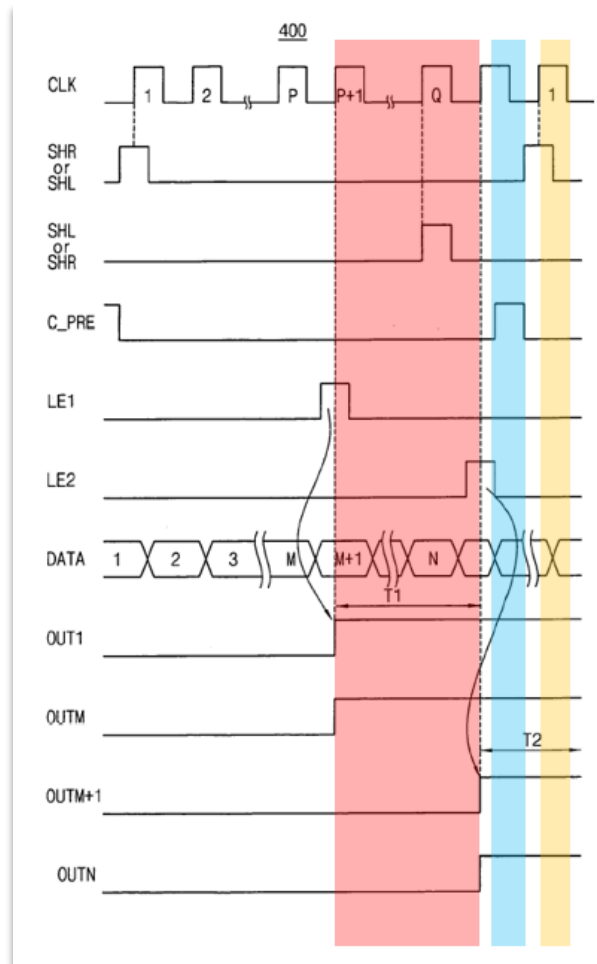


Ex. 1005 (Baek) at Fig. 3 (annotated).

86. Similar to the '047 Patent, Baek employs a pre-charge circuit to pre-charge the storage capacitor CST to reduce the overall charge time. Ex. 1005 (Baek) ¶¶[0062], [0063]. As shown in the Figure 3 above, a pre-charge circuit is connected to multiple current S/H circuits. Ex. 1005 (Baek) at Fig. 3. The pre-charge circuit

charges the storage capacitor in accordance with the C_PRE signal. Ex. 1005 (Baek) ¶¶[0062], [0063].

87. Also similar to the '047 Patent, Baek discloses the circuit may operate under three modes: (1) a voltage-supply mode (C_PRE signal is activated, annotated red); (2) a current supply mode (CLK signal is activated, annotated blue); and (3) a current output mode (latch enable signal is activated, annotated yellow). As shown in Figure 4 below, when C_PRE signal is activated (annotated in red), the pre-charge circuit applies a voltage to the storage capacitor CST to “pre-charge a voltage of the storage capacitor CST” Ex. 1005 (Baek) ¶¶[0062], [0063]. When CLK signal is activated (annotated in blue), current from DAC is supplied to the storage capacitor CST to further charge the capacitor to a level corresponding to the reference current. Ex. 1005 (Baek) ¶[0056]. When the latch enable signal (LE1 or LE2) is activated (annotated in yellow), the circuit outputs a current based on the voltage previously stored in the storage capacitor CST. Ex. 1005 (Baek) ¶¶[0057], [0058].



Ex. 1005 (Baek) at Fig. 4 (annotated).

88. Therefore, Baek teaches a driving device with a pre-charge function that reduces the time needed for charging a capacitor, solving the known problem identified in the '047 Patent and offering a similar solution.

C. SASAKI (EX. 1006)

a. Status of Sasaki as Prior Art

89. “Sasaki” refers to United States Patent Application Publication No. 2005/0017765, entitled “Current Generation Supply Circuit and Display Device.”

Sasaki names Kazuhiro Sasaki and Katsuhiko Morosawa as the inventors and was assigned to Casio. Sasaki was filed in the United States on July 14, 2004 and published on January 27, 2005. Thus, Sasaki published more than one year before the earliest possible priority date of the '047 Patent. Accordingly, I understand that Sasaki qualifies as prior art to the '047 Patent.

b. Overview of the Disclosure of Sasaki

90. The field of the invention in Sasaki includes “a display panel comprising with [*sic*] display pixels comprising current control type light emitting devices for executing a light generation operation at predetermined luminosity gradations based on gradation currents corresponding to the display signals.” Ex. 1006 (Sasaki) ¶[0003]. Sasaki discloses “[a] current generation supply circuit which supplies drive currents corresponding to digital signals for a plurality of loads.” Ex. 1006 (Sasaki) at Abstract.

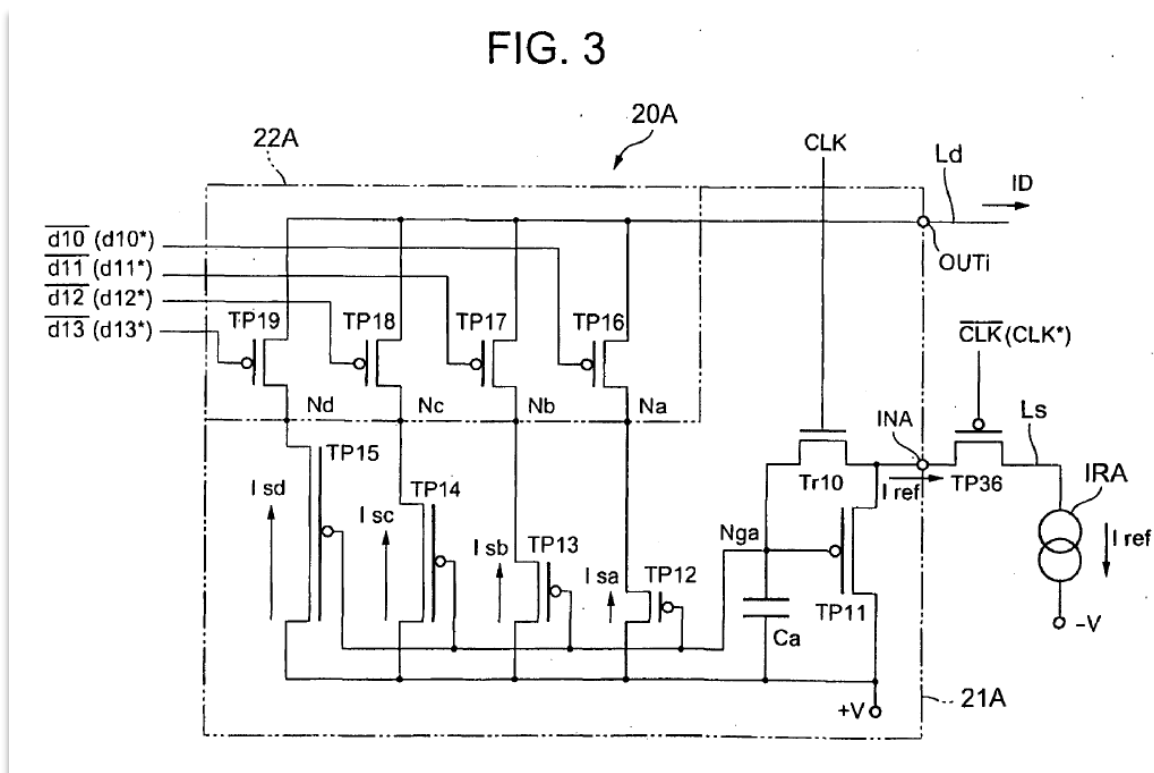
91. Sasaki recognizes “variations in the current values of the light generation drive currents become noticeably greater over a period of time, thereby resulting in the troublesome problem of acquiring the desired luminescent characteristic in a stable state.” Ex. 1006 (Sasaki) ¶[0009]. Further, Sasaki recognizes the problem identified in the '047 Patent (i.e., the problem of prolonged charging time):

[W]hen the reference current supplied particularly via the current supply source line is exceptionally low, the charge and discharge operation takes time and until the potential of the current supply source line is stabilized, a relatively lengthy period is required.

Ex. 1006 (Sasaki) ¶[0010].

92. Similar to the current output circuit described in the '047 Patent, a current generation section is disclosed in Sasaki. As shown in the Figure 3 below, the current generation section comprises a capacitor Ca “charge storage circuit,” which receives a reference current (I_{ref}) from a current supply source (IRA) and holds a voltage corresponding to the reference current I_{ref} . Ex. 1006 (Sasaki) ¶¶[0014], [0071]. Sasaki further discloses a set of module current transistors TP12-TP15, which generates analog currents based on the gate voltage (i.e. the voltage held in the capacitor Ca) of the transistors. Ex. 1006 (Sasaki) ¶[0063]. The output of analog currents of the module current transistors is controlled by a set of switching transistors TP16-TP19 in response to corresponding digital output signals (d10-d13). Ex. 1006 (Sasaki) ¶[0065]. Finally, the analog currents are transmitted to downstream channels and pixels. Therefore, Sasaki teaches a driving circuit with a layout similar to the one described in the '047 Patent.

FIG. 3



Ex. 1006 (Sasaki) at Fig. 3.

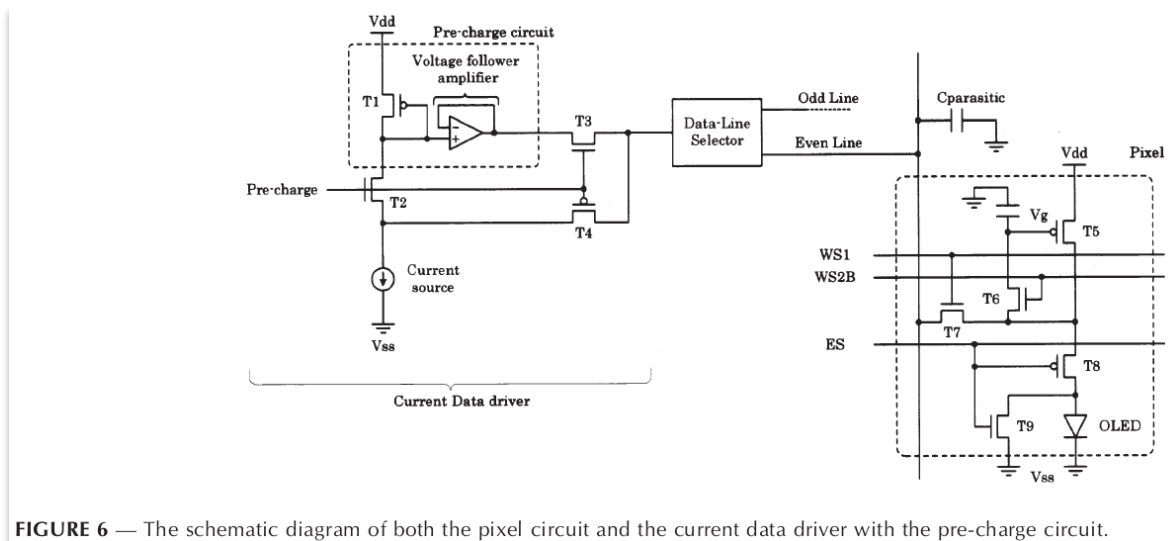
XII. GROUNDS 1 & 2: SHIMODA

93. It is my opinion that Claims 1-4, and 9 of the '047 Patent are each anticipated by Shimoda (Ex. 1004), corresponding to Ground 1. To the extent Patent Owner contends that any of these claims are not anticipated, then they would have been rendered obvious over Shimoda in view of the knowledge of a POSITA, corresponding to Ground 2.

A. INDEPENDENT CLAIM 1 OF THE '047 PATENT

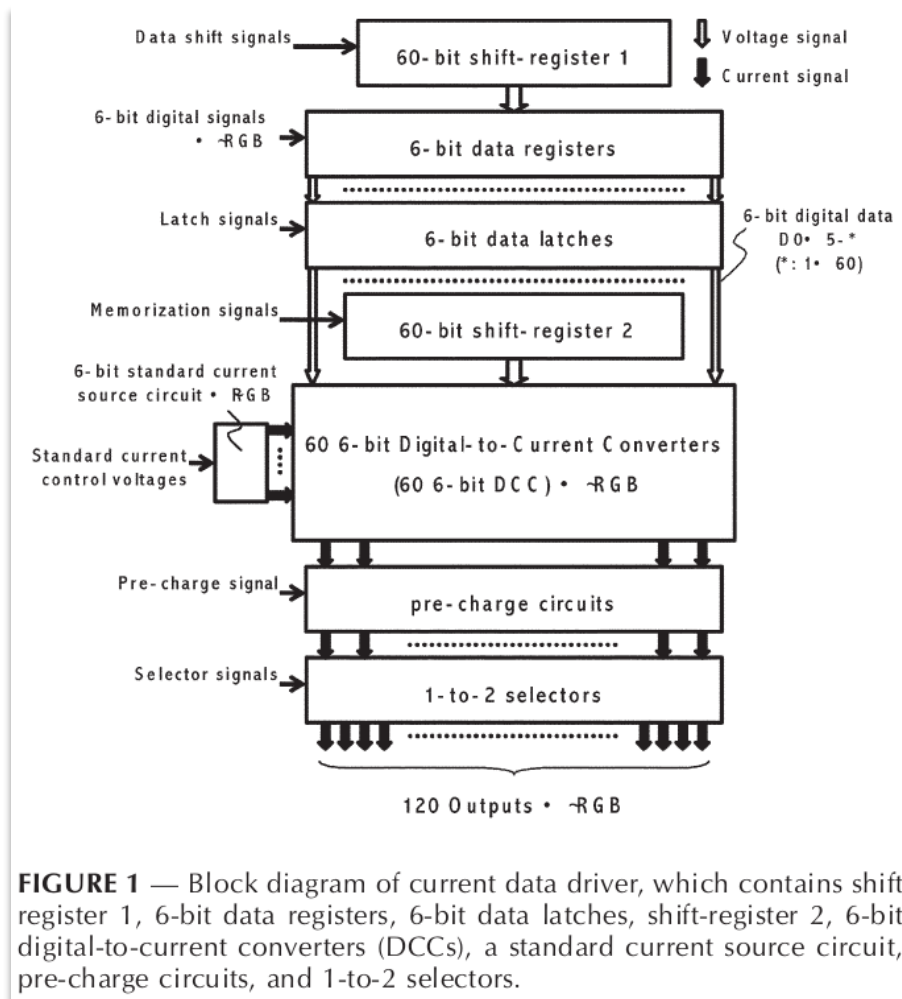
a. 1(pre): “A current driving device, comprising:”

94. To the extent the preamble is limiting, Shimoda discloses the preamble. The current driving device of Shimoda, as shown in Figure 6, includes an integrated current data driver (which contains the pre-charge circuit) and a pixel circuit.



Ex. 1004 (Shimoda) at Figure 6. As described by the caption, Figure 6 provides a “schematic diagram of both the pixel circuit and the integrated current data driver containing a pre-charge circuit,” as well as an OLED. *See also* Ex. 1004 (Shimoda) §3.1 (“Figure 6 is a diagram of both the pixel circuit and the integrated current data driver containing a pre-charge circuit.”).

95. In addition to being depicted in Figure 6, the current data driver is displayed in Figure 1 of Shimoda:



Ex. 1004 (Shimoda) at Figure 1. Shimoda discloses that the “current data driver is capable of outputting highly accurate ($\pm 0.8\%$) current determined by 6-bit digital input data.” Ex. 1004 (Shimoda) at Abstract. Regarding the pixel circuit, Shimoda explains that “the brightness of each pixel ... is dependent on the current in the OLED that is driven by each pixel circuit, and an important issue for poly-Si TFT OLED displays has been the pixel-driving technology needed to achieve uniformity in OLED currents.” Ex. 1004 (Shimoda) §1.

b. **1(a): “a first voltage supply source for supplying a first voltage;”**

96. Shimoda discloses this limitation. The “pre-charge circuit” in Shimoda is an example of the claimed “a first voltage supply source.” Shimoda describes the structure of the pre-charge circuit: “The pre-charge circuit is composed of one TFT (T1) and a voltage-follower amplifier.” Ex. 1004 (Shimoda) §3.1. The term “TFT” is an abbreviation for a “thin-film-transistor.” A voltage-follower amplifier is an op-amp circuit that acts as a buffer, whose output voltage is equal to the input voltage.

97. The “voltage-follower amplifier outputs the gate voltage of T1 into the gate electrode of T5, with T6 and T7 turned on. This pre-charge function rapidly pre-charges the voltage in the gate electrode of T5...” Ex. 1004 (Shimoda) §3.2. Thus, the output of the pre-charge circuit is an example of the claimed “a first voltage.”

98. The pre-charge circuit is shown in Figures 1 and 6 of Shimoda and is annotated in blue. The “a first voltage” that is supplied by the pre-charge circuit is annotated in green.

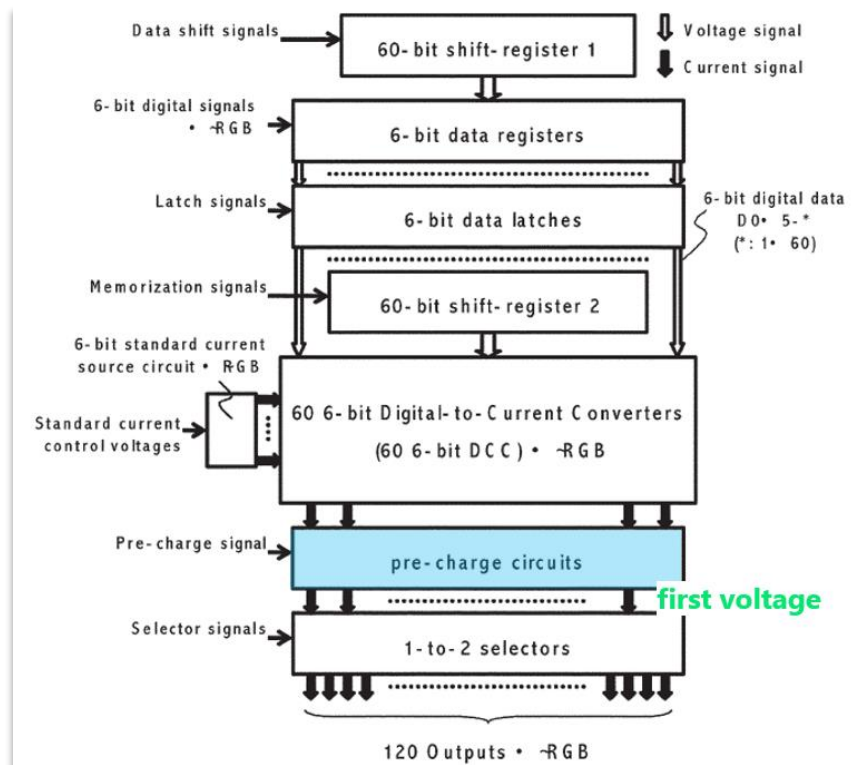


FIGURE 1 — Block diagram of current data driver, which contains shift register 1, 6-bit data registers, 6-bit data latches, shift-register 2, 6-bit digital-to-current converters (DCCs), a standard current source circuit, pre-charge circuits, and 1-to-2 selectors.

Ex. 1004 (Shimoda) at Fig. 1 (annotated).

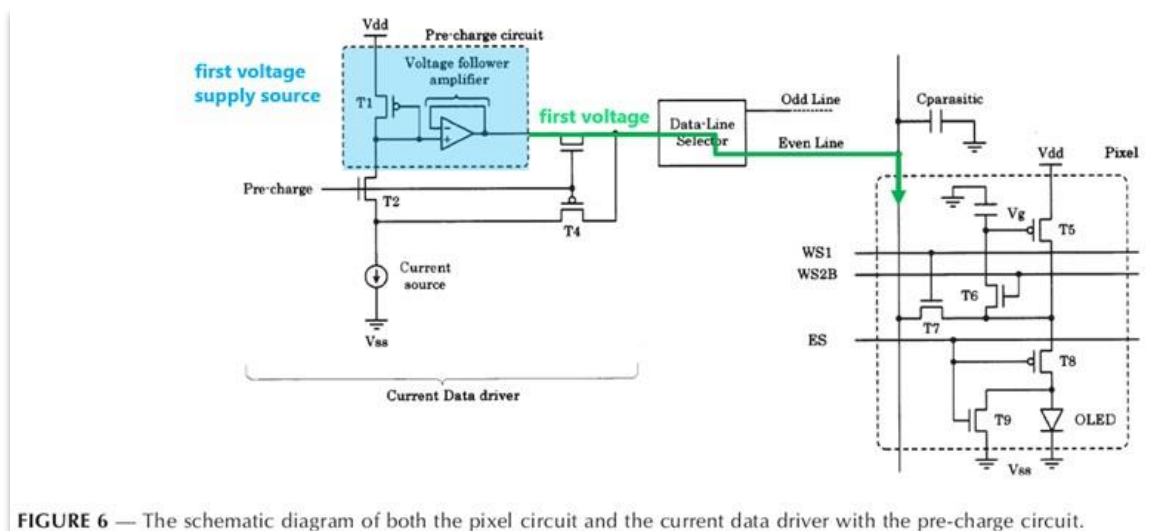


FIGURE 6 — The schematic diagram of both the pixel circuit and the current data driver with the pre-charge circuit.

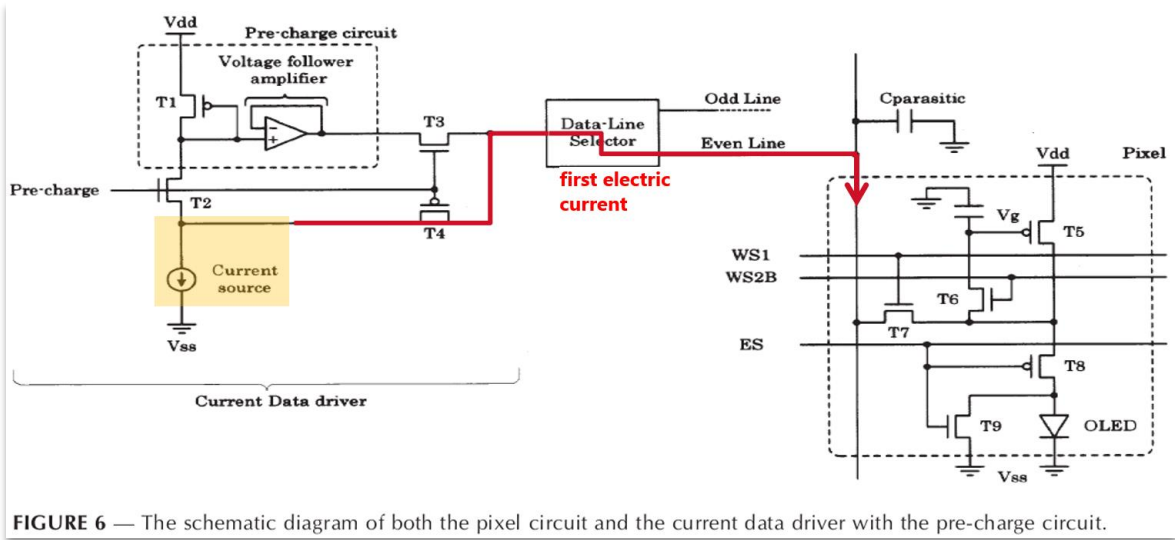
Ex. 1004 (Shimoda) at Fig. 6 (annotated).

c. **1(b): “a first current supply source for supplying a first electric current;”**

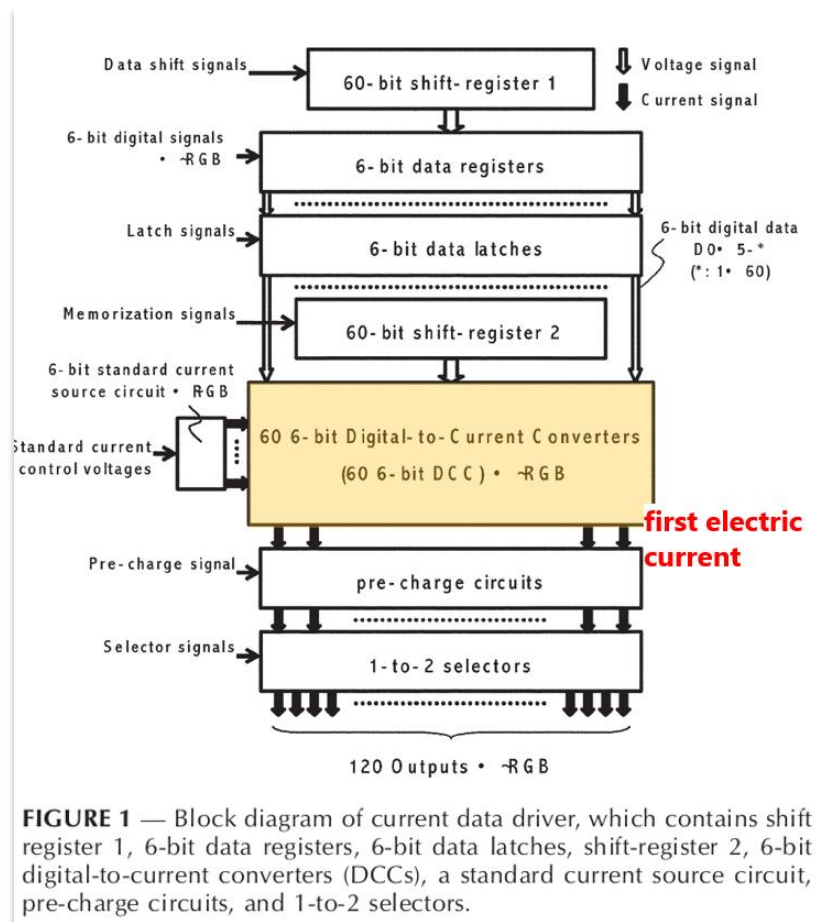
99. Shimoda discloses this limitation. Shimoda describes a “current source” containing a digital-to-current converter, i.e., “DCC,” which is an example of the claimed “a first current supply source.” As shown in Figure 6, the “current source indicated in the diagram represents a 6-bit DCC [digital-to-current converter] which generates an analog current on the basis of 6-bit digital data that has been input to it. ...” Ex. 1004 (Shimoda) §6.1 (emphasis added); *see also* Fig. 1 (caption, stating that the “current data driver ... contains 6-bit digital-to-current converters (DCC)”). The current supplied by the current DCC of Shimoda is an example of the claimed “a first electric current.” Shimoda explains regarding the current source:

Setting the current from the current source high makes it possible to compensate for the greater per-recharge error that occurs during current-programming periods. This improves the accuracy of current programming significantly.

Ex. 1004 (Shimoda) §3.2. Figure 6 has been annotated to show the claimed current source (annotated in gold) and the lines along which the claimed first electric current flows (annotated in red) supplied by that current source. The red arrow in Figure 6 (annotated below) indicates the direction of how energy is supplied to the pixel circuit, while the actual current (as indicated by the current source symbol) flows in the opposite direction.



Ex. 1004 (Shimoda) at Fig. 6 (annotated). The claimed current source (annotated in gold) can also be seen in Figure 1 of Shimoda.



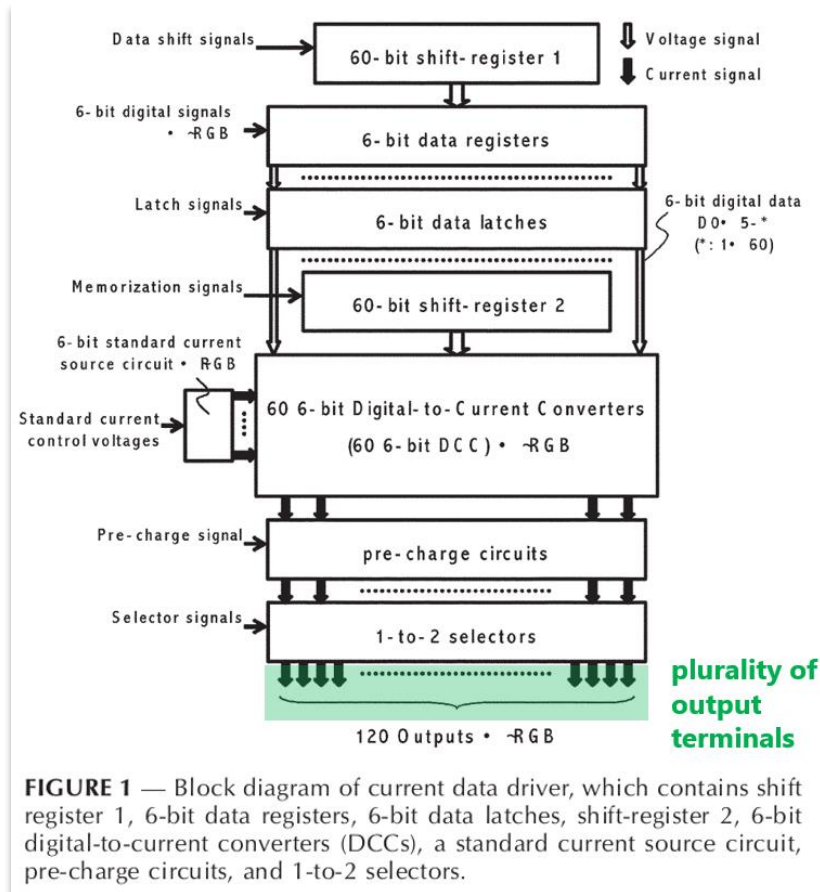
Ex. 1004 (Shimoda) at Fig. 1.

d. 1(c): “a plurality of output terminals;”

100. Shimoda discloses this limitation. Shimoda provides at least two examples of structure that constitutes a plurality of output terminals (i.e., two or more output terminals).

101. First, Shimoda explains that a display using the current data drivers and pixel circuits would include a pixel count of “120×RGB×136.” Ex. 1004 (Shimoda) §5 (Table 1). Thus, the display would include an array of 120×136 pixels, with each

pixel providing three colors (red, green, blue). Accordingly, Shimoda explains that each current data driver comprises at least 120 output terminals, annotated in green.

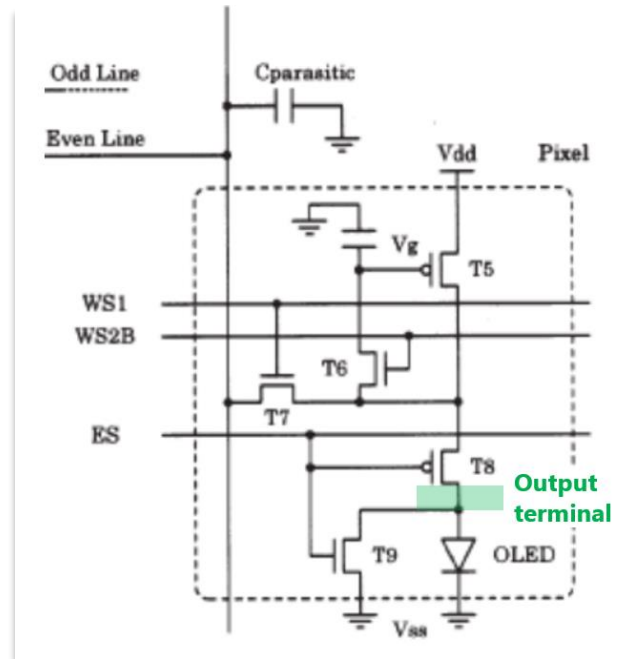


Ex. 1004 (Shimoda) at Fig. 1 (annotated).

102. Second, Shimoda provides another example of a plurality of output terminals. Shimoda discloses that for each pixel circuit, “[i]n order to control the emission period, the switching TFT (T8) is used to cut off the current to the OLED.”

Ex. 1004 (Shimoda) §3.1. The drain of transistor T8 (lower terminal) is connected

to the OLED, outputting the calibrated current to the OLED. Thus, the lower terminal of T8 is also an example of an output terminal. The lower terminal (drain) of transistor T8 is shown below in green:



Ex. 1004 (Shimoda) at Fig. 6 (annotated and excerpted). As explained above, the exemplary device in Shimoda comprises at least 120×136 pixels. Ex. 1004 (Shimoda) at Abstract (“A 1.9-in. 120×136 -pixel AMOLED display using these circuits was demonstrated”). And, as show in Figure 6 above, each individual pixel comprises at least one output terminal (annotated green). Ex. 1004 (Shimoda) at Fig. 6. Thus, Shimoda discloses a plurality of output terminals.

- e. **1(d)(1): “and a plurality of current output circuits for outputting an electric current in accordance with said first electric current, each of said current output circuits comprising”**

103. Shimoda discloses this limitation. Each pixel circuit is an example of the claimed “current output circuit,” because for example, it outputs current to an OLED. Though Figure 6 of Shimoda graphically depicts only a single pixel circuit, a POSITA would have recognized (or at least it would have been obvious) that there would be a many such pixel circuits (two or more) in the device disclosed by Shimoda.

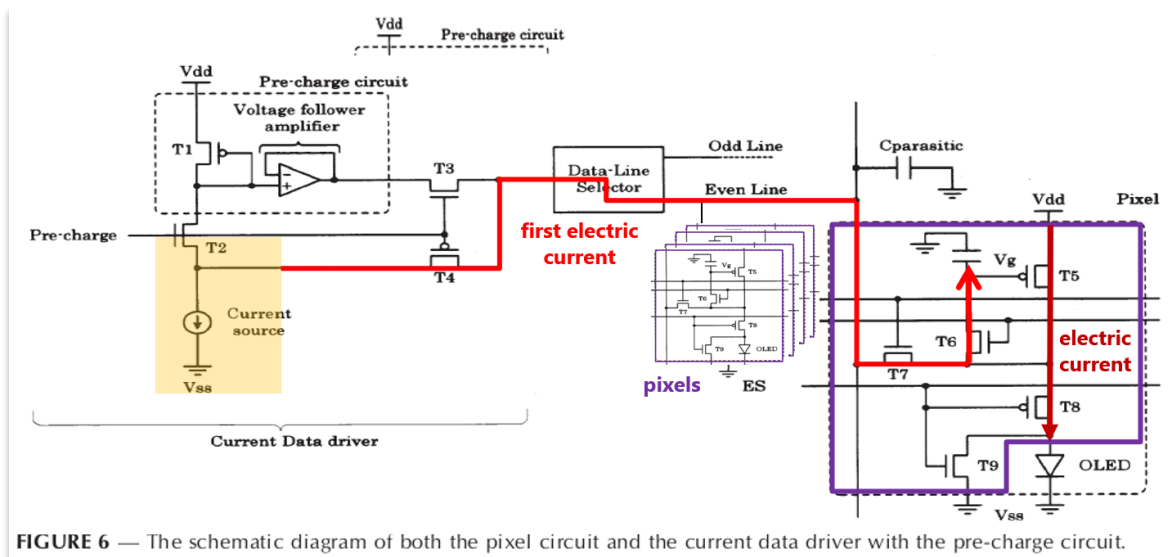
104. Regarding the claimed first electric current, and as described above for Claim Limitation 1(b), Shimoda explains that the current data driver is capable of “outputting highly accurate ($\pm 0.8\%$) current determined by 6-bit digital input data.” Ex. 1004 (Shimoda) at Abstract. The current source in Figure 6 of Shimoda is a 6-bit digital-to-current converter, which converts the 6-bit digital input data into a gray-scale current, which is supplied to the pixel circuit. *See*, Ex. 1004 (Shimoda) §§2.1, 3.1. As shown in Figure 6 below, each pixel circuit (annotated purple) receives a current (the claimed “first electric current,” annotated red) from the claimed current source (annotated gold) during a current-programming period.

In the subsequent current-programming period, T4 is turned on, T2 and T3 are turned off, the pre-charge circuit is disconnected, and the current from the current source is directly supplied to the pixel circuit.

Ex. 1004 (Shimoda) §3.2. Then during an emission period, the pixel circuit outputs a current (the claimed “an electric current,” annotated dark red) in accordance with the first electric current. *See*, Ex. 1004 (Shimoda) §3.2.

After the horizontal period, T6 and T7 are turned off, T8 is turned on, and a current programmed by the data driver is supplied to the OLED. The emission period is controlled by erase-scan signals which turn T8 and the reset TFT T9 on and off. Setting the emission period short makes it possible to set the current of the current source high enough to obtain the same average brightness over successive frame periods.

Ex. 1004 (Shimoda) §3.2. The current-programming period and the emission period are explained in more detail below regarding claim elements 1(f)-1(h).



Ex. 1004 (Shimoda) at Fig. 6 (annotated). The figure has been annotated to add multiple pixel circuits (labeled “pixels,” in purple), because Shimoda discloses (or at least renders obvious) that multiple such pixels would be present.

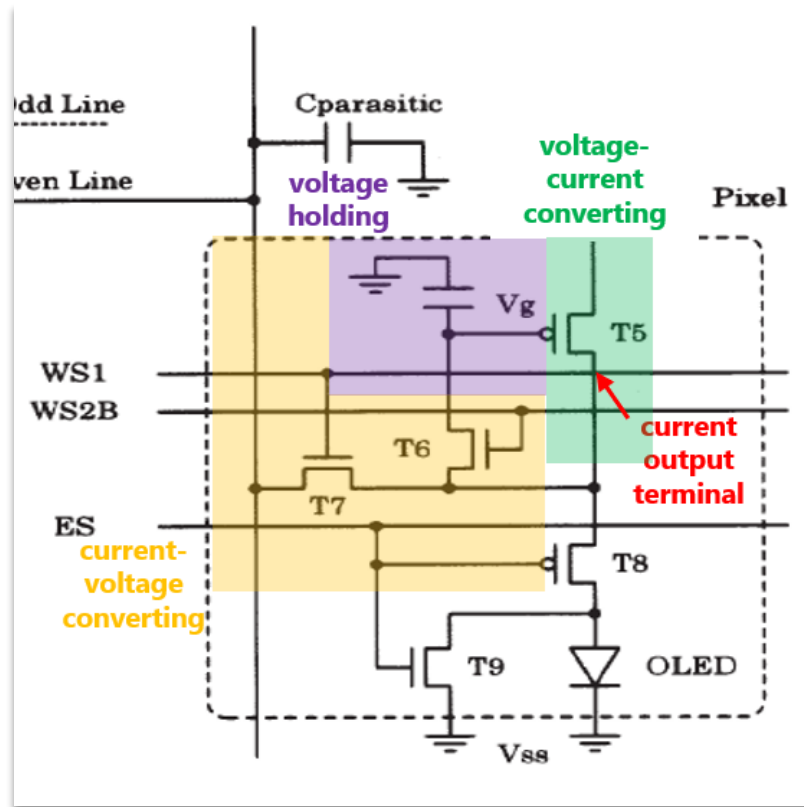
105. Each pixel circuit outputs an electric current “in accordance with” the first electric current (e.g., current from the DCC in current source). A POSITA would have recognized that one of the fundamental properties of a transistor is that it outputs a current in accordance with its gate voltage. During an emission period, the current output from transistor T5 is determined by the gate voltage of transistor T5, which is calibrated during the current-programming period by the first electric current. A POSITA would have recognized that the output electric current from transistor T5 is equal in magnitude of the first electric current, because the gate capacitor holds the gate voltage when the first electric current passes transistor T5 and applies the same gate voltage to transistor T5 during an emission period. *See*, Ex. 1004 (Shimoda) §3.2.

106. Though Figure 6 of Shimoda only graphically depicts one pixel circuit (current output circuit), a POSITA would have recognized (or in the alternative, it would have been obvious) that the device fabricated by Shimoda would have contained two or more identical pixel circuits. First, Shimoda describes there a display has multiple pixels and thus multiple pixel circuits: “120 × 136-pixel AMOLED display using these circuits.” Ex. 1004 (Shimoda) at Abstract; *see also* Shimoda §5 (Table 1, stating: “pixel count: 120 × RGB × 136”). Second, Shimoda explains that each OLED is driven by a pixel circuit: “This brightness is dependent on the current in the OLED that is driven by each pixel circuit” Ex. 1004

(Shimoda) §1. Third, Figure 6 above shows that the output of a pixel circuit is an OLED.

- f. **1(d)(2): “a current-voltage converting circuit, a voltage-current converting circuit, a voltage holding circuit having a terminal being connected to a reference voltage different from the first voltage, and at least one current output terminal, wherein,”**

107. Shimoda discloses this limitation. As shown in annotated Figure 6, each pixel circuit in Shimoda discloses a current-voltage converting circuit (annotated gold), a voltage-current converting circuit (annotated green), a voltage holding circuit (annotated purple) and at least one current output terminal (annotated red).

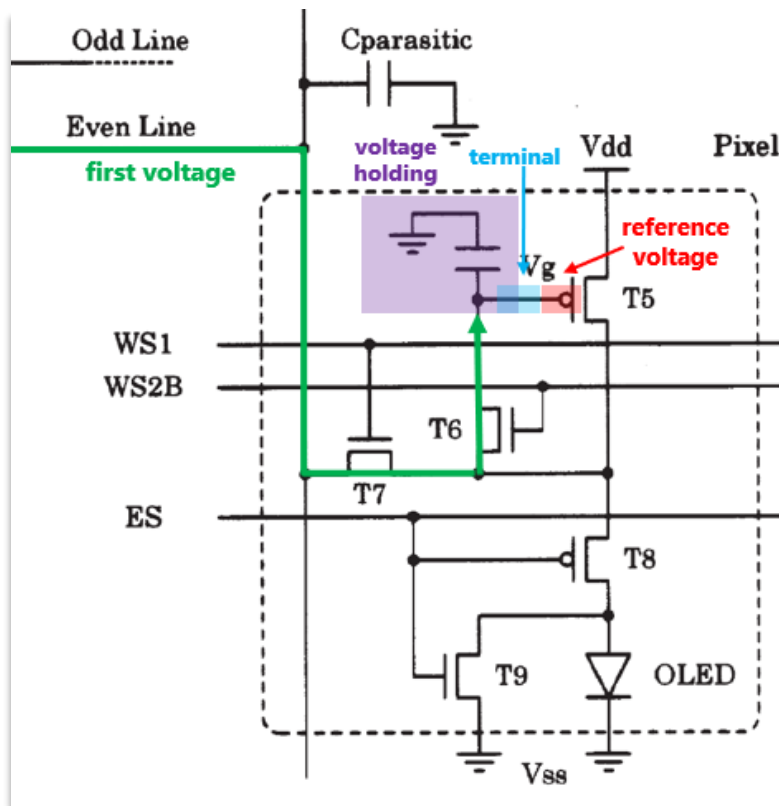


Ex. 1004 (Shimoda) at Fig. 6 (annotated and excerpted).

- i. **“a voltage holding circuit having a terminal being connected to a reference voltage different from the first voltage”**

108. Shimoda discloses this limitation. The pixel circuit includes a voltage holding circuit (annotated purple). A component of a voltage holding circuit includes a gate capacitor that stores the gate voltage (V_g) of transistor T5. A POSITA would have recognized that one of the fundamental properties of a capacitor is that it holds voltage. As shown in Figure 6 below, the gate capacitor has two ends. One end of the gate capacitor is connected to ground. The other end of the gate capacitor comprises a terminal (annotated red) connected to the gate of thin-

film transistor T5 and another terminal (annotated light green) connected to the first voltage supply source, which supplies the first voltage (annotated green). The gate capacitor thus holds the gate voltage of transistor T5 during the current-programming period. *See* Ex. 1004 (Shimoda) §3.2.



Ex. 1004 (Shimoda) at Fig. 6 (annotated and excerpted).

109. Shimoda also discloses that the voltage holding circuit has the claimed “a terminal being connected to a reference voltage different from the first voltage.” The gate capacitor is connected to ground and has a terminal (annotated blue) connected to the gate of transistor T5. As will be discussed further below, there are

at least two operation modes: a pre-charge period and current-programming period. The voltage on the capacitor corresponds to the claimed “first voltage” during the pre-charge period, and corresponds to a different voltage—the claimed “reference voltage”—during the current-programming period.

110. During the pre-charge period, the pre-charge circuit provides a first voltage that charges the gate capacitor and thus increases the gate voltage of transistor T5 to such a level that “a current roughly equivalent to the value of the current source flows through T5.” Ex. 1004 (Shimoda) §3.2. Following the pre-charge period is a current-programming period, during which the gate capacitor continues to be charged until it reaches a different voltage. This additional charging compensates for errors that may occur during a pre-charge period. Ex. 1004 (Shimoda) §3.2 (“While a pre-charge error may be generated if there exist variations in characteristics between T1 and T5, or if there is an offset voltage in the voltage-follower amplifier, this error can be compensated for during current-programming periods”).

111. By way of confirmation of my analysis, similar to Shimoda, the voltage-holding circuit in the '047 Patent also includes a capacitor for holding a voltage that is connected between ground and a transistor gate:

One end of a voltage holding capacitance element C1 is connected to a ground terminal, and the other end is connected in common to gate terminals of m-numbers of Nch transistors QN1-QNm

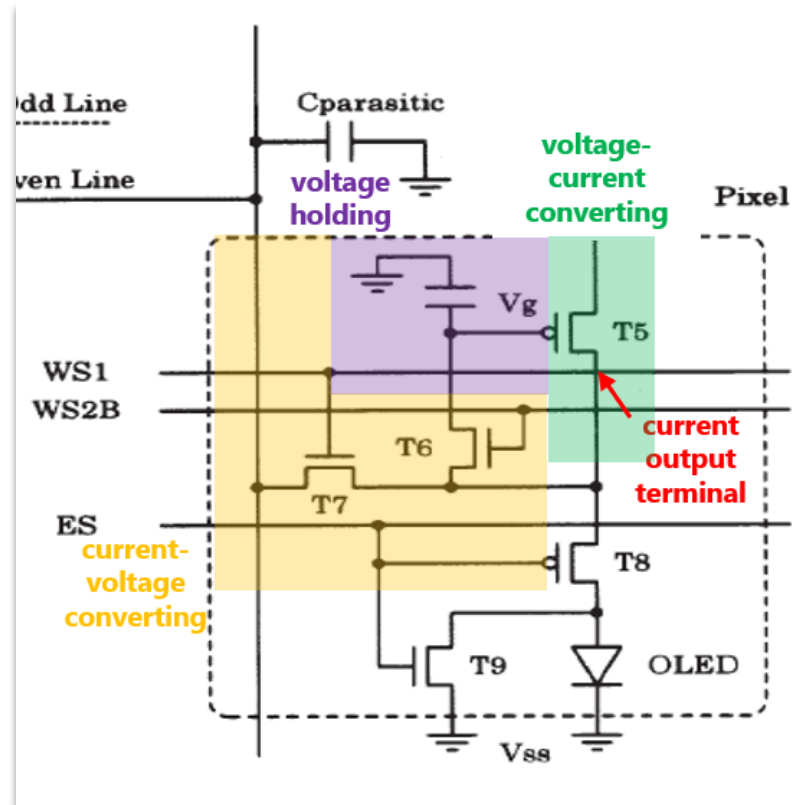
Ex. 1001 ('047 Patent) at 7:3-6. The capacitor C1 “holds the gate voltage for allowing the electric current with the same current value as that of the reference current to be flown.” Ex. 1001 ('047 Patent) at 8:11-15. Similar to the two charging periods in Shimoda, two supply modes are described in the '047 Patent: a voltage supply mode and a current supply mode. Under the voltage supply mode, the voltage on the capacitor corresponds to the claimed “first voltage.” Ex. 1001 ('047 Patent) at 7:48-52 (“At this time, the voltage holding capacitance element C1 is charged to a constant voltage (this corresponds to the first voltage, and will be referred to as a reference voltage² hereinafter) that is supplied from the voltage supply source V1.”). Under the current supply mode, the voltage on the capacitor corresponds to the claimed “reference voltage.” Ex. 1001 ('047 Patent) at 8:6-8 (“At this time, the voltage holding capacitance element C1 accumulates the electric charges in accordance with the gate voltages.”). Thus, Shimoda teaches an essentially identical circuit design and operation as the '047 Patent.

ii. “a current-voltage converting circuit”

112. Shimoda discloses this limitation. The pixel circuit includes a current-voltage converting circuit comprising an input terminal connected to the current

² This reference voltage is the first voltage and thus is not the claimed “reference voltage,” which is “different from the first voltage”

supply source, transistors T6-T7, and gate capacitor. The current-voltage converting circuit is annotated below in gold:



Ex. 1004 (Shimoda) at Fig. 6 (annotated and excerpted). The current-voltage converting circuit converts the first electric current from the current source to the gate voltage held at the gate capacitor. Ex. 1004 (Shimoda) §3.2. During a current-programming period (i.e. the claimed “current supply mode”), the switching transistors T6 and T7 are turned on, causing the first electric current to be supplied to the gate capacitor. *See*, Ex. 1004 (Shimoda) §3.2. The voltage across the gate capacitor (corresponding to the gate voltage of transistor T5) accumulates as the

current charges the gate capacitor. The current passing through transistor T5 then increases as the gate voltage increases, because one of the fundamental properties of a transistor is that it outputs current based on its gate voltage. *See* Ex. 1004 (Shimoda) at Fig. 8(a). As a result, the current charging the gate capacitor reduces as more of the first electric current is routed to the branch with transistor T5. When the current charging the capacitor reduces to zero, the capacitor is fully charged, retaining a voltage corresponding to gate voltage of transistor T5 that allows the entire first electric current flowing through transistor T5. *See*, Ex. 1004 (Shimoda) §3.2. The current-voltage converting process is then completed. *See*, Ex. 1004 (Shimoda) §3.2.

113. By way of confirmation of the analysis, the '047 Patent operates in the same manner as Shimoda. Under the current supply mode, “a current-voltage converting function is actuated.” Ex. 1001 ('047 Patent) at 8:60-61. Switches Sw1, Sw2, and G1-Gm are set to be in a conductive state, connecting the current supply source to the voltage holding capacitor C1 and current-voltage converting elements QN1-QNm. Ex. 1001 ('047 Patent) at 8:61-64; 10:28-36; Fig. 1A. Similar to Shimoda, the reference voltage is generated at the gates of transistors QN1-QNm and held in the voltage holding capacitor C1:

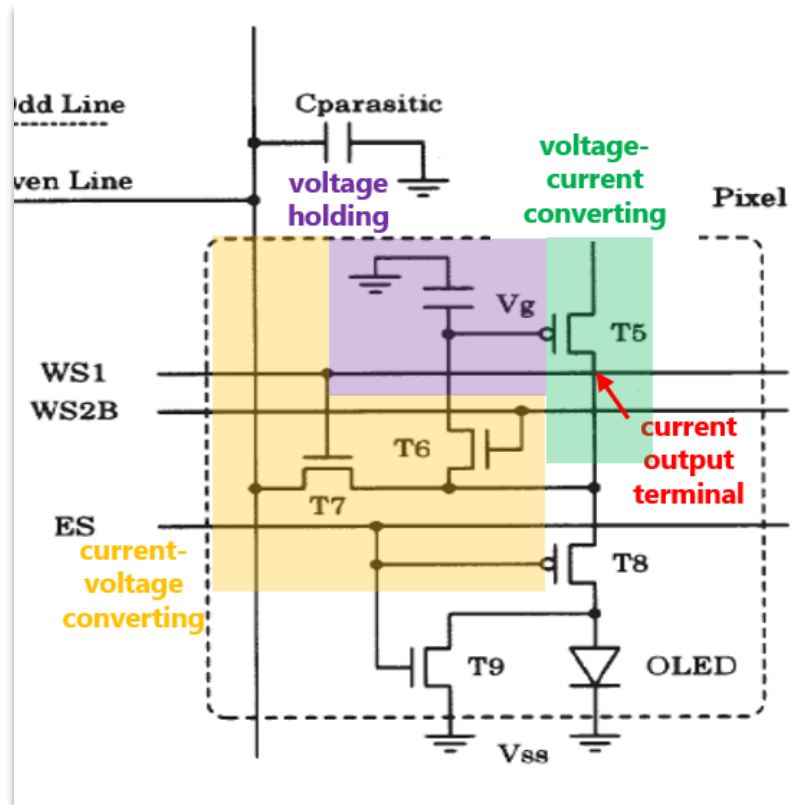
Therefore, the Nch transistors QN1-QNm have an electric current (reference current) with a constant current value from the reference current source I1 flown therein as a load. At this time, a gate voltage

for passing the electric current from the reference current source I1 is generated uniquely at the gates of the Nch transistors QN1-QNm. Therefore, the voltage holding capacitance element C1 accumulates the electric charges in accordance with the gate voltages.

Ex. 1001 ('047 Patent) at 8:3-11. Thus, Shimoda teaches an essentially identical operations as the '047 Patent.

iii. “a voltage-current converting circuit”

114. As shown in Figure 6 below, Shimoda discloses a voltage current converting circuit (annotated green). The pixel circuit includes thin-film transistor T5. During an emission period, switching transistors T6, T7, and T9 are turned off and switching transistor T8 is turned on. Thus, during an emission period, transistor T5 outputs a current in accordance with the voltage applied to its gate terminal through its drain terminal. The output current is further supplied to the downstream OLED.



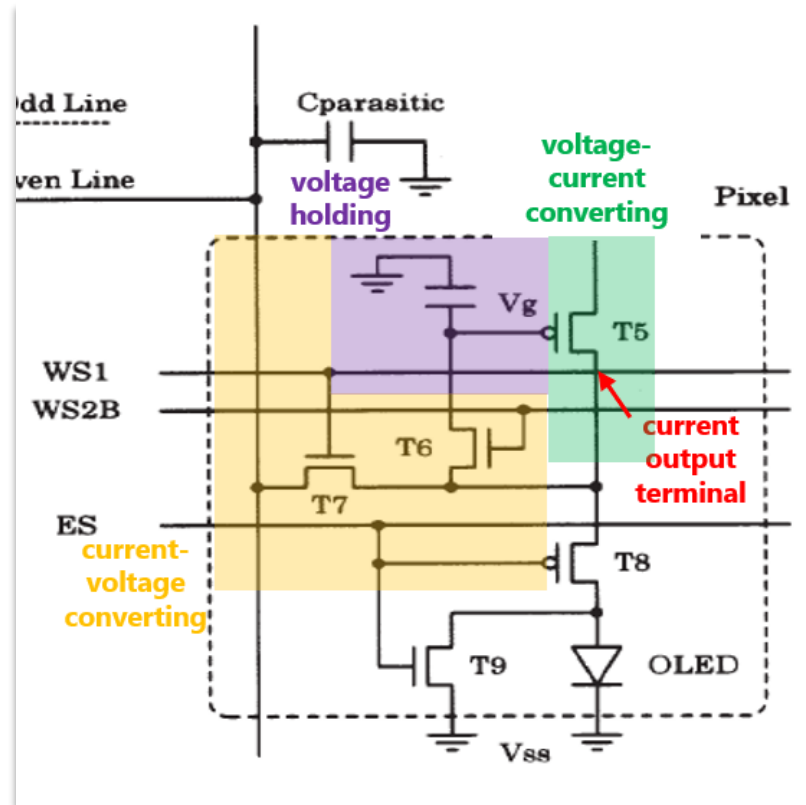
Ex. 1004 (Shimoda) at Fig. 6 (annotated and excerpted).

115. By way of confirmation of my analysis, similar to Shimoda, the '047 Patent explains that the voltage-current converting function is performed in the current output mode, where transistors QN1-QNm convert the voltage applied to the gate of QN1-QNm into current flowing through QN1-QNm. Ex. 1001 ('047 Patent) at 8:30-38.

iv. “at least one current output terminal”

116. Shimoda discloses this limitation. As shown in Figure 6 below, the drain terminal of the transistor T5 (annotated red) is an example of the claimed “current output terminal.” As explained above, transistor T5 outputs at the drain a

current in accordance with its gate voltage. Thus, the drain terminal of the transistor T5 is an example of the current output terminal.



Ex. 1004 (Shimoda) at Fig. 6 (annotated and excerpted).

117. By way of confirmation of my analysis, similar to Shimoda, the '047

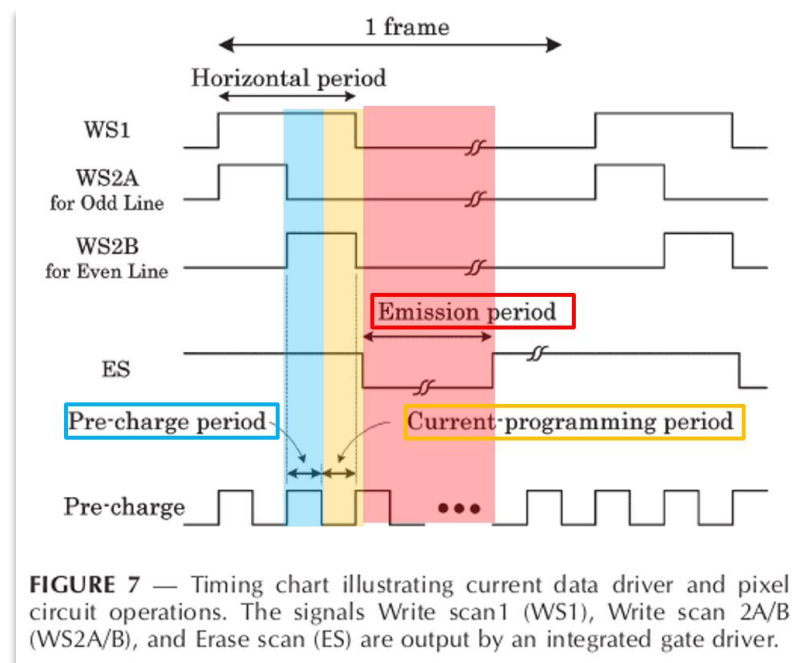
Patent explains that under a current output mode:

A gate voltage according to the electric charges accumulated in the voltage holding capacitance element C1 is applied to the gates of the Nch transistors QN1-QNm. Thus, it is possible to output a sink current having a current value proportional to the reference current in accordance with the conduction states of the current output switches So1, So2 and the signal response switches G1-Gm, through connecting a power source to the current output terminal T1 or the current output terminal T2.

Ex. 1001 ('047 Patent) at 8:30-33.

- g. **1(e): “each of said current output circuits operates in three operation modes including a voltage supply mode, a current supply mode, and a current output mode,”**

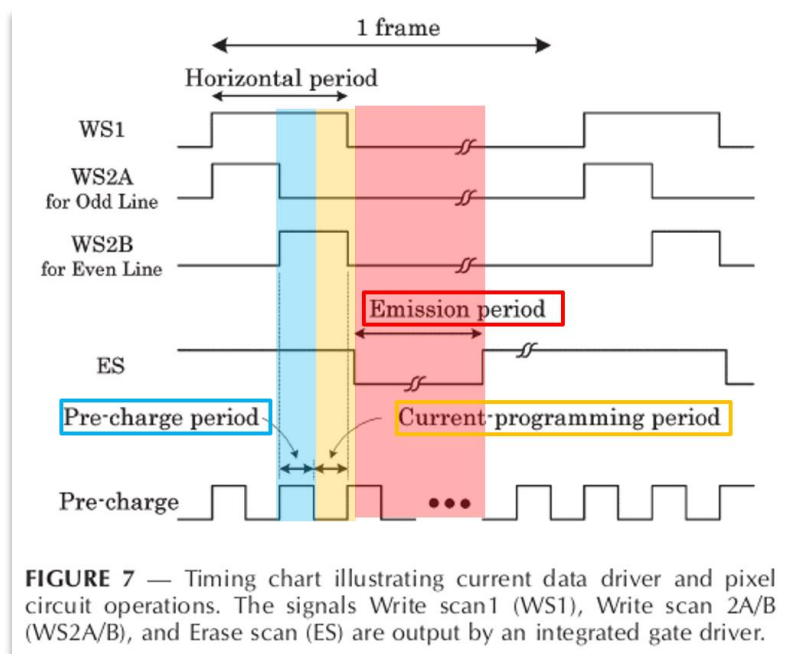
118. Shimoda discloses this limitation. Shimoda describes each of the pixel circuits operates in at least three operation modes. These modes include a pre-charge period (corresponding to the claimed “voltage supply mode,” annotated in blue), a current-programming period (corresponding to the claimed “current supply mode,” annotated in gold), and an emission period (corresponding to the claimed “current output mode,” annotated in red). These modes are shown in Figure 7, which according to the caption, is a “[t]iming chart illustrating current data driver and pixel circuit operations.”



Ex. 1004 (Shimoda) at Fig. 7 (annotated). These operation modes are described further below.

- h. **1(f): “under said voltage supply mode, each of said current output circuits receives said first voltage from said first voltage supply source, and the first voltage is supplied to another terminal of said voltage holding circuit,”**

119. Shimoda discloses operation under a voltage supply mode, including during a pre-charge period, which is annotated in blue. Shimoda discloses that the purpose of a “data-line pre-charge function [is] in order to reduce current-programming times and to achieve accurate current-programming at low gray-scale levels.” Ex. 1004 (Shimoda) §3. The pre-charge period can be seen as a portion of a horizontal period in Figure 7, annotated below in blue.

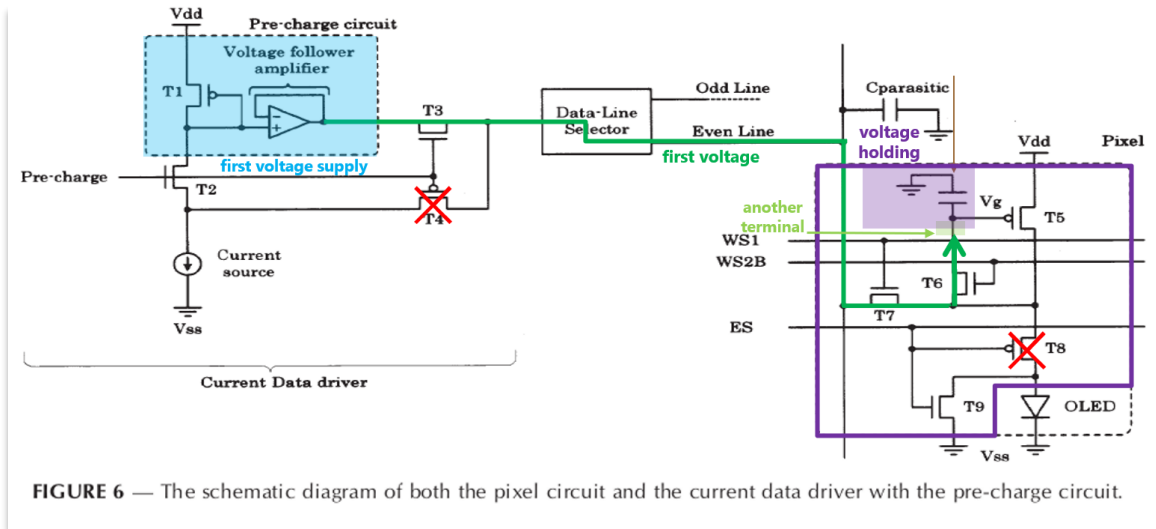


Ex. 1004 (Shimoda) at Fig. 7 (annotated). With reference to Figure 7, Shimoda describes the pre-charge period as follows:

A single horizontal period contains both the pre-charge and current-programming periods. In the pre-charge period, T2 and T3 are turned on, T4 is turned off, and current from the current source flows into T1. A voltage-follower amplifier outputs the gate voltage of T1 into the gate electrode of T5, with T6 and T7 turned on. This pre-charge function rapidly pre-charges the voltage in the gate electrode of T5 so that a current roughly equivalent to the value of the current source flows through T5.

Ex. 1004 (Shimoda) §3.2.

120. The pre-charge operation mode is shown below, with a red × placed over the transistor lines that are turned off. As shown in Figure 6, during the pre-charge period (the claimed “voltage supply mode”), a gate capacitor (part of the claimed “voltage-holding circuit,” annotated purple) in each of the pixel circuits (the claimed “current output circuits,” within the purple box) receives a voltage (the claimed “first voltage,” annotated green) from the pre-charge circuit (the claimed “first voltage supply source,” annotated blue). Figure 6 further shows the first voltage is supplied to another terminal (annotated light green) as claimed.



Ex. 1004 (Shimoda) at Fig. 6 (annotated).

121. During the pre-charge period, the first voltage from the pre-charge circuit is also supplied to “another terminal of said voltage holding circuit.” As described above, the gate capacitor is an example of a voltage holding circuit. In the pre-charge period, the gate capacitor is connected to the pre-charge circuit and is thus supplied by the first voltage. *See, e.g.*, Ex. 1004 (Shimoda) at §3.2 (describing that during the pre-charge period, T3 is turned on, T4 is turned off, T6 is turned on, and T7 is turned on, thus connecting the pre-charging circuit to the pixel circuit). Therefore, during the pre-charge period, the output of the pre-charge circuit is supplied to the lower terminal of the gate capacitor (i.e., the claimed “another terminal of said voltage-holding circuit”). *See* Ex. 1004 (Shimoda) at §3.2 (“[a] voltage-follower amplifier outputs the gate voltage of T1 into the gate electrode of T5, with T6 and T7 turned on”). Shimoda explains that “[t]his pre-charge function

rapidly pre-charges the voltage in the gate electrode of T5 so that a current roughly equivalent to the value of the current source flows through T5.” Ex. 1004 (Shimoda) §3.2.

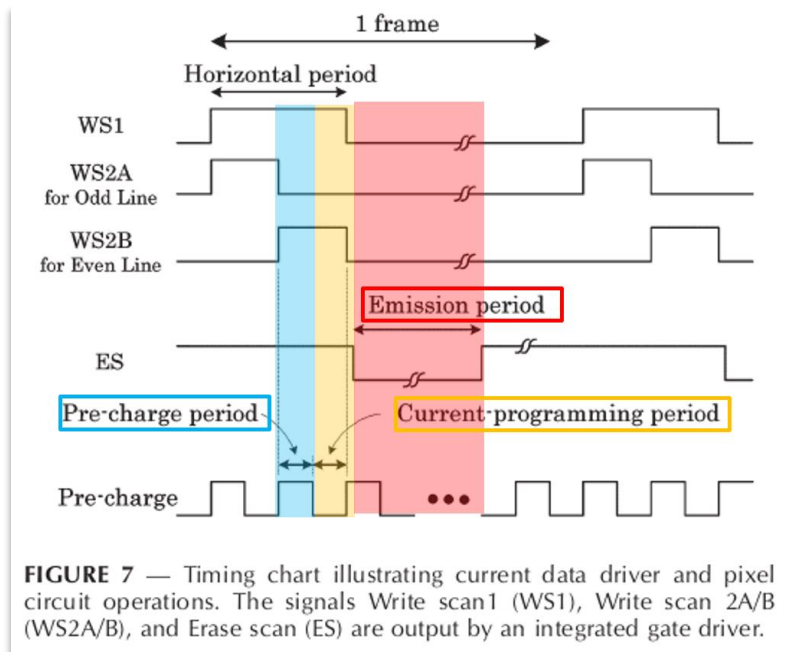
122. By way of confirmation of my analysis, similar to Shimoda, the '047 Patent explains that, under a voltage supply mode, the voltage holding capacitor is connected to the voltage supply source. Ex. 1001 ('047 Patent) at 7:44-48 (“the high-speeding switch Sw3 is set to a conductive state, so that the voltage supply source V1 and the node N2 are connected”). The capacitor C1 is then charged by the first voltage from voltage supply source. Ex. 1001 ('047 Patent) at 7:48-52 (“the voltage holding capacitance element C1 is charged to a constant voltage (this corresponds to the first voltage, and will be referred to as a reference voltage hereinafter) that is supplied from the voltage supply source V1”).

- i. **1(g): “under said current supply mode, each of said current output circuits receives said first current from said first current supply source, and generates a second voltage by said current-voltage converting circuit, and the first current is supplied to said another terminal of said voltage holding circuit, and”**

123. Shimoda discloses this limitation, providing operation under a current supply mode, including during a current-programming period.

- i. **“under said current supply mode, each of said current output circuits receives said first current from said first current supply source”**

124. The current-programming period can be seen as a portion of a horizontal period in Figure 7, annotated below in gold.



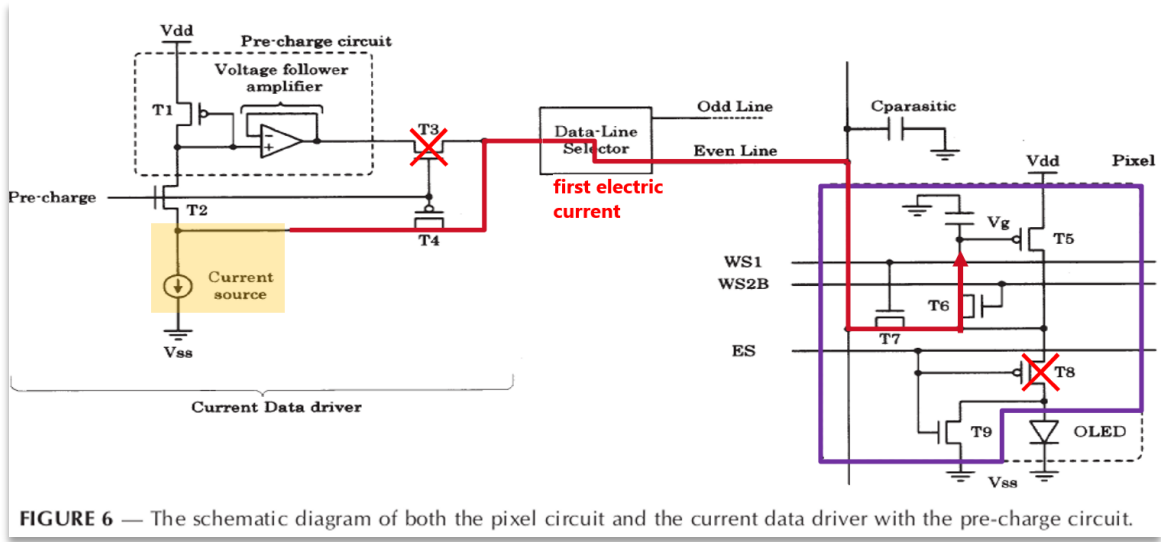
Ex. 1004 (Shimoda) at Fig. 7 (annotated). With reference to Figure 7, Shimoda describes the current-programming period as follows:

A single horizontal period contains both the pre-charge and current-programming periods. ... In the subsequent current-programming period, T4 is turned on, T2 and T3 are turned off, the pre-charge circuit is disconnected, and the current from the current source is directly supplied to the pixel circuit. While a pre-charge error may be generated if there exist variations in characteristics between T1 and T5, or if there is an offset voltage in the voltage-follower amplifier, this error can be compensated for during current-programming periods. Setting the current from the current source high makes it possible to compensate for the greater pre-charge error that occurs during current-programming

periods. This improves the accuracy of current programming significantly.

Ex. 1004 (Shimoda) §3.2. To summarize, and as shown in the annotated Fig. 6 below, during the current-programming period: transistors T2 and T3 are turned off (disconnecting the pre-charge circuit), transistor T4 is turned on (connecting the current source to the pixel circuit). In the meantime, transistors T7 and T6 remain turned on, further connecting the current source to the gate capacitor. Thus, the output current of the current source is supplied to the lower terminal of the gate capacitor (i.e., the claimed “another terminal of said voltage holding circuit”). *See*, Ex. 1004 (Shimoda) §3.2 (“the current from the current source is directly supplied to the pixel circuit.”).

125. Figure 6 has been annotated to show that, under the current supply mode, the pixel circuits (the claimed current output circuits, annotated purple) receive the claimed first current (annotated red) from the claimed first-current supply source (annotated gold). In Figure 6, a red X is placed over the lines that are turned off:



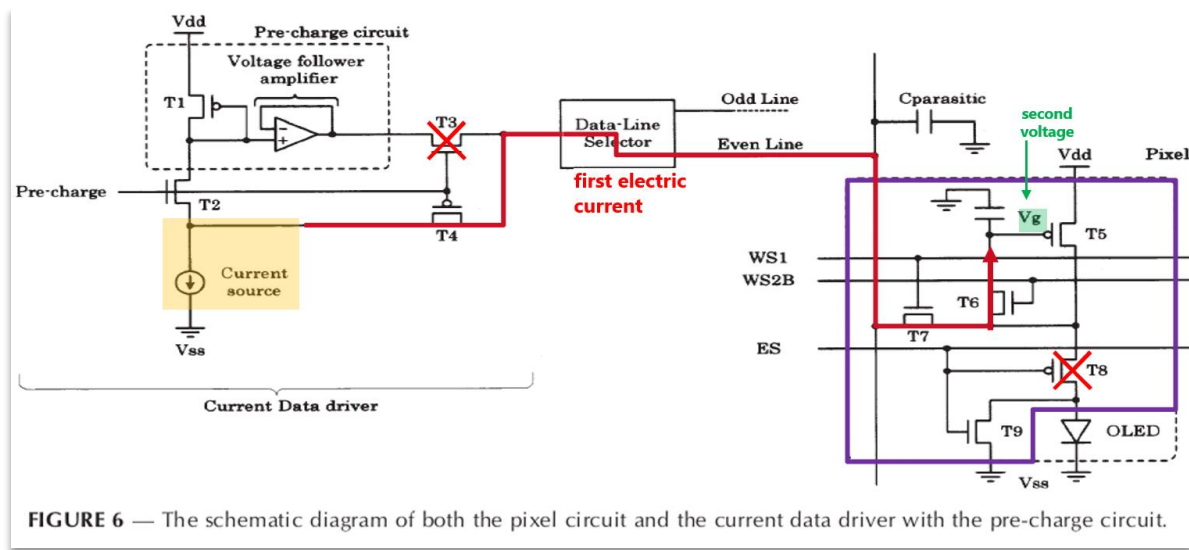
Ex. 1004 (Shimoda) at Fig. 6 (annotated). Thus, during a current-programming period (the claimed “current supply mode”), a gate capacitor within each pixel circuit (i.e., the claimed “current output circuit”) receives a current (the claimed “first current”) from the current source (the claimed “first current supply source”).

ii. “generates a second voltage by said current-voltage converting circuit”

126. During the current-programming period, a voltage (i.e., the claimed second voltage) is generated at the gate of transistor T5 and stored in the gate capacitor. During the current-programming period, a reference current from the current source (i.e., first electric current) continues to charge the capacitor after the capacitor was previously partially charged by the first voltage (during the pre-charge period). *See*, Ex. 1004 (Shimoda) §3.2, Fig. 8(a). The transistor T5 is configured to output a current in accordance with the gate voltage. By the end of the current-

programming period, the second voltage reaches a level where the transistor T5 outputs a current equivalent to the value of the first electric current. Ex. 1004 (Shimoda) §3.2, Fig. 8(a). Shimoda further explains the difference between the first voltage and the second voltage may exist because of “variations in characteristics between T1 and T5.” See, Ex. 1004 (Shimoda) §3.2 (“While a pre-charge error may be generated if there exist variations in characteristics between T1 and T5, or if there is an offset voltage in the voltage-follower amplifier, this error can be compensated for during current-programming periods.”).

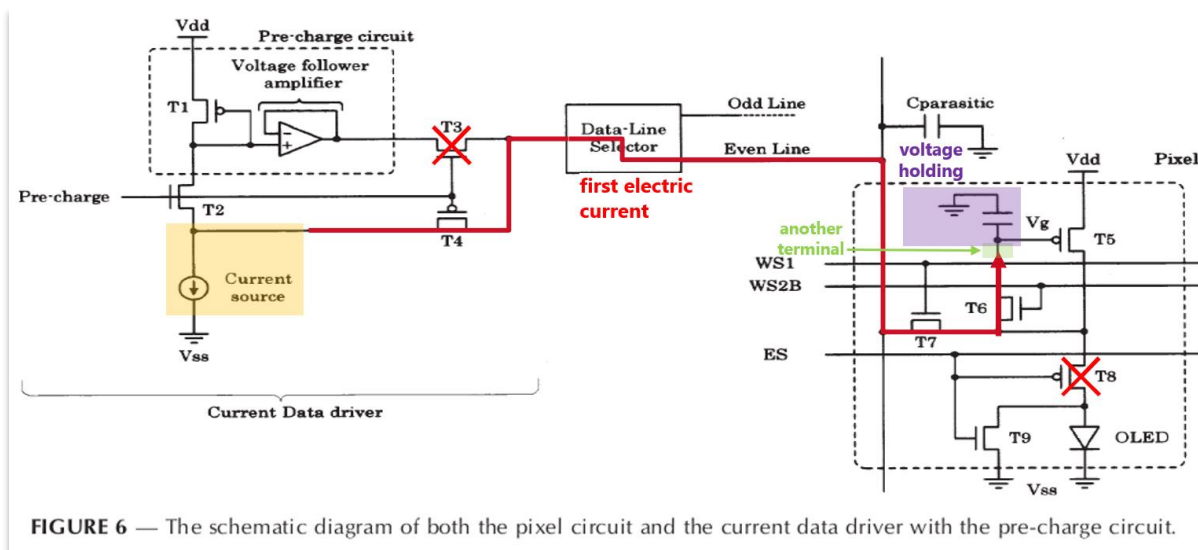
127. Figure 6 has been further annotated to show that, under the current supply mode, a second voltage is generated at the gate of transistor T5.



Ex. 1004 (Shimoda) at Fig. 6 (annotated).

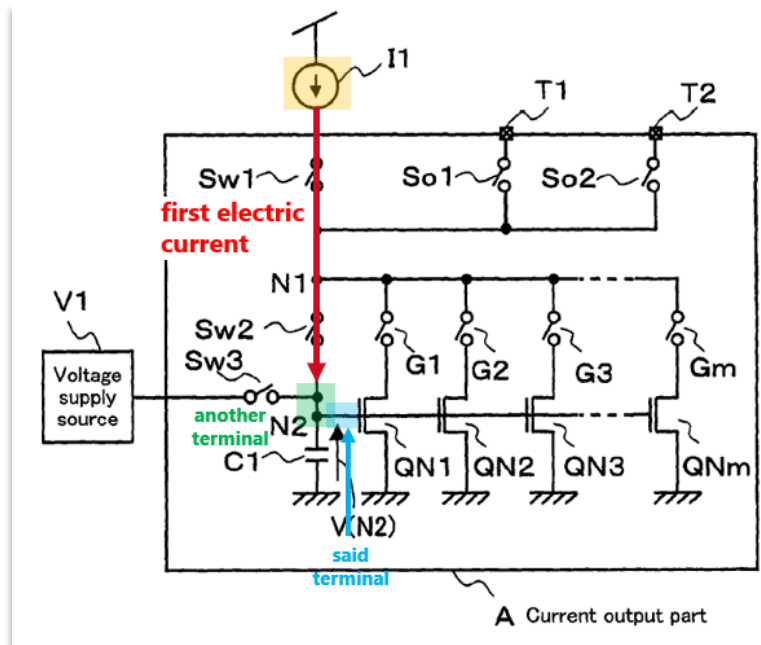
iii. “the first current is supplied to said another terminal of said voltage holding circuit”

128. As shown in the annotated Fig. 6 below, the first current from the current source is supplied to the “another terminal” (annotated in green), and from there to the gate capacitor. Ex. 1004 (Shimoda) §3.1, Fig. 6. The “another terminal” is part of the voltage holding circuit (purple).



Ex. 1004 (Shimoda) at Fig. 6 (annotated).

129. By way of confirmation of my analysis, similar to Shimoda, the '047 Patent explains that the first current is supplied to the second terminal of the voltage holding capacitor in a similar manner. Figure 1 of the '047 Patent is annotated to show that a first electric current is supplied to the marked “another terminal” of the voltage holding capacitor. Ex. 1001 ('047 Patent), 8:1-15.

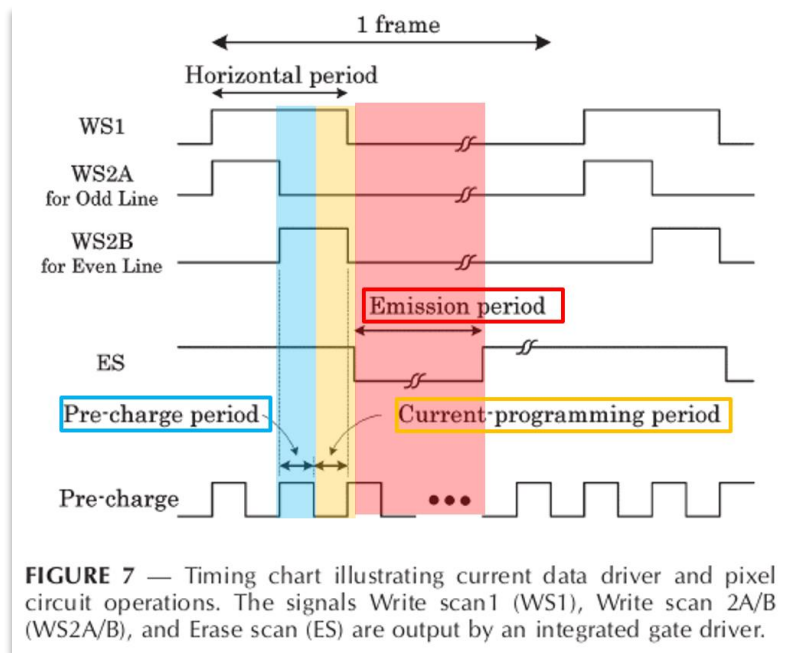


Ex. 1001 ('047 Patent) at Fig. 1A (annotated).

- j. **1(h): “under said current output mode, each of said current output circuits outputs an output current according to said voltage held in said voltage holding circuit by said voltage-current converting circuit.”**

130. Shimoda discloses this limitation, including during the emission period.

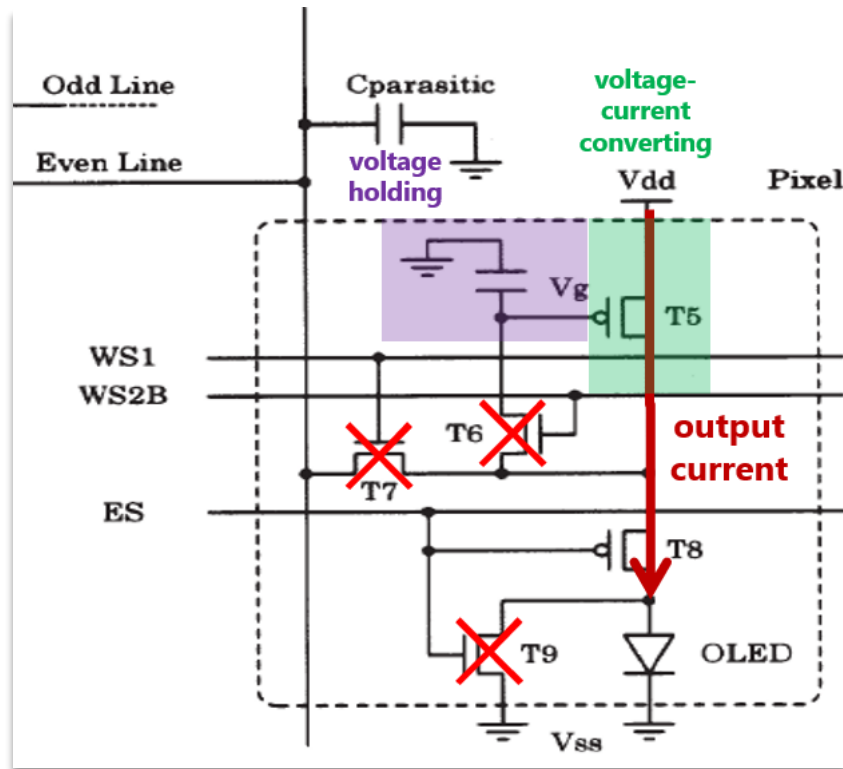
The emission period is when the pixel circuit outputs a current to a corresponding load OLED. The emission period can be seen in Figure 7, annotated in red below.



Ex. 1004 (Shimoda) at Fig. 7 (annotated). With reference to Figure 7, Shimoda describes the emission period as follows:

After the horizontal period, T6 and T7 are turned off, T8 is turned on, and a current programmed by the data driver is supplied to the OLED. The emission period is controlled by erase-scan signals which turn T8 and the reset TFT T9 on and off. Setting the emission period short makes it possible to set the current of the current source high enough to obtain the same average brightness over successive frame periods.

Ex. 1004 (Shimoda) §3.2. This operation mode is shown below, with a red × placed over the transistor lines that are turned off.



Ex. 1004 (Shimoda) at Fig. 6 (annotated and excerpted). As shown in the annotated Fig. 6 above, transistors $T7$ and $T6$ are turned off during the emission period, thus disconnecting the pre-charge circuit and the current source from the gate capacitor. The voltage held at the gate capacitor is then supplied to the gate electrode of transistor $T5$. A POSITA would have recognized that one of the fundamental properties of a transistor is that it outputs a current in accordance with its gate voltage. Transistor $T5$ then outputs a current according to its gate voltage. Thus, during the emission period, each pixel circuit outputs an output current (annotated dark red) according to the voltage held in the gate capacitor (the claimed “voltage

holding circuit,” annotated purple) by the transistor T5 (the claimed “voltage-current converting circuit,” annotated green).

B. CLAIMS DEPENDING FROM CLAIM 1 OF THE '047 PATENT

- a. **“2. The current driving device according to claim 1, wherein: each of said output terminals is connected to said current output terminals provided to said plurality of said current output circuits, and each of said plurality of current output circuits is connected in parallel to said first current supply source and said first voltage supply source used in common.”**

131. Shimoda discloses, or at least renders obvious, this claim.

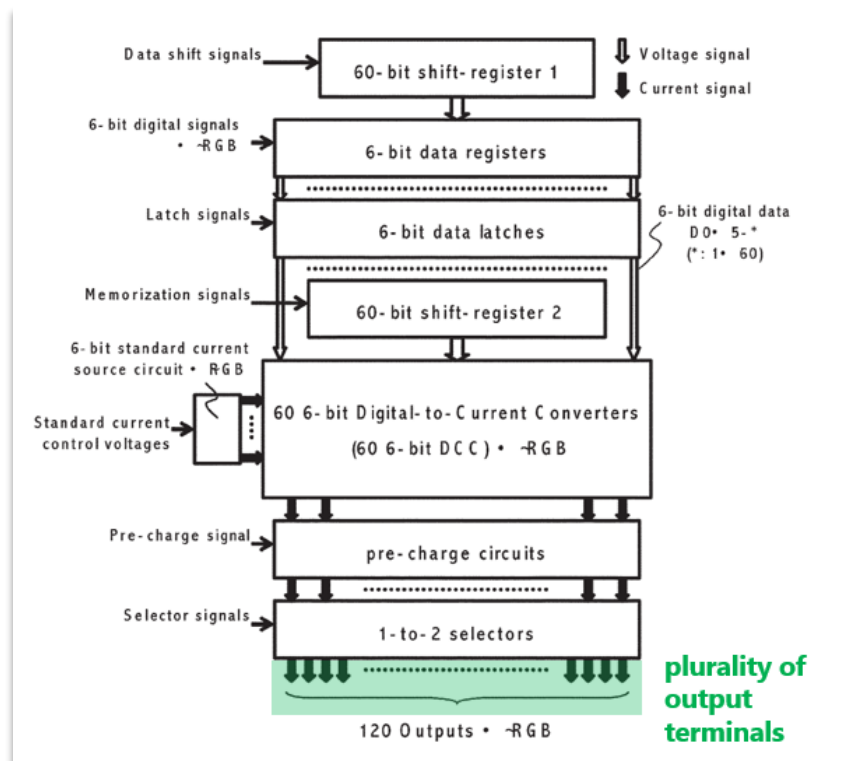
- i. **“each of said output terminals is connected to said current output terminals provided to said plurality of said current output circuits”**

132. Shimoda discloses “said current output terminals provided to said plurality of said current output circuits.” As described above for Claim Limitations 1(d)(1) and 1(d)(2), each pixel circuit is an example of a current output circuit. As also described above for Claim Limitations 1(d)(1) and 1(d)(2), a POSITA would have recognized (or at least it would have been obvious) that there would be a plurality of such pixel circuits present.

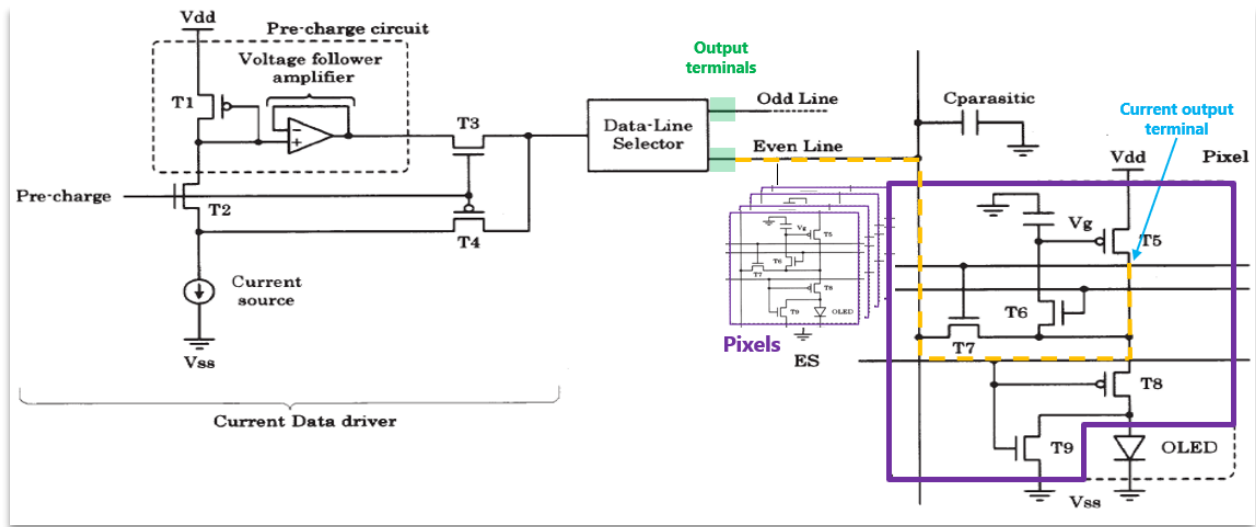
133. Transistors T5, each located within a corresponding pixel circuit, provide an example of current output terminals. As described above for Claim Limitation 1(c), Shimoda provides at least two examples of structure that constitutes

a plurality of output terminals. Under either example, Shimoda discloses “each of said output terminals is connected to said current output terminals.”

134. First, as described above for Claim Limitation 1(c), the output terminals following the 1-to-2 selectors in Figure 1 (annotated green) are an example of the claimed output terminals.



Ex. 1004 (Shimoda) at Fig. 1. Under this example, each output terminal is connected to the drain terminal of transistor T5 (the claimed current output terminal, annotated blue) as indicated by the yellow dash line in Figure 6.



Ex. 1004 (Shimoda) at Fig. 6 (annotated). The figure has been annotated to add multiple pixel circuits.

135. In Shimoda, each line (either even or odd) is connected with multiple pixels (as described above for Claim Limitation 1(d)(1)). Shimoda explains that a display using the current data drivers and pixel circuits would include a pixel count of “120×RGB×136.” Ex. 1004 (Shimoda) §5 (Table 1). Thus, the display in Shimoda would include an array of 120×136 pixels. Accordingly, a POSITA would have recognized that each line is connected to 136 pixels. Therefore, each output terminal is connected to a plurality of drain terminals of T5 (the claimed “current output terminals”) provided to current output circuits (the claimed “current output circuits”).

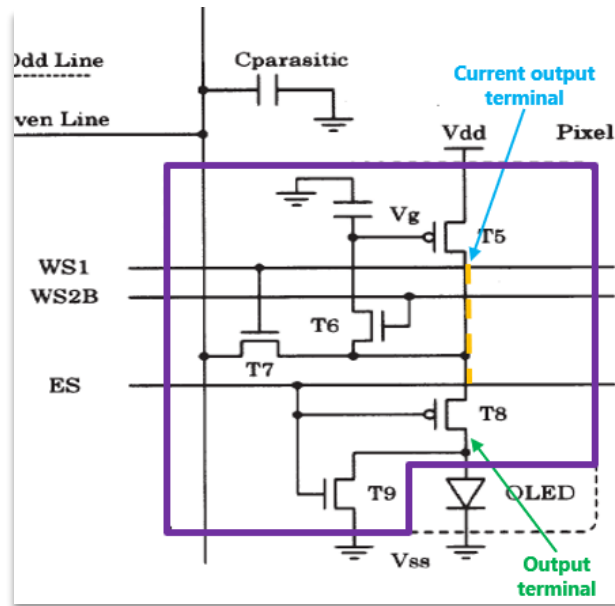
TABLE 1 — Display specifications.

Display size	1.9 in.
Pixel count	120 × RGB × 136
Pixel pitch	96 ppi
Peak luminance	>150 cd/m ²
Input data	Digital 6 bit × RGB
Input level	3 V I/F
Integrated circuits	Current data driver
	Gate driver
	Level shifter

Ex. 1004 (Shimoda) at Table 1 (annotated).

136. Second, as described above for Claim Limitation 1(c), the drain terminals of transistor T8 are another example of the claimed output terminals. Ex. 1004 (Shimoda) §3.2. As shown in Figure 6 below, the drain terminal of transistors T8 (the claimed “output terminals,” annotated green) are connected to the drain terminal of transistors T5 (the claimed “current output terminals,” annotated blue) provided to pixel circuits (the claimed “current output circuits,” annotated purple).

Ex. 1004 (Shimoda) at Fig. 6.



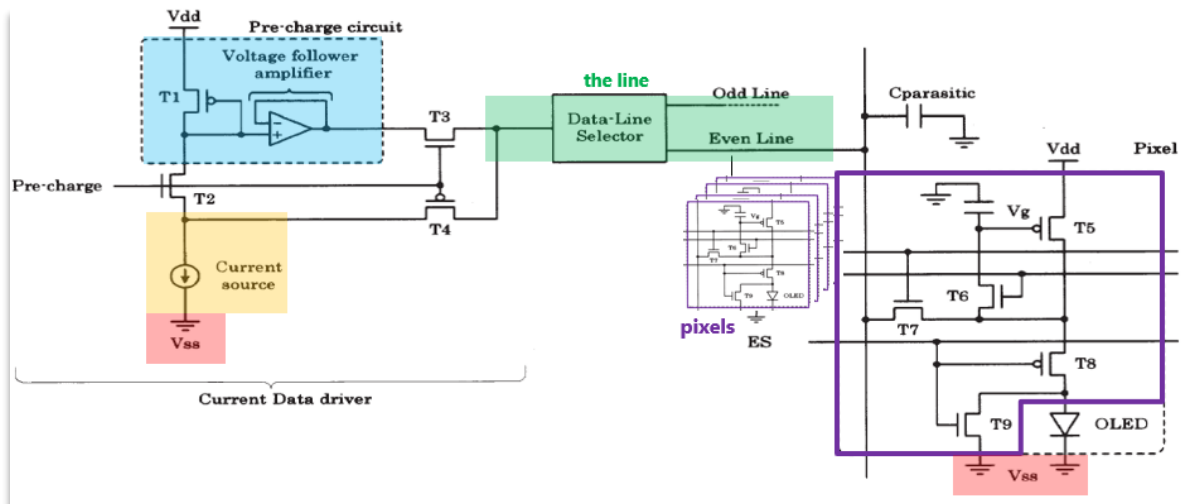
Ex. 1004 (Shimoda) at Fig. 6 (annotated and excerpted).

- ii. **“each of said plurality of current output circuits is connected in parallel to said first current supply source and said first voltage supply source used in common.”**

137. Shimoda discloses this element or at least renders it obvious. In both examples discussed for Claim Limitation 1(c), the pixel circuits are connected in parallel to said first current supply source and said first voltage supply source used in common. As indicated in the annotated Fig. 6 below, each of the pixel circuits share V_{ss} in common (annotated red). In addition, each of the pixel circuits are interposed on an even line (or an odd line), and a POSITA would have recognized (or at least it would have been obvious) that each line (whether even or odd) provides an equal voltage for all pixels interposed on that line. A POSITA would have recognized this fact for all pixels on the line, because a line in a circuit is equivalent

to a common node for the purpose of analyzing parallel or series connection. Thus, all pixel circuits on an even line (or all pixels on an odd line) share two common terminals—the line and Vss—and are thus in parallel with one another.

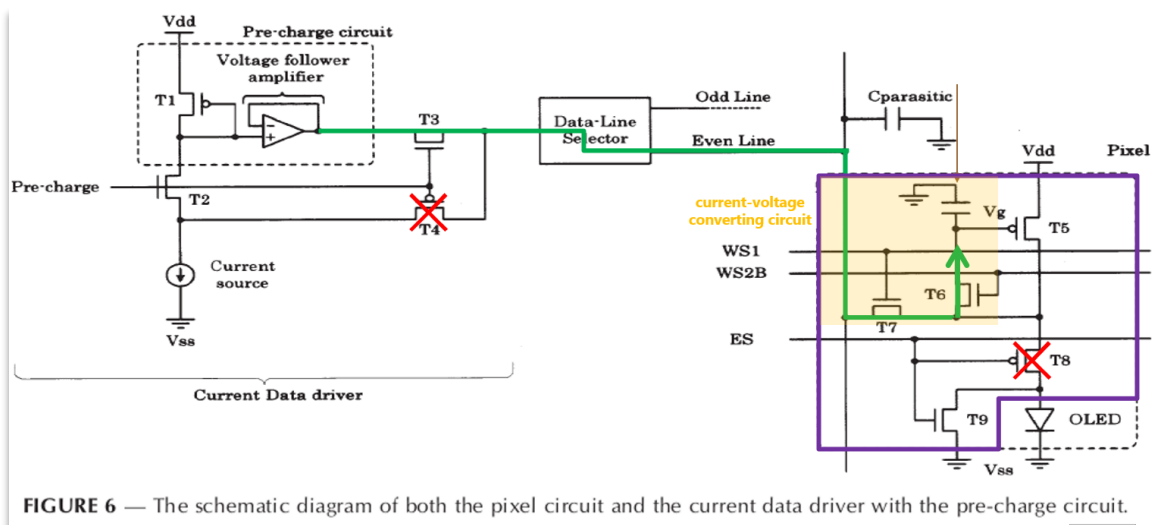
138. The pre-charge circuit (voltage source) and the current source are also interposed between the even line (or the odd line) and Vss. Ex. 1004 (Shimoda) §3.1, Fig. 6. A POSITA would have recognized that the data-line selector is essentially a collection of switches. When an even line (or an odd line) is selected, for example, the voltage supply and current supply are directly connected to the even line (or the odd line). Under this condition, the current supply, the pre-charge circuit, and the pixels of even line (or odd line) share a common node (e.g. the even or odd line). Therefore, Shimoda discloses the current output circuits are connected in parallel to the current supply and the first voltage supply source as claimed.



Ex. 1004 (Shimoda) at Fig. 6 (annotated).

- b. **“3. The current driving device according to claim 1, wherein, in each of said current output circuits, said current-voltage converting circuit is actuated under said voltage supply mode.”**

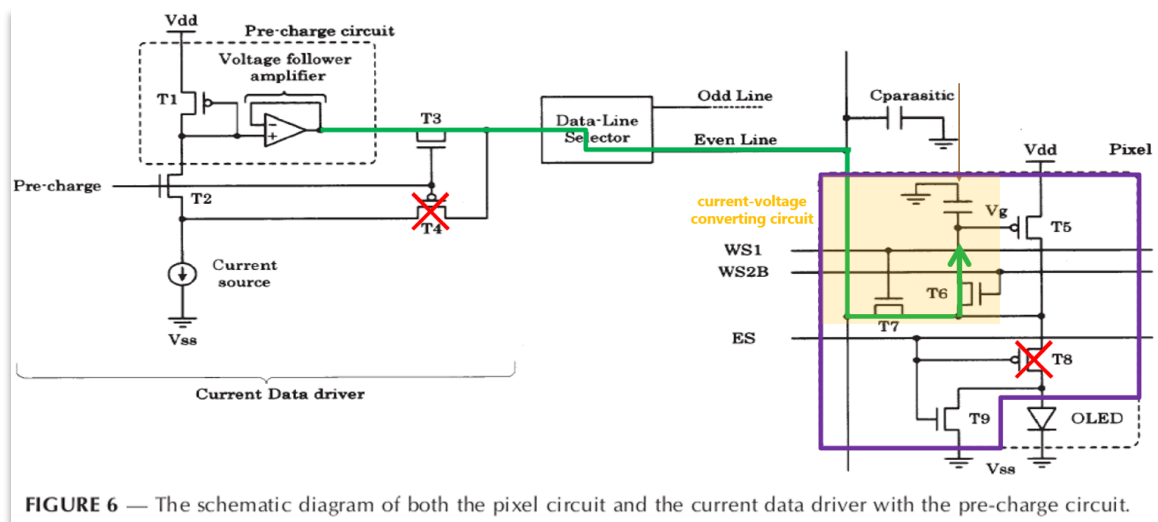
139. Shimoda discloses this claim. As discussed above for Claim Limitation 1(d)(2), a current-voltage converting circuit comprises an input terminal connected to the current supply source, transistors T6-T7, and gate capacitor. As shown in Figure 6, the circuit is actuated during the pre-charge period (the claimed “voltage supply mode”) because all components of the current-voltage converting circuit (annotated gold) are set to a conductive state. *See*, Ex. 1004 (Shimoda) §3.2, Fig. 6. The current-voltage converting circuit (annotated gold) is shown below, with a red × placed over the transistor lines that are turned off and a green arrow indicating that a voltage being supplied to the gate capacitor.



Ex. 1004 (Shimoda) at Fig. 6 (annotated).

- c. **“4. The current driving device according to claim 1, wherein each of said current output circuits is configured to stop said current-voltage converting circuit under said voltage supply mode.”**

140. Shimoda discloses, or at least renders obvious, this claim limitation. As shown in Figure 6 below, the transistor T4 is turned off during a pre-charge period (the claimed “voltage supply mode”). Ex. 1004 (Shimoda) at Fig. 6, §3.2. During the pre-charge period, the current-voltage converting circuit is stopped from converting a current into a gate voltage for the gate capacitor because the current supply source is disconnected from the gate capacitor (on account of transistor T4 being turned off), and a voltage from the pre-charge circuit is supplied directly to the gate capacitor. Ex. 1004 (Shimoda) §3.2. The current-voltage converting circuit (annotated gold) is shown below, with a red X placed over the transistor lines that are turned off and a green arrow indicating a voltage supplied to the gate capacitor.



Ex. 1004 (Shimoda) at Fig. 6 (annotated).

- d. **“9. A current-driving-type display device, comprising said current driving device according to claim 1 mounted thereon so as to be driven by said current driving device.”**

141. Shimoda discloses this element. Each of the active-matrix organic light-emitting diode (AMOLED) displays in Shimoda is an example of the claimed “current-driving-type display device.” Ex. 1004 (Shimoda) at Abstract (“an integrated poly-Si TFT current data driver with a data-line pre-charge function for active-matrix organic light-emitting diode (AMOLED) displays”). The AMOLED displays in Shimoda are current-driving-type displays because the displays are driven by current data drivers mounted thereon, and because the “brightness is dependent on the current in the OLED that is driven by each pixel circuit.” Ex. 1004 (Shimoda) §1 (emphasis added). Thus, Shimoda seeks “to integrate high-accuracy current data drivers into the AMOLED display substrate itself.” Ex. 1004 (Shimoda) §1.

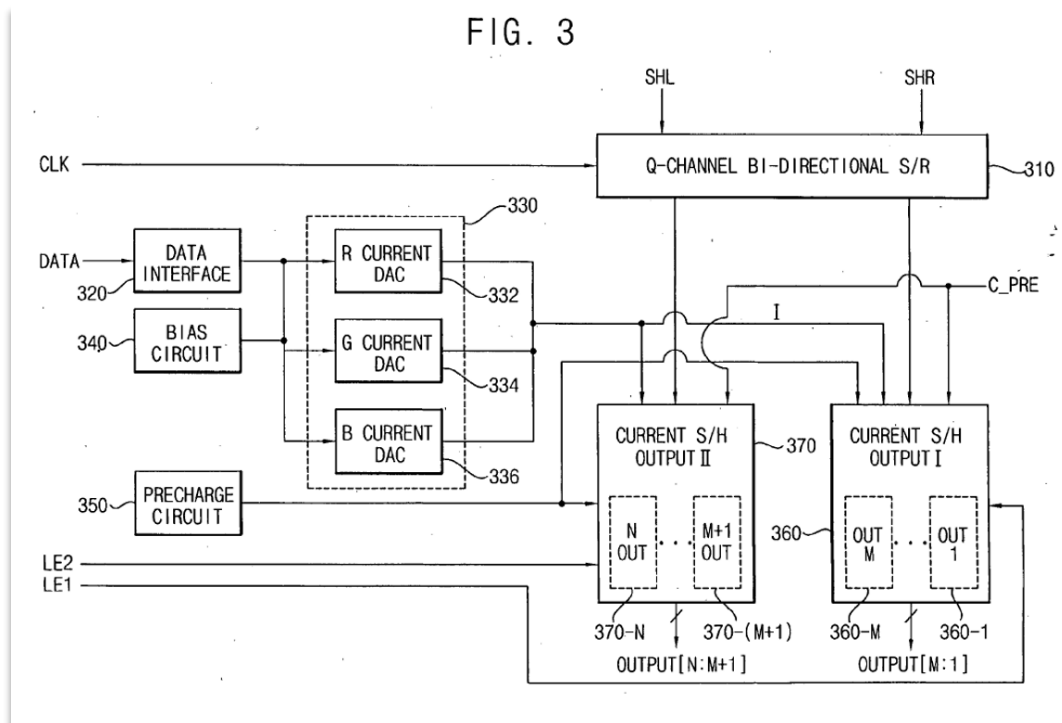
XIII. GROUNDS 3 & 4: BAEK

142. It is my opinion that Claims 1-4 and 9 of the '047 Patent are each anticipated by Baek (Ex. 1005), corresponding to Ground 3. To the extent Patent Owner contends that any of these claims are not anticipated, then they would have been rendered obvious over Baek in view of the knowledge of a POSITA, corresponding to Ground 4.

A. INDEPENDENT CLAIM 1 OF THE '047 PATENT

a. 1(preamble): “A current driving device, comprising:”

143. To the extent the preamble is limiting, Baek discloses the preamble. The “display driver circuit” of Baek is an example of the claimed “current driving device,” and is shown in Figure 3 below.



Ex. 1005 (Baek) at Fig. 3; Ex. 1005 (Baek) at ¶[0026] (“FIG. 3 is a block diagram illustrating a display driver circuit). Baek discloses that the “display driver circuit may include a bidirectional shift register 310, a data interface circuit 320, a current digital-to-analog conversion unit 330, a bias circuit 340, a pre-charge circuit

350, a first current sample/hold output circuit 360, and/or a second current sample/hold output circuit 370.” Ex. 1005 (Baek) ¶[0036].

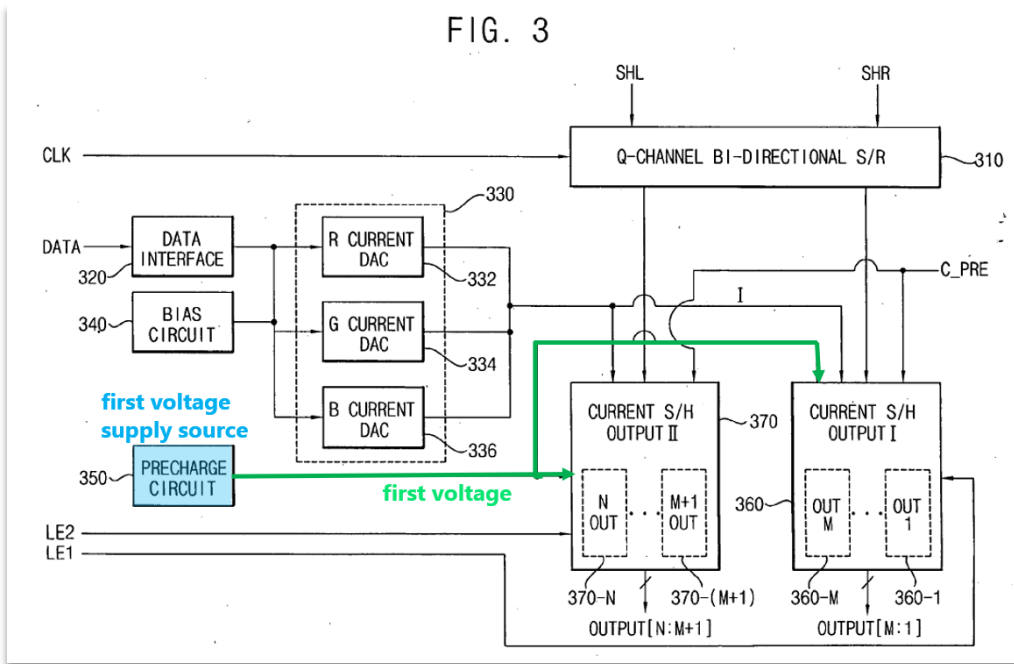
b. 1(a): “a first voltage supply source for supplying a first voltage;”

144. Baek discloses this limitation. The “pre-charge circuit” in Baek is an example of the claimed “a first voltage supply source.” The “pre-charge circuit 350” is a component of the “display driver circuit” discussed above. Ex. 1005 (Baek) ¶[0036] (“a display driver circuit may include ... a pre-charge circuit 350”). The pre-charge circuit supplies a voltage, which is an example of the claimed “a first voltage,” to a storage capacitor to reduce a charge time:

To further reduce a charge time, a fourth switch S4 may be turned on to pre-charge a voltage of the storage capacitor CST to a voltage level slightly lower than a threshold voltage of the first transistor M1 in response to the capacitor pre-charge signal C_PRE before the first switch S1 and the second switch S2 are turned on.”).

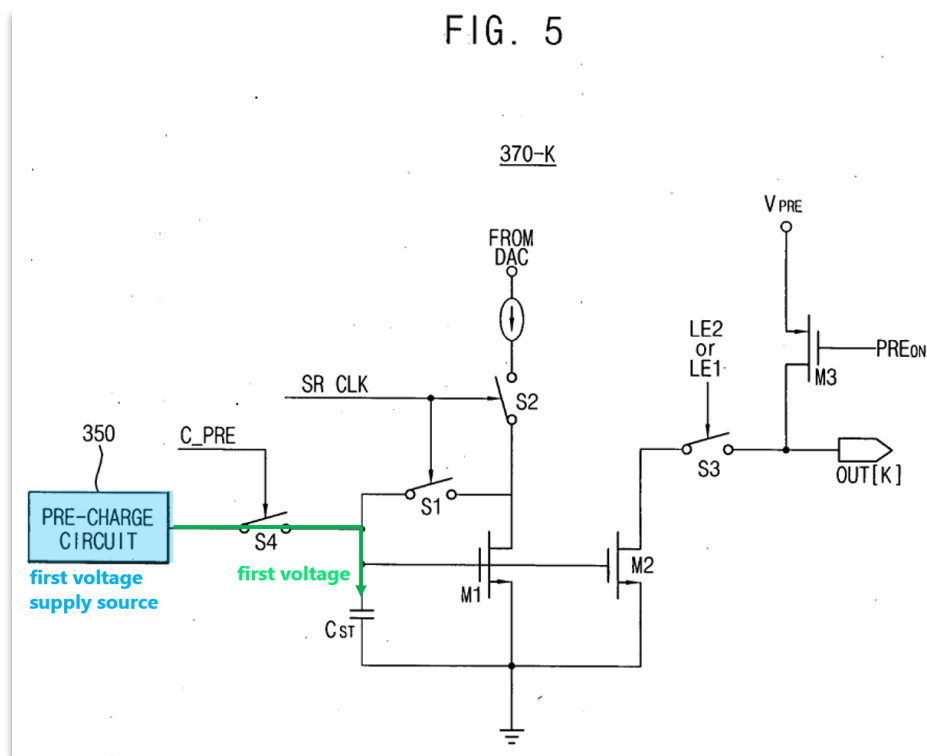
Ex. 1005 (Baek) ¶ [0062]. The pre-charge circuit is identified as item 350 in Figures 3 and 5 of Baek and is annotated in blue below. The storage capacitor is identified in Figure 5 as “CST,” and the lines along which the pre-charge circuit supplies “a first voltage” to the storage capacitor are annotated in green. These are illustrated in Figure 3 (showing the “display driver circuit”) and Figure 5, which provides an expanded view of the sample/hold circuit of Figure 3. Ex. 1005 (Baek) ¶¶[0026], [0028], [0055].

FIG. 3



Ex. 1005 (Baek) at Fig. 3 (annotated).

FIG. 5



Ex. 1005 (Baek) at Fig. 5 (annotated).

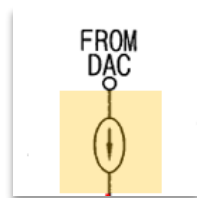
c. **1(b): “a first current supply source for supplying a first electric current;”**

145. Baek discloses this limitation. The current digital-to-analog conversion unit 330 (“DAC”) in Baek is an example of the claimed “a first current supply source.” Baek describes the current DAC as a component of the display driver circuit:

Referring to FIGS. 3 and 4, a display driver circuit may include a bidirectional shift register 310, a data interface circuit 320, a current digital-to-analog conversion unit 330 [(“DAC”)], a bias circuit 340, a pre-charge circuit 350, a first current sample/hold output circuit 360, and/or a second current sample/hold output circuit 370.

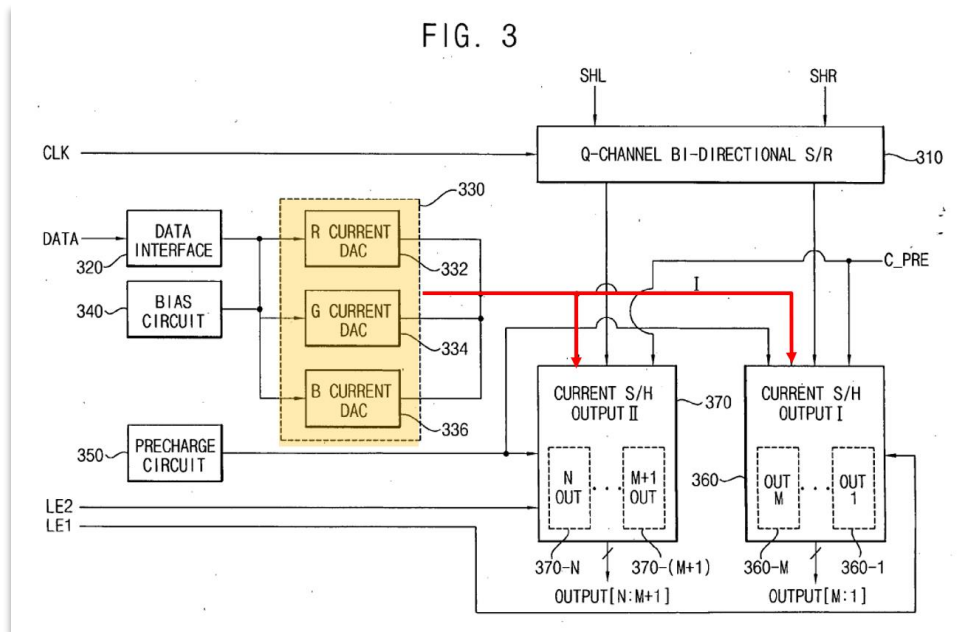
Ex. 1005 (Baek) ¶[0036] (emphasis added); Fig. 3. As its name indicates, a current DAC is a component that takes input digital data and converts it to an analog current.

Ex. 1005 (Baek) ¶[0044] (“The current digital-to-analog conversion unit 330 may convert gray-scale data provided from the data interface circuit 320 to an analog gray-scale current based on the gamma reference signal.”). Figure 5 of Baek confirms that the current DAC is an example of the claimed “current supply source,” because the signal from DAC is represented by a current source symbol.

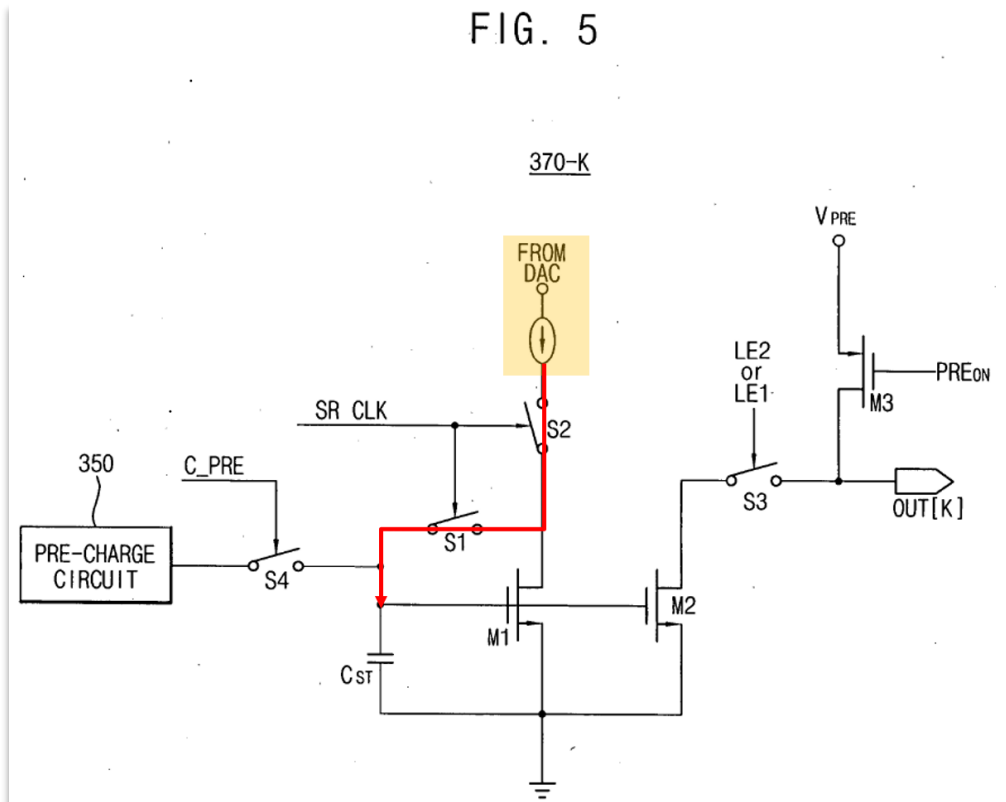


Ex. 1005 (Baek) at Fig. 5 (excerpted and annotated). As shown in Figure 5, this analog gray-scale current is supplied to each sample/hold output circuit (identified as “Current S/H Output”), specifically to the storage capacitor CST and to a gate of the transistor M1. When CLK signal is set to high (discussed further in subsequent limitations), the current DAC supplies current and charges CST; once the voltage across the terminals of CST exceeds the threshold voltage of transistor M1, current passes through transistor M1. *See* Ex. 1005 (Baek) ¶¶[0046], [0056]; Fig. 5. The current that the current DAC supplies to CST is an example of the claimed “first electric current.”

146. The current DAC (the claimed “current supply source”) is shown in Figures 3 and 5 of Baek and is annotated in gold. The lines along which the “first electric current” are supplied are annotated in red.



Ex. 1005 (Baek) at Fig. 3 (annotated).



Ex. 1005 (Baek) at Fig. 5 (annotated).

d. 1(c): “a plurality of output terminals;”

147. Baek discloses limitation. The output terminals OUT[1]-OUT[N] in Baek are an example of the claimed “a plurality of output terminals,” and Baek even refers to each of them as an “output terminal.”

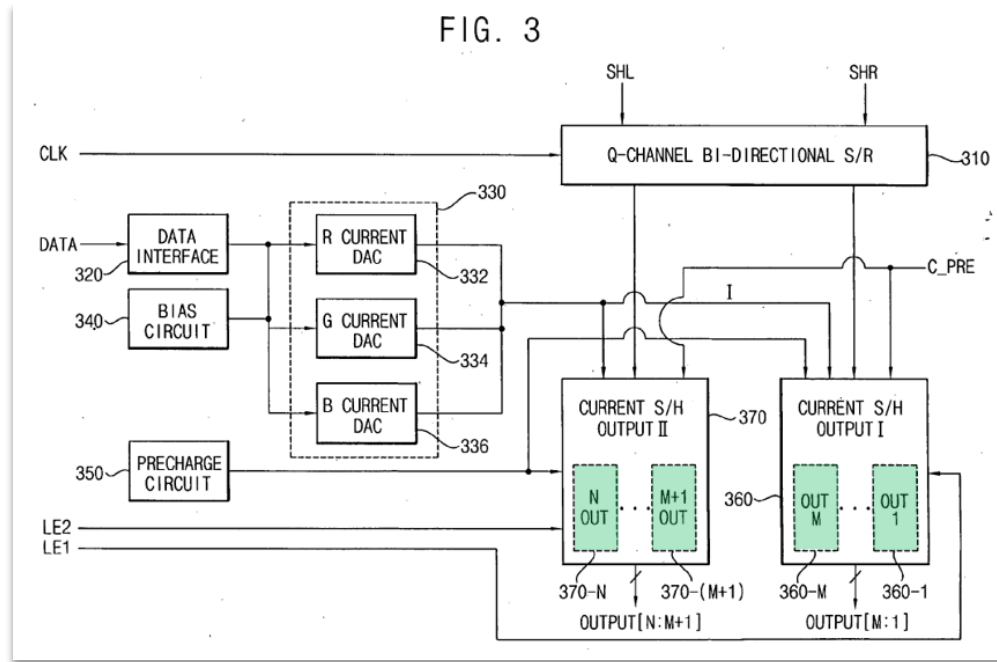
The output terminal OUT[K] may be used to drive a display panel (not shown) using a smaller current.

Ex. 1005 (Baek) ¶[0063]. The OUT[1]-OUT[N] notation is shorthand for indicating a multitude of output terminals—labeled terminal 1, terminal 2, terminal 3, ... terminal N—spread across current sample/hold circuit 360 and current sample/hold circuit 370. Within that multitude of terminals, Baek refers to an individual terminal as OUT[K]. Thus, the [1-N] is used in reference to the zoomed out view of Figure 3 of Baek to show a series of terminals, and the [K] is used in the zoomed in view of Figure 5 to show one individual terminal. In addition to referring to the series of terminals[1-N] as output terminals, Baek similarly refers to “OUT[K] as an “output terminal” in paragraphs [0058], [0061], and [0062]. “When the first latch enable signal LE1 or the second latch enable signal LE2 is activated, a third switch S3 may couple a drain of the second transistor M2 to an output terminal OUT[K].” Ex. 1005 (Baek) ¶[0058].

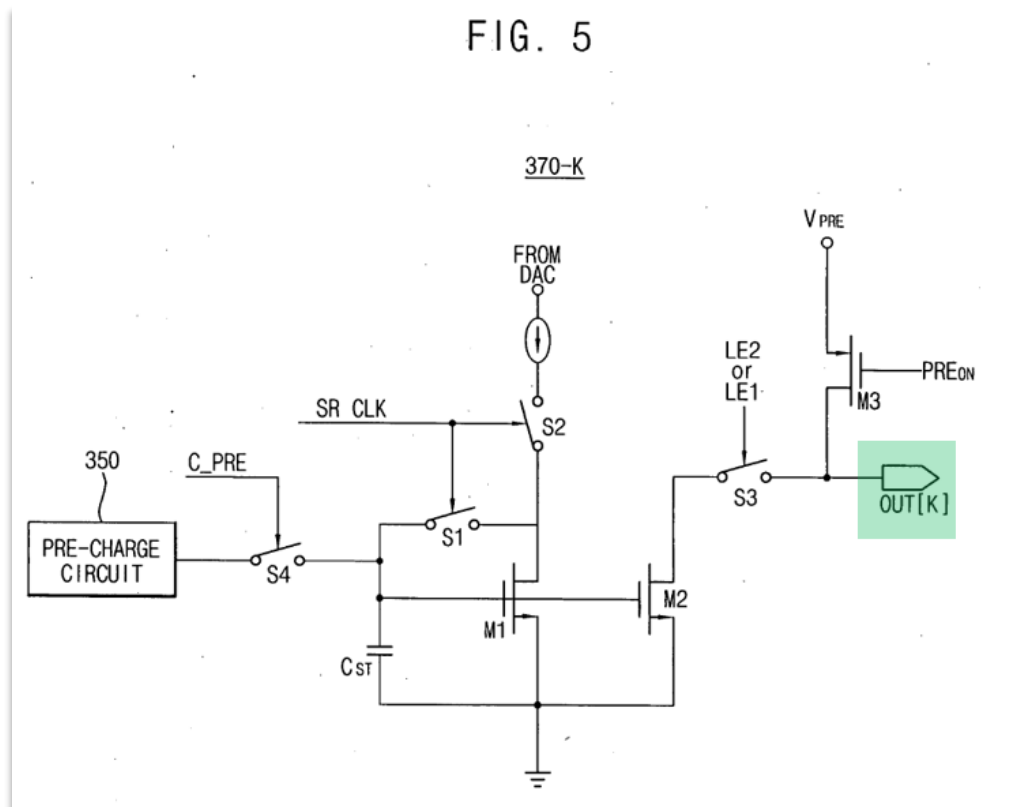
148. Each output terminal is associated with a corresponding current sample/hold circuit. For example, output terminal OUT[K], which is one of the output terminals of OUT[1] through OUT[N], is associated with current sample/hold circuit 370-K. Each of output terminal (e.g. OUT[K]) outputs an output signal (e.g., OUTPUT K) to a corresponding channel (e.g., channel K). As shown in Figure 3, the current sample/hold output circuit 360 comprises a plurality of sample/hold circuits 360₁ through 360_M (Baek does not use the subscript notation, and instead refers to the circuits as “360-1” through “360-M” in Figure 3). Similarly, current sample/hold output circuit 370 comprises a plurality of sample/hold circuits 370_{M+1} through 370_N (identified as “370-(M+1)” through “370-N”). Thus, Baek refers to OUT[1] through OUT[N] to refer to the output terminals spread across current sample/hold circuit 360 and current sample/hold circuit 370.

149. Baek discloses “[t]he first current sample/hold output circuit 360 may sample/hold the analog gray-scale current and may output signals OUTPUT 1 through OUTPUT M to the channels 1 through M.” Ex. 1005 (Baek) ¶[0045]. Baek further explains “when the first latch enable signal LE1 is activated, the output signals OUTPUT 1 through OUTPUT M may be activated to be output to the channels 1 through M” and “when the second latch enable signal LE2 is activated, the output signals OUTPUT M+1 through OUTPUT N may be activated to be output to the channels M+1 through N.” Ex. 1005 (Baek) ¶¶[0051], [0052]. The output

terminals Out[1]-Out[N] are shown in Figure 3 and a zoomed in view of output terminal OUT[K] is shown in Figure 5. The output terminals are annotated green.



Ex. 1005 (Baek) at Fig. 3 (annotated).



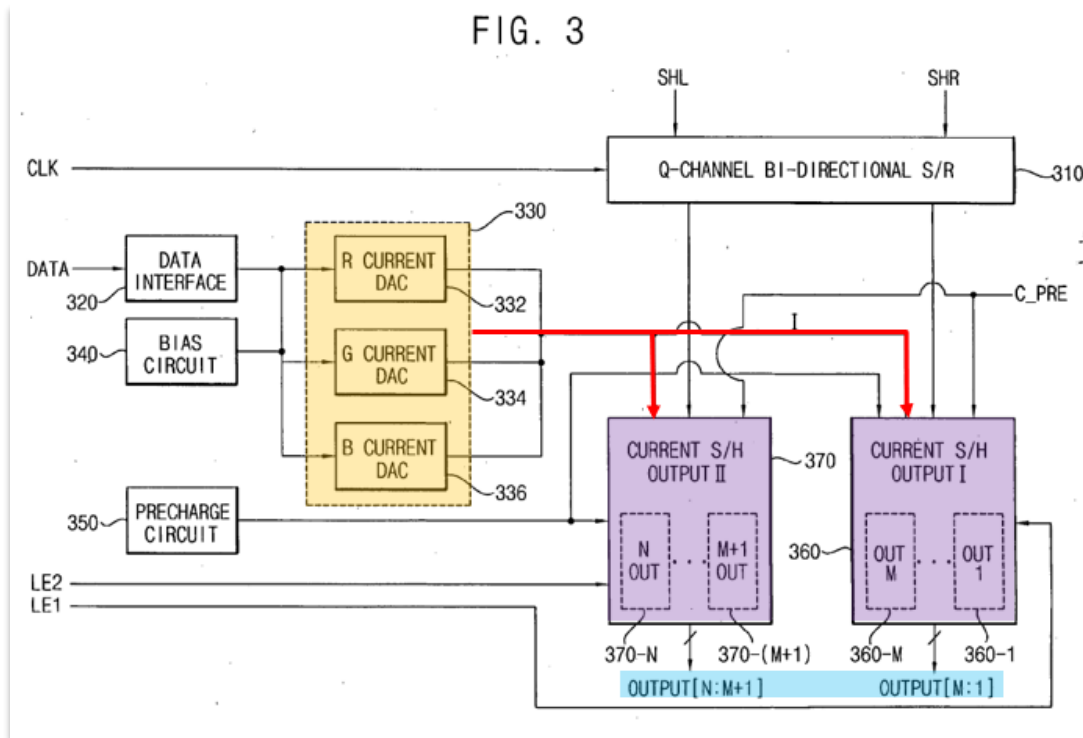
Ex. 1005 (Baek) at Fig. 5 (annotated).

- e. **1(d)(1): “and a plurality of current output circuits for outputting an electric current in accordance with said first electric current, each of said current output circuits comprising”**

150. Baek discloses this limitation. Baek discloses that “a display driver circuit may include . . . a first current sample/hold output circuit 360, and/or a second current sample/hold output circuit 370.” Ex. 1005 (Baek) ¶[0036]. Each of current sample/hold (S/H) output circuit 360 and current sample/hold output circuit 370 is an example of the claimed “current output circuit,” thus Baek discloses two or more (a plurality of) current output circuits.

151. The current sample/hold output circuits each output an electric current in accordance with said first electric current. As indicated by their name, the current sample/hold output circuits 360 and 370 sample and hold an analog gray-scale current (the claimed “first electric current,” which is discussed above for Claim Limitation 1(b)). Current sample/hold output circuit 360 also provides “output signals OUTPUT 1 through OUTPUT M to the channels 1 through M,” and current sample/hold output circuit 370 outputs signals “M+1 through N.” Ex. 1005 (Baek) ¶¶[0045], [0048]. The electric output signals from current sample/hold output circuits 360 and 370 are in accordance with the analog gray-scale current (“first electric current”). *See, e.g.*, Ex. 1005 (Baek) at claim 1 (stating that each “sample/hold output circuit” is “configured to provide the sample/hold analog gray-scale signal to a plurality of ... channels”); *see also* ¶[0061] (teaching that in some embodiments in which transistor M1 and M2 are of different size, the output current would be proportional to the input gray-scale current).

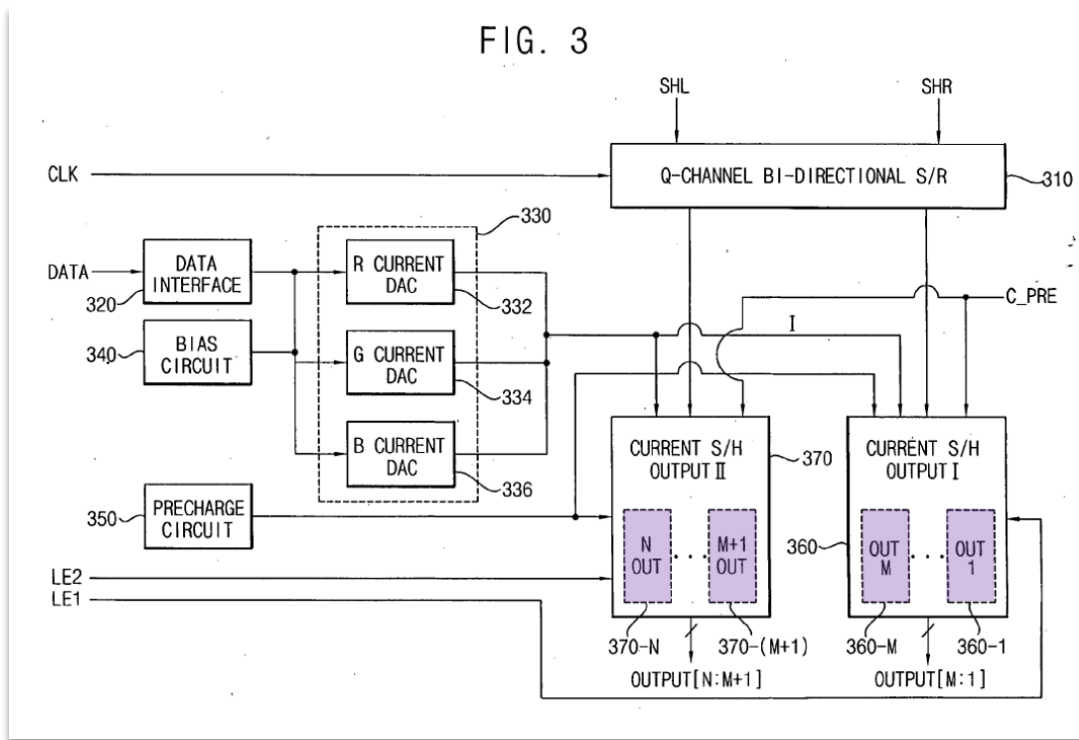
152. Current sample/hold output circuits 360 and 370 (the claimed “current output circuits”) are shown in Figure 3 of Baek and annotated in purple, with the input analog gray-scale current (the claimed “first electric current”) annotated in red and output signals (the claimed “an electric current”) annotated in blue.



Ex. 1005 (Baek) at Fig. 3 (annotated).

- f. **1(d)(2) “a current-voltage converting circuit, a voltage-current converting circuit, a voltage holding circuit having a terminal being connected to a reference voltage different from the first voltage, and at least one current output terminal, wherein”**

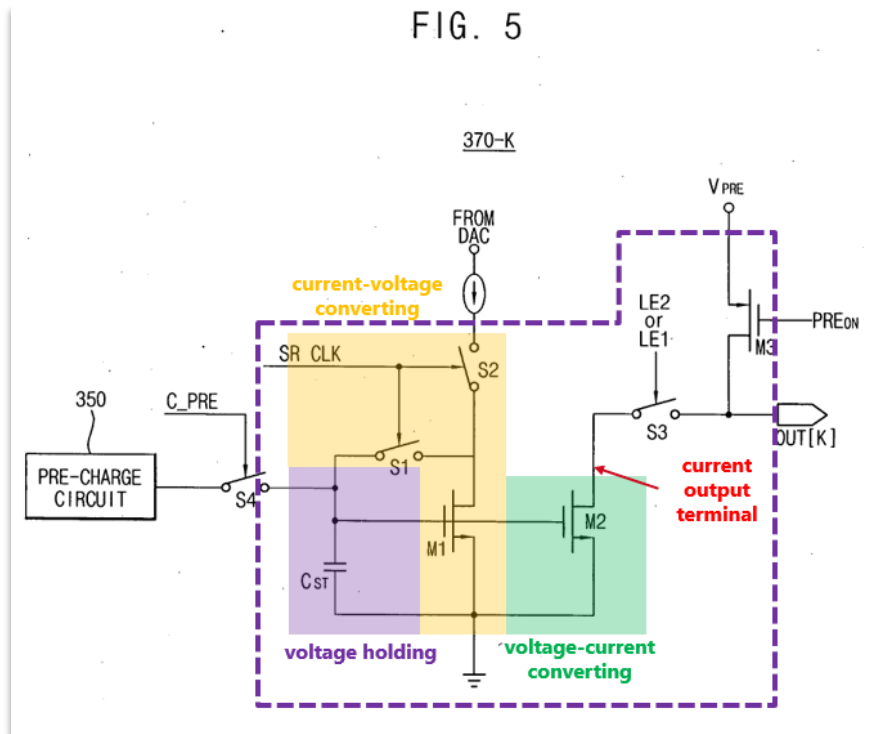
153. Baek discloses this limitation. As shown in Figure 3, current sample/hold output circuit 360 comprises M current sample/hold circuits (360₁–360_M, annotated purple) and current sample/hold output circuit 370 comprises (N–M) current sample/hold circuits (370_{M+1}–370_N, annotated purple).



Ex. 1005 (Baek) at Fig. 3 (annotated).

154. Figure 5 shows one such current sample/hold circuit 370_K, which is one of the current sample/hold circuits (within the set of 360₁–360_M) in Figure 3. Ex. 1005 (Baek) ¶[0028] (“FIG. 5 is a circuit diagram illustrating a current sample/hold circuit according to an example embodiment of the present invention.”). As shown in Figure 5 below, each current sample/hold circuit (such as current sample/hold circuit 370_K) includes within it circuits that are examples of the claimed “current-voltage converting circuit” (annotated gold), “voltage-current converting circuit” (annotated green), “voltage holding circuit having a terminal being connected to a

reference voltage different from the first voltage” (annotated purple), and “current output terminal” (annotated red). Ex. 1005 (Baek) at Fig. 5.

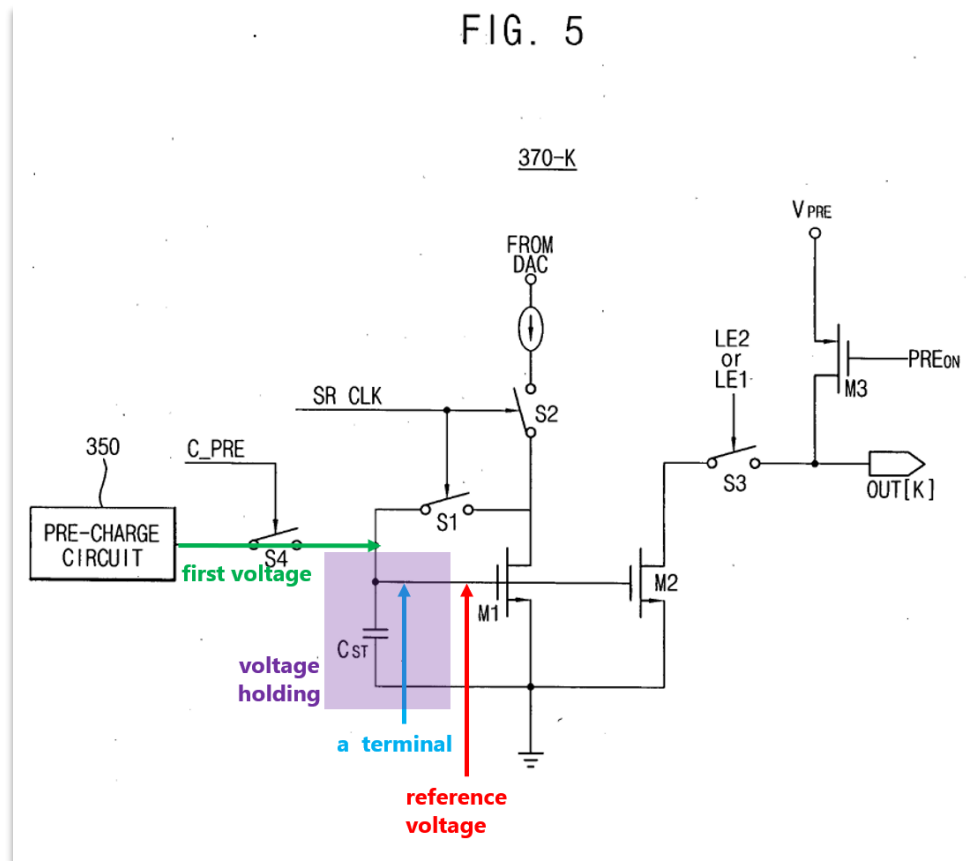


Ex. 1005 (Baek) at Fig. 5 (annotated).

- i. **“a voltage holding circuit having a terminal being connected to a reference voltage different from the first voltage”**

155. A storage holding capacitor C_{ST} is an example of the claimed “voltage holding circuit.” As shown in Figure 5 below, the storage capacitor C_{ST} (the claimed “voltage holding circuit,” annotated purple) has a terminal (annotated blue) connected to the gate of transistor $M1$, which supplies a reference voltage (annotated

red). The capacitor also has another terminal connected to the pre-charge circuit, which supplies the first voltage (annotated green).



Ex. 1005 (Baek) at Fig. 5 (annotated).

156. The storage capacitor C_{ST} is an example of the claimed “voltage holding circuit.” In Baek, the storage capacitor C_{ST} holds a voltage corresponding to the analog gray-scale current. Ex. 1005 (Baek) ¶[0057] (“the analog gray-scale current corresponding to the analog gray-scale current may be held in the storage capacitor C_{ST} ”). A POSITA would have recognized that the analog gray-scale

current is stored in the capacitor as a voltage, which is later applied to the gate of transistor M2.

157. Baek also discloses that the storage capacitor CST has the claimed “a terminal being connected to a reference voltage.” The storage capacitor CST is “coupled to the gate of the first transistor M1.” Ex. 1005 (Baek) ¶[0056]. The voltage at gate of transistor M1 is an example of the claimed “reference voltage.” As will be discussed further below, there are at least two charging modes in Baek: a pre-charge mode, under which a pre-charge signal (C_PRE) is activated; and a current charge mode, under which a corresponding clock signal (CLK) is activated. The voltage on the storage capacitor CST corresponds to the claimed “first voltage” during the pre-charge mode, and corresponds to the claimed “reference voltage” during the current charge mode. When a clock signal CLK is activated, switches S1 and S2 are closed (i.e., current flows) and the first electric current is applied to the gate and drain of transistor M1:

As a result, an analog gray-scale current output from a current digital-to-analog conversion unit 330 may be applied to a drain of the first transistor M1 via the second switch S2. At this time, because the first switch S1 is also turned on, the analog gray-scale current applied to the drain of the first transistor M1 may be applied to a gate of the first transistor M1.

Ex. 1005 (Baek) ¶[0056]. A POSITA would have recognized that, when a current is applied to a drain and a gate terminal of a transistor (such as transistor M1), the

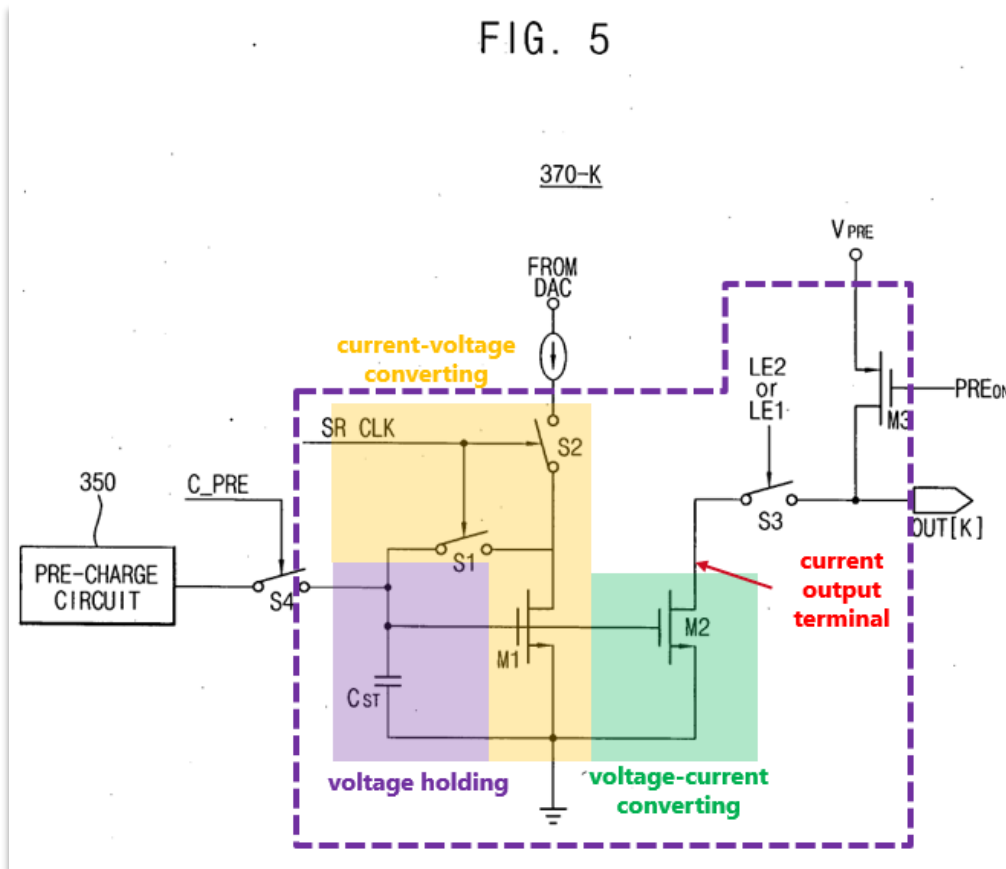
transistor behaves like a diode, accumulating a voltage at the gate and the drain of the transistor. This gate voltage on transistor M1 is thus an example of the claimed “reference voltage.”

158. The reference voltage is different than the first voltage provided by the pre-charge circuit. Baek discloses the pre-charge circuit may charge the storage capacitor CST to “a voltage level slightly lower than a threshold voltage of the first transistor M1.” Ex. 1005 (Baek) ¶[0062]. After the pre-charge period, a current from DAC (the claimed “first electric current”) continues charging the capacitor and thereby accumulates a different voltage at the gate of transistor M1 (the claimed “reference voltage”). Ex. 1005 (Baek) ¶¶[0056], [0062]. Further, a POSITA would have recognized that when current passes through M1, the gate voltage of transistor M1 is necessarily higher than its threshold voltage. One of the fundamental properties of a transistor is that current starts flowing through the transistor only when the gate voltage meets or exceeds a threshold voltage of the transistor. Therefore, the reference voltage is different from the first voltage.

ii. “a current-voltage converting circuit”

159. Baek discloses the claimed “current-voltage converting circuit.” Each current sample/hold circuit includes a circuit comprising switches S1 and S2 and transistor M1, which are an example of the claimed “current-voltage converting circuit.” The current-voltage converting circuit connects the current DAC (the

claimed “current source”) to the storage capacitor CST. This circuit converts the first electric current into a voltage stored at the storage capacitor CST. When a clock signal CLK is activated, the switches S1 and S2 are closed (current flows) and a reference voltage is generated at the gate of transistor M1, as described in the proceeding section. Ex. 1005 (Baek) ¶[0062]. This voltage is then stored in the storage capacitor. Ex. 1005 (Baek) ¶[0057] (“the analog gray-scale current corresponding to the analog gray-scale current may be held in the storage capacitor CST”).



Ex. 1005, Fig. 5 (annotated).

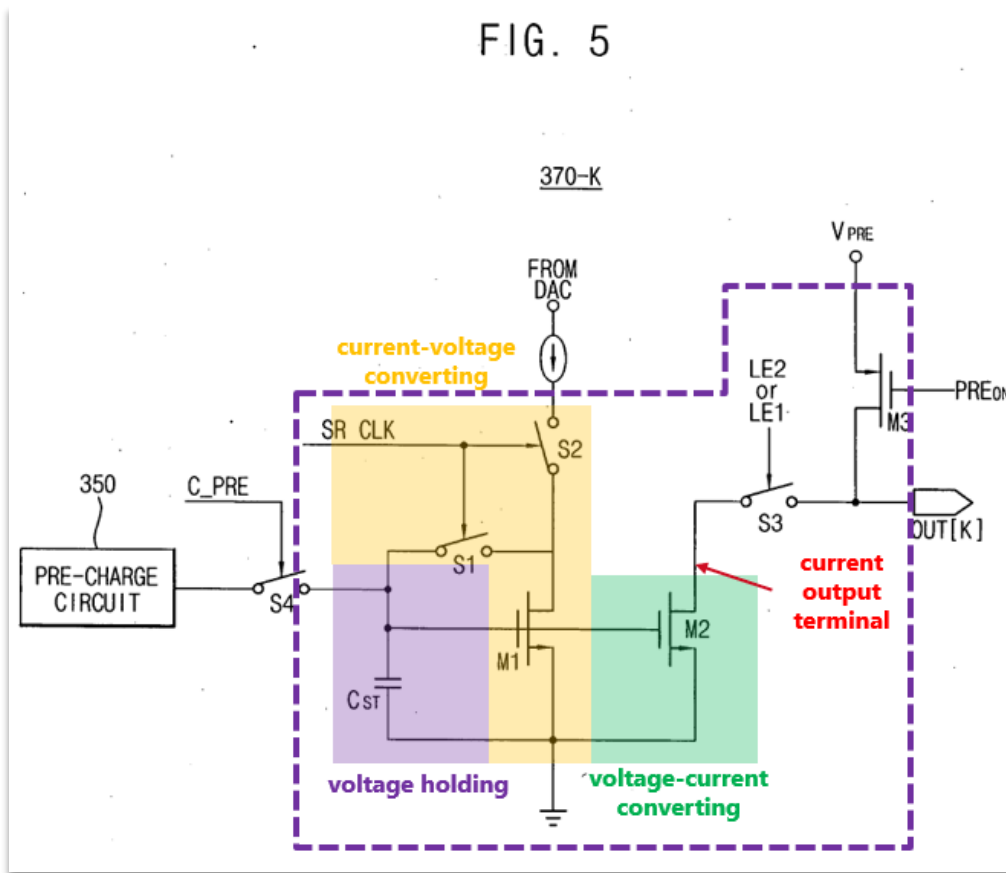
160. By way of confirmation of the analysis, the '047 Patent operates in the same manner as Baek. Under current supply mode, “a current-voltage converting function is actuated.” Ex. 1001 ('047 Patent) at 8:60-61. Switches Sw1, Sw2, and G1-Gm are set to be in a conductive state, connecting the current supply source to the voltage holding capacitor C1 and current-voltage converting elements QN1-QNm. Ex. 1001 ('047 Patent) at 8:61-64; 10:28-36; Fig. 1A. Similar to Baek, the reference voltage is generated at the gates of transistors QN1-QNm and held in the voltage holding capacitor C1:

Therefore, the Nch transistors QN1-QNm have an electric current (reference current) with a constant current value from the reference current source I1 flown therein as a load. At this time, a gate voltage for passing the electric current from the reference current source I1 is generated uniquely at the gates of the Nch transistors QN1-QNm. Therefore, the voltage holding capacitance element C1 accumulates the electric charges in accordance with the gate voltages.

Ex. 1001 ('047 Patent) at 8:3-11. Thus, Baek teaches an essentially identical operation as the '047 Patent.

iii. “a voltage-current converting circuit”

161. Baek also discloses this limitation. The circuit comprising transistor M2 is an example of the claimed “voltage-current converting circuit,” and is annotated green.



Ex. 1005, Fig. 5 (annotated). Baek explains that during current output mode (upon activating latch enable signals L1 or LE2), the transistor M2 “may have its gate coupled to the storage capacitor CST [and] output the analog gray-scale current to the output terminal OUT[K] based on the charged analog gray-scale current.” Ex. 1005 (Baek) ¶[0058]. Thus, a voltage held in the storage capacitor is applied to the gate of transistor M2. A POSITA would have recognized that transistor M2 converts the voltage applied to its gate into a corresponding current (between its drain and source), because one of the fundamental properties of a transistor is to output a current based on its gate voltage and because there is no current flowing from storage

capacitor CST to transistor M2. Therefore, this circuit converts the current stored in storage capacitor CST into output current.

162. By way of confirmation of my analysis, similar to Baek, the '047 Patent explains that the voltage-current converting function is performed in current output mode, where transistors QN1-QNm convert the voltage applied to the gate of QN1-QNm into current flowing through QN1-QNm. Ex. 1001 ('047 Patent) at 8:30-38.

iv. “at least one current output terminal”

163. Baek discloses this limitation. Each current/sample hold circuit contains transistor M2. The drain terminal of transistor M2 in Baek is an example of the claimed “at least one current output terminal.” Under a current output mode, switch S3 is closed (current flows), and a current from the drain terminal of transistor M2 passes through the switch S3 to the output terminal OUT[K]. Ex. 1005 (Baek) ¶[0058]. Thus, the drain terminal of transistor M2 is an example of the claimed “at least one current output terminal.”

164. By way of confirmation of my analysis, similar to Baek, the '047 Patent explains that under a current output mode:

A gate voltage according to the electric charges accumulated in the voltage holding capacitance element C1 is applied to the gates of the Nch transistors QN1-QNm. Thus, it is possible to output a sink current having a current value proportional to the reference current in accordance with the conduction states of the current output switches So1, So2 and the signal response switches G1-Gm, through connecting

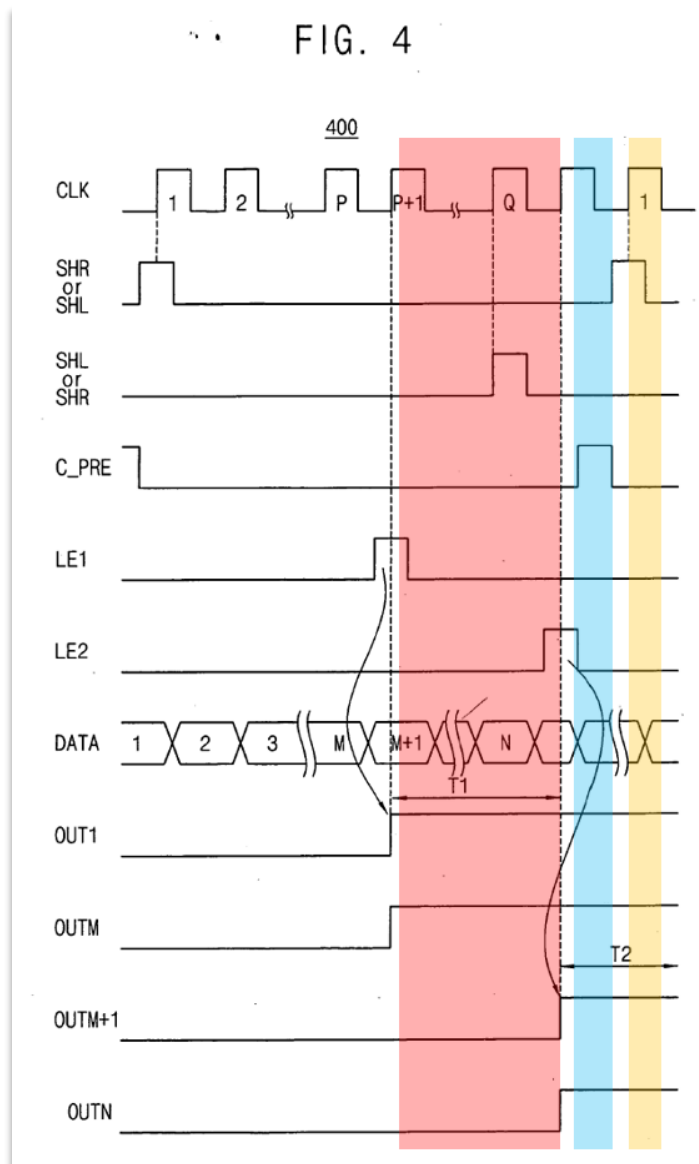
a power source to the current output terminal T1 or the current output terminal T2.

Ex. 1001 ('047 Patent) at 8:30-33.

- g. **1(e): “each of said current output circuits operates in three operation modes including a voltage supply mode, a current supply mode, and a current output mode,”**

165. Baek discloses this limitation. Baek discloses applying a pre-charge signal to initiate the claimed “voltage supply mode” (annotated in blue), applying a CLK signal to initiate the claimed “current supply mode” (annotated in gold), and applying an OUT signal and a latch enable signal (LE1 or LE2) to initiate the claimed “current output mode” (annotated in red).

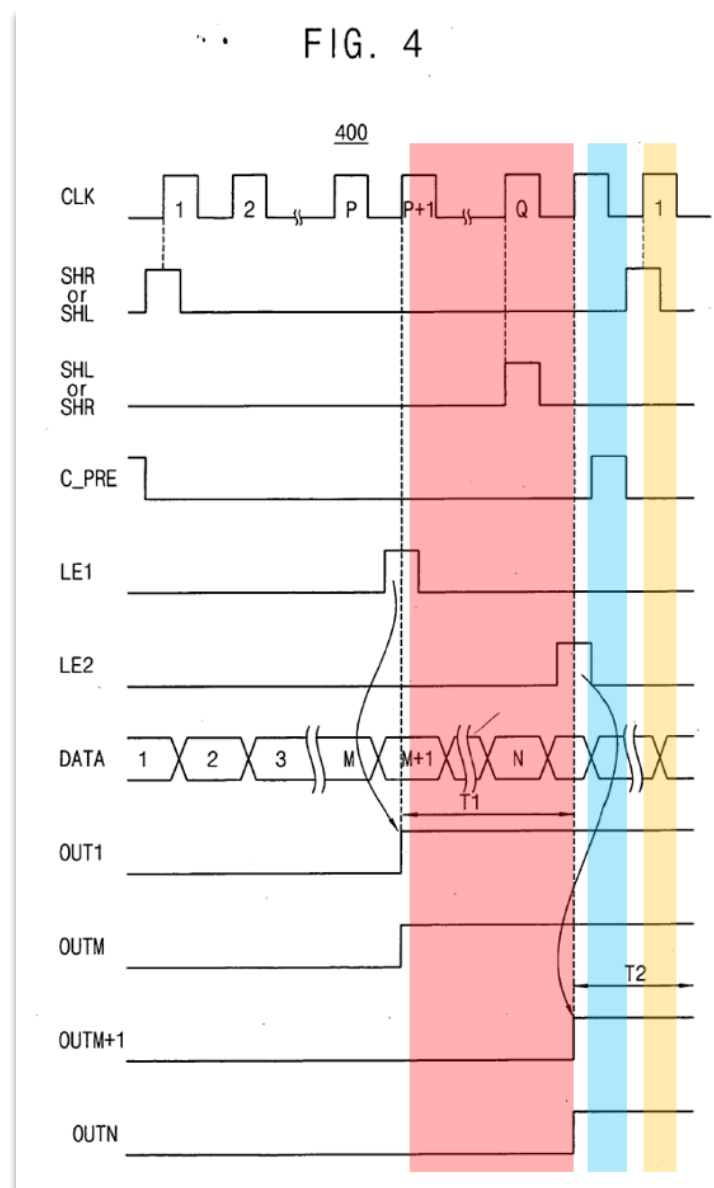
FIG. 4



Ex. 1005 (Baek) at Fig. 4 (annotated). These operation modes are described further below.

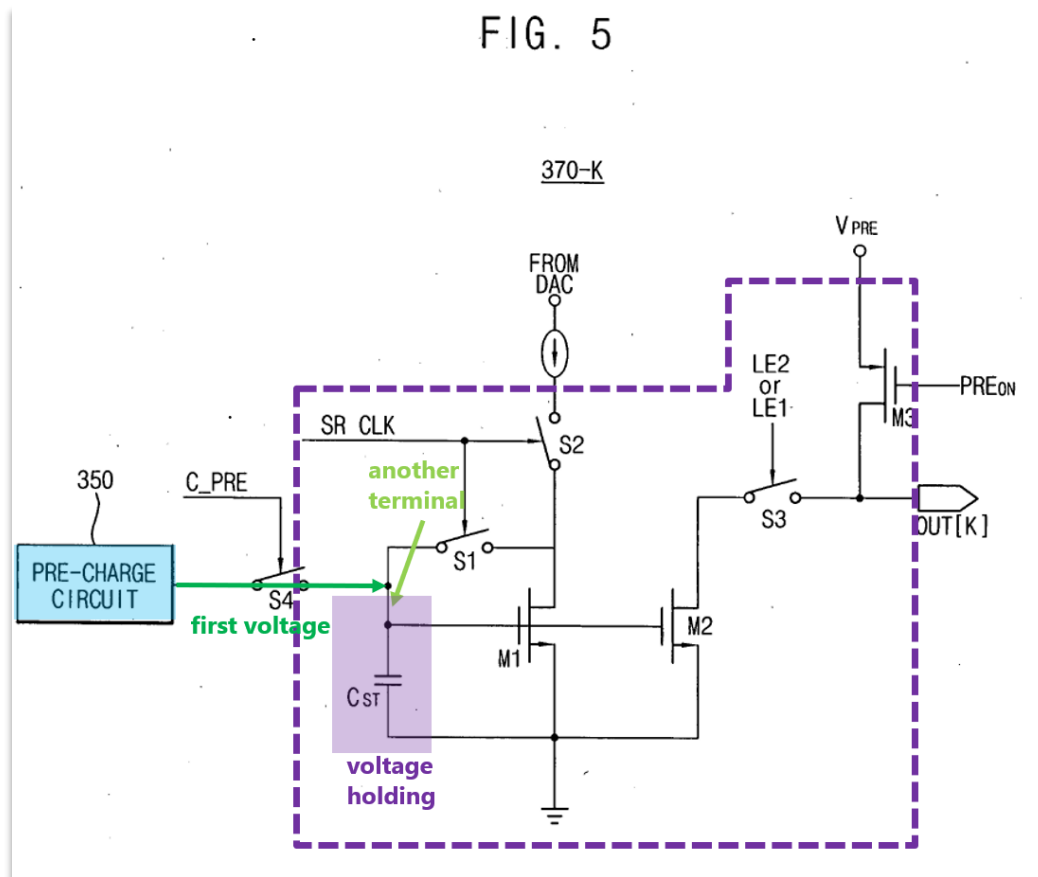
- h. **1(f). “under said voltage supply mode, each of said current output circuits receives said first voltage from said first voltage supply source, and the first voltage is supplied to another terminal of said voltage holding circuit,”**

166. Baek discloses this limitation. When the C_PRE signal is set to high, the current sample/hold circuit operates under the claimed “voltage supply mode.” This is shown in Figure 4 below, annotated blue.



Ex. 1005, Fig. 4 (annotated).

167. As shown in the annotated Fig. 5, each current sample/hold circuit (within the dotted purple box, part of current sample/hold output circuit, the claimed “current output circuit”) receives the first voltage (annotated green) from the pre-charge circuit (the claimed “first voltage supply source,” annotated blue). Baek explains “a fourth switch S4 may be turned on to pre-charge a voltage of the storage capacitor CST to a voltage level slightly lower than a threshold voltage of the first transistor M1 in response to the capacitor pre-charge signal C_PRE.” Ex. 1005 (Baek) ¶[0062]. Figure 5 below further shows the first voltage is supplied to another terminal (annotated light green) of the voltage storage circuit (annotated solid purple).



Ex. 1005 (Baek) at Fig. 5 (annotated).

168. By way of confirmation of my analysis, similar to Baek, the '047 Patent explains that, under a voltage supply mode, the voltage holding capacitor is connected to the voltage supply source. Ex. 1001 ('047 Patent) at 7:44-48 ("the high-speeding switch Sw3 is set to a conductive state, so that the voltage supply source V1 and the node N2 are connected"). The capacitor C1 is then charged by the first voltage from voltage supply source. Ex. 1001 ('047 Patent) at 7:48-52 ("the voltage holding capacitance element C1 is charged to a constant voltage (this

corresponds to the first voltage, and will be referred to as a reference voltage hereinafter) that is supplied from the voltage supply source V1”).

- i. **1(g). “under said current supply mode, each of said current output circuits receives said first current from said first current supply source, and generates a second voltage by said current-voltage converting circuit, and the first current is supplied to said another terminal of said voltage holding circuit, and”**

169. Baek discloses this element. When the SR CLK signal is activated, the current sample/hold circuit operates under the claimed “current supply mode.”

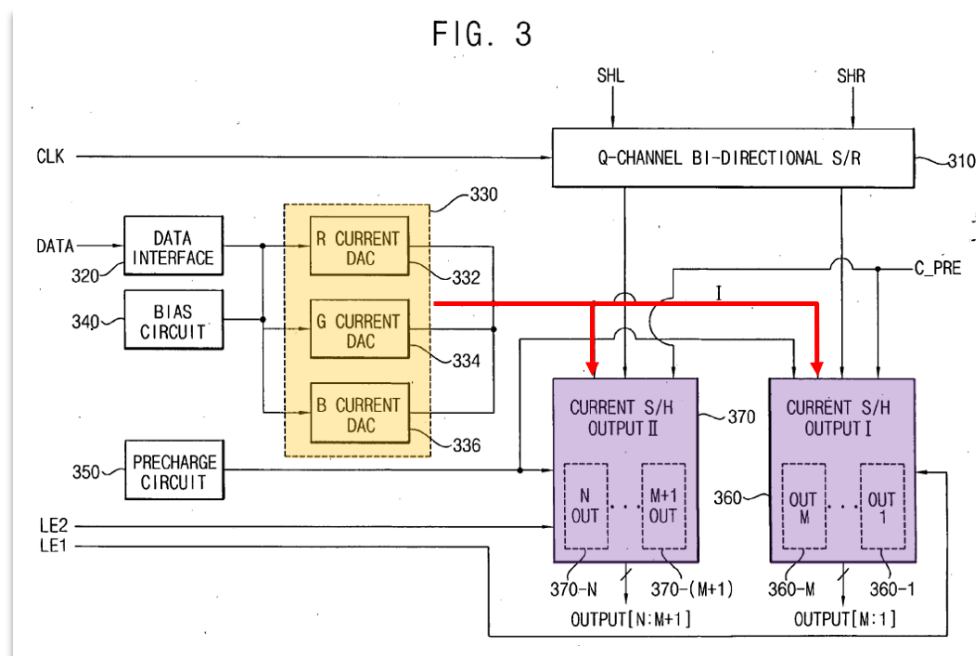
- i. **“under said current supply mode, each of said current output circuits receives said first current from said first current supply source”**

170. Under this mode, switches S1 and S2 are turned on and each current sample/hold output circuit (the claimed “current output circuits”) receives the gray-scale analog current from a current DAC (the claimed “first current from said first current supply source”). Ex. 1005 (Baek) ¶¶[0045] (“The first current sample/hold output circuit 360 may sample/hold the analog gray-scale current.”), [0044] (“The current digital-to-analog conversion unit 330 [“DAC”] may convert gray-scale data provided from the data interface circuit 320 to an analog gray-scale current based on the gamma reference signal.”). Specifically, the current will be applied to the gate and drain terminals of transistor M1, which is part of the current sample/hold output circuit. Ex. 1005 (Baek) ¶[0056]. Baek discloses:

As a result, an analog gray-scale current output from a current digital-to-analog conversion unit 330 may be applied to a drain of the first transistor M1 via the second switch S2. At this time, because the first switch S1 is also turned on, the analog gray-scale current applied to the drain of the first transistor M1 may be applied to a gate of the first transistor M1.

Ex. 1005 (Baek) ¶[0056].

171. The current DAC (the claimed “current supply source”) is shown in Figures 3 and is annotated in gold, and the current output circuits are annotated in purple. The lines along which the “first electric current” are supplied are annotated in red.



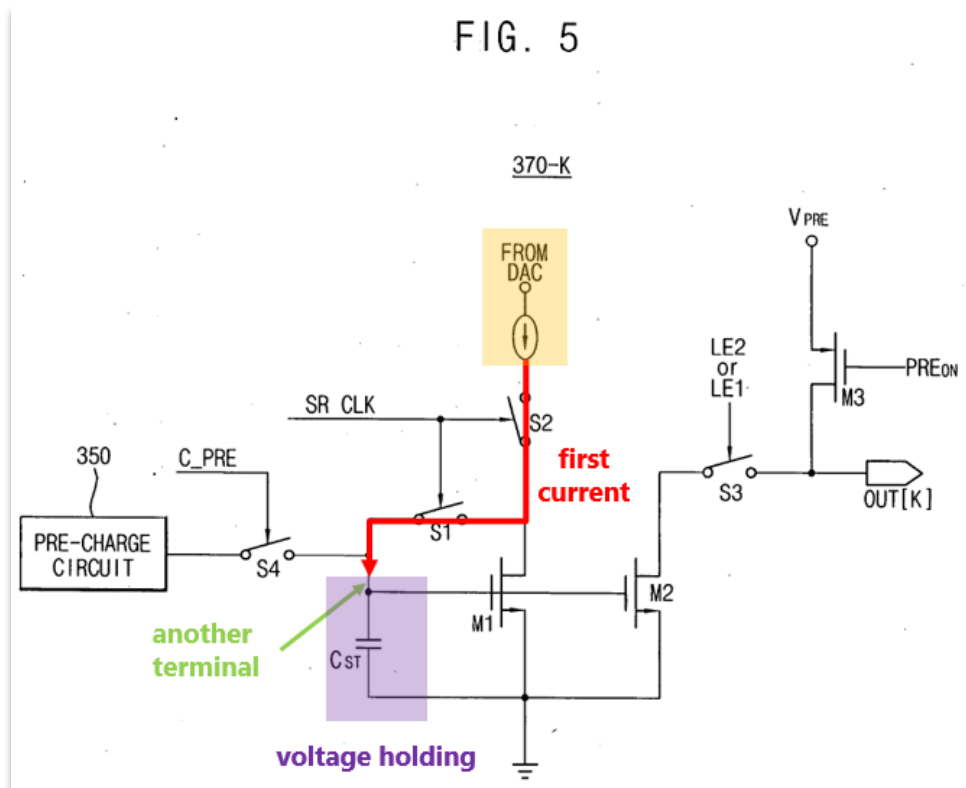
Ex. 1005 (Baek) at Fig. 3.

ii. “generates a second voltage by said current-voltage converting circuit, and”

172. Baek discloses this element. Under the current supply mode, the storage capacitor continues to be charged by current from the DAC. Under the voltage supply mode that preceded the current supply mode, the storage capacitor was charged by pre-charge circuit to “a voltage level slightly lower than a threshold voltage of the first transistor M1.” Because current from the DAC continues charging the pre-charged capacitor during the current supply mode, the voltage across the capacitor and the gate voltage of transistor M1 continue to change, thereby reaching a second voltage different from the pre-charge voltage. Ex. 1005, ¶[0056].

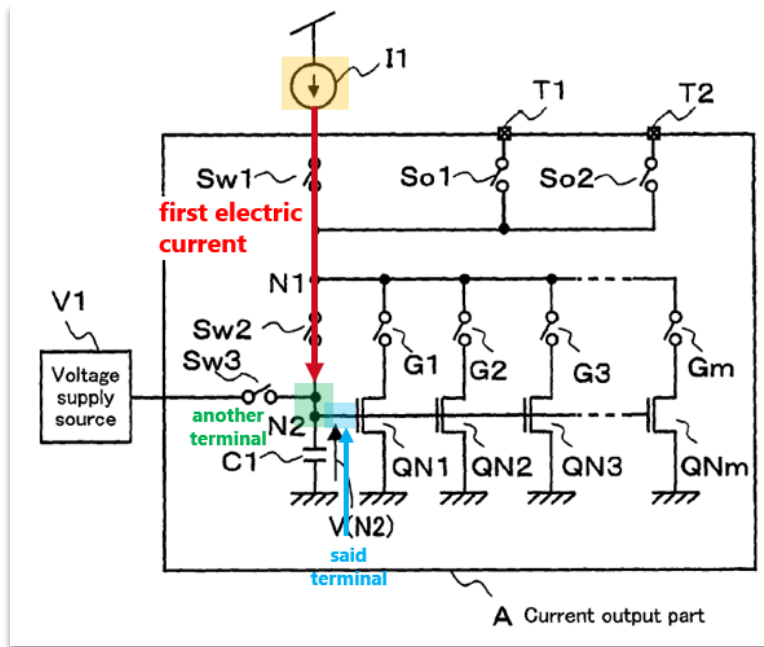
iii. the first current is supplied to said another terminal of said voltage holding circuit

173. As shown in Figure 5 below, the first current (annotated red) from the current source (annotated gold) is supplied to the claimed “another terminal” (annotated light green) of the storage capacitor CST (the claimed “voltage holding circuit,” annotated purple).



Ex. 1005 (Baek) at Fig. 5 (annotated), ¶[0056].

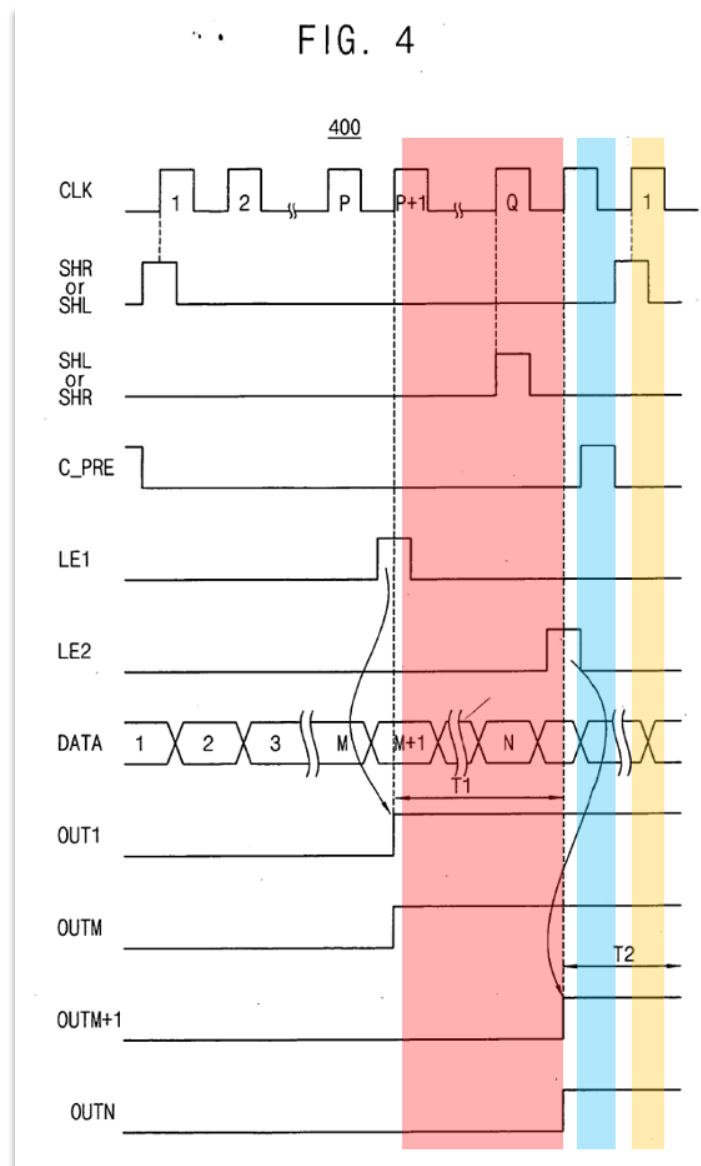
174. By way of confirmation of my analysis, similar to Baek, the '047 Patent explains that the first current is supplied to the second terminal of the voltage holding capacitor in a similar manner. Figure 1 of the '047 Patent is annotated to show that a second voltage is supplied to the marked "said terminal" of the voltage holding capacitor while a first electric current is supplied to the marked "another terminal" of the voltage holding capacitor.



Ex. 1001 ('047 Patent) at Fig. 1A (annotated).

- j. 1(h). “under said current output mode, each of said current output circuits outputs an output current according to said voltage held in said voltage holding circuit by said voltage-current converting circuit.”

175. Baek discloses this limitation. When a latch-enable signal LE1 or LE2 is activated, the current sample/hold circuit operates under the claimed “current output mode.”



Ex. 1005, Fig. 4 (annotated). Under the current output mode, which is annotated above in red, switch S3 is turned on and the transistor M2 outputs a current according to its gate voltage, which is the voltage stored in the storage capacitor CST.

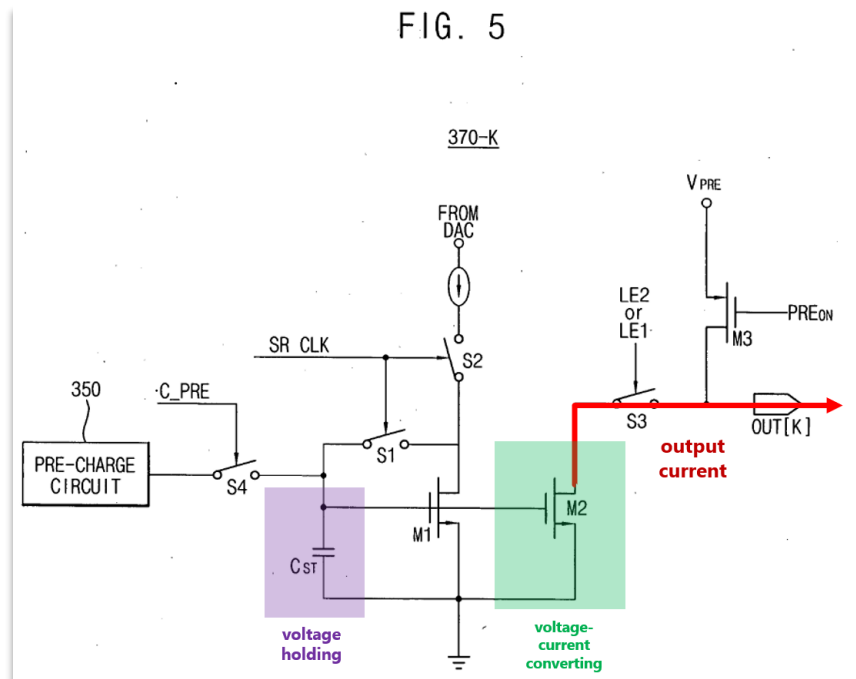
When the first latch enable signal LE1 or the second latch enable signal LE2 is activated, a third switch S3 may couple a drain of the second transistor M2 to an output terminal OUT[K], and the second transistor M2, which may have its gate coupled to the storage capacitor CST, may

output the analog gray-scale current to the output terminal OUT[K]
based on the charged analog gray-scale current.”

Ex. 1005 (Baek) ¶[0058].

176. A POSITA would have recognized that transistor M2 converts the voltage applied to its gate into a corresponding current, because one of the fundamental properties of a transistor is to output a current based on its gate voltage. The output current is set according to the voltage held in the voltage holding circuit (i.e., as opposed to a current from the voltage holding circuit), as there is no meaningful current flowing from storage capacitor CST to transistor M2. A POSITA would further have recognized that “the second transistor M2 . . . may output the analog gray-scale current . . . based on the charged analog gray-scale current,” meaning that the transistor M2 outputs a current based on the voltage applied to its gate, which is the voltage stored in the storage capacitor. *See* Ex. 1005 (Baek) ¶[0058].

FIG. 5



Ex. 1005 (Baek) at Fig. 5 (annotated).

B. CLAIMS DEPENDING FROM CLAIM 1 OF THE '047 PATENT

- a. “2. The current driving device according to claim 1, wherein: each of said output terminals is connected to said current output terminals provided to said plurality of said current output circuits, and each of said plurality of current output circuits is connected in parallel to said first current supply source and said first voltage supply source used in common”

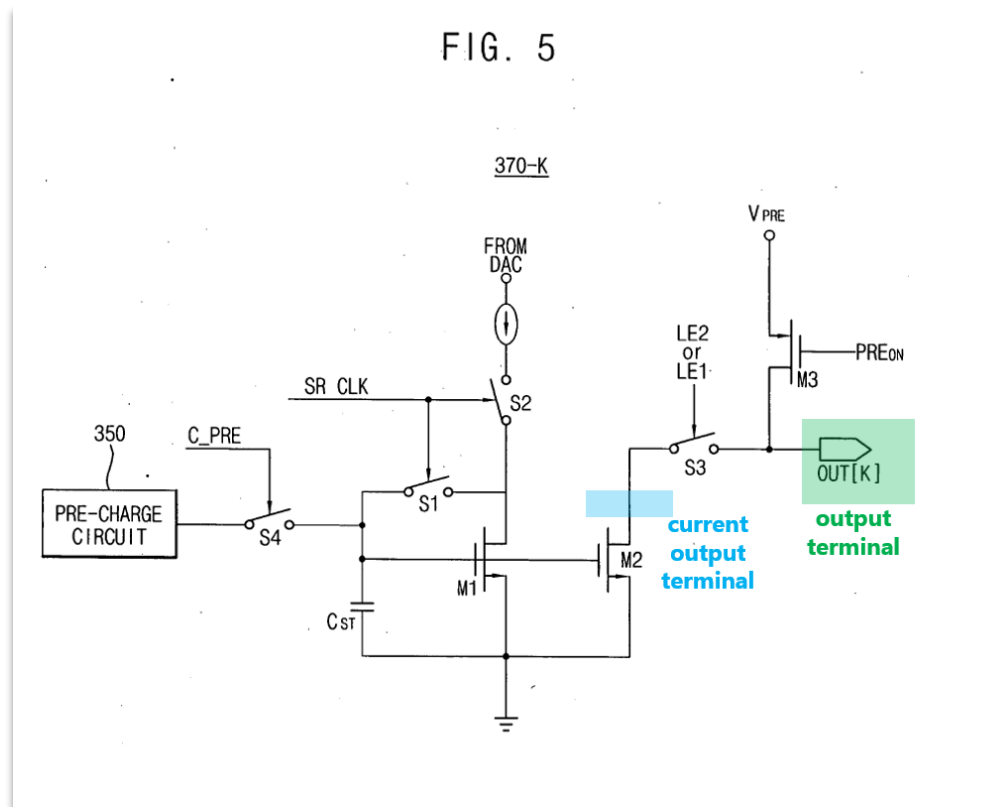
177. Baek discloses, or at least renders obvious, this claim.

- i. “each of said output terminals is connected to said current output terminals provided to said plurality of said current output circuits”**

178. Baek discloses this limitation. As described above for Claim

Limitation 1(c), the output terminals OUT[1] through OUT[N] are an example of

the claimed “output terminals.” As described above for Claim Limitations 1(d)(1) and 1(d)(2), the current sample/hold output circuits 360 and 370 are an example of the plurality of current output circuits. Also, the drain terminals of transistors M2, each located within a corresponding current sample/hold circuit, are an example of current output terminals. As shown in Figure 5 below, the drain terminal of transistor M2 (annotated blue) is connected to the output terminal OUT[K] (annotated green). Ex. 1005 (Baek) ¶[0058].

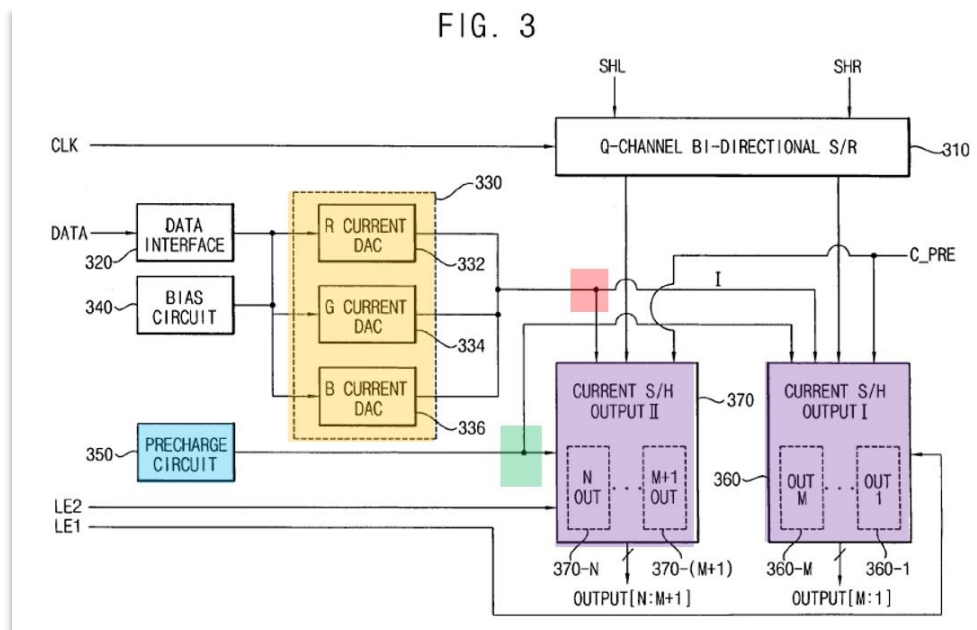


Ex. 1005 (Baek) at Fig. 5 (annotated).

179. Baek discloses each current sample/hold output circuit (360 and 370) comprises a plurality of current sample/hold circuits (360_{1-M} and $370_{(M+1)-N}$), each of which comprises a transistor M2. Ex. 1005 ¶¶[0038], [0039], [0055]; Figs. 3, 5. Thus, Baek discloses each of said output terminals is connected to said current output terminals provided to said plurality of said current output circuits as recited in claim 2.

- ii. **“each of said plurality of current output circuits is connected in parallel to said first current supply source and said first voltage supply source used in common.”**

180. Baek discloses this element or at least renders it obvious. As shown in Figure 3 below, current sample/hold output circuits 360 and 370 (annotated purple) and DAC 330 (annotated gold) are connected to a common node (annotated red). As shown in Figure 5, the current sample/hold output circuits 360 and 370 are grounded because the individual current sample/hold circuits within the current sample/hold output circuits 360 and 370 are grounded. A POSITA would have recognized that DAC 330 would also be grounded, or that it would have been obvious to do so, because it is necessary to have a power supply grounded in order to form a complete loop. Therefore, each of current sample/hold output circuits 360 and 370 is connected in parallel to DAC 330 used in common.



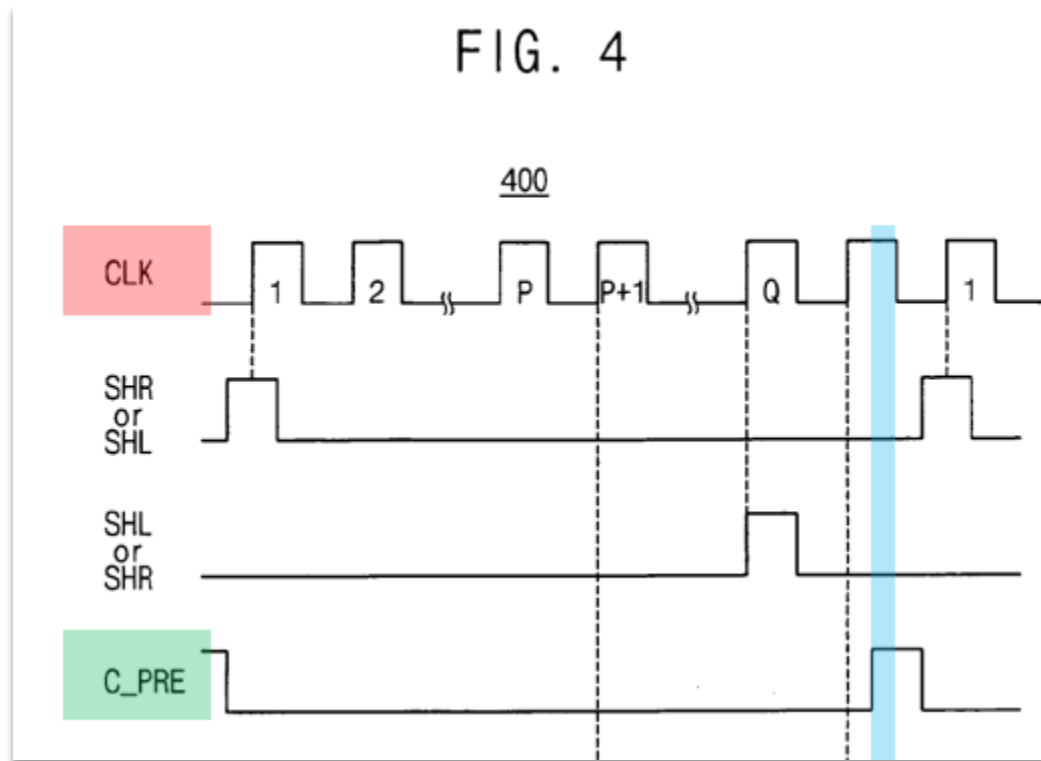
Ex. 1005 (Baek) at Fig. 3.

181. As shown in Figure 3 above, current sample/hold output circuit 360, current sample/hold output circuit 370, and pre-charge circuit 350 (annotated blue) are connected to a common node (annotated green). A POSITA would have recognized the pre-charge is also grounded because it is necessary to have a power supply grounded to form a complete loop. Therefore, each of current sample/hold output circuits 360 and 370 is connected in parallel to the pre-charge circuit used in common.

- b. **“3. The current driving device according to claim 1, wherein, in each of said current output circuits, said current-voltage converting circuit is actuated under said voltage supply mode.”**

182. Baek discloses this claim. As discussed above for Claim Limitation 1(f) and Claim Limitation 1(g), the driving device operates under the claimed “voltage supply mode” when control signal C_PRE is activated, and the driving device operates under the claimed “current supply mode” when a clock signal CLK is activated. When a clock signal CLK is activated, the switches S1 and S2 are closed and the current from DAC is supplied to the storage capacitor and the drain and gate terminals of transistor M1. Ex. 1005, ¶¶[0056], [0057]. The transistor M1 and storage capacitor CST then converts the current into a voltage stored at the storage capacitor CST. Thus, under the claimed current supply mode, the current-voltage converting circuit in Baek is actuated.

183. As shown in Figure 4 below, Baek discloses that C_PRE (annotated green) and CLK (annotated red) can be activated simultaneously (e.g., both set to high) during the timespan highlighted in blue. Therefore, Baek discloses the current-voltage converting circuit is actuated under the claimed voltage supply mode.



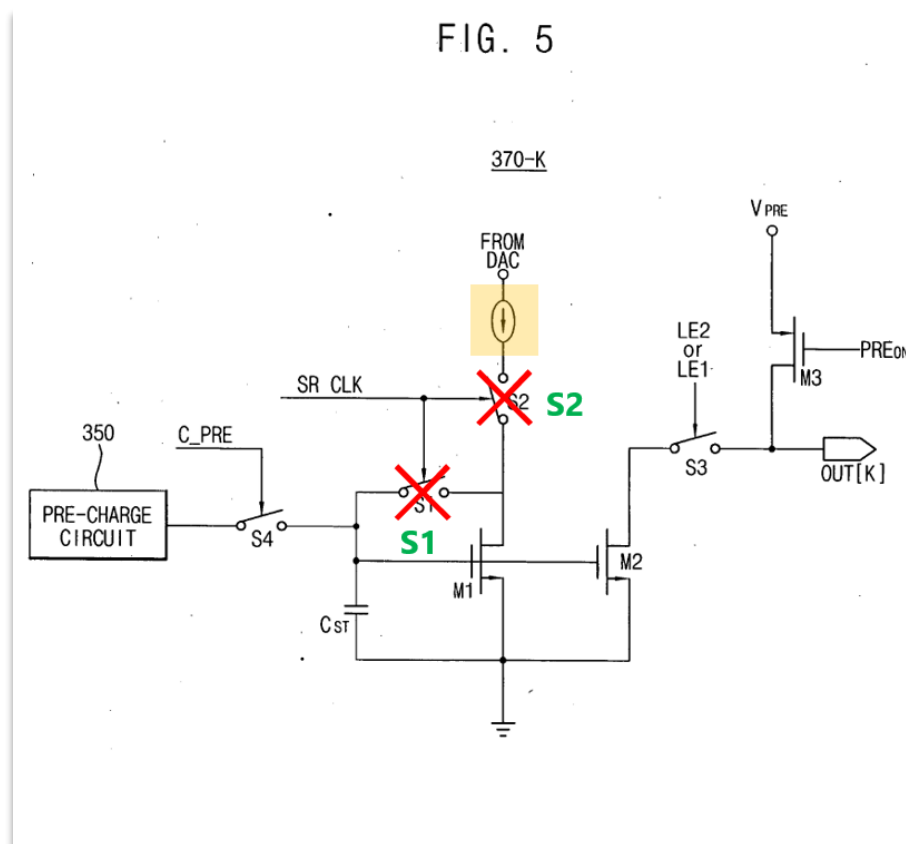
Ex. 1005 (Baek) at Fig. 4 (annotated and excerpted).

- c. **“4. The current driving device according to claim 1, wherein each of said current output circuits is configured to stop said current-voltage converting circuit under said voltage supply mode.”**

184. Baek discloses this claim. As discussed above for Claim Limitation 1(f) and Claim Limitation 1(g), the current driving device operates under the claimed “voltage supply mode” when control signal C_PRE is activated, and operates under the claimed “current supply mode” when a clock signal CLK is activated. As shown in Figure 5 below, when a clock signal CLK is deactivated, the switches S1 and S2

(annotated green) are open, isolating the current source DAC 330 from the current sample/hold circuit. The current-voltage converting circuit is thus stopped.

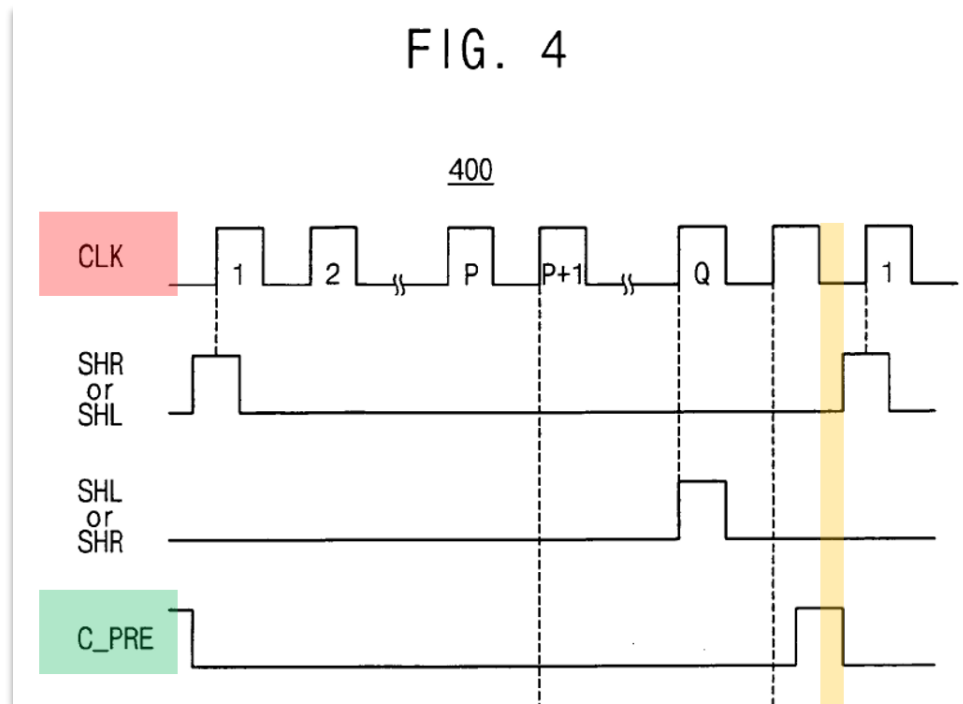
185. The current source (annotated gold) and switches S1 and S2 (annotated green) are shown in Figures 5 with a red \times placed over the switches that are open (i.e., current does not flow).



Ex. 1005 (Baek) at Fig. 5 (annotated).

186. As shown in Figure 4 below, Baek discloses that CLK (annotated red) can be deactivated when C_PRE (annotated green) is activated during the timespan

highlighted in gold. Ex. 1005 (Baek) at Fig. 4. Therefore, Baek discloses the current-voltage converting circuit is stopped under the claimed voltage supply mode.



Ex. 1005 (Baek) at Fig. 4 (annotated and excerpted).

- d. **“9. A current-driving-type display device, comprising said current driving device according to claim 1 mounted thereon so as to be driven by said current driving device.”**

187. Baek discloses this element. Baek discloses that “a display driver circuit for a flat display panel and a display driving method using the same.” Ex. 1005 (Baek) ¶[0003]. The display driver circuit would be mounted on the flat-panel display. Baek further discloses that “the display driver circuit according to example embodiments of the present invention may be applicable to Organic Light Emitting

Diode (OLED) display devices, for example, current-driven active matrix type OLED display devices.” Ex. 1005 (Baek) ¶[0064].

XIV. GROUND 5 & 6: SASAKI

188. It is my opinion that Claim 10 of the '047 Patent is anticipated by Sasaki (Ex. 1006), corresponding to Ground 5. To the extent Patent Owner contends that any of these claims are not anticipated, then they would have been rendered obvious over Sasaki in view of the knowledge of a POSITA, corresponding to Ground 6.

A. INDEPENDENT CLAIM 10 OF THE '047 PATENT

a. 10(preamble): “A current driving device, comprising:”

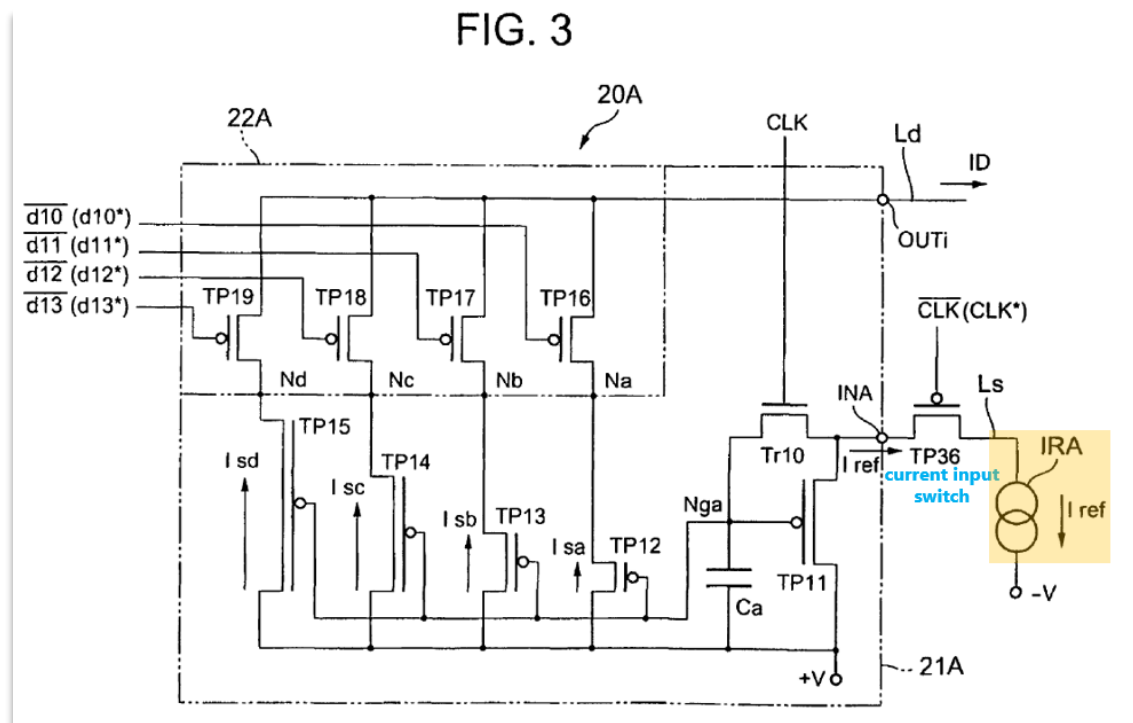
189. To the extent the preamble is limiting, Sasaki discloses the preamble. The driving device for the display device in Sasaki is an example of the claimed “current driving device.” Sasaki discloses a display device comprising a current generation supply circuit. Ex. 1006 (Sasaki) at ¶[0003]. The current generation supply circuit “supplies drive currents corresponding to digital signals for a plurality of loads.” Ex. 1006 (Sasaki) at Abstract (emphasis added).

b. 10(a): “a current input switch for controlling connection/disconnection states with respect to a current supply source;”

190. Sasaki discloses this limitation. The “current supply source control transistor TP36” in Sasaki is an example of the claimed “current input switch.” Ex. 1006 (Sasaki), ¶[0063]. As shown in Figure 3 below, the current supply source

control transistor TP36 (annotated blue) controls connection/disconnection states of “constant current generation source IRA.” Ex. 1006 (Sasaki) ¶¶[0062]-[0063], Fig.

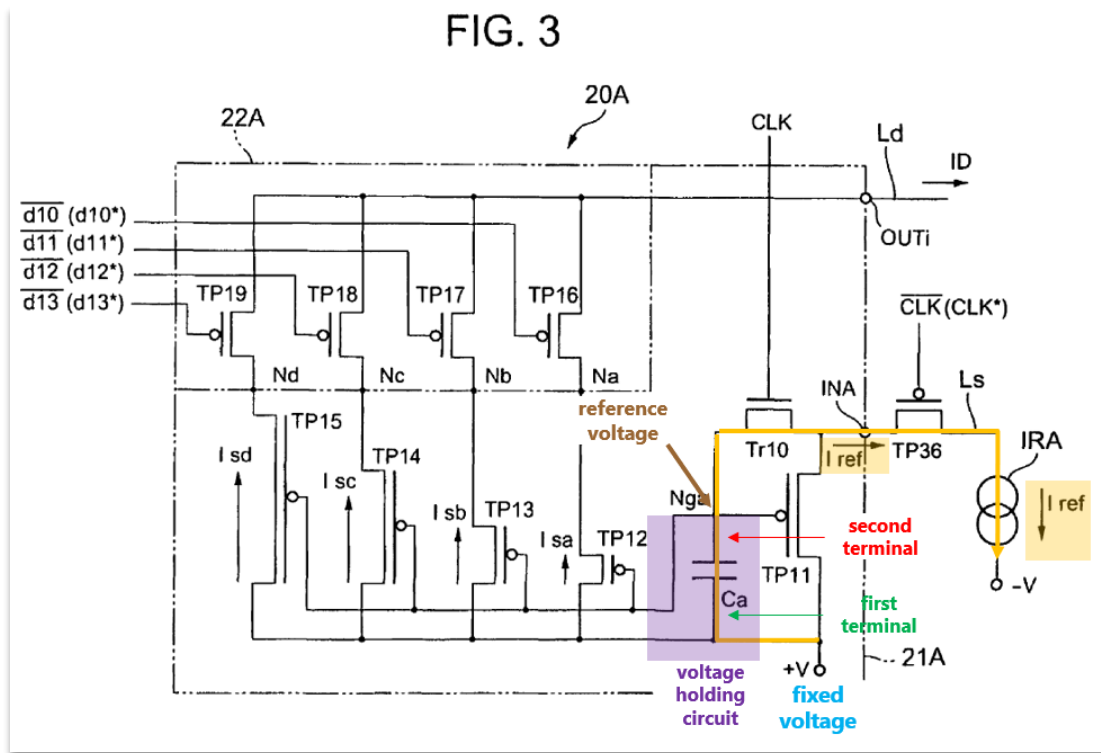
3. The item labeled IRA (annotated gold) is an example of the claimed “current supply source,” because it supplies a reference current I_{ref} . Ex. 1006 (Sasaki) ¶¶[0062]-[0063] (“reference current I_{ref} supplied from a constant current generation source I_{ref} ”).



Ex. 1006 (Sasaki) at Fig. 3 (annotated).

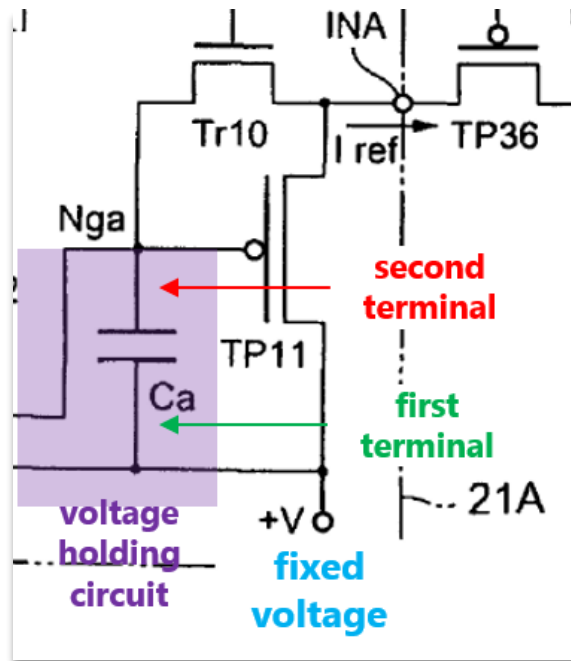
- c. **10(b): “a voltage holding circuit for holding a reference voltage, which is charged by a flown current, the voltage holding circuit having a first terminal and a second terminal, the first terminal being connected to a fixed voltage;”**

191. Sasaki discloses this limitation or at least renders it obvious. Sasaki describes a “charge storage circuit,” which includes “the capacitor Ca shown in Fig. 3.” Ex. 1006 (Sasaki) ¶[0138]. The charge storage circuit comprising the capacitor Ca is an example of the claimed “a voltage holding circuit.” The charge holding circuit has two terminals: “the capacitor Ca is connected between the high electric potential +V and the contact Nga (gate terminal of the reference current transistor TP11).” Ex. 1006 (Sasaki) ¶[0063]. The voltage holding circuit is shown in Figure 3 below and is annotated purple.



Ex. 1006 (Sasaki) at Fig. 3 (annotated).

192. As shown in Figure 3 below, charge storage circuit Ca (the claimed “voltage holding circuit,” annotated purple) has a first terminal (annotated green) and a second terminal (annotated red), the first terminal being connected to the high electric potential +V (annotated blue). A POSITA would have recognized that a high electric potential +V represents a constant voltage supply, which is an example of the claimed “fixed voltage.” +V along with designations such as V_{DD} and V_{CC} are commonly used on circuit diagrams to depict a fixed supply voltage that is supplied to the drain of a MOSFET.



Ex. 1006 (Sasaki) at Fig. 3 (annotated and excerpted). Sasaki discloses “[t]he capacitor Ca is connected between the high electric potential +V and the contact Nga (gate terminal of the reference current transistor TP11). Ex. 1006 (Sasaki) ¶[0063].

193. The charge storage circuit (capacitor Ca) holds a “specified voltage” that is charged by a reference current I_{ref} . Ex. 1006 (Sasaki) ¶[0071] (“[a]s a result based on the reference current I_{ref} , the electrical charge supplied to the contact Nga is stored in the capacitor Ca”); ¶[0077] (“the electrical charge is stored (charge) in the capacitor Ca and the refresh operation is executed by which the potential of the gate terminal (contact Nga) is recharged to specified Voltage”). The reference current I_{ref} is an example of the claimed “flowed current.” The specified voltage is an example of the claimed “reference voltage” and is annotated brown in Figure 3

above. The reference current I_{ref} is an example of the claimed “flown current” and is annotated in gold in Figure 3 above.

[I]n this non-selection state, when both the current supply source control transistor TP36 and the refresh control transistor Tr10 perform an “ON” operation, the reference current I_{ref} flows in the current path of the reference current transistor TP11 and the electrical charge of the reference current I_{ref} is supplied to the gate terminal (contact Nga) based on the channel width of the reference current transistor TP11.

Ex. 1006 (Sasaki) ¶[0077]. Sasaki discloses that the electric charge stored in the capacitor Ca is the result of the reference current I_{ref} . Ex. 1006 (Sasaki) ¶[0071] (“[a]s a result based on the reference current I_{ref} , the electrical charge supplied to the contact Nga is stored in the capacitor Ca”).

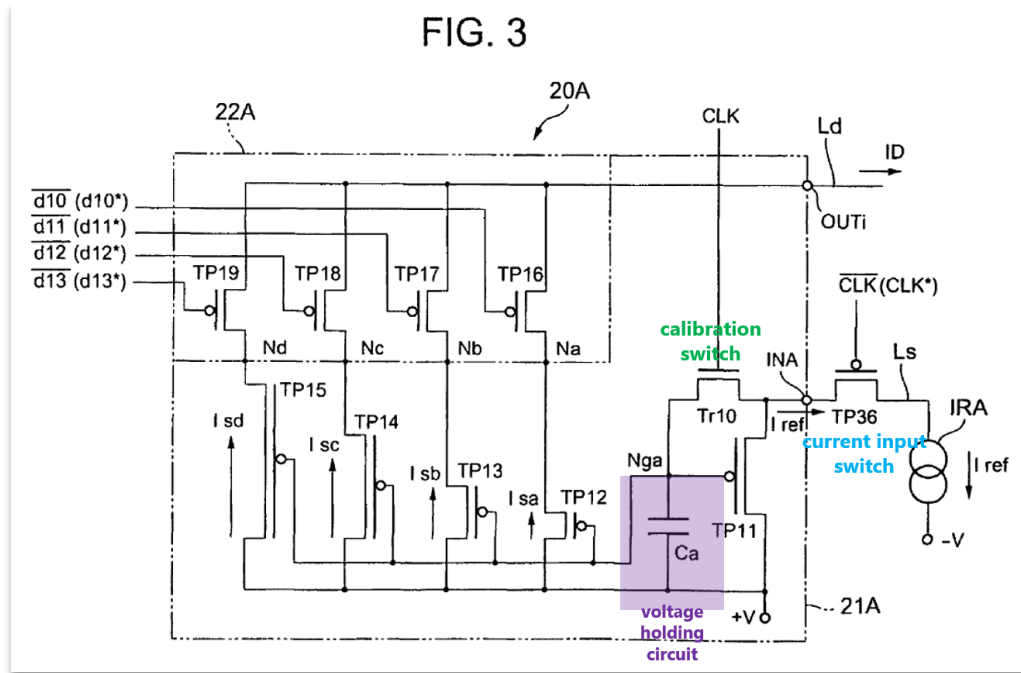
d. **10(c): “a calibration switch interposed between said current input switch and said voltage holding circuit;”**

194. Sasaki discloses this limitation. Refresh control transistor Tr10 is an example of the claimed “calibration switch.” In Sasaki, a refresh is performed to calibrate the voltage across the capacitor Ca.

Furthermore, in this non-selection state, when both the current supply source control transistor TP36 and the refresh control transistor Tr10 perform an “ON” operation, the reference current I_{ref} flows in the current path of the reference current transistor TP11 and the electrical charge of the reference current I_{ref} is supplied to the gate terminal (contact Nga) based on the channel width of the reference current transistor TP11.

Ex. 1006 (Sasaki) ¶[0077]. As shown in Figure 3 below, the refresh control transistor T10 (annotated green) is interposed between the current supply source

control transistor TP 36 (the claimed “current input switch,” annotated blue) and charge storage circuit (the claimed “voltage holding circuit,” annotated purple).



Ex. 1006 (Sasaki) at Fig. 3 (annotated).

195. The specification of the '047 Patent further confirms my conclusion.

Ex. 1001 ('047 Patent) at 1:37-49 (“‘Calibration’ means to have a reference current value by a reference current source stored in the current output part.”). In Sasaki, the calibration switch controls whether the reference current I_{ref} from the reference current supply source IRA is supplied to the capacitor CA to adjust the voltage stored in the capacitor. *See*, Ex. 1006 (Sasaki) at Fig. 3, [0077].

e. **10(d): “a plurality of voltage-current converting elements for generating an electric current in accordance with said reference voltage held in said voltage holding circuit;”**

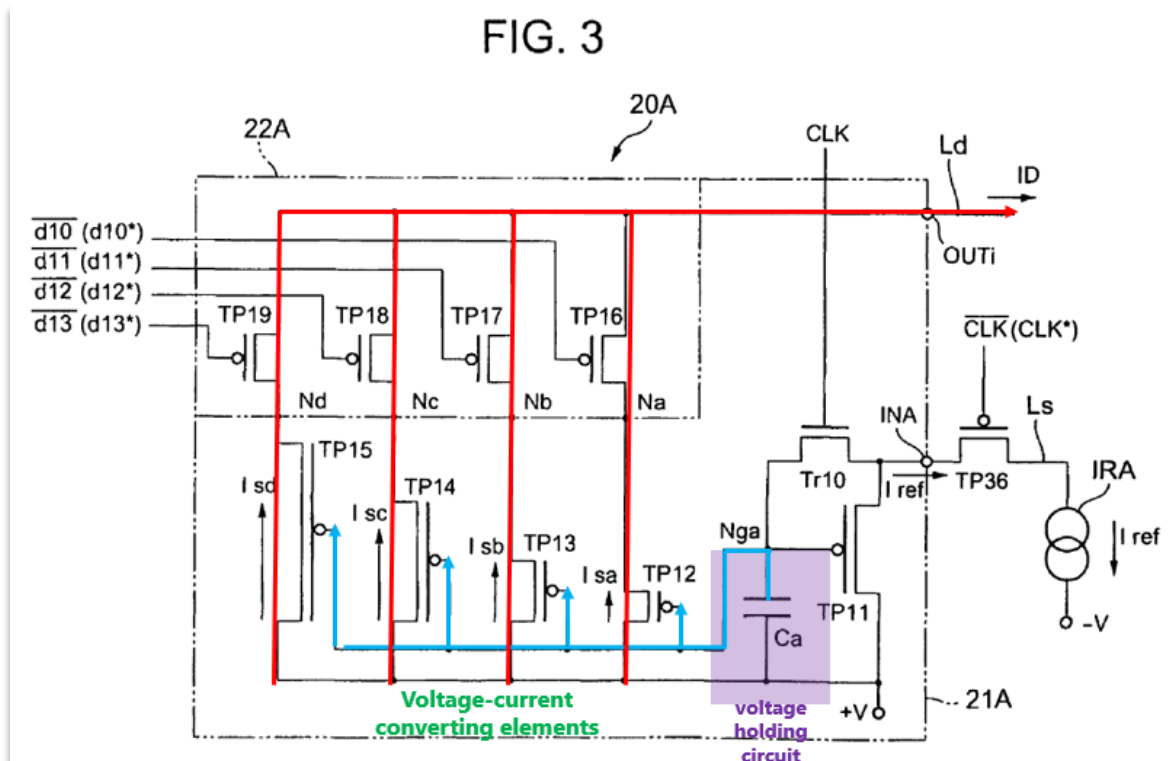
196. Sasaki discloses this limitation. A plurality of “module current transistors” (TP12-TP15) in Sasaki is an example of the claimed “a plurality of voltage-current converting elements.”

[T]he module currents I_{sa} – I_{sd} which flow to each of the module current transistors TP12~TP15 are set to have a ratio of current values different from each other relative to the constant reference current I_{ref} which flows to the reference current transistor TP11 established in the current mirror circuit section 21A stated above.

Ex. 1006 (Sasaki) ¶[0066]. Each of the module current transistors (TP12-TP15) generates an electric current in accordance with the reference voltage held in the capacitor C_a (the claimed “voltage holding capacitor”). As shown in Figure 3 below, a voltage held in the capacitor C_a is applied to the gates of transistors TP12 through TP15. A POSITA would have recognized that transistors TP12 through TP15 convert the voltage applied to their gate into a corresponding current (between drain and source), because one of the fundamental properties of transistors is to output current based on their gate voltage and because there is no current flowing from capacitor C_a to transistors TP12 through TP15. Therefore, this circuit converts the current stored in storage capacitor C_{ST} into output current.

197. As shown in Figure 3 below, each of the module current transistors (TP12-TP15, annotated green) receives the reference voltage from the capacitor C_a

(the claimed “voltage holding capacitor,” annotated purple) at its gate and outputs an electric current in accordance with that reference voltage. The lines along which the reference voltage is supplied are annotated in blue, and the lines along which output currents flow are annotated in red.



Ex. 1006 (Sasaki) at Fig. 3 (annotated).

198. By way of confirmation of my analysis, similar to Sasaki, the '047 Patent explains that the voltage-current converting function is performed in current output mode, where transistors QN1-QNm convert the voltage applied to the gate of QN1-QNm into current flowing through QN1-QNm. Ex. 1001 ('047 Patent) at 8:30-38.

- f. **10(e): “a plurality of signal response switches that are on/off controlled in accordance with inputted signals, each of said response switches being connected in series to a corresponding one of said voltage-current converting elements, and each of which being connected in parallel to said calibration switch;”**

199. Sasaki discloses this limitation. The switching transistors TP16-TP19 are an example of the claimed “signal response switches.” The on/off states of TP16-TP19 are controlled by data signals d10 through d13, which are examples of the claimed “inputted signals.”

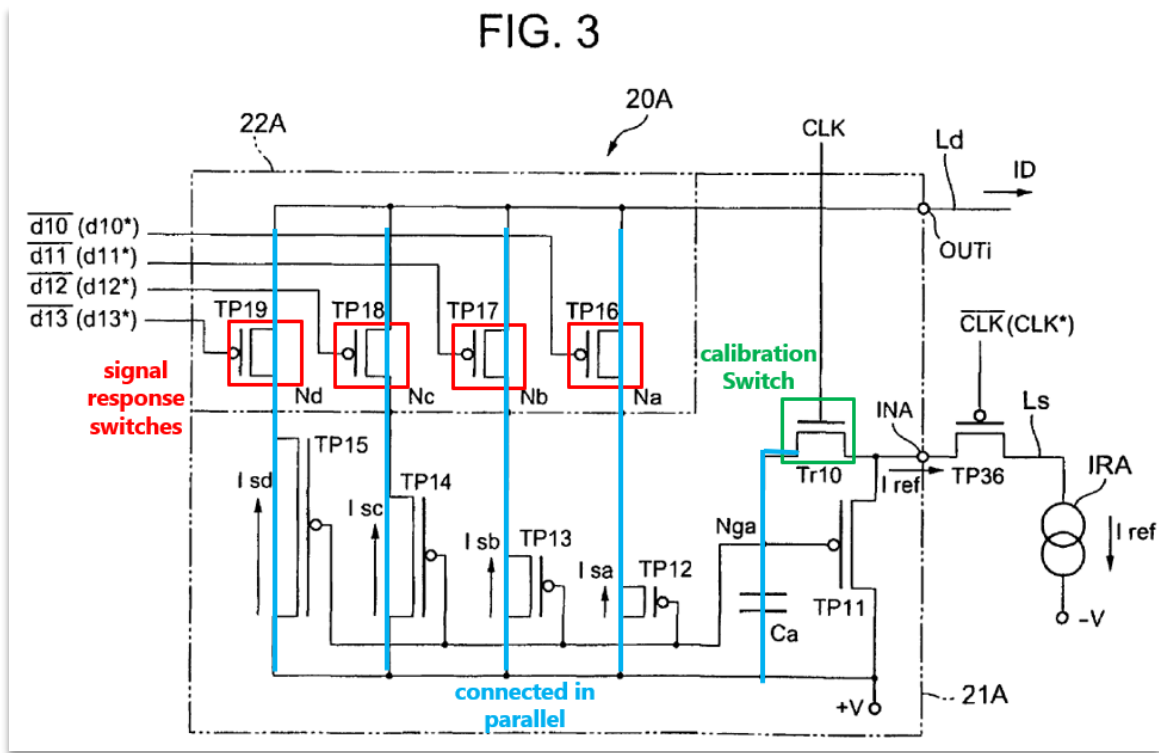
[I]n response to the signal levels of the output signals d10*~d13* from the above-mentioned latch circuits LC0~LC3, the particular switching transistors of the switching circuit section 22A perform an “ON” operation (Instances when any one or more of the switching transistors TP16~TP19 perform an “ON” operation, besides occurrences when any of the switching transistors TP16~TP19 perform an “OFF” operation is included.).

Ex. 1006 (Sasaki) ¶[0069].

[B]ased on the inverted output signals d10*~d13* outputted from the data latch section 102, the “ON/OFF” state of the plurality of switching transistors (equivalent to the switching transistors TP16~TP19 shown in FIG. 3) is controlled.

Ex. 1006 (Sasaki) ¶[0152].

200. As shown in the Figure 3 below, transistor TP19 (annotated red) is connected in series to the module current transistor TP15 (one of the claimed “voltage-current converting elements,” annotated gold). Similarly, each of the

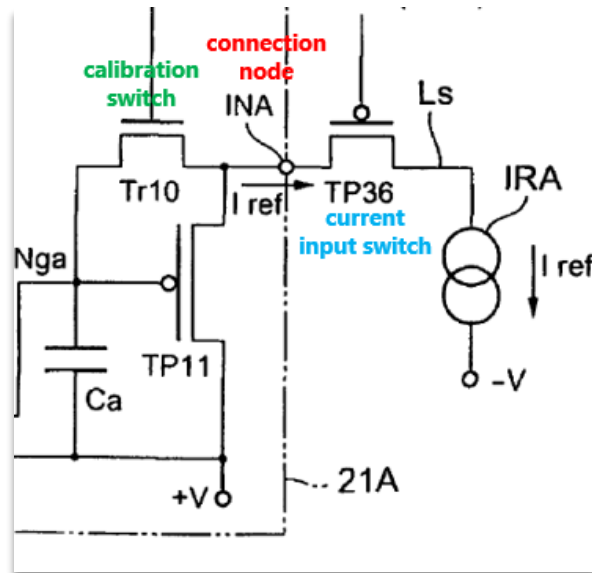


Ex. 1006 (Sasaki) at Fig. 3 (annotated).

g. 10(f): “a connection node provided between said current input switch and said calibration switch;”

202. Sasaki discloses this limitation. The current input contact INA in Sasaki is an example of the claimed “connection node.” The current input contact INA (referred as INA in Sasaki) is an input node of a corresponding current generation section 20A, receiving a reference current Iref from a corresponding reference current supplier IRA (referred as IRA in Sasaki). Ex. 1006 (Sasaki) ¶[0071]. The current input contact INA node is also referred as INi in Figure 10 of Sasaki. As shown in Figure 3 below, the current input contact INA is also connected to the fresh control transistor Tr10 (the claimed “calibration switch”). Thus, the

current input contact IN_A (annotated red) is provided between the current supply source control transistor TP 36 (the claimed “current input switch,” annotated blue) and refresh control transistor T10 (the claimed “calibration switch,” annotated green). Ex. 1006 (Sasaki) at Fig. 3.



Ex. 1006 (Sasaki) at Fig. 3 (annotated and excerpted).

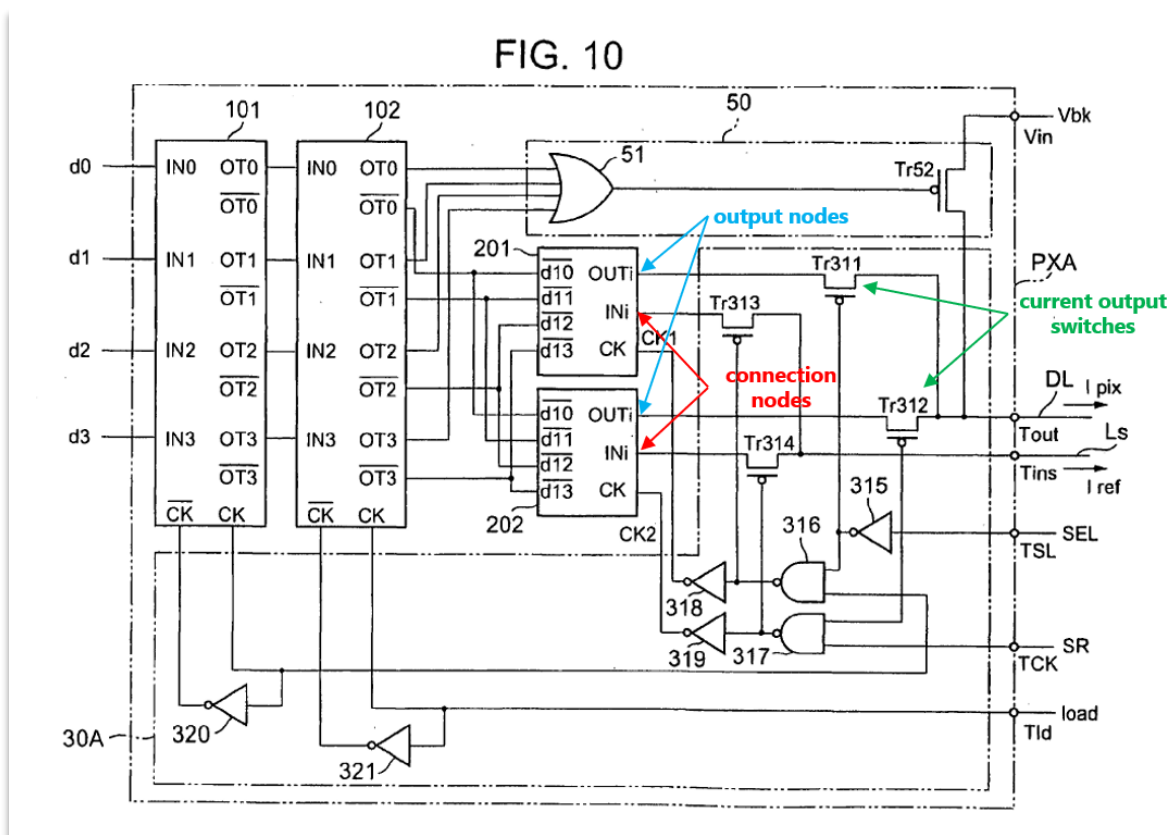
- h. 10(g): “a plurality of current output switches, each being interposed between the connection node and said plurality of current output terminals; and”**

203. Sasaki discloses this limitation. As shown in Figure 10, Sasaki discloses output control transistors TP311 and TP312 (the counterpart of TP311 and TP312 in Figure 3 is referred as TP31). Ex.1006 (Sasaki), Fig. 10. The output control transistors are an example of the claimed “current output switches,” because

each output control transistor (TP31, TP311, or TP312) controls the output of a corresponding current generation section.

When the high-level selection setting signal SL is inputted and in conjunction with reversal processing of the signal polarity by the inverter 32, the output control transistor TP31 performs an “ON” operation and the current output terminal OUTi (current output contact OUTi) of the current generation section 20A connects to the drive current supply line Ld via this output control transistor TP31.

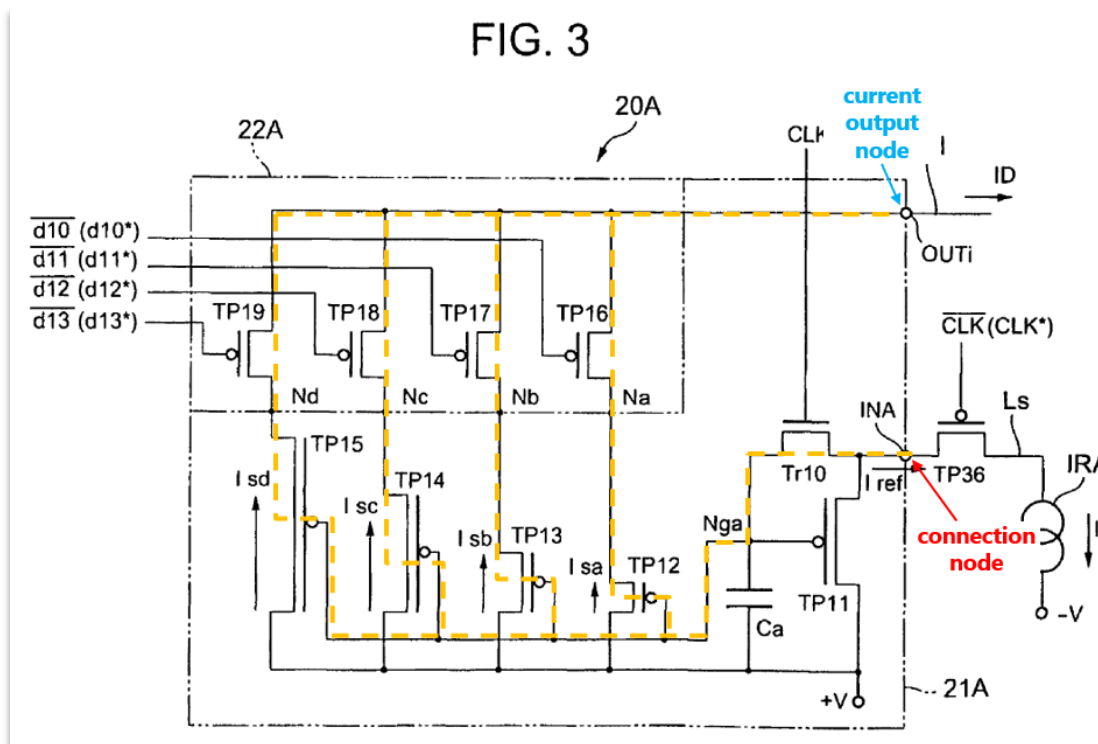
Ex. 1006 (Sasaki) ¶[0074].



Ex. 1006 (Sasaki) at Fig. 10 (annotated).

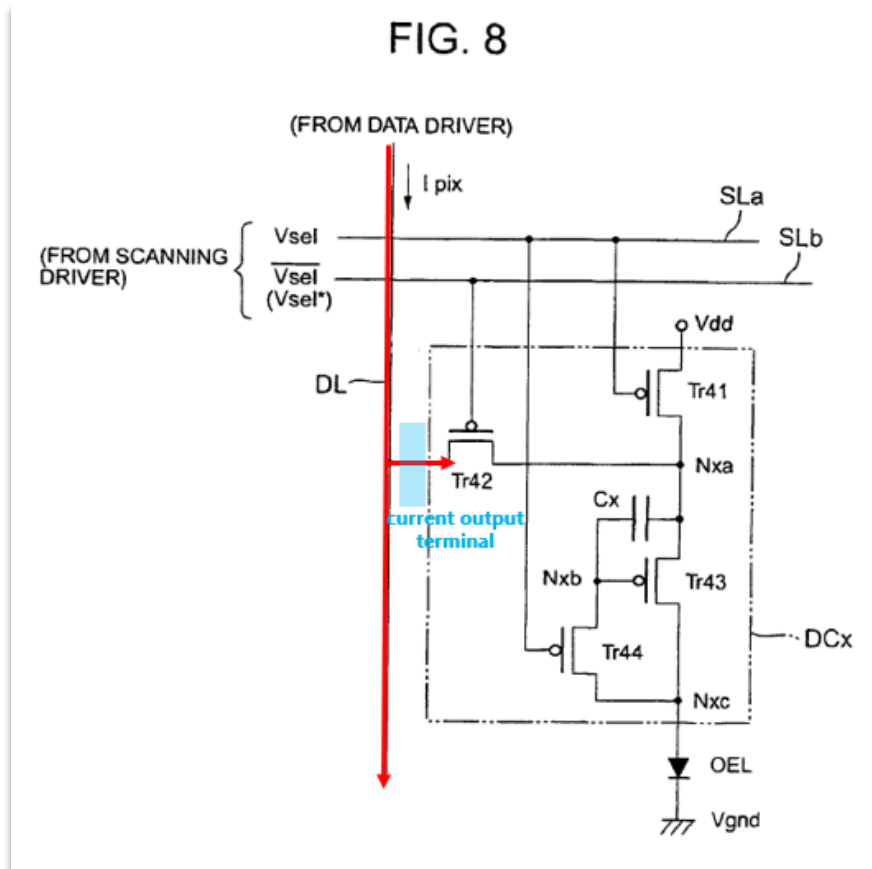
204. Each current output switch (TP311, TP312, or TP31) is connected to a corresponding connection node (current input contact IN_i or IN_A). As shown in

Figure 10 (annotated above), each current output switch is connected to a corresponding output node OUT_i (annotated blue), which is further connected to a corresponding current input contact IN_i (annotated red). Figure 3 of Sasaki below confirms the connection (annotated with yellow dashed lines) between output node OUT_i and input contact IN_i (referred as INA in Figure 3).



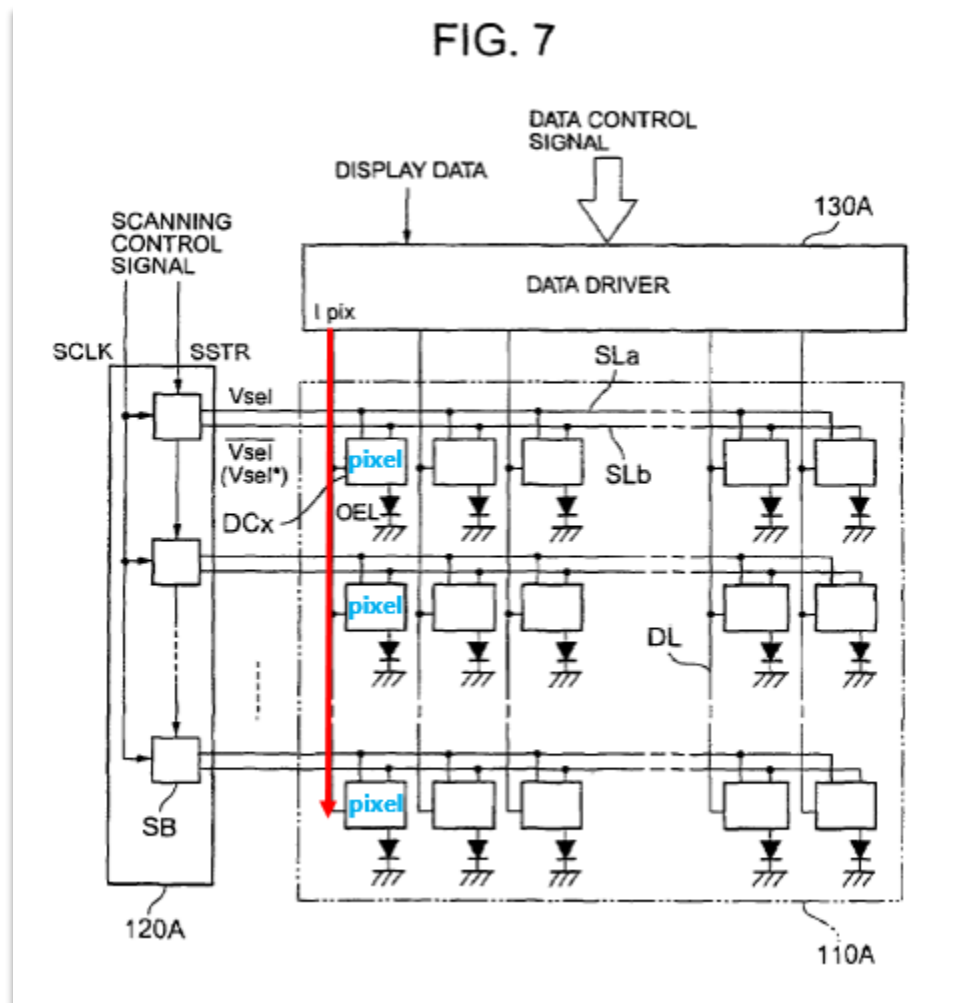
Ex. 1006 (Sasaki) at Fig. 10 (annotated).

205. As shown in Figure 8 below, the terminal (annotated blue) connecting the data line (DL, annotated red) to a pixel driver circuit DCx is an example of the claim current output terminal, outputting gradation currents I_{pix} to a pixel driver circuit DCx. Ex. 1006 (Sasaki) ¶[0116], Fig. 8.



Ex. 1006 (Sasaki) at Fig. 8 (annotated).

206. Sasaki discloses a plurality (two or more) of current output terminals. As shown in Figure 7 below, the data line **DL** (annotated red) is connected to a plurality of pixel driver circuits **DCx** (annotated purple), each of which connected to a corresponding current output terminal. Ex. 1006 (Sasaki) at ¶[0116], Fig. 7.



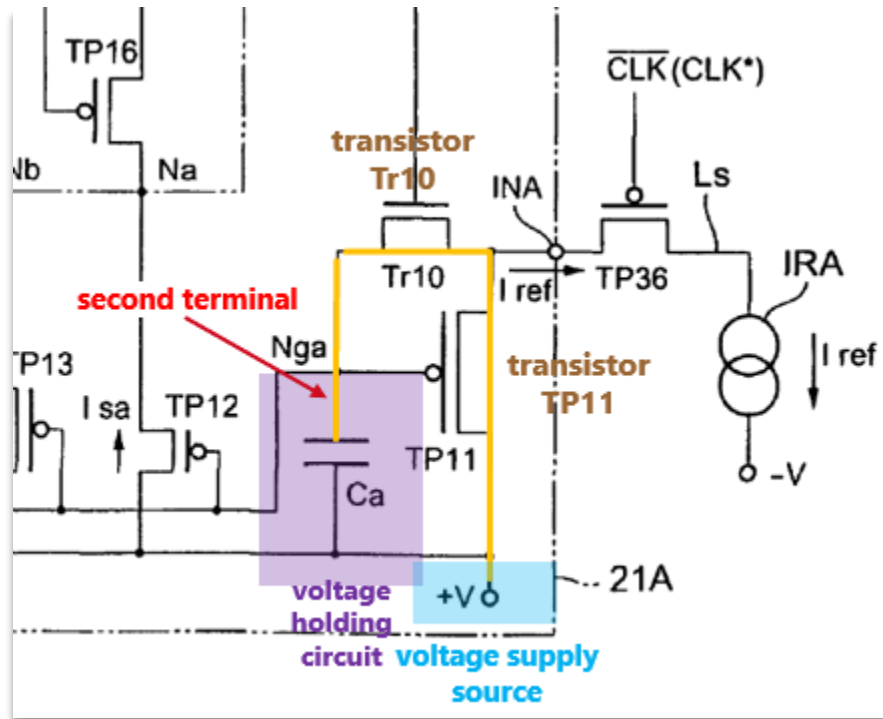
Ex. 1006 (Sasaki) at Fig. 7 (annotated).

207. Each of the current output switches TP311 and 312 is connected to the plurality of current output terminals. As shown in Figures 7, 8, and 10 above, current output switches TP311 and 312 are connected to the data line DL, outputs gradation current I_{pix} , and the data line DL is connected to a plurality of current output terminals located in a plurality of pixel driver circuits DCx.

208. Therefore, each of the current output switches is interposed between the current input node (IN_A) and a plurality of current output terminals.

- i. **10(h): “a high-speed switch for controlling connection/disconnection states of said voltage supply source with respect to the second terminal of said voltage holding circuit.”**

209. Sasaki discloses this limitation. Each of the transistor TP11 and transistor Tr10 is an example of the claimed “high-speed switch.” A POSITA would have recognized that transistors TP11 and Tr10 are high-speed switches, because they can be turned on and off within the timespan of a single frame. A POSITA would further have recognized that a high electric potential +V as an example of the claimed “voltage supply source.” As shown in Figure 3 below, each of transistor TP11 and Tr10 (annotated brown) controls connection/ disconnection states of a high electric potential (annotated blue) with respect to the second terminal of the capacitor Ca (the claimed “voltage holding circuit,” annotated purple). The connection between the high electric potential +V and the capacitor Ca is annotated in gold.



Ex. 1006 (Sasaki) at Fig. 3 (annotated and excerpted).

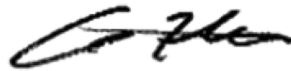
**XV. SECONDARY CONSIDERATIONS OF NON-OBVIOUSNESS
REGARDING THE CHALLENGED PATENT**

210. During prosecution of the Challenged Patent, the applicants did not discuss any secondary considerations of non-obviousness, and I am not aware of any secondary considerations that would support non-obviousness. Should the Patent Owner put forth any alleged evidence of secondary considerations in connection with the Challenged Patent, I reserve the right to consider such evidence, to consider whether any such evidence has a nexus to any claims of the Challenged Patent, and to update my analysis.

XVI. CONCLUSION

211. All statements made herein of my own knowledge are true, and all statements made on information and belief are believed to be true. I further understand that willful false statements and the like are punishable by fine or imprisonment, or both under Section 1001 of Title 18 of the United States Code. I declare under penalty of perjury that the foregoing is true and correct.

Executed on January 31, 2022.



Alex Z. Kattamis, Ph.D., P.E.

APPENDIX A



Alex Z. Kattamis, Ph.D., P.E, CFEI, CVFI

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Professional Profile

Dr. Kattamis is an electrical engineer with an extensive background in failure analysis and forensic engineering. He performs root cause analyses (RCA) relating to failures and fires in electrical systems ranging from semiconductor devices and consumer electronics to power generation, transmission and distribution equipment. Dr. Kattamis has also led large-scale condition assessments of mechanical, electrical, and plumbing (MEP) systems following natural disasters. He has an in depth knowledge of relevant electrical codes and standards including those of the IEC, IEEE, NEC, NESC, NFPA, OSHA, and UL.

Dr. Kattamis has expertise in the design, fabrication, and failure analysis of semiconductor devices including thin-film electronics, flexible electronics, memories, LEDs, LCDs, AMOLEDs, integrated circuits, and printed circuit boards. Dr. Kattamis is also has experience in investigating and providing testimony in intellectual property matters.

Dr. Kattamis received his Ph.D. in Electrical Engineering at Princeton University. His research focused on large-area flexible electronics including the design, fabrication and characterization of TFT display backplanes for electrophoretic displays and AMOLEDs on metal foils and polymer substrates. This included significant work in thin-film mechanics. His fabrication experience includes plasma-enhanced chemical vapor deposition, reactive-ion etching, sputter deposition, wet chemical processing, and photolithography.

Prior to his Ph.D., Dr. Kattamis worked at General Electric Industrial Systems, where he designed and implemented electronic trip units and current sensing systems for metering and switchgear. This included analog electronics design, modeling, and firmware coding.

Academic Credentials & Professional Honors

Ph.D., Electrical Engineering, Princeton University, 2007

M.A., Electrical Engineering, Princeton University, 2004

B.S.E., Electrical Engineering, University of Connecticut, *magna cum laude*, 2002

Princeton Plasma Physics Fellowship Recipient

Tau Beta Pi

Eta Kappa Nu

McGraw Graduate Fellow

General Electric Student Intern Award Recipient

Citigroup Scholarship Recipient

Licenses and Certifications

Licensed Professional Engineer, Connecticut, #PEN.0034121

Licensed Professional Engineer, Georgia, #PE045381

Licensed Professional Engineer, Electrical, Massachusetts, #55240

Licensed Professional Engineer, New York, #090343

Licensed Professional Engineer, Pennsylvania, #PE90289

Licensed Professional Engineer, Electrical, Rhode Island, #13344

Licensed Professional Engineer, Electrical and Computer, Texas, #137167

Certified Fire and Explosion Investigator (CFEI)

Certified Vehicle Fire Investigator (CVFI)

Prior Experience

Research Assistant; Princeton University (2002-2007)

Design Engineer; General Electric Industrial Systems (Summer 2001, 2002)

Professional Affiliations

Institute of Electrical and Electronic Engineers (member)

Society for Information Display (member)

Materials Research Society (member)

Languages

Greek

French

Publications

A. Z. Kattamis, P. F. Murphy, M. Pooley and A. Soane, "Water Infiltration in Common Residential and Commercial Power Cables Introduced by Capillary Action," 2020 IEEE Symposium on Product Compliance Engineering - (SPCE Portland), Portland, OR, USA, 2020, pp. 1-3, doi: 10.1109/SPCE50045.2020.9296167.

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Presentations

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Project Experience

Failure Analysis

- Root cause analysis of medical device failures
- Root cause analysis of lighting device failures

- Root cause analysis of failures in power strips used in data centers
- Hazard analysis for lighting devices
- Root cause analysis for motor run capacitor failures

Flexible Electronic Circuits

- Flexible aluminum substrate characterization
- Amorphous silicon thin-film transistor deposition
- Aluminum substrate passivation and coating for thin-film processing

Hard Disk Drives

- Patent and trade secret investigations relating to hard disk drive intellectual property
- Infringement analysis of accused hard disk drives products
- Prior art and validity analysis of patents related to hard disk drive patents

Light Emitting Devices

- Patent investigations relating to LED and laser diode intellectual property
- Reverse engineering focusing on device processing and characterization
- Infringement analysis of accused LEDs and laser diodes
- Prior art and validity analysis of patents related LEDs and laser diodes

Semiconductor Devices and Materials

- Patent investigations relating to semiconductor devices
- Reverse engineering focusing on packaging, processing and design of memories and other semiconductor devices
- Infringement analysis of accused memories and other semiconductor devices
- Prior art and validity analysis of patents related to memories and other semiconductor devices

Image Processing Software

- Reverse engineering focusing on image processing software and algorithms
- Infringement analysis of accused image processing products
- Prior art and validity analysis of patents related to image processing patents

Computer Networks

- Reverse engineering focusing on computer networks, including networks for providing financial services
- Infringement analysis of accused computer networking products

Fire Investigations

- Cause and origin of fires relating to wiring, electrical equipment and consumer electronics



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Testimony History

Innolux Corporation v. Semiconductor Energy Laboratory Co., Ltd., in the United States Patent and Trademark Office before the Patent and Trial Board, Case No. IPR2013-00064/65, 2013

Maxell, Ltd., et al., v. Huawei Device USA Inc., and Huawei Device Co., Ltd., in the United States District Court Eastern District of Texas, Case No. 5:17-cv-00033, 2019

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