

AO 120 (Rev. 08/10)

TO: Mail Stop 8 Director of the U.S. Patent and Trademark Office P.O. Box 1450 Alexandria, VA 22313-1450	REPORT ON THE FILING OR DETERMINATION OF AN ACTION REGARDING A PATENT OR TRADEMARK
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In Compliance with 35 U.S.C. § 290 and/or 15 U.S.C. § 1116 you are hereby advised that a court action has been filed in the U.S. District Court Eastern District of Texas on the following

☐ Trademarks or ☒ Patents. (☐ the patent action involves 35 U.S.C. § 292.);

DOCKET NO. 2:21-CV-00139	DATE FILED 4/20/2021	U.S. DISTRICT COURT Eastern District of Texas
PLAINTIFF Bishop Display Tech LLC		DEFENDANT Samsung Electronics Co., Ltd.; Samsung Electronics America, Inc.; and Samsung Display Co., Ltd., Korean Corp.
PATENT OR TRADEMARK NO.	DATE OF PATENT OR TRADEMARK	HOLDER OF PATENT OR TRADEMARK
1 6,819,377	11/16/2004	Bishop Display Tech LLC
2 6,822,706	11/23/2004	Bishop Display Tech LLC
3 7,583,347	9/1/2009	Bishop Display Tech LLC
4 7,995,047	8/9/2011	Bishop Display Tech LLC
5 8,093,830	1/10/2012	Bishop Display Tech LLC

In the above—entitled case, the following patent(s)/ trademark(s) have been included:

DATE INCLUDED	INCLUDED BY <input type="checkbox"/> Amendment <input type="checkbox"/> Answer <input type="checkbox"/> Cross Bill <input type="checkbox"/> Other Pleading	
PATENT OR TRADEMARK NO.	DATE OF PATENT OR TRADEMARK	HOLDER OF PATENT OR TRADEMARK
1 8,016,449	9/13/2011	Bishop Display Tech LLC
2		
3		
4		
5		

In the above—entitled case, the following decision has been rendered or judgement issued:

DECISION/JUDGEMENT

CLERK	(BY) DEPUTY CLERK	DATE
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Copy 1—Upon initiation of action, mail this copy to Director Copy 3—Upon termination of action, mail this copy to Director
Copy 2—Upon filing document adding patent(s), mail this copy to Director Copy 4—Case file copy



UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	ISSUE DATE	PATENT NO.	ATTORNEY DOCKET NO.	CONFIRMATION NO.
11/954,659	08/09/2011	7995047	056937-0414	4296

53080 7590 07/20/2011
MCDERMOTT WILL & EMERY LLP
600 13TH STREET, NW
WASHINGTON, DC 20005-3096

ISSUE NOTIFICATION

The projected patent number and issue date are specified above.

Determination of Patent Term Adjustment under 35 U.S.C. 154 (b) (application filed on or after May 29, 2000)

The Patent Term Adjustment is 904 day(s). Any patent to issue from the above-identified application will include an indication of the adjustment on the front page.

If a Continued Prosecution Application (CPA) was filed in the above-identified application, the filing date that determines Patent Term Adjustment is the filing date of the most recent CPA.

Applicant will be able to obtain more detailed information by accessing the Patent Application Information Retrieval (PAIR) WEB site (<http://pair.uspto.gov>).

Any questions regarding the Patent Term Extension or Adjustment determination should be directed to the Office of Patent Legal Administration at (571)-272-7702. Questions relating to issue and publication fee payments should be directed to the Application Assistance Unit (AAU) of the Office of Data Management (ODM) at (571)-272-4200.

APPLICANT(s) (Please see PAIR WEB site <http://pair.uspto.gov> for additional applicants):

Makoto MIZUKI, Kyoto, JAPAN;
Kazuyoshi Nishi, Kyoto, JAPAN;
Tetsuro Ohmori, Osaka, JAPAN;
Tomokazu Kojima, Osaka, JAPAN;
Hiroshi Kojima, Kyoto, JAPAN;

PART B - FEE(S) TRANSMITTAL

Complete and send this form, together with applicable fee(s), to: **Mail** **Mail Stop ISSUE FEE**
Commissioner for Patents
P.O. Box 1450
Alexandria, Virginia 22313-1450
or Fax **(571)-273-2885**

INSTRUCTIONS: This form should be used for transmitting the ISSUE FEE and PUBLICATION FEE (if required). Blocks 1 through 5 should be completed where appropriate. All further correspondence including the Patent, advance orders and notification of maintenance fees will be mailed to the current correspondence address as indicated unless corrected below or directed otherwise in Block 1, by (a) specifying a new correspondence address; and/or (b) indicating a separate "FEE ADDRESS" for maintenance fee notifications.

CURRENT CORRESPONDENCE ADDRESS (Note: Use Block 1 for any change of address)

53080 7590 05/31/2011
MCDERMOTT WILL & EMERY LLP
600 13TH STREET, NW
WASHINGTON, DC 20005-3096

Customer No: 53080

Note: A certificate of mailing can only be used for domestic mailings of the Fee(s) Transmittal. This certificate cannot be used for any other accompanying papers. Each additional paper, such as an assignment or formal drawing, must have its own certificate of mailing or transmission.

Certificate of Mailing or Transmission

I hereby certify that this Fee(s) Transmittal is being deposited with the United States Postal Service with sufficient postage for first class mail in an envelope addressed to the Mail Stop ISSUE FEE address above, or being facsimile transmitted to the USPTO (571) 273-2885, on the date indicated below.

(Depositor's name)
(Signature)
(Date)

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
11/954,659	12/12/2007	Makoto MIZUKI	056937-0414	4296

TITLE OF INVENTION: CURRENT DRIVING DEVICE

APPLN. TYPE	SMALL ENTITY	ISSUE FEE DUE	PUBLICATION FEE DUE	PREV. PAID ISSUE FEE	TOTAL FEE(S) DUE	DATE DUE
nonprovisional	NO	\$1510	\$300	\$0	\$1810	08/31/2011

EXAMINER	ART UNIT	CLASS-SUBCLASS
CHOWDHURY, AFROZA Y	2629	345-204000

1. Change of correspondence address or indication of "Fee Address" (37 CFR 1.363).

- ☐ Change of correspondence address (or Change of Correspondence Address Form PTO/SB/122) attached.
- ☐ "Fee Address" indication (or "Fee Address" Indication form PTO/SB/47; Rev. 03-02 or more recent) attached. **Use of a Customer Number is required.**

2. For printing on the patent front page, list

- (1) the names of up to 3 registered patent attorneys or agents OR, alternatively,
- (2) the name of a single firm (having as a member a registered attorney or agent) and the names of up to 2 registered patent attorneys or agents. If no name is listed, no name will be printed.

MCDERMOTT WILL & EMERY LLP
 2 _____
 3 _____

3. ASSIGNEE NAME AND RESIDENCE DATA TO BE PRINTED ON THE PATENT (print or type)

PLEASE NOTE: Unless an assignee is identified below, no assignee data will appear on the patent. If an assignee is identified below, the document has been filed for recordation as set forth in 37 CFR 3.11. Completion of this form is NOT a substitute for filing an assignment.

(A) NAME OF ASSIGNEE

PANASONIC CORPORATION

(B) RESIDENCE: (CITY and STATE OR COUNTRY)

Osaka, Japan

Please check the appropriate assignee category or categories (will not be printed on the patent): ☐ Individual ☒ Corporation or other private group entity ☐ Government

4a. The following fee(s) are submitted:

- ☒ Issue Fee
- ☒ Publication Fee (No small entity discount permitted)
- ☒ Advance Order - # of Copies **Four (4)**

4b. Payment of Fee(s): (Please first reapply any previously paid issue fee shown above)

- ☐ A check is enclosed.
- ☐ Payment by credit card. Form PTO-2038 is attached.
- ☒ The Director is hereby authorized to charge the required fee(s), any deficiency, or credit any overpayment, to Deposit Account Number **500417** (enclose an extra copy of this form).

5. Change in Entity Status (from status indicated above)

- ☐ a. Applicant claims SMALL ENTITY status. See 37 CFR 1.27. ☐ b. Applicant is no longer claiming SMALL ENTITY status. See 37 CFR 1.27(g)(2).

NOTE: The Issue Fee and Publication Fee (if required) will not be accepted from anyone other than the applicant; a registered attorney or agent; or the assignee or other party in interest as shown by the records of the United States Patent and Trademark Office.

Authorized Signature _____
 Typed or printed name **Michael E. Fogarty**

Date **June 29, 2011**
 Registration No. **36,139**

This collection of information is required by 37 CFR 1.311. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 12 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, Virginia 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, Virginia 22313-1450.

Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it displays a valid OMB control number.

Electronic Patent Application Fee Transmittal				
Application Number:		11954659		
Filing Date:		12-Dec-2007		
Title of Invention:		CURRENT DRIVING DEVICE		
First Named Inventor/Applicant Name:		Makoto MIZUKI		
Filer:		Michael E. Fogarty/stephanie sharrett		
Attorney Docket Number:		056937-0414		
Filed as Large Entity				
Utility under 35 USC 111(a) Filing Fees				
Description	Fee Code	Quantity	Amount	Sub-Total in USD(\$)
Basic Filing:				
Pages:				
Claims:				
Miscellaneous-Filing:				
Petition:				
Patent-Appeals-and-Interference:				
Post-Allowance-and-Post-Issuance:				
Utility Appl issue fee	1501	1	1510	1510
Publ. Fee- early, voluntary, or normal	1504	1	300	300

Description	Fee Code	Quantity	Amount	Sub-Total in USD(\$)
Extension-of-Time:				
Miscellaneous:				
Printed copy of patent - no color	8001	4	3	12
Total in USD (\$)				1822

Electronic Acknowledgement Receipt	
EFS ID:	10419611
Application Number:	11954659
International Application Number:	
Confirmation Number:	4296
Title of Invention:	CURRENT DRIVING DEVICE
First Named Inventor/Applicant Name:	Makoto MIZUKI
Customer Number:	53080
Filer:	Michael E. Fogarty/stephanie sharrett
Filer Authorized By:	Michael E. Fogarty
Attorney Docket Number:	056937-0414
Receipt Date:	29-JUN-2011
Filing Date:	12-DEC-2007
Time Stamp:	17:47:20
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	yes
Payment Type	Deposit Account
Payment was successfully received in RAM	\$1822
RAM confirmation Number	5153
Deposit Account	500417
Authorized User	

File Listing:

Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
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1	Issue Fee Payment (PTO-85B)	IF.PDF	103199 6904f793dd5de4b85bca4a1b0f60d2f73a41638b	no	1
Warnings:					
Information:					
2	Fee Worksheet (SB06)	fee-info.pdf	33504 31cfad2576379be480cfe320151f591e8f4a7d20	no	2
Warnings:					
Information:					
Total Files Size (in bytes):			136703		
<p>This Acknowledgement Receipt evidences receipt on the noted date by the USPTO of the indicated documents, characterized by the applicant, and including page counts, where applicable. It serves as evidence of receipt similar to a Post Card, as described in MPEP 503.</p> <p><u>New Applications Under 35 U.S.C. 111</u> If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application.</p> <p><u>National Stage of an International Application under 35 U.S.C. 371</u> If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.</p> <p><u>New International Application Filed with the USPTO as a Receiving Office</u> If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.</p>					



UNITED STATES PATENT AND TRADEMARK OFFICE

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United States Patent and Trademark Office
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NOTICE OF ALLOWANCE AND FEE(S) DUE

53080 7590 05/31/2011
MCDERMOTT WILL & EMERY LLP
600 13TH STREET, NW
WASHINGTON, DC 20005-3096

EXAMINER

CHOWDHURY, AFROZA Y

ART UNIT

PAPER NUMBER

2629

DATE MAILED: 05/31/2011

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
11/954,659	12/12/2007	Makoto MIZUKI	056937-0414	4296

TITLE OF INVENTION: CURRENT DRIVING DEVICE

APPLN. TYPE	SMALL ENTITY	ISSUE FEE DUE	PUBLICATION FEE DUE	PREV. PAID ISSUE FEE	TOTAL FEE(S) DUE	DATE DUE
nonprovisional	NO	\$1510	\$300	\$0	\$1810	08/31/2011

THE APPLICATION IDENTIFIED ABOVE HAS BEEN EXAMINED AND IS ALLOWED FOR ISSUANCE AS A PATENT. PROSECUTION ON THE MERITS IS CLOSED. THIS NOTICE OF ALLOWANCE IS NOT A GRANT OF PATENT RIGHTS. THIS APPLICATION IS SUBJECT TO WITHDRAWAL FROM ISSUE AT THE INITIATIVE OF THE OFFICE OR UPON PETITION BY THE APPLICANT. SEE 37 CFR 1.313 AND MPEP 1308.

THE ISSUE FEE AND PUBLICATION FEE (IF REQUIRED) MUST BE PAID WITHIN THREE MONTHS FROM THE MAILING DATE OF THIS NOTICE OR THIS APPLICATION SHALL BE REGARDED AS ABANDONED. THIS STATUTORY PERIOD CANNOT BE EXTENDED. SEE 35 U.S.C. 151. THE ISSUE FEE DUE INDICATED ABOVE DOES NOT REFLECT A CREDIT FOR ANY PREVIOUSLY PAID ISSUE FEE IN THIS APPLICATION. IF AN ISSUE FEE HAS PREVIOUSLY BEEN PAID IN THIS APPLICATION (AS SHOWN ABOVE), THE RETURN OF PART B OF THIS FORM WILL BE CONSIDERED A REQUEST TO REAPPLY THE PREVIOUSLY PAID ISSUE FEE TOWARD THE ISSUE FEE NOW DUE.

HOW TO REPLY TO THIS NOTICE:

I. Review the SMALL ENTITY status shown above.

If the SMALL ENTITY is shown as YES, verify your current SMALL ENTITY status:

A. If the status is the same, pay the TOTAL FEE(S) DUE shown above.

B. If the status above is to be removed, check box 5b on Part B - Fee(s) Transmittal and pay the PUBLICATION FEE (if required) and twice the amount of the ISSUE FEE shown above, or

If the SMALL ENTITY is shown as NO:

A. Pay TOTAL FEE(S) DUE shown above, or

B. If applicant claimed SMALL ENTITY status before, or is now claiming SMALL ENTITY status, check box 5a on Part B - Fee(s) Transmittal and pay the PUBLICATION FEE (if required) and 1/2 the ISSUE FEE shown above.

II. PART B - FEE(S) TRANSMITTAL, or its equivalent, must be completed and returned to the United States Patent and Trademark Office (USPTO) with your ISSUE FEE and PUBLICATION FEE (if required). If you are charging the fee(s) to your deposit account, section "4b" of Part B - Fee(s) Transmittal should be completed and an extra copy of the form should be submitted. If an equivalent of Part B is filed, a request to reapply a previously paid issue fee must be clearly made, and delays in processing may occur due to the difficulty in recognizing the paper as an equivalent of Part B.

III. All communications regarding this application must give the application number. Please direct all communications prior to issuance to Mail Stop ISSUE FEE unless advised to the contrary.

IMPORTANT REMINDER: Utility patents issuing on applications filed on or after Dec. 12, 1980 may require payment of maintenance fees. It is patentee's responsibility to ensure timely payment of maintenance fees when due.

PART B - FEE(S) TRANSMITTAL

**Complete and send this form, together with applicable fee(s), to: Mail Mail Stop ISSUE FEE
Commissioner for Patents
P.O. Box 1450
Alexandria, Virginia 22313-1450
or Fax (571)-273-2885**

INSTRUCTIONS: This form should be used for transmitting the ISSUE FEE and PUBLICATION FEE (if required). Blocks 1 through 5 should be completed where appropriate. All further correspondence including the Patent, advance orders and notification of maintenance fees will be mailed to the current correspondence address as indicated unless corrected below or directed otherwise in Block 1, by (a) specifying a new correspondence address; and/or (b) indicating a separate "FEE ADDRESS" for maintenance fee notifications.

CURRENT CORRESPONDENCE ADDRESS (Note: Use Block 1 for any change of address)

53080 7590 05/31/2011
MCDERMOTT WILL & EMERY LLP
600 13TH STREET, NW
WASHINGTON, DC 20005-3096

Note: A certificate of mailing can only be used for domestic mailings of the Fee(s) Transmittal. This certificate cannot be used for any other accompanying papers. Each additional paper, such as an assignment or formal drawing, must have its own certificate of mailing or transmission.

Certificate of Mailing or Transmission

I hereby certify that this Fee(s) Transmittal is being deposited with the United States Postal Service with sufficient postage for first class mail in an envelope addressed to the Mail Stop ISSUE FEE address above, or being facsimile transmitted to the USPTO (571) 273-2885, on the date indicated below.

(Depositor's name)
(Signature)
(Date)

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
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11/954,659	12/12/2007	Makoto MIZUKI	056937-0414	4296
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TITLE OF INVENTION: CURRENT DRIVING DEVICE

APPLN. TYPE	SMALL ENTITY	ISSUE FEE DUE	PUBLICATION FEE DUE	PREV. PAID ISSUE FEE	TOTAL FEE(S) DUE	DATE DUE
nonprovisional	NO	\$1510	\$300	\$0	\$1810	08/31/2011

EXAMINER	ART UNIT	CLASS-SUBCLASS
CHOWDHURY, AFROZA Y	2629	345-204000

1. Change of correspondence address or indication of "Fee Address" (37 CFR 1.363).

- ☐ Change of correspondence address (or Change of Correspondence Address form PTO/SB/122) attached.
- ☐ "Fee Address" indication (or "Fee Address" Indication form PTO/SB/47; Rev 03-02 or more recent) attached. **Use of a Customer Number is required.**

2. For printing on the patent front page, list

- (1) the names of up to 3 registered patent attorneys or agents OR, alternatively, 1 _____
- (2) the name of a single firm (having as a member a registered attorney or agent) and the names of up to 2 registered patent attorneys or agents. If no name is listed, no name will be printed. 2 _____
- 3 _____

3. ASSIGNEE NAME AND RESIDENCE DATA TO BE PRINTED ON THE PATENT (print or type)

PLEASE NOTE: Unless an assignee is identified below, no assignee data will appear on the patent. If an assignee is identified below, the document has been filed for recordation as set forth in 37 CFR 3.111. Completion of this form is NOT a substitute for filing an assignment.

(A) NAME OF ASSIGNEE

(B) RESIDENCE: (CITY and STATE OR COUNTRY)

Please check the appropriate assignee category or categories (will not be printed on the patent): ☐ Individual ☐ Corporation or other private group entity ☐ Government

4a. The following fee(s) are submitted:

- ☐ Issue Fee
- ☐ Publication Fee (No small entity discount permitted)
- ☐ Advance Order - # of Copies _____

4b. Payment of Fee(s): (Please first reapply any previously paid issue fee shown above)

- ☐ A check is enclosed.
- ☐ Payment by credit card. Form PTO-2038 is attached.
- ☐ The Director is hereby authorized to charge the required fee(s), any deficiency, or credit any overpayment, to Deposit Account Number _____ (enclose an extra copy of this form).

5. Change in Entity Status (from status indicated above)

- ☐ a. Applicant claims SMALL ENTITY status. See 37 CFR 1.27. ☐ b. Applicant is no longer claiming SMALL ENTITY status. See 37 CFR 1.27(g)(2).

NOTE: The Issue Fee and Publication Fee (if required) will not be accepted from anyone other than the applicant; a registered attorney or agent; or the assignee or other party in interest as shown by the records of the United States Patent and Trademark Office.

Authorized Signature _____

Date _____

Typed or printed name _____

Registration No. _____

This collection of information is required by 37 CFR 1.311. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 12 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, Virginia 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, Virginia 22313-1450.

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UNITED STATES DEPARTMENT OF COMMERCE
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www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
11/954,659	12/12/2007	Makoto MIZUKI	056937-0414	4296
53080	7590	05/31/2011	EXAMINER	
MCDERMOTT WILL & EMERY LLP			CHOWDHURY, AFROZA Y	
600 13TH STREET, NW			ART UNIT	PAPER NUMBER
WASHINGTON, DC 20005-3096			2629	

DATE MAILED: 05/31/2011

Determination of Patent Term Adjustment under 35 U.S.C. 154 (b) (application filed on or after May 29, 2000)

The Patent Term Adjustment to date is 664 day(s). If the issue fee is paid on the date that is three months after the mailing date of this notice and the patent issues on the Tuesday before the date that is 28 weeks (six and a half months) after the mailing date of this notice, the Patent Term Adjustment will be 664 day(s).

If a Continued Prosecution Application (CPA) was filed in the above-identified application, the filing date that determines Patent Term Adjustment is the filing date of the most recent CPA.

Applicant will be able to obtain more detailed information by accessing the Patent Application Information Retrieval (PAIR) WEB site (<http://pair.uspto.gov>).

Any questions regarding the Patent Term Extension or Adjustment determination should be directed to the Office of Patent Legal Administration at (571)-272-7702. Questions relating to issue and publication fee payments should be directed to the Customer Service Center of the Office of Patent Publication at 1-(888)-786-0101 or (571)-272-4200.

Privacy Act Statement

The Privacy Act of 1974 (P.L. 93-579) requires that you be given certain information in connection with your submission of the attached form related to a patent application or patent. Accordingly, pursuant to the requirements of the Act, please be advised that: (1) the general authority for the collection of this information is 35 U.S.C. 2(b)(2); (2) furnishing of the information solicited is voluntary; and (3) the principal purpose for which the information is used by the U.S. Patent and Trademark Office is to process and/or examine your submission related to a patent application or patent. If you do not furnish the requested information, the U.S. Patent and Trademark Office may not be able to process and/or examine your submission, which may result in termination of proceedings or abandonment of the application or expiration of the patent.

The information provided by you in this form will be subject to the following routine uses:

1. The information on this form will be treated confidentially to the extent allowed under the Freedom of Information Act (5 U.S.C. 552) and the Privacy Act (5 U.S.C. 552a). Records from this system of records may be disclosed to the Department of Justice to determine whether disclosure of these records is required by the Freedom of Information Act.
2. A record from this system of records may be disclosed, as a routine use, in the course of presenting evidence to a court, magistrate, or administrative tribunal, including disclosures to opposing counsel in the course of settlement negotiations.
3. A record in this system of records may be disclosed, as a routine use, to a Member of Congress submitting a request involving an individual, to whom the record pertains, when the individual has requested assistance from the Member with respect to the subject matter of the record.
4. A record in this system of records may be disclosed, as a routine use, to a contractor of the Agency having need for the information in order to perform a contract. Recipients of information shall be required to comply with the requirements of the Privacy Act of 1974, as amended, pursuant to 5 U.S.C. 552a(m).
5. A record related to an International Application filed under the Patent Cooperation Treaty in this system of records may be disclosed, as a routine use, to the International Bureau of the World Intellectual Property Organization, pursuant to the Patent Cooperation Treaty.
6. A record in this system of records may be disclosed, as a routine use, to another federal agency for purposes of National Security review (35 U.S.C. 181) and for review pursuant to the Atomic Energy Act (42 U.S.C. 218(c)).
7. A record from this system of records may be disclosed, as a routine use, to the Administrator, General Services, or his/her designee, during an inspection of records conducted by GSA as part of that agency's responsibility to recommend improvements in records management practices and programs, under authority of 44 U.S.C. 2904 and 2906. Such disclosure shall be made in accordance with the GSA regulations governing inspection of records for this purpose, and any other relevant (i.e., GSA or Commerce) directive. Such disclosure shall not be used to make determinations about individuals.
8. A record from this system of records may be disclosed, as a routine use, to the public after either publication of the application pursuant to 35 U.S.C. 122(b) or issuance of a patent pursuant to 35 U.S.C. 151. Further, a record may be disclosed, subject to the limitations of 37 CFR 1.14, as a routine use, to the public if the record was filed in an application which became abandoned or in which the proceedings were terminated and which application is referenced by either a published application, an application open to public inspection or an issued patent.
9. A record from this system of records may be disclosed, as a routine use, to a Federal, State, or local law enforcement agency, if the USPTO becomes aware of a violation or potential violation of law or regulation.

DETAILED ACTION

Allowable Subject Matter

1. Claims 1-10 are allowed.
2. The following is an examiner's statement of reasons for allowance:
As argued by the Applicants in the Remarks, dated **March 7, 2011**, the cited references have failed to teach **"disclose that a voltage holding circuit has a terminal being connected to a reference voltage different from the first voltage, and under the voltage supply mode, the first voltage is supplied to another terminal of the voltage holding circuit"** in combination with other limitations of claim 1, and **"the voltage holding circuit has a first terminal and a second terminal, the first terminal being connected to a fixed voltage, and the current driving device includes a high-speed switch for controlling connection/disconnection states of said voltage supply source with respect to the second terminal of said voltage holding circuit"** in combination with other limitations of claim 10.

Any comments considered necessary by applicant must be submitted no later than the payment of the issue fee and, to avoid processing delays, should preferably accompany the issue fee. Such submissions should be clearly labeled "Comments on Statement of Reasons for Allowance."

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to AFROZA CHOWDHURY whose telephone number is (571)270-1543. The examiner can normally be reached on 8:00-5:30 EST, 5/4/9.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, BIPIN SHALWALA can be reached on (571)272-7681. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

AC
5/19/2011

/Bipin Shalwala/
Supervisory Patent Examiner, Art
Unit 2629

Notice of References Cited	Application/Control No. 11/954,659	Applicant(s)/Patent Under Reexamination MIZUKI ET AL.	
	Examiner AFROZA CHOWDHURY	Art Unit 2629	Page 1 of 1

U.S. PATENT DOCUMENTS

*		Document Number Country Code-Number-Kind Code	Date MM-YYYY	Name	Classification
*	A	US-7,466,166	12-2008	Date et al.	327/108
*	B	US-7,221,349	05-2007	Hashido et al.	345/89
*	C	US-6,628,274	09-2003	Morita, Akira	345/209
*	D	US-7,064,969	06-2006	West, Richard T.	363/132
*	E	US-7,864,167	01-2011	Morosawa et al.	345/204
*	F	US-7,012,597	03-2006	Kasai, Toshiyuki	345/204
*	G	US-6,777,885	08-2004	Koyama, Jun	315/169.1
*	H	US-2004/0239668	12-2004	Morosawa et al.	345/212
*	I	US-2004/0108988	06-2004	Choi, Chang-Hwe	345/096
*	J	US-2002/0135314	09-2002	Kitahara et al.	315/169.3
*	K	US-6,882,186	04-2005	Nishitoba, Shigeo	327/108
*	L	US-6,777,885	08-2004	Koyama, Jun	315/169.1
*	M	US-6,765,560	07-2004	Ozawa, Tokuroh	345/204

FOREIGN PATENT DOCUMENTS

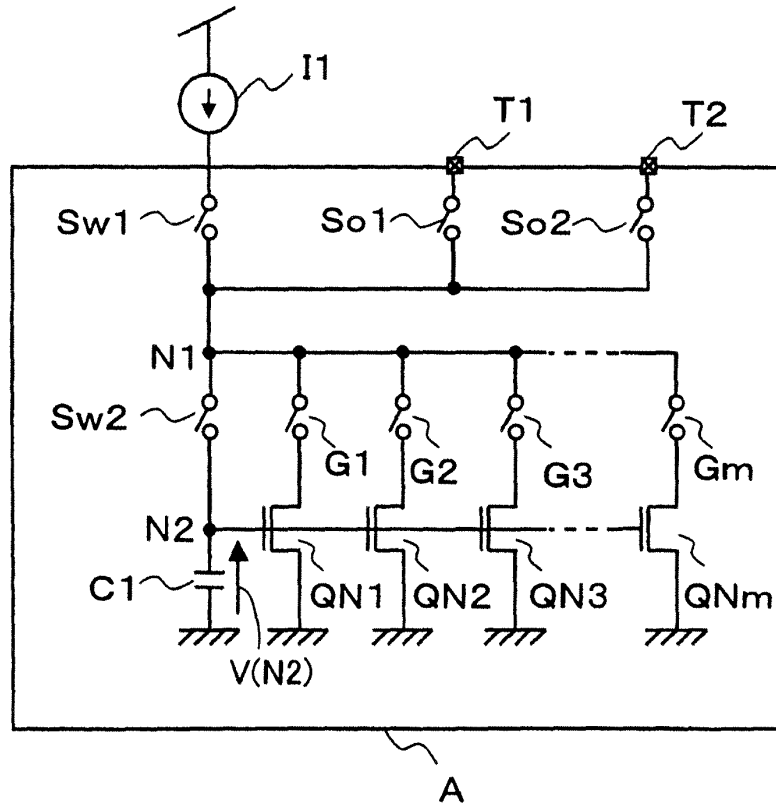
*		Document Number Country Code-Number-Kind Code	Date MM-YYYY	Country	Name	Classification
	N					
	O					
	P					
	Q					
	R					
	S					
	T					

NON-PATENT DOCUMENTS

*		Include as applicable: Author, Title Date, Publisher, Edition or Volume, Pertinent Pages)
	U	
	V	
	W	
	X	

*A copy of this reference is not being furnished with this Office action. (See MPEP § 707.05(a).)
Dates in MM-YYYY format are publication dates. Classifications may be US or foreign.

F I G. 6 A Prior Art



F I G. 6 B Prior Art

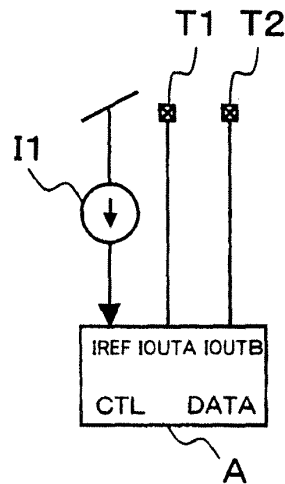
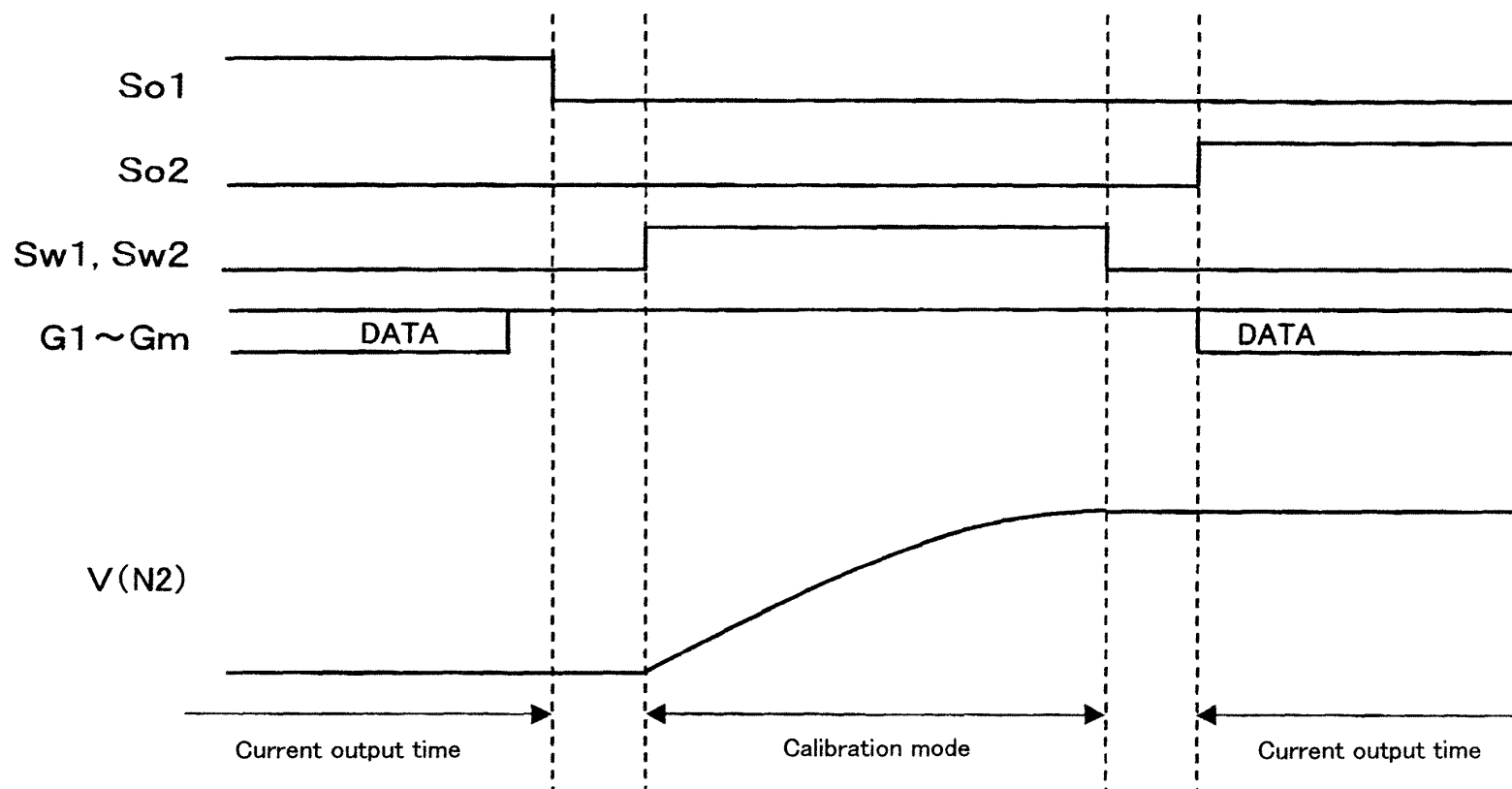


FIG. 7 Prior Art



F I G. 8 Prior Art

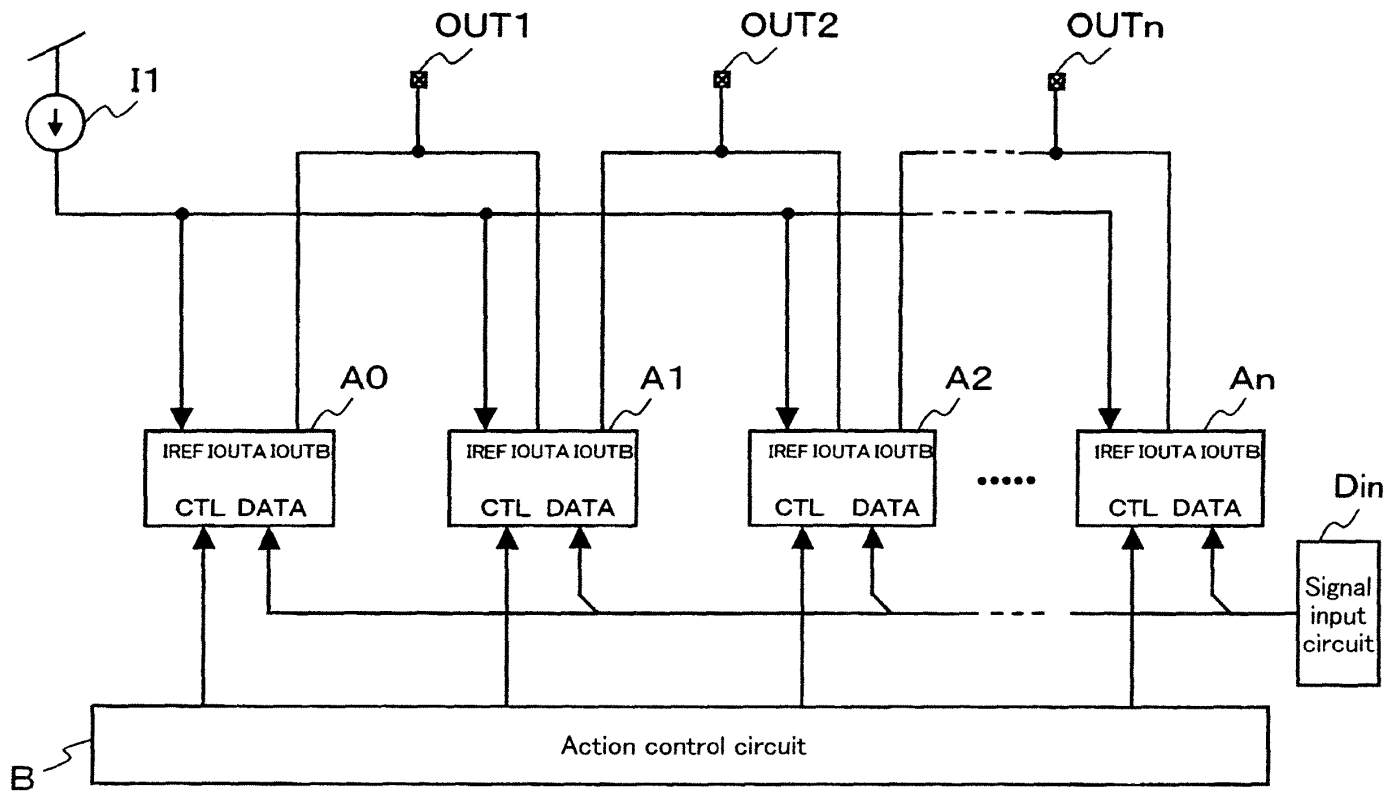
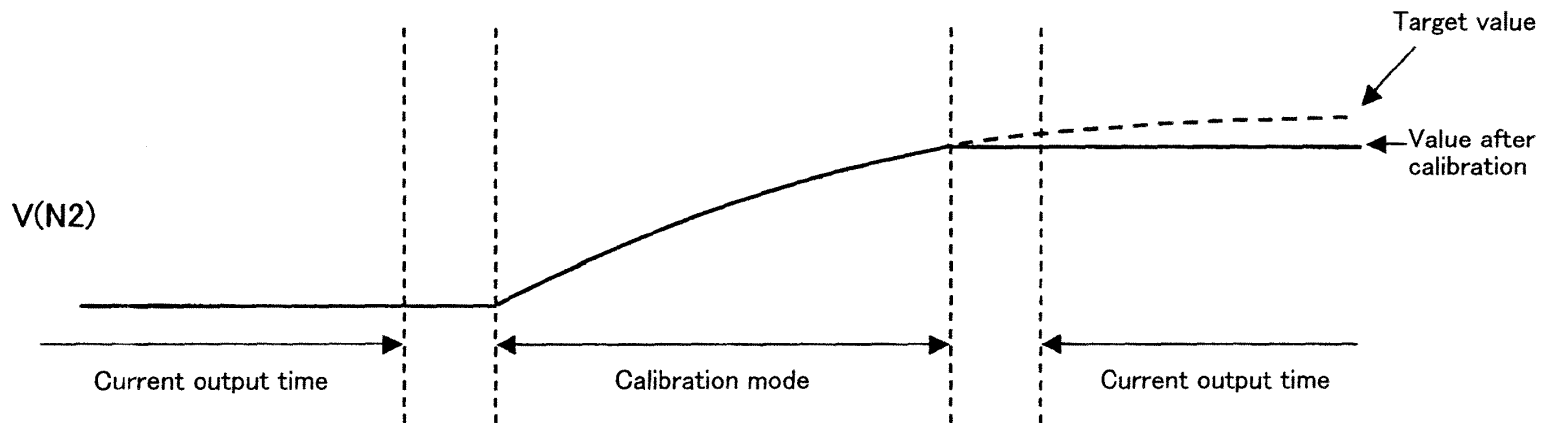


FIG. 9 Prior Art





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BIB DATA SHEET

CONFIRMATION NO. 4296

SERIAL NUMBER	FILING or 371(c) DATE	CLASS	GROUP ART UNIT	ATTORNEY DOCKET NO.		
11/954,659	12/12/2007	345	2629	056937-0414		
APPLICANTS Makoto MIZUKI, Kyoto, JAPAN; Kazuyoshi Nishi, Kyoto, JAPAN; Tetsuro Ohmori, Osaka, JAPAN; Tomokazu Kojima, Osaka, JAPAN; Hiroshi Kojima, Kyoto, JAPAN;						
** CONTINUING DATA ***** ** FOREIGN APPLICATIONS ***** JAPAN 2006-335850 12/13/2006 ** IF REQUIRED, FOREIGN FILING LICENSE GRANTED **						
Foreign Priority claimed <input checked="" type="checkbox"/> Yes <input type="checkbox"/> No	35 USC 119(a-d) conditions met <input checked="" type="checkbox"/> Yes <input type="checkbox"/> No	<input type="checkbox"/> Met after Allowance AC	STATE OR COUNTRY JAPAN	SHEETS DRAWINGS 9	TOTAL CLAIMS 10	INDEPENDENT CLAIMS 2
Verified and Acknowledged	/AFROZA Y CHOWDHURY/ Examiner's Signature		Initials			
ADDRESS MCDERMOTT WILL & EMERY LLP 600 13TH STREET, NW WASHINGTON, DC 20005-3096 UNITED STATES						
TITLE CURRENT DRIVING DEVICE						
FILING FEE RECEIVED 1030	FEES: Authority has been given in Paper No. _____ to charge/credit DEPOSIT ACCOUNT No. _____ for following:			<input type="checkbox"/> All Fees		
				<input type="checkbox"/> 1.16 Fees (Filing)		
				<input type="checkbox"/> 1.17 Fees (Processing Ext. of time)		
				<input type="checkbox"/> 1.18 Fees (Issue)		
				<input type="checkbox"/> Other _____		
			<input type="checkbox"/> Credit			

SHEET 1 OF 1

INFORMATION DISCLOSURE STATEMENT BY APPLICANT (Substitute for form 1449/PTO)				ATTY. DOCKET NO. 056937-0414		SERIAL NO. Not Yet Assigned 11954659	
				APPLICANT Makoto MIZUKI, et al.			
				FILING DATE December 12, 2007		GROUP 2629 Not Yet Assigned	
U.S. PATENT DOCUMENTS							
EXAMINER'S INITIALS	CITE NO.	Document Number Number-Kind Code ² (if known)	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear		
/A.C./		US 2005/0231241 A1	10-20-2005	Date, et al.	Corresponds w/ JP 2005-311591		
/A.C./		US 2004/0251844 A1	12-16-2004	Hashido et al.			
/A.C./		US 7,050,024 B2	05-23-2006	LeChevalier			
/A.C./		US 6,594,606 B2	07-15-2003	Everitt			
/A.C./		US 2006/0158402 A1	07-20-2006	Nathan et al.			
FOREIGN PATENT DOCUMENTS							
EXAMINER'S INITIALS	CITE NO.	Foreign Patent Document Country Code ² -Number 4-Kind Codes (if known)	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines Where Relevant Figures Appear	Translation Yes No	
/A.C./		JP 2005-311591	11-04-2005	MATSUSHITA ELECTRIC IND CO LTD	Corresponds w/ US 2005/0231241 A1	English Abstract	
/A.C./		JP 2004-219955	08-05-2004	TOSHIBA MATSUSHITA DISPLAY TECHNOLOGY CO LTD		English Abstract	
/A.C./		JP 2005-121843	05-12-2005	TOSHIBA MATSUSHITA DISPLAY TECHNOLOGY CO LTD		English Abstract	
OTHER ART (Including Author, Title, Date, Pertinent Pages, Etc.)							
EXAMINER'S INITIALS	CITE NO.	Include name of the author (in CAPITAL LETTERS), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.					
EXAMINER /Afroza Chowdhury/				DATE CONSIDERED 05/25/2011			

*EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.

1 Applicant's unique citation designation number (optional). 2 Applicant is to place a check mark here if English language Translation is attached.

EAST Search History

EAST Search History (Prior Art)

Ref #	Hits	Search Query	DBs	Default Operator	Plurals	Time Stamp
L1	5359	345/204.ccls.	US-PGPUB; USPAT; USOCR	OR	ON	2011/05/19 09:55
L2	3018	327/108.ccls.	US-PGPUB; USPAT; USOCR	OR	ON	2011/05/19 09:55
L3	14	(current near driv\$3) same (voltage adj holding adj circuit)	US-PGPUB; USPAT; USOCR	OR	ON	2011/05/19 09:57
L4	555	mizuki.in.	US-PGPUB; USPAT; USOCR	OR	ON	2011/05/19 09:58
L5	4	1 and 4	US-PGPUB; USPAT; USOCR	OR	ON	2011/05/19 09:58
L6	19	1 and 2	US-PGPUB; USPAT; USOCR	OR	ON	2011/05/19 09:59
L7	0	5 and (voltage adj holding adj circuit)	US-PGPUB; USPAT; USOCR	OR	ON	2011/05/19 09:59
L8	0	6 and (voltage adj holding adj circuit)	US-PGPUB; USPAT; USOCR	OR	ON	2011/05/19 09:59
L9	2	4 and (voltage adj holding adj circuit)	US-PGPUB; USPAT; USOCR	OR	ON	2011/05/19 09:59
L10	4	(current near driv\$3) same (voltage adj holding adj circuit)	EPO; JPO; DERWENT	OR	ON	2011/05/19 10:01
L15	7562349	"12" and "11"	US-PGPUB; USPAT; USOCR	OR	ON	2011/05/19 10:02
L19	0	(voltage adj holding adj circuit) same (reference adj voltage) near5 different near5 (first near voltage)	US-PGPUB; USPAT; USOCR	OR	ON	2011/05/19 10:09


L20	2	(voltage adj holding adj circuit) same (reference adj voltage) near5 different near5 (voltage)	US-PGPUB; USPAT; USOCR	OR	ON	2011/05/19 10:10
L21	6	(voltage adj holding adj circuit) same (reference near voltage) same different	US-PGPUB; USPAT; USOCR	OR	ON	2011/05/19 10:17
L22	0	(voltage adj holding adj circuit) same (first second) near terminal same (high \$1speed near2 switch)	US-PGPUB; USPAT; USOCR	OR	ON	2011/05/19 10:20
L24	0	(voltage adj holding adj circuit) same (first second) near terminal same (high \$1speed near2 switch)	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT	OR	ON	2011/05/19 10:20
L25	0	(voltage adj holding adj circuit) same (high\$1speed near2 switch)	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT	OR	ON	2011/05/19 10:20
L27	0	(voltage adj holding adj circuit) same (high\$1speed near2 switch \$3)	US-PGPUB; USPAT; USOCR	OR	ON	2011/05/19 10:21

EAST Search History (I nterference)

Ref #	Hits	Search Query	DBs	Default Operator	Plurals	Time Stamp
L11	14	(current near driv\$3) same (voltage adj holding adj circuit)	US-PGPUB; USPAT; UPAD	OR	ON	2011/05/19 10:01

L12	5356	345/204.ccls.	US-PGPUB; USPAT; UPAD	OR	ON	2011/05/19 10:01
L13	2918	327/108.ccls.	US-PGPUB; USPAT; UPAD	OR	ON	2011/05/19 10:01
L14	547	mizuki.in.	US-PGPUB; USPAT; UPAD	OR	ON	2011/05/19 10:01
L16	2	11 and 12	US-PGPUB; USPAT; UPAD	OR	ON	2011/05/19 10:02
L17	1	11 and 13	US-PGPUB; USPAT; UPAD	OR	ON	2011/05/19 10:02
L18	28	("20020021293" "20020041276" "20020084812" "20020135314" "20030040149" "20030048669" "20030058199" "20030128200" "20030151616" "20040075621" "20040108998" "20040239668" "20040263437" "20050017765" "20050017931" "20050057580" "20050157581" "20070217275" "6266000" "6323631" "6528951" "6556176" "6765560" "6777885" "6882186" "7012597" "7091937" "7256756").PN. OR ("7864167").URPN.	US-PGPUB; USPAT	OR	ON	2011/05/19 10:04
L23	0	(voltage adj holding adj circuit) same (first second) near terminal same (high\$1speed near2 switch)	US-PGPUB; USPAT; UPAD	OR	ON	2011/05/19 10:20
L26	0	(voltage adj holding adj circuit) same (high \$1speed near2 switch)	US-PGPUB; USPAT; UPAD	OR	ON	2011/05/19 10:21

5/ 19/ 2011 10:21:57 AM


<i>Search Notes</i> 	Application/Control No. 11954659	Applicant(s)/Patent Under Reexamination MIZUKI ET AL.
	Examiner AFROZA Y CHOWDHURY	Art Unit 2629

SEARCHED			
Class	Subclass	Date	Examiner
345	204	5/19/2011	AC
327	108	5/19/2011	AC

SEARCH NOTES		
Search Notes	Date	Examiner
EAST		AC

INTERFERENCE SEARCH			
Class	Subclass	Date	Examiner
updated search	all of the above	5/19/2011	AC


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Issue Classification 	Application/Control No. 11954659	Applicant(s)/Patent Under Reexamination MIZUKI ET AL.
	Examiner AFROZA CHOWDHURY	Art Unit 2629

ORIGINAL						INTERNATIONAL CLASSIFICATION												
CLASS		SUBCLASS				CLAIMED					NON-CLAIMED							
345		204				G	0	5	F	1 / 10 (2006.0)								
CROSS REFERENCE(S)																		
CLASS	SUBCLASS (ONE SUBCLASS PER BLOCK)																	
327	108																	

<input checked="" type="checkbox"/> Claims renumbered in the same order as presented by applicant <input type="checkbox"/> CPA <input type="checkbox"/> T.D. <input type="checkbox"/> R.1.47															
Final	Original	Final	Original	Final	Original	Final	Original	Final	Original	Final	Original	Final	Original	Final	Original
	1														
	2														
	3														
	4														
	5														
	6														
	7														
	8														
	9														
	10														

/AFROZA CHOWDHURY/ Examiner.Art Unit 2629 (Assistant Examiner)	5/19/2011 (Date)	Total Claims Allowed: 10	
/BIPIN SHALWALA/ Supervisory Patent Examiner.Art Unit 2629 (Primary Examiner)	05/19/2011 (Date)	O.G. Print Claim(s) 1	O.G. Print Figure 3

<i>Index of Claims</i> 	Application/Control No. 11954659	Applicant(s)/Patent Under Reexamination MIZUKI ET AL.
	Examiner AFROZA Y CHOWDHURY	Art Unit 2629

✓	Rejected	-	Cancelled	N	Non-Elected	A	Appeal
=	Allowed	÷	Restricted	I	Interference	O	Objected

<input checked="" type="checkbox"/> Claims renumbered in the same order as presented by applicant				<input type="checkbox"/> CPA		<input type="checkbox"/> T.D.		<input type="checkbox"/> R.1.47	
CLAIM		DATE							
Final	Original	12/02/2010	05/19/2011						
	1	✓	=						
	2	✓	=						
	3	✓	=						
	4	✓	=						
	5	✓	=						
	6	✓	=						
	7	✓	=						
	8	✓	=						
	9	✓	=						
	10	✓	=						

Docket No.: 056937-0414

PATENT

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of	:	Customer Number: 53080
	:	
Makoto MIZUKI, et al.	:	Confirmation Number: 4296
	:	
Application No.: 11/954,659	:	Group Art Unit: 2629
	:	
Filed: December 12, 2007	:	Examiner: Afroza Y. Chowdhury
	:	
For: CURRENT DRIVING DEVICE	:	

AMENDMENT

Mail Stop Amendment
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Sir:

In response to the Office Action dated December 8, 2010, wherein a three-month shortened statutory period for response is set to expire on March 8, 2011, Applicants respectfully request reconsideration of the above-identified application in view of the following amendments and remarks.

Attachment: Replacement Sheets (4)

AMENDMENT TO THE CLAIMS

The following claim listing replaces all prior listings and versions of the claims:

LISTING OF CLAIMS

1. (Currently Amended) A current driving device, comprising:

a first voltage supply [[part]] source for supplying a first voltage;

a first current supply [[part]] source for supplying a first electric current;

a plurality of output terminals; and

a plurality of current output [[parts]] circuits for outputting an electric current in accordance with said first electric current, each of said current output [[parts]] circuits comprising a current-voltage converting ~~function~~ circuit, a voltage-current converting ~~function~~ circuit, a voltage holding [[part]] circuit having a terminal being connected to a reference voltage different from the first voltage, and at least one current output terminal, wherein:

each of said current output ~~part takes~~ circuits operates in three operation modes [[, i.e.]] including a voltage supply mode, a current supply mode, and a current output mode,

under said voltage supply mode, each of said current output [[part]] circuits receives said first voltage from said first voltage supply [[part]] source, and ~~holds said voltage in the first voltage~~ is supplied to another terminal of said voltage holding [[part]] circuit,

under said current supply mode, each of said current output [[part]] circuits receives said first current from said first current supply [[part]] source, and generates a second voltage by said current-voltage converting ~~function~~ circuit, and ~~holds said voltage in the first current is supplied to~~ said another terminal of said voltage holding [[part]] circuit, and

under said current output mode, each of said current output ~~[[part]]~~ circuits outputs an output current according to said voltage held in said voltage holding ~~[[part]]~~ circuit by said voltage-current converting ~~function~~ circuit.

2. (Currently Amended) The current driving device according to claim 1, wherein:
each of said output terminals is connected to said current output terminals provided to said plurality of said current output ~~[[parts]]~~ circuits, and
each of said plurality of current output ~~[[parts]]~~ circuits is connected in parallel to said first current supply ~~[[part]]~~ source and said first voltage supply ~~[[part]]~~ source used in common.

3. (Currently Amended) The current driving device according to claim 1, wherein, in each of said current output ~~[[parts]]~~ circuits, ~~actuates~~ said current-voltage converting ~~function~~ circuit is actuated under said voltage supply mode.

4. (Currently Amended) The current driving device according to claim 1, wherein each of said current output ~~[[parts]]~~ circuits is configured to stop ~~comprises a function of stopping~~ said current-voltage converting ~~function~~ circuit under said voltage supply mode.

5. (Currently Amended) The current driving device according to ~~[[claims]]~~ claim 1, further comprising:

a second current supply ~~[[part]]~~ source for supplying a second electric current that is proportional to said first electric current; ~~[[,]]~~ and

a second current-voltage converting circuit for generating said first voltage by receiving said second electric current, wherein

said first voltage supply source controls supplies of said first voltage generated by said second current-voltage converting circuit to said current output circuits.

6. (Currently Amended) The current driving device according to claim 5, wherein said second current-voltage converting circuit comprises a switching part for short-circuiting a node at which said first voltage emerges to a reference voltage node.

7. (Currently Amended) The current driving device according to claim 1, further comprising a second voltage supply source with a larger voltage supply capacity than that of said first voltage supply source, wherein

the use of said first voltage supply source and the use of said second voltage supply source are switched in accordance with the number of said current output circuits that operate in said voltage supply mode among said plurality of current output circuits.

8. (Currently Amended) The current driving device according to claim 1, wherein said first voltage supply source is configured to change ~~constituted to be capable of changing~~ its voltage supply capacity in accordance with the number of said current output circuits that operate in said voltage supply mode among said plurality of current output circuits.

9. (Currently Amended) A current-driving-type display device, comprising said current driving device according to ~~[[claims]]~~ claim 1 mounted thereon so as to be driven by said current driving device.

10. (Currently Amended) A current driving device, comprising:

a current input switch for controlling connection/disconnection states with respect to a current supply ~~[[part]]~~ source;

a voltage holding ~~[[part]]~~ circuit for holding a reference voltage, which is charged by a flown current, the voltage holding circuit having a first terminal and a second terminal, the first terminal being connected to a fixed voltage;

a calibration switch interposed between said current input switch and said voltage holding ~~[[part]]~~ circuit;

a plurality of voltage-current converting elements for generating an electric current in accordance with said reference voltage held in said voltage holding ~~[[part]]~~ circuit;

a plurality of signal response switches that are on/off controlled in accordance with inputted signals, each of said response switches being connected in series to a corresponding one ~~[[each]]~~ of said voltage-current converting elements, and each of which being connected in parallel to said calibration switch;

a connection node provided between said current input switch and said calibration switch;

a plurality of current output switches, each being interposed between ~~[[a]]~~ the connection node, ~~which is provided between said current input switch and said calibration switch~~, and said plurality of current output terminals; and

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a ~~high-speeding~~ high-speed switch for controlling connection/disconnection states of said voltage supply ~~[[part]]~~ source with respect to the second terminal of said voltage holding ~~[[part]]~~ circuit.

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AMENDMENT TO THE DRAWINGS

The attached drawing sheets replace the original sheets including FIGS. 6A, 6B and 7-9.

In the amendment, these figures have been labeled with a “Prior Art” legend.

Attachment: Replacement Sheets (4)

REMARKS

Status of Claims

Claims 1-10 are pending, of which claims 1 and 10 are independent.

Claims 1-10 have been amended to correct informalities in the claim language and to more clearly define the claimed subject matter. Support for the amendment is found, for example, in FIGS. 1A and 3. No new matter has been added.

Objection to the Drawings

The Examiner objected to the drawings. Applicants respectfully submit that the amendment made to the drawings overcome this objection.

Rejection under 35 U.S.C. § 102

Claims 1-10 were rejected under 35 U.S.C. § 102(e) as being anticipated by Date et al. (US 7,466,166). Claims 1-10 were rejected under 35 U.S.C. § 102(e) as being anticipated by Hashido et al. (US 7,221,349). These rejections are traversed for at least the following reasons.

Applicants respectfully remind the Examiner that the factual determination of lack of novelty under 35 U.S.C. § 102 requires the identical disclosure in a single reference of each element of a claimed invention, such that the identically claimed invention is placed into the possession of one having ordinary skill in the art. *Helifix Ltd. v. Blok-Lok, Ltd.*, 208 F.3d 1339, 54 USPQ2d 1299 (Fed. Cir. 2000); *Electro Medical Systems S.A. v. Cooper Life Sciences, Inc.*, 34 F.3d 1048, 32 USPQ2d 1017 (Fed. Cir. 1994). Moreover, in imposing the rejection under 35 U.S.C. § 102, the Examiner is required to specifically identify wherein an applied reference is perceived to identically disclose each feature of a claimed invention. *In re Rijckaert*, 9 F.3d

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1531, 28 USPQ2d 1955 (Fed. Cir. 1993); *Lindemann Maschinenfabrik GMBH v. American Hoist & Derrick Co.*, 730 F.2d 1452, 221 USPQ 481 (Fed. Cir. 1984). There are significant differences between the claimed current driving device and the devices disclosed by Date or Hashido that would preclude the factual determination that Date or Hashido identically describes the claimed current driving device within the meaning of 35 U.S.C. § 102.

With respect to Data, Applicants respectfully submit that, at a minimum, Date fails to disclose that *a voltage holding circuit has a terminal being connected to a reference voltage different from the first voltage*, and *under the voltage supply mode, the first voltage is supplied to another terminal of the voltage holding circuit*, as recited by amended claim 1. In rejecting claim 1, the Examiner asserts that FIG. 3A of Date discloses the claimed first voltage supply part (source). It appears that the Examiner considers Vcc connected to capacitor 003 as the claimed first voltage supply source and capacitor 003 as the claimed voltage holding part (circuit). However, it is clear that FIG. 3A fails to disclose that a voltage holding circuit (003) has a terminal being connected to a reference voltage different from the first voltage (Vcc). As such, it is clear that Date fails to disclose the aforementioned features of amended claim 1 within the meaning of 35 U.S.C. § 102. Thus, claim 1 and all claims dependent thereon are patentable over Date.

Regarding claim 10, Applicants respectfully submit that, at a minimum, Date fails to disclose that *the voltage holding circuit has a first terminal and a second terminal, the first terminal being connected to a fixed voltage, and the current driving device includes a high-speed switch for controlling connection/disconnection states of **said voltage supply source with respect to the second terminal of said voltage holding circuit***, as recited by amended claim 10. It is clear that the cited portions of Date do not disclose the aforementioned features of claim 10 within the meaning of 35 U.S.C. § 102. Thus, claim 10 is patentable over Date.

With respect to Hashido, Applicants respectfully submit that the Examiner erroneously combined FIG. 2 and FIG. 4 of Hashido. It is clear that FIG. 2 of Hashido is directed to a pixel 2 of FIG. 1 (see, col. 7, lines 15-16 of Hashido), while FIG. 4 is directed to data current generating circuit 30 of FIG. 1 (see, col. 7, lines 21-23). As such, the Examiner's assertion has no merit.

Further, Applicants submit that Hashido fails to disclose that *a voltage holding circuit has a terminal being connected to a reference voltage different from the first voltage, and under the voltage supply mode, the first voltage is supplied to another terminal of the voltage holding circuit*, as recited by amended claim 1. It appears that the Examiner considers that capacitor 4 of FIG. 2 of Hashido corresponds to the claimed voltage holding part (circuit). However, it is clear that FIG. 2 fails to disclose that a voltage holding circuit (4) has a terminal being connected to a reference voltage different from the first voltage (Vdd). As such, it is clear that Hashido fails to disclose the aforementioned features of amended claim 1 within the meaning of 35 U.S.C. § 102. Thus, claim 1 and all claims dependent thereon are patentable over Hashido.

Similar to Date, Applicants respectfully submit that, at a minimum, Hashido fails to disclose that *the voltage holding circuit has a first terminal and a second terminal, the first terminal being connected to a fixed voltage, and the current driving device includes a high-speed switch for controlling connection/disconnection states of said voltage supply source with respect to the second terminal of said voltage holding circuit*, as recited by amended claim 10. It is clear that the cited portions of Hashido do not disclose the aforementioned features of claim 10 within the meaning of 35 U.S.C. § 102. Thus, claim 10 is patentable over Hashido.

Based on the foregoing, Applicants submit that all pending claims are patentable over Date and Hashido. Thus, Applicants request that the Examiner withdraw the rejections of claims 1-10 under 35 U.S.C. § 102.

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CONCLUSION

Having fully responded to all matters raised in the Office Action, Applicants submit that all claims are in condition for allowance, an indication for which is respectfully solicited. If there are any outstanding issues that might be resolved by an interview or an Examiner's amendment, the Examiner is requested to call Applicants' attorney at the telephone number shown below.

To the extent necessary, a petition for an extension of time under 37 C.F.R. § 1.136 is hereby made. Please charge any shortage in fees due in connection with the filing of this paper, including extension of time fees, to Deposit Account 500417 and please credit any excess fees to such deposit account.

Respectfully submitted,

McDERMOTT WILL & EMERY LLP



Takashi Saito
Limited Recognition No. L0123

600 13th Street, N.W.
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Facsimile: 202.756.8087
Date: March 7, 2011

**Please recognize our Customer No. 53080
as our correspondence address.**

FIG. 6A Prior Art

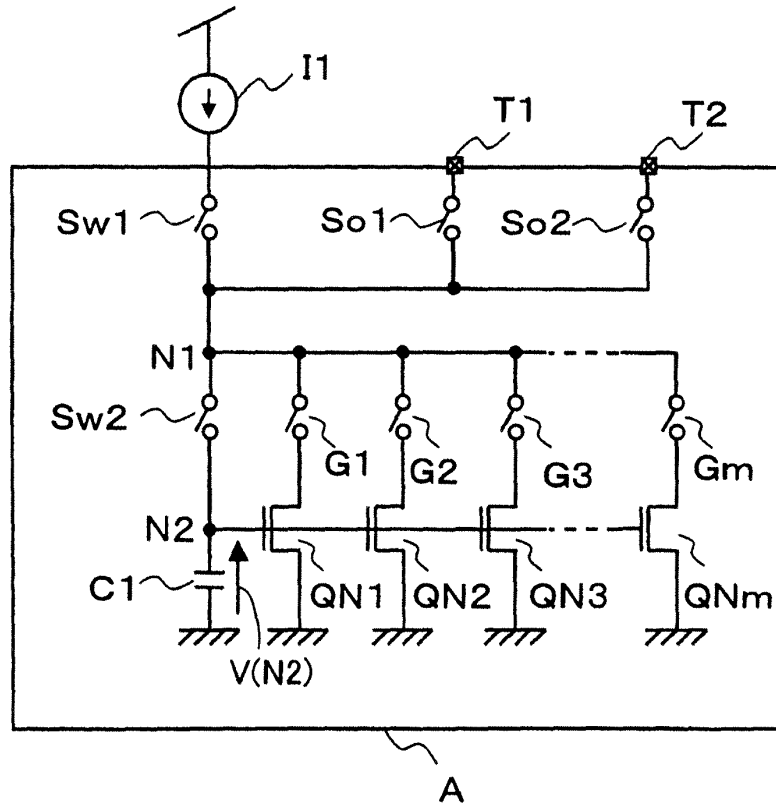


FIG. 6B Prior Art

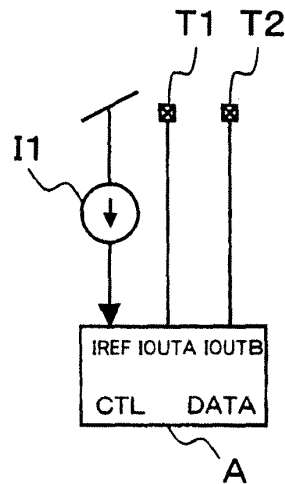


FIG. 7 Prior Art

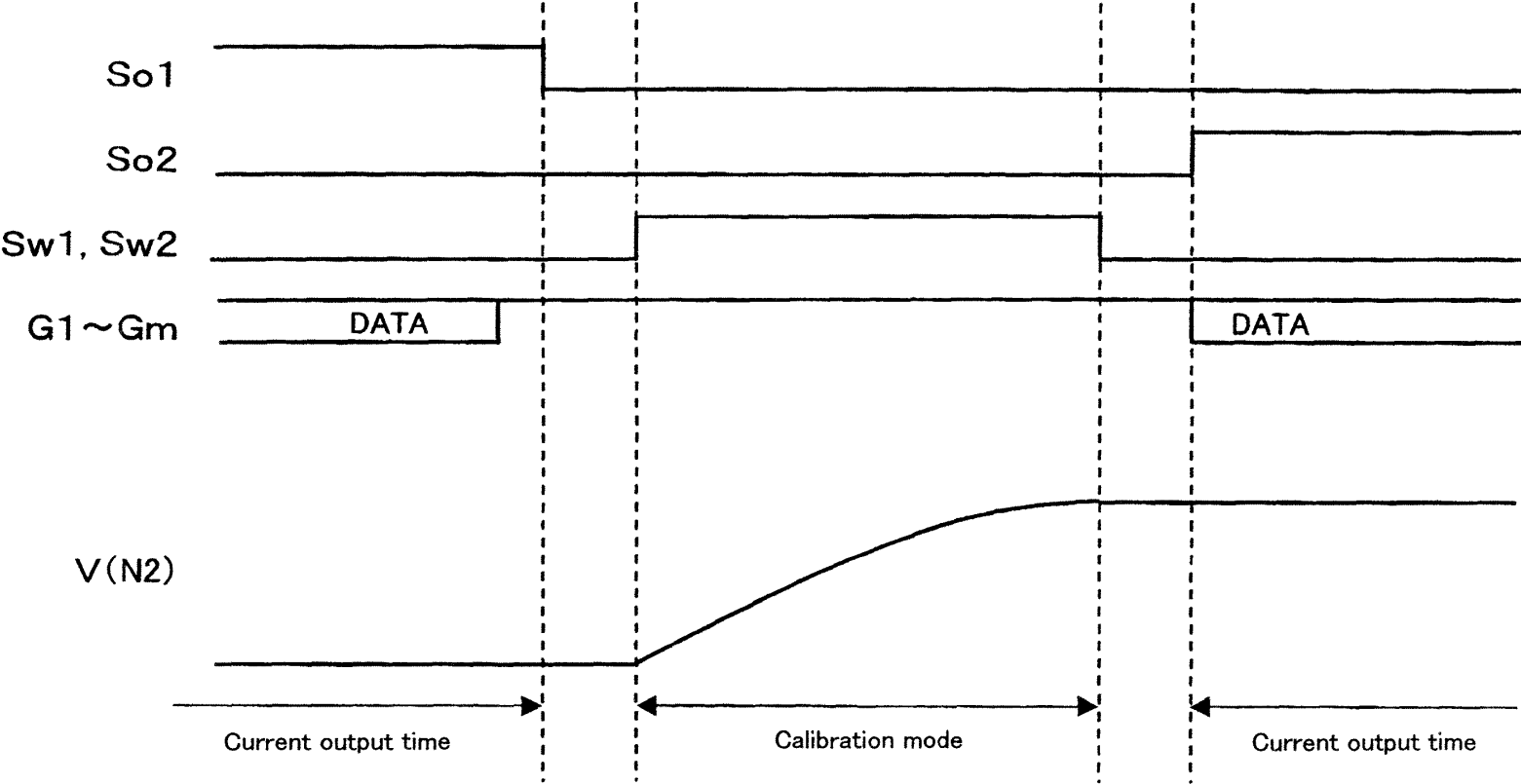
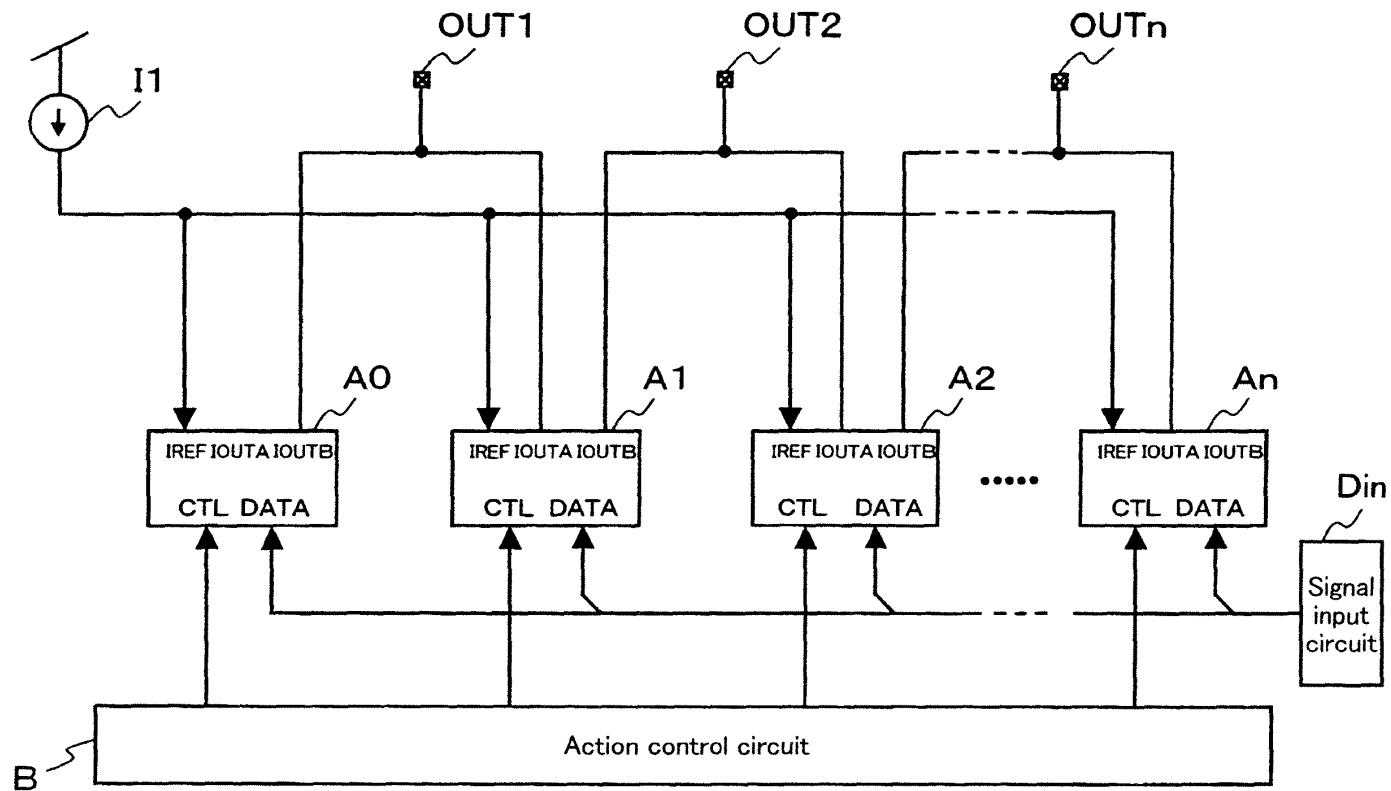
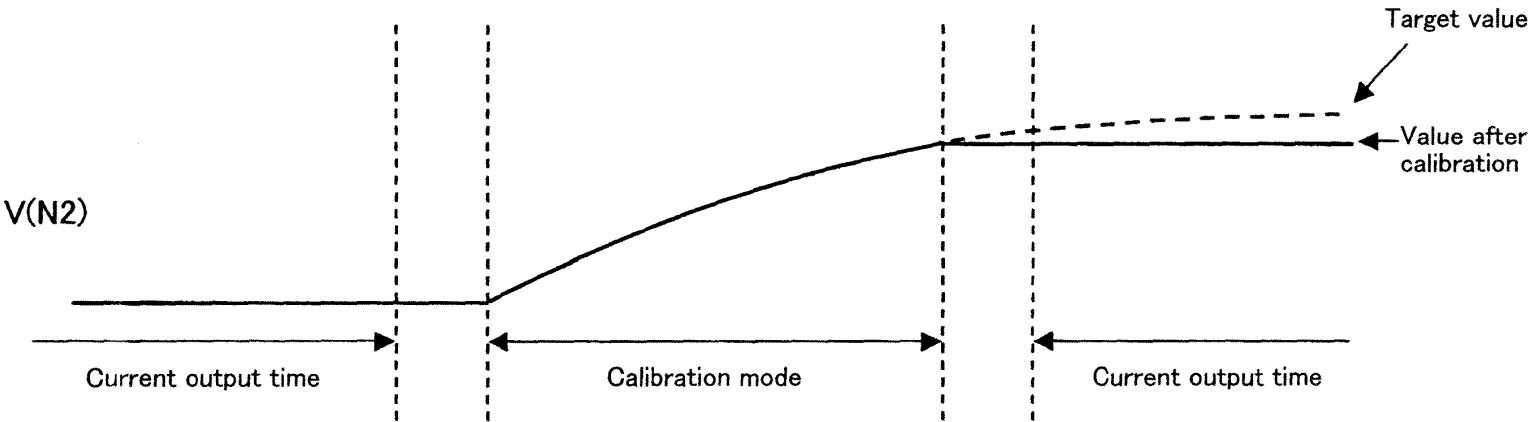


FIG. 8 Prior Art



Replacement Sheet: Application No. 11/954,659

FIG. 9 Prior Art



Electronic Acknowledgement Receipt	
EFS ID:	9605286
Application Number:	11954659
International Application Number:	
Confirmation Number:	4296
Title of Invention:	CURRENT DRIVING DEVICE
First Named Inventor/Applicant Name:	Makoto MIZUKI
Customer Number:	53080
Filer:	Michael E. Fogarty/3328/Matilda Mason
Filer Authorized By:	Michael E. Fogarty
Attorney Docket Number:	056937-0414
Receipt Date:	07-MAR-2011
Filing Date:	12-DEC-2007
Time Stamp:	19:53:36
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	no
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File Listing:

Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1		056937-0414Amendment.pdf	212372 598c0990a3cabf4c70a542618db065dfbb14ad43	yes	15

	Multipart Description/PDF files in .zip description		
	Document Description	Start	End
	Amendment/Req. Reconsideration-After Non-Final Reject	1	1
	Claims	2	6
	Specification	7	7
	Applicant Arguments/Remarks Made in an Amendment	8	11
	Drawings-only black and white line drawings	12	15
Warnings:			
Information:			
Total Files Size (in bytes):		212372	
<p>This Acknowledgement Receipt evidences receipt on the noted date by the USPTO of the indicated documents, characterized by the applicant, and including page counts, where applicable. It serves as evidence of receipt similar to a Post Card, as described in MPEP 503.</p> <p><u>New Applications Under 35 U.S.C. 111</u> If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application.</p> <p><u>National Stage of an International Application under 35 U.S.C. 371</u> If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.</p> <p><u>New International Application Filed with the USPTO as a Receiving Office</u> If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.</p>			

Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it displays a valid OMB control number.

PATENT APPLICATION FEE DETERMINATION RECORD Substitute for Form PTO-875					Application or Docket Number 11/954,659		Filing Date 12/12/2007		<input type="checkbox"/> To be Mailed		
APPLICATION AS FILED – PART I											
(Column 1)			(Column 2)			SMALL ENTITY <input type="checkbox"/> OR		OTHER THAN SMALL ENTITY			
FOR	NUMBER FILED	NUMBER EXTRA	RATE (\$)	FEE (\$)			RATE (\$)	FEE (\$)			
<input type="checkbox"/> BASIC FEE (37 CFR 1.16(a), (b), or (c))	N/A	N/A	N/A				N/A				
<input type="checkbox"/> SEARCH FEE (37 CFR 1.16(k), (i), or (m))	N/A	N/A	N/A				N/A				
<input type="checkbox"/> EXAMINATION FEE (37 CFR 1.16(o), (p), or (q))	N/A	N/A	N/A				N/A				
TOTAL CLAIMS (37 CFR 1.16(i))	minus 20 =	*	X \$ =		OR		X \$ =				
INDEPENDENT CLAIMS (37 CFR 1.16(h))	minus 3 =	*	X \$ =		OR		X \$ =				
<input type="checkbox"/> APPLICATION SIZE FEE (37 CFR 1.16(s))	If the specification and drawings exceed 100 sheets of paper, the application size fee due is \$250 (\$125 for small entity) for each additional 50 sheets or fraction thereof. See 35 U.S.C. 41(a)(1)(G) and 37 CFR 1.16(s).										
<input type="checkbox"/> MULTIPLE DEPENDENT CLAIM PRESENT (37 CFR 1.16(j))											
* If the difference in column 1 is less than zero, enter "0" in column 2.			TOTAL				TOTAL				
APPLICATION AS AMENDED – PART II											
(Column 1)			(Column 2)			(Column 3)		SMALL ENTITY OR		OTHER THAN SMALL ENTITY	
AMENDMENT	03/07/2011	CLAIMS REMAINING AFTER AMENDMENT		HIGHEST NUMBER PREVIOUSLY PAID FOR	PRESENT EXTRA	RATE (\$)	ADDITIONAL FEE (\$)		RATE (\$)	ADDITIONAL FEE (\$)	
	Total (37 CFR 1.16(i))	* 10	Minus	** 20	= 0	X \$ =		OR	X \$2=	0	
	Independent (37 CFR 1.16(h))	* 2	Minus	***3	= 0	X \$ =		OR	X \$220=	0	
	<input type="checkbox"/> Application Size Fee (37 CFR 1.16(s))										
	<input type="checkbox"/> FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))										
						TOTAL ADD'L FEE		OR	TOTAL ADD'L FEE	0	
AMENDMENT		CLAIMS REMAINING AFTER AMENDMENT		HIGHEST NUMBER PREVIOUSLY PAID FOR	PRESENT EXTRA	RATE (\$)	ADDITIONAL FEE (\$)		RATE (\$)	ADDITIONAL FEE (\$)	
	Total (37 CFR 1.16(i))	*	Minus	**	=	X \$ =		OR	X \$ =		
	Independent (37 CFR 1.16(h))	*	Minus	***	=	X \$ =		OR	X \$ =		
	<input type="checkbox"/> Application Size Fee (37 CFR 1.16(s))										
	<input type="checkbox"/> FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))										
						TOTAL ADD'L FEE		OR	TOTAL ADD'L FEE		
<p>* If the entry in column 1 is less than the entry in column 2, write "0" in column 3.</p> <p>** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 20, enter "20".</p> <p>*** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 3, enter "3".</p> <p>The "Highest Number Previously Paid For" (Total or Independent) is the highest number found in the appropriate box in column 1.</p>											

Legal Instrument Examiner:
/JOY DOBBS/

This collection of information is required by 37 CFR 1.16. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 12 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

If you need assistance in completing the form, call 1-800-PTO-9199 and select option 2.



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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
11/954,659	12/12/2007	Makoto MIZUKI	056937-0414	4296

53080 7590 12/08/2010
MCDERMOTT WILL & EMERY LLP
600 13TH STREET, NW
WASHINGTON, DC 20005-3096

EXAMINER

CHOWDHURY, AFROZA Y

ART UNIT	PAPER NUMBER
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2629

MAIL DATE	DELIVERY MODE
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12/08/2010

PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.		Applicant(s)	
	11/954,659		MIZUKI ET AL.	
	Examiner		Art Unit	
	AFROZA Y. CHOWDHURY		2629	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1) ☐ Responsive to communication(s) filed on ____.

2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.

3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4) ☒ Claim(s) 1-10 is/are pending in the application.

 4a) Of the above claim(s) ____ is/are withdrawn from consideration.

5) ☐ Claim(s) ____ is/are allowed.

6) ☒ Claim(s) 1-10 is/are rejected.

7) ☐ Claim(s) ____ is/are objected to.

8) ☐ Claim(s) ____ are subject to restriction and/or election requirement.

Application Papers

9) ☐ The specification is objected to by the Examiner.

10) ☐ The drawing(s) filed on ____ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.
 Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
 Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12) ☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

 a) ☒ All b) ☐ Some * c) ☐ None of:

 1. ☒ Certified copies of the priority documents have been received.

 2. ☐ Certified copies of the priority documents have been received in Application No. ____.

 3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

 * See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) <input checked="" type="checkbox"/> Notice of References Cited (PTO-892) 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948) 3) <input checked="" type="checkbox"/> Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date <u>12/12/2007</u> .	4) <input type="checkbox"/> Interview Summary (PTO-413) Paper No(s)/Mail Date. _____. 5) <input type="checkbox"/> Notice of Informal Patent Application 6) <input type="checkbox"/> Other: _____.
--	--

DETAILED ACTION

Drawings

1. **Figures 6A, 6B, and 7-9** should be designated by a legend such as --Prior Art-- because only that which is old is illustrated. See MPEP § 608.02(g). Corrected drawings in compliance with 37 CFR 1.121(d) are required in reply to the Office action to avoid abandonment of the application. The replacement sheet(s) should be labeled "Replacement Sheet" in the page header (as per 37 CFR 1.84(c)) so as not to obstruct any portion of the drawing figures. If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

Claim Rejections - 35 USC § 102

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

(e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

3. Claims 1-10 are rejected under 35 U.S.C. 102(e) as being anticipated by **Date et al.** (US Patent 7,466,166).

As to claim 1, Date et al. discloses a current driving device, comprising:

a first voltage supply part for supplying a first voltage (fig. 3A);
a first current supply part for supplying a first electric current (fig. 3A);
a plurality of output terminals (fig. 4); and
a plurality of current output parts for outputting an electric current in accordance with said first electric current, each of said current output parts comprising a current-voltage converting function, a voltage-current converting function, a voltage holding part, and at least one current output terminal (fig. 4), wherein
said current output part takes three operation modes, i.e. a voltage supply mode, a current supply mode, and a current output mode,
under said voltage supply mode, said current output part receives said first voltage from said first voltage supply part and holds said voltage in said voltage holding part (col. 11, lines 24-35, lines 49-67),
under said current supply mode, said current output part receives said first current from said first current supply part, and generates a second voltage by said current-voltage converting function and holds said voltage in said voltage holding part (col. 11, lines 24-35, lines 49-67), and
under said current output mode, said current output part outputs an output current according to said voltage held in said voltage holding part by said voltage-current converting function (col. 11, lines 24-35, col. 12, lines 2-17, col. 12, line 45 – col. 13, line 6).

As to claim 2, Date et al. teaches a current driving device wherein each of said output terminals is connected to said current output terminals provided to said plurality of said current output parts, and each of said plurality of current output parts is connected in parallel to said first current supply part and said first voltage supply part used in common (figs. 4, 6).

As to claim 3, Date et al. teaches current a driving device wherein each of said current output parts actuates said current-voltage converting function under said voltage supply mode (col. 3, lines 44-52).

As to claim 4, Date et al. teaches a current driving device according to claim 1, wherein each of said current output parts comprises a function of stopping said current-voltage converting function under said voltage supply mode (col. 11, lines 24-35, col. 12, lines 2-17, col. 12, line 45 – col. 13, line 6).

As to claim 5, Date et al. teaches a current driving device comprising a second current supply part for supplying a second electric current that is proportional to said first electric current, and a current-voltage converting part for generating said first voltage by receiving said second electric current, wherein said first voltage supply part controls supplies of said first voltage generated by said current-voltage converting part to said current output parts (col. 11, lines 24-35, col. 12, lines 2-17, col. 12, line 45 – col.

13, line 6).

As to claim 6, Date et al. teaches a current driving device wherein said current-voltage converting part comprises a switching part for short-circuiting a node at which said first voltage emerges to a reference voltage node (col. 11, lines 24-35, col. 12, lines 2-17, col. 12, line 45 – col. 13, line 6).

As to claim 7, Date et al. teaches a current driving device comprising a second voltage supply part with a larger voltage supply capacity than that of said first voltage supply part, wherein the use of said first voltage supply part and the use of said second voltage supply part are switched in accordance with the number of said current output parts that take said voltage supply mode among said plurality of current output parts (col. 11, lines 24-35, col. 12, lines 2-17, col. 12, line 45 – col. 13, line 6).

As to claim 8, Date et al. teaches a current driving device wherein said first voltage supply part is constituted to be capable of changing its voltage supply capacity in accordance with the number of said current output parts that take said voltage supply mode among said plurality of current output parts (col. 11, lines 24-35, col. 12, lines 2-17, col. 12, line 45 – col. 13, line 6).

As to claim 9, Date et al. teaches a current-driving-type display device, comprising said current driving device mounted thereon so as to be driven by said

current driving device (fig. 4).

As to claim 10, Date et al. teaches a current driving device, comprising:

a current input switch for controlling connection/disconnection states with respect to a current supply part (col. 11, lines 24-35, lines 49-67);

a voltage holding part for holding a reference voltage, which is charged by a flown current (col. 11, lines 24-35, lines 49-67);

a calibration switch interposed between said current input switch and said voltage holding part (col. 11, lines 24-35, col. 12, lines 2-17, col. 12, line 45 – col. 13, line 6);

a plurality of voltage-current converting elements for generating an electric current in accordance with said reference voltage held in said voltage holding part (fig. 4, col. 11, lines 24-35, col. 12, lines 2-17, col. 12, line 45 – col. 13, line 6);

a plurality of signal response switches that are on/off controlled in accordance with inputted signals, said response switches being connected in series to each of said voltage-current converting elements, and each of which being connected in parallel to said calibration switch (col. 11, lines 24-35, col. 12, lines 2-17, col. 12, line 45 – col. 13, line 6);

a plurality of current output switches, each being interposed between a connection node, which is provided between said current input switch and said calibration switch, and said plurality of current output terminals (col. 11, lines 24-35, col. 12, lines 2-17, col. 12, line 45 – col. 13, line 6); and

a high-speeding switch for controlling connection/disconnection states of said voltage supply part with respect to said voltage holding part (col. 11, lines 24-35, col. 12, lines 2-17, col. 12, line 45 – col. 13, line 6).

4. Claims 1-10 are rejected under 35 U.S.C. 102(e) as being anticipated by **Hashido et al.** (US Patent 7,221,349)

The applied reference has a common assignee with the instant application. Based upon the earlier effective U.S. filing date of the reference, it constitutes prior art under 35 U.S.C. 102(e). This rejection under 35 U.S.C. 102(e) might be overcome either by a showing under 37 CFR 1.132 that any invention disclosed but not claimed in the reference was derived from the inventor of this application and is thus not the invention “by another,” or by an appropriate showing under 37 CFR 1.131.

As to claim 1, Hashito et al. discloses a current driving device, comprising:
a first voltage supply part for supplying a first voltage (fig. 2(V_{dd}));
a first current supply part for supplying a first electric current (fig. 4(400), col. 12, lines 33-43);
a plurality of output terminals (fig. 2); and
a plurality of current output parts for outputting an electric current in accordance with said first electric current, each of said current output parts comprising a current-voltage converting function, a voltage-current converting function, a voltage holding part, and at least one current output terminal (figs. 2, 4), wherein

said current output part takes three operation modes, i.e. a voltage supply mode, a current supply mode, and a current output mode (figs. 2, 4),

under said voltage supply mode, said current output part receives said first voltage from said first voltage supply part and holds said voltage in said voltage holding part (col. 9, lines 24-56),

under said current supply mode, said current output part receives said first current from said first current supply part, and generates a second voltage by said current-voltage converting function and holds said voltage in said voltage holding part (col. 9, lines 24-56), and

under said current output mode, said current output part outputs an output current according to said voltage held in said voltage holding part by said voltage-current converting function (col. 9, lines 24-56).

As to claim 2, Hashito et al. teaches a current driving device wherein each of said output terminals is connected to said current output terminals provided to said plurality of said current output parts, and each of said plurality of current output parts is connected in parallel to said first current supply part and said first voltage supply part used in common (fig. 3).

As to claim 3, Hashito et al. teaches a current driving device wherein each of said current output parts actuates said current-voltage converting function under said voltage

supply mode (figs., 2-4).

As to claim 4, Hashito et al. teaches a current driving device wherein each of said current output parts comprises a function of stopping said current-voltage converting function under said voltage supply mode (figs., 2-4).

As to claim 5, Hashito et al. teaches a current driving device comprising a second current supply part for supplying a second electric current that is proportional to said first electric current, and a current-voltage converting part for generating said first voltage by receiving said second electric current, wherein said first voltage supply part controls supplies of said first voltage generated by said current-voltage converting part to said current output parts (figs., 2-4).

As to claim 6, Hashito et al. teaches a current driving device wherein said current-voltage converting part comprises a switching part for short-circuiting a node at which said first voltage emerges to a reference voltage node (figs., 2-4).

As to claim 7, Hashito et al. teaches a current driving device comprising a second voltage supply part with a larger voltage supply capacity than that of said first voltage supply part, wherein the use of said first voltage supply part and the use of said second voltage supply part are switched in accordance with the number of said current output parts that take said voltage supply mode among said plurality of current output parts

(figs.,. 2-4).

As to claim 8, Hashito et al. teaches a current driving device wherein said first voltage supply part is constituted to be capable of changing its voltage supply capacity in accordance with the number of said current output parts that take said voltage supply mode among said plurality of current output parts (figs.,. 2-4).

As to claim 9, Hashito et al. teaches a current-driving-type display device comprising said current driving device mounted thereon so as to be driven by said current driving device (figs.,. 2-4).

As to claim 10, Hashito et al. teaches a current driving device, comprising:
a current input switch for controlling connection/disconnection states with respect to a current supply part (col. 12, lines 34-64);
a voltage holding part for holding a reference voltage, which is charged by a flown current (col. 9, lines 17-41);
a calibration switch interposed between said current input switch and said voltage holding part (col. 12, lines 34-64);
a plurality of voltage-current converting elements for generating an electric current in accordance with said reference voltage held in said voltage holding part (fig. 4, col. 12, lines 34-64);

a plurality of signal response switches that are on/off controlled in accordance with inputted signals, said response switches being connected in series to each of said voltage-current converting elements, and each of which being connected in parallel to said calibration switch (col. 12, lines 34-64);

a plurality of current output switches, each being interposed between a connection node, which is provided between said current input switch and said calibration switch, and said plurality of current output terminals (col. 12, lines 34-64);
and

a high-speeding switch for controlling connection/disconnection states of said voltage supply part with respect to said voltage holding part (fig. 4, col. 13, lines 30-35).

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to AFROZA Y. CHOWDHURY whose telephone number is (571)270-1543. The examiner can normally be reached on 7:30-5:00 EST, 5/4/9.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Bipin Shalwala can be reached on 571-272-7681. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

AC
12/3/2010

/Bipin Shalwala/
Supervisory Patent Examiner, Art
Unit 2629

Notice of References Cited	Application/Control No. 11/954,659	Applicant(s)/Patent Under Reexamination MIZUKI ET AL.	
	Examiner AFROZA Y. CHOWDHURY	Art Unit 2629	Page 1 of 1

U.S. PATENT DOCUMENTS

*		Document Number Country Code-Number-Kind Code	Date MM-YYYY	Name	Classification
*	A	US-7,466,166	12-2008	Date et al.	327/108
*	B	US-7,221,349	05-2007	Hashido et al.	345/89
*	C	US-6,628,274	09-2003	Morita, Akira	345/209
*	D	US-7,064,969	06-2006	West, Richard T.	363/132
	E	US-			
	F	US-			
	G	US-			
	H	US-			
	I	US-			
	J	US-			
	K	US-			
	L	US-			
	M	US-			


FOREIGN PATENT DOCUMENTS

*		Document Number Country Code-Number-Kind Code	Date MM-YYYY	Country	Name	Classification
	N					
	O					
	P					
	Q					
	R					
	S					
	T					

NON-PATENT DOCUMENTS


*		Include as applicable: Author, Title Date, Publisher, Edition or Volume, Pertinent Pages)
	U	
	V	
	W	
	X	

*A copy of this reference is not being furnished with this Office action. (See MPEP § 707.05(a).)
Dates in MM-YYYY format are publication dates. Classifications may be US or foreign.

<p align="center"><i>Index of Claims</i></p> 	Application/Control No. 11954659	Applicant(s)/Patent Under Reexamination MIZUKI ET AL.
	Examiner AFROZA Y CHOWDHURY	Art Unit 2629

✓	Rejected	-	Cancelled	N	Non-Elected	A	Appeal
=	Allowed	÷	Restricted	I	Interference	O	Objected

<input type="checkbox"/> Claims renumbered in the same order as presented by applicant <input type="checkbox"/> CPA <input type="checkbox"/> T.D. <input type="checkbox"/> R.1.47										
CLAIM		DATE								
Final	Original	12/02/2010								
	1	✓								
	2	✓								
	3	✓								
	4	✓								
	5	✓								
	6	✓								
	7	✓								
	8	✓								
	9	✓								
	10	✓								

Search Notes 	Application/Control No. 11954659	Applicant(s)/Patent Under Reexamination MIZUKI ET AL.
	Examiner AFROZA Y CHOWDHURY	Art Unit 2629

SEARCHED			
Class	Subclass	Date	Examiner
345	76	12/2/2010	AC
327	108	12/2/2010	AC

SEARCH NOTES		
Search Notes	Date	Examiner
EAST	12/2/2010	AC

INTERFERENCE SEARCH			
Class	Subclass	Date	Examiner

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				APPLICANT Makoto MIZUKI, et al.			
				FILING DATE December 12, 2007		GROUP Not Yet Assigned	
U.S. PATENT DOCUMENTS							
EXAMINER'S INITIALS	CITE NO.	Document Number Number-Kind Code ² (if known)	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear		
/A.C./		US 2005/0231241 A1	10-20-2005	Date, et al.	Corresponds w/ JP 2005-311591		
/A.C./		US 2004/0251844 A1	12-16-2004	Hashido et al.			
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/A.C./		US 2006/0158402 A1	07-20-2006	Nathan et al.			
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EXAMINER'S INITIALS	CITE NO.	Foreign Patent Document Country Code ² -Number + Kind Codes (if known)	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines Where Relevant Figures Appear	Translation Yes No	
/A.C./		JP 2005-311591	11-04-2005	MATSUSHITA ELECTRIC IND CO LTD	Corresponds w/ US 2005/0231241 A1	English Abstract	
/A.C./		JP 2004-219955	08-05-2004	TOSHIBA MATSUSHITA DISPLAY TECHNOLOGY CO LTD		English Abstract	
/A.C./		JP 2005-121843	05-12-2005	TOSHIBA MATSUSHITA DISPLAY TECHNOLOGY CO LTD		English Abstract	
OTHER ART (Including Author, Title, Date, Pertinent Pages, Etc.)							
EXAMINER'S INITIALS	CITE NO.	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.					
EXAMINER /Afroza Chowdhury/				DATE CONSIDERED 11/30/2010			

*EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.

1 Applicant's unique citation designation number (optional). 2 Applicant is to place a check mark here if English language Translation is attached.

EAST Search History

EAST Search History (Prior Art)

Ref #	Hits	Search Query	DBs	Default Operator	Plurals	Time Stamp
L1	5	("20040251844" "20050231241" "20060158402" "6594606" "7050024").PN.	US-PGPUB; USPAT; USOCR	OR	ON	2010/12/03 09:59
L2	1	"7466166".pn.	US-PGPUB; USPAT; USOCR	OR	ON	2010/12/03 10:17
L3	1	(current near driv\$3) same (calibrat\$3 near7 (high\$2 fast\$2) near speed) same ((reference near current) near5 small near5 change)	US-PGPUB; USPAT; USOCR	OR	ON	2010/12/03 10:26
L4	1	(current near driv\$3) same (calibrat\$3 near7 (high\$2 fast\$2) near speed) same ((reference near current) near5 change)	US-PGPUB; USPAT; USOCR	OR	ON	2010/12/03 10:26
L5	1	(current near driv\$3) same (calibrat\$3 near3 speed) same ((reference near current) near5 change)	US-PGPUB; USPAT; USOCR	OR	ON	2010/12/03 10:28
L6	2	(current near driv\$3) same calibrat\$3 same ((reference near current) near5 change)	US-PGPUB; USPAT; USOCR	OR	ON	2010/12/03 10:29
L7	0	(current near driv\$3) same calibrat\$3 same ((reference near current) near5 change)	EPO; JPO; DERWENT	OR	ON	2010/12/03 10:29
L8	5	I1 and calibrat\$3	US-PGPUB; USPAT; USOCR	OR	ON	2010/12/03 10:30

L9	1	(current near driv\$3) same (calibrat\$3 near7 (high\$2 fast\$2) near speed) same (((reference program \$4) near current) near5 small near5 change)	US-PGPUB; USPAT; USOCR	OR	ON	2010/12/03 10:32
L10	1	(current near driv\$3) same (calibrat\$3 near7 (high\$2 fast\$2) near speed) same (((reference program \$4) near3 current) near5 small near5 change)	US-PGPUB; USPAT; USOCR	OR	ON	2010/12/03 10:32
L11	1	(current near driv\$3) and (calibrat\$3 near7 (high\$2 fast\$2) near speed) and (((reference program \$4) near3 current) near5 small near5 change)	US-PGPUB; USPAT; USOCR	OR	ON	2010/12/03 10:33
L12	1	(current near driv\$3) and (calibrat\$3 near7 (high\$2 fast\$2) near speed) and (((reference program \$4) near3 current) near5 small near5 change)	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT	OR	ON	2010/12/03 10:33
L13	1	(current near driv\$3) and (calibrat\$3 near7 (high\$2 fast\$2)) and (((reference program \$4) near3 current) near5 small near5 change)	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT	OR	ON	2010/12/03 10:33
L14	13	(current near driv\$3) and (calibrat\$3 near7 (high\$2 fast\$2)) and (((reference program \$4) near3 current) near5 change)	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT	OR	ON	2010/12/03 10:33
L15	1076	(current near driv\$3) and (high\$1speed\$3 near3 switch\$3)	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT	OR	ON	2010/12/03 10:58

L16	267	(current near driv\$3) and (high\$1speed\$3 near3 switch)	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT	OR	ON	2010/12/03 10:59
L17	23	(current near driv\$3) and (high\$1speed\$3 near3 switch) same voltage near3 supply	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT	OR	ON	2010/12/03 10:59
L18	8	display and (current near driv\$3) and (high\$1speed\$3 near3 switch) same voltage near3 supply	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT	OR	ON	2010/12/03 11:02
L19	8	(display panel) and (current near driv\$3) and (high\$1speed\$3 near3 switch) same voltage near3 supply	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT	OR	ON	2010/12/03 11:02
L20	1	I1 and (calibrat\$3 near7 (high\$2 fast\$2) near speed)	US-PGPUB; USPAT; USOCR	OR	ON	2010/12/03 11:44
L21	0	I1 and (high\$1speed\$3 near3 switch) same voltage near3 supply	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT	OR	ON	2010/12/03 11:44
L22	0	I1 and (high\$1speed\$3 near3 switch)	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT	OR	ON	2010/12/03 11:44
L23	1	I1 and (high\$1speed\$3)	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT	OR	ON	2010/12/03 11:45
L24	0	I1 and (high\$1speed\$3) same small near current	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT	OR	ON	2010/12/03 11:57
L25	0	I1 and (high\$1speed\$3) same small near3 current	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT	OR	ON	2010/12/03 11:57
L26	1	I1 and (high\$1speed\$3) and small near3 current	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT	OR	ON	2010/12/03 11:57

L27	161	(display panel) and (current near driv\$3) and (high\$1speed\$3) same voltage near3 supply	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT	OR	ON	2010/12/03 11:59
L28	894	(display panel) and (current near driv\$3) and (high\$1speed\$3) and small near3 current	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT	OR	ON	2010/12/03 12:00
L29	37	(display panel) and (current near driv\$3) and (high\$1speed\$3) and (small near3 change near3 current)	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT	OR	ON	2010/12/03 12:00
L30	3339	(display panel) and ((calibrat\$3 same current) ((switch\$3 control\$4) near5 (voltage near supply))) and (high\$1speed\$3)	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT	OR	ON	2010/12/03 12:09
L31	130	(display panel) and ((calibrat\$3 same current) ((switch\$3 control\$4) near5 (voltage near supply))) same (high\$1speed\$3)	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT	OR	ON	2010/12/03 12:09
L32	0	I1 and I31	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT	OR	ON	2010/12/03 12:10
L34	5	"345"/\$.ccls. and (display panel) and ((calibrat\$3 same current) ((switch\$3 control\$4) near5 (voltage near supply))) same (high\$1speed\$3)	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT	OR	ON	2010/12/03 12:10
L35	19	(display panel) and ((calibrat\$3 same current) ((switch\$3 control\$4) near5 (voltage near supply))) near7 (high\$1speed\$3)	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT	OR	ON	2010/12/03 12:12

L36	3	(display panel) and ((calibrat\$3 same current) ((switch\$3 control\$4) near5 (voltage near supply))) same (high\$1speed\$3)	EPO; JPO; DERWENT	OR	ON	2010/12/03 12:17
L37	127	(display panel) and ((calibrat\$3 same current) ((switch\$3 control\$4) near5 (voltage near supply))) same (high\$1speed\$3)	US-PGPUB; USPAT; USOCR	OR	ON	2010/12/03 12:17
L39	0	(OLED) and ((calibrat\$3 same current) ((switch\$3 control\$4) near5 (voltage near supply))) same (high\$1speed\$3)	US-PGPUB; USPAT; USOCR	OR	ON	2010/12/03 12:18
L40	67	(LED) and ((calibrat\$3 same current) ((switch\$3 control\$4) near5 (voltage near supply))) same (high\$1speed\$3)	US-PGPUB; USPAT; USOCR	OR	ON	2010/12/03 12:18
L41	13	(LED same (display panel)) and ((calibrat\$3 same current) ((switch\$3 control\$4) near5 (voltage near supply))) same (high\$1speed\$3)	US-PGPUB; USPAT; USOCR	OR	ON	2010/12/03 12:19

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MCDERMOTT WILL & EMERY LLP
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Title: CURRENT DRIVING DEVICE

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This is to certify that the annexed is a true copy of the following application as filed with this Office.

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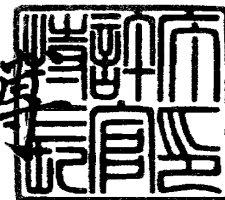
Applicant(s):

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2008年 5月15日

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肥塚雅博



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【書類名】 特許請求の範囲

【請求項 1】

第 1 の電圧を供給する第 1 の電圧供給手段と、
第 1 の電流を供給する第 1 の電流供給手段と、
複数の出力端子と、
電流 - 電圧変換機能、電圧 - 電流変換機能、電圧保持手段および 1 個以上の電流出力端子を有し、前記第 1 の電流に応じた電流を出力する複数の電流出力部とを備え、
前記電流出力部は、電圧供給モードと電流供給モードと電流出力モードの 3 つの動作モードをとり、
前記電圧供給モードでは、前記第 1 の電圧供給手段から前記第 1 の電圧を受けて前記電圧保持手段に保持し、
前記電流供給モードでは、前記第 1 の電流供給手段から前記第 1 の電流を受け、前記電流 - 電圧変換機能により第 2 の電圧を生成して前記電圧保持手段に保持し、
前記電流出力モードでは、前記電圧 - 電流変換機能により、前記電圧保持手段に保持されている電圧に応じた出力電流を出力するように構成されている電流駆動装置。

【請求項 2】

前記出力端子の各々は、複数の前記電流出力部に備わった前記電流出力端子と接続され、前記複数の電流出力部の各々が、共通の前記第 1 の電流供給手段および前記第 1 の電圧供給手段に対して並列に接続されている請求項 1 に記載の電流駆動装置。

【請求項 3】

前記電流出力部は、前記電圧供給モードにおいて、前記電流 - 電圧変換機能を作動させる請求項 1 または請求項 2 に記載の電流駆動装置。

【請求項 4】

前記電流出力部は、前記電圧供給モードにおいて、前記電流 - 電圧変換機能を停止する機能を備えている請求項 1 または請求項 2 に記載の電流駆動装置。

【請求項 5】

さらに、前記第 1 の電流と比例関係にある第 2 の電流を供給する第 2 の電流供給手段と、
前記第 2 の電流を受けて前記第 1 の電圧を生成する電流 - 電圧変換手段とを備え、
前記第 1 の電圧供給手段は、前記電流 - 電圧変換手段により生成された前記第 1 の電圧の前記電流出力部に対する供給を制御する請求項 1 から請求項 4 までのいずれかに記載の電流駆動装置。

【請求項 6】

前記電流 - 電圧変換手段は、前記第 1 の電圧が現れるノードを基準電圧ノードに短絡する切り替え手段を備えている請求項 5 に記載の電流駆動装置。

【請求項 7】

さらに、前記第 1 の電圧供給手段よりも電圧供給能力の大きい第 2 の電圧供給手段を備え、複数の前記電流出力部のうち前記電圧供給モードをとる前記電流出力部の数に応じて、前記第 1 の電圧供給手段と前記第 2 の電圧供給手段の使用を切り替えるように構成されている請求項 1 から請求項 6 までのいずれかに記載の電流駆動装置。

【請求項 8】

前記第 1 の電圧供給手段は、複数の前記電流出力部のうち前記電圧供給モードをとる前記電流出力部の数に応じて、その電圧供給能力が可変可能に構成されている請求項 1 から請求項 6 までのいずれかに記載の電流駆動装置。

【請求項 9】

請求項 1 から請求項 8 までのいずれかに記載の電流駆動装置を搭載し、この電流駆動装置によって駆動される電流駆動型の表示装置。

【請求項 10】

電流供給手段に対する接続・遮断を制御する電流入力用スイッチと、
流入電流によって充電され基準電圧を保持する電圧保持手段と、

前記電流入力用スイッチと前記電圧保持手段との間に介挿されたキャリブレーション用スイッチと、

前記電圧保持手段による基準電圧に応じた電流を生成する電圧 - 電流変換素子の複数と

、
前記電圧 - 電流変換素子のそれぞれに直列に接続され、前記キャリブレーション用スイッチに対してそれぞれ並列に接続され、入力されてくる信号に応じてオン・オフ制御される信号応答用スイッチの複数と、

前記電流入力用スイッチと前記キャリブレーション用スイッチとの接続ノードと複数の電流出力端子との間にそれぞれ介挿された電流出力用スイッチの複数と、

前記電圧保持手段に対して電圧供給手段の接続・遮断を制御する高速化スイッチとを備えた電流駆動装置。

【書類名】明細書

【発明の名称】電流駆動装置および表示装置

【技術分野】

【0001】

本発明は、電流駆動装置にかかわり、特には有機EL (Electro-Luminescence) パネルやLEDパネルなどの表示用ドライバとして好適な電流駆動装置に関する。また、表示装置に関する。

【背景技術】

【0002】

近年、フラットパネルディスプレイは大画面化、高精細化するとともに、薄型軽量化および低コスト化が進んできている。そのような背景の中で、表示用ドライバについては、出力端子間の出力電流のばらつきを低減することで、表示画質の均一性を高める性能が求められている。カレントミラーの静的動作の電流ばらつきは、個々のトランジスタの拡散プロセスによるばらつきや、電源配線の抵抗によるゲート電圧のばらつきなどがある。また、カレントミラーの動的動作におけるばらつきは、表示パネルからの電荷注入や瞬時的な電源の変動によるものがある。また、一般的にドライバ用半導体は、多出力構成であって平面パネルの額縁部に実装されるために棒状のスリム形状となっている。このLSI形状の制約により配置されるトランジスタの特性はスリムレイアウトの素子位置によって異なるため、カレントミラー構成では同一のゲート電圧が印加された場合であっても電流加算型DA変換回路の各々からの出力電流が等しくなるとはいえない。

【0003】

このようなばらつきの低減方法として、例えば図6に示すような電流出力部をもつ電流駆動装置がある（例えば特許文献1参照）。この電流出力部は、キャリブレーション機能と電流出力機能とを持つ。基準電流源による基準電流値を電流出力部に記憶させることを「キャリブレーション」という。

【0004】

キャリブレーションモード時は、電流出力用スイッチS_{o1}、S_{o2}を非導通状態とし、電流入力用スイッチS_{w1}、キャリブレーション用スイッチS_{w2}およびすべての信号応答用スイッチG₁～G_mを導通させる。電流出力端子T₁、T₂は外部と切り離される。ノードN₁とノードN₂が短絡され、N_{ch}トランジスタQ_{N1}～Q_{Nm}のドレインとゲートは短絡され、基準電流源I₁からの電流を受ける。これにより、N_{ch}トランジスタQ_{N1}～Q_{Nm}は、自身が基準電流源I₁からの電流を流すのに必要なゲート電圧をノードN₂に発生させる。電圧保持用容量素子C₁は、前記のゲート電圧に充電される。ノードN₂の電圧V(N₂)は、基準電流源I₁による基準電流と等しい電流をすべて導通状態にあるN_{ch}トランジスタQ_{N1}～Q_{Nm}に流させる能力の電圧に相当し、結局、電流出力部Aは基準電流源I₁による基準電流を記憶することになる。

【0005】

次に、電流出力モード時は、電流入力用スイッチS_{w1}、キャリブレーション用スイッチS_{w2}を非導通状態に切り替え、電流出力用スイッチS_{o1}、S_{o2}のいずれか一方を導通し他方は非導通とし、信号応答用スイッチG₁～G_mは外部から供給される入力信号に応じて導通、非導通が決定される。電圧保持用容量素子C₁はキャリブレーション動作により充電された値を保持し、N_{ch}トランジスタQ_{N1}～Q_{Nm}のゲート端子に供給し続ける。N_{ch}トランジスタQ_{N1}～Q_{Nm}は、信号応答用スイッチG₁～G_mの導通状態に応じて、ノードN₂の電圧V(N₂)に応じた電流を電流出力端子T₁、T₂のうちの導通状態にある方から出力する。

【0006】

次に、図6に示した電流加算型DA変換回路のキャリブレーション、電流出力の一連の動作のタイミングチャートを図7に示す。スイッチの導通状態を“H”で、非導通状態を“L”で表す。V(N₂)は、ノードN₂の電圧V(N₂)を表す。

【0007】

キャリブレーション前、電流出力部Aは、電流出力用スイッチS_{o1}を導通させ、ノードN₂の電圧V(N₂)と入力信号によって制御される信号応答用スイッチG₁～G_mの状態に応じた出力電流を電流出力端子T₁から出力している。電流出力用スイッチS_{o2}、電流入力用スイッチS_{w1}、キャリブレーション用スイッチS_{w2}は非導通とする。

【0008】

キャリブレーション期間中は、電流出力用スイッチS_{o1}、S_{o2}は非導通、電流入力用スイッチS_{w1}、キャリブレーション用スイッチS_{w2}を導通、NchトランジスタQ_{N1}～Q_{Nm}からの電流を選択する信号応答用スイッチG₁～G_mはすべて導通とする。これにより、NchトランジスタQ_{N1}～Q_{Nm}は、基準電流源I₁の電流のみが供給される状態となり、前述の動作に従ってノードN₂の電圧V(N₂)を決定する。

【0009】

以上のキャリブレーションを終えると、電流入力用スイッチS_{w1}、キャリブレーション用スイッチS_{w2}を非導通状態とし、電圧保持用容量素子C₁が電荷を保持する状態とする。つまり、ノードN₂の電圧V(N₂)を保持する状態とする。その後、電流出力用スイッチS_{o2}を導通状態とし、入力信号により信号応答用スイッチG₁～G_mで選択された電流の和を電流出力端子T₂から出力する。

【0010】

図6に示した電流出力部Aを利用した電流駆動装置の構成を図8に示す。(n+1)個の電流出力部A₀～A_nは、動作制御回路Bから制御信号により、キャリブレーションモード、電流出力モードの動作状態を制御する。信号入力回路D_{in}は、各電流出力部A₀～A_nの内部構成要素(図6参照)中の信号応答用スイッチG₁～G_mを制御する信号を与える。基準電流源I₁によるキャリブレーションは、各電流出力部A₀～A_nの内部動作により、(n+1)個の電流出力部A₀～A_nのうちの1個の電流出力部に対して行われる。キャリブレーションは、A₀からA₁、A₂、…A_nと順に行う。キャリブレーションを行っていない電流出力部は電流出力モードとなり、n個の出力端子OUT₁～OUT_nへ電流を出力する。電流出力は、A₀からA₁、A₂、…A_nと順に行う。

【0011】

上記の電流出力部による電流加算型DA変換回路を複数持った場合の基準電流を同一の電流源の電流に合わせ込むことができ、これにより、パネルの表示の均一化が実現できる。

【特許文献1】特開2005-311591号公報

【特許文献2】特開2004-219955号公報

【発明の開示】

【発明が解決しようとする課題】

【0012】

しかし、この方式では、基準電流源I₁の電流値が微小な場合に、電圧保持用容量素子C₁を充放電する能力が不足し、キャリブレーション期間内にNchトランジスタQ_{N1}～Q_{Nm}の電流が基準電流源I₁の電流の値に正確に合うように充電することが困難になる。この基準電流が微小なことによる電圧保持用容量素子C₁の充電不足の様子を図9に示す。

【0013】

また、基準電流源I₁の電流値が変化した場合に、逐次的なキャリブレーションでは、すべての電流出力部A₀～A_nの基準電流が更新されるまで、出力端子によって基準電流が異なる状態が発生する。

【0014】

本発明は、このような事情に鑑みて創作したものであり、基準電流が微小な場合や基準電流を変更した場合でも、キャリブレーションを高速に行い、出力電流の不均一性を改善する電流駆動装置を提供することを目的としている。

【課題を解決するための手段】

【0015】

本発明による電流駆動装置は、
第1の電圧を供給する第1の電圧供給手段と、
第1の電流を供給する第1の電流供給手段と、
複数の出力端子と、
電流 - 電圧変換機能、電圧 - 電流変換機能、電圧保持手段および1個以上の電流出力端子を有し、前記第1の電流に応じた電流を出力する複数の電流出力部とを備え、
前記電流出力部は、電圧供給モードと電流供給モードと電流出力モードの3つの動作モードをとり、
前記電圧供給モードでは、前記第1の電圧供給手段から前記第1の電圧を受けて前記電圧保持手段に保持し、
前記電流供給モードでは、前記第1の電流供給手段から前記第1の電流を受け、前記電流 - 電圧変換機能により第2の電圧を生成して前記電圧保持手段に保持し、
前記電流出力モードでは、前記電圧 - 電流変換機能により、前記電圧保持手段に保持されている電圧に応じた出力電流を出力するように構成されているものである。電圧供給モードと電流供給モードとがキャリブレーションモードに相当する。

【0016】

上記のように構成された電流駆動装置においては、電流出力部は、電圧供給モードにおいて第1の電圧供給手段より第1の電圧の供給を受け、この第1の電圧を電圧保持手段に保持する。次いで電流供給モードにおいて、電流出力部は第1の電流供給手段より第1の電流の供給を受け、電流 - 電圧変換機能により第2の電圧を生成し、この第2の電圧を電圧保持手段に保持する。これで、電圧保持手段への所定電圧への充電が高速化される。そして、電流出力モードにおいて、電流出力部は電圧 - 電流変換機能により、電圧保持手段に保持されている電圧に応じた電流を出力する。上記において、電圧保持手段に対する充電に際しては、第1の電圧によって目標電圧付近まで充電し、さらに第1の電流を供給して充電を行うので、第1の電流供給手段による基準電流が微小であっても、基準電流を得るまでの電圧保持手段への電圧供給動作が高速化され、また基準電流を正確に得ることが可能となる。

【0017】

上記構成の電流駆動装置において、前記出力端子の各々は、複数の前記電流出力部に備わった前記電流出力端子と接続され、前記複数の電流出力部の各々が、共通の前記第1の電流供給手段および前記第1の電圧供給手段に対して並列に接続されているという態様がある。このように構成すれば、起動直後や第1の電流が変化した場合など、すべての電流出力部に大幅なキャリブレーションが必要となった場合に、すべての電流出力部に備わった電圧保持手段を第1の電圧に仮充電することができ、第1の電流の変更による表示むらを抑えることが可能となる。

【0018】

また上記構成の電流駆動装置において、前記電流出力部は、前記電圧供給モードにおいて、前記電流 - 電圧変換機能を作動させるという態様がある。このように構成すれば、電圧保持手段に対する充電を、第1の電圧供給手段からの第1の電圧の供給による充電に加えて、第1の電流供給手段からの第1の電流を電圧に変換した上での充電との相乗が行われるので、さらなる高速化が実現可能となる。

【0019】

また上記構成の電流駆動装置において、前記電流出力部は、前記電圧供給モードにおいて、前記電流 - 電圧変換機能を停止する機能を備えているという態様がある。このように構成すれば、第1の電圧供給手段より供給される電流をすべて電圧保持手段の充電に利用でき、消費電力の低減が図られる。

【0020】

また上記構成の電流駆動装置において、さらに、前記第1の電流と比例関係にある第2の電流を供給する第2の電流供給手段と、前記第2の電流を受けて前記第1の電圧を生成する電流 - 電圧変換手段とを備え、前記第1の電圧供給手段は、前記電流 - 電圧変換手段

により生成された前記第1の電圧の前記電流出力部に対する供給を制御するという態様がある。このように構成すれば、第1の電圧供給手段が電流出力部に供給する第1の電圧が電流-電圧変換手段によって第2の電流から生成され、その第2の電流供給手段による第2の電流が第1の電流と比例関係にあるので、結局、第1の電圧が第1の電流に比例したものになる。したがって、第1の電圧について、電圧保持手段に保持させるべき電圧の最終目標値にほぼ一致する値の電圧を生成することが可能となる。

【0021】

また上記構成の電流駆動装置において、前記電流-電圧変換手段は、前記第1の電圧が現れるノードを基準電圧ノードに短絡する切り替え手段を備えているという態様がある。第1の電流や第2の電流を変更した場合には、電流-電圧変換手段により生成される第2の電圧の変更にも時間がかかる。これに対して、本構成によれば、切り替え手段を動作させることにより電流-電圧変換手段の出力電圧をリセットすることが可能であるので、電流-電圧変換手段による第2の電圧の変更が高速化される。

【0022】

また上記構成の電流駆動装置において、さらに、前記第1の電圧供給手段よりも電圧供給能力の大きい第2の電圧供給手段を備え、複数の前記電流出力部のうち前記電圧供給モードをとる前記電流出力部の数に応じて、前記第1の電圧供給手段と前記第2の電圧供給手段の使用を切り替えるように構成されているという態様がある。多数の電流出力部を持つ場合、電圧供給モードになる電流出力部の数により、電圧供給手段の負荷が大幅に変わる。本構成によれば、第2の電圧供給手段を追加し、負荷に応じて、第1の電圧供給手段と第2の電圧供給手段の使用を切り替えることで、出力電圧を滑らかに変化させることによるEMI（電磁妨害）の低減と消費電力の低減が実現される。

【0023】

あるいは上記構成の電流駆動装置において、前記第1の電圧供給手段は、複数の前記電流出力部のうち前記電圧供給モードをとる前記電流出力部の数に応じて、その電圧供給能力が可変可能に構成されているという態様がある。このように構成すれば、第1の電圧供給手段が負荷に応じて電圧供給能力を最適にする機能を備えることで、EMI（電磁妨害）の低減と必要面積の低減が実現される。

【0024】

上記の電流駆動装置に関連する本発明による表示装置は、上記のいずれかの電流駆動装置を搭載し、この電流駆動装置によって駆動される電流駆動型の表示装置である。この表示装置においては、画面表示の均一化が実現される。

【0025】

本発明による電流駆動装置は、
電流供給手段に対する接続・遮断を制御する電流入力用スイッチと、
流入電流によって充電され基準電圧を保持する電圧保持手段と、
前記電流入力用スイッチと前記電圧保持手段との間に介挿されたキャリブレーション用スイッチと、
前記電圧保持手段による基準電圧に応じた電流を生成する電圧-電流変換素子の複数と、

前記電圧-電流変換素子のそれぞれに直列に接続され、前記キャリブレーション用スイッチに対してそれぞれ並列に接続され、入力されてくる信号に応じてオン・オフ制御される信号応答用スイッチの複数と、

前記電流入力用スイッチと前記キャリブレーション用スイッチとの接続ノードと複数の電流出力端子との間にそれぞれ介挿された電流出力用スイッチの複数と、

前記電圧保持手段に対して電圧供給手段の接続・遮断を制御する高速化スイッチとを備えたものである。

【0026】

キャリブレーションモードは2つの段階からなる。電圧供給モードと電流供給モードとである。電圧供給モードでは、高速化スイッチを導通状態にして電圧供給手段を電圧保持

手段に接続し、電圧保持手段の電位レベルを高速に昇圧する。このとき、電流出力用スイッチはすべて非導通状態、キャリブレーション用スイッチおよびすべての信号応答用スイッチは導通状態とする。次いで、電流供給モードでは、高速化スイッチを非導通状態に切り替える。電流入力用スイッチおよびキャリブレーション用スイッチは導通状態とし、電圧 - 電流変換素子に流れる電流の合計値が電流供給手段から供給される基準電流値と等しくなり、その基準電流値に等しい電流を電圧 - 電流変換素子に流すことに対応した電圧を電圧保持手段に保持させることになる。すなわち、基準電流値を記憶することになる。このように、キャリブレーションモードでの前半段階である電圧供給モードでは電圧供給手段を用いて電圧保持手段の電位を高速に立ち上げ、キャリブレーションモードの後半段階では電流供給手段による基準電流値を正確に記憶するので、基準電流源の電流値が微小な場合であっても、基準電流を得るまでの電圧保持手段へ電圧供給する能力を電圧供給手段でまかない、電圧 - 電流変換素子に流れる電流が基準電流源の電流の値に正確に合うキャリブレーションの完成を高速に行うことが可能となる。

【発明の効果】

【0027】

本発明によれば、第1の電流供給手段による基準電流が微小であっても、第1の電圧によって電圧保持手段を目標電圧付近まで充電し、さらに第1の電流を供給して充電を行うので、基準電流を得るまでの電圧保持手段への電圧供給動作が高速化され、また基準電流を正確に得ることができる。

【0028】

また、出力電流の基準となる電流が変更された場合に、各電流出力部による出力電流の不均一性を改善することができる。

【発明を実施するための最良の形態】

【0029】

以下、本発明にかかわる電流駆動装置の実施の形態を図面を用いて詳細に説明する。なお、図中同一または相当部分には同一の符号を付してある。

【0030】

図1は本発明の実施の形態における電流駆動装置に搭載される電流出力部Aの構成を示す回路図、図2は電流出力部Aの動作を説明するタイミングチャート、図3は電流駆動装置の全体的な構成を示すブロック回路図、図4は電圧供給源V1の具体例を示す回路図である。以下、順次に説明する。

【0031】

<電流出力部>

まず、図1を用いて電流出力部Aを説明する。電圧保持用容量素子C1の一端が接地端子に接続され、他端がm個のNchトランジスタQN1～QNmのゲート端子に共通に接続されている。NchトランジスタQN1～QNmのソースはそれぞれ接地端子に接続され、ドレインはそれぞれ入力信号に応じてオン・オフ制御される信号応答用スイッチG1～Gmに直列に接続され、信号応答用スイッチG1～Gmの他端は共通に接続され、かつ電流入力用スイッチSw1を介して、一定の電流値（第1の電流）を電流出力部Aに供給する基準電流源I1に接続されているとともに、キャリブレーション用スイッチSw2を介して電圧保持用容量素子C1に接続されている。電流入力用スイッチSw1とキャリブレーション用スイッチSw2および信号応答用スイッチG1～Gmとの接続のノードN1が電流出力用スイッチSo1、So2を介してそれぞれ電流出力端子T1、T2に接続されている。ここまでの回路構成については、従来の技術の場合の図6の回路構成と同じである。本実施の形態においては、さらに、電圧保持用容量素子C1とキャリブレーション用スイッチSw2との接続のノードN2に対して、高速化スイッチSw3を介して、一定の電圧（第1の電圧）を電流出力部Aに供給する電圧供給源V1が接続されている。これが前述の第1の電圧供給手段に相当する。基準電流源I1が前述の第1の電流供給手段に相当する。電圧保持用容量素子C1が前述の電圧保持手段に相当する。なお、電圧保持用容量素子C1については、NchトランジスタQN1～QNmのゲート端子に本来備わっている

寄生容量で代用してもかまわない。

【0032】

この電流出力部Aは、電圧供給モードM1、電流供給モードM2および電流出力モードM3の3つの動作状態をとる。このうち電圧供給モードM1と電流供給モードM2とがキャリアブレーションモードMcを構成する。

【0033】

《電圧供給モードM1》

ここで、電流出力部Aの電圧供給モードM1について説明する。

【0034】

まず、電流出力用スイッチSo1、So2はそれぞれ非導通状態とし、電流出力端子T1、T2はノードN1から切り離される。そして、高速化スイッチSw3が導通状態とされ、電圧供給源V1とノードN2とが接続されている。このとき、電圧保持用容量素子C1は、電圧供給源V1より供給される一定の電圧（第1の電圧に相当。以下、基準電圧と記す。）に充電される。

【0035】

なお、この電圧供給モードM1のときに、次に説明する電流供給モードM2を同時に動作させることもあり得る。その場合、電流入力用スイッチSw1、キャリアブレーション用スイッチSw2およびすべての信号応答用スイッチG1～Gmが導通状態とされる。

【0036】

《電流供給モードM2》

次に、電流出力部Aの電流供給モードM2について説明する。この電流供給モードM2では、電流-電圧変換機能が作動する。そのため、電流入力用スイッチSw1、キャリアブレーション用スイッチSw2および信号応答用スイッチG1～Gmのすべてが導通状態とされる。高速化スイッチSw3は非導通状態に切り替えられ、ノードN2が電圧供給源V1から切り離される。電流出力用スイッチSo1、So2は非導通状態のままである。

【0037】

このとき、NchトランジスタQN1～QNmは、ドレインとゲートが接続されているので、ダイオード特性を示す。よって、NchトランジスタQN1～QNmは、負荷として基準電流源I1からの一定の電流値を有する電流（基準電流）を流すことになる。このとき、NchトランジスタQN1～QNmのゲートには、基準電流源I1からの基準電流を流すためのゲート電圧が一義的に発生する。したがって、電圧保持用容量素子C1は、このゲート電圧に応じた電荷を蓄積する。このように、電圧保持用容量素子C1は、基準電流と等しい電流値を有する電流を流すためのゲート電圧を保持する。電流出力部Aとしては基準電流値を記憶することになる。

【0038】

《電流出力モードM3》

次に、電流出力部Aの電流出力モードM3について説明する。この電流出力モードM3では、電圧-電流変換機能が作動する。そのため、電流入力用スイッチSw1およびキャリアブレーション用スイッチSw2が非導通状態とされ、電流出力用スイッチSo1、So2のいずれか一方が非導通状態から導通状態に切り替えられる。電流出力用スイッチSo1、So2は、同時には導通しない。高速化スイッチSw3は、非導通状態のままである。電圧保持用容量素子C1には、上述の電流供給モードM2の際に基準電流と等しい電流値を有する電流を流すためのゲート電圧に応じた電荷が蓄積されている。よって、NchトランジスタQN1～QNmのゲートには、電圧保持用容量素子C1に蓄積された電荷に応じたゲート電圧が印加されるので、電流出力端子T1またはT2に電源を接続すれば、電流出力用スイッチSo1、So2および信号応答用スイッチG1～Gmの導通設定に応じて、基準電流に比例する電流値を有する引き込み電流を出力することができる。出力電流は、信号応答用スイッチG1～Gmの導通設定にも依存し、NchトランジスタQN1～QNmの出力電流のうち、上記各トランジスタに接続された信号応答用スイッチG1～Gmが導通しているNchトランジスタが出力している電流の加算となる。なお、信号応答用ス

スイッチG1～Gmがすべて導通状態であれば、上述の電流供給を行った電流出力部Aの最大出力電流であり、その値は基準電流に等しくなる。

【0039】

この一連の動作により、基準電流を電流出力部Aにコピーして、この基準電流と入力信号に応じた電流を出力することができる。電流のコピーは、電流供給モードM2と電流出力モードM3のみでも可能であるが、電圧供給モードM1にて、NchトランジスタQN1～QNmのゲート端子の接続されたノードN1の電圧を、目標電圧（電流供給モードM2での収束電圧）付近まで充電することで、電圧保持用容量素子C1の充電不足を解消し、電流を高速にコピーできる。

【0040】

本実施の形態においては、NchトランジスタQN1～QNmの電流能力を、1倍、2倍、4倍…、 2^m 倍とすることで、mビットの電流加算型DA変換回路を構成することができる。なお、各ビット毎に基準電流源I1を用意するのでもよい。また、本実施の形態に示した電流加算型DA変換回路は一例に過ぎず、等しい電流のみをコピーする場合などは、信号応答用スイッチG1～Gmを除けばよい。

【0041】

ここで、図1(a)に示した電流出力部Aを図1(b)に示すように5端子回路素子として表すことにする。図1(b)において、電流出力部Aは、基準電流入力端子IREFと電圧入力端子VREFと電流出力端子IOUTと制御信号入力端子CTLと信号入力端子DATAを備える。基準電流入力端子IREFは基準電流源I1に接続され、電圧供給モードM1、電流供給モードM2において基準電流源I1からの電流を入力する。電圧入力端子VREFは電圧供給源V1に接続され、電圧供給モードM1において基準電圧を入力する。電流出力端子IOUTは電流出力モードM3になると、電流供給モードM2にて記憶された電流を出力する。制御信号入力端子CTLは動作状態を制御する制御信号を入力し、電流出力部A内の電流出力用スイッチS01、S02、電流入力用スイッチSw1、キャリブレーション用スイッチSw2、高速化スイッチSw3および信号応答用スイッチG1～Gmの切り替えを制御する。信号入力端子DATAは出力電流値を制御するmビットの入力信号を入力し、信号応答用スイッチG1～Gmの切り替えを制御する。

【0042】

次に、上記のように構成された本実施の形態の電流出力部Aの動作を図2のタイミングチャートを用いて説明する。図2は上記3つの動作状態（電圧供給モードM1、電流供給モードM2および電流出力モードM3）を示す。スイッチの導通状態を“H”で、非導通状態を“L”で表す。また、V(N2)はノードN2の電圧V(N2)を表す。ノードN2の電圧V(N2)は本実施の形態によるものを実線で、従来技術において電流供給モードM2のみのキャリブレーションを同時に開始した場合の電圧の様子を破線で示している。

【0043】

キャリブレーション前、電流出力部Aは、電流出力用スイッチS01を導通させ、ノードN2の電圧V(N2)と入力信号によって制御される信号応答用スイッチG1～Gmの状態に応じた出力電流を、電流出力端子T1から出力している。電流出力用スイッチS02、電流入力用スイッチSw1、キャリブレーション用スイッチSw2、高速化スイッチSw3は非導通とする。

【0044】

キャリブレーション期間全般において、電流出力用スイッチS01、S02は非導通とし、NchトランジスタQN1～QNmからの電流を選択する信号応答用スイッチG1～Gmは、すべて導通状態とする。詳しくは次のとおりである。電圧供給モードM1では、電流入力用スイッチSw1、キャリブレーション用スイッチSw2および高速化スイッチSw3を導通状態とすることで、基準電流および基準電圧を供給し、ノードN2から電圧保持用容量素子C1を充電する。電流供給モードM2では、電圧供給モードM1のスイッチの状態から、高速化スイッチSw3を非導通とする。これにより、NchトランジスタQN

1～QN_mには基準電流源I₁の電流のみが供給される状態となり、前述の動作に従って、ノードN₂の電圧V(N₂)を決定する。このノードN₂の電圧V(N₂)は、N_{ch}トランジスタQN₁～QN_mのすべてが導通状態にあるという条件下で基準電流源I₁による基準電流と等しい電流をN_{ch}トランジスタQN₁～QN_mに流させる能力の電圧に相当し、結局、電流出力部Aは基準電流源I₁による基準電流を記憶することになる。

【0045】

以上のキャリブレーションを終えると、まず電流入力用スイッチSw₁、キャリブレーション用スイッチSw₂を非導通状態とし、電圧保持用容量素子C₁が電荷を保持する状態とする。つまり、ノードN₂の電圧V(N₂)を保持する状態とする。その後、電流出力用スイッチSo₂を導通状態とし、入力信号により信号応答用スイッチG₁～G_mで選択された電流の和を電流出力端子T₂から出力する。

【0046】

なお、上記説明では、電圧供給モードM₁において、電流入力用スイッチSw₁、キャリブレーション用スイッチSw₂を導通して高速化を図っているが、電流入力用スイッチSw₁、キャリブレーション用スイッチSw₂を非導通状態としても従来技術と比べると高速に収束し、かつ上記説明の場合に比べて基準電流源の分の電流を削減することができる。

【0047】

次に、本実施の形態における電流駆動装置の全体構成について図3を用いて説明する。この電流駆動装置は、n個の出力端子OUT₁～OUT_nと、(n+1)個の電流出力部A₀～A_nと、第1の電流供給手段を構成する基準電流供給用トランジスタQP₁と、第2の電流供給手段を構成する基準電流供給用トランジスタQP₂と、電圧供給源V₁と、動作制御回路Bと、信号入力回路D_{in}と、電流-電圧変換用トランジスタQN_x、QP_xと、基準電流源I₁と、リセット用スイッチSw₄とを備える。電流出力部A₀～A_nの各々は図1に示した電流出力部であり、基準電流入力端子I_{REF}は基準電流供給用トランジスタQP₁に接続され、電圧入力端子V_{REF}は電圧供給源V₁に接続され、動作制御端子CTLは動作状態を制御する信号を動作制御回路Bから入力し、信号入力端子DATAは出力電流値を制御する信号を信号入力回路D_{in}から入力し、電流出力端子IOUTA、IOUTBはそれぞれ出力端子OUT₁～OUT_nのうちの1つに接続され、基準電流と入力信号DATAとに応じた出力電流を制御信号CTLの状態に応じて外部へ出力する。基準電流供給用トランジスタQP₁は、電流出力部A₀～A_nのI_{REF}端子と電源端子の間に接続され、ゲート端子はノードN₁₁に接続されている。基準電流供給用トランジスタQP₂は、ノードN₁₂と電源端子との間に接続され、ゲート端子はノードN₁₁に接続されている。Pチャンネル型の電流-電圧変換用トランジスタQP_xは、基準電流源I₁と電源端子との間に接続され、ゲートは自身のドレインと短絡されている。Nチャンネル型の電流-電圧変換用トランジスタQN_xは、基準電流供給用トランジスタQP₂と接地端子との間に接続され、ゲートは自身のドレインと短絡されている。リセット用スイッチSw₄は、ノードN₁₂と接地端子との間に接続されている。

【0048】

ここで、電流出力部A₀～A_nの電流出力端子IOUTA、IOUTBの接続は、以下の規則に従って割り当てる。電流出力部A₀の電流出力端子IOUTAは外部へ接続せず、電流出力端子IOUTBは電流駆動装置の出力端子OUT₁へ接続する。電流出力端子IOUTAは出力端子OUT₁へ接続し、電流出力端子IOUTBは出力端子OUT₂へ接続する。以降の電流出力部も同様にしていき、電流出力部A_nの電流出力端子IOUTAは出力端子OUT_nに接続し、電流出力端子IOUTBは外部へ接続しない。つまり、n個の出力端子OUT₁～OUT_nに対し、(n+1)個の電流出力部A₀～A_nのうち、i番目の電流出力部A_iにおいて、電流出力端子IOUTAはi番目の出力端子OUT_iに接続し、電流出力端子IOUTBは(i+1)番目の出力端子OUT_(i+1)に接続する。ただし、1番目の電流出力部A₀の電流出力端子IOUTAと、(n+1)番目の電流出力部A_nの電流出力端子IOUTBは、外部へ接続しない。

【0049】

1 番目の電流出力部A 0については電流出力用スイッチS o 1 および電流出力端子T 1 を備えなくてもよく、(n + 1) 番目の電流出力部A nの電流出力用スイッチS o 2と電流出力端子T 2についても同様である。

【0050】

ここでは、出力端子数nより1個多い電流出力部を用意しているが、例えば、出力端子1個に対して2個の電流出力部を用意しても、一方が電流出力、他方がキャリブレーションとすることができ、常に電流出力端子に出力電流を供給できる。また、必ずしもすべての出力端子が電流出力状態になくてもよい場合は、出力端子よりも電流出力部の方が少なくしてもよい。

【0051】

電流 - 電圧変換用トランジスタQ P xは電流 - 電圧変換手段として働く。基準電流源I 1の電流を受け、電流 - 電圧変換用トランジスタQ P xが基準電流源I 1に等しい電流を流すゲート電圧(第1の電圧)をノードN 1 1に発生させる。ゲート端子がノードN 1 1に接続された基準電流供給用トランジスタQ P 1, Q P 2は、基準電流源I 1による基準電流に比例した電流を、それぞれ電流出力部A 0 ~ A nのI R E F端子と電流 - 電圧変換用トランジスタQ N xへ供給する。

【0052】

電流 - 電圧変換用トランジスタQ N xは、基準電流供給用トランジスタQ P 2より基準電流源I 1の電流値に比例した電流を受ける。電流 - 電圧変換用トランジスタQ P xと同様、自身が、基準電流供給用トランジスタQ P 2より供給される電流を流すためのゲート電圧をノードN 1 2に発生させる。

【0053】

好ましくは、電流 - 電圧変換用トランジスタQ N xは、図1に示したNchトランジスタQ N 1 ~ Q N mのトランジスタのすべてを並列接続した構成にする。また、基準電流供給用トランジスタQ P 1, Q P 2より供給される電流を異なる値とする場合は、電流 - 電圧変換用トランジスタQ N xの電流 - 電圧変換能力を、基準電流供給用トランジスタQ P 1, Q P 2が供給する電流値の比率に合わせるとよい。つまり、基準電流供給用トランジスタQ P 2より供給される電流値を、基準電流供給用トランジスタQ P 1より供給される電流値の3倍とした場合、電流 - 電圧変換用トランジスタQ N xは、電流出力部A内のNchトランジスタQ N 1 ~ Q N mのすべてを並列接続したものを3つ分用意する。これにより、ノードN 1 2に、電流出力部Aが電流供給モードM2でNchトランジスタQ N 1 ~ Q N mのゲートに発生する電圧に極めて近い値の電圧を生成することができる。

【0054】

電圧供給源V 1は、上記のようにして電流 - 電圧変換用トランジスタQ N xによってノードN 1 2に発生した電圧を、電流出力部A 0 ~ A nのV R E F端子へ供給する。

【0055】

本実施の形態の電流駆動装置を実際の表示パネルに应用する場合、例えば、1ライン160画素とすると、出力端子数n = 160となり、電流出力部Aは161個必要となる。RGBカラーの場合は、電流出力部A 0 ~ A nと信号入力回路D inがこの3倍が必要となる。さらに、RGBで基準電流を個別に制御する場合は、図3に示した電流駆動装置のうち、基準電流供給用トランジスタQ P 1と、電圧供給源V 1が3組必要となる。動作制御回路Bは共用しても差し支えないが、個別制御してもよい。

【0056】

＜キャリブレーションモードM c＞

図3に示した電流駆動装置におけるキャリブレーションモードM cについて説明する。

【0057】

動作制御回路Bは、電流出力部A 0 ~ A nのうち1つをキャリブレーションモードM cに設定する。すなわち、電圧供給モードM1から電流供給モードM2と遷移させ、それ以外の電流出力部は電流出力モードM3に設定する。

【0058】

まず、電流出力部A0を電圧供給モードM1に設定する。電流出力部A1～Anは電流出力端子IOUTAよりそれぞれ出力端子OUT1～OUTnに電流を出力する状態に設定する。次に、電流出力部A0を電流供給モードM2に設定する。電流出力部A1～Anの動作設定は変更しない。以上により、電流出力部A0のキャリブレーションを行う。

【0059】

次に、電流出力部A0は電流出力端子IOUTBを出力端子OUT1に接続し、電流出力モードM3に設定する。電流出力部A2～Anと、出力端子OUT2～OUTnの接続は変更しない。この状態で、電流出力部A1を電圧供給モードM1、電流供給モードM2と遷移させ、キャリブレーションを行う。

【0060】

同様にして、キャリブレーション前の電流出力部の電流出力端子IOUTAまたはキャリブレーションの終わった電流出力部の電流出力端子IOUTBを出力端子に接続し、各電流出力部に対し、逐次キャリブレーションを行っていく。

【0061】

＜電流出力モードM3＞

次に、図3に示した電流駆動装置の電流出力モードM3について説明する。

【0062】

キャリブレーションモードMcに設定されていないn個の電流出力部Aは電流出力モードM3に設定され、信号入力回路Dinからそれぞれの電流出力部Aが接続されている出力端子に応じた表示データ信号を受ける。電流出力モードM3に設定されている電流出力部Aは、基準電流と上記表示データに応じた引き込み電流を出力する。

【0063】

＜リフレッシュ＞

キャリブレーションを1回しか行わない場合、電流出力部A0～Anの内部において、電圧保持容量素子C1やNchトランジスタQN1～QNmのゲートでのリークによって電圧保持容量素子C1に保持した基準電圧が変動してしまう。そのため、電流出力部に対するキャリブレーションを定期的に行う必要がある。このために、本実施の形態ではn個の出力端子OUT1～OUTnに対し、(n+1)個の電流出力部A0～Anを備え、電流を出力しない電流出力部に対しキャリブレーションを行う。

【0064】

なお、起動直後や基準電流の変更の直後以外において、一旦すべての電流供給部A0～Anにキャリブレーションを行った後は、すでに目標電圧に近い電圧が保持されているため、電圧供給モードM1によるキャリブレーションを省いてもよい。

【0065】

＜一括電圧供給モードM1'＞

上述の定期的なキャリブレーション、リフレッシュ動作のみを行う場合、本電流駆動装置の起動直後や基準電流を変更した場合には、各電流出力部のノードN2に必要な電圧を保持させなければ完全な出力が得られず、パネル表示において不均一を生じる。このため、起動時や基準電流変更時には、全電流出力部A0～AnのノードN2に対し、電流-電圧変換用トランジスタQNxにて生成する電圧を、電圧供給源V1によって一括で与える動作モードを備える。これにより全電流出力部A0～Anに、新たに設定された基準電流に近い電流値を記憶させることができ、逐次キャリブレーションによる表示の不均一性を改善することができる。

【0066】

＜基準電圧の再設定＞

上述のように各出力電流部は、電圧供給源V1によって新たな基準電流に近い電流値を仮に保持することができる。しかし、この電圧を供給するノードN12は、基準電流供給用トランジスタQP2からの吐き出し電流によって充電される。電流-電圧変換用トランジスタQNxは、吐き出し電流を供給する基準電流供給用トランジスタQP2の負荷にす

ぎないため、特に再設定される基準電流が微小な場合等、低い電圧に収束させることが困難である。このため、リセット用スイッチSw4を備え、ノードN12を接地電位に短絡する機能を備えることが望ましい。

【0067】

なお、上記実施の形態ではリセット用スイッチSw4は接地電位と電流-電圧変換用トランジスタQNxとの間に接続されているが、電流-電圧変換用トランジスタQNxの電位として予測される最低電位を生成し、この生成された電位のノードと電流-電圧変換用トランジスタQNxとの間に接続することで、電流-電圧変換用トランジスタQNx電位の再設定の動作をさらに高速化できる。

【0068】

定期的なキャリブレーションにおける電圧供給モードM1の処理を行う場合と、本項の一括電圧供給モードM1'の処理を行う場合とでは、電圧供給源V1から見た負荷が大幅に変化する。1個の電流出力部Aを充電する際に、n個の負荷に対応した電圧供給能力を使用すると、電圧供給ラインの電圧波形がひずみ、EMI（電磁妨害）等の問題を引き起こしやすくなる。逆に、1個の電流出力部に対応した電圧供給能力では、すべての電流出力部へ電圧を供給する場合に電圧供給能力が不足してしまう。この対策として、充電すべき容量の大きさに応じて、電圧供給部の電圧供給能力を可変とするとよい。

【0069】

一例として、電圧供給源V1内の出力段トランジスタの数を、上記各動作モードに応じて可変にすればよいものがある。そのような電圧供給源V1の例を図4に示す。電圧供給源V1は、差動増幅器Adと、NchトランジスタQN21、QN22と、PchトランジスタQP21、QP22と、スイッチSw5、Sw6、Sw7、Sw8により構成されている。差動増幅器Adは、その反転入力端子に電流-電圧変換用トランジスタQNxにより生成される基準電圧が入力され、非反転入力端子には電圧供給源V1の出力端子が接続され、電圧供給源V1全体としてボルテージフォロアを構成している。また、電圧供給源V1の出力端子には電流出力部A0～Anが接続されている。NchトランジスタQN21、QN22のゲートは差動増幅器Adの出力端子と接続され、ソースは接地端子に、ドレインはそれぞれスイッチSw5、Sw6を介して電圧供給源V1の出力端子へ接続されている。PchトランジスタQP21、QP22のゲートには外部より適当なバイアス電圧を与え、ソースは電源電位、ドレインはそれぞれスイッチSw7、Sw8を介して出力端子に接続されている。1個の電流出力部のみ、例えば電流出力部A0のみを電圧供給モードM1にする場合にはスイッチSw5、Sw7を導通状態、スイッチSw6、Sw8を非導通状態とすることで、電流出力部A0の電圧保持手段（図1の電圧保持用容量素子C1）のみ負荷とすることに最適な状態とする。電流出力部A0～Anのすべてを電圧供給モードM1とする場合、スイッチSw5、Sw6、Sw7、Sw8をすべて導通状態とすることで、すべての電流出力部に備わった電圧保持用容量素子C1への充電に対応できるように、電圧の供給能力を大きくする。これにより、電圧供給源V1は、負荷に応じて適切な電圧供給能力で電圧を供給できる。

【0070】

図5は本発明の別の実施の形態における電流駆動装置の構成を示す回路図である。定期的な電圧供給モードM1と一括電圧供給モードM1'とで、それぞれの動作モードのために、電圧供給能力の異なる第2の電圧供給手段を用意している。電流出力部の1個の負荷に対して電圧供給能力を合わせ込んだ第1の電圧供給手段としての電圧供給源V1に加えて、接続された電流出力部のすべてを負荷として電圧供給能力を合わせ込んだ第2の電圧供給手段としての電圧供給源V2を備えている。電圧供給源V1、V2には、動作制御回路Bより制御信号が入力される。電圧供給源V1および電圧供給源V2は、それぞれ第1の電圧を示すノードN12を入力とし、1つの電流出力部に対する電圧供給モードM1か、一括電圧供給モードM1'であるかによって、切り替え制御される。また、両電圧供給源の動作切り替え時にオーバーラップを設ければ、切り替え直後の出力波形の大きな変動を抑制できる。

【0071】

<効果>

以上のような構成により、基準電流を供給することによって電流出力部のキャリブレーションを行う電流駆動装置において、基準電流によるキャリブレーションの前に最終目標値に近い電圧を供給することで、キャリブレーション動作を高速化できる。これにより、基準電流が微小な場合や、パネルの大型化に伴う電流駆動装置の出力数の増大に対応することができる。

【0072】

なお、図1において、電流出力部の出力電流を吸い込み型とし、構成素子としてNchトランジスタを用いたが、出力電流が吐き出し型の場合には、Pchトランジスタを用いればよい。

【産業上の利用可能性】

【0073】

本発明の電流駆動装置は、出力電流の不均一性を改善することが可能であり、有機EL表示装置に用いられる電流駆動方式の表示装置のドライバ等として有用である。

【図面の簡単な説明】

【0074】

【図1】 本発明の実施の形態における電流出力部の構成を示す回路図

【図2】 図1に示す電流出力部の動作を示すタイミングチャート

【図3】 本発明の実施の形態における電流駆動装置の全体の構成を示すブロック回路図

【図4】 本発明の実施の形態における電圧供給源の具体的構成を示す回路図

【図5】 本発明の実施の形態の変形例における電流駆動装置の全体の構成を示すブロック回路図

【図6】 従来の技術における電流出力部の構成を示す回路図

【図7】 図6に示す電流駆動装置の動作を示すタイミングチャート

【図8】 従来の技術における電流駆動装置の全体の構成を示すブロック回路図

【図9】 図6に示した電流駆動装置において基準電流が微小な場合の動作を示すタイミングチャート

【符号の説明】

【0075】

A, A0～An 電流出力部

B 動作制御回路

C1 電圧保持用容量素子

Din 信号入力回路

G1～Gm 信号応答用スイッチ

I1 基準電流源

OUT1～OUTn 出力端子

QP1 基準電流供給用トランジスタ（第1の電流供給手段）

QP2 基準電流供給用トランジスタ（第2の電流供給手段）

QP_x, QN_x 電流-電圧変換用トランジスタ（電流-電圧変換手段）

QN1～QN_m Nchトランジスタ

So1, So2 電流出力用スイッチ

Sw1 電流入力用スイッチ

Sw2 キャリブレーション用スイッチ

Sw3 高速化スイッチ

T1, T2 電流出力端子

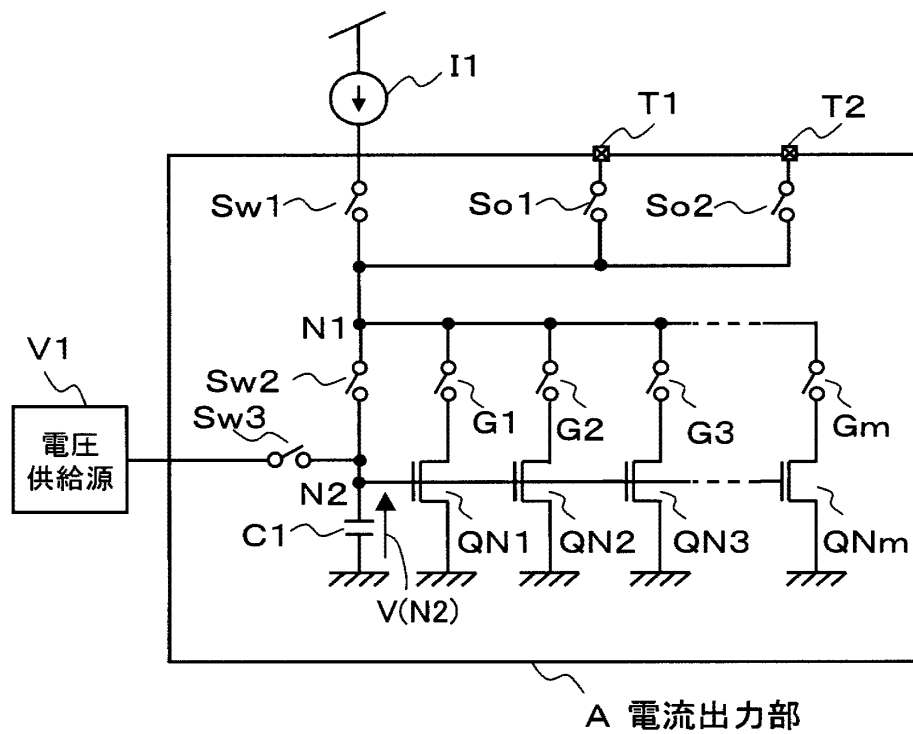
V1 電圧供給源（第1の電圧供給手段）

V2 電圧供給源（第2の電圧供給手段）

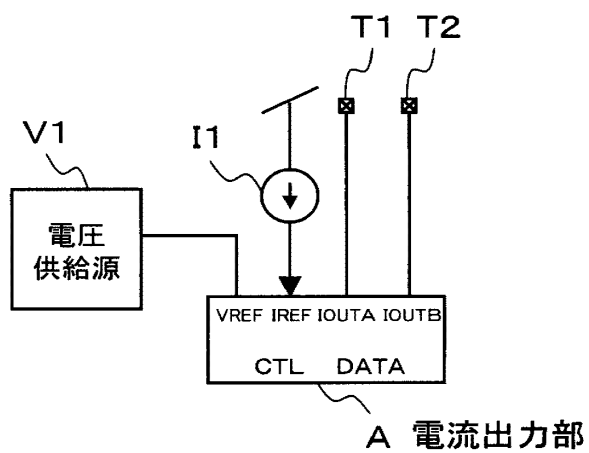
Vd 差動増幅器

【書類名】 図面
【図 1】

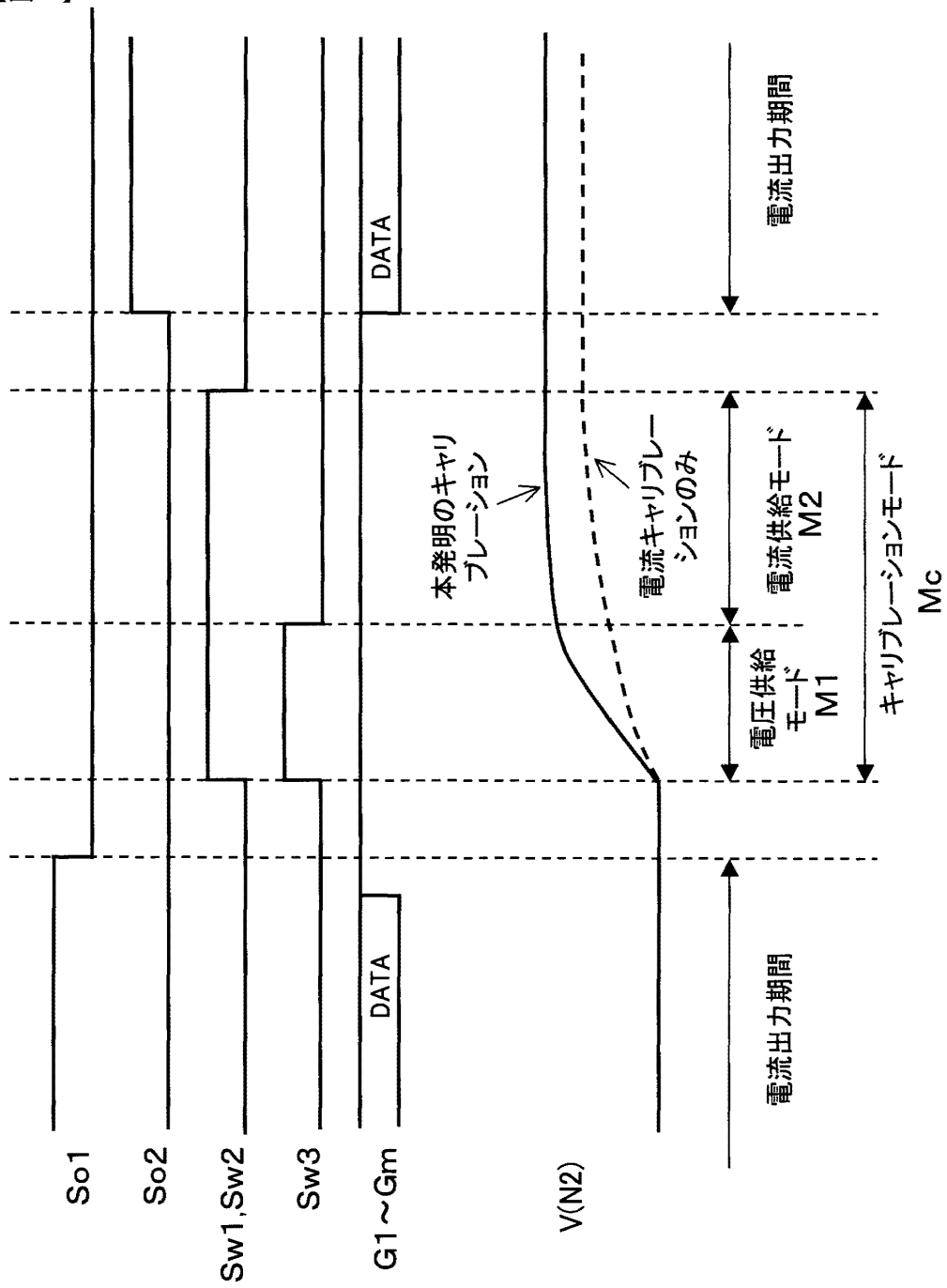
(a)

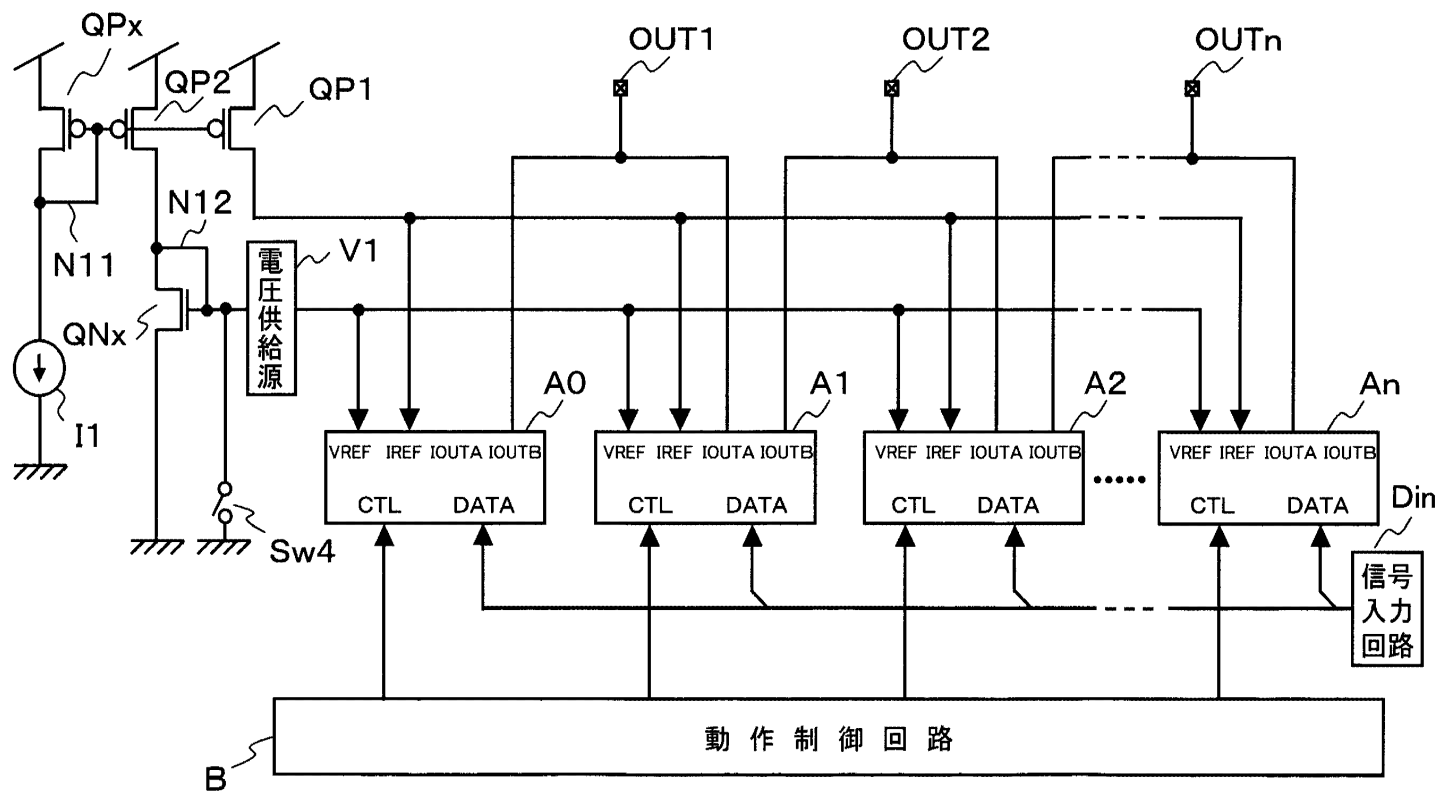


(b)

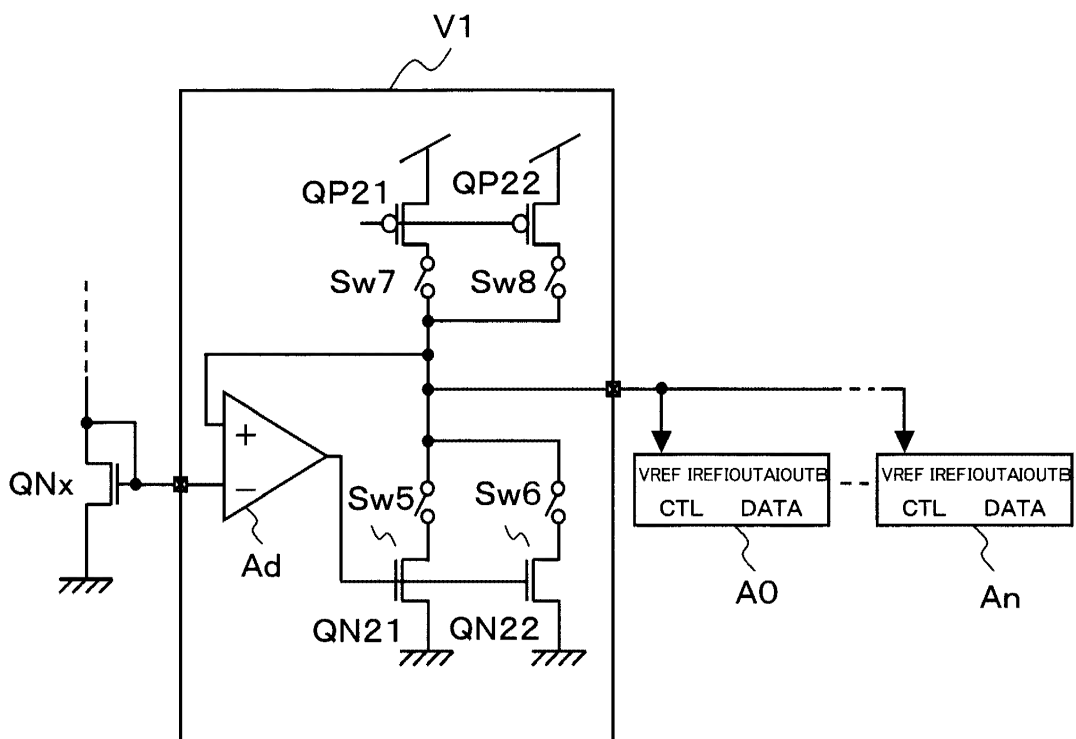


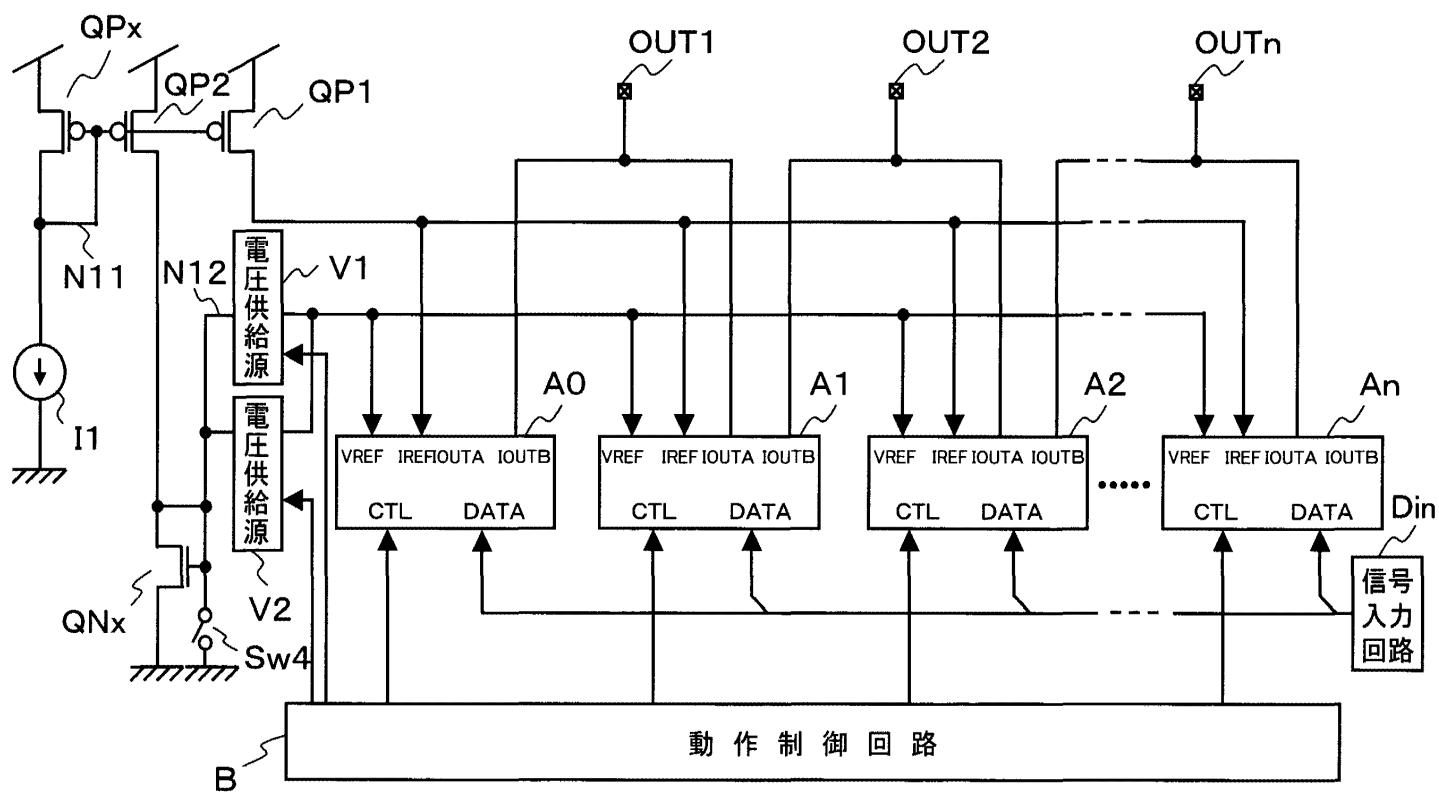
【図 2】





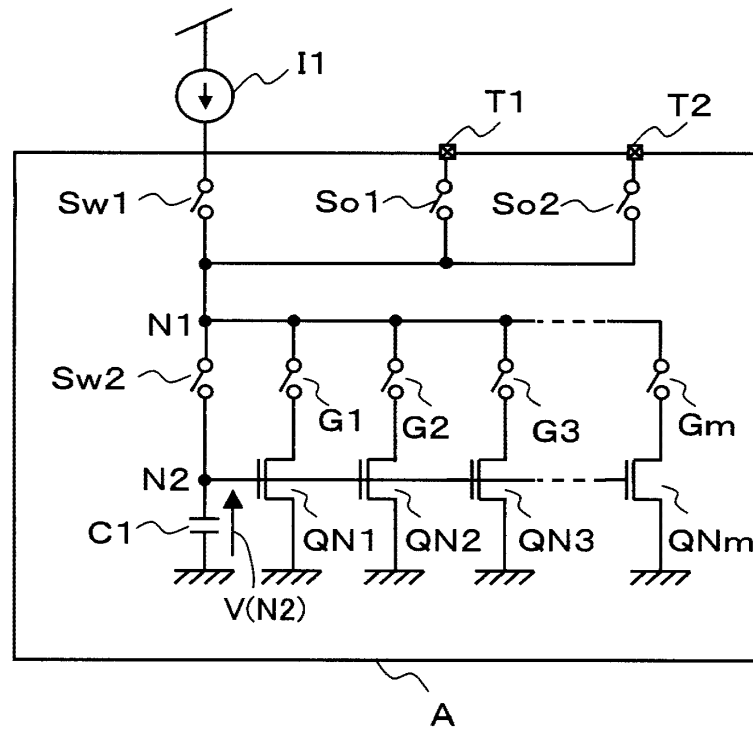
【図3】



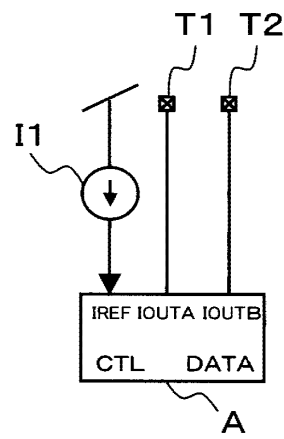


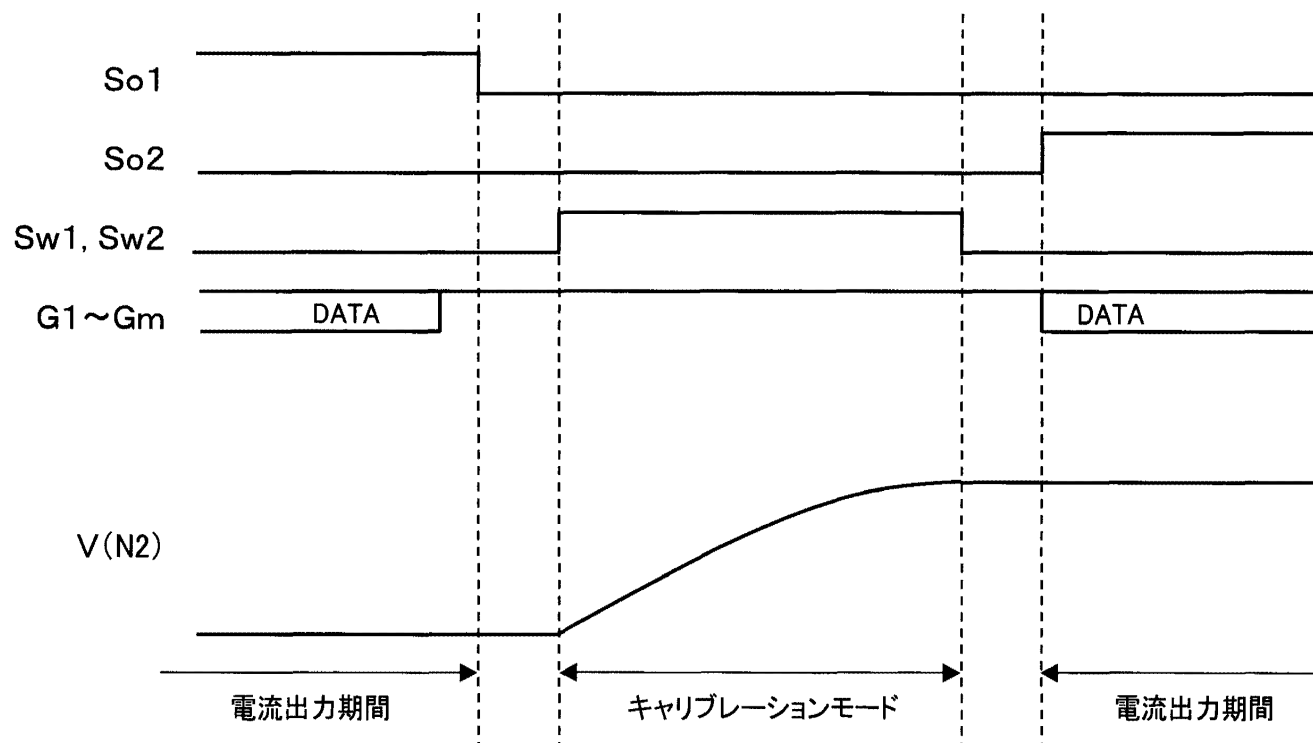
【圖 6】

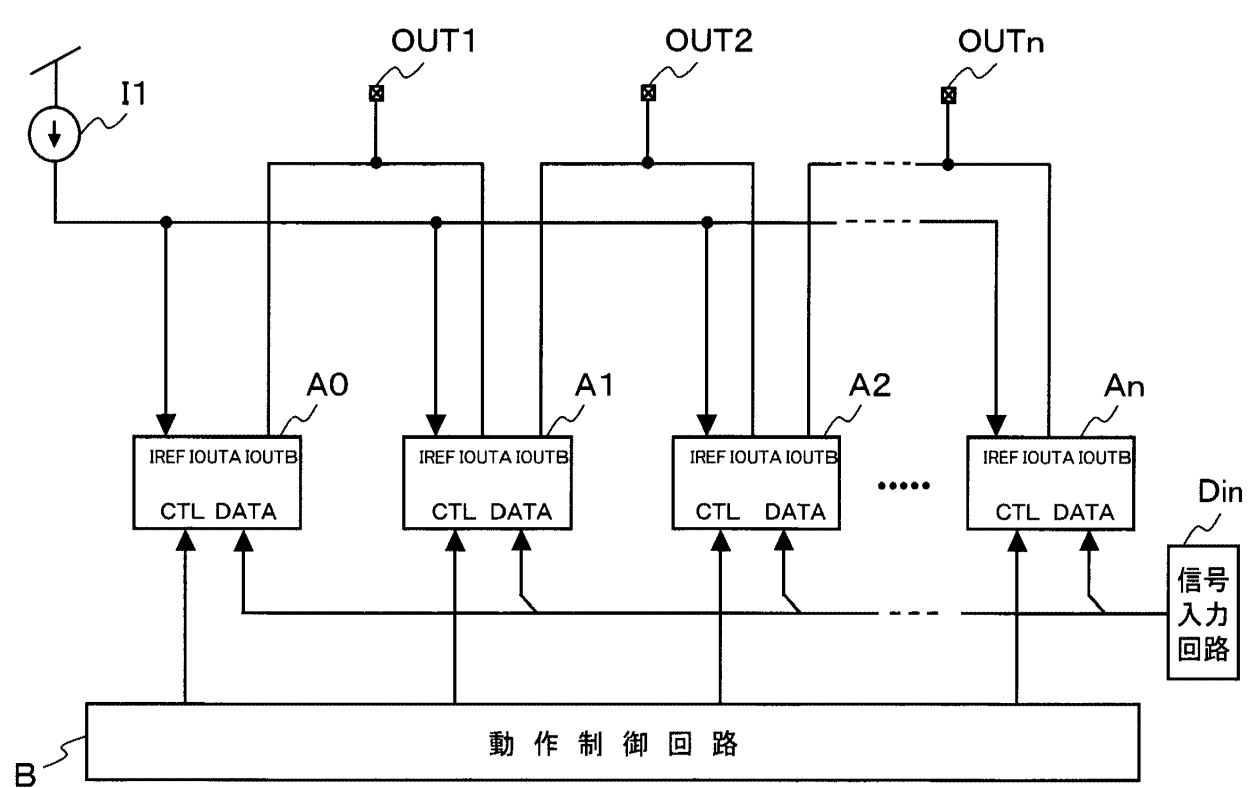
(a)



(b)

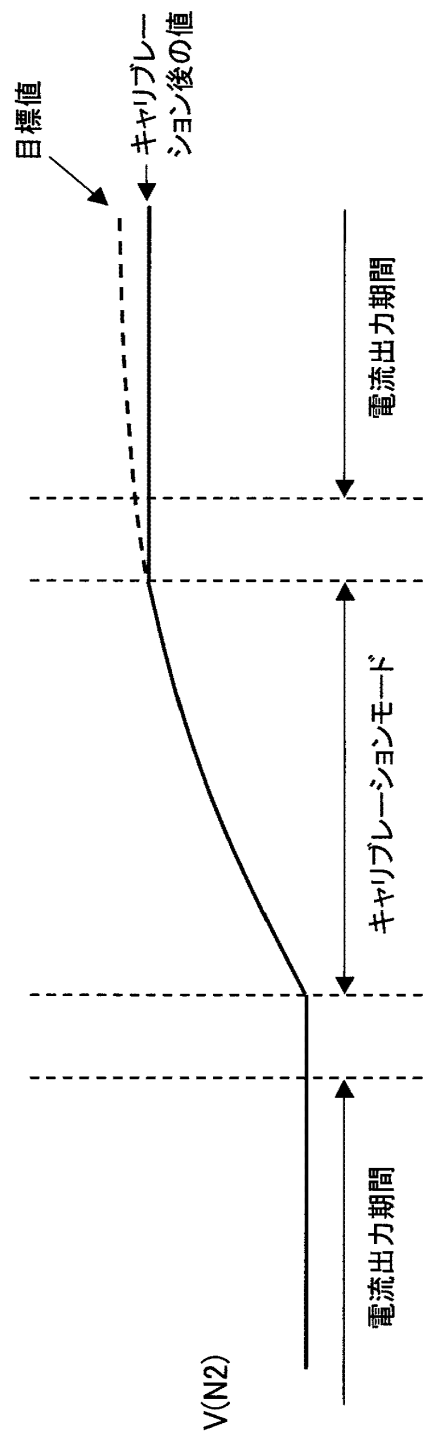






【8】

【図9】



【書類名】 要約書

【要約】

【課題】 電流出力部に電圧を保持することで基準電流を記憶し、出力端子間の電流を均一化する方式の電流駆動装置において、電流出力部のキャリブレーション時間が不足する。

【解決手段】 電圧供給手段V 1 と、電流供給手段Q P 1 と、電流 - 電圧変換機能、電圧 - 電流変換機能、電圧保持用容量素子C 1 を有する複数の電流出力部A 0 ～A n を備える。電流出力部は3つの動作モードをとり、電圧供給モードでは電圧供給手段V 1 からの電圧を受けて電圧保持用容量素子C 1 に保持し、電流供給モードでは電流供給手段Q P 1 からの電流を受け電流 - 電圧変換機能により第2の電圧を生成して電圧保持用容量素子C 1 に保持し、電流出力モードでは電圧 - 電流変換機能により電圧保持用容量素子C 1 に保持した電圧に応じた出力電流を出力する。基準電流によるキャリブレーションの前に、基準電圧により電流出力部を充電することで、電流出力部のキャリブレーションを高速に行う。

【選択図】 図3

【書類名】 手続補正書
【あて先】 特許庁長官 殿
【事件の表示】
【出願番号】 特願2006-335850
【補正をする者】
【識別番号】 000005821
【氏名又は名称】 松下電器産業株式会社
【代理人】
【識別番号】 100086737
【弁理士】
【氏名又は名称】 岡田 和秀
【電話番号】 06-6376-0857
【手続補正1】
【補正対象書類名】 明細書
【補正対象項目名】 0020
【補正方法】 変更
【補正の内容】
【0020】

また上記構成の電流駆動装置において、さらに、前記第1の電流と比例関係にある第2の電流を供給する第2の電流供給手段と、前記第2の電流を受けて前記第1の電圧を生成する電流-電圧変換手段とを備え、前記第1の電圧供給手段は、前記電流-電圧変換手段により生成された前記第1の電圧の前記電流出力部に対する供給を制御するという態様がある。このように構成すれば、第1の電圧供給手段が電流出力部に供給する第1の電圧が電流-電圧変換手段によって第2の電流から生成され、その第2の電流供給手段による第2の電流が第1の電流と比例関係にあるので、結局、第1の電圧が第1の電流に対応した値になる。したがって、第1の電圧について、電圧保持手段に保持させるべき電圧の最終目標値にほぼ一致する値の電圧を生成することが可能となる。

【手続補正2】
【補正対象書類名】 明細書
【補正対象項目名】 0041
【補正方法】 変更
【補正の内容】
【0041】

ここで、図1(a)に示した電流出力部Aを図1(b)に示すように6端子回路素子として表すことにする。図1(b)において、電流出力部Aは、基準電流入力端子IREFと電圧入力端子VREFと電流出力端子IOUTA、IOUTBと制御信号入力端子CTLと信号入力端子DATAを備える。基準電流入力端子IREFは基準電流源I1に接続され、電圧供給モードM1、電流供給モードM2において基準電流源I1からの電流を入力する。電圧入力端子VREFは電圧供給源V1に接続され、電圧供給モードM1において基準電圧を入力する。電流出力端子IOUTは電流出力モードM3になると、電流供給モードM2にて記憶された電流を出力する。制御信号入力端子CTLは動作状態を制御する制御信号を入力し、電流出力部A内の電流出力用スイッチS01、S02、電流入力用スイッチSw1、キャリブレーション用スイッチSw2、高速化スイッチSw3および信号応答用スイッチG1～Gmの切り替えを制御する。信号入力端子DATAは出力電流値を制御するmビットの入力信号を入力し、信号応答用スイッチG1～Gmの切り替えを制御する。

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11/954,659	12/12/2007	2816	1030	056937-0414	10	2

CONFIRMATION NO. 4296

53080
MCDERMOTT WILL & EMERY LLP
600 13TH STREET, NW
WASHINGTON, DC 20005-3096

FILING RECEIPT



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Date Mailed: 12/27/2007

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Power of Attorney: The patent practitioners associated with Customer Number 53080

Domestic Priority data as claimed by applicant

Foreign Applications

JAPAN 2006-335850 12/13/2006

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Projected Publication Date: To Be Determined - pending completion of Security Review

Non-Publication Request: No

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Title

CURRENT DRIVING DEVICE

Preliminary Class

327

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Case Docket Number: 056937-0414

Customer Number: 53080

**UTILITY PATENT APPLICATION
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Transmitted herewith for filing is the patent application of:

**INVENTOR: Makoto MIZUKI, Kazuyoshi NISHI, Tetsuro OHMORI,
Tomokazu KOJIMA, Hiroshi KOJIMA
FOR: CURRENT DRIVING DEVICE**

Enclosed are:

- ☒ 38 pages of specification, claims, abstract.
- ☒ Declaration and Power of Attorney.
- ☒ Priority Claimed.
- ☒ Request to retrieve Electronic Priority Application.
- ☒ 9 sheets of formal drawing.
- ☒ Information Disclosure Statement, Form PTO-1449 and reference.
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Independent Claims	2	-3	0	\$210.00	\$0.00
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Sheets of specification and drawing (\$250.00 for each 50 sheets in excess of 100)					\$0.00
Basic Filing Fee					\$310.00
Patent Search Fee					\$510.00
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Total of Above Calculations					\$1,030.00
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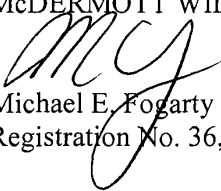
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Case Docket Number: 056937-0414

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Respectfully submitted,

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Date: December 12, 2007

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Case Docket Number: 056937-0414

Customer Number: 53080

**UTILITY PATENT APPLICATION
UNDER 37 CFR 1.53(b)**

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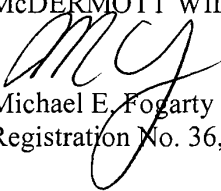
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CURRENT DRIVING DEVICE

FIELD OF THE INVENTION

- [1] The present invention relates to a current driving device used preferably as a driver for displays such as organic EL (Electro-luminescence) panels, LED panels, and the like.

BACKGROUND OF THE INVENTION

- [2] Recently, flat-panel displays have a larger screen and higher definition, while establishing reduction in thickness, weight, and cost. With such backgrounds, it is required for display drivers to improve the uniformity in the displayed image qualities through decreasing variations between output electric currents that are outputted from output terminals. Variations in the electric currents in static actions of current mirrors include variations caused due to fabrication processes of each transistor, variations of gate voltages caused due to resistances of power supply wirings, and the like. Further, variations due to dynamic actions of the current mirrors include variations caused due to injection of electric charges from a display panel or instantaneous fluctuations of power supply, for example. Furthermore, generally, a driver IC is formed in a multi-output structure with a stick-like slim shape, since it is mounted to a frame part of a flat panel. Because of restrictions in the LSI shape, characteristics of transistors disposed therein vary depending on positions of slim-layout elements. Therefore, even if a same gate voltage is applied in a current mirror structure, the output currents from each of current-summing DA converter circuits do not necessarily become the same.

- [3] As a method for decreasing such variations, there is a current driving device having a current output part, such as the one shown in FIG. 6A and FIG. 6B, for example (see US 2005/0231241A1, for example). This current output part has a calibration function and a current output function. "Calibration" means to have a reference current value by a reference current source stored in the current output part.
- [4] Under a calibration mode, current output switches So1 and So2 are set to a nonconductive state, while a current input switch Sw1, a calibration switch Sw2, and all signal response switches G1 - Gm are set to a conductive state. Current output terminals T1 and T2 are isolated from the outside. Nodes N1 and N2 are short-circuited, and drains and gates of Nch transistors QN1 - QNm are short-circuited to receive electric currents from a reference current source I1. Through this, the Nch transistors QN1 - QNm generate, at the node N2, a gate voltage that is necessary for allowing the electric current from the reference current source I1 to flow through the transistors themselves. A voltage holding capacitance element C1 is charged to the above-described gate voltage. A voltage V (N2) of the node N2 corresponds to a voltage that is capable of passing an electric current that is equal to the reference current generated by the reference current source I1 through the Nch transistors QN1 - QNm which are all in a conductive state. In conclusion, the current output part A comes to store the reference current generated by the reference current source I1.
- [5] Under a current output mode, the current input switch Sw1 and the calibration switch Sw2 are turned to a nonconductive

state, and either one of the current output switch So1 or So2 is set to a conductive state while the other is remained in a nonconductive state. The conduction state of the signal response switches G1 - Gm is determined depending on an input signal supplied from the outside. The voltage holding capacitance element C1 holds the voltage charged by the calibration action, and continues to supply the electric current to the gate terminals of the Nch transistors QN1 - QNm. The Nch transistors QN1 - QNm output an electric current in accordance with the voltage V (N2) of the node N2 from one (in an conductive state) of the current output terminals T1 and T2, in accordance with the conduction state of the signal response switches G1 - Gm.

[6] FIG. 7 shows a timing chart of a series of actions regarding calibration and output of the electric current performed in the current-summing DA converter circuit shown in FIG. 6A and FIG. 6B. The conductive state of the switches is shown with "H", and the nonconductive state thereof is shown with "L". "V (N2)" indicates the voltage V (N2) of the node N2.

[7] Before calibration, the current output part A sets the current output witch So1 to be in a conductive state, and outputs, from the current output terminal T1, the output current in accordance with the state of the signal response switches G1 - Gm which are controlled by the voltage V (N2) of the node N2 and an input signal. The current output switch So2, the current input switch Sw1, and the calibration switch Sw2 are set to be in a nonconductive state.

[8] During the calibration period, the current output switches So1, So2 are set to a nonconductive state, the current input

switch Sw1 and the calibration switch Sw2 are set to a conductive state, and the signal response switches G1 - Gm for selecting the electric currents from the Nch transistors QN1 - QNm are all set to a conductive state. Through this, the Nch transistors QN1 - QNm are set in a state where only the electric current of the reference current source I1 is supplied, and the voltage V (N2) of the node N2 is determined in accordance with the above-described actions.

[9] After completing the above-described calibration, the current input switch Sw1 and the calibration switch Sw2 are set to a nonconductive state, so that the voltage holding capacitance element C1 holds the electric charge. That is, the voltage V (N2) of the node N2 is being maintained. Thereafter, the current output switch So2 is set to a conductive state, and the sum of the electric currents selected by the signal response switches G1 - Gm in accordance with the input signal is outputted from the current output terminal T2.

[10] FIG. 8 shows a structure of a current driving device that utilizes the current output part A shown in FIG. 6A and FIG. 6B. (n+1)-numbers of current output parts A0 - An control the operation states under a calibration mode and a current output mode in accordance with control signals supplied from an action control circuit B. A signal input circuit Din supplies signals for controlling the signal response switches G1 -Gm within the internal structural elements (see FIG. 6A) of each of the current output parts A0 - An. Calibration by the reference current source I1 is performed on a single current output part among the (n+1)-numbers of current output parts

A0 - A1 by an internal operation of each of the current output parts A0 - An. Calibration is performed in order from A0, to A1, A2, ---, and to An. The current output parts that are not under calibration are set to be in the current output mode, and output an electric current to n-numbers of output terminals OUT1 - OUTn. The electric currents are outputted in order from A0 to A1, A2, ---, and to An.

[11] The reference current, when there are a plurality of current-summing DA converter circuits with the above-described current output parts, can be combined into the electric currents of the same current source. This makes it possible to achieve the uniformity in the display on a panel.

[12] Other related documents are: Japanese Unexamined Patent Publication 2004-219955, Japanese Unexamined Patent Publication 2005-121843, US2004/0251844A1, US7050024B2, US6594606B2, US2006/0158402A1.

[13] With this method, however, the capacity for charging/discharging the voltage holding capacitance element C1 becomes insufficient when the current value of the reference current source I1 is very small, so that it is difficult to charge the current of the Nch transistors QN1 - QNm to accurately meet the value of the current from the reference current source I1 within the calibration period. FIG. 9 shows the state where the voltage holding capacitance element C1 is insufficiently charged because the reference current is very small.

[14] Further, when there is a change in the current value of the reference current source I1, the reference currents become varied depending on the output terminals with the successive

calibration, until the reference currents of all the current output parts A0 - An are updated.

SUMMARY OF THE INVENTION

[15] An object of the present invention therefore is to provide a current driving device which can perform calibration at a high speed and improve the non-uniformity of the output currents even when a reference current is very small and when there is a change in the reference current.

[16] A current driving device of the present invention comprises:

- a first voltage supply part for supplying a first voltage;

- a first current supply part for supplying a first electric current;

- a plurality of output terminals; and

- a plurality of current output parts for outputting an electric current in accordance with the first electric current, each of the current output parts comprising a current-voltage converting function, a voltage-current converting function, a voltage holding part, and at least one current output terminal, wherein

- the current output part takes three operation modes, i.e. a voltage supply mode, a current supply mode, and a current output mode,

- under the voltage supply mode, the current output part receives the first voltage from the first voltage supply part and holds the voltage in the voltage holding part,

- under the current supply mode, the current output part receives the first current from the first current supply part, and generates a second voltage by the current-voltage converting function and holds the voltage in the voltage

holding part, and

under the current output mode, the current output part outputs an output current according to the voltage held in the voltage holding part by the voltage-current converting function. The voltage supply mode and the current supply mode correspond to the calibration mode.

[17] In the current driving device constituted in the manner described above, the current output part receives a supply of the first voltage from the first voltage supply part under the voltage supply mode, and holds the first voltage in the voltage holding part. Then, under the current supply mode, the current output part receives a supply of the first electric current from the first current supply part, generates the second voltage by the current-voltage converting function, and holds the second voltage in the voltage holding part. This makes it possible to charge the voltage holding part to a prescribed voltage at a higher speed. Then, under the current output mode, the current output part outputs an electric current according to the voltage held in the voltage holding part through the voltage-current converting function. For charging the voltage holding part, it is charged with the first voltage to a value close to the target voltage, and then charged further with a supply of the first electric current. Thus, even if the reference current supplied from the first current supply part is very small, it is possible to speed up the action for supplying the voltage to the voltage holding part until reaching the reference current and also to obtain the reference current accurately.

[18] In the current driving device with the above-described

structure, each of the output terminals is connected to the current output terminals provided to the plurality of the current output parts, and each of the plurality of current output parts is connected in parallel to the first current supply part and the first voltage supply part used in common. With this structure, the voltage holding parts provided to all the current output parts can be charged provisionally to the first voltage when it becomes necessary to perform extensive calibrations on all the current output parts, e.g. right after the startup or when there is a change in the first electric current. Therefore, it is possible to suppress unevenness in the display caused due to the change in the first electric current.

[19] Further, in the current driving device with the above-described structure, each of the current output parts actuates the current-voltage converting function under the voltage supply mode. With this structure, for charging the voltage holding part, the voltage obtained by converting the first electric current from the first current supply part can be combined with the supply of the first voltage from the first voltage supply part. Therefore, still higher speed charging can be achieved.

[20] Furthermore, in the current driving device with the above-described structure, each of the current output parts comprises a function of stopping the current-voltage converting function under the voltage supply mode. With this structure, all the electric currents supplied from the first voltage supply part can be utilized for charging the voltage holding part. Thus, the power consumption can be reduced.

[21] Moreover, the current driving device with the above-described structure further comprises a second current supply part for supplying a second electric current that is proportional to the first electric current, and a current-voltage converting part for generating the first voltage by receiving the second electric current, wherein the first voltage supply part controls supplies of the first voltage generated by the current-voltage converting part to the current output parts. With this structure, the first voltage supplied from the first voltage supply part to the current output part is generated from the second electric current by the current-voltage converting part. The second electric current from the second current supply part is proportional to the first electric current, so that the first voltage comes to have a value that corresponds to the first electric current. Therefore, it is possible to generate the first voltage having a value that almost equals to the final target value to be held in the voltage holding part.

[22] Further, in the current driving device with the above-described structure, the current-voltage converting part comprises a switching part for short-circuiting a node at which the first voltage emerges to a reference voltage node. When there is a change in the first electric current or the second electric current, it also takes time to change the second voltage generated by the current-voltage converting part. With this structure, however, the output voltage of the current-voltage converting part can be reset through actuating the switching part. Therefore, it is possible to speed up the change of the second voltage by the

current-voltage converting part.

[23] Furthermore, the current driving device with the above-described structure further comprises a second voltage supply part with a larger voltage supply capacity than that of the first voltage supply part, wherein the use of the first voltage supply part and the use of the second voltage supply part are switched in accordance with the number of the current output parts that take the voltage supply mode among the plurality of current output parts. When there are a large number of current output parts, the load of the voltage supply part changes largely depending on how many current output parts are under the voltage supply mode. With this structure, however, it is possible to reduce EMI (electromagnetic interference) and the power consumption by changing the output voltages smoothly through adding the second voltage supply part and switching between the use of the first voltage supply part and the use of the second voltage supply part in accordance with the load.

[24] Alternatively, in the current driving device with the above-described structure, the first voltage supply part is constituted to be capable of changing its voltage supply capacity in accordance with the number of the current output parts that take the voltage supply mode among the plurality of current output parts. With this structure, it is possible to reduce EMI (electromagnetic interference) and the required area because the first voltage supply part is provided with the function of optimizing the voltage supply capacity in accordance with the load.

[25] A display device according to the present invention related

to the current driving device described above comprises one of the above-described current driving devices mounted thereon so as to be driven by the current driving device. Displays on the screen can be made uniform with this display device.

[26] A current driving device according to the present invention comprises:

- a current input switch for controlling connection/disconnection states with respect to a current supply part;

- a voltage holding part for holding a reference voltage, which is charged by a flown current;

- a calibration switch interposed between the current input switch and the voltage holding part;

- a plurality of voltage-current converting elements for generating an electric current in accordance with the reference voltage held in the voltage holding part;

- a plurality of signal response switches that are on/off controlled in accordance with inputted signals, the response switches being connected in series to each of the voltage-current converting elements, and each of which being connected in parallel to the calibration switch;

- a plurality of current output switches, each being interposed between a connection node, which is provided between the current input switch and the calibration switch, and the plurality of current output terminals; and

- a high-speeding switch for controlling connection/disconnection states of the voltage supply part with respect to the voltage holding part.

[27] The calibration mode comprises two stages, i.e. the voltage supply mode and the current supply mode. In the voltage supply mode, the high-speeding switch is set to be in a conductive state to connect the voltage supply part to the voltage holding part in order to boost up the potential level of the voltage holding part at a high speed. At that time, the current output switches are all set to be in a nonconductive state, and the calibration switch and all the signal response switches are set to be in a conductive state. Then, in the current supply mode, the high-speeding switch is turned to a nonconductive state. The current input switch and the calibration switch are set to be in a conductive state, so that the sum of the current values flown in the voltage-current converting element becomes equal to the reference current value that is supplied from the current supply part. Thus, the voltage holding part comes to hold the voltage that corresponds to passing the current (equivalent to the reference current value) through the voltage-current converting element. That is, the reference current value is stored. As described, the potential of the voltage holding part is raised at a high speed by using the voltage supply part under the voltage supply mode that is the first half part of the calibration mode, and the reference current value by the current supply part is stored accurately in the latter half stage of the calibration mode. Therefore, even when the current value of the reference current source is very small, it becomes possible with the voltage supply part to compensate for the capacity for supplying the voltage to the voltage holding part till reaching the reference current and to complete the calibration at a high speed for

allowing the current flowing the voltage-current converting element to meet accurately with the current value of the reference current source.

BRIEF DESCRIPTION OF THE DRAWINGS

[28] The present invention is illustrated be way of example and not limitation in the figures of the accompanying drawings, in which like references indicate similar elements and in which:

FIG. 1A is a circuit diagram for showing a structure of a current output part according to a preferred embodiment of the present invention;

FIG. 1B is a block circuit diagram for showing the structure of the current output part according to the preferred embodiment of the present invention;

FIG. 2 is a timing chart for showing actions of the current output part shown in FIG. 1A and FIG. 1B;

FIG. 3 is a block circuit diagram for showing an overall structure of a current driving device according to the preferred embodiment of the present invention;

FIG. 4 is a circuit diagram for showing a specific structure of a voltage supply source according to the preferred embodiment of the present invention;

FIG. 5 is a block circuit diagram for showing an overall structure of a current driving device according to a modification example of the preferred embodiment of the present invention;

FIG. 6A is a circuit diagram for showing a structure of a current output part according to a conventional technique;

FIG. 6B is a block circuit diagram for showing the structure

of the current output part according to the conventional technique;

FIG. 7 is a timing chart for showing actions of the current output part shown in FIG. 6A and FIG. 6B;

FIG. 8 is a block circuit diagram for showing an overall structure of a current driving device according to the conventional technique; and

FIG. 9 is a timing chart for showing actions of the current output part shown in FIG. 6A and FIG. 6B, when a reference current is very small.

DETAILED DESCRIPTION OF THE INVENTION

[29] Hereinafter, an embodiment of a current driving device according to the present invention will be described in detail by referring to the accompanying drawings. Same reference numerals are applied to the same or corresponding components within the drawings.

[30] FIG. 1A is a circuit diagram for showing a structure of a current output part A that is mounted to a current driving device according to a preferred embodiment of the present invention, FIG. 1B is a block circuit diagram for showing the structure of the current output part A, FIG. 2 is a timing chart for describing actions of the current output part A, FIG. 3 is a block circuit diagram for showing the overall structure of the current driving device, and FIG. 4 is a circuit diagram for showing an embodiment of a voltage supply source V1.

[31] <Current Output Part>

First, the current output part A will be described by referring to FIG. 1A and FIG. 1B. One end of a voltage holding

capacitance element C1 is connected to a ground terminal, and the other end is connected in common to gate terminals of m-numbers of Nch transistors QN1 - QNm. Each source of the Nch transistors QN1 - QNm is connected to a ground terminal, and each drain thereof is connected in series to signal response switches G1 - Gm which are ON/OFF controlled in accordance with input signals. The other ends of the signal response switches G1 - Gm are connected in common, and are also connected, via a current input switch Sw1, to a reference current source I1 that supplies a constant current value (first electric current) to the current output part A, while being connected to the voltage holding capacitance element C1 via a calibration switch Sw2. A node N1 for connecting the current input switch Sw1, the calibration switch Sw2, and the signal response switches G1 - Gm is connected to current output terminals T1 and T2 via current output switches So1 and So2, respectively. The circuit structure that has been described heretofore is the same as the circuit structure of a conventional technique shown in FIG. 6A and FIG. 6B.

- [32] In this embodiment, further, a voltage supply source V1 for supplying a constant voltage (first voltage) to the current output part A is connected, via a high-speeding switch Sw3, to a node N2 that is a connection between the voltage holding capacitance element C1 and the calibration switch Sw2. The voltage supply source V1 corresponds to a first voltage supply part. The reference current source I1 corresponds to a first current supply part. The voltage holding capacitance element C1 corresponds to a voltage holding part. As the voltage holding capacitance element C1, a parasitic capacitance

provided originally to the gate terminals of the Nch transistors QN1 - QNm may be used instead.

[33] This current output part A takes three operation states such as a voltage supply mode M1, a current supply mode M2, and a current output mode M3. Among those, the voltage supply mode M1 and the current supply mode M2 constitute a calibration mode Mc.

[34] «Voltage Supply Mode M1»

Now, the voltage supply mode M1 of the current output part A will be described first.

[35] First, each of the current output switches So1 and So2 is set to a nonconductive state, so that the current output terminals T1 and T2 are isolated from the node N1. Further, the high-speeding switch Sw3 is set to a conductive state, so that the voltage supply source V1 and the node N2 are connected. At this time, the voltage holding capacitance element C1 is charged to a constant voltage (this corresponds to the first voltage, and will be referred to as a reference voltage hereinafter) that is supplied from the voltage supply source V1.

[36] It is also possible that the current supply mode M2 to be described next is activated simultaneously with the voltage supply mode M1. In that case, the current input switch Sw1, the calibration switch Sw2, and all the signal response switches G1 - Gm are set to be in a conductive state.

[37] «Current Supply Mode M2»

Next, the current supply mode M2 of the current output part A will be described. Under this current supply mode M2, a current-voltage converting function is actuated. Thus, the

current input switch Sw1, the calibration switch Sw2, and all the signal response switches G1 - Gm are set to be in a conductive state. The high-speeding switch Sw3 is turned to a nonconductive state so that the node N2 is isolated from the voltage supply source V1. The current output switches So1 and So2 are remained in the nonconductive state.

[38] At this time, the drains and gates of the Nch transistors QN1 - QNm are connected, thereby exhibiting a diode characteristic. Therefore, the Nch transistors QN1 - QNm have an electric current (reference current) with a constant current value from the reference current source I1 flown therein as a load. At this time, a gate voltage for passing the electric current from the reference current source I1 is generated uniquely at the gates of the Nch transistors QN1 - QNm. Therefore, the voltage holding capacitance element C1 accumulates the electric charges in accordance with the gate voltages. As described, the voltage holding capacitance element C1 holds the gate voltage for allowing the electric current with the same current value as that of the reference current to be flown. The current output part A stores the reference current value.

[39] «Current Output Mode M3»

Next, the current output mode M3 of the current output part A will be described. Under this current output mode M3, a voltage-current converting function is actuated. Thus, the current input switch Sw1 and the calibration switch Sw2 are set to be in a nonconductive state, and either the current output switches So1 or So2 is turned to a conductive state from a nonconductive state. The output switches So1 and So2

are not set to be in a conductive state simultaneously. The high-speeding switch Sw3 is remained in the nonconductive state. The voltage holding capacitance element C1 has an accumulation of the electric charges in accordance with the gate voltages for allowing the electric current with the same current value as that of the reference current to be flown under the above-described current supply mode M2. A gate voltage according to the electric charges accumulated in the voltage holding capacitance element C1 is applied to the gates of the Nch transistors QN1 - QNm. Thus, it is possible to output a sink current having a current value proportional to the reference current in accordance with the conduction states of the current output switches So1, So2 and the signal response switches G1 - Gm, through connecting a power source to the current output terminal T1 or the current output terminal T2. The output current also depends on the conduction states of the signal response switches G1 - Gm, which is the sum of the electric currents outputted from the Nch transistors whose signal response switches G1 - Gm (connected to each transistor) are in a conductive state among the output currents from the Nch transistors QN1 - QNm. If all the signal response switches G1 - Gm are in a conductive state, the output current obtained thereby is the maximum output current of the current output parts A under execution of the above-described current supply. The value thereof equals to the reference current.

[40] Through a series of these actions, it becomes possible to copy the reference current to the current output part A and to output the electric current in accordance with the reference current and an input signal. The electric current can be

copied with only the current supply mode M2 and the current output mode M3. However, with the voltage supply mode M1, an insufficient charge of the voltage holding capacitance element C1 can be overcome and the electric current can be copied at a higher speed by charging the voltage of the Node N1 that is connected to the gate terminals of the Nch transistors QN1 - QNm to a value close to a target voltage (convergent voltage under the current supply mode M2).

[41] With this embodiment, it is possible to constitute an m-bit current-summing DA converter circuit through multiplying the current capacities of the Nch transistors QN1 - QNm by 1, 2, 4, ---, 2^m . Alternatively, the reference current source I1 may be provided for each bit. Further, the current-summing DA converter circuit illustrated in the embodiment is merely an example, and the signal response switches G1 - Gm may be omitted for a case where only the equivalent electric current is to be copied, for example.

[42] Now, the current output part A shown in FIG. 1A is illustrated as a six-terminal circuit device as shown in FIG. 1B. In FIG. 1B, the current output part A comprises a reference current input terminal IREF, a voltage input terminal VREF, current output terminals IOUTA, IOUTB, a control signal input terminal CTL, and a signal input terminal DATA. The reference input terminal IREF is connected to the reference current source I1, and receives electric currents inputted from the reference current source I1 under the voltage supply mode M1 and the current supply mode M2. The voltage input terminal VREF is connected to the voltage supply source V1, and receives a reference voltage under the voltage supply mode M1. When the

current output terminal IOUT turns to the current output mode M3, the current output terminals IOUT output the electric current stored under the current supply mode M2. The control signal input terminal CTL receives inputs of control signals for controlling the operation states, and performs control for switching the current output switches So1, So2, the current input switch Sw1, the calibration switch Sw2, the high-speeding switch Sw3, and the signal response switches G1 - Gm within the current output part A. The signal input terminal DATA receives inputs of the input signals of m bits for controlling the output current values, and performs control for switching the signal response switches G1 - Gm.

[43] Next, actions of the current output part A according to the embodiment that is constituted in the above-described manner will be described by referring to the timing chart of FIG. 2. FIG. 2 illustrates the above-described three operation modes (the voltage supply mode M1, the current supply mode M2, and the current output mode M3). The conductive state of the switch is shown with "H", and the nonconductive state thereof is shown with "L". Further, "V (N2)" indicates the voltage V (N2) of the node N2. The voltage V (N2) of the node N2 according to the embodiment is illustrated with a solid line and the state of the voltage in the case of a conventional technique where the calibration only with the current supply mode M2 is started simultaneously is illustrated with a broken line.

[44] Before calibration, the current output part A sets the current output switch So1 to be in a conductive state, and outputs, from the current output terminal T1, the output

currents according to the states of the signal response switches G1 - Gm which are controlled by the voltage V (N2) of the node N2 and the input signals. The current output switch So2, the current input switch Sw1, the calibration switch Sw2, and the high-speeding switch Sw3 are in a nonconductive state.

[45] During the whole calibration period, the current output switches So1, So2 are set to be in a nonconductive state, and the signal response switches G1 - Gm for selecting the electric currents from the Nch transistors QN1 - QNm are all set to be in a conductive state. Details thereof are as follows. Under the voltage supply mode M1, the current input switch Sw1, the calibration switch Sw2, and the high-speeding switch Sw3 are set to be in a conductive state so as to supply the reference current and the reference voltage to charge the voltage holding capacitance element C1 from the node N2. Under the current supply mode M2, the high-speeding switch Sw3 is turned to a nonconductive state from the states of the switches under the voltage supply mode M1. Through this, only the electric current from the reference current source I1 is to be supplied to the Nch transistors QN1 - QNm, and the voltage V (N2) of the node N2 is determined according to the above-described actions. The voltage (N2) of the node N2 corresponds to a voltage that is capable of passing an electric current that is equivalent to the reference current by the reference current source I1 through the Nch transistors QN1 - QNm under such a condition that all the Nch transistors QN1 - QNm are in a conductive state. As a result, the current output part A comes to store the reference current by the reference current source I1.

- [46] After completing the calibration described above, first, the current input switch Sw1 and the calibration switch Sw2 are turned to a nonconductive state so that the voltage holding capacitance element C1 comes to hold the electric charge. That is, the voltage V (N2) of the node N2 is maintained. Thereafter, the current output switch So2 is turned to a conductive state to output, from the current output terminal T2, the sum of the electric currents that are selected by the signal response switches G1 - Gm based on the input signals.
- [47] In the explanations above, the current input switch Sw1 and the calibration switch Sw2 are turned to a conductive state to achieve high-speed actions under the voltage supply mode M1. However, even if the current switch Sw1 and the calibration switch Sw2 are in a nonconductive state, it is also possible to achieve faster convergence compared to the case of the conventional technique, and to reduce the electric current by the amount of the reference current source compared to the above-described case.
- [48] Next, the overall structure of the current driving device according to the embodiment will be described by referring to FIG. 3. This current driving device comprises: n-numbers of output terminals OUT1 - OUTn; (n+1)-numbers of current output parts A0 - An; a reference current supply transistor QP1 that constitutes a first current supply part; a reference current supply transistor QP2 that constitutes a second current supply part; a voltage supply source V1; an action control circuit B; a signal input circuit Din; current-voltage converting transistors QNx, QPx; a reference current source I1; and a reset switch Sw4. Each of the current output parts

A0 - An is the current output part shown in FIG. 1A. A reference current input terminal IREF is connected to the reference current supply transistor QP1, and a voltage input terminal VREF is connected to the voltage supply source V1. An action control terminal CTL receives signals for controlling the action states, which are inputted from the action control circuit B. A signal input terminal DATA receives signals for controlling the output current values from the signal input circuit Din. Each of current output terminals IOUTA and IOUTB is connected to one of the output terminals OUT1 - OUTn, and outputs an output current corresponding to the reference current and the input signal DATA to the outside in accordance with the state of the control signal CTL. The reference current supply transistor QP1 is connected between the IREF terminals of the current output parts A0 - An and a power supply terminal, and a gate terminal thereof is connected to a node N11. The reference current supply transistor QP2 is connected between a node N12 and the power supply terminal, and a gate terminal thereof is connected to the node N11. The P-channel-type current-voltage converting transistor QPx is connected between the reference current source I1 and the power supply terminal, and a gate terminal thereof is short-circuited with its drain. The N-channel-type current-voltage converting transistor QNx is connected between the reference current supply transistor QN2 and a ground terminal, and a gate terminal thereof is short-circuited with its drain. The reset switch Sw4 is connected between the node N12 and the ground terminal.

[49] Note here that connections of the current output terminals

IOUTA and IOUTB of the current output parts A0 - An are allocated according to the following rules. The current output terminal IOUTA of the current output part A0 is not connected to the outside, and the current output terminal IOUTB is connected to the output terminal OUT1 of the current driving device. The current output terminal IOUTA of the current output part A1 is connected to the output terminal OUT1, and the current output terminal IOUTB is connected to the output terminal OUT2. The current output parts thereafter are connected in the same manner, and the current output terminal IOUTA of the current output part An is connected to the output terminal OUTn while the current output terminal IOUTB is not connected to the outside. That is, for the n-numbers of output terminals OUT1 - OUTn, in the i-th current output part Ai among the (n+1)-numbers of current output parts A0 - An, the current output terminal IOUTA is connected to the i-th output terminal OUTi, and the current output terminal IOUTB is connected to the (i+1)-th output terminal OUT(i+1). However, the current output terminal IOUTA of the first current output part A0 and the current output terminal IOUTB of the (n+1)-th current output part An are not connected to the outside.

[50] It is not necessary for the first current output part A0 to have the current output switch So1 and the current output terminal T1, and for the (n+1)-th current output part An to have the current output switch So2 and the current output terminal T2.

[51] There are one more numbers (n+1) of current output parts prepared for the n-numbers of the output terminals in this case. However, it is also possible to prepare two current

output parts for a single output terminal, so that one of the output parts can be used as the current output and the other as the calibration. This makes it possible to supply the output current to the current output terminal at all times. Further, in a case where it is not necessary for all the output terminals to be in the current output state, the number of current output parts may be smaller than the number of output terminals.

[52] The current-voltage converting transistor QPx functions as a current-voltage converting part. Upon receiving the electric current from the reference current source I1, the current-voltage converting transistor QPx generates, at the node N1, a gate voltage (first voltage) for allowing the electric current that is equivalent to the reference current of the reference current source to flow therethrough. The reference current supply transistors QP1 and QP2 whose gate terminals are connected to the node N11 supply the electric current proportional to the reference current of the reference current source I1 to the IREF terminals of the current output parts A0 - An and the current-voltage converting transistor QNx, respectively.

[53] The current-voltage converting transistor QNx receives the electric current that is proportional to the current value of the reference current source I1 from the reference current supply transistor QP2. Like the current-voltage converting transistor QPx, the current-voltage converting transistor QNx itself generates, at the node N12, a gate voltage for allowing the electric current supplied from the reference current supply transistor QP2 to flow therethrough.

- [54] Preferably, the current-voltage converting transistor QNx is constituted in such a manner that all the Nch transistors QN1 - QNm shown in FIG. 1A are connected in parallel. Further, when the values of the electric currents supplied from the reference current supply transistors QP1 and QP2 have different values, the current-voltage converting capacity of the current-voltage converting transistor QNx may be set in accordance with a ratio of the current values supplied from the reference current supply transistors QP1 and QP2. That is, if the current value supplied from the reference current supply transistor QP2 is three times as large as the current value supplied from the reference current supply transistor QP1, three current-voltage converting transistors QNx, in each of which all the Nch transistors QN1 - QNm within the current output part A are connected in parallel, are prepared. Through this, it is possible to generate, at the node N2, the voltage that is extremely close to the voltage that is generated at the gates of the Nch transistors QN1 - QNm by the current output part A under the current supply mode M2.
- [55] The voltage supply source V1 supplies the voltage that is generated at the node N12 by the current-voltage converting transistor QNx in the manner described above to the VREF terminals of the current output parts A0 - An.
- [56] Considering a case of applying the current driving device according to the embodiment to an actual display panel, if there are 160 pixels in one line, the number of output terminals becomes 160 ($n = 160$). Thus, 161 current output parts A are required. In a case of RGB colors, there are required three times as many as the number of the current output parts A0

- An and the number of the signal input circuits Din. Furthermore, when the reference current is controlled individually for RGB, three sets of the reference current supply transistor QP1 and the voltage supply source V1 are required among the components of the current driving device shown in FIG. 3. The action control circuit B may be used in common or may be provided individually.

[57] <Calibration Mode Mc>

The calibration mode Mc of the current driving device shown in FIG. 3 will be described.

[58] The action control circuit B sets one of the current output parts A0 - An to be under the calibration mode Mc. That is, the mode thereof is shifted from the voltage supply mode M1 to the current supply mode M2, and the other current output parts are set to be under the current output mode M3.

[59] First, the current output part A0 is set to be under the voltage supply mode M1. Each of the current output parts A1 - An is set under such a condition that the electric current is outputted from the current output terminal IOUTA to the output terminals OUT1 - OUTn. Then, the current output part A0 is set to be under the current supply mode M2. No change is applied to the settings of the actions of the current output parts A1 - An. Through the above, calibration of the current output part A0 is performed.

[60] Next, the current output part A0 has the current output terminal IOUTB connected to the output terminal OUT1 to set the current output mode M3. No change is applied to the connections of the current output parts A2 - An and the output terminals OUT2 - OUTn. In this state, the current output part

A1 is shifted from the voltage supply mode M1 to the current supply mode M2 to perform calibration.

[61] In the same manner, the current output terminal IOUTA of the current output part before the calibration or the current output terminal IOUTB of the current output part after the calibration is connected to the output terminal so as to perform calibration successively for each of the current output parts.

[62] <Current Output Mode M3>

Next, the current output mode M3 of the current driving device shown in FIG. 3 will be described.

[63] The n-numbers of current output parts A that are not set under the calibration mode Mc are set under the current output mode M3, and receive display data signals from the signal input circuit Din according to the output terminals to which each of the current output parts A is connected. The current output part A set under the current output mode M3 outputs a sink current in accordance with the reference current and the aforementioned display data.

[64] <Refresh>

In a case where the calibration is performed only once, the reference voltage held in the voltage holding capacitance elements C1 is fluctuated due to leaks in the voltage holding capacitance elements C1 and in the gates of the Nch transistors QN1 - QNm within the current output parts A0 - An. Thus, it is necessary to perform calibration for the current output parts periodically. Therefore, the embodiment provides (n+1)-numbers of current output parts A0 - An for the n-numbers of output terminals OUT1 - OUTn, and performs calibration on

the current output part that is not in the mode of outputting the electric current.

[65] The voltage close to the target voltage is being maintained after performing the calibration once on all the current output parts A0 - An, except right after the startup or right after a change in the reference current. Thus, calibration under the voltage supply mode M1 may be omitted.

[66] <Collective Voltage Supply Mode M1'>

In a case where only the periodic calibration described above and a refresh action are performed, it is not possible to obtain a perfect output unless the necessary voltages are held at the nodes N2 of each current output part, when it is right after the startup of the current driving device or there is a change in the reference current. Thus, non-uniformity is generated in a panel display. Therefore, there is provided an operation mode where the voltage supply source V1 collectively supplies a voltage to be generated by the current-voltage converting transistor QNx to the nodes N2 of all the current output parts A0 - An at the time of the startup or changing the reference current. Through this, it becomes possible to store a current value that is close to a reference current that is set anew to all the current output parts A0 - An, so that the non-uniformity in the display caused due to the successive calibration can be improved.

[67] <Resetting of Reference Voltage>

As described above, each current output part is capable of provisionally holding the current value that is close to a new reference current because of the voltage supply source V1. However, the node N12 for supplying this voltage is

charged by a source current from the reference current supply transistor QP2. The current-voltage converting transistor QNx is merely a load for the reference current supply QP2 that supplies the source current. Thus, especially when the reset reference current is very small, it is difficult for the voltages (?) to be converged to a low voltage. Therefore, it is desirable that a reset switch Sw4 is deposited to provide a function of short-circuiting the node N12 to a ground potential.

[68] In the above-described embodiment, the reset switch Sw4 is connected between the ground potential and the current-voltage converting transistor QNx. However, by generating a lowest potential estimated as the potential of the current-voltage converting transistor QNx and connecting the reset switch Sw4 between the node of the generated potential and the current-voltage converting transistor QNx, the potential of the current-voltage converting transistor QNx can be reset still faster.

[69] There is a large difference in the load from the viewpoint of the voltage supply source V1 between the case of performing the processing of the voltage supply mode M1 with the periodic calibration and the case of performing the processing of the collective voltage supply mode M1' described in this section. If the voltage supply capacity corresponding to the n-numbers of loads is used for charging a single current output part A, a voltage waveform of the voltage supply line is distorted, and problems such as EMI (electromagnetic interference) may be induced. Inversely, the voltage supply capacity corresponding to a single current output part is insufficient

for supplying the voltage for all the current output parts. As a countermeasure for such problems, the voltage supply capacity of the voltage supply part may be varied in accordance with the extent of the capacitance to be charged.

[70] As an example, there is such a type that the number of output-stage transistors within the voltage supply source V1 is varied in accordance with each of the operation modes described above. FIG. 4 shows an example of such case. The voltage supply source V1 is constituted with: a differential amplifier Ad; Nch transistors QN21, QN22; Pch transistors QP21, QP22; and switches Sw5, Sw6, Sw7, and Sw8. The differential amplifier Ad receives, at its inverting input terminal, a reference voltage generated by a current-voltage converting transistor QNx. The output terminal of the voltage supply source V1 is connected to a non-inverting input terminal thereof, so that the voltage supply source V1 as a whole constitutes a voltage follower. Further, current output parts A0 - An are connected to the output terminal of the power supply source V1. Gates of the Nch transistors QN21 and QN22 are connected to the output terminal of the differential amplifier Ad, sources thereof are connected to a ground terminal, and drains thereof are connected to the output terminal of the voltage supply source V1 via the switches Sw5 and Sw6, respectively. A proper bias voltage is applied to gates of the Pch transistors QP21, QP22 from the outside, sources thereof are connected to a supply potential, and drains thereof are connected to the output terminal via the switches Sw7 and Sw8, respectively. When setting only one of the current output parts (for example, the current output part

A0) to be under the voltage supply mode M1, the switches Sw5, Sw7 are set to be in a conductive state and the switches Sw6, Sw8 are set to be in a nonconductive state so as to provide the optimum state for having only the voltage holding part (the voltage holding capacitance element C1 of FIG. 1) of the current output part A0 as a load. When setting all the current output parts A0 - An to be under the voltage supply mode M1, all the switches Sw5, Sw6, Sw7, and Sw8 are set to be in a conductive state to increase the voltage supply capacity so as to be able to charge the voltage holding capacitance elements C1 provided to all the current output parts. Through this, the voltage supply source V1 can supply the voltage with a proper voltage supply capacity in accordance with the load.

[71] FIG. 5 is a circuit diagram for showing a structure of a current driving device according to another embodiment of the present invention. In this embodiment, a second voltage supply part having a different voltage supply capacity is provided for each of the operation modes, i.e. the periodic voltage supply mode M1 and the collective voltage supply mode M1'. That is, in addition to the voltage supply source V1 as the first voltage supply part that has a proper voltage supply capacity for a single load of the current output part, the embodiment comprises a voltage supply source V2 as the second voltage supply part that has a proper voltage supply capacity for all the connected current output parts as the loads. Control signals are inputted to the voltage supply sources V1 and V2 from an action control circuit B. Each of the voltage supply sources V1 and V2 has a node N12 exhibiting a first voltage as the input, and is switch-controlled depending upon

whether the mode is set as the voltage supply mode M1 for a single current output part or the collective voltage supply mode M1'. Furthermore, by providing an overlapped period when switching the actions of both voltage supply sources, it is possible to suppress a large fluctuation in the output waveform right after switching the modes.

[72] <Effects>

Through the above-described structures, in the current driving device that performs calibration of the current output parts through supplying a reference current, it becomes possible to speed up the calibration action by supplying a voltage that is close to the final target value before the calibration executed by using the reference current. This makes it possible to deal with a case where the reference current is very small and a case where the number of outputs of the current driving device is increased in accordance with an increase in the scale of panel.

[73] In FIG. 1A, the output current of the current output part is a sink current and Nch transistors are used as the structural elements. In a case where the output current is a source current, however, Pch transistors may be used instead.

[74] While the invention has been described and illustrated in detail, it is to be clearly understood that this is intended be way of illustration and example only and is not to be taken by way of limitation, the spirit and scope of this invention being limited only be terms of the following claims.

WHAT IS CLAIMED IS:

1. A current driving device, comprising:
 - a first voltage supply part for supplying a first voltage;
 - a first current supply part for supplying a first electric current;
 - a plurality of output terminals; and
 - a plurality of current output parts for outputting an electric current in accordance with said first electric current, each of said current output parts comprising a current-voltage converting function, a voltage-current converting function, a voltage holding part, and at least one current output terminal, wherein
 - said current output part takes three operation modes, i.e. a voltage supply mode, a current supply mode, and a current output mode,
 - under said voltage supply mode, said current output part receives said first voltage from said first voltage supply part and holds said voltage in said voltage holding part,
 - under said current supply mode, said current output part receives said first current from said first current supply part, and generates a second voltage by said current-voltage converting function and holds said voltage in said voltage holding part, and
 - under said current output mode, said current output part outputs an output current according to said voltage held in said voltage holding part by said voltage-current converting function.

2. The current driving device according to claim 1, wherein each of said output terminals is connected to said current output terminals provided to said plurality of said current output parts, and each of said plurality of current output parts is connected in parallel to said first current supply part and said first voltage supply part used in common.

3. The current driving device according to claim 1, wherein each of said current output parts actuates said current-voltage converting function under said voltage supply mode.

4. The current driving device according to claim 1, wherein each of said current output parts comprises a function of stopping said current-voltage converting function under said voltage supply mode.

5. The current driving device according to claims 1, further comprising

a second current supply part for supplying a second electric current that is proportional to said first electric current, and

a current-voltage converting part for generating said first voltage by receiving said second electric current, wherein

said first voltage supply part controls supplies of said first voltage generated by said current-voltage converting part to said current output parts.

6. The current driving device according to claim 5, wherein said current-voltage converting part comprises a switching part for short-circuiting a node at which said first voltage emerges to a reference voltage node.

7. The current driving device according to claims 1, further comprising a second voltage supply part with a larger voltage supply capacity than that of said first voltage supply part, wherein

the use of said first voltage supply part and the use of said second voltage supply part are switched in accordance with the number of said current output parts that take said voltage supply mode among said plurality of current output parts.

8. The current driving device according to claims 1, wherein

said first voltage supply part is constituted to be capable of changing its voltage supply capacity in accordance with the number of said current output parts that take said voltage supply mode among said plurality of current output parts.

9. A current-driving-type display device, comprising said current driving device according to claims 1 mounted thereon so as to be driven by said current driving device.

10. A current driving device, comprising:

a current input switch for controlling connection/

disconnection states with respect to a current supply part;

a voltage holding part for holding a reference voltage, which is charged by a flown current;

a calibration switch interposed between said current input switch and said voltage holding part;

a plurality of voltage-current converting elements for generating an electric current in accordance with said reference voltage held in said voltage holding part;

a plurality of signal response switches that are on/off controlled in accordance with inputted signals, said response switches being connected in series to each of said voltage-current converting elements, and each of which being connected in parallel to said calibration switch;

a plurality of current output switches, each being interposed between a connection node, which is provided between said current input switch and said calibration switch, and said plurality of current output terminals; and

a high-speeding switch for controlling connection/disconnection states of said voltage supply part with respect to said voltage holding part.

ABSTRACT OF THE DISCLOSURE

A current driving device comprises: a voltage supply part; a current supply part; and a plurality of current output parts, each comprising a current-voltage converting function, a voltage-current converting function, and a voltage holding capacitance element. The current output part takes three operation modes. Under a voltage supply mode, the current output part receives a voltage from the voltage supply part and holds the voltage in the voltage holding capacitance element. Under a current supply mode, the current output part receives the current from the current supply part, generates a second voltage by the current-voltage converting function and holds the voltage in the voltage holding capacitance element. Under a current output part, the current output part outputs an output current according to the voltage held in the voltage holding capacitance element by the voltage-current converting function. By charging the current output part with the reference voltage before the calibration performed by using the reference current, calibration of the current output part is performed at a high speed.

FIG. 1A

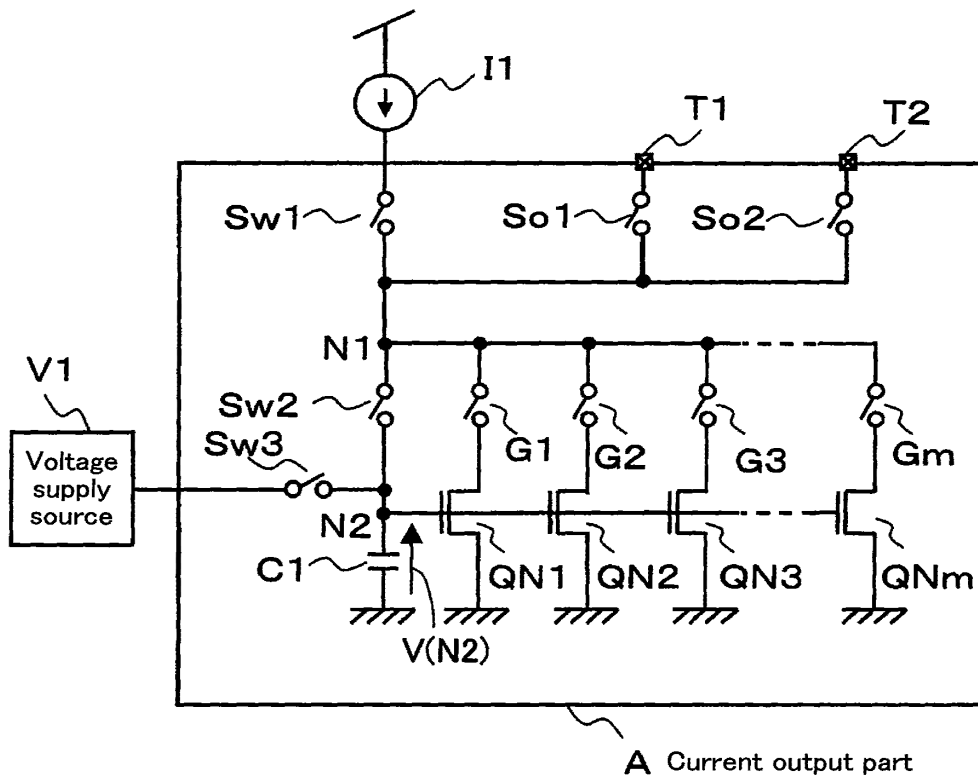


FIG. 1B

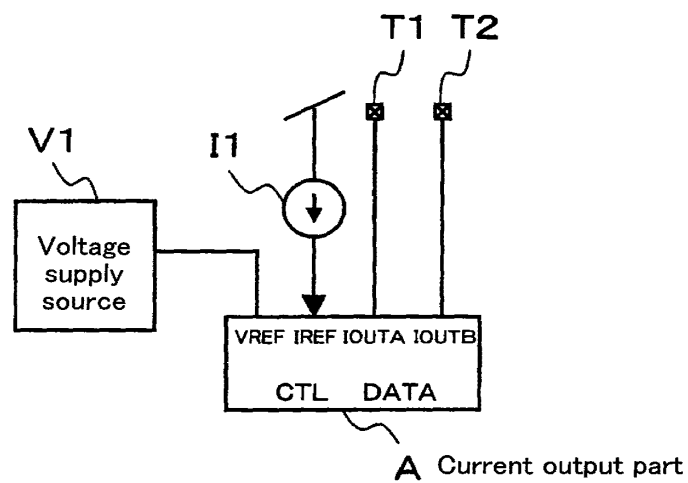
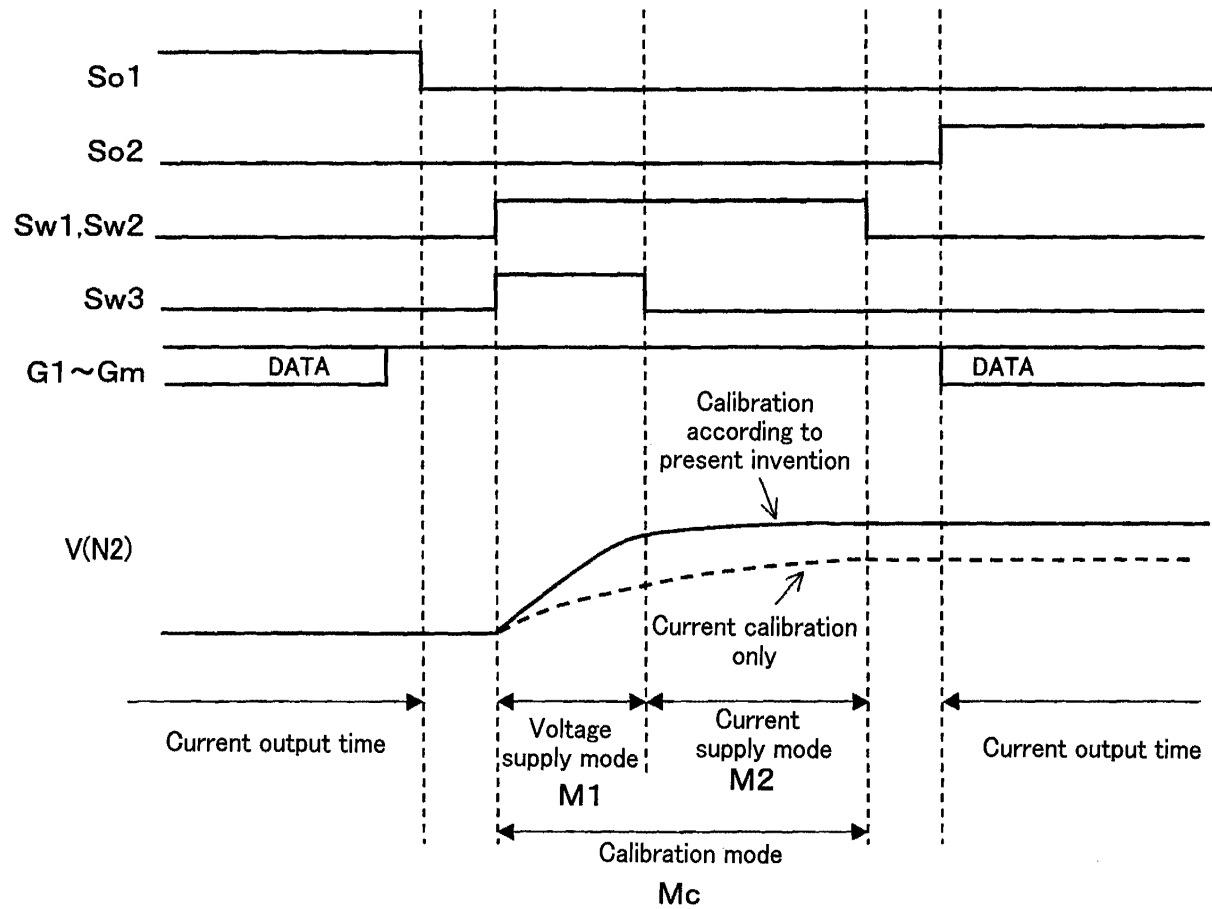


FIG. 2



F I G. 3

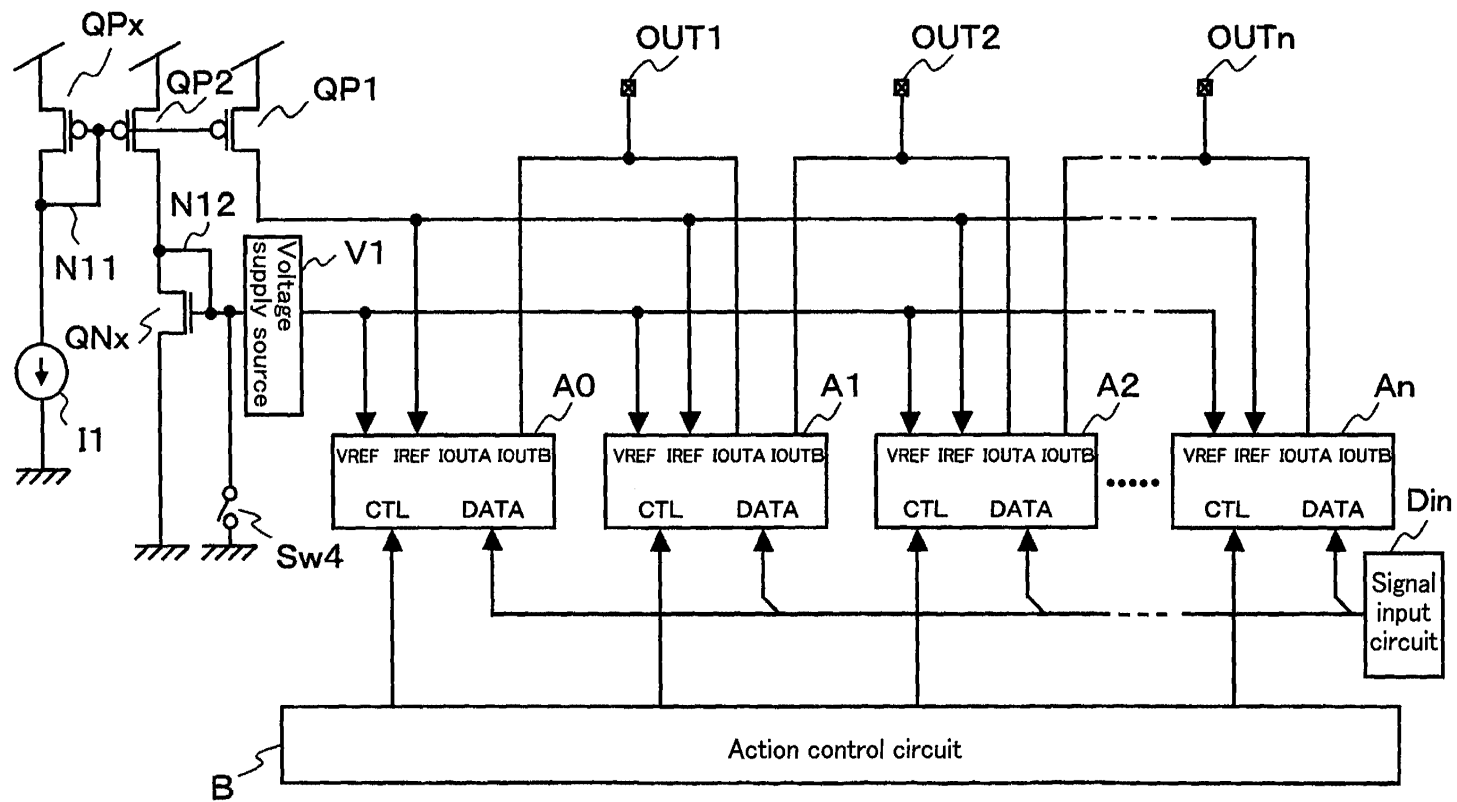


FIG. 5

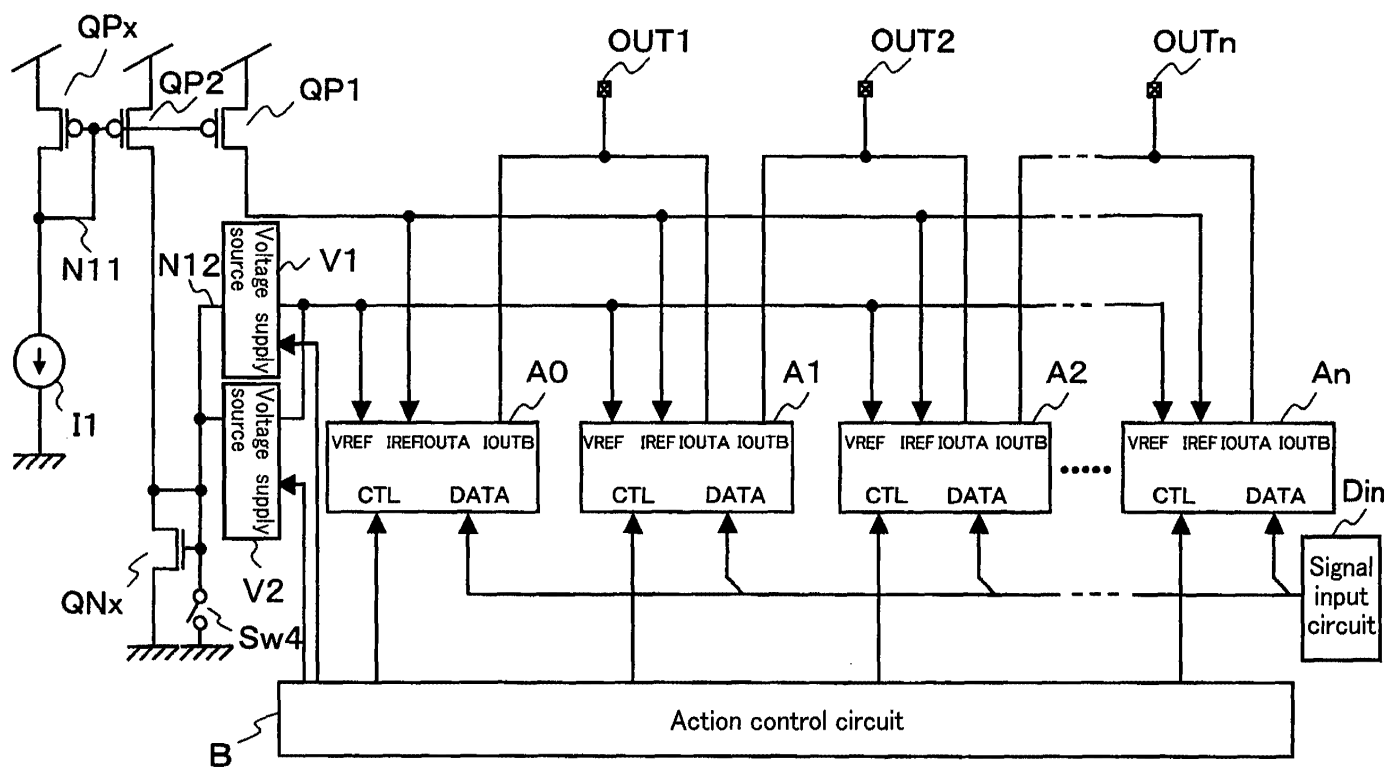


FIG. 6A

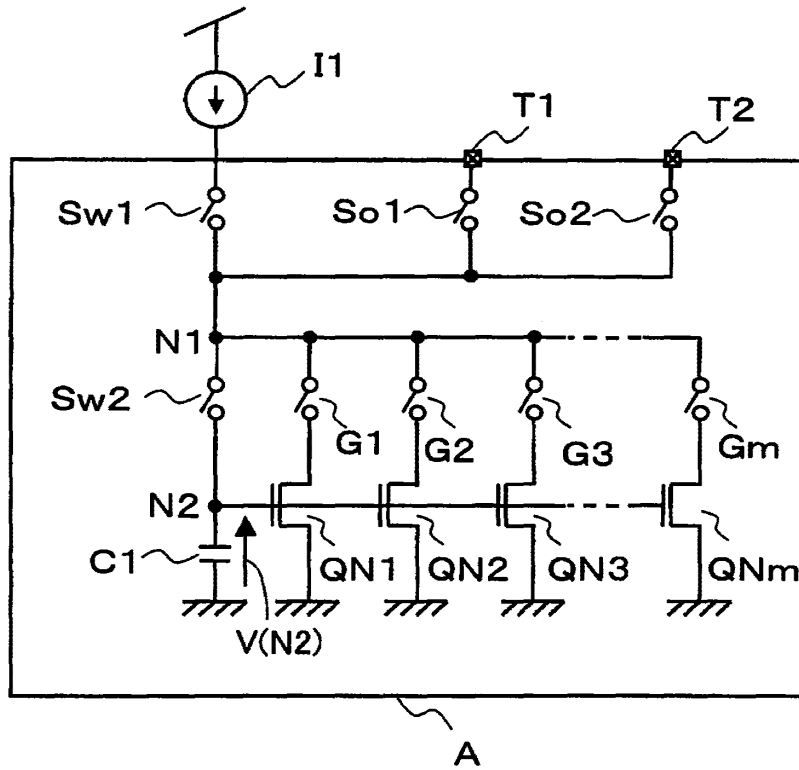


FIG. 6B

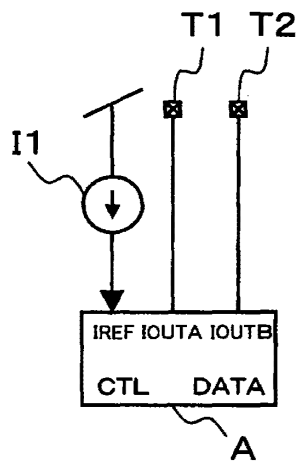


FIG. 7

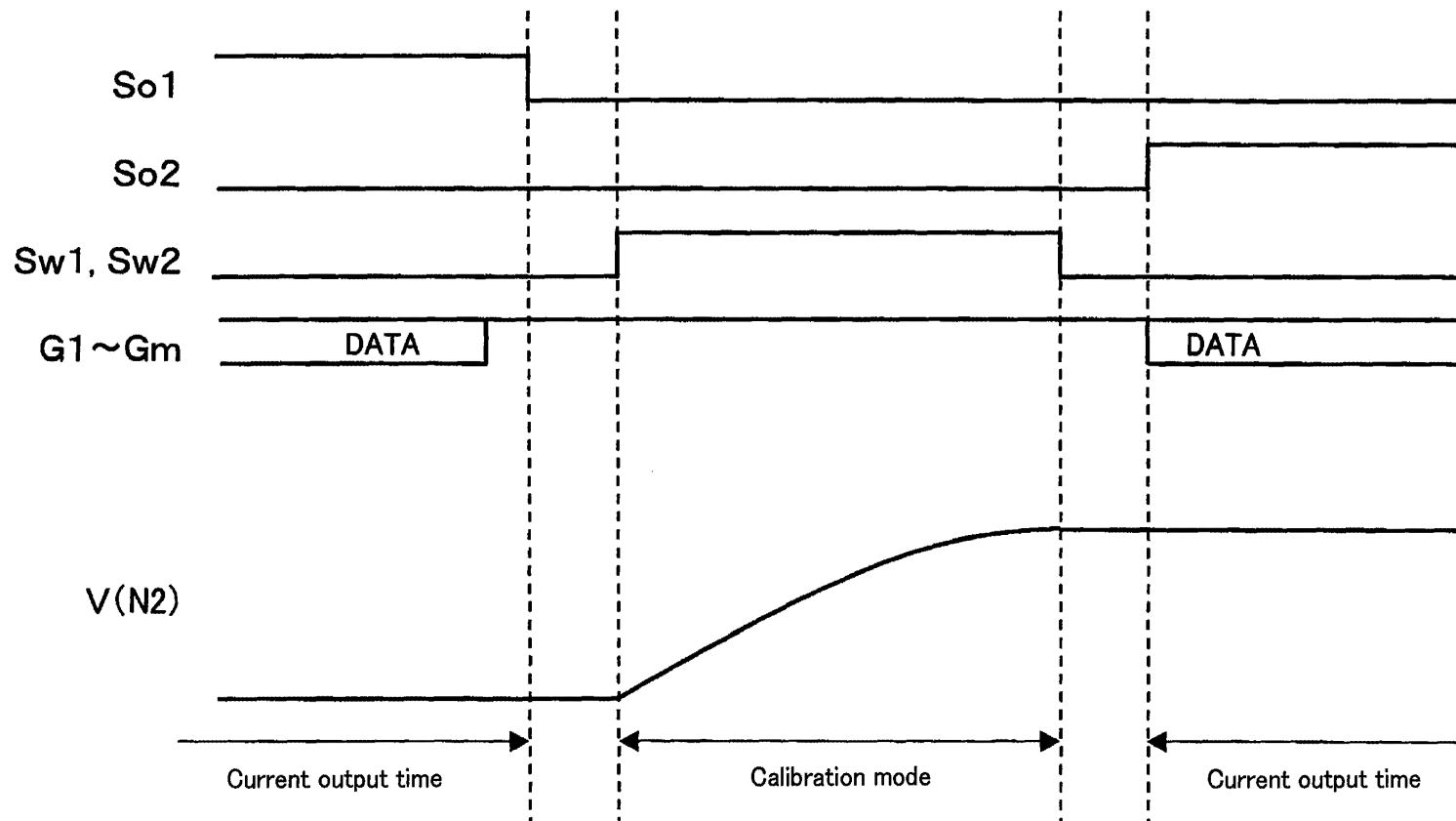


FIG. 8

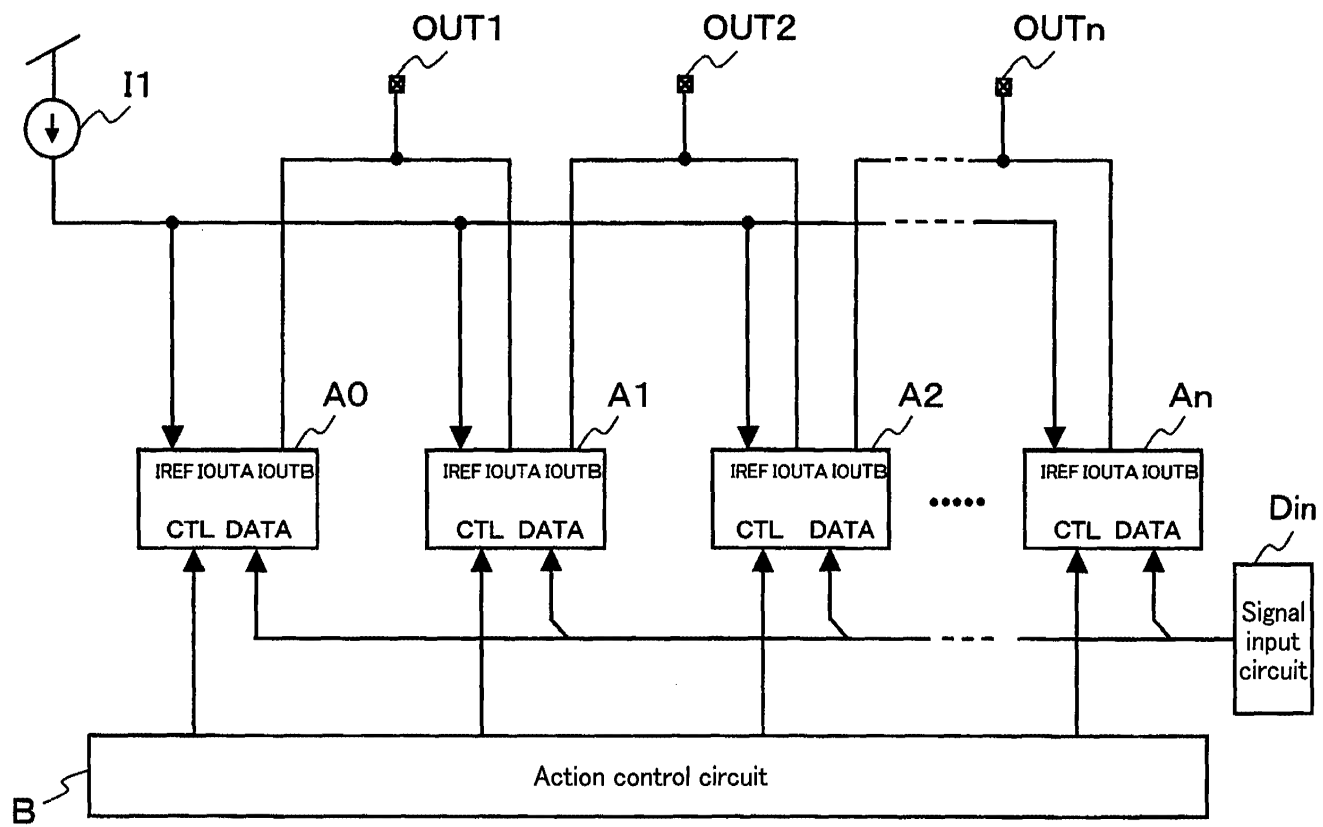
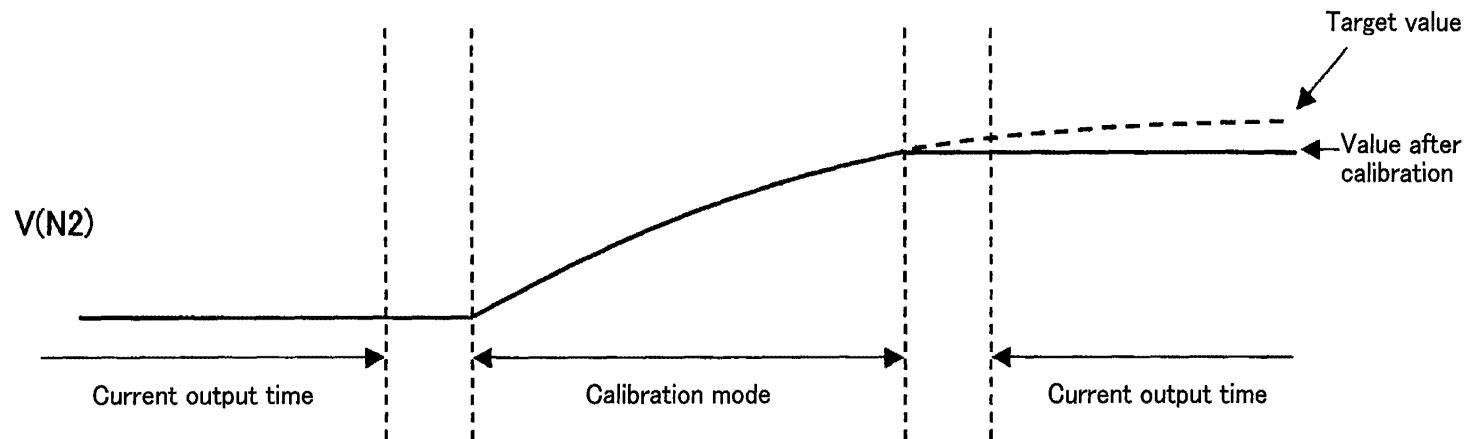


FIG. 9



Matsushita Ref*: P048138-01
 (* must be filled)
 Japan Firm Name: Okada Patent Office
 US Firm Name: MWE

Application Serial No. _____
 Japan Firm Ref: USA 07-52P
 US Firm Ref: _____

DECLARATION AND POWER OF ATTORNEY FOR U.S. PATENT APPLICATION

(a) ☒ Original (b) ☐ Supplemental (c) ☐ Substitute (d) ☐ PCT (e) ☐ Design

As a below named inventor, I hereby declare that: my residence, post office address and citizenship are as stated below next to my name; and I believe that I am the original, first and sole inventor (if only one name is listed below) or an original, first and joint inventor (if plural inventors are named below) of the subject matter which is claimed and for which a patent is sought on the invention entitled:

Title of Invention:

CURRENT DRIVING DEVICE

which is described and claimed in (if the following box is not checked, the specification of which is attached hereto):

1. For use when submitting this Declaration prior to U.S. application filing date			
(f) <input checked="" type="checkbox"/> the attached specification, or			
2. For use when submitting this Declaration after U.S. application filing date			
(g) <input type="checkbox"/> the specification in the U.S. Application:	Application No. (if available)	filed on: (must be filled)	
	and with amendments (if applicable):		filed on _____, or
3. For PCT-US national entry under 35 U.S.C. 371 (for use when filing this Declaration before and after the U.S. national entry date)			
(h) <input type="checkbox"/> the specification in the International Application: (Check here only for US national entry under 35 U.S.C. 371.)	PCT Application No.	filed on: (PCT filing date)	
	and with amendments (if applicable):		filed on _____

I hereby state that I have reviewed and understand the contents of the above-identified specification, including the claims, as amended by any amendment(s) referred to above.

I acknowledge my duty to disclose to the U.S. Patent and Trademark Office all information known to me to be material to patentability as defined in Title 37, Code of Federal Regulations, §1.56.

I hereby claim foreign priority benefits under Title 35, United States Code, §119 (a-d), §172, or §365(b) of any foreign application(s) for patent or inventor's certificate, or §365(a) of any PCT international application which designated at least one country other than the United States of America, listed below, and have also identified below any foreign application for patent or inventor's certificate, or of any PCT international application having a filing date before that of the application on which priority is claimed:

(Foreign Priority Information)

COUNTRY	APPLICATION NO.	DATE OF FILING	PRIORITY CLAIMED
Japan	2006-335850	December 13 2006	Yes

☐ Additional foreign or international application numbers are listed on a supplemental priority sheet attached hereto.

I hereby claim the benefit under Title 35, United States Code §119(e) of any United States Provisional application(s) listed below.

(US Provisional Application Information)

APPLICATION NO.	U.S. PROVISIONAL APPLICATION FILING DATE

☐ Additional U.S. provisional application numbers are listed on a supplemental priority sheet attached hereto.

I hereby claim the benefit under Title 35, United States Code §120 of any United States application(s), or §365(C) of any PCT international application designating the United States of America, listed below and, insofar as the subject matter of each of the claims of this application is not disclosed in the prior United States or PCT international application in the manner provided by the first paragraph of Title 35, United States Code §112, I acknowledge the duty to disclose information material to patentability as defined in Title 37, Code of Federal Regulations, §1.56 which occurred between the filing date of the prior application and the national or PCT international filing date of this application.

(Domestic Priority Information)

APPLICATION NO.	U.S. FILING DATE	STATUS: PATENTED, PENDING, ABANDONED

☐ Additional U.S. or international application numbers are listed on a supplemental priority sheet attached hereto.

POWER OF ATTORNEY: As a named inventor, I hereby appoint the attorneys and agents associated with U.S. Patent and Trademark Office Customer Number identified below to prosecute this application and to transact all business in the U.S. Patent and Trademark Office connected therewith, and direct that all correspondence be addressed to that customer number.

I hereby authorize the U.S. attorneys and agents associated with the customer number to accept and follow instructions from Matsushita Electric Industrial Co., Ltd., and any affiliated or subsidiary company thereof, received via their corporate representatives and/or their foreign patent attorneys or agents, if any, as to any action to be taken in the U.S. Patent and Trademark Office regarding this application without direct communication between the U.S. attorneys or agents and myself.

Direct Correspondence to:

CUSTOMER NUMBER 53080

I further declare that all statements made herein of my own knowledge are true, and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code, and that such willful false statements may jeopardize the validity of the application or any patent issuing thereon.

INVENTOR (s)

Full Name of Sole or First Inventor	FIRST NAME Makoto	LAST NAME MIZUKI	SIGNATURE <i>Makoto Mizuki</i>	DATE OF SIGNATURE November 29, 2007
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Post office address	ADDRESS c/o Matsushita Electric Industrial Co., Ltd. 1006, Oaza Kadoma, Kadoma-shi, Osaka 571-8501 Japan			

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Full Name of Fourth Inventor	FIRST NAME Tomokazu	LAST NAME KOJIMA	SIGNATURE <i>Tomokazu Kojima</i>	DATE OF SIGNATURE November 29, 2007
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Post office address	ADDRESS c/o Panasonic Semiconductor Systems and Technology Co., Ltd. 1006, Oaza Kadoma, Kadoma-shi, Osaka 571-8501 Japan			

Full Name of Fifth Inventor	FIRST NAME Hiroshi	LAST NAME KOJIMA	SIGNATURE <i>Hiroshi Kojima</i>	DATE OF SIGNATURE November 29, 2007
Residence & Citizenship	CITY, STATE or COUNTRY Kyoto, JAPAN			CITIZENSHIP JAPAN
Post office address	ADDRESS c/o Panasonic Semiconductor Systems and Technology Co., Ltd. 1006, Oaza Kadoma, Kadoma-shi, Osaka 571-8501 Japan			

INFORMATION DISCLOSURE STATEMENT BY APPLICANT (Substitute for form 1449/PTO)				ATTY. DOCKET NO. 056937-0414		SERIAL NO. Not Yet Assigned	
				APPLICANT Makoto MIZUKI, et al.			
				FILING DATE December 12, 2007		GROUP Not Yet Assigned	
U.S. PATENT DOCUMENTS							
EXAMINER'S INITIALS	CITE NO.	Document Number Number-Kind Code ₂ (if known)	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear		
		US 2005/0231241 A1	10-20-2005	Date, et al.	Corresponds w/ JP 2005-311591		
		US 2004/0251844 A1	12-16-2004	Hashido et al.			
		US 7,050,024 B2	05-23-2006	LeChevalier			
		US 6,594,606 B2	07-15-2003	Everitt			
		US 2006/0158402 A1	07-20-2006	Nathan et al.			
FOREIGN PATENT DOCUMENTS							
EXAMINER'S INITIALS	CITE NO.	Foreign Patent Document Country Code ₃ -Number 4 -Kind Codes (if known)	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines Where Relevant Figures Appear	Translation Yes No	
		JP 2005-311591	11-04-2005	MATSUSHITA ELECTRIC IND CO LTD	Corresponds w/ US 2005/0231241 A1	English Abstract	
		JP 2004-219955	08-05-2004	TOSHIBA MATSUSHITA DISPLAY TECHNOLOGY CO LTD		English Abstract	
		JP 2005-121843	05-12-2005	TOSHIBA MATSUSHITA DISPLAY TECHNOLOGY CO LTD		English Abstract	
OTHER ART (Including Author, Title, Date, Pertinent Pages, Etc.)							
EXAMINER'S INITIALS	CITE NO.	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.					
EXAMINER				DATE CONSIDERED			

*EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.

1 Applicant's unique citation designation number (optional). 2 Applicant is to place a check mark here if English language Translation is attached.

PATENT ABSTRACTS OF JAPAN

(11)Publication number : 2005-311591

(43)Date of publication of application : 04.11.2005

(51)Int.Cl. H03K 17/00
G09G 3/20
G09G 3/30
H03K 5/00

(21)Application number : 2004-124306 (71)Applicant : MATSUSHITA ELECTRIC IND CO LTD

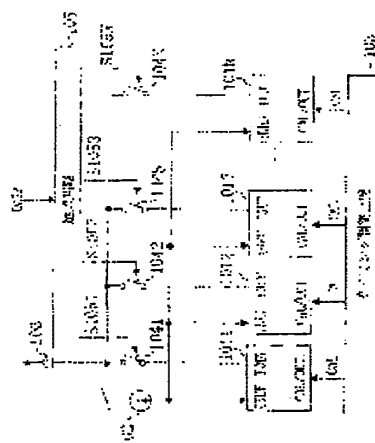
(22)Date of filing : 20.04.2004 (72)Inventor : DATE YOSHITO
MATSUZAWA AKIRA

(54) CURRENT DRIVER

(57)Abstract:

PROBLEM TO BE SOLVED: To provide a current driver for improving unevenness of output current.

SOLUTION: A timing control circuit 103 switches operation mode in current copy circuits 1011-101N. The current copy circuits 1011-101N store a reference current from a reference current source 102 in storage mode, and output the stored current to corresponding switches 1041-104N in output mode. A select circuit 105 turns the switches 1041-104N on/off depending on inputted display data DATA. A signal output terminal 106 sums currents being inputted from the current copy circuits 1011-101N through the switches 1041-104N and delivers the summed current as an output current.



PATENT ABSTRACTS OF JAPAN

(11)Publication number : 2004-219955

(43)Date of publication of application : 05.08.2004

(51)Int.Cl. G09G 3/30
G09G 3/20(21)Application number : 2003-010267 (71)Applicant : TOSHIBA MATSUSHITA DISPLAY
TECHNOLOGY CO LTD

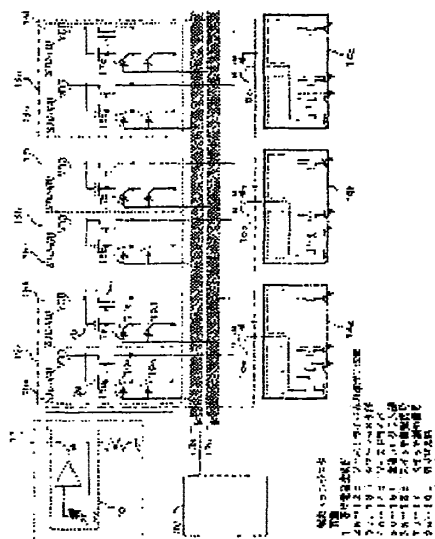
(22)Date of filing : 17.01.2003 (72)Inventor : TSUGE HITOSHI

(54) ELECTRIC CURRENT DRIVING APPARATUS AND ELECTRIC CURRENT DRIVING METHOD

(57)Abstract:

PROBLEM TO BE SOLVED: To reduce variation of output currents between driving apparatuses due to the variation of current values inputted into a reference current source in a driving apparatus in which the output current is determined by the current value of the reference current source.

SOLUTION: The current driving apparatus is provided with current program sections 15a to 15f which hold prescribed current value by a current copier system on the basis of input of identical reference current and output driving current of the prescribed current value, a control means 100 which controls whether input of the reference current is performed or output of the driving current to any external of N series is performed, shift registers 13a, 13b, and selectors 18a to 18c.



PATENT ABSTRACTS OF JAPAN

(11)Publication number : 2005-121843

(43)Date of publication of application : 12.05.2005

(51)Int.Cl. G09G 3/30
G09G 3/20
H03F 3/343
H05B 33/14

(21)Application number : 2003-355621

(71)Applicant : TOSHIBA MATSUSHITA DISPLAY
TECHNOLOGY CO LTD

(22)Date of filing : 15.10.2003

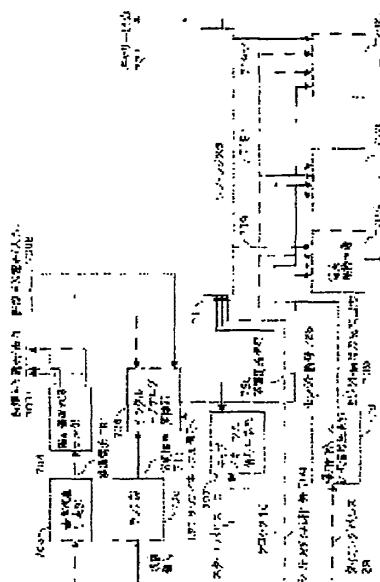
(72)Inventor : TSUGE HITOSHI

(54) CURRENT OUTPUT TYPE SEMICONDUCTOR CIRCUIT

(57)Abstract:

PROBLEM TO BE SOLVED: To solve the problem that an output current fluctuates due to the property variation of transistors when the reference current (current per one gradation) is distributed to respective outputs in a current output type semiconductor circuit performing current output to be used for a display device such as an organic electroluminescent element wherein a gray shade display is performed according to the amount of a current.

SOLUTION: The current output type semiconductor circuit comprises: a reference current generating part 703 for setting the current value per gradation; a gradation reference current generating part 704 for supplying the current corresponding to each gradation; a digital/analog converting part 706 for converting a video signal into current amount corresponding to the gradation; a chip enable signal generating part 707 for controlling whether the digital/analog converting part is to be operated or not; a shift register 21 for distributing the current corresponding to the video signal to each output; and current holding means 702a-702c for holding the distributed current for one horizontal scanning period. The current holding means comprises two current copier circuits.



Electronic Patent Application Fee Transmittal				
Application Number:				
Filing Date:				
Title of Invention:		CURRENT DRIVING DEVICE		
First Named Inventor/Applicant Name:		Makoto MIZUKI		
Filer:		Michael E. Fogarty/Lydia Nguyen		
Attorney Docket Number:		056937-0414		
Filed as Large Entity				
Utility Filing Fees				
Description	Fee Code	Quantity	Amount	Sub-Total in USD(\$)
Basic Filing:				
Utility application filing	1011	1	310	310
Utility Search Fee	1111	1	510	510
Utility Examination Fee	1311	1	210	210
Pages:				
Claims:				
Miscellaneous-Filing:				
Petition:				
Patent-Appeals-and-Interference:				

Description	Fee Code	Quantity	Amount	Sub-Total in USD(\$)
Post-Allowance-and-Post-Issuance:				
Extension-of-Time:				
Miscellaneous:				
Total in USD (\$)				1030

Electronic Acknowledgement Receipt	
EFS ID:	2579024
Application Number:	11954659
International Application Number:	
Confirmation Number:	4296
Title of Invention:	CURRENT DRIVING DEVICE
First Named Inventor/Applicant Name:	Makoto MIZUKI
Customer Number:	53080
Filer:	Michael E. Fogarty/Lydia Nguyen
Filer Authorized By:	Michael E. Fogarty
Attorney Docket Number:	056937-0414
Receipt Date:	12-DEC-2007
Filing Date:	
Time Stamp:	14:05:53
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	yes
Payment Type	Deposit Account
Payment was successfully received in RAM	\$ 1030
RAM confirmation Number	6745
Deposit Account	500417
Authorized User	
The Director of the USPTO is hereby authorized to charge indicated fees and credit any overpayment as follows: Charge any Additional Fees required under 37 C.F.R. Section 1.16 (National application filing, search, and examination fees)	

File Listing:					
Document Number	Document Description	File Name	File Size(Bytes) /Message Digest	Multi Part /.zip	Pages (if appl.)
1	Transmittal of New Application	New_utility.pdf	56795	no	2
			00a85e0d95daa9d9fa0a6919d1345c6e3c9ac08a		
Warnings:					
Information:					
2		Specification.pdf	1451702	yes	38
			b190b3ea627adf9d09b59df04a593a3d3c545862		
	Multipart Description/PDF files in .zip description				
	Document Description		Start	End	
	Specification		1	33	
	Claims		34	37	
	Abstract		38	38	
Warnings:					
Information:					
3	Drawings-only black and white line drawings	Drawings.pdf	110410	no	9
			7de32ebd2ebce0a75593520dc08d110c663cd30		
Warnings:					
Information:					
4	Oath or Declaration filed	Declaration.pdf	156587	no	3
			4164edd60d7983cc92168c07ddb33fc411b691bc		
Warnings:					
Information:					
5	Request for USPTO to retrieve priority docs	CPD.pdf	171516	no	3
			7c644d0dd714ea02ffa3647a7bd1fb12fe2104b6		
Warnings:					
Information:					
6		IDS.pdf	83878	yes	3
			8c4469816eeb6bcc8a1cdc22a91b968e74e50ae1		
	Multipart Description/PDF files in .zip description				
	Document Description		Start	End	
	Information Disclosure Statement Letter		1	2	

	Information Disclosure Statement (IDS) Filed	3	3
Warnings:			
Information:			
7		Reference.pdf	<div>114547</div> <div>73d795140b54be90628b314afcb8ab8353ead252</div> <div>yes</div> <div>3</div>
	Multipart Description/PDF files in .zip description		
	Document Description	Start	End
	Foreign Reference	1	1
	Foreign Reference	2	2
	Foreign Reference	3	3
Warnings:			
Information:			
8	Fee Worksheet (PTO-06)	fee-info.pdf	<div>8350</div> <div>8bf74a6d7e91ace7203bac8b1340ff19b0be16d2</div> <div>no</div> <div>2</div>
Warnings:			
Information:			
Total Files Size (in bytes):		2153785	
<p>This Acknowledgement Receipt evidences receipt on the noted date by the USPTO of the indicated documents, characterized by the applicant, and including page counts, where applicable. It serves as evidence of receipt similar to a Post Card, as described in MPEP 503.</p> <p><u>New Applications Under 35 U.S.C. 111</u> If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application.</p> <p><u>National Stage of an International Application under 35 U.S.C. 371</u> If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.</p> <p><u>New International Application Filed with the USPTO as a Receiving Office</u> If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.</p>			

Docket No.: 056937-0414

PATENT

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of	:	Customer Number: 53080
	:	
Makoto MIZUKI, et al.	:	Confirmation Number: Not Yet Assigned
	:	
Application No.: Not Yet Assigned	:	Group Art Unit: Not Yet Assigned
	:	
Filed: December 12, 2007	:	Examiner: Not Yet Assigned
	:	
For: CURRENT DRIVING DEVICE	:	

CLAIM OF PRIORITY

Mail Stop New Applications
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Sir:

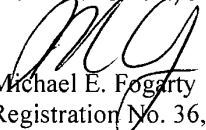
In accordance with the provisions of 35 U.S.C. 119, Applicants hereby claim the priority of:

Japanese Patent Application No. JP 2006-335850, filed on December 13, 2006

cited in the Declaration of the present application. A request to retrieve Electronic Priority
Application is being filed concurrently herewith.

Respectfully submitted,

McDERMOTT WILL & EMERY LLP


Michael E. Fogarty
Registration No. 36,139

600 13th Street, N.W.
Washington, DC 20005-3096
Phone: 202.756.8000 MEF:ln
Facsimile: 202.756.8087
Date: December 12, 2007

**Please recognize our Customer No. 53080 as
our correspondence address.**

**Request to Retrieve Electronic
Priority Application(s)**

Send completed form to: Commissioner for Patents
P.O. Box 1450, Alexandria, VA 22313-1450

COMPLETE IF KNOWN

Application Number	Not Yet Assigned
Filing Date	December 12, 2007
Art Unit	Not Yet Assigned
Examiner Name	Not Yet Assigned
Attorney Docket Number	056937-0414

The undersigned hereby requests the USPTO retrieve an electronic copy of each of the following foreign applications for which benefit has been claimed under 35 U.S.C. 119(a)-(d) from a foreign intellectual property office participating with the USPTO in a bilateral or multilateral priority document exchange agreement:

Please retrieve (check all that apply)

- ☒ The following applications originally filed in participating offices (only list the Participating Office and the Participating Office Application Number (columns 1 and 2 below)):
- ☐ The following applications originally filed in non-participating offices (must list the information for all three columns below):

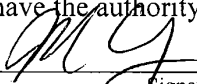
1. Participating Office with which the Priority Application, or the Copy, was filed (e.g., EPO)	2. Participating Office Application Number in which the Priority Application, or a Copy, was filed (e.g., 03101432)		3. Non-Participating Office Application Number (Priority Application), if applicable	
	App. No.	Filing Date	Office	App. No.
1. JPO	2006-335850	December 13, 2006		
2.				
3.				
4.				
5.				
6.				

This Request to Retrieve Electronic Priority Application(s) (Request) should be filed within the later of four months from the date of filing the above-identified application claiming foreign priority, or sixteen months from the filing date of the foreign application to which priority is claimed.

This Request should be submitted concurrently with the claim for priority, or thereafter. The USPTO will not attempt to retrieve the identified priority application(s) until applicant identifies the indicated priority application(s) on the oath or declaration or an application data sheet in compliance with 37 CFR 1.63(c).

Applicants are advised to consult Private PAIR (accessed through www.uspto.gov) to assure that the retrieval has been successful. The applicant remains ultimately responsible for the submission of the certified copy of the foreign application(s) within the period set forth in 37 CFR 1.55(a) (before the U.S. application issues as a patent) if the USPTO does not timely retrieve the identified priority application(s).

I hereby declare that I have the authority to grant access to the above-identified applications.



Signature

Michael E. Fogarty
Printed or Typed Name

Title

December 12, 2007

Date

202.756.8000

Telephone Number

36,139

Registration Number, if applicable

This collection of information is required by 37 CFR 1.55(d). The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process an application). Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.11 and 1.14. This collection is estimated to take 8 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.

If you need assistance in completing the form, call 1-800-PTO-9199 and select option 2.

Privacy Act Statement

The **Privacy Act of 1974 (P.L. 93-579)** requires that you be given certain information in connection with your submission of the attached form related to a patent application or patent. Accordingly, pursuant to the requirements of the Act, please be advised that: (1) the general authority for the collection of this information is 35 U.S.C. 2(b)(2); (2) furnishing of the information solicited is voluntary; and (3) the principal purpose for which the information is used by the U.S. Patent and Trademark Office is to process and/or examine your submission related to a patent application or patent. If you do not furnish the requested information, the U.S. Patent and Trademark Office may not be able to process and/or examine your submission, which may result in termination of proceedings or abandonment of the application or expiration of the patent.

The information provided by you in this form will be subject to the following routine uses:

1. The information on this form will be treated confidentially to the extent allowed under the Freedom of Information Act (5 U.S.C. 552) and the Privacy Act (5 U.S.C. 552a). Records from this system of records may be disclosed to the Department of Justice to determine whether disclosure of these records is required by the Freedom of Information Act.
2. A record from this system of records may be disclosed, as a routine use, in the course of presenting evidence to a court, magistrate, or administrative tribunal, including disclosures to opposing counsel in the course of settlement negotiations.
3. A record in this system of records may be disclosed, as a routine use, to a Member of Congress submitting a request involving an individual, to whom the record pertains, when the individual has requested assistance from the Member with respect to the subject matter of the record.
4. A record in this system of records may be disclosed, as a routine use, to a contractor of the Agency having need for the information in order to perform a contract. Recipients of information shall be required to comply with the requirements of the Privacy Act of 1974, as amended, pursuant to 5 U.S.C. 552a(m).
5. A record related to an International Application filed under the Patent Cooperation Treaty in this system of records may be disclosed, as a routine use, to the International Bureau of the World Intellectual Property Organization, pursuant to the Patent Cooperation Treaty.
6. A record in this system of records may be disclosed, as a routine use, to another federal agency for purposes of National Security review (35 U.S.C. 181) and for review pursuant to the Atomic Energy Act (42 U.S.C. 218(c)).
7. A record from this system of records may be disclosed, as a routine use, to the Administrator, General Services, or his/her designee, during an inspection of records conducted by GSA as part of that agency's responsibility to recommend improvements in records management practices and programs, under authority of 44 U.S.C. 2904 and 2906. Such disclosure shall be made in accordance with the GSA regulations governing inspection of records for this purpose, and any other relevant (i.e., GSA or Commerce) directive. Such disclosure shall not be used to make determinations about individuals.
8. A record from this system of records may be disclosed, as a routine use, to the public after either publication of the application pursuant to 35 U.S.C. 122(b) or issuance of a patent pursuant to 35 U.S.C. 151. Further, a record may be disclosed, subject to the limitations of 37 CFR 1.14, as a routine use, to the public if the record was filed in an application which became abandoned or in which the proceedings were terminated and which application is referenced by either a published application, an application open to public inspection or an issued patent.
9. A record from this system of records may be disclosed, as a routine use, to a Federal, State, or local law enforcement agency, if the USPTO becomes aware of a violation or potential violation of law or regulation.

Docket No.: 056937-0414

PATENT

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of	:	Customer Number: 53080
	:	
Makoto MIZUKI, et al.	:	Confirmation Number: Not Yet Assigned
	:	
Application No.: Not Yet Assigned	:	Group Art Unit: Not Yet Assigned
	:	
Filed: December 12, 2007	:	Examiner: Not Yet Assigned
	:	
For: CURRENT DRIVING DEVICE	:	

INFORMATION DISCLOSURE STATEMENT

Mail Stop Amendment
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Dear Sir:

In accordance with the provisions of 37 C.F.R. 1.56, 1.97 and 1.98, the attention of the Patent and Trademark Office is hereby directed to the documents listed on the attached form PTO-1449. It is respectfully requested that the documents be expressly considered during the prosecution of this application, and that the documents be made of record therein and appear among the "References Cited" on any patent to issue therefrom.

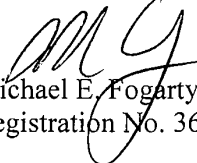
This Information Disclosure Statement is being filed within three months of the U.S. filing date OR before the mailing date of a first Office Action on the merits. No certification or fee is required.

The relevance of the references cited on the attached Form-1449, if any is discussed in the present specification.

Please charge any shortage in fees due in connection with the filing of this paper,
including extension of time fees, to Deposit Account 500417 and please credit any excess fees to
such deposit account.

Respectfully submitted,

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Date: December 12, 2007

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12/12/2007

Approved for use through 7/31/2006. OMB 0651-0032

U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE

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PATENT APPLICATION FEE DETERMINATION

Substitute for Form PTO-875

Application or Docket Number

11/954,659

APPLICATION AS FILED – PART I

(Column 1) (Column 2)

FOR		NUMBER EXTRA
BASIC FEE (37 CFR 1.16(a), (b), or (c))		
SEARCH FEE (37 CFR 1.16(k), (l), or (m))		
EXAMINATION FEE (37 CFR 1.16(o), (p), or (q))		
TOTAL CLAIMS (37 CFR 1.16(i))	10	*
INDEPENDENT CLAIMS (37 CFR 1.16(h))	2	minus 3 = *
APPLICATION SIZE FEE (37 CFR 1.16(s))	If the specification and drawings exceed 100 sheets of paper, the application size fee due is \$250 (\$125 for small entity) for each additional 50 sheets or fraction thereof. See 35 U.S.C. 41(a)(1)(G) and 37 CFR	
MULTIPLE DEPENDENT CLAIM PRESENT (37 CFR 1.16(j))		

SMALL ENTITY

RATE (\$)	FEE (\$)
N/A	
TOTAL	

OR

OTHER THAN SMALL ENTITY

RATE (\$)	FEE (\$)
	310
	510
	210
N/A	
TOTAL	1030

* If the difference in column 1 is less than zero, enter "0" in column 2.

APPLICATION AS AMENDED – PART II

(Column 1) (Column 2) (Column 3)

AMENDMENT A		CLAIMS REMAINING AFTER AMENDMENT		HIGHEST NUMBER PREVIOUSLY PAID FOR	PRESENT EXTRA
	Total (37 CFR 1.16(i))	*	Minus	**	=
	Independent (37 CFR 1.16(h))	*	Minus	***	=
	Application Size Fee (37 CFR 1.16(s))				
FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))					

SMALL ENTITY

RATE (\$)	ADDITIONAL FEE (\$)
X =	
X =	
N/A	
TOTAL ADD'T FEE	

OR

OTHER THAN SMALL ENTITY

RATE (\$)	ADDITIONAL FEE (\$)
X =	
X =	
N/A	
TOTAL ADD'T FEE	

(Column 1) (Column 2) (Column 3)

AMENDMENT B		CLAIMS REMAINING AFTER AMENDMENT		HIGHEST NUMBER PREVIOUSLY PAID FOR	PRESENT EXTRA
	Total (37 CFR 1.16(i))	*	Minus	**	=
	Independent (37 CFR 1.16(h))	*	Minus	***	=
	Application Size Fee (37 CFR 1.16(s))				
FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))					

SMALL ENTITY

RATE (\$)	ADDITIONAL FEE (\$)
X =	
X =	
N/A	
TOTAL ADD'T FEE	

OR

OTHER THAN SMALL ENTITY

RATE (\$)	ADDITIONAL FEE (\$)
X =	
X =	
N/A	
TOTAL ADD'T FEE	

* If the entry in column 1 is less than the entry in column 2, write "0" in column 3.

** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 20, enter "20".

*** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 3, enter "3".

The "Highest Number Previously Paid For" (Total or Independent) is the highest number found in the appropriate box in column 1.

This collection of information is required by 37 CFR 1.16. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 12 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

If you need assistance in completing the form, call 1-800-PTO-9199 and select option 2.