

# $V_t$ Compensated voltage-data a-Si TFT AMOLED pixel circuits

James L. Sanford  
Frank R. Libsch

**Abstract** — Active-matrix organic light-emitting-diode (AMOLED) displays are now entering the marketplace. The use of a thin-film-transistor (TFT) active matrix allows OLED displays to be larger in size, higher in resolutions and lower in power dissipation than is possible using a conventional passive matrix. A number of TFT active-matrix pixel circuits have been developed for luminance control, while correcting for initial and electrically stressed TFT parameter variations. Previous circuits and driving methods are reviewed. A new driving method is presented in which the threshold-voltage ( $V_t$ ) compensation performance, along with various circuit improvements for amorphous-silicon (a-Si) TFT pixel circuits using voltage data, are discussed. This new driving method along with various circuit improvements is demonstrated in a state-of-the-art 20-in. a-Si TFT AMOLED HDTV.

**Keywords** — Active matrix, amorphous silicon (a-Si), organic light-emitting diode (OLED), light-emitting diode (LED), thin-film transistor (TFT), threshold voltage, threshold-voltage compensation.

## 1 Introduction

Due to their high brightness and efficiency, the development of organic light-emitting diodes (OLEDs) has lead to considerable interest for use in displays.<sup>1</sup> OLED display products were first commercialized incorporating passive-matrix addressing in 1999 for use in automotive stereo displays.<sup>2,3</sup> Passive-matrix OLED displays are now being used in mobile telephones and even electric shavers. While conventional passive-matrix addressing simplifies the display fabrication, the number of rows is limited to a few hundred.<sup>4,5</sup> Since the OLED is on only when being addressed, high peak currents are required to obtain average brightness levels. Row line resistance, column line resistance, and various OLED electrical characteristics restrict display luminance, size, format, and efficiency. Some improvements are possible by tiling multiple passive-matrix displays or by fabricating a monolithic array of passive-matrix sub-arrays with associated drive electronics on the substrate backside.<sup>6</sup> For very-high-information-content displays, the cost of these approaches is likely to be prohibitive.

Thin-film-transistor (TFT) active-matrix backplanes can virtually eliminate the limitations of display content, size, format, luminance, and efficiency. Kodak has incorporated a small AMOLED display in their commercially available EasyShare LS633 digital camera.<sup>7</sup> Large-area high-resolution AMOLED TFT displays are being demonstrated with active-matrix TFT backplanes.<sup>8–10</sup> The largest AMOLED display demonstrated to date, for example, uses a-Si TFT backplanes to achieve 20-in. diagonal HDTV formats with peak brightness ( $>500$  cd/m<sup>2</sup>), with an efficiency  $>20$  cd/A NTSC white.<sup>10</sup> TFT active-matrix backplanes were initially developed for making large-sized and high-resolution liquid-crystal displays (LCDs). The pixel circuit simply consists of a TFT connected to a storage capacitor

and the pixel LC electrode. The impedance of the liquid-crystal materials used is that of a capacitor whose value varies as a function of applied voltage as the refractive index changes. TFT performance is sufficient to stabilize the storage-capacitor voltage and LC voltage within a row time. The percentage of time that the pixel TFT is on and conducts is very low ( $\sim 0.1$ – $1\%$ ). Applied data and LC voltages alternate polarity from frame to frame to avoid image sticking due to ion plating in the LC. The alternating data voltages and low duty factor on times tend to stabilize transistor characteristics such as threshold voltage for long operating lifetimes in AMLCDs.

Driving OLEDs uniformly with TFTs is more challenging than driving liquid crystal. The main reasons are (1) OLED current-dependent luminance, (2) high OLED capacitance, (3) large TFT dimensions with high gate-to-drain capacitance ( $C_{gd}$ ) and gate-to-source capacitance ( $C_{gs}$ ), and (4) threshold voltage and mobility variations. The drive TFT should provide a continuous current over a large portion of the frame time to efficiently drive the OLED to desired luminance levels. The pixel area limits the number of TFTs and their widths, which is directly proportional to TFT transconductance. As a result, the OLED driving TFT transconductance can be limited. The mobility ( $\mu$ ) of low-temperature polysilicon (LTPS) can be one to two orders of magnitude higher than that of amorphous-silicon (a-Si). As a consequence, LTPS TFT widths can be smaller, with possibilities of allowing for more TFTs in the pixel area for additional error correction. In addition, the LTPS TFT terminal voltages may be lower, yielding better power-efficient operation. As a result of high gate capacitances, TFT on/off switching can create large voltage offsets. Thus, offset correction is required. The OLED capacitance is so large that the OLED current and voltage cannot be driven into equi-

Revised version of a paper presented at the 2003 SID International Symposium, Seminar, and Exhibition, held May 20–22, 2003, in Baltimore, Maryland, U.S.A., and at the 2003 International Display Research Conference, held September 16–18, 2003, in Phoenix, Arizona, U.S.A.

The authors are with the IBM T. J. Watson Research Center, M/S 25-137, 1101 Kitchawan Road, Route 134, P.O. Box 218, Yorktown Heights, NY 10598; telephone 914/945-1568, fax -2141, e-mail: sanfordj@us.ibm.com

© Copyright 2004 Society for Information Display 1071-0922/04/1201-0065\$1.00

librium within a typical row time (10–30  $\mu\text{sec}$ ). This can result in luminance that depends upon the previous state. Pixel-to-pixel variations in  $V_t$  and  $\mu$  add to unwanted luminance variations. With LTPS, initial  $V_t$  and mobility variations exist due to grain size and boundary variations.<sup>11</sup> Time-related electrical stress variations in both  $V_t$  and mobility usually occur.<sup>12,13</sup> In contrast, in most a-Si processes, the initial  $V_t$  and  $\mu$  are uniform within a backplane.<sup>10,14</sup> While time-related electrical stress may produce large  $V_t$  variations, there is typically little change in mobility.<sup>15</sup> Optimized AC terminal voltages help to minimize time-related electrical stress variations.<sup>16</sup>

Various techniques have been employed to minimize the impact of TFT variations with the use of simple pixel circuits. For example, restricting the use of an AMOLED display to video can assure that all pixels experience the same electrical stress. Another method is to operate the OLED driving TFT in a highly nonlinear manner such as an on-off switch.<sup>17,18</sup> In one method, to obtain gray-level images, the bits are sequentially written with binary-weighted timing to the array. This requires a custom-designed frame buffer. In another method, the binary data bits are decoded to drive separate subpixel OLEDs.

A lower cost solution is to send analog data to the pixel circuit and to have the driving method compensate for the  $V_t$  and  $\mu$  variations in the OLED driving TFT. The need for  $V_t$  compensation and previous  $V_t$  compensation methods are discussed. A distinction is made regarding current or voltage data and the logical use of such data for a-Si and LTPS backplanes. Due to its inherent lower manufacturing cost, a-Si backplanes for driving OLEDs is of interest. Emphasis on lower cost also creates a need for simpler voltage-data circuits along with simpler driving methods. New pixel circuits and driving methods with performance results are presented.<sup>19,20</sup> Further improvements and display system integration methods are discussed.

## 2 Prior art

### 2.1 Simple pixel circuits: The need for $V_t$ compensation

The purpose of an ideal AMOLED pixel circuit is to convert the data signal into a predetermined non-varying current for the OLED. Almost all pixel circuits using only conventional active-matrix-addressing schemes are  $V_t$  dependent. To illustrate this point, two relatively simple pixel circuits, a voltage follower and a current source, are shown in Fig. 1. In Fig. 1(a), data in the form of voltage is written onto the data storage capacitor, C, by T1 when the gate line signal is switched high. Transistor T3 operates as a voltage source follower to provide OLED current. Operating in the saturation regime, T3 drain-to-source current,  $I$ , is proportional to  $(V_{\text{data}} - V_{\text{OLED}} - V_t)^2$  for  $V_{\text{data}} < V_{\text{dd}} + V_t$ , where  $V_t$  is the T3 threshold voltage. It is desirable for the OLED driving transistor to operate in saturation so as to minimize current dependence on drain-to-source voltage. In addition to cur-

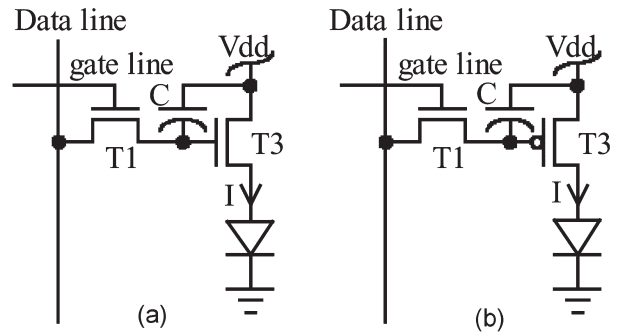


FIGURE 1 — Simple AMOLED pixel circuits; (a) voltage follower, (b) current source.

rent dependence on  $V_t$ , the current also depends on the OLED voltage. The OLED voltage may vary from pixel to pixel and increase slowly with usage,  $\sim 0.1$ – $1$  mV/hour, providing additional sources of non-uniformity.

The current dependence on OLED voltage is eliminated by using the circuit shown in Fig. 1(b). T3 is a PFET device connected in a common source arrangement, allowing T3 to operate as a current source. The current is proportional to  $(V_{\text{dd}} - V_{\text{data}} - V_t)^2$  for  $V_{\text{dd}} + V_t > V_{\text{data}} > V_{\text{OLED}} - V_t$ . As such, the drive current is independent of the OLED voltage.

There are some other operating issues with the circuits in Fig. 1. First, turning T1 off will increase the voltage across C because of T1's gate-to-source capacitance. This is a systematic effect that can be compensated for by modifying the applied data voltages. Second, as the OLED luminance is changed from one frame to the next, the OLED voltage will change, which modifies the voltage across C due to T3's  $C_{\text{gs}}$  coupling in Fig. 1(a) and T3's  $C_{\text{gd}}$  coupling in Fig. 1(b). Several addressing frames using the same data level may be needed for stabilizing the luminance. Thus, a need exists for incorporating  $V_t$  compensation.

### 2.2 Voltage-data $V_t$ compensation

The first  $V_t$ -compensation AMOLED pixel circuit used voltage data ( $V_{\text{data}}$ ) and four TFTs with two additional row line-control signals.<sup>21</sup> The circuit is shown in Fig. 2. Seven sequential operations are performed to address each row. First, with a low SW input signal and a high AZ input signal, the gate line voltage is switched with  $V_{\text{dd}}$  on the data line. Second, the AZ signal is set low, turning T2 on. A voltage across both capacitors is developed that forces T3 to conduct. Third, the SW input signal is pulsed high, turning T4 off and isolating the circuit from the OLED. With T2 on, a voltage that is proportional to the threshold voltage of T3, due to T3 conduction, is developed across both capacitors. Fourth, the AZ input voltage is switched high, turning T2 off. Fifth, the data voltage for luminance is then presented on the data line. A part of the data voltage is coupled onto the capacitor C by capacitor  $C_c$ . Sixth, the gate line signal is set high. Sev-

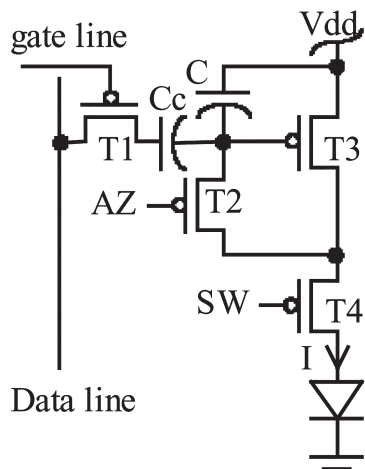


FIGURE 2 — Data voltage pixel with threshold compensation.

enth, the SW input signal is pulsed low turning T4 on and allowing current to flow into the OLED. The OLED current is, to a first order, proportional to the square of the data voltage coupled onto capacitor C.

The circuit in Fig. 2 is fairly complex. It uses four transistors and two storage capacitors. In addition, two other signals and drivers, SW and AZ inputs, are needed for each row. Simulations have shown that there is not sufficient time to accurately set the threshold voltage and write data within a typical row time. To account for high OLED capacitance, a two-row timing scheme was developed for a prototype QVGA display.<sup>22</sup> With this driving method, it is unlikely the circuit in Fig. 2 can be made to work for a higher-resolution display having shorter row times. Accurately setting the threshold voltage on the storage capacitor is a time-consuming operation.

### 2.3 Current data $V_t$ compensation

Another threshold-voltage compensation approach uses data in the form of current or current data ( $I_{data}$ ).<sup>17</sup> Data line current is used to directly set the current flowing through the OLED driving transistor. Both the circuit and driving method are simpler than the circuit shown in Fig. 2. Figure 3 shows two circuit implementations. The circuits consist of four transistors, one capacitor and only one additional input. The driving method consists of four sequential steps. First, the SW signal is switched high turning off T4 to isolate the pixel circuit from  $V_{DD}$  in Fig. 3(a) or from the OLED in Fig. 3(b). Second, in Fig. 3(a), a data current is put onto the data line while the gate line is pulled low, turning on T1 and T2, allowing the data current to flow into the pixel circuit. In Fig. 3(b), a data current is pulled out of the data line while the gate line voltage is set high turning T1 and T2 on. In both cases, the data current flows through both T2 and T3 until the current through T3 matches the data current. Third, the gate line voltage is switched high

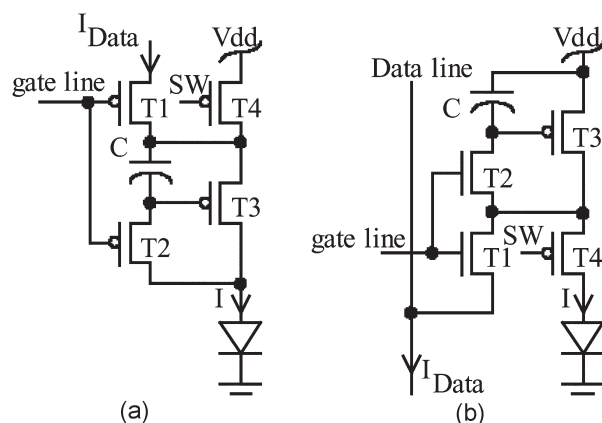


FIGURE 3 — poly-Si current data pixel circuits.

in Fig. 3(a) and is switched low in Fig. 3(b). Fourth, the SW input signal is pulled, connecting the pixel circuit to  $V_{dd}$  in Fig. 3(a) and to the OLED in Fig. 3(b).

Ignoring the capacitor-voltage errors arising from switching of the row and SW inputs, the  $I_{data}$  method does account for any changes in  $V_t$  and  $\mu$  in the OLED driving transistor T3. However, for dark-gray data levels, the low data current is not able to charge or discharge the data line for pixel circuit to reach equilibrium within a row time. There are some solutions to this issue. One solution is to incorporate high data currents with a current mirror that provides a reduction in the ratio data current to the OLED current.<sup>9</sup> However, this arrangement does not directly set the current of the OLED driving transistor. The current through the OLED driving TFT can be different than the current mirror ratio of the data current because of variations in fabrication and differences in electrical stress. Another solution is to modulate the SW input signal in Fig. 3 at a low duty factor to compensate for the use of high data currents. A third solution is to drive the SW input in Fig. 3 with time binary-weighted digital data.<sup>24</sup> A reference current is used in the place of current data.

Recently, threshold-voltage compensation circuits using  $I_{data}$  for an a-Si TFT active matrix are being considered.<sup>25</sup> Figure 4 shows an a-Si pixel circuit using only NFETs. The circuit operation is essentially the same as the circuits shown in Fig. 3. Since the drain and source currents are identical, it is only a matter of perspective to use NFETs to form current sources. The SW input signal can be eliminated by connecting the input to  $V_{dd}$ . This allows T4 to function like a diode and still provide some power-supply isolation when writing.

While a-Si is able to produce steady-state currents suitable for reasonable brightness levels, the terminal voltages are fairly large. Due to the high terminal voltages resulting from low  $\mu$  the two transistors in series between the power supply and the OLED significantly add to the power dissipation. As a result, the circuit in Fig. 4 may not be suitable for large-sized displays having high luminance. Fur-

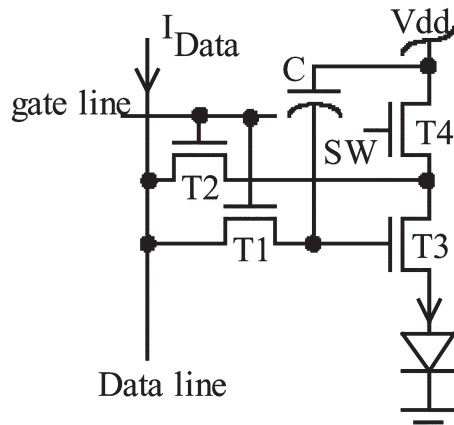


FIGURE 4 — An a-Si current data pixel circuit.

thermore, unlike poly-Si where the current data drivers may be designed into the display panel, a-Si backplanes must incorporate crystalline-silicon data drivers. Commercial  $I_{data}$  drivers are not available. An  $I_{data}$  driver for various display sizes, formats, pixel designs, and brightness levels are more complex and costly than  $V_{data}$  drivers to design and build.

### 3 A new voltage-data $V_t$ compensation method for a-Si

It is generally accepted that the backplane fabrication using a-Si is lower in cost than that for poly-Si. Since, a-Si mobility does not vary within a backplane or with electrical stress over time, it seems appropriate to use the  $V_{data}$  compensation method with a-Si. In contrast, it seems appropriate to use  $I_{data}$  with poly-Si since mobility varies across the backplane.  $V_{data}$  allows the use of low-cost commercial LCD data drivers and eliminates the cost associated with crystalline-silicon  $I_{data}$  drivers.

In the design of an AMOLED pixel circuit, there are many design tradeoffs such as cost, display lifetime, the number and size of the pixel circuit components, data voltage range, and power dissipation. As seen with the  $V_{data}$  pixel circuit shown in Fig. 2, additional row control signals

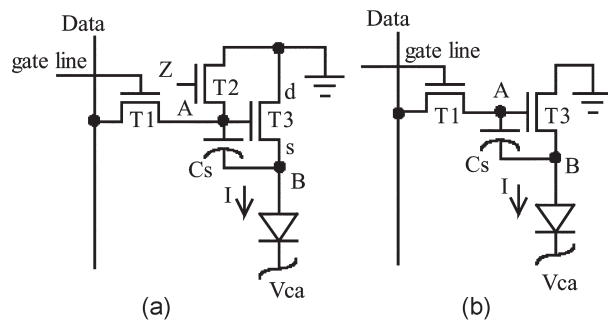


FIGURE 5 — (a) Initial pixel circuit; (b) a simpler circuit.

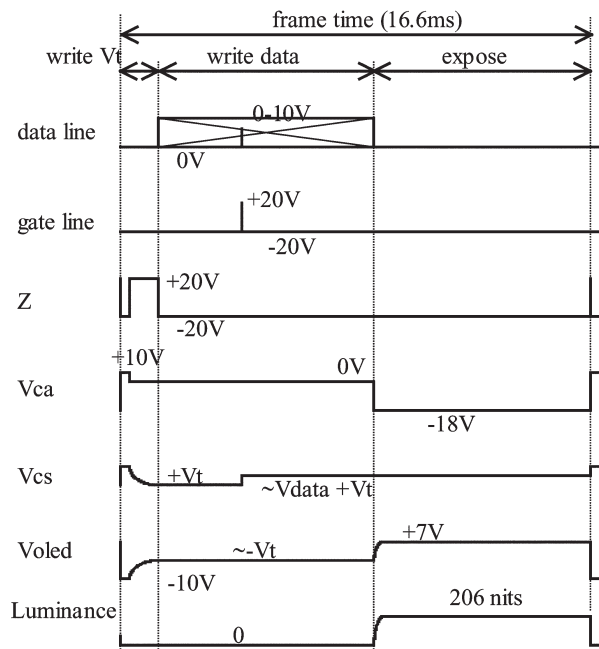
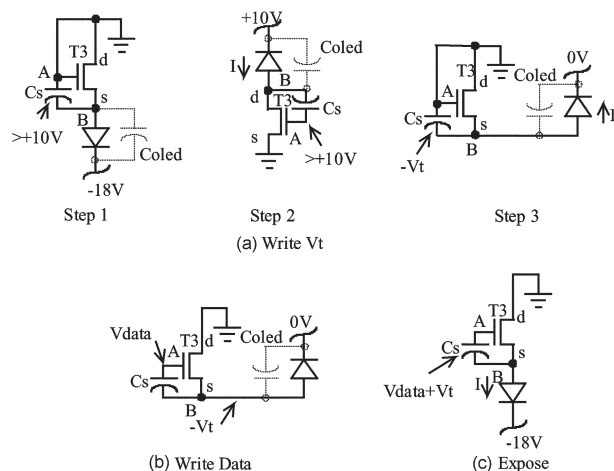


FIGURE 6 — Signal timing for Fig. 5(a).

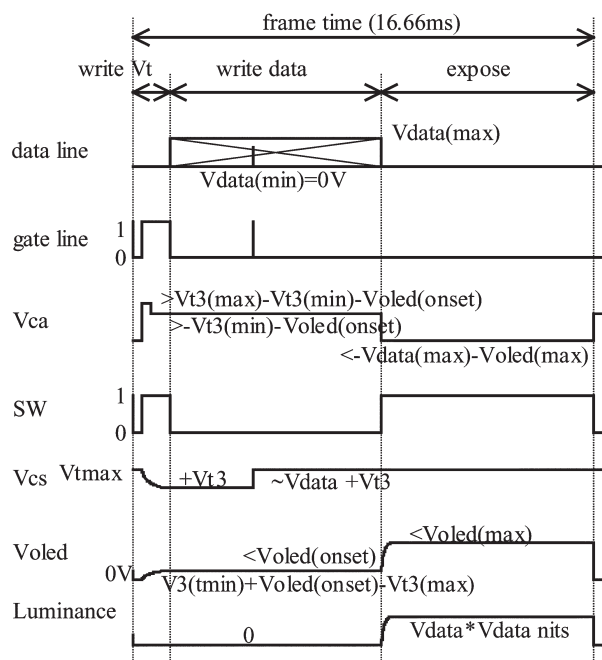
are needed. For a-Si backplanes, this requires a custom-designed crystalline-silicon row driver, which would be more expensive than commercial LCD row drivers. The on time or duty factor of the OLED current driving TFT needs to be a large part of the frame in order to produce sufficient luminance. Too much variation in  $V_t$  will produce objectionable luminance variation. The large duty cycle severely stresses the OLED driving TFT. By increasing the width of the OLED driving TFT, the terminal voltages can be reduced. On the other hand, the TFT width cannot be too large or else the TFT will not fit within the pixel area or leave room for the other pixel circuit components. It may also be necessary for the TFT terminal voltage polarities to be alternated to further reduce the electrical stress in order to meet the display lifetime requirements. The size of the data storage capacitor also impacts the time required to establish the threshold voltage, the time to write data, the amount of pixel area, the voltage offsets, and  $V_t$  errors due to switching signals. In addition, the range of data voltages (just off to maximum luminance) should be large relative to  $V_t$  to minimize the impact of  $V_t$  compensation errors. For operation in the saturation regime, the OLED driving TFT drain-to-source voltage needs to be equal to or greater than the data voltage range. A larger data voltage range results in higher power dissipation. The different design tradeoffs depend largely upon the application.

Simpler  $V_{data}$   $V_t$  compensation pixel circuits are possible by using multilevel cathode voltages, use of the OLED capacitance, elimination of write data conduction, and

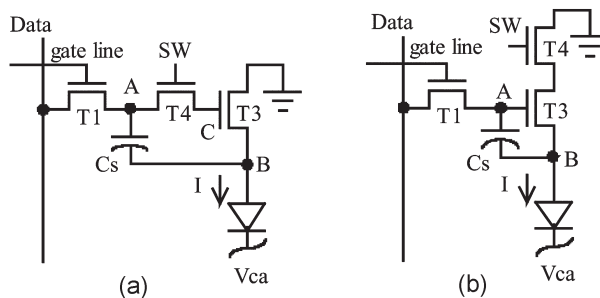


**FIGURE 7** — Figure 5 equivalent circuits for the different circuit operation.

device merging. An initial pixel circuit and signal timing incorporating a multilevel cathode voltage is shown in Figs. 5(a) and 6, respectively. The equivalent circuit for each step is shown in Fig. 7. The frame time is segmented into a write  $V_t$  period, a write data period, and an expose period. This allows the write  $V_t$  step to be longer than a row time. At the beginning of the write  $V_t$  period (step 1), the Z input signal is momentarily pulled high to assure that a voltage greater than T3's  $V_t$  ( $\sim 10$  V) is established on the storage capacitor  $C_s$ . The cathode voltage ( $V_{ca}$ ) is then switched from  $-18$  V to  $+10$  V with a low Z input (step 2). This reverse biases the



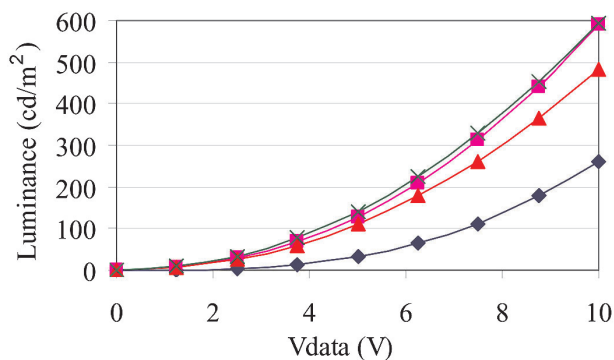
**FIGURE 8** — Signal timing for Figs. 5(b), 9, and 13.



**FIGURE 9** — Circuits that inhibit write period conduction in T3.

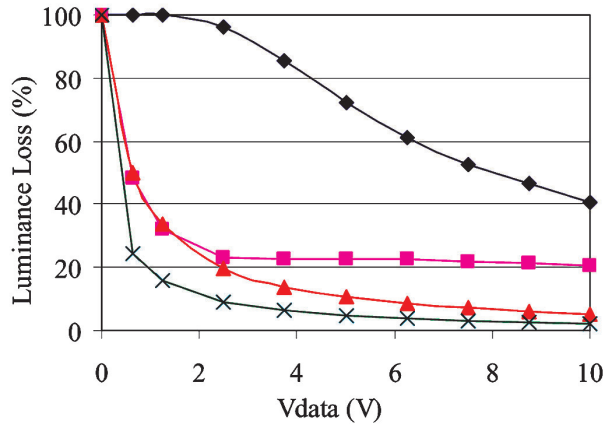
OLED via the reverse (source-to-drain) conduction of T3. In addition, the gate-to-drain voltage and drain-to-source voltage is reversed for removing residual charge induced from normal operation. The duration and voltages in this step can be adjusted to minimize the electrical stress due to T3 driving the OLED. The  $V_{ca}$  is then set to  $0$  V with a high Z input signal (step 3). The T3's drain-to-source conduction then establishes a voltage that is approximately equal to T3's  $V_t$  across  $C_s$  and the OLED cathode-to-anode terminals. Since the settling time is non-linear, the duration and accuracy are best determined with circuit simulations. During the write data period, the Z input is low while data is written onto node A. Since the OLED capacitance is much greater than  $C_s$  and T3's  $C_{gs}$ , node B is maintained at  $-V_t$  during the write data period. The resulting voltage on  $C_s$  is  $V_{data} + V_t$ . During the expose period, the  $V_{ca}$  is set to  $-18$  V assuring that T3 operates in saturation. The current through T3 and the OLED is proportional to  $(V_{data} + V_t - V_t)^2$  or just  $V_{data}^2$ . SW and  $V_{ca}$  are connected to all of the pixels in the display.

The circuit in Fig. 5(b) functions in a similar manner, but without T2. The gate-line signal timing has been modified and is shown in Fig. 8. The gate-signal timing during the write  $V_t$  period along with the  $0$ -V data line voltage performs the same function that T2 and SW input did for the circuit in Fig. 5(a). The required operating signal voltage amplitudes are shown as a function of circuit properties. This notation allows for signal and power dissipation optimi-



**FIGURE 10** — Luminance for standard voltage follower circuit (diamonds); Fig. 5(b) (squares), Fig. 9(a) (triangles), and Fig. 9(b) (x).

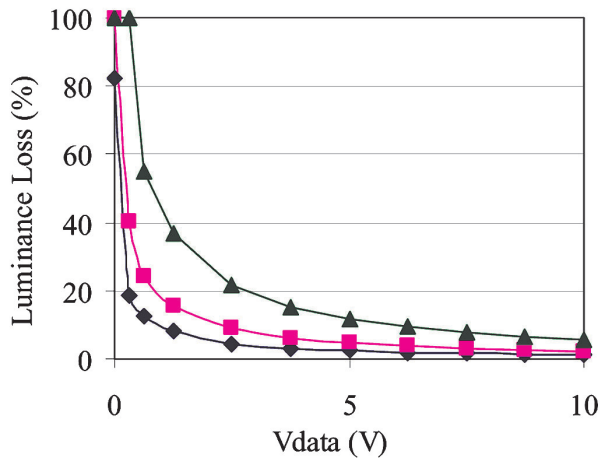




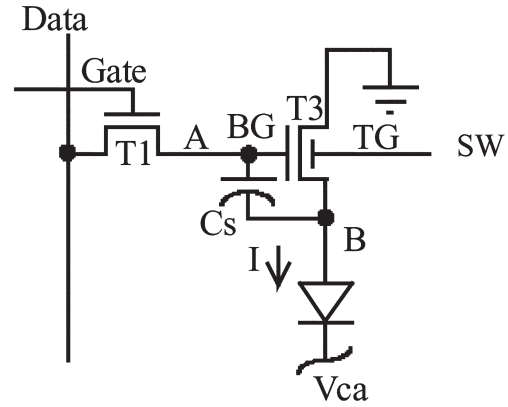
**FIGURE 11** — Percent luminance loss due to 2-V  $V_t$  increase for standard voltage follower (diamond); Fig. 5(b) (squares), Fig. 9(a) (triangles), and Fig. 9(b) (x).

zation. The SW signal timing shown in Fig. 8 is for use with the circuits in Figs. 9 and 13.

The circuits in Fig. 5, to a first order, do correct for  $V_t$  variations from one pixel circuit to another. However, as data is written onto the storage capacitor  $C_s$ , T3 conducts, charging up node B and reducing the voltage across  $C_s$ . The previously written  $V_t$  is also effectively reduced, thereby lowering the amount of  $V_t$  compensation. The circuits shown in Fig. 9 with the signal timing in Fig. 8 inhibit current flow through T3 during the write data period. The SW signal input is switched low during the write data period. In Fig. 9(a), T4 is off, which isolates the data from T3's gate. At the expose period, the SW signal is set high turning T4 on and connecting  $C_s$  to the gate of T3. Since, for luminance, the voltage on the positive  $C_s$  terminal, node A, is greater than the voltage at the gate of T4, node C, some portion of the charge on  $C_s$  will be redistributed onto node C. This capacitance divider action also effectively reduces the previously



**FIGURE 12** — Percent luminance loss for a 1 V (diamonds), 2 V (squares), and 5 V (triangles)  $V_t$  increase for the Fig. 9(b) circuit.



**FIGURE 13** — Circuit with a top- and bottom-gate TFT.

written  $V_t$ , reducing the amount of  $V_t$  compensation. In Fig. 9(b), T4 is off, not allowing current to flow through T3 during the write data period. Since T4 is connected in series with T3 to provide current to the OLED, T4's drain-to-source voltage must be added to the magnitude of  $V_{ca}$ . The additional voltage increases the power dissipation.

## 4 Results

With nearly identical conditions, the circuits in Figs. 5(b), 9(a), and 9(b) have somewhat different transfer functions or input-to-output functions, where the input is the  $V_{data}$  voltage and the output is the OLED luminance. The ideal transfer function would be proportional to  $V_{data}^2$  and be  $V_t$  independent. Results of transient simulation depicting the transfer functions of these circuits are shown in Fig. 10. The transfer function of a standard voltage follower circuit similar to that shown in Fig. 5(b), which does not incorporate the signal timing in Fig. 8 and where  $V_{ca}$  is fixed at  $-4.5$  V and T3's drain is connected to  $+13.5$  V, is shown for comparison. The capacitance of  $C_s$  is  $0.5$  pF. A model for a small-molecule low-off-current OLED having a  $\sim 4$ -cd/A efficiency is used. The OLED forward voltage at  $500$  cd/m<sup>2</sup> is  $\sim 7$  V, the OLED capacitance is  $\sim 6$  pF, and the TFT mobility is  $0.7$  cm<sup>2</sup>/V-sec. The channel length for all TFTs is  $8$   $\mu$ m. The channel width of T1 and T3 for all circuits is  $48$  and  $64$   $\mu$ m, respectively. The channel width for T4 in Fig. 9(b) is  $48$   $\mu$ m. A low off luminance level with  $V_{data} = 0$  is obtained by using the gate line, SW, and  $V_{ca}$  voltage levels as shown in Fig. 6, and transistor widths mentioned above, to balance the charge pulled out of the  $C_s$  as the gate line is switched low when data is written with charge put into  $C_s$  as T4 is turned on and  $V_{ca}$  is set to low at the beginning of the expose period. In order to obtain a low luminance level of  $<0.3$  cd/m<sup>2</sup> with  $V_{data} = 0$ , the width of T4 in Fig. 9(a) was set to  $4$   $\mu$ m. The write  $V_t$  period is  $0.5$  msec with the write data period splitting the remaining frame time with the expose period.

The relatively low luminance output with data voltage for the standard voltage follower (diamond data points)

resulted from lower data voltage on  $C_s$  since the OLED voltage is current dependent. The standard voltage follower results shown here are equilibrated; that is, with the same  $V_{\text{data}}$  for five repeated frame times. The output luminance of the circuit shown in Fig. 9(a) (triangle data points) is less than that of the circuits shown in Figs. 5(b) and 9(b), as a result of the circuit charge redistribution discussed earlier. The luminance of the circuit in Fig. 9(b) (X data points) is slightly higher than that of the circuit in Fig. 5(b) (square data points) due to the elimination of T3 conduction during the write data period.

Rather than repeat Fig. 10, which shows luminance versus  $V_t$ , it is more useful to present the percent loss in luminance with an increase in  $V_t$ . The plot in Fig. 11 shows the percent luminance loss resulting from a +2 V increase in  $V_t$  over a 0–10-V data voltage range for the standard voltage follower circuit (diamond data points), the circuit in Fig. 5(b) (square data points), the circuit in Fig. 9(a) (triangle data points), and the circuit in Fig. 9(b) (X data points). As expected, the luminance loss for the standard voltage follower circuit is the largest, having ~100% at  $V_{\text{data}} = 2$  V and 40% at  $V_{\text{data}} = 10$  V. The circuit in Fig. 5(b) reduced the luminance loss to ~25% at  $V_{\text{data}} = 2$  V and to ~20% for  $V_{\text{data}} = 10$  V. For the circuit shown in Fig. 9(a), the luminance loss is ~5% at  $V_{\text{data}} = 10$  V. The circuit in Fig. 9(b) gave the lowest luminance loss; ~10% for  $V_{\text{data}} = 2$  V and ~2.3% for  $V_{\text{data}} = 10$  V, respectively.

Shown in Fig. 12 is the percent luminance loss over a 0–10-V data voltage range for a 1, 2, and 5 V  $V_t$  increase for the circuit shown in Fig. 9(b). Even with a 5-V  $V_t$  increase, the luminance loss is <30% for  $V_{\text{data}} = 2$  V and <6% for  $V_{\text{data}} = 10$  V.

There are several sources of error that explain the luminance loss for these  $V_t$ -compensated circuits. First, during the write  $V_t$  period, the differences in  $V_t$  are stored to within 10 mV for 2-V  $V_t$  difference. Second, signal switching at the end of the write  $V_t$  period and during the write data period reduces the stored  $V_t$  difference by about 15 mV. For the circuit shown in Fig. 5(b), there is an error of 800 mV in the stored  $V_t$  difference due to conduction when data is written. Third, for the circuit shown in Fig. 9, most of the loss occurs when  $V_{ca}$  is set to -18 V at the beginning of the expose period. Since T3's  $V_t$  is established on the OLED capacitance, there is an increased voltage swing across the OLED as the OLED turns on with  $V_t$ . The voltage swing pulls charge out of the positive terminal of  $C_s$  through the  $C_{gs}$  and  $C_{gd}$  capacitance of T1 and T3, respectively. Differences in  $V_t$  established on the OLED at the end of the write  $V_t$  period will induce a voltage difference on  $C_s$ . The stored  $V_t$  difference is reduced by another 75 mV for 2-V difference in  $V_t$ . This error can only be reduced by increasing  $C_s$ , reducing the  $C_{gs}$  and  $C_{gd}$  capacitance and OLED current. Reducing the OLED current allows for the reduction of TFT widths, voltages, time-related voltage stress, and the amount of  $V_t$  variation.

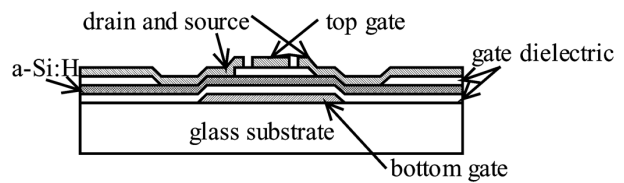


FIGURE 14 — Structure of top- and bottom-gate TFT.

## 5 Additional improvements

### 5.1 Device merging

The circuit shown in Fig. 13 is a lower-power alternative to the circuit shown in Fig. 9(b). TFT T3 is shown as having a top and bottom gate<sup>26</sup>. T3 is a functional merging of T3 and T4 in Fig. 9(b). The structure of the top- and bottom-gate TFT is shown in Fig. 14. With the exception of the top gate, the structure of the device is that of a standard bottom-gate TFT. The bottom gate operates as an accumulation gate. The top gate is formed or etched at the same time as drain and source is formed without additional fabrication steps. Since the top gate does not overlap the drain and source contacts, it can only deplete or pinch off the channel. The top gate stops conduction through the TFT during the write  $V_t$  and write data periods. The width of the top gate and spaces to the drain and source metal can be minimum process feature dimensions, thus enabling the same bottom-gate channel length dimension as that in single-gate TFT implementation. The SW input switching has less effect on the  $C_s$  voltage than the circuit shown in Fig. 9(b). Due to extra gate dielectric and narrow length, the top-gate to bottom-gate capacitance is approximately 10× less than the conventional bottom-gate  $C_{gd}$  or the bottom gate  $C_{gs}$ . The top-gate  $C_{gs}$  and the top-gate  $C_{gd}$  capacitance are also ~10× smaller in comparison to that of the bottom gate. While characteristics are highly process dependent, the  $V_t$ -compensation performance is expected to be similar to that of the circuit shown in Fig. 9(b).

### 5.2 Simpler and faster operation

The a-Si circuits shown in Figs. 5, 9, and 13 use multilevel cathode voltage switching, and these circuits take 0.5 msec to write the  $V_t$  on the data-storage capacitor. The multilevel cathode voltage switching can be eliminated, a faster write  $V_t$  time and lower cost are obtained with a somewhat more complex pixel circuit. The circuit is shown in Fig. 15 and the associated timing diagram is shown in Fig. 16. An additional TFT T5, an additional voltage input  $V_a$ , and input signal RS are incorporated to quickly reverse the voltage across the OLED without changing the OLED cathode voltage,  $V_{ca}$ . At the beginning of the write  $V_t$  period, the RS and gate line input signals are switched high with 0 V on the data line. This reverse biases the OLED to -8 V. In one step, the circuit is set up for setting  $V_t$  on the storage capacitor. Since the  $V_{ca}$  terminal voltage is not set low during the beginning

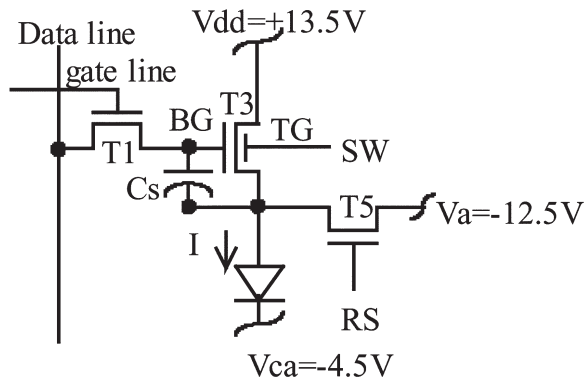


FIGURE 15 — Faster and simpler operation.

of the expose period, a voltage larger than  $V_t$  is needed on the storage capacitor prior to writing data to offset the charge pulled out of the storage capacitor when the gate line voltage is switched low when writing data. In setting the capacitor voltage prior to writing data, the capacitor voltage needs to be  $V_t$  plus the gate line turnoff offset; typically 1 V. This voltage can be set much faster than with the other a-Si circuits;  $\sim 150 \mu\text{sec}$  as compared to 0.5 msec. The OLED cathode is a high-capacitance connection. There is some power supply and driver cost associated with multi-level cathode voltage switching. In Fig. 15,  $V_{ca}$  and  $V_a$  are fixed voltages. The capacitance of the RS signal is much lower than that of the OLED cathode and is easier to drive.

One potential drawback of this circuit and driving method is that the gate-to-drain and drain-to-source terminal voltage of T3 do not alternate polarity. The circuit, however, does allow for the possibility of alternating the gate-to-drain voltages with the use of high data voltages with a time allocated period.

## 6 System integration

In Fig. 5(b), it is assumed that all the row driver outputs can be set high simultaneously during the write  $V_t$  period. Clock rates for high-voltage gate drivers can be less than 1 MHz. For such drivers, it could take more than 1 msec to switch all the rows to high. However, a number of gate drivers have output gates to simultaneously switch the outputs to high for testing purposes. In other cases, the shift registers used for row selection can be made transparent so that a high row selection state can very quickly propagate through to all row latches without clocking. Otherwise, a TFT, T2 in Fig. 5(a), can be used. The drawback is that T2 adds additional stray capacitance to node A which impacts the  $V_t$ -compensation performance.

Another possible system integration issue is that the data is written to display in about half the frame time. This requires that the data bandwidth from the frame buffer and data driver speed be twice as fast as in typical displays. It is possible to spread out writing data over the entire frame

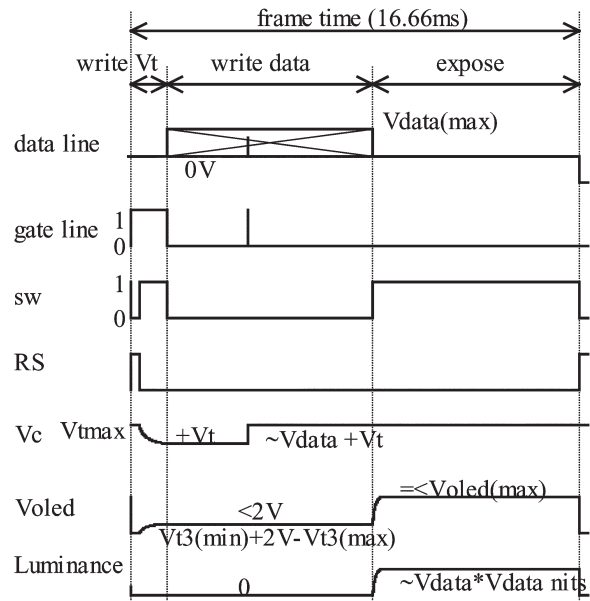


FIGURE 16 — Timing form for Fig. 15.

time. With separate upper-half display and lower-half display signal timing and connections for the gate drivers,  $V_{ca}$ , SW, RS if used, and Z if used, the operation of the lower display half can be delayed about half a frame time relative to the upper half of the display. This partitioning allows writing the data in a typical manner to the display.

## 7 Conclusion

Simpler a-Si pixel circuits and driving methods with  $V_t$  compensation using LCD data and gate drivers are presented. Only one additional backplane signal (SW) and only two or three TFTs per pixel are used. Along with signal timing diagrams, the  $V_t$ -compensation performance for these circuits are presented. With a 4-cd/A efficient OLED, the luminance loss is  $<10\%$  over 95% of the luminance range for a 2-V increase in  $V_t$ . If optimized for a higher efficiency OLED, luminance loss with  $V_t$  would be proportionally less. The use of cathode voltage switching reduces the residual charge due to electrical stress on the OLED and OLED current generating TFT by reversing the terminal voltages. The pixel circuit implementations presented allows use of commercial LCD data and gate drivers for low cost AMOLED displays. Pixel circuits similar to those shown in Figs. 5 and 9 are used in a 20-in.-AMOLED display.<sup>10</sup> With improvements in OLED efficiencies and lifetimes, a-Si AMOLED displays should be suitable for most applications. The simulations compare favorably with the 20-in.-AMOLED display, which optimizes the organic material and LED structure to obtain an efficiency greater than 20-cd/A NTSC white, with a measured luminance loss less than 1% over 95% of the luminance range for a 2-V increase in  $V_t$ .



## References

- 1 C W Tang and S A Van Slyke, *Appl Phys Lett* **51**, 913 (1987).
- 2 T Tohma, *Proc IDRC '97*, F1-F4 (1997).
- 3 D Lieberman, "Next-gen flat panel display technology poised for big growth," *EE Times* **45**, (November 15, 1999).
- 4 G Gu and S R Forest, "Design of Flat-Panel Displays Based upon Organic Light-Emitting Devices," *IEEE J Selected Topics in Quantum Electronics* **4**, No. 1, 83-99 (1998).
- 5 T Van de Biggelaar, I Camps, M Childs, M Flueter, A Giraldo, S Godfrey, I M Hunter, M T Johnson, H Lifka, R Los, A Sempel, J M Shannon, M J Trainor, R W Wilks, and N D Young, "Passive and active matrix addressed polymer light emitting diode displays," *Flat Panel Display Technology and Display Metrology II, Proceedings of SPIE* **4295**, 134-146 (2001).
- 6 J Sanford and F Libsch, "High Information Content Passive OLED Displays," *IDRC '02*, 101-104 (2002).
- 7 <http://www.kodak.com/US/en/corp/display/LS633.html>
- 8 G Rajeswaran, M Itoh, M Boroson, S Barry, T K Hatwar, K B Kahen, K Yoneda, R Yokoyama, T Yamada, N Komiyama, H Kanno, and H Takahashi, "Active matrix low temperature poly-Si TFT/LED full color displays: development status," *SID Intl Symp Digest Tech Papers*, 974-977 (2000).
- 9 T Sasaoka, M Sekiya, A Yumoto, J Yamada, T Hirano, Y Iwase, T Yamada, T Ishibashi, T Mori, M Asano, S Tamura, and T Urabe, "A 13.0-in. AM-OLED display with top emitting structure and adaptive current mode programmed pixel circuit (TAC)," *SID Intl Symp Digest Tech Papers*, 384-387 (2001).
- 10 T Tsujimura, Y Kobayashi, K Murayama, A Tanaka, M Morooka, E Fukumoto, H Fujimoto, J Sekine, K Kanoh, K Takeda, K Miwa, M Asano, N Ikeda, S Kohara, S Ono, C-T Chung, R-M Chen, J-W Chung, C-W Huang, H-R Guo, C-C Yang, C-C Hsu, H-J Huang, W Riess, H Riel, S Karg, T Beierlein, D Gundlach, S Alvarado, C Rost, P Mueller, F Libsch, M Mastro, R Polastre, A Lien, J Sanford, and R Kaufman, "A 20-in. OLED Display Driven by Super-a-Si Technology *SID Intl Symp Digest Tech Papers*, 6-9 (2003).
- 11 See Chapter 4 and references therein, in book *Thin Film Transistors*, C. Kagan and P. Andry, eds. (Marcel Dekker, Inc., NY, 2003).
- 12 D Fish, N Young, M Childs, W Steer, D George, D McCulloch, S Godfrey, M Trainer, M Johnson, A Giraldo, H Lifka, and I Hunter, "A Comparison of Pixel Circuits for Active Matrix Polymer/Organic LED Displays," *SID Intl Symp Digest Tech Papers*, 968-971 (2002).
- 13 F R Libsch, C Wong, and P McFarland, "Role of Charge Transport and Trapping in the Reliability of Submicron Polysilicon Thin Film Transistors," *Proc IEEE IEDM*, 739-743 (1991).
- 14 R Troutman and F Libsch, "Modeling and Parameter Extraction of Amorphous Silicon Thin-Film Transistors for Active-Matrix Liquid-Crystal Displays," *Proc IEEE IEDM*, 855-858 (1990).
- 15 F R Libsch and J Kanicki, "Bias-stress-induced stretched-exponential time dependence of charge injection and trapping in amorphous thin-film transistors," *Appl Phys Lett* **62**, 1286-1288 (1993).
- 16 F R Libsch and J Kanicki, "TFT Lifetime in LCD Operation," *SID Intl Symp Digest Tech Papers*, 455-458 (1993).
- 17 M Mizukami, K Inukai, H Yamagata, T Konuma, T Nishi, J Koyama, S Yamazaki, and T Tsutsui, "6-Bit digital VGA OLED," *SID Intl Symp Digest Tech Papers*, 912-915 (2000).
- 18 M Kimura, H Maeda, Y Matsueda, H Kobayashi, S Miyashita, and T Shimoda, "An area-ratio gray-scale method to achieve image uniformity in TFT-LEPDs," *J SID* **8/2**, 93-97 (2000).
- 19 J Sanford and F Libsch, "TFT AMOLED pixel circuits and driving methods," *SID Intl Symp Digest Tech Papers*, 10-13 (2003).
- 20 J Sanford and F Libsch, "V<sub>t</sub> compensation performance of Voltage data AMOLED pixel circuits," *IDRC '03*, 38-41 (2003).
- 21 R M A Dawson, Z Shen, D A Furst, S Connor, J Hsu, M G Kane, R G Stewart, A Ipri, C N King, P J Green, R T Flegal, S Pearson, W A Barrow, E Dickey, K Ping, C W Tang, S Van Slyke, F Chen, J Shi, J C Sturm, and M H Lu, "Design of an improved pixel for polysilicon active-matrix organic LED display," *SID Intl Symp Digest Tech Papers*, 11-15 (1998).
- 22 R M A Dawson, Z Shen, D A Furst, S Connor, J Hsu, M G Kane, R G Stewart, A Ipri, C N King, P J Green, R T Flegal, S Pearson, W A Barrow, E Dickey, K Ping, C W Tang, S Van Slyke, C H Chen, J Shi, M H Lu, M Moskewicz, and J C Sturm, "A Poly-Si Active-Matrix OLED Display with Integrated Drivers," *SID Intl Symp Digest Tech Papers*, 438-441 (1999).
- 23 R M A Dawson, Z Shen, D A Furst, S Connor, J Hsu, M G Kane, R G Stewart, A Ipri, C N King, P J Green, R T Flegal, S Pearson, W A Barrow, E Dickey, K Ping, S Robinson, C W Tang, S Van Slyke, F Chen, J Shi, M H Lu, and J C Sturm, "The impact of the transient response of organic light emitting diodes on the design of active matrix OLED displays," *IEDM* **98**, 875-878 (1998).
- 24 M Shimoda, K Abe, H Haga, H Asda, K Hayama, K Iguchi, D Iga, H Imura, and S Miyano, "An integrated poly-Si TFT current data driver with a data-line precharge function," *J SID* **11/3**, 461-466 (2003).
- 25 R Hattori, T Ysukamizu, R Tsuchiya, K Miyake, Y He, and J Kanicki, "Current-writing active-matrix circuit for organic light-emitting diode display using a-Si:H thin-film-transistors," *IEICE Trans Electron* **E83-c**, No. 5, 779-782 (May, 2000).
- 26 B-S Wu, J-S Cheng, H-K Tsai, T-L Lin, T-S Weng, W-J Lin, and H-K Chen, "A novel depletion-gate amorphous silicon thin-film transistor," *IEEE Electron Device Letters* **13**, No. 1, 17-19 (January 1992).



**James L. Sanford** is a Senior Engineer at the IBM T. J. Watson Research Center. He received his B.S.E.E. from the Ohio State University in 1972 and joined IBM. His recent work activities have included LCoS for projection, high-frame-rate holographic storage light valves, OLED-on-silicon direct-view VGA wristwatch displays, and a-Si AMOLED displays. IBM honors include two Outstanding Technical Achievement Awards and six Invention Achievement Awards. Mr. Sanford is a member of the Society of Information Display.



**Frank R. Libsch** has been a Research Staff Member at IBM in the Thomas J. Watson Research Center since 1989. Dr. Libsch has managed groups engaged in advanced flat-panel-display devices, processes, and test research at the T. J. Watson Research Center. He is now manager of the Advanced Optical Interconnect and Packaging Group, which is responsible for defining and executing IBM's exploratory high bandwidth electrical and

optical interconnect road map for server technology. In addition to managing the wide range of technical activities from silicon-based light modulators and detectors to PCB integrated single- and multi-mode optical waveguides and coupling packages, Dr. Libsch maintains an active research career that centers on various aspects of drive schemes and electronics, pixel designs, CMOS FETs and TFTs inorganic and organic solid-state devices, physics and fabrication technology and their application in various direct view and projection, transmissive, emissive, and reflective flat-panel displays. He holds over 25 U.S. and foreign patents and is the author or coauthor of over 75 technical publications, including recent book chapters entitled *Thin-Film Transistors in Active-Matrix Liquid Crystal Displays (AMLCDs)* in the Marcel Dekker published book *Thin-Film Transistors*, and *SONOS Nonvolatile Semiconductor Memories* in the IEEE published book *Nonvolatile Semiconductor Memory Technology*. Dr. Libsch is a member of the IEEE, SID, MRS, New York Academy of Sciences, and Sigma Xi. He has served as guest co-editor on several occasions, including the recent March 2002 IEEE Proceedings Special Issue on Displays, and the MRS Symposium Proceedings Volume 558 on *Flat-Panel Displays and Sensors-Principles Materials and Processes*. He has recently served as the chairperson of the AMLCD Subcommittee of the Society of Information Display for four continuous years, the Technical Program Chair for SID 2001, and the General Chair for SID 2003. He formed the Technical Program OLED Subcommittee for the 2001 Symposium. He continues to be a member of this subcommittee.