P-40: A Novel Data Driving Method and Circuits for AMOLED Displays

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Abstract

A novel current-mode driving method and driving circuits are proposed for AMOLED displays. The data driving speed in conventional current-mode driving methods is dramatically enhanced by the proposed method and circuits. The proposed method shortens data driving time with feedback of the transient charging current from the parasitic capacitance of an adjacent data line. The current consumption and chip size of the data driver IC are reduced by a half, because one data driving circuit can drive two data lines of a display panel. 10 nA data current can be transferred to the pixel circuit of a display panel with sub-nA accuracy in 15 µsec. The data line parasitic resistance and capacitance are 4 kohm and 20 pF, respectively.

1. Introduction

Offering wide viewing angle, fast response, low power consumption, and thinness, AMOLED displays hold promise as next generation flat panel displays. Compared to LCDs, PDPs, and CRTs, however, the quality of AMOLED displays from a display uniformity point of view is not satisfactory.

Various driving schemes and pixel circuits have been introduced in efforts to improve the display uniformity of AMOLED displays due to variations of pixel-to-pixel characteristics [1-9]. These driving schemes, including the proposed driving method, can be technologically categorized as shown in Figure 1.

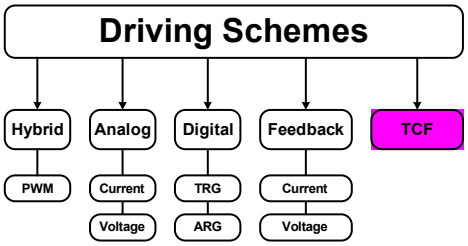

Figure 1. Tree of data driving schemes

Voltage-mode driving methods and pixel circuits cannot compensate mobility variation effects on display uniformity, although they provide fast driving speed [5].

In terms of display uniformity, the driving method and the pixel circuit that offer the best performance are current-mode driving and current-copy pixel, respectively [5]. However, high speed data driving is beyond attainment with the conventional current-mode data driver for large pre-charge error voltages, because data currents must drive data lines and pixels in the end of the scan time [6].

In this paper, a novel data driving method and circuits that remarkably reduce data driving time by utilizing feedback of the transient charging current generated from an adjacent data line are described.

2. Operation Principle

Long data line charging/discharging time prevents the application of current-mode driving to display panels. Figure 2 shows the proposed data driver architecture. In order to enhance the data driving speed, the transient cancellation feedback (TCF) output driver has been composed. The TCF output driver adaptively provides the required transient charging current for a data line parasitic capacitance and transfers data current to the pixel circuit simultaneously. The adaptive generation of the transient charging current for a data line capacitance shortens the data driving time because the transient current adaptively charges the data line capacitance instead of the data current.

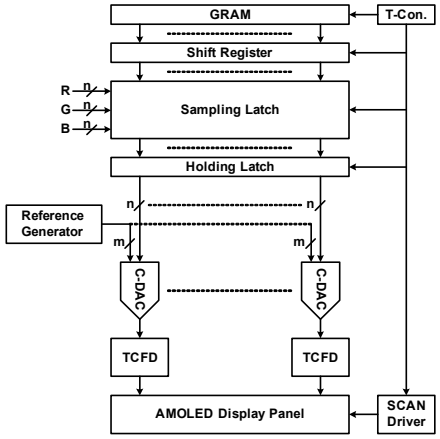

Figure 2. Current-mode data driver architecture with the output drivers

Figure 3 shows the conceptual operation of the TCF output driver. For fast transfer of a data current (I_{DATA}) to a pixel current (I_{pixel}), the parasitic capacitance of a data line (C_{PP}) should be charged swiftly with a large current. The variable current source (I_{BT}), which is controlled by sensing the voltage variation at node A (V_A), adaptively supplies the required transient charging current for the data line. V_A senses the change of I_{DATA} and generates the control voltage (V_B) according to this change. I_{BT} has two current components, one is static (I_B) and the other is transient. This transient component is the charging current of C_{PP}. The data driving speed and accuracy depend on the accuracy and promptness of the I_{BT}.

The implemented circuits of the TCF concept given in Figure 3 are shown Figure 4. The capacitance and the initial voltage of the

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data line should be known first so as to generate the required transient charging current.

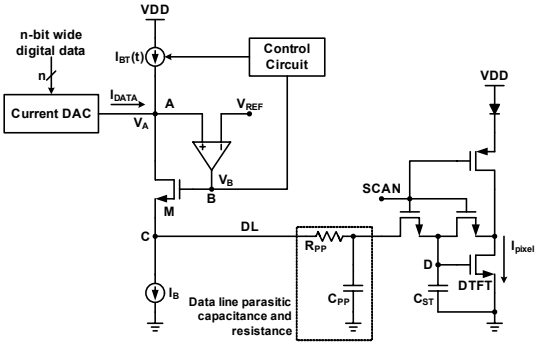
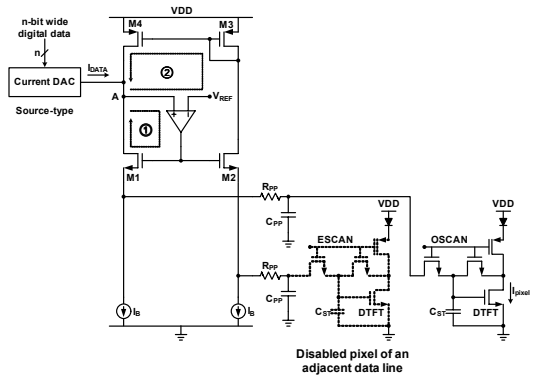
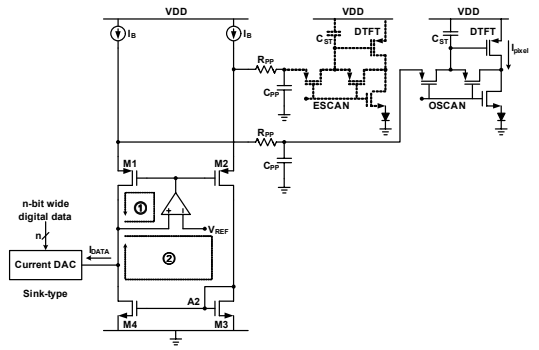


Figure 3. Conceptual operation of the transient cancellation feedback (TCF) driving method

The data line capacitance can be extracted from an adjacent data line, because the capacitance of a data line is almost the same as that of an adjacent data line. The adjacent data line provides the data line capacitance by disabling the SCAN signal, as shown in Figure 4.



(a) Source-type TCF circuit



(b) Sink-type TCF circuit

Figure 4. Implemented circuits for transient cancellation feedback driving

Equalization and pre-charge function define the initial voltage of the data line and its adjacent data line, as shown in Figure 5. Hence, the required transient charging current can be predicted from the current flowing in this adjacent data line, as shown in Figures 4 and 5.

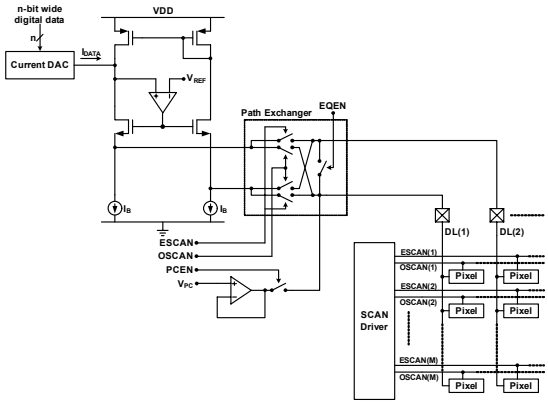


Figure 5. Application of the data driver to a display panel

The required quantity of charge for a data line is given in equation (1) and the quantity of generated charge from an adjacent data line is given in equation (2). The error charge, i.e., the difference between these two charge quantities, is given in equation (3). C_{PP} is the equivalent data line capacitance, C_{ST} is the storage capacitance of a pixel, and ΔV_{DL} is the voltage swing of a data line. The parasitic capacitance of a data line can be charged quickly as the error charge converges to zero by the operation of two feedback-loops. The loop ① monitors states of transferring I_{DATA} to Ipixel and generates a control voltage for the loop ②. The loop ② generates the transient charging current according to the control voltage. When the error charge converges to zero, the variation of voltage at node A no longer exists and I_{DATA} is transferred to I_{pixel} at the same time.

$$\Delta Q_{DL} = \left(C_{PP} + C_{ST}\right) \cdot \Delta V_{DL} \quad (1)$$

$$\Delta Q_{DDL} = C_{PP} \cdot \left(\Delta V_{DL} + V_{GS1} - V_{GS2}\right) \quad (2)$$

$$\Delta Q_{error} = C_{PP} \cdot \left(V_{GS2} - V_{GS1}\right) + C_{ST} \cdot \Delta V_{DL} \quad (3)$$

3. Panel Applications and Operation Timing Diagram

Figures 5 and 6 show the application of the proposed driving circuits and the operation timing diagram, respectively.

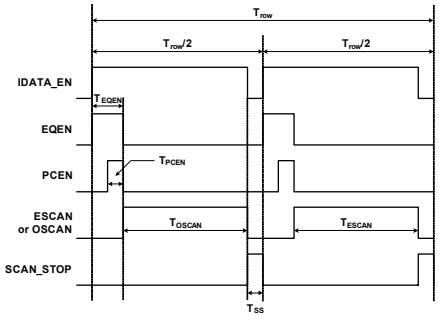
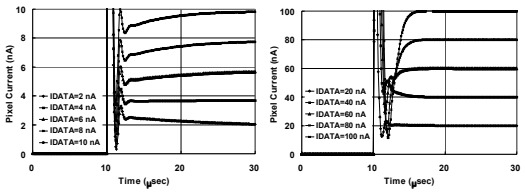


Figure 6. Operation timing diagram

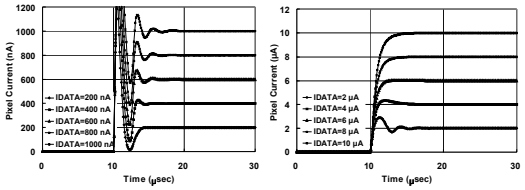
The path exchanger in Figure 5 enables one data driving circuit to drive two data lines by selecting the connection between a driving circuit and two data lines of a panel from ESCAN and OSCAN signals. The function of the path exchanger is advantageous in terms of chip size and current consumption. One complete scan time (T_{row}) is composed of ESCAN (T_{ESCAN}), OSCAN (T_{OSCAN}), two equalizations (T_{EQEN}), and two scan stops (T_{SS}), as shown in Figure 6. EQEN makes the average data line voltage of a data line and its adjacent data line while PCEN adjusts this average voltage if necessary. The functioning of EQEN and PCEN significantly shortens the data driving time.

4. Simulation Results

A distributed R-C model of 4 kohm resistance and 20 pF capacitance is applied as a data line load in order to evaluate the driving performance of the proposed driving method and circuit. The settling characteristics of the pixel currents in response to data currents from 2 nA to 10 μA are shown in Figure 7.



(a) 2 nA-step driving (b) 20 nA-step driving



(c) 200 nA-step driving (d) 2 μA-step driving

Figure 7. Step responses (SCAN enabled at 10 μsec)

The feasibility of nA-order data driving is verified from the simulation results. Figure 8 shows the error currents according to the data currents with the given data driving times.

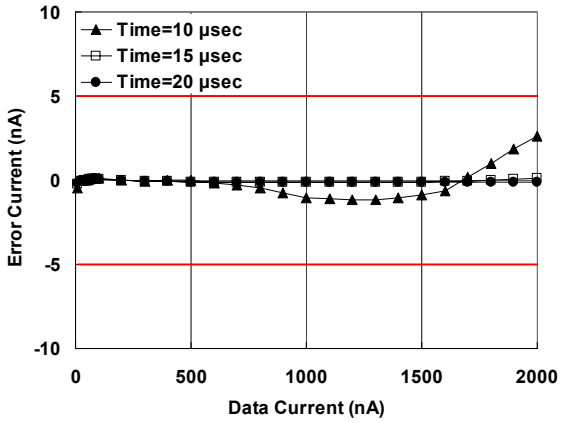
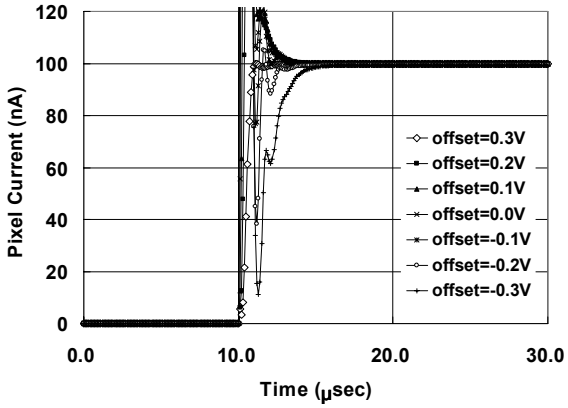
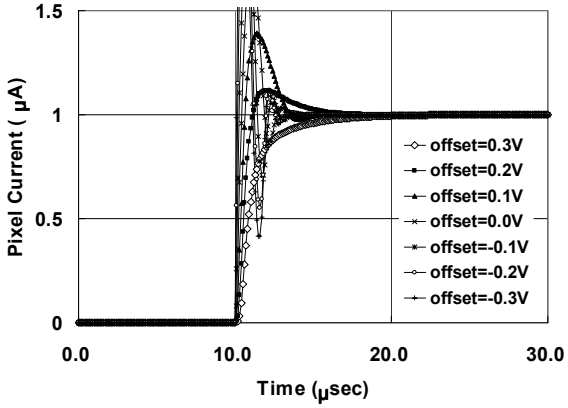


Figure 8. Current driving speed and accuracy according to data currents

The possibilities of 10 nA and several-nA data driving are verified from the results with 10 μsec and 15 μsec driving times, respectively. Figure 9 shows that the data driving time fluctuation is not significant even with ±300 mV threshold voltage (V_T) variations of DTFT in a pixel circuit.



(a) I_{DATA} = 100 nA



(b) I_{DATA} = 1 μA

Figure 9. Data driving performance with ±300 mV V_T variation (SCAN enabled at 10 μsec)

The performance of the proposed driving method and circuits are summarized in Table 1.

Table 1. Achieved specifications

Load conditions		
	DL resistance :	**2.2 kohm for QGVA** **3.7 kohm for VGA**
	DL capacitance :	**6.6 pF for QVGA** **13.5 pF for VGA**
Simulation load condition		
	DL resistance :	**4.0 kohm**
	DL capacitance :	**20 pF**
Driving speed and accuracy		
	10 µsec for ± 3 nA error current **15 µsec for ± 0.1nA error current**	
Current consumption		
	8 µA/channel effectively	

5. Conclusions

The retard of data driving speed in conventional current-mode driving methods due to the parasitic capacitance of a data line is overcome by TCF driving. The operation of this circuit is verified with a Cadence SPECTRE simulation. The proposed method maintains data driving speed and accuracy even with variation of TFTs and massive parasitic capacitance. One data driving circuit drives two data lines through the use of a path exchanger. The proposed approach can be applied for driving poly-silicon panels as well as a-Si panels. It is shown that the TCF driving method is a viable solution to the speed limitation of conventional current-mode driving methods.

7. References

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