

UNITED STATES PATENT AND TRADEMARK OFFICE
BEFORE THE PATENT TRIAL AND APPEAL BOARD

SAMSUNG ELECTRONICS CO., LTD, MICRON TECHNOLOGY, INC.,
MICRON SEMICONDUCTOR PRODUCTS, INC., and MICRON
TECHNOLOGY TEXAS LLC,¹
Petitioners,

v.

NETLIST, INC.,
Patent Owner.

Case No. IPR2022-00615
Patent No. 7,619,912 C1

PATENT OWNER'S REQUEST FOR DIRECTOR REVIEW

¹ Micron Technology, Inc., Micron Semiconductor Products, Inc., and Micron Technology Texas LLC filed a motion for joinder and a petition in IPR2023-00203 and have been joined as petitioners to this proceeding.

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Pursuant to 37 C.F.R. § 42.71(d) and the Revised Interim Director Review Process, Patent Owner Netlist, Inc., respectfully requests Director Review of the Board's Final Written Decision (Paper 96, "FWD"), in which the Board incorrectly concluded that claim 16 of U.S. Patent No. 7,619,912 C1 (EX1001, "the '912 patent") is unpatentable as obvious over the Ellsberry reference (EX1037).

I. INTRODUCTION

The Board's final written decision presents important issues of law and policy related to the recognition of priority dates for patents challenged in *inter partes* review. Director Review is necessary to clarify that the Board must consider evidence of how skilled artisans would understand priority-document disclosures, as well as to clarify evidentiary burdens in priority disputes.

The Board wrongly ignored the perspective of the person of ordinary skill in the art ("POSITA") at the time of invention when it denied claim 16 the benefit of U.S. Provisional 60/588,244's (EX1005, "the '244 provisional") priority date because that application does not expressly recite two specific words ("bank address") appearing in claim 16. This error fatally undermines the Board's obviousness determination, which rests *solely* on a subsequently filed, published, and abandoned patent application reference (Ellsberry). There is no dispute that if claim 16 is entitled to the July 15, 2004 priority date of the '244 provisional," Ellsberry does not qualify as prior art to claim 16 of the '912 patent.

Evidence of record demonstrates that a POSITA reading the '244 provisional would understand that the inventors had possession of the claimed invention, including the “bank address” signals required by the JEDEC-standardized memory modules and devices dominating the industry at that time. The Board acknowledged Netlist’s arguments to that effect but did not address—much less refute—Netlist’s cited evidence of the POSITA’s perspective. *See* FWD 29. Instead, the Board (1) noted that “[t]here is no [express] mention of ‘bank address’ signals in the '244 provisional”; (2) mischaracterized Netlist’s explanation and supporting evidence of how a POSITA would understand the '244 provisional disclosure as “a chain of inferences”; and (3) concluded without explanation that this purported chain of inferences was “too long and speculative” to support a priority claim. *Id.* at 29-30.

The Board’s erroneous rejection of claim 16’s entitlement to the '244 provisional’s filing date flows directly from multiple legal errors. For example, the Board ran afoul of binding Federal Circuit precedent that the written description requirement does not require priority applications to use the exact terms appearing in the claim *in haec verba*, *Blue Calypso, LLC v. Groupon, Inc.*, 815 F.3d 1331, 1345-46 (Fed. Cir. 2016), as well as the maxim that “[a] patent need not teach, and preferably omits, what is well known in the art” (MPEP §2164.01). Here, the “bank address” signals allegedly missing from the '244 provisional were indisputably well known in the art. Compounding these errors, the Board failed to provide the requisite

reasoned, legally sufficient, factually supported explanation for its conclusory determination. *See, e.g., In re Nuvasive, Inc.*, 842 F.3d 1376, 1383 (Fed. Cir. 2016) (requiring a “reasoned explanation” rather than “summariz[ing] and reject[ing] arguments without explaining why”).²

The Board made a similar mistake in rejecting claim 16’s entitlement to the March 2005 priority date of U.S. Patent No. 7,286,436 (EX1009, “the ’436 patent”), which also predates Ellsberry. Again, the Board placed undue emphasis on the lack of a verbatim recitation of a well-known concept (a “register”) in the disclosure. *See* FWD at 31. The ’436 patent discloses sequential logic, which according to Petitioner’s own expert normally includes at least one register to store state values. *See* EX2103 (Wolfe Dep. Tr.), 117:16-119:18. The Board nonetheless found that a POSITA would not have viewed the inventors as in possession of the “register” element based on speculation that other types of circuits allegedly *also* could have been used to store state values. FWD at 31; *see also id.* at 31 n.7 (compounding the error by relying on new evidence that the parties had no opportunity to address);

² Netlist reserves the right to challenge additional errors on appeal, including but not limited to the incorrect construction and application of the claim term “rank,” the misinterpretation of “printed publications” in 35 U.S.C. § 311(b), and the lack of substantial evidence to support the Board’s interpretation of the Ellsberry reference.

EX3021. The Board cites no authority and provides no explanation for why a POSITA's knowledge of these other structures negates an understanding that the inventors possessed the invention as claimed. The Board also erroneously concluded that the claimed circuit "comprising a logic element and a register" cannot be supported by a "logic element 646" that includes both a register and a separate logic function (i.e., the claimed "logic element") as argued by Netlist, and made no findings regarding the last element of the claim. FWD at 31-33.

Additionally, the Board faulted Netlist for "only address[ing] in its Response how the '436 patent allegedly provides written description support for 'each disputed limitation,' i.e., those raised by Petitioner." FWD at 33. That approach is at odds with the structure of IPR as well as other panel decisions. Director Review is warranted. The Board should not require Netlist to address issues not in dispute.

II. BACKGROUND

The Board's obviousness determination rests entirely on the Ellsberry reference. FWD at 55. As the Board acknowledged, Ellsberry was considered, but deemed not prior art, during the initial examination of the '912 patent; and it was disclosed in an IDS and considered during the decade-long reexamination and appeal process in which the Examiner, the Board, and the Federal Circuit confirmed the patentability of claim 16 at issue here without amendment. *See* Paper 20 at 8, 23.

Claim 16 relates to computer memory modules and recites, among other

things, a printed circuit board coupled to both a plurality of DDR memory devices arranged in ranks and a “circuit comprising a logic element and a register, the logic element receiving a set of input signals from the computer system, the set of input signals comprising at least one row/column address signal, *bank address* signals, and at least one chip-select signal.” EX1001, p.44 (3:9-43) (emphasis added). Petitioner contends that claim 16 is not adequately supported by the ’244 provisional based *solely* on the recited “bank address” signals. *See* Petition at 63 (arguing that the ’244 provisional “disclos[es] an ASIC Decoder, which could be a ‘*logic element*,’ but there is no disclosure it receives any ‘*bank address*’ signals”).

Netlist explained that a POSITA would understand—through the ’244 provisional’s use of terms characteristic of JEDEC-standardized memory modules and its association of “control signals” with memory commands (*e.g.*, EX1005, ¶¶ 5, 19), as well as the POSITA’s undisputed knowledge of contemporaneous JEDEC standards that specify the signals making up such commands (*see* Petition at 6)—that the “control signals” received by the decoder ASIC as expressly disclosed in Figure 1 and throughout the text of the ’244 provisional (*e.g.*, EX1001, Fig. 1, ¶¶ 5, 10-19, Table 1) would include bank address signals. *E.g.*, Paper 67 (POR), at 63-69; Paper 80 (Sur-Reply), at 22-24; EX2062 (Brogioli Decl.), ¶¶ 61-67.

For example, the ’244 provisional discloses memory modules having “ranks” of memory devices that receive chip-select signals. EX1005, ¶¶ 2, 4. “Rank” is a

JEDEC-coined term, and chip-select signals are essential to a JEDEC-style memory. POR 64, 67-68; EX2112; EX2062, ¶¶ 60, 67; EX1034, p.2. Petitioner does not dispute that, at the time of the '244 provisional and years before, “90% of DRAM production [was] in compliance with the [JEDEC DDRx] standards.” *Rambus Inc. v. FTC*, 522 F.3d 456, 459-61 (D.C. Cir. 2008); *accord* EX2103 (Wolfe Dep. Tr.), 72:7-73:2. Petitioner’s own expert agreed that references to a DRAM device “could include a [JEDEC] DDR or DDR2 device” in 2004 or 2005. EX2103, 73:9-15.

Significantly, Petitioner itself cites JEDEC specifications indicating that certain standardized commands necessarily *require* bank address signals. POR at 65; Petition at 42-43, EX1029 (JEDEC DDR2), p.49. Petitioner’s expert agreed that the module to which DDR2 devices are coupled would ordinarily receive a bank address control signal for read and write operations. EX2103, 69:1-10, 71:5-20. He also agreed that a POSITA would understand that “it would be ordinary for a personal computer to send ... bank address signals to the memory module for a read and write operation at the time of the invention.” *Id.* at 74:2-75:5.

Netlist also highlighted the '244 provisional’s express disclosure that “an address signal” is an example of a “control signal” used to generate additional chip-select signals when two smaller (i.e., lower density) DRAMs emulate a larger (i.e., higher density) DRAM. POR 69-70; EX1005, ¶ 5. This express disclosure, coupled with the knowledge that, for certain memory densities, a bank address signal would

serve to differentiate DRAMs of different densities, would mean to a POSITA that “bank address” is received as part of the control signals. POR 69-70; EX2062, ¶ 65.

The Board acknowledged—but did not specifically address—these arguments. *See* FWD at 26-27, 29. The Board also summarized additional arguments regarding, for example, certain types of data collisions. *Id.* at 28-29. But the Board’s one-paragraph analysis and conclusion relied on the lack of an express disclosures of “bank address” signals in the ’244 provisional and mischaracterized Netlist’s arguments and evidence as a series of inferences. *See id.* at 29-30. Three of the alleged “inferences” (Nos. 1, 2, and 4) appear straightforward based on the record evidence discussed above, including the POSITA’s understanding that the ’244 provisional pertains to DDR memory modules, that DDR-containing modules at the time would use bank address signals according to JEDEC standards, and that bank address signals would be included in the ’244 provisional control signals. Another alleged “inference” (No. 3) merely restates that the ’244 provisional does not expressly recite “bank address” signals. And the Board’s unwillingness to accept the last “inference” (No. 5) reflects a miscomprehension of facts: while row/column addresses may be used to differentiate DRAMs of certain density combinations, bank addresses are needed when two 512Mb DDR2 devices emulate a 1Gb DDR2 device. *See* POR 69-70. There is no evidence to the contrary. Thus, a POSITA would understand that bank address signals are received by the logic element to generate

the additional chip select signals, instead of being sent directly to DRAMs as Samsung suggests. Without any fact finding, the Board concluded that this purported “chain of inferences” was “too long and speculative” to demonstrate possession of the claimed invention. FWD at 30.

With respect to the ’436 patent, which independently provides support for a priority date that excludes Ellsberry as prior art, Petitioner alleged that it fails to disclose a “register.” *See* EX1001, p.44, 3:9-43 (claim 16) (reciting, among other things, “a circuit coupled to the printed circuit board ... comprising a logic element and a register”). The Board again focused on whether the specific term “register” appears in the ’436 patent, even though Petitioner’s expert acknowledged that sequential logic—words that do appear in the specification—normally would be understood to include a register to store state values. EX2103, 117:16–119:18. The Board based its finding on the assertion that registers are not the only structure that could store state values. The Board also misconstrued the term “circuit” by importing a limitation without explanation. Finally, the Board faulted Netlist for not specifically identifying support in the ’436 patent for undisputed claim elements.

III. ARGUMENT

A. The Board Legally Erred by Requiring an Express Disclosure of Specific Claim Language and Failing to Consider How a Skilled Artisan Would Understand the ’244 Provisional’s Disclosures

The Federal Circuit has repeatedly held that a patent document need not recite

the claimed invention verbatim to satisfy the written description requirement. *Ariad Pharms., Inc. v. Eli Lilly & Co.*, 598 F.3d 1336, 1352 (Fed. Cir. 2010) (en banc) (specification need not recite claimed invention *in haec verba*). The Board acknowledged this binding precedent but nonetheless placed undue emphasis on the omission of the specific term “bank address” signals in the ’244 provisional and “register” in the ’436 patent, ignoring the fact that both were well-known features for standard memory modules at the time. *See* FWD at 29, 31-32; *see also Blue Calypso*, 815 F.3d at 1345 (expressing concern that “the Board did not cite any evidence other than the fact that the terms were not present in the specification”).

A proper analysis would have determined “whether the disclosure of the [’244 provisional] reasonably conveys to those skilled in the art that the inventor had possession of the claimed subject matter as of the filing date.” *Ariad*, 598 F.3d at 1351. This analysis is not limited to a lay understanding of the disclosures. After all, “the patent specification is written for a person of skill in the art, and such a person comes to the patent with the knowledge of what has come before.” *LizardTech, Inc. v. Earth Res. Mapping, Inc.*, 424 F.3d 1336, 1345 (Fed. Cir. 2005). For that reason, “it is unnecessary to spell out every detail of the invention in the specification.” *Id.*

The Board should have determined—but did not—whether a POSITA would understand the ’244 provisional disclosure to encompass JEDEC-standardized memory modules and devices, which the parties agree require “bank address”

signals, and which the parties likewise agree were well-known in the art. “[A] patentee may rely on information that is well-known in the art to the extent it informs how a relevant artisan would reasonably understand what is actually described in the specification.” *BASF Plant Sci., LP v. Commonwealth Sci. & Indus. Rsch. Org.*, 28 F.4th 1247, 1264 (Fed. Cir. 2022) (internal quotation marks omitted). Indeed, a patent document “need not teach, and preferably omits, what is well known in the art.” *Spectra-Physics, Inc. v. Coherent, Inc.*, 827 F.2d 1524, 1534 (Fed. Cir. 1987); *accord In re Howarth*, 654 F.2d 103, 105 (C.C.P.A. 1981) (“An inventor need not, however, explain every detail since he is speaking to those skilled in the art. What is conventional knowledge will be read into the disclosure.”); *Hologic, Inc. v. Smith & Nephew, Inc.*, 884 F.3d 1357, 1361 (Fed. Cir. 2018) (for predictable arts, “a lower level of detail is required”).

Here, the Board improperly rejected the possibility that a POSITA would understand the ’244 provisional disclosure to convey possession of a logic element that receives “bank address” signals because it did not first determine whether the POSITA would understand that the ’244 provisional disclosure encompassed JEDEC-standardized DDR and DDR2 SDRAM memory devices and JEDEC-standardized memory modules. The Board should have considered the teachings of those JEDEC specifications, particularly because Petitioner itself contends that the POSITA “would have been knowledgeable about the JEDEC DDR (EX1030;

EX1031) and DDR2 (EX1029; EX1039) SDRAM standards ... and the JEDEC 21-C (EX1032; EX1040) standard,” which pertains to memory modules. Petition at 6. Accordingly, these standards reflect knowledge that a POSITA “would clearly have possessed,” and “satisfaction of the written description requirement does not require either the recitation or incorporation by reference” of the well-known bank address signals. *Falko-Gunter Falkner v. Inglis*, 448 F.3d 1357, 1365, 1368 (Fed. Cir. 2006).

Viewed through the proper legal lens of the POSITA’s understanding, the supposed “long and speculative” chain of inferences collapses to a simple question: whether—consistent with the overwhelming evidence described above—a POSITA would understand the ’244 provisional to encompass JEDEC-standardized DDR and DDR2 memory devices and modules. If so, a POSITA would understand that the control signals received for the disclosed memory commands (such as “activation, read, write, precharge, and refresh,” EX1005, ¶ 19) would necessarily include “bank address” signals received by the logic, e.g., to create additional chip select signals for certain JEDEC-specified memory densities and commands. *See, e.g.*, POR at 65; Sur-Reply at 23-24; Petition at 42-43, EX1029, pp. 6, 49; EX1030, p.7; EX2062, ¶¶ 62-64; EX2103, 69:1-10, 71:5-20; EX1005, ¶¶ 5, 19. Ellsberry is not prior art.

B. The Board Made Similar Mistakes in Rejecting Claim 16’s Entitlement to the ’436 Patent’s Priority Date

When analyzing whether claim 16 is independently supported by the

disclosures of the '436 patent, the Board likewise improperly focused on whether the '436 patent expressly discloses a “register.” But the '436 patent expressly discloses sequential logic, which Petitioner’s expert acknowledged “normally” would be understood by a POSITA to include registers. EX2103, 117:16-21; *see also id.*, 118:16-20 (to perform sequential logic, “you would need both state storage in the form of a register or equivalent, plus ... combinatorial logic functions”), 119:14-18 (a POSITA would have understood what sequential logic describes).

The Board nevertheless concluded, based on its assertion that other electrical elements could also store states, that a POSITA would not have understood the inventors to possess a circuit that comprised a logic element and a register. FWD at 30-31. To support that conclusion, the Board improperly relied in part on evidence that appeared nowhere in the parties’ submissions and that the parties were never given the opportunity to address. FWD at 31 n.7 (citing EX3021); *Genzyme Therapeutic Prod. Ltd. P’ship v. Biomarin Pharm. Inc.*, 825 F.3d 1360, 1366 (Fed. Cir. 2016) (introduction of new evidence requires “notice of the evidence and an opportunity to respond to it” under the APA). But even if such new evidence were appropriate, the question is whether a POSITA would have understood that the inventors were in possession of an invention that uses a circuit comprising both a logic element and a register. That Dr. Wolfe later hedged that sequential logic could involve “a register *or equivalent*” (EX2103, 118:16-20) does not negate the fact that

a POSITA would understand that sequential logic “[n]ormally ... describes a combination of logic functions [i.e., logic elements] and registers.” *Id.*, 117:16-21. At bottom, the undisputed evidence demonstrates that a POSITA would have understood the ’436 patent’s disclosure of sequential logic to include possession of the claimed “register” structure, which satisfies the written description requirement. *See Hologic*, 884 F.3d at 1364 (holding that an application reasonably conveyed possession of a claimed feature to a POSITA despite not being “necessarily” included in the disclosed structure).

The Board further erred by effectively reading a “separate and distinct” limitation into claim 16. Specifically, the Board determined that a circuit that “comprises a logic element and a register” means that the logic element and register must be “two different things.” FWD at 31-32. Thus, the Board concluded that even if ’436 patent “implies the existence of a register,” that register could not satisfy the written description requirement because it would be “part of” the logic element. *Id.* The Board provides no justification for this claim construction, which runs counter to precedent. *See Linear Tech. Corp. v. ITC*, 566 F.3d 1049, 1055 (Fed. Cir. 2009) (affirming construction of “second circuit” and “third circuit” to not require entirely separate and distinct circuits and holding that “the ... circuits must only perform their stated functions”). Moreover, sequential logic would include separate logic functions (logic elements) and registers, as Dr. Wolfe testified. EX2103, 117:16-21.

C. Director Review Is Necessary to Ensure Consistent, Legally Sound, and Adequately Supported Application of the Priority Analysis

The Board's final written decision in this case reflects erroneous conclusions of law regarding the written description requirement that led to an erroneous finding of material fact regarding the priority date. The Board also failed to make adequate supporting fact findings or provide a reasoned explanation for its conclusion. These errors implicate important issues of law and policy that warrant Director Review. The Board's errors and conclusory reasoning are particularly egregious in view of the rigorous patentability vetting already applied to claim 16 of the '912 patent.

D. Director Review Is Also Necessary to Clarify the Patent Owner's Burden of Production When a Petitioner Challenges Priority

The Board's allocation of evidentiary burdens in the priority context presents another issue meriting Director Review to resolve inconsistent panel decisions. *See, e.g., Continental Auto. Sys., Inc. v. Intellectual Ventures II LLC*, IPR2022-00972, Paper 49, at 24-25 (PTAB Dec. 5, 2023) (requiring patent owner to identify written description support in only the single disputed claim element). Here, the Board faulted Netlist for not showing how the '436 patent provides support for *each and every* element of claim 16, even those not in dispute. FWD at 33-34. The Board cited *Tech. Licensing Corp. v. Videotek, Inc.*, 545 F.3d 1316 (Fed. Cir. 2008), but that reliance was misplaced, as the court focused only on the disputed limitation.

Requiring patent owners to address every element of every challenged claim

is neither equitable nor efficient, particularly in view of the limited briefing and narrow scope of *inter partes* review proceedings. That approach requires patent owners to address issues in the first instance for which petitioners bear the burden of persuasion. It also facilitates unnecessary sandbagging, as petitioners can identify a single (or even no) allegedly unsupported claim term in their petition and reserve additional arguments for reply. Consequently, some panels have held that patent owners need only respond “commensurate in scope” to the “specific points and contentions” made by petitioners regarding priority for the challenged claims. *Lupin Ltd. v. Pozen, Inc.*, IPR2015-01775, Paper 15, at 10-11 (PTAB Mar. 1, 2016); *accord Focal Therapeutics, Inc. v. SenoRx, Inc.* IPR2014-00116, Paper 8 at 9-10 (PTAB Apr. 22, 2014); *Fitbit, Inc. v. BodyMedia, Inc.*, IPR2016-00707, Paper 9 at 10-11 (PTAB Sep. 8, 2016). Director Review provides an opportunity to resolve these panel splits and clarify the extent of patent owners’ burden of production.

IV. CONCLUSION

For these reasons, the Director should grant review and reverse the Board’s final written decision finding claim 16 unpatentable as obvious over Ellsberry.

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Respectfully submitted,

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CERTIFICATE OF SERVICE

I hereby certify, pursuant to 37 C.F.R. § 42.6, that on May 17, 2024, a complete copy of **PATENT OWNER'S REQUEST FOR DIRECTOR REVIEW** was served upon the following, by ELECTRONIC MAIL:

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