UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

LITE-ON TECHNOLOGY CORPORATION,
Petitioner,

v.

SENSOR ELECTRONIC TECHNOLOGY, INC.,
Patent Owner

IPR2022-00780
U.S. Patent No. 9,923,117

PETITION FOR *INTER PARTES* REVIEW OF U.S. PATENT NO. 9,923,117

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EXHIBIT LIST

Exhibit No.	Description
Exhibit 1001	U.S. Patent No. 9,923,117 to Shatalov et al., filed on December 30, 2015, and issued on March 20, 2018 (the "**'117 Patent**").
Exhibit 1002	Declaration of James Richard Shealy, Ph.D.
Exhibit 1003	Curriculum Vitae of James Richard Shealy, Ph.D.
Exhibit 1004	U.S. Patent Application Publication No. 2007/0085093 to Ohmae *et al*. ("**Ohmae**")
Exhibit 1005	Japan Patent No. 2000-22283 to Ban *et al*. ("**Ban**")
Exhibit 1006	W.O. Publication No. 2013/023197 to Shur *et al*. ("**Shur**")
Exhibit 1007	U.S. Patent Application Publication No. 2004/0031956 to Saxler ("**Saxler**")
Exhibit 1008	U.S. Patent No. 6,478,871
Exhibit 1009	Phase separation and ordering in InGaN alloys grown by molecular beam epitaxy
Exhibit 1010	Growth kinetics of AlGaN films by plasma-assisted molecular-beam epitaxy
Exhibit 1011	Phase Separation and Atomic Ordering in AlGaInN Alloys
Exhibit 1012	Nitride-based semiconductors for blue and green light-emitting devices
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Exhibit 1014	Alloy scattering in ternary III-V compounds

Exhibit No.	Description
Exhibit 1015	Epitaxial Lateral Overgrowth Techniques Used In Group III Nitride Epitaxy
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Exhibit 1017	Electrical and structure properties of AlGaN: a comparison with CVD diamond by Stutzmann ("**Stutzmann**")
Exhibit 1018	File History for the '117 Patent
Exhibit 1019	U.S. Patent No. 6,201,262
Exhibit 1020	Agreed Motion for Extension of time for Defendants to Respond to Plaintiff's Complaint
Exhibit 1021	Patent Owner's Cover Pleading to its Infringement Contentions (July 27, 2021)
Exhibit 1022	Defendants' Answer and Counterclaims

I. MANDATORY NOTICES

A. Real Party-In-Interest (37 C.F.R. §42.8(b)(1))

Petitioner Lite-On Technology Corporation ("Lite-On") is a real party-in-interest. Petitioner also identifies Lite-On Technology USA, Inc., Lite-On, Inc., and Lite-On Trading USA, Inc. as real parties-in-interest because Lite-On Technology USA, Inc. is a wholly owned subsidiary of Lite-On Technology Corporation, and Lite-On, Inc. and Lite-On Trading USA, Inc. are wholly owned subsidiaries of Lite-On Technology USA, Inc. These entities are also identified because they are defendants in the related district court litigation discussed below.

B. Identification of Related Matters (37 C.F.R. §42.8(b)(2))

Patent Owner has asserted U.S. Patent No. 9,923,117 (the "'117 Patent") along with other patents against the above-identified real parties-in-interest in a co-pending litigation, *Sensor Electronic Technology, Inc. v. Lite-On Technology Corporation et al.*, No. 6:21-cv-322-ADA (W.D. Tex.) ("Texas Action"). Petitioner waived service of the original complaint in the Texas Action on April 14, 2021, and the above-identified subsidiaries (direct and indirect) of Petitioner were served with the original complaint on April 8, 2021. Ex[1020]. Patent Owner has asserted Claim 1 of the '117 Patent against the above-identified real parties-in-interest. Ex[1021].

Petitioner has also asserted U.S. Patent Nos. 10,916,685 (the "'685 Patent"), 8,829,549 (the "'549 Patent"), 8,587,013 (the "'013 Patent"), 8,872,202 (the "'202 Patent"), and RE47,088 (the "'088 Patent") against Patent Owner in the Texas Action. Ex[1022]. Patent Owner has filed petitions for *inter partes* review against those patents under the following case numbers:

- '685 Patent (IPR2022-00395);
- '549 Patent (IPR2022-00396);
- '013 Patent (IPR2022-00397);
- '202 Patent (IPR2022-00406); and
- '088 Patent (IPR2022-00419).

C. Counsel and Service Information (37 C.F.R. §§42.8(b)(3) & (b)(4))

Petitioner designates the following Lead and Backup Counsel. Concurrently filed with this Petition is a Power of Attorney for appointing the following Lead and Backup Counsel, per 37 C.F.R. § 42.10(b). Service via hand-delivery may be made at the postal mailing addresses below. Petitioner consents to electronic service by e-mail at the following address: **lite-on_117ipr@pillsburylaw.com**.

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D. Payment of Fees (37 C.F.R. §42.103)

Petitioner authorizes the Patent and Trademark Office to charge Deposit Account No. 033975 for the petition fee and for any other required fees.

II. INTRODUCTION

Petitioner Lite-On hereby petitions to institute *inter partes* review ("IPR") of Claim 1 of U.S. Patent No. 9,923,117 (the "'117 Patent") (Ex[1001]), and to cancel that claim as unpatentable under 35 U.S.C. § 103.

The prior art references presented in this Petition—Ohmae (Ex[1004]), Ban (Ex[1005]), Shur (Ex[1006]), and Saxler (Ex[1007])—disclose light-emitting diode ("LED") structures with inhomogeneous regions, as recited by Claim 1. The invalidity grounds herein therefore establish that Claim 1 of the '117 Patent would have been obvious to a person of ordinary skill in the art ("POSITA") before the date of the alleged invention in February 2013. Accordingly, Claim 1 of the '117 Patent is invalid under 35 U.S.C. § 103 and should be cancelled.

III. STATEMENT OF PRECISE RELIEF REQUESTED FOR EACH CHALLENGED CLAIM

A. Claims for Which Review Is Requested

Petitioner respectfully requests review of Claim 1 of the '117 Patent pursuant to 37 C.F.R. § 42.300 and cancellation of that claim as unpatentable. Petitioner certifies that it is not barred or estopped from requesting IPR on the identified grounds, including under any of 35 U.S.C. §§ 315(e) or 325(e) or 37 C.F.R. § 42.302(b) or (c).

B. Statutory Grounds of Challenge

Claim 1 of the '117 Patent is unpatentable under 35 U.S.C. § 103 because it is obvious, as shown in the grounds below.

Ground	Invalidity	Exhibit
1	Claim 1 is rendered obvious over Ohmae (Ex[1004]) in view of the knowledge of a POSITA under 35 U.S.C. § 103.	**1004**
2	Claim 1 is rendered obvious over Ban (Ex[1005]) in view of the knowledge of a POSITA under 35 U.S.C. § 103.	**1005**
3	Claim 1 is rendered obvious over Shur (Ex[1006]) in view of the knowledge of a POSITA under 35 U.S.C. § 103.	**1006**
4	Claim 1 is rendered obvious over Saxler (Ex[1007]) in view of the knowledge of a POSITA under 35 U.S.C. § 103.	**1007**

Petitioner's invalidity grounds are supported by the Declaration of Dr. James Richard Shealy, a Professor in the School of Electrical and Computer Engineering at Cornell University. Ex[1002], ¶¶1, 6-8. Dr. Shealy has "been involved in the science and engineering of light emitting diodes ('LEDs') and high-power compound semiconductor resistors for over 40 years." *Id*. at ¶6. He joined the faculty at Cornell in 1987 and was promoted to full professor in 1998. *Id*. ¶¶6-18.

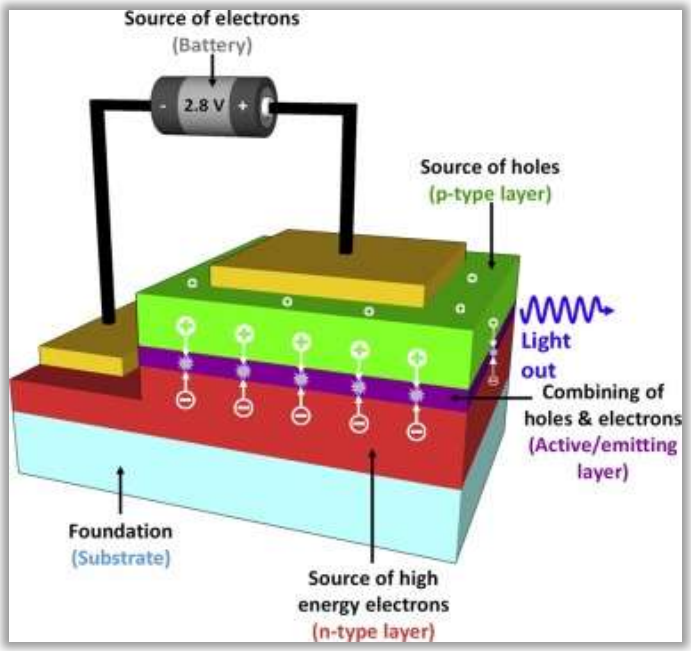
IV. OVERVIEW OF THE STATE OF THE ART

The '117 Patent concerns LED structures with inhomogeneous regions. Ex[1001], '117 Patent, at Title, 2:4-5; Ex[1002], Dr. Shealy Decl., ¶¶36-39. This was nothing new in the art. *See generally* Ex[1002], ¶¶44-52.

A. Background of LED Technology

A light-emitting diode, or an LED, is a semiconductor-based light source that emits light when current flows through it. *Id*. at ¶44. An LED is comprised of "a p-n junction diode having a p-type region (positive terminal) and an n-type region (negative terminal)." *Id*. A p-type region of a semiconductor has a larger concentration of holes than electrons, whereas an n-type region of a semiconductor has a larger concentration of electrons than holes. *Id*.

As shown in the graphic below, when voltage is applied across the terminals of the LED (the terminals shown as yellow structures to the right), electrons (formed in the conduction band of the semiconductor, shown in red) recombine with holes (formed in the valence band of the semiconductor, shown in green) to release photons (the purple light wave). *Id*. "This recombination process, often referred to as electroluminescence, is how an LED generates and emits light." *Id*.



Prior to the filing of the provisional application for the '117 Patent on

February 25, 2013, "alloy group III-Nitride or gallium nitride (GaN) based materials, such as GaN, InGaN, and AlGaN, were well known and have been used for years in the design and development of" LEDs. *Id*. at ¶45 (citing Ex[1009]-Ex[1013]). All semiconductor materials have a "band gap" relating to the difference in energy between the valence band and the conduction band of a semiconductor material. *Id*. at ¶46. Therefore, "all GaN based semiconductors (*e.g.*, AlGaN, GaN) have a band gap as an inherent property of the material." *Id*.

B. Inhomogeneous Regions

Compound semiconductor materials have been synthesized using a variety of methods since the 1960s. *Id*. at ¶47. "For GaN based semiconductor materials having at least three chemical elements (*e.g.*, InGaN or AlGaN), the distribution of metal atoms (*e.g.*, In, Al, Ga) within the crystal structure of the material during growth of the semiconductor layer can vary, including randomly, leading to compositional fluctuations, which are sometimes referred to as inhomogeneities, across the lateral dimension (the direction parallel to the surface of the substrate)." *Id*. at ¶49 (citing Ex[1009]). For example, in a single layer of AlGaN, there may inherently be more Ga atoms than Al atoms at one location and more Al atoms than Ga atoms at another location within the semiconductor layer due to random ordering. *Id*. (citing Ex[1013]). "This inherent, compositional fluctuation of the

GaN based semiconductor alloys can lead to inhomogeneous regions in the semiconductor layer, and the phenomenon was well known before the invention of the '117 Patent." *Id*.

For instance, it has been known since at least the 1970s that compound semiconductor materials have lateral inhomogeneities caused by lateral changes or differences in the composition of the semiconductor material. *Id*. at ¶¶47-48. "The random distribution of the alloy's components gives rise to an electron scattering mechanism caused by the local (and lateral) changes in the semiconductor bandgap." *Id*. at ¶47.

"The random distribution of the alloy's components is native to the epitaxial processes used to form the semiconductor materials." *Id*. at ¶48. This is described in the '117 Patent as well: "Ternary and quaternary nitride semiconductor epitaxial layers inherently grow inhomogeneously due to contrasting optimum growth conditions needed for respective binary layers." Ex[1001],18:15-18 (emphasis added); Ex[1002], ¶48. In other words, it was clear to a POSITA that growth of compound semiconductor alloys will necessarily result in compositional fluctuations and inhomogeneous regions within the semiconductor layer. Ex[1002], ¶48. Accordingly, the '117 Patent did not invent inhomogeneous regions in a GaN-based semiconductor because the ability to include

inhomogeneous regions in a semiconductor layer was already well-known. *Id*. at ¶48.

C. Epitaxial Lateral Overgrowth

A POSITA would have understood that epitaxial lateral overgrowth ("ELO") techniques could also be used to create inhomogeneous regions. *Id*. at ¶51. ELO of GaN and AlGaN materials dates to the early 2000s. *Id*. For example, in a 2001 review article, "lateral inhomogeneous regions are known to appear from the laterally patterned ELO mask (*e.g.*, silicon dioxide) itself and from the distribution of threading dislocations in the GaN above the mask which are often concentrated above the openings in the patterned masking layer." *Id*. (citing Ex[1015]). "ELO predates the '117 Patent by over a decade and ELO produces the inhomogeneous regions." *Id*. at ¶52 (citing Ex[1016]).

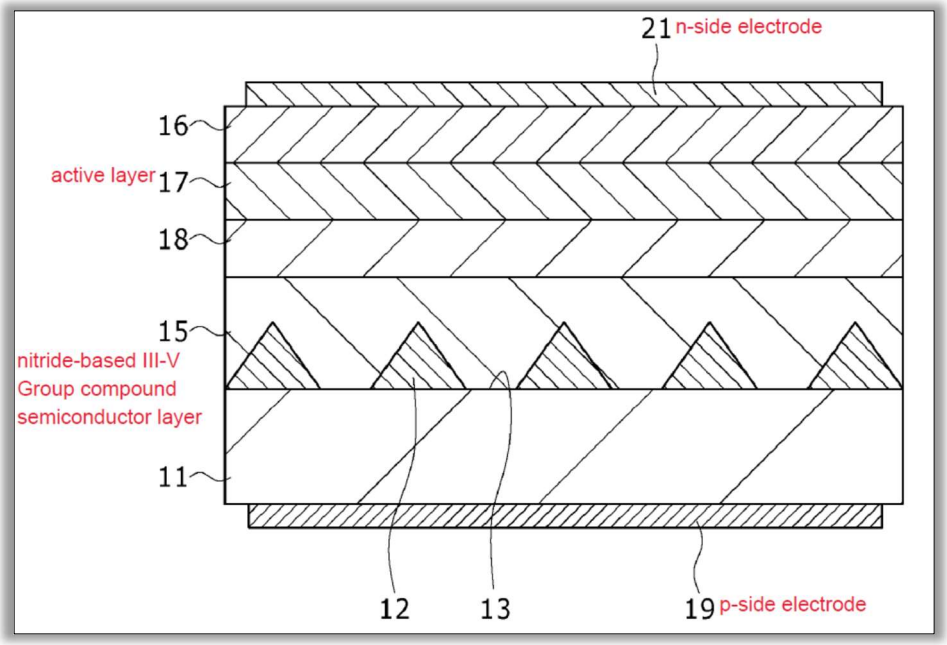
In fact, the '117 Patent recognizes that it was known that ELO can be used to form inhomogeneous regions: "Aspects of the invention provide a semiconductor structure. . . . The semiconductor structure can include inhomogeneous regions formed by one or more of patterning, masking, epitaxial growth, epitaxial overgrowth, deposition techniques, and/or the like." Ex[1001], 4:4-14 (emphasis added); Ex[1002], ¶50.

D. U.S. Patent Application Publication No. 2007/0085093 to Ohmae et al. ("Ohmae") (Ex[1004])

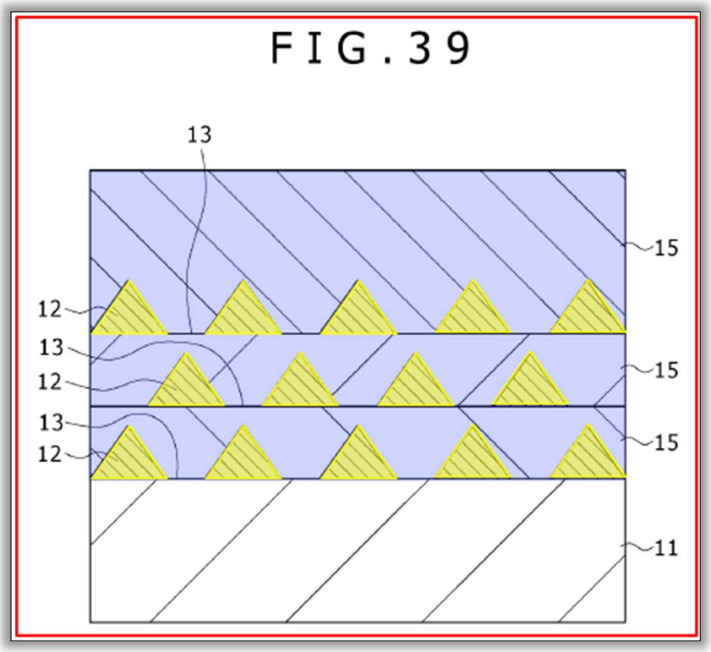
Ohmae is a U.S. patent application filed by Sony Corporation that was published on April 19, 2007. Ex[1004]. Ohmae is therefore prior art to the '117 Patent under at least pre-AIA 35 U.S.C. § 102(b).[1]

Ohmae discloses inhomogeneous regions in a LED structure. In particular, Ohmae concerns a "method for manufacturing a light-emitting diode." Ex[1004], Abstract. Ohmae's light-emitting diode includes a "nitride-based III-V Group compound semiconductor layer 15," "an active layer 17," and "a p-side electrode 19." *Id.* at ¶[0231]. As shown in annotated Figure 35, below, the nitride-based III-V Group compound semiconductor layer 15 is located between the active layer 17 and the p-side electrode 19.

[1] The '117 Patent claims priority to a provisional application filed on February 25, 2013, which would render the effective filing date before the March 16, 2013 cut-off for the application of AIA 35 U.S.C. §§102 and 103. *See* 35 U.S.C. §100(i)(1)(B).



Ohmae also teaches "forming protruded portions 12 on the substrate 11, followed by repeating the step plural times" and "the protruded portions in the respective layers are formed at positions that are mutually shifted by a half cycle within planes parallel to the main surface of the substrate 11." *Id.* at ¶[0247]. Figure 39, reproduced and annotated below, shows a plurality of yellow protruded portions 12 ("inhomogeneous regions") arranged within multiple levels of the blue semiconductor layer 15 along a height direction of the semiconductor layer 15:



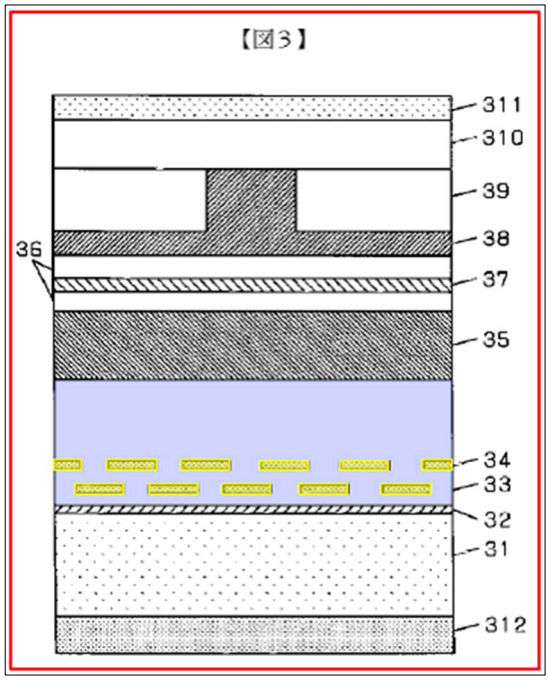
E. Japanese Patent App. Pub. 2000-22283 to Ban ("Ban") (Ex[1005])

Ban is a Japanese Patent Application filed by Panasonic Corporation that was published on January 21, 2000. Ex[1005].[2] Ban is therefore prior art to the '117 Patent under at least pre-AIA 35 U.S.C. § 102(b).

Ban also discloses inhomogeneous regions in an LED structure. Ban teaches a "semiconductor device used in a light emitting element." Ex[1005], ¶[0001]. The structure of the semiconductor laser device includes an n-type GaN layer 33, a SiO_2 mask layer 34, a GaInN quantum well active layer 37, and a Ni/Au layer 312

[2] Ex[1005] includes Ban, a certified English translation of Ban, and the translator's affidavit.

formed on the back surface of the substrate. *Id.* at ¶[0042]. Furthermore, multiple layers of the SiO_2 mask layer 34 are grown with the mask shifted between the first layer and the second layer. *Id.* at ¶[0046]. The result is the blue-colored n-type GaN layer 33 ("semiconductor layer") including a plurality of yellow-colored SiO_2 mask layers 34 ("inhomogeneous regions") arranged within multiple levels of the semiconductor layer along a height direction of the semiconductor layer, shown in annotated Figure 3 below.

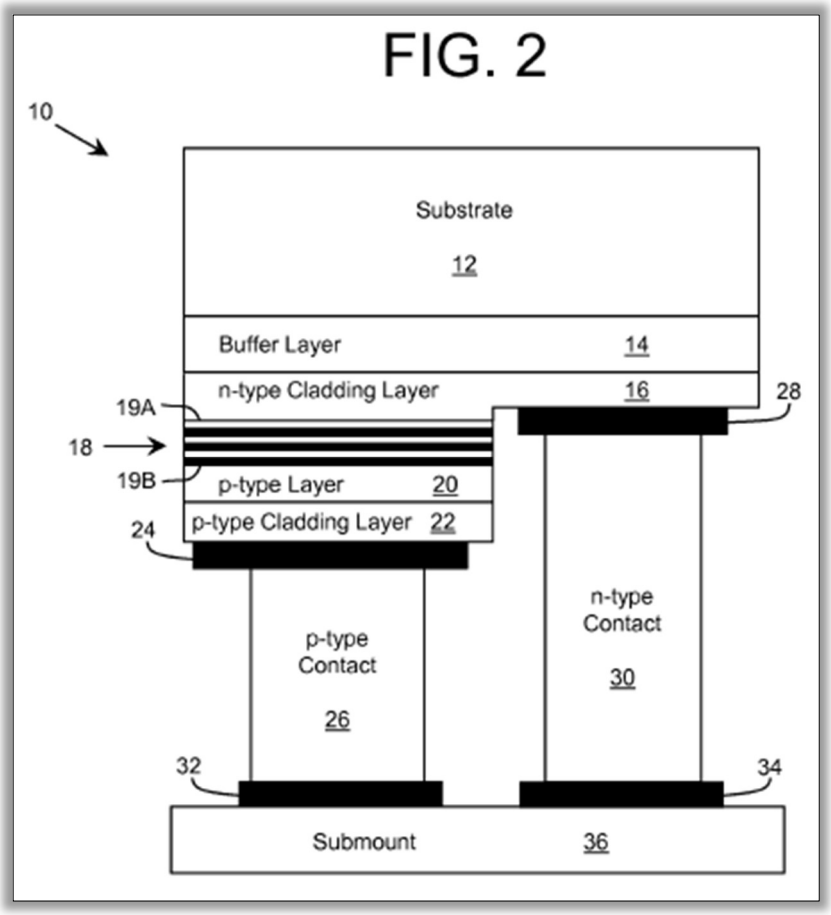


F. W.O. Pub. No. 2013/023197 to Shur ("Shur") (Ex[1006])

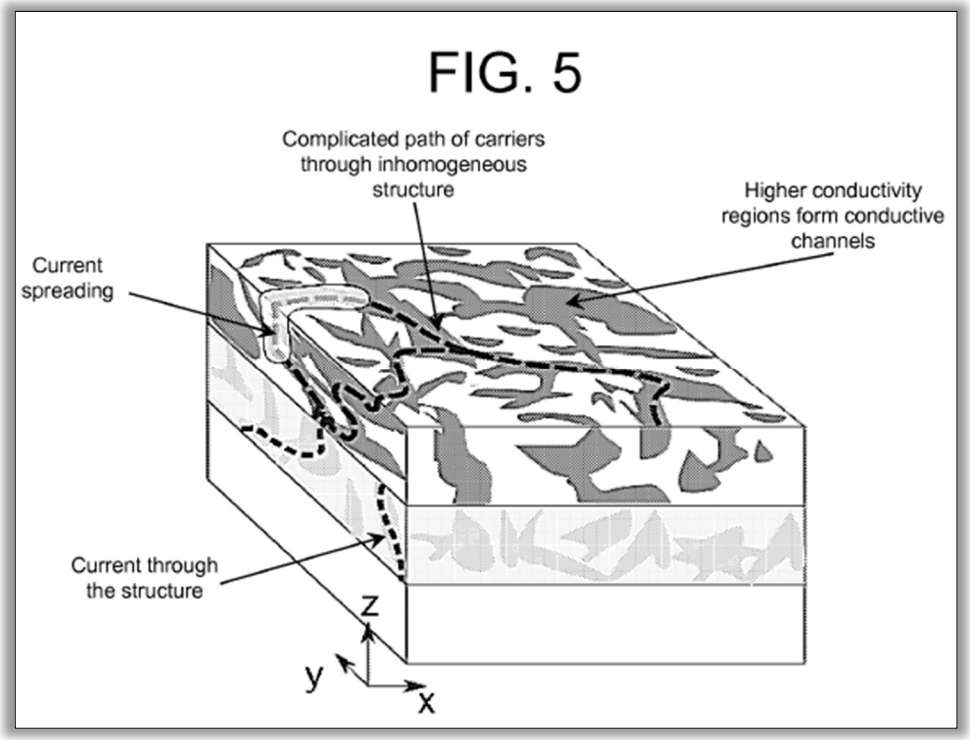
Shur is an international WIPO application filed by Patent Owner that was published on February 14, 2013 (i.e., 11 days before the earliest date of invention for the '117 Patent of February 25, 2013). *See* Ex[1006]. Shur is therefore prior

art to the '117 Patent under at least pre-AIA 35 U.S.C. § 102(a).

Shur discloses "an emitting device." Ex[1006], ¶[0002]. The emitting device 10 of Shur includes a heterostructure comprising a substrate 12, an active region 18, a p-type cladding layer 22, and a p-side metal 24. *Id.* at ¶¶[0033], [0036]. The p-type cladding layer 22 also comprises a magnesium-doped AlGaN/AlGaN short period superlattice structure (SPSL). *Id.* at ¶[0036]. The emitting device configuration is shown in Figure 2 below:



The layer 22 of Shur includes inhomogeneous regions. *Id.* at ¶[0054]. Figure 5, below, shows a schematic representation of the inhomogeneous regions within layer 22:

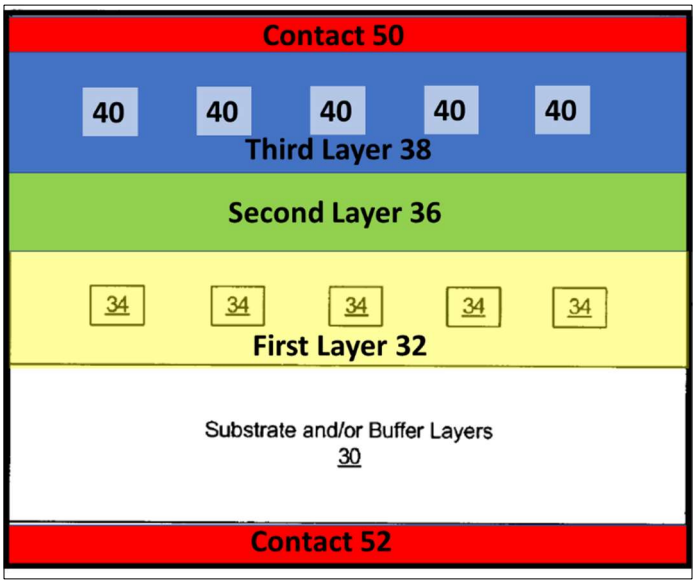


G. U.S. Patent Application Publication No. 2004/0031956 to Saxler ("Saxler") (Ex[1007])

Saxler is a U.S. patent application filed by Cree Inc. that was published on February 19, 2004. Ex[1007]. Saxler is therefore prior art to the '117 Patent under at least pre-AIA 35 U.S.C. § 102(b).

Saxler discloses a "Group III nitride based semiconductor structure." Ex[1007] at ¶[0016]. The semiconductor structure includes, *e.g.*, a vertical diode

structure as depicted in Figure 4, comprising a quantum well layer 36, a third layer 38 and contact 50. *Id.* at ¶[0026]. Annotated FIG. 4 of Saxler, below, shows a group III nitride semiconductor layer (first layer 32 or third layer 38) located between the active region (layer 36, as shown in green) and the metallic contact (contact 50 or contact 52, as shown in red).

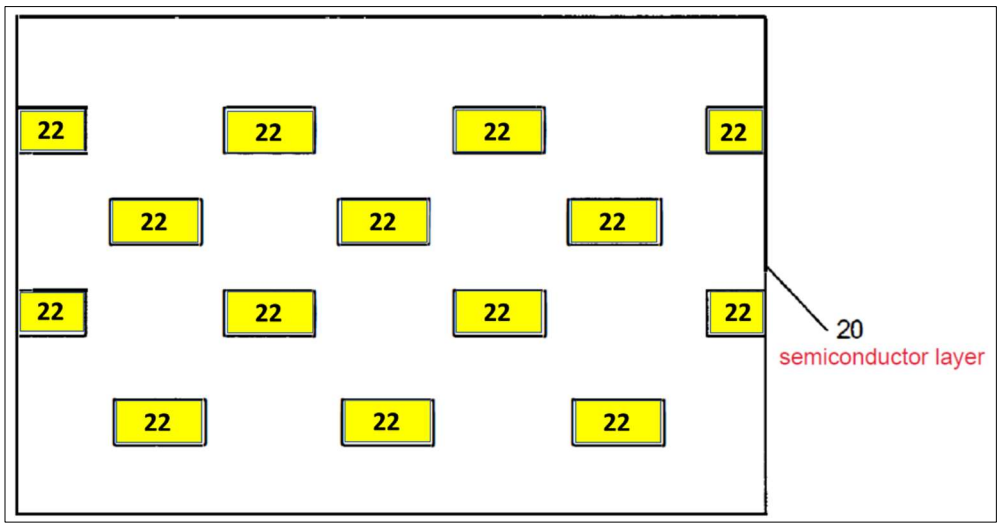


(Annotated FIG. 4 of Saxler)

As shown above, Figure 4 shows that the third layer 38 of the diode structure can include multiple regions 40 embedded therein. Furthermore, Saxler teaches that the nitride-based III-V compound semiconductor layer (*e.g.*, layer 20) can include "multiple courses of regions 22" that are embedded within the same semiconductor layer. *Id.* at ¶[0021].

Annotated FIG. 3 of Saxler, below, shows that the semiconductor layer 20

includes a plurality of inhomogeneous regions (the regions 22 are shown in yellow) arranged within multiple levels of the semiconductor layer (layer 20) along a height direction (vertical direction) of the semiconductor layer.



(Annotated FIG. 3 of Saxler)

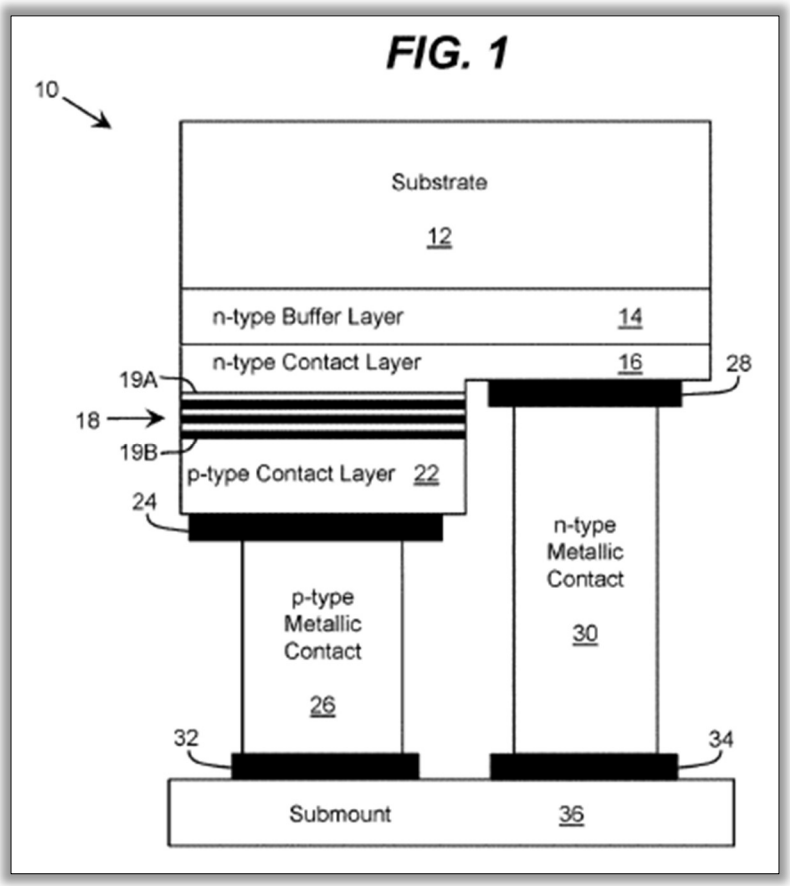
V. THE '117 PATENT

The '117 Patent acknowledges that conventional LEDs are composed of semiconductor layers. Ex[1001], 1:38. Each semiconductor layer has a particular combination of molar fractions for the various chemical elements, which influences the optical properties of the semiconductor layer. *Id.* at 1:24-28. Specifically, a refractive index and absorption characteristics of a semiconductor layer are sensitive to the molar fractions of the semiconductor alloy forming the layer. *Id.* at 1:48-51.

In this context, the '117 Patent discusses deep ultraviolet LEDs, which are

LEDs capable of producing light in the ultraviolet range invisible to the naked eye. The '117 Patent contends that conventional deep ultraviolet LEDs "have a low efficiency due to light trapping within the device, light absorption in the semiconductor layers, as well as light absorption in the contact regions." *Id.* at 1:52-55. The '117 Patent purports to improve the prior art structure with "a design using ultraviolet transparent p-type cladding and contact layers, an ultraviolet reflecting ohmic contact, and chip encapsulation having an optimized shape and refractive index" so that the light extraction efficiency is improved. *Id.* at 1:55-60.

In the allegedly new LED structure described in the '117 Patent, the semiconductor layer includes a plurality of inhomogeneous regions. *Id.* at 2:4-5. This LED structure is depicted in Figure 1 of the '117 Patent (reproduced below), where the emitting device 10 includes a semiconductor heterostructure having multiple semiconductor layers, including an active region 18 and a p-type contact layer 22:



The ’117 Patent discloses that the p-type contact layer 22 is a group III nitride semiconductor layer. *Id.* at 5:11-18. The ’117 Patent also discloses a p-type metallic contact 26. Figure 1 above shows that the p-type contact layer 22 (“group III nitride semiconductor layer”) is located between the active region 18 and the p-type metallic contact 26.

The p-type contact layer 22 has one or more inhomogeneous regions located therein. *Id.* at 5:36-39. These inhomogeneous regions are arranged at different levels along a height of the semiconductor structure. *Id.* at 6:41-45. This can be

seen by the inhomogeneous regions 40A-C in Figure 3A, below:

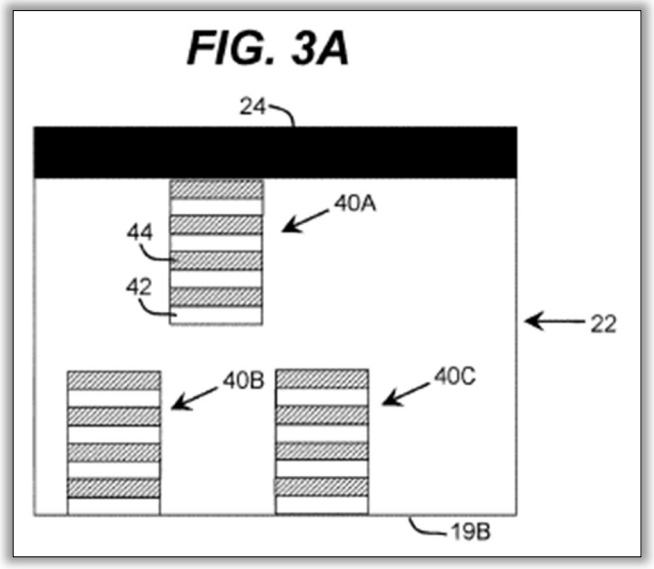


Figure 3A shows that inhomogeneous regions 40A in a first level are vertically offset from inhomogeneous regions 40B and 40C in a second level. The inhomogeneous regions can include one or more of the following: a set of transparent regions, a set of reflective regions, and/or a set of conductive regions. *Id.* at 5:43-46. Furthermore, each inhomogeneous region in the p-type contact layer "can have a set of attributes that differ from the group III nitride material forming the semiconductor layer." *Id.* at 13:14-17.

Challenged Claim 1 of the '117 Patent recites these concepts as follows:

1. [**preamble**] A semiconductor heterostructure, comprising:

[**1a**] an active region;

[**1b**] a metallic contact;

[**1c**] a group III nitride semiconductor layer located between the active region and the metallic contact,

[**1d**] the semiconductor layer including a plurality of inhomogeneous regions arranged within multiple levels of the semiconductor layer along a height direction of the semiconductor layer,

[**1e**] wherein some of the inhomogeneous regions in a first level of the semiconductor layer are vertically offset from inhomogeneous regions in a second level of the semiconductor layer, and

[**1f**] wherein the plurality of inhomogeneous regions include one or more of a set of transparent regions, a set of reflective regions and/or a set of conductive regions,

[**1g**] each of the inhomogeneous regions having a set of attributes differing from a group III nitride material forming the semiconductor layer.

VI. CLAIM CONSTRUCTION

Petitioner contends that, unless otherwise specifically noted herein, the claim terms in the '117 Patent are accorded their ordinary and customary meaning that they would have to a POSITA at the time of the alleged invention in view of the specification. *See also* Ex[1002], Dr. Shealy Decl., ¶¶53-54. For clarity, the ordinary and customary meaning of "inhomogeneous regions" in Claim 1 should take into account how that term is described in the '117 Patent. For example, the '117 Patent discloses that:

> Each inhomogeneous region has <u>one or more attributes that differ</u> from a material forming the semiconductor layer. The inhomogeneous regions can include one or

> more regions configured based on radiation having a target wavelength. These regions can include transparent and/or reflective regions. The inhomogeneous regions also can include one or more regions having a higher conductivity than a conductivity of the radiation-based regions, e.g., at least ten percent higher.

Ex[1001], 2:5-13 (emphasis added); Ex[1002], ¶55. Furthermore, the '117 Patent states that the "semiconductor structure can include inhomogeneous regions formed by one or more of patterning, masking, epitaxial growth, epitaxial overgrowth, deposition techniques, and/or the like." Ex[1001], 4:11-14; Ex[1002], ¶55.

With respect to a "conductive region," the '117 Patent describes that:

> A conductive region can be configured to promote conductivity of carriers in the semiconductor structure. A conductive region can have a higher concentration of carriers due to, for example, a locally reduced band gap of the semiconductor layer, a local high doping of the semiconductor layer, and/or the like.

Ex[1001], 5:60-65 (emphasis added); Ex[1002], ¶56. The '117 Patent continues that, "[i]n an embodiment, a conductive region has a conductivity at least ten percent higher than a conductivity of a transparent region and a conductivity of a reflective region and a higher conductivity than a base semiconductor material for the layer." Ex[1001], 6:5-9 (emphasis added); Ex[1002], ¶56.

With respect to a "transparent region," the '117 Patent explains that "a

region is a transparent region when the region allows at least ten percent of radiation having a target wavelength, which is radiated at a normal incidence to an interface of the region, to pass there through." Ex[1001], 5:46-49 (emphasis added); Ex[1002], ¶56.

Similarly, regarding a "reflective region," the '117 Patent discloses that, "as used herein, a region is a reflective region when the region reflects at least ten percent of radiation having a target wavelength, which is radiated at a normal incidence to an interface of the region," and, "[i]n an embodiment, the target wavelength of the radiation corresponds to a wavelength of radiation emitted or sensed by the active region 18 during operation of the device 10." Ex[1001], 5:50-53 (emphasis added); Ex[1002], ¶57. The '117 Patent further explains that a "reflective region can be formed of one or more composite mirrors" and a "composite mirror includes any structure having multiple sublayers of dielectric or metallic material." Ex[1001], 6:64-66; Ex[1002], ¶57.

The '117 Patent also discloses that, "[a]s used herein, unless otherwise noted, the term 'set' means one or more (i.e., at least one)[.]" Ex[1001], 3:67-4:1; Ex[1002], ¶58.

Petitioner's interpretation of the claim terms is further explained for each claim limitation in relation to the prior art discussed in invalidity Grounds 1-4,

below.[3]

VII. A PERSON HAVING ORDINARY SKILL IN THE ART

A POSITA with respect to the '117 Patent would have a Bachelor's degree in physics, electrical engineering, materials science, or a related field, and three to five years of experience in semiconductor devices, with specific experience in nitride based LEDs. Ex[1002], Dr. Shealy Decl., ¶¶30-34. However, even if a definition requiring less skill and experience is adopted, the invalidity grounds below would not be affected, especially as the prior art discloses each limitation of Claim 1 of the '117 Patent. *See id*. at ¶35.

VIII. SUMMARY OF THE PROSECUTION HISTORY

The '117 Patent was filed on December 30, 2015 and purports to claim priority to Provisional Application No. 61/768,581, filed on February 25, 2013. Ex[1001], (22), (60). The '117 Patent is also a continuation-in-part of the application that issued as U.S. Patent No. 9,331,224 (the "'224 Patent"). *Id*. at

[3] Petitioner reserves the right to address any claim construction positions taken by the Patent Owner in its Preliminary Response, including under 37 C.F.R. § 42.108(c). Petitioner further reserves its right to show that claims of the '395 Patent are invalid under 35 U.S.C. §112 in the co-pending litigation.

(63). To overcome a double patenting rejection, the '117 Patent is terminally disclaimed to the '224 Patent. *Id*. at Notice; Ex[1018], 54, 75.

The prior art Ohmae (Ex[1004]) and Ban (Ex[1005]) references were not cited or discussed during prosecution of the '117 Patent. Ex[1001]; Ex[1018]. The Shur reference (Ex[1006]) was cited in an IDS but was not discussed during prosecution. Ex[1001]; Ex[1018]. The prior art Saxler reference (Ex[1007]) was used as the basis for an obviousness rejection in combination with U.S. Patent Application Publication No. 2013/0270514 to Saxler ("Saxler '514") for claims not challenged here (claims 8-10). *See, e.g*., Ex[1018], 100-102. As potentially relevant in this proceeding, Applicant argued that the combination of Saxler '514 (the base reference) and Saxler "does not disclose or suggest a single semiconductor layer having a plurality of inhomogeneous regions arranged within multiple levels of the single semiconductor layer." Ex[1008], 74. The Applicant was wrong, as explained in detail in Ground 4, below. *See* Ex[1002], ¶43.

IX. GROUND 1: OHMAE RENDERS OBVIOUS CLAIM 1 OF THE '117 PATENT.

As set forth below, a POSITA would have understood that Ohmae renders obvious each of the limitations recited in Claim 1 of the '117 Patent. *See id.*, ¶¶70-84. The analysis below shows that there is no meaningful difference between the scope of the prior art and the limitations of Claim 1 of the '117 Patent.

Furthermore, Petitioner is unaware of any secondary considerations of non-obviousness that would change this conclusion. *See also* Ex[1002], ¶¶146-147.[4] Therefore, Claim 1 is obvious over Ohmae in view of the knowledge of a POSITA, as explained below.

A. Independent Claim 1

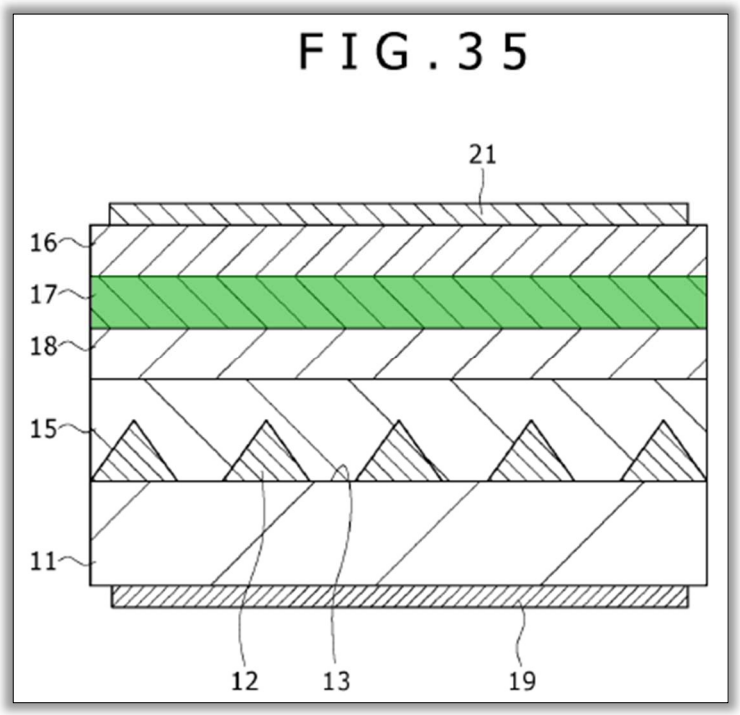
Preamble: A semiconductor heterostructure, comprising:

To the extent that the preamble is limiting, Ohmae discloses this subject matter. Ex[1002], ¶68. For example, Ohmae discloses that "FIG. 35 is a sectional view illustrating a method for manufacturing a light-emitting diode according to a further embodiment of the invention." Ex[1004] at [0100]; Ex[1002], ¶70. The '117 Patent teaches that, "[i]n general, each emitting device 10 includes a semiconductor heterostructure having multiple semiconductor layers." Ex[1001], 4:34-36. Therefore, the light-emitting diode of Ohmae is a semiconductor heterostructure having multiple semiconductor layers. Ex[1002], ¶70.

[4] If Patent Owner alleges that any secondary considerations support the non-obviousness of Claim 1, which is its burden, then Petitioner reserves the right to submit rebuttal evidence and argument under 37 C.F.R. § 42.108(c).

[1a] an active region;

Ohmae discloses an active region. Ex[1002], ¶71. For example, Ohmae teaches "an active layer 17 using a nitride-based III-V Group compound semiconductor." Ex[1004] at ¶[0157]; Ex[1002], ¶71. The active region of Ohmae is shown in green shading in Figure 35 below:



(Annotated FIG. 35)

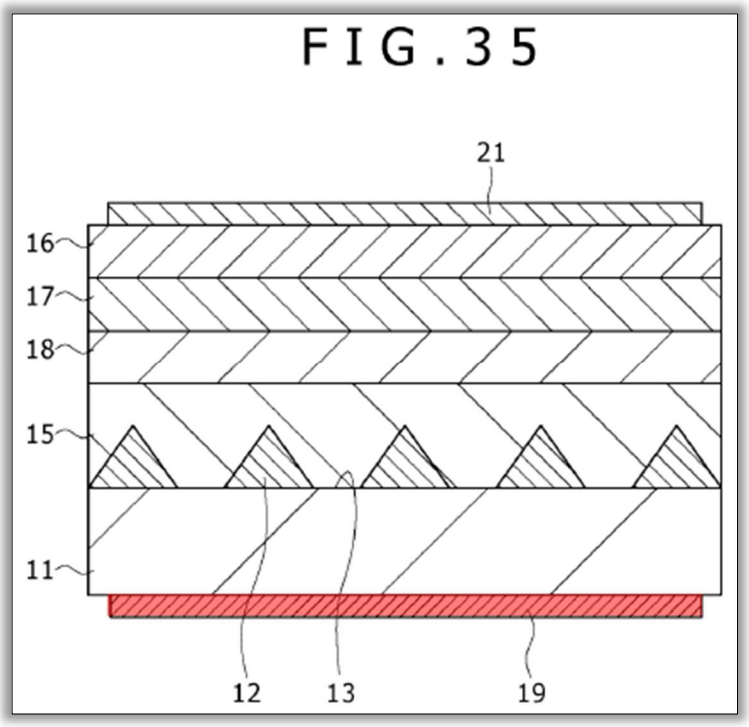
Ex[1002], ¶71.

[1b] a metallic contact;

Ohmae discloses a metallic contact. Ex[1002], ¶¶72-73. For example, Ohmae teaches "a p-side electrode 19." Ex[1004] at ¶[0231]. Furthermore,

Ohmae discloses that "[t]he material for the p-side electrode 19 includes, for example, Ag or Pd/Ag, or if necessary, barrier metals made of Ti, W, Cr, WN, CrN or the like." *Id.* at ¶[0167]. The '117 Patent teaches that the metallic contacts "comprise highly conductive metal." Ex[1001], 5:34-35. Therefore, the p-side electrode 19 of Ohmae, which includes highly conductive metal, is a metallic contact. Ex[1002], ¶72.

The p-side electrode 19 (the claimed "metallic contact") is shown in red in Figure 35, below:

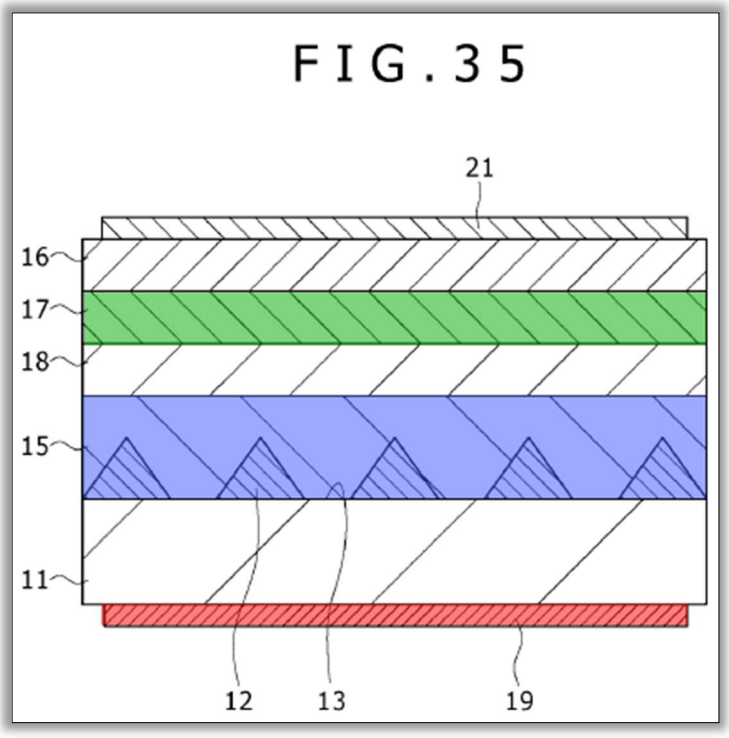


(Annotated FIG. 35)

Ex[1002], ¶73.

[1c] a group III nitride semiconductor layer located between the active region and the metallic contact;

Ohmae discloses this limitation. Ex[1002], ¶74. For example, Ohmae teaches a "nitride-based III-V Group compound semiconductor layer 15" located between the active region (active layer 17) and the metallic contact (p-side electrode 19). Ex[1004] at ¶[0231]. As shown in annotated Figure 35 below, the nitride-based III-V Group compound semiconductor layer 15 (shaded in blue) is located between the active region 17 (shaded in green) and the p-side electrode 19 (the claimed "metallic contact" shaded in red).



(Annotated FIG. 35)

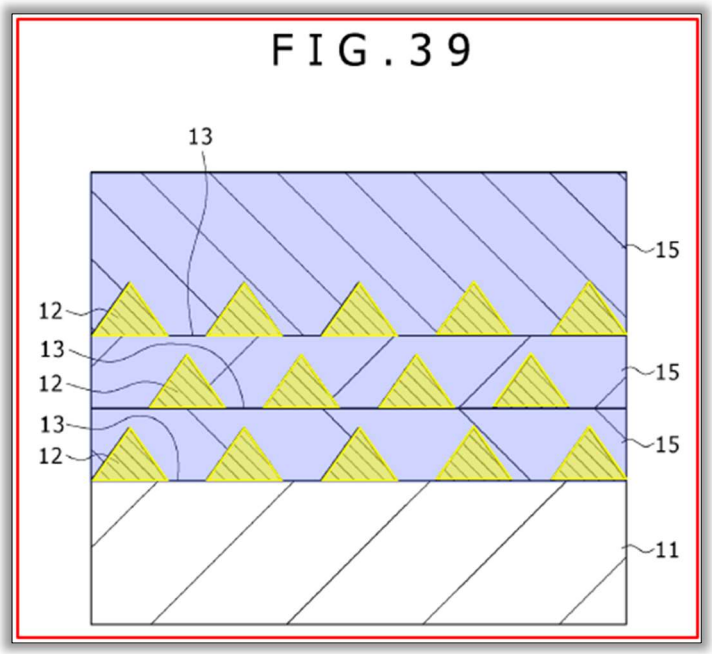
[1d] the semiconductor layer including a plurality of inhomogeneous regions arranged within multiple levels of the semiconductor layer along a height direction of the semiconductor layer;

Ohmae discloses this limitation. Ex[1002], ¶¶75-78. For example, Ohmae discloses forming a plurality of protruded portions on the substrate and subsequently growing a nitride-based III-V Group semiconductor layer that embeds the protruded portions. Ex[1004] at ¶[0021]. In particular, "the step of forming protruded portions 12 and growing the nitride-based III-V Group compound semiconductor layer 15 like the first embodiment starts from forming protruded portions 12 on the substrate 11, followed by repeating the step plural times." *Id.* at ¶[0247]. Ohmae also discloses that the "materials for the protruded portion may be of various types and may be electrically conductive or non-conductive," such as, "for example, dielectric materials such as oxides, nitrides, carbides and the like and conductors such as of metals, alloys and the like (including transparent conductors)." *Id.* at ¶[0026].

As explained by Dr. Shealy: "protruded portions made of dielectric materials or conductors would constitute inhomogeneous regions within the semiconductor layer composed of nitride-based III-V Group compound semiconductor" and "the nitride-based semiconductor material grown on top of the protruded portions are also inhomogeneous regions." Ex[1002], ¶76. In fact, the '117 Patent includes

examples for forming inhomogeneous regions that includes the methods disclosed in Ohmae: "The semiconductor structure can include inhomogeneous regions formed by one or more of patterning, masking, epitaxial growth, epitaxial overgrowth, deposition techniques, and/or the like." Ex[1001], 4:4-14; Ex[1002], ¶76.

Furthermore, "repeating the step of forming protruded portions and growing the semiconductor layer results in a plurality of inhomogeneous regions arranged within multiple levels of the semiconductor layer along a height direction of the semiconductor layer." Ex[1002], ¶77. Figure 39 (annotated below) shows a plurality of yellow protruded portions 12 (the claimed "inhomogeneous regions") arranged within multiple levels of the blue semiconductor layer 15 along a height direction of the semiconductor layer 15:



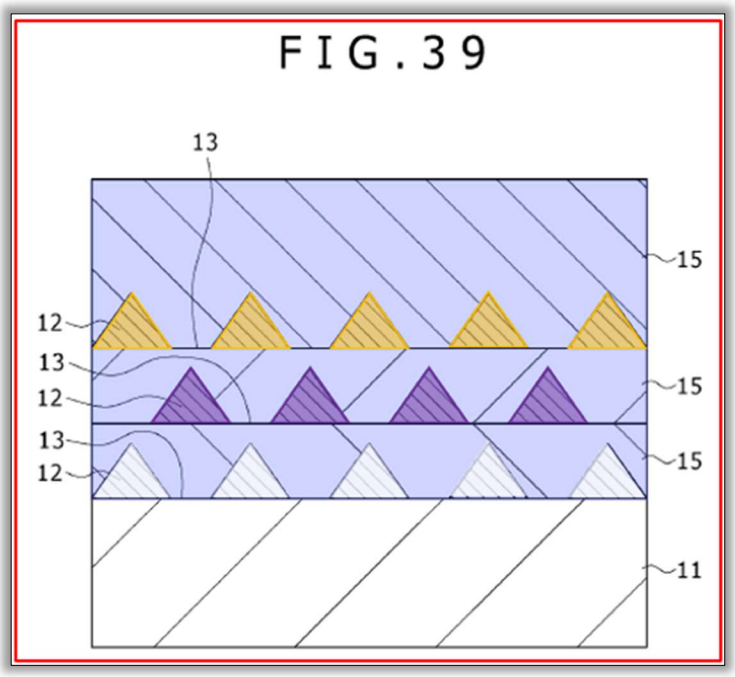
(Annotated FIG. 39)

As shown and described with respect to Figure 39 of Ohmae, the nitride-based III-V Group compound semiconductor layer 15 in Figure 35 of Ohmae includes multiple levels (i.e., multiple sub-layers 15), and the protruded portions 12 are arranged within the multiple levels of the nitride-based III-V Group compound semiconductor layer 15 along the vertical direction. Ex[1002], ¶78. Accordingly, Ohmae discloses this limitation because multiple levels of the protruded portions (as well as semiconductor material grown on top of the protruded portions) form a plurality of inhomogeneous regions arranged within multiple levels of the semiconductor layer along a height direction of the semiconductor layer. *Id*.

[1e] wherein some of the inhomogeneous regions in a first level of the semiconductor layer are vertically offset from inhomogeneous regions in a second level of the semiconductor layer, and,

Ohmae discloses this limitation. Ex[1002], ¶¶79-80. For example, Ohmae discloses that "the step of forming protruded portions 12 and growing the nitride-based III-V Group compound semiconductor layer 15 like the first embodiment starts from forming protruded portions 12 on the substrate 11, followed by repeating the step plural times" and that, "[i]n this case, the protruded portions in the respective layers are formed at positions that are mutually shifted by a half cycle within planes parallel to the main surface of the substrate 11." Ex[1004] at ¶[0247] (emphasis added).

Dr. Shealy explains that a POSITA "would understand that as a result of the layers formed at positions that are **mutually shifted by a half cycle**, some of the inhomogeneous regions in a first level of the semiconductor layer are vertically offset (*e.g.*, vertically misaligned) from inhomogeneous regions in a second level of the semiconductor layer." Ex[1002], ¶80 (emphasis in original). Annotated Figure 39, below, shows that the inhomogeneous regions in a first level of the semiconductor layer (shaded in orange) are vertically offset from inhomogeneous regions in a second level of the semiconductor layer (shaded in purple):



(Annotated FIG. 39)

[1f] wherein the plurality of inhomogeneous regions include one or more of a set of transparent regions, a set of reflective regions and/or a set of conductive regions,

Ohmae discloses this limitation. Ex[1002], ¶¶81-82. For example, Ohmae discloses that "the materials for the protruded portion may be of various types and may be conductive or non-conductive," such as, "for example, dielectric materials such as oxides, nitrides, carbides and the like and conductors such as of metals, alloys and the like (including transparent conductors)." Ex[1004] at ¶[0026] (emphasis added). Because Ohmae explicitly discloses that the protruded portions are made of "transparent" and "conductor" material, the protruded portions of Ohmae formed of "oxides," "conductors," and "transparent conductors" constitute

a set of transparent regions and a set of conductive regions. Ex[1002], ¶81. Furthermore, "metals are reflective." *Id*. Again, the '117 Patent discloses that "a region is a reflective region when the region reflects at least ten percent of radiation having a target wavelength." Ex[1001], 5:50-52. Thus, the "metal" protruded portion of Ohmae constitutes a set of reflective regions. Ex[1002], ¶81. In fact, Ohmae discloses that "the second portion 12b of the protruded portion 12 is made of a metal or an alloy" and "light emitted from the active layer 17 can be reflected to a side opposite to the substrate 11[.]" Ex[1004] at ¶[0210] (emphasis added).

Therefore, Ohmae discloses wherein the plurality of inhomogeneous regions include one or more of a set of transparent regions, a set of reflective regions and/or a set of conductive regions. Ex[1002], ¶82.

[1g] each of the inhomogeneous regions having a set of attributes differing from a group III nitride material forming the semiconductor layer.

Ohmae discloses this limitation. Ex[1002], ¶83. For example, Ohmae discloses that "the materials for the protruded portion may be of various types and may be electrically conductive or non-conductive," including, "for example, dielectric materials such as oxides, nitrides, carbides and the like and conductors such as of metals, alloys and the like (including transparent conductors)."

Ex[1004] at [0026] (emphasis added). As Dr. Shealy explains, "[d]ielectric materials and conductors have different material attributes than the group III nitride semiconductor material" because, "[f]or example, dielectric materials are electrically insulating; metals and conductors are electrical conducting; in contrast, semiconductor materials have an electrical conductivity that falls between that of a metal and an insulator." Ex[1002], ¶83. Furthermore, dielectric materials and conductors have different chemical compositions than the group III nitride semiconductor material. *Id*. Therefore, due to their different material attributes, the protruded portions made of dielectric materials or conductors in Ohmae have a set of attributes different from the nitride-based III-V Group compound semiconductor layer. *Id*.

Accordingly, Ohmae discloses this limitation and renders obvious Claim 1 of the '117 Patent. *See also id*. at ¶84.

X. GROUND 2: BAN RENDERS OBVIOUS CLAIM 1 OF THE '117 PATENT.

A POSITA would have understood that Ban renders obvious each limitation recited in Claim 1. *See* Ex[1002], ¶¶86-100. The analysis below shows that there is no meaningful difference between the scope of the prior art and the limitations of Claim 1 of the '117 Patent. Furthermore, Petitioner is unaware of any secondary considerations of non-obviousness that would change this conclusion.

See also id. at ¶¶146-147. Therefore, Claim 1 is obvious over Ban in view of the knowledge of a POSITA, as explained below.

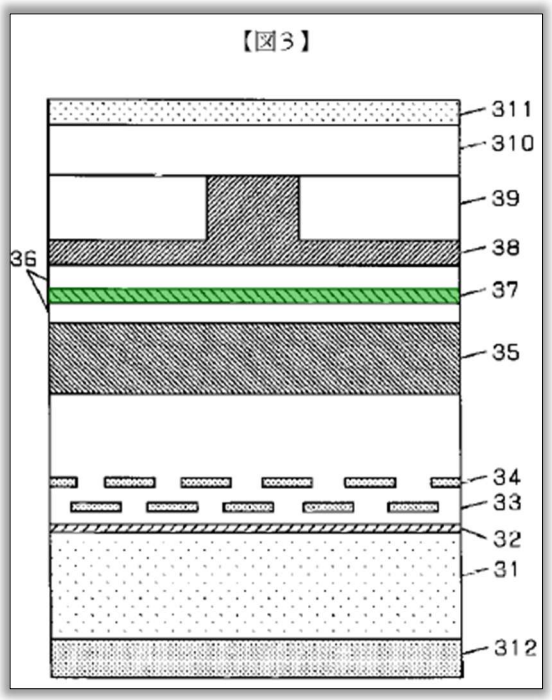
A. Independent Claim 1

Preamble: A semiconductor heterostructure, comprising:

To the extent that the preamble is limiting, Ban discloses this subject matter. Ex[1002], ¶87. For example, Ban discloses "a manufacturing method of the semiconductor device used in a light emitting element." Ex[1005] at ¶[0001]. Again, the '117 Patent teaches that, "[i]n general, each emitting device 10 includes a semiconductor heterostructure having multiple semiconductor layers." Ex[1001], 4:34-36. Therefore, a POSITA "would have understood that the light emitting element of Ban is a semiconductor heterostructure having multiple semiconductor layers." Ex[1002], ¶87.

[1a] an active region;

Ban discloses an active region. Ex[1002], ¶88. For example, Ban discloses that region "37 is a GaInN quantum well active layer." Ex[1005] at ¶[0042]. Annotated Figure 3 of Ban, below, shows the active region (shaded in green):



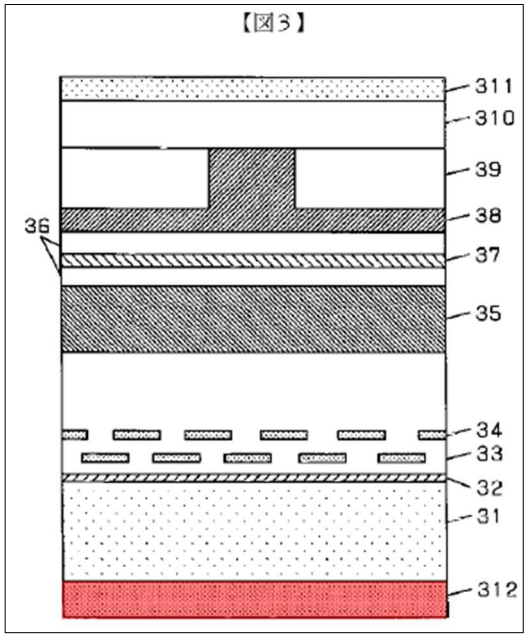
(Annotated FIG. 3)

Ex[1002], ¶88.

[1b] a metallic contact;

Ban discloses a metallic contact. Ex[1002], ¶89. For example, Ban discloses that "a Ni/Au layer 312 (with a film thickness of 500nm) is formed on the back surface of the substrate." Ex[1005] at ¶[0042]. Ban also discloses that "a Ni/Au layer" can "serve as the metal layer." *Id.* at [0034]. The '117 Patent describes that metallic contacts "comprise highly conductive metal." Ex[1001], 5:34-35. The Ni/Au layer of Ban formed on the back surface of the substrate is a

metal layer that constitutes the metallic contact. Ex[1002], ¶89. Annotated Figure 3 of Ban, below, shows the metallic contact (shaded in red):



(Annotated FIG. 3)

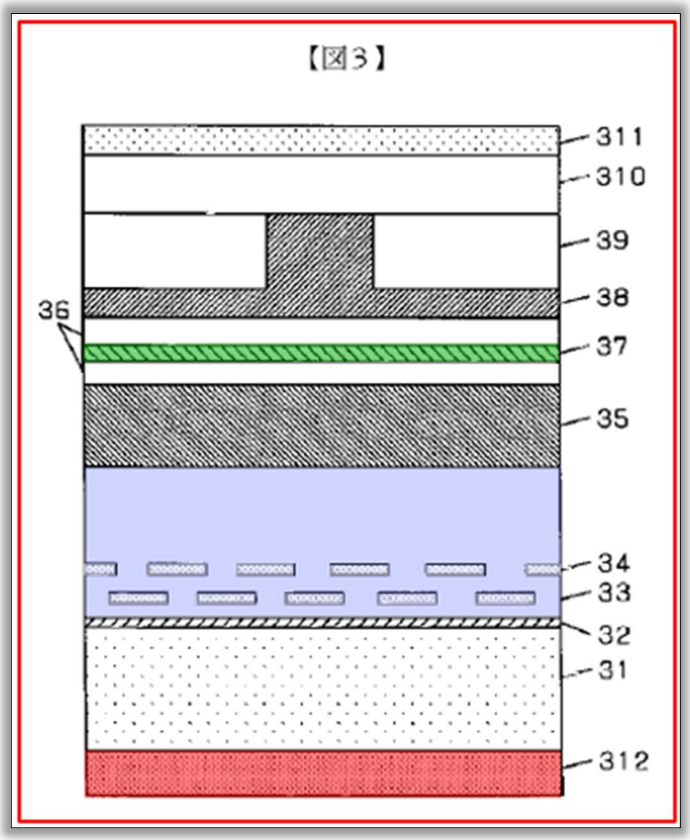
Ex[1002], ¶89.

[1c] a group III nitride semiconductor layer located between the active region and the metallic contact;

Ban discloses this limitation. Ex[1002], ¶¶90-91. For example, Ban discloses that region "33 is an n-type GaN layer," which is a "group III-V compound semiconductor layer." Ex[1005] at ¶¶[0042], [0043].

Ban also discloses that its group III nitride semiconductor layer is located between the active region and the metallic contact. Ex[1002], ¶91. As shown in annotated Figure 3 of Ban, below, the n-type GaN layer 33 (the claimed "group III

nitride semiconductor layer", excluding the SiO_2 mask layers 34, and shaded in blue) is located between the active layer 37 (the claimed "active region" shaded in green) and the Ni/Au layer 312 (the claimed "metallic contact" shaded in red).



(Annotated FIG. 3)

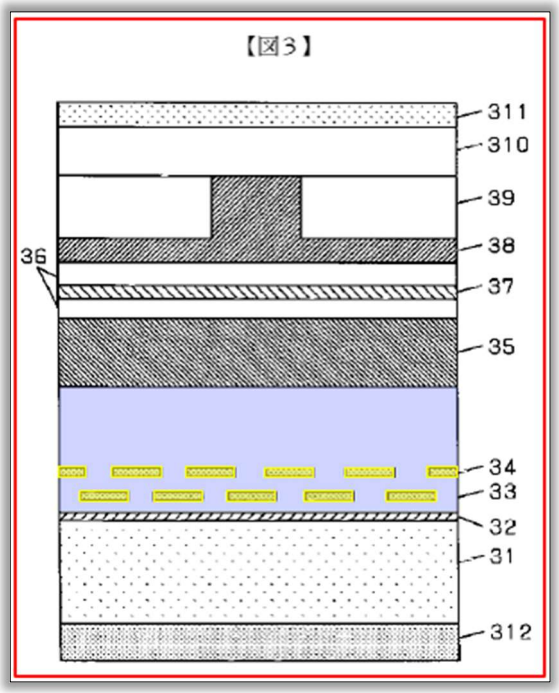
Ex[1002], ¶91.

[1d] the semiconductor layer including a plurality of inhomogeneous regions arranged within multiple levels of the semiconductor layer along a height direction of the semiconductor layer;

Ban discloses this limitation. Ex[1002], ¶¶92-93. For example, Ban discloses a "SiO_2 mask layer," which "is embedded in a stripe shape in the group

III-V compound semiconductor layer on the substrate." Ex[1005] at ¶¶[0042], [0043]. As Dr. Shealy explains, "the SiO_2 mask layer constitutes an inhomogeneous region." Ex[1002], ¶92. Again, the '117 Patent describes similar examples for forming inhomogeneous regions as in Ban: "The semiconductor structure can include inhomogeneous regions formed by one or more of patterning, masking, epitaxial growth, epitaxial overgrowth, deposition techniques, and/or the like." Ex[1001], 4:4-14.

Ban teaches that "a SiO_2 mask layer 34 … is formed by plasma CVD or the like, and a striped opening with a pitch of 4μm and a width of 1.5μm is formed in the [1-100] direction of the GaN." Ex[1005] at ¶[0045]. Then "the stripe shaped SiO_2 mask layer 34 … of the second layer is formed in the same direction as above by the plasma CVD method or the like." *Id.* at ¶[0046]. The result is the blue-shaded n-type GaN layer 33 (the claimed "semiconductor layer") including a plurality of yellow-shaded SiO_2 mask layers 34 (the claimed "inhomogeneous regions") arranged within multiple levels of the semiconductor layer along a height direction of the semiconductor layer, as shown in annotated Figure 3, below.



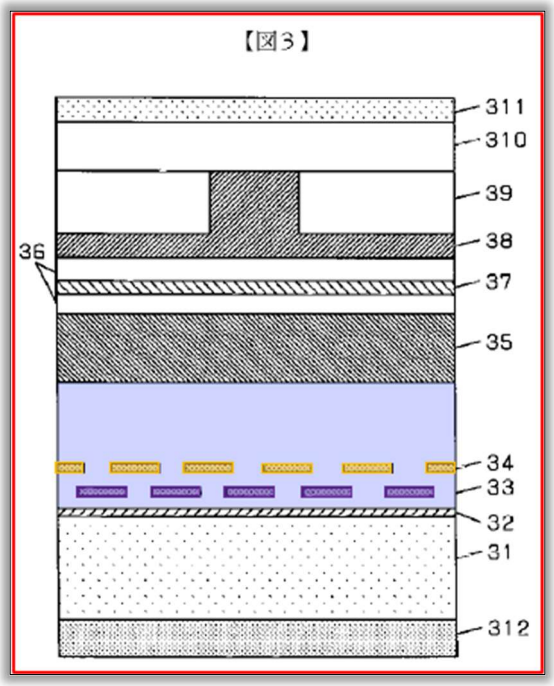
(Annotated FIG. 3)

Ex[1002], ¶ 93.

[1e] wherein some of the inhomogeneous regions in a first level of the semiconductor layer are vertically offset from inhomogeneous regions in a second level of the semiconductor layer, and,

Ban discloses this limitation. Ex[1002], ¶94. For example, Ban discloses that to form the second layer, "the opening of the mask is shifted to the mask of the first layer to form the mask of the second layer." Ex[1005] at ¶[0046] (emphasis added). A POSITA would have understood "that the shifting of the mask opening causes mask of the first layer to be vertically offset (*e.g.*, vertically misaligned) from the mask of the second layer." Ex[1002], ¶94 (emphasis in original).

Annotated Figure 3, below, shows that the inhomogeneous regions in a first level of the semiconductor layer (shaded in orange) are vertically offset from inhomogeneous regions in a second level of the semiconductor layer (shaded in purple).



(Annotated FIG. 3)

Ex[1002], ¶94.

[1f] wherein the plurality of inhomogeneous regions include one or more of a set of transparent regions, a set of reflective regions and/or a set of conductive regions,

Ban discloses this limitation. Ex[1002], ¶¶95-97. Ban discloses a "SiO_2 mask layer," which "is embedded in a stripe shape in the group III-V compound semiconductor layer on the substrate." Ex[1005] at ¶¶[0042], [0043].

The '117 Patent states that "a region is a transparent region when the region allows at least ten percent of radiation having a target wavelength, which is radiated at a normal incidence to an interface of the region, to pass there through." Ex[1001], 5:46-49. A POSITA would have understood "that SiO_2 (which is similar to fused silica or quartz glass) is a transparent material because it allows at least 10% of radiation having a target wavelength of Ban (e.g., UV to blue light) to pass through." Ex[1002], ¶96. For instance, Ban discloses that the "intermediate layer 36 may be formed of a transparent insulating material," such as "SiO_2, SiN_x, Al_2O_3, HfO, TiO_2, or ZrO." Ex[1016], 4:65-5:2 (emphasis added). Therefore, the SiO_2 mask layer 34 of Ban forms a plurality of transparent inhomogeneous regions. Ex[1002], ¶96.

Accordingly, Ban discloses wherein the plurality of inhomogeneous regions include one or more of a set of transparent regions, a set of reflective regions and/or a set of conductive regions. *Id*. at ¶97.

[1g] each of the inhomogeneous regions having a set of attributes differing from a group III nitride material forming the semiconductor layer.

Ban discloses this limitation. Ex[1002], ¶¶98-100. For example, Ban discloses that "SiO_2 is embedded in a stripe shape in the group III-V compound semiconductor layer on the substrate." Ex[1005] at ¶[0043]. A POSITA would

have understood "that the SiO_2 mask layer is made of a dielectric material that has material attributes substantially different from the n-type GaN semiconductor layer" and that "the SiO_2 mask layer form a transparent region that has material attributes substantially different from the n-type GaN semiconductor layer." Ex[1002], ¶98. Therefore, Ban discloses that each of the inhomogeneous regions have a set of attributes different from a group III nitride material forming the semiconductor layer. *Id*. at ¶99.

Accordingly, Ban discloses this limitation and renders obvious Claim 1 of the '117 Patent. *See also id*. at ¶100.

XI. GROUND 3: SHUR RENDERS OBVIOUS CLAIM 1 OF THE '117 PATENT.

A POSITA would have understood that Shur renders obvious each limitation recited in Claim 1. *See* Ex[1002], ¶¶99-118. The analysis below shows that there is no meaningful difference between the scope of the prior art and the limitations of Claim 1 of the '117 Patent. Furthermore, Petitioner is unaware of any secondary considerations of non-obviousness that would change this conclusion. *See also id*. at ¶¶144-145. Therefore, Claim 1 is obvious over Shur in view of the knowledge of a POSITA, as explained below.

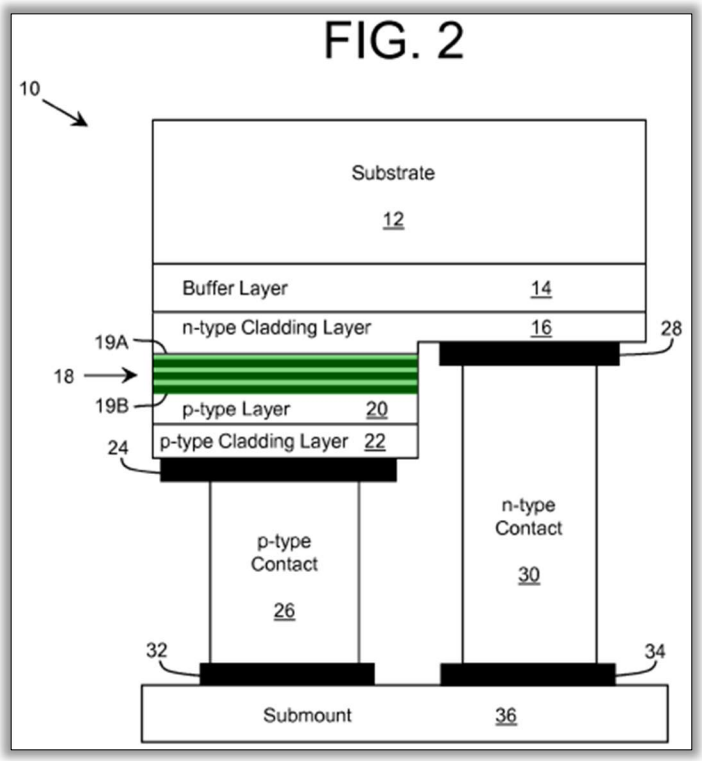
A. Independent Claim 1

Preamble: A semiconductor heterostructure, comprising:

To the extent that the preamble is limiting, Shur discloses this subject matter. Ex[1002], ¶102. For example, Shur discloses a semiconductor device (e.g., emitting device 10 of FIG. 2) that includes a heterostructure. Ex[1006] at ¶[0033], Fig. 2. Therefore, Shur discloses a semiconductor heterostructure. Ex[1002], ¶102.

[1a] an active region;

Shur discloses an active region. Ex[1002], ¶¶103-104. For example, Shur discloses "an active region 18." Ex[1006] at ¶[0033]. This element is shaded in green in annotated Figure 2, below:



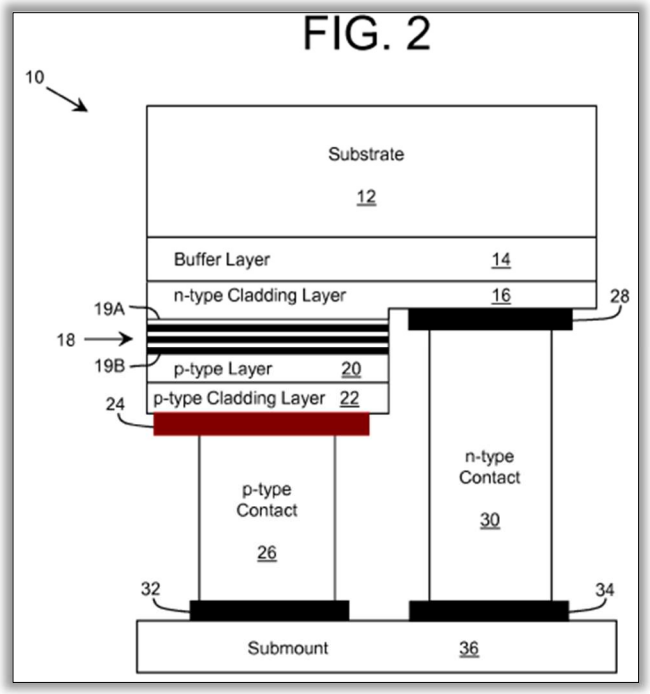
(Annotated FIG. 2)

Ex[1002], ¶103. Furthermore, Shur discloses "an active region 18 (e.g., a series of alternating quantum wells and barriers) composed of $In_yAl_xGa_{1-x-y}N$, $Ga_zIn_yAl_xB_{1-x-y-z}N$, and $Al_xGa_{1-x}N$ semiconductor alloy, or the like." Ex[1005] at ¶[0035]. Therefore, Shur discloses an active region. Ex[1002], ¶104.

[1b] a metallic contact;

Shur discloses a metallic contact. Ex[1002], ¶¶105-106. For example, Shur discloses a p-side "metal 24" that can form an "ohmic contact[]." Ex[1006] at [0036]. A POSITA would have understood "that the p-side metal and the ohmic

contact are metallic contacts of the semiconductor device." Ex[1002], ¶107. The p-side metal 24 is shaded in red in annotated Figure 2, below:



(Annotated FIG. 2)

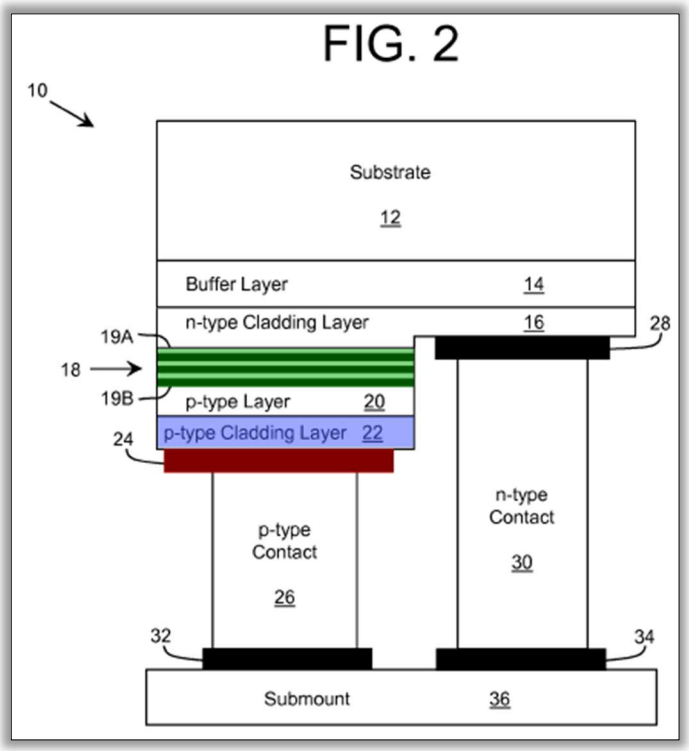
Id. Therefore, the p-side metal 24 of Shur constitutes the claimed metallic contact. *Id*. at ¶106.

[1c] a group III nitride semiconductor layer located between the active region and the metallic contact;

Shur discloses this limitation. Ex[1002], ¶¶109-110. For example, Shur discloses that "the p-type cladding layer 22 . . . can comprise a short period superlattice lattice structure, such as an at least partially transparent magnesium (Mg)-doped AlGaN/AlGaN short period superlattice structure (SPSL)." Ex[1006]

at ¶[0036]. A POSITA would have understood "that AlGaN is a group III nitride semiconductor layer because aluminum (Al) and gallium (Ga) are both group III elements and combined with nitride (N) form AlGaN, which is a group III nitride." Ex[1002], ¶109. Thus, the p-type cladding layer 22 of Shur constitutes a group III nitride semiconductor layer. *Id*.

Shur further discloses the group III nitride semiconductor layer is located between the active region and the metallic contact. *Id*. at ¶110. As shown in annotated Figure 2, below, the p-type cladding layer 22 (the claimed "group III nitride semiconductor layer" shaded in blue) is located between the active region 18 (the claimed "active region" shaded in green) and the p-side metal 24 (the claimed "metallic contact" shaded in red):



(Annotated FIG. 2)

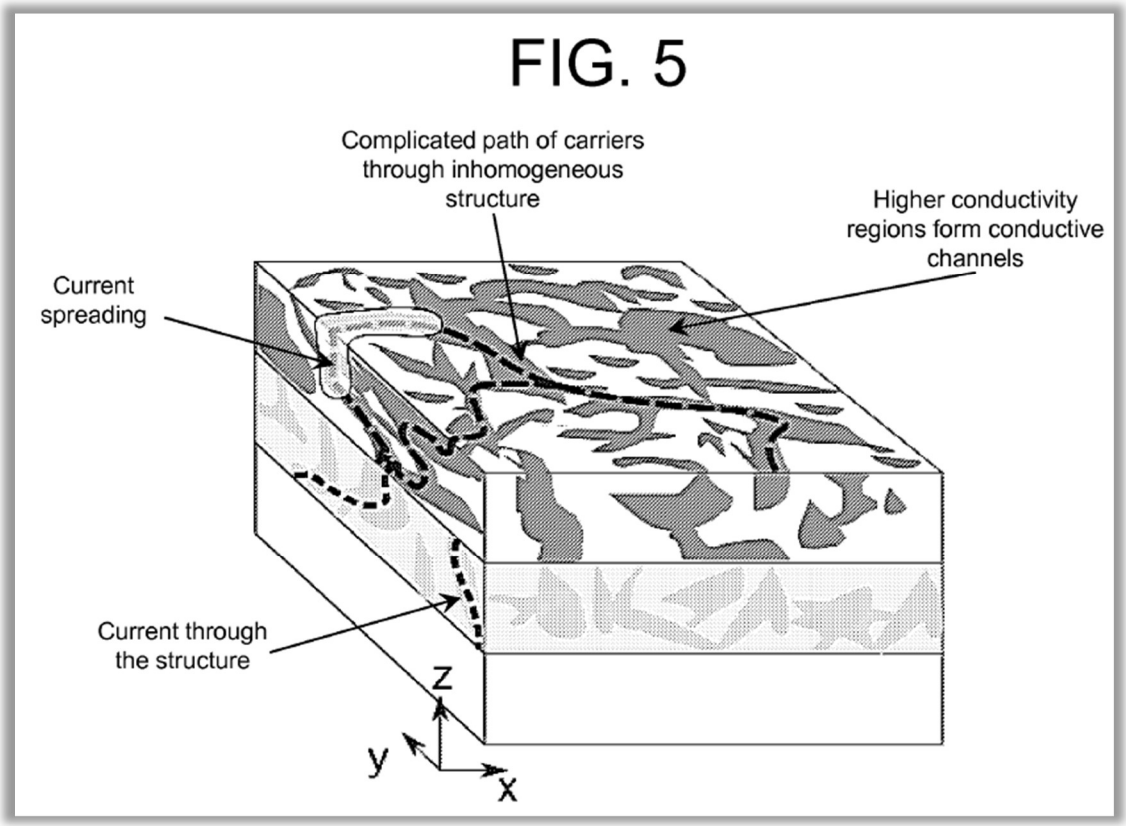
Id.

[1d] the semiconductor layer including a plurality of inhomogeneous regions arranged within multiple levels of the semiconductor layer along a height direction of the semiconductor layer;

Shur discloses this limitation. Ex[1002], ¶¶111-116. For example, Shur describes that "one or more of the semiconductor layers of the device 10 can comprise nano-scale and/or micron-scale localized compositional and/or doping inhomogeneities along the lateral dimensions of the device die." Ex[1006] at ¶[0042]. Shur discloses that these "inhomogeneities are incorporated into a layer

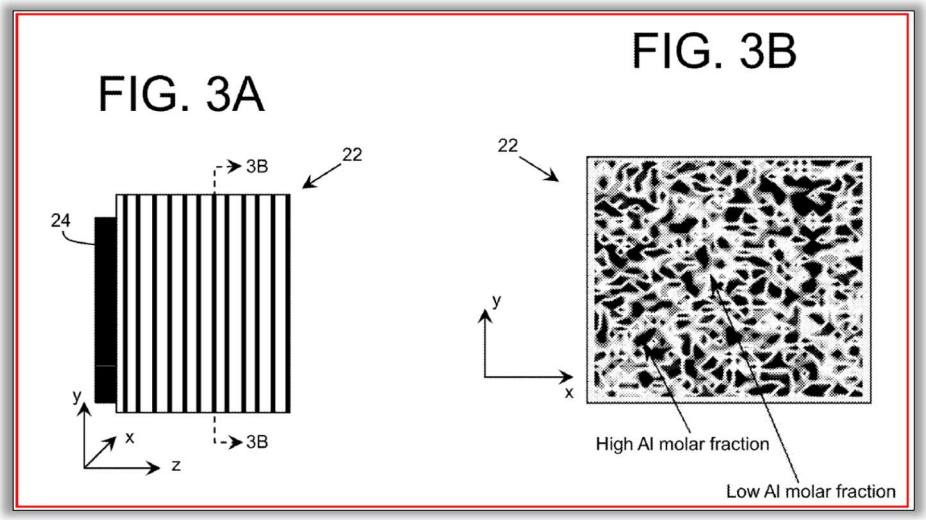
formed using a p-type superlattice, such as the p-type cladding layer 22." *Id.* at [0044].

Figure 5 of Shur "shows a schematic representation of an illustrative carrier path in a complicated energy landscape caused by the inhomogeneities according to an embodiment." *Id*. at ¶[0054].



Shur also discloses that the semiconductor layer includes a plurality of inhomogeneous regions arranged within multiple levels of the semiconductor layer along a height direction of the semiconductor layer. Ex[1002], ¶111. For example, as reproduced below, "FIGS. 3A and 3B show illustrative schematic

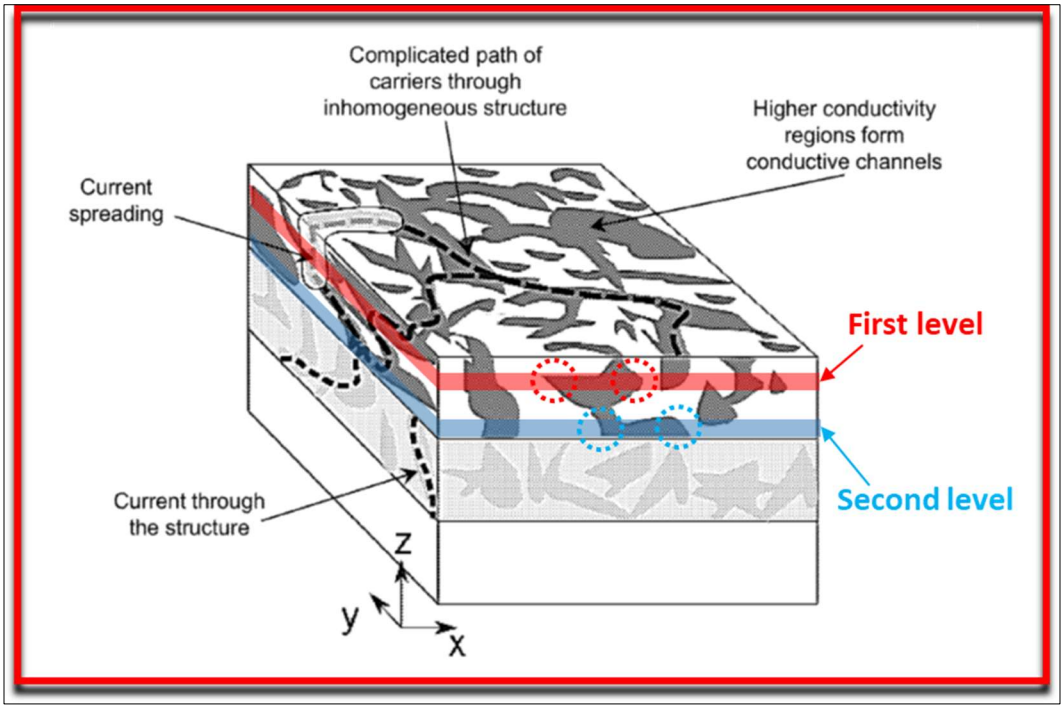
representations of the p-type cladding layer 22 formed using a p-type superlattice" and "FIG. 3A illustrates variation in aluminum composition within the layer 22 along the height of the layer (e.g., indicated by direction z) in a direction normal to a surface of the layer 22 adjacent to the p-type metal 24"; "FIG. 3B illustrates variation in the aluminum composition of the p-type cladding layer 22 in the lateral directions (e.g., indicated by directions x and y) of the layer 22." Ex[1006] at ¶¶[0045]-[0046].



A POSITA would have understood "that each layer of the multi-layer superlattice (as shown in FIG. 3A) includes a plurality of inhomogeneous regions within such layer (as shown in FIG. 3B)." Ex[1002], ¶114. Therefore, Shur discloses that the semiconductor layer (e.g., p-type cladding layer 22) includes a plurality of inhomogeneous regions arranged within multiple levels of the

semiconductor layer along a height direction of the semiconductor layer. *Id*.

Furthermore, annotated Figure 5, below, shows a plurality of inhomogeneous regions arranged within multiple levels of the semiconductor layer along a height direction z of the semiconductor layer. *Id*. at ¶113. For example, a first level of the semiconductor layer is shaded in red and a second level of the semiconductor layer is shaded in blue. Additionally, the inhomogeneous regions within the first level (within red circles) are vertically offset from the inhomogeneous regions within the second level (within blue circles).

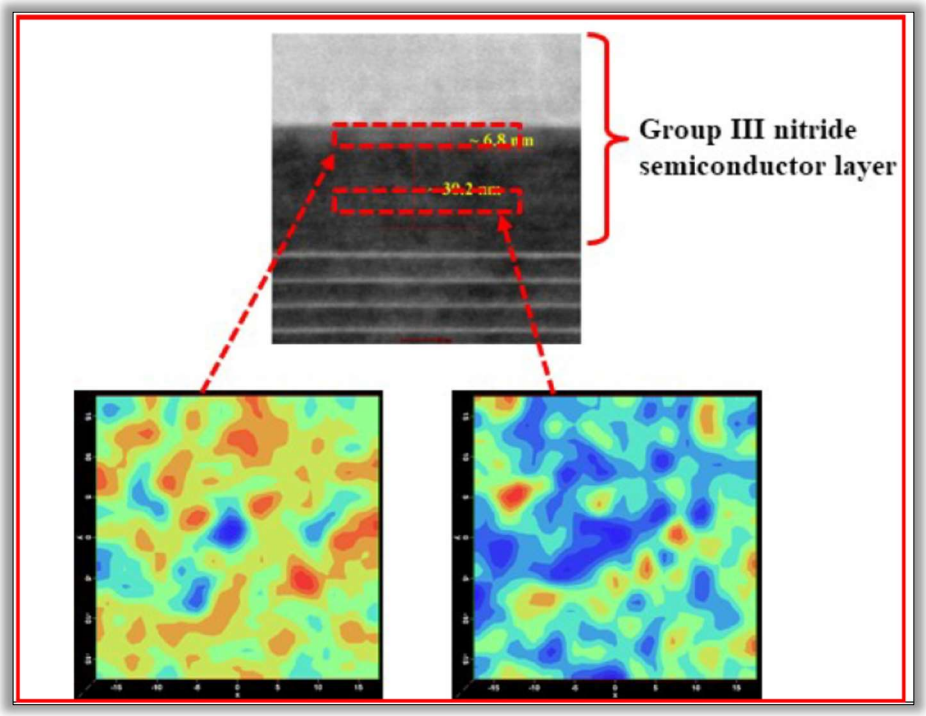


(Annotated FIG. 5)

As such, a POSITA would have understood "that FIG. 5 of Shur teaches a plurality of inhomogeneous regions arranged within multiple levels of the semiconductor

layer along a height direction z of the semiconductor layer." *Id*. at ¶113.

Indeed, as shown below, the "inhomogeneous regions" of Shur are similar to what Patent Owner has contended constitutes "inhomogeneous regions" in its infringement allegations in the related litigation:



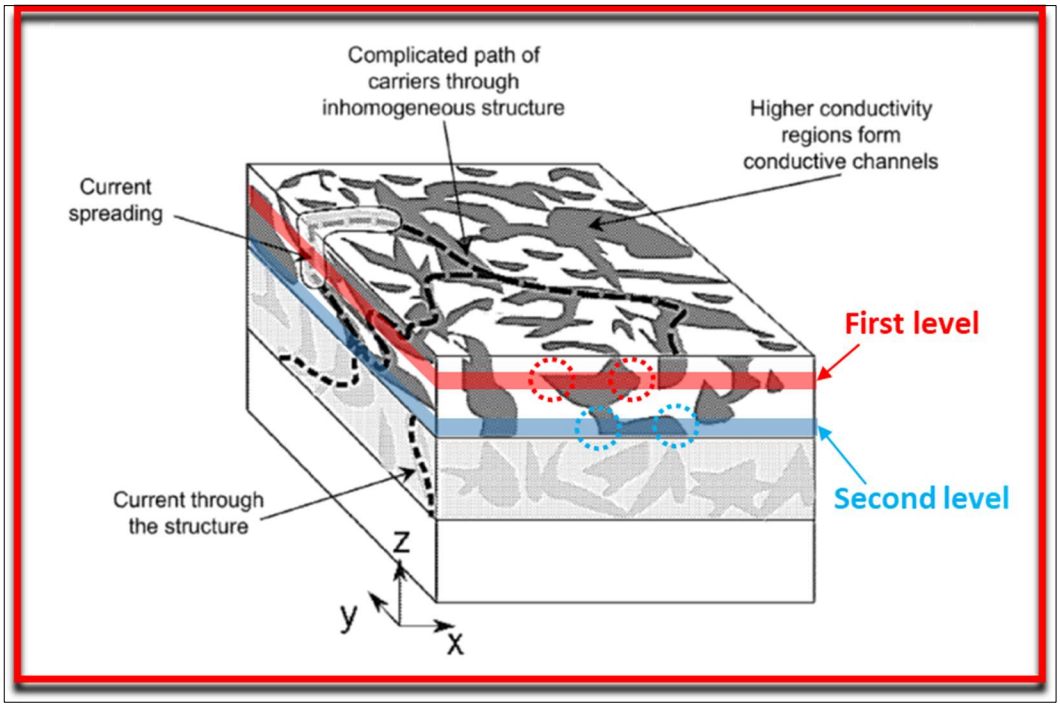
(Infringement contention by Patent Owner)

Id. at ¶116; Ex[1021].

[1e] wherein some of the inhomogeneous regions in a first level of the semiconductor layer are vertically offset from inhomogeneous regions in a second level of the semiconductor layer, and,

Shur discloses this limitation. Ex[1002], ¶117. Annotated Figure 5 shows red-circled inhomogeneous regions in a first level of the semiconductor layer that are vertically offset from blue-circled inhomogeneous regions in a second level of

the semiconductor layer. *Id*. "[E]ach of the red circle or blue circle constitutes an inhomogeneous region within the semiconductor layer; thus, Shur discloses this limitation." *Id*.



(Annotated FIG. 5)

[1f] wherein the plurality of inhomogeneous regions include one or more of a set of transparent regions, a set of reflective regions and/or a set of conductive regions,

Shur discloses this limitation. Ex[1002], ¶118. For example, Shur discloses that "the inhomogeneities will result in lower band gap regions, which . . . form a set of higher conductive regions of carrier conductive channels in the semiconductor layer," and "the inhomogeneities also will result in high band gap regions, which form a set of at least partially transparent regions within the layer."

Ex[1006] at [0042] (emphasis added). Because the inhomogeneous regions of Shur constitute either transparent regions or conductive regions, Shur discloses this limitation. Ex[1002], ¶118.

[1g] each of the inhomogeneous regions having a set of attributes differing from a group III nitride material forming the semiconductor layer.

Shur discloses this limitation. Ex[1002], ¶119. For example, Shur discloses that "[t]hese inhomogeneities provide variation of band gap energy in a lateral direction of the layer, which results in a complicated energy landscape for a lateral cross section of the layer" and "the inhomogeneities will result in lower band gap regions, which become places of charge localization and form a set of higher conductive regions of carrier conductive channels in the semiconductor layer." Ex[1006] at ¶[0042] (emphasis added). "These higher conductive regions have an improved vertical conductivity over that of a substantially homogenous layer of the material," and "the inhomogeneities also will result in high band gap regions, which form a set of at least partially transparent regions within the layer, each of which has an improved vertical transparency over that of a substantially homogenous layer of the material." *Id.* (emphasis added). Thus, "each of the inhomogeneous regions has a set of material attributes—*e.g.*, variation of band gap energy, higher conductive regions, improved vertical conductivity, and improved

vertical transparency—differing from a group III nitride material forming the semiconductor layer." Ex[1002], ¶119.

Accordingly, Shur discloses this limitation and renders obvious Claim 1 of the '117 Patent. *See also id*. at ¶120.

XII. GROUND 4: SAXLER RENDERS OBVIOUS CLAIM 1 OF THE '117 PATENT.

A POSITA would have understood that Saxler renders obvious each limitation recited in Claim 1. *See* Ex[1002], ¶¶121-145. The analysis below also shows that there is no meaningful difference between the scope of the prior art and the limitations of Claim 1 of the '117 Patent. Furthermore, Petitioner is unaware of any secondary considerations of non-obviousness that would change this conclusion. *See also id*. at ¶¶146-147. Therefore, Claim 1 is obvious over Saxler in view of the knowledge of a POSITA, as explained below.

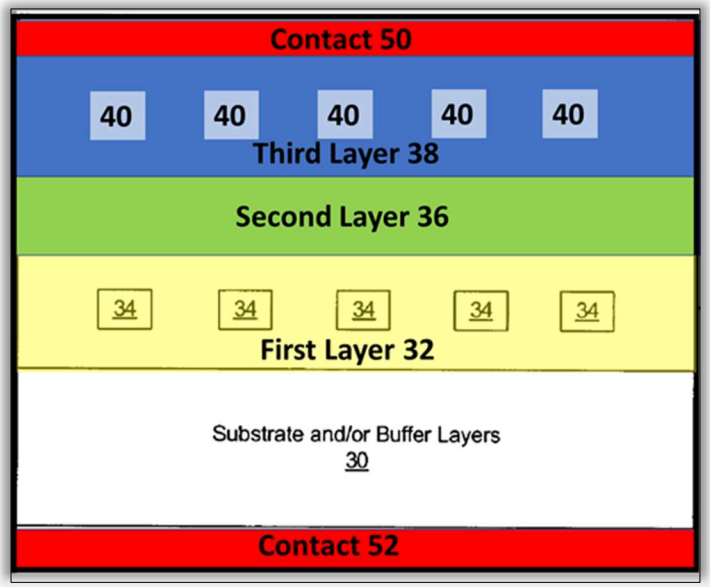
A. Independent Claim 1

Preamble: A semiconductor heterostructure, comprising:

To the extent that the preamble is limiting, Saxler discloses this subject matter. Ex[1002], ¶124. For example, Saxler discloses a Group III nitride based semiconductor structure (e.g., gallium nitride-based light emitting diode) and a vertical semiconductor diode structure. Ex[1007] at ¶¶[0016]-[0017], Fig. 4.

[1a] an active region;

Saxler discloses an active region. Ex[1002], ¶125. For example, Saxler discloses that an "optional second layer 36 of a third semiconductor material(s) may be provided between the first layer 32 and a third layer 38 and may have a lower bandgap than that of the first layer 32 and the third layer 38 to provide a well region for the device." Ex[1007] at ¶[0026]. Annotated FIG. 4 of Saxler, below, shows the active region (layer 36, shaded in green):



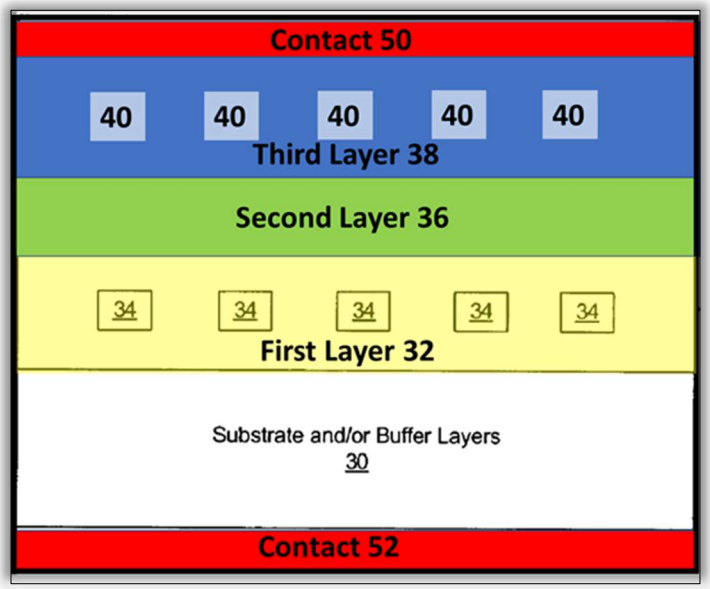
(Annotated FIG. 4 of Saxler)

Ex[1002], ¶125. Saxler also discloses that "the first layer 32, second layer 36 and/or third layer 38 may be multiple layers, for example, in a multi-quantum well embodiment of the present invention." Ex[1007] at ¶[0028]. A POSITA would have understood "that because FIG. 4 represents a vertical diode structure that can

be applied to light emitting devices, the 'well region' or 'multi-quantum well' semiconductor layers disclosed by Saxler are active regions for the semiconductor device." Ex[1002], ¶123.

[1b] a metallic contact;

Saxler discloses a metallic contact. Ex[1002], ¶126. For example, Saxler discloses that contact 50 can be provided above the third layer 38. Ex[1007] at ¶[0026], Fig. 4. A POSITA would have understood "that contact 50 (and alternatively, contact 52) is a metallic contact of the semiconductor device; specifically, a POSITA would understand that contact 50 is an ohmic contact made of metal." Ex[1002], ¶126. Annotated FIG. 4 of Saxler, below, shows a metallic contact (contact 50 or contact 52, shaded in red):



(Annotated FIG. 4 of Saxler)

Id. Furthermore, Saxler incorporates by reference U.S. Patent No. 6,201,262, which discloses forming an ohmic contact to a conductive substrate. *Id*.; Ex[1019], 8:20-38.

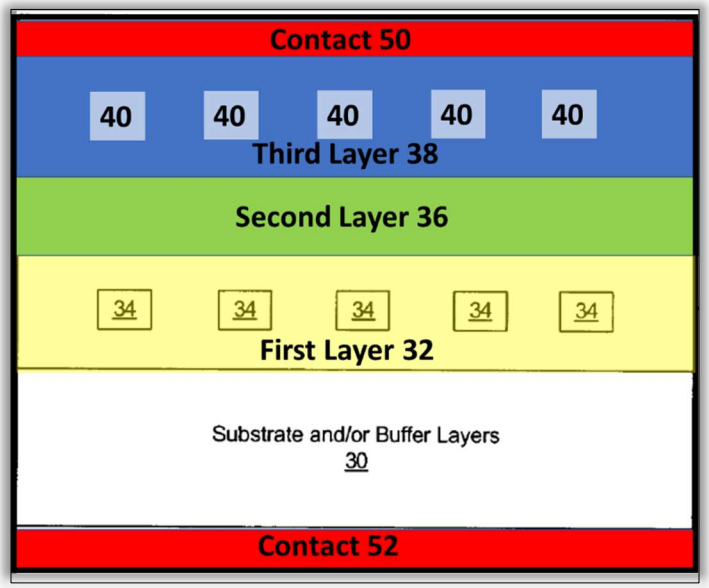
[1c] a group III nitride semiconductor layer located between the active region and the metallic contact;

Saxler discloses this limitation. Ex[1002], ¶¶127-129. For example, Saxler describes that "the third layer 38 and the regions 40 are both AlInGaN based materials." Ex[1007] at ¶[0027]. Saxler also discloses that the "third layer 38 is a fourth wide bandgap semiconductor material" and "incorporated in the third layer 38 are regions 40 of a fifth wide bandgap semiconductor material." *Id.*

A POSITA would have understood that the "wide bandgap semiconductor material" and "AlInGaN based material" of Saxler are group III nitride semiconductor materials. Ex[1002], ¶128. Indeed, Saxler discloses that "the wide bandgap material is a Group III nitride," such as "a gallium nitride based semiconductor material, such as GaN, AlGaN, AlInGaN or the like." Ex[1007] at ¶[0010]. Therefore, the third layer 38 (and first layer 32) of Saxler is a group III nitride semiconductor layer. Ex[1002], ¶128.

Saxler further discloses that first layer 32 or third layer 38 (each is a group III nitride semiconductor layer) is located between the active region and the metallic contact. *Id*. at ¶129. Annotated FIG. 4 of Saxler, below, shows a group

III nitride semiconductor layer (first layer 32 or third layer 38) located between the active region (layer 36, shaded in green) and the metallic contact (contact 50 or contact 52, shaded in red).



(Annotated FIG. 4 of Saxler)

Id.

[1d] the semiconductor layer including a plurality of inhomogeneous regions arranged within multiple levels of the semiconductor layer along a height direction of the semiconductor layer;

Saxler discloses this limitation. Ex[1002], ¶¶130-134. For example, Saxler discloses "a first layer 20 of wide bandgap semiconductor material having a first bandgap has included therein regions 22 of wide bandgap semiconductor material having a second bandgap"; "the layer 20 has a narrower bandgap than the regions 22"; "most of the doping is provided in the regions 22 to minimize ionized

impurity scattering and maximize ionization of dopants"; "[b]y providing regions 22, rather than continuous layers, improved electrical conductivity in the vertical direction (i.e. a direction substantially orthogonal to the growth plane) may be achieved"; and "regions 22 may be provided that are aligned, staggered and/or random relative to each other." Ex[1007] at ¶¶[0018]-[0021]. Saxler further teaches that "regions 22 may be provided by a blanket formation of a layer of the wider bandgap semiconductor material and the patterning of that layer." *Id.* at ¶[0023].

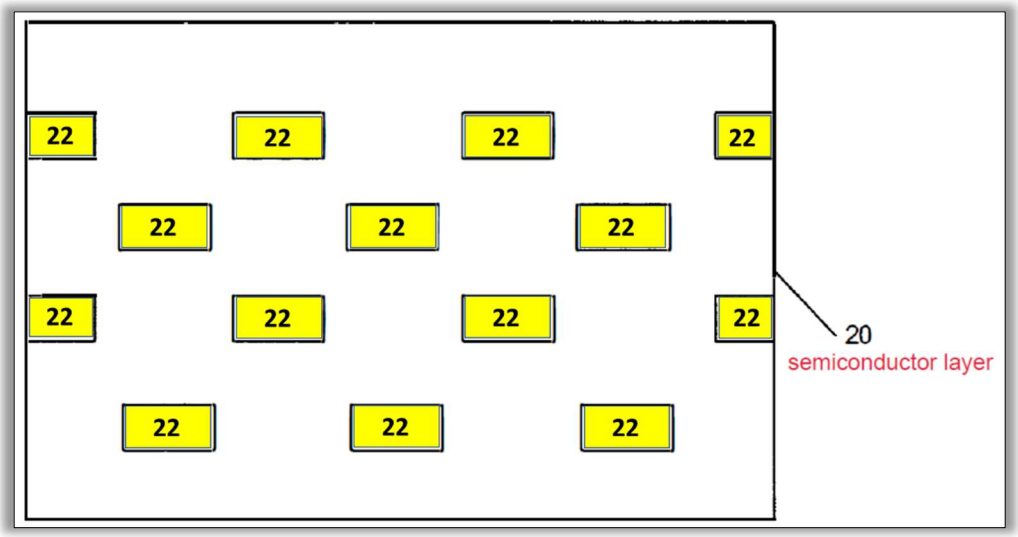
As Dr. Shealy explains, "the regions 22 constitute inhomogeneous regions because these regions can include wider bandgap material, transparent regions, and contribute to higher electrical conductivity of the semiconductor layer 20 in which the regions 22 are embedded." Ex[1002], ¶131. The '117 Patent teaches that:

> Each inhomogeneous region has <u>one or more attributes that differ</u> from a material forming the semiconductor layer. The inhomogeneous regions can include one or more regions configured based on radiation having a target wavelength. These regions can include <u>transparent and/or reflective regions</u>. The inhomogeneous regions also can include one or more regions having a <u>higher conductivity</u> than a conductivity of the radiation-based regions, e.g., at least ten percent higher.

Ex[1001], 2:5-13 (emphasis added).

The ’117 Patent also discloses that a “conductive region can be configured to promote conductivity of carriers in the semiconductor structure,” and a “conductive region can have a higher concentration of carriers due to, for example, a locally reduced band gap of the semiconductor layer, a local high doping of the semiconductor layer, and/or the like.” *Id.* at 5:60-65 (emphasis added). Furthermore, the ’117 Patent describes that the “semiconductor structure can include inhomogeneous regions formed by one or more of patterning, masking, epitaxial growth, epitaxial overgrowth, deposition techniques, and/or the like.” *Id*. at 4:11-14.

Similarly, annotated FIG. 3 of Saxler, below, shows the semiconductor layer 20 including a plurality of inhomogeneous regions (the regions 22, shaded in yellow) arranged within multiple levels of the semiconductor layer (layer 20) along a height direction (vertical direction) of the semiconductor layer.



(Annotated FIG. 3 of Saxler)

"A POSITA would have understood that layer 20 with embedded regions 22 can be applied to the diode structure shown in FIG. 4 of Saxler." Ex[1002], ¶133. In fact, Saxler's teaching of the regions 22 embedded in the layer 20 can be applied to any light emitting diode structure. *See* Ex[1007] at ¶[0030]; Ex[1002], ¶133. For example, Saxler discloses that "FIG. 4 illustrates the utilization of embodiments of the present invention in a simplified vertical diode structure" and "third layer 38 is a fourth wide bandgap semiconductor material," and "[i]ncorporated in the third layer 38 are regions 40 of a fifth wide bandgap semiconductor material where the bandgap of the fourth wide bandgap semiconductor material is narrower than the bandgap of the fifth wide bandgap semiconductor material." Ex[1007] at ¶¶[0024], [0027] (emphasis added).

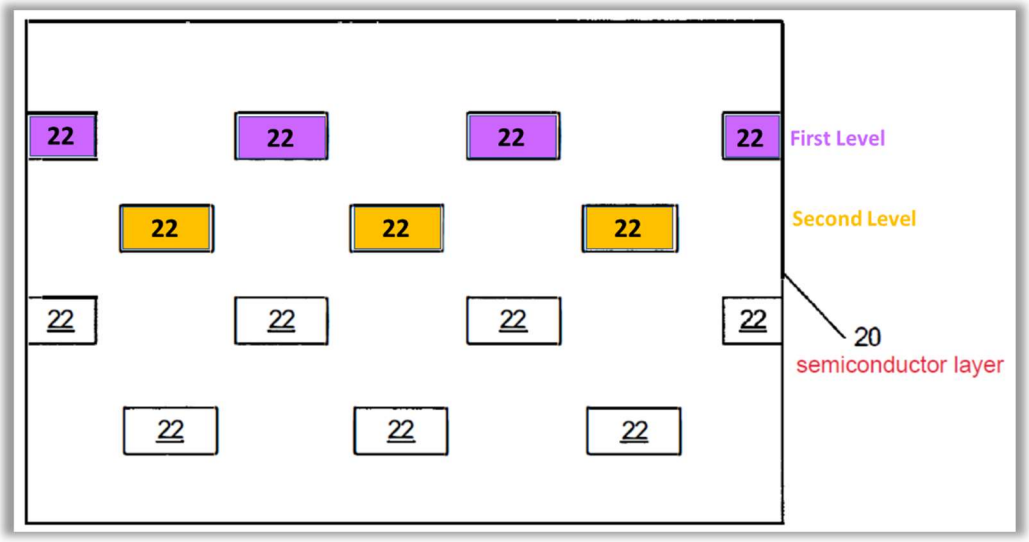
Accordingly, a POSITA would have understood "that Saxler's teaching of the regions 22 embedded in the layer 20 can be applied to first layer 32 (which includes embedded regions 34) and third layer 38 (which includes embedded regions 40) of FIG. 4 of Saxler." Ex[1002], ¶134. Indeed, Saxler expressly discloses that embodiments of its invention (e.g., its teaching of the regions 22 embedded in the layer 20) can be applied to other light emitting diode structures and incorporated by reference several disclosures. *See* Ex[1007] at ¶[0030]. Saxler therefore discloses this limitation or at least renders it obvious. *See* Ex[1002], ¶134.

Therefore, the Applicant misrepresented or ignored Saxler's disclosures during original prosecution of the '117 Patent with respect to this limitation, and the Examiner, who did not make any specific findings regarding Saxler, erred in allowing Claim 1 over a rejection based in part on Saxler. *See* Ex[1018].

[1e] wherein some of the inhomogeneous regions in a first level of the semiconductor layer are vertically offset from inhomogeneous regions in a second level of the semiconductor layer, and,

Saxler discloses this limitation. Ex[1002], ¶135. For example, Saxler discloses that "the layer 20 includes differing courses of regions 22 that are staggered." Ex[1007] at ¶[0021]. Annotated FIG. 3 of Saxler, below, shows the inhomogeneous regions in a first level (the regions 22, shaded in purple) of the

semiconductor layer are vertically offset from inhomogeneous regions in a second level (the regions 22, shaded in orange) of the semiconductor layer.



(Annotated FIG. 3 of Saxler)

Ex[1002], ¶135.

[1f] wherein the plurality of inhomogeneous regions include one or more of a set of transparent regions, a set of reflective regions and/or a set of conductive regions,

Saxler discloses this limitation. Ex[1002], ¶¶136-141. For example, Saxler discloses "a first layer 20 of wide bandgap semiconductor material having a first bandgap has included therein regions 22 of wide bandgap semiconductor material having a second bandgap"; "the layer 20 has a narrower bandgap than the regions 22"; "most of the doping is provided in the regions 22 to minimize ionized impurity scattering and maximize ionization of dopants"; and "[b]y providing regions 22, rather than continuous layers, improved electrical conductivity in the

vertical direction (i.e. a direction substantially orthogonal to the growth plane) may be achieved." Ex[1007] at ¶¶[0018]-[0020] (emphasis added).

The '117 Patent teaches that a "conductive region can be configured to promote conductivity of carriers in the semiconductor structure," and a "conductive region can have a higher concentration of carriers due to, for example, a locally reduced band gap of the semiconductor layer, a local high doping of the semiconductor layer, and/or the like." Ex[1001], 5:60-65 (emphasis added). The '117 Patent further discloses that "a conductive region has a conductivity at least ten percent higher than a conductivity of a transparent region and a conductivity of a reflective region and a higher conductivity than a base semiconductor material for the layer." *Id.* at 6:5-9 (emphasis added). The '117 Patent also explains that "a region is a transparent region when the region allows at least ten percent of radiation having a target wavelength, which is radiated at a normal incidence to an interface of the region, to pass there through." *Id.* at 5:46-49 (emphasis added).

A POSITA would have understood "that because the regions 22 have higher doping and contribute to improved electrical conductivity, the regions 22 are conductive regions." Ex[1002], ¶138. A POSITA would have also understood "that because Saxler teaches regions 22 have wider bandgap than the layer 20 in which the regions 22 are embedded, the regions 22 allows for higher optical

transmission and are transparent regions." *Id*.

And, again, Saxler's teaching of the regions 22 embedded in the layer 20 can be applied to any light emitting diode structure. Ex[1007] at ¶[0030]. For example, Saxler discloses that "FIG. 4 illustrates the utilization of embodiments of the present invention in a simplified vertical diode structure" and "third layer 38 is a fourth wide bandgap semiconductor material," and "[i]ncorporated in the third layer 38 are regions 40 of a fifth wide bandgap semiconductor material where the bandgap of the fourth wide bandgap semiconductor material is narrower than the bandgap of the fifth wide bandgap semiconductor material." Ex[1007] at ¶¶[0024], [0027] (emphasis added).

A POSITA would have understood "that in the exemplary diode structure of FIG. 4 of Saxler, the third layer 38 (which is the p-type layer) and first layer 32 (which is the n-type layer) must have a wider bandgap than the quantum well light emitting layer 36 so that third layer 38 and first layer 32 are transparent to the target wavelength of the light emitting diode and the light emitted from the light emitting layer 36 is not absorbed." Ex[1002], ¶140. A POSITA would have also understood "that because the regions 40 embedded in the third layer 38 (and regions 34 embedded in the first layer 32) have wider bandgap than third layer 38, such regions 40 (and regions 34) are likewise transparent to the target wavelength

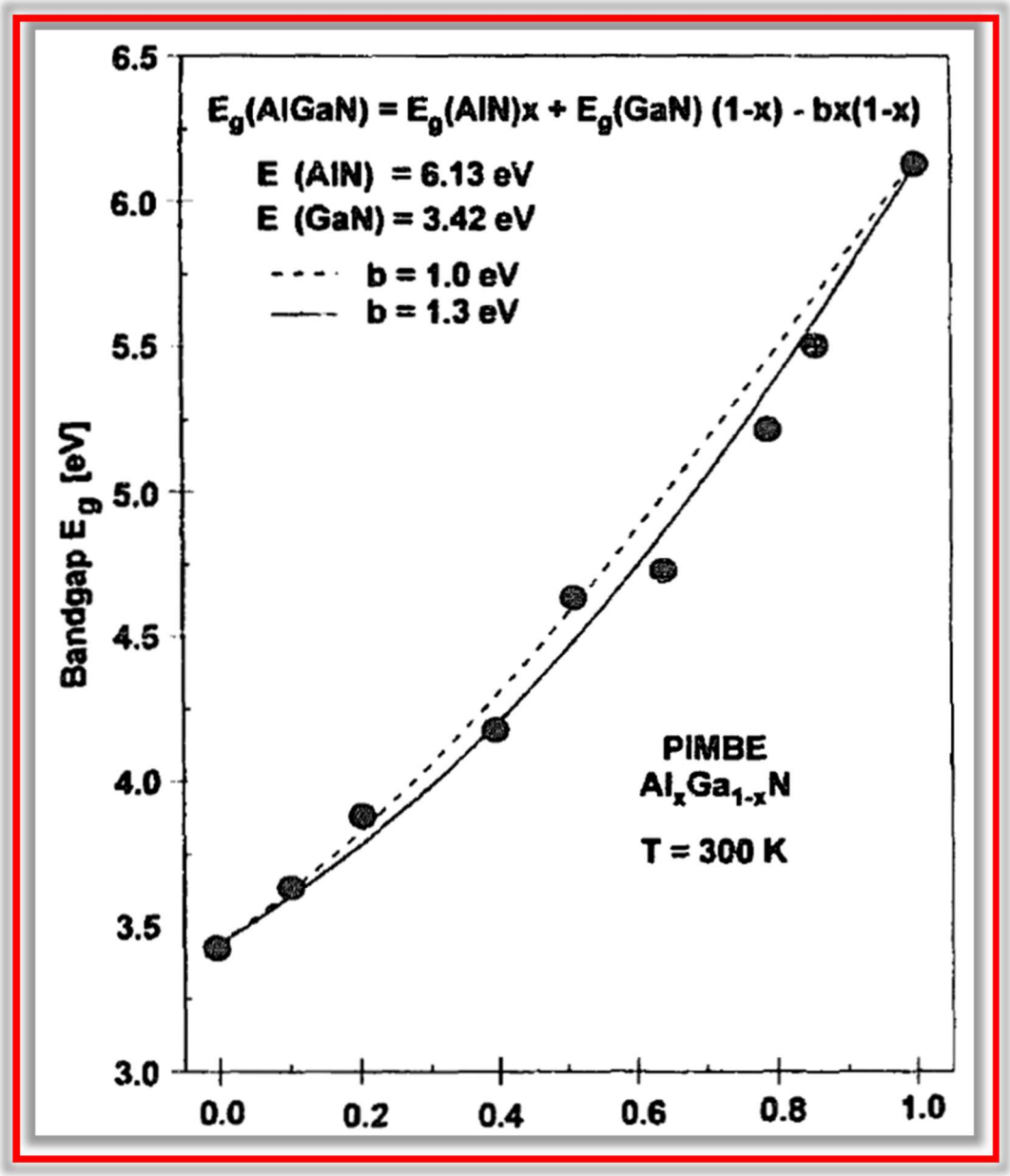
of the light emitting diode." *Id*. As such, a POSITA would have understood "that similar to the regions 22, the regions 40 (and regions 34) are also transparent regions." *Id*.

Therefore, Saxler discloses wherein the plurality of inhomogeneous regions include one or more of a set of transparent regions, a set of reflective regions and/or a set of conductive regions. *Id*. at ¶141.

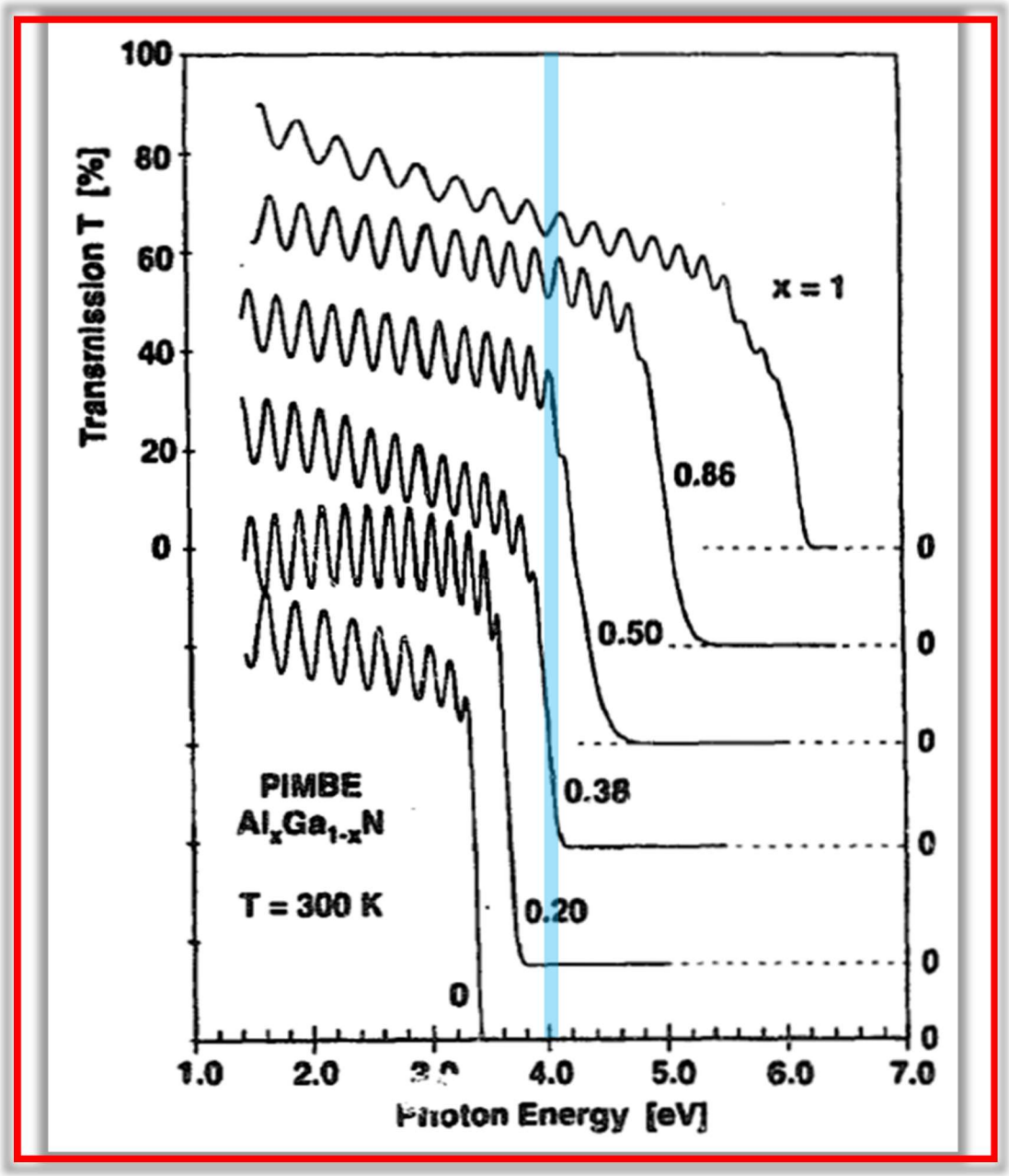
[1g] each of the inhomogeneous regions having a set of attributes differing from a group III nitride material forming the semiconductor layer.

Saxler discloses this limitation. Ex[1002], ¶¶142-144. For example, Saxler discloses that the regions 22 and regions 40 (and regions 34) have wider bandgap than the layer 20/layer 38 in which they are embedded: "In any case, the layer 20 has a narrower bandgap than the regions 22," "the composition of the regions 22 and the layer 20 may be the same, however, the mole fractions may be varied to provide differing bandgaps," and "[t]he third layer 38 is a fourth wide bandgap semiconductor material," and "[i]ncorporated in the third layer 38 are regions 40 of a fifth wide bandgap semiconductor material where the bandgap of the fourth wide bandgap semiconductor material is narrower than the bandgap of the fifth wide bandgap semiconductor material." Ex[1007] at ¶¶[0019], [0027] (emphasis added).

A POSITA would have understood "that because the regions 22/regions 40/regions 34 have wider bandgap and different composition mole fraction than the layer 20/layer 38/layer 32 in which the regions 22/regions 40/regions 34 are embedded, the regions 22/regions 40/regions 34 have material attributes (*e.g.*, bandgap, composition mole fraction, and/or optical transmission) from the layer 20/layer 38/layer 32." Ex[1002], ¶143. In fact, it was well-known to a POSITA "that higher Al concentration in AlGaN results in a wider bandgap," as shown for example in Figure 4 of Stutzmann (a 1998 publication titled "Electrical and structure properties of AlGaN: a comparison with CVD diamond"), which shows that the optical transmission for AlGaN increases with higher Al concentration. Ex[1002], ¶143 (citing Ex[1017]). For example, for a photon energy of 4 eV (which equates to UV emission at about 310 nm, as shown by a vertical blue bar), FIG. 4 of Stutzmann shows that the optical transmission is about 60% when the Al concentration, x = 0.86, and about 40% when x = 0.5:



(FIG. 3 of Stutzmann)



(Annotated FIG. 4 of Stutzmann)

Ex[1002], ¶143. Thus, Saxler discloses that each of the inhomogeneous regions have a set of attributes different from a group III nitride material forming the semiconductor layer. *Id*. at ¶144.

Accordingly, Saxler discloses this limitation and renders obvious Claim 1 of the '117 Patent. *See also id*. at ¶145.

XIII. INSTITUTION IS APPROPRIATE UNDER 35 U.S.C. § 325(d).

Section 325(d) does not prevent institution of this Petition even though Saxler was considered and Shur was cited but not discussed during prosecution of the '117 Patent. Under Section 325(d), "[i]n determining whether to institute or order a proceeding . . . the Director may take into account whether, and reject the 5 petition or request because, the same or substantially the same prior art or arguments previously were presented to the Office." 35 U.S.C. § 325(d). Analysis under Section 325(d) breaks down into two prongs: (1) "whether the same or substantially the same art previously was presented to the Office or whether the same or substantially the same arguments previously were presented to the Office"; and, if so, (2) "whether the petitioner has demonstrated that the Office erred in a manner material to the patentability of the challenged claims." *Advanced Bionics LLC v. Med-EL Elektromedizinische Geräte* GMBH, IPR2019-01469, Paper 6 at 8-11 (PTAB Feb. 13, 2020 (citing the *Becton, Dickinson* factors) (precedential).

Thus, that Saxler was considered during prosecution, as discussed above, does not prevent institution under Section 325(d). Saxler was not considered alone, and, in any event, the Applicant only argued that the combination of Saxler '514 and Saxler "does not disclose or suggest a single semiconductor layer having a plurality of inhomogeneous regions arranged within multiple levels of the single semiconductor structure." Ex[1008], 74. As the Petition establishes with respect to limitation 1d in Ground 4, the Applicant was wrong. The prior art, as well as Petitioner's expert testimony—which was not before the PTO during prosecution—shows that Saxler discloses this claimed structure and at least renders it obvious. A material error therefore occurred during prosecution of the '117 Patent because Saxler discloses the limitations of Claim 1, the Applicant mispresented or ignored Saxler's disclosures, and the Examiner allowed Claim 1 to issue without any specific findings regarding Saxler (Ex. 1018). *See SharkNinja v. iRobot*, IPR2020-00733, Paper 11 at 42 (October 6, 2020) ("Material error may include, for example, an examiner 'misapprehending or overlooking specific teachings of the relevant prior art where those teachings impact patentability of the challenged claims.' Moreover, 'if the record of the Office's previous consideration of the art is not well developed or silent, then a petitioner may show the Office erred by overlooking something persuasive.') (quoting *Advanced Bionics*). Thus,

even if Patent Owner can establish that the first prong of the *Advanced Bionics* test is met, Section 325(d) does not support discretionary denial here.

Furthermore, the prior art Ohmae and Ban references presented in this Petition were not cited or considered during prosecution of the '117 Patent.

Previous PTAB precedent therefore confirms that Section 325(d) does not prevent institution here. For example, the decision in *Praxair* is instructive. There, even though the Board found that two primary references were cited during prosecution, and one was actually relied upon by the Office in rejecting challenged claims, institution was proper because the proposed grounds of invalidity also included additional references not before the examiner. *Praxair Distribution, Inc. v. Ino Therapeutics, LLC*, IPR2015-00893, paper 14 at 8-9 (PTAB Sept. 22, 2015) 15 ("Patent Owner does not identify with specificity where 'substantially the same . . . arguments'—substantially the same combinations of references—were before the Examiner."); *see also Amber.IO, Inc. D/B/A Two Tap v. 72Lux, Inc. D/B/A Shoppable*, IPR2020-00015, Paper 8 at 18-20 (PTAB April 1, 2020); *Apple, Inc. v. Omni Medsci, Inc*., IPR2020-00029, Paper 7 at 52-55 (PTAB April 22, 2020); *Navistar, Inc. v. Fatigue Fracture Tech., LLC*, IPR2018-00853, Paper 13 at 17 (Sept. 12, 2018) (ruling "the fact that [references] were of record, but not

applied in any rejection by the Examiner . . . provides little impetus for us to exercise our discretion to deny institution under § 325(d)").

XIV. CONCLUSION

For the foregoing reasons, Petitioner respectfully requests that a trial for *inter partes* review of the '117 Patent be instituted and that Claim 1 be cancelled.

Dated: March 29, 2022

Respectfully submitted,

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CERTIFICATE OF COMPLIANCE

1. The undersigned certifies that this brief complies with the type volume limitations of 37 CFR § 42.24(a)(1)(i). This brief contains 10,992 words (excluding the table of contents, the table of authorities, mandatory notices under 37 CFR § 42.8, the certificate of service, certificate of compliance, and appendix of exhibits), as calculated by the "Word Count" feature of Microsoft Word 360, the word processing program used to create it.

2. The undersigned further certifies that this brief complies with the typeface requirements of 37 CFR § 42.6(a)(2)(ii) and typestyle requirements of 37 CFR § 42.6(a)(2)(iii). This brief has been prepared in a proportionally spaced typeface using Microsoft Word in Times New Roman 14-point font

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CERTIFICATE OF SERVICE

The undersigned hereby certifies that a true copy of the foregoing

PETITION FOR *INTER PARTES* REVIEW OF U.S. PATENT NO. 9,923,117

and supporting materials have been served in its entirety by FedEx on March 29, 2022 on Patent Owner at the correspondence address for the attorney of record for U.S. Patent No. 9,923,117 shown in USPTO PAIR:

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