PTO/SB/80 (11-08)
Approved for use through 11/30/2011. OMB 0651-0035
U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE

POWER OF ATTORNEY TO PROSECUTE APPLICATIONS BEFORE THE USPTO

I hereby revoke all previous powers of attorney given in the application identified in the attached statement under 37 CFR 3.73(b).

I hereby appoint:

☑ Practitioners associated with the Customer Number: 11698

OR

☐ Practitioner(s) named below (if more than ten patent practitioners are to be named, then a customer number must be used):

Name	Registration Number	Name	Registration Number

as attorney(s) or agent(s) to represent the undersigned before the United States Patent and Trademark Office (USPTO) in connection with any and all patent applications assigned only to the undersigned according to the USPTO assignment records or assignment documents attached to this form in accordance with 37 CFR 3.73(b).

Please change the correspondence address for the application identified in the attached statement under 37 CFR 3.73(b) to:

☑ The address associated with Customer Number: 11698

OR

☐ Firm or Individual Name			
Address			
City		State	Zip
Country			
Telephone		Email	

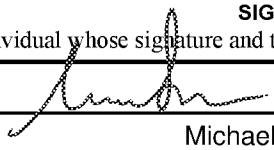
Assignee Name and Address:

Sensor Electronic Technology, Inc.
1195 Atlas Road
Columbia, SC 29209

A copy of this form, together with a statement under 37 CFR 3.73(b) (Form PTO/SB/96 or equivalent) is required to be filed in each application in which this form is used. The statement under 37 CFR 3.73(b) may be completed by one of the practitioners appointed in this form if the appointed practitioner is authorized to act on behalf of the assignee, and must identify the application in which this Power of Attorney is to be filed.

SIGNATURE of Assignee of Record

The individual whose signature and title is supplied below is authorized to act on behalf of the assignee

Signature		Date	02/15/2013
Name	Michael Shur	Telephone	+1(518) 253 6819
Title	Vice-President		

If you need assistance in completing the form, call 1-800-PTO-9199 and select option 2.

Privacy Act Statement

The **Privacy Act of 1974 (P.L. 93-579)** requires that you be given certain information in connection with your submission of the attached form related to a patent application or patent. Accordingly, pursuant to the requirements of the Act, please be advised that: (1) the general authority for the collection of this information is 35 U.S.C. 2(b)(2); (2) furnishing of the information solicited is voluntary; and (3) the principal purpose for which the information is used by the U.S. Patent and Trademark Office is to process and/or examine your submission related to a patent application or patent. If you do not furnish the requested information, the U.S. Patent and Trademark Office may not be able to process and/or examine your submission, which may result in termination of proceedings or abandonment of the application or expiration of the patent.

The information provided by you in this form will be subject to the following routine uses:

1. The information on this form will be treated confidentially to the extent allowed under the Freedom of Information Act (5 U.S.C. 552) and the Privacy Act (5 U.S.C 552a). Records from this system of records may be disclosed to the Department of Justice to determine whether disclosure of these records is required by the Freedom of Information Act.
2. A record from this system of records may be disclosed, as a routine use, in the course of presenting evidence to a court, magistrate, or administrative tribunal, including disclosures to opposing counsel in the course of settlement negotiations.
3. A record in this system of records may be disclosed, as a routine use, to a Member of Congress submitting a request involving an individual, to whom the record pertains, when the individual has requested assistance from the Member with respect to the subject matter of the record.
4. A record in this system of records may be disclosed, as a routine use, to a contractor of the Agency having need for the information in order to perform a contract. Recipients of information shall be required to comply with the requirements of the Privacy Act of 1974, as amended, pursuant to 5 U.S.C. 552a(m).
5. A record related to an International Application filed under the Patent Cooperation Treaty in this system of records may be disclosed, as a routine use, to the International Bureau of the World Intellectual Property Organization, pursuant to the Patent Cooperation Treaty.
6. A record in this system of records may be disclosed, as a routine use, to another federal agency for purposes of National Security review (35 U.S.C. 181) and for review pursuant to the Atomic Energy Act (42 U.S.C. 218(c)).
7. A record from this system of records may be disclosed, as a routine use, to the Administrator, General Services, or his/her designee, during an inspection of records conducted by GSA as part of that agency's responsibility to recommend improvements in records management practices and programs, under authority of 44 U.S.C. 2904 and 2906. Such disclosure shall be made in accordance with the GSA regulations governing inspection of records for this purpose, and any other relevant (*i.e.*, GSA or Commerce) directive. Such disclosure shall not be used to make determinations about individuals.
8. A record from this system of records may be disclosed, as a routine use, to the public after either publication of the application pursuant to 35 U.S.C. 122(b) or issuance of a patent pursuant to 35 U.S.C. 151. Further, a record may be disclosed, subject to the limitations of 37 CFR 1.14, as a routine use, to the public if the record was filed in an application which became abandoned or in which the proceedings were terminated and which application is referenced by either a published application, an application open to public inspection or an issued patent.
9. A record from this system of records may be disclosed, as a routine use, to a Federal, State, or local law enforcement agency, if the USPTO becomes aware of a violation or potential violation of law or regulation.

PTO/AIA/14 (11-15)
Approved for use through 04/30/2017. OMB 0651-0032
U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE

Application Data Sheet 37 CFR 1.76	Attorney Docket Number	SETI-0110-CIP-US
	Application Number	
Title of Invention	Semiconductor Structure with Inhomogeneous Regions	

The application data sheet is part of the provisional or nonprovisional application for which it is being submitted. The following form contains the bibliographic data arranged in a format specified by the United States Patent and Trademark Office as outlined in 37 CFR 1.76.
This document may be completed electronically and submitted to the Office in electronic format using the Electronic Filing System (EFS) or the document may be printed and included in a paper filed application.

Secrecy Order 37 CFR 5.2:

☐ Portions or all of the application associated with this Application Data Sheet may fall under a Secrecy Order pursuant to 37 CFR 5.2 (Paper filers only. Applications that fall under Secrecy Order may not be filed electronically.)

Inventor Information:

Inventor 1 Remove

Legal Name

Prefix	Given Name	Middle Name	Family Name	Suffix
	Maxim	S.	Shatalov	

Residence Information (Select One) ● US Residency ○ Non US Residency ○ Active US Military Service

City	State/Province	Country of Residence
Columbia	SC	US

Mailing Address of Inventor:

Address 1	Sensor Electronic Technology, Inc.
Address 2	1195 Atlas Road

City	State/Province	Postal Code	Country
Columbia	SC	29209	US

Inventor 2 Remove

Legal Name

Prefix	Given Name	Middle Name	Family Name	Suffix
	Alexander		Dobrinsky	

Residence Information (Select One) ◉ US Residency ○ Non US Residency ○ Active US Military Service

City	State/Province	Country of Residence
Loudonville	NY	US

Mailing Address of Inventor:

Address 1	23 Green Meadows Lane
Address 2	

City	State/Province	Postal Code	Country
Loudonville	NY	12211	US

Inventor 3 Remove

Legal Name

Prefix	Given Name	Middle Name	Family Name	Suffix
	Alexander		Lunev	

Residence Information (Select One) ◉ US Residency ○ Non US Residency ○ Active US Military Service

Application Data Sheet 37 CFR 1.76	Attorney Docket Number	SETI-0110-CIP-US
	Application Number	
Title of Invention	Semiconductor Structure with Inhomogeneous Regions	

City	Columbia	State/Province	SC	Country of Residence	US

Mailing Address of Inventor:

Address 1	117 Park Shore Drv. East		
Address 2			
City	Columbia	State/Province	SC
Postal Code	29223	Country	US

Inventor 4 Remove

Legal Name

Prefix	Given Name	Middle Name	Family Name	Suffix
	Rakesh		Jain	

Residence Information (Select One) ◉ US Residency ○ Non US Residency ○ Active US Military Service

City	Columbia	State/Province	SC	Country of Residence	US

Mailing Address of Inventor:

Address 1	Sensor Electronic Technology, Inc.		
Address 2	1195 Atlas Road		
City	Columbia	State/Province	SC
Postal Code	29209	Country	US

Inventor 5 Remove

Legal Name

Prefix	Given Name	Middle Name	Family Name	Suffix
	Jinwei		Yang	

Residence Information (Select One) ◉ US Residency ○ Non US Residency ○ Active US Military Service

City	Columbia	State/Province	SC	Country of Residence	US

Mailing Address of Inventor:

Address 1	Sensor Electronic Technology, Inc.		
Address 2	1195 Atlas Road		
City	Columbia	State/Province	SC
Postal Code	29209	Country	US

Inventor 6 Remove

Legal Name

Prefix	Given Name	Middle Name	Family Name	Suffix
	Michael		Shur	

Residence Information (Select One) ◉ US Residency ○ Non US Residency ○ Active US Military Service

City	Latham	State/Province	NY	Country of Residence	US

PTO/AIA/14 (11-15)
Approved for use through 04/30/2017. OMB 0651-0032
U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE

Application Data Sheet 37 CFR 1.76	Attorney Docket Number	SETI-0110-CIP-US
	Application Number	
Title of Invention	Semiconductor Structure with Inhomogeneous Regions	

Mailing Address of Inventor:

Address 1	10 Starboard Way		
Address 2			
City	Latham	**State/Province**	NY
Postal Code	12110	**Country** i	US

Inventor 7 Remove

Legal Name

Prefix	Given Name	Middle Name	Family Name	Suffix
	Remigijus		Gaska	

Residence Information (Select One) ◉ US Residency ○ Non US Residency ○ Active US Military Service

City	Columbia	**State/Province**	SC	**Country of Residence** i	US

Mailing Address of Inventor:

Address 1	432 Press Lindler Road		
Address 2			
City	Columbia	**State/Province**	SC
Postal Code	29212	**Country** i	US

All Inventors Must Be Listed - Additional Inventor Information blocks may be generated within this form by selecting the **Add** button. Add

Correspondence Information:

Enter either Customer Number or complete the Correspondence Information section below.
For further information see 37 CFR 1.33(a).

☐ **An Address is being provided for the correspondence Information of this application.**

Customer Number	11698		
Email Address		Add Email	Remove Email

Application Information:

Title of the Invention	Semiconductor Structure with Inhomogeneous Regions		
Attorney Docket Number	SETI-0110-CIP-US	**Small Entity Status Claimed**	☐
Application Type	Nonprovisional		
Subject Matter	Utility		
Total Number of Drawing Sheets (if any)	15	**Suggested Figure for Publication (if any)**	

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Application Data Sheet 37 CFR 1.76	Attorney Docket Number	SETI-0110-CIP-US
	Application Number	
Title of Invention	Semiconductor Structure with Inhomogeneous Regions	

Filing By Reference:

Only complete this section when filing an application by reference under 35 U.S.C. 111(c) and 37 CFR 1.57(a). Do not complete this section if application papers including a specification and any drawings are being filed. Any domestic benefit or foreign priority information must be provided in the appropriate section(s) below (i.e., "Domestic Benefit/National Stage Information" and "Foreign Priority Information").

For the purposes of a filing date under 37 CFR 1.53(b), the description and any drawings of the present application are replaced by this reference to the previously filed application, subject to conditions and requirements of 37 CFR 1.57(a).

Application number of the previously filed application	Filing date (YYYY-MM-DD)	Intellectual Property Authority or Country

Publication Information:

☐ Request Early Publication (Fee required at time of Request 37 CFR 1.219)

☐ **Request Not to Publish.** I hereby request that the attached application not be published under 35 U.S.C. 122(b) and certify that the invention disclosed in the attached application **has not and will not** be the subject of an application filed in another country, or under a multilateral international agreement, that requires publication at eighteen months after filing.

Representative Information:

Representative information should be provided for all practitioners having a power of attorney in the application. Providing this information in the Application Data Sheet does not constitute a power of attorney in the application (see 37 CFR 1.32).
Either enter Customer Number or complete the Representative Name section below. If both sections are completed the customer Number will be used for the Representative Information during processing.

Please Select One:	● Customer Number	US Patent Practitioner	○ Limited Recognition (37 CFR 11.9)
Customer Number	11698		

Domestic Benefit/National Stage Information:

This section allows for the applicant to either claim benefit under 35 U.S.C. 119(e), 120, 121, 365(c), or 386(c) or indicate National Stage entry from a PCT application. Providing benefit claim information in the Application Data Sheet constitutes the specific reference required by 35 U.S.C. 119(e) or 120, and 37 CFR 1.78.
When referring to the current application, please leave the "Application Number" field blank.

Prior Application Status	Pending		Remove
Application Number	Continuity Type	Prior Application Number	Filing or 371(c) Date (YYYY-MM-DD)
	Continuation in part of	14189012	2014-02-25

PTO/AIA/14 (11-15)
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Application Data Sheet 37 CFR 1.76	Attorney Docket Number	SETI-0110-CIP-US
	Application Number	
Title of Invention	Semiconductor Structure with Inhomogeneous Regions	

Prior Application Status	Expired		Remove
Application Number	Continuity Type	Prior Application Number	Filing or 371(c) Date (YYYY-MM-DD)
14189012	Claims benefit of provisional	61768581	2013-02-25

Additional Domestic Benefit/National Stage Data may be generated within this form by selecting the **Add** button. Add

Foreign Priority Information:

This section allows for the applicant to claim priority to a foreign application. Providing this information in the application data sheet constitutes the claim for priority as required by 35 U.S.C. 119(b) and 37 CFR 1.55. When priority is claimed to a foreign application that is eligible for retrieval under the priority document exchange program (PDX)[i] the information will be used by the Office to automatically attempt retrieval pursuant to 37 CFR 1.55(i)(1) and (2). Under the PDX program, applicant bears the ultimate responsibility for ensuring that a copy of the foreign application is received by the Office from the participating foreign intellectual property office, or a certified copy of the foreign priority application is filed, within the time period specified in 37 CFR 1.55(g)(1).

Remove

Application Number	Country[i]	Filing Date (YYYY-MM-DD)	Access Code[i] (if applicable)

Additional Foreign Priority Data may be generated within this form by selecting the **Add** button. Add

Statement under 37 CFR 1.55 or 1.78 for AIA (First Inventor to File) Transition Applications

☒ This application (1) claims priority to or the benefit of an application filed before March 16, 2013 and (2) also contains, or contained at any time, a claim to a claimed invention that has an effective filing date on or after March 16, 2013.
NOTE: By providing this statement under 37 CFR 1.55 or 1.78, this application, with a filing date on or after March 16, 2013, will be examined under the first inventor to file provisions of the AIA.

Application Data Sheet 37 CFR 1.76	Attorney Docket Number	SETI-0110-CIP-US
	Application Number	
Title of Invention	Semiconductor Structure with Inhomogeneous Regions	

Authorization or Opt-Out of Authorization to Permit Access:

When this Application Data Sheet is properly signed and filed with the application, applicant has provided written authority to permit a participating foreign intellectual property (IP) office access to the instant application-as-filed (see paragraph A in subsection 1 below) and the European Patent Office (EPO) access to any search results from the instant application (see paragraph B in subsection 1 below).

Should applicant choose not to provide an authorization identified in subsection 1 below, applicant **must opt-out** of the authorization by checking the corresponding box A or B or both in subsection 2 below.

NOTE: This section of the Application Data Sheet is **ONLY** reviewed and processed with the **INITIAL** filing of an application. After the initial filing of an application, an Application Data Sheet cannot be used to provide or rescind authorization for access by a foreign IP office(s). Instead, Form PTO/SB/39 or PTO/SB/69 must be used as appropriate.

1. Authorization to Permit Access by a Foreign Intellectual Property Office(s)

A. Priority Document Exchange (PDX) - Unless box A in subsection 2 (opt-out of authorization) is checked, the undersigned hereby **grants the USPTO authority** to provide the European Patent Office (EPO), the Japan Patent Office (JPO), the Korean Intellectual Property Office (KIPO), the State Intellectual Property Office of the People's Republic of China (SIPO), the World Intellectual Property Organization (WIPO), and any other foreign intellectual property office participating with the USPTO in a bilateral or multilateral priority document exchange agreement in which a foreign application claiming priority to the instant patent application is filed, access to: (1) the instant patent application-as-filed and its related bibliographic data, (2) any foreign or domestic application to which priority or benefit is claimed by the instant application and its related bibliographic data, and (3) the date of filing of this Authorization. See 37 CFR 1.14(h)(1).

B. Search Results from U.S. Application to EPO - Unless box B in subsection 2 (opt-out of authorization) is checked, the undersigned hereby **grants the USPTO authority** to provide the EPO access to the bibliographic data and search results from the instant patent application when a European patent application claiming priority to the instant patent application is filed. See 37 CFR 1.14(h)(2).

The applicant is reminded that the EPO's Rule 141(1) EPC (European Patent Convention) requires applicants to submit a copy of search results from the instant application without delay in a European patent application that claims priority to the instant application.

2. Opt-Out of Authorizations to Permit Access by a Foreign Intellectual Property Office(s)

☐ A. Applicant **DOES NOT** authorize the USPTO to permit a participating foreign IP office access to the instant application-as-filed. If this box is checked, the USPTO will not be providing a participating foreign IP office with any documents and information identified in subsection 1A above.

☐ B. Applicant **DOES NOT** authorize the USPTO to transmit to the EPO any search results from the instant patent application. If this box is checked, the USPTO will not be providing the EPO with search results from the instant application.

NOTE: Once the application has published or is otherwise publicly available, the USPTO may provide access to the application in accordance with 37 CFR 1.14.

PTO/AIA/14 (11-15)
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Application Data Sheet 37 CFR 1.76	Attorney Docket Number	SETI-0110-CIP-US
	Application Number	
Title of Invention	Semiconductor Structure with Inhomogeneous Regions	

Applicant Information:

Providing assignment information in this section does not substitute for compliance with any requirement of part 3 of Title 37 of CFR to have an assignment recorded by the Office.

Applicant 1 — Remove

If the applicant is the inventor (or the remaining joint inventor or inventors under 37 CFR 1.45), this section should not be completed. The information to be provided in this section is the name and address of the legal representative who is the applicant under 37 CFR 1.43; or the name and address of the assignee, person to whom the inventor is under an obligation to assign the invention, or person who otherwise shows sufficient proprietary interest in the matter who is the applicant under 37 CFR 1.46. If the applicant is an applicant under 37 CFR 1.46 (assignee, person to whom the inventor is obligated to assign, or person who otherwise shows sufficient proprietary interest) together with one or more joint inventors, then the joint inventor or inventors who are also the applicant should be identified in this section.

Clear

● Assignee	Legal Representative under 35 U.S.C. 117	Joint Inventor
Person to whom the inventor is obligated to assign.	Person who shows sufficient proprietary interest	

If applicant is the legal representative, indicate the authority to file the patent application, the inventor is:

Name of the Deceased or Legally Incapacitated Inventor:

If the Applicant is an Organization check here. ☒

Organization Name	Sensor Electronic Technology, Inc.		
Mailing Address Information For Applicant:			
Address 1	1195 Atlas Road		
Address 2			
City	Columbia	**State/Province**	SC
Country	US	Postal Code	29209
Phone Number		Fax Number	
Email Address			

Additional Applicant Data may be generated within this form by selecting the Add button. Add

Assignee Information including Non-Applicant Assignee Information:

Providing assignment information in this section does not substitute for compliance with any requirement of part 3 of Title 37 of CFR to have an assignment recorded by the Office.

PTO/AIA/14 (11-15)
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U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE

Application Data Sheet 37 CFR 1.76	Attorney Docket Number	SETI-0110-CIP-US
	Application Number	
Title of Invention	Semiconductor Structure with Inhomogeneous Regions	

Assignee 1

Complete this section if assignee information, including non-applicant assignee information, is desired to be included on the patent application publication. An assignee-applicant identified in the "Applicant Information" section will appear on the patent application publication as an applicant. For an assignee-applicant, complete this section only if identification as an assignee is also desired on the patent application publication.

Remove

If the Assignee or Non-Applicant Assignee is an Organization check here. ☒

Organization Name	Sensor Electronic Technology, Inc.

Mailing Address Information For Assignee including Non-Applicant Assignee:

Address 1	1195 Atlas Road		
Address 2			
City	Columbia	**State/Province**	SC
Country i	US	Postal Code	29209
Phone Number		Fax Number	
Email Address			

Additional Assignee or Non-Applicant Assignee Data may be generated within this form by selecting the Add button. Add

Signature:

Remove

NOTE: This Application Data Sheet must be signed in accordance with 37 CFR 1.33(b). **However, if this Application Data Sheet is submitted with the INITIAL filing of the application and either box A or B is not checked in subsection 2 of the "Authorization or Opt-Out of Authorization to Permit Access" section, then this form must also be signed in accordance with 37 CFR 1.14(c).**

This Application Data Sheet **must** be signed by a patent practitioner if one or more of the applicants is a **juristic entity** (e.g., corporation or association). If the applicant is two or more joint inventors, this form must be signed by a patent practitioner, **all** joint inventors who are the applicant, or one or more joint inventor-applicants who have been given power of attorney (e.g., see USPTO Form PTO/AIA/81) on behalf of **all** joint inventor-applicants.

See 37 CFR 1.4(d) for the manner of making signatures and certifications.

Signature	/John W. LaBatt/			Date (YYYY-MM-DD)	2015-12-30
First Name	John	Last Name	LaBatt	Registration Number	48301

Additional Signature may be generated within this form by selecting the Add button. Add

PTO/AIA/14 (11-15)
Approved for use through 04/30/2017. OMB 0651-0032
U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE

Application Data Sheet 37 CFR 1.76	Attorney Docket Number	SETI-0110-CIP-US
	Application Number	
Title of Invention	Semiconductor Structure with Inhomogeneous Regions	

This collection of information is required by 37 CFR 1.76. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 23 minutes to complete, including gathering, preparing, and submitting the completed application data sheet form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

Privacy Act Statement

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The information provided by you in this form will be subject to the following routine uses:

1 The information on this form will be treated confidentially to the extent allowed under the Freedom of Information Act (5 U.S.C. 552) and the Privacy Act (5 U.S.C. 552a). Records from this system of records may be disclosed to the Department of Justice to determine whether the Freedom of Information Act requires disclosure of these records.

2. A record from this system of records may be disclosed, as a routine use, in the course of presenting evidence to a court, magistrate, or administrative tribunal, including disclosures to opposing counsel in the course of settlement negotiations.

3 A record in this system of records may be disclosed, as a routine use, to a Member of Congress submitting a request involving an individual, to whom the record pertains, when the individual has requested assistance from the Member with respect to the subject matter of the record.

4. A record in this system of records may be disclosed, as a routine use, to a contractor of the Agency having need for the information in order to perform a contract. Recipients of information shall be required to comply with the requirements of the Privacy Act of 1974, as amended, pursuant to 5 U.S.C. 552a(m).

5. A record related to an International Application filed under the Patent Cooperation Treaty in this system of records may be disclosed, as a routine use, to the International Bureau of the World Intellectual Property Organization, pursuant to the Patent CooperationTreaty.

6. A record in this system of records may be disclosed, as a routine use, to another federal agency for purposes of National Security review (35 U.S.C. 181) and for review pursuant to the Atomic Energy Act (42 U.S.C. 218(c)).

7. A record from this system of records may be disclosed, as a routine use, to the Administrator, General Services, or his/her designee, during an inspection of records conducted by GSA as part of that agency's responsibility to recommend improvements in records management practices and programs, under authority of 44 U.S.C. 2904 and 2906. Such disclosure shall be made in accordance with the GSA regulations governing inspection of records for this purpose, and any other relevant (i.e., GSA or Commerce) directive. Such disclosure shall not be used to make determinations about individuals.

8. A record from this system of records may be disclosed, as a routine use, to the public after either publication of the application pursuant to 35 U.S.C. 122(b) or issuance of a patent pursuant to 35 U.S.C. 151. Further, a record may be disclosed, subject to the limitations of 37 CFR 1.14, as a routine use, to the public if the record was filed in an application which became abandoned or in which the proceedings were terminated and which application is referenced by either a published application, an application open to public inspections or an issued patent.

9. A record from this system of records may be disclosed, as a routine use, to a Federal, State, or local law enforcement agency, if the USPTO becomes aware of a violation or potential violation of law or regulation.

Electronic Patent Application Fee Transmittal

Application Number:	
Filing Date:	
Title of Invention:	Semiconductor Structure with Inhomogeneous Regions
First Named Inventor/Applicant Name:	Maxim S. Shatalov
Filer:	John W LaBatt
Attorney Docket Number:	SETI-0110-CIP-US

Filed as Large Entity

Filing Fees for Utility under 35 USC 111(a)

Description	Fee Code	Quantity	Amount	Sub-Total in USD($)
Basic Filing:				
Utility application filing	1011	1	280	280
Utility Search Fee	1111	1	600	600
Utility Examination Fee	1311	1	720	720
Pages:				
Claims:				
Miscellaneous-Filing:				
Late Filing Fee for Oath or Declaration	1051	1	140	140
Petition:				

Description	Fee Code	Quantity	Amount	Sub-Total in USD($)
Patent-Appeals-and-Interference:				
Post-Allowance-and-Post-Issuance:				
Extension-of-Time:				
Miscellaneous:				
		Total in USD ($)		**1740**

Electronic Acknowledgement Receipt

EFS ID:	24489891
Application Number:	14984156
International Application Number:	
Confirmation Number:	5890
Title of Invention:	Semiconductor Structure with Inhomogeneous Regions
First Named Inventor/Applicant Name:	Maxim S. Shatalov
Customer Number:	11698
Filer:	John W LaBatt
Filer Authorized By:	
Attorney Docket Number:	SETI-0110-CIP-US
Receipt Date:	30-DEC-2015
Filing Date:	
Time Stamp:	14:22:21
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File Listing:

Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1	Drawings-only black and white line drawings	SETI-0110-CIP-US_Drawings.pdf	819563 aab9d7b033d4c4c0b9fa752bc637f84ea3dec30e	no	15
Warnings:					
Information:					
2		SETI-0110-CIP-US_Application.pdf	213808 6217f395b2d626372ead3b3c7af8ebc6ec13f914	yes	46

	Multipart Description/PDF files in .zip description		
	Document Description	**Start**	**End**
	Specification	1	39
	Claims	40	45
	Abstract	46	46

Warnings:					
Information:					
3	Oath or Declaration filed	SETI-0110-CIP-US_Declaration.pdf	63755 b1a08da23d26f2a0a4e878fe66f026df6eb4a6a8	no	7
Warnings:					
Information:					
4	Power of Attorney	SETPatentsSharedPOA_Signed.pdf	237711 efbbd4886e02792fb65ad2dd3a6c7ce6739b209e	no	2
Warnings:					
Information:					
5	Application Data Sheet	SETI-0110-CIP-US_ADS.pdf	1823436 d98d3b98f79b59027cfabb62984784dcbd8d6334	no	10
Warnings:					
Information:					
6	Fee Worksheet (SB06)	fee-info.pdf	36778 b1a87cd5b0487b842515fc5b5145e028100e311b	no	2

Warnings:	
Information:	
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FIG. 1

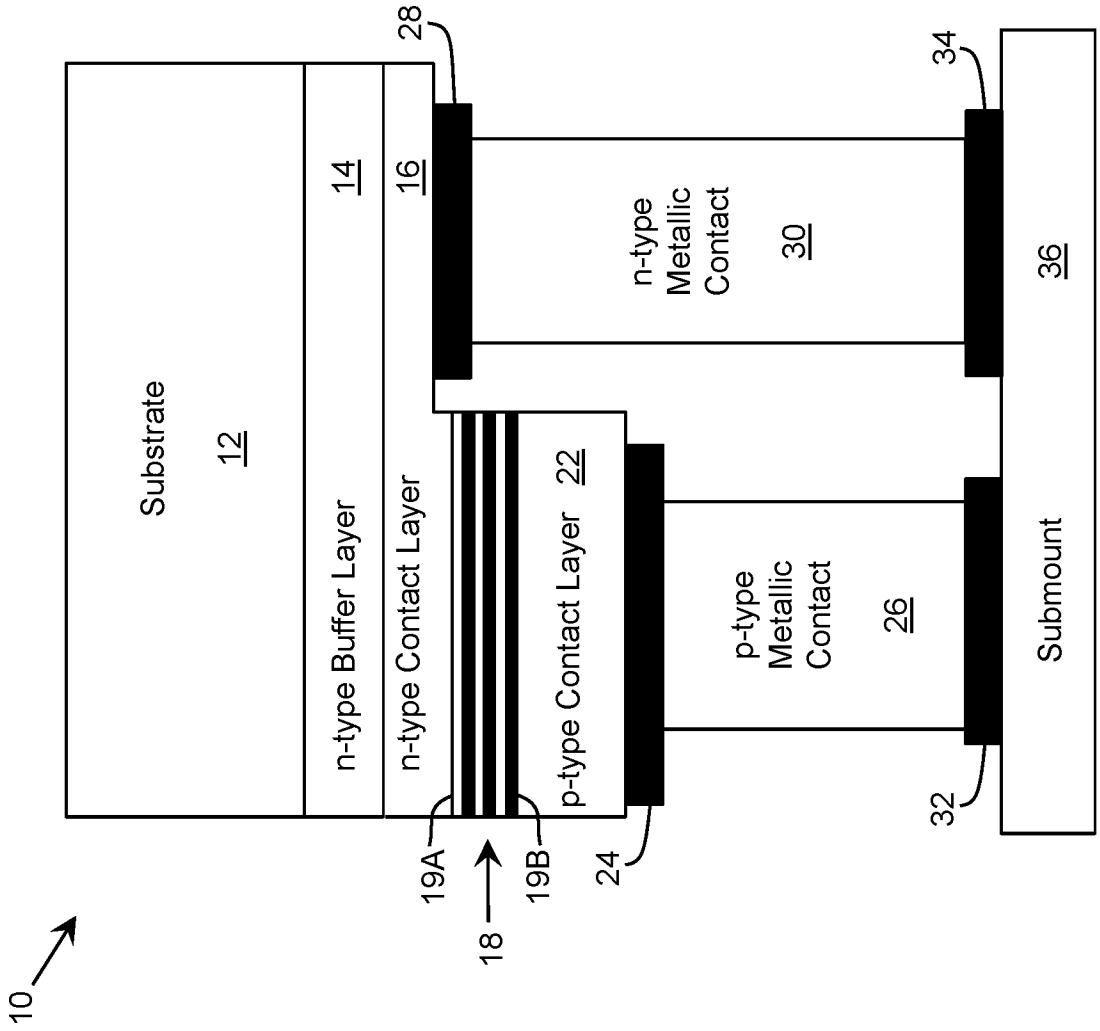

Substrate
12
n-type Buffer Layer
14
n-type Contact Layer
16
p-type Contact Layer
22
n-type
Metallic
Contact
30
p-type
Metallic
Contact
26
Submount
36
28
34
32
24
19A
19B
18
10

FIG. 2

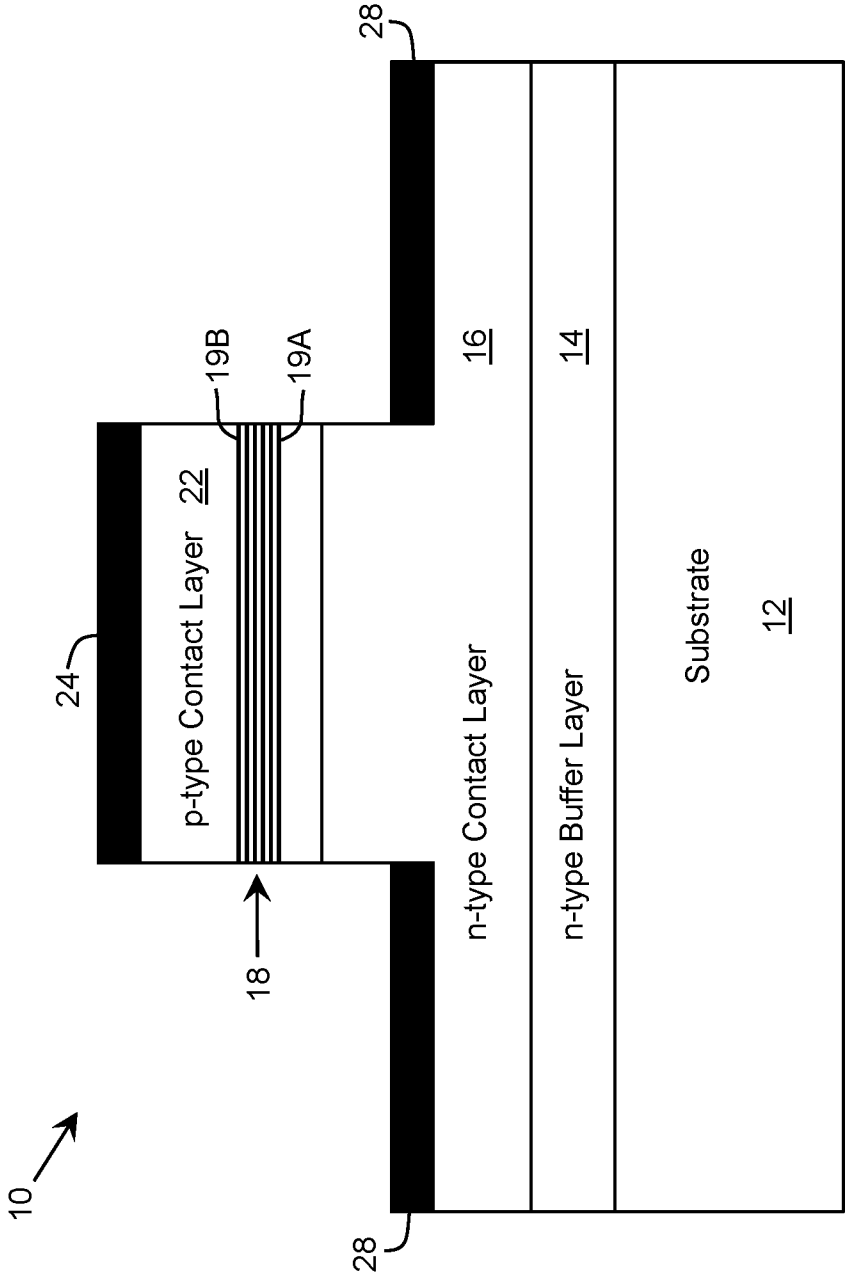

28
19B
19A
16
14
24
p-type Contact Layer 22
n-type Contact Layer
n-type Buffer Layer
Substrate
12
18
10
28

FIG. 3A

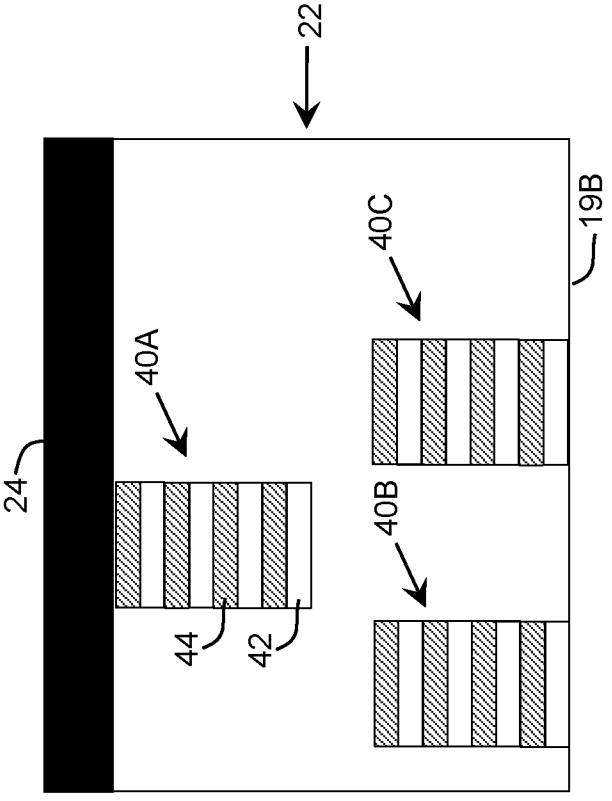
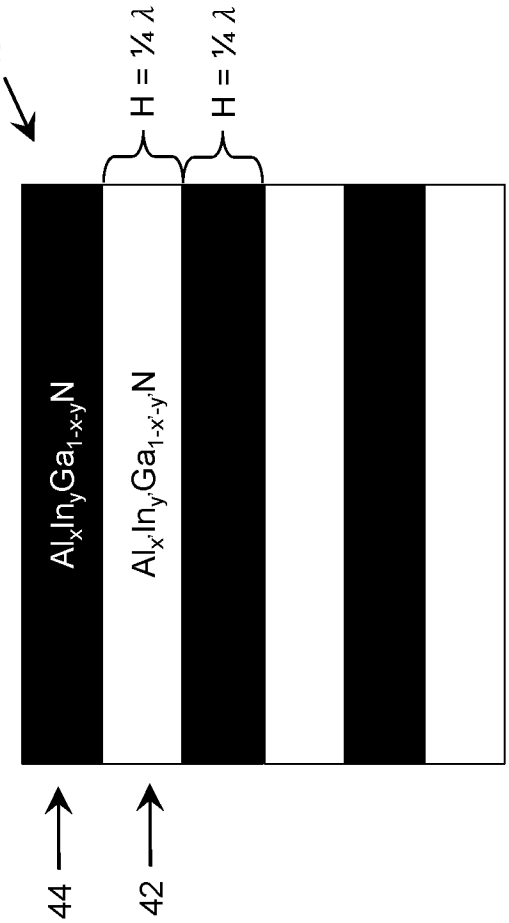

22
24
40A
40B
40C
19B
44
42

FIG. 3B


40
H = ¼ λ
H = ¼ λ
$Al_xIn_yGa_{1-x-y}N$
$Al_{x'}In_{y'}Ga_{1-x'-y'}N$
44
42

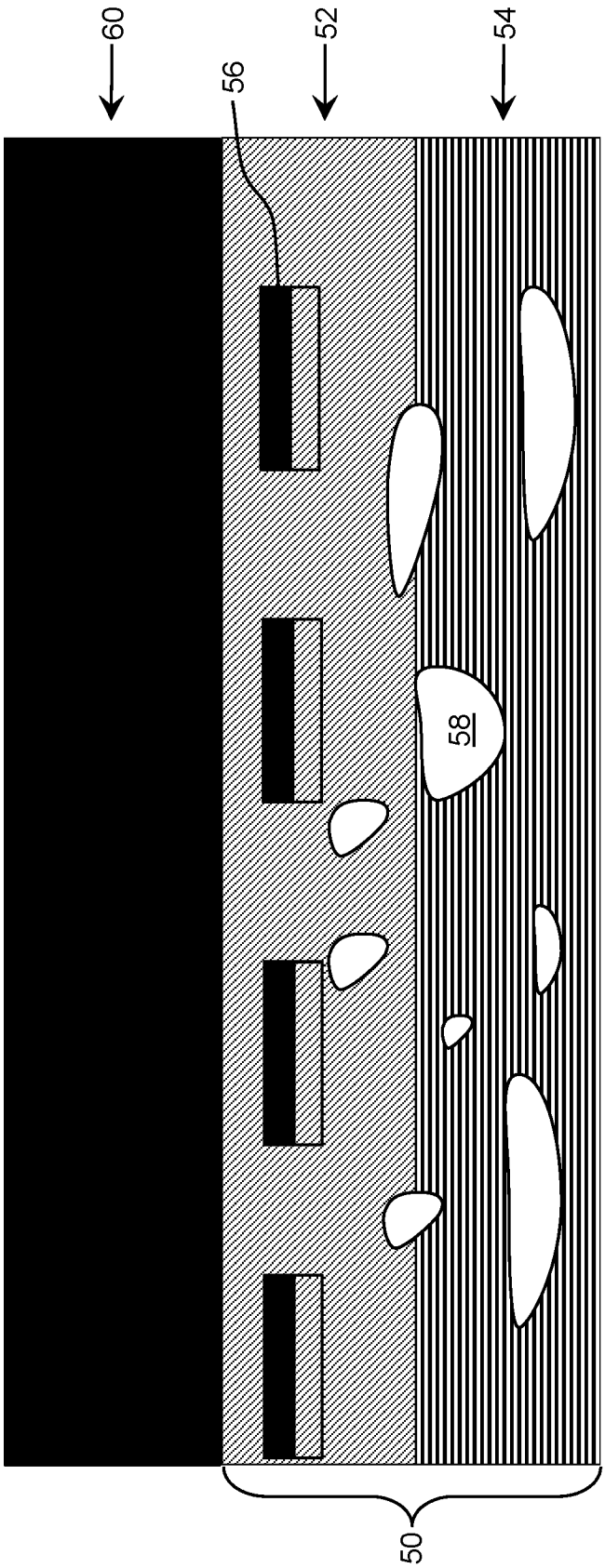


FIG. 4

FIG. 5

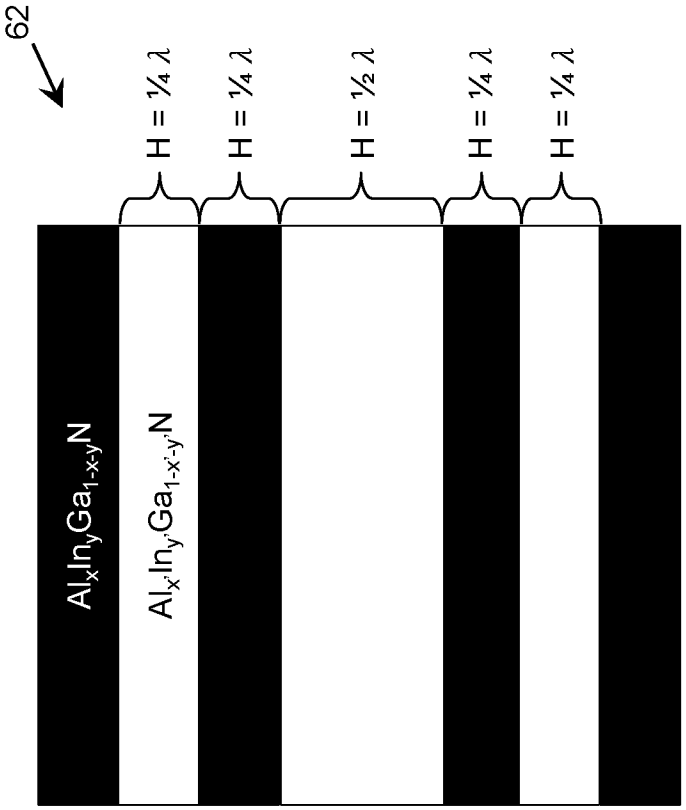
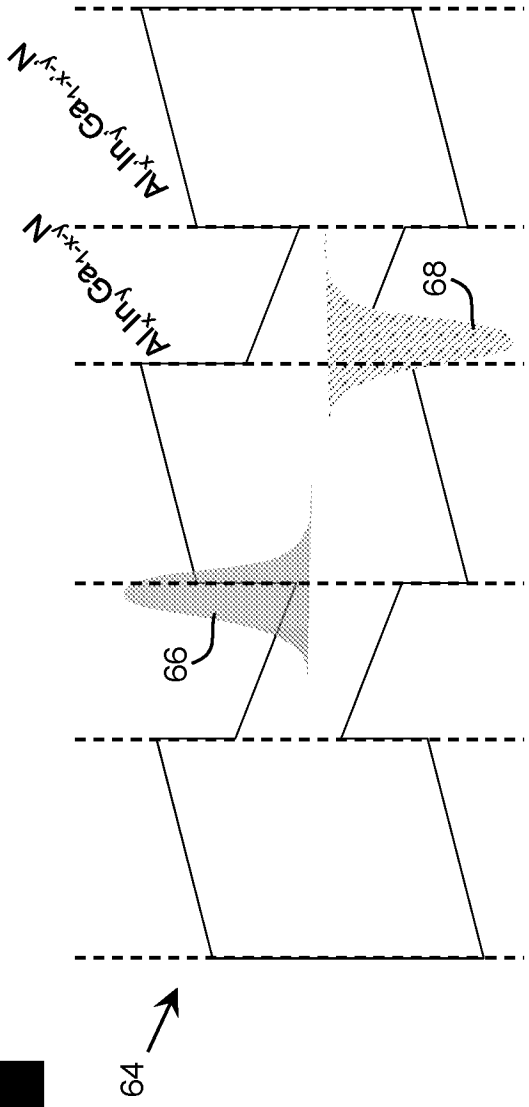

62
H = ¼ λ
H = ¼ λ
H = ½ λ
H = ¼ λ
H = ¼ λ
AlxInyGa1-x-yN
Alx'Iny'Ga1-x'-y'N

FIG. 6


AlxInyGa1-x-yN
AlxInyGa1-x-yN
68
66
64

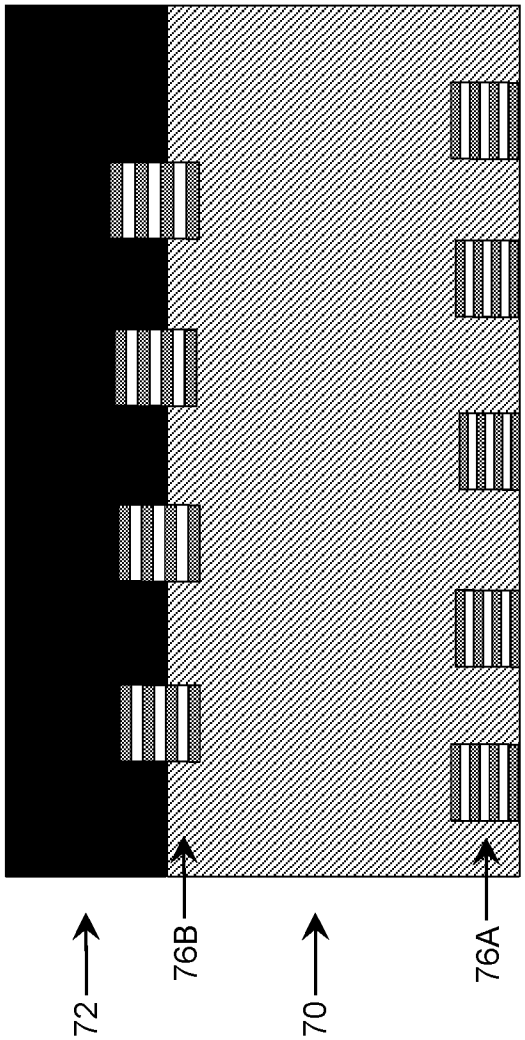


FIG. 7B

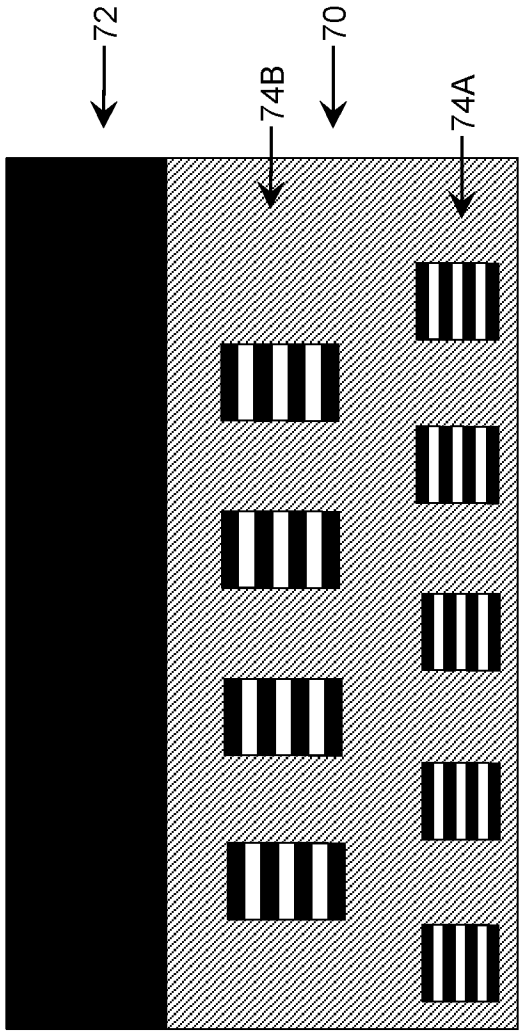
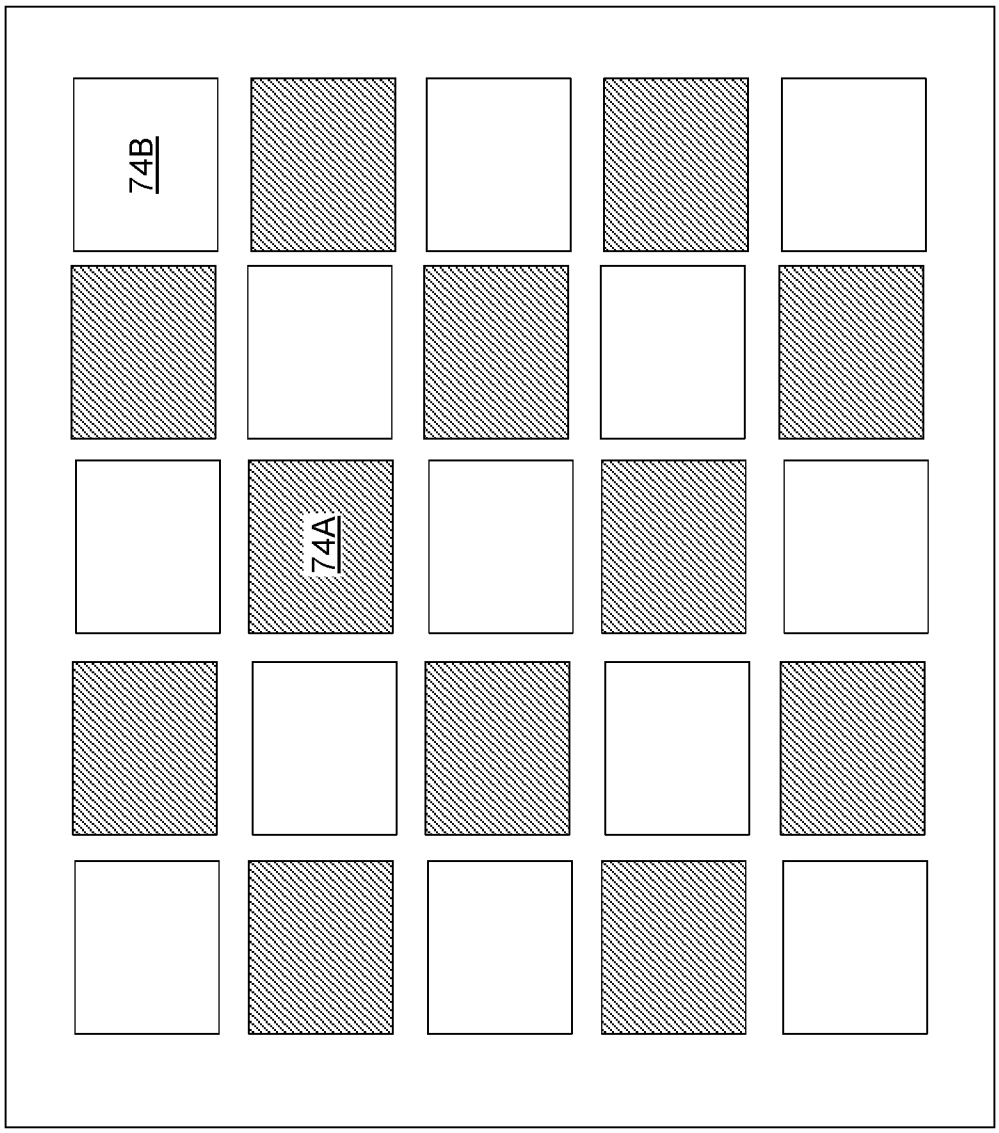


FIG. 7A

FIG. 7C



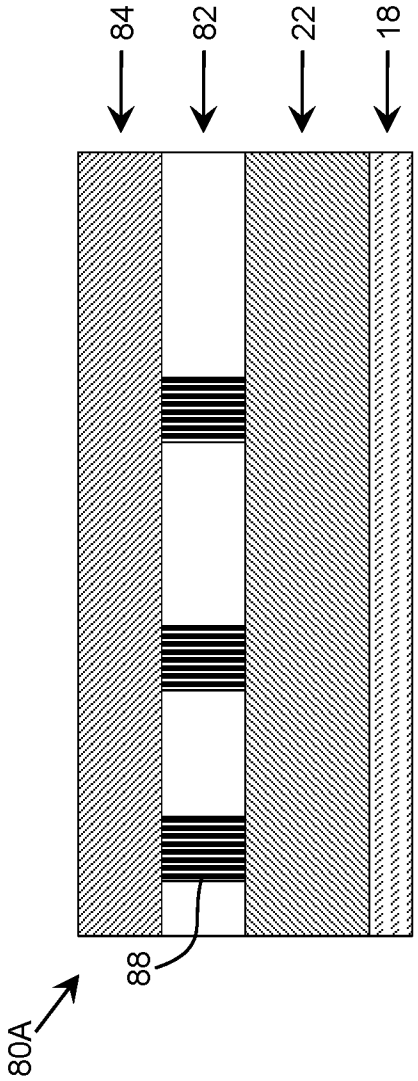


FIG. 8A

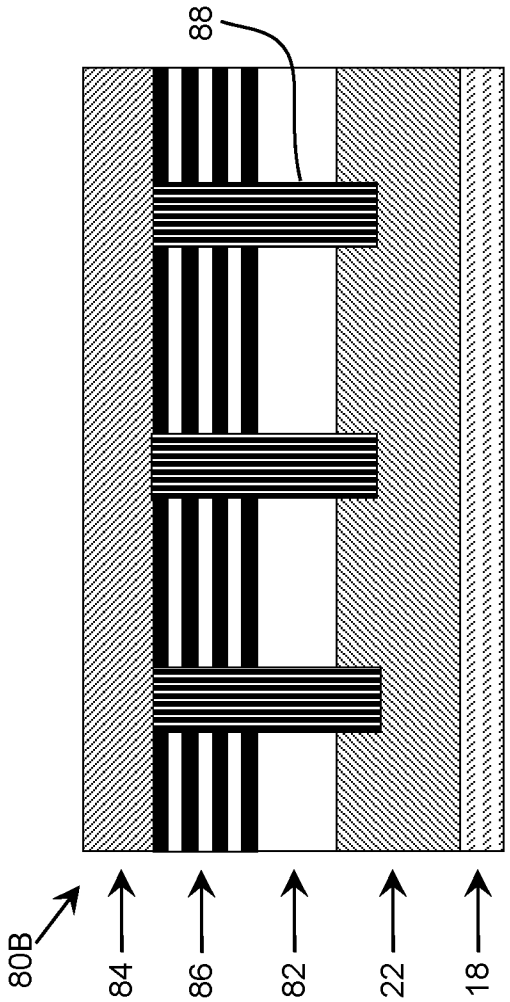


FIG. 8B

FIG. 9

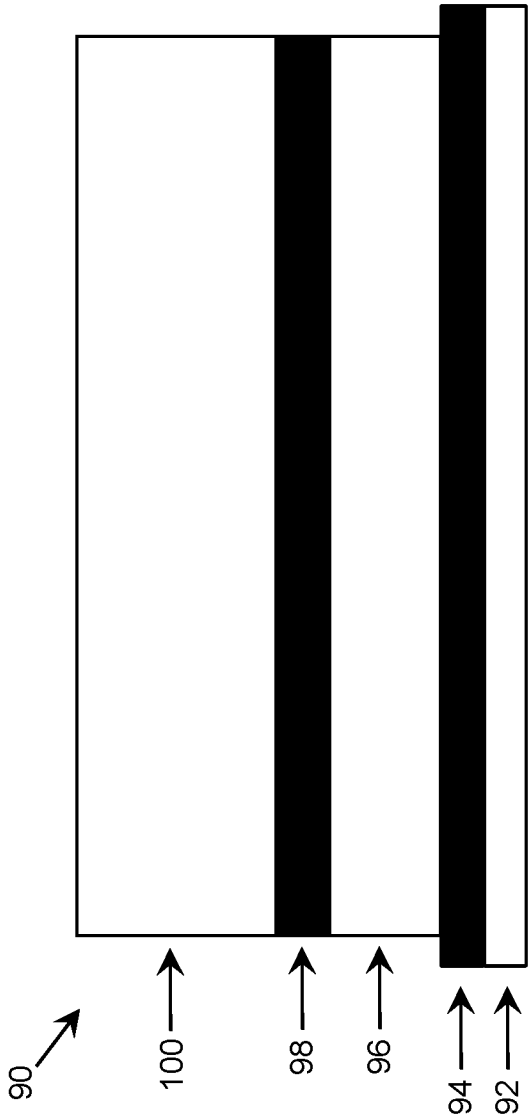

90
100
98
96
94
92

FIG. 10

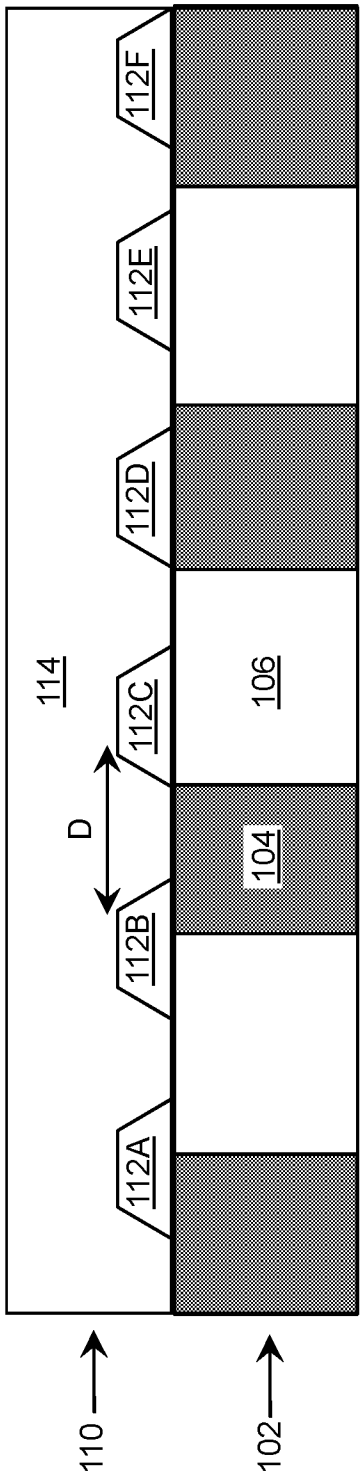

112F
112E
112D
112C
112B
112A
114
D
104
106
110
102

FIG. 11A

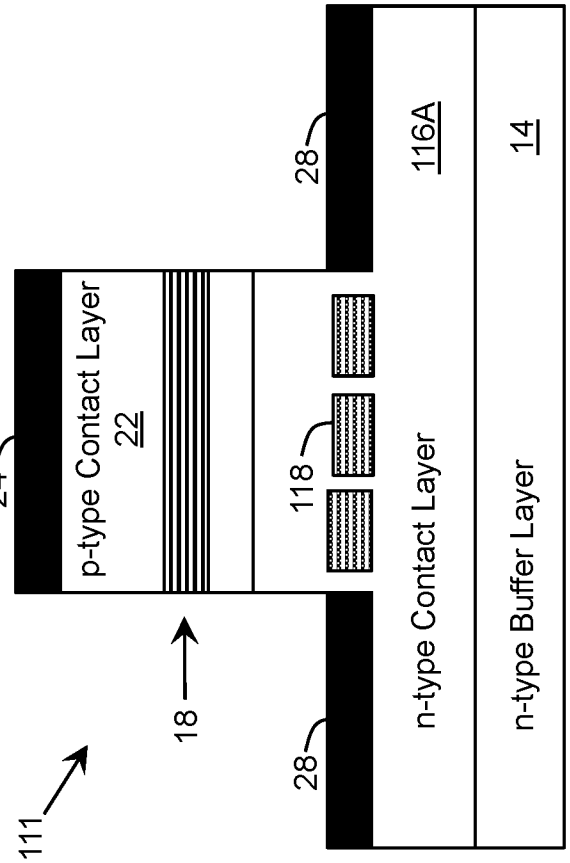


FIG. 11B

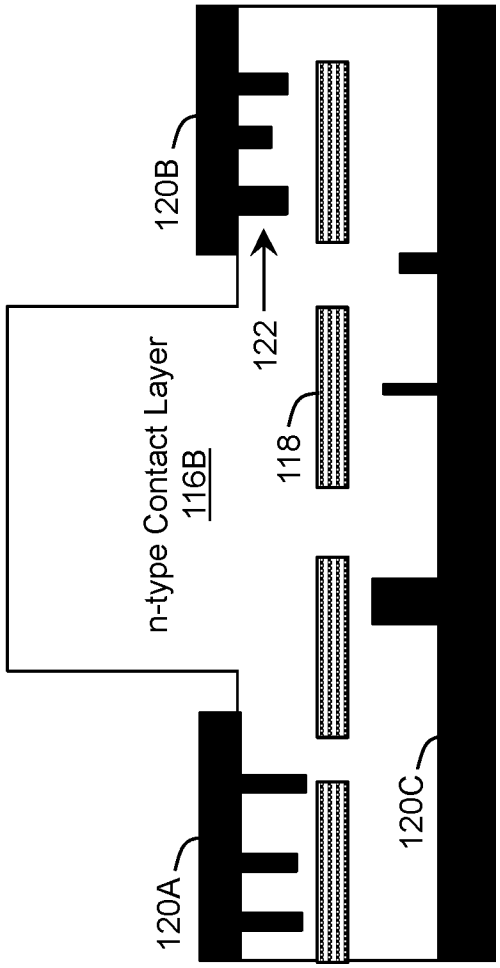
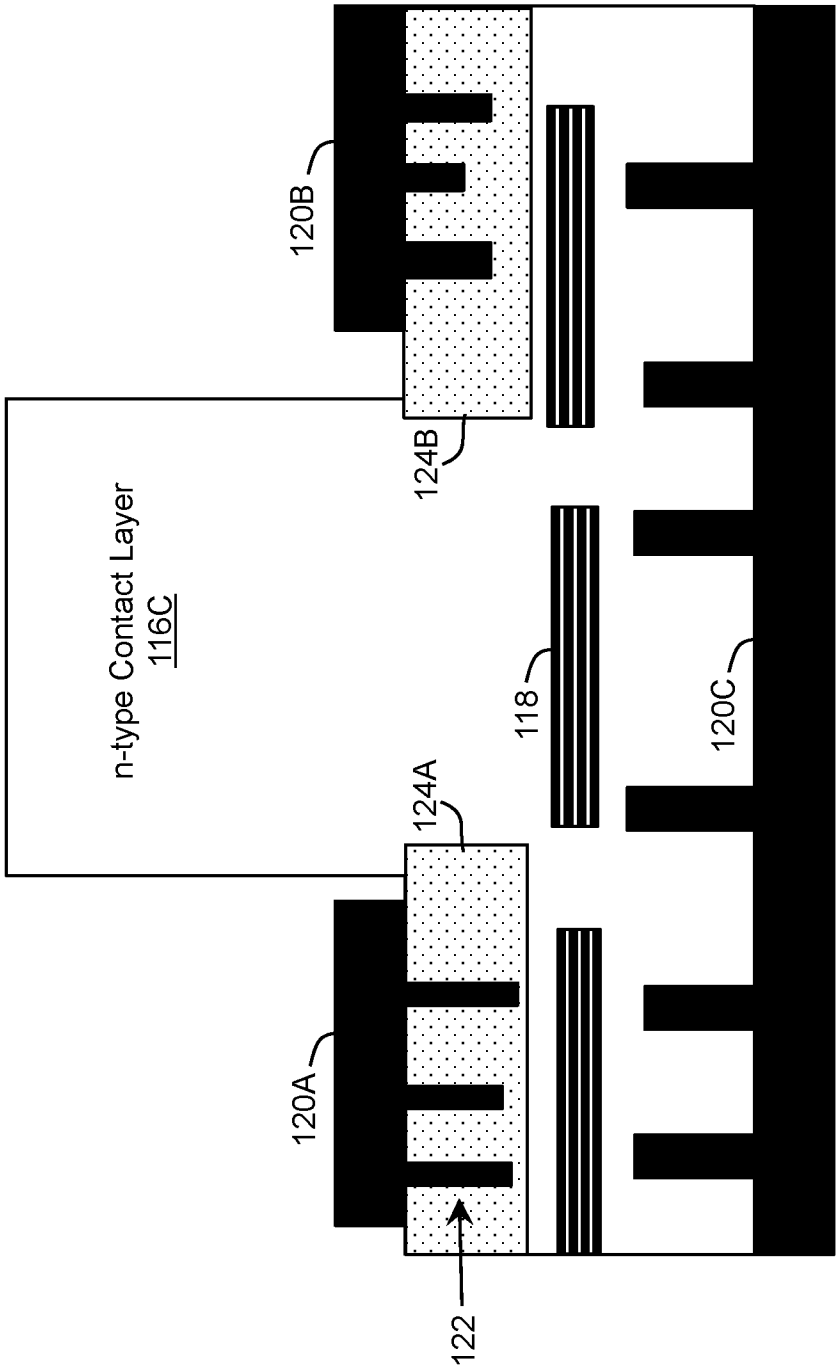


FIG. 11C



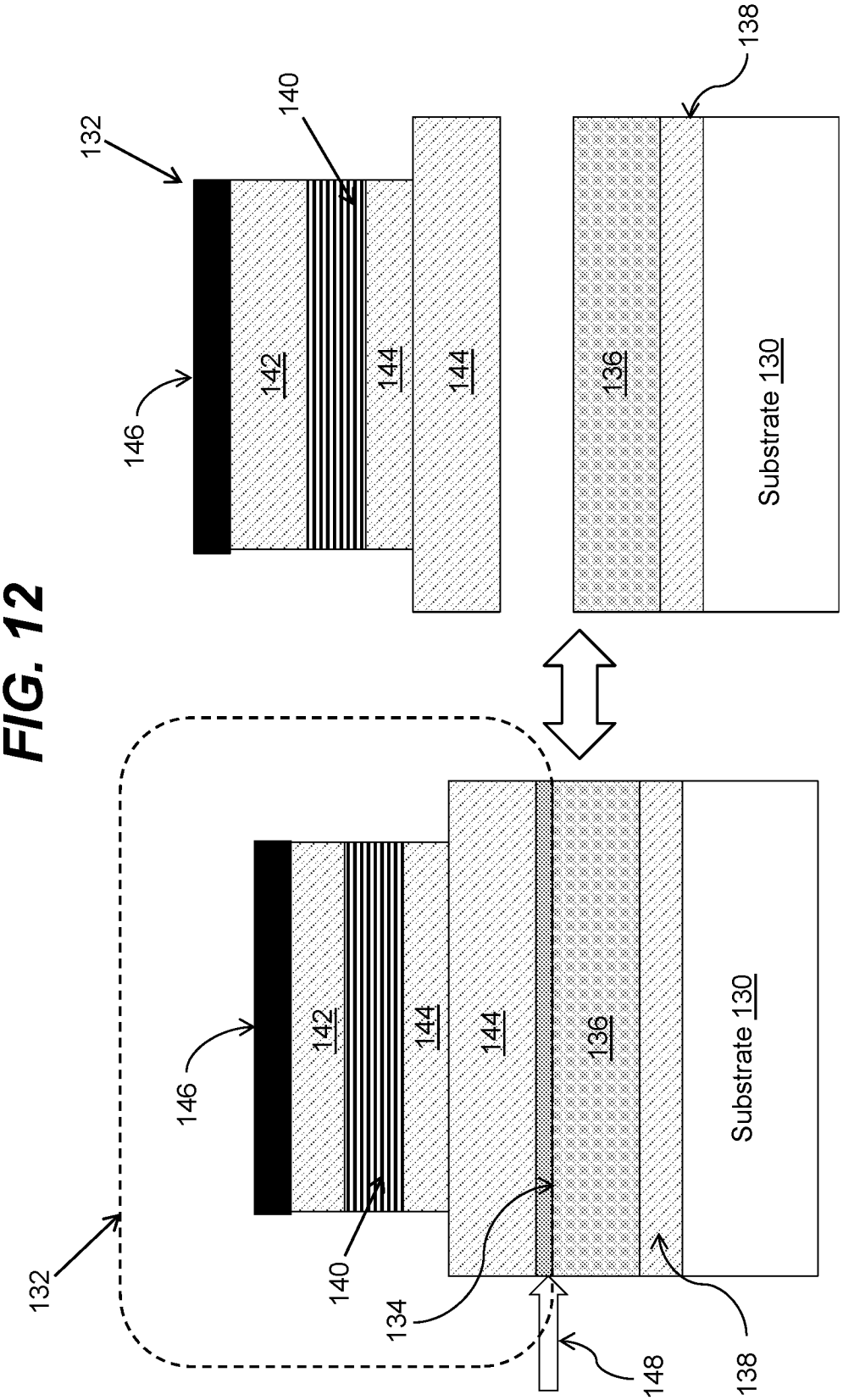
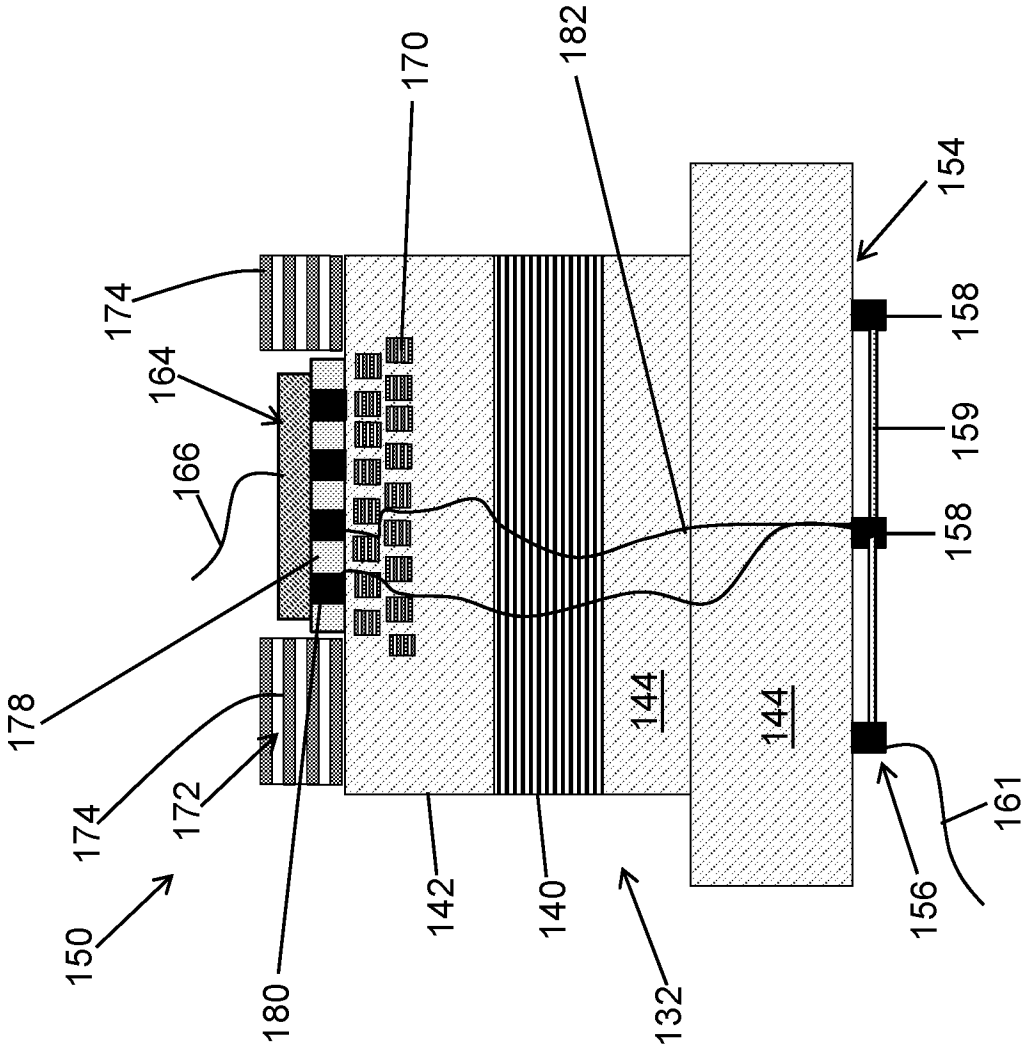

132
140
138
146
142
144
144
136
Substrate 130
146
142
144
144
136
Substrate 130
132
140
134
148
138

FIG. 12

FIG. 13A


170
182
154
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158
164
159
166
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150
180
132

FIG. 13B

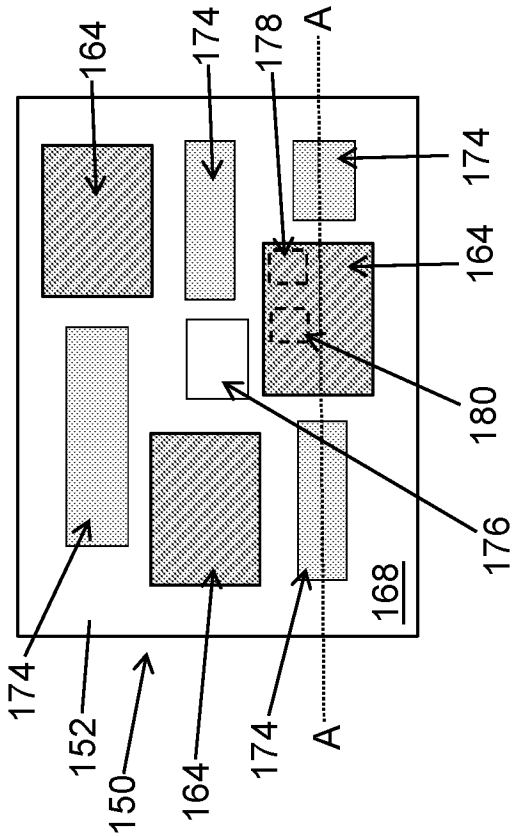


FIG. 13C

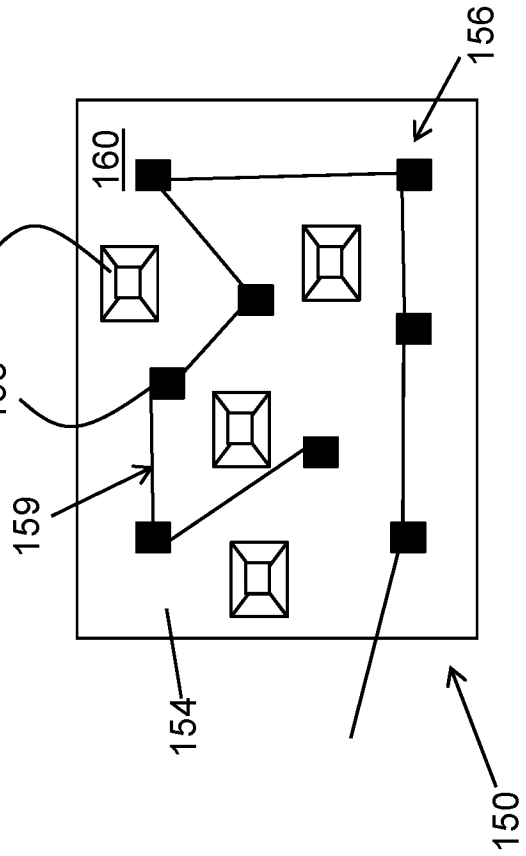
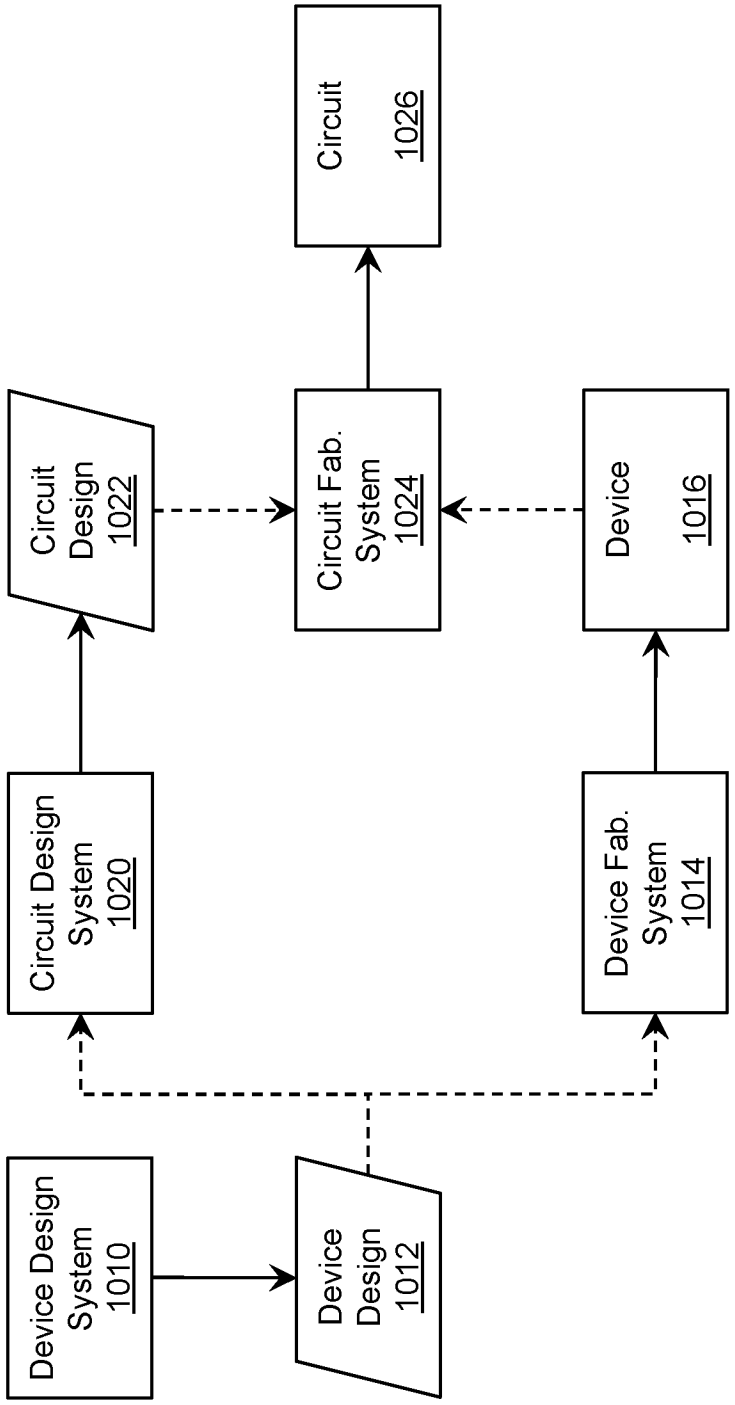


FIG. 14


Device Design System 1010
Device Design 1012
Circuit Design System 1020
Circuit Design 1022
Device Fab. System 1014
Circuit Fab. System 1024
Device 1016
Circuit 1026

Semiconductor Structure with Inhomogeneous Regions

REFERENCE TO RELATED APPLICATIONS

[0001] The present patent application is a continuation-in-part application of U.S. Application No. 14/189,012, entitled "Semiconductor Structure with Inhomogeneous Regions," which was filed on 25 February 2014, now pending, which claims the benefit of U.S. Provisional Application No. 61/768,581, entitled "Reflective, Transparent, Conductive Semiconductor Structure, Optoelectronic Device With The Same, and Method of Making The Same," which was filed on 25 February 2013, each of which is hereby incorporated by reference in its entirety to provide continuity of disclosure.

TECHNICAL FIELD

[0002] The disclosure relates generally to semiconductor devices, and more particularly, to emitting semiconductor devices, such as deep ultraviolet light emitting devices.

BACKGROUND ART

[0003] Semiconductor emitting devices, such as light emitting diodes (LEDs) and laser diodes (LDs), include, but are not limited to, solid state emitting devices composed of group III-V semiconductors. A subset of group III-V semiconductors includes group III-Nitride alloys, which can include binary, ternary and quaternary alloys of indium (In), aluminum (Al), gallium (Ga), and nitrogen (N). Illustrative group III-Nitride based LEDs and LDs can be of the form $In_yAl_xGa_{1-x-y}N$, where x and y indicate the molar fraction of a given element, $0 \leq x, y \leq 1$, and $0 \leq x+y \leq 1$. Other illustrative group III-Nitride based

LEDs and LDs are based on boron (B) nitride (BN) and can be of the form $Ga_zIn_yAl_xB_{1-x-y-z}N$, where $0 \leq x, y, z \leq 1$, and $0 \leq x+y+z \leq 1$.

[0004] An LED is typically composed of semiconducting layers. During operation of the LED, a voltage bias applied across doped layers leads to injection of electrons and holes into an active layer where electron-hole recombination leads to light generation. Light is generated in the active layer with uniform angular distribution and escapes the LED die by traversing semiconductor layers in all directions. Each semiconducting layer has a particular combination of molar fractions for the various elements (e.g., given values of x, y, and/or z), which influences the optical properties of the semiconducting layer. In particular, a refractive index and absorption characteristics of a semiconducting layer are sensitive to the molar fractions of the semiconductor alloy forming the layer.

[0005] Current state of the art deep ultraviolet LEDs (DUV LEDs) have a low efficiency due to light trapping within the device, light absorption in the semiconductor layers, as well as light absorption in the contact regions. To improve light extraction efficiency for the DUV LEDs, one approach proposes a design using ultraviolet transparent p-type cladding and contact layers, an ultraviolet reflecting ohmic contact, and chip encapsulation having an optimized shape and refractive index.

SUMMARY OF THE INVENTION

[0006] This Summary Of The Invention introduces a selection of certain concepts in a brief form that are further described below in the Detailed Description Of The Invention. It is not intended to exclusively identify key features or essential features of the claimed

subject matter set forth in the Claims, nor is it intended as an aid in determining the scope of the claimed subject matter.

[0007] Aspects of the invention provide a semiconductor layer including a plurality of inhomogeneous regions. Each inhomogeneous region has one or more attributes that differ from a material forming the semiconductor layer. The inhomogeneous regions can include one or more regions configured based on radiation having a target wavelength. These regions can include transparent and/or reflective regions. The inhomogeneous regions also can include one or more regions having a higher conductivity than a conductivity of the radiation-based regions, e.g., at least ten percent higher. In one embodiment, the semiconductor layer can be used to form an optoelectronic device.

[0008] A first aspect of the invention provides a semiconductor heterostructure comprising: an active region; a metallic contact; a group III nitride semiconductor layer located between the active region and the metallic contact, the semiconductor layer including a plurality of inhomogeneous regions arranged within multiple levels of the semiconductor layer, wherein some of the inhomogeneous regions in a first level of the semiconductor layer are vertically offset from inhomogeneous regions in a second level of the semiconductor layer, and wherein the plurality of inhomogeneous regions include one or more of a set of transparent regions, a set of reflective regions and/or a set of conductive regions, each of the inhomogeneous regions having a set of attributes differing from a group III nitride material forming the semiconductor layer.

[0009] A second aspect of the invention provides a method, comprising: fabricating a semiconductor heterostructure, wherein the semiconductor heterostructure comprises:

an active region; a metallic contact; a group III nitride semiconductor layer located between the active region and the metallic contact, the semiconductor layer including a plurality of inhomogeneous regions arranged within multiple levels of the semiconductor layer, wherein some of the inhomogeneous regions in a first level of the semiconductor layer are vertically offset from inhomogeneous regions in a second level of the semiconductor layer, and wherein the plurality of inhomogeneous regions include one or more of a set of transparent regions, a set of reflective regions and/or a set of conductive regions, each of the inhomogeneous regions having a set of attributes differing from a group III nitride material forming the semiconductor layer.

[0010] A third aspect of the invention provides an optoelectronic device, comprising: a semiconductor heterostructure, obtained through laser lift-off, having a first side and a second side, the semiconductor heterostructure including: a group III nitride semiconductor layer including a plurality of inhomogeneous regions, each inhomogeneous region having a set of attributes differing from a group III nitride material forming the semiconductor layer, wherein the plurality of inhomogeneous regions include: a set of first inhomogeneous regions configured based on radiation having a target wavelength, wherein the set of first inhomogeneous regions are at least one of: transparent to the radiation or reflective of the radiation; and a set of second inhomogeneous regions having a conductivity at least ten percent higher than a conductivity of the set of first inhomogeneous regions, wherein each of the sets of inhomogeneous regions occupy at least five percent of at least one of: a lateral planar area of the semiconductor layer or a volume of the semiconductor layer, and wherein at least some of the sets of inhomogeneous regions do not fully overlap..

[0011] The illustrative aspects of the invention are designed to solve one or more of the problems herein described and/or one or more other problems not discussed.

BRIEF DESCRIPTION OF THE DRAWINGS

[0012] These and other features of the disclosure will be more readily understood from the following detailed description of the various aspects of the invention taken in conjunction with the accompanying drawings that depict various aspects of the invention.

[0013] FIG. 1 shows a typical design of a flip-chip emitting device according to an embodiment.

[0014] FIG. 2 shows a typical design of an emitting device including a mesa structure according to an embodiment.

[0015] FIG. 3A shows a layer including a plurality of reflective regions, while FIG. 3B shows an illustrative reflective region according to embodiments.

[0016] FIG. 4 shows an illustrative semiconductor structure according to an embodiment.

[0017] FIG. 5 shows a structure for an illustrative Fabry-Perot interference filter according to an embodiment.

[0018] FIG. 6 shows a band diagram of an illustrative embodiment of a horizontally conductive material according to an embodiment.

[0019] FIGS. 7A-7C show illustrative arrangements of reflective regions according to embodiments.

[0020] FIGS. 8A and 8B show illustrative reflective regions comprising omnidirectional mirrors according to embodiments.

[0021] FIG. 9 shows an illustrative multilayered metallic contact according to an embodiment.

[0022] FIG. 10 shows an illustrative interface between a semiconductor layer and a metallic contact according to an embodiment.

[0023] FIGS. 11A-11C show illustrative n-type contact layers including reflective regions according to embodiments.

[0024] FIG. 12 shows a schematic of a laser lift-off method to lift a semiconductor structure such as any of the structures described herein from a substrate according to an embodiment.

[0025] FIGS. 13A-13C show multiple views of an optoelectronic device formed from a semiconductor heterostructure lifted off from a substrate according to an embodiment.

[0026] FIG. 14 shows an illustrative flow diagram for fabricating a circuit according to an embodiment.

[0027] It is noted that the drawings may not be to scale. The drawings are intended to depict only typical aspects of the invention, and therefore should not be considered as limiting the scope of the invention. In the drawings, like numbering represents like elements between the drawings.

DETAILED DESCRIPTION OF THE INVENTION

[0028] As indicated above, aspects of the invention provide a semiconductor layer including a plurality of inhomogeneous regions. Each inhomogeneous region has one or more attributes that differ from a material forming the semiconductor layer. The inhomogeneous regions can include one or more regions configured based on radiation having a target wavelength. These regions can include transparent and/or reflective

regions. The inhomogeneous regions also can include one or more regions having a higher conductivity than a conductivity of the radiation-based regions, e.g., at least ten percent higher. As used herein, unless otherwise noted, the term "set" means one or more (i.e., at least one) and the phrase "any solution" means any now known or later developed solution.

[0029] Aspects of the invention provide a semiconductor structure (e.g., a semiconductor layer) that can be incorporated into an optoelectronic device, such as a light emitting diode (LED), a vertical LED, a light emitting laser, a light sensor, a photodetector, an avalanche diode, and/or the like, after removing the semiconductor structure from a substrate using a technique, such as, for example, a laser lift off technique. The semiconductor structure can include inhomogeneous regions formed by one or more of: patterning, masking, epitaxial growth, epitaxial overgrowth, deposition techniques, and/or the like. Deposition techniques can include thermal evaporation, magnetron sputtering, ion-beam deposition, laser beam evaporation, and/or the like. In a more particular embodiment, the semiconductor structure comprises a group III nitride semiconductor layer. The inhomogeneous regions can include various types of inhomogeneous regions and can be located within the semiconductor structure in various arrangements. Aspects of the invention are further described in conjunction with emitting devices, such as group III nitride-based emitting devices, including an active region configured to generate radiation during operation of the device. However, it is understood that the invention can be applied to other types of optoelectronic devices.

[0030] Flip-chip technology is frequently utilized to control light extraction and thermal management of a LED, such as a deep ultraviolet (DUV) LED. Turning to the drawings, FIG. 1 shows a typical design of a flip-chip emitting device 10 according to an embodiment, while FIG. 2 shows a typical design of an emitting device 10 including a mesa structure according to an embodiment. In general, each emitting device 10 includes a semiconductor heterostructure having multiple semiconductor layers. Each semiconductor layer typically has lateral dimensions significantly larger than the layer height. Such a semiconductor layer is referred to herein as a planar layer and the discussion distinguishes between two directions: a direction in plane (e.g., extending right to left and into and out of the page in the drawing) and a direction perpendicular to the plane (e.g., extending top to bottom in the drawing). In a typical embodiment, the lateral dimensions of a layer can reach several square millimeters, whereas the height of the layer is typically measured in micrometers and nanometers. A planar area of the layer is typically referred to as the area of the layer or the area of the semiconductor structure. A lateral planar area is defined as an area of a surface of the semiconductor layer and is parallel to the surface of the substrate used for epitaxial growth.

[0031] As illustrated, each emitting device 10 includes a heterostructure comprising a substrate 12, a buffer layer 14 adjacent to the substrate 12, an n-type contact layer 16 (e.g., an electron supply layer) adjacent to the buffer layer 14, and an active region 18 having an n-type side 19A adjacent to the n-type cladding layer 16. Furthermore, the heterostructure of each emitting device 10 includes a p-type contact layer 22 (e.g., a hole supply layer) adjacent to a p-type side 19B of the active region 18. It is understood that the emitting devices 10 are only illustrative of various configurations of

heterostructures. To this extent, a heterostructure can include one or more additional layers, which are not shown.

[0032] In a more particular illustrative embodiment, an emitting device 10 is a group III-V materials based device, in which some or all of the various layers are formed of elements selected from the group III-V materials system. In a still more particular illustrative embodiment, the various layers of the emitting device 10 are formed of group III nitride based materials. Group III nitride materials comprise one or more group III elements (e.g., boron (B), aluminum (Al), gallium (Ga), and indium (In)) and nitrogen (N), such that $B_WAl_XGa_YIn_ZN$, where $0 \leq W, X, Y, Z \leq 1$, and $W+X+Y+Z = 1$. Illustrative group III nitride materials include AlN, GaN, InN, BN, AlGaN, AlInN, AlBN, AlGaInN, AlGaBN, AlInBN, and AlGaInBN with any molar fraction of group III elements.

[0033] An illustrative embodiment of a group III nitride based emitting device 10 includes an active region 18 (e.g., a series of alternating quantum wells and barriers) composed of $In_yAl_xGa_{1-x-y}N$, $Ga_zIn_yAl_xB_{1-x-y-z}N$, an $Al_xGa_{1-x}N$ semiconductor alloy, or the like. Similarly, both the n-type contact layer 16 and the p-type contact layer 22 can be composed of an $In_yAl_xGa_{1-x-y}N$ alloy, a $Ga_zIn_yAl_xB_{1-x-y-z}N$ alloy, or the like. The molar fractions given by *x*, *y*, and *z* can vary between the various layers 16, 18, and 22. The substrate 12 can be sapphire, silicon carbide (SiC), silicon (Si), GaN, AlGaN, AlON, $LiGaO_2$, or another suitable material, and the buffer layer 14 can be composed of AlN, an AlGaN/AlN superlattice, and/or the like.

[0034] A p-type metal 24 can be attached to the p-type contact layer 22 and a n-type metal 28 can be attached to the n-type contact layer 16. The p-type metal 24 and the n-type metal 28 can form ohmic contacts to the corresponding layers 22, 16, respectively.

As shown with respect to the emitting device 10 of FIG. 1, a p-type metallic contact 26 can be attached to the p-type metal 24 and an n-type metallic contact 30 can be attached to the n-type metal 28. In an embodiment, the p-type metal 24 and the n-type metal 28 each comprise several conductive and reflective metal layers, while the n-type metallic contact 30 and the p-type metallic contact 26 each comprise highly conductive metal.

[0035] In an embodiment, an emitting device 10 includes one or more layers, such as the n-type contact layer 16 and/or the p-type contact layer 22, formed of a semiconductor structure having one or more inhomogeneous regions located therein. The inhomogeneous regions can include one or more regions configured based on radiation having a target wavelength and/or one or more regions configured based on a desired conductivity. To this extent, the inhomogeneous regions can include one or more of: a set of transparent regions, a set of reflective regions, and/or a set of conductive regions. As used herein, a region is a transparent region when the region allows at least ten percent of radiation having a target wavelength, which is radiated at a normal incidence to an interface of the region, to pass there through. Furthermore, as used herein, a region is a reflective region when the region reflects at least ten percent of radiation having a target wavelength, which is radiated at a normal incidence to an interface of the region. In an embodiment, the target wavelength of the radiation corresponds to a wavelength of radiation emitted or sensed by the active region 18 during operation of the device 10. For a given layer, the wavelength can be measured in a material of consideration and can depend on a refractive index of the material.

[0036] A conductive region can be configured to promote conductivity of carriers in the semiconductor structure. A conductive region can have a higher concentration of carriers due to, for example, a locally reduced band gap of the semiconductor layer, a local high doping of the semiconductor layer, and/or the like. In an illustrative embodiment, the conductive region is formed of a group III nitride semiconductor material. In this case, a high local level of doping can be achieved by locally reducing an aluminum content, by polarization doping resulting in graded layers, and/or the like. Regardless, the improved conductivity can maintain an overall conductivity of the semiconductor structure. In an embodiment, a conductive region has a conductivity at least ten percent higher than a conductivity of a transparent region and a conductivity of a reflective region and a higher conductivity than a base semiconductor material for the layer.

[0037] A conductive region described herein can be anisotropic in the layer normal and/or lateral directions. For example, one or more of the conductive regions can have a high conductivity in a layer normal direction but not in the layer lateral direction, while one or more other conductive regions can have a high conductivity in the layer lateral direction but not in the layer normal direction. The conductive regions with high conductivity in the layer normal direction are referred to as regions with vertical conductivity, while conductive regions with high conductivity in the layer lateral direction are referred to as regions with horizontal conductivity. Similar to an isotropic conductive region, an anisotropic conductive region can have a conductivity in the preferred semiconductor direction that is at least ten percent higher than a conductivity of the reflective and transparent regions in the preferred direction.

[0038] Regions of each type (transparent, reflective, and conductive) can be incorporated into the semiconductor structure (e.g., a layer in the emitting device 10) and have an area that is a fraction of the area of the entire semiconductor structure. In an embodiment, the area of the region is approximately a few percent of the area of the semiconductor structure or more (e.g., greater than or equal to approximately three percent of the area of the semiconductor structure). Additionally, a region can have a height that is smaller than a height of the corresponding semiconductor structure. For example, a region can have a height that is fifty percent or ten percent of the height of the semiconductor layer. A region can be located anywhere within the semiconductor structure, including completely within the semiconductor structure or located adjacent to either planar side of the semiconductor structure. In an embodiment, the semiconductor structure includes multiple regions of the same type, which can be located in various portions of the semiconductor structure and can be present at different levels along a height of the semiconductor structure. To this extent, two or more of the regions of the same type can at least partially overlap with one another. In an embodiment, regions of the same type occupy at least five percent of the volume of the semiconductor structure. In another embodiment, regions of the same type occupy at least five percent of the lateral planar area of the semiconductor structure.

[0039] A semiconductor structure can include regions of one or more types. When regions of multiple types are included, the regions of different types can be located anywhere within the semiconductor structure with respect to one another. For example, a transparent region can be located adjacent to a reflective region, a conductive region can be located adjacent to a transparent region and/or a reflective region, and/or the

like. Additionally, a single region can comprise both a transparent region, by allowing at least ten percent of radiation of a target wavelength to pass there through, and a reflective region, by reflecting at least ten percent of the radiation.

[0040] A reflective region can be formed of one or more composite mirrors. A composite mirror includes any structure having multiple sublayers of dielectric or metallic material. Such a composite mirror can be an omnidirectional mirror, which comprises a layer of material having a low index of refraction followed by a metallic reflector or a Bragg mirror. To this extent, FIG. 3A shows a layer including a plurality of reflective regions while FIG. 3B shows an illustrative reflective region according to embodiments. In FIG. 3A, the layer can correspond to a p-type contact layer 22, which is located adjacent to a p-type metal 24. However, it is understood that this is only illustrative. The p-type contact layer 22 is shown including three reflective regions 40A-40C located therein. As illustrated, each reflective region 40A-40C is located adjacent to a planar side of the p-type contact layer 22. However, it is understood that the number of and relative locations of the reflective regions 40A-40C are also only illustrative of various possible configurations.

[0041] As illustrated, a reflective region 40A-40C can be formed of a composite mirror having alternating sublayers of low index of refraction material 42 and relatively high index of refraction material 44 (e.g., a metallic reflector or a Bragg mirror). Furthermore, a sublayer of the reflective region 40A-40C closest to the p-type side 19B of the active region can be formed of a low index of refraction material 42. In an embodiment shown in FIG. 3B, a reflective region 40 (e.g., a Bragg mirror) can be epitaxially grown, and include a superlattice of group III nitride semiconductor sublayers 42, 44 of $Al_xIn_yGa_{1-x-}$

$_{y}N/Al_{x'}In_{y'}Ga_{1-x'-y'}N$, where x, y, x', and y' are chosen such that a refractive index of one sublayer is different from a refractive index of another sublayer by at least two percent (five percent in another embodiment). In a more particular embodiment, the refractive index of a group III nitride semiconductor alloy varies between values of 2.2 and 2.7 by adjusting a molar fraction of aluminum and/or indium. In an illustrative embodiment, x (the molar fraction of aluminum in one of the sublayers) is greater than 0.4. Only values with relatively high molar fractions are important in order to have Bragg mirrors with low absorption characteristics. Typical Bragg mirrors are designed to have alternative sublayers of low and high refractive index, with sublayer thicknesses being a quarter of a target wavelength (λ), wherein the target wavelength corresponds to a wavelength of radiation measured in the semiconductor material. In an embodiment, the Bragg mirror includes at least ten layers.

[0042] In an embodiment, a semiconductor structure, such as the p-type contact layer 22, includes a sufficient number and configuration of reflective regions 40A-40C (e.g., Bragg mirrors) to provide at least a ten percent reflectivity for the entire semiconductor structure 22. In another embodiment, the reflective regions 40A-40C also can serve as transparent regions, which concurrently transmit and reflect at least ten percent of the radiation. In still another embodiment, such a transparent and reflective region can reflect at least twenty percent of radiation having a target wavelength at the normal direction to the region surface.

[0043] A reflective region 40 can be formed using another deposition solution, such as thermal evaporation, magnetron sputtering, ion-beam deposition, laser beam evaporation, and/or the like. A reflective region 40 formed using an alternative solution

to epitaxial growth can utilize one or more of a larger selection of materials for the sublayers. For example, a reflective region 40 can include sublayers of a low index of refraction material, such as silicon dioxide (SiO_2), magnesium oxide (MgO), magnesium fluoride (MgF_2), and/or the like, and sublayers of a high index of refraction material such as aluminum oxide (Al_2O_3), scandium oxide (Sc_2O_3), magnesium aluminum oxide ($MgAl_2O_3$), and a group III nitride (e.g., $Al_xIn_yGa_{1-x-y}N$). As a result, a larger variability in the refractive indices of the sublayers is possible. For example, the refractive index of one sublayer can differ from the refractive index of another sublayer by at least three percent (ten percent in a more particular embodiment). In an embodiment, a sublayer with a low index of refraction can be deposited followed by either a metallic reflector or a Bragg mirror. Similar to Bragg mirrors grown epitaxially, a thickness of each sublayer can be chosen to be a quarter of a target wavelength, where the target wavelength is the wavelength of the radiation measured in the sublayer material.

[0044] A semiconductor structure (e.g., the p-type contact layer 22) including transparent, reflective, and/or conductive regions can be fabricated using patterning. For example, an initial group III nitride semiconductor layer can be epitaxially grown on a surface, followed by deposition of transparent, reflective, and/or conductive (vertically and/or horizontally) region(s) over the semiconductor layer by means of thermal evaporation, magnetron sputtering, ion-beam deposition, laser beam evaporation, and/or the like. Alternatively, one or more of the regions can be epitaxially grown above the group III nitride semiconductor layer. The deposited region(s) can be patterned, e.g., using photolithography, which includes depositing a photoresist, exposing patterned areas to high intensity light, and etching the exposed areas. Some portions of

the deposited region(s) can be etched, and a group III nitride semiconductor layer is overgrown in the etched regions. The process of patterning can be repeated, again depositing a next layer of transparent, reflective, and/or conductive region(s). More complicated deposition and patterning are also possible, which can result in various arrangements of transparent, reflective, and/or conductive regions. For example, after etching portions of the deposited region(s), a second set of region(s) of a different type can be deposited in the etched regions (e.g., to form laterally adjacent regions of different types).

[0045] FIG. 4 shows an illustrative semiconductor structure 50 according to an embodiment. The semiconductor structure 50 includes a vertically conductive region 52 and a background base semiconductor structure 54 and is located adjacent to a metallic contact 60. In an embodiment, the background base semiconductor structure 54 comprises a group III nitride semiconductor layer, a structure composed of group III nitride semiconductor layers, or the like. In a more particular embodiment, the background base semiconductor structure 54 comprises a superlattice comprising $Al_xIn_yGa_{1-x-y}N/Al_{x'}In_{y'}Ga_{1-x'-y'}N$ sublayers. In this case, the superlattice can have an enhanced horizontal conductivity. The semiconductor structure 50 further includes reflective regions 56 (e.g., composite mirrors) and transparent regions 58. As illustrated, the transparent regions 58 can be located at several different levels within the semiconductor structure 50. Similarly, while not shown in FIG. 4, the reflective regions 56 can be located at different levels. A size of the regions 56, 58 can vary, e.g., based on a method utilized for fabricating such regions 56, 58. For example, regions 56, 58 formed using epitaxial growth can be ten to one thousand nanometers, whereas

regions 56, 58 produced through patterning can result in a region size of several micrometers or larger.

[0046] In an embodiment, a semiconductor structure can include transparent regions and reflective regions interspersed with vertically conductive regions such that any lateral cross section of the semiconductor structure contains at least one transparent or reflective region and at least one vertically conductive region. For example, the semiconductor structure 50 can include a sufficient number of reflective regions 56 and transparent regions 58 arranged in conjunction with the vertically conductive region 52 to meet such a condition. Still further, an illustrative arrangement of regions can include regions of two or more types laterally adjacent to one another (e.g., joined). For example, a semiconductor structure can include an arrangement in which transparent or reflective regions are laterally adjacent to vertically conductive regions.

[0047] In an embodiment, a transparent region, such as one or more of the transparent regions 58, comprises an $Al_xIn_yGa_{1-x-y}N/Al_{x'}In_{y'}Ga_{1-x'-y'}N$ superlattice with x, y, x' and y' chosen such that the transparency of the superlattice is at least ten percent for a target wavelength of radiation. In another embodiment, the transparent region can be configured to form a Fabry-Perot interference filter for a target wavelength of radiation. For example, FIG. 5 shows a structure for an illustrative Fabry-Perot interference filter 62 according to an embodiment. In this case, the filter 62 comprises a superlattice including a series of alternating layers of $Al_xIn_yGa_{1-x-y}N/Al_{x'}In_{y'}Ga_{1-x'-y'}N$, where x and x' molar fractions are larger than 0.35. The molar fractions x, x' are chosen to improve a transparency of the layers within the superlattice to radiation having a target wavelength. In an embodiment, y and y' are both zero (i.e., the layers do not

include indium). Each layer in the superlattice has a thickness of approximately one quarter the target wavelength (λ), except for a middle layer having a thickness of approximately one half the target wavelength. In this manner, the filter 62 only transmits radiation having the target wavelength. In another embodiment, the transparent region 58 includes aluminum oxide (Al_2O_3), fused silica, aluminum nitride, or the like which can be deposited by means of thermal evaporation, magnetron sputtering, ion-beam deposition, or laser beam evaporation, and/or the like.

[0048] As discussed herein, a semiconductor structure can include a material having an enhanced horizontal conductivity (e.g., the background base semiconductor structure 54 of FIG. 4). FIG. 6 shows a band diagram 64 of an illustrative embodiment of a horizontally conductive material according to an embodiment. In this case, the material comprises an $Al_xIn_yGa_{1-x-y}N/Al_{x'}In_{y'}Ga_{1-x'-y'}N$ superlattice having barriers and quantum wells alternating along a height of the material. Regions 66 and 68 correspond to localized concentration of electrons and holes, respectively, and result in the formation of two dimensional carrier gases. In particular, region 66 results in the formation of a two dimensional electron gas (2DEG), while region 68 results in the formation of a two dimensional hole gas (2DHG). The carrier gases have a high mobility in the lateral direction, which results in a horizontally conductive layer. In general, higher changes in band gap produce larger polarization fields, which can lead to an increase concentration of the carrier gases. In an illustrative example, a superlattice including layers of $GaN/Al_{0.3}Ga_{0.7}N$ provides a horizontally conductive material superlattice. In another embodiment, more than a two percent change in band gap is desired for formation of 2DEG.

[0049] As discussed herein, regions of any of the types (e.g., reflective, transparent, or conductive), can be located in various arrangements within a semiconductor structure. To this extent, FIGS. 7A-7C show illustrative arrangements of reflective regions according to embodiments. In FIG. 7A, a semiconductor base layer 70 is located adjacent to a metal contact 72 and includes two levels 74A, 74B of reflective regions. Each level 74A, 74B of reflective regions is immersed in the semiconductor base layer 70. Additionally, reflective regions located in level 74B are laterally offset (staggered) from reflective regions located in level 74A. FIG. 7C shows a top view of an embodiment in which the levels 74A, 74B of reflective regions can be staggered in a manner that forms a checkerboard arrangement. In FIG. 7B, a first level 76A of reflective regions is located adjacent to an interface of the semiconductor base layer 70, while a second level 76B of reflective regions penetrates the metal contact 72. It is understood that these arrangements are only illustrative of various possible arrangements of regions.

[0050] FIGS. 8A and 8B show illustrative reflective regions 80A, 80B comprising omnidirectional mirrors according to embodiments. The mirror for each reflective region 80A, 80B comprises a low refractive index layer 82 located within a contact layer, such as the p-type contact layer 22. Additionally, each reflective region 80A, 80B comprises a highly reflective layer 84 located adjacent to an opposite side of the low refractive index layer 82 as the active region 18. Reflective region 80B further includes a distributed dielectric mirror 86 located between the low refractive index layer 82 and the highly reflective layer 84. The reflective regions 80A, 80B can further include a set of conductive regions 88, each of which can extend from the contact layer 22 to the highly

reflective layer 84. The conductive regions 88 can comprise metallic or other conductive material regions. In an embodiment, the conductive regions 88 can be fabricated by etching the low refractive index layer 82 and distributed dielectric mirror 86 to access the contact layer 22 located underneath.

[0051] A semiconductor structure can include any combination and/or arrangement of the various types of regions, which can be selected based on a set of performance requirements for the semiconductor structure and/or the corresponding device. In an embodiment, the semiconductor structure can include vertically and horizontally conductive regions arranged to form an interconnected network of conductive paths through the semiconductor structure. The term "interconnected" network does not necessarily imply that all the conductive regions form a single network. As used herein, the term is applied loosely and includes clusters of overlapping conductive regions disconnected by gaps. In an embodiment, a typical cluster size and cluster density is chosen to match a conductivity requirement of the semiconductor structure. For example, for a semiconductor structure formed adjacent to a p-type contact, the cluster density and cluster size can be chosen to provide such conductivity of the p-type contact that a voltage drop across the p-type contact is ten percent or less than a voltage drop across the entire device.

[0052] As discussed herein, an embodiment of the semiconductor structure can be included in an optoelectronic device, such as a light emitting diode, a deep ultraviolet light emitting diode, a light sensor, other types of optoelectronic solid state devices, and/or the like. In a more specific embodiment, the semiconductor structure is incorporated in such a device to improve light extraction characteristics of the

corresponding device. Returning to FIGS. 1 and 2, a semiconductor structure described herein can be incorporated as some or all of the p-type contact layer 22 and/or n-type contact layer 16.

[0053] In an embodiment of the device 10 shown in FIG. 1 or FIG. 2, a metallic contact 24 and/or a metallic contact 28 can comprise a multilayered structure. For example, the metallic contact 24, 28 can include an ohmic layer adjacent to the corresponding contact layer 22, 16, respectively, followed by a reflective layer located adjacent to the ohmic layer. The ohmic layer can be transparent to radiation having a target wavelength as described herein, while the reflective layer can be reflective to radiation having the target wavelength. In a more specific embodiment, the ohmic layer allows at least twenty percent of radiation having a target wavelength, which is radiated at a normal incidence to an interface of the ohmic layer, to pass there through. In another more specific embodiment, the reflective layer reflects at least fifty percent of radiation having the target wavelength, which is radiated at a normal incidence to an interface of the reflective layer. In an embodiment, the target wavelength corresponds to ultraviolet light, e.g., within a range of wavelengths between approximately 260 and approximately 360 nanometers.

[0054] A metallic contact 24 and/or a metallic contact 28 can include one or more additional layers, e.g., to improve stability, reflectivity, and/or conductive properties of the ohmic contact. For example, FIG. 9 shows an illustrative multilayered metallic contact 90 according to an embodiment. In this case, the contact 90 includes an ohmic layer 92, an ohmic protective layer 94, a reflective layer 96, a reflective protective layer 98, and a conductive metallic layer 100. Each layer 92, 94, 96, 98, 100 can be formed

of any suitable material and can be fabricated using any solution. For example, the ohmic contact layer 92 can be one of: cobalt (Co), nickel (Ni), palladium (Pd), iron (Fe), platinum (Pt), or the like. Additionally, the ohmic contact layer 92 can include one or sub-layers of metals. Such a sub-layer can include the above metals as well as: Pd, rhodium (Rh), ruthenium (Ru), osmium (Os), iridium (Ir), thorium (Th), and boron (B), and can incorporate one or more of: calcium (Ca), magnesium (Mg), beryllium (Be), manganese (Mn), or tin (Sn), with a maximum concentration up to approximately 10^{21} cm^{-3}. For example, the ohmic layer 92 can include: a sub-layer of Co/Mg/Ni having a thickness of approximately one to two nanometers, which can act as an adhesive; a two to five nanometer sub-layer of palladium, which can provide a good ohmic contact; and a sub-layer of rhodium having a thickness of approximately 150 Angstroms. The ohmic protective layer 94 can comprise: Pt, rhenium (Re), Pd, Rh, Ru, Os, Ir, or the like; an oxide, such as indium tin oxide (ITO), zinc oxide (ZnO), or the like; and/or the like. The ohmic protective layer 94 can be as thick as few tens of nanometers. The reflective layer 96 can comprise Al, and be relatively thick (e.g., as much as a few hundred nanometers). A reflective protective layer 98 can comprise titanium (Ti), zirconium (Zr), hafnium (Hf), molybdenum (Mo), tungsten (W), Pd, Rh, Ru, Os, Ir, vanadium (V), chromium (Cr), Pt, or their allows. A conductive metallic layer 100 can comprise a layer of any type of material having a high electrical conductivity, including copper (Cu), silver (Ag), gold (Au), nickel (Ni), or their alloys.

[0055] An ohmic layer and/or reflective layer of a metallic contact 24 and/or a metallic contact 28 can be discontinuous. For example, a layer can comprise a plurality of island formations. The island formations can have a characteristic size of between ten

to two thousand nanometers (up to one hundred thousand nanometers in another embodiment) and can be separated from one another by a characteristic distance of approximately the same order as the characteristic size of the islands. In an embodiment, the ohmic and reflective islands are interspersed with each other. Similarly, a semiconductor layer located adjacent to a metallic contact 24 and/or a metallic contact 28 can have a laterally inhomogeneous structure.

[0056] For example, FIG. 10 shows an illustrative interface between a semiconductor layer 102 and a metallic contact 110 according to an embodiment. The semiconductor layer 102 is shown including laterally adjacent regions 104, 106, which can have distinct properties. In an embodiment, a first set of regions 104 comprise conductive regions, while a second set of regions 106 comprise transparent or reflective regions. The metallic contact 110 is shown having an ohmic layer formed of a plurality of ohmic islands 112A-112F, over which a reflective layer 114 can be located. The ohmic islands 112A-112F can be randomly located or patterned. Furthermore, an alignment of the ohmic islands 112A-112F with respect to the regions 104, 106 of the semiconductor layer 102 can be random or predetermined. In the latter case, any solution can be utilized for the alignment including for example, semiconductor layer patterning and overgrowth, ohmic layer patterning, and/or the like. As illustrated, a characteristic distance D between the ohmic islands 112A-112F can be comparable to a characteristic lateral size of the ohmic islands 112A-112F.

[0057] FIGS. 11A-11C show illustrative n-type contact layers 116A-116C, respectively, including reflective regions 118 according to embodiments. The reflective regions 118 can comprise, for example, superlattices of $Al_xIn_yGa_{1-x-y}N/Al_{x'}In_{y'}Ga_{1-x'-y'}N$

layers, which can be grown epitaxially. Since the n-type contact layers 116A, 116B can have thicknesses of several microns, relatively thick composite reflective regions 118 can be utilized which can lead to a higher degree of reflection. As illustrated in FIG. 11A, inclusion of the reflective regions 118 in the n-type contact layer 116A can provide a more efficient reflection of radiation towards the p-type contact 24. For an efficient extraction of radiation from the device 111, the p-type contact 24 and the p-type contact layer 22 should be transparent to the radiation generated by the active region 18 (e.g., transmitting at least thirty percent of the radiation of a target wavelength in an embodiment).

[0058] As shown in FIGS. 11B and 11C, a n-type metal contact 120A-120C can include metallic protrusions 122 extending into the n-type contact layer 116B, 116C. Furthermore, as shown in FIG. 11C, a n-type contact layer 116C can include conductive regions 124A, 124B having high horizontal conductivity in a location of the protrusions 122. The protrusions 122 can deliver the current to the horizontally conductive regions 124A, 124B, which can spread the current horizontally to other regions having a high vertical conductivity (e.g., the background base semiconductor structure of the n-type contact layer 116C). Furthermore, a n-type metal contact, such as the metal contact 120C, can be adjacent to region(s) of high vertical conductivity. The metal contact 120C provides a vertical design for the n-type contact structure and can be included alone or in combination with the horizontal designed metal contacts 120A, 120B. In an embodiment, the metal contact 120C is formed by removing a substrate used for epitaxial growth of the semiconductor layer(s) and depositing the n-type metal contact 120C on the exposed surface of the semiconductor layer.

[0059] Any of the semiconductor structures described herein, as well as other structures that include any of the concepts of the various embodiments described herein can be incorporated into an optoelectronic device such as one of those devices listed above. FIG. 12 shows a schematic of a laser lift-off method to lift a semiconductor structure, such as any of the structures described herein, from a substrate 130 according to an embodiment. As shown on the left-hand side of FIG. 12, a semiconductor heterostructure 132 can be formed on the substrate 130 via a sacrificial layer 134, a semiconductor layer 136 and a buffer layer 138.

[0060] The semiconductor heterostructure 132 can include an active region 140, a p-type contact layer 142 located on a first side of the active region 140, and a n-type contact layer 144 located on a second side of the active region 140 opposite the first side. A p-type metal layer 146 can be formed on the p-type contact layer 142. Any of the aforementioned materials are suitable for use with the active region 140, the p-type contact layer 142, the n-type contact layer 144 and the p-type metal layer 146. A semiconductor heterostructure formed from group III nitride layers is one example of materials that can be used since these layers can grow over the substrate 130, the sacrificial layer 134, the semiconductor layer 136 and the buffer layer 138.

[0061] Although not shown in FIG. 12, either one or both of the p-type contact layer 142 and the n-type contact layer 144 can include a group III nitride semiconductor layer having a plurality of inhomogeneous regions that can take the form of any of the previously described embodiments. In this manner, each inhomogeneous region in either the p-type contact layer 142 and the n-type contact layer 144 can have a set of attributes that differ from the group III nitride material forming the semiconductor layer.

In one embodiment, the plurality of inhomogeneous regions can include a set of first inhomogeneous regions configured based on radiation having a target wavelength, wherein the set of first inhomogeneous regions are at least one of: transparent to the radiation or reflective of the radiation: The plurality of inhomogeneous regions can further include a set of second inhomogeneous regions having a conductivity that is at least ten percent higher than a conductivity of the set of first inhomogeneous regions. Each of the sets of inhomogeneous regions can occupy at least five percent of at least one of: a lateral planar area of the semiconductor layer or a volume of the semiconductor layer. In one embodiment, at least some of the sets of inhomogeneous regions do not fully overlap with each other.

[0062] The substrate 130 can include any substrate that is well-known for growing semiconductor layers thereon. One example of a substrate can include sapphire, but other substrates are possible. The buffer layer 138 can be a semiconductor layer that provides some separation from the semiconductor heterostructure 132. The buffer layer 138 can include, but is not limited to, aluminum nitride or gallium nitride. In some embodiments, the buffer layer 138 can comprise an $Al_xGa_{1-x}N$ layer, with $x > 0.8$.

[0063] The semiconductor layer 136 can serve to improve the subsequent heterostructure by reducing the number of dislocations present in the heterostructure. In an embodiment, the semiconductor layer 136 comprises an AlN layer grown under conditions allowing for reduction of dislocations. For example, the semiconductor layer 136 can be grown to have a variable V/III ratio or a presence of one or more AlGaN interlayers. In other cases, the semiconductor layer 136 can contain an $Al_xGa_{1-x}N/Al_yGa_{1-y}N$ superlattice, in which x and y differ by at least 5%. In one embodiment,

the semiconductor layer 136 can include $Al_xIn_yB_zGa_{1-x-y-z}N$. For an embodiment in which an optoelectronic device is an ultraviolet light emitting diode, for which the described technology is preferential, the semiconductor layer 136 can include AlN having a thickness that is chosen to minimize the number of dislocations in subsequent layers. In one embodiment, a typical thickness for a semiconductor layer 136 including AlN can range from about 1 micrometers to about 10 micrometers.

[0064] The sacrificial layer 134 can include a material that is capable of being grown over the semiconductor heterostructure 132 with the semiconductor layer 136, the buffer layer 138 and the substrate layer 130 coupled thereto. In one embodiment, the sacrificial layer 134 can be suitable for use in lift-off techniques where the semiconductor heterostructure 132 is removed from the substrate 130, including the sacrificial layer 134, the semiconductor layer 136, and the buffer layer 138, using laser radiation and subsequent fabrication of an optoelectronic device. In one embodiment, the sacrificial layer 134 can include a group III nitride semiconductor layer with a bandgap value that is lower than the bandgap value of any layer in the semiconductor heterostructure 132. For example, the sacrificial layer 134 can include GaN. In another embodiment, the sacrificial layer 134 can include columnar structures comprising group III nitride semiconductors epitaxially grown over a masked region that has holes or openings for growing sacrificial layer material. For example, the sacrificial layer 134 can include alternating GaN/AlN layers of $Al_xGa_{1-x}N/Al_yGa_{1-y}N$ layers having a difference between molar fractions of x and y that is at least 0.1 and preferably greater than 0.5. In one embodiment, the sacrificial layer 134 can include a large number of compositional lateral fluctuations. For example, the sacrificial layer 134 can include

compositional fluctuations in $Al_xIn_yGa_{1-x-y}N$ alloy with fluctuations both in aluminum and indium molar fractions. In another embodiment, the sacrificial layer 134 can include a semiconductor layer containing holes, vacancies, or a set of disjoint columnar structures. In one embodiment, the sacrificial layer 134 can include combinations of any of the aforementioned sacrificial layers. Also, the sacrificial layer 134 can include tensile and compressive layers

[0065] The thickness of the sacrificial layer 134 can be selected to result in maximum stresses and strains within the layer without significantly altering the number of dislocations within the layer. In one embodiment, the thickness of the sacrificial layer 134 can range from about 10 nanometers (nm) to about 500 nanometers (nm). The exact optimal thickness of the sacrificial layer 134 can be determined by growing the sacrificial layer with different thicknesses and determining the limiting thickness that leads to the onset of dislocations. In one embodiment, the optimal thickness of the sacrificial layer 134 can be selected to be about 10% lower than the maximum allowable thickness before the onset of dislocations. U.S. Provisional Application 62/187707, entitled "A method of releasing group III nitride semiconductor heterostructure," which was filed on 1 July 2015 provides further details of a sacrificial layer and is incorporated herein by reference.

[0066] In one embodiment, the semiconductor heterostructure 132 can be separated from the substrate 130 by irradiating the semiconductor layers that can form the heterostructure from the substrate side to decompose the sacrificial layer, thus separating the semiconductor heterostructure 132 from the substrate 130, the semiconductor layer 136 and the buffer layer 138. A laser lift-off is one example of a

laser radiation technique that can be used to lift semiconductor layers such as a semiconductor heterostructure from a substrate. A laser lift-off is a well-known technique in the art that is used to separate semiconductor layers from a substrate, which can result in improved characteristics of a subsequently fabricated optoelectronic device. U.S. Provisional Application 62/187707 provides further details of several laser-lift off techniques that can be used to irradiate group III nitride semiconductor layers from the substrate side to decompose a sacrificial layer. As shown in the right-hand side of FIG. 12, the semiconductor heterostructure 132 is lifted off the substrate 130, the semiconductor layer 136 and the buffer layer 138 upon the application of a laser emission 148 (left-hand side of FIG. 12). In particular, the laser emission at a specified wavelength is absorbed by the sacrificial layer 134, causing it to decompose, separating the semiconductor heterostructure 132 from the substrate 130.

[0067] FIGS. 13A-13C show multiple views of an optoelectronic device 150 formed from the semiconductor heterostructure 132 depicted in FIG. 12 after a laser lifted off from the substrate 130 according to an embodiment. In particular, FIG. 13A shows a cross-sectional view of the optoelectronic device 150 taken from a cut line AA in FIG. 13B, which shows a top plan view of a top surface 152 of the optoelectronic device 150, while FIG. 13C shows a bottom plan view of a bottom surface 154 of the optoelectronic device 150.

[0068] As shown in FIGS. 13A and 13C, the bottom surface 154 of the optoelectronic device 150 can have a metallic n-type contact 156 having a plurality of metallic domains 158 connected by electrical contacts 159. In particular, the metallic n-type contact 156 and connected metallic domains 158 can be formed on a first side 160 of the n-type

contact layer 144 with an electrical contact 161, such as an n-type electrical contact, coupled to the metallic n-type contact 156. The metallic n-type contact 156 and connected metallic domains 158 can serve to conduct electrical current through the device 150 and/or scatter or reflect the light generated by the device 150. In one embodiment, the metallic n-type contact 156 and connected metallic domains 158 can be made from materials that can include, but are not limited to, titanium, nickel, chromium, a combination of two or more of the materials, and/or the like. It is noted that the electrical contacts 159 that connect the metallic domains 158 can be made sufficiently thin to not pose a significant obstruction to the emitted light from the optoelectronic device 150. The metallic domains 158, which can be n-type domains, can also cover a small fraction of the area of the first side 160 of the metallic n-type contact 156 as not to pose a significant obstruction to the emitted light.

[0069] FIG. 13C also shows that the bottom surface 154 of the optoelectronic device 150 can have roughness elements 162 to improve light extraction from the device. In particular, the roughness elements 162 are interspersed with the metallic domains 158 of the metallic n-type contact 156. The roughness elements can include, but are not limited to, protrusions within the substrate, externally deposited roughness elements comprising shapes of Al_2O_3 or SiO_2, and/or the like.

[0070] As shown in FIGS. 13A and 13B, the top surface 152 of the optoelectronic device 150 can have metallic contact domains 164 formed thereon with an electrical contact 166 coupled thereto. In one embodiment, the metallic contact domains 164 can be p-type metallic contact domains that are formed on a side 168 of the p-type contact layer 142, and the electrical contact 166 can be a p-type electrical contact. As shown in

FIG. 13B, the metallic contact domains 164 can be located on various locations throughout the side 168 of the p-type contact layer 142. Each of these metallic contact domains 164 can coupled to an electrical contact 166. In one embodiment, the p-type metallic contact domains 164 can be made from materials that can include, but are not limited to, nickel, rhodium, palladium, aluminum, and/or the like. In an embodiment, a metallic contact domain 164 comprises a multi-layer metallic structure with the first metallic layer being nickel. The electrical contact 166, which as noted above can be a p-type electrical contact, can be made from materials that can include, but are not limited to, UV reflective material, aluminum, rhodium or other conductive and partially UV reflective metal, and/or the like.

[0071] The optoelectronic device 150 can also include UV reflective elements 170 that can protect the p-type contact layer electrical contact 166 by preventing emitted UV radiation from being absorbed by the p-type contact layer electrical contact 166. In one embodiment, the reflective elements 170 can be incorporated or embedded within the p-type contact layer 142. In one embodiment, the reflective elements 170 can be incorporated in multiple levels of the p-type contact layer 142. As shown in FIG. 13A, the reflective elements 170 in each level can be staggered with reflective elements in an adjacent level such that there is an offset in position between elements in the different levels. It is understood that the two levels depicted in FIG. 13A are illustrative of one example, and that it is possible to have more levels, or only one level.

[0072] The reflective elements 170 can include, but are not limited to, a dielectric, metallic reflective islands, Bragg mirrors, omnidirectional reflectors such as combination of metallic and dielectric films, and combinations thereof. In an embodiment where the

reflective elements 170 are formed from Bragg mirrors, these elements can include alternating layers of dielectric with at least one of the layers being Hf_2O_3. In another embodiment, the Bragg mirrors can be formed from alternating layers of one of Hf_2O_3 and Al_2O_3, H_2O_3 and SiO_2, and Al_2O_3 and SiO_2. The alternating layers of H_2O_3 and SiO_2 can have the highest contrast in the index of refraction, and thus, can provide the best reflection. These types of Bragg mirrors can be obtained by depositing alternative sequences of the dielectric material with subsequent patterning. It is understood that several deposition patterning and overgrowth steps may be needed to produce the right combination of reflective domains such that the reflective elements 170 can have the staggered arrangement illustrated in FIG. 13A. The Bragg mirrors can also be combined with a highly reflective layer. As used herein, a highly reflective layer is a layer that is at least 50% reflective to a normal radiation. For example, the highly reflective layer can include a metallic layer such as aluminum. In another embodiment, the highly reflective layer can include a dielectric or a polymer layer that is diffusively reflective such as polytetrafluoroethylene (PTFE), a highly ultraviolet reflective expanded polytetrafluoroethylene (ePTFE) membrane (e.g., GORE® Diffuse Reflector Material), and/or the like.

[0073] Although not shown in the figures, the reflective elements 170 can be incorporated within the n-type contact layer 144. In this manner, the reflective elements 170 can aid in improving light extraction of the optoelectronic device 150.

[0074] The top surface 152 of the optoelectronic device 150 can further include a p-type metallic contact 172 having p-type metallic domains 174 formed on the side 168 of the p-type contact layer 142. Each of the p-type metallic domains 174 can be separated

from adjacent p-type metallic domains 174 by a predetermined spacing. In one embodiment, as shown in FIGS. 13A-13B, the p-type metallic domains 174 can be separated by a p-type metallic contact domain 164. The p-type metallic domains 174 serve to reflect the light, while the domains 164 can be used primarily for delivering current to the semiconductor structure. In one embodiment, the p-type metallic domains 174 can be made from materials that can include, but are not limited to, UV reflective material, such as aluminum or rhodium.

[0075] Regions between the p-type metallic contact domain 164 and the p-type metallic domains 174 can include a transparent or reflective domain 176. It is understood for clarity that only one transparent or reflective domain 176 is shown in FIG. 13B, however, it is understood that more of these domains can be deployed on the top surface 152 of the optoelectronic device 150 In one embodiment, the transparent or reflective domain 176 can include either a UV transparent or partially UV transparent material or reflective Bragg mirrors that act as UV reflective domains. In another embodiment, the domain 176 can include omnidirectional mirrors such as a layer of dielectric and a layer of highly reflective metal. In an embodiment the highly reflective metal can be substituted by a highly ultraviolet reflective expanded polytetrafluoroethylene (ePTFE) membrane (e.g., GORE® Diffuse Reflector Material), and/or the like.

[0076] The top surface 152 of the optoelectronic device 150 can also have a passivation layer 178 with or without disjoint domains 180. As shown in FIGS. 13A-13B, the passivation layer 178 and the disjoint domains 180 can be formed on a surface of the p-type contact layer 142. In one embodiment, the passivation layer 178 and the

disjoint domains 180 can be formed underneath the metallic p-type contact domain 164. The passivation layer 178 can function to reduce deterioration of the surface, and possible recombination effects at the surface, while the role of the disjoint domains 180 is to reduce absorption of light at the p-type surface. As shown in FIG. 13A, electrical contacts 182 can connect the disjoint domains 180 to the metallic domains 158 of the metallic n-type contact 156 so that the domains 180 can form an electrical network. In one embodiment, the passivation layer 178 can include, but is not limited to, a dielectric material such as SiO_2, Al_2O_3, Si_3N_4, and or the like. In one embodiment, the disjoint domains 180 can include, but are not limited to, nickel and rhodium based domains.

[0077] It is understood that not all of the elements described for the optoelectronic device 150 as shown in FIGS. 13A-13C are necessary for use. For example, a regular contact structure can be used in conjunction with the reflective elements 170. As used herein, a regular contact structure is a continuous metallic layer deposited over a semiconductor layer, which is followed by annealing to form a contact to the semiconductor layer. Alternatively, the reflective elements 170 can be absent from the optoelectronic device 150. In such an embodiment, the contact structure can utilize the disjoint domains 180. Alternatively, it is understood that reflective elements 170 that utilize Bragg mirrors do not have to be arranged in a staggered formation and can have other formations. In addition, it is understood that details of the n-type contact layer 144 can also vary. For example, the n-type contact layer 144 can include conductive, partially transparent oxide domains. In addition, the exact position of the roughness elements 162 can also be varied. Furthermore, it is possible that the n-type contact layer 144 can take the form of the structure depicted in FIG. 11A after using a lift-off

technique. In this embodiment, then the entire surface 160 of the n-type contact layer 144 can contain roughness elements. Furthermore, the metallic n-type contact 156 and the connected metallic domains 158 of the n-type contact layer 144 can be partially located on the surface 160. In this manner, it would be partially deposited as shown in FIG. 11A.

[0078] The optoelectronic device 150 depicted in FIGS. 13A-13C, which can take the form of a vertical device having reflective, transparent and contacts can have several benefits. A first benefit is that there will be vertical current flow in the device that avoids current crowding, which is due to the location of the metallic p-type contact domains 164 and the n-type contact 156. This makes the optoelectronic device 150 suited to operate as a vertical light emitting diode having a vertical structure obtained through a laser lift-off technique. A second benefit is that the optoelectronic device 150 can have a larger emitting area as there is no area required for placing the n-type contact.

[0079] Various embodiments of the semiconductor structures described herein can be fabricated using any solution, including patterning, masking, epitaxial growth, and/or the like. An illustrative solution for producing a laterally inhomogeneous semiconductor structure includes depositing group III nitride semiconductor alloys under a faceted and/or three-dimensional growth mode as shown and described in U.S. Patent No. 7,812,366. This solution is notably different from conventional approaches of growing AlGaN films and can lead to a surface morphology having large scale faceting evidencing metal droplets. In conventional approaches, the films are typically produced at a very high gallium flux, which results in a surface of the AlGaN film typically having a smooth morphology. In another embodiment described herein, inhomogeneous regions

within a semiconductor structure can be produced using a MOCVD approach, which is distinctly different from the approach described in U.S. Patent No. 7,812,366.

[0080] Ternary and quaternary nitride semiconductor epitaxial layers inherently grow inhomogeneously due to contrasting optimum growth conditions needed for respective binary layers. In an embodiment, inhomogeneity in aluminum-containing nitride layers is further enhanced by intentionally lowering a mobility of aluminum adatoms. For example, aluminum mobility on the growing surface is strongly influenced by growth temperature and V/III molar ratio. In an illustrative embodiment, three dimensional inhomogeneous structures are formed with V/III ratio being above 1000 (e.g., in a range between 1000 and 100000) and growth temperatures being in the range of 500 – 1300 degrees Celsius. Adjacent semiconductor layers can be grown using such a group V/III ratio and growth temperatures, while varying a molar fraction of one or more of the elements (e.g., a molar fraction of aluminum can differ by at least one percent between adjacent layers).

[0081] In one embodiment, the invention provides a method of designing and/or fabricating a circuit that includes one or more of the devices designed and fabricated as described herein (e.g., including one or more emitting devices including a semiconductor structure described herein). To this extent, FIG. 14 shows an illustrative flow diagram for fabricating a circuit 1026 according to an embodiment. Initially, a user can utilize a device design system 1010 to generate a device design 1012 for a semiconductor device as described herein. The device design 1012 can comprise program code, which can be used by a device fabrication system 1014 to generate a set of physical devices 1016 according to the features defined by the device design 1012.

Similarly, the device design 1012 can be provided to a circuit design system 1020 (e.g., as an available component for use in circuits), which a user can utilize to generate a circuit design 1022 (e.g., by connecting one or more inputs and outputs to various devices included in a circuit). The circuit design 1022 can comprise program code that includes a device designed as described herein. In any event, the circuit design 1022 and/or one or more physical devices 1016 can be provided to a circuit fabrication system 1024, which can generate a physical circuit 1026 according to the circuit design 1022. The physical circuit 1026 can include one or more devices 1016 designed as described herein.

[0082] In another embodiment, the invention provides a device design system 1010 for designing and/or a device fabrication system 1014 for fabricating a semiconductor device 1016 as described herein. In this case, the system 1010, 1014 can comprise a general purpose computing device, which is programmed to implement a method of designing and/or fabricating the semiconductor device 1016 as described herein. Similarly, an embodiment of the invention provides a circuit design system 1020 for designing and/or a circuit fabrication system 1024 for fabricating a circuit 1026 that includes at least one device 1016 designed and/or fabricated as described herein. In this case, the system 1020, 1024 can comprise a general purpose computing device, which is programmed to implement a method of designing and/or fabricating the circuit 1026 including at least one semiconductor device 1016 as described herein.

[0083] In still another embodiment, the invention provides a computer program fixed in at least one computer-readable medium, which when executed, enables a computer system to implement a method of designing and/or fabricating a semiconductor device

as described herein. For example, the computer program can enable the device design system 1010 to generate the device design 1012 as described herein. To this extent, the computer-readable medium includes program code, which implements some or all of a process described herein when executed by the computer system. It is understood that the term "computer-readable medium" comprises one or more of any type of tangible medium of expression, now known or later developed, from which a stored copy of the program code can be perceived, reproduced, or otherwise communicated by a computing device.

[0084] In another embodiment, the invention provides a method of providing a copy of program code, which implements some or all of a process described herein when executed by a computer system. In this case, a computer system can process a copy of the program code to generate and transmit, for reception at a second, distinct location, a set of data signals that has one or more of its characteristics set and/or changed in such a manner as to encode a copy of the program code in the set of data signals. Similarly, an embodiment of the invention provides a method of acquiring a copy of program code that implements some or all of a process described herein, which includes a computer system receiving the set of data signals described herein, and translating the set of data signals into a copy of the computer program fixed in at least one computer-readable medium. In either case, the set of data signals can be transmitted/received using any type of communications link.

[0085] In still another embodiment, the invention provides a method of generating a device design system 1010 for designing and/or a device fabrication system 1014 for fabricating a semiconductor device as described herein. In this case, a computer

system can be obtained (e.g., created, maintained, made available, etc.) and one or more components for performing a process described herein can be obtained (e.g., created, purchased, used, modified, etc.) and deployed to the computer system. To this extent, the deployment can comprise one or more of: (1) installing program code on a computing device; (2) adding one or more computing and/or I/O devices to the computer system; (3) incorporating and/or modifying the computer system to enable it to perform a process described herein; and/or the like.

[0086] The foregoing description of various aspects of the invention has been presented for purposes of illustration and description. It is not intended to be exhaustive or to limit the invention to the precise form disclosed, and obviously, many modifications and variations are possible. Such modifications and variations that may be apparent to an individual in the art are included within the scope of the invention as defined by the accompanying claims.

CLAIMS

What is claimed is:

1. A semiconductor heterostructure, comprising:

an active region;

a metallic contact;

a group III nitride semiconductor layer located between the active region and the metallic contact, the semiconductor layer including a plurality of inhomogeneous regions arranged within multiple levels of the semiconductor layer, wherein some of the inhomogeneous regions in a first level of the semiconductor layer are vertically offset from inhomogeneous regions in a second level of the semiconductor layer, and wherein the plurality of inhomogeneous regions include one or more of a set of transparent regions, a set of reflective regions and/or a set of conductive regions, each of the inhomogeneous regions having a set of attributes differing from a group III nitride material forming the semiconductor layer.

2. The semiconductor heterostructure of claim 1, wherein each of the inhomogeneous regions in the first level and the second level of the semiconductor layer includes a set of reflective regions.

3. The semiconductor heterostructure of claim 1, wherein each of the plurality of inhomogeneous regions in the first level of the semiconductor layer extend into the

metallic contact and each of the plurality of inhomogeneous regions in the second level of the semiconductor layer are located at an interface of the semiconductor layer.

4. The semiconductor heterostructure of claim 1, wherein all of the inhomogeneous regions in the first level of the semiconductor layer are staggered with the inhomogeneous regions in the second level of the semiconductor layer to form a checkerboard arrangement of the inhomogeneous regions within the semiconductor layer.

5. The semiconductor heterostructure of claim 1, wherein the inhomogeneous regions in the first level of the semiconductor layer each has a surface contacting the metallic contact, wherein at least one metal protrusion from the metallic contact extends into each inhomogeneous region.

6. The semiconductor heterostructure of claim 5, wherein each of the inhomogeneous regions in the first level of the semiconductor layer comprises a set of conductive regions and each of the inhomogeneous regions in the second level of the semiconductor layer comprises a set of reflective regions.

7. The semiconductor heterostructure of claim 6, wherein each of the inhomogeneous regions in the second level of the semiconductor layer has at least one metal protrusion extending from the metallic contact into the semiconductor layer that is directed to a surface of the inhomogeneous region without contact thereof.

8. A method, comprising:

fabricating a semiconductor heterostructure, wherein the semiconductor heterostructure comprises:

an active region;

a metallic contact;

a group III nitride semiconductor layer located between the active region and the metallic contact, the semiconductor layer including a plurality of inhomogeneous regions arranged within multiple levels of the semiconductor layer, wherein some of the inhomogeneous regions in a first level of the semiconductor layer are vertically offset from inhomogeneous regions in a second level of the semiconductor layer, and wherein the plurality of inhomogeneous regions include one or more of a set of transparent regions, a set of reflective regions and/or a set of conductive regions, each of the inhomogeneous regions having a set of attributes differing from a group III nitride material forming the semiconductor layer.

9. The method of claim 8, wherein the fabricating includes:

epitaxially growing a portion of the group III nitride semiconductor layer;

forming at least one of the sets of inhomogeneous regions on a surface of the portion of the group III nitride semiconductor layer; and

epitaxially over-growing the group III nitride semiconductor layer after the forming.

10. The method of claim 9, wherein the forming includes:

depositing the at least one of the sets of inhomogeneous regions using one of: thermal evaporation, magnetron sputtering, ion-beam deposition, or laser beam evaporation; and

patterning the at least one of the sets of inhomogeneous regions using photolithography.

11. An optoelectronic device, comprising:

a semiconductor heterostructure, obtained through laser lift-off, having a first side and a second side, the semiconductor heterostructure including:

a group III nitride semiconductor layer including a plurality of inhomogeneous regions, each inhomogeneous region having a set of attributes differing from a group III nitride material forming the semiconductor layer, wherein the plurality of inhomogeneous regions include:

a set of first inhomogeneous regions configured based on radiation having a target wavelength, wherein the set of first inhomogeneous regions are at least one of: transparent to the radiation or reflective of the radiation; and

a set of second inhomogeneous regions having a conductivity at least ten percent higher than a conductivity of the set of first inhomogeneous regions, wherein each of the sets of inhomogeneous regions occupy at least five percent of at least one of: a lateral planar area of the semiconductor layer or a volume of the semiconductor layer, and wherein at least some of the sets of inhomogeneous regions do not fully overlap.

12. The optoelectronic device of claim 11, further comprising a first metallic contact having a plurality of connected metallic domains formed on the first side of the semiconductor heterostructure.

13. The optoelectronic device of claim 11, further comprising a plurality of roughness elements formed on the first side of the semiconductor heterostructure.

14. The optoelectronic device of claim 11, further comprising a plurality of metallic contact domains formed on the second side of the semiconductor heterostructure.

15. The optoelectronic device of claim 11, further comprising a plurality of reflective elements incorporated within the semiconductor heterostructure proximate a surface of the second side of the semiconductor heterostructure.

16. The optoelectronic device of claim 15, wherein the plurality of reflective elements comprise one of dielectrics, metallic reflective islands, Bragg mirrors and combinations thereof.

17. The optoelectronic device of claim 15, wherein the plurality of reflective elements comprise alternating layers of one of Hf_2O_3 and Al_2O_3, H_2O_3 and SiO_2, and Al_2O_3 and SiO_2.

18. The optoelectronic device of claim 11, further comprising a plurality of Bragg domains formed on the second side of the semiconductor heterostructure.

19. The optoelectronic device of claim 11, further comprising a second metallic contact having metallic domains formed on the second side of the semiconductor heterostructure, each of the metallic domains separated from an adjacent metallic domain by a predetermined spacing.

20. The optoelectronic device of claim 11, further comprising a passivation layer formed on the second side of the semiconductor heterostructure and a plurality of disjoint domains interspersed within the passivation layer.

ABSTRACT

A semiconductor layer including a plurality of inhomogeneous regions is provided. Each inhomogeneous region has one or more attributes that differ from a material forming the semiconductor layer. The inhomogeneous regions can include one or more regions configured based on radiation having a target wavelength. These regions can include transparent and/or reflective regions. The inhomogeneous regions also can include one or more regions having a higher conductivity than a conductivity of the radiation-based regions, e.g., at least ten percent higher. In one embodiment, the semiconductor layer is used to form an optoelectronic device.

DECLARATION (37 CFR 1.63) FOR UTILITY OR DESIGN PATENT APPLICATION USING AN APPLICATION DATA SHEET (37 CFR 1.76)

As a below named inventor, I hereby declare that:

This declaration is directed to:

Title of the Invention: Semiconductor Structure with Inhomogeneous Regions

Attorney Docket Number: SETI-0110-CIP-US

the specification of which:

☒ is attached hereto, or

☐ is United States Patent Application No. _____ filed on _____, or

☐ is PCT International Application No. _____ filed on _____.

The above-identified application was made or authorized to be made by me.

I believe that I am the original inventor or an original joint inventor of a claimed invention in the application.

I hereby state that I have reviewed and understand the contents of the above-identified application, including the claims.

I hereby acknowledge that I have a duty to disclose information which is material to the patentability as defined in Title 37, Code of Federal Regulations, §1.56.

I hereby acknowledge that any willful false statement made in this declaration is punishable under 18 U.S.C. 1001 by fine or imprisonment of not more than five (5) years, or both.

Legal Name of inventor: **Maxim S. Shatalov**

Inventor's Signature: /_____/

Date: _____

Note: An application data sheet, including naming the entire inventive entity, must accompany this form.

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Legal Name of inventor: **Alexander Dobrinsky**

Inventor's Signature: /_____/

Date: _____

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Legal Name of inventor: **Alexander Lunev**

Inventor's Signature: /_____/

Date: _____

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Legal Name of inventor: **Rakesh Jain**

Inventor's Signature: /_____/

Date: _____

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Legal Name of inventor: **Jinwei Yang**

Inventor's Signature: /_____/

Date: _____

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Legal Name of inventor: **Michael Shur**

Inventor's Signature: /_____/

Date: _____

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Legal Name of inventor: **Remigijus Gaska**

Inventor's Signature: /_____/

Date: _____

Note: An application data sheet, including naming the entire inventive entity, must accompany this form.

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U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE

INFORMATION DISCLOSURE STATEMENT BY APPLICANT

(Not for submission under 37 CFR 1.99)

Application Number	14984156
Filing Date	2015-12-30
First Named Inventor	Shatalov et al.
Art Unit	
Examiner Name	
Attorney Docket Number	SETI-0110-CIP-US

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INFORMATION DISCLOSURE STATEMENT BY APPLICANT (Not for submission under 37 CFR 1.99)		
	Application Number	14984156
	Filing Date	2015-12-30
	First Named Inventor	Shatalov et al.
	Art Unit	
	Examiner Name	
	Attorney Docket Number	SETI-0110-CIP-US

	1	2013023197	WO	A2	2013-02-14	Sensor Electronic Technology, Inc.		

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	1	SHATALOV, M. et al., "AlGaN Deep-Ultraviolet Light-Emitting Diodes with External Quantum Efficiency above 10%," Applied Physics Express, July 2012, 3 pages, Vol. 5, No. 8.	
	2	WHITE, S., Application No. 14/189,012, Attorney Docket No. SETI-0110-US, Notice of Allowance, 30 September 2015, 8 pages	
	3	WHITE, S., Application No. 14/189,012, Attorney Docket No. SETI-0110-US, Ex Parte Quayle, 24 September 2015, 17 pages	

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(81) Designated States *(unless otherwise indicated, for every kind of national protection available)*: AE, AG, AL, AM, AO, AT, AU, AZ, BA, BB, BG, BH, BN, BR, BW, BY, BZ, CA, CH, CL, CN, CO, CR, CU, CZ, DE, DK, DM, DO, DZ, EC, EE, EG, ES, FI, GB, GD, GE, GH, GM, GT, HN, HR, HU, ID, IL, IN, IS, JP, KE, KG, KM, KN, KP, KR, KZ, LA, LC, LK, LR, LS, LT, LU, LY, MA, MD, ME, MG, MK, MN, MW, MX, MY, MZ, NA, NG, NI, NO, NZ, OM, PE, PG, PH, PL, PT, QA, RO, RS, RU, RW, SC, SD, SE, SG, SK, SL, SM, ST, SV, SY, TH, TJ, TM, TN, TR, TT, TZ, UA, UG, US, UZ, VC, VN, ZA, ZM, ZW.

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Declarations under Rule 4.17:

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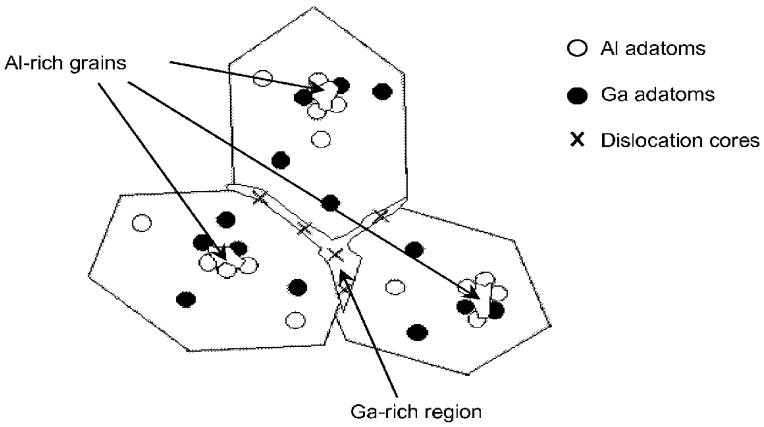
[Continued on next page]

(54) **Title**: EMITTING DEVICE WITH COMPOSITIONAL AND DOPING INHOMOGENEITIES IN SEMICONDUCTOR LAYERS

FIG. 1
Prior Art



(57) **Abstract**: A device including one or more layers with lateral regions configured to facilitate the transmission of radiation through the layer and lateral regions configured to facilitate current flow through the layer is provided. The layer can comprise a short period superlattice, which includes barriers alternating with wells. In this case, the barriers can include both transparent regions, which are configured to reduce an amount of radiation that is absorbed in the layer, and higher conductive regions, which are configured to keep the voltage drop across the layer within a desired range.

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EMITTING DEVICE WITH COMPOSITIONAL AND DOPING INHOMOGENEITIES IN SEMICONDUCTOR LAYERS

REFERENCE TO RELATED APPLICATIONS

[0001] The current application claims the benefit of co-pending U.S. Provisional Application No. 61/522,425, titled "Light Emitting Diodes with Compositional and Doping Inhomogeneities in Semiconductor Layers," which was filed on 11 August 2011 and co-pending U.S. Provisional Application No. 61/600,701, titled "Light Emitting Diodes with Compositional and Doping Inhomogeneities in Semiconductor Layers," which was filed on 19 February 2012, both of which are hereby incorporated by reference.

TECHNICAL FIELD

[0002] The disclosure relates generally to emitting devices, and more particularly, to an emitting device with improved efficiency.

BACKGROUND ART

[0003] Semiconductor emitting devices, such as light emitting diodes (LEDs) and laser diodes (LDs), include solid state emitting devices composed of group III-V semiconductors. A subset of group III-V semiconductors includes group III nitride alloys, which can include binary, ternary and quaternary alloys of indium (In), aluminum (Al), gallium (Ga), and nitrogen (N). Illustrative group III nitride based LEDs and LDs can be of the form $In_yAl_xGa_{1-x-y}N$, where x and y indicate the molar fraction of a given element, $0 \leq x, y \leq 1$, and $0 \leq x+y \leq 1$. Other illustrative group III nitride based LEDs and LDs are based on boron (B) nitride (BN) and can be of the form $Ga_zIn_yAl_xB_{1-x-y-z}N$, where $0 \leq x, y, z \leq 1$, and $0 \leq x+y+z \leq 1$.

[0004] An LED is typically composed of semiconducting layers. During operation of the LED, an applied bias across doped layers leads to injection of electrons and holes into an active layer where electron-hole recombination leads to light generation. Light is generated with uniform angular distribution and escapes the LED die by traversing semiconductor layers in all directions. Each semiconducting layer has a particular combination of molar fractions (e.g., x, y, and z) for the various elements, which influences the electronic and optical properties of the layer. In particular, the refractive

index and absorption characteristics of a layer are sensitive to the molar fractions of the semiconductor alloy. Variation of the molar fraction throughout a layer results in variation in the index of refraction and the band gap energy of the layer.

[0005] Ultraviolet LEDs are typically grown using group III-V semiconductor layers such as layers of $Al_xGa_{1-x}N$. It was found that the material properties of $Al_xGa_{1-x}N$ alloys change as the amount of aluminum in the alloy is increased. With proper growth conditions, it also was found that the aluminum did not incorporate uniformly throughout the AlGaN layer (i.e., the material has areas of high and low concentrations of aluminum spread throughout). These compositional fluctuations, together with doping fluctuations, also known as localized inhomogeneities, result in carrier localization and lead to the creation of conduction layers for carriers.

[0006] The effect of compositional fluctuations have been well studied for blue LEDs with pioneering work of S. Chichibu, T. Azuhata, T. Sota and S. Nakamura, Applied Physics Letters. 1997 May 1, 70, 2822; S. Chichibu, K. Wada, and S. Nakamura, Applied Physics Letters, vol. 71, pp. 2346-2348, Oct. 1997, each of which is incorporated herein by reference in its entirety. The localization effect resulting from the creation of localized inhomogeneities has natural occurrence for InAlGaN alloys attributed to indium segregation. These effects have been reported in works of E. Monroy, N. Gogneau, F. Enjalbert, F. Fossard, D. Jalabert, E. Bellet-Amalric, Le Si Dang, and B. Daudin, J. Appl. Phys. 94, 3121 (2003); Mee-Yi Ryu, C. Q. Chen, E. Kuokstis, J. W. Yang, G. Simin, and M. Asif Khan, Appl. Phys. Lett. 80, 3730 (2002); H. Hirayama, A. Kinoshita, T. Yamabi, Y. Enomoto, A. Hirata, T. Araki, Y. Nanishi, and Y. Aoyagi, Appl. Phys. Lett. 80, 207 (2002); C. H. Chen, Y. F. Chen, Z. H. Lan, L. C. Chen, K. H. Chen, H. X. Jiang, and J. Y. Lin, Appl. Phys. Lett. 84, 1480 (2004), each of which is incorporated herein by reference in its entirety. Further, small additions of indium were shown to smooth out the band-bottom potential profile in AlInGaN layers owing to improved crystal quality. The effect of incorporation of 1% of indium to AlGaN semiconductor layer also has been studied. Similar to other studies, the creation of compositional inhomogeneities in a semiconductor layer with distinct double-scaled potential profile was observed, which indicates that indium atoms produce clusters of uniform consistency interspersed in AlGaN background semiconductor alloy.

[0007] During the growth process of AlGaN semiconductor layers, small islands with high aluminum content are formed. See A. Pinos, V. Liuolia, S. Marcinkevičius, J.

Yang, R. Gaska, and M. S. Shur, Journal of Applied Physics, vol. 109, no. 11, p. 113516, 2011), which is incorporated herein by reference in its entirety. Grains with high aluminum content are separated by domain boundaries containing extended defects, which are formed in order to accommodate the relative difference in crystal orientation among the islands. These defects have high gallium content.

[0008] Details of compositional fluctuation in AlGaN semiconductors have been studied by photoluminescence (PL) measured using scanning near field optical microscopy (SNOM). Using this technique, the band gap fluctuations were observed to be of order of 50 meV. The fluctuations increase with higher aluminum content. For samples with low aluminum content (less than 0.4 molar fraction), the small-scale fluctuations occur within larger domains and are believed to be due to an inhomogeneous stress field and dislocations. For the aluminum molar fraction of 0.42 and higher, the small-scale potential variations were observed over the whole sample and assigned to the formation of Al-rich grains during the growth. Larger area potential variations of 25–40 meV, most clearly observed in the layers with a lower AlN molar fraction, have been attributed to Ga-rich regions close to grain boundaries or atomic layer steps. Analysis of the PL spectra allows evaluating average potential fluctuations due to inhomogeneous growth of AlGaN layers. Some findings suggest that there are two spatial scales of potential fluctuation – large scale of order of 1 μm and small scale that is less than 100 nm. Potential fluctuations reach amplitudes of few tens of meV at each scale.

[0009] FIG. 1 shows a schematic of compositional fluctuation according to the prior art. During the initial growth stage, adjacent small islands, from which the growth starts, coalesce into larger grains. As the islands enlarge, Ga adatoms, having a larger lateral mobility than Al adatoms, reach the island boundaries more rapidly, thus the Ga concentration in the coalescence regions is higher than in the center of the islands. The composition pattern, which is formed during the coalescence, is maintained as the growth proceeds vertically. As a result of the coalescence, the domain boundaries usually contain extended defects that form to accommodate the relative difference in crystal orientation among the islands. Even in layers with smooth surfaces containing elongated layer steps, screw/mixed dislocations occur due to the local compositional inhomogeneities.

[0010] High magnesium doping can lead to the creation of mini-bands originating from the discrete acceptor levels. A red shift in room temperature photoluminescence spectra has been observed giving an indication that miniband levels are emerging for acceptor concentration levels of the order of $n=10^{19}$-10^{20} ($1/cm^3$). In high acceptor concentration domains, hole wavefunctions may overlap thus forming hole conduction pathways through the material. These pathways lead to an increase of conductivity through semiconductor layers.

SUMMARY OF THE INVENTION

[0011] In light of the above, the inventors recognize that compositional and/or doping inhomogeneities allow for the development of conduction channels, e.g., in p-type superlattice layers. At the same time, the regions high in aluminum content allow for low light absorption (e.g., a higher transmission coefficient). The inventors propose to achieve a desired balance of higher conduction with reduced light absorption by tailoring semiconductor properties through the use of composite inhomogeneities, thereby obtaining a more optimal semiconductor material for light emitting/transmission applications.

[0012] Aspects of the invention provide a device including one or more layers with lateral regions configured to facilitate the transmission of radiation through the layer and lateral regions configured to facilitate current flow through the layer. The layer can comprise a short period superlattice, which includes barriers alternating with wells. In this case, the barriers can include both transparent regions, which are configured to reduce an amount of radiation that is absorbed in the layer, and higher conductive regions, which are configured to keep the voltage drop across the layer within a desired range.

[0013] A first aspect of the invention provides a device comprising: a short period superlattice (SPSL) semiconductor layer comprising a plurality of barriers, wherein a composition of at least one barrier varies along the lateral dimensions of the at least one barrier such that a lateral cross section of the at least one barrier includes: a set of transparent regions, each transparent region having a transmission coefficient for a target radiation wavelength, l, greater than or equal to approximately sixty percent, wherein the set of transparent regions are at least ten percent of an area of the lateral cross section of the at least one barrier; and a set of higher conductive regions

occupying a sufficient area of the area of the lateral cross section of the at least one barrier and having an average resistance per unit area to a vertical current flow resulting in a total voltage drop across the SPSL of less than approximately five volts.

[0014] A second aspect of the invention provides a device comprising: a short period superlattice (SPSL) semiconductor layer comprising a plurality of barriers, wherein a lateral cross section of each barrier includes: a set of transparent regions, each transparent region having a transmission coefficient for a target radiation wavelength, l, greater than or equal to approximately sixty percent, wherein the set of transparent regions are at least ten percent of an area of the lateral cross section of the barrier; and a set of higher conductive regions occupying a sufficient area of the area of the lateral cross section of the barrier and having an average resistance per unit area to a vertical current flow resulting in a total voltage drop across the SPSL of less than approximately five volts.

[0015] A third aspect of the invention provides a method of fabricating a device comprising: forming a short period superlattice (SPSL) semiconductor layer comprising a plurality of barriers, wherein a lateral cross section of each barrier includes: a set of transparent regions, each transparent region having a transmission coefficient for a target radiation wavelength, l, greater than or equal to approximately sixty percent, wherein the set of transparent regions are at least ten percent of an area of the lateral cross section of the barrier; and a set of higher conductive regions occupying a sufficient area of the area of the lateral cross section of the barrier and having an average resistance per unit area to a vertical current flow resulting in a total voltage drop across the SPSL of less than approximately five volts.

[0016] The illustrative aspects of the invention are designed to solve one or more of the problems herein described and/or one or more other problems not discussed.

BRIEF DESCRIPTION OF THE DRAWINGS

[0017] These and other features of the disclosure will be more readily understood from the following detailed description of the various aspects of the invention taken in conjunction with the accompanying drawings that depict various aspects of the invention.

[0018] FIG. 1 shows a schematic of compositional fluctuation according to the prior art.

[0019] FIG. 2 shows a schematic structure of an illustrative emitting device according to an embodiment.

[0020] FIGS. 3A and 3B show illustrative schematic representations of a p-type layer formed using a p-type superlattice according to an embodiment.

[0021] FIG. 4 shows an illustrative band variation for a p-type superlattice according to an embodiment.

[0022] FIG. 5 shows a schematic representation of an illustrative carrier path in a complicated energy landscape caused by the inhomogeneities according to an embodiment.

[0023] FIG. 6 shows illustrative maps corresponding to an $Al_{50}Ga_{50}N$ layer.

[0024] FIG. 7 shows the effect of the absorption coefficient of a p-type superlattice layer on the total extracted light from an illustrative light emitting diode structure according to an embodiment.

[0025] FIG. 8 shows a numerical fit to the ray tracing data shown in FIG. 7 according to an embodiment.

[0026] FIG. 9 shows a plot of the wall plug efficiency as a function of the conductance area fraction for typical light emitting diode materials according to an embodiment.

[0027] FIG. 10 shows a typical dependence of the absorption coefficient on the wavelength for various aluminum molar fractions in a $Al_xGa_{1-x}N$ alloy according to an embodiment.

[0028] FIG. 11 shows how the content of the aluminum can be chosen for each emitted wavelength according to an embodiment.

[0029] FIG. 12 shows an illustrative flow diagram for fabricating a circuit according to an embodiment.

[0030] It is noted that the drawings may not be to scale. The drawings are intended to depict only typical aspects of the invention, and therefore should not be considered as limiting the scope of the invention. In the drawings, like numbering represents like elements between the drawings.

DETAILED DESCRIPTION OF THE INVENTION

[0031] As indicated above, aspects of the invention provide a device including one or more layers with lateral regions configured to facilitate the transmission of radiation

through the layer and lateral regions configured to facilitate current flow through the layer. The layer can comprise a short period superlattice, which includes barriers alternating with wells. In this case, the barriers can include both transparent regions, which are configured to reduce an amount of radiation that is absorbed in the layer, and higher conductive regions, which are configured to keep the voltage drop across the layer within a desired range. As used herein, unless otherwise noted, the term "set" means one or more (i.e., at least one) and the phrase "any solution" means any now known or later developed solution.

[0032] Turning to the drawings, FIG. 2 shows a schematic structure of an illustrative emitting device 10 according to an embodiment. In a more particular embodiment, the emitting device 10 is configured to operate as a light emitting diode (LED), such as a conventional or super luminescent LED. Alternatively, the emitting device 10 can be configured to operate as a laser diode (LD). In either case, during operation of the emitting device 10, application of a bias comparable to the band gap results in the emission of electromagnetic radiation from an active region 18 of the emitting device 10. The electromagnetic radiation emitted by the emitting device 10 can comprise a peak wavelength within any range of wavelengths, including visible light, ultraviolet radiation, deep ultraviolet radiation, infrared light, and/or the like. In an embodiment, the device is configured to emit radiation having a dominant wavelength within the ultraviolet range of wavelengths. In a more specific embodiment, the dominant wavelength is within a range of wavelengths between approximately 210 and approximately 350 nanometers.

[0033] The emitting device 10 includes a heterostructure comprising a substrate 12, a buffer layer 14 adjacent to the substrate 12, an n-type cladding layer 16 (e.g., an electron supply layer) adjacent to the buffer layer 14, and an active region 18 having an n-type side 19A adjacent to the n-type cladding layer 16. Furthermore, the heterostructure of the emitting device 10 includes a p-type layer 20 (e.g., an electron blocking layer) adjacent to a p-type side 19B of the active region 18 and a p-type cladding layer 22 (e.g., a hole supply layer) adjacent to the p-type layer 20.

[0034] In a more particular illustrative embodiment, the emitting device 10 is a group III-V materials based device, in which some or all of the various layers are formed of elements selected from the group III-V materials system. In a still more particular illustrative embodiment, the various layers of the emitting device 10 are formed of

group III nitride based materials. Group III nitride materials comprise one or more group III elements (e.g., boron (B), aluminum (Al), gallium (Ga), and indium (In)) and nitrogen (N), such that $B_WAl_XGa_YIn_ZN$, where $0 \leq W, X, Y, Z \leq 1$, and $W+X+Y+Z = 1$. Illustrative group III nitride materials include binary, ternary and quaternary alloys such as, AlN, GaN, InN, BN, AlGaN, AlInN, AlBN, AlGaInN, AlGaBN, AlInBN, and AlGaInBN with any molar fraction of group III elements.

[0035] An illustrative embodiment of a group III nitride based emitting device 10 includes an active region 18 (e.g., a series of alternating quantum wells and barriers) composed of $In_yAl_xGa_{1-x-y}N$, $Ga_zIn_yAl_xB_{1-x-y-z}N$, an $Al_xGa_{1-x}N$ semiconductor alloy, or the like. Similarly, both the n-type cladding layer 16 and the p-type layer 20 can be composed of an $In_yAl_xGa_{1-x-y}N$ alloy, a $Ga_zIn_yAl_xB_{1-x-y-z}N$ alloy, or the like. The molar fractions given by *x*, *y*, and *z* can vary between the various layers 16, 18, and 20. The substrate 12 can be sapphire, silicon carbide (SiC), silicon (Si), GaN, AlGaN, AlON, $LiGaO_2$, or another suitable material, and the buffer layer 14 can be composed of AlN, an AlGaN/AlN superlattice, and/or the like.

[0036] As shown with respect to the emitting device 10, a p-type metal 24 can be attached to the p-type cladding layer 22 and a p-type contact 26 can be attached to the p-type metal 24. Similarly, an n-type metal 28 can be attached to the n-type cladding layer 16 and an n-type contact 30 can be attached to the n-type metal 28. The p-type metal 24 and the n-type metal 28 can form ohmic contacts to the corresponding layers 22, 16, respectively. In an embodiment, the p-type metal 24 and the n-type metal 28 each comprise several conductive and reflective metal layers, while the n-type contact 30 and the p-type contact 26 each comprise highly conductive metal. In an embodiment, the p-type cladding layer 22 and/or the p-type contact 26 can be at least partially transparent (e.g., semi-transparent or transparent) to the electromagnetic radiation generated by the active region 18. For example, the p-type cladding layer 22 and/or the p-type contact 26 can comprise a short period superlattice lattice structure, such as an at least partially transparent magnesium (Mg)-doped AlGaN/AlGaN short period superlattice structure (SPSL). Furthermore, the p-type contact 26 and/or the n-type contact 30 can be at least partially reflective of the electromagnetic radiation generated by the active region 18. In another embodiment, the n-type cladding layer 16 and/or the n-type contact 30 can be formed

of a short period superlattice, such as an AlGaN SPSL, which is at least partially transparent to the electromagnetic radiation generated by the active region 18.

[0037] As used herein, a layer is at least partially transparent when the layer allows at least a portion of electromagnetic radiation in a corresponding range of radiation wavelengths to pass there through. For example, a layer can be configured to be at least partially transparent to a range of radiation wavelengths corresponding to a peak emission wavelength for the light (such as ultraviolet light or deep ultraviolet light) emitted by the active region 18 (e.g., peak emission wavelength +/- five nanometers). As used herein, a layer is at least partially transparent to radiation if it allows more than approximately 0.5 percent of the radiation to pass there through. In a more particular embodiment, an at least partially transparent layer is configured to allow more than approximately five percent of the radiation to pass there through. Similarly, a layer is at least partially reflective when the layer reflects at least a portion of the relevant electromagnetic radiation (e.g., light having wavelengths close to the peak emission of the active region). In an embodiment, an at least partially reflective layer is configured to reflect at least approximately five percent of the radiation.

[0038] As further shown with respect to the emitting device 10, the device 10 can be mounted to a submount 36 via the contacts 26, 30. In this case, the substrate 12 is located on the top of the emitting device 10. To this extent, the p-type contact 26 and the n-type contact 30 can both be attached to a submount 36 via contact pads 32, 34, respectively. The submount 36 can be formed of aluminum nitride (AlN), silicon carbide (SiC), and/or the like.

[0039] Any of the various layers of the emitting device 10 can comprise a substantially uniform composition or a graded composition. For example, a layer can comprise a graded composition at a heterointerface with another layer. In an embodiment, the p-type layer 20 comprises a p-type blocking layer having a graded composition. The graded composition(s) can be included to, for example, reduce stress, improve carrier injection, and/or the like. Similarly, a layer can comprise a superlattice including a plurality of periods, which can be configured to reduce stress, and/or the like. In this case, the composition and/or width of each period can vary periodically or aperiodically from period to period.

[0040] It is understood that the layer configuration of the emitting device 10 described herein is only illustrative. To this extent, an emitting device/heterostructure

can include an alternative layer configuration, one or more additional layers, and/or the like. As a result, while the various layers are shown immediately adjacent to one another (e.g., contacting one another), it is understood that one or more intermediate layers can be present in an emitting device/heterostructure. For example, an illustrative emitting device/heterostructure can include an undoped layer between the active region 18 and one or both of the p-type cladding layer 22 and the electron supply layer 16.

[0041] Furthermore, an emitting device/heterostructure can include a Distributive Bragg Reflector (DBR) structure, which can be configured to reflect light of particular wavelength(s), such as those emitted by the active region 18, thereby enhancing the output power of the device/heterostructure. For example, the DBR structure can be located between the p-type cladding layer 22 and the active region 18. Similarly, a device/heterostructure can include a p-type layer located between the p-type cladding layer 22 and the active region 18. The DBR structure and/or the p-type layer can comprise any composition based on a desired wavelength of the light generated by the device/heterostructure. In one embodiment, the DBR structure comprises a Mg, Mn, Be, or Mg+Si-doped p-type composition. The p-type layer can comprise a p-type AlGaN, AlInGaN, and/or the like. It is understood that a device/heterostructure can include both the DBR structure and the p-type layer (which can be located between the DBR structure and the p-type cladding layer 22) or can include only one of the DBR structure or the p-type layer. In an embodiment, the p-type layer can be included in the device/heterostructure in place of an electron blocking layer. In another embodiment, the p-type layer can be included between the p-type cladding layer 22 and the electron blocking layer.

[0042] Regardless, as described herein, one or more of the semiconductor layers of the device 10 can comprise nano-scale and/or micron-scale localized compositional and/or doping inhomogeneities along the lateral dimensions of the device die. For example, a semiconductor layer can be p-doped with magnesium or n-doped with silicon to create the inhomogeneities. These inhomogeneities provide variation of band gap energy in a lateral direction of the layer, which results in a complicated energy landscape for a lateral cross section of the layer. In particular, the inhomogeneities will result in lower band gap regions, which become places of charge localization and form a set of higher conductive regions of carrier conductive channels

in the semiconductor layer. These higher conductive regions have an improved vertical conductivity over that of a substantially homogenous layer of the material. Additionally, the inhomogeneities also will result in high band gap regions, which form a set of at least partially transparent regions within the layer, each of which has an improved vertical transparency over that of a substantially homogenous layer of the material.

[0043] Inclusion of the inhomogeneities in one or more of the semiconductor layers of the device 10 can result in an improvement in the efficiency of the device 10. The inhomogeneities can be included in any layer of the semiconductor device 10. To this extent, the inhomogeneities can be included in a superlattice region, a nucleation region, a buffer layer, a cladding layer, an active region, and/or the like of the device 10. In an embodiment, the inhomogeneities are incorporated into one or more injection layers, such as the n-type cladding layer 16, the p-type layer 20, the p-type cladding layer 22, the n-type contact 30, the p-type contact 26, and/or the like.

[0044] In an illustrative embodiment described further herein, the inhomogeneities are incorporated into a layer formed using a p-type superlattice, such as the p-type cladding layer 22. For example, the p-type cladding layer 22 can comprise a periodic structure composed of a set of barriers alternating with a set of wells. In a more specific embodiment, the sets of barriers and wells are each formed of a group III nitride material where each barrier comprises a higher aluminum content (molar fraction) than the adjacent well(s). In a still more specific embodiment, each barrier and well in the periodic structure can have a thickness less than approximately three nanometers. The p-type cladding layer 22 can be modulation p-doped with magnesium to incorporate the inhomogeneities. In an embodiment, the doping is such that a concentration of magnesium in the barrier regions is higher than $5 \cdot 10^{18}$ [$1/cm^3$] and a concentration of magnesium in the well regions is lower than $5 \cdot 10^{15}$ [$1/cm^3$].

[0045] FIGS. 3A and 3B show illustrative schematic representations of the p-type cladding layer 22 formed using a p-type superlattice according to an embodiment. The p-type cladding layer 22 is shown adjacent to the p-type metal 24. In FIGS. 3A and 3B, areas with a high aluminum composition are indicated by the dark regions, while areas with a low aluminum composition are indicated by the lighter/bright regions. To this extent, FIG. 3A illustrates variation in aluminum composition within

the layer 22 along the height of the layer (e.g., indicated by direction z) in a direction normal to a surface of the layer 22 adjacent to the p-type metal 24. In particular, the p-type cladding layer 22 can be formed of a p-type $Al_xGa_{1-x}N/Al_yGa_{1-y}N$ superlattice, where molar fractions x and y correspond to the molar fractions of barriers and wells, respectively, and where the molar fraction x is greater than the molar fraction y. Each barrier and well can be approximately a few nanometers in thickness. For example, the wells can have a thickness in a range between approximately one and approximately six nanometers, and the barriers can have a thickness in a range between approximately five and approximately twenty nanometers.

[0046] FIG. 3B illustrates variation in the aluminum composition of the p-type cladding layer 22 in the lateral directions (e.g., indicated by directions x and y) of the layer 22. FIG. 3B can correspond to a lateral cross section of the layer 22 taken along a barrier of the layer 22. As used herein, the term lateral means the plane of the layer 22 that is substantially parallel with the surface of the layer 22 adjacent to another layer of the device 10 (FIG. 2), such as the surface of the layer 22 adjacent to the p-type metal 24. As illustrated, the lateral cross section of the layer 22 includes a set of transparent regions, which correspond to those regions having a relatively high aluminum content, and a set of higher conductive regions, which correspond to those regions having a relatively low aluminum content.

[0047] The set of transparent regions can be configured to allow a significant amount of the radiation to pass through the layer 22, while the set of higher conductive regions can be configured to keep the voltage drop across the layer 22 within a desired range (e.g., less than five volts). In an embodiment, the set of transparent regions occupy at least ten percent of the lateral area of the layer 22, while the set of higher conductive regions occupy at least approximately two percent (five percent in a more specific embodiment) of the lateral area of the layer 22. Furthermore, in an embodiment, a band gap of the higher conductive regions is at least five percent smaller than the band gap of the transparent regions. In a more particular embodiment, the transparent regions comprise a transmission coefficient for radiation of a target wavelength higher than approximately sixty percent (eighty percent in a still more particular embodiment), while the higher conductive regions have a resistance per unit area to vertical current flow that is smaller than approximately 10^{-2} ohm·cm^2. As used herein, the term transmission coefficient means

the ratio of an amount of radiation exiting of the region to an amount of radiation entering the region.

[0048] The transparent and conductive regions can be formed using any solution. For example, the layer 22 can be grown using migration-enhanced metalorganic chemical vapor deposition (MEMOCVD). During the growth, inhomogeneities in the lateral direction of a molar fraction of one or more elements, such as aluminum, gallium, indium, boron, and/or the like, can be allowed of the layer 22. In an embodiment, such compositional inhomogeneities can vary by at least one percent.

[0049] Furthermore, the layer 22 can have a non-uniform distribution of a thickness of one or more of the barriers in the SPSL. The non-uniform distribution can be configured to create the transparent regions and the higher conductive regions. In an embodiment, the non-uniform distribution is accomplished by growing a film under a facetted or three-dimensional growth mode. This growth mode is achieved while growing under conditions where the growth rate of the film is determined by the arrival rate of active nitrogen (N-limited). Furthermore, this growth mode is achieved by growing under nearly stoichiometric conditions where the ratio of the arrival rate of group-III atoms (Al, Ga) and the arrival rate of active nitrogen is about unity. Moreover, the nanometer scale compositional inhomogeneities are self-assembled within the film as a result of such a growth mode.

[0050] In an embodiment, an illustrative process can be implemented to provide a growth mode for producing an $Al_xGa_{1-x}N$ alloy film, which can be utilized as a p-type layer in an emitting device. Such a growth mode can be defined by substrate temperature, a ratio of the group V/group III elements, doping concentration, and/or the like. For example, the substrate temperature can be between approximately 750 and approximately 1300 degrees Celsius. Additionally, an inhomogeneous distribution of aluminum can be obtained by controlling a density of screw dislocations present in the material. The density of the screw dislocations can be controlled, for example, by alternating the group V/group III element ratio in the SPSL layers. The group V/group III element ratio can be in a range of ratios between approximately 20 and approximately 10000.

[0051] Still further, the growth of the layer 22 can allow a non-uniform compositional distribution along the barrier height and/or barrier thickness. Even further, when the layer 22 is doped, the growth of the layer 22 can allow a non-uniform doping

distribution along the barrier height and/or barrier thickness. For example, modulation doping of the layer 22 can be utilized to create a variation of acceptor concentration within the layer that exceeds approximately $1x10^{18}$ $1/cm^3$.

[0052] In an embodiment, an SPSL layer described herein can be formed directly on an inhomogeneous layer (e.g., p-type layer 20 shown in FIG. 2), which can promote the SPSL semiconductor layer (e.g., layer 22 shown in FIG. 2) to form the transparent and conductive regions. The inhomogeneous layer can be grown in a similar manner as the SPSL semiconductor layer and also include transparent and conductive regions as described herein. However, the growth temperature of the inhomogeneous layer can be at least approximately two hundred degrees Celsius lower than the growth temperature used for growing the SPSL semiconductor layer. Furthermore, a thickness of the inhomogeneous layer can be less than approximately 20 nanometers. In an embodiment, the growth of the inhomogeneous layer can include: enabling the three dimensional (e.g., side and upward) coalescence of islands (e.g., of Al), which are grown at a temperature approximately two hundred degrees Celsius lower than the temperature used for growing the SPSL semiconductor layer; followed by two dimensional growth of the inhomogeneous layer around the islands using distinctly different growth conditions than during the formation of the islands. For example, the two dimensional growth can be at a temperature and/or a group V/group III element ratio comparable to that used for growing the SPSL semiconductor layer. The growth of islands followed by two dimensional growth can be repeated one or more times to form the inhomogeneous layer. While use of MEMOCVD is described herein, it is understood that growth of one or more of the layers can utilize another growth solution, such as metallo organic chemical vapor deposition (MOCVD), molecular beam epitaxy (MBE, as utilized in US Patent No. 7,812,366), and/or the like.

[0053] FIG. 4 shows an illustrative band variation for a p-type superlattice, such as the layer 22 shown in FIGS. 3A and 3B, according to an embodiment. Built in polarization fields result in the skewed band levels. The skewed band levels lead to the localization of carriers. For cases when doping is relatively small in the superlattice quantum wells, but relatively high in the barriers, acceptor ionization in the barriers is possible and can result in a large concentration of holes in the quantum wells, which leads to the formation of a two-dimensional carrier gas illustrated by the grey “clouded” regions of FIG. 4. In an embodiment, the quantum wells have a

concentration less than $5 \cdot 10^{17}$ [1/cm^3] (e.g., a concentration less than $5 \cdot 10^{15}$ [1/cm^3]), while the barriers have a concentration greater than $5 \cdot 10^{17}$ [1/cm^3] (e.g., a concentration higher than $5 \cdot 10^{18}$ [1/cm^3]).

[0054] The carrier path through the layer 22 (FIGS. 3A and 3B) is composed of a diffusive lateral component due to the high mobility of carriers in the lateral direction, barrier tunneling, and/or penetration through conducting channels in a direction normal to the semiconductor layer 22. FIG. 5 shows a schematic representation of an illustrative carrier path in a complicated energy landscape caused by the inhomogeneities according to an embodiment. As illustrated, the carrier path runs through the low energy valleys (e.g., higher conductivity regions) of the energy landscape (indicated by dark regions), and propagates through regions containing a high concentration of dopants. In these valleys and regions, the electrons and holes experience smaller energy barriers, which they can penetrate through using the low energy valleys. In an embodiment, a characteristic distance between the higher conducting regions is less than a lateral current spreading length within the layer. For example, the lateral current spreading length can be 0.1 μm or larger.

[0055] FIG. 6 shows illustrative maps corresponding to an $Al_{50}Ga_{50}N$ layer. In particular, FIG. 6 includes: a) a near-field photoluminescence map of the peak intensity; b) a near-field photoluminescence map of the peak energy; d) a near-field photoluminescence map of the full width at half maximum (FWHM); c) a map of near-field and far-field spectra; e) a map of intensity correlation; and f) a map of FWHM correlation. As illustrated, the emission is non-uniform throughout the active layer structure and includes high intensity red shifted regions, which are correlated to islands containing lower aluminum content than the surrounding area.

[0056] A theoretical basis for the devices described herein is included for clarity. However, it is understood that the invention is not limited to the inventor's current understanding of the benefits described herein or the basis for such benefits.

[0057] The overall wall plug efficiency of a light emitting device, such as device 10 (FIG. 2), is related to tradeoffs associated with the conductivity and the transparent characteristics of the semiconductor layers. In particular, the p-type cladding layer(s) can have a low conductivity and highest absorption coefficient compared to all other layers in a deep ultraviolet LED. Consider the total resistance of the device 10 as a sum of a resistance due to p-type cladding layer(s) (R_p) and a resistance due to all

other components of the device 10, such as the resistances of the active region 18, n-type cladding layer 16, the contact resistances, and/or the like (R_r). The total voltage (V_T) across the device 10 is given by:

$$V_T = V_{on} + I(R_r + R_p)$$

With V_{on} being a turn on voltage and I being the current. The total power dissipated (P_{dis}) on a device 10 is:

$$P_{dis} = IV_T = I^2(R_p + R_r) + IV_{on}$$

[0058] A device 10, such as a light emitting diode, described herein can operate at a set current I. Furthermore, assume that R_r is fixed and known. The resistivity of a p-type contact layer, R_p, can be written as:

$$\frac{1}{R_p} = \frac{1}{R_1} + \frac{1}{R_2}$$

Here, R_1 is a portion of the p-type superlattice (PSL) 22 (FIGS. 3A and 3B) with a relatively low resistance and a relatively low transparency, while R_2 is a part of the PSL lattice with a relatively high resistance and a relatively high transparency. For cases when $R_1 \ll R_2$, it is sufficient to approximate $R_p \sim R_1$. This simple model assumes that most of the conduction in the p-type superlattice 22 happens through channels, which are connected domains with a lower concentration of aluminum and a higher concentration of dopants. Regions of the PSL 22 with a low resistance can be described by their characteristic resistivity ρ_1, as well as the gross cross sectional area that corresponds to these regions (further denoted as A_1); thus:

$$R_1 = \rho_1 L_{PSL}/A_1.$$

Here L_{PSL} denotes the corresponding length of the layer. Using $f = A_1/A$, where A is a total area of a device, then:

$$R_1 = [(\rho_1 L_{PSL})/A]\ (1/f) = R_0/f.$$

As a simple approximation, the resistance R_0 can be taken to be the resistance of a p-type contact layer composed of bulk GaN semiconductor material.

[0059] FIG. 7 shows the effect of the absorption coefficient of the PSL layer 22 on the total extracted light from an illustrative light emitting diode structure according to an embodiment. The effect is shown in the context of a deep ultraviolet LED, and was obtained through ray tracing simulations. As illustrated, the total radiative power of the LED depends roughly linearly on $\log_{10}(\alpha/\alpha_0)$, with α_0 being a normalization

parameter. FIG. 8 shows a numerical fit to the ray tracing data according to an embodiment. Radiative power is then written as:

$$P_{out} = A - B\log_{10}(\alpha/\alpha_0)$$

where A, and B are fitting constants.

[0060] The transmittance of a layer is related to the absorption coefficient and the p-type cladding layer as:

$$T = T_0\exp(-\alpha L_{PSL})$$

If a part of the area of a p-type cladding layer is not substantially transparent but is more conductive (this area is A_1), then the total transmission is given by (under an assumption of a uniform light flux per unit area):

$$T_{tot} = T\left(1 - \frac{A_1}{A}\right) = T(1-f) = T_0\exp\left(-\alpha' L_{PSL}\right)$$

Here α' is a modification of the absorption coefficient due to area A_1 not being transparent. From this it follows that:

$$\exp(-\alpha L_{PSL})\,(1-f) = \exp\left(-\alpha' L_{PSL}\right) \text{ or } \alpha' = \alpha - \log(1-f)/L_{PSL}$$

Using the expression for P_{out}, with $\alpha' = \alpha'(f;\alpha)$: $P_{out} = A - B\log_{10}(\alpha'/\alpha_0)$ and we can calculate the wall plug efficiency as:

$$WPE(f) = P_{out}(f)/P_{dis}(f).$$

[0061] Wall plug efficiency can have a maximum for a particular value of f and can depend on the resistivity of the device, a thickness of the PSL, and the absorption coefficient α. FIG. 9 shows a plot of the WPE as a function of the conductance area fraction, *f*, for typical LED materials according to an embodiment. As illustrated, a peak wall plug efficiency is obtained at a value of the conductance area fraction *f* between approximately 0.3 and 0.6. In an embodiment, a total area of the set of transparent regions in a lateral cross section of the PSL is at least ten percent (*f* = 0.1) of the total area of the lateral cross section. In a more particular embodiment, the total area of the set of transparent regions is between approximately thirty and sixty percent of the total area of the lateral cross section.

[0062] It is important to observe that the average distance between inhomogeneities should be on the order of current spreading length in order for the device to have uniform current/light emission throughout the semiconducting layers. Current spreading length in one period of a PSL is given by:

$$L_{spread} = \sqrt{\frac{lkT}{q\rho J_0}},$$

where l is the thickness of a period layer, ρ is the resistivity of a current spreading layer, and J_0 is a current density. Using this formula, the current spreading length is estimated to be between approximately 0.1 μm and approximately 1 μm.

[0063] As discussed herein, the set of higher conductive regions can be configured to keep the voltage drop across the layer within a desired range. In an embodiment, a target resistance per area for the layer can be calculated based on attributes of the layer and attributes of the operating environment for the device. For example, an illustrative device configuration can include a layer that is 200 nanometers thick and has a lateral cross sectional area of 200 micrometers by 200 micrometers, a target voltage drop of one Volt across the layer, and an operating current of 0.02 Amperes. In this case, a target total resistance of the layer can be calculated as 1 Volt/0.02 Amps = 50 Ohms, and a target resistivity of the layer can be calculated as:

$$50 \text{ Ohms} \times 4\times10^{-8}/(2\times10^{-7}) = 10 \text{ Ohm·m}.$$

Using a target resistivity of 1000 Ohm*cm, a target resistance per area of a 200 nanometer thick layer can be calculated as:

$$1000 \text{ Ohm·cm} \times 2\times10^{-5} \text{ cm} = 2\times10^{-2} \text{ Ohm·cm}^2.$$

[0064] The transparency of a short period superlattice (SPSL) can be calculated by either averaging the optical absorption and refraction coefficients of the SPSL or computing absorption and reflection coefficients numerically using Maxwell equations. The absorption coefficients, α, depend on the absorption edge of the semiconductor material which is a function of the molar fractions x, y, and z of a $Ga_zIn_yAl_xB_{1-x-y-z}N$ semiconductor alloy for a group III nitride semiconductor material. FIG. 10 shows a typical dependence of the absorption coefficient on the wavelength for various aluminum molar fractions in a $Al_xGa_{1-x}N$ alloy according to an embodiment. In order to maintain a target absorption coefficient of a p-type layer at orders of 10^4 inverse centimeters, the content of aluminum in the SPSL barriers can be carefully chosen for each emitted wavelength. FIG. 11 shows how the content of the aluminum can be chosen for each emitted wavelength according to an embodiment. Note that the dependence of $x = x(\lambda)$ is linear, with

$$x = -0.0048\lambda + 1.83.$$

To this extent, x can provide a threshold value for a molar fraction of aluminum, which can be selected to be approximately equal to or exceed the threshold value.

[0065] It is understood that aspects of the invention can be incorporated into various types of structures/devices, solutions for designing the various types of structures/devices, and/or solutions for fabricating the various types of structures/devices.

[0066] For example, an embodiment of the invention can be implemented as part of a solution for designing and/or fabricating a structure and/or a resulting device/structure as described in U.S. Patent Application No. 12/987,102, titled "Superlattice Structure," which was filed on 8 January 2011, and which claims the benefit of U.S. Provisional Application No. 61/293,614, titled "Superlattice Structures and Devices," which was filed on 8 January 2010, both of which are hereby incorporated by reference. Similarly, an embodiment of the invention can be implemented as part of a solution for designing and/or fabricating a structure and/or a resulting device/structure as described in U.S. Patent Application No. 13/162,895, titled "Superlattice Structure," which was filed on 17 June 2011, which is hereby incorporated by reference. In either case, the structure/device can comprise a superlattice layer including a plurality of periods, each of which is formed from a plurality of sub-layers. Each sub-layer comprises a different composition than the adjacent sub-layer(s) and comprises a polarization that is opposite a polarization of the adjacent sub-layer(s). Furthermore, one or more of the sub-layers can comprise lateral region(s) configured to facilitate the transmission of radiation, such as ultraviolet radiation, through the layer and lateral region(s) configured to facilitate current flow through the sub-layer as described herein.

[0067] Furthermore, an embodiment of the invention can be implemented as part of a solution for designing and/or fabricating a structure and/or a resulting device/structure as described in U.S. Patent Application No. 12/960,476, titled "Semiconductor Material Doping," which was filed on 4 December 2010, and which claims the benefit of U.S. Provisional Application No. 61/266,523, titled "Method of Doping and Semiconductor Devices," which was filed on 4 December 2009, both of which are hereby incorporated by reference. Similarly, an embodiment of the invention can be implemented as part of a solution for designing and/or fabricating a structure and/or a resulting device/structure as described in U.S. Patent Application

No. 13/162,908, titled “Semiconductor Material Doping,” which was filed on 17 June 2011, which is hereby incorporated by reference. In either case, the structure/device can comprise a superlattice structure as described herein, in which a target band discontinuity between a quantum well and an adjacent barrier is selected to coincide with an activation energy of a dopant for the quantum well and/or barrier. For example, a target valence band discontinuity can be selected such that a dopant energy level of a dopant in the adjacent barrier coincides with a valence energy band edge for the quantum well and/or a ground state energy for free carriers in a valence energy band for the quantum well. Additionally, a target doping level for the quantum well and/or adjacent barrier can be selected to facilitate a real space transfer of holes across the barrier. The quantum well and the adjacent barrier can be formed such that the actual band discontinuity and/or actual doping level(s) correspond to the relevant target(s).

[0068] Furthermore, an embodiment of the invention can be implemented as part of a solution for designing and/or fabricating a structure and/or a resulting device/structure as described in U.S. Patent Application No. 13/161,961, titled "Deep Ultraviolet Light Emitting Diode," which was filed on 16 June 2011, and which claims the benefit of U.S. Provisional Application No. 61/356,484, titled "Deep Ultraviolet Light Emitting Diode," which was filed on 18 June 2010, both of which are hereby incorporated by reference. In this case, the structure/device, such as a light emitting diode, can include an n-type contact layer and a light generating structure, which includes a set of quantum wells, adjacent to the n-type contact layer. The contact layer and light generating structure can be configured so that a difference between an energy of the n-type contact layer and an electron ground state energy of a quantum well is greater than an energy of a polar optical phonon in a material of the light generating structure. Additionally, the light generating structure can be configured so that its width is comparable to a mean free path for emission of a polar optical phonon by an electron injected into the light generating structure. The diode can include a blocking layer, which is configured so that a difference between an energy of the blocking layer and the electron ground state energy of a quantum well is greater than the energy of the polar optical phonon in the material of the light generating structure. The diode can include a composite contact, including an adhesion layer, which is at least partially transparent to light generated by the light generating structure and a

reflecting metal layer configured to reflect at least a portion of the light generated by the light generating structure. The n-type contact layer, light generating structure, blocking layer, and/or composite contact can include a superlattice configured as shown and described herein.

[0069] While shown and described herein as a method of designing and/or fabricating an emitting device to improve extraction of light from the device, it is understood that aspects of the invention further provide various alternative embodiments. For example, aspects of the invention can be implemented to facilitate the transmission of light within the device, e.g., as part of optical pumping of a laser light generating structure, excitation of a carrier gas using a laser pulse, and/or the like. Similarly, an embodiment of the invention can be implemented in conjunction with a sensing device, such as a photosensor or a photodetector. In each case, a profiled surface can be included in an exterior surface of the device and/or an interface of two adjacent layers of the device in order to facilitate the transmission of light through the interface in a desired direction.

[0070] In one embodiment, the invention provides a method of designing and/or fabricating a circuit that includes one or more of the devices designed and fabricated as described herein. To this extent, FIG. 12 shows an illustrative flow diagram for fabricating a circuit 126 according to an embodiment. Initially, a user can utilize a device design system 110 to generate a device design 112 for a semiconductor device as described herein. The device design 112 can comprise program code, which can be used by a device fabrication system 114 to generate a set of physical devices 116 according to the features defined by the device design 112. Similarly, the device design 112 can be provided to a circuit design system 120 (e.g., as an available component for use in circuits), which a user can utilize to generate a circuit design 122 (e.g., by connecting one or more inputs and outputs to various devices included in a circuit). The circuit design 122 can comprise program code that includes a device designed as described herein. In any event, the circuit design 122 and/or one or more physical devices 116 can be provided to a circuit fabrication system 124, which can generate a physical circuit 126 according to the circuit design 122. The physical circuit 126 can include one or more devices 116 designed as described herein.

[0071] In another embodiment, the invention provides a device design system 110 for designing and/or a device fabrication system 114 for fabricating a semiconductor device 116 as described herein. In this case, the system 110, 114 can comprise a general purpose computing device, which is programmed to implement a method of designing and/or fabricating the semiconductor device 116 as described herein. Similarly, an embodiment of the invention provides a circuit design system 120 for designing and/or a circuit fabrication system 124 for fabricating a circuit 126 that includes at least one device 116 designed and/or fabricated as described herein. In this case, the system 120, 124 can comprise a general purpose computing device, which is programmed to implement a method of designing and/or fabricating the circuit 126 including at least one semiconductor device 116 as described herein.

[0072] In still another embodiment, the invention provides a computer program fixed in at least one computer-readable medium, which when executed, enables a computer system to implement a method of designing and/or fabricating a semiconductor device as described herein. For example, the computer program can enable the device design system 110 to generate the device design 112 as described herein. To this extent, the computer-readable medium includes program code, which implements some or all of a process described herein when executed by the computer system. It is understood that the term "computer-readable medium" comprises one or more of any type of tangible medium of expression, now known or later developed, from which a stored copy of the program code can be perceived, reproduced, or otherwise communicated by a computing device.

[0073] In another embodiment, the invention provides a method of providing a copy of program code, which implements some or all of a process described herein when executed by a computer system. In this case, a computer system can process a copy of the program code to generate and transmit, for reception at a second, distinct location, a set of data signals that has one or more of its characteristics set and/or changed in such a manner as to encode a copy of the program code in the set of data signals. Similarly, an embodiment of the invention provides a method of acquiring a copy of program code that implements some or all of a process described herein, which includes a computer system receiving the set of data signals described herein, and translating the set of data signals into a copy of the computer program fixed in at

least one computer-readable medium. In either case, the set of data signals can be transmitted/received using any type of communications link.

[0074] In still another embodiment, the invention provides a method of generating a device design system 110 for designing and/or a device fabrication system 114 for fabricating a semiconductor device as described herein. In this case, a computer system can be obtained (e.g., created, maintained, made available, etc.) and one or more components for performing a process described herein can be obtained (e.g., created, purchased, used, modified, etc.) and deployed to the computer system. To this extent, the deployment can comprise one or more of: (1) installing program code on a computing device; (2) adding one or more computing and/or I/O devices to the computer system; (3) incorporating and/or modifying the computer system to enable it to perform a process described herein; and/or the like.

[0075] The foregoing description of various aspects of the invention has been presented for purposes of illustration and description. It is not intended to be exhaustive or to limit the invention to the precise form disclosed, and obviously, many modifications and variations are possible. Such modifications and variations that may be apparent to an individual in the art are included within the scope of the invention as defined by the accompanying claims.

CLAIMS

What is claimed is:

1. A device comprising:

a short period superlattice (SPSL) semiconductor layer comprising a plurality of barriers, wherein a composition of at least one barrier varies along lateral dimensions of the at least one barrier such that a lateral cross section of the at least one barrier includes:

a set of transparent regions, each transparent region having a transmission coefficient for a target radiation wavelength, l, greater than or equal to approximately sixty percent, wherein the set of transparent regions are at least ten percent of an area of the lateral cross section of the at least one barrier; and

a set of higher conductive regions occupying a sufficient area of the area of the lateral cross section of the at least one barrier and having an average resistance per unit area to a vertical current flow resulting in a total voltage drop across the SPSL of less than approximately five volts.

2. The device of claim 1, wherein the device is configured to emit radiation having a dominant wavelength equal to l, wherein l is within a range of approximately 210 and approximately 350 nanometers.

3. The device of claim 1, wherein the at least one barrier is formed of an $Al_xGa_{1-x}N$ alloy, where x is a molar fraction of aluminum and where x is greater than approximately $-0.0048l + 1.83$ for each transparent region.

4. The device of claim 3, wherein each of the set of higher conductive regions comprises a molar fraction of aluminum providing a band gap at least five percent smaller than a band gap of the set of transparent regions.

5. The device of claim 1, wherein the set of higher conductive regions occupy at least two percent of the area of the lateral cross section of the at least one barrier.

6. The device of claim 1, wherein the average resistance per unit area to the vertical current flow for the set of higher conductive areas is less than or equal to approximately 10^{-2} ohm·cm^2.

7. The device of claim 1, wherein the transmission coefficient is greater than or equal to approximately eighty percent.

8. The device of claim 1, wherein the device is configured to operate as one of: a light emitting diode or a laser.

9. The device of claim 1, wherein the at least one barrier is formed of an $Ga_zIn_yAl_xB_{1-x-y-z}N$ alloy, where x, y, and z are molar fractions of aluminum, indium, and gallium, respectively, and wherein the at least one barrier includes inhomogeneities in at least one of: x, y, or z.

10. The device of claim 1, wherein the plurality of barriers alternate with a plurality of wells, and wherein each of the plurality of barriers and each of the plurality of wells has a thickness less than or equal to approximately five nanometers.

11. The device of claim 1, wherein the set of set of transparent regions and the set of higher conductive regions are formed using nano-scale inhomogeneities.

12. The device of claim 1, wherein a characteristic distance between two higher conductive regions in the set of higher conductive regions is less than a lateral current spreading length.

13. A device comprising:

a short period superlattice (SPSL) semiconductor layer comprising a plurality of barriers, wherein a lateral cross section of each barrier includes:

a set of transparent regions, each transparent region having a transmission coefficient for a target radiation wavelength, l, greater than or equal to approximately sixty percent, wherein the set of transparent regions are at least ten percent of an area of the lateral cross section of the barrier; and

a set of higher conductive regions occupying a sufficient area of the area of the lateral cross section of the barrier and having an average resistance per unit area to a vertical current flow resulting in a total voltage drop across the SPSL of less than approximately five volts.

14. The device of claim 13, wherein each barrier is formed of an $Al_xGa_{1-x}N$ alloy, where x is a molar fraction of aluminum and where x is greater than approximately $-0.0048\lambda + 1.83$ for each transparent region.

15. The device of claim 13, wherein the set of transparent regions and the set of higher conductive regions are formed by a non-uniform barrier thickness of each barrier.

16. The device of claim 13, wherein the set of transparent regions and the set of higher conductive regions are formed by a non-uniform compositional distribution along the barrier thickness of each barrier.

17. The device of claim 13, wherein the set of transparent regions and the set of higher conductive regions are formed by a non-uniform doping distribution along the barrier thickness of each barrier.

18. A method of fabricating a device comprising:

forming a short period superlattice (SPSL) semiconductor layer comprising a plurality of barriers, wherein a lateral cross section of each barrier includes:

a set of transparent regions, each transparent region having a transmission coefficient for a target radiation wavelength, λ, greater than or equal to approximately sixty percent, wherein the set of transparent regions are at least ten percent of an area of the lateral cross section of the barrier; and

a set of higher conductive regions occupying a sufficient area of the area of the lateral cross section of the barrier and having an average resistance per unit area to a vertical current flow resulting in a total voltage drop across the SPSL of less than approximately five volts.

19. The method of claim 18, wherein the forming includes forming each barrier of an $Al_xGa_{1-x}N$ alloy, where x is a molar fraction of aluminum and where x is greater than approximately $-0.0048l + 1.83$ for each transparent region.

20. The method of claim 18, wherein the forming includes forming the set of transparent regions and the set of higher conductive regions using a non-uniform barrier thickness of each barrier.

21. The method of claim 18, wherein the forming includes forming the set of transparent regions and the set of higher conductive regions using a non-uniform compositional distribution along the barrier thickness of each barrier.

22. The method of claim 18, wherein the forming includes forming the set of transparent regions and the set of higher conductive regions using a non-uniform doping distribution along the barrier thickness of each barrier.

23. The method of claim 18, further comprising forming an inhomogeneous layer, wherein the SPSL semiconductor layer is formed directly on the inhomogeneous layer, and wherein at least a portion of the forming the inhomogeneous layer is performed at an inhomogeneous growth temperature at least approximately two hundred degrees Celsius lower than a temperature for forming the SPSL semiconductor layer.

24. The method of claim 23, wherein forming the inhomogeneous layer includes:

enabling three-dimensional islands to coalesce at the inhomogeneous growth temperature; and

enabling two-dimensional growth around the islands at a growth temperature comparable to the temperature for forming the SPSL semiconductor layer.

FIG. 1
Prior Art

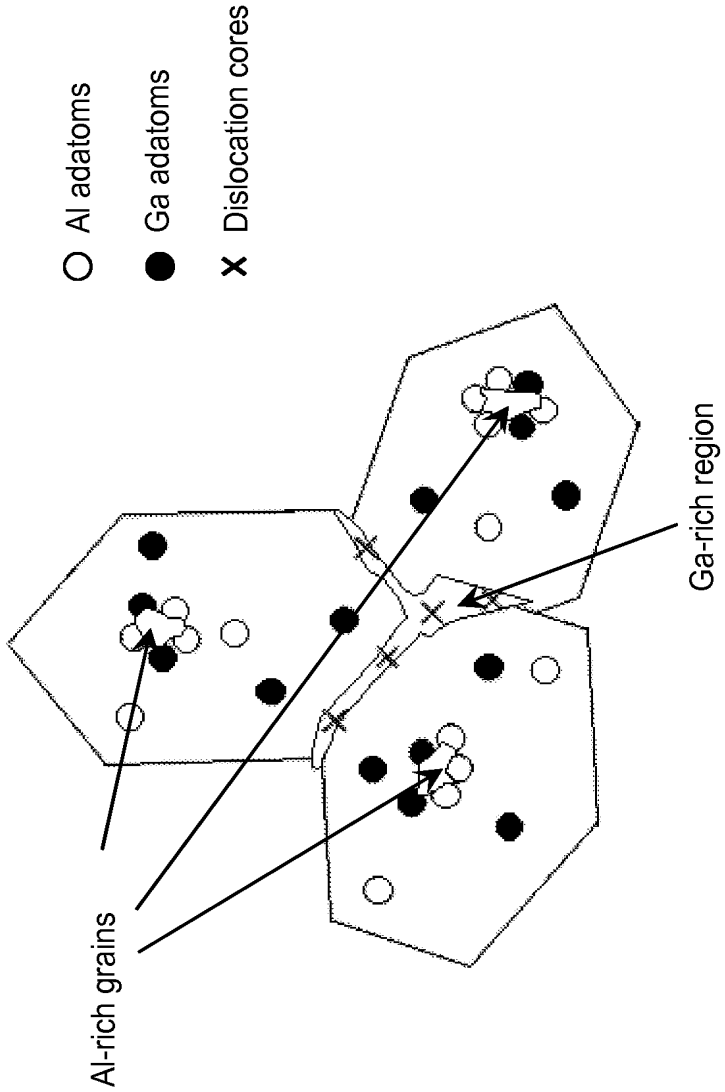


FIG. 2

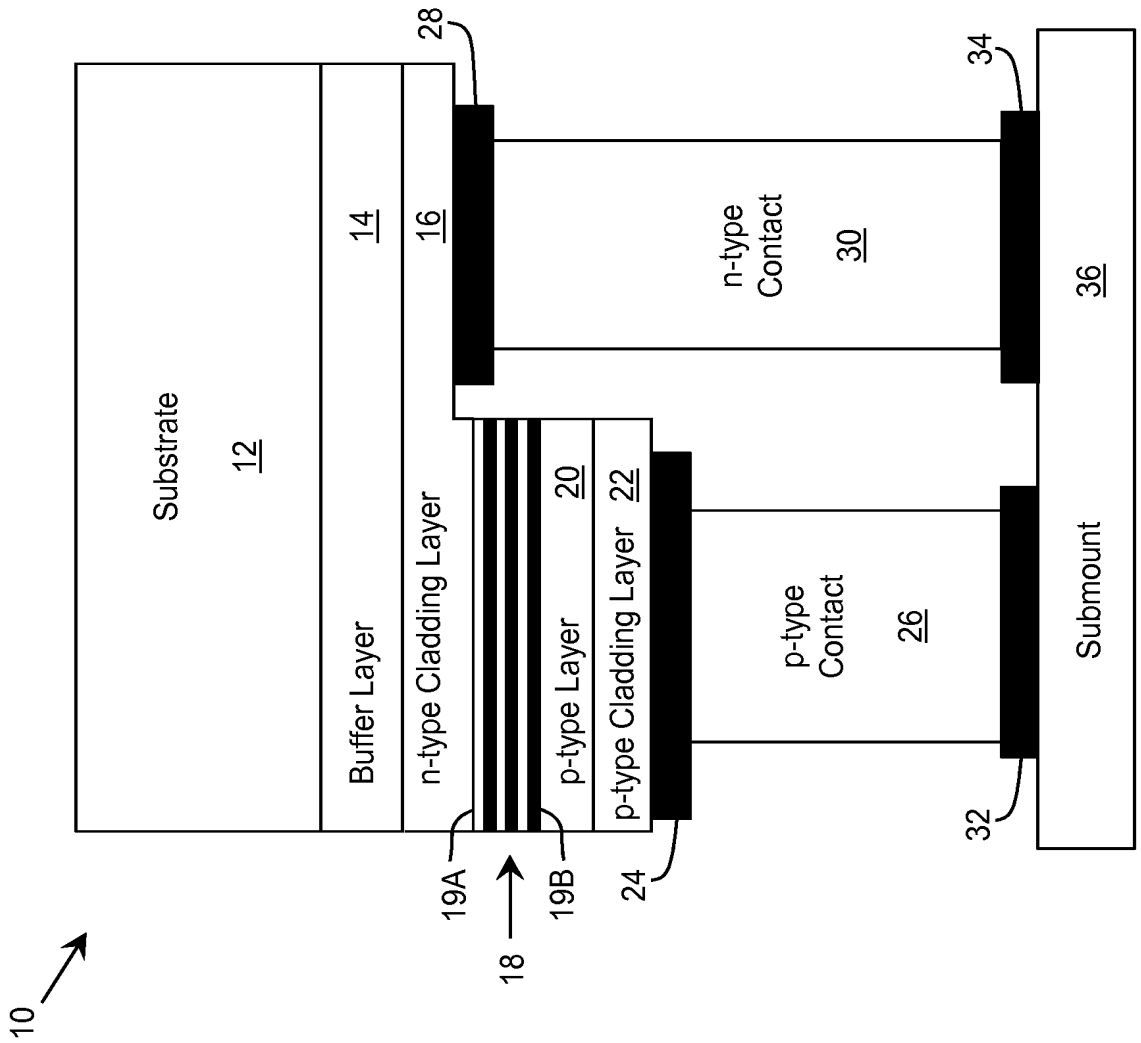

10
18
19A
19B
24
28
32
34
Substrate
12
Buffer Layer
14
n-type Cladding Layer
16
p-type Layer
20
p-type Cladding Layer
22
n-type Contact
30
p-type Contact
26
Submount
36

FIG. 3B

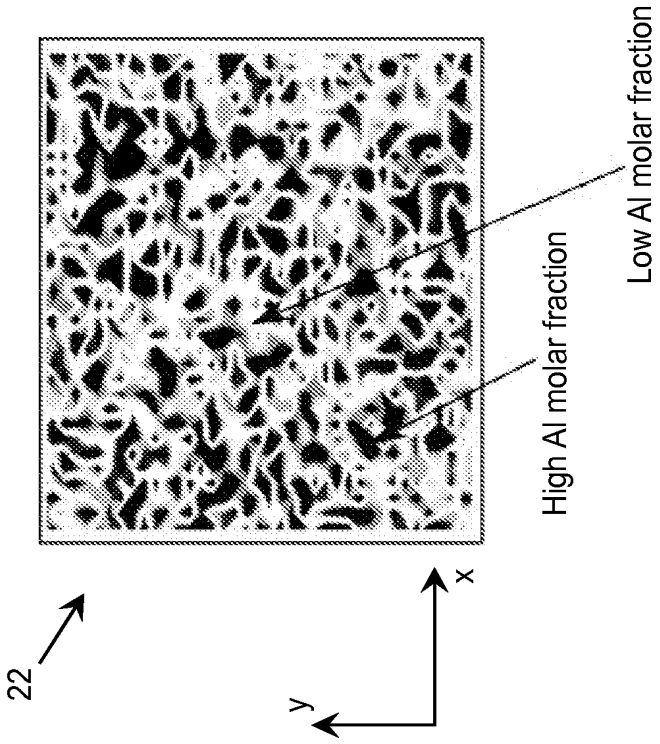

Low Al molar fraction
High Al molar fraction
22
x
y

FIG. 3A

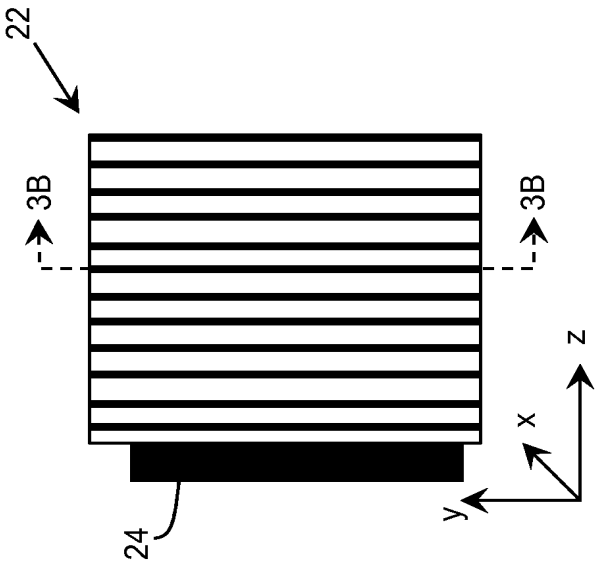

22
3B
3B
24
z
x
y

FIG. 4

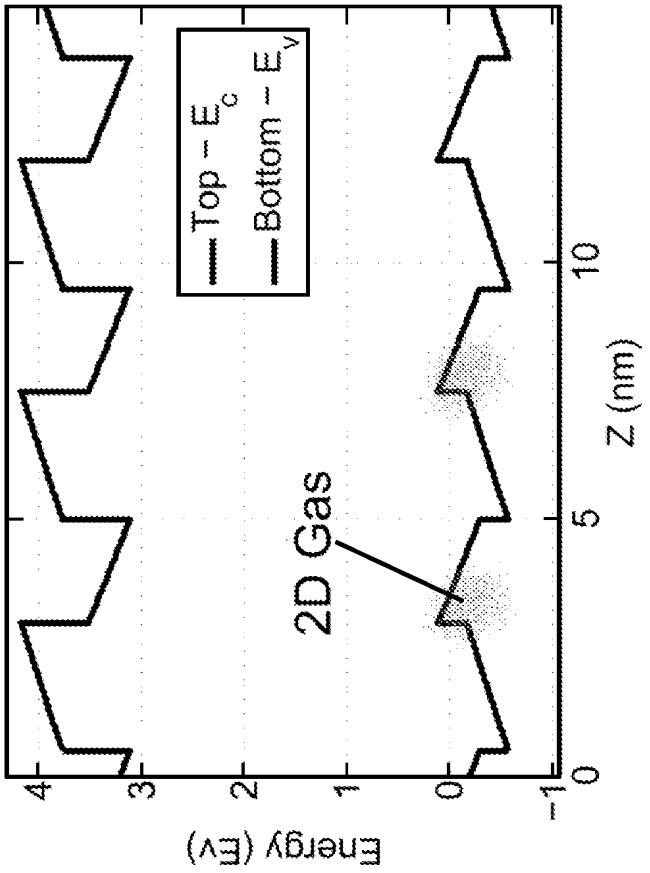


FIG. 5

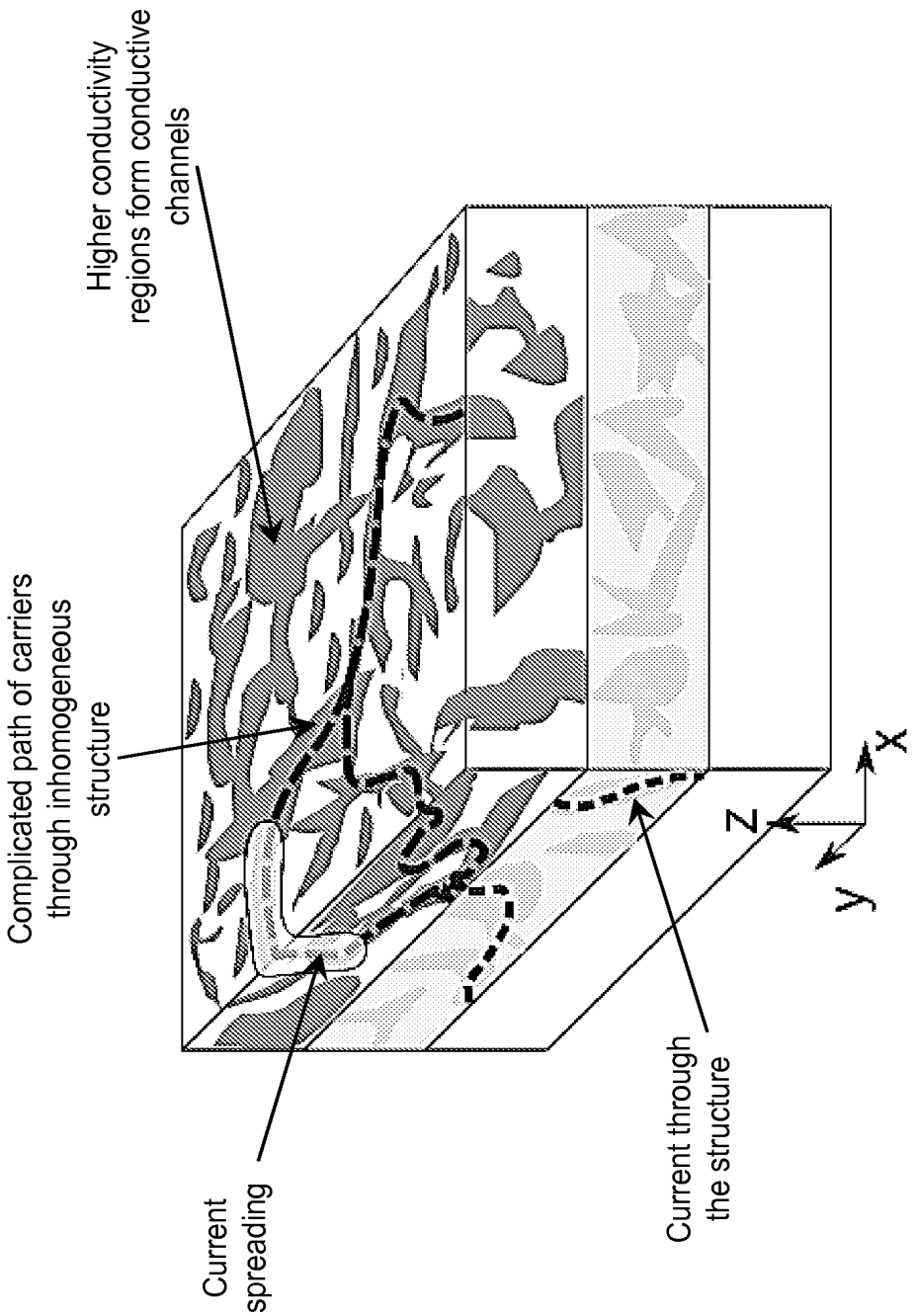

Higher conductivity regions form conductive channels
Complicated path of carriers through inhomogeneous structure
Current spreading
Current through the structure
Z
X
y

FIG. 6

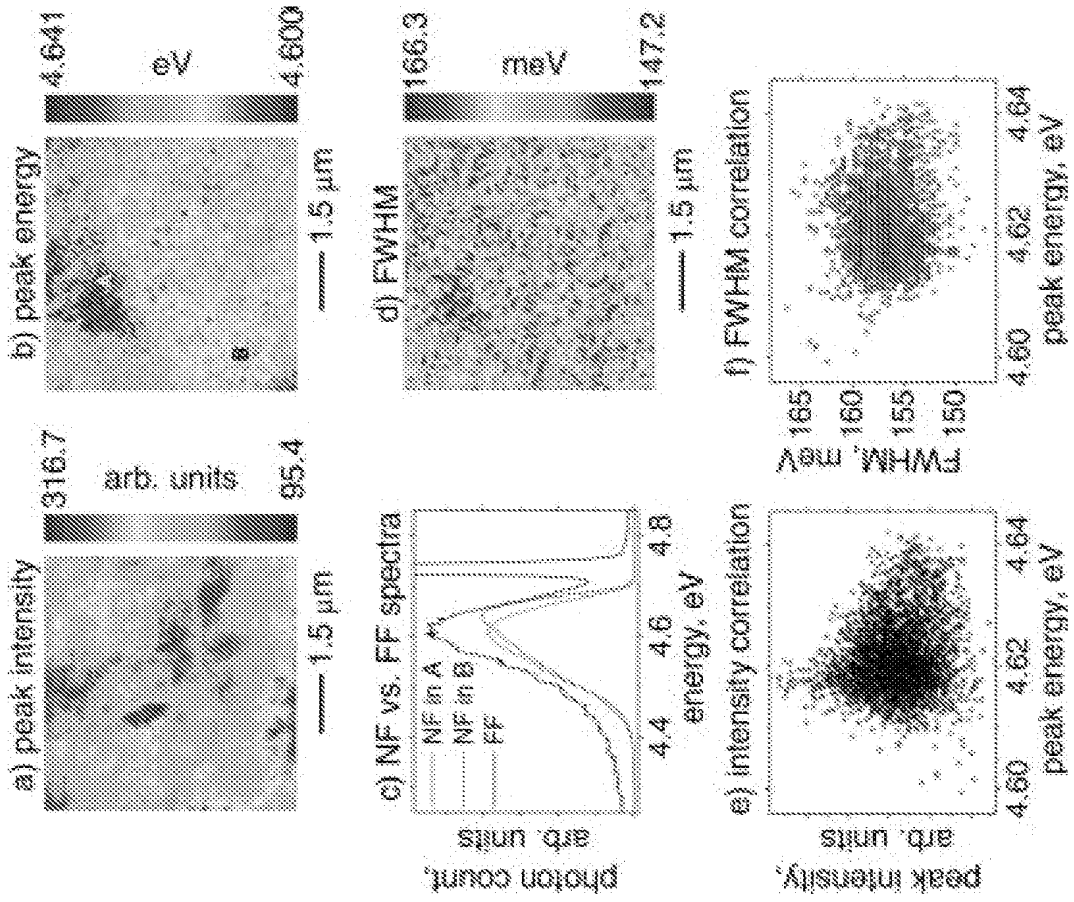

a) peak intensity
316.7
arb. units
95.4
1.5 μm
b) peak energy
4.641
eV
4.600
1.5 μm
c) NF vs. FF spectra
NF in A
NF in B
FF
photon count, arb. units
4.4
4.6
4.8
energy, eV
d) FWHM
166.3
meV
147.2
1.5 μm
e) intensity correlation
peak intensity, arb. units
4.60
4.62
4.64
peak energy, eV
f) FWHM correlation
FWHM, meV
165
160
155
150
4.60
4.62
4.64
peak energy, eV

FIG. 7

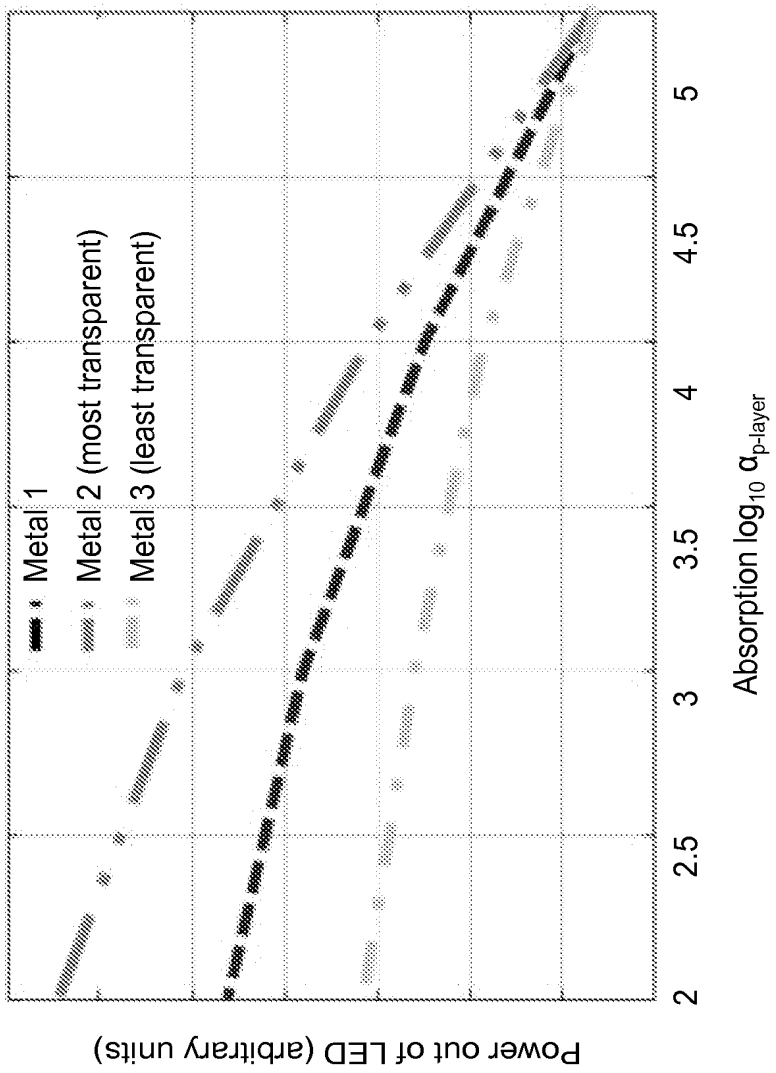

Metal 1
Metal 2 (most transparent)
Metal 3 (least transparent)
Power out of LED (arbitrary units)
2
2.5
3
3.5
4
4.5
5
Absorption log10 αp-layer

FIG. 8

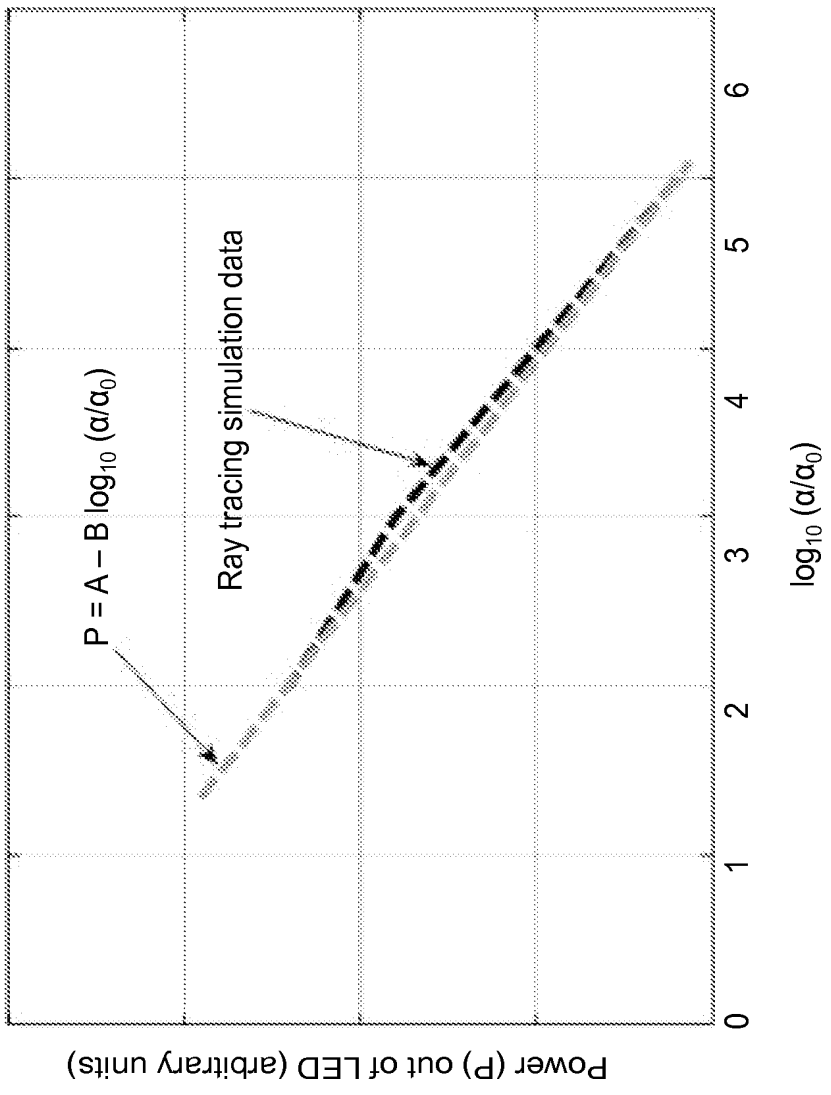

P = A – B log10 (α/α0)
Ray tracing simulation data
Power (P) out of LED (arbitrary units)
log10 (α/α0)
0
1
2
3
4
5
6

FIG. 9

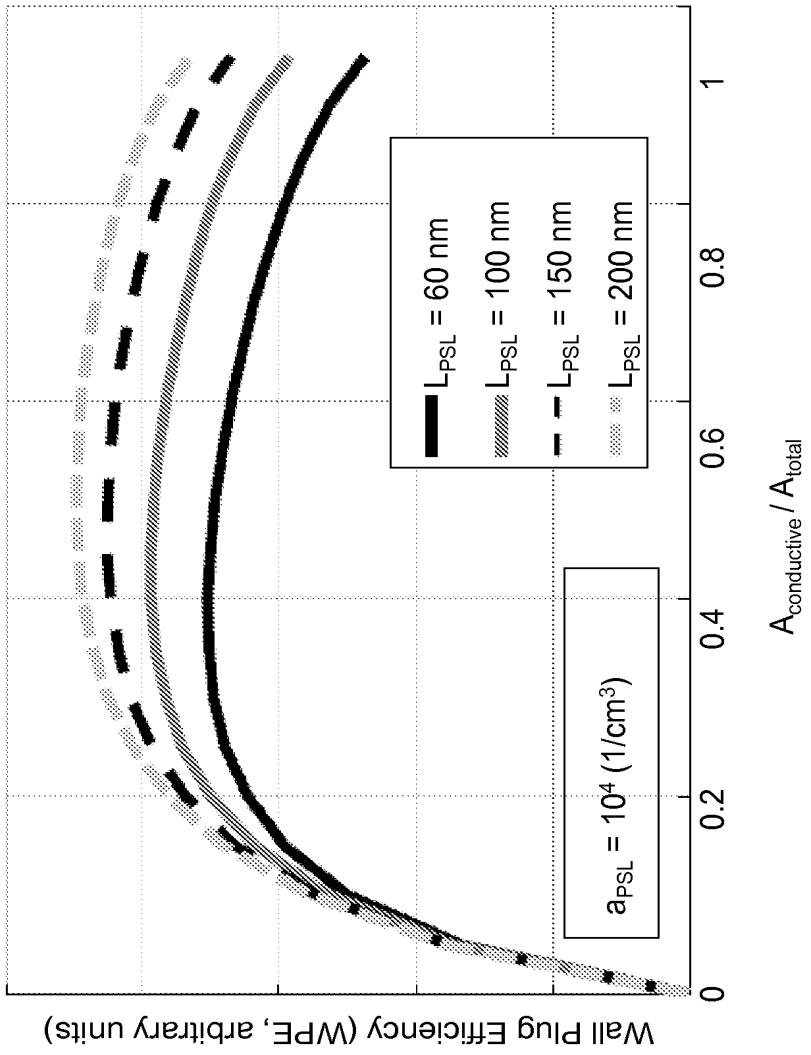

Wall Plug Efficiency (WPE, arbitrary units)
0
0.2
0.4
0.6
0.8
1
$A_{conductive} / A_{total}$
L_{PSL} = 60 nm
L_{PSL} = 100 nm
L_{PSL} = 150 nm
L_{PSL} = 200 nm
$a_{PSL} = 10^4$ (1/cm^3)

FIG. 10

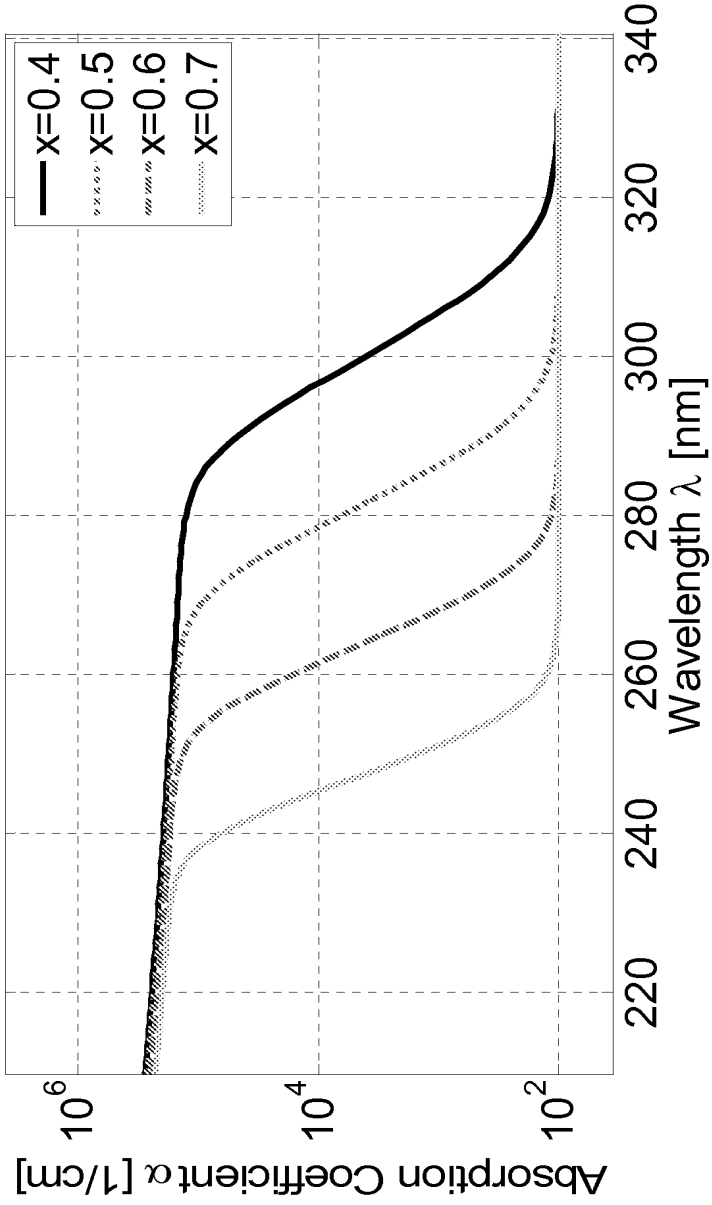

x=0.4
x=0.5
x=0.6
x=0.7
Absorption Coefficient α [1/cm]
10^6
10^4
10^2
220
240
260
280
300
320
340
Wavelength λ [nm]

FIG. 11

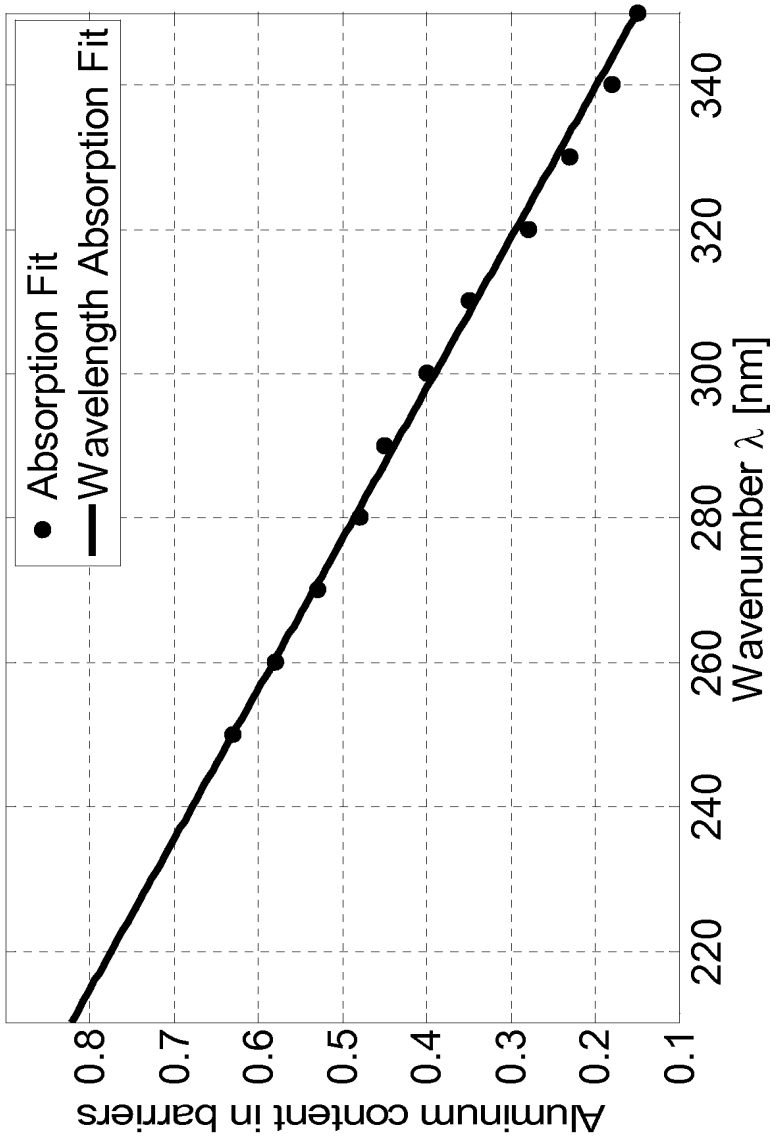
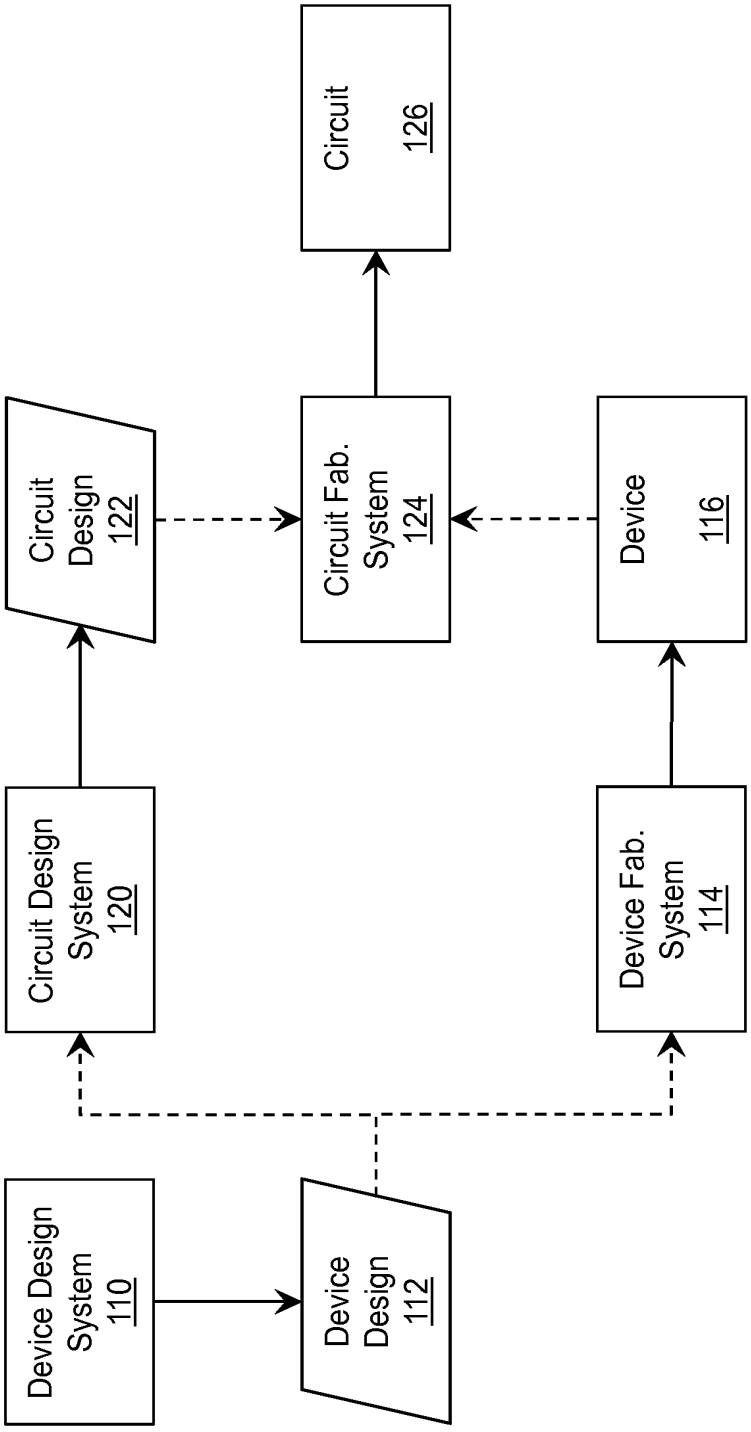

Absorption Fit
Wavelength Absorption Fit
Aluminum content in barriers
0.8
0.7
0.6
0.5
0.4
0.3
0.2
0.1
220
240
260
280
300
320
340
Wavenumber λ [nm]

FIG. 12


Device Design System 110
Device Design 112
Circuit Design System 120
Circuit Design 122
Device Fab. System 114
Device 116
Circuit Fab. System 124
Circuit 126

Electronic Acknowledgement Receipt

EFS ID:	24500260
Application Number:	14984156
International Application Number:	
Confirmation Number:	5890
Title of Invention:	Semiconductor Structure with Inhomogeneous Regions
First Named Inventor/Applicant Name:	
Customer Number:	11698
Filer:	John W LaBatt
Filer Authorized By:	
Attorney Docket Number:	SETI-0110-CIP-US
Receipt Date:	05-JAN-2016
Filing Date:	
Time Stamp:	09:18:57
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	no

File Listing:

Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1	Information Disclosure Statement (IDS) Form (SB08)	SETI-0110-CIP-US_IDS.pdf	1035418 852e70e848b963080a4737f1792550c31d387e28	no	4

Warnings:	
Information:	

2	Foreign Reference	WO2013023197.pdf	1739187 445e1616d68b816577c47ebc927c7c7576ba995a	no	41
Warnings:					
Information:					
3	Non Patent Literature	Shatalov_AlGaNDeep-UltravioletLight-EmittingDiodes.pdf	427100 32797b4b52c476b4d23450dc90f283cff2d097bb	no	3
Warnings:					
Information:					
4	Non Patent Literature	SETI-0110-US_NoticeofAllowance_12-30-15.pdf	413549 7ed47ead0d07a6b0617953513 47f4193f9e5d070	no	8
Warnings:					
Information:					
5	Non Patent Literature	SETI-0110-US_ExParteQuayle_09-24-15.pdf	740637 606917883108ea7dd8e62acfe2570a773ae643c2	no	17
Warnings:					
Information:					
		Total Files Size (in bytes):	4355891		

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New Applications Under 35 U.S.C. 111

If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application.

National Stage of an International Application under 35 U.S.C. 371

If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.

New International Application Filed with the USPTO as a Receiving Office

If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.

PATENT APPLICATION FEE DETERMINATION RECORD

Substitute for Form PTO-875

Application or Docket Number: 14/984,156

APPLICATION AS FILED - PART I

FOR	(Column 1) NUMBER FILED	(Column 2) NUMBER EXTRA	SMALL ENTITY RATE($)	SMALL ENTITY FEE($)	OR	OTHER THAN SMALL ENTITY RATE($)	OTHER THAN SMALL ENTITY FEE($)
BASIC FEE (37 CFR 1.16(a), (b), or (c))	N/A	N/A	N/A			N/A	280
SEARCH FEE (37 CFR 1.16(k), (i), or (m))	N/A	N/A	N/A			N/A	600
EXAMINATION FEE (37 CFR 1.16(o), (p), or (q))	N/A	N/A	N/A			N/A	720
TOTAL CLAIMS (37 CFR 1.16(i))	20 minus 20 =	*			OR	x 80 =	0.00
INDEPENDENT CLAIMS (37 CFR 1.16(h))	3 minus 3 =	*				x 420 =	0.00
APPLICATION SIZE FEE (37 CFR 1.16(s))	If the specification and drawings exceed 100 sheets of paper, the application size fee due is $310 ($155 for small entity) for each additional 50 sheets or fraction thereof. See 35 U.S.C. 41(a)(1)(G) and 37 CFR 1.16(s).						0.00
MULTIPLE DEPENDENT CLAIM PRESENT (37 CFR 1.16(j))							0.00
* If the difference in column 1 is less than zero, enter "0" in column 2.			TOTAL			TOTAL	1600

APPLICATION AS AMENDED - PART II

		(Column 1) CLAIMS REMAINING AFTER AMENDMENT		(Column 2) HIGHEST NUMBER PREVIOUSLY PAID FOR	(Column 3) PRESENT EXTRA	SMALL ENTITY RATE($)	SMALL ENTITY ADDITIONAL FEE($)	OR	OTHER THAN SMALL ENTITY RATE($)	OTHER THAN SMALL ENTITY ADDITIONAL FEE($)
AMENDMENT A	Total (37 CFR 1.16(i))	*	Minus	**	=	x =		OR	x =	
	Independent (37 CFR 1.16(h))	*	Minus	***	=	x =		OR	x =	
	Application Size Fee (37 CFR 1.16(s))									
	FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))							OR		
						TOTAL ADD'L FEE		OR	TOTAL ADD'L FEE	

		(Column 1) CLAIMS REMAINING AFTER AMENDMENT		(Column 2) HIGHEST NUMBER PREVIOUSLY PAID FOR	(Column 3) PRESENT EXTRA	RATE($)	ADDITIONAL FEE($)		RATE($)	ADDITIONAL FEE($)
AMENDMENT B	Total (37 CFR 1.16(i))	*	Minus	**	=	x =		OR	x =	
	Independent (37 CFR 1.16(h))	*	Minus	***	=	x =		OR	x =	
	Application Size Fee (37 CFR 1.16(s))									
	FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))							OR		
						TOTAL ADD'L FEE		OR	TOTAL ADD'L FEE	

* If the entry in column 1 is less than the entry in column 2, write "0" in column 3.
** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 20, enter "20".
*** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 3, enter "3".
The "Highest Number Previously Paid For" (Total or Independent) is the highest found in the appropriate box in column 1.

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APPLICATION NUMBER	FILING or 371(c) DATE	GRP ART UNIT	FIL FEE REC'D	ATTY.DOCKET.NO	TOT CLAIMS	IND CLAIMS
14/984,156	12/30/2015	2811	1740	SETI-0110-CIP-US	20	3

CONFIRMATION NO. 5890

FILING RECEIPT

11698
LaBatt, LLC (SET)
PO Box 630
Valatie, NY 12184

OC000000079956255

Date Mailed: 01/19/2016

Receipt is acknowledged of this non-provisional patent application. The application will be taken up for examination in due course. Applicant will be notified as to the results of the examination. Any correspondence concerning the application must include the following identification information: the U.S. APPLICATION NUMBER, FILING DATE, NAME OF APPLICANT, and TITLE OF INVENTION. Fees transmitted by check or draft are subject to collection. Please verify the accuracy of the data presented on this receipt. **If an error is noted on this Filing Receipt, please submit a written request for a Filing Receipt Correction. Please provide a copy of this Filing Receipt with the changes noted thereon. If you received a "Notice to File Missing Parts" for this application, please submit any corrections to this Filing Receipt with your reply to the Notice. When the USPTO processes the reply to the Notice, the USPTO will generate another Filing Receipt incorporating the requested corrections**

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Assignment For Published Patent Application

Sensor Electronic Technology, Inc., Columbia, SC

Power of Attorney: The patent practitioners associated with Customer Number 11698

Domestic Priority data as claimed by applicant

This application is a CIP of 14/189,012 02/25/2014
which claims benefit of 61/768,581 02/25/2013

Foreign Applications for which priority is claimed (You may be eligible to benefit from the **Patent Prosecution Highway** program at the USPTO. Please see http://www.uspto.gov for more information.) - None.
Foreign application information must be provided in an Application Data Sheet in order to constitute a claim to foreign priority. See 37 CFR 1.55 and 1.76.

Permission to Access Application via Priority Document Exchange: Yes

Permission to Access Search Results: Yes

Applicant may provide or rescind an authorization for access using Form PTO/SB/39 or Form PTO/SB/69 as appropriate.

If Required, Foreign Filing License Granted: 01/15/2016
The country code and number of your priority application, to be used for filing abroad under the Paris Convention, is **US 14/984,156**
Projected Publication Date: 04/28/2016
Non-Publication Request: No
Early Publication Request: No
Title

Semiconductor Structure with Inhomogeneous Regions

Preliminary Class

257

Statement under 37 CFR 1.55 or 1.78 for AIA (First Inventor to File) Transition Applications: Yes

PROTECTING YOUR INVENTION OUTSIDE THE UNITED STATES

Since the rights granted by a U.S. patent extend only throughout the territory of the United States and have no effect in a foreign country, an inventor who wishes patent protection in another country must apply for a patent in a specific country or in regional patent offices. Applicants may wish to consider the filing of an international application under the Patent Cooperation Treaty (PCT). An international (PCT) application generally has the same effect as a regular national patent application in each PCT-member country. The PCT process **simplifies** the filing of patent applications on the same invention in member countries, but **does not result** in a grant of "an international patent" and does not eliminate the need of applicants to file additional documents and fees in countries where patent protection is desired.

Almost every country has its own patent law, and a person desiring a patent in a particular country must make an application for patent in that country in accordance with its particular laws. Since the laws of many countries differ in various respects from the patent law of the United States, applicants are advised to seek guidance from specific foreign countries to ensure that patent rights are not lost prematurely.

Applicants also are advised that in the case of inventions made in the United States, the Director of the USPTO must issue a license before applicants can apply for a patent in a foreign country. The filing of a U.S. patent application serves as a request for a foreign filing license. The application's filing receipt contains further information and guidance as to the status of applicant's license for foreign filing.

Applicants may wish to consult the USPTO booklet, "General Information Concerning Patents" (specifically, the section entitled "Treaties and Foreign Patents") for more information on timeframes and deadlines for filing foreign patent applications. The guide is available either by contacting the USPTO Contact Center at 800-786-9199, or it can be viewed on the USPTO website at http://www.uspto.gov/web/offices/pac/doc/general/index.html.

For information on preventing theft of your intellectual property (patents, trademarks and copyrights), you may wish to consult the U.S. Government website, http://www.stopfakes.gov. Part of a Department of Commerce initiative, this website includes self-help "toolkits" giving innovators guidance on how to protect intellectual property in specific

countries such as China, Korea and Mexico. For questions regarding patent enforcement issues, applicants may call the U.S. Government hotline at 1-866-999-HALT (1-866-999-4258).

LICENSE FOR FOREIGN FILING UNDER

Title 35, United States Code, Section 184

Title 37, Code of Federal Regulations, 5.11 & 5.15

GRANTED

The applicant has been granted a license under 35 U.S.C. 184, if the phrase "IF REQUIRED, FOREIGN FILING LICENSE GRANTED" followed by a date appears on this form. Such licenses are issued in all applications where the conditions for issuance of a license have been met, regardless of whether or not a license may be required as set forth in 37 CFR 5.15. The scope and limitations of this license are set forth in 37 CFR 5.15(a) unless an earlier license has been issued under 37 CFR 5.15(b). The license is subject to revocation upon written notification. The date indicated is the effective date of the license, unless an earlier license of similar scope has been granted under 37 CFR 5.13 or 5.14.

This license is to be retained by the licensee and may be used at any time on or after the effective date thereof unless it is revoked. This license is automatically transferred to any related applications(s) filed under 37 CFR 1.53(d). This license is not retroactive.

The grant of a license does not in any way lessen the responsibility of a licensee for the security of the subject matter as imposed by any Government contract or the provisions of existing laws relating to espionage and the national security or the export of technical data. Licensees should apprise themselves of current regulations especially with respect to certain countries, of other agencies, particularly the Office of Defense Trade Controls, Department of State (with respect to Arms, Munitions and Implements of War (22 CFR 121-128)); the Bureau of Industry and Security, Department of Commerce (15 CFR parts 730-774); the Office of Foreign AssetsControl, Department of Treasury (31 CFR Parts 500+) and the Department of Energy.

NOT GRANTED

No license under 35 U.S.C. 184 has been granted at this time, if the phrase "IF REQUIRED, FOREIGN FILING LICENSE GRANTED" DOES NOT appear on this form. Applicant may still petition for a license under 37 CFR 5.12, if a license is desired before the expiration of 6 months from the filing date of the application. If 6 months has lapsed from the filing date of this application and the licensee has not received any indication of a secrecy order under 35 U.S.C. 181, the licensee may foreign file the application pursuant to 37 CFR 5.15(b).

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The United States represents the largest, most dynamic marketplace in the world and is an unparalleled location for business investment, innovation, and commercialization of new technologies. The U.S. offers tremendous resources and advantages for those who invest and manufacture goods here. Through SelectUSA, our nation works to promote and facilitate business investment. SelectUSA provides information assistance to the international investor community; serves as an ombudsman for existing and potential investors; advocates on behalf of U.S. cities, states, and regions competing for global investment; and counsels U.S. economic development organizations on investment attraction best practices. To learn more about why the United States is the best country in the world to develop

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United States Patent and Trademark Office
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Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NUMBER	FILING OR 371(C) DATE	FIRST NAMED APPLICANT	ATTY. DOCKET NO./TITLE
14/984,156	12/30/2015	Maxim S. Shatalov	SETI-0110-CIP-US

CONFIRMATION NO. 5890

11698
LaBatt, LLC (SET)
PO Box 630
Valatie, NY 12184

INFORMAL NOTICE

OC000000079956256

Date Mailed: 01/19/2016

INFORMATIONAL NOTICE TO APPLICANT

Applicant is notified that the above-identified application contains the deficiencies noted below. No period for reply is set forth in this notice for correction of these deficiencies. However, if a deficiency relates to the inventor's oath or declaration, the applicant must file an oath or declaration in compliance with 37 CFR 1.63, or a substitute statement in compliance with 37 CFR 1.64, executed by or with respect to each actual inventor no later than the expiration of the time period set in the "Notice of Allowability" to avoid abandonment. See 37 CFR 1.53(f).

The item(s) indicated below are also required and should be submitted with any reply to this notice to avoid further processing delays.

- A properly executed inventor's oath or declaration has not been received for the following inventor(s):
  Maxim S. Shatalov
  Alexander Dobrinsky
  Alexander Lunev
  Rakesh Jain
  Jinwei Yang
  Michael Shur
  Remigijus Gaska

Questions about the contents of this notice and the requirements it sets forth should be directed to the Office of Data Management, Application Assistance Unit, at **(571) 272-4000** or **(571) 272-4200** or **1-888-786-0101**.

/rmohamed/

DECLARATION (37 CFR 1.63) FOR UTILITY OR DESIGN PATENT APPLICATION USING AN APPLICATION DATA SHEET (37 CFR 1.76)

As a below named inventor, I hereby declare that:

This declaration is directed to:

Title of the Invention: Semiconductor Structure with Inhomogeneous Regions

Attorney Docket Number: SETI-0110-CIP-US

the specification of which:

☒ is attached hereto, or

☐ is United States Patent Application No. _____ filed on _____, or

☐ is PCT International Application No. _____ filed on _____.

The above-identified application was made or authorized to be made by me.

I believe that I am the original inventor or an original joint inventor of a claimed invention in the application.

I hereby state that I have reviewed and understand the contents of the above-identified application, including the claims.

I hereby acknowledge that I have a duty to disclose information which is material to the patentability as defined in Title 37, Code of Federal Regulations, §1.56.

I hereby acknowledge that any willful false statement made in this declaration is punishable under 18 U.S.C. 1001 by fine or imprisonment of not more than five (5) years, or both.

Legal Name of inventor: **Maxim S. Shatalov**

Inventor's Signature: /Max Shatalov/ Digitally signed by Max Shatalov DN: cn=Max Shatalov, o=Sensor Electronic Technology, Inc., ou, email=shatalov@s-et.com, c=US Date: 2015.12.30 10:29:44 -05'00'

Date: 12/30/2015

Note: An application data sheet, including naming the entire inventive entity, must accompany this form.

DECLARATION (37 CFR 1.63) FOR UTILITY OR DESIGN PATENT APPLICATION USING AN APPLICATION DATA SHEET (37 CFR 1.76)

As a below named inventor, I hereby declare that:

This declaration is directed to:

Title of the Invention: Semiconductor Structure with Inhomogeneous Regions

Attorney Docket Number: SETI-0110-CIP-US

the specification of which:

☒ is attached hereto, or

☐ is United States Patent Application No. _____ filed on _____, or

☐ is PCT International Application No. _____ filed on _____.

The above-identified application was made or authorized to be made by me.

I believe that I am the original inventor or an original joint inventor of a claimed invention in the application.

I hereby state that I have reviewed and understand the contents of the above-identified application, including the claims.

I hereby acknowledge that I have a duty to disclose information which is material to the patentability as defined in Title 37, Code of Federal Regulations, §1.56.

I hereby acknowledge that any willful false statement made in this declaration is punishable under 18 U.S.C. 1001 by fine or imprisonment of not more than five (5) years, or both.

Legal Name of inventor: **Alexander Dobrinsky**

Inventor's Signature: /Alexander Dobrinsky/

Date: 12/30/2015

Note: An application data sheet, including naming the entire inventive entity, must accompany this form.

DECLARATION (37 CFR 1.63) FOR UTILITY OR DESIGN PATENT APPLICATION USING AN APPLICATION DATA SHEET (37 CFR 1.76)

As a below named inventor, I hereby declare that:

This declaration is directed to:

Title of the Invention: Semiconductor Structure with Inhomogeneous Regions

Attorney Docket Number: SETI-0110-CIP-US

the specification of which:

☒ is attached hereto, or

☐ is United States Patent Application No. _____ filed on _____, or

☐ is PCT International Application No. _____ filed on _____.

The above-identified application was made or authorized to be made by me.

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I hereby state that I have reviewed and understand the contents of the above-identified application, including the claims.

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I hereby acknowledge that any willful false statement made in this declaration is punishable under 18 U.S.C. 1001 by fine or imprisonment of not more than five (5) years, or both.

Legal Name of inventor: **Alexander Lunev**

Inventor's Signature: /_____/

Date: _____

Note: An application data sheet, including naming the entire inventive entity, must accompany this form.

DECLARATION (37 CFR 1.63) FOR UTILITY OR DESIGN PATENT APPLICATION USING AN APPLICATION DATA SHEET (37 CFR 1.76)

As a below named inventor, I hereby declare that:

This declaration is directed to:

Title of the Invention: Semiconductor Structure with Inhomogeneous Regions

Attorney Docket Number: SETI-0110-CIP-US

the specification of which:

☒ is attached hereto, or

☐ is United States Patent Application No. _____ filed on _____, or

☐ is PCT International Application No. _____ filed on _____.

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I hereby acknowledge that any willful false statement made in this declaration is punishable under 18 U.S.C. 1001 by fine or imprisonment of not more than five (5) years, or both.

Legal Name of inventor: **Rakesh Jain**

Inventor's Signature: /  /

Date: 12/30/2015

Note: An application data sheet, including naming the entire inventive entity, must accompany this form.

DECLARATION (37 CFR 1.63) FOR UTILITY OR DESIGN PATENT APPLICATION USING AN APPLICATION DATA SHEET (37 CFR 1.76)

As a below named inventor, I hereby declare that:

This declaration is directed to:

Title of the Invention: Semiconductor Structure with Inhomogeneous Regions

Attorney Docket Number: SETI-0110-CIP-US

the specification of which:

☒ is attached hereto, or

☐ is United States Patent Application No. _____ filed on _____, or

☐ is PCT International Application No. _____ filed on _____.

The above-identified application was made or authorized to be made by me.

I believe that I am the original inventor or an original joint inventor of a claimed invention in the application.

I hereby state that I have reviewed and understand the contents of the above-identified application, including the claims.

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I hereby acknowledge that any willful false statement made in this declaration is punishable under 18 U.S.C. 1001 by fine or imprisonment of not more than five (5) years, or both.

Legal Name of inventor: **Jinwei Yang**

Inventor's Signature: /Jinwei Yang/

Date: 1/1/2016

Note: An application data sheet, including naming the entire inventive entity, must accompany this form.

DECLARATION (37 CFR 1.63) FOR UTILITY OR DESIGN PATENT APPLICATION USING AN APPLICATION DATA SHEET (37 CFR 1.76)

As a below named inventor, I hereby declare that:

This declaration is directed to:

Title of the Invention: Semiconductor Structure with Inhomogeneous Regions

Attorney Docket Number: SETI-0110-CIP-US

the specification of which:

☒ is attached hereto, or

☐ is United States Patent Application No. _____ filed on _____, or

☐ is PCT International Application No. _____ filed on _____.

The above-identified application was made or authorized to be made by me.

I believe that I am the original inventor or an original joint inventor of a claimed invention in the application.

I hereby state that I have reviewed and understand the contents of the above-identified application, including the claims.

I hereby acknowledge that I have a duty to disclose information which is material to the patentability as defined in Title 37, Code of Federal Regulations, §1.56.

I hereby acknowledge that any willful false statement made in this declaration is punishable under 18 U.S.C. 1001 by fine or imprisonment of not more than five (5) years, or both.

Legal Name of inventor: **Michael Shur**

Inventor's Signature: /_____/

Date: 12/30/2015

Note: An application data sheet, including naming the entire inventive entity, must accompany this form.

DECLARATION (37 CFR 1.63) FOR UTILITY OR DESIGN PATENT APPLICATION USING AN APPLICATION DATA SHEET (37 CFR 1.76)

As a below named inventor, I hereby declare that:

This declaration is directed to:

Title of the Invention: Semiconductor Structure with Inhomogeneous Regions

Attorney Docket Number: SETI-0110-CIP-US

the specification of which:

☒ is attached hereto, or

☐ is United States Patent Application No. _____ filed on _____, or

☐ is PCT International Application No. _____ filed on _____.

The above-identified application was made or authorized to be made by me.

I believe that I am the original inventor or an original joint inventor of a claimed invention in the application.

I hereby state that I have reviewed and understand the contents of the above-identified application, including the claims.

I hereby acknowledge that I have a duty to disclose information which is material to the patentability as defined in Title 37, Code of Federal Regulations, §1.56.

I hereby acknowledge that any willful false statement made in this declaration is punishable under 18 U.S.C. 1001 by fine or imprisonment of not more than five (5) years, or both.

Legal Name of inventor: **Remigijus Gaska**

Inventor's Signature: /R. Gaska/

Date: 1/5/2016

Note: An application data sheet, including naming the entire inventive entity, must accompany this form.

Doc code: Oath
Document Description: Oath or declaration filed

PTO/AIA/02 (07-13)
Approved for use through 04/30/2017. OMB 0651-0032
U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE

SUBSTITUTE STATEMENT IN LIEU OF AN OATH OR DECLARATION FOR UTILITY OR DESIGN PATENT APPLICATION (35 U.S.C. 115(d) AND 37 CFR 1.64)

Title of Invention	Semiconductor Structure with Inhomogeneous Regions

This statement is directed to:

☐ The attached application,

OR

☒ United States application or PCT international application number 14984156 filed on 12-30-2015.

LEGAL NAME of inventor to whom this substitute statement applies:

(*E.g.*, Given Name (first and middle (if any)) and Family Name or Surname)

Alexander Lunev

Residence (except for a deceased or legally incapacitated inventor):

City	State	Country
Columbia	SC	US

Mailing Address (except for a deceased or legally incapacitated inventor):

117 Park Shore Drv. East

City	State	Zip	Country
Columbia	SC	29223	US

I believe the above-named inventor or joint inventor to be the original inventor or an original joint inventor of a claimed invention in the application.

The above-identified application was made or authorized to be made by me.

I hereby acknowledge that any willful false statement made in this statement is punishable under 18 U.S.C. 1001 by fine or imprisonment of not more than five (5) years, or both.

Relationship to the inventor to whom this substitute statement applies:

- ☐ Legal Representative (for deceased or legally incapacitated inventor only),
- ☐ Assignee,
- ☒ Person to whom the inventor is under an obligation to assign,
- ☐ Person who otherwise shows a sufficient proprietary interest in the matter (petition under 37 CFR 1.46 is required), or
- ☐ Joint Inventor.

PTO/SB/AIA02 (07-13)
Approved for use through 01/31/2014. OMB 0651-0032
U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE

SUBSTITUTE STATEMENT

Circumstances permitting execution of this substitute statement:

- ☐ Inventor is deceased,
- ☐ Inventor is under legal incapacity,
- ☐ Inventor cannot be found or reached after diligent effort, or
- ☒ Inventor has refused to execute the oath or declaration under 37 CFR 1.63.

If there are joint inventors, please check the appropriate box below:

- ☒ An application data sheet under 37 CFR 1.76 (PTO/AIA/14 or equivalent) naming the entire inventive entity has been or is currently submitted.

OR

- ☐ An application data sheet under 37 CFR 1.76 (PTO/AIA/14 or equivalent) has not been submitted. Thus, a Substitute Statement Supplemental Sheet (PTO/AIA/11 or equivalent) naming the entire inventive entity and providing inventor information is attached. See 37 CFR 1.64(b).

WARNING:

Petitioner/applicant is cautioned to avoid submitting personal information in documents filed in a patent application that may contribute to identity theft. Personal information such as social security numbers, bank account numbers, or credit card numbers (other than a check or credit card authorization form PTO-2038 submitted for payment purposes) is never required by the USPTO to support a petition or an application. If this type of personal information is included in documents submitted to the USPTO, petitioners/applicants should consider redacting such personal information from the documents before submitting them to the USPTO. Petitioner/applicant is advised that the record of a patent application is available to the public after publication of the application (unless a non-publication request in compliance with 37 CFR 1.213(a) is made in the application) or issuance of a patent. Furthermore, the record from an abandoned application may also be available to the public if the application is referenced in a published application or an issued patent (see 37 CFR 1.14). Checks and credit card authorization forms PTO-2038 submitted for payment purposes are not retained in the application file and therefore are not publicly available.

PERSON EXECUTING THIS SUBSTITUTE STATEMENT:

Name: Michael Shur | Date (Optional):

Signature: / Michael Shur / | /

APPLICANT NAME AND TITLE OF PERSON EXECUTING THIS SUBSTITUTE STATEMENT:

If the applicant is a juristic entity, list the applicant name and the title of the signer:

Applicant Name: Sensor Electronic Technology, Inc.

Title of Person Executing This Substitute Statement: Vice President

The signer, whose title is supplied above, is authorized to act on behalf of the applicant.

Residence of the signer (unless provided in an application data sheet, PTO/AIA/14 or equivalent):

City Latham | State NY | Country US

Mailing Address of the signer (unless provided in an application data sheet, PTO/AIA/14 or equivalent)

10 Starboard Way

City Latham | State NY | Zip 12110 | Country US

Note: Use an additional PTO/AIA/02 form for each inventor who is deceased, legally incapacitated, cannot be found or reached after diligent effort, or has refused to execute the oath or declaration under 37 CFR 1.63.

Electronic Acknowledgement Receipt

EFS ID:	24996044
Application Number:	14984156
International Application Number:	
Confirmation Number:	5890
Title of Invention:	Semiconductor Structure with Inhomogeneous Regions
First Named Inventor/Applicant Name:	Maxim S. Shatalov
Customer Number:	11698
Filer:	John W LaBatt
Filer Authorized By:	
Attorney Docket Number:	SETI-0110-CIP-US
Receipt Date:	24-FEB-2016
Filing Date:	30-DEC-2015
Time Stamp:	15:01:13
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	no

File Listing:

Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1	Oath or Declaration filed	SETI-0110-CIP-US_DeclarationSigned.pdf	699818 bd6197875a4f9b2c7d068f25078693179ba1237e	no	7

Warnings:	
Information:	

2	Oath or Declaration filed	SETI-0110-CIP-US_SubstituteStatementALunev.pdf	184282 6c7c55c8b7e6976c0fd06c70d167f5eb2ccd8120	no	2

Warnings:	
Information:	
Total Files Size (in bytes):	884100

This Acknowledgement Receipt evidences receipt on the noted date by the USPTO of the indicated documents, characterized by the applicant, and including page counts, where applicable. It serves as evidence of receipt similar to a Post Card, as described in MPEP 503.

New Applications Under 35 U.S.C. 111

If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application.

National Stage of an International Application under 35 U.S.C. 371

If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.

New International Application Filed with the USPTO as a Receiving Office

If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.

UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NUMBER	FILING OR 371(C) DATE	FIRST NAMED APPLICANT	ATTY. DOCKET NO./TITLE
14/984,156	12/30/2015	Maxim S. Shatalov	SETI-0110-CIP-US

CONFIRMATION NO. 5890

11698
LaBatt, LLC (SET)
PO Box 630
Valatie, NY 12184

PUBLICATION NOTICE

OC000000082528353

Title: Semiconductor Structure with Inhomogeneous Regions

Publication No.US-2016-0118536-A1
Publication Date:04/28/2016

NOTICE OF PUBLICATION OF APPLICATION

The above-identified application will be electronically published as a patent application publication pursuant to 37 CFR 1.211, et seq. The patent application publication number and publication date are set forth above.

The publication may be accessed through the USPTO's publically available Searchable Databases via the Internet at www.uspto.gov. The direct link to access the publication is currently http://www.uspto.gov/patft/.

The publication process established by the Office does not provide for mailing a copy of the publication to applicant. A copy of the publication may be obtained from the Office upon payment of the appropriate fee set forth in 37 CFR 1.19(a)(1). Orders for copies of patent application publications are handled by the USPTO's Office of Public Records. The Office of Public Records can be reached by telephone at (703) 308-9726 or (800) 972-6382, by facsimile at (703) 305-8759, by mail addressed to the United States Patent and Trademark Office, Office of Public Records, Alexandria, VA 22313-1450 or via the Internet.

In addition, information on the status of the application, including the mailing date of Office actions and the dates of receipt of correspondence filed in the Office, may also be accessed via the Internet through the Patent Electronic Business Center at www.uspto.gov using the public side of the Patent Application Information and Retrieval (PAIR) system. The direct link to access this status information is currently http://pair.uspto.gov/. Prior to publication, such status information is confidential and may only be obtained by applicant using the private side of PAIR.

Further assistance in electronically accessing the publication, or about PAIR, is available by calling the Patent Electronic Business Center at 1-866-217-9197.

Office of Data Managment, Application Assistance Unit (571) 272-4000, or (571) 272-4200, or 1-888-786-0101

PTO/SB/08a (03-15)
Approved for use through 07/31/2016. OMB 0651-0031
U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE

INFORMATION DISCLOSURE STATEMENT BY APPLICANT

(Not for submission under 37 CFR 1.99)

Application Number	14984156
Filing Date	2015-12-30
First Named Inventor	Shatalov et al.
Art Unit	2811
Examiner Name	
Attorney Docket Number	SETI-0110-CIP-US

U.S.PATENTS Remove

Examiner Initial*	Cite No	Patent Number	Kind Code[1]	Issue Date	Name of Patentee or Applicant of cited Document	Pages,Columns,Lines where Relevant Passages or Relevant Figures Appear
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Examiner Initial*	Cite No	Publication Number	Kind Code[1]	Publication Date	Name of Patentee or Applicant of cited Document	Pages,Columns,Lines where Relevant Passages or Relevant Figures Appear
	1	20160197228	A1	2016-07-07	Shatalov et al.	

If you wish to add additional U.S. Published Application citation information please click the Add button. Add

FOREIGN PATENT DOCUMENTS Remove

Examiner Initial*	Cite No	Foreign Document Number[3]	Country Code[2] i	Kind Code[4]	Publication Date	Name of Patentee or Applicant of cited Document	Pages,Columns,Lines where Relevant Passages or Relevant Figures Appear	T[5]
	1							

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NON-PATENT LITERATURE DOCUMENTS Remove

Examiner Initials*	Cite No	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc), date, pages(s), volume-issue number(s), publisher, city and/or country where published.	T[5]

INFORMATION DISCLOSURE STATEMENT BY APPLICANT (Not for submission under 37 CFR 1.99)		
	Application Number	14984156
	Filing Date	2015-12-30
	First Named Inventor	Shatalov et al.
	Art Unit	2811
	Examiner Name	
	Attorney Docket Number	SETI-0110-CIP-US

	1		

If you wish to add additional non-patent literature document citation information please click the Add button Add

EXAMINER SIGNATURE

Examiner Signature		Date Considered	

*EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through a citation if not in conformance and not considered. Include copy of this form with next communication to applicant.

[1] See Kind Codes of USPTO Patent Documents at www.USPTO.GOV or MPEP 901.04. [2] Enter office that issued the document, by the two-letter code (WIPO Standard ST.3). [3] For Japanese patent documents, the indication of the year of the reign of the Emperor must precede the serial number of the patent document. [4] Kind of document by the appropriate symbols as indicated on the document under WIPO Standard ST.16 if possible. [5] Applicant is to place a check mark here if English language translation is attached.

INFORMATION DISCLOSURE STATEMENT BY APPLICANT (Not for submission under 37 CFR 1.99)		
	Application Number	14984156
	Filing Date	2015-12-30
	First Named Inventor	Shatalov et al.
	Art Unit	2811
	Examiner Name	
	Attorney Docket Number	SETI-0110-CIP-US

CERTIFICATION STATEMENT

Please see 37 CFR 1.97 and 1.98 to make the appropriate selection(s):

That each item of information contained in the information disclosure statement was first cited in any communication from a foreign patent office in a counterpart foreign application not more than three months prior to the filing of the information disclosure statement. See 37 CFR 1.97(e)(1).

OR

☐ That no item of information contained in the information disclosure statement was cited in a communication from a foreign patent office in a counterpart foreign application, and, to the knowledge of the person signing the certification after making reasonable inquiry, no item of information contained in the information disclosure statement was known to any individual designated in 37 CFR 1.56(c) more than three months prior to the filing of the information disclosure statement. See 37 CFR 1.97(e)(2).

See attached certification statement.

The fee set forth in 37 CFR 1.17 (p) has been submitted herewith.

☒ A certification statement is not submitted herewith.

SIGNATURE

A signature of the applicant or representative is required in accordance with CFR 1.33, 10.18. Please see CFR 1.4(d) for the form of the signature.

Signature	/Elaine C. Berlin/	Date (YYYY-MM-DD)	2016-07-25
Name/Print	Elaine C. Berlin	Registration Number	61194

This collection of information is required by 37 CFR 1.97 and 1.98. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 1 hour to complete, including gathering, preparing and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

Privacy Act Statement

The Privacy Act of 1974 (P.L. 93-579) requires that you be given certain information in connection with your submission of the attached form related to a patent application or patent. Accordingly, pursuant to the requirements of the Act, please be advised that: (1) the general authority for the collection of this information is 35 U.S.C. 2(b)(2); (2) furnishing of the information solicited is voluntary; and (3) the principal purpose for which the information is used by the U.S. Patent and Trademark Office is to process and/or examine your submission related to a patent application or patent. If you do not furnish the requested information, the U.S. Patent and Trademark Office may not be able to process and/or examine your submission, which may result in termination of proceedings or abandonment of the application or expiration of the patent.

The information provided by you in this form will be subject to the following routine uses:

1. The information on this form will be treated confidentially to the extent allowed under the Freedom of Information Act (5 U.S.C. 552) and the Privacy Act (5 U.S.C. 552a). Records from this system of records may be disclosed to the Department of Justice to determine whether the Freedom of Information Act requires disclosure of these record s.

2. A record from this system of records may be disclosed, as a routine use, in the course of presenting evidence to a court, magistrate, or administrative tribunal, including disclosures to opposing counsel in the course of settlement negotiations.

3. A record in this system of records may be disclosed, as a routine use, to a Member of Congress submitting a request involving an individual, to whom the record pertains, when the individual has requested assistance from the Member with respect to the subject matter of the record.

4. A record in this system of records may be disclosed, as a routine use, to a contractor of the Agency having need for the information in order to perform a contract. Recipients of information shall be required to comply with the requirements of the Privacy Act of 1974, as amended, pursuant to 5 U.S.C. 552a(m).

5. A record related to an International Application filed under the Patent Cooperation Treaty in this system of records may be disclosed, as a routine use, to the International Bureau of the World Intellectual Property Organization, pursuant to the Patent Cooperation Treaty.

6. A record in this system of records may be disclosed, as a routine use, to another federal agency for purposes of National Security review (35 U.S.C. 181) and for review pursuant to the Atomic Energy Act (42 U.S.C. 218(c)).

7. A record from this system of records may be disclosed, as a routine use, to the Administrator, General Services, or his/her designee, during an inspection of records conducted by GSA as part of that agency's responsibility to recommend improvements in records management practices and programs, under authority of 44 U.S.C. 2904 and 2906. Such disclosure shall be made in accordance with the GSA regulations governing inspection of records for this purpose, and any other relevant (i.e., GSA or Commerce) directive. Such disclosure shall not be used to make determinations about individuals.

8. A record from this system of records may be disclosed, as a routine use, to the public after either publication of the application pursuant to 35 U.S.C. 122(b) or issuance of a patent pursuant to 35 U.S.C. 151. Further, a record may be disclosed, subject to the limitations of 37 CFR 1.14, as a routine use, to the public if the record was filed in an application which became abandoned or in which the proceedings were terminated and which application is referenced by either a published application, an application open to public inspections or an issued patent.

9. A record from this system of records may be disclosed, as a routine use, to a Federal, State, or local law enforcement agency, if the USPTO becomes aware of a violation or potential violation of law or regulation.

Electronic Acknowledgement Receipt

EFS ID:	26445188
Application Number:	14984156
International Application Number:	
Confirmation Number:	5890
Title of Invention:	Semiconductor Structure with Inhomogeneous Regions
First Named Inventor/Applicant Name:	Maxim S. Shatalov
Customer Number:	11698
Filer:	Elaine Chi Berlin
Filer Authorized By:	
Attorney Docket Number:	SETI-0110-CIP-US
Receipt Date:	25-JUL-2016
Filing Date:	30-DEC-2015
Time Stamp:	15:24:14
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	no

File Listing:

Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1	Information Disclosure Statement (IDS) Form (SB08)	SETI-0110-CIP-US_IDS2.pdf	1034909 36072c33c2a8be1c3c403b5ca390f27bd7b3f69c	no	4

Warnings:

Information:	
Total Files Size (in bytes):	1034909

This Acknowledgement Receipt evidences receipt on the noted date by the USPTO of the indicated documents, characterized by the applicant, and including page counts, where applicable. It serves as evidence of receipt similar to a Post Card, as described in MPEP 503.

New Applications Under 35 U.S.C. 111

If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application.

National Stage of an International Application under 35 U.S.C. 371

If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.

New International Application Filed with the USPTO as a Receiving Office

If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.

UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
14/984,156	12/30/2015	Maxim S. Shatalov	SETI-0110-CIP-US	5890

11698 7590 02/08/2017

LaBatt, LLC (SET)
PO Box 630
Valatie, NY 12184

EXAMINER
ERDEM, FAZLI

ART UNIT	PAPER NUMBER
2826	

NOTIFICATION DATE	DELIVERY MODE
02/08/2017	ELECTRONIC

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

adobrinsky@s-et.com
national@labattlaw.com

Office Action Summary	Application No. 14/984,156	Applicant(s) SHATALOV ET AL.	
	Examiner FAZLI ERDEM	Art Unit 2826	AIA (First Inventor to File) Status Yes

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTHS FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *12/30/15*.

☐ A declaration(s)/affidavit(s) under **37 CFR 1.130(b)** was/were filed on _____.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ An election was made by the applicant in response to a restriction requirement set forth during the interview on _____; the restriction requirement and election have been incorporated into this action.

4)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims*

5)☒ Claim(s) *1-20* is/are pending in the application.

5a) Of the above claim(s) _____ is/are withdrawn from consideration.

6)☐ Claim(s) _____ is/are allowed.

7)☒ Claim(s) *1-20* is/are rejected.

8)☐ Claim(s) _____ is/are objected to.

9)☐ Claim(s) _____ are subject to restriction and/or election requirement.

* If any claims have been determined allowable, you may be eligible to benefit from the **Patent Prosecution Highway** program at a participating intellectual property office for the corresponding application. For more information, please see http://www.uspto.gov/patents/init_events/pph/index.jsp or send an inquiry to PPHfeedback@uspto.gov.

Application Papers

10)☐ The specification is objected to by the Examiner.

11)☒ The drawing(s) filed on *12/30/15* is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

Certified copies:

a)☐ All b)☐ Some** c)☐ None of the:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

** See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)

2) ☒ Information Disclosure Statement(s) (PTO/SB/08a and/or PTO/SB/08b) Paper No(s)/Mail Date *1/5/2016, 7/25/16*.

3) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .

4) ☐ Other: _____.

The present application, filed on or after March 16, 2013, is being examined under the first inventor to file provisions of the AIA.

DETAILED ACTION

Double Patenting

The nonstatutory double patenting rejection is based on a judicially created doctrine grounded in public policy (a policy reflected in the statute) so as to prevent the unjustified or improper timewise extension of the "right to exclude" granted by a patent and to prevent possible harassment by multiple assignees. A nonstatutory double patenting rejection is appropriate where the conflicting claims are not identical, but at least one examined application claim is not patentably distinct from the reference claim(s) because the examined application claim is either anticipated by, or would have been obvious over, the reference claim(s). See, e.g., *In re Berg*, 140 F.3d 1428, 46 USPQ2d 1226 (Fed. Cir. 1998); *In re Goodman*, 11 F.3d 1046, 29 USPQ2d 2010 (Fed. Cir. 1993); *In re Longi*, 759 F.2d 887, 225 USPQ 645 (Fed. Cir. 1985); *In re Van Ornum*, 686 F.2d 937, 214 USPQ 761 (CCPA 1982); *In re Vogel*, 422 F.2d 438, 164 USPQ 619 (CCPA 1970); *In re Thorington*, 418 F.2d 528, 163 USPQ 644 (CCPA 1969).

A timely filed terminal disclaimer in compliance with 37 CFR 1.321(c) or 1.321(d) may be used to overcome an actual or provisional rejection based on nonstatutory double patenting provided the reference application or patent either is shown to be commonly owned with the examined application, or claims an invention made as a result of activities undertaken within the scope of a joint research agreement. See MPEP § 717.02 for applications subject to examination under the first inventor to file

provisions of the AIA as explained in MPEP § 2159. See MPEP §§ 706.02(l)(1) - 706.02(l)(3) for applications not subject to examination under the first inventor to file provisions of the AIA. A terminal disclaimer must be signed in compliance with 37 CFR 1.321(b).

The USPTO Internet website contains terminal disclaimer forms which may be used. Please visit www.uspto.gov/patent/patents-forms. The filing date of the application in which the form is filed determines what form (e.g., PTO/SB/25, PTO/SB/26, PTO/AIA/25, or PTO/AIA/26) should be used. A web-based eTerminal Disclaimer may be filled out completely online using web-screens. An eTerminal Disclaimer that meets all requirements is auto-processed and approved immediately upon submission. For more information about eTerminal Disclaimers, refer to www.uspto.gov/patents/process/file/efs/guidance/eTD-info-I.jsp.

Claims 1-20 are rejected on the ground of nonstatutory double patenting as being unpatentable over claims 1-21 U.S. Patent No. 9,331,244. Although the claims at issue are not identical, they are not patentably distinct from each other because

They both disclose semiconductor heterostructure comprising group III nitride semiconductor layer with inhomogeneous regions (especially see Claim 9 of '244 in comparison to the Claim 4 of the instant application)

Claims 1-20 provisionally rejected on the ground of nonstatutory double patenting as being unpatentable over claims 1-20 of copending Application No. 15/225,403 (US2016/0336483). Although the claims at issue are not identical, they are not patentably distinct from each other because

They both disclose semiconductor heterostructure comprising group III nitride semiconductor layer with inhomogeneous regions (especially see Claim 1 of '244 in comparison to the Claim 1 of the instant application with respect to the “attributes” limitation)

This is a provisional nonstatutory double patenting rejection because the patentably indistinct claims have not in fact been patented.

DETAILED ACTION

Claim Rejections - 35 USC § 103

In the event the determination of the status of the application as subject to AIA 35 U.S.C. 102 and 103 (or as subject to pre-AIA 35 U.S.C. 102 and 103) is incorrect, any correction of the statutory basis for the rejection will not be considered a new ground of rejection if the prior art relied upon, and the rationale supporting the rejection, would be the same under either status.

The following is a quotation of 35 U.S.C. 103 which forms the basis for all obviousness rejections set forth in this Office action:

> A patent for a claimed invention may not be obtained, notwithstanding that the claimed invention is not identically disclosed as set forth in section 102, if the differences between the claimed invention and the prior art are such that the claimed invention as a whole would have been obvious before the effective filing date of the claimed invention to a person having ordinary skill in the art to which the claimed invention pertains. Patentability shall not be negated by the manner in which the invention was made.

Claims 1-7 are is/are rejected under 35 U.S.C. 103 as being unpatentable over Saxler (2013/0270514) in view of Jain et al. (2015/0372193).

Regarding Claim 1, in Fig. 6, Saxler et al. discloses a semiconductor heterostructure, comprising: an active region 24A/24B; a metallic contact 32/34; a group

III nitride semiconductor layer D1/D2/D3 located between the active region and the metallic contact, the semiconductor layer including a plurality of inhomogeneous regions12A/12B arranged within multiple levels of the semiconductor layer, wherein some of the inhomogeneous regions in a first level of the semiconductor layer are vertically offset from inhomogeneous regions in a second level of the semiconductor layer, and wherein the plurality of inhomogeneous regions include one or more of a set of transparent regions, a set of reflective regions and/or a set of conductive regions. Saxler fails to disclose the required limitation where each of the inhomogeneous regions having a set of attributes differing from a group III nitride material forming the semiconductor layer. However, Jain et al. discloses a patterned layer design for group III nitride layer growth where in paragraphs 0059, 0061, 0062, the required limitation of differing "attributes" is disclosed.

It would have been obvious to one of having ordinary skill in the art at the time of effective filing to have the required differing attributes limitation in Saxler as taught by Jain et al. in for stress reduction purposes.

Regarding Claim 2, in Fig. 6 of Saxler, each of the inhomogeneous regions in the first level and the second level of the semiconductor layer includes a set of reflective regions.

Regarding Claim 3, in Fig. 6 of Saxler, each of the plurality of inhomogeneous regions in the first level of the semiconductor layer extend into the metallic contact and each of the plurality of inhomogeneous regions in the second level of the semiconductor layer are located at an interface of the semiconductor layer.

Regarding Claim 4, in Fig. 6 of Saxler, all of the inhomogeneous regions in the first level of the semiconductor layer are staggered with the inhomogeneous regions in the second level of the semiconductor layer to form a checkerboard arrangement of the inhomogeneous regions within the semiconductor layer.

Regarding Claim 5, in Fig. 6 of Saxler, the inhomogeneous regions in the first level of the semiconductor layer each has a surface contacting the metallic contact, wherein at least one metal protrusion from the metallic contact extends into each inhomogeneous region.

Regarding Claim 6, in Fig. 6 of Saxler, each of the inhomogeneous regions in the first level of the semiconductor layer comprises a set of conductive regions and each of the inhomogeneous regions in the second level of the semiconductor layer comprises a set of reflective regions.

Regarding Claim 7, in Fig. 6 of Saxler, each of the inhomogeneous regions in the second level of the semiconductor layer has at least one metal protrusion extending from the metallic contact into the semiconductor layer that is directed to a surface of the inhomogeneous region without contact thereof.

Claims 8-10 are is/are rejected under 35 U.S.C. 103 as being unpatentable over Saxler (2013/0270514) in view of Saxler et al. (2004/0031956).

Regarding Claim 8, in Fig. 6, Saxler ‘514 discloes

fabricating a semiconductor heterostructure, wherein the semiconductor heterostructure comprises: an active region; a metallic contact; a group III nitride semiconductor layer located between the active region and the metallic contact, the

semiconductor layer including a plurality of inhomogeneous regions arranged within multiple levels of the semiconductor layer, wherein some of the inhomogeneous regions in a first level of the semiconductor layer are vertically offset from inhomogeneous regions in a second level of the semiconductor layer, and wherein the plurality of inhomogeneous regions include one or more of a set of transparent regions, a set of reflective regions and/or a set of conductive regions. Saxler ‘514 fails to disclose the required limitation where each of the inhomogeneous regions having a set of attributes differing from a group III nitride material forming the semiconductor layer. However, Saxler ‘956 heterogeneous bandgap structures wherein paragraphs 0019 and 0021, the required limitation of differing "attributes” is disclosed.

It would have been obvious to one of having ordinary skill in the art at the time of effective filing to have the required differing attributes limitation in Saxler ‘514 as taught by Saxler ‘956. in for stress reduction purposes.

Regarding Claim 9, in Saxler ‘514, the fabricating includes: epitaxially growing a portion of the group III nitride semiconductor layer; forming at least one of the sets of inhomogeneous regions on a surface of the portion of the group III nitride semiconductor layer; and epitaxially over-growing the group III nitride semiconductor layer after the forming.

Regarding Claim 10, in Saxler '514, forming includes: depositing the at least one of the sets of inhomogeneous regions using one of: thermal evaporation, magnetron sputtering, ion-beam deposition, or laser beam evaporation; and patterning the at least one of the sets of inhomogeneous regions using photolithography.

Claims 11-20 are rejected under 35 U.S.C. 103 as being unpatentable over Saxler (2013/0270514) in view of Jain et al. (2014/0134773).

Regarding Claim 11, in Fig. 6, Saxler discloses a semiconductor heterostructure, obtained through laser lift-off, having a first side and a second side, the semiconductor heterostructure including: a group III nitride semiconductor layer including a plurality of inhomogeneous regions, each inhomogeneous region having a set of attributes differing from a group III nitride material forming the semiconductor layer, wherein the plurality of inhomogeneous regions include: a set of first inhomogeneous regions configured based on radiation having a target wavelength, wherein the set of first inhomogeneous regions are at least one of: transparent to the radiation or reflective of the radiation; a lateral planar area of the semiconductor layer or a volume of the semiconductor layer, and wherein at least some of the sets of inhomogeneous regions do not fully overlap. Saxler et al. fails to disclose the limitation " a set of second inhomogeneous regions having a conductivity at least ten percent higher than a conductivity of the set of first inhomogeneous regions, wherein each of the sets of inhomogeneous regions occupy at least five percent". However, Jain et al discloses a pattern layer design for group III nitride layer growth where in paragraphs 0010 and 0036 the required limitation is disclosed.

It would have been obvious to one of having ordinary skill in the art at the time of effective filing to have the required percentage limitation in Saxler as taught by Jain et al. in for stress reduction purposes.

Regarding Claim 12, in Fig. 6 of Saxler comprising a first metallic contact having a plurality of connected metallic domains formed on the first side of the semiconductor heterostructure.

Regarding Claim 13, paragraphs 0045-0047 of Jain et al., further comprising a plurality of roughness elements formed on the first side of the semiconductor heterostructure.

Regarding Claim 14, Figs. 4 and 6 of Jain et al. disclose a plurality of metallic contact domains formed on the second side of the semiconductor heterostructure.

Regarding Claim 15, Fig. 6 of Saxler a plurality of reflective elements incorporated within the semiconductor heterostructure proximate a surface of the second side of the semiconductor heterostructure.

Regarding Claim 16, Fig. 6 of Saxler et al., the plurality of reflective elements comprise one of dielectrics, metallic reflective islands, Bragg mirrors and combinations thereof.

Regarding Claim 17, Fig. 6 of Saxler et al. discloses that the plurality of reflective elements comprise alternating layers of one of Hf203 and A1203, H203 and SiO2, and A1203 and SiO2.

Regarding Claim 18, Fig. 6 of Saxler et al. discloses a plurality of Bragg domains formed on the second side of the semiconductor heterostructure.

Regarding Claim 19, Figs 12-14 of Jain et al. disclose a second metallic contact having metallic domains formed on the second side of the semiconductor

heterostructure, each of the metallic domains separated from an adjacent metallic domain by a predetermined spacing.

Regarding Claim 20, paragraphs 0041 and 0042 of Jain et al. disclose a passivation layer formed on the second side of the semiconductor heterostructure and a plurality of disjoint domains interspersed within the passivation layer.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to FAZLI ERDEM whose telephone number is (571)272-1914. The examiner can normally be reached on M-F 8:00 - 5:00.

Examiner interviews are available via telephone, in-person, and video conferencing using a USPTO supplied web-based collaboration tool. To schedule an interview, applicant is encouraged to use the USPTO Automated Interview Request (AIR) at http://www.uspto.gov/interviewpractice.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Davienne Monbleau can be reached on 571-272-1945. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/FAZLI ERDEM/
Examiner, Art Unit 2826
2/2/2017

Notice of References Cited	Application/Control No. 14/984,156	Applicant(s)/Patent Under Reexamination SHATALOV ET AL.	
	Examiner FAZLI ERDEM	Art Unit 2826	Page 1 of 1

U.S. PATENT DOCUMENTS

*		Document Number Country Code-Number-Kind Code	Date MM-YYYY	Name	CPC Classification	US Classification
*	A	US-2004/0031956 A1	02-2004	Saxler, Adam William	H01L21/02378	257/14
*	B	US-2013/0270514 A1	10-2013	Saxler; Adam William	H01L33/08	257/13
*	C	US-9,331,244 B2	05-2016	Shatalov; Maxim S	H01L33/32	1/1
*	D	US-2014/0134773 A1	05-2014	Jain; Rakesh	H01L33/32	438/44
*	E	US-2015/0372193 A1	12-2015	Jain; Rakesh	H01L33/32	257/98
*	F	US-2014/0110754 A1	04-2014	Jain; Rakesh	H01L21/0237	257/190
*	G	US-2016/0336483 A1	11-2016	Shatalov; Maxim S.	H01L33/10	1/1
	H	US-				
	I	US-				
	J	US-				
	K	US-				
	L	US-				
	M	US-				

FOREIGN PATENT DOCUMENTS

*		Document Number Country Code-Number-Kind Code	Date MM-YYYY	Country	Name	CPC Classification
	N					
	O					
	P					
	Q					
	R					
	S					
	T					

NON-PATENT DOCUMENTS

*		Include as applicable: Author, Title Date, Publisher, Edition or Volume, Pertinent Pages)
	U	
	V	
	W	
	X	

*A copy of this reference is not being furnished with this Office action. (See MPEP § 707.05(a).)
Dates in MM-YYYY format are publication dates. Classifications may be US or foreign.

Index of Claims	Application/Control No.	Applicant(s)/Patent Under Reexamination
	14984156	SHATALOV ET AL.
	Examiner	**Art Unit**
	FAZLI ERDEM	2826

✓	Rejected	-	Cancelled	N	Non-Elected	A	Appeal
=	Allowed	÷	Restricted	I	Interference	O	Objected

☐ Claims renumbered in the same order as presented by applicant ☐ CPA ☐ T.D. ☐ R.1.47

CLAIM		DATE								
Final	Original	02/02/2017								
	1	✓								
	2	✓								
	3	✓								
	4	✓								
	5	✓								
	6	✓								
	7	✓								
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	15	✓								
	16	✓								
	17	✓								
	18	✓								
	19	✓								
	20	✓								

Search Notes	Application/Control No.	Applicant(s)/Patent Under Reexamination
	14984156	SHATALOV ET AL.
	Examiner	Art Unit
	FAZLI ERDEM	2826

CPC- SEARCHED		
Symbol	Date	Examiner
H01L33/10	2/2/2017	FE
H01L33/007	2/2/2017	FE
H01L33/32	2/2/2017	FE

CPC COMBINATION SETS - SEARCHED		
Symbol	Date	Examiner

US CLASSIFICATION SEARCHED			
Class	Subclass	Date	Examiner

SEARCH NOTES		
Search Notes	Date	Examiner
H01L33/10	2/2/2017	FE
H01L33/007	2/2/2017	FE
H01L33/32	2/2/2017	FE
Inventors are searched	2/2/2017	FE
Assignee is searched	2/2/2017	FE
CPC search limited with text is conducted	2/2/2017	FE
Searched 257/94 limited with text	2/2/2017	FE
EAST Search history is attached	2/2/2017	FE

INTERFERENCE SEARCH			
US Class/ CPC Symbol	US Subclass / CPC Group	Date	Examiner

Doc code: IDS
Doc description: Information Disclosure Statement (IDS) Filed

PTO/SB/08a (03-15)
Approved for use through 07/31/2016. OMB 0651-0031
U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE

INFORMATION DISCLOSURE STATEMENT BY APPLICANT

(Not for submission under 37 CFR 1.99)

Application Number	14984156
Filing Date	2015-12-30
First Named Inventor	Shatalov et al.
Art Unit	
Examiner Name	
Attorney Docket Number	SETI-0110-CIP-US

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Examiner Initial*	Cite No	Patent Number	Kind Code[1]	Issue Date	Name of Patentee or Applicant of cited Document	Pages,Columns,Lines where Relevant Passages or Relevant Figures Appear
	1	7812366	B1	2010-10-12	Sampath et al.	

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	1	20140016660	A1	2014-01-16	Lunev et al.	
	2	20130320352	A1	2013-12-05	Gaevski et al.	
	3	20130146907	A1	2013-06-13	Lunev et al.	
	4	20090272993	A1	2009-11-05	Cheong	

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Examiner Initial*	Cite No	Foreign Document Number[3]	Country Code[2] i	Kind Code[4]	Publication Date	Name of Patentee or Applicant of cited Document	Pages,Columns,Lines where Relevant Passages or Relevant Figures Appear	T[5]

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INFORMATION DISCLOSURE STATEMENT BY APPLICANT

(Not for submission under 37 CFR 1.99)

Application Number	14984156
Filing Date	2015-12-30
First Named Inventor	Shatalov et al.
Art Unit	
Examiner Name	
Attorney Docket Number	SETI-0110-CIP-US

	1	2013023197	WO	A2	2013-02-14	Sensor Electronic Technology, Inc.		

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Examiner Initials*	Cite No	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc), date, pages(s), volume-issue number(s), publisher, city and/or country where published.	T[5]
	1	SHATALOV, M. et al., "AlGaN Deep-Ultraviolet Light-Emitting Diodes with External Quantum Efficiency above 10%," Applied Physics Express, July 2012, 3 pages, Vol. 5, No. 8.	
	2	WHITE, S., Application No. 14/189,012, Attorney Docket No. SETI-0110-US, Notice of Allowance, 30 September 2015, 8 pages	
	3	WHITE, S., Application No. 14/189,012, Attorney Docket No. SETI-0110-US, Ex Parte Quayle, 24 September 2015, 17 pages	

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Examiner Signature	/FAZLI ERDEM/	Date Considered	02/02/2017

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[1] See Kind Codes of USPTO Patent Documents at www.USPTO.GOV or MPEP 901.04. [2] Enter office that issued the document, by the two-letter code (WIPO Standard ST.3). [3] For Japanese patent documents, the indication of the year of the reign of the Emperor must precede the serial number of the patent document. [4] Kind of document by the appropriate symbols as indicated on the document under WIPO Standard ST.16 if possible. [5] Applicant is to place a check mark here if English language translation is attached.

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Filing Date	2015-12-30
First Named Inventor	Shatalov et al.
Art Unit	
Examiner Name	
Attorney Docket Number	SETI-0110-CIP-US

CERTIFICATION STATEMENT

Please see 37 CFR 1.97 and 1.98 to make the appropriate selection(s):

That each item of information contained in the information disclosure statement was first cited in any communication from a foreign patent office in a counterpart foreign application not more than three months prior to the filing of the information disclosure statement. See 37 CFR 1.97(e)(1).

OR

☐ That no item of information contained in the information disclosure statement was cited in a communication from a foreign patent office in a counterpart foreign application, and, to the knowledge of the person signing the certification after making reasonable inquiry, no item of information contained in the information disclosure statement was known to any individual designated in 37 CFR 1.56(c) more than three months prior to the filing of the information disclosure statement. See 37 CFR 1.97(e)(2).

See attached certification statement.

The fee set forth in 37 CFR 1.17 (p) has been submitted herewith.

☒ A certification statement is not submitted herewith.

SIGNATURE

A signature of the applicant or representative is required in accordance with CFR 1.33, 10.18. Please see CFR 1.4(d) for the form of the signature.

Signature	/John W. LaBatt/	Date (YYYY-MM-DD)	2015-12-31
Name/Print	John W. LaBatt	Registration Number	48301

This collection of information is required by 37 CFR 1.97 and 1.98. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 1 hour to complete, including gathering, preparing and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

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The information provided by you in this form will be subject to the following routine uses:

1. The information on this form will be treated confidentially to the extent allowed under the Freedom of Information Act (5 U.S.C. 552) and the Privacy Act (5 U.S.C. 552a). Records from this system of records may be disclosed to the Department of Justice to determine whether the Freedom of Information Act requires disclosure of these record s.

2. A record from this system of records may be disclosed, as a routine use, in the course of presenting evidence to a court, magistrate, or administrative tribunal, including disclosures to opposing counsel in the course of settlement negotiations.

3. A record in this system of records may be disclosed, as a routine use, to a Member of Congress submitting a request involving an individual, to whom the record pertains, when the individual has requested assistance from the Member with respect to the subject matter of the record.

4. A record in this system of records may be disclosed, as a routine use, to a contractor of the Agency having need for the information in order to perform a contract. Recipients of information shall be required to comply with the requirements of the Privacy Act of 1974, as amended, pursuant to 5 U.S.C. 552a(m).

5. A record related to an International Application filed under the Patent Cooperation Treaty in this system of records may be disclosed, as a routine use, to the International Bureau of the World Intellectual Property Organization, pursuant to the Patent Cooperation Treaty.

6. A record in this system of records may be disclosed, as a routine use, to another federal agency for purposes of National Security review (35 U.S.C. 181) and for review pursuant to the Atomic Energy Act (42 U.S.C. 218(c)).

7. A record from this system of records may be disclosed, as a routine use, to the Administrator, General Services, or his/her designee, during an inspection of records conducted by GSA as part of that agency's responsibility to recommend improvements in records management practices and programs, under authority of 44 U.S.C. 2904 and 2906. Such disclosure shall be made in accordance with the GSA regulations governing inspection of records for this purpose, and any other relevant (i.e., GSA or Commerce) directive. Such disclosure shall not be used to make determinations about individuals.

8. A record from this system of records may be disclosed, as a routine use, to the public after either publication of the application pursuant to 35 U.S.C. 122(b) or issuance of a patent pursuant to 35 U.S.C. 151. Further, a record may be disclosed, subject to the limitations of 37 CFR 1.14, as a routine use, to the public if the record was filed in an application which became abandoned or in which the proceedings were terminated and which application is referenced by either a published application, an application open to public inspections or an issued patent.

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Doc code: IDS
Doc description: Information Disclosure Statement (IDS) Filed

PTO/SB/08a (03-15)
Approved for use through 07/31/2016. OMB 0651-0031
U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE

INFORMATION DISCLOSURE STATEMENT BY APPLICANT

(Not for submission under 37 CFR 1.99)

Application Number	14984156
Filing Date	2015-12-30
First Named Inventor	Shatalov et al.
Art Unit	2811
Examiner Name	
Attorney Docket Number	SETI-0110-CIP-US

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/F.E/	1	20160197228	A1	2016-07-07	Shatalov et al.	

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Examiner Initial*	Cite No	Foreign Document Number[3]	Country Code[2] i	Kind Code[4]	Publication Date	Name of Patentee or Applicant of cited Document	Pages,Columns,Lines where Relevant Passages or Relevant Figures Appear	T[5]
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Examiner Signature	/FAZLI ERDEM/	Date Considered	02/02/2017

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Signature	/Elaine C. Berlin/	Date (YYYY-MM-DD)	2016-07-25
Name/Print	Elaine C. Berlin	Registration Number	61194

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EAST Search History

EAST Search History (Prior Art)

Ref #	Hits	Search Query	DBs	Default Operator	Plurals	Time Stamp
L2	0	inhomeogeneous near region same (layer or level) same (offset or overlap or overlapping or overlapped or stagger or staggering or staggered or checkerboard or checker-board or checker near board) same transparent same reflective same conductive	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2017/02/02 13:03
L3	0	inhomeogeneous near region same (layer or level) same (offset or overlap or overlapping or overlapped or stagger or staggering or staggered or checkerboard or checker-board or checker near board) same (transparent or reflective or conductive)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2017/02/02 13:04
L4	10628	(inhomeogeneous near region or reflective or transparent or conductive) same (layer or level) same (offset or overlap or overlapping or overlapped or stagger or staggering or staggered or checkerboard or checker-board or checker near board) same (vertically or lateral or vertical or vertically)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2017/02/02 13:05
L5	14	group near III same (inhomeogeneous near region or reflective or transparent or conductive) same (layer or level) same (offset or overlap or overlapping or overlapped or stagger or staggering or staggered or checkerboard or checker-board or checker near board) same (vertically or lateral or vertical or vertically)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2017/02/02 13:05
L6	1	group near III same (inhomeogeneous near region or reflective or transparent or conductive) same (layer or level) same (offset or overlap or overlapping or overlapped or stagger or staggering or staggered or checkerboard or checker-board or checker near board) same (vertically or lateral or vertical or vertically) and offset near10 mask	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2017/02/02 13:08
L7	1	group near III same (inhomeogeneous near region or reflective or transparent or conductive) same (layer or level) same (offset or overlap or overlapping or overlapped or stagger or staggering or staggered or checkerboard or checker-board or checker near board) same (vertically or lateral or vertical or vertically) and offset near10 (mask or masking or masked)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2017/02/02 13:09
L8	5	group near III same (inhomeogeneous	US-PGPUB;	OR	ON	2017/02/02

		near region or reflective or transparent or conductive) same (layer or level) same (offset or overlap or overlapping or overlapped or stagger or staggering or staggered or checkerboard or checker-board or checker near board) same (vertically or lateral or vertical or vertically) and offset and (mask or masking or masked)	USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB			13:10
L9	1	group near III same (inhomeogeneous near region or reflective or transparent or conductive) same (layer or level) same (offset or overlap or overlapping or overlapped or stagger or staggering or staggered or checkerboard or checker-board or checker near board) same (vertically or lateral or vertical or vertically) and offset and (mask or masking or masked).clm.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2017/02/02 13:10
L10	16	group near III same (inhomeogeneous near region or reflective or transparent or conductive) same (layer or level) same (offset or overlap or overlapping or overlapped or stagger or staggering or staggered or checkerboard or checker-board or checker near board) same (vertically or lateral or laterally or vertical or vertically)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2017/02/02 13:11
L11	7	group near III same (inhomeogeneous near region or reflective or transparent or conductive) same (layer or level) same (offset or overlap or overlapping or overlapped or stagger or staggering or staggered or checkerboard or checker-board or checker near board) near10 (vertically or lateral or laterally or vertical or vertically)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2017/02/02 13:11
L12	122	(US-20160336483-$ or US-20160118536-$ or US-20150295133-$ or US-20170005224-$ or US-20160380150-$ or US-20160343901-$ or US-20140134773-$ or US-20160315449-$ or US-20160315219-$ or US-20160260867-$ or US-20160247885-$ or US-20160093771-$ or US-20140191261-$ or US-20140239312-$ or US-20160190387-$ or US-20160172544-$ or US-20140096669-$ or US-20160155902-$ or US-20160149099-$ or US-20160118535-$ or US-20160118534-$ or US-20160118531-$ or US-20160111618-$ or US-20160064631-$ or US-20130193409-$ or US-20160058020-$).did. or (US-20160049551-$ or US-20160035936-$ or US-20150297767-$ or US-20150255672-$ or US-20150228855-$ or US-20150179751-$ or US-20150165079-$ or US-20150108428-$ or US-20150091043-$ or US-20150083994-$ or US-20150069270-$ or US-20160197228-$ or US-20140346441-$ or US-20070081081-$ or US-20160211412-$ or US-20140110734-$ or US-20140158980-$ or	US-PGPUB; USPAT; USOCR; FPRS; EPO; DERWENT	OR	ON	2017/02/02 13:12

		US-20140064314-$ or US-20140016660-$ or US-20130320352-$ or US-20130146907-$ or US-20090272993-$ or US-20130277642-$ or US-20140110754-$ or US-20130193480-$ or US-20160225941-$ or US-20130055694-$).did. or (US-20130161305-$ or US-20070196682-$ or US-20150372193-$ or US-20160322535-$ or US-20130256828-$ or US-20080182403-$ or US-20070117348-$ or US-20030224591-$ or US-20140191284-$ or US-20140000693-$ or US-20080230815-$ or US-20130270514-$ or US-20110013656-$ or US-20100001375-$ or US-20020197830-$ or US-20120112188-$ or US-20120001220-$ or US-20110147791-$ or US-20020137249-$ or US-20140332374-$ or US-20140061057-$ or US-20040004215-$ or US-20070278518-$ or US-20070228416-$ or US-20130052463-$ or US-20100290675-$ or US-20160118490-$).did. or (US-20160111501-$ or US-20130240945-$).did. or (US-9331244-$ or US-9406840-$ or US-7812366-$ or US-9281441-$ or US-9312428-$ or US-4148132-$ or US-9105792-$ or US-9397260-$ or US-7361973-$ or US-7485516-$ or US-8293618-$ or US-7332795-$ or US-8886334-$ or US-8097926-$ or US-8372726-$ or US-4990989-$ or US-4894703-$).did. or (US-3351698-$).did. or (WO-2014179523-$ or WO-2013126828-$ or WO-2015175369-$ or CN-104979440-$ or KR-20150041557-$ or KR-20160025069-$ or KR-20140110754-$ or KR-20100012827-$ or KR-20000003968-$ or WO-2009005227-$).did. or (WO-2009005227-$).did. or (US-20160197228-$ or US-20160118536-$ or WO-2013082592-$ or US-20140239312-$ or US-20160336483-$ or US-20120217496-$ or WO-2012000114-$ or US-20110315956-$ or WO-2010048537-$).did.				
L13	21	l12 and (epi or epitaxy or epitaxial or epitaxially) near10 overgrowth	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2017/02/02 13:13
L14	13	l12 and ((epi or epitaxy or epitaxial or epitaxially) near10 overgrowth or elo) and (lateral or laterally or vertical or vertically) near10 (offset or stagger or staggering or staggered or overlap or overlapping or overlapped or checkerboard or checker-board or checker near board)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2017/02/02 13:14
L15	3	l12 and ((epi or epitaxy or epitaxial or epitaxially) near10 overgrowth or elo)	US-PGPUB; USPAT;	OR	ON	2017/02/02 13:15

		and (lateral or laterally or vertical or vertically) near10 (offset or stagger or staggering or staggered or overlap or overlapping or overlapped or checkerboard or checker-board or checker near board) and lift near off	USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB			
L16	10	l12 and ((epi or epitaxy or epitaxial or epitaxially) near10 overgrowth or elo) and (lateral or laterally or vertical or vertically) near10 (offset or stagger or staggering or staggered or overlap or overlapping or overlapped or checkerboard or checker-board or checker near board) near10 (layer or level)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2017/02/02 13:15
L17	1	l12 and ((epi or epitaxy or epitaxial or epitaxially) or elo) same (lateral or laterally or vertical or vertically) near10 (offset or stagger or staggering or staggered or overlap or overlapping or overlapped or checkerboard or checker-board or checker near board) near10 (layer or level)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2017/02/02 13:17
L18	0	l12 and type near III same ((epi or epitaxy or epitaxial or epitaxially) or elo) same (lateral or laterally or vertical or vertically) near10 (offset or stagger or staggering or staggered or overlap or overlapping or overlapped or checkerboard or checker-board or checker near board) near10 (layer or level)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2017/02/02 13:17
L19	0	type near III same ((epi or epitaxy or epitaxial or epitaxially) or elo) same (lateral or laterally or vertical or vertically) near10 (offset or stagger or staggering or staggered or overlap or overlapping or overlapped or checkerboard or checker-board or checker near board) near10 (layer or level)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2017/02/02 13:17
L20	0	type near III same (lateral or laterally or vertical or vertically) near10 (offset or stagger or staggering or staggered or overlap or overlapping or overlapped or checkerboard or checker-board or checker near board) near10 (layer or level)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2017/02/02 13:17
L21	29	group near III same (lateral or laterally or vertical or vertically) near10 (offset or stagger or staggering or staggered or overlap or overlapping or overlapped or checkerboard or checker-board or checker near board) near10 (layer or level)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2017/02/02 13:18
L22	2	heterostructure same group near III same (lateral or laterally or vertical or vertically) near10 (offset or stagger or staggering or staggered or overlap or overlapping or overlapped or checkerboard or checker-board or checker near board) near10 (layer or	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2017/02/02 13:19

		level)				
L23	2	heterostructure same group near III same (lateral or laterally or vertical or vertically) near10 (offset or stagger or staggering or staggered or overlap or overlapping or overlapped or checkerboard or checker-board or checker near board) near10 (layer or level) same (transparent or reflective or conductive)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2017/02/02 13:20
L24	5	group near III same (lateral or laterally or vertical or vertically) near10 (offset or stagger or staggering or staggered or overlap or overlapping or overlapped or checkerboard or checker-board or checker near board) near10 (layer or level) same (transparent or reflective or conductive)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2017/02/02 13:20
L25	123	(US-20160336483-$ or US-20160118536-$ or US-20150295133-$ or US-20170005224-$ or US-20160380150-$ or US-20160343901-$ or US-20140134773-$ or US-20160315449-$ or US-20160315219-$ or US-20160260867-$ or US-20160247885-$ or US-20160093771-$ or US-20140191261-$ or US-20140239312-$ or US-20160190387-$ or US-20160172544-$ or US-20140096669-$ or US-20160155902-$ or US-20160149099-$ or US-20160118535-$ or US-20160118534-$ or US-20160118531-$ or US-20160111618-$ or US-20160064631-$ or US-20130193409-$ or US-20160058020-$).did. or (US-20160049551-$ or US-20160035936-$ or US-20150297767-$ or US-20150255672-$ or US-20150228855-$ or US-20150179751-$ or US-20150165079-$ or US-20150108428-$ or US-20150091043-$ or US-20150083994-$ or US-20150069270-$ or US-20160197228-$ or US-20140346441-$ or US-20070081081-$ or US-20160211412-$ or US-20140110734-$ or US-20140158980-$ or US-20140064314-$ or US-20140016660-$ or US-20130320352-$ or US-20130146907-$ or US-20090272993-$ or US-20130277642-$ or US-20140110754-$ or US-20130193480-$ or US-20160225941-$ or US-20130055694-$).did. or (US-20130161305-$ or US-20070196682-$ or US-20150372193-$ or US-20160322535-$ or US-20130256828-$ or US-20080182403-$ or US-20070117348-$ or US-20030224591-$ or US-20140191284-$ or US-20140000693-$ or US-20080230815-$ or US-20130270514-$ or US-20110013656-$ or US-20100001375-$ or US-20020197830-$ or US-20120112188-$ or US-20120001220-$ or US-20110147791-$ or US-20020137249-$ or US-20140332374-$ or US-20140061057-$ or US-	US-PGPUB; USPAT; USOCR; FPRS; EPO; DERWENT	OR	ON	2017/02/02 13:27

		20040004215-$ or US-20070278518-$ or US-20070228416-$ or US-20130052463-$ or US-20100290675-$ or US-20160118490-$).did. or (US-20160111501-$ or US-20130240945-$ or US-20040159843-$).did. or (US-9331244-$ or US-9406840-$ or US-7812366-$ or US-9281441-$ or US-9312428-$ or US-4148132-$ or US-9105792-$ or US-9397260-$ or US-7361973-$ or US-7485516-$ or US-8293618-$ or US-7332795-$ or US-8886334-$ or US-8097926-$ or US-8372726-$ or US-4990989-$ or US-4894703-$).did. or (US-3351698-$).did. or (WO-2014179523-$ or WO-2013126828-$ or WO-2015175369-$ or CN-104979440-$ or KR-20150041557-$ or KR-20160025069-$ or KR-20140110754-$ or KR-20100012827-$ or KR-20000003968-$ or WO-2009005227-$).did. or (WO-2009005227-$).did. or (US-20160197228-$ or US-20160118536-$ or WO-2013082592-$ or US-20140239312-$ or US-20160336483-$ or US-20120217496-$ or WO-2012000114-$ or US-20110315956-$ or WO-2010048537-$).did.				
L26	45	l25 and attribute	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2017/02/02 13:27
L27	8	l25 and different near2 attribute	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2017/02/02 13:28
L28	17	l25 and (differ or differing or different) near5 attribute	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2017/02/02 13:29
L29	34087	(elo or ((epi or epitaxy or epitaxial) near5 (lateral or laterally) near5 overgrowth))	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2017/02/02 13:32
L30	190	(elo or ((epi or epitaxy or epitaxial) near5 (lateral or laterally) near5 overgrowth)) same (mask or masking or masked or pattern or patterning or patterned) same group near III	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT;	OR	ON	2017/02/02 13:33

			IBM_TDB			
L31	17	(elo or ((epi or epitaxy or epitaxial) near5 (lateral or laterally) near5 overgrowth)) same (mask or masking or masked or pattern or patterning or patterned) same group near III and (offset or stagger or staggering or staggered or checkerboard or checker near board) near10 (layer or level)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2017/02/02 13:33
L32	84	group near III.clm. and (offset or stagger or staggering or staggered or checkerboard or checker near board) near10 (layer or level).clm.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2017/02/02 13:34
L33	127	(US-20160336483-$ or US-20160118536-$ or US-20150295133-$ or US-20170005224-$ or US-20160380150-$ or US-20160343901-$ or US-20140134773-$ or US-20160315449-$ or US-20160315219-$ or US-20160260867-$ or US-20160247885-$ or US-20160093771-$ or US-20140191261-$ or US-20140239312-$ or US-20160190387-$ or US-20160172544-$ or US-20140096669-$ or US-20160155902-$ or US-20160149099-$ or US-20160118535-$ or US-20160118534-$ or US-20160118531-$ or US-20160111618-$ or US-20160064631-$ or US-20130193409-$ or US-20160058020-$).did. or (US-20160049551-$ or US-20160035936-$ or US-20150297767-$ or US-20150255672-$ or US-20150228855-$ or US-20150179751-$ or US-20150165079-$ or US-20150108428-$ or US-20150091043-$ or US-20150083994-$ or US-20150069270-$ or US-20160197228-$ or US-20140346441-$ or US-20070081081-$ or US-20160211412-$ or US-20140110734-$ or US-20140158980-$ or US-20140064314-$ or US-20140016660-$ or US-20130320352-$ or US-20130146907-$ or US-20090272993-$ or US-20130277642-$ or US-20140110754-$ or US-20130193480-$ or US-20160225941-$ or US-20130055694-$).did. or (US-20130161305-$ or US-20070196682-$ or US-20150372193-$ or US-20160322535-$ or US-20130256828-$ or US-20080182403-$ or US-20070117348-$ or US-20030224591-$ or US-20140191284-$ or US-20140000693-$ or US-20080230815-$ or US-20130270514-$ or US-20110013656-$ or US-20100001375-$ or US-20020197830-$ or US-20120112188-$ or US-20120001220-$ or US-20110147791-$ or US-20020137249-$ or US-20140332374-$ or US-20140061057-$ or US-20040004215-$ or US-20070278518-$ or US-20070228416-$ or US-20130052463-	US-PGPUB; USPAT; USOCR; FPRS; EPO; DERWENT	OR	ON	2017/02/02 13:36

		$ or US-20100290675-$ or US-20160118490-$).did. or (US-20160111501-$ or US-20130240945-$ or US-20040159843-$ or US-20090180505-$ or US-20110005570-$ or US-20080150085-$ or US-20060267043-$).did. or (US-9331244-$ or US-9406840-$ or US-7812366-$ or US-9281441-$ or US-9312428-$ or US-4148132-$ or US-9105792-$ or US-9397260-$ or US-7361973-$ or US-7485516-$ or US-8293618-$ or US-7332795-$ or US-8886334-$ or US-8097926-$ or US-8372726-$ or US-4990989-$ or US-4894703-$).did. or (US-3351698-$).did. or (WO-2014179523-$ or WO-2013126828-$ or WO-2015175369-$ or CN-104979440-$ or KR-20150041557-$ or KR-20160025069-$ or KR-20140110754-$ or KR-20100012827-$ or KR-20000003968-$ or WO-2009005227-$).did. or (WO-2009005227-$).did. or (US-20160197228-$ or US-20160118536-$ or WO-2013082592-$ or US-20140239312-$ or US-20160336483-$ or US-20120217496-$ or WO-2012000114-$ or US-20110315956-$ or WO-2010048537-$).did.				
L34	67	l33 and heterostructure	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2017/02/02 13:36
L35	41	l33 and heterostructure and bragg	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2017/02/02 13:37
L36	21	l33 and heterostructure and bragg and offset	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2017/02/02 13:38
L37	7	l33 and heterostructure and bragg and offset near10 (laterall or vertically or vertical or lateral).clm.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2017/02/02 13:39
L38	8	l33 and heterostructure and bragg and offset near10 (laterall or vertically or vertical or lateral or horizontal or horizontally).clm.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT;	OR	ON	2017/02/02 13:39

			IBM_TDB			
L39	17	heterostructure and bragg and offset near10 (laterall or vertically or vertical or lateral or horizontal or horizontally).clm.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2017/02/02 13:40
L40	10	heterostructure and bragg and offset near10 (laterall or vertically or vertical or lateral or horizontal or horizontally).clm. and group near III.clm.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2017/02/02 13:40
L41	2	heterostructure and bragg and offset near10 (laterall or vertically or vertical or lateral or horizontal or horizontally).clm. and group near III.clm. and (transparent or reflective or conductive).clm.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2017/02/02 13:40
L42	1156	maxim near2 shatalov.in. or alexander near2 dobrinsky.in. or alexander near2 lunev.in. or rakesh near2 jain.in. or jinwei near2 yang.in. or michael near2 shur.in. or ramigijus near2 gaska.in.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2017/02/02 13:42
L43	316	l42 and heterostructure	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2017/02/02 13:43
L44	232	l43 and group near III	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2017/02/02 13:43
L45	7	l44 and (offset near5 (lateral or laterally or vertical or vertically or horizontal or horizontally)).clm.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2017/02/02 13:43
L46	1156	maxim near2 shatalov.in. or alexander near2 dobrinsky.in. or alexander near2 lunev.in. or rakesh near2 jain.in. or jinwei near2 yang.in. or michael near2 shur.in. or remigijus near2 gaska.in.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2017/02/02 13:46
L47	7	l46 and (offset near5 (lateral or laterally or vertical or vertically or horizontal or horizontally)).clm.	US-PGPUB; USPAT; USOCR; FPRS;	OR	ON	2017/02/02 13:46

			EPO; JPO; DERWENT; IBM_TDB			
L48	142426	sensor near2 electronic	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2017/02/02 13:46
L49	795	sensor near2 electronic.as. or sensor near2 electronic.aanm.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2017/02/02 13:46
L50	7	l49 and (offset near5 (lateral or laterally or vertical or vertically or horizontal or horizontally)).clm.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2017/02/02 13:47
L51	3935	257/94.ccls.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2017/02/02 13:47
L52	2	l51 and (offset near5 (lateral or laterally or vertical or vertically or horizontal or horizontally)).clm.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2017/02/02 13:47
L53	0	l51 and group near III.clm. and (offset near5 (lateral or laterally or vertical or vertically or horizontal or horizontally)).clm.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2017/02/02 13:47
L54	20432	H01L33/07.cpc. or H01L33/10.cpc. or H01L33/32.cpc.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2017/02/02 13:48
L55	8	l54 and group near III.clm. and (offset near5 (lateral or laterally or vertical or vertically or horizontal or horizontally)).clm.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2017/02/02 13:48
L56	27655	H01L33/007.cpc. or H01L33/10.cpc. or H01L33/32.cpc.	US-PGPUB; USPAT;	OR	ON	2017/02/02 13:48

			USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB			
L57	8	l56 and group near III.clm. and (offset near5 (lateral or laterally or vertical or vertically or horizontal or horizontally)).clm.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2017/02/02 13:48
L58	0	l56 and group near III.clm. and (offset near5 (lateral or laterally or vertical or vertically or horizontal or horizontally)).clm. and lif near off	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2017/02/02 13:49
L59	1	l56 and group near III.clm. and (offset near5 (lateral or laterally or vertical or vertically or horizontal or horizontally)).clm. and lift near off	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2017/02/02 13:49
L60	4	group near III.clm. and (offset near5 (lateral or laterally or vertical or vertically or horizontal or horizontally)).clm. and lift near off	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2017/02/02 13:49
L61	12	group near III and (offset near5 (lateral or laterally or vertical or vertically or horizontal or horizontally)).clm. and lift near off	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2017/02/02 13:49
L62	14	group near III and (offset near10 (lateral or laterally or vertical or vertically or horizontal or horizontally)).clm. and lift near off	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2017/02/02 13:50
L63	139	group near III and (offset near10 (lateral or laterally or vertical or vertically or horizontal or horizontally)).clm.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2017/02/02 13:50
L64	24	group near III and (offset near10 (lateral or laterally or vertical or vertically or horizontal or horizontally)).clm. and heterostructure	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2017/02/02 13:50

L65	16	group near III and (offset near10 (lateral or laterally or vertical or vertically or horizontal or horizontally)).clm. and heterostructure and (reflective or transparent)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2017/02/02 13:51
L66	1	group near III and (offset near10 (lateral or laterally or vertical or vertically or horizontal or horizontally)).clm. and heterostructure and (reflective or transparent) and (liftoff or lift-off or lift near off)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2017/02/02 13:52
L67	2	group near III and (offset near10 (lateral or laterally or vertical or vertically or horizontal or horizontally)).clm. and heterostructure and (reflective or transparent) and (elo or liftoff or lift-off or lift near off)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2017/02/02 13:53
L68	6	group near III and (offset near10 (lateral or laterally or vertical or vertically or horizontal or horizontally)) and (elo or overgrowth or over-growth) and heterostructure and (reflective or transparent) and (liftoff or lift-off or lift near off)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2017/02/02 13:53

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EAST Search History

EAST Search History (Prior Art)

Ref #	Hits	Search Query	DBs	Default Operator	Plurals	Time Stamp
L2	0	inhomeogeneous near region same (layer or level) same (offset or overlap or overlapping or overlapped or stagger or staggering or staggered or checkerboard or checker-board or checker near board) same transparent same reflective same conductive	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2017/02/02 13:03
L3	0	inhomeogeneous near region same (layer or level) same (offset or overlap or overlapping or overlapped or stagger or staggering or staggered or checkerboard or checker-board or checker near board) same (transparent or reflective or conductive)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2017/02/02 13:04
L4	10628	(inhomeogeneous near region or reflective or transparent or conductive) same (layer or level) same (offset or overlap or overlapping or overlapped or stagger or staggering or staggered or checkerboard or checker-board or checker near board) same (vertically or lateral or vertical or vertically)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2017/02/02 13:05
L5	14	group near III same (inhomeogeneous near region or reflective or transparent or conductive) same (layer or level) same (offset or overlap or overlapping or overlapped or stagger or staggering or staggered or checkerboard or checker-board or checker near board) same (vertically or lateral or vertical or vertically)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2017/02/02 13:05
L6	1	group near III same (inhomeogeneous near region or reflective or transparent or conductive) same (layer or level) same (offset or overlap or overlapping or overlapped or stagger or staggering or staggered or checkerboard or checker-board or checker near board) same (vertically or lateral or vertical or vertically) and offset near10 mask	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2017/02/02 13:08
L7	1	group near III same (inhomeogeneous near region or reflective or transparent or conductive) same (layer or level) same (offset or overlap or overlapping or overlapped or stagger or staggering or staggered or checkerboard or checker-board or checker near board) same (vertically or lateral or vertical or vertically) and offset near10 (mask or masking or masked)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2017/02/02 13:09
L8	5	group near III same (inhomeogeneous	US-PGPUB;	OR	ON	2017/02/02

		near region or reflective or transparent or conductive) same (layer or level) same (offset or overlap or overlapping or overlapped or stagger or staggering or staggered or checkerboard or checker-board or checker near board) same (vertically or lateral or vertical or vertically) and offset and (mask or masking or masked)	USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB			13:10
L9	1	group near III same (inhomeogeneous near region or reflective or transparent or conductive) same (layer or level) same (offset or overlap or overlapping or overlapped or stagger or staggering or staggered or checkerboard or checker-board or checker near board) same (vertically or lateral or vertical or vertically) and offset and (mask or masking or masked).clm.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2017/02/02 13:10
L10	16	group near III same (inhomeogeneous near region or reflective or transparent or conductive) same (layer or level) same (offset or overlap or overlapping or overlapped or stagger or staggering or staggered or checkerboard or checker-board or checker near board) same (vertically or lateral or laterally or vertical or vertically)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2017/02/02 13:11
L11	7	group near III same (inhomeogeneous near region or reflective or transparent or conductive) same (layer or level) same (offset or overlap or overlapping or overlapped or stagger or staggering or staggered or checkerboard or checker-board or checker near board) near10 (vertically or lateral or laterally or vertical or vertically)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2017/02/02 13:11
L12	122	(US-20160336483-$ or US-20160118536-$ or US-20150295133-$ or US-20170005224-$ or US-20160380150-$ or US-20160343901-$ or US-20140134773-$ or US-20160315449-$ or US-20160315219-$ or US-20160260867-$ or US-20160247885-$ or US-20160093771-$ or US-20140191261-$ or US-20140239312-$ or US-20160190387-$ or US-20160172544-$ or US-20140096669-$ or US-20160155902-$ or US-20160149099-$ or US-20160118535-$ or US-20160118534-$ or US-20160118531-$ or US-20160111618-$ or US-20160064631-$ or US-20130193409-$ or US-20160058020-$).did. or (US-20160049551-$ or US-20160035936-$ or US-20150297767-$ or US-20150255672-$ or US-20150228855-$ or US-20150179751-$ or US-20150165079-$ or US-20150108428-$ or US-20150091043-$ or US-20150083994-$ or US-20150069270-$ or US-20160197228-$ or US-20140346441-$ or US-20070081081-$ or US-20160211412-$ or US-20140110734-$ or US-20140158980-$ or	US-PGPUB; USPAT; USOCR; FPRS; EPO; DERWENT	OR	ON	2017/02/02 13:12

		US-20140064314-$ or US-20140016660-$ or US-20130320352-$ or US-20130146907-$ or US-20090272993-$ or US-20130277642-$ or US-20140110754-$ or US-20130193480-$ or US-20160225941-$ or US-20130055694-$).did. or (US-20130161305-$ or US-20070196682-$ or US-20150372193-$ or US-20160322535-$ or US-20130256828-$ or US-20080182403-$ or US-20070117348-$ or US-20030224591-$ or US-20140191284-$ or US-20140000693-$ or US-20080230815-$ or US-20130270514-$ or US-20110013656-$ or US-20100001375-$ or US-20020197830-$ or US-20120112188-$ or US-20120001220-$ or US-20110147791-$ or US-20020137249-$ or US-20140332374-$ or US-20140061057-$ or US-20040004215-$ or US-20070278518-$ or US-20070228416-$ or US-20130052463-$ or US-20100290675-$ or US-20160118490-$).did. or (US-20160111501-$ or US-20130240945-$).did. or (US-9331244-$ or US-9406840-$ or US-7812366-$ or US-9281441-$ or US-9312428-$ or US-4148132-$ or US-9105792-$ or US-9397260-$ or US-7361973-$ or US-7485516-$ or US-8293618-$ or US-7332795-$ or US-8886334-$ or US-8097926-$ or US-8372726-$ or US-4990989-$ or US-4894703-$).did. or (US-3351698-$).did. or (WO-2014179523-$ or WO-2013126828-$ or WO-2015175369-$ or CN-104979440-$ or KR-20150041557-$ or KR-20160025069-$ or KR-20140110754-$ or KR-20100012827-$ or KR-20000003968-$ or WO-2009005227-$).did. or (WO-2009005227-$).did. or (US-20160197228-$ or US-20160118536-$ or WO-2013082592-$ or US-20140239312-$ or US-20160336483-$ or US-20120217496-$ or WO-2012000114-$ or US-20110315956-$ or WO-2010048537-$).did.				
L13	21	l12 and (epi or epitaxy or epitaxial or epitaxially) near10 overgrowth	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2017/02/02 13:13
L14	13	l12 and ((epi or epitaxy or epitaxial or epitaxially) near10 overgrowth or elo) and (lateral or laterally or vertical or vertically) near10 (offset or stagger or staggering or staggered or overlap or overlapping or overlapped or checkerboard or checker-board or checker near board)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2017/02/02 13:14
L15	3	l12 and ((epi or epitaxy or epitaxial or epitaxially) near10 overgrowth or elo)	US-PGPUB; USPAT;	OR	ON	2017/02/02 13:15

		and (lateral or laterally or vertical or vertically) near10 (offset or stagger or staggering or staggered or overlap or overlapping or overlapped or checkerboard or checker-board or checker near board) and lift near off	USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB			
L16	10	l12 and ((epi or epitaxy or epitaxial or epitaxially) near10 overgrowth or elo) and (lateral or laterally or vertical or vertically) near10 (offset or stagger or staggering or staggered or overlap or overlapping or overlapped or checkerboard or checker-board or checker near board) near10 (layer or level)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2017/02/02 13:15
L17	1	l12 and ((epi or epitaxy or epitaxial or epitaxially) or elo) same (lateral or laterally or vertical or vertically) near10 (offset or stagger or staggering or staggered or overlap or overlapping or overlapped or checkerboard or checker-board or checker near board) near10 (layer or level)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2017/02/02 13:17
L18	0	l12 and type near III same ((epi or epitaxy or epitaxial or epitaxially) or elo) same (lateral or laterally or vertical or vertically) near10 (offset or stagger or staggering or staggered or overlap or overlapping or overlapped or checkerboard or checker-board or checker near board) near10 (layer or level)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2017/02/02 13:17
L19	0	type near III same ((epi or epitaxy or epitaxial or epitaxially) or elo) same (lateral or laterally or vertical or vertically) near10 (offset or stagger or staggering or staggered or overlap or overlapping or overlapped or checkerboard or checker-board or checker near board) near10 (layer or level)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2017/02/02 13:17
L20	0	type near III same (lateral or laterally or vertical or vertically) near10 (offset or stagger or staggering or staggered or overlap or overlapping or overlapped or checkerboard or checker-board or checker near board) near10 (layer or level)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2017/02/02 13:17
L21	29	group near III same (lateral or laterally or vertical or vertically) near10 (offset or stagger or staggering or staggered or overlap or overlapping or overlapped or checkerboard or checker-board or checker near board) near10 (layer or level)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2017/02/02 13:18
L22	2	heterostructure same group near III same (lateral or laterally or vertical or vertically) near10 (offset or stagger or staggering or staggered or overlap or overlapping or overlapped or checkerboard or checker-board or checker near board) near10 (layer or	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2017/02/02 13:19

		level)				
L23	2	heterostructure same group near III same (lateral or laterally or vertical or vertically) near10 (offset or stagger or staggering or staggered or overlap or overlapping or overlapped or checkerboard or checker-board or checker near board) near10 (layer or level) same (transparent or reflective or conductive)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2017/02/02 13:20
L24	5	group near III same (lateral or laterally or vertical or vertically) near10 (offset or stagger or staggering or staggered or overlap or overlapping or overlapped or checkerboard or checker-board or checker near board) near10 (layer or level) same (transparent or reflective or conductive)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2017/02/02 13:20
L25	123	(US-20160336483-$ or US-20160118536-$ or US-20150295133-$ or US-20170005224-$ or US-20160380150-$ or US-20160343901-$ or US-20140134773-$ or US-20160315449-$ or US-20160315219-$ or US-20160260867-$ or US-20160247885-$ or US-20160093771-$ or US-20140191261-$ or US-20140239312-$ or US-20160190387-$ or US-20160172544-$ or US-20140096669-$ or US-20160155902-$ or US-20160149099-$ or US-20160118535-$ or US-20160118534-$ or US-20160118531-$ or US-20160111618-$ or US-20160064631-$ or US-20130193409-$ or US-20160058020-$).did. or (US-20160049551-$ or US-20160035936-$ or US-20150297767-$ or US-20150255672-$ or US-20150228855-$ or US-20150179751-$ or US-20150165079-$ or US-20150108428-$ or US-20150091043-$ or US-20150083994-$ or US-20150069270-$ or US-20160197228-$ or US-20140346441-$ or US-20070081081-$ or US-20160211412-$ or US-20140110734-$ or US-20140158980-$ or US-20140064314-$ or US-20140016660-$ or US-20130320352-$ or US-20130146907-$ or US-20090272993-$ or US-20130277642-$ or US-20140110754-$ or US-20130193480-$ or US-20160225941-$ or US-20130055694-$).did. or (US-20130161305-$ or US-20070196682-$ or US-20150372193-$ or US-20160322535-$ or US-20130256828-$ or US-20080182403-$ or US-20070117348-$ or US-20030224591-$ or US-20140191284-$ or US-20140000693-$ or US-20080230815-$ or US-20130270514-$ or US-20110013656-$ or US-20100001375-$ or US-20020197830-$ or US-20120112188-$ or US-20120001220-$ or US-20110147791-$ or US-20020137249-$ or US-20140332374-$ or US-20140061057-$ or US-	US-PGPUB; USPAT; USOCR; FPRS; EPO; DERWENT	OR	ON	2017/02/02 13:27

		20040004215-$ or US-20070278518-$ or US-20070228416-$ or US-20130052463-$ or US-20100290675-$ or US-20160118490-$).did. or (US-20160111501-$ or US-20130240945-$ or US-20040159843-$).did. or (US-9331244-$ or US-9406840-$ or US-7812366-$ or US-9281441-$ or US-9312428-$ or US-4148132-$ or US-9105792-$ or US-9397260-$ or US-7361973-$ or US-7485516-$ or US-8293618-$ or US-7332795-$ or US-8886334-$ or US-8097926-$ or US-8372726-$ or US-4990989-$ or US-4894703-$).did. or (US-3351698-$).did. or (WO-2014179523-$ or WO-2013126828-$ or WO-2015175369-$ or CN-104979440-$ or KR-20150041557-$ or KR-20160025069-$ or KR-20140110754-$ or KR-20100012827-$ or KR-20000003968-$ or WO-2009005227-$).did. or (WO-2009005227-$).did. or (US-20160197228-$ or US-20160118536-$ or WO-2013082592-$ or US-20140239312-$ or US-20160336483-$ or US-20120217496-$ or WO-2012000114-$ or US-20110315956-$ or WO-2010048537-$).did.				
L26	45	l25 and attribute	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2017/02/02 13:27
L27	8	l25 and different near2 attribute	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2017/02/02 13:28
L28	17	l25 and (differ or differing or different) near5 attribute	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2017/02/02 13:29
L29	34087	(elo or ((epi or epitaxy or epitaxial) near5 (lateral or laterally) near5 overgrowth))	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2017/02/02 13:32
L30	190	(elo or ((epi or epitaxy or epitaxial) near5 (lateral or laterally) near5 overgrowth)) same (mask or masking or masked or pattern or patterning or patterned) same group near III	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT;	OR	ON	2017/02/02 13:33

			IBM_TDB			
L31	17	(elo or ((epi or epitaxy or epitaxial) near5 (lateral or laterally) near5 overgrowth)) same (mask or masking or masked or pattern or patterning or patterned) same group near III and (offset or stagger or staggering or staggered or checkerboard or checker near board) near10 (layer or level)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2017/02/02 13:33
L32	84	group near III.clm. and (offset or stagger or staggering or staggered or checkerboard or checker near board) near10 (layer or level).clm.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2017/02/02 13:34
L33	127	(US-20160336483-$ or US-20160118536-$ or US-20150295133-$ or US-20170005224-$ or US-20160380150-$ or US-20160343901-$ or US-20140134773-$ or US-20160315449-$ or US-20160315219-$ or US-20160260867-$ or US-20160247885-$ or US-20160093771-$ or US-20140191261-$ or US-20140239312-$ or US-20160190387-$ or US-20160172544-$ or US-20140096669-$ or US-20160155902-$ or US-20160149099-$ or US-20160118535-$ or US-20160118534-$ or US-20160118531-$ or US-20160111618-$ or US-20160064631-$ or US-20130193409-$ or US-20160058020-$).did. or (US-20160049551-$ or US-20160035936-$ or US-20150297767-$ or US-20150255672-$ or US-20150228855-$ or US-20150179751-$ or US-20150165079-$ or US-20150108428-$ or US-20150091043-$ or US-20150083994-$ or US-20150069270-$ or US-20160197228-$ or US-20140346441-$ or US-20070081081-$ or US-20160211412-$ or US-20140110734-$ or US-20140158980-$ or US-20140064314-$ or US-20140016660-$ or US-20130320352-$ or US-20130146907-$ or US-20090272993-$ or US-20130277642-$ or US-20140110754-$ or US-20130193480-$ or US-20160225941-$ or US-20130055694-$).did. or (US-20130161305-$ or US-20070196682-$ or US-20150372193-$ or US-20160322535-$ or US-20130256828-$ or US-20080182403-$ or US-20070117348-$ or US-20030224591-$ or US-20140191284-$ or US-20140000693-$ or US-20080230815-$ or US-20130270514-$ or US-20110013656-$ or US-20100001375-$ or US-20020197830-$ or US-20120112188-$ or US-20120001220-$ or US-20110147791-$ or US-20020137249-$ or US-20140332374-$ or US-20140061057-$ or US-20040004215-$ or US-20070278518-$ or US-20070228416-$ or US-20130052463-	US-PGPUB; USPAT; USOCR; FPRS; EPO; DERWENT	OR	ON	2017/02/02 13:36

		$ or US-20100290675-$ or US-20160118490-$).did. or (US-20160111501-$ or US-20130240945-$ or US-20040159843-$ or US-20090180505-$ or US-20110005570-$ or US-20080150085-$ or US-20060267043-$).did. or (US-9331244-$ or US-9406840-$ or US-7812366-$ or US-9281441-$ or US-9312428-$ or US-4148132-$ or US-9105792-$ or US-9397260-$ or US-7361973-$ or US-7485516-$ or US-8293618-$ or US-7332795-$ or US-8886334-$ or US-8097926-$ or US-8372726-$ or US-4990989-$ or US-4894703-$).did. or (US-3351698-$).did. or (WO-2014179523-$ or WO-2013126828-$ or WO-2015175369-$ or CN-104979440-$ or KR-20150041557-$ or KR-20160025069-$ or KR-20140110754-$ or KR-20100012827-$ or KR-20000003968-$ or WO-2009005227-$).did. or (WO-2009005227-$).did. or (US-20160197228-$ or US-20160118536-$ or WO-2013082592-$ or US-20140239312-$ or US-20160336483-$ or US-20120217496-$ or WO-2012000114-$ or US-20110315956-$ or WO-2010048537-$).did.				
L34	67	l33 and heterostructure	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2017/02/02 13:36
L35	41	l33 and heterostructure and bragg	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2017/02/02 13:37
L36	21	l33 and heterostructure and bragg and offset	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2017/02/02 13:38
L37	7	l33 and heterostructure and bragg and offset near10 (laterall or vertically or vertical or lateral).clm.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2017/02/02 13:39
L38	8	l33 and heterostructure and bragg and offset near10 (laterall or vertically or vertical or lateral or horizontal or horizontally).clm.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT;	OR	ON	2017/02/02 13:39

			IBM_TDB			
L39	17	heterostructure and bragg and offset near10 (laterall or vertically or vertical or lateral or horizontal or horizontally).clm.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2017/02/02 13:40
L40	10	heterostructure and bragg and offset near10 (laterall or vertically or vertical or lateral or horizontal or horizontally).clm. and group near III.clm.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2017/02/02 13:40
L41	2	heterostructure and bragg and offset near10 (laterall or vertically or vertical or lateral or horizontal or horizontally).clm. and group near III.clm. and (transparent or reflective or conductive).clm.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2017/02/02 13:40
L42	1156	maxim near2 shatalov.in. or alexander near2 dobrinsky.in. or alexander near2 lunev.in. or rakesh near2 jain.in. or jinwei near2 yang.in. or michael near2 shur.in. or ramigijus near2 gaska.in.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2017/02/02 13:42
L43	316	l42 and heterostructure	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2017/02/02 13:43
L44	232	l43 and group near III	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2017/02/02 13:43
L45	7	l44 and (offset near5 (lateral or laterally or vertical or vertically or horizontal or horizontally)).clm.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2017/02/02 13:43
L46	1156	maxim near2 shatalov.in. or alexander near2 dobrinsky.in. or alexander near2 lunev.in. or rakesh near2 jain.in. or jinwei near2 yang.in. or michael near2 shur.in. or remigijus near2 gaska.in.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2017/02/02 13:46
L47	7	l46 and (offset near5 (lateral or laterally or vertical or vertically or horizontal or horizontally)).clm.	US-PGPUB; USPAT; USOCR; FPRS;	OR	ON	2017/02/02 13:46

			EPO; JPO; DERWENT; IBM_TDB			
L48	142426	sensor near2 electronic	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2017/02/02 13:46
L49	795	sensor near2 electronic.as. or sensor near2 electronic.aanm.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2017/02/02 13:46
L50	7	l49 and (offset near5 (lateral or laterally or vertical or vertically or horizontal or horizontally)).clm.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2017/02/02 13:47
L51	3935	257/94.ccls.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2017/02/02 13:47
L52	2	l51 and (offset near5 (lateral or laterally or vertical or vertically or horizontal or horizontally)).clm.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2017/02/02 13:47
L53	0	l51 and group near III.clm. and (offset near5 (lateral or laterally or vertical or vertically or horizontal or horizontally)).clm.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2017/02/02 13:47
L54	20432	H01L33/07.cpc. or H01L33/10.cpc. or H01L33/32.cpc.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2017/02/02 13:48
L55	8	l54 and group near III.clm. and (offset near5 (lateral or laterally or vertical or vertically or horizontal or horizontally)).clm.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2017/02/02 13:48
L56	27655	H01L33/007.cpc. or H01L33/10.cpc. or H01L33/32.cpc.	US-PGPUB; USPAT;	OR	ON	2017/02/02 13:48

			USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB			
L57	8	l56 and group near III.clm. and (offset near5 (lateral or laterally or vertical or vertically or horizontal or horizontally)).clm.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2017/02/02 13:48
L58	0	l56 and group near III.clm. and (offset near5 (lateral or laterally or vertical or vertically or horizontal or horizontally)).clm. and lif near off	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2017/02/02 13:49
L59	1	l56 and group near III.clm. and (offset near5 (lateral or laterally or vertical or vertically or horizontal or horizontally)).clm. and lift near off	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2017/02/02 13:49
L60	4	group near III.clm. and (offset near5 (lateral or laterally or vertical or vertically or horizontal or horizontally)).clm. and lift near off	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2017/02/02 13:49
L61	12	group near III and (offset near5 (lateral or laterally or vertical or vertically or horizontal or horizontally)).clm. and lift near off	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2017/02/02 13:49
L62	14	group near III and (offset near10 (lateral or laterally or vertical or vertically or horizontal or horizontally)).clm. and lift near off	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2017/02/02 13:50
L63	139	group near III and (offset near10 (lateral or laterally or vertical or vertically or horizontal or horizontally)).clm.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2017/02/02 13:50
L64	24	group near III and (offset near10 (lateral or laterally or vertical or vertically or horizontal or horizontally)).clm. and heterostructure	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2017/02/02 13:50

L65	16	group near III and (offset near10 (lateral or laterally or vertical or vertically or horizontal or horizontally)).clm. and heterostructure and (reflective or transparent)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2017/02/02 13:51

2/2/2017 1:52:10 PM
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EAST Search History

EAST Search History (Prior Art)

Ref #	Hits	Search Query	DBs	Default Operator	Plurals	Time Stamp
L1	2	14/984156	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2017/02/01 14:51
L2	1	inhomogeneous same checkerboard same staggered	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2017/02/01 14:54
L3	24	inhomogeneous same staggered	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2017/02/01 14:54
L4	217	shatalov near2 maxim	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2017/02/01 14:56
L5	2	"20160197228"	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2017/02/01 14:57
L6	5	14/189012	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2017/02/01 14:57
L7	44	(US-20160336483-$ or US-20160118536-$ or US-20150295133-$ or US-20170005224-$ or US-20160380150-$ or US-20160343901-$ or US-20140134773-$ or US-20160315449-$ or US-20160315219-$ or US-20160260867-$ or US-20160247885-$ or US-20160093771-$ or US-20140191261-$ or US-20140239312-$ or US-20160190387-$ or	US-PGPUB; FPRS; DERWENT	OR	ON	2017/02/01 14:58

		US-20160172544-$ or US-20140096669-$ or US-20160155902-$ or US-20160149099-$ or US-20160118535-$ or US-20160118534-$ or US-20160118531-$ or US-20160111618-$ or US-20160064631-$ or US-20130193409-$ or US-20160058020-$).did. or (US-20160049551-$ or US-20160035936-$ or US-20150297767-$ or US-20150255672-$ or US-20150228855-$ or US-20150179751-$ or US-20150165079-$ or US-20150108428-$ or US-20150091043-$ or US-20150083994-$ or US-20150069270-$ or US-20160197228-$).did. or (WO-2014179523-$ or WO-2013126828-$ or WO-2015175369-$ or CN-104979440-$).did. or (US-20160197228-$).did.				
L8	7	l7 and inhomogeneous near region.clm.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2017/02/01 14:58
L9	2	l7 and inhomogeneous near region same (offset or stagger or staggered).clm.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2017/02/01 14:59
L10	4	l7 and inhomogeneous near region same (offset or stagger or staggered) same level	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2017/02/01 14:59
L11	2	l7 and inhomogeneous near region same (offset or stagger or staggered) same (second near (laye or level))	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2017/02/01 15:00
L12	2	l7 and inhomogeneous near region same (offset or stagger or staggered) same (second near (layer or level))	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2017/02/01 15:00
L13	0	l7 and inhomogeneous near region same (offset or stagger or staggered) same (second near (layer or level)) same (first near (level or layer)) same semicondcutor	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2017/02/01 15:01
L14	1	l7 and inhomogeneous near region same (offset or stagger or staggered) same	US-PGPUB; USPAT;	OR	ON	2017/02/01 15:01

		(second near (layer or level)) same (first near (level or layer)) same semiconductor	USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB			
L15	1	inhomogeneous near region same (offset or stagger or staggered) same (second near (layer or level)) same (first near (level or layer)) same semiconductor	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2017/02/01 15:02
L16	1	inhomogeneous near region same (second near (layer or level)) same (first near (level or layer)) same semiconductor	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2017/02/01 15:03
L17	3	inhomogeneous near region same (second near (layer or level)) near10 (first near (level or layer)) near10 offset	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2017/02/01 15:04
L18	3	inhomogeneous near region.clm. and (second near (layer or level)) near10 (first near (level or layer)) near10 offset	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2017/02/01 15:05
L19	3	inhomogeneous near region.clm. and (second near (layer or level)) near10 (first near (level or layer)) near10 (stagger or staggering or staggered or offset)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2017/02/01 15:06
L20	3	inhomogeneous near region.clm. and (second near (layer or level)) near10 (first near (level or layer)) near10 (stagger or staggering or staggered or offset or overlap or overlapping or overlapped)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2017/02/01 15:07
L21	3	inhomogeneous near region same (second near (layer or level)) near10 (first near (level or layer)) near10 (stagger or staggering or staggered or offset or overlap or overlapping or overlapped)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2017/02/01 15:07
L22	356	sensor near electronic and checkerboard	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2017/02/01 15:08

L23	35	sensor near electronic and checkerboard and inhomogeneous	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2017/02/01 15:09
L24	1	sensor near electronic and checkerboard same inhomogeneous	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2017/02/01 15:09
L25	19	sensor near electronic and checkerboard same semiconductor	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2017/02/01 15:09
L26	11	sensor near electronic and checkerboard same semiconductor same (layer or level)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2017/02/01 15:09
L27	5	sensor near electronic and checkerboard same semiconductor same (layer or level) same (offset or stagger or staggering or staggered or overlap or overlapping or overlapped)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2017/02/01 15:10
L28	5	sensor near electronic and checkerboard same semiconductor same (layer or level) same (offset or stagger or staggering or staggered or overlap or overlapping or overlapped) same transparent	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2017/02/01 15:11
L29	5	checkerboard same semiconductor same (layer or level) same (offset or stagger or staggering or staggered or overlap or overlapping or overlapped) same transparent	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2017/02/01 15:12
L30	5	checkerboard same semiconductor same (layer or level) same (offset or stagger or staggering or staggered or overlap or overlapping or overlapped) same transparent same reflective same conductive	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2017/02/01 15:13
L31	103	semiconductor same (layer or level) same (offset or stagger or staggering or staggered or overlap or overlapping or overlapped) same transparent same reflective same conductive	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO;	OR	ON	2017/02/01 15:15

			DERWENT; IBM_TDB			
L32	10	semiconductor same (layer or level) same (offset or stagger or staggering or staggered or overlap or overlapping or overlapped) same transparent same reflective same conductive same (laterally or vertically)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2017/02/01 15:16
L33	42	("20090272993" | "20130146907" | "20130320352" | "20140016660" | "20160197228" | "7812366")	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2017/02/01 15:21
L34	61	(US-20160336483-$ or US-20160118536-$ or US-20150295133-$ or US-20170005224-$ or US-20160380150-$ or US-20160343901-$ or US-20140134773-$ or US-20160315449-$ or US-20160315219-$ or US-20160260867-$ or US-20160247885-$ or US-20160093771-$ or US-20140191261-$ or US-20140239312-$ or US-20160190387-$ or US-20160172544-$ or US-20140096669-$ or US-20160155902-$ or US-20160149099-$ or US-20160118535-$ or US-20160118534-$ or US-20160118531-$ or US-20160111618-$ or US-20160064631-$ or US-20130193409-$ or US-20160058020-$).did. or (US-20160049551-$ or US-20160035936-$ or US-20150297767-$ or US-20150255672-$ or US-20150228855-$ or US-20150179751-$ or US-20150165079-$ or US-20150108428-$ or US-20150091043-$ or US-20150083994-$ or US-20150069270-$ or US-20160197228-$ or US-20140346441-$ or US-20070081081-$ or US-20160211412-$ or US-20140110734-$ or US-20140158980-$ or US-20140064314-$ or US-20140016660-$ or US-20130320352-$ or US-20130146907-$ or US-20090272993-$ or US-20130277642-$).did. or (US-9331244-$ or US-9406840-$ or US-7812366-$ or US-9281441-$).did. or (WO-2014179523-$ or WO-2013126828-$ or WO-2015175369-$ or CN-104979440-$ or KR-20150041557-$).did. or (US-20160197228-$ or US-20160118536-$).did.	US-PGPUB; USPAT; FPRS; DERWENT	OR	ON	2017/02/01 15:24
L35	14	l34 and checkerboard	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2017/02/01 15:24
L36	10	l34 and (checkerboard or checker near board) near10 (level or layer)	US-PGPUB; USPAT; USOCR;	OR	ON	2017/02/01 15:26

			FPRS; EPO; JPO; DERWENT; IBM_TDB			
L37	0	l34 and (checkerboard or checker near board) near10 (level or layer) near10 (lateral or laterally or vertical or vertically)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2017/02/01 15:27
L38	0	l34 and (checkerboard or checker near board) with (level or layer) with (lateral or laterally or vertical or vertically)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2017/02/01 15:27
L39	10	l34 and (checkerboard or checker near board) with (level or layer) same (lateral or laterally or vertical or vertically)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2017/02/01 15:27
L40	13	l34 and (checkerboard or checker near board) same (level or layer) same (lateral or laterally or vertical or vertically)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2017/02/01 15:28
L41	4	"20140110754"	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2017/02/01 15:29
L42	1	"20140110754" and (offset or stagger or staggering or staggered)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2017/02/01 15:30
L43	7	13/692191	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2017/02/01 15:30
L44	331	("20090057646" | "20110037097" | "7312474" | "7888154" | "20080153191" | "20090200645" | "20010024871" | "20070231488" | "20100252834" | "6472695" | "20060160345" | "20110266520" | "7811847" | "20070231488" | "20090057646" | "20080274268" | "20050045905" |	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2017/02/01 15:33

		"5880491" | "8236672" | "20090239357" | "5306924" | "20040219702" | "5880491" | "20020005514" | "6518644" | "7081410" | "20020005514" | "20050045895" | "20100230713")				
L45	7	l44 and (stagger or staggering or staggered)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2017/02/01 15:33
L46	31	l44 and (stagger or staggering or staggered or offset)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2017/02/01 15:34
L47	1	l44 and (stagger or staggering or staggered or offset) same checkerboard	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2017/02/01 15:35
L48	4	14/150930	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2017/02/01 15:35
L49	3	l48 and (stagger or staggering or staggered or offset) same checkerboard	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2017/02/01 15:36
L50	3	l48 and (stagger or staggering or staggered or offset) same checkerboard same (lateral or laterally or vertical or vertically)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2017/02/01 15:36
L51	351	(stagger or staggering or staggered or offset) same checkerboard same (lateral or laterally or vertical or vertically)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2017/02/01 15:37
L52	351	(stagger or staggering or staggered or offset) same checkerboard same (lateral or laterally or vertical or vertically)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2017/02/01 15:38

L53	22	(stagger or staggering or staggered or offset) same checkerboard same (lateral or laterally or vertical or vertically) and (gan or nitride).clm.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2017/02/01 15:39
L54	11	(stagger or staggering or staggered or offset) same checkerboard same (lateral or laterally or vertical or vertically) and (gan or nitride).clm. and reflective	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2017/02/01 15:40
L55	11	(stagger or staggering or staggered or offset) same checkerboard same (lateral or laterally or vertical or vertically) and (gan or nitride).clm. and reflective and transparent	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2017/02/01 15:41
L56	11	(stagger or staggering or staggered or offset) same checkerboard same (lateral or laterally or vertical or vertically) and (gan or nitride).clm. and reflective same transparent	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2017/02/01 15:41
L57	11	(stagger or staggering or staggered or offset) same checkerboard same (lateral or laterally or vertical or vertically) and (gan or nitride).clm. and reflective same transparent same percent	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2017/02/01 15:42
L58	7	shatalov and dobrinsky and lunev and jain and yang and shur and gaska	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2017/02/01 15:48
L59	77	(US-20160336483-$ or US-20160118536-$ or US-20150295133-$ or US-20170005224-$ or US-20160380150-$ or US-20160343901-$ or US-20140134773-$ or US-20160315449-$ or US-20160315219-$ or US-20160260867-$ or US-20160247885-$ or US-20160093771-$ or US-20140191261-$ or US-20140239312-$ or US-20160190387-$ or US-20160172544-$ or US-20140096669-$ or US-20160155902-$ or US-20160149099-$ or US-20160118535-$ or US-20160118534-$ or US-20160118531-$ or US-20160111618-$ or US-20160064631-$ or US-20130193409-$ or US-20160058020-$).did. or (US-20160049551-$ or US-20160035936-$ or US-20150297767-$ or US-20150255672-$ or US-20150228855-$ or US-20150179751-$ or US-20150165079-$ or	US-PGPUB; USPAT; FPRS; DERWENT	OR	ON	2017/02/01 15:53

		US-20150108428-$ or US-20150091043-$ or US-20150083994-$ or US-20150069270-$ or US-20160197228-$ or US-20140346441-$ or US-20070081081-$ or US-20160211412-$ or US-20140110734-$ or US-20140158980-$ or US-20140064314-$ or US-20140016660-$ or US-20130320352-$ or US-20130146907-$ or US-20090272993-$ or US-20130277642-$ or US-20140110754-$ or US-20130193480-$ or US-20160225941-$ or US-20130055694-$).did. or (US-20130161305-$ or US-20070196682-$ or US-20150372193-$ or US-20160322535-$).did. or (US-9331244-$ or US-9406840-$ or US-7812366-$ or US-9281441-$ or US-9312428-$ or US-4148132-$ or US-9105792-$ or US-9397260-$).did. or (WO-2014179523-$ or WO-2013126828-$ or WO-2015175369-$ or CN-104979440-$ or KR-20150041557-$ or KR-20160025069-$ or KR-20140110754-$).did. or (US-20160197228-$ or US-20160118536-$ or WO-2013082592-$ or US-20140239312-$).did.				
L60	4	l59 and laser near10 lift-off	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2017/02/01 15:53
L61	4	l59 and laser near10 lift-off and conductivity	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2017/02/01 15:53
L62	4	l59 and lift-off and conductivity	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2017/02/01 15:54
L63	5	l59 and (lift near off or lift-off)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2017/02/01 15:54
L64	264	vertically same offset same (reflective or conductive).clm.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2017/02/01 15:59
L65	1	(nitride or gan) same semiconductor same vertically same offset same (reflective or	US-PGPUB; USPAT;	OR	ON	2017/02/01 15:59

		conductive).clm.	USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB			
L66	9	(nitride or gan) same semiconductor same vertically same offset same (reflective or conductive)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2017/02/01 15:59
L67	2	(nitride or gan) same semiconductor same vertically same offset same (reflective or conductive).ti,ab,clm.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2017/02/01 16:00
L68	2	(nitride or gan) same semiconductor same vertically near2 offset same (reflective or conductive).ti,ab,clm.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2017/02/01 16:00
L69	8	(nitride or gan) same semiconductor same vertically near2 offset.ti,ab,clm.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2017/02/01 16:01
L70	548	(nitride or gan) same semiconductor same offset.ti,ab,clm.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2017/02/01 16:01
L71	432	(nitride or gan) same semiconductor same offset same (layer or level).ti,ab,clm.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2017/02/01 16:01
L72	33	(nitride or gan) same semiconductor same offset same (layer or level) same (reflective or transparent or conductive).ti,ab,clm.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2017/02/01 16:02
L73	79	(nitride or gan) same semiconductor same offset same (layer or level) same (reflective or transparent or conductive) same (hole or inhomogeneous or cavity or recess)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2017/02/01 16:02

L74	93	(nitride or gan) same semiconductor same offset same (layer or level) same (reflective or transparent or conductive) same (inhomogeneous or pattern or patterning or patterned)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2017/02/01 16:03
L75	55	(nitride or gan) same semiconductor same offset with (layer or level) same (reflective or transparent or conductive) same (inhomogeneous or pattern or patterning or patterned)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2017/02/01 16:03
L76	6	(nitride or gan) same semiconductor same offset with (layer or level) same (reflective or transparent or conductive) same (inhomogeneous or pattern or patterning or patterned).ti,ab,clm.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2017/02/01 16:03
L77	3	(nitride or gan) same semiconductor same offset with (layer or level) same (reflective or transparent or conductive) same (inhomogeneous or pattern or patterning or patterned) same group	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2017/02/01 16:04
L78	3	(nitride or gan) same semiconductor same offset with (layer or level) same (attributes or reflective or transparent or conductive) same (inhomogeneous or pattern or patterning or patterned) same group	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2017/02/01 16:04
L79	2	group near10 (nitride or gan) same semiconductor same offset with (layer or level) same (attributes or reflective or transparent or conductive) same (inhomogeneous or pattern or patterning or patterned)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2017/02/01 16:05
L80	9	group near10 (nitride or gan) same semiconductor same offset with (layer or level) same (attributes or reflective or transparent or conductive)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2017/02/01 16:05
L81	9	group near10 "iii" near10 (nitride or gan) same semiconductor same offset with (layer or level) same (attributes or reflective or transparent or conductive)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2017/02/01 16:06
L82	0	group near10 "iii" near10 (nitride or gan) same semiconductor same offset same (stagger or staggering or staggered) same (checkerboard or checker near board)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO;	OR	ON	2017/02/01 16:07

			DERWENT; IBM_TDB			
L83	0	group near10 "iii" near10 (nitride or gan) same semiconductor same (stagger or staggering or staggered) same (checkerboard or checker near board)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2017/02/01 16:07
L84	6	group near10 "iii" near10 (nitride or gan) same semiconductor same (checkerboard or checker near board)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2017/02/01 16:07
L85	28	group near10 "iii" near10 (nitride or gan) near10 semiconductor.ti,ab,clm. and (checkerboard or checker near board)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2017/02/01 16:08
L86	2	group near10 "iii" near10 (nitride or gan) near10 semiconductor.ti,ab,clm. and (checkerboard or checker near board) and (liftoff or lift-off or lift near off)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2017/02/01 16:08
L87	172	offset and (checkerboard or checker near board) and (liftoff or lift-off or lift near off)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2017/02/01 16:09
L88	13	offset and (checkerboard or checker near board) and (liftoff or lift-off or lift near off) and group near III	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2017/02/01 16:09
L89	11	group near III near2 semiconductor.clm. and inhomogeneous.clm.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2017/02/01 16:10
L90	6	group near III near2 semiconductor.clm. same inhomogeneous.clm.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2017/02/01 16:10
L91	10	group near III near2 semiconductor same inhomogeneous near region	US-PGPUB; USPAT; USOCR;	OR	ON	2017/02/01 16:11

			FPRS; EPO; JPO; DERWENT; IBM_TDB			
L92	110	(US-20160336483-$ or US-20160118536-$ or US-20150295133-$ or US-20170005224-$ or US-20160380150-$ or US-20160343901-$ or US-20140134773-$ or US-20160315449-$ or US-20160315219-$ or US-20160260867-$ or US-20160247885-$ or US-20160093771-$ or US-20140191261-$ or US-20140239312-$ or US-20160190387-$ or US-20160172544-$ or US-20140096669-$ or US-20160155902-$ or US-20160149099-$ or US-20160118535-$ or US-20160118534-$ or US-20160118531-$ or US-20160111618-$ or US-20160064631-$ or US-20130193409-$ or US-20160058020-$).did. or (US-20160049551-$ or US-20160035936-$ or US-20150297767-$ or US-20150255672-$ or US-20150228855-$ or US-20150179751-$ or US-20150165079-$ or US-20150108428-$ or US-20150091043-$ or US-20150083994-$ or US-20150069270-$ or US-20160197228-$ or US-20140346441-$ or US-20070081081-$ or US-20160211412-$ or US-20140110734-$ or US-20140158980-$ or US-20140064314-$ or US-20140016660-$ or US-20130320352-$ or US-20130146907-$ or US-20090272993-$ or US-20130277642-$ or US-20140110754-$ or US-20130193480-$ or US-20160225941-$ or US-20130055694-$).did. or (US-20130161305-$ or US-20070196682-$ or US-20150372193-$ or US-20160322535-$ or US-20130256828-$ or US-20080182403-$ or US-20070117348-$ or US-20030224591-$ or US-20140191284-$ or US-20140000693-$ or US-20080230815-$ or US-20130270514-$ or US-20110013656-$ or US-20100001375-$ or US-20020197830-$ or US-20120112188-$ or US-20120001220-$ or US-20110147791-$ or US-20020137249-$ or US-20140332374-$ or US-20140061057-$ or US-20040004215-$ or US-20070278518-$ or US-20070228416-$).did. or (US-9331244-$ or US-9406840-$ or US-7812366-$ or US-9281441-$ or US-9312428-$ or US-4148132-$ or US-9105792-$ or US-9397260-$ or US-7361973-$ or US-7485516-$ or US-8293618-$ or US-7332795-$ or US-8886334-$ or US-8097926-$ or US-8372726-$).did. or (WO-2014179523-$ or WO-2013126828-$ or WO-2015175369-$ or CN-104979440-$ or KR-20150041557-$ or KR-20160025069-$ or KR-20140110754-$ or KR-20100012827-$ or KR-20000003968-$ or WO-2009005227-$).did. or (WO-	US-PGPUB; USPAT; FPRS; EPO; DERWENT	OR	ON	2017/02/01 16:11

		2009005227-$).did. or (US-20160197228-$ or US-20160118536-$ or WO-2013082592-$ or US-20140239312-$ or US-20160336483-$).did.				
L93	5	l92 and reflective near region.clm.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2017/02/01 16:12
L94	0	l92 and reflective same conductive same transpaarent	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2017/02/01 16:12
L95	35	l92 and reflective same conductive same transparent	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2017/02/01 16:12
L96	32	l92 and reflective same conductive same transparent same region	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2017/02/01 16:13
L97	6	l92 and reflective same conductive same transparent same region same (offset or stagger or staggering or staggered)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2017/02/01 16:13
L98	6	l92 and reflective same conductive same transparent same region same (offset or stagger or staggering or staggered or checker or checker near board or checkerboard)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2017/02/01 16:14
L99	0	l92 and semicondcutor same reflective same conductive same transparent same region same (offset or stagger or staggering or staggered or checker or checker near board or checkerboard)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2017/02/01 16:14
L100	0	semicondcutor same reflective same conductive same transparent same region same (offset or stagger or staggering or staggered or checker or checker near board or checkerboard)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2017/02/01 16:14
L101	12	semiconductor same reflective same	US-PGPUB;	OR	ON	2017/02/01

		conductive same transparent same region same (offset or stagger or staggering or staggered or checker or checker near board or checkerboard)	USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB			16:15

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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Serial No.:	14/984,156	Conf. No.:	5890
Filing Date:	30 Dec 2015	Art Unit:	2826
Inventor(s):	Shatalov et al.	Examiner:	Erdem, Fazli
Title:	Semiconductor Structure with Inhomogeneous Regions	Docket No.:	SETI-0110-CIP-US

Mail Stop Amendment
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

AMENDMENT

This paper is being filed in response to the Office Action dated 8 February 2017.

Please amend the above-identified application as follows:

AMENDMENTS TO THE CLAIMS

The following listing of claims replaces all prior versions, and listings, of claims in the application.

1. (Original) A semiconductor heterostructure, comprising:

an active region;

a metallic contact;

a group III nitride semiconductor layer located between the active region and the metallic contact, the semiconductor layer including a plurality of inhomogeneous regions arranged within multiple levels of the semiconductor layer, wherein some of the inhomogeneous regions in a first level of the semiconductor layer are vertically offset from inhomogeneous regions in a second level of the semiconductor layer, and wherein the plurality of inhomogeneous regions include one or more of a set of transparent regions, a set of reflective regions and/or a set of conductive regions, each of the inhomogeneous regions having a set of attributes differing from a group III nitride material forming the semiconductor layer.

2. (Original) The semiconductor heterostructure of claim 1, wherein each of the inhomogeneous regions in the first level and the second level of the semiconductor layer includes a set of reflective regions.

3. (Original) The semiconductor heterostructure of claim 1, wherein each of the plurality of inhomogeneous regions in the first level of the semiconductor layer extend into the

metallic contact and each of the plurality of inhomogeneous regions in the second level of the semiconductor layer are located at an interface of the semiconductor layer.

4. (Original) The semiconductor heterostructure of claim 1, wherein all of the inhomogeneous regions in the first level of the semiconductor layer are staggered with the inhomogeneous regions in the second level of the semiconductor layer to form a checkerboard arrangement of the inhomogeneous regions within the semiconductor layer.

5. (Original) The semiconductor heterostructure of claim 1, wherein the inhomogeneous regions in the first level of the semiconductor layer each has a surface contacting the metallic contact, wherein at least one metal protrusion from the metallic contact extends into each inhomogeneous region.

6. (Original) The semiconductor heterostructure of claim 5, wherein each of the inhomogeneous regions in the first level of the semiconductor layer comprises a set of conductive regions and each of the inhomogeneous regions in the second level of the semiconductor layer comprises a set of reflective regions.

7. (Original) The semiconductor heterostructure of claim 6, wherein each of the inhomogeneous regions in the second level of the semiconductor layer has at least one metal protrusion extending from the metallic contact into the semiconductor layer that is directed to a surface of the inhomogeneous region without contact thereof.

8. (Currently amended) A method, comprising:

fabricating a semiconductor heterostructure, wherein the semiconductor heterostructure comprises:

an active region;

a metallic contact;

a single group III nitride semiconductor layer located between the active region and the metallic contact, the semiconductor layer including a plurality of inhomogeneous regions arranged within multiple levels of the semiconductor layer, wherein some of the inhomogeneous regions in a first level of the semiconductor layer are vertically offset from inhomogeneous regions in a second level of the semiconductor layer, and wherein the plurality of inhomogeneous regions include one or more of a set of transparent regions, a set of reflective regions and/or a set of conductive regions, each of the inhomogeneous regions having a set of attributes differing from a group III nitride material forming the semiconductor layer.

9. (Original) The method of claim 8, wherein the fabricating includes:

epitaxially growing a portion of the group III nitride semiconductor layer;

forming at least one of the sets of inhomogeneous regions on a surface of the portion of the group III nitride semiconductor layer; and

epitaxially over-growing the group III nitride semiconductor layer after the forming.

10. (Original) The method of claim 9, wherein the forming includes:

depositing the at least one of the sets of inhomogeneous regions using one of: thermal evaporation, magnetron sputtering, ion-beam deposition, or laser beam evaporation; and

patterning the at least one of the sets of inhomogeneous regions using photolithography.

11. (Currently amended) An optoelectronic device, comprising:

a semiconductor heterostructure~~, obtained through laser lift-off,~~ having a first side and a second side, the semiconductor heterostructure including:

a group III nitride semiconductor layer including a plurality of inhomogeneous regions, each inhomogeneous region having a set of attributes differing from a group III nitride material forming the semiconductor layer, wherein the plurality of inhomogeneous regions include:

a set of first inhomogeneous regions configured based on radiation having a target wavelength, wherein the set of first inhomogeneous regions are at least one of: transparent to the radiation or reflective of the radiation; and

a set of second inhomogeneous regions having a conductivity at least ten percent higher than a conductivity of the set of first inhomogeneous regions, wherein each of the sets of inhomogeneous regions occupy at least five percent of at least one of: a lateral planar area of the semiconductor layer or a volume of the semiconductor layer, and wherein at least some of the sets of inhomogeneous regions do not fully overlap.

12. (Original) The optoelectronic device of claim 11, further comprising a first metallic contact having a plurality of connected metallic domains formed on the first side of the semiconductor heterostructure.

13. (Original) The optoelectronic device of claim 11, further comprising a plurality of roughness elements formed on the first side of the semiconductor heterostructure.

14. (Original) The optoelectronic device of claim 11, further comprising a plurality of metallic contact domains formed on the second side of the semiconductor heterostructure.

15. (Original) The optoelectronic device of claim 11, further comprising a plurality of reflective elements incorporated within the semiconductor heterostructure proximate a surface of the second side of the semiconductor heterostructure.

16. (Original) The optoelectronic device of claim 15, wherein the plurality of reflective elements comprise one of dielectrics, metallic reflective islands, Bragg mirrors and combinations thereof.

17. (Original) The optoelectronic device of claim 15, wherein the plurality of reflective elements comprise alternating layers of one of Hf_2O_3 and Al_2O_3, H_2O_3 and SiO_2, and Al_2O_3 and SiO_2.

18. (Original) The optoelectronic device of claim 11, further comprising a plurality of Bragg domains formed on the second side of the semiconductor heterostructure.

19. (Original) The optoelectronic device of claim 11, further comprising a second metallic contact having metallic domains formed on the second side of the semiconductor heterostructure, each of the metallic domains separated from an adjacent metallic domain by a predetermined spacing.

20. (Original) The optoelectronic device of claim 11, further comprising a passivation layer formed on the second side of the semiconductor heterostructure and a plurality of disjoint domains interspersed within the passivation layer.

REMARKS

With this response, Applicant amended claims 8 and 11. No new matter has been added. Applicant is not conceding that the claims prior to this amendment are not patentable over the prior art cited by the Examiner. The present amendment is only for facilitating expeditious prosecution of the present patent application. Applicant does not acquiesce in the correctness of the rejections and reserves the right to present specific arguments regarding any rejected claims not specifically addressed herein. Further, Applicant respectfully reserves the right to pursue the full scope of the subject matter of these claims and any others in one or more subsequent patent applications that claim priority to the present patent application. Applicant requests further examination and reconsideration of the present patent application as set forth in pending claims 1-20.

Obvious-Type Double Patenting

Claims 1-20 are rejected on the ground of non-statutory double patenting as being unpatentable over claims 1-21 of U.S. Patent No. 9,331,244. In addition, claims 1-20 are rejected on the ground of non-statutory double patenting as being unpatentable over claims 1-20 of co-pending U.S. Patent Application Serial No. 15/225,403.

Applicant does not acquiesce with the appropriateness of the obviousness-type double patenting rejections as the scope and content of claims 1-20 of the present patent application has changed from that of the original filing in which the rejections are based. To this extent, Applicant respectfully requests reconsideration of the

obviousness-type double patenting rejections in view of the claims as they are currently presented.

35 U.S.C. §103 Rejection of Claims 1-7

Claims 1-7 are rejected under 35 U.S.C. §103 as allegedly being unpatentable over Saxler (US Patent Application Publication No. 2013/0270514), hereafter "Saxler," in view of Jain et al. (US Patent Application Publication No. 2015/0372193), hereafter "Jain."

Applicant respectfully traverses the §103 rejection of claims 1-7 under Saxler in view of Jain because Jain is ineffective as prior art against the claimed invention. According to 35 U.S.C. §102(b)(2)(C):

> [a] disclosure shall not be prior art to a claimed invention under subsection [§102(a)(2)] if — … the subject matter disclosed and the claimed invention, not later than the effective filing date of the claimed invention, were owned by the same person or subject to an obligation of assignment to the same person.

In the present case, claims 1-7 recite subject matter that pertains to material that is disclosed by the parent application (US Patent No. 9,331,244) of the present continuation-in-part (CIP) application. Thus, the subject matter of claims 1-7 is afforded the effective filing date of the parent application, which is February 25, 2013. Jain has a publication date of December 24, 2015 which is after the effective filing date of February 25, 2013 for the subject matter recited in claims 1-7. In addition, Applicant submits that the claimed invention and Jain were owned by the same person or subject to an obligation of assignment to the same entity, Sensor Electronic Technology, Inc., not later than the effective filing date of the claimed invention. As set forth in section

2154.02(C) of the Manual of Patent Examining Procedure, this statement is sufficient to establish that the §102(b)(2)(C) exception applies.

Because both provisions of §102(b)(2)(C) are met as evidenced above, Jain is not available as prior art against claims 1-7 under either §102 or §103. Accordingly, a *prima facie* case for rejecting claims 1-7 under §103 has not been established. Therefore, Applicant respectfully requests that the Examiner reconsider and remove the §103 rejection of claims 1-7 under Saxler in view of Jain.

35 U.S.C. §103 Rejection of Claims 8-10

Claims 8-10 are rejected under 35 U.S.C. §103 as allegedly being unpatentable over Saxler in view of Saxler et al. (US Patent Application Publication No. 2004/0031956), hereafter "Saxler 2004." Applicant submits that claims 8-10 are patentably distinguishable over Saxler in view of Saxler 2004.

Applicant amended independent claim 8 to better define the patentable features of the group III nitride semiconductor layer. Claim 8 now recites, *inter alia*, that the group III nitride semiconductor layer is a single layer. Thus, the plurality of inhomogeneous regions are arranged within multiple levels of this single semiconductor layer. FIGS. 7A and 11C are examples of sections in the application that provide support for this amendment.

The combination of Saxler in view of Saxler 2004 does not disclose or suggest a single semiconductor layer having a plurality of inhomogeneous regions arranged within multiple levels of the single semiconductor layer. At best, the combination of Saxler in view of Saxler 2004 discloses one level of inhomogeneous regions arranged within a

single semiconductor layer. For example, FIG. 6 of Saxler shows a first set of discontinuous regions 12A in a first N-GAN layer 22B and another set of discontinuous regions 12B in a second N-GAN layer 22C. Both the first N-GAN layer 22B and the second N-GAN layer 22C are separate and distinct semiconductor layers. Each of these layers only has a single level of discontinuous regions therein and not multiple levels. Similarly, FIG. 4 of Saxler 2004 shows a first set of discontinuous regions 34 in a first layer 32 and another set of discontinuous regions 40 in a third layer 38, with a second layer 36 separating layers 32 and 38. Both the first layer 32 and the third layer 38 are separate and distinct semiconductor layers. Each of these layers in Saxler 2004 only have a single level of discontinuous regions and not multiple levels. In view of these distinctions, Saxler in view of Saxler 2004 does not disclose or suggest a single semiconductor layer having a plurality of inhomogeneous regions arranged within multiple levels of the single semiconductor layer.

Accordingly, Applicant respectfully submits that Saxler in view of Saxler 2004 does not disclose or suggest all of the limitations set forth in claim 8. Claims 9-10 depend directly or indirectly from now presumably allowable claim 8, and thus are allowable by dependency. Accordingly, Applicant submits that claims 8-10 are patentably distinguishable over Saxler in view of Saxler 2004. Therefore, Applicant requests that the Examiner remove the §103 rejection of claims 8-10 under Saxler in view of Saxler 2004.

35 U.S.C. §103 Rejection of Claims 11-20

Claims 11-20 are rejected under 35 U.S.C. §103 as allegedly being unpatentable over Saxler in view of Jain et al. (US Patent Application Publication No. 2014/0134773), hereafter "Jain 2014." Applicant submits that claims 11-20 are patentably distinguishable over Saxler in view of Jain 2014.

Applicant amended independent claim 11 to remove the phrase "obtained through laser lift-off." The subject matter recited in amended claim 11 is clearly disclosed by the parent application (US Patent No. 9,331,244).

In light of this amendment, Applicant submits that Jain 2014 is ineffective as prior art against claim 11 per §102(b)(2)(C). In particular, Jain 2014 has a publication date of May 15, 2014 which is after the effective filing date for the subject matter recited in claim 11 that is disclosed by the parent application. In addition, Applicant submits that the invention set forth in claim 11 and Jain 2014 were owned by the same person or subject to an obligation of assignment to the same entity, Sensor Electronic Technology, Inc., not later than the effective filing date of the claimed invention. Accordingly, Jain 2014 is not available as prior art against claim 11 under either §102 or §103 because both provisions of §102(b)(2)(C) are met.

With Jain 2014 disqualified as prior art, a *prima facie* case for rejecting claim 11 under §103 has not been established. Therefore, Applicant respectfully requests that the Examiner reconsider and remove the §103 rejection of claim 11 and depending claims 12-20 under Saxler in view of Jain 2014.

Conclusion

In view of the foregoing amendments and remarks, Applicant requests that the Examiner reconsider this application. If the Examiner has any questions regarding the present patent application, the Examiner can contact Applicant's attorney at the number listed below.

Respectfully submitted,

/John LaBatt/

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Valatie, NY 12184
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Dated: 8 May 2017

Electronic Acknowledgement Receipt

EFS ID:	29138633
Application Number:	14984156
International Application Number:	
Confirmation Number:	5890
Title of Invention:	Semiconductor Structure with Inhomogeneous Regions
First Named Inventor/Applicant Name:	Maxim S. Shatalov
Customer Number:	11698
Filer:	John W LaBatt
Filer Authorized By:	
Attorney Docket Number:	SETI-0110-CIP-US
Receipt Date:	08-MAY-2017
Filing Date:	30-DEC-2015
Time Stamp:	11:50:30
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	no

File Listing:

Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1		SETI-0110-CIP-US_Amendment1.pdf	88096 567b1d996518aa18b8d7e83021844945bd052084	yes	13

	Multipart Description/PDF files in .zip description		
	Document Description	**Start**	**End**
	Amendment/Req. Reconsideration-After Non-Final Reject	1	1
	Claims	2	7
	Applicant Arguments/Remarks Made in an Amendment	8	13
Warnings:			
Information:			
	Total Files Size (in bytes):	88096	

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New Applications Under 35 U.S.C. 111

If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application.

National Stage of an International Application under 35 U.S.C. 371

If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.

New International Application Filed with the USPTO as a Receiving Office

If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.

PTO/SB/06 (09-11)
Approved for use through 1/31/2014. OMB 0651-0032
U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE
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PATENT APPLICATION FEE DETERMINATION RECORD Substitute for Form PTO-875	Application or Docket Number 14/984,156	Filing Date 12/30/2015	☐ To be Mailed

ENTITY: ☒ LARGE ☐ SMALL ☐ MICRO

APPLICATION AS FILED – PART I

	(Column 1)	(Column 2)		
FOR	NUMBER FILED	NUMBER EXTRA	RATE ($)	FEE ($)
☐ BASIC FEE (37 CFR 1.16(a), (b), or (c))	N/A	N/A	N/A	
☐ SEARCH FEE (37 CFR 1.16(k), (i), or (m))	N/A	N/A	N/A	
☐ EXAMINATION FEE (37 CFR 1.16(o), (p), or (q))	N/A	N/A	N/A	
TOTAL CLAIMS (37 CFR 1.16(i))	minus 20 =	*	X $ =	
INDEPENDENT CLAIMS (37 CFR 1.16(h))	minus 3 =	*	X $ =	
☐ APPLICATION SIZE FEE (37 CFR 1.16(s))	If the specification and drawings exceed 100 sheets of paper, the application size fee due is $310 ($155 for small entity) for each additional 50 sheets or fraction thereof. See 35 U.S.C. 41(a)(1)(G) and 37 CFR 1.16(s).			
☐ MULTIPLE DEPENDENT CLAIM PRESENT (37 CFR 1.16(j))				
* If the difference in column 1 is less than zero, enter "0" in column 2.			TOTAL	

APPLICATION AS AMENDED – PART II

		(Column 1)		(Column 2)	(Column 3)		
	05/08/2017	CLAIMS REMAINING AFTER AMENDMENT		HIGHEST NUMBER PREVIOUSLY PAID FOR	PRESENT EXTRA	RATE ($)	ADDITIONAL FEE ($)
AMENDMENT	Total (37 CFR 1.16(i))	* 20	Minus	** 20	= 0	X $80 =	0
	Independent (37 CFR 1.16(h))	* 3	Minus	***3	= 0	X $420 =	0
	☐ Application Size Fee (37 CFR 1.16(s))						
	☐ FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))						
						TOTAL ADD'L FEE	**0**

		(Column 1)		(Column 2)	(Column 3)		
		CLAIMS REMAINING AFTER AMENDMENT		HIGHEST NUMBER PREVIOUSLY PAID FOR	PRESENT EXTRA	RATE ($)	ADDITIONAL FEE ($)
AMENDMENT	Total (37 CFR 1.16(i))	*	Minus	**	=	X $ =	
	Independent (37 CFR 1.16(h))	*	Minus	***	=	X $ =	
	☐ Application Size Fee (37 CFR 1.16(s))						
	☐ FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))						
						TOTAL ADD'L FEE	

* If the entry in column 1 is less than the entry in column 2, write "0" in column 3.

** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 20, enter "20".

*** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 3, enter "3".

The "Highest Number Previously Paid For" (Total or Independent) is the highest number found in the appropriate box in column 1.

LIE
TAMMY D. MCBETH BROWN

PTO/SB/08a (03-15)
Approved for use through 07/31/2016. OMB 0651-0031
U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE

INFORMATION DISCLOSURE STATEMENT BY APPLICANT

(Not for submission under 37 CFR 1.99)

Application Number	14984156
Filing Date	2015-12-30
First Named Inventor	Shatalov et al.
Art Unit	2811
Examiner Name	
Attorney Docket Number	SETI-0110-CIP-US

U.S.PATENTS Remove

Examiner Initial*	Cite No	Patent Number	Kind Code[1]	Issue Date	Name of Patentee or Applicant of cited Document	Pages,Columns,Lines where Relevant Passages or Relevant Figures Appear
	1	5602418		1997-02-11	Imai et al.	

If you wish to add additional U.S. Patent citation information please click the Add button. Add

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Examiner Initial*	Cite No	Publication Number	Kind Code[1]	Publication Date	Name of Patentee or Applicant of cited Document	Pages,Columns,Lines where Relevant Passages or Relevant Figures Appear
	1	20160118536	A1	2016-04-28	Shatalov et al.	
	2	20150243840	A1	2015-08-27	Johnston et al.	

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INFORMATION DISCLOSURE STATEMENT BY APPLICANT (Not for submission under 37 CFR 1.99)		
	Application Number	14984156
	Filing Date	2015-12-30
	First Named Inventor	Shatalov et al.
	Art Unit	2811
	Examiner Name	
	Attorney Docket Number	SETI-0110-CIP-US

Examiner Initials*	Cite No	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc), date, pages(s), volume-issue number(s), publisher, city and/or country where published.	T[5]
	1	ERDEM, F., Application No. 15/225,403, Attorney Docket No. SETI-0110-CIP2-US, Office Action1, 5 April 2017, 14 pages	

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EXAMINER SIGNATURE

Examiner Signature		Date Considered	

*EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through a citation if not in conformance and not considered. Include copy of this form with next communication to applicant.

[1] See Kind Codes of USPTO Patent Documents at www.USPTO.GOV or MPEP 901.04. [2] Enter office that issued the document, by the two-letter code (WIPO Standard ST.3). [3] For Japanese patent documents, the indication of the year of the reign of the Emperor must precede the serial number of the patent document. [4] Kind of document by the appropriate symbols as indicated on the document under WIPO Standard ST.16 if possible. [5] Applicant is to place a check mark here if English language translation is attached.

INFORMATION DISCLOSURE STATEMENT BY APPLICANT (Not for submission under 37 CFR 1.99)		
	Application Number	14984156
	Filing Date	2015-12-30
	First Named Inventor	Shatalov et al.
	Art Unit	2811
	Examiner Name	
	Attorney Docket Number	SETI-0110-CIP-US

CERTIFICATION STATEMENT

Please see 37 CFR 1.97 and 1.98 to make the appropriate selection(s):

That each item of information contained in the information disclosure statement was first cited in any communication from a foreign patent office in a counterpart foreign application not more than three months prior to the filing of the information disclosure statement. See 37 CFR 1.97(e)(1).

OR

☒ That no item of information contained in the information disclosure statement was cited in a communication from a foreign patent office in a counterpart foreign application, and, to the knowledge of the person signing the certification after making reasonable inquiry, no item of information contained in the information disclosure statement was known to any individual designated in 37 CFR 1.56(c) more than three months prior to the filing of the information disclosure statement. See 37 CFR 1.97(e)(2).

See attached certification statement.

The fee set forth in 37 CFR 1.17 (p) has been submitted herewith.

A certification statement is not submitted herewith.

SIGNATURE

A signature of the applicant or representative is required in accordance with CFR 1.33, 10.18. Please see CFR 1.4(d) for the form of the signature.

Signature	/Elaine C. Berlin/	Date (YYYY-MM-DD)	2017-06-02
Name/Print	Elaine C. Berlin	Registration Number	61194

This collection of information is required by 37 CFR 1.97 and 1.98. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 1 hour to complete, including gathering, preparing and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

Privacy Act Statement

The Privacy Act of 1974 (P.L. 93-579) requires that you be given certain information in connection with your submission of the attached form related to a patent application or patent. Accordingly, pursuant to the requirements of the Act, please be advised that: (1) the general authority for the collection of this information is 35 U.S.C. 2(b)(2); (2) furnishing of the information solicited is voluntary; and (3) the principal purpose for which the information is used by the U.S. Patent and Trademark Office is to process and/or examine your submission related to a patent application or patent. If you do not furnish the requested information, the U.S. Patent and Trademark Office may not be able to process and/or examine your submission, which may result in termination of proceedings or abandonment of the application or expiration of the patent.

The information provided by you in this form will be subject to the following routine uses:

1. The information on this form will be treated confidentially to the extent allowed under the Freedom of Information Act (5 U.S.C. 552) and the Privacy Act (5 U.S.C. 552a). Records from this system of records may be disclosed to the Department of Justice to determine whether the Freedom of Information Act requires disclosure of these record s.

2. A record from this system of records may be disclosed, as a routine use, in the course of presenting evidence to a court, magistrate, or administrative tribunal, including disclosures to opposing counsel in the course of settlement negotiations.

3. A record in this system of records may be disclosed, as a routine use, to a Member of Congress submitting a request involving an individual, to whom the record pertains, when the individual has requested assistance from the Member with respect to the subject matter of the record.

4. A record in this system of records may be disclosed, as a routine use, to a contractor of the Agency having need for the information in order to perform a contract. Recipients of information shall be required to comply with the requirements of the Privacy Act of 1974, as amended, pursuant to 5 U.S.C. 552a(m).

5. A record related to an International Application filed under the Patent Cooperation Treaty in this system of records may be disclosed, as a routine use, to the International Bureau of the World Intellectual Property Organization, pursuant to the Patent Cooperation Treaty.

6. A record in this system of records may be disclosed, as a routine use, to another federal agency for purposes of National Security review (35 U.S.C. 181) and for review pursuant to the Atomic Energy Act (42 U.S.C. 218(c)).

7. A record from this system of records may be disclosed, as a routine use, to the Administrator, General Services, or his/her designee, during an inspection of records conducted by GSA as part of that agency's responsibility to recommend improvements in records management practices and programs, under authority of 44 U.S.C. 2904 and 2906. Such disclosure shall be made in accordance with the GSA regulations governing inspection of records for this purpose, and any other relevant (i.e., GSA or Commerce) directive. Such disclosure shall not be used to make determinations about individuals.

8. A record from this system of records may be disclosed, as a routine use, to the public after either publication of the application pursuant to 35 U.S.C. 122(b) or issuance of a patent pursuant to 35 U.S.C. 151. Further, a record may be disclosed, subject to the limitations of 37 CFR 1.14, as a routine use, to the public if the record was filed in an application which became abandoned or in which the proceedings were terminated and which application is referenced by either a published application, an application open to public inspections or an issued patent.

9. A record from this system of records may be disclosed, as a routine use, to a Federal, State, or local law enforcement agency, if the USPTO becomes aware of a violation or potential violation of law or regulation.

Electronic Acknowledgement Receipt

EFS ID:	29384977
Application Number:	14984156
International Application Number:	
Confirmation Number:	5890
Title of Invention:	Semiconductor Structure with Inhomogeneous Regions
First Named Inventor/Applicant Name:	Maxim S. Shatalov
Customer Number:	11698
Filer:	Elaine Chi Berlin
Filer Authorized By:	
Attorney Docket Number:	SETI-0110-CIP-US
Receipt Date:	05-JUN-2017
Filing Date:	30-DEC-2015
Time Stamp:	09:52:26
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	no

File Listing:

Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1	Information Disclosure Statement (IDS) Form (SB08)	SETI-0110-CIP-US_IDS3.pdf	1035092 726dbd9a515f9fafbd975e8233d8b794c4aad6d1	no	4

Warnings:

Information:					
2	Non Patent Literature	SETI-0110-CIP2-US_OfficeAction1_04-05-17.pdf	656953 28b478d30ef1380a48d77e37e4357d32c68ebe49	no	14
Warnings:					
Information:					
			Total Files Size (in bytes):	1692045	

This Acknowledgement Receipt evidences receipt on the noted date by the USPTO of the indicated documents, characterized by the applicant, and including page counts, where applicable. It serves as evidence of receipt similar to a Post Card, as described in MPEP 503.

New Applications Under 35 U.S.C. 111

If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application.

National Stage of an International Application under 35 U.S.C. 371

If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.

New International Application Filed with the USPTO as a Receiving Office

If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.

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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
14/984,156	12/30/2015	Maxim S. Shatalov	SETI-0110-CIP-US	5890

11698 7590 08/04/2017

LaBatt, LLC (SET)
PO Box 630
Valatie, NY 12184

EXAMINER
ERDEM, FAZLI

ART UNIT	PAPER NUMBER
2826	

NOTIFICATION DATE	DELIVERY MODE
08/04/2017	ELECTRONIC

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

adobrinsky@s-et.com
national@labattlaw.com

Office Action Summary	Application No. 14/984,156	Applicant(s) SHATALOV ET AL.	
	Examiner FAZLI ERDEM	Art Unit 2826	AIA (First Inventor to File) Status Yes

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTHS FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *6/5/2017*.

☐ A declaration(s)/affidavit(s) under **37 CFR 1.130(b)** was/were filed on _____.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ An election was made by the applicant in response to a restriction requirement set forth during the interview on _____; the restriction requirement and election have been incorporated into this action.

4)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims*

5)☒ Claim(s) *1-20* is/are pending in the application.

5a) Of the above claim(s) _____ is/are withdrawn from consideration.

6)☐ Claim(s) _____ is/are allowed.

7)☒ Claim(s) *1-20* is/are rejected.

8)☐ Claim(s) _____ is/are objected to.

9)☐ Claim(s) _____ are subject to restriction and/or election requirement.

* If any claims have been determined allowable, you may be eligible to benefit from the **Patent Prosecution Highway** program at a participating intellectual property office for the corresponding application. For more information, please see http://www.uspto.gov/patents/init_events/pph/index.jsp or send an inquiry to PPHfeedback@uspto.gov.

Application Papers

10)☐ The specification is objected to by the Examiner.

11)☒ The drawing(s) filed on *12/30/2015* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

Certified copies:

a)☐ All b)☐ Some** c)☐ None of the:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

** See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)

2) ☒ Information Disclosure Statement(s) (PTO/SB/08a and/or PTO/SB/08b) Paper No(s)/Mail Date *6/5/2017*.

3) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .

4) ☐ Other: _____.

The present application, filed on or after March 16, 2013, is being examined under the first inventor to file provisions of the AIA.

DETAILED ACTION

Response to Arguments

Applicant's arguments, filed on 6/5/017 with respect to 35 USC 103 rejection on claims 1-7 have been fully considered and are persuasive (see arguments on pages 9 and 10 of the remarks filed on 6/5/2017). The non-final rejection of 2/8/2017 has been withdrawn.

Applicant's arguments, filed on 6/5/017 with respect to 35 USC 103 rejection on claims 11-20 have been fully considered and are persuasive (see arguments on page 12 of the remarks filed on 6/5/2017). The non-final rejection of 2/8/2017 has been withdrawn.

Applicant's arguments filed 6/5/2017, with respect to Obvious-Type Double patenting on claims 1-20 have been fully considered but they are not persuasive (see page 8-10 of the remarks filed on 6/5/2017.

With respect to claims 1-20, double patenting rejections do still apply as explained below.

Applicant's arguments filed 6/5/2017, with respect to 35 USC 103 rejection on claims 8-10 have been fully considered but they are not persuasive (see page 10 and 11 of the remarks filed on 6/5/2017.)

With respect to the claims 8-10, the amendment with the wording "single" does not have a support in the specification and claims as originally filed.

Double Patenting

The nonstatutory double patenting rejection is based on a judicially created doctrine grounded in public policy (a policy reflected in the statute) so as to prevent the unjustified or improper timewise extension of the "right to exclude" granted by a patent and to prevent possible harassment by multiple assignees. A nonstatutory double patenting rejection is appropriate where the conflicting claims are not identical, but at least one examined application claim is not patentably distinct from the reference claim(s) because the examined application claim is either anticipated by, or would have been obvious over, the reference claim(s). See, e.g., *In re Berg*, 140 F.3d 1428, 46 USPQ2d 1226 (Fed. Cir. 1998); *In re Goodman*, 11 F.3d 1046, 29 USPQ2d 2010 (Fed. Cir. 1993); *In re Longi*, 759 F.2d 887, 225 USPQ 645 (Fed. Cir. 1985); *In re Van Ornum*, 686 F.2d 937, 214 USPQ 761 (CCPA 1982); *In re Vogel*, 422 F.2d 438, 164 USPQ 619 (CCPA 1970); *In re Thorington*, 418 F.2d 528, 163 USPQ 644 (CCPA 1969).

A timely filed terminal disclaimer in compliance with 37 CFR 1.321(c) or 1.321(d) may be used to overcome an actual or provisional rejection based on nonstatutory double patenting provided the reference application or patent either is shown to be commonly owned with the examined application, or claims an invention made as a result of activities undertaken within the scope of a joint research agreement. See MPEP § 717.02 for applications subject to examination under the first inventor to file provisions of the AIA as explained in MPEP § 2159. See MPEP §§ 706.02(l)(1) - 706.02(l)(3) for applications not subject to examination under the first inventor to file

provisions of the AIA. A terminal disclaimer must be signed in compliance with 37 CFR 1.321(b).

The USPTO Internet website contains terminal disclaimer forms which may be used. Please visit www.uspto.gov/patent/patents-forms. The filing date of the application in which the form is filed determines what form (e.g., PTO/SB/25, PTO/SB/26, PTO/AIA/25, or PTO/AIA/26) should be used. A web-based eTerminal Disclaimer may be filled out completely online using web-screens. An eTerminal Disclaimer that meets all requirements is auto-processed and approved immediately upon submission. For more information about eTerminal Disclaimers, refer to www.uspto.gov/patents/process/file/efs/guidance/eTD-info-I.jsp.

Claims 1-20 are rejected on the ground of nonstatutory double patenting as being unpatentable over claims 1-21 U.S. Patent No. 9,331,244. Although the claims at issue are not identical, they are not patentably distinct from each other because

They both disclose semiconductor heterostructure comprising group III nitride semiconductor layer with inhomogeneous regions (especially see Claim 9 of '244 in comparison to the Claim 4 of the instant application)

Claims 1-20 provisionally rejected on the ground of nonstatutory double patenting as being unpatentable over claims 1-20 of copending Application No. 15/225,403 (US2016/0336483). Although the claims at issue are not identical, they are not patentably distinct from each other because

They both disclose semiconductor heterostructure comprising group III nitride semiconductor layer with inhomogeneous regions (especially see Claim 1 of '244 in

comparison to the Claim 1 of the instant application with respect to the “attributes” limitation)

This is a provisional nonstatutory double patenting rejection because the patentably indistinct claims have not in fact been patented.

Claim Rejections - 35 USC § 112

The following is a quotation of the first paragraph of 35 U.S.C. 112(a):

> (a) IN GENERAL.—The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same, and shall set forth the best mode contemplated by the inventor or joint inventor of carrying out the invention.

The following is a quotation of the first paragraph of pre-AIA 35 U.S.C. 112:

> The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same, and shall set forth the best mode contemplated by the inventor of carrying out his invention.

Claims 8-10 are rejected under 35 U.S.C. 112(a) or 35 U.S.C. 112 (pre-AIA), first paragraph, as failing to comply with the written description requirement. The claim(s) contains subject matter which was not described in the specification in such a way as to reasonably convey to one skilled in the relevant art that the inventor or a joint inventor, or for pre-AIA the inventor(s), at the time the application was filed, had possession of the claimed invention.

The wording “single layer” does not have a support in the specification and claims as originally filed. For the examination purpose, the claim is treated as without the wording "single layer".

With respect to the applicant’s argument (see page 10 second to last paragraph of the remarks filed on 5/8/2017) that the support is provided in Figs. 7A and 11C, paragraph 0052 of the instant application as published has "semiconductor base layer" and not "semiconductor layer" and paragraph 0061 of the instant application as published has “semiconductor layer(s)” instead of “semiconductor layer”.

Claim Rejections - 35 USC § 103

In the event the determination of the status of the application as subject to AIA 35 U.S.C. 102 and 103 (or as subject to pre-AIA 35 U.S.C. 102 and 103) is incorrect, any correction of the statutory basis for the rejection will not be considered a new ground of rejection if the prior art relied upon, and the rationale supporting the rejection, would be the same under either status.

The following is a quotation of 35 U.S.C. 103 which forms the basis for all obviousness rejections set forth in this Office action:

> A patent for a claimed invention may not be obtained, notwithstanding that the claimed invention is not identically disclosed as set forth in section 102, if the differences between the claimed invention and the prior art are such that the claimed invention as a whole would have been obvious before the effective filing date of the claimed invention to a person having ordinary skill in the art to which the claimed invention pertains. Patentability shall not be negated by the manner in which the invention was made.

Claims 8-10 are is/are rejected under 35 U.S.C. 103 as being unpatentable over Saxler (2013/0270514) in view of Saxler et al. (2004/0031956).

Regarding Claim 8, in Fig. 6, Saxler ‘514 discloes

fabricating a semiconductor heterostructure, wherein the semiconductor heterostructure comprises: an active region; a metallic contact; a group III nitride semiconductor layer located between the active region and the metallic contact, the semiconductor layer including a plurality of inhomogeneous regions arranged within multiple levels of the semiconductor layer, wherein some of the inhomogeneous regions in a first level of the semiconductor layer are vertically offset from inhomogeneous regions in a second level of the semiconductor layer, and wherein the plurality of inhomogeneous regions include one or more of a set of transparent regions, a set of reflective regions and/or a set of conductive regions. Saxler ‘514 fails to disclose the required limitation where each of the inhomogeneous regions having a set of attributes differing from a group III nitride material forming the semiconductor layer. However, Saxler ‘956 heterogeneous bandgap structures wherein paragraphs 0019 and 0021, the required limitation of differing "attributes” is disclosed.

It would have been obvious to one of having ordinary skill in the art at the time of effective filing to have the required differing attributes limitation in Saxler ‘514 as taught by Saxler ‘956. in for stress reduction purposes.

Regarding Claim 9, in Saxler ‘514, the fabricating includes: epitaxially growing a portion of the group III nitride semiconductor layer; forming at least one of the sets of inhomogeneous regions on a surface of the portion of the group III nitride semiconductor layer; and epitaxially over-growing the group III nitride semiconductor layer after the forming.

Regarding Claim 10, in Saxler '514, forming includes: depositing the at least one of the sets of inhomogeneous regions using one of: thermal evaporation, magnetron sputtering, ion-beam deposition, or laser beam evaporation; and patterning the at least one of the sets of inhomogeneous regions using photolithography.

Conclusion

THIS ACTION IS MADE FINAL. Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to FAZLI ERDEM whose telephone number is (571)272-1914. The examiner can normally be reached on M-F 8:00 - 5:00.

Examiner interviews are available via telephone, in-person, and video conferencing using a USPTO supplied web-based collaboration tool. To schedule an

interview, applicant is encouraged to use the USPTO Automated Interview Request (AIR) at http://www.uspto.gov/interviewpractice.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Davienne Monbleau can be reached on 571-272-1945. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/FAZLI ERDEM/
Primary Examiner, Art Unit 2826
7/31/2017

PTO/SB/08a (03-15)
Approved for use through 07/31/2016. OMB 0651-0031
U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE

INFORMATION DISCLOSURE STATEMENT BY APPLICANT

(Not for submission under 37 CFR 1.99)

Application Number	14984156
Filing Date	2015-12-30
First Named Inventor	Shatalov et al.
Art Unit	2811
Examiner Name	
Attorney Docket Number	SETI-0110-CIP-US

U.S.PATENTS Remove

Examiner Initial*	Cite No	Patent Number	Kind Code[1]	Issue Date	Name of Patentee or Applicant of cited Document	Pages,Columns,Lines where Relevant Passages or Relevant Figures Appear
/F.E/	1	5602418		1997-02-11	Imai et al.	

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Examiner Initial*	Cite No	Publication Number	Kind Code[1]	Publication Date	Name of Patentee or Applicant of cited Document	Pages,Columns,Lines where Relevant Passages or Relevant Figures Appear
/F.E/	1	20160118536	A1	2016-04-28	Shatalov et al.	
/F.E/	2	20150243840	A1	2015-08-27	Johnston et al.	

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Examiner Initial*	Cite No	Foreign Document Number[3]	Country Code[2] i	Kind Code[4]	Publication Date	Name of Patentee or Applicant of cited Document	Pages,Columns,Lines where Relevant Passages or Relevant Figures Appear	T[5]
	1							

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Examiner Initials*	Cite No	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc), date, pages(s), volume-issue number(s), publisher, city and/or country where published.	T[5]
/F.E/	1	ERDEM, F., Application No. 15/225,403, Attorney Docket No. SETI-0110-CIP2-US, Office Action1, 5 April 2017, 14 pages	

If you wish to add additional non-patent literature document citation information please click the Add button Add

EXAMINER SIGNATURE

Examiner Signature	/FAZLI ERDEM/	Date Considered	07/31/2017

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[1] See Kind Codes of USPTO Patent Documents at www.USPTO.GOV or MPEP 901.04. [2] Enter office that issued the document, by the two-letter code (WIPO Standard ST.3). [3] For Japanese patent documents, the indication of the year of the reign of the Emperor must precede the serial number of the patent document. [4] Kind of document by the appropriate symbols as indicated on the document under WIPO Standard ST.16 if possible. [5] Applicant is to place a check mark here if English language translation is attached.

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	Attorney Docket Number	SETI-0110-CIP-US

CERTIFICATION STATEMENT

Please see 37 CFR 1.97 and 1.98 to make the appropriate selection(s):

That each item of information contained in the information disclosure statement was first cited in any communication from a foreign patent office in a counterpart foreign application not more than three months prior to the filing of the information disclosure statement. See 37 CFR 1.97(e)(1).

OR

☒ That no item of information contained in the information disclosure statement was cited in a communication from a foreign patent office in a counterpart foreign application, and, to the knowledge of the person signing the certification after making reasonable inquiry, no item of information contained in the information disclosure statement was known to any individual designated in 37 CFR 1.56(c) more than three months prior to the filing of the information disclosure statement. See 37 CFR 1.97(e)(2).

See attached certification statement.

The fee set forth in 37 CFR 1.17 (p) has been submitted herewith.

A certification statement is not submitted herewith.

SIGNATURE

A signature of the applicant or representative is required in accordance with CFR 1.33, 10.18. Please see CFR 1.4(d) for the form of the signature.

Signature	/Elaine C. Berlin/	Date (YYYY-MM-DD)	2017-06-02
Name/Print	Elaine C. Berlin	Registration Number	61194

This collection of information is required by 37 CFR 1.97 and 1.98. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 1 hour to complete, including gathering, preparing and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

Privacy Act Statement

The Privacy Act of 1974 (P.L. 93-579) requires that you be given certain information in connection with your submission of the attached form related to a patent application or patent. Accordingly, pursuant to the requirements of the Act, please be advised that: (1) the general authority for the collection of this information is 35 U.S.C. 2(b)(2); (2) furnishing of the information solicited is voluntary; and (3) the principal purpose for which the information is used by the U.S. Patent and Trademark Office is to process and/or examine your submission related to a patent application or patent. If you do not furnish the requested information, the U.S. Patent and Trademark Office may not be able to process and/or examine your submission, which may result in termination of proceedings or abandonment of the application or expiration of the patent.

The information provided by you in this form will be subject to the following routine uses:

1. The information on this form will be treated confidentially to the extent allowed under the Freedom of Information Act (5 U.S.C. 552) and the Privacy Act (5 U.S.C. 552a). Records from this system of records may be disclosed to the Department of Justice to determine whether the Freedom of Information Act requires disclosure of these record s.

2. A record from this system of records may be disclosed, as a routine use, in the course of presenting evidence to a court, magistrate, or administrative tribunal, including disclosures to opposing counsel in the course of settlement negotiations.

3. A record in this system of records may be disclosed, as a routine use, to a Member of Congress submitting a request involving an individual, to whom the record pertains, when the individual has requested assistance from the Member with respect to the subject matter of the record.

4. A record in this system of records may be disclosed, as a routine use, to a contractor of the Agency having need for the information in order to perform a contract. Recipients of information shall be required to comply with the requirements of the Privacy Act of 1974, as amended, pursuant to 5 U.S.C. 552a(m).

5. A record related to an International Application filed under the Patent Cooperation Treaty in this system of records may be disclosed, as a routine use, to the International Bureau of the World Intellectual Property Organization, pursuant to the Patent Cooperation Treaty.

6. A record in this system of records may be disclosed, as a routine use, to another federal agency for purposes of National Security review (35 U.S.C. 181) and for review pursuant to the Atomic Energy Act (42 U.S.C. 218(c)).

7. A record from this system of records may be disclosed, as a routine use, to the Administrator, General Services, or his/her designee, during an inspection of records conducted by GSA as part of that agency's responsibility to recommend improvements in records management practices and programs, under authority of 44 U.S.C. 2904 and 2906. Such disclosure shall be made in accordance with the GSA regulations governing inspection of records for this purpose, and any other relevant (i.e., GSA or Commerce) directive. Such disclosure shall not be used to make determinations about individuals.

8. A record from this system of records may be disclosed, as a routine use, to the public after either publication of the application pursuant to 35 U.S.C. 122(b) or issuance of a patent pursuant to 35 U.S.C. 151. Further, a record may be disclosed, subject to the limitations of 37 CFR 1.14, as a routine use, to the public if the record was filed in an application which became abandoned or in which the proceedings were terminated and which application is referenced by either a published application, an application open to public inspections or an issued patent.

9. A record from this system of records may be disclosed, as a routine use, to a Federal, State, or local law enforcement agency, if the USPTO becomes aware of a violation or potential violation of law or regulation.

Search Notes	Application/Control No.	Applicant(s)/Patent Under Reexamination
	14984156	SHATALOV ET AL.
	Examiner	Art Unit
	FAZLI ERDEM	2826

CPC- SEARCHED		
Symbol	Date	Examiner
H01L33/10	2/2/2017	FE
H01L33/007	2/2/2017	FE
H01L33/32	2/2/2017	FE

CPC COMBINATION SETS - SEARCHED		
Symbol	Date	Examiner

US CLASSIFICATION SEARCHED			
Class	Subclass	Date	Examiner

* See search history printout included with this form or the SEARCH NOTES box below to determine the scope of the search.

SEARCH NOTES		
Search Notes	Date	Examiner
H01L33/10	2/2/2017	FE
H01L33/007	2/2/2017	FE
H01L33/32	2/2/2017	FE
Inventors are searched	2/2/2017	FE
Assignee is searched	2/2/2017	FE
CPC search limited with text is conducted	2/2/2017	FE
Searched 257/94 limited with text	2/2/2017	FE
EAST Search history is attached	2/2/2017	FE
Updated EAST Search history is attached	7/31/2017	FE

INTERFERENCE SEARCH

US Class/ CPC Symbol	US Subclass / CPC Group	Date	Examiner

EAST Search History

EAST Search History (Prior Art)

Ref #	Hits	Search Query	DBs	Default Operator	Plurals	Time Stamp
S212	56	nitride near2 semiconductor same inhomogeneous	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2017/07/31 10:58
S213	6	nitride near2 semiconductor same inhomogeneous same level	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2017/07/31 10:58
S214	2	nitride near2 semiconductor same inhomogeneous same level same transparent	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2017/07/31 10:59
S215	2	nitride near2 semiconductor same inhomogeneous same level same transparent same offset	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2017/07/31 11:07
S216	3	inhomogeneous same level same transparent same offset	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2017/07/31 11:30
S217	2	group near III same level same transparent same offset	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2017/07/31 11:31
S218	136	group near III same level same transparent	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2017/07/31 11:33
S219	55	group near III same level same	US-PGPUB;	OR	ON	2017/07/31

		transparent same nitride	USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB			11:34
S220	23	group near III same level same transparent same nitride and offset	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2017/07/31 11:34
S221	3	group near III same level same transparent same nitride and offset.clm.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2017/07/31 11:35
S222	148	(US-20160336483-$ or US-20160118536-$ or US-20150295133-$ or US-20170005224-$ or US-20160380150-$ or US-20160343901-$ or US-20140134773-$ or US-20160315449-$ or US-20160315219-$ or US-20160260867-$ or US-20160247885-$ or US-20160093771-$ or US-20140191261-$ or US-20140239312-$ or US-20160190387-$ or US-20160172544-$ or US-20140096669-$ or US-20160155902-$ or US-20160149099-$ or US-20160118535-$ or US-20160118534-$ or US-20160118531-$ or US-20160111618-$ or US-20160064631-$ or US-20130193409-$ or US-20160058020-$).did. or (US-20160049551-$ or US-20160035936-$ or US-20150297767-$ or US-20150255672-$ or US-20150228855-$ or US-20150179751-$ or US-20150165079-$ or US-20150108428-$ or US-20150091043-$ or US-20150083994-$ or US-20150069270-$ or US-20160197228-$ or US-20140346441-$ or US-20070081081-$ or US-20160211412-$ or US-20140110734-$ or US-20140158980-$ or US-20140064314-$ or US-20140016660-$ or US-20130320352-$ or US-20130146907-$ or US-20090272993-$ or US-20130277642-$ or US-20140110754-$ or US-20130193480-$ or US-20160225941-$ or US-20130055694-$).did. or (US-20130161305-$ or US-20070196682-$ or US-20150372193-$ or US-20160322535-$ or US-20130256828-$ or US-20080182403-$ or US-20070117348-$ or US-20030224591-$ or US-20140191284-$ or US-20140000693-$ or US-20080230815-$ or US-20130270514-$ or US-20110013656-$ or US-20100001375-$ or US-20020197830-$ or US-20120112188-$ or US-20120001220-$ or US-20110147791-$ or	US-PGPUB; USPAT; USOCR; FPRS; EPO; DERWENT	OR	ON	2017/07/31 11:36

		US-20020137249-$ or US-20140332374-$ or US-20140061057-$ or US-20040004215-$ or US-20070278518-$ or US-20070228416-$ or US-20130052463-$ or US-20100290675-$ or US-20160118490-$).did. or (US-20160111501-$ or US-20130240945-$ or US-20040159843-$ or US-20090180505-$ or US-20110005570-$ or US-20080150085-$ or US-20060267043-$ or US-20150349187-$ or US-20130181219-$ or US-20140346566-$ or US-20120165759-$ or US-20110089440-$ or US-20100123268-$ or US-20070145417-$ or US-20130264570-$ or US-20160365475-$ or US-20160365284-$ or US-20110188530-$ or US-20150069217-$ or US-20050285541-$ or US-20140349427-$ or US-20140147650-$ or US-20020173089-$ or US-20100126570-$).did. or (US-9331244-$ or US-9406840-$ or US-7812366-$ or US-9281441-$ or US-9312428-$ or US-4148132-$ or US-9105792-$ or US-9397260-$ or US-7361973-$ or US-7485516-$ or US-8293618-$ or US-7332795-$ or US-8886334-$ or US-8097926-$ or US-8372726-$ or US-4990989-$ or US-4894703-$ or US-9450124-$ or US-6376864-$ or US-4891093-$ or US-4888085-$).did. or (US-3351698-$).did. or (WO-2014179523-$ or WO-2013126828-$ or WO-2015175369-$ or CN-104979440-$ or KR-20150041557-$ or KR-20160025069-$ or KR-20140110754-$ or KR-20100012827-$ or KR-20000003968-$ or WO-2009005227-$).did. or (WO-2009005227-$).did. or (US-20160197228-$ or US-20160118536-$ or WO-2013082592-$ or US-20140239312-$ or US-20160336483-$ or US-20120217496-$ or WO-2012000114-$ or US-20110315956-$ or WO-2010048537-$).did.				
S223	42	S222 and offset.clm.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2017/07/31 11:36
S224	3	S222 and offset.clm. and inhomogeneous.clm.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2017/07/31 11:36
S225	3	("5602418" | "20160118536" | "20150243840").PN.	US-PGPUB; USPAT	OR	ON	2017/07/31 11:52
S226	130	("5602418" | "20160118536" | "20150243840")	US-PGPUB; USPAT	OR	ON	2017/07/31 11:52
S227	54	S226 and single near2 layer	US-PGPUB;	OR	ON	2017/07/31

			USPAT			11:52
S228	0	S226 and (homogeneous or inhomogeneous) and single near2 layer	US-PGPUB; USPAT	OR	ON	2017/07/31 11:53
S229	148	(US-20160336483-$ or US-20160118536-$ or US-20150295133-$ or US-20170005224-$ or US-20160380150-$ or US-20160343901-$ or US-20140134773-$ or US-20160315449-$ or US-20160315219-$ or US-20160260867-$ or US-20160247885-$ or US-20160093771-$ or US-20140191261-$ or US-20140239312-$ or US-20160190387-$ or US-20160172544-$ or US-20140096669-$ or US-20160155902-$ or US-20160149099-$ or US-20160118535-$ or US-20160118534-$ or US-20160118531-$ or US-20160111618-$ or US-20160064631-$ or US-20130193409-$ or US-20160058020-$).did. or (US-20160049551-$ or US-20160035936-$ or US-20150297767-$ or US-20150255672-$ or US-20150228855-$ or US-20150179751-$ or US-20150165079-$ or US-20150108428-$ or US-20150091043-$ or US-20150083994-$ or US-20150069270-$ or US-20160197228-$ or US-20140346441-$ or US-20070081081-$ or US-20160211412-$ or US-20140110734-$ or US-20140158980-$ or US-20140064314-$ or US-20140016660-$ or US-20130320352-$ or US-20130146907-$ or US-20090272993-$ or US-20130277642-$ or US-20140110754-$ or US-20130193480-$ or US-20160225941-$ or US-20130055694-$).did. or (US-20130161305-$ or US-20070196682-$ or US-20150372193-$ or US-20160322535-$ or US-20130256828-$ or US-20080182403-$ or US-20070117348-$ or US-20030224591-$ or US-20140191284-$ or US-20140000693-$ or US-20080230815-$ or US-20130270514-$ or US-20110013656-$ or US-20100001375-$ or US-20020197830-$ or US-20120112188-$ or US-20120001220-$ or US-20110147791-$ or US-20020137249-$ or US-20140332374-$ or US-20140061057-$ or US-20040004215-$ or US-20070278518-$ or US-20070228416-$ or US-20130052463-$ or US-20100290675-$ or US-20160118490-$).did. or (US-20160111501-$ or US-20130240945-$ or US-20040159843-$ or US-20090180505-$ or US-20110005570-$ or US-20080150085-$ or US-20060267043-$ or US-20150349187-$ or US-20130181219-$ or US-20140346566-$ or US-20120165759-$ or US-20110089440-$ or US-20100123268-$ or US-20070145417-$ or US-20130264570-$ or US-20160365475-$ or US-20160365284-$ or US-20110188530-$ or US-20150069217-$ or US-20050285541-$ or US-	US-PGPUB; USPAT; USOCR; FPRS; EPO; DERWENT	OR	ON	2017/07/31 11:53

		20140349427-$ or US-20140147650-$ or US-20020173089-$ or US-20100126570-$).did. or (US-9331244-$ or US-9406840-$ or US-7812366-$ or US-9281441-$ or US-9312428-$ or US-4148132-$ or US-9105792-$ or US-9397260-$ or US-7361973-$ or US-7485516-$ or US-8293618-$ or US-7332795-$ or US-8886334-$ or US-8097926-$ or US-8372726-$ or US-4990989-$ or US-4894703-$ or US-9450124-$ or US-6376864-$ or US-4891093-$ or US-4888085-$).did. or (US-3351698-$).did. or (WO-2014179523-$ or WO-2013126828-$ or WO-2015175369-$ or CN-104979440-$ or KR-20150041557-$ or KR-20160025069-$ or KR-20140110754-$ or KR-20100012827-$ or KR-20000003968-$ or WO-2009005227-$).did. or (WO-2009005227-$).did. or (US-20160197228-$ or US-20160118536-$ or WO-2013082592-$ or US-20140239312-$ or US-20160336483-$ or US-20120217496-$ or WO-2012000114-$ or US-20110315956-$ or WO-2010048537-$).did.				
S230	7	S229 and (homogeneous or inhomogeneous) and single near2 layer	US-PGPUB; USPAT	OR	ON	2017/07/31 11:54
S231	7	S229 and (homogeneous or inhomogeneous) and single near layer	US-PGPUB; USPAT	OR	ON	2017/07/31 11:54
S232	1	S229 and (homogeneous or inhomogeneous) same single near layer	US-PGPUB; USPAT	OR	ON	2017/07/31 11:54
S233	1	group near III near10 nitride near10 semiconductor same active same metallic same inhomogeneous	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2017/07/31 11:56
S234	6	group near III near10 nitride near10 semiconductor same active same contact same inhomogeneous	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2017/07/31 11:56
S235	8	"9331244"	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2017/07/31 12:17
S236	5	S235 and (metal or metallic or contact).clm.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2017/07/31 12:18
S237	3	S235 and inhomogeneous.clm. and transparent.clm.	US-PGPUB; USPAT;	OR	ON	2017/07/31 12:20

			USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB			
S238	2	14/984156	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2017/07/31 12:47
S239	0	S238 and nitride near2 semiconductor near2 layer near2 single near2 layer	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2017/07/31 12:47
S240	2	S238 and nitride near2 semiconductor near2 layer	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2017/07/31 12:47
S241	2	S238 and nitride near2 semiconductor near2 layer same active same contact	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2017/07/31 12:48
S242	2	S238 and nitride near2 semiconductor near2 layer	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2017/07/31 12:55
S243	2	S238 and nitride near2 semiconductor near2 layer near10 between	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2017/07/31 12:59
S244	3	14/189,012 and nitride near2 semiconductor near2 layer near10 between	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2017/07/31 12:59
S245	6	14/189,012	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2017/07/31 13:00

S246	3	S245 and nitride near2 semiconductor near2 layer near10 between	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2017/07/31 13:00
S247	6	S245 and nitride near2 semiconductor near2 layer	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2017/07/31 13:00

7/ 31/ 2017 2:14:49 PM
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Index of Claims	Application/Control No.	Applicant(s)/Patent Under Reexamination
	14984156	SHATALOV ET AL.
	Examiner	**Art Unit**
	FAZLI ERDEM	2826

✓	Rejected	-	Cancelled	N	Non-Elected	A	Appeal
=	Allowed	÷	Restricted	I	Interference	O	Objected

☐ Claims renumbered in the same order as presented by applicant ☐ CPA ☐ T.D. ☐ R.1.47

CLAIM		DATE								
Final	Original	02/02/2017	07/31/2017							
	1	✓	✓							
	2	✓	✓							
	3	✓	✓							
	4	✓	✓							
	5	✓	✓							
	6	✓	✓							
	7	✓	✓							
	8	✓	✓							
	9	✓	✓							
	10	✓	✓							
	11	✓	✓							
	12	✓	✓							
	13	✓	✓							
	14	✓	✓							
	15	✓	✓							
	16	✓	✓							
	17	✓	✓							
	18	✓	✓							
	19	✓	✓							
	20	✓	✓							

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UNITED STATES DEPARTMENT OF COMMERCE
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www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
14/984,156	12/30/2015	Maxim S. Shatalov	SETI-0110-CIP-US	5890

11698 7590 08/04/2017

LaBatt, LLC (SET)
PO Box 630
Valatie, NY 12184

EXAMINER
ERDEM, FAZLI

ART UNIT	PAPER NUMBER
2826	

NOTIFICATION DATE	DELIVERY MODE
08/04/2017	ELECTRONIC

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

adobrinsky@s-et.com
national@labattlaw.com

Office Action Summary	Application No. 14/984,156	Applicant(s) SHATALOV ET AL.	
	Examiner FAZLI ERDEM	Art Unit 2826	AIA (First Inventor to File) Status Yes

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTHS FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *6/5/2017*.

☐ A declaration(s)/affidavit(s) under **37 CFR 1.130(b)** was/were filed on _____.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ An election was made by the applicant in response to a restriction requirement set forth during the interview on _____; the restriction requirement and election have been incorporated into this action.

4)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims*

5)☒ Claim(s) *1-20* is/are pending in the application.

5a) Of the above claim(s) _____ is/are withdrawn from consideration.

6)☐ Claim(s) _____ is/are allowed.

7)☒ Claim(s) *1-20* is/are rejected.

8)☐ Claim(s) _____ is/are objected to.

9)☐ Claim(s) _____ are subject to restriction and/or election requirement.

* If any claims have been determined allowable, you may be eligible to benefit from the **Patent Prosecution Highway** program at a participating intellectual property office for the corresponding application. For more information, please see http://www.uspto.gov/patents/init_events/pph/index.jsp or send an inquiry to PPHfeedback@uspto.gov.

Application Papers

10)☐ The specification is objected to by the Examiner.

11)☒ The drawing(s) filed on *12/30/2015* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

Certified copies:

a)☐ All b)☐ Some** c)☐ None of the:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

** See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)

2) ☒ Information Disclosure Statement(s) (PTO/SB/08a and/or PTO/SB/08b) Paper No(s)/Mail Date *6/5/2017*.

3) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .

4) ☐ Other: _____.

The present application, filed on or after March 16, 2013, is being examined under the first inventor to file provisions of the AIA.

DETAILED ACTION

Response to Arguments

Applicant's arguments, filed on 6/5/017 with respect to 35 USC 103 rejection on claims 1-7 have been fully considered and are persuasive (see arguments on pages 9 and 10 of the remarks filed on 6/5/2017). The non-final rejection of 2/8/2017 has been withdrawn.

Applicant's arguments, filed on 6/5/017 with respect to 35 USC 103 rejection on claims 11-20 have been fully considered and are persuasive (see arguments on page 12 of the remarks filed on 6/5/2017). The non-final rejection of 2/8/2017 has been withdrawn.

Applicant's arguments filed 6/5/2017, with respect to Obvious-Type Double patenting on claims 1-20 have been fully considered but they are not persuasive (see page 8-10 of the remarks filed on 6/5/2017.

With respect to claims 1-20, double patenting rejections do still apply as explained below.

Applicant's arguments filed 6/5/2017, with respect to 35 USC 103 rejection on claims 8-10 have been fully considered but they are not persuasive (see page 10 and 11 of the remarks filed on 6/5/2017.)

With respect to the claims 8-10, the amendment with the wording "single" does not have a support in the specification and claims as originally filed.

Double Patenting

The nonstatutory double patenting rejection is based on a judicially created doctrine grounded in public policy (a policy reflected in the statute) so as to prevent the unjustified or improper timewise extension of the "right to exclude" granted by a patent and to prevent possible harassment by multiple assignees. A nonstatutory double patenting rejection is appropriate where the conflicting claims are not identical, but at least one examined application claim is not patentably distinct from the reference claim(s) because the examined application claim is either anticipated by, or would have been obvious over, the reference claim(s). See, e.g., *In re Berg*, 140 F.3d 1428, 46 USPQ2d 1226 (Fed. Cir. 1998); *In re Goodman*, 11 F.3d 1046, 29 USPQ2d 2010 (Fed. Cir. 1993); *In re Longi*, 759 F.2d 887, 225 USPQ 645 (Fed. Cir. 1985); *In re Van Ornum*, 686 F.2d 937, 214 USPQ 761 (CCPA 1982); *In re Vogel*, 422 F.2d 438, 164 USPQ 619 (CCPA 1970); *In re Thorington*, 418 F.2d 528, 163 USPQ 644 (CCPA 1969).

A timely filed terminal disclaimer in compliance with 37 CFR 1.321(c) or 1.321(d) may be used to overcome an actual or provisional rejection based on nonstatutory double patenting provided the reference application or patent either is shown to be commonly owned with the examined application, or claims an invention made as a result of activities undertaken within the scope of a joint research agreement. See MPEP § 717.02 for applications subject to examination under the first inventor to file provisions of the AIA as explained in MPEP § 2159. See MPEP §§ 706.02(l)(1) - 706.02(l)(3) for applications not subject to examination under the first inventor to file

provisions of the AIA. A terminal disclaimer must be signed in compliance with 37 CFR 1.321(b).

The USPTO Internet website contains terminal disclaimer forms which may be used. Please visit www.uspto.gov/patent/patents-forms. The filing date of the application in which the form is filed determines what form (e.g., PTO/SB/25, PTO/SB/26, PTO/AIA/25, or PTO/AIA/26) should be used. A web-based eTerminal Disclaimer may be filled out completely online using web-screens. An eTerminal Disclaimer that meets all requirements is auto-processed and approved immediately upon submission. For more information about eTerminal Disclaimers, refer to www.uspto.gov/patents/process/file/efs/guidance/eTD-info-I.jsp.

Claims 1-20 are rejected on the ground of nonstatutory double patenting as being unpatentable over claims 1-21 U.S. Patent No. 9,331,244. Although the claims at issue are not identical, they are not patentably distinct from each other because

They both disclose semiconductor heterostructure comprising group III nitride semiconductor layer with inhomogeneous regions (especially see Claim 9 of '244 in comparison to the Claim 4 of the instant application)

Claims 1-20 provisionally rejected on the ground of nonstatutory double patenting as being unpatentable over claims 1-20 of copending Application No. 15/225,403 (US2016/0336483). Although the claims at issue are not identical, they are not patentably distinct from each other because

They both disclose semiconductor heterostructure comprising group III nitride semiconductor layer with inhomogeneous regions (especially see Claim 1 of '244 in

comparison to the Claim 1 of the instant application with respect to the “attributes” limitation)

This is a provisional nonstatutory double patenting rejection because the patentably indistinct claims have not in fact been patented.

Claim Rejections - 35 USC § 112

The following is a quotation of the first paragraph of 35 U.S.C. 112(a):

> (a) IN GENERAL.—The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same, and shall set forth the best mode contemplated by the inventor or joint inventor of carrying out the invention.

The following is a quotation of the first paragraph of pre-AIA 35 U.S.C. 112:

> The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same, and shall set forth the best mode contemplated by the inventor of carrying out his invention.

Claims 8-10 are rejected under 35 U.S.C. 112(a) or 35 U.S.C. 112 (pre-AIA), first paragraph, as failing to comply with the written description requirement. The claim(s) contains subject matter which was not described in the specification in such a way as to reasonably convey to one skilled in the relevant art that the inventor or a joint inventor, or for pre-AIA the inventor(s), at the time the application was filed, had possession of the claimed invention.

The wording “single layer” does not have a support in the specification and claims as originally filed. For the examination purpose, the claim is treated as without the wording "single layer".

With respect to the applicant’s argument (see page 10 second to last paragraph of the remarks filed on 5/8/2017) that the support is provided in Figs. 7A and 11C, paragraph 0052 of the instant application as published has "semiconductor base layer" and not "semiconductor layer" and paragraph 0061 of the instant application as published has “semiconductor layer(s)” instead of “semiconductor layer”.

Claim Rejections - 35 USC § 103

In the event the determination of the status of the application as subject to AIA 35 U.S.C. 102 and 103 (or as subject to pre-AIA 35 U.S.C. 102 and 103) is incorrect, any correction of the statutory basis for the rejection will not be considered a new ground of rejection if the prior art relied upon, and the rationale supporting the rejection, would be the same under either status.

The following is a quotation of 35 U.S.C. 103 which forms the basis for all obviousness rejections set forth in this Office action:

> A patent for a claimed invention may not be obtained, notwithstanding that the claimed invention is not identically disclosed as set forth in section 102, if the differences between the claimed invention and the prior art are such that the claimed invention as a whole would have been obvious before the effective filing date of the claimed invention to a person having ordinary skill in the art to which the claimed invention pertains. Patentability shall not be negated by the manner in which the invention was made.

Claims 8-10 are is/are rejected under 35 U.S.C. 103 as being unpatentable over Saxler (2013/0270514) in view of Saxler et al. (2004/0031956).

Regarding Claim 8, in Fig. 6, Saxler ‘514 discloes

fabricating a semiconductor heterostructure, wherein the semiconductor heterostructure comprises: an active region; a metallic contact; a group III nitride semiconductor layer located between the active region and the metallic contact, the semiconductor layer including a plurality of inhomogeneous regions arranged within multiple levels of the semiconductor layer, wherein some of the inhomogeneous regions in a first level of the semiconductor layer are vertically offset from inhomogeneous regions in a second level of the semiconductor layer, and wherein the plurality of inhomogeneous regions include one or more of a set of transparent regions, a set of reflective regions and/or a set of conductive regions. Saxler ‘514 fails to disclose the required limitation where each of the inhomogeneous regions having a set of attributes differing from a group III nitride material forming the semiconductor layer. However, Saxler ‘956 heterogeneous bandgap structures wherein paragraphs 0019 and 0021, the required limitation of differing "attributes” is disclosed.

It would have been obvious to one of having ordinary skill in the art at the time of effective filing to have the required differing attributes limitation in Saxler ‘514 as taught by Saxler ‘956. in for stress reduction purposes.

Regarding Claim 9, in Saxler ‘514, the fabricating includes: epitaxially growing a portion of the group III nitride semiconductor layer; forming at least one of the sets of inhomogeneous regions on a surface of the portion of the group III nitride semiconductor layer; and epitaxially over-growing the group III nitride semiconductor layer after the forming.

Regarding Claim 10, in Saxler '514, forming includes: depositing the at least one of the sets of inhomogeneous regions using one of: thermal evaporation, magnetron sputtering, ion-beam deposition, or laser beam evaporation; and patterning the at least one of the sets of inhomogeneous regions using photolithography.

Conclusion

THIS ACTION IS MADE FINAL. Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to FAZLI ERDEM whose telephone number is (571)272-1914. The examiner can normally be reached on M-F 8:00 - 5:00.

Examiner interviews are available via telephone, in-person, and video conferencing using a USPTO supplied web-based collaboration tool. To schedule an

interview, applicant is encouraged to use the USPTO Automated Interview Request (AIR) at http://www.uspto.gov/interviewpractice.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Davienne Monbleau can be reached on 571-272-1945. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/FAZLI ERDEM/
Primary Examiner, Art Unit 2826
7/31/2017

PTO/SB/08a (03-15)
Approved for use through 07/31/2016. OMB 0651-0031
U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE

INFORMATION DISCLOSURE STATEMENT BY APPLICANT

(Not for submission under 37 CFR 1.99)

Application Number	14984156
Filing Date	2015-12-30
First Named Inventor	Shatalov et al.
Art Unit	2811
Examiner Name	
Attorney Docket Number	SETI-0110-CIP-US

U.S.PATENTS Remove

Examiner Initial*	Cite No	Patent Number	Kind Code[1]	Issue Date	Name of Patentee or Applicant of cited Document	Pages,Columns,Lines where Relevant Passages or Relevant Figures Appear
/F.E/	1	5602418		1997-02-11	Imai et al.	

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Examiner Initial*	Cite No	Publication Number	Kind Code[1]	Publication Date	Name of Patentee or Applicant of cited Document	Pages,Columns,Lines where Relevant Passages or Relevant Figures Appear
/F.E/	1	20160118536	A1	2016-04-28	Shatalov et al.	
/F.E/	2	20150243840	A1	2015-08-27	Johnston et al.	

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INFORMATION DISCLOSURE STATEMENT BY APPLICANT (Not for submission under 37 CFR 1.99)		
	Application Number	14984156
	Filing Date	2015-12-30
	First Named Inventor	Shatalov et al.
	Art Unit	2811
	Examiner Name	
	Attorney Docket Number	SETI-0110-CIP-US

Examiner Initials*	Cite No	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc), date, pages(s), volume-issue number(s), publisher, city and/or country where published.	T[5]
/F.E/	1	ERDEM, F., Application No. 15/225,403, Attorney Docket No. SETI-0110-CIP2-US, Office Action1, 5 April 2017, 14 pages	

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EXAMINER SIGNATURE

Examiner Signature	/FAZLI ERDEM/	Date Considered	07/31/2017

*EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through a citation if not in conformance and not considered. Include copy of this form with next communication to applicant.

[1] See Kind Codes of USPTO Patent Documents at www.USPTO.GOV or MPEP 901.04. [2] Enter office that issued the document, by the two-letter code (WIPO Standard ST.3). [3] For Japanese patent documents, the indication of the year of the reign of the Emperor must precede the serial number of the patent document. [4] Kind of document by the appropriate symbols as indicated on the document under WIPO Standard ST.16 if possible. [5] Applicant is to place a check mark here if English language translation is attached.

INFORMATION DISCLOSURE STATEMENT BY APPLICANT (Not for submission under 37 CFR 1.99)		
	Application Number	14984156
	Filing Date	2015-12-30
	First Named Inventor	Shatalov et al.
	Art Unit	2811
	Examiner Name	
	Attorney Docket Number	SETI-0110-CIP-US

CERTIFICATION STATEMENT

Please see 37 CFR 1.97 and 1.98 to make the appropriate selection(s):

That each item of information contained in the information disclosure statement was first cited in any communication from a foreign patent office in a counterpart foreign application not more than three months prior to the filing of the information disclosure statement. See 37 CFR 1.97(e)(1).

OR

☒ That no item of information contained in the information disclosure statement was cited in a communication from a foreign patent office in a counterpart foreign application, and, to the knowledge of the person signing the certification after making reasonable inquiry, no item of information contained in the information disclosure statement was known to any individual designated in 37 CFR 1.56(c) more than three months prior to the filing of the information disclosure statement. See 37 CFR 1.97(e)(2).

See attached certification statement.

The fee set forth in 37 CFR 1.17 (p) has been submitted herewith.

A certification statement is not submitted herewith.

SIGNATURE

A signature of the applicant or representative is required in accordance with CFR 1.33, 10.18. Please see CFR 1.4(d) for the form of the signature.

Signature	/Elaine C. Berlin/	Date (YYYY-MM-DD)	2017-06-02
Name/Print	Elaine C. Berlin	Registration Number	61194

This collection of information is required by 37 CFR 1.97 and 1.98. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 1 hour to complete, including gathering, preparing and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

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The Privacy Act of 1974 (P.L. 93-579) requires that you be given certain information in connection with your submission of the attached form related to a patent application or patent. Accordingly, pursuant to the requirements of the Act, please be advised that: (1) the general authority for the collection of this information is 35 U.S.C. 2(b)(2); (2) furnishing of the information solicited is voluntary; and (3) the principal purpose for which the information is used by the U.S. Patent and Trademark Office is to process and/or examine your submission related to a patent application or patent. If you do not furnish the requested information, the U.S. Patent and Trademark Office may not be able to process and/or examine your submission, which may result in termination of proceedings or abandonment of the application or expiration of the patent.

The information provided by you in this form will be subject to the following routine uses:

1. The information on this form will be treated confidentially to the extent allowed under the Freedom of Information Act (5 U.S.C. 552) and the Privacy Act (5 U.S.C. 552a). Records from this system of records may be disclosed to the Department of Justice to determine whether the Freedom of Information Act requires disclosure of these record s.

2. A record from this system of records may be disclosed, as a routine use, in the course of presenting evidence to a court, magistrate, or administrative tribunal, including disclosures to opposing counsel in the course of settlement negotiations.

3. A record in this system of records may be disclosed, as a routine use, to a Member of Congress submitting a request involving an individual, to whom the record pertains, when the individual has requested assistance from the Member with respect to the subject matter of the record.

4. A record in this system of records may be disclosed, as a routine use, to a contractor of the Agency having need for the information in order to perform a contract. Recipients of information shall be required to comply with the requirements of the Privacy Act of 1974, as amended, pursuant to 5 U.S.C. 552a(m).

5. A record related to an International Application filed under the Patent Cooperation Treaty in this system of records may be disclosed, as a routine use, to the International Bureau of the World Intellectual Property Organization, pursuant to the Patent Cooperation Treaty.

6. A record in this system of records may be disclosed, as a routine use, to another federal agency for purposes of National Security review (35 U.S.C. 181) and for review pursuant to the Atomic Energy Act (42 U.S.C. 218(c)).

7. A record from this system of records may be disclosed, as a routine use, to the Administrator, General Services, or his/her designee, during an inspection of records conducted by GSA as part of that agency's responsibility to recommend improvements in records management practices and programs, under authority of 44 U.S.C. 2904 and 2906. Such disclosure shall be made in accordance with the GSA regulations governing inspection of records for this purpose, and any other relevant (i.e., GSA or Commerce) directive. Such disclosure shall not be used to make determinations about individuals.

8. A record from this system of records may be disclosed, as a routine use, to the public after either publication of the application pursuant to 35 U.S.C. 122(b) or issuance of a patent pursuant to 35 U.S.C. 151. Further, a record may be disclosed, subject to the limitations of 37 CFR 1.14, as a routine use, to the public if the record was filed in an application which became abandoned or in which the proceedings were terminated and which application is referenced by either a published application, an application open to public inspections or an issued patent.

9. A record from this system of records may be disclosed, as a routine use, to a Federal, State, or local law enforcement agency, if the USPTO becomes aware of a violation or potential violation of law or regulation.

Search Notes	Application/Control No.	Applicant(s)/Patent Under Reexamination
	14984156	SHATALOV ET AL.
	Examiner	Art Unit
	FAZLI ERDEM	2826

CPC- SEARCHED		
Symbol	Date	Examiner
H01L33/10	2/2/2017	FE
H01L33/007	2/2/2017	FE
H01L33/32	2/2/2017	FE

CPC COMBINATION SETS - SEARCHED		
Symbol	Date	Examiner

US CLASSIFICATION SEARCHED			
Class	Subclass	Date	Examiner

* See search history printout included with this form or the SEARCH NOTES box below to determine the scope of the search.

SEARCH NOTES		
Search Notes	Date	Examiner
H01L33/10	2/2/2017	FE
H01L33/007	2/2/2017	FE
H01L33/32	2/2/2017	FE
Inventors are searched	2/2/2017	FE
Assignee is searched	2/2/2017	FE
CPC search limited with text is conducted	2/2/2017	FE
Searched 257/94 limited with text	2/2/2017	FE
EAST Search history is attached	2/2/2017	FE
Updated EAST Search history is attached	7/31/2017	FE

INTERFERENCE SEARCH

US Class/ CPC Symbol	US Subclass / CPC Group	Date	Examiner

EAST Search History

EAST Search History (Prior Art)

Ref #	Hits	Search Query	DBs	Default Operator	Plurals	Time Stamp
S212	56	nitride near2 semiconductor same inhomogeneous	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2017/07/31 10:58
S213	6	nitride near2 semiconductor same inhomogeneous same level	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2017/07/31 10:58
S214	2	nitride near2 semiconductor same inhomogeneous same level same transparent	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2017/07/31 10:59
S215	2	nitride near2 semiconductor same inhomogeneous same level same transparent same offset	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2017/07/31 11:07
S216	3	inhomogeneous same level same transparent same offset	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2017/07/31 11:30
S217	2	group near III same level same transparent same offset	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2017/07/31 11:31
S218	136	group near III same level same transparent	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2017/07/31 11:33
S219	55	group near III same level same	US-PGPUB;	OR	ON	2017/07/31

		transparent same nitride	USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB			11:34
S220	23	group near III same level same transparent same nitride and offset	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2017/07/31 11:34
S221	3	group near III same level same transparent same nitride and offset.clm.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2017/07/31 11:35
S222	148	(US-20160336483-$ or US-20160118536-$ or US-20150295133-$ or US-20170005224-$ or US-20160380150-$ or US-20160343901-$ or US-20140134773-$ or US-20160315449-$ or US-20160315219-$ or US-20160260867-$ or US-20160247885-$ or US-20160093771-$ or US-20140191261-$ or US-20140239312-$ or US-20160190387-$ or US-20160172544-$ or US-20140096669-$ or US-20160155902-$ or US-20160149099-$ or US-20160118535-$ or US-20160118534-$ or US-20160118531-$ or US-20160111618-$ or US-20160064631-$ or US-20130193409-$ or US-20160058020-$).did. or (US-20160049551-$ or US-20160035936-$ or US-20150297767-$ or US-20150255672-$ or US-20150228855-$ or US-20150179751-$ or US-20150165079-$ or US-20150108428-$ or US-20150091043-$ or US-20150083994-$ or US-20150069270-$ or US-20160197228-$ or US-20140346441-$ or US-20070081081-$ or US-20160211412-$ or US-20140110734-$ or US-20140158980-$ or US-20140064314-$ or US-20140016660-$ or US-20130320352-$ or US-20130146907-$ or US-20090272993-$ or US-20130277642-$ or US-20140110754-$ or US-20130193480-$ or US-20160225941-$ or US-20130055694-$).did. or (US-20130161305-$ or US-20070196682-$ or US-20150372193-$ or US-20160322535-$ or US-20130256828-$ or US-20080182403-$ or US-20070117348-$ or US-20030224591-$ or US-20140191284-$ or US-20140000693-$ or US-20080230815-$ or US-20130270514-$ or US-20110013656-$ or US-20100001375-$ or US-20020197830-$ or US-20120112188-$ or US-20120001220-$ or US-20110147791-$ or	US-PGPUB; USPAT; USOCR; FPRS; EPO; DERWENT	OR	ON	2017/07/31 11:36

		US-20020137249-$ or US-20140332374-$ or US-20140061057-$ or US-20040004215-$ or US-20070278518-$ or US-20070228416-$ or US-20130052463-$ or US-20100290675-$ or US-20160118490-$).did. or (US-20160111501-$ or US-20130240945-$ or US-20040159843-$ or US-20090180505-$ or US-20110005570-$ or US-20080150085-$ or US-20060267043-$ or US-20150349187-$ or US-20130181219-$ or US-20140346566-$ or US-20120165759-$ or US-20110089440-$ or US-20100123268-$ or US-20070145417-$ or US-20130264570-$ or US-20160365475-$ or US-20160365284-$ or US-20110188530-$ or US-20150069217-$ or US-20050285541-$ or US-20140349427-$ or US-20140147650-$ or US-20020173089-$ or US-20100126570-$).did. or (US-9331244-$ or US-9406840-$ or US-7812366-$ or US-9281441-$ or US-9312428-$ or US-4148132-$ or US-9105792-$ or US-9397260-$ or US-7361973-$ or US-7485516-$ or US-8293618-$ or US-7332795-$ or US-8886334-$ or US-8097926-$ or US-8372726-$ or US-4990989-$ or US-4894703-$ or US-9450124-$ or US-6376864-$ or US-4891093-$ or US-4888085-$).did. or (US-3351698-$).did. or (WO-2014179523-$ or WO-2013126828-$ or WO-2015175369-$ or CN-104979440-$ or KR-20150041557-$ or KR-20160025069-$ or KR-20140110754-$ or KR-20100012827-$ or KR-20000003968-$ or WO-2009005227-$).did. or (WO-2009005227-$).did. or (US-20160197228-$ or US-20160118536-$ or WO-2013082592-$ or US-20140239312-$ or US-20160336483-$ or US-20120217496-$ or WO-2012000114-$ or US-20110315956-$ or WO-2010048537-$).did.				
S223	42	S222 and offset.clm.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2017/07/31 11:36
S224	3	S222 and offset.clm. and inhomogeneous.clm.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2017/07/31 11:36
S225	3	("5602418" | "20160118536" | "20150243840").PN.	US-PGPUB; USPAT	OR	ON	2017/07/31 11:52
S226	130	("5602418" | "20160118536" | "20150243840")	US-PGPUB; USPAT	OR	ON	2017/07/31 11:52
S227	54	S226 and single near2 layer	US-PGPUB;	OR	ON	2017/07/31

			USPAT			11:52
S228	0	S226 and (homogeneous or inhomogeneous) and single near2 layer	US-PGPUB; USPAT	OR	ON	2017/07/31 11:53
S229	148	(US-20160336483-$ or US-20160118536-$ or US-20150295133-$ or US-20170005224-$ or US-20160380150-$ or US-20160343901-$ or US-20140134773-$ or US-20160315449-$ or US-20160315219-$ or US-20160260867-$ or US-20160247885-$ or US-20160093771-$ or US-20140191261-$ or US-20140239312-$ or US-20160190387-$ or US-20160172544-$ or US-20140096669-$ or US-20160155902-$ or US-20160149099-$ or US-20160118535-$ or US-20160118534-$ or US-20160118531-$ or US-20160111618-$ or US-20160064631-$ or US-20130193409-$ or US-20160058020-$).did. or (US-20160049551-$ or US-20160035936-$ or US-20150297767-$ or US-20150255672-$ or US-20150228855-$ or US-20150179751-$ or US-20150165079-$ or US-20150108428-$ or US-20150091043-$ or US-20150083994-$ or US-20150069270-$ or US-20160197228-$ or US-20140346441-$ or US-20070081081-$ or US-20160211412-$ or US-20140110734-$ or US-20140158980-$ or US-20140064314-$ or US-20140016660-$ or US-20130320352-$ or US-20130146907-$ or US-20090272993-$ or US-20130277642-$ or US-20140110754-$ or US-20130193480-$ or US-20160225941-$ or US-20130055694-$).did. or (US-20130161305-$ or US-20070196682-$ or US-20150372193-$ or US-20160322535-$ or US-20130256828-$ or US-20080182403-$ or US-20070117348-$ or US-20030224591-$ or US-20140191284-$ or US-20140000693-$ or US-20080230815-$ or US-20130270514-$ or US-20110013656-$ or US-20100001375-$ or US-20020197830-$ or US-20120112188-$ or US-20120001220-$ or US-20110147791-$ or US-20020137249-$ or US-20140332374-$ or US-20140061057-$ or US-20040004215-$ or US-20070278518-$ or US-20070228416-$ or US-20130052463-$ or US-20100290675-$ or US-20160118490-$).did. or (US-20160111501-$ or US-20130240945-$ or US-20040159843-$ or US-20090180505-$ or US-20110005570-$ or US-20080150085-$ or US-20060267043-$ or US-20150349187-$ or US-20130181219-$ or US-20140346566-$ or US-20120165759-$ or US-20110089440-$ or US-20100123268-$ or US-20070145417-$ or US-20130264570-$ or US-20160365475-$ or US-20160365284-$ or US-20110188530-$ or US-20150069217-$ or US-20050285541-$ or US-	US-PGPUB; USPAT; USOCR; FPRS; EPO; DERWENT	OR	ON	2017/07/31 11:53

		20140349427-$ or US-20140147650-$ or US-20020173089-$ or US-20100126570-$).did. or (US-9331244-$ or US-9406840-$ or US-7812366-$ or US-9281441-$ or US-9312428-$ or US-4148132-$ or US-9105792-$ or US-9397260-$ or US-7361973-$ or US-7485516-$ or US-8293618-$ or US-7332795-$ or US-8886334-$ or US-8097926-$ or US-8372726-$ or US-4990989-$ or US-4894703-$ or US-9450124-$ or US-6376864-$ or US-4891093-$ or US-4888085-$).did. or (US-3351698-$).did. or (WO-2014179523-$ or WO-2013126828-$ or WO-2015175369-$ or CN-104979440-$ or KR-20150041557-$ or KR-20160025069-$ or KR-20140110754-$ or KR-20100012827-$ or KR-20000003968-$ or WO-2009005227-$).did. or (WO-2009005227-$).did. or (US-20160197228-$ or US-20160118536-$ or WO-2013082592-$ or US-20140239312-$ or US-20160336483-$ or US-20120217496-$ or WO-2012000114-$ or US-20110315956-$ or WO-2010048537-$).did.				
S230	7	S229 and (homogeneous or inhomogeneous) and single near2 layer	US-PGPUB; USPAT	OR	ON	2017/07/31 11:54
S231	7	S229 and (homogeneous or inhomogeneous) and single near layer	US-PGPUB; USPAT	OR	ON	2017/07/31 11:54
S232	1	S229 and (homogeneous or inhomogeneous) same single near layer	US-PGPUB; USPAT	OR	ON	2017/07/31 11:54
S233	1	group near III near10 nitride near10 semiconductor same active same metallic same inhomogeneous	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2017/07/31 11:56
S234	6	group near III near10 nitride near10 semiconductor same active same contact same inhomogeneous	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2017/07/31 11:56
S235	8	"9331244"	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2017/07/31 12:17
S236	5	S235 and (metal or metallic or contact).clm.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2017/07/31 12:18
S237	3	S235 and inhomogeneous.clm. and transparent.clm.	US-PGPUB; USPAT;	OR	ON	2017/07/31 12:20

			USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB			
S238	2	14/984156	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2017/07/31 12:47
S239	0	S238 and nitride near2 semiconductor near2 layer near2 single near2 layer	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2017/07/31 12:47
S240	2	S238 and nitride near2 semiconductor near2 layer	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2017/07/31 12:47
S241	2	S238 and nitride near2 semiconductor near2 layer same active same contact	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2017/07/31 12:48
S242	2	S238 and nitride near2 semiconductor near2 layer	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2017/07/31 12:55
S243	2	S238 and nitride near2 semiconductor near2 layer near10 between	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2017/07/31 12:59
S244	3	14/189,012 and nitride near2 semiconductor near2 layer near10 between	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2017/07/31 12:59
S245	6	14/189,012	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2017/07/31 13:00

S246	3	S245 and nitride near2 semiconductor near2 layer near10 between	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2017/07/31 13:00
S247	6	S245 and nitride near2 semiconductor near2 layer	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2017/07/31 13:00

7/ 31/ 2017 2:14:49 PM
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Index of Claims	Application/Control No.	Applicant(s)/Patent Under Reexamination
	14984156	SHATALOV ET AL.
	Examiner	**Art Unit**
	FAZLI ERDEM	2826

✓	Rejected	-	Cancelled	N	Non-Elected	A	Appeal
=	Allowed	÷	Restricted	I	Interference	O	Objected

☐ Claims renumbered in the same order as presented by applicant ☐ CPA ☐ T.D. ☐ R.1.47

CLAIM		DATE								
Final	Original	02/02/2017	07/31/2017							
	1	✓	✓							
	2	✓	✓							
	3	✓	✓							
	4	✓	✓							
	5	✓	✓							
	6	✓	✓							
	7	✓	✓							
	8	✓	✓							
	9	✓	✓							
	10	✓	✓							
	11	✓	✓							
	12	✓	✓							
	13	✓	✓							
	14	✓	✓							
	15	✓	✓							
	16	✓	✓							
	17	✓	✓							
	18	✓	✓							
	19	✓	✓							
	20	✓	✓							

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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
14/984,156	12/30/2015	Maxim S. Shatalov	SETI-0110-CIP-US	5890

11698 7590 09/01/2017

LaBatt, LLC (SET)
PO Box 630
Valatie, NY 12184

EXAMINER
ERDEM, FAZLI

ART UNIT	PAPER NUMBER
2826	

NOTIFICATION DATE	DELIVERY MODE
09/01/2017	ELECTRONIC

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

adobrinsky@s-et.com
national@labattlaw.com

Applicant-Initiated Interview Summary	Application No.	Applicant(s)	
	14/984,156	SHATALOV ET AL.	
	Examiner	Art Unit	
	FAZLI ERDEM	2826	

All participants (applicant, applicant's representative, PTO personnel):

(1) *Fazli Erdem*. (3)_____.

(2) *David Goldman*. (4)_____.

Date of Interview: *25 August 2017*.

Type: ☒ Telephonic ☐ Video Conference
☐ Personal [copy given to: ☐ applicant ☐ applicant's representative]

Exhibit shown or demonstration conducted: ☐ Yes ☐ No.
If Yes, brief description: _____.

Issues Discussed ☐101 ☒112 ☐102 ☒103 ☐Others
(For each of the checked box(es) above, please describe below the issue and detailed description of the discussion)

Claim(s) discussed: *1 and 8*.

Identification of prior art discussed: *Saxler '514 and '956*.

Substance of Interview
(For each issue discussed, provide a detailed description and indicate if agreement was reached. Some topics may include: identification or clarification of a reference or a portion thereof, claim interpretation, proposed amendments, arguments of any applied references etc...)

Examiner will withdraw the 35 USC 112 rejection and 35 USC 103 rejection based on Saxler if the distinguishing amendments made to differentiate between "layer" and "level". Examiner suggested paragraph 0038 of the application as published to make the amendment i.e. semicondcutor layer having multiple levels along the height direction. Examiner brought Jain et al. 2014/0134773 as possible potential prior art which can be overcome with a joint ownership statement. Examiner and the applicant agreed that a terminal disclaimer should be filed in order to overcome the double patenting rejections.

Applicant recordation instructions: The formal written reply to the last Office action must include the substance of the interview. (See MPEP section 713.04). If a reply to the last Office action has already been filed, applicant is given a non-extendable period of the longer of one month or thirty days from this interview date, or the mailing date of this interview summary form, whichever is later, to file a statement of the substance of the interview

Examiner recordation instructions: Examiners must summarize the substance of any interview of record. A complete and proper recordation of the substance of an interview should include the items listed in MPEP 713.04 for complete and proper recordation including the identification of the general thrust of each argument or issue discussed, a general indication of any other pertinent matters discussed regarding patentability and the general results or outcome of the interview, to include an indication as to whether or not agreement was reached on the issues raised.

☐ Attachment

/FAZLI ERDEM/
Primary Examiner, Art Unit 2826
8/25/2017

Summary of Record of Interview Requirements

Manual of Patent Examining Procedure (MPEP), Section 713.04, Substance of Interview Must be Made of Record
A complete written statement as to the substance of any face-to-face, video conference, or telephone interview with regard to an application must be made of record in the application whether or not an agreement with the examiner was reached at the interview.

Title 37 Code of Federal Regulations (CFR) § 1.133 Interviews
Paragraph (b)

In every instance where reconsideration is requested in view of an interview with an examiner, a complete written statement of the reasons presented at the interview as warranting favorable action must be filed by the applicant. An interview does not remove the necessity for reply to Office action as specified in §§ 1.111, 1.135. (35 U.S.C. 132)

37 CFR §1.2 Business to be transacted in writing.
All business with the Patent or Trademark Office should be transacted in writing. The personal attendance of applicants or their attorneys or agents at the Patent and Trademark Office is unnecessary. The action of the Patent and Trademark Office will be based exclusively on the written record in the Office. No attention will be paid to any alleged oral promise, stipulation, or understanding in relation to which there is disagreement or doubt.

The action of the Patent and Trademark Office cannot be based exclusively on the written record in the Office if that record is itself incomplete through the failure to record the substance of interviews.

It is the responsibility of the applicant or the attorney or agent to make the substance of an interview of record in the application file, unless the examiner indicates he or she will do so. It is the examiner's responsibility to see that such a record is made and to correct material inaccuracies which bear directly on the question of patentability.

Examiners must complete an Interview Summary Form for each interview held where a matter of substance has been discussed during the interview by checking the appropriate boxes and filling in the blanks. Discussions regarding only procedural matters, directed solely to restriction requirements for which interview recordation is otherwise provided for in Section 812.01 of the Manual of Patent Examining Procedure, or pointing out typographical errors or unreadable script in Office actions or the like, are excluded from the interview recordation procedures below. Where the substance of an interview is completely recorded in an Examiners Amendment, no separate Interview Summary Record is required.

The Interview Summary Form shall be given an appropriate Paper No., placed in the right hand portion of the file, and listed on the "Contents" section of the file wrapper. In a personal interview, a duplicate of the Form is given to the applicant (or attorney or agent) at the conclusion of the interview. In the case of a telephone or video-conference interview, the copy is mailed to the applicant's correspondence address either with or prior to the next official communication. If additional correspondence from the examiner is not likely before an allowance or if other circumstances dictate, the Form should be mailed promptly after the interview rather than with the next official communication.

The Form provides for recordation of the following information:
- Application Number (Series Code and Serial Number)
- Name of applicant
- Name of examiner
- Date of interview
- Type of interview (telephonic, video-conference, or personal)
- Name of participant(s) (applicant, attorney or agent, examiner, other PTO personnel, etc.)
- An indication whether or not an exhibit was shown or a demonstration conducted
- An identification of the specific prior art discussed
- An indication whether an agreement was reached and if so, a description of the general nature of the agreement (may be by attachment of a copy of amendments or claims agreed as being allowable). Note: Agreement as to allowability is tentative and does not restrict further action by the examiner to the contrary.
- The signature of the examiner who conducted the interview (if Form is not an attachment to a signed Office action)

It is desirable that the examiner orally remind the applicant of his or her obligation to record the substance of the interview of each case. It should be noted, however, that the Interview Summary Form will not normally be considered a complete and proper recordation of the interview unless it includes, or is supplemented by the applicant or the examiner to include, all of the applicable items required below concerning the substance of the interview.

A complete and proper recordation of the substance of any interview should include at least the following applicable items:
1) A brief description of the nature of any exhibit shown or any demonstration conducted,
2) an identification of the claims discussed,
3) an identification of the specific prior art discussed,
4) an identification of the principal proposed amendments of a substantive nature discussed, unless these are already described on the Interview Summary Form completed by the Examiner,
5) a brief identification of the general thrust of the principal arguments presented to the examiner,
   (The identification of arguments need not be lengthy or elaborate. A verbatim or highly detailed description of the arguments is not required. The identification of the arguments is sufficient if the general nature or thrust of the principal arguments made to the examiner can be understood in the context of the application file. Of course, the applicant may desire to emphasize and fully describe those arguments which he or she feels were or might be persuasive to the examiner.)
6) a general indication of any other pertinent matters discussed, and
7) if appropriate, the general results or outcome of the interview unless already described in the Interview Summary Form completed by the examiner.

Examiners are expected to carefully review the applicant's record of the substance of an interview. If the record is not complete and accurate, the examiner will give the applicant an extendable one month time period to correct the record.

Examiner to Check for Accuracy

If the claims are allowable for other reasons of record, the examiner should send a letter setting forth the examiner's version of the statement attributed to him or her. If the record is complete and accurate, the examiner should place the indication, "Interview Record OK" on the paper recording the substance of the interview along with the date and the examiner's initials.

Doc Code: DIST.E.FILE **Document Description: Electronic Terminal Disclaimer - Filed**	PTO/SB/26 U.S. Patent and Trademark Office Department of Commerce

Electronic Petition Request	**TERMINAL DISCLAIMER TO OBVIATE A DOUBLE PATENTING REJECTION OVER A "PRIOR" PATENT**
Application Number	14984156
Filing Date	30-Dec-2015
First Named Inventor	Maxim Shatalov
Attorney Docket Number	SETI-0110-CIP-US
Title of Invention	Semiconductor Structure with Inhomogeneous Regions

☒ Filing of terminal disclaimer does not obviate requirement for response under 37 CFR 1.111 to outstanding Office Action

☒ This electronic Terminal Disclaimer is not being used for a Joint Research Agreement.

Owner	Percent Interest
Sensor Electronic Technology, Inc.	100%

The owner(s) with percent interest listed above in the instant application hereby disclaims, except as provided below, the terminal part of the statutory term of any patent granted on the instant application which would extend beyond the expiration date of the full statutory term of prior patent number(s)

9331244

as the term of said prior patent is presently shortened by any terminal disclaimer. The owner hereby agrees that any patent so granted on the instant application shall be enforceable only for and during such period that it and the prior patent are commonly owned. This agreement runs with any patent granted on the instant application and is binding upon the grantee, its successors or assigns.

In making the above disclaimer, the owner does not disclaim the terminal part of the term of any patent granted on the instant application that would extend to the expiration date of the full statutory term of the prior patent, "as the term of said prior patent is presently shortened by any terminal disclaimer," in the event that said prior patent later:
- expires for failure to pay a maintenance fee;
- is held unenforceable;
- is found invalid by a court of competent jurisdiction;
- is statutorily disclaimed in whole or terminally disclaimed under 37 CFR 1.321;
- has all claims canceled by a reexamination certificate;
- is reissued; or
- is in any manner terminated prior to the expiration of its full statutory term as presently shortened by any terminal disclaimer.

◉ Terminal disclaimer fee under 37 CFR 1.20(d) is included with Electronic Terminal Disclaimer request.

○	I certify, in accordance with 37 CFR 1.4(d)(4), that the terminal disclaimer fee under 37 CFR 1.20(d) required for this terminal disclaimer has already been paid in the above-identified application.

Applicant claims the following fee status:

○ Small Entity

○ Micro Entity

◉ Regular Undiscounted

I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code and that such willful false statements may jeopardize the validity of the application or any patent issued thereon.

THIS PORTION MUST BE COMPLETED BY THE SIGNATORY OR SIGNATORIES

I certify, in accordance with 37 CFR 1.4(d)(4) that I am:

◉ An attorney or agent registered to practice before the Patent and Trademark Office who is of record in this application

Registration Number 48301

○ A sole inventor

○ A joint inventor; I certify that I am authorized to sign this submission on behalf of all of the inventors as evidenced by the power of attorney in the application

○ A joint inventor; all of whom are signing this request

Signature	/John W. LaBatt/
Name	John W. LaBatt

*Statement under 37 CFR 3.73(b) is required if terminal disclaimer is signed by the assignee (owner).
Form PTO/SB/96 may be used for making this certification. See MPEP § 324.

Electronic Patent Application Fee Transmittal

Application Number:	14984156
Filing Date:	30-Dec-2015
Title of Invention:	Semiconductor Structure with Inhomogeneous Regions
First Named Inventor/Applicant Name:	Maxim S. Shatalov
Filer:	John W LaBatt
Attorney Docket Number:	SETI-0110-CIP-US

Filed as Large Entity

Filing Fees for Utility under 35 USC 111(a)

Description	Fee Code	Quantity	Amount	Sub-Total in USD($)
Basic Filing:				
STATUTORY OR TERMINAL DISCLAIMER	1814	1	160	160
Pages:				
Claims:				
Miscellaneous-Filing:				
Petition:				
Patent-Appeals-and-Interference:				
Post-Allowance-and-Post-Issuance:				

Description	Fee Code	Quantity	Amount	Sub-Total in USD($)
Extension-of-Time:				
Miscellaneous:				
			Total in USD ($)	**160**

Doc Code: DISQ.E.FILE
Document Description: Electronic Terminal Disclaimer – Approved

Application No.: 14984156

Filing Date: 30-Dec-2015

Applicant/Patent under Reexamination: Shatalov

Electronic Terminal Disclaimer filed on October 4, 2017

☒ APPROVED

This patent is subject to a terminal disclaimer

☐ DISAPPROVED

Approved/Disapproved by: Electronic Terminal Disclaimer automatically approved by EFS-Web

U.S. Patent and Trademark Office

Electronic Acknowledgement Receipt

EFS ID:	30559541
Application Number:	14984156
International Application Number:	
Confirmation Number:	5890
Title of Invention:	Semiconductor Structure with Inhomogeneous Regions
First Named Inventor/Applicant Name:	Maxim S. Shatalov
Customer Number:	11698
Filer:	John W LaBatt
Filer Authorized By:	
Attorney Docket Number:	SETI-0110-CIP-US
Receipt Date:	04-OCT-2017
Filing Date:	30-DEC-2015
Time Stamp:	11:15:40
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	yes
Payment Type	CARD
Payment was successfully received in RAM	$160
RAM confirmation Number	100417INTEFSW11153800
Deposit Account	
Authorized User	

The Director of the USPTO is hereby authorized to charge indicated fees and credit any overpayment as follows:

File Listing:

Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1	Terminal Disclaimer-Filed (Electronic)	eTerminal-Disclaimer.pdf	33473 6f3db1bfd9df6ff957ec0d497782e49b88671dd6	no	2
Warnings:					
Information:					
2	Fee Worksheet (SB06)	fee-info.pdf	30711 7ae8574d32d820c5e3cbd4eb8fc50d98e0082776	no	2
Warnings:					
Information:					
		Total Files Size (in bytes):	64184		

This Acknowledgement Receipt evidences receipt on the noted date by the USPTO of the indicated documents, characterized by the applicant, and including page counts, where applicable. It serves as evidence of receipt similar to a Post Card, as described in MPEP 503.

New Applications Under 35 U.S.C. 111

If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application.

National Stage of an International Application under 35 U.S.C. 371

If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.

New International Application Filed with the USPTO as a Receiving Office

If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Serial No.:	14/984,156	Conf. No.:	5890
Filing Date:	30 December 2015	Art Unit:	2826
Inventor(s):	Shatalov et al.	Examiner:	Erdem, Fazli
Title:	Semiconductor Structure with Inhomogeneous Regions	Docket No.:	SETI-0110-CIP-US

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Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

AFTER FINAL AMENDMENT

In response to the Final Office Action dated 4 August 2017 (hereafter the "Final"), Applicant requests further consideration and examination of the above-identified patent application in view of the following amendments and remarks. Applicant is submitting an After Final Consideration Pilot Program Request form with this correspondence, which contains Applicant's certification and request for consideration of this reply under the After Final Consideration Pilot 2.0 (AFCP 2.0) program.

AMENDMENTS TO THE CLAIMS

The following listing of claims replaces all prior versions, and listings, of claims in the application.

1. (Currently amended) A semiconductor heterostructure, comprising:

an active region;

a metallic contact;

a group III nitride semiconductor layer located between the active region and the metallic contact, the semiconductor layer including a plurality of inhomogeneous regions arranged within multiple levels of the semiconductor layer along a height direction of the semiconductor layer, wherein some of the inhomogeneous regions in a first level of the semiconductor layer are vertically offset from inhomogeneous regions in a second level of the semiconductor layer, and wherein the plurality of inhomogeneous regions include one or more of a set of transparent regions, a set of reflective regions and/or a set of conductive regions, each of the inhomogeneous regions having a set of attributes differing from a group III nitride material forming the semiconductor layer.

2. (Original) The semiconductor heterostructure of claim 1, wherein each of the inhomogeneous regions in the first level and the second level of the semiconductor layer includes a set of reflective regions.

3. (Original) The semiconductor heterostructure of claim 1, wherein each of the plurality of inhomogeneous regions in the first level of the semiconductor layer extend into the

metallic contact and each of the plurality of inhomogeneous regions in the second level of the semiconductor layer are located at an interface of the semiconductor layer.

4. (Original) The semiconductor heterostructure of claim 1, wherein all of the inhomogeneous regions in the first level of the semiconductor layer are staggered with the inhomogeneous regions in the second level of the semiconductor layer to form a checkerboard arrangement of the inhomogeneous regions within the semiconductor layer.

5. (Original) The semiconductor heterostructure of claim 1, wherein the inhomogeneous regions in the first level of the semiconductor layer each has a surface contacting the metallic contact, wherein at least one metal protrusion from the metallic contact extends into each inhomogeneous region.

6. (Original) The semiconductor heterostructure of claim 5, wherein each of the inhomogeneous regions in the first level of the semiconductor layer comprises a set of conductive regions and each of the inhomogeneous regions in the second level of the semiconductor layer comprises a set of reflective regions.

7. (Original) The semiconductor heterostructure of claim 6, wherein each of the inhomogeneous regions in the second level of the semiconductor layer has at least one metal protrusion extending from the metallic contact into the semiconductor layer that is directed to a surface of the inhomogeneous region without contact thereof.

8. (Currently amended) A method, comprising:

fabricating a semiconductor heterostructure, wherein the semiconductor heterostructure comprises:

an active region;

a metallic contact;

a single group III nitride semiconductor layer located between the active region and the metallic contact, the semiconductor layer including a plurality of inhomogeneous regions arranged within multiple levels of the semiconductor layer along a height direction of the semiconductor layer, wherein some of the inhomogeneous regions in a first level of the semiconductor layer are vertically offset from inhomogeneous regions in a second level of the semiconductor layer, and wherein the plurality of inhomogeneous regions include one or more of a set of transparent regions, a set of reflective regions and/or a set of conductive regions, each of the inhomogeneous regions having a set of attributes differing from a group III nitride material forming the semiconductor layer.

9. (Original) The method of claim 8, wherein the fabricating includes:

epitaxially growing a portion of the group III nitride semiconductor layer;

forming at least one of the sets of inhomogeneous regions on a surface of the portion of the group III nitride semiconductor layer; and

epitaxially over-growing the group III nitride semiconductor layer after the forming.

10. (Original) The method of claim 9, wherein the forming includes:

depositing the at least one of the sets of inhomogeneous regions using one of: thermal evaporation, magnetron sputtering, ion-beam deposition, or laser beam evaporation; and

patterning the at least one of the sets of inhomogeneous regions using photolithography.

11. (Previously presented) An optoelectronic device, comprising:

a semiconductor heterostructure having a first side and a second side, the semiconductor heterostructure including:

a group III nitride semiconductor layer including a plurality of inhomogeneous regions, each inhomogeneous region having a set of attributes differing from a group III nitride material forming the semiconductor layer, wherein the plurality of inhomogeneous regions include:

a set of first inhomogeneous regions configured based on radiation having a target wavelength, wherein the set of first inhomogeneous regions are at least one of: transparent to the radiation or reflective of the radiation; and

a set of second inhomogeneous regions having a conductivity at least ten percent higher than a conductivity of the set of first inhomogeneous regions, wherein each of the sets of inhomogeneous regions occupy at least five percent of at least one of: a lateral planar area of the semiconductor layer or a volume of the semiconductor layer, and

wherein at least some of the sets of inhomogeneous regions do not fully overlap.

12. (Original) The optoelectronic device of claim 11, further comprising a first metallic contact having a plurality of connected metallic domains formed on the first side of the semiconductor heterostructure.

13. (Original) The optoelectronic device of claim 11, further comprising a plurality of roughness elements formed on the first side of the semiconductor heterostructure.

14. (Original) The optoelectronic device of claim 11, further comprising a plurality of metallic contact domains formed on the second side of the semiconductor heterostructure.

15. (Original) The optoelectronic device of claim 11, further comprising a plurality of reflective elements incorporated within the semiconductor heterostructure proximate a surface of the second side of the semiconductor heterostructure.

16. (Original) The optoelectronic device of claim 15, wherein the plurality of reflective elements comprise one of dielectrics, metallic reflective islands, Bragg mirrors and combinations thereof.

17. (Original) The optoelectronic device of claim 15, wherein the plurality of reflective elements comprise alternating layers of one of Hf_2O_3 and Al_2O_3, H_2O_3 and SiO_2, and Al_2O_3 and SiO_2.

18. (Original) The optoelectronic device of claim 11, further comprising a plurality of Bragg domains formed on the second side of the semiconductor heterostructure.

19. (Original) The optoelectronic device of claim 11, further comprising a second metallic contact having metallic domains formed on the second side of the semiconductor heterostructure, each of the metallic domains separated from an adjacent metallic domain by a predetermined spacing.

20. (Original) The optoelectronic device of claim 11, further comprising a passivation layer formed on the second side of the semiconductor heterostructure and a plurality of disjoint domains interspersed within the passivation layer.

REMARKS

With this response, Applicant amended claims 1 and 8. No new matter has been added. Applicant is not conceding that the claims prior to this amendment are not patentable over the prior art cited by the Examiner. The present amendment is only for facilitating expeditious prosecution of the present patent application. Applicant does not acquiesce in the correctness of the rejections and reserves the right to present specific arguments regarding any rejected claims not specifically addressed herein. Further, Applicant respectfully reserves the right to pursue the full scope of the subject matter of these claims and any others in one or more subsequent patent applications that claim priority to the present patent application.

Also, Applicant submits that this amendment, which is in compliance with 37 CFR §1.116(b), does not raise any new issues that would require further consideration and/or search. Entry and consideration of this amendment would take a minimal amount of time to determine whether it places the present patent application in condition for allowance. Accordingly, Applicant respectfully requests entry of this amendment and further examination and reconsideration of the present patent application per the AFCP 2.0.

Applicant Initiated Interview Summary

On August 25, 2017, Applicant's representative, David Goldman spoke with Examiner Fazli Erdem to discuss the outstanding rejections of claims 8-10 under 35 U.S.C. §112(a) or §112 (pre-AIA), first paragraph, and 35 U.S.C. §103 as allegedly being unpatentable over Saxler (US Patent Application Publication No. 2013/0270514),

hereafter "Saxler," in view of Saxler et al. (US Patent Application Publication No. 2004/0031956), hereafter "Saxler 2004."

In the discussion, the Examiner indicated that he would remove the §112(a) or §112 (pre-AIA), first paragraph rejection of claims 8-10 in light of the points raised by the Applicant which are summarized below in the section of this response that addresses the §112 rejection. With independent claim 8 interpreted with the "single" layer terminology, the Examiner indicated that he would remove the §103 rejection of claims 8-10 under Saxler in view of Saxler 2004. The distinctions between claims 8-10 and Saxler in view of Saxler 2004 are summarized below in the section of this response that addresses the §103 rejection.

During the discussion, the Examiner raised a concern regarding the term "multiple levels of the semiconductor layer" as set forth in claims 1 and 8. In particular, the Examiner submitted that a clarification was needed to distinguish the levels from the semiconductor layer. Without acquiescing to this concern, Applicant amended claims 1 and 8 to recite that the plurality of inhomogeneous regions are arranged within multiple levels of the semiconductor layer "along a height direction of the semiconductor layer" in order to expedite prosecution and obtain a Notice of Allowance. Paragraph 0038 is an example of a section in the application that provides support for the change made to claims 1 and 8. Applicant submits that the amendment to claims 1 and 8 distinguishes the levels from the semiconductor layer, and thus obviates the concern raised by the Examiner in the discussion.

The Examiner also noted that Jain et al. (US Patent Application Publication No. 2014/0134773), hereafter "Jain," is a reference that he could apply in a potential prior art rejection of the claimed invention. Applicant respectfully traverses any such prior art rejection of the claimed invention under Jain because this reference is ineffective as prior art. According to 35 U.S.C. §102(b)(2)(C):

> [a] disclosure shall not be prior art to a claimed invention under subsection [§102(a)(2)] if — … the subject matter disclosed and the claimed invention, not later than the effective filing date of the claimed invention, were owned by the same person or subject to an obligation of assignment to the same person.

In the present case, the claimed subject matter is directed to material that is disclosed by the parent application (US Patent No. 9,331,244) of the present continuation-in-part (CIP) application. Thus, the subject matter of the claims is afforded the effective filing date of the parent application, which is February 25, 2013. Jain has a publication date of May 15, 2014 which is after the effective filing date of February 25, 2013 for the claimed subject matter. In addition, Applicant submits that the claimed invention and Jain were owned by the same person or subject to an obligation of assignment to the same entity, Sensor Electronic Technology, Inc., not later than the effective filing date of the claimed invention. As set forth in section 2154.02(C) of the Manual of Patent Examining Procedure, this statement is sufficient to establish that the §102(b)(2)(C) exception applies. Because both provisions of §102(b)(2)(C) are met as evidenced above, Jain is not available as prior art against the claimed invention under either §102 or §103, and thus obviates the Examiner's view point regarding Jain as potential prior art against the claimed invention.

35 U.S.C. §112(a) or §112 (pre-AIA), First Paragraph Rejection of Claims 8-10

As mentioned above, claims 8-10 are rejected under 35 U.S.C. §112(a) or §112 (pre-AIA), first paragraph as allegedly failing to comply with the written description requirement. In particular, the Examiner alleged that the claims contain subject matter which was not described in the specification in such a way as to reasonably convey to one skilled in the relevant art that the inventor or a joint inventor, or for pre-AIA the inventor(s), at the time the application was filed, had possession of the claimed invention. More specifically, the Examiner submitted that the wording "single layer" in claim 8 does not have support in the specification as originally filed.

Applicant respectfully traverses the rejection of claims 8-10 under §112(a) or §112 (pre-AIA), first paragraph and submits that FIG. 7A is an example of a section in the application that provides support for the use of "a single group III nitride semiconductor layer." The term "single" is not expressly used in the written description that corresponds with the layer 70 in FIG. 7A, but the figure clearly shows that the layer 70 includes only one layer in number. Paragraph 0049 and FIG. 7A disclose that the layer 70 can include two levels (74A and 74B) each containing inhomogeneous regions.

According to the Guidelines for the Examination of Patent Applications Under the 35 U.S.C. 112(a) or Pre-AIA 35 U.S.C. 112, para. 1, "Written Description" Requirement, set forth in MPEP 2163 I, an applicant can show possession of the claimed invention by describing the claimed invention with all of its limitations using such descriptive means as words, structures, figures, diagrams, and formulas that fully set forth the claimed invention. *Lockwood v. Amer. Airlines, Inc.,* 107 F.3d 1565, 1572, 41USPQ2d 1961, 1966 (Fed. Cir. 1997). Because possession of the claimed invention may be shown in

any number of ways, there is no *in haec verba* requirement (MPEP 2163 I B). Newly added claim limitations must be supported in the specification through express, implicit, or inherent disclosure (*Id.*).

In the present case, Applicant submits that the single layer terminology is at least implicitly disclosed by reference element 70 in FIG. 7A of the drawings. Per MPEP 2163 II A 3, drawings alone may provide a 'written description' of an invention. Those of ordinary skill in the art would understand that the representation of the semiconductor layer 70 in FIG. 7A at least implies (and arguably expressly describes) that the semiconductor layer 70 includes a single layer with multiple levels of inhomogeneous regions, as the layer 70 includes only one layer in number.

In view of the foregoing, Applicant respectfully submits that ordinarily skilled artisans would reasonably conclude that Applicant possessed the claimed "single group III nitride semiconductor layer" on the basis of the aforementioned implicit disclosure provided through FIG. 7A. Thus, the present application adequately describes the claimed single layer terminology.

With regard to the Examiner's comments on page 6 of the Final, Applicant notes that the cited paragraphs from the published application (US 2016/0118536) do not appear to be pertinent to FIGS. 7A and 11C. In particular, paragraph 0052 discusses possible options for what a semiconductor structure can entail, while paragraph 0061 is directed to FIG. 12. Nevertheless, Applicant submits the Examiner's remarks do not negate Applicant's view that the layer 70 in FIG. 7A supports the use of the single layer terminology, and more specifically, "a single group III nitride semiconductor layer."

Even though paragraph 0049 describes the layer 70 as "a semiconductor base layer" and not a "semiconductor layer," Applicant respectfully submits that the layer 70 in FIG. 7A is a sole or single semiconductor layer that can include a group III nitride material per paragraph 0032. Thus, a single group III nitride semiconductor layer is reasonable terminology to use in a claim to represent the layer 70 of FIG. 7A. The use of the term "base" is used to generally convey the understanding that the layer 70 can act as a foundation for the multiple levels of the inhomogeneous regions in the layer. The term "base" is not essential terminology, and thus its recitation in the claims is not imperative.

The other comment in page 6 of the Final that pertains to the term "semiconductor layer(s)," appears to refer to paragraph 0058. This paragraph with this instance of "semiconductor layer(s)" generally refers to the epitaxial growth of the semiconductor layers in all of the various embodiments described in the application, some of which have multiple layers, and some like FIG. 7A which have a single semiconductor layer. Therefore, Applicant submits that there is nothing in paragraph 0058 which refutes Applicant's view that the layer 70 in FIG. 7A supports "a single group III nitride semiconductor layer."

In light of the above remarks, Applicant submits that the Examiner's concerns raised in the §112(a) or §112 (pre-AIA), first paragraph rejection for purportedly failing to comply with the written description requirement are obviated. Accordingly, Applicant respectfully requests that the Examiner reconsider and remove the rejection of claims 8-10 under §112(a) or §112 (pre-AIA), first paragraph.

35 U.S.C. §103 Rejection of Claims 8-10

As noted above, claims 8-10 are rejected under 35 U.S.C. §103 as allegedly being unpatentable over Saxler in view of Saxler 2004.

Applicant submits that claims 8-10 are patentably distinguishable over Saxler in view of Saxler 2004. As contended in Applicant's response dated 8 May 2017, the combination of Saxler in view of Saxler 2004 does not disclose or suggest a single semiconductor layer having a plurality of inhomogeneous regions arranged within multiple levels of the single semiconductor layer. At best, the combination of Saxler in view of Saxler 2004 discloses one level of inhomogeneous regions arranged within a single semiconductor layer.

For example, FIG. 6 of Saxler shows a first set of discontinuous regions 12A in a first N-GAN layer 22B and another set of discontinuous regions 12B in a second N-GAN layer 22C. Both the first N-GAN layer 22B and the second N-GAN layer 22C are separate and distinct semiconductor layers. Each of these layers only has a single level of discontinuous regions therein and not multiple levels. Similarly, FIG. 4 of Saxler 2004 shows a first set of discontinuous regions 34 in a first layer 32 and another set of discontinuous regions 40 in a third layer 38, with a second layer 36 separating layers 32 and 38. Both the first layer 32 and the third layer 38 are separate and distinct semiconductor layers. Each of these layers in Saxler 2004 only have a single level of discontinuous regions and not multiple levels. In view of these distinctions, Saxler in view of Saxler 2004 does not disclose or suggest a single semiconductor layer having a plurality of inhomogeneous regions arranged within multiple levels of the single semiconductor layer.

Accordingly, Applicant respectfully submits that Saxler in view of Saxler 2004 does not disclose or suggest all of the limitations set forth in claim 8. Claims 9-10 depend directly or indirectly from now presumably allowable claim 8, and thus are allowable by dependency. Accordingly, Applicant submits that claims 8-10 are patentably distinguishable over Saxler in view of Saxler 2004. Therefore, Applicant requests that the Examiner remove the §103 rejection of claims 8-10 under Saxler in view of Saxler 2004.

Obvious-Type Double Patenting

Claims 1-20 are rejected on the ground of non-statutory double patenting as being unpatentable over claims 1-21 of U.S. Patent No. 9,331,244.

Without acquiescing to the appropriateness of the obviousness-type double patenting rejection, enclosed herewith is a terminal disclaimer that disclaims the terminal part of any patent on the present invention which would extend beyond the expiration date of the full statutory term of U.S. Patent No. 9,331,244. Accordingly, Applicant submits that the non-statutory double patenting rejection of claims 1-20 as being unpatentable over claims 1-21 of U.S. Patent No. 9,331,244 has been obviated. Therefore, Applicant requests that the Examiner reconsider and remove this outstanding double patenting rejection.

Claims 1-20 are also rejected on the ground of non-statutory double patenting as being unpatentable over claims 1-20 of co-pending U.S. Patent Application Serial No. 15/225,403.

Applicant traverses the rejection of claims 1-20 of the present application on the ground of non-statutory double patenting over claims 1-20 of co-pending U.S. Patent

Application Serial No. 15/225,403 in light of MPEP 1490, VI., D., which relates to two (or more) pending applications, in which the claims of each are rejected over the other on the ground of provisional non-statutory double patenting. According to the second paragraph of MPEP 1490, VI., D.:

> [i]f the provisional [non-statutory double patenting (ODP)] rejections in both applications are the only rejections remaining in those applications, the examiner should then withdraw the provisional ODP rejection in the earlier-filed application thereby permitting that application to issue without need of a terminal disclaimer. A terminal disclaimer must be required in the later-filed application before the provisional ODP rejection can be withdrawn and the application be permitted to issue.

Further, according to the third paragraph of MPEP 1490, VI., D.:

> [t]he phrase "earlier-filed" for determining in which application the terminal disclaimer need not be filed, is to be interpreted as follows:
>
> (B)
>
> (2) Where two applications are entitled to the benefit of the same U.S. nonprovisional application under 35 U.S.C. 120, 121 or 365(c), if all the conflicting claims of one of the applications are not appropriately supported in the parent application (and therefore, not entitled to the benefit of the filing date of the parent application), while the conflicting claims of the other application are appropriately supported in the parent application (and therefore, entitled to the benefit of the filing date of the parent application), then the other application is the earlier-filed application. If none of the conflicting claims of either application are appropriately supported in the parent application, then the actual filing dates of the two applications govern.
>
> (C)
>
> A 35 U.S.C. 119(e) benefit is NOT taken into account in determining which is the "earlier-filed" application.

In the present scenario, the only rejections remaining in the present application and U.S. Patent Application Serial No. 15/225,403 are the provisional ODP rejections, in which the claims of each are rejected over the other on the ground of provisional non-

statutory double patenting. Both the present application and U.S. Patent Application Serial No. 15/225,403 stem from a common parent application, U.S. Patent No. 9,331,244. The claims of the present application as currently recited are afforded the benefit of the priority to the parent application. Additionally, the present application was filed prior to U.S. Patent Application Serial No. 15/225,403. As a result, the present application is the earlier-filed application.

Per MPEP 1490, VI., D, a terminal disclaimer is not required for the earlier-filed application, and thus, the present application should issue without the need for one. Accordingly, Applicant requests that the Examiner withdraw the provisional non-statutory double patenting rejection of claims 1-20 of the present application over claims 1-20 of co-pending U.S. Patent Application Serial No. 15/225,403.

Conclusion

In view of the foregoing amendments and remarks, Applicant requests that the Examiner reconsider this application and issue a Notice of Allowance indicating the allowability of claims 1-20.

As noted above, this amendment, which is in compliance with 37 CFR §1.116(b), does not raise any new issues that would require further consideration and/or search. Essentially, Applicant amended claims 1 and 8 with some minor features to address a concern raised by the Examiner.

Applicant submits that entry and consideration of this amendment in light of the prior art of record would take a minimal amount of time to determine whether it places the present patent application in condition for allowance. Accordingly, Applicant

respectfully requests that the Examiner enter and consider this amendment in accordance with AFCP 2.0, and issue a Notice of Allowance indicating the allowability of claims 1-20.

If the Examiner has any questions regarding the present patent application, the Examiner can contact Applicant's attorney at the number listed below.

Respectfully submitted,

/John LaBatt/

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Dated: 4 October 2017

Doc Code: A.NE.AFCP
Document Description: After Final Consideration Pilot Program Request

PTO/SB/434 (05-13)

CERTIFICATION AND REQUEST FOR CONSIDERATION UNDER THE AFTER FINAL CONSIDERATION PILOT PROGRAM 2.0

Practitioner Docket No.:	Application No.:	Filing Date:
SETI-0110-CIP-US	14984156	2015-12-30
First Named Inventor:	**Title:**	
Maxim S. Shatalov	Semiconductor Structure with Inhomogeneous Regions	

APPLICANT HEREBY CERTIFIES THE FOLLOWING AND REQUESTS CONSIDERATION UNDER THE AFTER FINAL CONSIDERATION PILOT PROGRAM 2.0 (AFCP 2.0) OF THE ACCOMPANYING RESPONSE UNDER 37 CFR 1.116.

1. The above-identified application is (i) an original utility, plant, or design nonprovisional application filed under 35 U.S.C. 111(a) [a continuing application (*e.g.*, a continuation or divisional application) is filed under 35 U.S.C. 111(a) and is eligible under (i)], or (ii) an international application that has entered the national stage in compliance with 35 U.S.C. 371(c).
2. The above-identified application contains an outstanding final rejection.
3. Submitted herewith is a response under 37 CFR 1.116 to the outstanding final rejection. The response includes an amendment to at least one independent claim, and the amendment does not broaden the scope of the independent claim in any aspect.
4. This certification and request for consideration under AFCP 2.0 is the only AFCP 2.0 certification and request filed in response to the outstanding final rejection.
5. Applicant is willing and available to participate in any interview requested by the examiner concerning the present response.
6. This certification and request is being filed electronically using the Office's electronic filing system (EFS-Web).
7. Any fees that would be necessary consistent with current practice concerning responses after final rejection under 37 CFR 1.116, *e.g.*, extension of time fees, are being concurrently filed herewith. [There is no additional fee required to request consideration under AFCP 2.0.]
8. By filing this certification and request, applicant acknowledges the following:
    - Reissue applications and reexamination proceedings are not eligible to participate in AFCP 2.0.
    - The examiner will verify that the AFCP 2.0 submission is compliant, *i.e.*, that the requirements of the program have been met (see items 1 to 7 above). For compliant submissions:
        - The examiner will review the response under 37 CFR 1.116 to determine if additional search and/or consideration (i) is necessitated by the amendment and (ii) could be completed within the time allotted under AFCP 2.0. If additional search and/or consideration is required but cannot be completed within the allotted time, the examiner will process the submission consistent with current practice concerning responses after final rejection under 37 CFR 1.116, *e.g.*, by mailing an advisory action.
        - If the examiner determines that the amendment does not necessitate additional search and/or consideration, or if the examiner determines that additional search and/or consideration is required and could be completed within the allotted time, then the examiner will consider whether the amendment places the application in condition for allowance (after completing the additional search and/or consideration, if required). If the examiner determines that the amendment does not place the application in condition for allowance, then the examiner will contact the applicant and request an interview.
            - The interview will be conducted by the examiner, and if the examiner does not have negotiation authority, a primary examiner and/or supervisory patent examiner will also participate.
            - If the applicant declines the interview, or if the interview cannot be scheduled within ten (10) calendar days from the date that the examiner first contacts the applicant, then the examiner will proceed consistent with current practice concerning responses after final rejection under 37 CFR 1.116.

Signature	Date
/John W. LaBatt/	2017-10-04
Name (Print/Typed)	**Practitioner Registration No.**
John W. LaBatt	48301

***Note**: This form must be signed in accordance with 37 CFR 1.33. See 37 CFR 1.4(d) for signature requirements and certifications. Submit multiple forms if more than one signature is required, see below*.*

[✓] * Total of 1 forms are submitted.

Privacy Act Statement

The **Privacy Act of 1974 (P.L. 93-579)** requires that you be given certain information in connection with your submission of the attached form related to a patent application or patent. Accordingly, pursuant to the requirements of the Act, please be advised that: (1) the general authority for the collection of this information is 35 U.S.C. 2(b)(2); (2) furnishing of the information solicited is voluntary; and (3) the principal purpose for which the information is used by the U.S. Patent and Trademark Office is to process and/or examine your submission related to a patent application or patent. If you do not furnish the requested information, the U.S. Patent and Trademark Office may not be able to process and/or examine your submission, which may result in termination of proceedings or abandonment of the application or expiration of the patent.

The information provided by you in this form will be subject to the following routine uses:

1. The information on this form will be treated confidentially to the extent allowed under the Freedom of Information Act (5 U.S.C. 552) and the Privacy Act (5 U.S.C 552a). Records from this system of records may be disclosed to the Department of Justice to determine whether disclosure of these records is required by the Freedom of Information Act.
2. A record from this system of records may be disclosed, as a routine use, in the course of presenting evidence to a court, magistrate, or administrative tribunal, including disclosures to opposing counsel in the course of settlement negotiations.
3. A record in this system of records may be disclosed, as a routine use, to a Member of Congress submitting a request involving an individual, to whom the record pertains, when the individual has requested assistance from the Member with respect to the subject matter of the record.
4. A record in this system of records may be disclosed, as a routine use, to a contractor of the Agency having need for the information in order to perform a contract. Recipients of information shall be required to comply with the requirements of the Privacy Act of 1974, as amended, pursuant to 5 U.S.C. 552a(m).
5. A record related to an International Application filed under the Patent Cooperation Treaty in this system of records may be disclosed, as a routine use, to the International Bureau of the World Intellectual Property Organization, pursuant to the Patent Cooperation Treaty.
6. A record in this system of records may be disclosed, as a routine use, to another federal agency for purposes of National Security review (35 U.S.C. 181) and for review pursuant to the Atomic Energy Act (42 U.S.C. 218(c)).
7. A record from this system of records may be disclosed, as a routine use, to the Administrator, General Services, or his/her designee, during an inspection of records conducted by GSA as part of that agency's responsibility to recommend improvements in records management practices and programs, under authority of 44 U.S.C. 2904 and 2906. Such disclosure shall be made in accordance with the GSA regulations governing inspection of records for this purpose, and any other relevant (*i.e.*, GSA or Commerce) directive. Such disclosure shall not be used to make determinations about individuals.
8. A record from this system of records may be disclosed, as a routine use, to the public after either publication of the application pursuant to 35 U.S.C. 122(b) or issuance of a patent pursuant to 35 U.S.C. 151. Further, a record may be disclosed, subject to the limitations of 37 CFR 1.14, as a routine use, to the public if the record was filed in an application which became abandoned or in which the proceedings were terminated and which application is referenced by either a published application, an application open to public inspection or an issued patent.
9. A record from this system of records may be disclosed, as a routine use, to a Federal, State, or local law enforcement agency, if the USPTO becomes aware of a violation or potential violation of law or regulation.

PTO/SB/08a (03-15)
Approved for use through 07/31/2016. OMB 0651-0031
U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE

INFORMATION DISCLOSURE STATEMENT BY APPLICANT

(Not for submission under 37 CFR 1.99)

Application Number	14984156
Filing Date	2015-12-30
First Named Inventor	Shatalov et al.
Art Unit	2811
Examiner Name	
Attorney Docket Number	SETI-0110-CIP-US

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INFORMATION DISCLOSURE STATEMENT BY APPLICANT (Not for submission under 37 CFR 1.99)		
	Application Number	14984156
	Filing Date	2015-12-30
	First Named Inventor	Shatalov et al.
	Art Unit	2811
	Examiner Name	
	Attorney Docket Number	SETI-0110-CIP-US

	1	TRAN, M., Application No. 15/069,178, Attorney Docket No. SETI-0110-US2, Office Action1, 1 August 2017, 18 pages
	2	ERDEM, F., Application No. 15/225,403, Attorney Docket No. SETI-0110-CIP2-US, Final Office Action1, 27 September 2017, 15 pages

If you wish to add additional non-patent literature document citation information please click the Add button Add

EXAMINER SIGNATURE

Examiner Signature		Date Considered	

*EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through a citation if not in conformance and not considered. Include copy of this form with next communication to applicant.

[1] See Kind Codes of USPTO Patent Documents at www.USPTO.GOV or MPEP 901.04. [2] Enter office that issued the document, by the two-letter code (WIPO Standard ST.3). [3] For Japanese patent documents, the indication of the year of the reign of the Emperor must precede the serial number of the patent document. [4] Kind of document by the appropriate symbols as indicated on the document under WIPO Standard ST.16 if possible. [5] Applicant is to place a check mark here if English language translation is attached.

INFORMATION DISCLOSURE STATEMENT BY APPLICANT (Not for submission under 37 CFR 1.99)		
	Application Number	14984156
	Filing Date	2015-12-30
	First Named Inventor	Shatalov et al.
	Art Unit	2811
	Examiner Name	
	Attorney Docket Number	SETI-0110-CIP-US

CERTIFICATION STATEMENT

Please see 37 CFR 1.97 and 1.98 to make the appropriate selection(s):

That each item of information contained in the information disclosure statement was first cited in any communication from a foreign patent office in a counterpart foreign application not more than three months prior to the filing of the information disclosure statement. See 37 CFR 1.97(e)(1).

OR

☒ That no item of information contained in the information disclosure statement was cited in a communication from a foreign patent office in a counterpart foreign application, and, to the knowledge of the person signing the certification after making reasonable inquiry, no item of information contained in the information disclosure statement was known to any individual designated in 37 CFR 1.56(c) more than three months prior to the filing of the information disclosure statement. See 37 CFR 1.97(e)(2).

See attached certification statement.

☒ The fee set forth in 37 CFR 1.17 (p) has been submitted herewith.

A certification statement is not submitted herewith.

SIGNATURE

A signature of the applicant or representative is required in accordance with CFR 1.33, 10.18. Please see CFR 1.4(d) for the form of the signature.

Signature	/John W. LaBatt/	Date (YYYY-MM-DD)	2017-10-04
Name/Print	John W. LaBatt	Registration Number	48301

This collection of information is required by 37 CFR 1.97 and 1.98. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 1 hour to complete, including gathering, preparing and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

Privacy Act Statement

The Privacy Act of 1974 (P.L. 93-579) requires that you be given certain information in connection with your submission of the attached form related to a patent application or patent. Accordingly, pursuant to the requirements of the Act, please be advised that: (1) the general authority for the collection of this information is 35 U.S.C. 2(b)(2); (2) furnishing of the information solicited is voluntary; and (3) the principal purpose for which the information is used by the U.S. Patent and Trademark Office is to process and/or examine your submission related to a patent application or patent. If you do not furnish the requested information, the U.S. Patent and Trademark Office may not be able to process and/or examine your submission, which may result in termination of proceedings or abandonment of the application or expiration of the patent.

The information provided by you in this form will be subject to the following routine uses:

1. The information on this form will be treated confidentially to the extent allowed under the Freedom of Information Act (5 U.S.C. 552) and the Privacy Act (5 U.S.C. 552a). Records from this system of records may be disclosed to the Department of Justice to determine whether the Freedom of Information Act requires disclosure of these record s.

2. A record from this system of records may be disclosed, as a routine use, in the course of presenting evidence to a court, magistrate, or administrative tribunal, including disclosures to opposing counsel in the course of settlement negotiations.

3. A record in this system of records may be disclosed, as a routine use, to a Member of Congress submitting a request involving an individual, to whom the record pertains, when the individual has requested assistance from the Member with respect to the subject matter of the record.

4. A record in this system of records may be disclosed, as a routine use, to a contractor of the Agency having need for the information in order to perform a contract. Recipients of information shall be required to comply with the requirements of the Privacy Act of 1974, as amended, pursuant to 5 U.S.C. 552a(m).

5. A record related to an International Application filed under the Patent Cooperation Treaty in this system of records may be disclosed, as a routine use, to the International Bureau of the World Intellectual Property Organization, pursuant to the Patent Cooperation Treaty.

6. A record in this system of records may be disclosed, as a routine use, to another federal agency for purposes of National Security review (35 U.S.C. 181) and for review pursuant to the Atomic Energy Act (42 U.S.C. 218(c)).

7. A record from this system of records may be disclosed, as a routine use, to the Administrator, General Services, or his/her designee, during an inspection of records conducted by GSA as part of that agency's responsibility to recommend improvements in records management practices and programs, under authority of 44 U.S.C. 2904 and 2906. Such disclosure shall be made in accordance with the GSA regulations governing inspection of records for this purpose, and any other relevant (i.e., GSA or Commerce) directive. Such disclosure shall not be used to make determinations about individuals.

8. A record from this system of records may be disclosed, as a routine use, to the public after either publication of the application pursuant to 35 U.S.C. 122(b) or issuance of a patent pursuant to 35 U.S.C. 151. Further, a record may be disclosed, subject to the limitations of 37 CFR 1.14, as a routine use, to the public if the record was filed in an application which became abandoned or in which the proceedings were terminated and which application is referenced by either a published application, an application open to public inspections or an issued patent.

9. A record from this system of records may be disclosed, as a routine use, to a Federal, State, or local law enforcement agency, if the USPTO becomes aware of a violation or potential violation of law or regulation.

Electronic Patent Application Fee Transmittal

Application Number:	14984156
Filing Date:	30-Dec-2015
Title of Invention:	Semiconductor Structure with Inhomogeneous Regions
First Named Inventor/Applicant Name:	Maxim S. Shatalov
Filer:	John W LaBatt
Attorney Docket Number:	SETI-0110-CIP-US

Filed as Large Entity

Filing Fees for Utility under 35 USC 111(a)

Description	Fee Code	Quantity	Amount	Sub-Total in USD($)
Basic Filing:				
Pages:				
Claims:				
Miscellaneous-Filing:				
Petition:				
Patent-Appeals-and-Interference:				
Post-Allowance-and-Post-Issuance:				
Extension-of-Time:				

Description	Fee Code	Quantity	Amount	Sub-Total in USD($)
Miscellaneous:				
Submission- Information Disclosure Stmt	1806	1	180	180
		Total in USD ($)		**180**

Electronic Acknowledgement Receipt

EFS ID:	30559817
Application Number:	14984156
International Application Number:	
Confirmation Number:	5890
Title of Invention:	Semiconductor Structure with Inhomogeneous Regions
First Named Inventor/Applicant Name:	Maxim S. Shatalov
Customer Number:	11698
Filer:	John W LaBatt
Filer Authorized By:	
Attorney Docket Number:	SETI-0110-CIP-US
Receipt Date:	04-OCT-2017
Filing Date:	30-DEC-2015
Time Stamp:	11:29:46
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	yes
Payment Type	CARD
Payment was successfully received in RAM	$180
RAM confirmation Number	100417INTEFSW11300800
Deposit Account	
Authorized User	

The Director of the USPTO is hereby authorized to charge indicated fees and credit any overpayment as follows:

File Listing:

Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1		SETI-0110-CIP-US_AFAmendment1.pdf	125394 de9c8def41d18e339c51b8b69aa778a29646e3d1	yes	18
	Multipart Description/PDF files in .zip description				
	Document Description		**Start**	**End**	
	Response After Final Action		1	1	
	Claims		2	7	
	Applicant Arguments/Remarks Made in an Amendment		8	18	
Warnings:					
Information:					
2	After Final Consideration Program Request	SETI-0110-CIP-US_AFCPRequest.pdf	226699 2c69cff8f7993b22e108ebf269b5f488bec9c509	no	2
Warnings:					
Information:					
3	Information Disclosure Statement (IDS) Form (SB08)	SETI-0110-CIP-US_IDS4.pdf	1035046 a1fe22336a9b94e1e36b21ffa3b16fa95f513603	no	4
Warnings:					
Information:					
A U.S. Patent Number Citation or a U.S. Publication Number Citation is required in the Information Disclosure Statement (IDS) form for autoloading of data into USPTO systems. You may remove the form to add the required data in order to correct the Informational Message if you are citing U.S. References. If you chose not to include U.S. References, the image of the form will be processed and be made available within the Image File Wrapper (IFW) system. However, no data will be extracted from this form. Any additional data such as Foreign Patent Documents or Non Patent Literature will be manually reviewed and keyed into USPTO systems.					
4	Non Patent Literature	SETI-0110-US2_OfficeAction1_08-01-17.pdf	790610 0630f7e0b29223f0b720bf6b59b3e3b5719fd31b	no	18
Warnings:					
Information:					

5	Non Patent Literature	SETI-0110-CIP2-US_FinalOfficeAction1_09-27-17.pdf	772484 947943a4fb95b8acd6c4f99583cb7ac212368187	no	15
Warnings:					
Information:					
6	Fee Worksheet (SB06)	fee-info.pdf	30616 8fe666088681fd423a87b59f30c87581ec699398	no	2
Warnings:					
Information:					
			Total Files Size (in bytes):	2980849	

This Acknowledgement Receipt evidences receipt on the noted date by the USPTO of the indicated documents, characterized by the applicant, and including page counts, where applicable. It serves as evidence of receipt similar to a Post Card, as described in MPEP 503.

New Applications Under 35 U.S.C. 111

If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application.

National Stage of an International Application under 35 U.S.C. 371

If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.

New International Application Filed with the USPTO as a Receiving Office

If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.

PTO/SB/06 (09-11)
Approved for use through 1/31/2014. OMB 0651-0032
U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE
Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it displays a valid OMB control number.

PATENT APPLICATION FEE DETERMINATION RECORD Substitute for Form PTO-875	Application or Docket Number 14/984,156	Filing Date 12/30/2015	☐ To be Mailed

ENTITY: ☒ LARGE ☐ SMALL ☐ MICRO

APPLICATION AS FILED – PART I

FOR	(Column 1) NUMBER FILED	(Column 2) NUMBER EXTRA	RATE ($)	FEE ($)
☐ BASIC FEE (37 CFR 1.16(a), (b), or (c))	N/A	N/A	N/A	
☐ SEARCH FEE (37 CFR 1.16(k), (i), or (m))	N/A	N/A	N/A	
☐ EXAMINATION FEE (37 CFR 1.16(o), (p), or (q))	N/A	N/A	N/A	
TOTAL CLAIMS (37 CFR 1.16(i))	minus 20 =	*	X $ =	
INDEPENDENT CLAIMS (37 CFR 1.16(h))	minus 3 =	*	X $ =	
☐ APPLICATION SIZE FEE (37 CFR 1.16(s))	If the specification and drawings exceed 100 sheets of paper, the application size fee due is $310 ($155 for small entity) for each additional 50 sheets or fraction thereof. See 35 U.S.C. 41(a)(1)(G) and 37 CFR 1.16(s).			
☐ MULTIPLE DEPENDENT CLAIM PRESENT (37 CFR 1.16(j))				
* If the difference in column 1 is less than zero, enter "0" in column 2.			TOTAL	

APPLICATION AS AMENDED – PART II

AMENDMENT	10/04/2017	(Column 1) CLAIMS REMAINING AFTER AMENDMENT		(Column 2) HIGHEST NUMBER PREVIOUSLY PAID FOR	(Column 3) PRESENT EXTRA	RATE ($)	ADDITIONAL FEE ($)
	Total (37 CFR 1.16(i))	* 20	Minus	** 20	= 0	X $80 =	0
	Independent (37 CFR 1.16(h))	* 3	Minus	***3	= 0	X $420 =	0
	☐ Application Size Fee (37 CFR 1.16(s))						
	☐ FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))						
						TOTAL ADD'L FEE	0

AMENDMENT		(Column 1) CLAIMS REMAINING AFTER AMENDMENT		(Column 2) HIGHEST NUMBER PREVIOUSLY PAID FOR	(Column 3) PRESENT EXTRA	RATE ($)	ADDITIONAL FEE ($)
	Total (37 CFR 1.16(i))	*	Minus	**	=	X $ =	
	Independent (37 CFR 1.16(h))	*	Minus	***	=	X $ =	
	☐ Application Size Fee (37 CFR 1.16(s))						
	☐ FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))						
						TOTAL ADD'L FEE	

* If the entry in column 1 is less than the entry in column 2, write "0" in column 3.
** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 20, enter "20".
*** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 3, enter "3".
The "Highest Number Previously Paid For" (Total or Independent) is the highest number found in the appropriate box in column 1.

LIE
LAJUAN HICKSON

UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

NOTICE OF ALLOWANCE AND FEE(S) DUE

11698 7590 10/27/2017

LaBatt, LLC (SET)
PO Box 630
Valatie, NY 12184

EXAMINER	
ERDEM, FAZLI	
ART UNIT	PAPER NUMBER
2826	

DATE MAILED: 10/27/2017

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
14/984,156	12/30/2015	Maxim S. Shatalov	SETI-0110-CIP-US	5890

TITLE OF INVENTION: Semiconductor Structure with Inhomogeneous Regions

APPLN. TYPE	ENTITY STATUS	ISSUE FEE DUE	PUBLICATION FEE DUE	PREV. PAID ISSUE FEE	TOTAL FEE(S) DUE	DATE DUE
nonprovisional	UNDISCOUNTED	$960	$0	$0	$960	01/29/2018

THE APPLICATION IDENTIFIED ABOVE HAS BEEN EXAMINED AND IS ALLOWED FOR ISSUANCE AS A PATENT. PROSECUTION ON THE MERITS IS CLOSED. THIS NOTICE OF ALLOWANCE IS NOT A GRANT OF PATENT RIGHTS. THIS APPLICATION IS SUBJECT TO WITHDRAWAL FROM ISSUE AT THE INITIATIVE OF THE OFFICE OR UPON PETITION BY THE APPLICANT. SEE 37 CFR 1.313 AND MPEP 1308.

THE ISSUE FEE AND PUBLICATION FEE (IF REQUIRED) MUST BE PAID WITHIN THREE MONTHS FROM THE MAILING DATE OF THIS NOTICE OR THIS APPLICATION SHALL BE REGARDED AS ABANDONED. THIS STATUTORY PERIOD CANNOT BE EXTENDED. SEE 35 U.S.C. 151. THE ISSUE FEE DUE INDICATED ABOVE DOES NOT REFLECT A CREDIT FOR ANY PREVIOUSLY PAID ISSUE FEE IN THIS APPLICATION. IF AN ISSUE FEE HAS PREVIOUSLY BEEN PAID IN THIS APPLICATION (AS SHOWN ABOVE), THE RETURN OF PART B OF THIS FORM WILL BE CONSIDERED A REQUEST TO REAPPLY THE PREVIOUSLY PAID ISSUE FEE TOWARD THE ISSUE FEE NOW DUE.

HOW TO REPLY TO THIS NOTICE:

I. Review the ENTITY STATUS shown above. If the ENTITY STATUS is shown as SMALL or MICRO, verify whether entitlement to that entity status still applies.

If the ENTITY STATUS is the same as shown above, pay the TOTAL FEE(S) DUE shown above.

If the ENTITY STATUS is changed from that shown above, on PART B - FEE(S) TRANSMITTAL, complete section number 5 titled "Change in Entity Status (from status indicated above)".

For purposes of this notice, small entity fees are 1/2 the amount of undiscounted fees, and micro entity fees are 1/2 the amount of small entity fees.

II. PART B - FEE(S) TRANSMITTAL, or its equivalent, must be completed and returned to the United States Patent and Trademark Office (USPTO) with your ISSUE FEE and PUBLICATION FEE (if required). If you are charging the fee(s) to your deposit account, section "4b" of Part B - Fee(s) Transmittal should be completed and an extra copy of the form should be submitted. If an equivalent of Part B is filed, a request to reapply a previously paid issue fee must be clearly made, and delays in processing may occur due to the difficulty in recognizing the paper as an equivalent of Part B.

III. All communications regarding this application must give the application number. Please direct all communications prior to issuance to Mail Stop ISSUE FEE unless advised to the contrary.

IMPORTANT REMINDER: Maintenance fees are due in utility patents issuing on applications filed on or after Dec. 12, 1980. It is patentee's responsibility to ensure timely payment of maintenance fees when due. More information is available at www.uspto.gov/PatentMaintenanceFees.

PART B - FEE(S) TRANSMITTAL

Complete and send this form, together with applicable fee(s), to: Mail **Mail Stop ISSUE FEE**
Commissioner for Patents
P.O. Box 1450
Alexandria, Virginia 22313-1450
or Fax (571)-273-2885

INSTRUCTIONS: This form should be used for transmitting the ISSUE FEE and PUBLICATION FEE (if required). Blocks 1 through 5 should be completed where appropriate. All further correspondence including the Patent, advance orders and notification of maintenance fees will be mailed to the current correspondence address as indicated unless corrected below or directed otherwise in Block 1, by (a) specifying a new correspondence address; and/or (b) indicating a separate "FEE ADDRESS" for maintenance fee notifications.

CURRENT CORRESPONDENCE ADDRESS (Note: Use Block 1 for any change of address)

11698 7590 10/27/2017
LaBatt, LLC (SET)
PO Box 630
Valatie, NY 12184

Note: A certificate of mailing can only be used for domestic mailings of the Fee(s) Transmittal. This certificate cannot be used for any other accompanying papers. Each additional paper, such as an assignment or formal drawing, must have its own certificate of mailing or transmission.

Certificate of Mailing or Transmission
I hereby certify that this Fee(s) Transmittal is being deposited with the United States Postal Service with sufficient postage for first class mail in an envelope addressed to the Mail Stop ISSUE FEE address above, or being facsimile transmitted to the USPTO (571) 273-2885, on the date indicated below.

(Depositor's name)
(Signature)
(Date)

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
14/984,156	12/30/2015	Maxim S. Shatalov	SETI-0110-CIP-US	5890

TITLE OF INVENTION: Semiconductor Structure with Inhomogeneous Regions

APPLN. TYPE	ENTITY STATUS	ISSUE FEE DUE	PUBLICATION FEE DUE	PREV. PAID ISSUE FEE	TOTAL FEE(S) DUE	DATE DUE
nonprovisional	UNDISCOUNTED	$960	$0	$0	$960	01/29/2018

EXAMINER	ART UNIT	CLASS-SUBCLASS
ERDEM, FAZLI	2826	257-094000

1. Change of correspondence address or indication of "Fee Address" (37 CFR 1.363).
❑ Change of correspondence address (or Change of Correspondence Address form PTO/SB/122) attached.
❑ "Fee Address" indication (or "Fee Address" Indication form PTO/SB/47; Rev 03-02 or more recent) attached. **Use of a Customer Number is required.**

2. For printing on the patent front page, list
(1) The names of up to 3 registered patent attorneys or agents OR, alternatively,
(2) The name of a single firm (having as a member a registered attorney or agent) and the names of up to 2 registered patent attorneys or agents. If no name is listed, no name will be printed.
1 _____
2 _____
3 _____

3. ASSIGNEE NAME AND RESIDENCE DATA TO BE PRINTED ON THE PATENT (print or type)

PLEASE NOTE: Unless an assignee is identified below, no assignee data will appear on the patent. If an assignee is identified below, the document has been filed for recordation as set forth in 37 CFR 3.11. Completion of this form is NOT a substitute for filing an assignment.

(A) NAME OF ASSIGNEE (B) RESIDENCE: (CITY and STATE OR COUNTRY)

Please check the appropriate assignee category or categories (will not be printed on the patent) : ❑ Individual ❑ Corporation or other private group entity ❑ Government

4a. The following fee(s) are submitted:
❑ Issue Fee
❑ Publication Fee (No small entity discount permitted)
❑ Advance Order - # of Copies _____

4b. Payment of Fee(s): **(Please first reapply any previously paid issue fee shown above)**
❑ A check is enclosed.
❑ Payment by credit card. Form PTO-2038 is attached.
❑ The director is hereby authorized to charge the required fee(s), any deficiency, or credits any overpayment, to Deposit Account Number _____ (enclose an extra copy of this form).

5. **Change in Entity Status** (from status indicated above)
❑ Applicant certifying micro entity status. See 37 CFR 1.29
NOTE: Absent a valid certification of Micro Entity Status (see forms PTO/SB/15A and 15B), issue fee payment in the micro entity amount will not be accepted at the risk of application abandonment.
❑ Applicant asserting small entity status. See 37 CFR 1.27
NOTE: If the application was previously under micro entity status, checking this box will be taken to be a notification of loss of entitlement to micro entity status.
❑ Applicant changing to regular undiscounted fee status.
NOTE: Checking this box will be taken to be a notification of loss of entitlement to small or micro entity status, as applicable.

NOTE: This form must be signed in accordance with 37 CFR 1.31 and 1.33. See 37 CFR 1.4 for signature requirements and certifications.

Authorized Signature _____ Date _____

Typed or printed name _____ Registration No. _____

UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
14/984,156	12/30/2015	Maxim S. Shatalov	SETI-0110-CIP-US	5890

11698 7590 10/27/2017

LaBatt, LLC (SET)
PO Box 630
Valatie, NY 12184

EXAMINER	
ERDEM, FAZLI	

ART UNIT	PAPER NUMBER
2826	

DATE MAILED: 10/27/2017

Determination of Patent Term Adjustment under 35 U.S.C. 154 (b)
(Applications filed on or after May 29, 2000)

The Office has discontinued providing a Patent Term Adjustment (PTA) calculation with the Notice of Allowance.

Section 1(h)(2) of the AIA Technical Corrections Act amended 35 U.S.C. 154(b)(3)(B)(i) to eliminate the requirement that the Office provide a patent term adjustment determination with the notice of allowance. See Revisions to Patent Term Adjustment, 78 Fed. Reg. 19416, 19417 (Apr. 1, 2013). Therefore, the Office is no longer providing an initial patent term adjustment determination with the notice of allowance. The Office will continue to provide a patent term adjustment determination with the Issue Notification Letter that is mailed to applicant approximately three weeks prior to the issue date of the patent, and will include the patent term adjustment on the patent. Any request for reconsideration of the patent term adjustment determination (or reinstatement of patent term adjustment) should follow the process outlined in 37 CFR 1.705.

Any questions regarding the Patent Term Extension or Adjustment determination should be directed to the Office of Patent Legal Administration at (571)-272-7702. Questions relating to issue and publication fee payments should be directed to the Customer Service Center of the Office of Patent Publication at 1-(888)-786-0101 or (571)-272-4200.

OMB Clearance and PRA Burden Statement for PTOL-85 Part B

The Paperwork Reduction Act (PRA) of 1995 requires Federal agencies to obtain Office of Management and Budget approval before requesting most types of information from the public. When OMB approves an agency request to collect information from the public, OMB (i) provides a valid OMB Control Number and expiration date for the agency to display on the instrument that will be used to collect the information and (ii) requires the agency to inform the public about the OMB Control Number's legal significance in accordance with 5 CFR 1320.5(b).

The information collected by PTOL-85 Part B is required by 37 CFR 1.311. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 12 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, Virginia 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, Virginia 22313-1450. Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it displays a valid OMB control number.

Privacy Act Statement

The Privacy Act of 1974 (P.L. 93-579) requires that you be given certain information in connection with your submission of the attached form related to a patent application or patent. Accordingly, pursuant to the requirements of the Act, please be advised that: (1) the general authority for the collection of this information is 35 U.S.C. 2(b)(2); (2) furnishing of the information solicited is voluntary; and (3) the principal purpose for which the information is used by the U.S. Patent and Trademark Office is to process and/or examine your submission related to a patent application or patent. If you do not furnish the requested information, the U.S. Patent and Trademark Office may not be able to process and/or examine your submission, which may result in termination of proceedings or abandonment of the application or expiration of the patent.

The information provided by you in this form will be subject to the following routine uses:

1. The information on this form will be treated confidentially to the extent allowed under the Freedom of Information Act (5 U.S.C. 552) and the Privacy Act (5 U.S.C 552a). Records from this system of records may be disclosed to the Department of Justice to determine whether disclosure of these records is required by the Freedom of Information Act.
2. A record from this system of records may be disclosed, as a routine use, in the course of presenting evidence to a court, magistrate, or administrative tribunal, including disclosures to opposing counsel in the course of settlement negotiations.
3. A record in this system of records may be disclosed, as a routine use, to a Member of Congress submitting a request involving an individual, to whom the record pertains, when the individual has requested assistance from the Member with respect to the subject matter of the record.
4. A record in this system of records may be disclosed, as a routine use, to a contractor of the Agency having need for the information in order to perform a contract. Recipients of information shall be required to comply with the requirements of the Privacy Act of 1974, as amended, pursuant to 5 U.S.C. 552a(m).
5. A record related to an International Application filed under the Patent Cooperation Treaty in this system of records may be disclosed, as a routine use, to the International Bureau of the World Intellectual Property Organization, pursuant to the Patent Cooperation Treaty.
6. A record in this system of records may be disclosed, as a routine use, to another federal agency for purposes of National Security review (35 U.S.C. 181) and for review pursuant to the Atomic Energy Act (42 U.S.C. 218(c)).
7. A record from this system of records may be disclosed, as a routine use, to the Administrator, General Services, or his/her designee, during an inspection of records conducted by GSA as part of that agency's responsibility to recommend improvements in records management practices and programs, under authority of 44 U.S.C. 2904 and 2906. Such disclosure shall be made in accordance with the GSA regulations governing inspection of records for this purpose, and any other relevant (i.e., GSA or Commerce) directive. Such disclosure shall not be used to make determinations about individuals.
8. A record from this system of records may be disclosed, as a routine use, to the public after either publication of the application pursuant to 35 U.S.C. 122(b) or issuance of a patent pursuant to 35 U.S.C. 151. Further, a record may be disclosed, subject to the limitations of 37 CFR 1.14, as a routine use, to the public if the record was filed in an application which became abandoned or in which the proceedings were terminated and which application is referenced by either a published application, an application open to public inspection or an issued patent.
9. A record from this system of records may be disclosed, as a routine use, to a Federal, State, or local law enforcement agency, if the USPTO becomes aware of a violation or potential violation of law or regulation.

Notice of Allowability	Application No. 14/984,156	Applicant(s) SHATALOV ET AL.	
	Examiner FAZLI ERDEM	Art Unit 2826	AIA (First Inventor to File) Status Yes

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address--

All claims being allowable, PROSECUTION ON THE MERITS IS (OR REMAINS) CLOSED in this application. If not included herewith (or previously mailed), a Notice of Allowance (PTOL-85) or other appropriate communication will be mailed in due course. **THIS NOTICE OF ALLOWABILITY IS NOT A GRANT OF PATENT RIGHTS.** This application is subject to withdrawal from issue at the initiative of the Office or upon petition by the applicant. See 37 CFR 1.313 and MPEP 1308.

1. ☒ This communication is responsive to *After final response filed on 10/4/2017*.
   ☐ A declaration(s)/affidavit(s) under **37 CFR 1.130(b)** was/were filed on_____.
2. ☐ An election was made by the applicant in response to a restriction requirement set forth during the interview on _____; the restriction requirement and election have been incorporated into this action.
3. ☒ The allowed claim(s) is/are *1-20*. As a result of the allowed claim(s), you may be eligible to benefit from the **Patent Prosecution Highway** program at a participating intellectual property office for the corresponding application. For more information, please see http://www.uspto.gov/patents/init_events/pph/index.jsp or send an inquiry to PPHfeedback@uspto.gov.
4. ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

   Certified copies:

   a) ☐ All b) ☐ Some *c) ☐ None of the:
   1. ☐ Certified copies of the priority documents have been received.
   2. ☐ Certified copies of the priority documents have been received in Application No. _____ .
   3. ☐ Copies of the certified copies of the priority documents have been received in this national stage application from the International Bureau (PCT Rule 17.2(a)).

   * Certified copies not received: _____.

Applicant has THREE MONTHS FROM THE "MAILING DATE" of this communication to file a reply complying with the requirements noted below. Failure to timely comply will result in ABANDONMENT of this application.
THIS THREE-MONTH PERIOD IS NOT EXTENDABLE.

5. ☐ CORRECTED DRAWINGS (as "replacement sheets") must be submitted.
   ☐ including changes required by the attached Examiner's Amendment / Comment or in the Office action of Paper No./Mail Date _____.

   Identifying indicia such as the application number (see 37 CFR 1.84(c)) should be written on the drawings in the front (not the back) of each sheet. Replacement sheet(s) should be labeled as such in the header according to 37 CFR 1.121(d).
6. ☐ DEPOSIT OF and/or INFORMATION about the deposit of BIOLOGICAL MATERIAL must be submitted. Note the attached Examiner's comment regarding REQUIREMENT FOR THE DEPOSIT OF BIOLOGICAL MATERIAL.

Attachment(s)

1. ☐ Notice of References Cited (PTO-892)
2. ☒ Information Disclosure Statements (PTO/SB/08), Paper No./Mail Date 10/4/2017
3. ☐ Examiner's Comment Regarding Requirement for Deposit of Biological Material
4. ☐ Interview Summary (PTO-413), Paper No./Mail Date _____ .
5. ☐ Examiner's Amendment/Comment
6. ☒ Examiner's Statement of Reasons for Allowance
7. ☒ Other *PTO 2323*.

/FAZLI ERDEM/
Primary Examiner, Art Unit 2826
10/20/2017

The present application, filed on or after March 16, 2013, is being examined under the first inventor to file provisions of the AIA.

DETAILED ACTION

Terminal Disclaimer

The terminal disclaimer filed on 10/04/2017 has been recorded.

Allowable Subject Matter

Claims 1-20 are allowed.

The following is an examiner's statement of reasons for allowance:

Regarding Claim 1, prior art failed to disclose or fairly suggest a semiconductor heterostructur, comprising, in addition to other claimed features, a group III nitride semiconductor layer including a plurality of inhomogeneous regions arranged within multiple levels of the semiconductor along a height direction of the semiconductor layer (amended on 10/4/2017) wherein some of the inhomogeneous regions in a first level of the semiconductor layer are vertically offset from inhomogeneous regions in a second level of the semiconductor layer, and wherein the plurality of inhomogeneous region include one or more of a set of transparent regions, a set of reflective regions and/or a set of conductive regions, each of the inhomogeneous regions having a set of attributes differing from a group III nitride material forming the semiconductor layer. Claims 2-7 depend from claim 1 and hence are allowed for the same reason therein.

Regarding Claim 8, prior art fail to disclose or fairly suggest a method comprising fabricating a semiconductor hetero structure wherein the semiconductor heterostructure comprises, in addition to other claimed features, a group III nitride semiconductor layer

including a plurality of inhomogeneous regions arranged within multiple levels of the semiconductor along a height direction of the semiconductor layer (amended on 10/4/2017) wherein some of the inhomogeneous regions in a first level of the semiconductor layer are vertically offset from inhomogeneous regions in a second level of the semiconductor layer, and wherein the plurality of inhomogeneous region include one or more of a set of transparent regions, a set of reflective regions and/or a set of conductive regions, each of the inhomogeneous regions having a set of attributes differing from a group III nitride material forming the semiconductor layer. Claims 9 and 10 depend from claim 8 and hence are allowed for the same reason therein.

Regarding Claim 11, prior art failed to disclose or fairly suggest an optoelectronic device comprising a semiconductor hetero structure including, in addition to other claimed features, a plurality of inhomogeneous regions that include a set of first inhomogeneous regions configured based on radiation having a target wavelength, where the set of inhomogeneous regions at least one of transparent to the radiation or reflective of the radiation, and a second set of inhomogeneous region, wherein each of the sets of inhomogeneous regions occupy at least five percent of at least one of a lateral planar area of the semiconductor layer or a volume of the semiconductor layer and where at least some of the sets of inhomogeneous regions do not fully overlap. Claims 12-20 depend from claim 11 and hence are allowed for the same reason therein.

Any comments considered necessary by applicant must be submitted no later than the payment of the issue fee and, to avoid processing delays, should preferably

accompany the issue fee. Such submissions should be clearly labeled "Comments on Statement of Reasons for Allowance."

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to FAZLI ERDEM whose telephone number is (571)272-1914. The examiner can normally be reached on M-F 8:00 - 5:00.

Examiner interviews are available via telephone, in-person, and video conferencing using a USPTO supplied web-based collaboration tool. To schedule an interview, applicant is encouraged to use the USPTO Automated Interview Request (AIR) at http://www.uspto.gov/interviewpractice.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Davienne Monbleau can be reached on 571-272-1945. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/FAZLI ERDEM/
Primary Examiner, Art Unit 2826
10/20/2017

EAST Search History

EAST Search History (Interference)

Ref #	Hits	Search Query	DBs	Default Operator	Plurals	Time Stamp
L42	115982	shatalov.in. or dobrinsky.in. or lunev.in. or jain.in. or yang.in. or shur.in. or gaska.in.	US-PGPUB; USPAT	OR	ON	2017/10/20 12:56
L43	385	sensor near electronic.as. or sensor near electronic.aanm.	US-PGPUB; USPAT	OR	ON	2017/10/20 12:57
L44	12555	257/94.ccls. or H01L33/10.cpc. or H01L33/007.cpc. or H01L33/32.cpc.	US-PGPUB; USPAT	OR	ON	2017/10/20 12:57
L45	128030	l42 or l43 or l44	US-PGPUB; USPAT	OR	ON	2017/10/20 12:58
L46	2234	l45 and bragg	US-PGPUB; USPAT	OR	ON	2017/10/20 12:58
L47	22	l46 and inhomogeneous near2 region	US-PGPUB; USPAT	OR	ON	2017/10/20 12:58
L48	20	l47 and reflective	US-PGPUB; USPAT	OR	ON	2017/10/20 12:58
L49	0	l48 and targe near2 (radiation or wavelength)	US-PGPUB; USPAT	OR	ON	2017/10/20 12:58
L50	18	l48 and target near2 (radiation or wavelength)	US-PGPUB; USPAT	OR	ON	2017/10/20 12:58
L51	5	l50 and level near10 offset	US-PGPUB; USPAT	OR	ON	2017/10/20 12:58
L52	3	l50 and offset.clm.	US-PGPUB; USPAT	OR	ON	2017/10/20 12:59
L53	0	l50 and target with second near2 set.clm.	US-PGPUB; USPAT	OR	ON	2017/10/20 12:59
L54	4	l50 and target same second near2 set.clm.	US-PGPUB; USPAT	OR	ON	2017/10/20 12:59

10/20/2017 1:00:19 PM
C:\Users\ferdem\Documents\EAST\Workspaces\14984156_case.wsp

Issue Classification	Application/Control No.	Applicant(s)/Patent Under Reexamination
	14984156	SHATALOV ET AL.
	Examiner	**Art Unit**
	FAZLI ERDEM	2826

CPC								
Symbol							**Type**	**Version**
H01L		33	/	10			F	2013-01-01
H01L		33	/	007			I	2013-01-01
H01L		33	/	32			I	2013-01-01
H01L		33	/	12			A	2013-01-01
H01L		33	/	46			A	2013-01-01
			/					
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CPC Combination Sets								
Symbol							**Type**	**Set**	**Ranking**	**Version**
			/							
			/							

(Assistant Examiner)	(Date)	**Total Claims Allowed:** 20	
/FAZLI ERDEM/ Primary Examiner.Art Unit 2826	10/20/2017	O.G. Print Claim(s)	O.G. Print Figure
(Primary Examiner)	(Date)	1	13A

Issue Classification	Application/Control No.	Applicant(s)/Patent Under Reexamination
	14984156	SHATALOV ET AL.
	Examiner	**Art Unit**
	FAZLI ERDEM	2826

US ORIGINAL CLASSIFICATION	
CLASS	**SUBCLASS**
257	94

CROSS REFERENCE(S)					
CLASS	**SUBCLASS (ONE SUBCLASS PER BLOCK)**				

INTERNATIONAL CLASSIFICATION														
CLAIMED						**NON-CLAIMED**					
H	0	1	L	33 / 32 (2010.01.01)										
H	0	1	L	33 / 10 (2010.01.01)										

(Assistant Examiner)	(Date)	**Total Claims Allowed:** 20	
/FAZLI ERDEM/ Primary Examiner.Art Unit 2826	10/20/2017	O.G. Print Claim(s)	O.G. Print Figure
(Primary Examiner)	(Date)	1	13A

Issue Classification	Application/Control No.	Applicant(s)/Patent Under Reexamination
	14984156	SHATALOV ET AL.
	Examiner	**Art Unit**
	FAZLI ERDEM	2826

☒ **Claims renumbered in the same order as presented by applicant** ☐ **CPA** ☐ **T.D.** ☐ **R.1.47**

Final	Original	Final	Original	Final	Original	Final	Original	Final	Original	Final	Original	Final	Original	Final	Original

(Assistant Examiner)	(Date)	**Total Claims Allowed:** 20	
/FAZLI ERDEM/ Primary Examiner.Art Unit 2826	10/20/2017	O.G. Print Claim(s)	O.G. Print Figure
(Primary Examiner)	(Date)	1	13A

Search Notes	Application/Control No.	Applicant(s)/Patent Under Reexamination
	14984156	SHATALOV ET AL.
	Examiner	Art Unit
	FAZLI ERDEM	2826

CPC- SEARCHED		
Symbol	Date	Examiner
H01L33/10	2/2/2017	FE
H01L33/007	2/2/2017	FE
H01L33/32	2/2/2017	FE
H01L33/007	10/20/2017	FE
H01L33/10	10/20/2017	FE
H01L33/32	10/20/2017	FE

CPC COMBINATION SETS - SEARCHED		
Symbol	Date	Examiner

US CLASSIFICATION SEARCHED			
Class	Subclass	Date	Examiner

* See search history printout included with this form or the SEARCH NOTES box below to determine the scope of the search.

SEARCH NOTES		
Search Notes	Date	Examiner
H01L33/10	2/2/2017	FE
H01L33/007	2/2/2017	FE
H01L33/32	2/2/2017	FE
Inventors are searched	2/2/2017	FE
Assignee is searched	2/2/2017	FE
CPC search limited with text is conducted	2/2/2017	FE
Searched 257/94 limited with text	2/2/2017	FE
EAST Search history is attached	2/2/2017	FE
Updated EAST Search history is attached	7/31/2017	FE
Inventors are searched	10/20/2017	FE
Assignee is searched	10/20/2017	FE

SEARCH NOTES		
Search Notes	**Date**	**Examiner**
Searched 257/94 limited with text	10/20/2017	FE
Searched H01L33/007, 10, 32 limited with text	10/20/2017	FE
Interference search is conducted	10/20/2017	FE
Updated EAST Search history is attached	10/20/2017	FE

INTERFERENCE SEARCH			
US Class/ CPC Symbol	**US Subclass / CPC Group**	**Date**	**Examiner**
257	94	10/20/2017	FE
H01L33	007, 10, 32	10/20/2017	FE

AFCP 2.0 Decision	Application No.	Applicant(s)
	14/984,156	SHATALOV ET AL.
	Examiner	Art Unit
	FAZLI ERDEM	2826

This is in response to the After Final Consideration Pilot request filed 04 October 2017.

1. **Improper Request** – The AFCP 2.0 request is improper for the following reason(s) and the after final amendment submitted with the request will be treated under pre-pilot procedure.

   ☐ An AFCP 2.0 request form PTO/SB/434 (or equivalent document) was not submitted.

   ☐ A non-broadening amendment to at least one independent claim was not submitted.

   ☐ A proper AFCP 2.0 request was submitted in response to the most recent final rejection.

   ☐ Other:

2. **Proper Request**

   A. After final amendment submitted with the request will not be treated under AFCP 2.0.
   The after final amendment cannot be reviewed and a search conducted within the guidelines of the pilot program.

   ☐ The after final amendment will be treated under pre-pilot procedure.

   B. Updated search and/or completed additional consideration.
   The examiner performed an updated search and/or completed additional consideration of the after final amendment within the time authorized for the pilot program. The result(s) of the updated search and/or completed additional consideration are:

   ☒ 1. All of the rejections in the most recent final Office action are overcome and a Notice of Allowance is issued herewith.

   ☐ 2. The after final amendment would not overcome all of the rejections in the most recent final Office action. See attached interview summary for further details.

   ☐ 3. The after final amendment was reviewed, and it raises a new issue(s). See attached interview summary for further details.

   ☐ 4. The after final amendment raises new issues, but would overcome all of the rejections in the most recent final Office action. A decision on determining allowability could not be made within the guidelines of the pilot. See attached interview summary for further details, including any newly discovered prior art.

   ☐ 5. Other:

   Examiner Note: Please attach an interview summary when necessary as described above.

Doc code: IDS
Doc description: Information Disclosure Statement (IDS) Filed

PTO/SB/08a (03-15)
Approved for use through 07/31/2016. OMB 0651-0031
U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE

INFORMATION DISCLOSURE STATEMENT BY APPLICANT

(Not for submission under 37 CFR 1.99)

Application Number	14984156
Filing Date	2015-12-30
First Named Inventor	Shatalov et al.
Art Unit	2811
Examiner Name	
Attorney Docket Number	SETI-0110-CIP-US

U.S.PATENTS Remove

Examiner Initial*	Cite No	Patent Number	Kind Code[1]	Issue Date	Name of Patentee or Applicant of cited Document	Pages,Columns,Lines where Relevant Passages or Relevant Figures Appear
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Examiner Initial*	Cite No	Publication Number	Kind Code[1]	Publication Date	Name of Patentee or Applicant of cited Document	Pages,Columns,Lines where Relevant Passages or Relevant Figures Appear
	1					

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Examiner Initial*	Cite No	Foreign Document Number[3]	Country Code[2] i	Kind Code[4]	Publication Date	Name of Patentee or Applicant of cited Document	Pages,Columns,Lines where Relevant Passages or Relevant Figures Appear	T[5]
	1							

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NON-PATENT LITERATURE DOCUMENTS Remove

Examiner Initials*	Cite No	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc), date, pages(s), volume-issue number(s), publisher, city and/or country where published.	T[5]

INFORMATION DISCLOSURE STATEMENT BY APPLICANT

(Not for submission under 37 CFR 1.99)

Application Number	14984156
Filing Date	2015-12-30
First Named Inventor	Shatalov et al.
Art Unit	2811
Examiner Name	
Attorney Docket Number	SETI-0110-CIP-US

/F.E/	1	TRAN, M., Application No. 15/069,178, Attorney Docket No. SETI-0110-US2, Office Action1, 1 August 2017, 18 pages	
/F.E/	2	ERDEM, F., Application No. 15/225,403, Attorney Docket No. SETI-0110-CIP2-US, Final Office Action1, 27 September 2017, 15 pages	

If you wish to add additional non-patent literature document citation information please click the Add button Add

EXAMINER SIGNATURE

Examiner Signature	/FAZLI ERDEM/	Date Considered	10/20/2017

*EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through a citation if not in conformance and not considered. Include copy of this form with next communication to applicant.

[1] See Kind Codes of USPTO Patent Documents at www.USPTO.GOV or MPEP 901.04. [2] Enter office that issued the document, by the two-letter code (WIPO Standard ST.3). [3] For Japanese patent documents, the indication of the year of the reign of the Emperor must precede the serial number of the patent document. [4] Kind of document by the appropriate symbols as indicated on the document under WIPO Standard ST.16 if possible. [5] Applicant is to place a check mark here if English language translation is attached.

INFORMATION DISCLOSURE STATEMENT BY APPLICANT

(Not for submission under 37 CFR 1.99)

Application Number	14984156
Filing Date	2015-12-30
First Named Inventor	Shatalov et al.
Art Unit	2811
Examiner Name	
Attorney Docket Number	SETI-0110-CIP-US

CERTIFICATION STATEMENT

Please see 37 CFR 1.97 and 1.98 to make the appropriate selection(s):

That each item of information contained in the information disclosure statement was first cited in any communication from a foreign patent office in a counterpart foreign application not more than three months prior to the filing of the information disclosure statement. See 37 CFR 1.97(e)(1).

OR

☒ That no item of information contained in the information disclosure statement was cited in a communication from a foreign patent office in a counterpart foreign application, and, to the knowledge of the person signing the certification after making reasonable inquiry, no item of information contained in the information disclosure statement was known to any individual designated in 37 CFR 1.56(c) more than three months prior to the filing of the information disclosure statement. See 37 CFR 1.97(e)(2).

See attached certification statement.

☒ The fee set forth in 37 CFR 1.17 (p) has been submitted herewith.

A certification statement is not submitted herewith.

SIGNATURE

A signature of the applicant or representative is required in accordance with CFR 1.33, 10.18. Please see CFR 1.4(d) for the form of the signature.

Signature	/John W. LaBatt/	Date (YYYY-MM-DD)	2017-10-04
Name/Print	John W. LaBatt	Registration Number	48301

This collection of information is required by 37 CFR 1.97 and 1.98. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 1 hour to complete, including gathering, preparing and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

Privacy Act Statement

The Privacy Act of 1974 (P.L. 93-579) requires that you be given certain information in connection with your submission of the attached form related to a patent application or patent. Accordingly, pursuant to the requirements of the Act, please be advised that: (1) the general authority for the collection of this information is 35 U.S.C. 2(b)(2); (2) furnishing of the information solicited is voluntary; and (3) the principal purpose for which the information is used by the U.S. Patent and Trademark Office is to process and/or examine your submission related to a patent application or patent. If you do not furnish the requested information, the U.S. Patent and Trademark Office may not be able to process and/or examine your submission, which may result in termination of proceedings or abandonment of the application or expiration of the patent.

The information provided by you in this form will be subject to the following routine uses:

1. The information on this form will be treated confidentially to the extent allowed under the Freedom of Information Act (5 U.S.C. 552) and the Privacy Act (5 U.S.C. 552a). Records from this system of records may be disclosed to the Department of Justice to determine whether the Freedom of Information Act requires disclosure of these record s.

2. A record from this system of records may be disclosed, as a routine use, in the course of presenting evidence to a court, magistrate, or administrative tribunal, including disclosures to opposing counsel in the course of settlement negotiations.

3. A record in this system of records may be disclosed, as a routine use, to a Member of Congress submitting a request involving an individual, to whom the record pertains, when the individual has requested assistance from the Member with respect to the subject matter of the record.

4. A record in this system of records may be disclosed, as a routine use, to a contractor of the Agency having need for the information in order to perform a contract. Recipients of information shall be required to comply with the requirements of the Privacy Act of 1974, as amended, pursuant to 5 U.S.C. 552a(m).

5. A record related to an International Application filed under the Patent Cooperation Treaty in this system of records may be disclosed, as a routine use, to the International Bureau of the World Intellectual Property Organization, pursuant to the Patent Cooperation Treaty.

6. A record in this system of records may be disclosed, as a routine use, to another federal agency for purposes of National Security review (35 U.S.C. 181) and for review pursuant to the Atomic Energy Act (42 U.S.C. 218(c)).

7. A record from this system of records may be disclosed, as a routine use, to the Administrator, General Services, or his/her designee, during an inspection of records conducted by GSA as part of that agency's responsibility to recommend improvements in records management practices and programs, under authority of 44 U.S.C. 2904 and 2906. Such disclosure shall be made in accordance with the GSA regulations governing inspection of records for this purpose, and any other relevant (i.e., GSA or Commerce) directive. Such disclosure shall not be used to make determinations about individuals.

8. A record from this system of records may be disclosed, as a routine use, to the public after either publication of the application pursuant to 35 U.S.C. 122(b) or issuance of a patent pursuant to 35 U.S.C. 151. Further, a record may be disclosed, subject to the limitations of 37 CFR 1.14, as a routine use, to the public if the record was filed in an application which became abandoned or in which the proceedings were terminated and which application is referenced by either a published application, an application open to public inspections or an issued patent.

9. A record from this system of records may be disclosed, as a routine use, to a Federal, State, or local law enforcement agency, if the USPTO becomes aware of a violation or potential violation of law or regulation.

UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

BIB DATA SHEET

CONFIRMATION NO. 5890

SERIAL NUMBER	FILING or 371(c) DATE RULE	CLASS	GROUP ART UNIT	ATTORNEY DOCKET NO.
14/984,156	12/30/2015	257	2826	SETI-0110-CIP-US

APPLICANTS

Sensor Electronic Technology, Inc., Columbia, SC;

INVENTORS

Maxim S. Shatalov, Columbia, SC;
Alexander Dobrinsky, Loudonville, NY;
Alexander Lunev, Columbia, SC;
Rakesh Jain, Columbia, SC;
Jinwei Yang, Columbia, SC;
Michael Shur, Latham, NY;
Remigijus Gaska, Columbia, SC;

**** CONTINUING DATA ***************************

This application is a CIP of 14/189,012 02/25/2014 PAT 9331244
which claims benefit of 61/768,581 02/25/2013

**** FOREIGN APPLICATIONS ***************************

**** IF REQUIRED, FOREIGN FILING LICENSE GRANTED ****

01/15/2016

Foreign Priority claimed ☐ Yes ☑ No 35 USC 119(a-d) conditions met ☐ Yes ☐ No Verified and Acknowledged /FAZLI ERDEM/ Examiner's Signature	☐ Met after Allowance Initials	STATE OR COUNTRY	SHEETS DRAWINGS	TOTAL CLAIMS	INDEPENDENT CLAIMS
		SC	15	20	3

ADDRESS

LaBatt, LLC (SET)
PO Box 630
Valatie, NY 12184
UNITED STATES

TITLE

Semiconductor Structure with Inhomogeneous Regions

FILING FEE RECEIVED		
1740	FEES: Authority has been given in Paper No._____ to charge/credit DEPOSIT ACCOUNT No._____ for following:	☐ All Fees ☐ 1.16 Fees (Filing) ☐ 1.17 Fees (Processing Ext. of time) ☐ 1.18 Fees (Issue) ☐ Other _____ ☐ Credit

EAST Search History

EAST Search History (Prior Art)

Ref #	Hits	Search Query	DBs	Default Operator	Plurals	Time Stamp
L1	2	14/984156 and (reflective or conductive or transparent) same mirror same bragg same contact	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2017/10/20 11:56
L2	0	14/984156 and (reflective or conductive or transparent) same mirror same bragg same contact same buffer	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2017/10/20 11:56
L3	1	14/984156 and (reflective or conductive or transparent) same contact same buffer	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2017/10/20 11:56
L4	1	14/984156 and inhomogeneous same (reflective or conductive or transparent) same contact same buffer	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2017/10/20 11:57
L5	2	inhomogeneous same (reflective or conductive or transparent) same contact same buffer	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2017/10/20 11:57
L6	1	inhomogeneous same (reflective or conductive or transparent) same contact same buffer and 14/984,156	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2017/10/20 11:58
L7	2	inhomogeneous same (reflective or conductive or transparent) and contact same buffer and 14/984,156	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2017/10/20 11:58
L8	62	inhomogeneous same (reflective or	US-PGPUB;	OR	ON	2017/10/20

		conductive or transparent) and contact same buffer	USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB			12:19
L9	12	inhomogeneous same (reflective or conductive or transparent) and contact same buffer and offset	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2017/10/20 12:20
L10	11	inhomogeneous same (reflective or conductive or transparent) and contact same buffer and offset and level	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2017/10/20 12:20
L11	5	inhomogeneous same (reflective or conductive or transparent) and contact same buffer and (lateral or laterally) same offset and level	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2017/10/20 12:21
L12	5	inhomogeneous same (reflective or conductive or transparent) and contact same buffer and (lateral or laterally) same offset same level	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2017/10/20 12:21
L13	0	inhomogeneous same (reflective or conductive or transparent) and contact same buffer and (lateral or laterally) same offset same level.clm.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2017/10/20 12:21
L14	0	inhomogeneous same (lateral or laterally) same offset same level.clm.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2017/10/20 12:21
L15	0	inhomogeneous same (lateral or laterally) same offset same level	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2017/10/20 12:21
L16	0	inhomogeneous same (lateral or laterally) near2 offset same level	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT;	OR	ON	2017/10/20 12:25

			IBM_TDB			
L17	3	inhomogeneous same (lateral or laterally) near2 offset	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2017/10/20 12:25
L18	6	inhomogeneous same (vertical or vertically) near2 offset	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2017/10/20 12:25
L19	1	inhomogeneous same (vertical or vertically) near2 offset same level.clm.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2017/10/20 12:25
L20	2	inhomogeneous same (vertical or vertically) near2 offset same level same attributes	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2017/10/20 12:26
L21	5	inhomogeneous same attributes same (nitride near2 semiconductor).clm.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2017/10/20 12:33
L22	6	inhomogeneous same attributes same (nitride near2 semiconductor) same target	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2017/10/20 12:33
L23	5	inhomogeneous same attributes same (nitride near2 semiconductor) same target.clm.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2017/10/20 12:33
L24	5	inhomogeneous same attributes same (nitride near2 semiconductor) same target same set.clm.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2017/10/20 12:34
L25	4	inhomogeneous same attributes same (nitride near2 semiconductor) same target same set near2 second.clm.	US-PGPUB; USPAT; USOCR; FPRS; EPO;	OR	ON	2017/10/20 12:34

			JPO; DERWENT; IBM_TDB			
L26	6	14/189012	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2017/10/20 12:36
L27	6	"14189012"	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2017/10/20 12:36
L28	2252534	shatalov.in. or dobrinsky.in. or lunev.in. or jain.in. or yang.in. or shur.in. or gaska.in.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2017/10/20 12:50
L29	971	sensor near electronic.as. or sensor near electronic.aanm.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2017/10/20 12:50
L30	2252681	l28 or l29	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2017/10/20 12:50
L31	9	l30 and (inhomogeneous same (reflective or transparent or conductive) same attributes)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2017/10/20 12:50
L32	7	l30 and (inhomogeneous same (reflective or transparent or conductive) same attributes) same (((vertical or vertically) near2 offset) or (target near2 radiation))	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2017/10/20 12:51
L33	5	l30 and (inhomogeneous same (reflective or transparent or conductive) same attributes) same (((vertical or vertically) near2 offset) or (target near2 (vavelength or radiation))).clm.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2017/10/20 12:52
L34	5	l30 and set same (inhomogeneous same (reflective or transparent or	US-PGPUB; USPAT;	OR	ON	2017/10/20 12:53

		conductive) same attributes) same (((vertical or vertically) near2 offset) or (target near2 (vavelength or radiation))).clm.	USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB			
L35	3	l30 and set same (inhomogeneous same (reflective or transparent or conductive) same attributes) same (((vertical or vertically) near2 offset) or (target near2 (vavelength or radiation))).clm. and offset.clm.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2017/10/20 12:54
L36	0	l30 and set same (inhomogeneous same (reflective or transparent or conductive) same attributes) same (((vertical or vertically) near2 offset) or (target near2 (vavelength or radiation))).clm. and target near10 second near10 set.clm.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2017/10/20 12:54
L37	4	l30 and set same (inhomogeneous same (reflective or transparent or conductive) same attributes) same (((vertical or vertically) near2 offset) or (target near2 (vavelength or radiation))).clm. and target same second near10 set.clm.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2017/10/20 12:55
L38	34475	257/94.ccls. or H01L33/10.cpc. or H01L33/007.cpc. or H01L33/32.cpc.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2017/10/20 12:56
L39	4	l38 and set same (inhomogeneous same (reflective or transparent or conductive) same attributes) same (((vertical or vertically) near2 offset) or (target near2 (vavelength or radiation))).clm. and target same second near10 set.clm.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2017/10/20 12:56
L40	5	l38 and set same (inhomogeneous same (reflective or transparent or conductive) same attributes) same (((vertical or vertically) near2 offset) or (target near2 (vavelength or radiation))).clm.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2017/10/20 12:56
L41	5	l38 and set same (inhomogeneous same (reflective or transparent or conductive) same attributes) same (((vertical or vertically) near2 offset) or (target near2 (vavelength or radiation))) and bragg	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2017/10/20 12:56

10/20/2017 1:00:07 PM
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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Serial No.:	14/984,156	Conf. No.:	5890
Filing Date:	30 December 2015	Art Unit:	2826
Inventor(s):	Shatalov et al.	Examiner:	Erdem, Fazli
Title:	Semiconductor Structure with Inhomogeneous Regions	Docket No.:	SETI-0110-CIP-US

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Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

AFTER FINAL AMENDMENT

In response to the Final Office Action dated 4 August 2017 (hereafter the "Final"), Applicant requests further consideration and examination of the above-identified patent application in view of the following amendments and remarks. Applicant is submitting an After Final Consideration Pilot Program Request form with this correspondence, which contains Applicant's certification and request for consideration of this reply under the After Final Consideration Pilot 2.0 (AFCP 2.0) program.

EAST Search History

EAST Search History (Prior Art)

Ref #	Hits	Search Query	DBs	Default Operator	Plurals	Time Stamp
L1	2	14/984156 and (reflective or conductive or transparent) same mirror same bragg same contact	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2017/10/20 11:56
L2	0	14/984156 and (reflective or conductive or transparent) same mirror same bragg same contact same buffer	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2017/10/20 11:56
L3	1	14/984156 and (reflective or conductive or transparent) same contact same buffer	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2017/10/20 11:56
L4	1	14/984156 and inhomogeneous same (reflective or conductive or transparent) same contact same buffer	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2017/10/20 11:57
L5	2	inhomogeneous same (reflective or conductive or transparent) same contact same buffer	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2017/10/20 11:57
L6	1	inhomogeneous same (reflective or conductive or transparent) same contact same buffer and 14/984,156	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2017/10/20 11:58
L7	2	inhomogeneous same (reflective or conductive or transparent) and contact same buffer and 14/984,156	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2017/10/20 11:58
L8	62	inhomogeneous same (reflective or	US-PGPUB;	OR	ON	2017/10/20

		conductive or transparent) and contact same buffer	USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB			12:19
L9	12	inhomogeneous same (reflective or conductive or transparent) and contact same buffer and offset	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2017/10/20 12:20
L10	11	inhomogeneous same (reflective or conductive or transparent) and contact same buffer and offset and level	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2017/10/20 12:20
L11	5	inhomogeneous same (reflective or conductive or transparent) and contact same buffer and (lateral or laterally) same offset and level	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2017/10/20 12:21
L12	5	inhomogeneous same (reflective or conductive or transparent) and contact same buffer and (lateral or laterally) same offset same level	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2017/10/20 12:21
L13	0	inhomogeneous same (reflective or conductive or transparent) and contact same buffer and (lateral or laterally) same offset same level.clm.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2017/10/20 12:21
L14	0	inhomogeneous same (lateral or laterally) same offset same level.clm.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2017/10/20 12:21
L15	0	inhomogeneous same (lateral or laterally) same offset same level	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2017/10/20 12:21
L16	0	inhomogeneous same (lateral or laterally) near2 offset same level	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT;	OR	ON	2017/10/20 12:25

			IBM_TDB			
L17	3	inhomogeneous same (lateral or laterally) near2 offset	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2017/10/20 12:25
L18	6	inhomogeneous same (vertical or vertically) near2 offset	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2017/10/20 12:25
L19	1	inhomogeneous same (vertical or vertically) near2 offset same level.clm.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2017/10/20 12:25
L20	2	inhomogeneous same (vertical or vertically) near2 offset same level same attributes	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2017/10/20 12:26
L21	5	inhomogeneous same attributes same (nitride near2 semiconductor).clm.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2017/10/20 12:33
L22	6	inhomogeneous same attributes same (nitride near2 semiconductor) same target	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2017/10/20 12:33
L23	5	inhomogeneous same attributes same (nitride near2 semiconductor) same target.clm.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2017/10/20 12:33
L24	5	inhomogeneous same attributes same (nitride near2 semiconductor) same target same set.clm.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2017/10/20 12:34
L25	4	inhomogeneous same attributes same (nitride near2 semiconductor) same target same set near2 second.clm.	US-PGPUB; USPAT; USOCR; FPRS; EPO;	OR	ON	2017/10/20 12:34

			JPO; DERWENT; IBM_TDB			
L26	6	14/189012	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2017/10/20 12:36
L27	6	"14189012"	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2017/10/20 12:36
L28	2252534	shatalov.in. or dobrinsky.in. or lunev.in. or jain.in. or yang.in. or shur.in. or gaska.in.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2017/10/20 12:50
L29	971	sensor near electronic.as. or sensor near electronic.aanm.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2017/10/20 12:50
L30	2252681	l28 or l29	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2017/10/20 12:50
L31	9	l30 and (inhomogeneous same (reflective or transparent or conductive) same attributes)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2017/10/20 12:50
L32	7	l30 and (inhomogeneous same (reflective or transparent or conductive) same attributes) same (((vertical or vertically) near2 offset) or (target near2 radiation))	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2017/10/20 12:51
L33	5	l30 and (inhomogeneous same (reflective or transparent or conductive) same attributes) same (((vertical or vertically) near2 offset) or (target near2 (vavelength or radiation))).clm.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2017/10/20 12:52
L34	5	l30 and set same (inhomogeneous same (reflective or transparent or	US-PGPUB; USPAT;	OR	ON	2017/10/20 12:53

		conductive) same attributes) same (((vertical or vertically) near2 offset) or (target near2 (vavelength or radiation))).clm.	USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB			
L35	3	l30 and set same (inhomogeneous same (reflective or transparent or conductive) same attributes) same (((vertical or vertically) near2 offset) or (target near2 (vavelength or radiation))).clm. and offset.clm.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2017/10/20 12:54
L36	0	l30 and set same (inhomogeneous same (reflective or transparent or conductive) same attributes) same (((vertical or vertically) near2 offset) or (target near2 (vavelength or radiation))).clm. and target near10 second near10 set.clm.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2017/10/20 12:54
L37	4	l30 and set same (inhomogeneous same (reflective or transparent or conductive) same attributes) same (((vertical or vertically) near2 offset) or (target near2 (vavelength or radiation))).clm. and target same second near10 set.clm.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2017/10/20 12:55
L38	34475	257/94.ccls. or H01L33/10.cpc. or H01L33/007.cpc. or H01L33/32.cpc.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2017/10/20 12:56
L39	4	l38 and set same (inhomogeneous same (reflective or transparent or conductive) same attributes) same (((vertical or vertically) near2 offset) or (target near2 (vavelength or radiation))).clm. and target same second near10 set.clm.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2017/10/20 12:56
L40	5	l38 and set same (inhomogeneous same (reflective or transparent or conductive) same attributes) same (((vertical or vertically) near2 offset) or (target near2 (vavelength or radiation))).clm.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2017/10/20 12:56
L41	5	l38 and set same (inhomogeneous same (reflective or transparent or conductive) same attributes) same (((vertical or vertically) near2 offset) or (target near2 (vavelength or radiation))) and bragg	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2017/10/20 12:56
L55	3	"15069178"	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2017/10/20 13:04

L56	9	("20150243840" | "20160118536" | "5602418" | "20160197228" | "20090272993" | "20130146907" | "20130320352" | "20140016660" | "7812366").PN.	US-PGPUB; USPAT	OR	ON	2017/10/20 13:05
L57	160	("20150243840" | "20160118536" | "5602418" | "20160197228" | "20090272993" | "20130146907" | "20130320352" | "20140016660" | "7812366")	US-PGPUB; USPAT	OR	ON	2017/10/20 13:07
L58	27	l57 and bragg	US-PGPUB; USPAT	OR	ON	2017/10/20 13:07
L59	21	l58 and reflective same (conductive or transparent)	US-PGPUB; USPAT	OR	ON	2017/10/20 13:07
L60	18	l59 and attributes	US-PGPUB; USPAT	OR	ON	2017/10/20 13:07
L61	6	l59 and attributes same set.clm.	US-PGPUB; USPAT	OR	ON	2017/10/20 13:08
L62	37	"20120049152" or "6946682"	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2017/10/20 13:10
L63	4	l62 and (sensor or optoelectronic or photodiode or photodetector or detector).clm.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2017/10/20 13:11
L64	0	l63 and offset	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2017/10/20 13:11
L65	1	l57 and (vertical or vertically) same offset same level	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2017/10/20 13:12

10/ 20/ 2017 1:12:30 PM
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PTO/SB/08a (03-15)
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INFORMATION DISCLOSURE STATEMENT BY APPLICANT

(Not for submission under 37 CFR 1.99)

Application Number	14984156
Filing Date	2015-12-30
First Named Inventor	Shatalov et al.
Art Unit	2811
Examiner Name	Erdem, Fazli
Attorney Docket Number	SETI-0110-CIP-US

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INFORMATION DISCLOSURE STATEMENT BY APPLICANT (Not for submission under 37 CFR 1.99)		
	Application Number	14984156
	Filing Date	2015-12-30
	First Named Inventor	Shatalov et al.
	Art Unit	2811
	Examiner Name	Erdem, Fazli
	Attorney Docket Number	SETI-0110-CIP-US

	1	TRAN, M., Application No. 15/069,178, Attorney Docket No. SETI-0110-US2, Notice of Allowance, 26 October 2017, 12 pages
	2	ERDEM, F., Application No. 15/225,403, Attorney Docket No. SETI-0110-CIP2-US, Notice of Allowance, 30 October 2017, 10 pages

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EXAMINER SIGNATURE

Examiner Signature		Date Considered	

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[1] See Kind Codes of USPTO Patent Documents at www.USPTO.GOV or MPEP 901.04. [2] Enter office that issued the document, by the two-letter code (WIPO Standard ST.3). [3] For Japanese patent documents, the indication of the year of the reign of the Emperor must precede the serial number of the patent document. [4] Kind of document by the appropriate symbols as indicated on the document under WIPO Standard ST.16 if possible. [5] Applicant is to place a check mark here if English language translation is attached.

INFORMATION DISCLOSURE STATEMENT BY APPLICANT

(Not for submission under 37 CFR 1.99)

Application Number	14984156
Filing Date	2015-12-30
First Named Inventor	Shatalov et al.
Art Unit	2811
Examiner Name	Erdem, Fazli
Attorney Docket Number	SETI-0110-CIP-US

CERTIFICATION STATEMENT

Please see 37 CFR 1.97 and 1.98 to make the appropriate selection(s):

That each item of information contained in the information disclosure statement was first cited in any communication from a foreign patent office in a counterpart foreign application not more than three months prior to the filing of the information disclosure statement. See 37 CFR 1.97(e)(1).

OR

☒ That no item of information contained in the information disclosure statement was cited in a communication from a foreign patent office in a counterpart foreign application, and, to the knowledge of the person signing the certification after making reasonable inquiry, no item of information contained in the information disclosure statement was known to any individual designated in 37 CFR 1.56(c) more than three months prior to the filing of the information disclosure statement. See 37 CFR 1.97(e)(2).

See attached certification statement.

☒ The fee set forth in 37 CFR 1.17 (p) has been submitted herewith.

A certification statement is not submitted herewith.

SIGNATURE

A signature of the applicant or representative is required in accordance with CFR 1.33, 10.18. Please see CFR 1.4(d) for the form of the signature.

Signature	/John W. LaBatt/	Date (YYYY-MM-DD)	2018-01-25
Name/Print	John W. LaBatt	Registration Number	48301

This collection of information is required by 37 CFR 1.97 and 1.98. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 1 hour to complete, including gathering, preparing and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

Privacy Act Statement

The Privacy Act of 1974 (P.L. 93-579) requires that you be given certain information in connection with your submission of the attached form related to a patent application or patent. Accordingly, pursuant to the requirements of the Act, please be advised that: (1) the general authority for the collection of this information is 35 U.S.C. 2(b)(2); (2) furnishing of the information solicited is voluntary; and (3) the principal purpose for which the information is used by the U.S. Patent and Trademark Office is to process and/or examine your submission related to a patent application or patent. If you do not furnish the requested information, the U.S. Patent and Trademark Office may not be able to process and/or examine your submission, which may result in termination of proceedings or abandonment of the application or expiration of the patent.

The information provided by you in this form will be subject to the following routine uses:

1. The information on this form will be treated confidentially to the extent allowed under the Freedom of Information Act (5 U.S.C. 552) and the Privacy Act (5 U.S.C. 552a). Records from this system of records may be disclosed to the Department of Justice to determine whether the Freedom of Information Act requires disclosure of these record s.

2. A record from this system of records may be disclosed, as a routine use, in the course of presenting evidence to a court, magistrate, or administrative tribunal, including disclosures to opposing counsel in the course of settlement negotiations.

3. A record in this system of records may be disclosed, as a routine use, to a Member of Congress submitting a request involving an individual, to whom the record pertains, when the individual has requested assistance from the Member with respect to the subject matter of the record.

4. A record in this system of records may be disclosed, as a routine use, to a contractor of the Agency having need for the information in order to perform a contract. Recipients of information shall be required to comply with the requirements of the Privacy Act of 1974, as amended, pursuant to 5 U.S.C. 552a(m).

5. A record related to an International Application filed under the Patent Cooperation Treaty in this system of records may be disclosed, as a routine use, to the International Bureau of the World Intellectual Property Organization, pursuant to the Patent Cooperation Treaty.

6. A record in this system of records may be disclosed, as a routine use, to another federal agency for purposes of National Security review (35 U.S.C. 181) and for review pursuant to the Atomic Energy Act (42 U.S.C. 218(c)).

7. A record from this system of records may be disclosed, as a routine use, to the Administrator, General Services, or his/her designee, during an inspection of records conducted by GSA as part of that agency's responsibility to recommend improvements in records management practices and programs, under authority of 44 U.S.C. 2904 and 2906. Such disclosure shall be made in accordance with the GSA regulations governing inspection of records for this purpose, and any other relevant (i.e., GSA or Commerce) directive. Such disclosure shall not be used to make determinations about individuals.

8. A record from this system of records may be disclosed, as a routine use, to the public after either publication of the application pursuant to 35 U.S.C. 122(b) or issuance of a patent pursuant to 35 U.S.C. 151. Further, a record may be disclosed, subject to the limitations of 37 CFR 1.14, as a routine use, to the public if the record was filed in an application which became abandoned or in which the proceedings were terminated and which application is referenced by either a published application, an application open to public inspections or an issued patent.

9. A record from this system of records may be disclosed, as a routine use, to a Federal, State, or local law enforcement agency, if the USPTO becomes aware of a violation or potential violation of law or regulation.

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Serial No.:	14/984,156	Conf. No.:	5890
Filing Date:	30 December 2015	Art Unit:	2826
Inventor(s):	Shatalov et al.	Examiner:	Erdem, Fazli
Title:	Semiconductor Structure with Inhomogeneous Regions	Docket No.:	SETI-0110-CIP-US

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Authorization to Charge Deposit Account

For the above-referenced matter, the Director is hereby authorized to:

☒ Charge any additional fee(s) or underpayment of fee(s); and

☒ Credit any overpayment of fee(s),

to Deposit Account Number: **506059**.

Respectfully submitted,

John W. LaBatt, Reg. No. 48,301
LaBatt, LLC
PO Box 630
Valatie, NY 12184
(518) 755-3658 - Telephone
(518) 514-1360 - Facsimile

Dated: 25 January 2018

Electronic Patent Application Fee Transmittal

Application Number:	14984156
Filing Date:	30-Dec-2015
Title of Invention:	Semiconductor Structure with Inhomogeneous Regions
First Named Inventor/Applicant Name:	Maxim S. Shatalov
Filer:	John W LaBatt
Attorney Docket Number:	SETI-0110-CIP-US

Filed as Large Entity

Filing Fees for Utility under 35 USC 111(a)

Description	Fee Code	Quantity	Amount	Sub-Total in USD($)
Basic Filing:				
Pages:				
Claims:				
Miscellaneous-Filing:				
Petition:				
Patent-Appeals-and-Interference:				
Post-Allowance-and-Post-Issuance:				
UTILITY APPL ISSUE FEE	1501	1	960	960

Description	Fee Code	Quantity	Amount	Sub-Total in USD($)
Extension-of-Time:				
Miscellaneous:				
Submission- Information Disclosure Stmt	1806	1	240	240
		Total in USD ($)		**1200**

Electronic Acknowledgement Receipt

EFS ID:	31600445
Application Number:	14984156
International Application Number:	
Confirmation Number:	5890
Title of Invention:	Semiconductor Structure with Inhomogeneous Regions
First Named Inventor/Applicant Name:	Maxim S. Shatalov
Customer Number:	11698
Filer:	John W LaBatt
Filer Authorized By:	
Attorney Docket Number:	SETI-0110-CIP-US
Receipt Date:	25-JAN-2018
Filing Date:	30-DEC-2015
Time Stamp:	16:12:49
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	yes
Payment Type	CARD
Payment was successfully received in RAM	$1200
RAM confirmation Number	012618INTEFSW16155400
Deposit Account	
Authorized User	

The Director of the USPTO is hereby authorized to charge indicated fees and credit any overpayment as follows:

File Listing:

Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1	Issue Fee Payment (PTO-85B)	SETI-0110-CIP-US_IssueFeeTransmittal.pdf	1019405 cc7495c46a0cd3dea8c2a681daa12f3f9f086402	no	1
Warnings:					
Information:					
2	Information Disclosure Statement (IDS) Form (SB08)	SETI-0110-CIP-US_IDS5.pdf	1035059 69eb8e62aa5ba4efbf1f3727e0bf8fc9fee73aae	no	4
Warnings:					
Information:					
A U.S. Patent Number Citation or a U.S. Publication Number Citation is required in the Information Disclosure Statement (IDS) form for autoloading of data into USPTO systems. You may remove the form to add the required data in order to correct the Informational Message if you are citing U.S. References. If you chose not to include U.S. References, the image of the form will be processed and be made available within the Image File Wrapper (IFW) system. However, no data will be extracted from this form. Any additional data such as Foreign Patent Documents or Non Patent Literature will be manually reviewed and keyed into USPTO systems.					
3	Non Patent Literature	SETI-0110-US2_NoticeofAllowance_10-26-17.pdf	663034 46e719728ea037e01c2b620b47e35f6bf19fd00c	no	12
Warnings:					
Information:					
4	Non Patent Literature	SETI-0110-CIP2-US_NoticeofAllowance-AFCPDecision_10-30-17.pdf	500640 d09bd9fc96c9265ea95f68964c3cdb23741def1b	no	10
Warnings:					
Information:					
5	Post Allowance Communication - Incoming	SETI-0110-CIP-US_AuthorizationtoChargeDepositAccount.pdf	41251 03934585f2c92bc967c824f4c2fda57ee5da653c	no	1
Warnings:					
Information:					

6	Fee Worksheet (SB06)	fee-info.pdf	32280 ff921bc3d4c5b4f644d6c90efb80f359ad814502	no	2

Warnings:	
Information:	
Total Files Size (in bytes):	3291669

This Acknowledgement Receipt evidences receipt on the noted date by the USPTO of the indicated documents, characterized by the applicant, and including page counts, where applicable. It serves as evidence of receipt similar to a Post Card, as described in MPEP 503.

New Applications Under 35 U.S.C. 111

If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application.

National Stage of an International Application under 35 U.S.C. 371

If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.

New International Application Filed with the USPTO as a Receiving Office

If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.

PART B - FEE(S) TRANSMITTAL

Complete and send this form, together with applicable fee(s), to: Mail **Mail Stop ISSUE FEE**
Commissioner for Patents
P.O. Box 1450
Alexandria, Virginia 22313-1450
or Fax (571)-273-2885

INSTRUCTIONS: This form should be used for transmitting the ISSUE FEE and PUBLICATION FEE (if required). Blocks 1 through 5 should be completed where appropriate. All further correspondence including the Patent, advance orders and notification of maintenance fees will be mailed to the current correspondence address as indicated unless corrected below or directed otherwise in Block 1, by (a) specifying a new correspondence address; and/or (b) indicating a separate "FEE ADDRESS" for maintenance fee notifications.

CURRENT CORRESPONDENCE ADDRESS (Note: Use Block 1 for any change of address)

11698 7590 10/27/2017
LaBatt, LLC (SET)
PO Box 630
Valatie, NY 12184

Note: A certificate of mailing can only be used for domestic mailings of the Fee(s) Transmittal. This certificate cannot be used for any other accompanying papers. Each additional paper, such as an assignment or formal drawing, must have its own certificate of mailing or transmission.

Certificate of Mailing or Transmission
I hereby certify that this Fee(s) Transmittal is being deposited with the United States Postal Service with sufficient postage for first class mail in an envelope addressed to the Mail Stop ISSUE FEE address above, or being facsimile transmitted to the USPTO (571) 273-2885, on the date indicated below.

(Depositor's name)
(Signature)
(Date)

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
14/984,156	12/30/2015	Maxim S. Shatalov	SETI-0110-CIP-US	5890

TITLE OF INVENTION: Semiconductor Structure with Inhomogeneous Regions

APPLN. TYPE	ENTITY STATUS	ISSUE FEE DUE	PUBLICATION FEE DUE	PREV. PAID ISSUE FEE	TOTAL FEE(S) DUE	DATE DUE
nonprovisional	UNDISCOUNTED	$960	$0	$0	$960	01/29/2018

EXAMINER	ART UNIT	CLASS-SUBCLASS
ERDEM, FAZLI	2826	257-094000

1. Change of correspondence address or indication of "Fee Address" (37 CFR 1.363).
☐ Change of correspondence address (or Change of Correspondence Address form PTO/SB/122) attached.
☐ "Fee Address" indication (or "Fee Address" Indication form PTO/SB/47; Rev 03-02 or more recent) attached. **Use of a Customer Number is required.**

2. For printing on the patent front page, list
(1) The names of up to 3 registered patent attorneys or agents OR, alternatively,
(2) The name of a single firm (having as a member a registered attorney or agent) and the names of up to 2 registered patent attorneys or agents. If no name is listed, no name will be printed.
1 LaBatt, LLC
2
3

3. ASSIGNEE NAME AND RESIDENCE DATA TO BE PRINTED ON THE PATENT (print or type)

PLEASE NOTE: Unless an assignee is identified below, no assignee data will appear on the patent. If an assignee is identified below, the document has been filed for recordation as set forth in 37 CFR 3.11. Completion of this form is NOT a substitute for filing an assignment.

(A) NAME OF ASSIGNEE: Sensor Electronic Technology, Inc.
(B) RESIDENCE: (CITY and STATE OR COUNTRY): Columbia, South Carolina

Please check the appropriate assignee category or categories (will not be printed on the patent) : ☐ Individual ☒ Corporation or other private group entity ☐ Government

4a. The following fee(s) are submitted:
☒ Issue Fee
☒ Publication Fee (No small entity discount permitted)
☐ Advance Order - # of Copies _____

4b. Payment of Fee(s): **(Please first reapply any previously paid issue fee shown above)**
☐ A check is enclosed.
☒ Payment by credit card. ~~Form PTO-2038 is attached.~~
☒ The director is hereby authorized to charge the required fee(s), any deficiency, or credits any overpayment, to Deposit Account Number 506059 (enclose an extra copy of this form).

5. **Change in Entity Status** (from status indicated above)
☐ Applicant certifying micro entity status. See 37 CFR 1.29
NOTE: Absent a valid certification of Micro Entity Status (see forms PTO/SB/15A and 15B), issue fee payment in the micro entity amount will not be accepted at the risk of application abandonment.
☐ Applicant asserting small entity status. See 37 CFR 1.27
NOTE: If the application was previously under micro entity status, checking this box will be taken to be a notification of loss of entitlement to micro entity status.
☐ Applicant changing to regular undiscounted fee status.
NOTE: Checking this box will be taken to be a notification of loss of entitlement to small or micro entity status, as applicable.

NOTE: This form must be signed in accordance with 37 CFR 1.31 and 1.33. See 37 CFR 1.4 for signature requirements and certifications.

Authorized Signature /John W. LaBatt/ Date 25 January 2018
Typed or printed name John W. LaBatt Registration No. 48,301

UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
14/984,156	12/30/2015	Maxim S. Shatalov	SETI-0110-CIP-US	5890

11698 7590 02/16/2018

LaBatt, LLC (SET)
PO Box 630
Valatie, NY 12184

EXAMINER
ERDEM, FAZLI

ART UNIT	PAPER NUMBER
2826	

NOTIFICATION DATE	DELIVERY MODE
02/16/2018	ELECTRONIC

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

adobrinsky@s-et.com
national@labattlaw.com

Corrected Notice of Allowability	Application No. 14/984,156	Applicant(s) SHATALOV ET AL.	
	Examiner FAZLI ERDEM	Art Unit 2826	AIA (First Inventor to File) Status Yes

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address--

All claims being allowable, PROSECUTION ON THE MERITS IS (OR REMAINS) CLOSED in this application. If not included herewith (or previously mailed), a Notice of Allowance (PTOL-85) or other appropriate communication will be mailed in due course. **THIS NOTICE OF ALLOWABILITY IS NOT A GRANT OF PATENT RIGHTS.** This application is subject to withdrawal from issue at the initiative of the Office or upon petition by the applicant. See 37 CFR 1.313 and MPEP 1308.

1. ☒ This communication is responsive to *IDS filed on 1/25/2018*.
   ☐ A declaration(s)/affidavit(s) under **37 CFR 1.130(b)** was/were filed on_____.
2. ☐ An election was made by the applicant in response to a restriction requirement set forth during the interview on _____; the restriction requirement and election have been incorporated into this action.
3. ☒ The allowed claim(s) is/are *1-20*. As a result of the allowed claim(s), you may be eligible to benefit from the **Patent Prosecution Highway** program at a participating intellectual property office for the corresponding application. For more information, please see http://www.uspto.gov/patents/init_events/pph/index.jsp or send an inquiry to PPHfeedback@uspto.gov.
4. ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

   Certified copies:

   a) ☐ All b) ☐ Some *c) ☐ None of the:
   1. ☐ Certified copies of the priority documents have been received.
   2. ☐ Certified copies of the priority documents have been received in Application No. _____ .
   3. ☐ Copies of the certified copies of the priority documents have been received in this national stage application from the International Bureau (PCT Rule 17.2(a)).

   * Certified copies not received: _____.

Applicant has THREE MONTHS FROM THE "MAILING DATE" of this communication to file a reply complying with the requirements noted below. Failure to timely comply will result in ABANDONMENT of this application.
THIS THREE-MONTH PERIOD IS NOT EXTENDABLE.

5. ☐ CORRECTED DRAWINGS (as "replacement sheets") must be submitted.
   ☐ including changes required by the attached Examiner's Amendment / Comment or in the Office action of Paper No./Mail Date _____.

   Identifying indicia such as the application number (see 37 CFR 1.84(c)) should be written on the drawings in the front (not the back) of each sheet. Replacement sheet(s) should be labeled as such in the header according to 37 CFR 1.121(d).
6. ☐ DEPOSIT OF and/or INFORMATION about the deposit of BIOLOGICAL MATERIAL must be submitted. Note the attached Examiner's comment regarding REQUIREMENT FOR THE DEPOSIT OF BIOLOGICAL MATERIAL.

Attachment(s)

1. ☐ Notice of References Cited (PTO-892)
2. ☒ Information Disclosure Statements (PTO/SB/08), Paper No./Mail Date 1/25/2018
3. ☐ Examiner's Comment Regarding Requirement for Deposit of Biological Material
4. ☐ Interview Summary (PTO-413), Paper No./Mail Date _____ .
5. ☐ Examiner's Amendment/Comment
6. ☐ Examiner's Statement of Reasons for Allowance
7. ☐ Other _____.

/FAZLI ERDEM/
Examiner, Art Unit 2826

PTO/SB/08a (03-15)
Approved for use through 07/31/2016. OMB 0651-0031
U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE

INFORMATION DISCLOSURE STATEMENT BY APPLICANT

(Not for submission under 37 CFR 1.99)

Application Number	14984156
Filing Date	2015-12-30
First Named Inventor	Shatalov et al.
Art Unit	2811
Examiner Name	Erdem, Fazli
Attorney Docket Number	SETI-0110-CIP-US

U.S.PATENTS Remove

Examiner Initial*	Cite No	Patent Number	Kind Code[1]	Issue Date	Name of Patentee or Applicant of cited Document	Pages,Columns,Lines where Relevant Passages or Relevant Figures Appear
	1					

If you wish to add additional U.S. Patent citation information please click the Add button. Add

U.S.PATENT APPLICATION PUBLICATIONS Remove

Examiner Initial*	Cite No	Publication Number	Kind Code[1]	Publication Date	Name of Patentee or Applicant of cited Document	Pages,Columns,Lines where Relevant Passages or Relevant Figures Appear
	1					

If you wish to add additional U.S. Published Application citation information please click the Add button. Add

FOREIGN PATENT DOCUMENTS Remove

Examiner Initial*	Cite No	Foreign Document Number[3]	Country Code[2] i	Kind Code[4]	Publication Date	Name of Patentee or Applicant of cited Document	Pages,Columns,Lines where Relevant Passages or Relevant Figures Appear	T[5]
	1							

If you wish to add additional Foreign Patent Document citation information please click the Add button Add

NON-PATENT LITERATURE DOCUMENTS Remove

Examiner Initials*	Cite No	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc), date, pages(s), volume-issue number(s), publisher, city and/or country where published.	T[5]

INFORMATION DISCLOSURE STATEMENT BY APPLICANT (Not for submission under 37 CFR 1.99)		
	Application Number	14984156
	Filing Date	2015-12-30
	First Named Inventor	Shatalov et al.
	Art Unit	2811
	Examiner Name	Erdem, Fazli
	Attorney Docket Number	SETI-0110-CIP-US

/F.E/	1	TRAN, M., Application No. 15/069,178, Attorney Docket No. SETI-0110-US2, Notice of Allowance, 26 October 2017, 12 pages
/F.E/	2	ERDEM, F., Application No. 15/225,403, Attorney Docket No. SETI-0110-CIP2-US, Notice of Allowance, 30 October 2017, 10 pages

If you wish to add additional non-patent literature document citation information please click the Add button Add

EXAMINER SIGNATURE

Examiner Signature	/FAZLI ERDEM/	Date Considered	02/12/2018

*EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through a citation if not in conformance and not considered. Include copy of this form with next communication to applicant.

[1] See Kind Codes of USPTO Patent Documents at www.USPTO.GOV or MPEP 901.04. [2] Enter office that issued the document, by the two-letter code (WIPO Standard ST.3). [3] For Japanese patent documents, the indication of the year of the reign of the Emperor must precede the serial number of the patent document. [4] Kind of document by the appropriate symbols as indicated on the document under WIPO Standard ST.16 if possible. [5] Applicant is to place a check mark here if English language translation is attached.

INFORMATION DISCLOSURE STATEMENT BY APPLICANT

(Not for submission under 37 CFR 1.99)

Application Number	14984156
Filing Date	2015-12-30
First Named Inventor	Shatalov et al.
Art Unit	2811
Examiner Name	Erdem, Fazli
Attorney Docket Number	SETI-0110-CIP-US

CERTIFICATION STATEMENT

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OR

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See attached certification statement.

☒ The fee set forth in 37 CFR 1.17 (p) has been submitted herewith.

A certification statement is not submitted herewith.

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Signature	/John W. LaBatt/	Date (YYYY-MM-DD)	2018-01-25
Name/Print	John W. LaBatt	Registration Number	48301

This collection of information is required by 37 CFR 1.97 and 1.98. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 1 hour to complete, including gathering, preparing and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

Privacy Act Statement

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The information provided by you in this form will be subject to the following routine uses:

1. The information on this form will be treated confidentially to the extent allowed under the Freedom of Information Act (5 U.S.C. 552) and the Privacy Act (5 U.S.C. 552a). Records from this system of records may be disclosed to the Department of Justice to determine whether the Freedom of Information Act requires disclosure of these record s.

2. A record from this system of records may be disclosed, as a routine use, in the course of presenting evidence to a court, magistrate, or administrative tribunal, including disclosures to opposing counsel in the course of settlement negotiations.

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5. A record related to an International Application filed under the Patent Cooperation Treaty in this system of records may be disclosed, as a routine use, to the International Bureau of the World Intellectual Property Organization, pursuant to the Patent Cooperation Treaty.

6. A record in this system of records may be disclosed, as a routine use, to another federal agency for purposes of National Security review (35 U.S.C. 181) and for review pursuant to the Atomic Energy Act (42 U.S.C. 218(c)).

7. A record from this system of records may be disclosed, as a routine use, to the Administrator, General Services, or his/her designee, during an inspection of records conducted by GSA as part of that agency's responsibility to recommend improvements in records management practices and programs, under authority of 44 U.S.C. 2904 and 2906. Such disclosure shall be made in accordance with the GSA regulations governing inspection of records for this purpose, and any other relevant (i.e., GSA or Commerce) directive. Such disclosure shall not be used to make determinations about individuals.

8. A record from this system of records may be disclosed, as a routine use, to the public after either publication of the application pursuant to 35 U.S.C. 122(b) or issuance of a patent pursuant to 35 U.S.C. 151. Further, a record may be disclosed, subject to the limitations of 37 CFR 1.14, as a routine use, to the public if the record was filed in an application which became abandoned or in which the proceedings were terminated and which application is referenced by either a published application, an application open to public inspections or an issued patent.

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ISSUE NOTIFICATION

The projected patent number and issue date are specified above.

Determination of Patent Term Adjustment under 35 U.S.C. 154 (b)
(application filed on or after May 29, 2000)

The Patent Term Adjustment is 0 day(s). Any patent to issue from the above-identified application will include an indication of the adjustment on the front page.

If a Continued Prosecution Application (CPA) was filed in the above-identified application, the filing date that determines Patent Term Adjustment is the filing date of the most recent CPA.

Applicant will be able to obtain more detailed information by accessing the Patent Application Information Retrieval (PAIR) WEB site (http://pair.uspto.gov).

Any questions regarding the Patent Term Extension or Adjustment determination should be directed to the Office of Patent Legal Administration at (571)-272-7702. Questions relating to issue and publication fee payments should be directed to the Application Assistance Unit (AAU) of the Office of Data Management (ODM) at (571)-272-4200.

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