IN THE UNITED STATES DISTRICT COURT 1 FOR THE EASTERN DISTRICT OF TEXAS 2 MARSHALL DIVISION TQ DELTA, LLC., CAUSE NO. 2:21-CV-310-JRG 3 () (Lead Case) Plaintiff, 4 5 vs. COMMSCOPE HOLDING COMPANY, 6 INC., et al., 7 Defendants. 8 CAUSE NO. 2:21-CV-309-JRG TQ DELTA, LLC., () (Member Case) 9 Plaintiff, 10 vs. 11 NOKIA OF AMERICA CORPORATION, MARSHALL, TEXAS et al., 12) JUNE 1, 2022 (Defendants.) 9:00 A.M. 13 14 15 16 MARKMAN HEARING 17 BEFORE THE HONORABLE RODNEY GILSTRAP UNITED STATES CHIEF DISTRICT JUDGE 18 19 20 TQ Delta Exhibit 2012 21 COMMSCOPE, INC. v. TQ DELTA, LLC IPR2022-00833 22 SHAWN McROBERTS, RMR, CRR 100 E. HOUSTON STREET 23 MARSHALL, TEXAS 75670 (903) 923-8546 24 shawn_mcroberts@txed.uscourts.gov 25

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MR. ONG: Nothing further on that term, Your Honor. 1 Thank you. 2 THE COURT: Okay. Thank you. 3 All right. Let me ask you this, counsel. Item 7 here, 4 5 hasn't this really already been covered? Do we need to argue 6 this separately before we go on to 'shared memory'; the 'each bonded transceiver utilizing/selecting at least one 7 transmission parameter to reduce a difference in latency 8 between the bonded transceivers'? I mean, didn't we just 9 cover that, in essence. 10 MR. HURT: Yes. Christian Hurt for the Plaintiff. 11 Yes, Your Honor, those two terms were briefed together, 12 argued together. There's no separate argument, at least from 13 Plaintiff's view, between the two -- what is item 6 in the 4-3 14 chart and item 7 in the 4-3 chart. 15 16 THE COURT: Do you agree with that, Mr. Ong? 17 MR. ONG: We do, Your Honor. THE COURT: Okay. Then let's move on, in light of 18 that, to 'shared memory'/'sharing the memory'/'a memory 19 wherein the memory is operable to be shared.' 20 Let's start with Plaintiff. 21 MR. McANDREWS: Good morning, Your Honor. Peter 2.2 McAndrews for Plaintiff. 23 THE COURT: Go ahead, counsel. 24 So the dispute with 'shared memory' MR. McANDREWS: 25

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1 is TQ Delta wants to stick with the construction that was 2 provided in Delaware. Defendants want to go with plain and 3 ordinary. And the reason for that is because there's two 4 types of what they would potentially call shared memory that 5 are inconsistent with the usage of the term in the patent 6 specification and in the claims.

7 So the claims speak to allocating memory. I'm sorry. 8 The claims speak to 'allocating shared memory between an 9 interleaver function and a deinterleaver function'. The 10 construction that Judge Andrews provided was 'common memory 11 used by at least two functions where a portion of the memory 12 can be used by either one of the functions'.

And what this construction does is it eliminates two 13 other types of memory that the Defendants we believe would 14 like to call shared memory. One of them is -- and it's best 15 to look at figure 1 of the patent just for a baseline here. 16 17 So in figure 1, it shows a shared memory element 120 that sits between the transmitter portion that has interleavers in it 18 and the receiver portion that has deinterleavers in it. This 19 is a single transceiver, so it transmits information outward 20 and it receives information inward; it interleaves for data 21 leaving the device; it deinterleaves for data entering the 2.2 device. 23

24 So one of the types of memory that they'd like to call 25 shared memory is something called interprocess memory where

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what it would require is the deinterleaver and interleaver of 1 the same device are using this memory block to pass 2 information to each other. And, of course, that doesn't make 3 This transceiver is communicating with a device on any sense. 4 the other end of the line, so it doesn't make any sense for 5 6 the interleaver to be communicating through the shared memory with a deinterleaver. So that's one thing that Judge Andrews' 7 construction eliminates. 8

The other thing that Judge Andrews' construction 9 eliminates is merely having a common pool of memory where some 10 portion of it is used for the interleaver and another portion 11 is used for the deinterleaver, but those can never cross over; 12 you can never -- you have a hard line -- yes, it's a common 13 pool of memory, but there's a hard line where a particular 14 portion of that memory will only ever be used for one 15 function, like the interleaver, and the other portion will 16 17 only ever be used for the deinterleaver.

The reason why we know that that's inconsistent with the 18 specification, Your Honor, and it's actually best illustrated 19 by the examples provided in column 6, 7, and 8 of the patent, 20 21 and so it's describing a common pool of memory of the amount of 20 kilobytes, and then it gives examples of different types 2.2 of allocations. In one allocation, one latency path, so the 23 interleaver, for example, is using 16 kilobytes of memory of 24 the 20; the other latency path, the deinterleaver, for 25

1	example, is using four kilobytes, and so we've got a $16/4$
2	split within the 20 kilobytes of memory. That's example 1.
3	Example 3 describes where, instead, you have one latency
4	path is 10 kilobytes and the other latency path is 10
5	kilobytes, you still have a total of 20, but now six of the
6	kilobytes of memory that were once used for the interleaver
7	are now being used for the deinterleaver. And so the concept
8	is you have this flexible memory that allows some portion of
9	it to be used for one function at one time and a different
10	function at another time.
11	There's actually while it's not describing this, one
12	way to think of how prior art would have worked is in column
13	8, around line 15, it's describing three latency paths, so
14	perhaps two interleavers and a deinterleaver, and it's saying
15	each of them could be a maximum of 16 big, 16 in size.
16	In the prior art when you had even if you had a common
17	pool of memory, those would there would be a hard line
18	dividing them, so you would need 48 kilobytes of memory.
19	You've got 16, 16, and 16. But what this is saying is that's
20	the maximum I can use for any particular latency path, but
21	then it gives a third I'm sorry. It gives an additional
22	restriction and says, Well, I only have a 20 of total shared
23	memory, so now we've got to figure out how to divide that up.
24	So we can use 20, but we can't use the full maximum on any
25	particular latency path.

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1	So these examples are illustrating the idea of common
2	memory, but common memory where some portion of it is can
3	be used for interleaving at one time and deinterleaving at
4	another time.
5	THE COURT: Does 'can be used for interleaving at
6	one time and can be used for deinterleaving at another time'
7	necessarily equate to 'at some time must be used'? I mean,
8	does the ability to use this flexible memory, it's does it
9	mean that over time it will necessarily have to be used in
10	both functions?
11	MR. McANDREWS: Your Honor, it does not mean that.
12	It would mean that you have hardware set up, so, first of all,
13	that the memory hardware is accessible by both the interleaver
14	and deinterleaver functions, so that would be one thing that
15	is a requirement for it to be capable of or that it can do
16	this. The other thing is the way the source code is written
17	is the source code could take that common block of memory and
18	decide ahead of time, I'm going to divide it so no function
19	can ever step over the other guy's line. You know, the
20	example would be I divide a 20 kilobyte memory into ahead of
21	time so it is always 10 for one function, 10 for another
22	function. That would be a situation where 'can' doesn't work.
23	The source code itself set up that memory so that you can't
24	step over the line into the other space.
25	But if the source code allows flexibility in assigning
22 23	function. That would be a situation where 'can' doesn't w The source code itself set up that memory so that you can'

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portions of the memory to the interleaver and the 1 deinterleaver, and we intend to show that through our 2 infringement proofs, that would be a capability -- that would 3 be the capability of allocating one portion to the interleaver 4 at one time and allocating that same portion to the 5 6 deinterleaver at another time. It doesn't --THE COURT: I understand that. But I guess what I'm 7 trying to get you to address for me is your understanding of 8 the Delaware construction of memory can be used doesn't 9 involve or include the concept that over time it eventually 10 It doesn't have to be; it just can be. 11 must be. MR. McANDREWS: That's correct, Your Honor. 12 THE COURT: Okay. 13 MR. McANDREWS: So if the device would infringe as 14 sold as opposed to you'd have to observe it during the course 15 of its actual use by a particular customer. 16 17 THE COURT: Okay. That's what I wanted you to touch 18 on. What else here? 19 MR. McANDREWS: I think that's it for Plaintiff for 20 21 now, Your Honor. THE COURT: And you're not proposing anything 2.2 different for these claim terms that were not previously 23 construed in Delaware; you're just effectively saying it's all 24 subsumed by the one construction? 25

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1	MR. McANDREWS: That's correct, Your Honor. I mean,
2	possibly, you know, adjusting obviously for the context, but
3	'shared memory', 'sharing memory', 'configured to be shared',
4	'operable to be shared', they all are the same concept of a
5	portion of the memory can be used for the interleaver at one
6	time and the deinterleaver at another time.
7	THE COURT: All right. Thank you, counsel.
8	Let me hear from Defendants, please.
9	MR. MARAIS: Thank you, Your Honor. Nic Marais on
10	behalf of Defendants.
11	THE COURT: Please proceed.
12	MR. MARAIS: Thank you.
13	As an initial matter, I just want to point out
14	And if I can please switch to the elmo.
15	So what TQ Delta seems to be arguing in this case is the
16	notion that a shared memory here, or at least their
17	construction of a shared memory encapsulates all shared
18	memories. The one thing I just want to point out is that is
19	not how the Delaware court construed this term.
20	If we look down here, we can see that the Delaware court
21	indicated that the Plaintiff points to two different types of
22	shared memory, and those are the types that Mr. McAndrews
23	pointed to earlier, that are unlike the shared memory
24	described in the patents. And what it ultimately concluded
25	is, based on those two different types it said over here, What

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1	we're going to do is we're going to adopt this languagethe
2	common memory can be used by either one of those functions.
3	So while we are Your Honor's point that 'can be'
4	doesn't necessarily require, that does make us a lot more
5	comfortable with their position that they are not necessarily
6	requiring that a portion of the memory or at least that
7	there's ever a second allocation that actually shows a single
8	portion of the memory or a single block of memory being
9	allocated to two different portions, we still believe what
10	TQ Delta is trying to get at is they are reading out two
11	embodiments of a shared memory, and at least a shared
12	memory that a person of ordinary skill would understand a
13	shared memory to be.
14	Now, where we think the Delaware court erred, Your
15	Honor
16	Do you mind, can we please switch back here?
17	Is we think the Delaware court erred by importing a
18	limitation of the claims that is not in every single claim,
19	and that really just describes a particular use case of a
20	shared memory. And they are importing that limitation into
21	every single time you see the term 'shared memory'.
22	So what I have up here on the slide, Your Honor, is a
23	claim 9 of '882 Patent. And we can see it says 'shared
24	memory' a number of times. And then we have the '608 Patent,
25	claim 2, which is part of the same family, and here we see at

Shawn M. McRoberts, RMR, CRR Page 11 of 14 Federal Official Court Reporter the top it says 'a memory is operable to be shared'. So again, that's just the same term as 'shared memory', and the parties agree that that's -- those terms are being construed consistently.

But what that term ultimately does -- or what this claim 5 6 ultimately does is it goes on to explain how that sharing actually happens. And it says here, "The sharing comprises 7 using a first portion of the memory for the interleaver 8 function and simultaneously using a second portion of the 9 memory different than that for the first portion for the 10 deinterleaver function." And then, importantly, it goes on 11 and says, "and the first and second portions of the memory are 12 configurable such that one or more bytes of the memory can be 13 used by the interleaver function at one particular time, and 14 the same one or more bytes of the memory can be used by the 15 16 deinterleaver function at a second time."

17 And so it's our view is that everything that's underlined in red there, Your Honor, aligns with a second clause of 18 TQ Delta's construction, which is where a portion of the 19 memory can be used by either one of those functions. 20 And every time you see 'shared memory' in claims like the '882 21 Patent--it's also in a number of other patents--it does --2.2 that does not include this limitation. What we understand TQ 23 Delta to be trying to do is import this entire limitation into 24 that. 25

1	THE COURT: And is that to avoid some prior art?
2	What's the rationale behind it? Usually that's what's behind
3	it when the plaintiff tries to import a limitation, as opposed
4	to defendant who's trying to avoid infringement.
5	MR. MARAIS: That's exactly right, Your Honor.
6	And if we can switch back to the elmo.
7	So sideways is a little tricky here. If you look here
8	so starting from 'second' at the bottom of the page here, it
9	says, "Second, and Plaintiff notes that yet another type of
10	shared memory, known as ping-pang memory both involves
11	transmission in a single direction and uses a shared memory
12	exclusively for an interleaver or for a deinterleaver at any
13	one time."
14	Now, this ping-pang memory is a term that comes directly
15	out of one of our prior art references, Your Honor, and often
16	it's actually referred to as ping-pong memory, so we know it
17	comes out of that reference because it's one of the few
18	references that would refer to as ping pang instead. And what
19	the court ultimately did in the claim construction is it
20	effectively read out this prior art reference by narrowing the
21	claim language.
22	THE COURT: Okay. What else?
23	MR. MARAIS: So the only other thing I would add,
24	Your Honor, is that ultimately the
25	Well, let me switch back.

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1	Ultimately we agree that a shared memory is, you know, a
2	memory that would be used by two or more functions, but
3	ultimately it just has to have the ability to allocate that
4	memory amongst those different functions. It doesn't have to
5	do it. It doesn't ever have to have a second allocation of
6	that memory. It doesn't ever have to even if it does have
7	a second allocation of that memory, a single particular block
8	of that memory does not necessarily have to service as two
9	functions. You can have an allocation, as Mr. Hurt was
10	talking about, or I apologize as Mr. McAndrews talks
11	about the example where you have 16 bites and four bytes,
12	there could be an allocation that re-allocates to 12 bytes and
13	two bytes. A portion or a single block of that memory would
14	never have overlapped between those functions, but it wouldn't
15	changing the fact that it's still a shared memory.
16	I have nothing further, Your Honor.
17	THE COURT: Okay. Thank you.
18	All right. Let's go on to the next area of dispute
19	including 'wherein the generated message indicates how the
20	memory has been allocated between the first deinterleaving
21	function and the second deinterleaving function', as well as
22	'a message indicating how the shared memory is to be used by
23	the interleaver or the deinterleaver'.
24	I'll hear from Plaintiff, Mr. Davis.
25	MR. DAVIS: Thank you, Your Honor.

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