

# THPM 19.5

## TCP: A NEXT GENERATION FOR TV CONTROL PROCESSING

Ole Steinfatt, Philips Semiconductors, Hamburg, Germany  
Peter Klapproth and Hans Tichelaar,  
Philips Semiconductors, Eindhoven, The Netherlands

### ABSTRACT

*We present a new 32-bit RISC integrated TV Telecommunications and Control Processor (TCP)<sup>1</sup> with bit-mapped graphics and all the necessary interfaces for use in high-end TV sets. This allows TVs to implement complex user interfaces like WindowsCE<sup>®</sup>.*

### INTRODUCTION

TV control processing and user interfaces are becoming more and more complex. Starting from a few LEDs and a 4-bit microprocessor, via 8-bit microcontrollers to 16-bit controllers with character based graphics support, we now have reached a new generation based on 32-bit RISC microcontrollers. These state-of-the-art microcontrollers provide high-quality graphics and greater interactivity for applications like Internet TV, enhanced teletext or GUI. The TCP belongs to this new generation.

### FUNCTIONAL DESCRIPTION

The TCP is a highly integrated system IC combining a powerful RISC CPU with a co-processor for bit-mapped graphics output, memory controllers and various I/O peripherals. The main building blocks are:

#### CPU

The RISC core is an internal development. The key features are MIPSII and MIPS16 instruction sets (for code compactness), 8 kbyte instruction cache, 4 kbyte data cache, 5-stage pipeline designed for 81 MHz (used at 48 MHz in TCP), MMU (required for certain operating systems), Debug Support Unit (DSU), and a Multiply Accumulator (MAC) for DSP-like applications e.g. a software modem.

1. The IC is available commercially as SAA7430.

An architectural concept for video processing including the IC will be presented at the 1999 ICCE conference in paper # 222, "A Video Display Processing Platform for Future TV Concepts" by Peter de With et al.. Multi-window video processing on the IC will be presented at the 1999 ICCE conference in paper # 223, "Chip-set for Video Display of Multimedia Information" by Egbert Jaspers et al..

### GFX

TCP supports true and high color display modes, alpha channel for blending, programmable resolution (up to 1280 × 1000), IDTV sync-mode support and a hardware cursor overlay.

### SDRAM Controller

This supports a range of 16-64 Mbit devices and has a dedicated interface to GFX. It is also used as a high-performance communication channel to a companion chip for enhanced quality TV output.

### Modem interface

A software modem can be realized using the CPU's MAC engine via a line interface companion chip, as in hand-held PCs.

### Other features

The following interfaces have been implemented to fulfil the task of a TV controller: low resolution ADC, dual I<sup>2</sup>C-bus, dual UART, bidirectional remote control interface, general purpose I/O, interrupt controller, multiple timer and static memory interface (connecting e.g. FLASH memory, EPROM).

To ease software development, an Enhanced JTAG (EJTAG) debug port is provided as a communication channel between a development system host computer and the TCP. EJTAG is an industry standard backed by multiple MIPS processor and tool vendors. It gives the host computer total control over the TCP target system and allows real-time visibility of the processor instruction flow.

The modular TCP chip architecture is based on an in-house architecture framework called PRISC, which prescribes standards for on-chip communication. Key elements are specifications for a system bus (Peripheral Interconnect bus or "PI-Bus") and generic interfacing to Intellectual Property (IP) cores. PRISC is a foundation for platform-based system IC design. It enables the creation of common re-usable blocks that can be exchanged between projects for reducing development time, cost and risk. PRISC has been proven to be invaluable for multi-site projects like TCP.

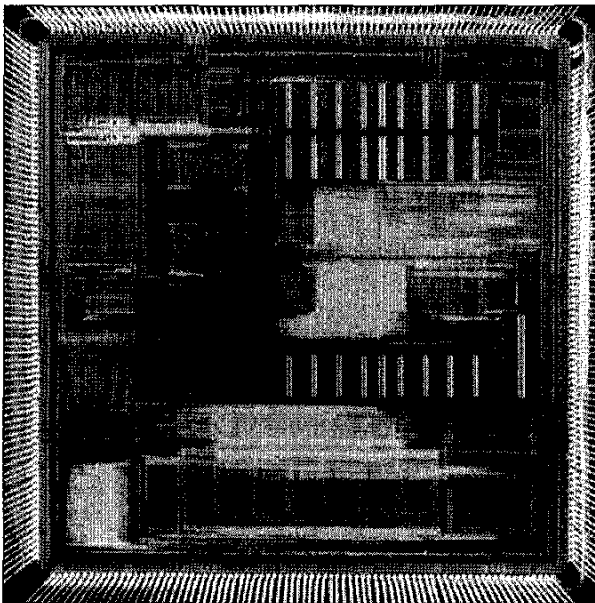
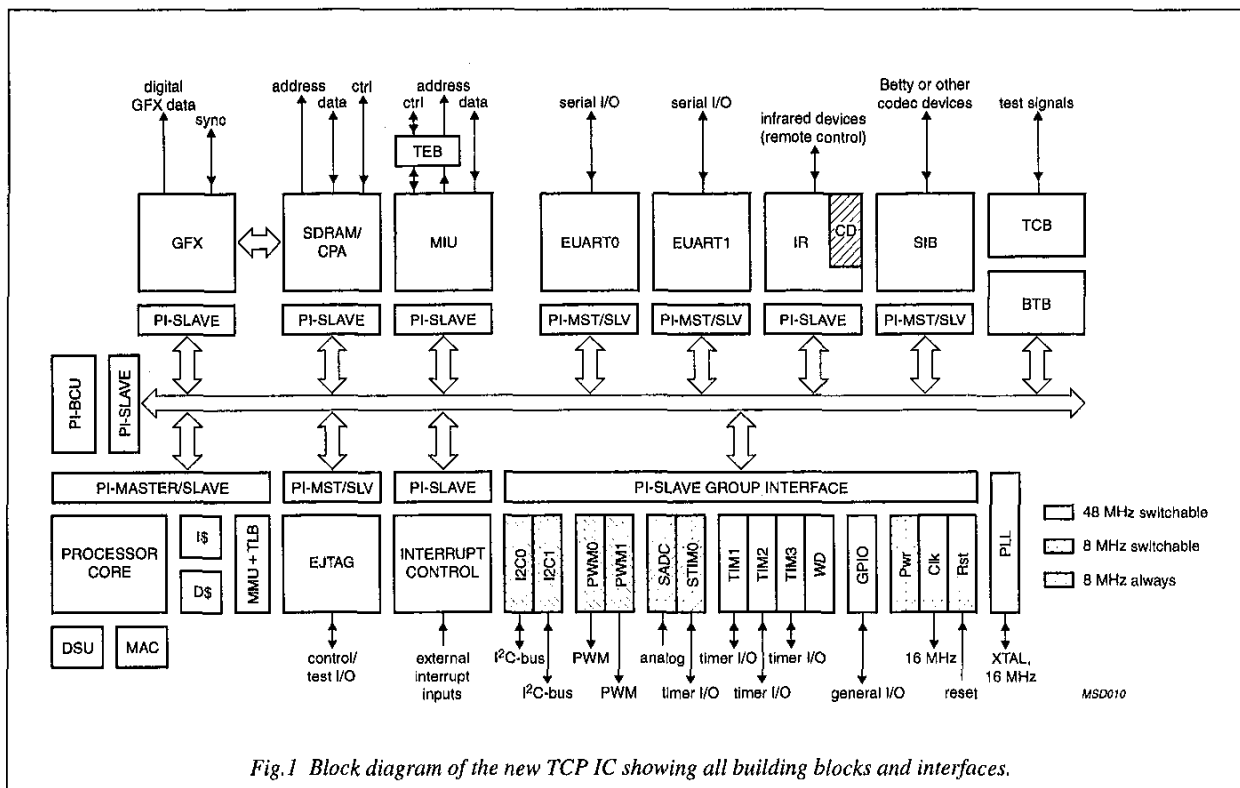


Fig.2 Photomicrograph of the new IC.

A full chip verification strategy including C-based test benches, cycle-based simulation and emulation guaranteed the proper operation of the silicon before tape-out. Evaluation of the silicon showed that all verified features worked as expected.

## CONCLUSION

The TCP represents a new generation of ICs for TV control. It is available as silicon with 80 mm<sup>2</sup> area in a 352-pin ball-grid array package (BGA352) and has 214 active I/Os. It is manufactured in a 0.35-micron CMOS process with five metal layers. The chip was designed for an internal clock frequency of 48 MHz. Measurements with the silicon have shown that the internal bus runs up to 66 MHz and the maximum speed of the GFX output is 96 MHz.

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