

AO 120 (Rev. 08/10)

TO: Mail Stop 8 Director of the U.S. Patent and Trademark Office P.O. Box 1450 Alexandria, VA 22313-1450	REPORT ON THE FILING OR DETERMINATION OF AN ACTION REGARDING A PATENT OR TRADEMARK

In Compliance with 35 U.S.C. § 290 and/or 15 U.S.C. § 1116 you are hereby advised that a court action has been filed in the U.S. District Court Eastern District of Texas - Marshall Division on the following

☐ Trademarks or ☒ Patents. (☐ the patent action involves 35 U.S.C. § 292.);

DOCKET NO. 2:21-cv-310	DATE FILED 8/13/2021	U.S. DISTRICT COURT Eastern District of Texas - Marshall Division
PLAINTIFF TQ Delta, LLC		DEFENDANT CommScope Holding Company, Inc., et al.
PATENT OR TRADEMARK NO.	DATE OF PATENT OR TRADEMARK	HOLDER OF PATENT OR TRADEMARK
1 See Attachment A		
2		
3		
4		
5		

In the above—entitled case, the following patent(s)/ trademark(s) have been included:

DATE INCLUDED	INCLUDED BY ☐ Amendment ☐ Answer ☐ Cross Bill ☐ Other Pleading
PATENT OR TRADEMARK NO.	DATE OF PATENT OR TRADEMARK
1	
2	
3	
4	
5	

In the above—entitled case, the following decision has been rendered or judgement issued:

DECISION/JUDGEMENT		
CLERK	(BY) DEPUTY CLERK	DATE

Copy 1—Upon initiation of action, mail this copy to Director Copy 3—Upon termination of action, mail this copy to Director
 Copy 2—Upon filing document adding patent(s), mail this copy to Director Copy 4—Case file copy

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NOTICE OF FILING OF PATENTS ATTACHMENT A

NOTICE OF FILING OF PATENTS		
PATENT NUMBER	DATE OF PATENT	HOLDER OF PATENT
U.S. Patent No. 7,453,881	November 18, 2008	TQ Delta, LLC
U.S. Patent No. 7,570,686	August 4, 2009	TQ Delta, LLC
U.S. Patent No. 7,844,882	November 30, 2010	TQ Delta, LLC
U.S. Patent No. 8,090,008	January 3, 2012	TQ Delta, LLC
U.S. Patent No. 8,276,048	September 25, 2012	TQ Delta, LLC
U.S. Patent No. 8,462,835	June 11, 2013	TQ Delta, LLC
U.S. Patent No. 8,468,411	June 18, 2013	TQ Delta, LLC
U.S. Patent No. 8,937,988	January 20, 2015	TQ Delta, LLC
U.S. Patent No. 9,094,348	July 28, 2015	TQ Delta, LLC
U.S. Patent No. 9,154,354	October 6, 2015	TQ Delta, LLC
U.S. Patent No. 9,485,055	November 1, 2016	TQ Delta, LLC
U.S. Patent No. 10,567,112	February 18, 2020	TQ Delta, LLC
U.S. Patent No. 10,833,809	November 10, 2020	TQ Delta, LLC

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PATENT ASSIGNMENT COVER SHEET

Electronic Version v1.1
Stylesheet Version v1.2

EPAS ID: PAT6478922

SUBMISSION TYPE:	NEW ASSIGNMENT	
NATURE OF CONVEYANCE:	AMENDED AND RESTATED INTELLECTUAL PROPERTY SECURITY AGREEMENT	
CONVEYING PARTY DATA		
Name		Execution Date
TQ DELTA LLC		12/31/2020
RECEIVING PARTY DATA		
Name:	ALTER DOMUS (US) LLC	
Street Address:	225 W. WASHINGTON ST., 9TH FLOOR	
City:	CHICAGO	
State/Country:	ILLINOIS	
Postal Code:	60606	
PROPERTY NUMBERS Total: 227		
Property Type	Number	
Patent Number:	5497398	
Patent Number:	5631610	
Patent Number:	5636246	
Patent Number:	5715280	
Patent Number:	5751716	
Patent Number:	5832030	
Patent Number:	6445730	
Patent Number:	6731695	
Patent Number:	6748016	
Patent Number:	6760373	
Patent Number:	6801570	
Patent Number:	6870888	
Patent Number:	6961369	
Patent Number:	7180938	
Patent Number:	7292627	
Patent Number:	7451379	
Patent Number:	7453881	
Patent Number:	7471721	
Patent Number:	7558329	
Patent Number:	7570686	

Property Type	Number
Patent Number:	7636389
Patent Number:	7656976
Patent Number:	7697598
Patent Number:	7769104
Patent Number:	7796705
Patent Number:	7809028
Patent Number:	7831890
Patent Number:	7835430
Patent Number:	7836381
Patent Number:	7844882
Patent Number:	7889784
Patent Number:	7925958
Patent Number:	7978706
Patent Number:	7978753
Patent Number:	7979778
Patent Number:	8073041
Patent Number:	8090008
Patent Number:	8102909
Patent Number:	8218610
Patent Number:	8238412
Patent Number:	8276048
Patent Number:	8335271
Patent Number:	8335956
Patent Number:	8355427
Patent Number:	8374226
Patent Number:	8391191
Patent Number:	8407546
Patent Number:	8422511
Patent Number:	8432956
Patent Number:	8437382
Patent Number:	8462835
Patent Number:	8468411
Patent Number:	8495473
Patent Number:	8516337
Patent Number:	8594162
Patent Number:	8595577
Patent Number:	8607126
Patent Number:	8611404

Property Type	Number
Patent Number:	8625660
Patent Number:	8634449
Patent Number:	8645784
Patent Number:	8649305
Patent Number:	8718158
Patent Number:	8743931
Patent Number:	8743932
Patent Number:	8750352
Patent Number:	8782498
Patent Number:	8792574
Patent Number:	8793553
Patent Number:	8831031
Patent Number:	8837610
Patent Number:	8913649
Patent Number:	8929423
Patent Number:	8929470
Patent Number:	8937988
Patent Number:	8984366
Patent Number:	9014193
Patent Number:	9014243
Patent Number:	9065886
Patent Number:	9069718
Patent Number:	9094268
Patent Number:	9094348
Patent Number:	9154354
Patent Number:	9191039
Patent Number:	9264533
Patent Number:	9276612
Patent Number:	9286251
Patent Number:	9300324
Patent Number:	9300601
Patent Number:	9319512
Patent Number:	9479637
Patent Number:	9485055
Patent Number:	9485128
Patent Number:	9521003
Patent Number:	9547608
Patent Number:	9621198

Property Type	Number
Patent Number:	9749235
Patent Number:	9755876
Patent Number:	9838531
Patent Number:	9893921
Patent Number:	9894014
Patent Number:	9898220
Patent Number:	9973624
Patent Number:	10044473
Patent Number:	10049003
Patent Number:	10187240
Patent Number:	10264119
Patent Number:	10341261
Patent Number:	10346243
Patent Number:	10409510
Patent Number:	10419059
Patent Number:	10484140
Patent Number:	10498495
Patent Number:	10567112
Patent Number:	10579291
Patent Number:	10623559
Patent Number:	10708104
Patent Number:	10805040
Patent Number:	10833809
Application Number:	09768275
Application Number:	09836295
Application Number:	09882046
Application Number:	10175815
Application Number:	10202688
Application Number:	10597482
Application Number:	10631745
Application Number:	10743946
Application Number:	10778083
Application Number:	10802867
Application Number:	10834193
Application Number:	11058289
Application Number:	11090183
Application Number:	11140246
Application Number:	11200002

Property Type	Number
Application Number:	11242024
Application Number:	11289516
Application Number:	11430251
Application Number:	11434249
Application Number:	11616630
Application Number:	11748806
Application Number:	11972340
Application Number:	12383056
Application Number:	12478577
Application Number:	12615077
Application Number:	12640838
Application Number:	12783733
Application Number:	12783737
Application Number:	12783744
Application Number:	12783755
Application Number:	12783788
Application Number:	12783796
Application Number:	12783801
Application Number:	12783825
Application Number:	12783839
Application Number:	13330943
Application Number:	13467392
Application Number:	14285911
Application Number:	14485937
Application Number:	14577769
Application Number:	14724345
Application Number:	14757630
Application Number:	14865966
Application Number:	14932599
Application Number:	15054499
Application Number:	15077506
Application Number:	15084788
Application Number:	15180274
Application Number:	15298817
Application Number:	15304920
Application Number:	15479866
Application Number:	16428232
Application Number:	16544003

Property Type	Number
Application Number:	16561835
Application Number:	16569144
Application Number:	16781802
Application Number:	17027196
Application Number:	60072447
Application Number:	60090891
Application Number:	60109876
Application Number:	60144562
Application Number:	60164134
Application Number:	60172343
Application Number:	60174865
Application Number:	60177944
Application Number:	60197727
Application Number:	60212233
Application Number:	60224308
Application Number:	60241468
Application Number:	60241664
Application Number:	60278936
Application Number:	60283467
Application Number:	60287968
Application Number:	60293034
Application Number:	60309631
Application Number:	60327440
Application Number:	60400550
Application Number:	60549804
Application Number:	60555982
Application Number:	60613594
Application Number:	60618269
Application Number:	60619618
Application Number:	60792236
Application Number:	60849650
Application Number:	60989542
Application Number:	61011267
Application Number:	61183845
Application Number:	61985168
PCT Number:	US0019247
PCT Number:	US0030958
PCT Number:	US0100418

Property Type	Number
PCT Number:	US0102341
PCT Number:	US0112555
PCT Number:	US0132503
PCT Number:	US0141015
PCT Number:	US0209411
PCT Number:	US0224326
PCT Number:	US0231649
PCT Number:	US0323965
PCT Number:	US0533922
PCT Number:	US0536015
PCT Number:	US9406713
PCT Number:	US9515115
PCT Number:	US9708209
PCT Number:	US9708222
PCT Number:	US9708549
PCT Number:	US9708756
PCT Number:	US9914467

CORRESPONDENCE DATA

Fax Number: (202)887-4288

Correspondence will be sent to the e-mail address first; if that is unsuccessful, it will be sent using a fax number, if provided; if that is unsuccessful, it will be sent via US Mail.

Phone: 2028874000

Email: dlee@akingump.com

Correspondent Name: DAVID C. LEE

Address Line 1: 2001 K STREET N.W.

Address Line 2: AKIN GUMP STRAUSS HAUER & FELD LLP

Address Line 4: WASHINGTON, D.C. 20006

ATTORNEY DOCKET NUMBER:	697820.0023
NAME OF SUBMITTER:	DAVID C. LEE
SIGNATURE:	/David C. Lee/
DATE SIGNED:	01/04/2021
	This document serves as an Oath/Declaration (37 CFR 1.63).

Total Attachments: 25

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EXECUTION VERSION

AMENDED AND RESTATED INTELLECTUAL PROPERTY SECURITY AGREEMENT

This AMENDED AND RESTATED INTELLECTUAL PROPERTY SECURITY AGREEMENT (as amended, restated, amended and restated, supplemented or otherwise modified from time to time, the “**IP Security Agreement**”), dated as of December 31, 2020, is made by each undersigned grantor (each, a “**Grantor**”, and, collectively, the “**Grantors**”) in favor of ALTER DOMUS (US) LLC, a Delaware limited liability company, as collateral agent for its own benefit and the benefit of the Lenders (as defined in the Credit Agreement defined below) (in such capacity, together with its successor and assigns in such capacity, the “**Collateral Agent**”). Capitalized terms used herein and not otherwise defined herein shall have the meanings assigned to such terms in the Credit Agreement or the Security Agreement (as defined below), as applicable.

WHEREAS, the Borrower, ALTER DOMUS (US) LLC, as Administrative Agent (as defined therein), the Collateral Agent and the Lenders from time party thereto, are each party to that certain Amended and Restated Credit Agreement, dated as of December 31, 2020 (as amended, restated, amended and restated, supplemented or otherwise modified from time to time, the “**Credit Agreement**”), pursuant to which the Lenders have agreed, among other things, to continue the existing term loan and extend further credit to the Borrower in the form of delayed draw term loans upon the terms and subject to the conditions specified therein;

WHEREAS, in connection with the Credit Agreement, each Grantor has entered into the Amended and Restated Security Agreement, dated as of December 31, 2020 (as amended, restated, amended and restated, supplemented or otherwise modified from time to time, the “**Security Agreement**”) in order to induce the Lenders to make and continue to make, as applicable, Loans; and

WHEREAS, under the terms of the Security Agreement, each Grantor has granted to the Collateral Agent, for the ratable benefit of the Credit Parties, a security interest in, among other property, certain intellectual property of such Grantor, and has agreed as a condition thereof to execute this IP Security Agreement for recording with the United States Patent and Trademark Office and the United States Copyright Office, as the case may be.

NOW, THEREFORE, for good and valuable consideration, the receipt and sufficiency of which are hereby acknowledged, each Grantor agrees as follows:

(a) **Grant of Security Interest.** As security for the prompt and complete payment or performance, as the case may be, in full of the Secured Obligations, each Grantor hereby grants to the Collateral Agent for itself and the ratable benefit of the Credit Parties, a security interest in all of its right, title and interest in and to all of the following personal property, whether now owned by or owing to or hereafter acquired by or arising in favor of such Grantor (collectively, the “**IP Collateral**”):

(i) all Trademark registrations and applications for Trademark registration in the United States Patent and Trademark Office listed on Schedule I hereto;

(ii) all issued Patents and pending Patent applications in the United States Patent and Trademark Office listed on Schedule II hereto;

(iii) all Copyright registrations and pending applications for Copyright registration in the United States Copyright Office listed on Schedule III; and

(iv) all Proceeds and products of any and all of the foregoing and all supporting obligations, collateral security and guarantees given by any Person with respect to any of the foregoing;

provided, however, that notwithstanding any of the other provisions herein (and notwithstanding any recording of the Collateral Agent's Lien made in the United States Patent and Trademark Office, United States Copyright Office, or other registry office in any other jurisdiction), this Short-Form IP Security Agreement shall not constitute a grant of a security interest in any Trademark applications filed in the United States Patent and Trademark Office on the basis of such Grantor's "intent-to-use" such trademark, unless and until acceptable evidence of use of the Trademark has been filed with and accepted by the United States Patent and Trademark Office pursuant to Section 1(c) or Section 1(d) of the Lanham Act (15 U.S.C. 1051, et seq.), to the extent that granting a lien in such Trademark application prior to such filing would adversely affect the enforceability or validity of such Trademark application.

(b) Security for Secured Obligations. The grant of a security interest in the IP Collateral by each Grantor under this IP Security Agreement secures the payment of all Secured Obligations of such Grantor now or hereafter existing under or in respect of the Loan Documents, whether direct or indirect, absolute or contingent, and whether for principal, reimbursement obligations, interest, premiums, penalties, fees, indemnifications, contract causes of action, costs, expenses or otherwise, subject to the terms and provisions thereof.

(c) Recordation. This IP Security Agreement has been executed and delivered by each Grantor for the purpose of recording the grant of security interest herein with the United States Patent and Trademark Office and the United States Copyright Office, as the case may be. Each Grantor authorizes and requests that the Register of Copyrights, the Commissioner for Patents and the Commissioner for Trademarks and any other applicable government officer record this IP Security Agreement.

(d) Execution in Counterparts. This IP Security Agreement may be executed in any number of counterparts, each of which when so executed shall be deemed to be an original and all of which taken together shall constitute one and the same agreement.

(e) Grants, Rights and Remedies. This IP Security Agreement has been entered into in conjunction with the provisions of the Security Agreement. The Grantor does hereby acknowledge and confirm that the grant of the security interest hereunder to, and the rights and remedies of, the Collateral Agent with respect to the Collateral are more fully set forth in the Security Agreement, the terms and provisions of which are incorporated herein by reference as if fully set forth herein. In the event of any conflict between the terms of this IP Security Agreement and the terms of the Security Agreement, the terms of the Security Agreement shall govern.

(f) Governing Law. THIS IP SECURITY AGREEMENT SHALL BE GOVERNED BY, AND CONSTRUED IN ACCORDANCE WITH, THE LAW OF THE STATE OF NEW YORK.

(g) General. Sections 10.04, 10.14(b) and 10.15 of the Credit Agreement are hereby incorporated by reference into this IP Security Agreement *mutatis mutandis* and shall apply hereto.

(h) Severability. In case any one or more of the provisions contained in this IP Security Agreement should be held invalid, illegal or unenforceable in any respect, the validity, legality and enforceability of the remaining provisions contained herein and in the Security Agreement shall not in any way be affected or impaired thereby (it being understood that the invalidity of a particular provision in a particular jurisdiction shall not in and of itself affect the validity of such provision in any other jurisdiction). The parties hereto shall endeavor in good-faith negotiations to replace the invalid, illegal or unenforceable provisions with valid provisions the economic effect of which comes as close as possible to that of the invalid, illegal or unenforceable provisions.

(i) Amendment and Restatement. This IP Security Agreement is an amendment and restatement but not a novation of that certain Intellectual Property Security Agreement, dated as of October 5, 2018, in favor of the Collateral Agent (as amended, modified or supplemented prior to the date hereof, the “**Original IP Security Agreement**”). All Liens and security interests securing payment of the Secured Obligations under the Original IP Security Agreement are hereby collectively, renewed, extended, ratified and brought forward as security for the payment and performance of the Secured Obligations. Each Grantor hereby (i) reaffirms each Lien, pledge and security interest granted to the Collateral Agent under or in connection with the Original IP Security Agreement, (ii) agrees that after giving effect to this IP Security Agreement such Liens, pledges and security interests shall continue in full force and effect, and (iii) agrees that such Liens, pledges and security interests continue to secure the full and prompt payment and performance of all of the Secured Obligations.

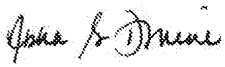
[Remainder of Page Intentionally Blank]

IN WITNESS WHEREOF, each Grantor has caused this IP Security Agreement to be duly executed and delivered by its officer thereunto duly authorized as of the date first above written.

TQ DELTA LLC, as Grantor

By: TQCAP GP, LLC, its manager

By: TECHQUITY CAPITAL MANAGEMENT,
LLC, its sole member

By: 
Name: Abha Divine
Title: Managing Director

[Signature Page to A&R IP Security Agreement]

ACCEPTED AND AGREED
as of the date first above written.

ALTER DOMUS (US) LLC,
as Collateral Agent

By: J. K.
Name: Jon Kirschmeier
Title: Associate Counsel

[Signature Page to A&R IP Security Agreement]

Schedule I

Trademarks

UNITED STATES TRADEMARKS:

Registrations / Applications:

OWNER	REGISTRATION/ APPLICATION NUMBER	TRADEMARK
TQ Delta LLC	5110447	TQ DELTA

Schedule II

Patents

(see attached)

TQ DELTA, LLC
Privileged and Confidential / Attorney Client Communication

Reference #	Title	Country ID	Status	Serial #	Filed Date	Publication #	Patent #	Issue Date	Expiration Date
6936-2-CON-2	Systems and Methods for Establishing a Diagnostic Transmission Mode and Communicating Over the Same	US	ISSUED	10/619,691	7/16/03	US 2004-0202237 A1	7,570,686	8/4/09	10/1/22
6936-2-CON-2-1	Multicarrier Modulation Messaging for Frequency Domain Received Idle Channel Noise Information	US	ISSUED	12/477,742	6/3/09	US 2009-0238254 A1	7,835,430	11/16/10	1/8/21
6936-2-CON-2-1-1	Multicarrier Modulation Messaging for Power Level Per Subchannel Information	US	EXPIRED	12/779,660	5/13/10	US 2010-0226418 A1	8,238,412	8/7/12	4/7/20
6936-2-CON-2-1-2	Multicarrier Modulation Messaging for SNR Per Subchannel During Showtime Information	US	ISSUED	12/779,708	5/13/10	US 2010-0220775 A1	7,889,784	2/15/11	1/8/21
6936-2-CON-2-1-3	Systems and Methods for Establishing a Diagnostic Transmission Mode and Communicating Over the Same	US	ISSUED	13/004,254	1/11/11	US 2011-0103443 A1	8,634,449	1/21/14	7/4/21
6936-2-CON-2-1-4	Multicarrier Modulation Messaging for Power Level Per Subchannel Information	US	ISSUED	13/476,310	5/21/12	US 2012-0230476 A1	8,432,596	4/30/13	1/8/21
6936-2-CON-2-1-5	Systems and Methods for a Transceiver to Transmit or Receive Test Information Over a Communication Channel Using Multicarrier Modulation	US	ISSUED	13/873,892	4/30/13	US 2013-0243049 A1	8,743,931	6/3/14	1/8/21
6936-2-CON-2-1-6	Systems and Methods for Establishing a Diagnostic Transmission Mode and Communicating Over the Same	US	ISSUED	14/153,282	1/13/14	US 2014-0126616 A1	8,929,423	1/6/15	1/8/21
8303-2-CON-2-1-7	Systems and Methods for Establishing a Diagnostic Transmission Mode and Communicating Over the Same	US	ISSUED	14/282,254	5/20/14	US 2014-0254645 A1	9,319,512	4/19/16	1/8/21
8303-2-CON-2-1-8	Systems and Methods for Establishing a Diagnostic Transmission Mode and Communicating Over the Same	US	ABANDONED	14/577,769	12/19/14	US 2015-0103936 A1			2/16/16
8303-2-CON-2-1-9	SYSTEMS AND METHODS FOR ESTABLISHING A DIAGNOSTIC TRANSMISSION MODE AND COMMUNICATING OVER THE SAME	US	ISSUED	14/818,731	8/5/15	US 2015-0341488 A1	9,264,533	2/16/16	1/8/21
8303-2-CON-2-1-10	SYSTEMS AND METHODS FOR ESTABLISHING A DIAGNOSTIC TRANSMISSION MODE AND COMMUNICATING OVER THE SAME	US	ISSUED	14/991,431	1/8/16	US 2016-0127537 A1	9,479,637	10/25/16	1/8/21
6936-2-CON-2-1-11	SYSTEMS AND METHODS FOR ESTABLISHING A DIAGNOSTIC TRANSMISSION MODE AND COMMUNICATING OVER THE SAME	US	ISSUED	15/016,432	2/5/16	US 2016-0165042 A1	9,973,624	5/15/18	1/8/21
6936-2-CON-2-1-12	SYSTEMS AND METHODS FOR ESTABLISHING A DIAGNOSTIC TRANSMISSION MODE AND COMMUNICATING OVER THE SAME	US	ISSUED	15/098,932	4/14/16	US 2016-0227026 A1	10,264,119	4/16/19	1/8/21
6936-2-CON-2-1-13	SYSTEMS AND METHODS FOR ESTABLISHING A DIAGNOSTIC TRANSMISSION MODE AND COMMUNICATING OVER THE SAME	US	ISSUED	15/295,602	10/17/16	US 2017-0034343 A1	9,838,531	12/5/17	1/8/21
6936-2-CON-2-1-14	SYSTEMS AND METHODS FOR ESTABLISHING A DIAGNOSTIC TRANSMISSION MODE AND COMMUNICATING OVER THE SAME	US	ISSUED	15/958,878	4/20/18	US 2018-0249001 A1	10,623,559	4/14/20	1/8/21
6936-2-PAU-4-DIV	Diagnostic Methods and Systems for Multicarrier Modems	AU	ISSUED	2008203520	1/8/01	AU 2008203520	2008203520	11/5/09	1/8/21
6936-2-PAU-4-DIV-2	SYSTEMS AND METHODS FOR ESTABLISHING A DIAGNOSTIC TRANSMISSION MODE AND COMMUNICATING OVER THE SAME	AU	ABANDONED	2009222537	1/8/01	AU 2009222537	2009222537	12/22/11	1/4/17
6936-2-PAU-4-DIV-3	SYSTEMS AND METHODS FOR ESTABLISHING A DIAGNOSTIC TRANSMISSION MODE AND COMMUNICATING OVER THE SAME	AU	ABANDONED	2011247879	1/8/01		2011247879	9/18/14	1/4/17
6936-2-PAU-4-DIV-4	SYSTEMS AND METHODS FOR ESTABLISHING A DIAGNOSTIC TRANSMISSION MODE AND COMMUNICATING OVER THE SAME	AU	ABANDONED	2014208320	1/8/01		2014208320	3/12/15	1/4/17
8303-2-PAU-4-DIV-5	DIAGNOSTIC METHODS AND SYSTEMS FOR MULTICARRIER MODEMS	AU	ABANDONED	2015200087	1/8/01				2/28/17
8303-2-PAU-4-DIV-6	DIAGNOSTIC METHODS AND SYSTEMS FOR MULTICARRIER MODEMS	AU	ABANDONED	2017201226	1/8/01		2017201226	9/7/17	12/6/19
8303-2-PAU-4-DIV-7	DIAGNOSTIC METHODS AND SYSTEMS FOR MULTICARRIER MODEMS	AU	ABANDONED	2017210489	1/8/01				12/6/19
6936-2-PCA	Diagnostic Methods and Systems for Multicarrier Modems	CA	ISSUED	2,394,491	1/8/01	CA 2394491	2,394,491	3/29/11	1/8/21
6936-2-PCA-DIV	Diagnostic Methods and Systems for Multicarrier Modems	CA	ABANDONED	2,726,826	1/8/01	CA 2726826	2,726,826	11/20/12	12/23/16
6936-2-PCA-DIV-2	Diagnostic Methods and Systems for Multicarrier Modems	CA	EXPIRED	2,788,662	1/8/01		2,788,662	1/3/17	1/8/20
6936-2-PCA-DIV-3	Diagnostic Methods and Systems for Multicarrier Modems	CA	ISSUED	2,948,960	1/8/01		2,948,960	6/23/20	1/8/21
6936-2-PCT	SYSTEMS AND METHODS FOR ESTABLISHING A DIAGNOSTIC TRANSMISSION MODE AND COMMUNICATING OVER THE SAME	WO	NAT PHASE	PCT/US01/00418	1/8/01	WO 2001/52516			

6936-2-PEP-5	SYSTEMS AND METHODS FOR ESTABLISHING A DIAGNOSTIC TRANSMISSION MODE AND COMMUNICATING OVER THE SAME	EP	ISSUED	06022008.4	1/8/01	1755253	1755253	7/13/11	1/8/21
6936-2-PEP-5-BE	SYSTEMS AND METHODS FOR ESTABLISHING A DIAGNOSTIC TRANSMISSION MODE AND COMMUNICATING OVER THE SAME	BE	ISSUED	06022008.4	1/8/01	N/A	1755253	7/13/11	1/8/21
6936-2-PEP-5-CH	SYSTEMS AND METHODS FOR ESTABLISHING A DIAGNOSTIC TRANSMISSION MODE AND COMMUNICATING OVER THE SAME	CH	ISSUED	06022008.4	1/8/01	N/A	1755253	7/13/11	1/8/21
6936-2-PEP-5-DE	SYSTEMS AND METHODS FOR ESTABLISHING A DIAGNOSTIC TRANSMISSION MODE AND COMMUNICATING OVER THE SAME	DE	ISSUED	06022008.4	1/8/01	N/A	1755253	7/13/11	1/8/21
6936-2-PEP-5-ES	SYSTEMS AND METHODS FOR ESTABLISHING A DIAGNOSTIC TRANSMISSION MODE AND COMMUNICATING OVER THE SAME	ES	ISSUED	06022008.4	1/8/01	N/A	1755253	7/13/11	1/8/21
6936-2-PEP-5-FR	SYSTEMS AND METHODS FOR ESTABLISHING A DIAGNOSTIC TRANSMISSION MODE AND COMMUNICATING OVER THE SAME	FR	ISSUED	06022008.4	1/8/01	N/A	1755253	7/13/11	1/8/21
6936-2-PEP-5-GB	SYSTEMS AND METHODS FOR ESTABLISHING A DIAGNOSTIC TRANSMISSION MODE AND COMMUNICATING OVER THE SAME	GB	ISSUED	06022008.4	1/8/01	N/A	1755253	7/13/11	1/8/21
6936-2-PEP-5-GR	SYSTEMS AND METHODS FOR ESTABLISHING A DIAGNOSTIC TRANSMISSION MODE AND COMMUNICATING OVER THE SAME	GR	ABANDONED	06022008.4	1/8/01	N/A	1755253	7/13/11	12/6/19
6936-2-PEP-5-HK	SYSTEMS AND METHODS FOR ESTABLISHING A DIAGNOSTIC TRANSMISSION MODE AND COMMUNICATING OVER THE SAME	HK	ABANDONED	07108499.2	1/8/01	HK 1100379			8/4/11
6936-2-PEP-5-IE	SYSTEMS AND METHODS FOR ESTABLISHING A DIAGNOSTIC TRANSMISSION MODE AND COMMUNICATING OVER THE SAME	IE	ISSUED	06022008.4	1/8/01	N/A	1755253	7/13/11	1/8/21
6936-2-PEP-5-IT	SYSTEMS AND METHODS FOR ESTABLISHING A DIAGNOSTIC TRANSMISSION MODE AND COMMUNICATING OVER THE SAME	IT	ISSUED	06022008.4	1/8/01	N/A	1755253	7/13/11	1/8/21
6936-2-PEP-5-NL	SYSTEMS AND METHODS FOR ESTABLISHING A DIAGNOSTIC TRANSMISSION MODE AND COMMUNICATING OVER THE SAME	NL	ISSUED	06022008.4	1/8/01	N/A	1755253	7/13/11	1/8/21
6936-2-PEP-5-DIV-1	SYSTEMS AND METHODS FOR ESTABLISHING A DIAGNOSTIC TRANSMISSION MODE AND COMMUNICATING OVER THE SAME	EP	ISSUED	10011985.8	1/8/01	2276182	2276182	2/26/20	1/8/21
6936-2-PEP-5-DIV-1-DE	SYSTEMS AND METHODS FOR ESTABLISHING A DIAGNOSTIC TRANSMISSION MODE AND COMMUNICATING OVER THE SAME	DE	ISSUED	10011985.8	1/8/01	2276182	60151242.1	2/26/20	1/8/21
6936-2-PEP-5-DIV-1-FR	SYSTEMS AND METHODS FOR ESTABLISHING A DIAGNOSTIC TRANSMISSION MODE AND COMMUNICATING OVER THE SAME	FR	ISSUED	10011985.8	1/8/01		2276182	2/26/20	1/8/21
6936-2-PEP-5-DIV-1-GB	SYSTEMS AND METHODS FOR ESTABLISHING A DIAGNOSTIC TRANSMISSION MODE AND COMMUNICATING OVER THE SAME	GB	ISSUED	10011985.8	1/8/01		2276182	2/26/20	1/8/21
6936-2-PEP-5-DIV-1-HK	SYSTEMS AND METHODS FOR ESTABLISHING A DIAGNOSTIC TRANSMISSION MODE AND COMMUNICATING OVER THE SAME	HK	ABANDONED	11101591.8	1/8/01	HK 1147612			12/5/19
6936-2-PEP-5-DIV-2	SYSTEMS AND METHODS FOR ESTABLISHING A DIAGNOSTIC TRANSMISSION MODE AND COMMUNICATING OVER THE SAME	EP	ABANDONED	10011983.3	1/8/01	2293459			12/12/19
6936-2-PEP-5-DIV-2-HK	SYSTEMS AND METHODS FOR ESTABLISHING A DIAGNOSTIC TRANSMISSION MODE AND COMMUNICATING OVER THE SAME	HK	ABANDONED	11103980.3	1/8/01	HK 1149982			12/12/19
6936-2-PEP-5-DIV-3	SYSTEMS AND METHODS FOR ESTABLISHING A DIAGNOSTIC TRANSMISSION MODE AND COMMUNICATING OVER THE SAME	EP	ISSUED	10011984.1	1/8/01	2317684	2317684	2/26/20	1/8/21
6936-2-PEP-5-DIV-3-DE	SYSTEMS AND METHODS FOR ESTABLISHING A DIAGNOSTIC TRANSMISSION MODE AND COMMUNICATING OVER THE SAME	DE	ISSUED	10011984.1	1/8/01	2317684	60151241.3	2/26/20	1/8/21
6936-2-PEP-5-DIV-3-FR	SYSTEMS AND METHODS FOR ESTABLISHING A DIAGNOSTIC TRANSMISSION MODE AND COMMUNICATING OVER THE SAME	FR	ISSUED	10011984.1	1/8/01		2317684	2/26/20	1/8/21
6936-2-PEP-5-DIV-3-GB	SYSTEMS AND METHODS FOR ESTABLISHING A DIAGNOSTIC TRANSMISSION MODE AND COMMUNICATING OVER THE SAME	GB	ISSUED	10011984.1	1/8/01		2317684	2/26/20	1/8/21
6936-2-PEP-5-DIV-3-HK	SYSTEMS AND METHODS FOR ESTABLISHING A DIAGNOSTIC TRANSMISSION MODE AND COMMUNICATING OVER THE SAME	HK	ABANDONED	11106469.6	1/8/01	1152597			11/11/19

6936-2-PEP-5-DIV-3-NL	SYSTEMS AND METHODS FOR ESTABLISHING A DIAGNOSTIC TRANSMISSION MODE AND COMMUNICATING OVER THE SAME	NL	ISSUED	10011984.1	1/8/01		2317684	2/26/20	1/8/21
6936-2-PEP-5-DIV-4	SYSTEMS AND METHODS FOR ESTABLISHING A DIAGNOSTIC TRANSMISSION MODE AND COMMUNICATING OVER THE SAME	EP	ISSUED	10011982.5	1/8/01	2270996	2270996	3/7/18	1/8/21
6936-2-PEP-5-DIV-4-DE	SYSTEMS AND METHODS FOR ESTABLISHING A DIAGNOSTIC TRANSMISSION MODE AND COMMUNICATING OVER THE SAME	DE	ISSUED	10011982.5	1/8/01		2270996	3/7/18	1/8/21
6936-2-PEP-5-DIV-4-FR	SYSTEMS AND METHODS FOR ESTABLISHING A DIAGNOSTIC TRANSMISSION MODE AND COMMUNICATING OVER THE SAME	FR	ISSUED	10011982.5	1/8/01		2270996	3/7/18	1/8/21
6936-2-PEP-5-DIV-4-GB	SYSTEMS AND METHODS FOR ESTABLISHING A DIAGNOSTIC TRANSMISSION MODE AND COMMUNICATING OVER THE SAME	GB	ISSUED	10011982.5	1/8/01		2270996	3/7/18	1/8/21
6936-2-PEP-5-DIV-4-HK	SYSTEMS AND METHODS FOR ESTABLISHING A DIAGNOSTIC TRANSMISSION MODE AND COMMUNICATING OVER THE SAME	HK	ISSUED	11101590.0	1/8/01	HK 1147611	HK 1147611	9/21/18	1/8/21
6936-2-PEP-5-DIV-5	SYSTEMS AND METHODS FOR ESTABLISHING A DIAGNOSTIC TRANSMISSION MODE AND COMMUNICATING OVER THE SAME	EP	ABANDONED	18159847.5	1/8/01	3349386			12/12/19
6936-2-PEP-5-DIV-5-HK	SYSTEMS AND METHODS FOR ESTABLISHING A DIAGNOSTIC TRANSMISSION MODE AND COMMUNICATING OVER THE SAME	HK	ABANDONED	18113502.4	1/8/01	1254420			1/14/20
6936-2-PIP	SYSTEMS AND METHODS FOR ESTABLISHING A DIAGNOSTIC TRANSMISSION MODE AND COMMUNICATING OVER THE SAME	JP	ABANDONED	2001-552611	1/8/01	JP 2003/520504			7/13/11
6936-2-PIP-DIV	SYSTEMS AND METHODS FOR ESTABLISHING A DIAGNOSTIC TRANSMISSION MODE AND COMMUNICATING OVER THE SAME	JP	ISSUED	2008-191051	1/8/01	2009-027721	4722972	4/15/11	1/8/21
6936-2-PIP-DIV-2	SYSTEMS AND METHODS FOR ESTABLISHING A DIAGNOSTIC TRANSMISSION MODE AND COMMUNICATING OVER THE SAME	JP	ABANDONED	2011-012155	1/8/01	2011-151808			6/21/13
6936-2-PROV-1	MULTICARRIER MODULATION SYSTEM WITH REMOTE DIAGNOSTIC TRANSMISSION MODE	US	EXPIRED	60/174,865	1/7/00	N/A			1/7/01
6936-2-PROV-2	CHARACTERIZATION OF TRANSMISSION LINES USING BROADBAND SIGNALS IN A MULTI-CARRIER DSL SYSTEM	US	EXPIRED	60/224,308	8/10/00	N/A			8/10/01
6936-16	SYSTEMS AND METHODS FOR MULTI-PAIR ATM OVER DSL	US	ISSUED	10/264,258	10/4/02	US 2003-0091053 A1	7,453,881	11/18/08	7/24/25
6936-16-CDN	SYSTEMS AND METHODS FOR MULTI-PAIR OVER DSL	US	ISSUED	12/247,741	10/8/08	US 2009-0028158 A1	7,809,028	10/5/10	10/4/22
6936-16-CDN-2	Combining Multiple DSL Transceivers for a High Data Rate Connection	US	ISSUED	12/769,277	4/28/10	US 2010-0208737 A1	7,978,706	7/12/11	10/4/22
6936-16-CDN-3	Systems and Methods for Multi-Pair ATM Over DSL	US	ISSUED	12/783,777	5/20/10	US 2010-0290471 A1	8,422,511	4/16/13	10/4/22
6936-16-CDN-4	Systems and Methods for Multi-Pair ATM Over DSL	US	ISSUED	13/863,038	4/15/13	US 2013-0223453	8,831,031	9/9/14	10/4/22
6936-16-CDN-5	BONDING DEVICE AND METHOD	US	ISSUED	14/465,502	8/21/14	US 2014-0362863 A1	9,014,193	4/21/15	10/4/22
6936-16-CDN-6	BONDING DEVICE AND METHOD	US	ISSUED	14/682,435	4/9/15	US 2015-0215239 A1	9,300,601	3/29/16	10/4/22
6936-16-CDN-7	BONDING DEVICE AND METHOD	US	ISSUED	15/057,741	3/1/16	US 2016-0182406 A1	9,894,014	2/13/18	10/4/22
6936-16-CDN-8	BONDING DEVICE AND METHOD	US	ISSUED	15/882,619	1/29/18	US 2018-0152395 A1	10,341,261	7/2/19	10/4/22
6936-16-PCA	SYSTEMS AND METHODS FOR MULTI-PAIR ATM OVER DSL	CA	ISSUED	2,461,320	10/4/02	CA 2461320	2,461,320	10/25/11	10/4/22
6936-16-PCT	SYSTEMS AND METHODS FOR MULTI-PAIR ATM OVER DSL	WO	NAT PHASE	PCT/US02/31649	10/4/02	WO 2003/032555			
6936-16-PEP	SYSTEMS AND METHODS FOR MULTI-PAIR ATM OVER DSL	EP	ISSUED	02778433.9	10/4/02	1433277	1433277	7/25/12	10/4/22
6936-16-PEPBE	SYSTEMS AND METHODS FOR MULTI-PAIR ATM OVER DSL	BE	ISSUED	02778433.9	10/4/02		1433277	7/25/12	10/4/22
6936-16-PEPDE	SYSTEMS AND METHODS FOR MULTI-PAIR ATM OVER DSL	DE	ISSUED	02778433.9	10/4/02		1433277	7/25/12	10/4/22
6936-16-PEPFR	SYSTEMS AND METHODS FOR MULTI-PAIR ATM OVER DSL	FR	ISSUED	02778433.9	10/4/02		1433277	7/25/12	10/4/22
6936-16-PEPGB	SYSTEMS AND METHODS FOR MULTI-PAIR ATM OVER DSL	GB	ISSUED	02778433.9	10/4/02		1433277	7/25/12	10/4/22
6936-16-PEP-DIV	SYSTEMS AND METHODS FOR MULTI-PAIR ATM OVER DSL	EP	ISSUED	12002728.9	10/4/02	2506508	2506508	5/2/18	10/4/22
6936-16-PEP-DIV-DE	SYSTEMS AND METHODS FOR MULTI-PAIR ATM OVER DSL	DE	ISSUED	12002728.9	10/4/02		2506508	5/2/18	10/4/22
6936-16-PEP-DIV-FR	SYSTEMS AND METHODS FOR MULTI-PAIR ATM OVER DSL	FR	ISSUED	12002728.9	10/4/02		2506508	5/2/18	10/4/22
6936-16-PEP-DIV-GB	SYSTEMS AND METHODS FOR MULTI-PAIR ATM OVER DSL	GB	ISSUED	12002728.9	10/4/02		2506508	5/2/18	10/4/22
6936-16-PEP-DIV-2	SYSTEMS AND METHODS FOR MULTI-PAIR ATM OVER DSL	EP	ISSUED	18170134.3	10/4/02	3386128	3386128	7/24/19	10/4/22
6936-16-PEP-DIV-2-DE	SYSTEMS AND METHODS FOR MULTI-PAIR ATM OVER DSL	DE	ISSUED	18170134.3	10/4/02	3386128	DE60249960.7	7/24/19	10/4/22
6936-16-PEP-DIV-2-FR	SYSTEMS AND METHODS FOR MULTI-PAIR ATM OVER DSL	FR	ISSUED	18170134.3	10/4/02		3386128	7/24/19	10/4/22
6936-16-PEP-DIV-2-GB	SYSTEMS AND METHODS FOR MULTI-PAIR ATM OVER DSL	GB	ISSUED	18170134.3	10/4/02		3386128	7/24/19	10/4/22

6936-16-PEP-DIV-2-NL	SYSTEMS AND METHODS FOR MULTI-PAIR ATM OVER DSL	NL	ISSUED	18170134.3	10/4/02		3386128	7/24/19	10/4/22
6936-16-PROV	MULTI-PAIR ATM OVER DSL	US	EXPIRED	60/327,440	10/5/01	N/A			10/5/02
6936-54	RESOURCE SHARING IN A TELECOMMUNICATIONS ENVIRONMENT	US	ISSUED	11/246,163	10/11/05	US 2006-0088054 A1	7,831,890	11/9/10	11/7/28
6936-54-CDN	RESOURCE SHARING IN A TELECOMMUNICATIONS ENVIRONMENT	US	ISSUED	12/761,586	4/16/10	US 2010-0228924 A1	7,844,882	11/30/10	10/11/25
6936-54-CDN-2	Computer Readable Medium with Instructions for Resource Sharing in a Telecommunications Environment	US	ISSUED	12/853,020	8/9/10	US 2010-0306628 A1	7,836,381	11/16/10	10/11/25
6936-54-CDN-3	RESOURCE SHARING IN A TELECOMMUNICATIONS ENVIRONMENT	US	ISSUED	12/901,699	10/11/10	US 2011-0029844 A1	8,276,048	9/25/12	10/11/25
6936-54-CDN-4	RESOURCE SHARING IN A TELECOMMUNICATIONS ENVIRONMENT	US	ISSUED	13/567,261	8/6/12	US 2012-0297148 A1	8,495,473	7/23/13	10/11/25
6936-54-CDN-5	RESOURCE SHARING IN A TELECOMMUNICATIONS ENVIRONMENT	US	ISSUED	13/942,938	7/16/13	US 2013-0308689 A1	8,607,126	12/10/13	10/11/25
6936-54-CDN-6	RESOURCE SHARING IN A TELECOMMUNICATIONS ENVIRONMENT	US	ISSUED	14/081,469	11/15/13	US 2014-0075128 A1	9,069,718	6/30/15	10/11/25
6936-54-CDN-7	RESOURCE SHARING IN A TELECOMMUNICATIONS ENVIRONMENT	US	ISSUED	14/730,874	6/4/15	US 2015-0268863 A1	9,286,251	3/15/16	10/11/25
6936-54-CDN-8	RESOURCE SHARING IN A TELECOMMUNICATIONS ENVIRONMENT	US	ISSUED	15/046,821	2/18/16	US 2016-0179389 A1	9,547,608	1/17/17	10/11/25
6936-54-CDN-9	RESOURCE SHARING IN A TELECOMMUNICATIONS ENVIRONMENT	US	ISSUED	15/372,841	12/8/16	US 2017-0090811 A1	9,898,220	2/20/18	10/11/25
6936-54-CDN-10	RESOURCE SHARING IN A TELECOMMUNICATIONS ENVIRONMENT	US	ISSUED	15/874,277	1/18/18	US 2018-0157436 A1	10,409,510	9/10/19	10/11/25
6936-54-CDN-10-DIV	RESOURCE SHARING IN A TELECOMMUNICATIONS ENVIRONMENT	US	ISSUED	16/261,109	1/29/19	US 2019-0155530 A1	10,579,291	3/3/20	10/11/25
6936-54-CDN-11	RESOURCE SHARING IN A TELECOMMUNICATIONS ENVIRONMENT	US	PUBLISHED	16/544,003	8/19/19	US 2019-0369891 A1			10/11/25
6936-54-PAU	Resource Sharing in a Telecommunications Environment	AU	ABANDONED	2005296086	10/11/05	AU 2005296086			4/6/11
6936-54-PAU-DIV	Resource Sharing in a Telecommunications Environment	AU	ABANDONED	2011201250	10/11/05	AU 2011201250			2/23/15
6936-54-PAU-DIV-2	Resource Sharing in a Telecommunications Environment	AU	ISSUED	2015200618	10/11/05		2015200618	11/12/15	10/11/25
6936-54-PCA	Resource Sharing in a Telecommunications Environment	CA	ISSUED	2,580,280	10/11/05	CA 2580280	2,580,280	3/10/15	10/11/25
6936-54-PCA-DIV	Resource Sharing in a Telecommunications Environment	CA	ABANDONED	2,869,452	10/11/05		2,869,452	1/19/16	9/25/17
6936-54-PCA-DIV-2	Resource Sharing in a Telecommunications Environment	CA	ABANDONED	2,909,150	10/11/05		2,909,150	11/7/17	9/4/20
6936-54-PCA-DIV-3	Resource Sharing in a Telecommunications Environment	CA	ISSUED	2,980,607	10/11/05		2,980,607	4/7/20	10/11/25
6936-54-PCN	Resource Sharing in a Telecommunications Environment	CN	ABANDONED	200580032703.1	10/11/05	CN101057438A			7/14/15
6936-54-PCN-DIV	Resource Sharing in a Telecommunications Environment	CN	ISSUED	201510413116.2	10/11/05	104993912	ZL201510413116.2	12/3/19	10/11/25
6936-54-PCT	RESOURCE SHARING IN A TELECOMMUNICATIONS ENVIRONMENT	WO	NAT PHASE	PCT/US05/36015	10/11/05	WO 2006/044227 A1			
6936-54-PEP	RESOURCE SHARING IN A TELECOMMUNICATIONS ENVIRONMENT	EP	ISSUED	05807443.6	10/11/05	EP 1832028	1832028	1/31/18	10/11/25
6936-54-PEPDE	RESOURCE SHARING IN A TELECOMMUNICATIONS ENVIRONMENT	DE	ISSUED	05807443.6	10/11/05		1832028	1/31/18	10/11/25
6936-54-PEPFR	RESOURCE SHARING IN A TELECOMMUNICATIONS ENVIRONMENT	FR	ISSUED	05807443.6	10/11/05		1832028	1/31/18	10/11/25
6936-54-PEPGB	RESOURCE SHARING IN A TELECOMMUNICATIONS ENVIRONMENT	GB	ISSUED	05807443.6	10/11/05		1832028	1/31/18	10/11/25
6936-54-PEPHK	RESOURCE SHARING IN A TELECOMMUNICATIONS ENVIRONMENT	HK	ISSUED	07110121.4	10/11/05	HK 1102043	HK 1102043	7/6/18	10/11/25
6936-54-PEP-DIV	RESOURCE SHARING IN A TELECOMMUNICATIONS ENVIRONMENT	EP	PUBLISHED	18153945.3	10/11/05	3340511			10/11/25
6936-54-PEP-DIV-HK	RESOURCE SHARING IN A TELECOMMUNICATIONS ENVIRONMENT	HK	PUBLISHED	18113503.3	10/11/05	1254421			10/11/25
6936-54-PIN	Resource Sharing in a Telecommunications Environment	IN	ABANDONED	1208/KOLNP/2007	10/11/05	IN 1208/KOLNP/2007			10/12/24
6936-54-PIP	Resource Sharing in a Telecommunications Environment	JP	ISSUED	2007-533818	10/11/05	2008-516533	4889646	12/22/11	10/11/25
6936-54-PIP-DIV	Resource Sharing in a Telecommunications Environment	JP	ABANDONED	2008-264540	10/11/05	2009-065692	4976359	4/20/12	2/21/17
6936-54-PKR	Method and System for Allocating Shared Memory in a Transceiver	KR	ISSUED	10-2007-7008270	10/11/05	10-2007-0065369	10-1160717	6/21/12	10/11/25
6936-54-PKR-DIV	Method for Allocating Memory in a Transceiver	KR	ABANDONED	10-2010-7022463	10/11/05	10-2010/0116234	10-1160765	6/21/12	3/10/17
6936-54-PROV	RESOURCE SHARING IN A TELECOMMUNICATIONS ENVIRONMENT	US	EXPIRED	60/618,269	10/12/04	N/A			10/12/05

6936-47	SYSTEM AND METHOD FOR SCRAMBLING THE PHASE OF THE CARRIERS IN A MULTICARRIER COMMUNICATIONS SYSTEM	US	ISSUED	09/710,310	11/9/00	N/A	6,961,369	11/1/05	7/28/23
6936-47-CDN	SYSTEM AND METHOD FOR SCRAMBLING THE PHASE OF THE CARRIERS IN A MULTICARRIER COMMUNICATIONS SYSTEM	US	EXPIRED	11/211,535	8/26/05	US 2006-0002454 A1	7,292,627	11/6/07	11/9/20
6936-47-CDN-2	System and Method for Scrambling the Phase of the Carriers in a Multicarrier Communications System	US	EXPIRED	11/863,581	9/28/07	US 2008-0069253 A1	7,471,721	12/30/08	11/9/20
6936-47-CDN-3	System and Method for Scrambling the Phase of the Carriers in a Multicarrier Communications System	US	EXPIRED	12/255,713	10/22/08	US 2009-0110105 A1	7,769,104	8/3/10	11/9/20
6936-47-CDN-4	System and Method for Scrambling the Phase of the Carriers in a Multicarrier Communications System	US	EXPIRED	12/783,725	5/20/10	US 2010-0290507 A1	8,090,008	1/3/12	11/9/20
6936-47-CDN-5	System and Method for Scrambling the Phase of the Carriers in a Multicarrier Communications System	US	EXPIRED	13/303,417	11/23/11	US 2012-0069878 A1	8,718,138	5/6/14	11/18/20
6936-47-CDN-6	System and Method for Scrambling the Phase of the Carriers in a Multicarrier Communications System	US	EXPIRED	14/256,677	4/18/14	US 2014-0226737 A1	8,929,470	1/6/15	11/9/20
6936-47-CDN-7	System and Method for Scrambling the Phase of the Carriers in a Multicarrier Communications System	US	EXPIRED	14/540,332	11/13/14	US 2015-0071385 A1	9,755,876	9/3/17	11/9/20
6936-47-CDN-8	System and Method for Scrambling the Phase of the Carriers in a Multicarrier Communications System	US	EXPIRED	15/693,914	9/1/17	US 2018-0013599 A1	10,187,240	1/22/19	11/9/20
6936-47-CDN-DIV	System and Method for Descrambling the Phase of the Carriers in a Multicarrier Communications System	US	ISSUED	11/860,080	9/24/07		8,073,041	12/6/11	11/5/23
6936-47-CDN-DIV-CON	System and method for descrambling the phase of carriers in a multicarrier communications system	US	EXPIRED	13/284,549	10/28/11	US 2012-0044977 A1	8,218,610	7/10/12	11/9/20
6936-47-CDN-DIV-CON-2	System and Method for Descrambling the Phase of Carriers in a Multicarrier Communications System	US	EXPIRED	13/439,605	4/4/12	US 2012-0195353 A1	8,355,427	1/15/13	11/9/20
6936-47-CDN-DIV-CON-3	System and Method for Scrambling Using a Bit Scrambler and a Phase Scrambler	US	EXPIRED	13/718,016	12/18/12	US 2013-0136160-A1	9,014,243	4/21/15	11/9/20
6936-47-CDN-DIV-CON-4	SYSTEM AND METHOD FOR SCRAMBLING USING A BIT SCRAMBLER AND A PHASE SCRAMBLER	US	EXPIRED	14/684,737	4/13/15	US 2015-0222467 A1	9,485,128	11/1/16	11/9/20
6936-47-CDN-DIV-CON-5	SYSTEM AND METHOD FOR SCRAMBLING USING A BIT SCRAMBLER AND A PHASE SCRAMBLER	US	PUBUSHED	15/298,817	10/20/16	US 2017-0041173 A1			11/9/20
6936-47-PAU	SYSTEM AND METHOD FOR SCRAMBLING THE PHASE OF THE CARRIERS IN A MULTICARRIER COMMUNICATIONS SYSTEM	AU	ABANDONED	13964/01	11/9/00	AU 1596401			11/9/20
6936-47-PCA	SYSTEM AND METHOD FOR SCRAMBLING THE PHASE OF THE CARRIERS IN A MULTICARRIER COMMUNICATIONS SYSTEM	CA	ABANDONED	2,387,812	11/9/00	CA2387812			11/9/20
6936-47-PCT	SYSTEM AND METHOD FOR SCRAMBLING THE PHASE OF THE CARRIERS IN A MULTICARRIER COMMUNICATIONS SYSTEM	WO	NAT PHASE	PCT/US00/030958	11/9/00	WO 2001/035591			
6936-47-PEP	SYSTEM AND METHOD FOR SCRAMBLING THE PHASE OF THE CARRIERS IN A MULTICARRIER COMMUNICATIONS SYSTEM	EP	ABANDONED	00978507.2	11/9/00	EP 1228615			11/9/20
6936-47-PIP	SYSTEM AND METHOD FOR SCRAMBLING THE PHASE OF THE CARRIERS IN A MULTICARRIER COMMUNICATIONS SYSTEM	JP	ABANDONED	2001-537217	11/9/00	2003-514444A			11/9/20
6936-47-PIP-DIV	System and Method for Scrambling the Phase of the Carriers in a Multicarrier Communications System	JP	ABANDONED	2006-345675	11/9/00	JP 2007/129755			11/9/20
6936-47-PKR	SYSTEM AND METHOD FOR SCRAMBLING THE PHASE OF THE CARRIERS IN A MULTICARRIER COMMUNICATIONS SYSTEM	KR	ABANDONED	2002-7005830	11/9/00	10-2002-0049025			11/9/20
6936-47-PROV	SYSTEM AND METHOD FOR SCRAMBLING THE PHASE OF THE CARRIERS IN A MULTICARRIER COMMUNICATIONS SYSTEM	US	EXPIRED	60/164,134	11/9/99	N/A			11/9/00
6936-53	CRC COUNTER NORMALIZATION	US	ISSUED	11/232,899	9/23/05	US 2006-0069980 A1	7,451,379	11/11/08	3/8/27
6936-53-CDN	CRC COUNTER NORMALIZATION	US	ISSUED	12/236,902	9/24/08	US 2009-0019346	7,925,958	4/12/11	5/4/26
6936-53-CDN-2	CRC COUNTER NORMALIZATION	US	ISSUED	12/783,771	5/20/10	US 2010-0293444 A1	7,979,778	7/12/11	9/23/25
6936-53-CDN-3	CRC COUNTER NORMALIZATION	US	ISSUED	13/156,098	6/8/11	US 2011-0239087 A1	8,516,337	8/20/13	9/23/25
6936-53-CDN-4	CRC COUNTER NORMALIZATION	US	ISSUED	13/968,880	8/16/13	US 2013-0339828 A1	8,793,553	7/29/14	9/23/25
6936-53-CDN-5	CRC COUNTER NORMALIZATION	US	ISSUED	14/338,503	7/23/14	US 2014-0337683 A1	8,984,366	3/17/15	9/23/25
6936-53-CDN-6	CRC COUNTER NORMALIZATION	US	ISSUED	14/638,889	3/4/15	US 2015-0180508 A1	9,300,324	3/29/16	9/23/25
6936-53-CDN-7	CRC COUNTER NORMALIZATION	US	ISSUED	15/062,522	3/7/16	US 2016-0188403 A1	10,049,003	8/14/18	9/23/25
6936-53-CDN-8	CRC COUNTER NORMALIZATION	US	ISSUED	16/037,825	7/17/18	US 2018-0341544 A1	10,346,243	7/9/19	9/23/25
6936-53-CDN-9	CRC COUNTER NORMALIZATION	US	PUBUSHED	16/428,232	5/31/19	US 2019-0286514 A1			9/23/25
6936-53-PAU	CRC COUNTER NORMALIZATION	AU	ISSUED	2005289753	9/23/05	AU 2005289753	2005289753	3/19/09	9/23/25
6936-53-PAU-DIV	CRC COUNTER NORMALIZATION	AU	ABANDONED	2009200784	9/23/05	AU 2009200784			6/27/11
6936-53-PCA	CRC COUNTER NORMALIZATION	CA	ISSUED	2,550,263	9/23/05	CA 2550263	2,550,263	11/2/10	9/23/25

6936-53-PCA-DIV	CRC COUNTER NORMALIZATION	CA	ABANDONED	2,711,718	9/23/05	CA 2711718	2,711,718	3/24/15	7/28/20
6936-53-PCA-DIV-2	CRC COUNTER NORMALIZATION	CA	ABANDONED	2,876,137	9/23/05		2,876,137	9/13/16	9/12/18
6936-53-PCA-DIV-3	CRC COUNTER NORMALIZATION	CA	ABANDONED	2,935,980	9/23/05		2,935,980	1/8/19	7/28/20
6936-53-PCA-DIV-4	CRC COUNTER NORMALIZATION	CA	ABANDONED	3,023,907	9/23/05		3,023,907	6/4/19	7/28/20
6936-53-PCN	CRC COUNTER NORMALIZATION	CN	ISSUED	200580008869.X	9/23/05	CN1934817A	200580008869.X	5/16/12	9/23/25
6936-53-PCN-DIV	CRC COUNTER NORMALIZATION	CN	ABANDONED	201210063701.0	9/23/05	CN 102624488	201210063701.0	11/25/15	7/25/17
6936-53-PCN-DIV-HK	A Method and a system for Cyclic Redundancy Checksum (CRC) Anomaly Counter Normalization, and a Module Performing the Method.	HK	ABANDONED	13101408.9	9/23/05	HK1174752			3/22/16
6936-53-PCT	CRC COUNTER NORMALIZATION	WO	NAT PHASE	PCT/US05/03922	9/23/05	WO 2006/036723 A1			
6936-53-PEP	CRC COUNTER NORMALIZATION	EP	ISSUED	05799765.2	9/23/05	1792430	1792430	7/20/11	9/23/25
6936-53-PEPBE	CRC COUNTER NORMALIZATION	BE	ABANDONED	05799765.2	9/23/05	N/A	1792430	7/20/11	8/4/20
6936-53-PEPCH	CRC COUNTER NORMALIZATION	CH	ABANDONED	05799765.2	9/23/05	N/A	1792430	7/20/11	8/4/20
6936-53-PEPDE	CRC COUNTER NORMALIZATION	DE	ISSUED	05799765.2	9/23/05	N/A	1792430	7/20/11	9/23/25
6936-53-PEPDK	CRC COUNTER NORMALIZATION	DK	ABANDONED	05799765.2	9/23/05	N/A	1792430	7/20/11	8/4/20
6936-53-PEPFR	CRC COUNTER NORMALIZATION	FR	ISSUED	05799765.2	9/23/05	N/A	1792430	7/20/11	9/23/25
6936-53-PEPGB	CRC COUNTER NORMALIZATION	GB	ABANDONED	05799765.2	9/23/05	N/A	1792430	7/20/11	8/6/19
6936-53-PEPHK	CRC COUNTER NORMALIZATION	HK	ABANDONED	07110654.9	9/23/05	HK 1102488			8/4/11
6936-53-PEPIE	CRC COUNTER NORMALIZATION	IE	ABANDONED	05799765.2	9/23/05	N/A	1792430	7/20/11	8/4/20
6936-53-PEPINL	CRC COUNTER NORMALIZATION	NL	ISSUED	05799765.2	9/23/05	N/A	1792430	7/20/11	9/23/25
6936-53-PEPSE	CRC COUNTER NORMALIZATION	SE	ABANDONED	05799765.2	9/23/05	N/A	1792430	7/20/11	8/4/20
6936-53-PEP-DIV	CRC COUNTER NORMALIZATION	EP	ISSUED	11005906.0	9/23/05	EP2381610A1	2381610	12/21/16	9/23/25
6936-53-PEP-DIV-DE	CRC COUNTER NORMALIZATION	DE	ISSUED	11005906.0	9/23/05		2381610	12/21/16	9/23/25
6936-53-PEP-DIV-FR	CRC COUNTER NORMALIZATION	FR	ISSUED	11005906.0	9/23/05		2381610	12/21/16	9/23/25
6936-53-PEP-DIV-GB	CRC COUNTER NORMALIZATION	GB	ISSUED	11005906.0	9/23/05		2381610	12/21/16	9/23/25
6936-53-PEP-DIV-2	CRC COUNTER NORMALIZATION	EP	ISSUED	16020487.1	9/23/05	3176973	3176973	6/17/20	9/23/25
6936-53-PEP-DIV-2-DE	CRC COUNTER NORMALIZATION	DE	ISSUED	16020487.1	9/23/05		3176973	6/17/20	9/23/25
6936-53-PEP-DIV-2-FR	CRC COUNTER NORMALIZATION	FR	ISSUED	16020487.1	9/23/05		3176973	6/17/20	9/23/25
6936-53-PEP-DIV-2-GB	CRC COUNTER NORMALIZATION	GB	ISSUED	16020487.1	9/23/05		3176973	6/17/20	9/23/25
6936-52-PIN	CRC COUNTER NORMALIZATION	IN	ABANDONED	1601/KOLNP/2006	9/23/05	IN 1601/KOLNP/2006			9/23/25
6936-53-PJP	CRC COUNTER NORMALIZATION	JP	ABANDONED	2006-551651	9/23/05	2007-519382			10/12/11
6936-53-PJP-DIV	CRC COUNTER NORMALIZATION	JP	ABANDONED	2006-345676	9/23/05	JP 2007/151145			10/12/11
6936-53-PJP-DIV-2	CRC COUNTER NORMALIZATION	JP	ISSUED	2010-042193	9/23/05	2010-178353	5237317	4/5/13	9/23/25
6936-53-PJP-DIV-3	CRC COUNTER NORMALIZATION	JP	ISSUED	2012-194723	9/23/05	2013-009417	3823936	10/16/15	9/23/25
6936-53-PJP-DIV-4	CRC COUNTER NORMALIZATION	JP	ISSUED	2015-105633	9/23/05	2015-167401	6215254	9/29/17	9/23/25
6936-53-PJP-DIV-5	CRC COUNTER NORMALIZATION	JP	ISSUED	2016-162059	9/23/05	2016-220241	6335230	5/11/18	9/23/25
6936-53-PKR	CRC COUNTER NORMALIZATION	KR	ISSUED	10-2006-7011697	9/23/05	10-2007-0072425	10-0955190	4/20/10	9/23/25
6936-53-PKR-DIV	CRC COUNTER NORMALIZATION	KR	ABANDONED	10-2010-7005285	9/23/05	10-2010/0035665			9/23/25
6936-53-PKR-DIV-2	CRC COUNTER NORMALIZATION	KR	ABANDONED	10-2010-7024190	9/23/05	10-2010-0120722			9/23/25
6936-53-PROV	CRC COUNTER NORMALIZATION METHOD AND SYSTEM	US	EXPIRE	60/613,594	9/25/04	N/A			9/25/05
6936-52-PCA	Impulse Noise Management	CA	ISSUED	2,555,757	3/3/05	CA 2555757	2,555,757	1/20/15	3/3/25
6936-52-PCA-REI	Impulse Noise Management	CA	ISSUED	2,555,757R	3/3/05		2,555,757	3/27/18	3/3/25
6936-52-PCN	On-Line Impulse Noise Protection (INP) Adaptation	CN	ABANDONED	200580006738.8	3/3/05	CN1926794A			11/10/11
6936-52-PCT	ON-LINE IMPULSE NOISE PROTECTION (INP) ADAPTATION	WO	NAT PHASE	PCT/US05/06842	3/3/05	WO 2005/086405 A3			
6936-52-PEP	Impulse Noise Management	EP	ABANDONED	05724394.1	3/3/05	EP 1721403			3/3/25
6936-52-PEPHK	ON-LINE IMPULSE NOISE PROTECTION (INP) ADAPTATION	HK	ABANDONED	07105044.1	3/3/05	HK 1097672			8/23/12
6936-52-PEP-DIV	Impulse Noise Management	EP	ABANDONED	10006702.4	3/3/05	2228936			3/7/11
6936-52-PEP-DIV-HK	Impulse Noise Management	HK	ABANDONED	10110020.1	3/3/05	HK 1143672			8/23/12
6936-52-PIN	ON-LINE IMPULSE NOISE PROTECTION (INP) ADAPTATION	IN	ABANDONED	2155/KOLNP/2006	7/31/06	IN 2137/KOLNP/2006			7/31/26
6936-52-PROV	ON-LINE IMPULSE NOISE PROTECTION (INP) ADAPTATION	US	EXPIRE	60/549,804	3/3/04	N/A			3/3/05
6936-52-PROV-2	IMPULSE NOISE PROTECTION (INP) TRAINING	US	EXPIRE	60/555,982	3/24/04	N/A			3/24/05
6936-52-PUS	Impulse Noise Management	US	ABANDONED	10/597,482	7/27/06	US 2008-0232444 A1			10/14/11
6936-52-PUS-CON	Impulse Noise Management	US	ISSUED	12/769,193	4/28/10	US 2010-0220771 A1	8,462,835	6/11/13	3/3/25
6936-52-PUS-CON-2	Impulse Noise Management	US	ISSUED	13/914,852	6/11/13	US 2013-0272355 A1	8,594,162	11/26/13	3/3/25
6936-52-PUS-CON-3	Impulse Noise Management	US	ISSUED	14/075,077	11/8/13	US 2014-0064343 A1	8,743,932	6/3/14	3/3/25
6936-52-PUS-CON-4	Impulse Noise Management	US	ABANDONED	14/285,911	5/23/14	US 2014-0254643 A1			2/11/16
6936-52-PUS-CON-5	IMPULSE NOISE MANAGEMENT	US	ABANDONED	14/757,630	12/23/15	US 2016-0127079 A1			9/10/18
6936-52-PUS-CON-6	IMPULSE NOISE MANAGEMENT	US	ISSUED	16/126,027	9/10/18	US 2019-0007164 A1	10,567,112	2/18/20	3/3/25
6936-52-PUS-CON-6-DIV	IMPULSE NOISE MANAGEMENT	US	ISSUED	16/448,939	6/21/19	US 2019-0312667 A1	10,805,040	10/13/20	3/3/25
6936-52-PUS-CON-7	IMPULSE NOISE MANAGEMENT	US	PUBLISHED	16/781,802	2/4/20	US 2020-0177304 A1			3/3/25
6936-28	MULTICARRIER TRANSMISSION SYSTEM WITH LOW POWER SLEEP MODE AND RAPID-ON CAPABILITY	US	EXPIRE	09/581,400	6/13/00	N/A	6,445,730	9/3/02	1/26/19
6936-28-CON	MULTICARRIER TRANSMISSION SYSTEM WITH LOW POWER SLEEP MODE AND RAPID-ON CAPABILITY	US	ABANDONED	10/175,815	6/21/02	US 2002-0150152			5/17/04
6936-28-CON-1	MULTICARRIER TRANSMISSION SYSTEM WITH LOW POWER SLEEP MODE AND RAPID-ON CAPABILITY	US	ABANDONED	10/778,083	2/17/04	US 2004-0166906			5/30/05
6936-28-CON-2	MULTICARRIER TRANSMISSION SYSTEM WITH LOW POWER SLEEP MODE AND RAPID-ON CAPABILITY	US	ABANDONED	11/090,183	3/28/05	US 2005-0185726 A1			3/12/06
6936-28-CON-3	MULTICARRIER TRANSMISSION SYSTEM WITH LOW POWER SLEEP MODE AND RAPID-ON CAPABILITY	US	ABANDONED	11/285,516	11/30/05	US 2006-0078060 A1			

6936-28-CD-N-4	MULTICARRIER TRANSMISSION SYSTEM WITH LOW POWER SLEEP MODE AND RAPID-ON CAPABILITY	US	EXPIRED	11/425,507	6/21/06	US 2006-0233273 A1	7,697,598	4/13/10	1/26/19
6936-28-CD-N-5	Multicarrier Transmission System with Low Power Sleep Mode and Rapid-on Capability	US	ABANDONED	12/615,946	11/10/09	US 2010-0054312 A1	7,978,753	7/12/11	12/12/18
6936-28-CD-N-6	Multicarrier Transmission System with Low Power Sleep Mode and Rapid-On Capability	US	EXPIRED	13/152,558	6/3/11	US 2011-0235691 A1	8,437,382	5/7/13	1/26/19
6936-28-CD-N-7	Multicarrier Transmission System with Low Power Sleep Mode and Rapid-On Capability	US	EXPIRED	13/887,889	5/6/13	US 2013-0243051-A1	8,611,404	12/17/13	1/26/19
6936-28-CD-N-8	Multicarrier Transmission System with Low Power Sleep Mode and Rapid-On Capability	US	EXPIRED	14/092,248	11/27/13	US 2014-0086287 A1	8,750,352	6/10/14	1/26/19
6936-28-CD-N-9	Multicarrier Transmission System with Low Power Sleep Mode and Rapid-On Capability	US	ABANDONED	14/295,981	6/4/14	US 2014-0286379 A1	9,094,268	7/28/15	12/12/18
6936-28-CD-N-10	MULTICARRIER TRANSMISSION SYSTEM WITH LOW POWER SLEEP MODE AND RAPID-ON CAPABILITY	US	EXPIRED	14/798,014	7/13/15	US 2015-0326404 A1	9,521,003	12/13/16	1/26/19
6936-28-CD-N-11	MULTICARRIER TRANSMISSION SYSTEM WITH LOW POWER SLEEP MODE AND RAPID-ON CAPABILITY	US	ABANDONED	15/180,274	6/13/16	US 2016-0286493 A1			11/19/18
6936-28-PAU	MULTICARRIER TRANSMISSION SYSTEM WITH LOW POWER SLEEP MODE AND RAPID-ON CAPABILITY	AU	EXPIRED	23409/99	1/26/99	AU 2340999	764933	12/18/03	1/26/19
6936-28-PAU-2	MULTICARRIER TRANSMISSION SYSTEM WITH LOW POWER SLEEP MODE AND RAPID-ON CAPABILITY	AU	ABANDONED	2003266426	12/4/03	AU 2003266429			3/10/05
6936-28-PCA	MULTICARRIER TRANSMISSION SYSTEM WITH LOW POWER SLEEP MODE AND RAPID-ON CAPABILITY	CA	EXPIRED	2,357,551	1/26/99	CA 2357551	2,357,551	9/30/08	1/26/19
6936-28-PCA-DIV	Multicarrier Transmission System With Low Power Sleep Mode and Rapid-On Capability	CA	ABANDONED	2,633,064	1/26/99	CA 2633064	2,633,064	4/2/13	12/23/16
6936-28-PCA-DIV-2	Multicarrier Transmission System With Low Power Sleep Mode and Rapid-On Capability	CA	EXPIRED	2,800,005	1/26/99		2,800,005	3/14/17	1/26/19
6936-28-PCT	MULTICARRIER TRANSMISSION SYSTEM WITH LOW POWER SLEEP MODE AND RAPID-ON CAPABILITY	WO	NAT PHASE	PCT/US99/01339	1/26/99	WO 2000/045559			
6936-28-PEP	MULTICARRIER TRANSMISSION SYSTEM WITH LOW POWER SLEEP MODE AND RAPID-ON CAPABILITY	EP	EXPIRED	99903370.7	1/26/99	1145518	1145518	11/24/04	1/26/19
6936-28-PEPGB	MULTICARRIER TRANSMISSION SYSTEM WITH LOW POWER SLEEP MODE AND RAPID-ON CAPABILITY	GB	EXPIRED	99903370.7	1/26/99	N/A	1145518	11/24/04	1/26/19
6936-28-PEP-2	MULTICARRIER TRANSMISSION SYSTEM WITH LOW POWER SLEEP MODE AND RAPID-ON CAPABILITY	EP	EXPIRED	04022871.0	1/26/99	1524812	1524812	10/31/07	1/26/19
6936-28-PEP-2-DE	MULTICARRIER TRANSMISSION SYSTEM WITH LOW POWER SLEEP MODE AND RAPID-ON CAPABILITY	DE	EXPIRED	04022871.0	1/26/99	N/A	1524812	10/31/07	1/26/19
6936-28-PEP-2-FR	MULTICARRIER TRANSMISSION SYSTEM WITH LOW POWER SLEEP MODE AND RAPID-ON CAPABILITY	FR	EXPIRED	04022871.0	1/26/99	N/A	1524812	10/31/07	1/26/19
6936-28-PEP-2-GB	MULTICARRIER TRANSMISSION SYSTEM WITH LOW POWER SLEEP MODE AND RAPID-ON CAPABILITY	GB	EXPIRED	04022871.0	1/26/99	N/A	1524812	10/31/07	1/26/19
6936-28-PEP-3	Multicarrier Transmission System with Low Power Sleep Mode and Rapid-on-Capability	EP	EXPIRED	07021150.3	1/26/99	1901512	1901512	11/23/11	1/26/19
6936-28-PEP-3-DE	Multicarrier Transmission System with Low Power Sleep Mode and Rapid-on-Capability	DE	EXPIRED	07021150.3	1/26/99	N/A	1901512	11/23/11	1/26/19
6936-28-PEP-3-FR	Multicarrier Transmission System with Low Power Sleep Mode and Rapid-on-Capability	FR	EXPIRED	07021150.3	1/26/99	N/A	1901512	11/23/11	1/26/19
6936-28-PEP-3-GB	Multicarrier Transmission System with Low Power Sleep Mode and Rapid-on-Capability	GB	EXPIRED	07021150.3	1/26/99	N/A	1901512	11/23/11	1/26/19
6936-28-PEP-3-HK	Multicarrier Transmission System with Low Power Sleep Mode and Rapid-on-Capability	HK	ABANDONED	08110349.9	1/26/99	HK 1117978			7/28/11
6936-28-PEP-3-DIV-1	Multicarrier Transmission System with Low Power Sleep Mode and Rapid-on-Capability	EP	EXPIRED	10011996.5	1/26/99	2302857	2302857	9/2/15	1/26/19
6936-28-PEP-3-DIV-1-DE	Multicarrier Transmission System with Low Power Sleep Mode and Rapid-on-Capability	DE	EXPIRED	10011996.5	1/26/99		2302857	9/2/15	1/26/19
6936-28-PEP-3-DIV-1-FR	Multicarrier Transmission System with Low Power Sleep Mode and Rapid-on-Capability	FR	EXPIRED	10011996.5	1/26/99		2302857	9/2/15	1/26/19
6936-28-PEP-3-DIV-1-GB	Multicarrier Transmission System with Low Power Sleep Mode and Rapid-on-Capability	GB	EXPIRED	10011996.5	1/26/99		2302857	9/2/15	1/26/19
6936-28-PEP-3-DIV-2	Multicarrier Transmission System with Low Power Sleep Mode and Rapid-on-Capability	EP	EXPIRED	10012013.8	1/26/99	2330749	2330749	4/30/14	1/26/19
6936-28-PEP-3-DIV-2-DE	Multicarrier Transmission System with Low Power Sleep Mode and Rapid-on-Capability	DE	EXPIRED	10012013.8	1/26/99		2330749	4/30/14	1/26/19
6936-28-PEP-3-DIV-2-FR	Multicarrier Transmission System with Low Power Sleep Mode and Rapid-on-Capability	FR	EXPIRED	10012013.8	1/26/99		2330749	4/30/14	1/26/19

6936-28-PEP-3-DIV-2-GB	Multicarrier Transmission System with Low Power Sleep Mode and Rapid-on-Capability	GB	EXPIRED	10012013.8	1/26/99		2330749	4/30/14	1/26/19
6936-28-PIP	MULTICARRIER TRANSMISSION SYSTEM WITH LOW POWER SLEEP MODE AND RAPID-ON CAPABILITY	JP	EXPIRED	2000-596705	1/26/99	2003-518341	4282907	3/27/09	1/26/19
6936-28-PIP-DIV	MULTICARRIER TRANSMISSION SYSTEM WITH LOW POWER SLEEP MODE AND RAPID-ON CAPABILITY	JP	ABANDONED	2008-323651	1/26/99	N/A			1/26/19
6936-28-PKR	MULTICARRIER TRANSMISSION SYSTEM WITH LOW POWER SLEEP MODE AND RAPID-ON CAPABILITY	KR	ABANDONED	7009402/2001	1/26/99	10-2001-0108132			5/15/06
6936-28-PROV	MULTICARRIER TRANSMISSION SYSTEM WITH LOW POWER SLEEP MODE AND RAPID-ON CAPABILITY	US	EXPIRED	60/072,447	1/26/98	N/A			1/26/99
6936-55-PAU	Initialization in the Presence of Impulse Noise	AU	ISSUED	2005295758	10/14/05	AU 2005295758	2005295758	7/9/10	10/14/25
6936-55-PAU-2	Initialization in the Presence of Impulse Noise	AU	ABANDONED	2010202626	10/14/05	AU 2010202626			6/27/11
6936-55-PCA	DMT Symbol Repetition in the Presence of Impulse Noise	CA	ISSUED	2,582,106	10/14/05	2,582,106	2,582,106	4/28/15	10/14/25
6936-55-PCA-DIV	DMT Symbol Repetition in the Presence of Impulse Noise	CA	ABANDONED	2,881,036	10/14/05	2,881,036		12/22/15	9/8/20
6936-55-PCA-DIV-2	DMT Symbol Repetition in the Presence of Impulse Noise	CA	ABANDONED	2,906,478	10/14/05		2,906,478	1/8/19	10/14/25
6936-55-PCN	Initialization in the Presence of Impulse Noise	CN	ISSUED	200580034464.3	10/14/05	CN101040480A	200580034464.3	8/31/11	10/14/25
6936-55-PCV-HK	DMT Symbol Repetition in the Presence of Impulse Noise	HK	ISSUED	08102934.7	10/14/05	HK 1108783	HK1108783	12/16/11	10/14/25
6936-55-PCT	DMT Symbol Repetition in the Presence of Impulse Noise	WO	NAT PHASE	PCT/US05/36815	10/14/05	WO 2006/044533 A1			
6936-55-PEP	DMT SYMBOL REPETITION IN THE PRESENCE OF IMPULSE NOISE	EP	ISSUED	05810124.7	10/14/05	1800427	1800427	6/20/12	10/14/25
6936-55-PEPBE	Initialization in the Presence of Impulse Noise	BE	ISSUED	05810124.7	10/14/05		1800427	6/20/12	10/14/25
6936-55-PEPCH	Initialization in the Presence of Impulse Noise	CH	ABANDONED	05810124.7	10/14/05		1800427	6/20/12	9/8/20
6936-55-PEPDE	Initialization in the Presence of Impulse Noise	DE	ISSUED	05810124.7	10/14/05		1800427	6/20/12	10/14/25
6936-55-PEPDK	Initialization in the Presence of Impulse Noise	DK	ABANDONED	05810124.7	10/14/05		1800427	6/20/12	10/14/25
6936-55-PEPES	Initialization in the Presence of Impulse Noise	ES	ISSUED	05810124.7	10/14/05		1800427	6/20/12	10/14/25
6936-55-PEPFR	Initialization in the Presence of Impulse Noise	FR	ISSUED	05810124.7	10/14/05		1800427	6/20/12	10/14/25
6936-55-PEPGB	Initialization in the Presence of Impulse Noise	GB	ISSUED	05810124.7	10/14/05		1800427	6/20/12	10/14/25
6936-55-PEPHK	Initialization in the Presence of Impulse Noise	HK	ISSUED	07112380.6	10/14/05	HK 1103889	1103889	12/28/12	10/14/25
6936-55-PEPIT	Initialization in the Presence of Impulse Noise	IT	ISSUED	05810124.7	10/14/05		1800427	6/20/12	10/14/25
6936-55-PEPNL	Initialization in the Presence of Impulse Noise	NL	ISSUED	05810124.7	10/14/05		1800427	6/20/12	10/14/25
6936-55-PEPSE	Initialization in the Presence of Impulse Noise	SE	ABANDONED	05810124.7	10/14/05		1800427	6/20/12	10/14/25
6936-55-PEP-DIV	Initialization in the Presence of Impulse Noise	EP	ISSUED	11000980.0	10/14/05	2312784	2312784	2/1/17	10/14/25
6936-55-PEP-DIV-DE	Initialization in the Presence of Impulse Noise	DE	ISSUED	11000980.0	10/14/05		2312784	2/1/17	10/14/25
6936-55-PEP-DIV-FR	Initialization in the Presence of Impulse Noise	FR	ISSUED	11000980.0	10/14/05		2312784	2/1/17	10/14/25
6936-55-PEP-DIV-GB	Initialization in the Presence of Impulse Noise	GB	ISSUED	11000980.0	10/14/05		2312784	2/1/17	10/14/25
6936-55-PEP-DIV-2	Initialization in the Presence of Impulse Noise	EP	PUBLISHED	17020039.8	10/14/05	3220567			10/14/25
6936-55-PEP-DIV-2-HK	Initialization in the Presence of Impulse Noise	HK	PUBLISHED	18100419.3	10/14/15	1241167			10/14/35
6936-55-PIN	Initialization in the Presence of Impulse Noise	IN	ABANDONED	1209/KOLNP/2007	10/14/05	IN 1209/KOLNP/2007			10/15/24
6936-55-PIP	DMT Symbol Repetition in the Presence of Impulse Noise	JP	ABANDONED	2007-536883	10/14/05	2008-517535			4/15/13
6936-55-PIP-DIV	DMT Symbol Repetition in the Presence of Impulse Noise	JP	ABANDONED	2008-264567	10/14/05	2009-081862			4/15/13
6936-55-PKR	DMT SYMBOL REPETITION IN THE PRESENCE OF IMPULSE NOISE	KR	ISSUED	10-2007-7008275	10/14/05	10-2007-0061867	10-1272404	5/31/13	10/14/25
6936-55-PKR-DIV	DMT Symbol Repetition in the Presence of Impulse Noise	KR	ISSUED	10-2010-7022479	10/14/05	10-2010/03121542	10-1314976	9/27/13	10/14/25
6936-55-PKR-DIV-2	DMT Symbol Repetition in the Presence of Impulse Noise	KR	ABANDONED	10-2012-7021605	10/14/05				4/16/13
6936-55-PROV	XDSL INITIALIZATION IN THE PRESENCE OF IMPULSE NOISE	US	EXPIRED	60/619,618	10/15/04	N/A			10/15/05
6936-55-PUS	DMT Symbol Repetition in the Presence of Impulse Noise	US	ISSUED	11/575,598	3/20/07	US 2007-0217491 A1	7,796,705	9/14/10	8/22/27
6936-55-PUS-CON	Impulse Noise Protection During Initialization	US	ISSUED	12/769,747	4/29/10	US 2010-0208842 A1	8,913,649	12/16/14	10/14/25
6936-55-PUS-CON-2	DMT Symbol Repetition in the Presence of Impulse Noise	US	ISSUED	14/559,156	12/3/14	US 2015-0146821 A1	9,621,198	4/11/17	10/14/25
6936-55-PUS-CON-3	DMT SYMBOL REPETITION IN THE PRESENCE OF IMPULSE NOISE	US	ABANDONED	15/479,866	4/5/17	US 2017-0214487 A1			9/12/19
6936-55-PUS-CON-4	DMT SYMBOL REPETITION IN THE PRESENCE OF IMPULSE NOISE	US	PUBLISHED	16/569,144	9/12/19	US 2020-0007268 A1			10/14/25
6936-57-PAU	Packet Retransmission and Memory Sharing	AU	ABANDONED	2007257055	4/12/07	AU 2007257055			4/12/27
6936-57-PBR	Packet Retransmission and Memory Sharing	BR	ISSUED	PI-0709871-5	4/12/07	BR P10/709871	PI 0709871-5	10/15/19	10/15/29
6936-57-PCA	Packet Retransmission and Memory Sharing	CA	ISSUED	2,647,589	4/12/07	CA 2647589	2,647,589	8/21/18	4/12/27

6936-57-PCA-DIV	Packet Retransmission and Memory Sharing	CA	PENDING	3/11,163	4/12/07			4/12/27
6936-57-PCN	Packet Retransmission and Memory Sharing	CN	ABANDONED	200780012891.0	4/12/07	CNI01421992A		4/16/13
6936-57-PCN-HK	Packet Retransmission and Memory Sharing	HK	ABANDONED	09109954.6	4/12/07	HK 1133132		4/16/13
6936-57-PCD	Packet Retransmission and Memory Sharing	CO	ABANDONED	08-109.377	4/12/07	08-109.377		4/12/27
6936-57-PCI	Packet Retransmission and Memory Sharing	WO	NAT PHASE	PCT/US07/66522	4/12/07	WO 2007/143277		
6936-57-PEP	Packet Retransmission and Memory Sharing	EP	ISSUED	07811844.5	4/12/07	2005674	2005674	9/28/16
6936-57-PEP-DE	Packet Retransmission and Memory Sharing	DE	ISSUED	07811844.5	4/12/07		2005674	9/28/16
6936-57-PEP-FR	Packet Retransmission and Memory Sharing	FR	ISSUED	07811844.5	4/12/07		2005674	9/28/16
6936-57-PEP-GB	Packet Retransmission and Memory Sharing	GB	ISSUED	07811844.5	4/12/07		2005674	9/28/16
6936-57-PEP-DIV	Packet Retransmission and Memory Sharing	EP	ISSUED	1000001.7.3	4/12/07	2178254	2178254	2/8/17
6936-57-PEP-DIV-DE	Packet Retransmission and Memory Sharing	DE	ISSUED	1000001.7.3	4/12/07		2178254	2/8/17
6936-57-PEP-DIV-FR	Packet Retransmission and Memory Sharing	FR	ISSUED	1000001.7.3	4/12/07		2178254	2/8/17
6936-57-PEP-DIV-GB	Packet Retransmission and Memory Sharing	GB	ISSUED	1000001.7.3	4/12/07		2178254	2/8/17
6936-57-PEP-DIV-HK	Packet Retransmission and Memory Sharing	HK	ABANDONED	10104429.1	4/12/07	HK 1136723		10/26/16
6936-57-PEP-DIV-2	Packet Retransmission and Memory Sharing	EP	ISSUED	10000016.5	4/12/07	2173071	2173071	6/26/13
6936-57-PEP-DIV-2-BE	Packet Retransmission and Memory Sharing	BE	ABANDONED	10000016.5	4/12/07		2173071	6/26/13
6936-57-PEP-DIV-2-DE	Packet Retransmission and Memory Sharing	DE	ABANDONED	10000016.5	4/12/07		2173071	6/26/13
6936-57-PEP-DIV-2-FR	Packet Retransmission and Memory Sharing	FR	ABANDONED	10000016.5	4/12/07		2173071	6/26/13
6936-57-PEP-DIV-2-GB	Packet Retransmission and Memory Sharing	GB	ABANDONED	10000016.5	4/12/07		2173071	6/26/13
6936-57-PEP-DIV-2-HK	Packet Retransmission and Memory Sharing	HK	ABANDONED	10103698.7	4/12/07	HK 1135537	1135537	11/15/13
6936-57-PEP-DIV-3	Packet Retransmission and Memory Sharing	EP	ISSUED	17020026.5	4/12/07	3190756	3190756	10/31/18
6936-57-PEP-DIV-3-DE	Packet Retransmission and Memory Sharing	DE	ISSUED	17020026.5	4/12/07		3190756	10/31/18
6936-57-PEP-DIV-3-FR	Packet Retransmission and Memory Sharing	FR	ISSUED	17020026.5	4/12/07		3190756	10/31/18
6936-57-PEP-DIV-3-GB	Packet Retransmission and Memory Sharing	GB	ISSUED	17020026.5	4/12/07		3190756	10/31/18
6936-57-PEP-DIV-4	Packet Retransmission and Memory Sharing	EP	PUBLISHED	17020525.6	4/12/07	3301871		4/12/27
6936-57-PEP-DIV-4-HK	Packet Retransmission and Memory Sharing	HK	PENDING	18110134.6	4/12/07			4/12/27
6936-57-PIN	Packet Retransmission and Memory Sharing	IN	ABANDONED	4084/KOLNP/2008	4/12/07	IN 4084/KOLNP/2008		4/12/27
6936-57-PJP	6936 and Memory Sharing	JP	ABANDONED	2009-503623	4/12/07	2009-533973		2/27/12
6936-57-PJP-DIV	Packet Retransmission and Memory Sharing	JP	ABANDONED	2010-017356	4/12/07	2010-136427		10/2/12
6936-57-PJP-DIV-2	Packet Retransmission and Memory Sharing	JP	ISSUED	2012-042978	4/12/07	2012-151863	5486621	2/28/14
6936-57-PJP-DIV-3	Packet Retransmission and Memory Sharing	JP	ISSUED	2013-246257	4/12/07	2014-090433	5948307	6/10/16
6936-57-PKR	Packet Retransmission and Memory Sharing	KR	ISSUED	10-2008-7024792	4/12/07	10-2008-0108127	10-1736999	5/11/17
6936-57-PKR-DIV	Packet Retransmission and Memory Sharing	KR	ABANDONED	10-2014-7005299	4/12/07			6/20/16
6936-57-PKR-DIV-2	Packet Retransmission and Memory Sharing	KR	ABANDONED	10-2017-7012757	4/12/07			1/12/18
6936-57-PKR-DIV-3	Packet Retransmission and Memory Sharing	KR	ISSUED	10-2017-7036067	4/12/07		10-1952812	2/21/19
6936-57-PKR-DIV-4	Packet Retransmission and Memory Sharing	KR	ISSUED	10-2019-7005116	4/12/07		10-2151398	8/28/20
6936-57-PMX	Packet Retransmission and Memory Sharing	MX	ISSUED	MX/a/2008/012505	4/12/07	MX 2008012505	301471	7/18/12
6936-57-PMX-DIV	Packet Retransmission and Memory Sharing	MX	ABANDONED	MX/a/2011/005751	4/12/07			4/12/27
6936-57-PROV	XDSL PACKET RETRANSMISSION MECHANISM	US	EXPIRED	60/792,236	4/12/06	N/A		4/12/07
6936-57-PUS	Packet Retransmission and Memory Sharing	US	ISSUED	12/295,828	10/2/08	US 2009-0300450 A1	8,335,956	12/18/12
6936-57-PUS-CON	Packet Retransmission and Memory Sharing	US	ISSUED	12/783,758	5/20/10	US 2011-0002331 A1	8,407,546	3/26/13
6936-57-PUS-CON-2	Packet Retransmission and Memory Sharing	US	ISSUED	13/766,059	2/13/13	US 2013-0163592 A1	8,645,784	2/4/14
6936-57-PUS-CON-3	Packet Retransmission and Memory Sharing	US	ISSUED	14/159,125	1/20/14	US 2014-0133491 A1	9,485,055	11/1/16
6936-57-PUS-CON-4	PACKET RETRANSMISSION AND MEMORY SHARING	US	ISSUED	15/298,526	10/20/16	US 2017-0041224 A1	10,044,473	8/7/18
6936-57-PUS-CON-5	PACKET RETRANSMISSION AND MEMORY SHARING	US	ISSUED	16/046,494	7/26/18	US 2018-0331790 A1	10,484,140	11/19/19
6936-57-PUS-CON-6	PACKET RETRANSMISSION AND MEMORY SHARING	US	PUBLISHED	16/561,835	9/5/19	US 2019-0393991 A1		4/12/27
6936-57-PUS-DIV	Packet Retransmission	US	ISSUED	12/760,728	4/15/10	US 2010-0205501 A1	8,595,577	11/26/13
6936-57-PUS-DIV-CON	Packet Retransmission	US	ISSUED	12/783,765	5/20/10	US 2010-0332935 A1	8,468,411	6/18/13
6936-57-PUS-DIV-CON-2	Packet Retransmission	US	ISSUED	14/075,194	11/8/13	US 2014-0068366 A1	9,094,348	7/28/15
6936-57-PUS-DIV-CON-3	Packet Retransmission	US	ISSUED	14/742,334	6/17/15	US 2015-0312001 A1	9,749,235	8/29/17

6936-57-PUS-DIV-CDN-4	Packet Retransmission	US	ISSUED	15/678,870	8/16/17	US 2017-0373971 A1	10,498,495	12/3/19	4/12/27
6936-57-PUS-DIV-CDN-5	TECHNIQUES FOR PACKET AND MESSAGE COMMUNICATION IN A MULTICARRIER TRANSCIVER ENVIRONMENT	US	ISSUED	16/701,343	12/3/19	US 2020-0106558 A1	10,833,809	11/10/20	4/12/27
6936-57-PUS-DIV-CDN-6	PACKET RETRANSMISSION	US	PENDING	17/027,196	9/21/20				4/12/27
6936-59-PROV	ADSL Packet Retransmission Mechanism With Examples	US	EXPIRE D	60/849,650	10/5/06	N/A			10/5/07
6936-26	SYSTEMS AND METHODS FOR A MULTICARRIER MODULATION SYSTEM WITH A VARIABLE MARGIN	US	ABANDONED	09/836,295	4/18/01	US 2002-0009135			10/4/05
6936-26-CDN	SYSTEMS AND METHODS FOR A MULTICARRIER MODULATION SYSTEM WITH A VARIABLE MARGIN	US	ABANDONED	11/242,024	10/4/05	US 2006-0018395 A1			4/18/21
6936-26-CDN-2	Systems and Methods for a Multicarrier Modulation System with a Variable Margin	US	ABANDONED	11/972,340	1/10/08	US 2008-0107204 A1			7/27/11
6936-26-CDN-3	Systems and Methods for a Multicarrier Modulation System with a Variable Margin	US	ISSUED	12/694,143	1/26/10	US 2010-0128810 A1	8,374,226	2/12/13	7/3/21
6936-26-CDN-4	Systems and Methods for a Multicarrier Modulation System with a Variable Margin	US	ABANDONED	13/467,392	5/9/12	US 2012-0219047 A1			4/18/21
6936-26-CDN-5	Systems and Methods for a Multicarrier Modulation System with a Variable Margin	US	ISSUED	13/764,529	2/11/13	US 2013-0148708 A1	8,625,660	1/7/14	4/18/21
6936-26-CDN-6	Systems and Methods for a Multicarrier Modulation System with a Variable Margin	US	ISSUED	14/079,285	11/13/13	US 2014-0072062 A1	8,937,988	1/20/15	4/18/21
6936-26-CDN-7	Systems and Methods for a Multicarrier Modulation System with a Variable Margin	US	ISSUED	14/591,612	1/7/15	US 2015-0117557 A1	9,154,354	10/6/15	4/18/21
6936-26-CDN-8	SYSTEMS AND METHODS FOR A MULTICARRIER MODULATION SYSTEM WITH A VARIABLE MARGIN	US	ABANDONED	14/965,966	9/25/15	US 2016-0013962 A1			12/13/16
6936-26-CDN-9	SYSTEMS AND METHODS FOR A MULTICARRIER MODULATION SYSTEM WITH A VARIABLE MARGIN	US	ISSUED	15/348,372	11/10/16	US 2017-0078125 A1	9,893,921	2/13/18	4/18/21
6936-26-CDN-10	SYSTEMS AND METHODS FOR A MULTICARRIER MODULATION SYSTEM WITH A VARIABLE MARGIN	US	ISSUED	15/886,295	2/1/18	US 2018-0159711 A1	10,708,104	7/7/20	4/18/21
6936-26-PAU	MULTICARRIER MODULATION SYSTEM WITH VARIABLE MARGIN TO ACCOUNT FOR TIME VARYING IMPAIRMENTS	AU	ABANDONED	2001257081	4/18/01	N/A			
6936-26-PAU-CON	Data Allocation with Variable SNR Margins	AU	ISSUED	2007200448	4/18/01	AU 2007200448	2007200448	8/6/09	4/18/21
6936-26-PAU-CON-2	Data Allocation with Variable SNR Margins	AU	ABANDONED	2009202880	4/18/05	AU 2009202880			10/18/11
6936-26-PCA	MULTICARRIER MODULATION SYSTEM WITH VARIABLE MARGIN TO ACCOUNT FOR TIME VARYING IMPAIRMENTS	CA	ISSUED	2,406,151	4/18/01	CA 2405151	2,406,151	4/13/10	4/18/21
6936-26-PCA-2	DATA ALLOCATION WITH VARIABLE SNR MARGINS	CA	ABANDONED	2,689,952	4/18/01	CA 689952			2/24/11
6936-26-PCT	MULTICARRIER MODULATION SYSTEM WITH VARIABLE MARGIN TO ACCOUNT FOR TIME VARYING IMPAIRMENTS	WO	NAT PHASE	PCT/US01/12555	4/18/01	WO 2001/080510			
6936-26-PEP	MULTICARRIER MODULATION SYSTEM WITH VARIABLE MARGIN TO ACCOUNT FOR TIME VARYING IMPAIRMENTS	EP	ABANDONED	01930554.9	4/18/01	EP 1275229	1275229	3/21/07	4/18/21
6936-26-PEPBE	Data Allocation With Variable SNR Margins	BE	ABANDONED	01930554.9	4/18/01	N/A	1275229	3/21/07	4/18/21
6936-26-PEPDE	Data Allocation With Variable SNR Margins	DE	ABANDONED	01930554.9	4/18/01	N/A	1275229	3/21/07	4/18/21
6936-26-PEPFR	Data Allocation With Variable SNR Margins	FR	ABANDONED	01930554.9	4/18/01	N/A	1275229	3/21/07	4/18/21
6936-26-PEPGB	Data Allocation With Variable SNR Margins	GB	ABANDONED	01930554.9	4/18/01	N/A	1275229	3/21/07	4/18/21
6936-26-PEP-DIV	Data Allocation With Variable SNR Margins	EP	ISSUED	07005676.7	4/18/01	1830535	1830535	6/15/11	4/18/21
6936-26-PEP-DIV-BE	Data Allocation With Variable SNR Margins	BE	ISSUED	07005676.7	4/18/01	N/A	1830535	9/5/07	4/18/21
6936-26-PEP-DIV-DE	Data Allocation With Variable SNR Margins	DE	ISSUED	07005676.7	4/18/01		1830535	6/15/11	4/18/21
6936-26-PEP-DIV-FR	Data Allocation With Variable SNR Margins	FR	ISSUED	07005676.7	4/18/01	N/A	1830535	9/5/07	4/18/21
6936-26-PEP-DIV-GB	Data Allocation With Variable SNR Margins	GB	ISSUED	07005676.7	4/18/01	N/A	1830535	9/5/07	4/18/21
6936-26-PEP-DIV-2	MULTICARRIER MODULATION SYSTEM WITH VARIABLE MARGIN TO ACCOUNT FOR TIME VARYING IMPAIRMENTS	EP	ABANDONED	10011998.1	4/18/01	2267963			4/18/21
6936-26-PJP	MULTICARRIER MODULATION SYSTEM WITH VARIABLE MARGIN TO ACCOUNT FOR TIME VARYING IMPAIRMENTS	JP	ABANDONED	2001-576639	4/18/01	2004-501535			4/18/21
6936-26-PKR	MULTICARRIER MODULATION SYSTEM WITH VARIABLE MARGIN TO ACCOUNT FOR TIME VARYING IMPAIRMENTS	KR	ABANDONED	2002-7013983	4/18/01	10-2002-087990			4/18/21
6936-26-PROV	MULTICARRIER MODULATION SYSTEM WITH VARIABLE MARGIN TO ACCOUNT FOR TIME VARYING IMPAIRMENTS	US	EXPIRE D	60/197,727	4/18/00	N/A			4/18/01

6936-7-CON	MULTICARRIER COMMUNICATION WITH VARIABLE OVERHEAD RATE	US	ABANDONED	10/202,688	7/25/02	US 2003-0007509			7/13/06
6936-7-PAU	MULTICARRIER COMMUNICATION WITH VARIABLE OVERHEAD RATE	AU	EXPIRED	48339/99	6/25/99	AU 4833999	750898	11/21/02	6/25/19
6936-7-PAU-2	MULTICARRIER COMMUNICATION WITH VARIABLE OVERHEAD RATE	AU	EXPIRED	2002301627	6/25/99	AU 2002301627	2002301627	8/6/04	6/25/19
6936-7-PAU-3	MULTICARRIER COMMUNICATION WITH VARIABLE OVERHEAD RATE	AU	ABANDONED	2004203322	6/25/99	AU 2004203322	2004203322	10/11/07	5/4/17
6936-7-PAU-4	Multicarrier Communication With Variable Overhead Rate	AU	ABANDONED	2007202930	6/25/99	AU 2007202930			6/25/19
6936-7-PAU-4-DIV	Multicarrier Communication With Variable Overhead Rate	AU	ABANDONED	2010249199	6/25/99	AU 2010249199			6/25/19
6936-7-PCA	MULTICARRIER COMMUNICATION WITH VARIABLE OVERHEAD RATE	CA	ABANDONED	2,335,865	6/25/99	CA 2333865	2,335,865	12/16/08	3/10/17
6936-7-PCA-DIV	MULTICARRIER COMMUNICATION WITH VARIABLE OVERHEAD RATE	CA	EXPIRED	2,641,978	6/25/99	CA 2641978	2,641,978	1/6/15	6/25/19
6936-7-PCA-DIV-2	MULTICARRIER COMMUNICATION WITH VARIABLE OVERHEAD RATE	CA	EXPIRED	2,867,539	6/25/99		2,867,539	3/14/17	6/25/19
6936-7-PCT	MULTICARRIER COMMUNICATION WITH VARIABLE OVERHEAD RATE	WO	NAT PHASE	PCT/US99/14467	6/25/99	WO 2000/001127			
6936-7-PEP-2	MULTICARRIER COMMUNICATION WITH VARIABLE OVERHEAD RATE	EP	EXPIRED	04012683.1	6/25/99	1453268	1453268	3/8/06	6/25/19
6936-7-PEPAT-2	MULTICARRIER COMMUNICATION WITH VARIABLE OVERHEAD RATE	AT	EXPIRED	04012683.1	6/25/99	N/A	1453268	3/8/06	6/25/19
6936-7-PEPBE-2	MULTICARRIER COMMUNICATION WITH VARIABLE OVERHEAD RATE	BE	EXPIRED	04012683.1	6/25/99	N/A	1453268	3/8/06	6/25/19
6936-7-PEPCH-2	MULTICARRIER COMMUNICATION WITH VARIABLE OVERHEAD RATE	CH	EXPIRED	04012683.1	6/25/99	N/A	1453268	3/8/06	6/25/19
6936-7-PEPDE-2	Multicarrier Communication With Variable Overhead Rate	DE	EXPIRED	04012683.1	6/25/99	N/A	1453268	3/8/06	6/25/19
6936-7-PEPES-2	MULTICARRIER COMMUNICATION WITH VARIABLE OVERHEAD RATE	ES	EXPIRED	04012683.1	6/25/99	N/A	1453268	3/8/06	6/25/19
6936-7-PEPFI-2	MULTICARRIER COMMUNICATION WITH VARIABLE OVERHEAD RATE	FI	EXPIRED	04012683.1	6/25/99	N/A	1453268	3/8/06	6/25/19
6936-7-PEPFR-2	MULTICARRIER COMMUNICATION WITH VARIABLE OVERHEAD RATE	FR	EXPIRED	04012683.1	6/25/99	N/A	1453268	3/8/06	6/25/19
6936-7-PEPGB-2	MULTICARRIER COMMUNICATION WITH VARIABLE OVERHEAD RATE	GB	EXPIRED	04012683.1	6/25/99	N/A	1453268	3/8/06	6/25/19
6936-7-PEPGR-2	MULTICARRIER COMMUNICATION WITH VARIABLE OVERHEAD RATE	GR	EXPIRED	04012683.1	6/25/99	N/A	1453268	3/8/06	6/25/19
6936-7-PEPHK-2	MULTICARRIER COMMUNICATION WITH VARIABLE OVERHEAD RATE	HK	EXPIRED	05101665.7	6/25/99	HK 1068080	HK1068080	5/6/06	6/25/19
6936-7-PEPIE-2	MULTICARRIER COMMUNICATION WITH VARIABLE OVERHEAD RATE	IE	EXPIRED	04012683.1	6/25/99	N/A	1453268	3/8/06	6/25/19
6936-7-PEPIT-2	MULTICARRIER COMMUNICATION WITH VARIABLE OVERHEAD RATE	IT	EXPIRED	04012683.1	6/25/99	N/A	1453268	3/8/06	6/25/19
6936-7-PEPNL-2	MULTICARRIER COMMUNICATION WITH VARIABLE OVERHEAD RATE	NL	EXPIRED	04012683.1	6/25/99	N/A	1453268	3/8/06	6/25/19
6936-7-PEPS-2	MULTICARRIER COMMUNICATION WITH VARIABLE OVERHEAD RATE	SE	EXPIRED	04012683.1	6/25/99	N/A	1453268	3/8/06	6/25/19
6936-7-PEP-3	MULTICARRIER COMMUNICATION WITH VARIABLE OVERHEAD RATE	EP	EXPIRED	06004566.3	6/25/99	EP 1667392	1667392	1/10/18	6/25/19
6936-7-PEP-3-DE	MULTICARRIER COMMUNICATION WITH VARIABLE OVERHEAD RATE	DE	EXPIRED	06004566.3	6/25/99		1667392	1/10/18	6/25/19
6936-7-PEP-3-FR	MULTICARRIER COMMUNICATION WITH VARIABLE OVERHEAD RATE	FR	EXPIRED	06004566.3	6/25/99		1667392	1/10/18	6/25/19
6936-7-PEP-3-GB	MULTICARRIER COMMUNICATION WITH VARIABLE OVERHEAD RATE	GB	EXPIRED	06004566.3	6/25/99		1667392	1/10/18	6/25/19
6936-7-PEP-3-HK	MULTICARRIER COMMUNICATION WITH VARIABLE OVERHEAD RATE	HK	EXPIRED	06112790.1	6/25/99	1091070	HK1091070	6/22/18	6/25/19
6936-7-PEP-3-DIV-1	MULTICARRIER COMMUNICATION WITH VARIABLE OVERHEAD RATE	EP	EXPIRED	10011974.2	6/25/99	2278765	2278765	11/7/18	6/25/19
6936-7-PEP-3-DIV-1-AT	MULTICARRIER COMMUNICATION WITH VARIABLE OVERHEAD RATE	AT	EXPIRED	10011974.2	6/25/99		2278765	11/7/18	6/25/19
6936-7-PEP-3-DIV-1-BE	MULTICARRIER COMMUNICATION WITH VARIABLE OVERHEAD RATE	BE	EXPIRED	10011974.2	6/25/99		2278765	11/7/18	6/25/19
6936-7-PEP-3-DIV-1-CH	MULTICARRIER COMMUNICATION WITH VARIABLE OVERHEAD RATE	CH	EXPIRED	10011974.2	6/25/99		2278765	11/7/18	6/25/19
6936-7-PEP-3-DIV-1-DE	MULTICARRIER COMMUNICATION WITH VARIABLE OVERHEAD RATE	DE	EXPIRED	10011974.2	6/25/99	2278765	DE 699 45 900.1	11/7/18	6/25/19
6936-7-PEP-3-DIV-1-ES	MULTICARRIER COMMUNICATION WITH VARIABLE OVERHEAD RATE	ES	EXPIRED	10011974.2	6/25/99		2278765	11/7/18	6/25/19
6936-7-PEP-3-DIV-1-FI	MULTICARRIER COMMUNICATION WITH VARIABLE OVERHEAD RATE	FI	EXPIRED	10011974.2	6/25/99		2278765	11/7/18	6/25/19
6936-7-PEP-3-DIV-1-FR	MULTICARRIER COMMUNICATION WITH VARIABLE OVERHEAD RATE	FR	EXPIRED	10011974.2	6/25/99		2278765	11/7/18	6/25/19
6936-7-PEP-3-DIV-1-GB	MULTICARRIER COMMUNICATION WITH VARIABLE OVERHEAD RATE	GB	EXPIRED	10011974.2	6/25/99		2278765	11/7/18	6/25/19
6936-7-PEP-3-DIV-1-GR	MULTICARRIER COMMUNICATION WITH VARIABLE OVERHEAD RATE	GR	EXPIRED	10011974.2	6/25/99		2278765	11/7/18	6/25/19
6936-7-PEP-3-DIV-1-IE	MULTICARRIER COMMUNICATION WITH VARIABLE OVERHEAD RATE	IE	EXPIRED	10011974.2	6/25/99		2278765	11/7/18	6/25/19
6936-7-PEP-3-DIV-1-IT	MULTICARRIER COMMUNICATION WITH VARIABLE OVERHEAD RATE	IT	EXPIRED	10011974.2	6/25/99		2278765	11/7/18	6/25/19
6936-7-PEP-3-DIV-1-NL	MULTICARRIER COMMUNICATION WITH VARIABLE OVERHEAD RATE	NL	EXPIRED	10011974.2	6/25/99		2278765	11/7/18	6/25/19
6936-7-PEP-3-DIV-1-SE	MULTICARRIER COMMUNICATION WITH VARIABLE OVERHEAD RATE	SE	EXPIRED	10011974.2	6/25/99		2278765	11/7/18	6/25/19
6936-7-PEP-3-DIV-2	MULTICARRIER COMMUNICATION WITH VARIABLE OVERHEAD RATE	EP	EXPIRED	10011980.9	6/25/99	2278766	2278766	11/7/18	6/25/19
6936-7-PEP-3-DIV-2-DE	MULTICARRIER COMMUNICATION WITH VARIABLE OVERHEAD RATE	DE	EXPIRED	10011980.9	6/25/99	2278766	DE 699 45 902.8	11/7/18	6/25/19
6936-7-PEP-3-DIV-2-FR	MULTICARRIER COMMUNICATION WITH VARIABLE OVERHEAD RATE	FR	EXPIRED	10011980.9	6/25/99		2278766	11/7/18	6/25/19
6936-7-PEP-3-DIV-2-GB	MULTICARRIER COMMUNICATION WITH VARIABLE OVERHEAD RATE	GB	EXPIRED	10011980.9	6/25/99		2278766	11/7/18	6/25/19

6936-7-PEP-3-DIV-3	MULTICARRIER COMMUNICATION WITH VARIABLE OVERHEAD RATE	EP	EXPIRED	10011981.7	6/25/99	2278767	2278767	11/7/18	6/25/19
6936-7-PEP-3-DIV-3-DE	MULTICARRIER COMMUNICATION WITH VARIABLE OVERHEAD RATE	DE	EXPIRED	10011981.7	6/25/99	2278767	DE 699 45 903.6	11/7/18	6/25/19
6936-7-PEP-3-DIV-3-FR	MULTICARRIER COMMUNICATION WITH VARIABLE OVERHEAD RATE	FR	EXPIRED	10011981.7	6/25/99		2278767	11/7/18	6/25/19
6936-7-PEP-3-DIV-3-GB	MULTICARRIER COMMUNICATION WITH VARIABLE OVERHEAD RATE	GB	EXPIRED	10011981.7	6/25/99		2278767	11/7/18	6/25/19
6936-7-PKR	MULTICARRIER COMMUNICATION WITH VARIABLE OVERHEAD RATE	KR	ABANDONED	2000-7014830	6/25/99	10-2001-0053220	10-0955169	4/20/10	3/10/17
6936-7-PKR-2	MULTICARRIER COMMUNICATION WITH VARIABLE OVERHEAD RATE	KR	EXPIRED	10-2010-7002843	6/25/99	10-2010-0031635	10-1006609	12/30/10	6/25/19
6936-7-PKR-3	MULTICARRIER COMMUNICATION WITH VARIABLE OVERHEAD RATE	KR	ABANDONED	10-2010-7021589	6/25/99	10-2010-0121683			6/25/19
6936-7-PROV	MULTICARRIER COMMUNICATION WITH VARIABLE OVERHEAD RATE	US	EXPIRED	60/090,891	6/26/98	N/A			6/26/99
6936-3	SYSTEM AND METHOD FOR THE APPLICATION OF AN LMS METHOD TO UPDATING AN ECHO CANCELLER IN AN ADSL MODEM	US	ABANDONED	09/768,275	1/25/01	US 2001-0040875			8/25/05
6936-3-CON	SYSTEM AND METHOD FOR THE APPLICATION OF AN LMS METHOD TO UPDATING AN ECHO CANCELLER IN AN ADSL MODEM	US	ABANDONED	11/058,289	2/16/05	US 2005-0141441 A1			5/9/06
6936-3-CON-2	SYSTEM AND METHOD FOR THE APPLICATION OF AN LMS METHOD TO UPDATING AN ECHO CANCELLER IN AN ADSL MODEM	US	ABANDONED	11/430,251	5/9/06	US 2006-0215587 A1			12/10/10
6936-3-CON-3	SYSTEM AND METHOD FOR THE APPLICATION OF AN LMS METHOD TO UPDATING AN ECHO CANCELLER IN AN ADSL MODEM	US	ISSUED	12/783,740	5/20/10	US 2010-0296663 A1	8,391,191	3/3/13	1/29/21
6936-3-CON-4	SYSTEM AND METHOD FOR THE APPLICATION OF AN LMS METHOD TO UPDATING AN ECHO CANCELLER IN AN ADSL MODEM	US	ABANDONED	12/783,744	5/20/10	N/A			2/18/11
6936-3-CON-5	SYSTEM AND METHOD FOR THE APPLICATION OF AN LMS METHOD TO UPDATING AN ECHO CANCELLER IN AN ADSL MODEM	US	ISSUED	13/772,516	2/21/13	US 2013-0163749 A1	8,649,305	2/11/14	1/25/21
6936-3-CON-6	System and Method for the Application of an LMS Method to Updating an Echo Canceller in an ADSL Modem	US	ISSUED	14/164,632	1/27/14	US 2014-0140499 A1	9,065,886	6/23/15	1/25/21
6936-3-CON-7	SYSTEM AND METHOD FOR THE APPLICATION OF AN LMS METHOD TO UPDATING AN ECHO CANCELLER IN A MULTICARRIER TRANSCIVER	US	ABANDONED	14/724,345	5/28/15	US 2015-0288808 A1			11/4/16
6936-3-PAU	SYSTEM AND METHOD FOR THE APPLICATION OF AN LMS METHOD TO UPDATING AN ECHO CANCELLER COEFFICIENTS IN AN ADSL MODEM	AU	ABANDONED	32943/01	1/25/01	AU 3294301	783527	2/16/06	1/4/17
6936-3-PCA	System and Method for the Application of an LMS Method to Updating an Echo Canceller in an ADSL Modem	CA	ABANDONED	2,396,162	1/25/01	CA 2396162			4/25/12
6936-3-PCT	APPLICATION OF LMS METHOD TO UPDATING ECHO CANCELLER COEFFICIENTS IN ADSL MODEM	WO	NAT PHASE	PCT/US01/02341	1/25/01	WO 2001/056184			
6936-3-PEP	APPLICATION OF LMS METHOD TO UPDATING ECHO CANCELLER COEFFICIENTS IN ADSL MODEM	EP	ABANDONED	01905022.8	1/25/01	EP 1250766	1250766	9/17/08	12/12/19
6936-3-PEP-BE	APPLICATION OF LMS METHOD TO UPDATING ECHO CANCELLER COEFFICIENTS IN ADSL MODEM	BE	ABANDONED	01905022.8	1/25/01	N/A	1250766	9/17/08	12/12/19
6936-3-PEP-DE	APPLICATION OF LMS METHOD TO UPDATING ECHO CANCELLER COEFFICIENTS IN ADSL MODEM	DE	ABANDONED	01905022.8	1/25/01	N/A	1250766	9/17/08	12/12/19
6936-3-PEP-FR	APPLICATION OF LMS METHOD TO UPDATING ECHO CANCELLER COEFFICIENTS IN ADSL MODEM	FR	ABANDONED	01905022.8	1/25/01	N/A	1250766	9/17/08	12/12/19
6936-3-PEP-GB	APPLICATION OF LMS METHOD TO UPDATING ECHO CANCELLER COEFFICIENTS IN ADSL MODEM	GB	ABANDONED	01905022.8	1/25/01	N/A	1250766	9/17/08	12/12/19
6936-3-PEP-DIV	System and Method for the Application of an LMS Method to Updating an Echo Canceller in an ADSL Modem	EP	ABANDONED	08015818.1	1/25/01	1 993 884			1/25/21
6936-3-PEP-DIV-2	System and Method for the Application of an LMS Method to Updating an Echo Canceller in an ADSL Modem	EP	ABANDONED	10011999.9	1/25/01	2267913			1/25/21
6936-3-PIP	APPLICATION OF LMS METHOD TO UPDATING ECHO CANCELLER COEFFICIENTS IN ADSL MODEM	JP	ABANDONED	2001-555226	1/25/01	JP 2003-521194			1/25/21
6936-3-PKR	APPLICATION OF LMS METHOD TO UPDATING ECHO CANCELLER COEFFICIENTS IN ADSL MODEM	KR	ABANDONED	2002-7009465	1/25/01	10-2002-0069265			1/25/21
6936-3-PKR-DIV	APPLICATION OF LMS METHOD TO UPDATING ECHO CANCELLER COEFFICIENTS IN ADSL MODEM	KR	ABANDONED	10-2010-7006184	1/25/01	10-2010-0034063			1/25/21
6936-3-PROV	APPLICATION OF LMS METHOD TO UPDATING ECHO CANCELLER COEFFICIENTS IN ADSL MODEM	US	EXPIRED	60/177,944	1/25/00	N/A			1/25/01

6936-14	SYSTEMS AND METHODS FOR MULTICARRIER MODULATION USING MULTI-TAP FREQUENCY-DOMAIN EQUALIZER AND DECISION FEEDBACK	US	ISSUED	10/211,425	8/2/02	US 2003-0067865	6,760,373	7/6/04	8/2/22
6936-14-CDN	SYSTEMS AND METHODS FOR MULTICARRIER MODULATION USING MULTI-TAP FREQUENCY-DOMAIN EQUALIZER AND DECISION FEEDBACK	US	ABANDONED	10/834,193	4/29/04	US 2004-0202239			8/2/22
6936-14-CDN-2	Systems and Methods for Multicarrier Modulation Using Multi-Tap Frequency-Domain Equalizer and Decision Feedback	US	ISSUED	11/964,409	12/26/07	US 2008-0101452 A1	7,656,976	2/2/10	8/2/22
6936-14-CDN-3	SYSTEMS AND METHODS FOR MULTICARRIER MODULATION USING MULTI-TAP FREQUENCY-DOMAIN EQUALIZER AND DECISION FEEDBACK	US	ABANDONED	12/640,838	12/17/09	US 2010-0098149 A1			9/23/11
6936-14-CDN-4	SYSTEMS AND METHODS FOR MULTICARRIER MODULATION USING MULTI-TAP FREQUENCY-DOMAIN EQUALIZER AND DECISION FEEDBACK	US	ABANDONED	12/783,796	5/20/10	US 2010-0296570 A1			3/2/11
6936-14-CDN-5	SYSTEMS AND METHODS FOR MULTICARRIER MODULATION USING MULTI-TAP FREQUENCY-DOMAIN EQUALIZER AND DECISION FEEDBACK	US	ABANDONED	12/783,801	5/20/10	N/A			2/18/11
6936-14-PCT	SYSTEMS AND METHOD FOR MULTICARRIER MODULATION USING MULTI-TAP FREQUENCY-DOMAIN EQUALIZER AND DECISION FEEDBACK	WO	NAT PHASE	PCT/US02/24326	8/2/02	WO 2003/012990			
6936-14-PROV	MULTICARRIER MODULATION METHOD USING MULTI-TAP FREQUENCY-DOMAIN EQUALIZATION AND DECISION FEEDBACK	US	EXPIRED	60/309,631	8/2/01	N/A			8/2/02
6936-19	MULTI-CARRIER TRANSMITTER	US	EXPIRED	08/105,796	8/12/93	N/A	5,497,398	3/5/96	8/12/13
6936-19-PCT	MULTI-CARRIER TRANSMITTER	WO	NAT PHASE	PCT/US94/06713	6/13/94	WO 1995/005711			
6936-21	SYSTEMS AND METHODS FOR IMPLEMENTING RECEIVER TRANSPARENT Q-MODE	US	ISSUED	10/106,329	3/27/02	US 2002/0196861	6,731,695	5/4/04	3/27/21
6936-21-CDN	SYSTEMS AND METHODS FOR IMPLEMENTING RECEIVER TRANSPARENT Q-MODE	US	ABANDONED	10/802,867	3/18/04	US 2004-0184552 A1			11/10/05
6936-21-CDN-2	SYSTEMS AND METHODS FOR IMPLEMENTING RECEIVER TRANSPARENT Q-MODE	US	ABANDONED	11/200,002	8/10/05	US 2006-0039490 A1			8/7/06
6936-21-CDN-3	SYSTEMS AND METHODS FOR IMPLEMENTING RECEIVER TRANSPARENT Q-MODE	US	ABANDONED	11/434,249	5/16/06	US 2006-0203927 A1			3/27/22
6936-21-CDN-4	SYSTEMS AND METHODS FOR IMPLEMENTING RECEIVER TRANSPARENT Q-MODE	US	ISSUED	11/674,871	2/14/07	US 2007-0147540 A1	7,558,329	7/7/09	3/27/22
6936-21-CDN-5	Systems and Methods for Implementing Receiver Transparent Q-Mode	US	ABANDONED	12/478,577	6/4/09	US 2009-0290620 A1			7/25/11
6936-21-CDN-6	Systems and Methods for Implementing Receiver Transparent Q-Mode	US	ISSUED	12/783,749	5/20/10	US 2010-0290558 A1	8,335,271	12/18/12	3/27/22
6936-21-CDN-7	Systems and Methods for Implementing Receiver Transparent Q-Mode	US	ABANDONED	12/783,755	5/20/10	US 2010-0296604 A1			3/27/22
6936-21-CDN-8	Systems and Methods for Implementing Receiver Transparent Q-Mode	US	ISSUED	13/693,394	12/4/12	US 2013-0094608 A1	8,792,574	7/29/14	3/27/22
6936-21-CDN-9	RANDOMIZATION USING AN XOR SCRAMBLER IN MULTICARRIER COMMUNICATIONS	US	ISSUED	14/308,934	6/19/14	US 2014-0294116 A1	9,191,039	11/17/15	3/27/22
6936-21-CDN-10	SYSTEMS AND METHODS FOR IMPLEMENTING RECEIVER TRANSPARENT Q-MODE	US	ABANDONED	14/932,599	11/4/15	US 2016-0056857 A1			11/14/17
6936-21-CDN-11	SYSTEMS AND METHODS FOR IMPLEMENTING RECEIVER TRANSPARENT Q-MODE	US	ISSUED	15/812,705	11/14/17	US 2018-0068590 A1	10,419,059	9/17/19	3/27/22
6936-21-PAU	RECEIVER TRANSPARENT Q-MODE	AU	ABANDONED	2002248711	3/27/02	AU 2002248711			1/4/05
6936-21-PCA	RECEIVER TRANSPARENT Q-MODE	CA	ABANDONED	2,439,804	3/27/02	CA 2439804			
6936-21-PCT	RECEIVER TRANSPARENT Q-MODE	WO	NAT PHASE	PCT/US02/09411	3/27/02	WO02/078244			
6936-21-PEP	RECEIVER TRANSPARENT Q-MODE	EP	ABANDONED	02717728.6	3/27/02	EP1374469			11/2/04
6936-21-PPP	RECEIVER TRANSPARENT Q-MODE	JP	ABANDONED	2002-576356	3/27/02	JP 2004-538676			3/10/05
6936-21-PRR	RECEIVER TRANSPARENT Q-MODE	KR	ABANDONED	2003-7012442	3/27/02	10-2004-0004562			
6936-21-PROV-1	RECEIVER TRANSPARENT Q-MODE	US	EXPIRED	60/278,936	3/27/01	N/A			3/27/02
6936-21-PROV-2	RECEIVER TRANSPARENT Q-MODE WITH ON-LINE RECONFIGURATION	US	EXPIRED	60/283,467	4/12/01	N/A			4/12/02
6936-21-PROV-3	RECEIVER TRANSPARENT Q-MODE WITH ON-LINE RECONFIGURATION AND SCRAMBLING	US	EXPIRED	60/287,968	5/1/01	N/A			5/1/02
6936-21-PROV-4	RECEIVER TRANSPARENT Q-MODE WITH ON-LINE RECONFIGURATION, SCRAMBLING AND Q-MODE SYMBOL DISTORTION	US	EXPIRED	60/293,034	5/23/01	N/A			5/23/02
6936-22	MULTI-CARRIER TRANSMISSION SYSTEM ADAPTED FOR PACKET DATA TRANSFER	US	EXPIRED	08/670,245	6/19/96	N/A	5,751,716	5/12/98	6/19/16
6936-22-PCT	MULTI-CARRIER TRANSMISSION SYSTEM ADAPTED FOR PACKET DATA TRANSFER	WO	NAT PHASE	PCT/US97/08736	5/17/97	WO 1997/049208			
6936-22-PEP	MULTI-CARRIER TRANSMISSION SYSTEM ADAPTED FOR PACKET DATA TRANSFER	EP	ABANDONED	57925713.6	5/17/97	N/A			9/5/00

6936-23	SYSTEMS AND METHODS THAT PROVIDE FREQUENCY DOMAIN SUPPLEMENTAL TRAINING OF THE TIME DOMAIN EQUALIZER FOR DMT	US	ISSUED	09/982,065	10/19/01	US 2002-0057734	7,180,938	2/20/07	10/14/23
6936-23-CDN	Systems and Methods That Provide Frequency Domain Supplemental Training of the Time Domain Equalizer for DMT	US	ABANDONED	11/616,630	12/27/06	US 2007-0104262			10/19/21
6936-23-CDN-2	Systems and Methods That Provide Frequency Domain Supplemental Training of the Time Domain Equalizer for DMT	US	ABANDONED	12/013,874	1/14/08	US 2008-0107164 A1	7,636,389	12/22/09	3/14/17
6936-23-CDN-3	Systems and Methods That Provide Frequency Domain Supplemental Training of the Time Domain Equalizer for DMT	US	ABANDONED	12/615,077	11/9/09	US 2010-0054321 A1			2/28/11
6936-23-CDN-4	Systems and Methods That Provide Frequency Domain Supplemental Training of the Time Domain Equalizer for DMT	US	ISSUED	12/783,783	5/20/10	US 2010-0290514 A1	8,102,909	1/24/12	10/19/21
6936-23-CDN-5	Systems and Methods That Provide Frequency Domain Supplemental Training of the Time Domain Equalizer for DMT	US	ABANDONED	12/783,788	5/20/10	N/A			2/17/11
6936-23-CDN-6	Systems and Methods That Provide Frequency Domain Supplemental Training of the Time Domain Equalizer for DMT	US	ABANDONED	13/330,943	12/20/11	US 2012-0087399 A1			9/19/13
6936-23-PCT	SYSTEMS AND METHODS THAT PROVIDE FREQUENCY DOMAIN SUPPLEMENTAL TRAINING OF THE TIME DOMAIN EQUALIZER FOR DMT	WO	NAT PHASE	PCT/US01/32503	10/19/01	WO 2002/038926			
6936-23-PROV	FREQUENCY DOMAIN SUPPLEMENTAL TRAINING OF THE TIME DOMAIN EQUALIZER FOR DMT	US	EXPIRED	60/241,664	10/19/00	N/A			10/19/01
6936-24	MULTICARRIER TRANSMISSION SYSTEM	US	EXPIRED	08/340,747	11/16/94	N/A	5,636,246	6/3/97	11/16/14
6936-24-PAU	MULTICARRIER TRANSMISSION SYSTEM	AU	EXPIRED	41666/96	11/17/95	AU 4166696	708318	11/11/99	11/17/15
6936-24-PCT	MULTICARRIER TRANSMISSION SYSTEM	WO	NAT PHASE	PCT/US95/15115	11/17/95	WO 1997/026711			
6936-24-PGB	MULTICARRIER TRANSMISSION SYSTEM	GB	EXPIRED	9709849.5	11/17/95	GB 2320401	2320401	4/12/00	11/17/15
6936-25	BIT ALLOCATION AMONG CARRIERS IN MULTICARRIER COMMUNICATIONS	US	EXPIRED	09/600,971	7/20/00	N/A	6,870,888	3/22/05	11/23/19
6936-25-PAU	ALLOCATION OF COMMUNICATION BITS AMONG CARRIERS IN MULTICARRIER COMMUNICATIONS	AU	ABANDONED	18292/00	11/23/99	AU 1829200	754597	3/6/03	11/22/16
6936-25-PAU-2	ALLOCATION OF COMMUNICATION BITS AMONG CARRIERS IN MULTICARRIER COMMUNICATIONS	AU	ABANDONED	2002302029	11/18/02	AU 2002302029			11/19/03
6936-25-PCA	ALLOCATION OF COMMUNICATION BITS AMONG CARRIERS IN MULTICARRIER COMMUNICATIONS	CA	ABANDONED	2,350,916	11/23/99	CA 2350916	2,350,916	11/20/07	9/25/17
6936-25-PCA-DIV	Bit Allocation Among Carriers in Multicarrier Communications	CA	EXPIRED	2,599,805	11/23/99	CA 2599805	2,599,805	9/29/09	11/23/19
6936-25-PCT	ALLOCATION OF COMMUNICATION BITS AMONG CARRIERS IN MULTICARRIER COMMUNICATIONS	WO	NAT PHASE	PCT/US99/27798	11/23/99	WO 2000/031940			
6936-25-PEP	ALLOCATION OF COMMUNICATION BITS AMONG CARRIERS IN MULTICARRIER COMMUNICATIONS	EP	EXPIRED	99961782.2	11/23/99	1133858	1133838	6/30/04	11/23/19
6936-25-PEPGB	ALLOCATION OF COMMUNICATION BITS AMONG CARRIERS IN MULTICARRIER COMMUNICATIONS	GB	EXPIRED	99961782.2	11/23/99	N/A	1133838	6/30/04	11/23/19
6936-25-PEP-2	ALLOCATION OF COMMUNICATION BITS AMONG CARRIERS IN MULTICARRIER COMMUNICATIONS	EP	ABANDONED	04012682.3	11/23/99	1453267			11/23/19
6936-25-PEP-2-DIV-1	ALLOCATION OF COMMUNICATION BITS AMONG CARRIERS IN MULTICARRIER COMMUNICATIONS	EP	ABANDONED	10011993.2	11/23/99	2264932			11/23/19
6936-25-PJP	ALLOCATION OF COMMUNICATION BITS AMONG CARRIERS IN MULTICARRIER COMMUNICATIONS	JP	ABANDONED	2000-584658	11/23/99	2002-531010			11/23/19
6936-25-PJP-DIV	ALLOCATION OF COMMUNICATION BITS AMONG CARRIERS IN MULTICARRIER COMMUNICATIONS	JP	ABANDONED	2010-56580	11/23/99	2010-141931			11/23/19
6936-25-PKR	ALLOCATION OF COMMUNICATION BITS AMONG CARRIERS IN MULTICARRIER COMMUNICATIONS	KR	ABANDONED	2001-7006580	11/23/99	10-2001-0101081			11/23/19
6936-25-PROV	ALLOCATION OF COMMUNICATION BITS AMONG CARRIERS IN MULTICARRIER COMMUNICATIONS	US	EXPIRED	60/109,876	11/25/98	N/A			11/25/99
6936-30	MULTI-TAP FREQUENCY DOMAIN EQUALIZATION WITH DECISION FEEDBACK AND TRELLIS DECODING	US	ABANDONED	10/631,745	8/1/03	US 2004-0096008 A1			8/1/23
6936-30-DIV	MULTI-TAP FREQUENCY DOMAIN EQUALIZATION WITH DECISION FEEDBACK AND TRELLIS DECODING	US	ABANDONED	11/748,806	5/15/07	US 2007-0211812			6/20/11
6936-30-DIV-CON	MULTI-TAP FREQUENCY DOMAIN EQUALIZATION WITH DECISION FEEDBACK AND TRELLIS DECODING	US	ABANDONED	12/783,733	5/20/10	US 2010-0293442 A1			2/25/13
6936-30-DIV-CON-2	MULTI-TAP FREQUENCY DOMAIN EQUALIZATION WITH DECISION FEEDBACK AND TRELLIS DECODING	US	ABANDONED	12/783,737	5/20/10	US 2010-0295882 A1			2/25/13

6936-30-PCT	COMBINED MULTI-TAP FREQUENCY DOMAIN EQUALIZATION WITH DECISION FEEDBACK AND TRELLIS DECODING	WO	NAT PHASE	PCT/US03/23965	8/1/03	WO 2004/014032 A3			
6936-30-PROV	COMBINED MULTI-TAP FREQUENCY DOMAIN EQUALIZATION WITH DECISION FEEDBACK AND TRELLIS DECODING	US	EXPIRED	60/400,550	8/1/02	N/A			8/1/03
6936-36	A SYSTEM AND METHOD FOR TRANSMITTING MESSAGES BETWEEN TRANSCEIVERS USING ELECTROMAGNETICALLY COUPLED SIGNALS	US	ISSUED	09/616,954	7/14/00	N/A	6,748,016	6/8/04	7/5/22
6936-36-CDN	SYSTEM AND METHOD FOR TRANSMITTING MESSAGES BETWEEN TRANSCEIVERS USING ELECTROMAGNETICALLY COUPLED SIGNALS	US	ABANDONED	10/743,946	12/24/03	US 2004-0136463 A1			8/27/04
6936-36-PAU	A SYSTEM AND METHOD FOR TRANSMITTING MESSAGES BETWEEN TRANSCEIVERS USING ELECTROMAGNETICALLY COUPLED SIGNALS	AU	ABANDONED	59347/00	7/14/00				1/13/05
6936-36-PCA	A SYSTEM AND METHOD FOR TRANSMITTING MESSAGES BETWEEN TRANSCEIVERS USING ELECTROMAGNETICALLY COUPLED SIGNALS	CA	ABANDONED	2378046	7/14/00				1/13/05
6936-36-PCT	A SYSTEM AND METHOD FOR TRANSMITTING MESSAGES BETWEEN TRANSCEIVERS USING ELECTROMAGNETICALLY COUPLED SIGNALS	WO	NAT PHASE	PCT/US00/19247	7/14/00				
6936-36-PEP	A SYSTEM AND METHOD FOR TRANSMITTING MESSAGES BETWEEN TRANSCEIVERS USING ELECTROMAGNETICALLY COUPLED SIGNALS	EP	ABANDONED	00945396.0	7/14/00				1/13/05
6936-36-PJP	A SYSTEM AND METHOD FOR TRANSMITTING MESSAGES BETWEEN TRANSCEIVERS USING ELECTROMAGNETICALLY COUPLED SIGNALS	JP	ABANDONED	2001-511007	7/14/00				1/13/05
6936-36-PKR	A SYSTEM AND METHOD FOR TRANSMITTING MESSAGES BETWEEN TRANSCEIVERS USING ELECTROMAGNETICALLY COUPLED SIGNALS	KR	ABANDONED	7000562/2002	7/14/00				1/13/05
6936-36-PROV	A SYSTEM AND METHOD FOR TRANSMITTING MESSAGES BETWEEN TRANSCEIVERS USING ELECTROMAGNETICALLY COUPLED SIGNALS	US	EXPIRED	60/144,562	7/16/99	N/A			7/16/00
6936-41	MULTI-CARRIER TRANSMISSION SYSTEM UTILIZING CHANNELS WITH DIFFERENT ERROR RATES	US	EXPIRED	08/661,974	6/12/96	N/A	5,832,090	11/3/98	6/12/16
6936-41-PCT	MULTI-CARRIER TRANSMISSION SYSTEM UTILIZING CHANNELS WITH DIFFERENT ERROR RATES	WO	NAT PHASE	PCT/US97/08222	5/17/97	WO 1997/48204			
6936-45	SINGLE SIDE-BAND MODULATION SYSTEM FOR USE IN DIGITALLY IMPLEMENTED MULTICARRIER TRANSMISSION SYSTEMS	US	EXPIRED	08/591,831	1/25/96	N/A	5,631,610	5/20/97	1/25/16
6936-45-PAU	SINGLE SIDE-BAND MODULATION SYSTEM FOR USE IN DIGITALLY IMPLEMENTED MULTICARRIER TRANSMISSION SYSTEMS	AU	EXPIRED	31342/97	5/17/97	AU 3134297	738201	1/3/02	5/17/17
6936-45-PCA	SINGLE SIDE-BAND MODULATION SYSTEM FOR USE IN DIGITALLY IMPLEMENTED MULTICARRIER TRANSMISSION SYSTEMS	CA	ABANDONED	2289537	5/17/97				7/12/04
6936-45-PCT	SINGLE SIDE-BAND MODULATION SYSTEM FOR USE IN DIGITALLY IMPLEMENTED MULTICARRIER TRANSMISSION SYSTEMS	WO	NAT PHASE	PCT/US97/08549	5/17/97	WO 1998/053552			
6936-45-PEP	SINGLE SIDE-BAND MODULATION SYSTEM FOR USE IN DIGITALLY IMPLEMENTED MULTICARRIER TRANSMISSION SYSTEMS	EP	ABANDONED	97926623.6	5/17/97				3/27/03
6936-45-PJP	SINGLE SIDE-BAND MODULATION SYSTEM FOR USE IN DIGITALLY IMPLEMENTED MULTICARRIER TRANSMISSION SYSTEMS	JP	ABANDONED	10-550313	5/17/97				5/6/04
6936-46	METHOD FOR PARTIALLY MODULATING AND DEMODULATING DATA IN A MULTICARRIER TRANSMISSION SYSTEM	US	EXPIRED	08/668,575	6/20/96	N/A	5,715,280	2/3/98	6/20/16
6936-46-PAU	METHOD FOR PARTIALLY MODULATING AND DEMODULATING DATA IN A MULTICARRIER TRANSMISSION SYSTEM	AU	EXPIRED	30673/97	5/17/97	AU 3067397	743020	5/2/02	5/17/17
6936-46-PCA	METHOD FOR PARTIALLY MODULATING AND DEMODULATING DATA IN A MULTICARRIER TRANSMISSION SYSTEM	CA	ABANDONED	2289529	5/17/97				6/17/03

6936-46-PCT	METHOD FOR PARTIALLY MODULATING AND DEMODULATING DATA IN A MULTICARRIER TRANSMISSION SYSTEM	WO	NAT PHASE	PCT/US97/08209	5/17/97	WO 1998/053572			
6936-46-PEP	METHOD FOR PARTIALLY MODULATING AND DEMODULATING DATA IN A MULTICARRIER TRANSMISSION SYSTEM	EP	ABANDONED	97925573.4	5/17/97				4/16/03
6936-46-PJP	METHOD FOR PARTIALLY MODULATING AND DEMODULATING DATA IN A MULTICARRIER TRANSMISSION SYSTEM	JP	ABANDONED	10-550306	5/17/97				5/13/04
6936-48	INTELLIGENT RATE OPTION DETERMINATION METHOD APPLIED TO ADSL TRANSCIVER	US	ISSUED	09/738,785	12/15/00	US 2001-0030998 A1	6,801,570	10/5/04	12/15/20
6936-48-PROV	INTELLIGENT RATE OPTION DETERMINATION METHOD APPLIED TO ADSL TRANSCIVER	US	EXPIRED	60/172,343	12/16/99	N/A			12/16/00
6936-50	SYSTEMS AND METHODS FOR LDPC CODED MODULATION	US	ABANDONED	09/882,046	6/18/01	US 2002-0042899			5/31/05
6936-50-DIV	SYSTEMS AND METHODS FOR LDPC CODED MODULATION	US	ABANDONED	11/140,246	5/31/05	US 2005-0229088 A1			6/18/21
6936-50-DIV-2	SYSTEMS AND METHODS FOR LDPC CODED MODULATION	US	ABANDONED	12/383,056	3/19/09	US 2009-0183048 A1			4/20/16
6936-50-DIV-2-CON	SYSTEMS AND METHODS FOR LDPC CODED MODULATION	US	ABANDONED	12/783,825	5/20/10	US 2010-0295573 A1			5/30/11
6936-50-DIV-2-CON-2	Systems and Methods for LDPC Coded Modulation	US	ABANDONED	12/783,839	5/20/10	US 2010-0295574 A1			6/1/11
6936-50-DIV-3	SYSTEMS AND METHODS FOR LDPC CODED MODULATION	US	ABANDONED	15/077,506	3/22/16	US 2016-0204901 A1			1/13/17
6936-50-PAU	SYSTEMS AND METHODS FOR LDPC CODED MODULATION	AU	ABANDONED	2001267096	6/18/01	AU 2001267096			3/28/06
6936-50-PCA	SYSTEMS AND METHODS FOR LDPC CODED MODULATION	CA	ABANDONED	2,409,179	6/18/01	CA 2409179			2/24/11
6936-50-PCT	SYSTEMS AND METHODS FOR LDPC CODED MODULATION	WO	NAT PHASE	PCT/US01/41015	6/18/01	WO 2001/097387			
6936-50-PEP	SYSTEMS AND METHODS FOR LDPC CODED MODULATION	EP	ABANDONED	01944712.7	6/18/01	EP 1290802			
6936-50-PJP	SYSTEMS AND METHODS FOR LDPC CODED MODULATION	JP	ABANDONED	2002-511477	6/18/01	2004-503979			10/27/11
6936-50-PKR	SYSTEMS AND METHODS FOR LDPC CODED MODULATION	KR	ABANDONED	2002-7017148	6/18/01	10-2003-0036227			6/18/21
6936-50-PKR-DIV	SYSTEMS AND METHODS FOR LDPC CODED MODULATION	KR	ABANDONED	10-2010-7006498	6/18/01	10-2010-00469063			6/18/21
6936-50-PROV	LDPC CODED MODULATION LOW DENSITY PARITY CHECK (LDPC)	US	EXPIRED	60/212,233	6/16/00	N/A			6/16/01
6936-50-PROV-2	CODED MODULATION FOR ADSL	US	EXPIRED	60/241,468	10/18/00	N/A			10/18/01
6936-60-PCA	Stable Low Power Mode for Multicarrier Transceivers	CA	ABANDONED	2,706,362	11/21/08	CA 2706362			12/21/16
6936-60-PCN	Stable Low Power Mode for Multicarrier Transceivers	CN	ABANDONED	200880117277.5	11/21/08	CN101868951A	ZL200880117277.5	9/7/16	9/20/17
6936-60-PCN-DIV	Stable Low Power Mode for Multicarrier Transceivers	CN	ABANDONED	201310088357.5	11/21/08	CN103227767	ZL201310088357.5	4/12/17	9/20/17
6936-60-PCN-HK	Stable Low Power Mode for Multicarrier Transceivers	HK	ABANDONED	10110838.3	11/21/08	HK1144345			12/12/16
6936-60-PCT	Stable Low Power Mode for Multicarrier Transceivers	WO	NAT PHASE	PCT/US08/84322	11/21/08	WO 2009/067633			
6936-60-PEP	Stable Low Power Mode for Multicarrier Transceivers	EP	ABANDONED	08852660.3	11/21/08	EP 2223489	2223489	4/20/16	7/6/17
6936-60-PEP-DE	Stable Low Power Mode for Multicarrier Transceivers	DE	ABANDONED	08852660.3	11/21/08		2223489	4/20/16	7/6/17
6936-60-PEP-FR	Stable Low Power Mode for Multicarrier Transceivers	FR	ABANDONED	08852660.3	11/21/08		2223489	4/20/16	7/6/17
6936-60-PEP-GB	Stable Low Power Mode for Multicarrier Transceivers	GB	ABANDONED	08852660.3	11/21/08		2223489	4/20/16	7/6/17
6936-60-PEPHK	Stable Low Power Mode for Multicarrier Transceivers	HK	ABANDONED	10109672.4	11/21/08	HK 1143261			2/11/16
6936-60-PIN	Stable Low Power Mode for Multicarrier Transceivers	IN	ABANDONED	1800/KOLNP/2010	11/21/08				11/21/28
6936-60-PJP	Stable Low Power Mode for Multicarrier Transceivers	JP	ABANDONED	2010-535086	11/21/08	2011-504709			11/21/28
6936-60-PROV	Stable Low Power Mode for Multicarrier Transceivers	US	EXPIRED	60/989,542	11/21/07	N/A			11/21/08
6936-60-PUS	Stable Low Power Mode for Multicarrier Transceivers	US	ISSUED	12/739,330	8/12/10	US 2010-0296555 A1	8,837,610	9/16/14	6/24/29
6936-60-PUS-CON	Stable Low Power Mode for Multicarrier Transceivers	US	ABANDONED	14/485,937	9/15/14	US 2015-0003504 A1			5/10/16
6936-60-PUS-CON-2	STABLE LOW POWER MODE FOR MULTICARRIER TRANSCIVERS	US	ABANDONED	15/084,788	3/30/16	US 2016-0212275 A1			6/7/17
6936-61-PROV	Stable Low Power Mode for Multicarrier Transceivers (Second Edition)	US	EXPIRED	61/011,267	1/16/08	N/A			1/16/09
6936-84-PCT	Reed-Solomon Erasure Decoding with Error Detection for Retransmission	WO	NAT PHASE	PCT/US10/37195	6/3/10	WO 2010/141677			
6936-84-PROV	Reed-Solomon Erasure Decoding with Error Detection for Retransmission	US	EXPIRED	61/183,845	6/3/09	N/A			6/3/10
6936-84-PUS	Reed-Solomon Erasure Decoding with Error Detection for Retransmission	US	ISSUED	13/322,170	2/8/12	US 2012-0144259 A1	8,782,498	7/15/14	11/15/30
6936-84-PUS-CON	Reed-Solomon Erasure Decoding with Error Detection for Retransmission	US	ISSUED	14/328,237	7/10/14	US 2014-0323306 A1	9,276,612	3/1/16	6/3/30
6936-84-PUS-CON-2	REF-SOLOMON ERASURE DECODING WITH ERROR DETECTION FOR RETRANSMISSION	US	ABANDONED	15/054,499	2/26/16	US 2016-0182089 A1			5/9/18
6936-85-PCA	Low Power Mode with Legacy Compatibility	CA	PENDING	2,944,006	4/28/15				4/28/35
6936-85-PCT	Low Power Mode with Legacy Compatibility	WO	NAT PHASE	PCT/US15/27983	4/28/15	WO 2015/168117			

6936-85-PEP	Low Power Mode with Legacy Compatibility	EP	ISSUED	15721495.8	4/28/15	3138206	3138206	6/10/20	4/28/35
6936-85-PEPDE	Low Power Mode with Legacy Compatibility	DE	ISSUED	15721495.8	4/28/15		3138206	6/10/20	4/28/35
6936-85-PEPFR	Low Power Mode with Legacy Compatibility	FR	ISSUED	15721495.8	4/28/15		3138206	6/10/20	4/28/35
6936-85-PEPGB	Low Power Mode with Legacy Compatibility	GB	ISSUED	15721495.8	4/28/15		3138206	6/10/20	4/28/35
6936-85-PEPNL	Low Power Mode with Legacy Compatibility	NL	ISSUED	15721495.8	4/28/15		3138206	6/10/20	4/28/35
6936-85-PEP-DIV	Low Power Mode with Legacy Compatibility	EP	ABANDONED	20178740.5	4/28/15				9/30/20
6936-85-PJP	Low Power Mode with Legacy Compatibility	JP	ISSUED	2016-363176	4/28/15	2017-516391	6592006	9/27/19	4/28/35
6936-85-PKR	Low Power Mode with Legacy Compatibility	KR	PENDING	10-2016-7029383	4/28/15				4/28/35
6936-85-PROV	Low Power Mode with Legacy Compatibility	US	EXPIRED	61/985,168	4/28/14				4/28/15
6936-85-PUS	LOW POWER MODE WITH LEGACY COMPATIBILITY	US	PUBLISHED	15/304,920	10/18/16	US 2017-0187512 A1			4/28/35

Schedule III

Copyrights

None

AO 120 (Rev. 08/10)

TO: Mail Stop 8 Director of the U.S. Patent and Trademark Office P.O. Box 1450 Alexandria, VA 22313-1450	REPORT ON THE FILING OR DETERMINATION OF AN ACTION REGARDING A PATENT OR TRADEMARK

In Compliance with 35 U.S.C. § 290 and/or 15 U.S.C. § 1116 you are hereby advised that a court action has been
filed in the U.S. District Court Transferred to Delaware from Alabama on the following

☐ Trademarks or ☒ Patents. (☐ the patent action involves 35 U.S.C. § 292.);

DOCKET NO. 15-cv-121-RGA	DATE FILED 7/17/2014	U.S. DISTRICT COURT Transferred to Delaware from Alabama
PLAINTIFF ADTRAN, Inc.		DEFENDANT TQ Delta, LLC
PATENT OR TRADEMARK NO.	DATE OF PATENT OR TRADEMARK	HOLDER OF PATENT OR TRADEMARK
1 See Attachment #1		
2		
3		
4		
5		

In the above—entitled case, the following patent(s)/ trademark(s) have been included:

DATE INCLUDED 3/13/2015	INCLUDED BY ☐ Amendment ☒ Answer ☐ Cross Bill ☐ Other Pleading	
PATENT OR TRADEMARK NO.	DATE OF PATENT OR TRADEMARK	HOLDER OF PATENT OR TRADEMARK
1 See Attachment #2		
2		
3		
4		
5		

In the above—entitled case, the following decision has been rendered or judgement issued:

DECISION/JUDGEMENT

CLERK	(BY) DEPUTY CLERK	DATE

Copy 1—Upon initiation of action, mail this copy to Director Copy 3—Upon termination of action, mail this copy to Director
Copy 2—Upon filing document adding patent(s), mail this copy to Director Copy 4—Case file copy

Attachment #1

Patent or Trademark No.	Date of Patent or Trademark	Holder of Patent or Trademark
1.U.S. 7,453,881 B2	11/18/2008	TQ Delta, LLC
2.U.S. 7,809,028 B2	10/05/2010	TQ Delta, LLC
3.U.S. 7,978,706 B2	7/12/2011	TQ Delta, LLC
4.U.S. 8,422,511 B2	4/16/2013	TQ Delta, LLC
5.U.S. 6,445,730 B1	9/03/2002	TQ Delta, LLC
6.U.S. 7,292,627 B2	11/6/2007	TQ Delta, LLC
7.U.S. 7,451,379 B2	11/11/2008	TQ Delta, LLC
8.U.S. 7,471,721 B2	12/30/2008	TQ Delta, LLC
9.U.S. 7,570,686 B2	8/4/2009	TQ Delta, LLC
10. U.S. 7,831,890 B2	11/09/2010	TQ Delta, LLC
11. U.S. 7,835,430 B2	11/16/2010	TQ Delta, LLC
12. U.S. 7,836,381 B1	11/16/2010	TQ Delta, LLC
13. U.S. 7,844,882 B2	11/30/2010	TQ Delta, LLC
14. U.S. 7,889,784 B2	2/15/2011	TQ Delta, LLC
15. U.S. 7,925,958 B2	04/12/2011	TQ Delta, LLC
16. U.S. 7,978,753 B2	07/12/2011	TQ Delta, LLC
17. U.S. 7,979,778 B2	07/12/2011	TQ Delta, LLC
18. U.S. 8,073,041 B1	12/6/2011	TQ Delta, LLC
19. U.S. 8,090,008 B2	1/3/2012	TQ Delta, LLC
20. U.S. 8,218,610 B2	7/10/2012	TQ Delta, LLC
21. U.S. 8,238,412 B2	08/07/2012	TQ Delta, LLC
22. U.S. 8,276,048 B2	09/25/2012	TQ Delta, LLC
23. U.S. 8,355,427 B2	1/15/2013	TQ Delta, LLC

24. U.S. 8,432,956 B2	4/30/2013	TQ Delta, LLC
25. U.S. 8,437,382 B2	5/7/2013	TQ Delta, LLC
26. U.S. 8,462,835 B2	6/11/2013	TQ Delta, LLC
27. U.S. 8,495,473 B2	7/23/2013	TQ Delta, LLC
28. U.S. 8,516,337 B2	08/20/2013	TQ Delta, LLC

	PATENT OR TRADEMARK NO.	DATE OF PATENT OR TRADEMARK	HOLDER OF PATENT OR TRADEMARK
1	US 7,796,705 B2	9/14/2010	TQ Delta, LLC
2	US 8,335,956 B2	12/18/2012	TQ Delta, LLC
3	US 8,407,546 B2	3/26/2013	TQ Delta, LLC
4	US 8,468,411 B2	6/18/2013	TQ Delta, LLC
5	US 8,645,784 B2	2/4/2014	TQ Delta, LLC
6	US 8,595,577 B2	11/26/2013	TQ Delta, LLC

UNITED STATES PATENT AND TRADEMARK OFFICE
CERTIFICATE OF CORRECTION

PATENT NO. : 8,276,048 B2
APPLICATION NO. : 12/901699
DATED : September 25, 2012
INVENTOR(S) : Marcos C. Tzannes et al.

Page 1 of 1

It is certified that error appears in the above-identified patent and that said Letters Patent is hereby corrected as shown below:

In the Claims:

At Column 11, Claim 5, line 16, delete "transmission" and insert -- reception --

At Column 12, Claim 5, line 3, delete "received" and insert -- transmitted --

Signed and Sealed this
Twenty-eighth Day of October, 2014



Michelle K. Lee
Deputy Director of the United States Patent and Trademark Office

SPE RESPONSE FOR CERTIFICATE OF CORRECTION

Paper No.:20140929

DATE : September 29, 2014

TO SPE OF : ART UNIT 2117

SUBJECT : Request for Certificate of Correction on Patent No.: 8,276,048

A response is requested with respect to the accompanying request for a certificate of correction.

Please complete this form and return with file, within **7** days to:

Certificates of Correction Branch - ST (South Tower) 9A22

Palm location **7590** - Tel. No. (703) 305-8309

With respect to the change(s) requested, correcting Office and/or Applicant's errors, should the patent read as shown in the certificate of correction? No new matter should be introduced, nor should the scope or meaning of the claims be changed.

Thank You For Your Assistance

Certificates of Correction Branch

The request for issuing the above-identified correction(s) is hereby:

Note your decision on the appropriated box.

☒ **Approved**

All changes apply.

☐ **Approved in Part**

Specify below which changes **do not** apply.

☐ **Denied**

State the reasons for denial below.

Comments:

/AJAY BHATIA/
Supervisory Patent Examiner, Art Unit 2117

SPE RESPONSE FOR CERTIFICATE OF CORRECTION

DATE : 09/26/14

TO SPE OF : ART UNIT: 2117 Examiner: TABONE JR, JOHN

SUBJECT : Request for Certificate of Correction for Appl. No.: 12901699 Patent No.: 8276048

CofC mailroom date: 08/13/14

Please respond to this request for a certificate of correction within 7 days.

FOR IFW FILES:

Please review the requested changes/corrections as shown in the **COCIN** document(s) in the IFW application image. No new matter should be introduced, nor should the scope or meaning of the claims be changed.

Please complete the response (see below) and forward the completed response to scanning using document code **COCX**.

FOR PAPER FILES:

Please review the requested changes/corrections as shown in the attached certificate of correction. Please complete this form (see below) and forward it with the file to:

Certificates of Correction Branch (CofC)

Randolph Square – 9D10-A

Palm Location 7580

You can fax the Directors/SPE response to 571-272-3421

Note: **Should the changes to claim 5 be approved?**

Lamonte Newsome

Certificates of Correction Branch

571-272-3421

Thank You For Your Assistance

The request for issuing the above-identified correction(s) is hereby:

Note your decision on the appropriate box.

SPE RESPONSE FOR CERTIFICATE OF CORRECTION

☐ **Approved**

All changes apply.

☐ **Approved in Part**

Specify below which changes **do not** apply.

☐ **Denied**

State the reasons for denial below.

Comments: _____

SPE

Art Unit

AO 120 (Rev. 08/10)

TO: Mail Stop 8 Director of the U.S. Patent and Trademark Office P.O. Box 1450 Alexandria, VA 22313-1450	REPORT ON THE FILING OR DETERMINATION OF AN ACTION REGARDING A PATENT OR TRADEMARK

In Compliance with 35 U.S.C. § 290 and/or 15 U.S.C. § 1116 you are hereby advised that a court action has been filed in the U.S. District Court District of Delaware on the following

☐ Trademarks or ☒ Patents. (☐ the patent action involves 35 U.S.C. § 292.):

DOCKET NO.	DATE FILED 7/18/2014	U.S. DISTRICT COURT District of Delaware
PLAINTIFF TQ Delta, LLC		DEFENDANT ADTRAN, Inc.
PATENT OR TRADEMARK NO.	DATE OF PATENT OR TRADEMARK	HOLDER OF PATENT OR TRADEMARK
1 See Attached		
2 32 Pts		
3		
4		
5		

In the above—entitled case, the following patent(s)/ trademark(s) have been included:

DATE INCLUDED	INCLUDED BY ☐ Amendment ☐ Answer ☐ Cross Bill ☐ Other Pleading		
PATENT OR TRADEMARK NO.	DATE OF PATENT OR TRADEMARK	HOLDER OF PATENT OR TRADEMARK	
1			
2			
3			
4			
5			

In the above—entitled case, the following decision has been rendered or judgement issued:

DECISION/JUDGEMENT		
CLERK	(BY) DEPUTY CLERK	DATE

Copy 1—Upon initiation of action, mail this copy to Director Copy 3—Upon termination of action, mail this copy to Director
 Copy 2—Upon filing document adding patent(s), mail this copy to Director Copy 4—Case file copy

	PATENT OR TRADEMARK NO.	DATE OF PATENT OR TRADEMARK	HOLDER OF PATENT OR TRADEMARK
1	US 8,090,008 B2	1/3/2012	TQ Delta, LLC
2	US 8,073,041 B1	12/6/2011	TQ Delta, LLC
3	US 7,292,627 B2	11/6/2007	TQ Delta, LLC
4	US 7,471,721 B2	12/30/2008	TQ Delta, LLC
5	US 8,218,610 B2	7/10/2012	TQ Delta, LLC
6	US 8,355,427 B2	1/15/2013	TQ Delta, LLC
7	US 7,453,881 B2	11/18/2008	TQ Delta, LLC
8	US 7,809,028 B2	10/5/2010	TQ Delta, LLC
9	US 7,978,706 B2	7/12/2011	TQ Delta, LLC
10	US 8,422,511 B2	4/16/2013	TQ Delta, LLC
11	US 7,889,784 B2	2/15/2011	TQ Delta, LLC
12	US 7,835,430 B2	11/16/2010	TQ Delta, LLC
13	US 7,570,686 B2	8/4/2009	TQ Delta, LLC
14	US 8,238,412 B2	8/7/2012	TQ Delta, LLC
15	US 8,432,956 B2	4/30/2013	TQ Delta, LLC
16	US 7,451,379 B2	11/11/2008	TQ Delta, LLC
17	US 8,516,337 B2	8/20/2013	TQ Delta, LLC
18	US 7,979,778 B2	7/12/2011	TQ Delta, LLC
19	US 7,925,958 B2	4/12/2011	TQ Delta, LLC
20	US 8,462,835 B2	6/11/2013	TQ Delta, LLC
21	US 8,594,162 B2	11/26/2013	TQ Delta, LLC
22	US 7,978,753 B2	7/12/2011	TQ Delta, LLC
23	US 6,445,730 B1	9/3/2002	TQ Delta, LLC
24	US 8,611,404 B2	12/17/2013	TQ Delta, LLC
25	US 8,437,382 B2	5/7/2013	TQ Delta, LLC
26	US 7,836,381 B1	11/16/2010	TQ Delta, LLC
27	US 7,844,882 B2	11/30/2010	TQ Delta, LLC
28	US 8,276,048 B2	9/25/2012	TQ Delta, LLC
29	US 8,495,473 B2	7/23/2013	TQ Delta, LLC
30	US 8,607,126 B1	12/10/2013	TQ Delta, LLC
31	US 7,831,890 B2	11/9/2010	TQ Delta, LLC
32	US 8,625,660 B2	1/7/2014	TQ Delta, LLC

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In Re the Application of: Marcos C. Tzannes)
Patent No.: 8,276,048)
Issued: September 25, 2012)
Confirmation No.: 1676)
Atty. File No.: 6936-54-CON-3)

Application No.: 12/901,699
Filed: October 11, 2010
Examiner: TABONE JR., John J.
Art Unit: 2117

For: RESOURCE SHARING IN A TELECOMMUNICATIONS ENVIRONMENT

REQUEST FOR CERTIFICATE OF CORRECTION OF PATENT FOR
APPLICANT'S MISTAKE (37 C.F.R §1.323)

Attn: Certificate of Corrections Branch
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Sir:

This is a request for a Certificate of Correction under 37 C.F.R. 1.323 for the above-identified patent. Attached is form PTO/SB/44. Applicants have determined that there were typographic errors in claim 5 which were the mistake of the Applicant. The corrections do not introduce new matter, do not require re-examination, and do not materially affect the scope or meaning of the patent.

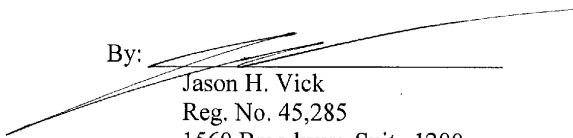
- At Column 11, Claim 5, line 16, delete "transmission" and insert -- reception --
- At Column 12, Claim 5, line 3, delete "received" and insert -- transmitted --

Payment in the amount of \$100.00, as required by 37 C.F.R. § 1.20(a) is being submitted herewith. Although no additional fees are believed due in connection with the filing of this paper, please charge any additional fees deemed necessary or credit any overpayment to Deposit Account No. 19-1970.

Respectfully submitted,

SHERIDAN ROSS P.C.

Date: 12/1/17

By: 

Jason H. Vick
Reg. No. 45,285
1560 Broadway, Suite 1200
Denver, Colorado 80202
Telephone: 303-863-9700

**UNITED STATES PATENT AND TRADEMARK OFFICE
CERTIFICATE OF CORRECTION**Page 1 of 1

PATENT NO. : 8,276,048

APPLICATION NO.: 12/901,699

ISSUE DATE : September 25, 2012

INVENTOR(S) : Marcos C. Tzannes et al.

It is certified that an error appears or errors appear in the above-identified patent and that said Letters Patent is hereby corrected as shown below:

At Column 11, Claim 5, line 16, delete "transmission" and insert -- reception --

At Column 12, Claim 5, line 3, delete "received" and insert -- transmitted --

MAILING ADDRESS OF SENDER (Please do not use customer number below):

Jason H. Vick / Sheridan Ross, PC
1560 Broadway, Suite 1200
Denver, CO 80202

This collection of information is required by 37 CFR 1.322, 1.323, and 1.324. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 1.0 hour to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Attention Certificate of Corrections Branch, Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

If you need assistance in completing the form, call 1-800-PTO-9199 and select option 2.

Electronic Patent Application Fee Transmittal				
Application Number:		12901699		
Filing Date:		11-Oct-2010		
Title of Invention:		RESOURCE SHARING IN A TELECOMMUNICATIONS ENVIRONMENT		
First Named Inventor/Applicant Name:		Marcos C. Tzannes		
Filer:		Jason Vick/Joanne Vos		
Attorney Docket Number:		6936-54-CON-3		
Filed as Large Entity				
Utility under 35 USC 111(a) Filing Fees				
Description	Fee Code	Quantity	Amount	Sub-Total in USD(\$)
Basic Filing:				
Pages:				
Claims:				
Miscellaneous-Filing:				
Petition:				
Patent-Appeals-and-Interference:				
Post-Allowance-and-Post-Issuance:				
Certificate of Correction	1811	1	100	100
Extension-of-Time:				

Description	Fee Code	Quantity	Amount	Sub-Total in USD(\$)
Miscellaneous:				
Total in USD (\$)				100

Electronic Acknowledgement Receipt	
EFS ID:	19854400
Application Number:	12901699
International Application Number:	
Confirmation Number:	1676
Title of Invention:	RESOURCE SHARING IN A TELECOMMUNICATIONS ENVIRONMENT
First Named Inventor/Applicant Name:	Marcos C. Tzannes
Customer Number:	62574
Filer:	Jason Vick/Joanne Vos
Filer Authorized By:	Jason Vick
Attorney Docket Number:	6936-54-CON-3
Receipt Date:	13-AUG-2014
Filing Date:	11-OCT-2010
Time Stamp:	14:15:48
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	yes
Payment Type	Deposit Account
Payment was successfully received in RAM	\$100
RAM confirmation Number	482
Deposit Account	191970
Authorized User	
The Director of the USPTO is hereby authorized to charge indicated fees and credit any overpayment as follows: Charge any Additional Fees required under 37 C.F.R. Section 1.16 (National application filing, search, and examination fees) Charge any Additional Fees required under 37 C.F.R. Section 1.17 (Patent application and reexamination processing fees)	

Charge any Additional Fees required under 37 C.F.R. Section 1.19 (Document supply fees)					
Charge any Additional Fees required under 37 C.F.R. Section 1.20 (Post Issuance fees)					
Charge any Additional Fees required under 37 C.F.R. Section 1.21 (Miscellaneous fees and charges)					
File Listing:					
Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1	Request for Certificate of Correction	Request_for_Certificate_of_Correction.pdf	293431 d81207f24e2fd1ee3a40dae5cac5871aafd b36a	no	3
Warnings:					
Information:					
2	Fee Worksheet (SB06)	fee-info.pdf	29805 ccddb7ea29939cc5d810e4b0d49855ee8 cca35	no	2
Warnings:					
Information:					
Total Files Size (in bytes):			323236		
This Acknowledgement Receipt evidences receipt on the noted date by the USPTO of the indicated documents, characterized by the applicant, and including page counts, where applicable. It serves as evidence of receipt similar to a Post Card, as described in MPEP 503. <u>New Applications Under 35 U.S.C. 111</u> If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application. <u>National Stage of an International Application under 35 U.S.C. 371</u> If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course. <u>New International Application Filed with the USPTO as a Receiving Office</u> If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.					

Birch, Melvin (Akima)

From: ded_nefreply@ded.uscourts.gov
Sent: Wednesday, November 20, 2013 4:56 PM
To: ded_ecf@ded.uscourts.gov
Subject: Activity in Case 1:13-cv-01835-RGA TQ Delta LLC v. Pace Americas Inc.
Patent/Trademark Report to Commissioner

This is an automatic e-mail message generated by the CM/ECF system. Please **DO NOT RESPOND** to this e-mail because the mail box is unattended.

NOTE TO PUBLIC ACCESS USERS Judicial Conference of the United States policy permits attorneys of record and parties in a case (including pro se litigants) to receive one free electronic copy of all documents filed electronically, if receipt is required by law or directed by the filer. PACER access fees apply to all other users. To avoid later charges, download a copy of each document during this first viewing. However, if the referenced document is a transcript, the free copy and 30 page limit do not apply.

U.S. District Court

District of Delaware

Notice of Electronic Filing

The following transaction was entered by Farnan, Brian on 11/20/2013 at 4:56 PM EST and filed on 11/20/2013

Case Name: TQ Delta LLC v. Pace Americas Inc.

Case Number: 1:13-cv-01835-RGA

Filer:

Document Number: 7

Docket Text:

Report to the Commissioner of Patents and Trademarks for Patent/Trademark Number(s) US 8,090,008 B2; US 8,073,041 B1; US 7,292,627 B2; US 7,471,721 B2; US 8,218,610 B2; US 8,355,427 B2; US 7,453,881 B2; US 7,978,706 B2; US 8,422,511 B2; US 7,889,784 B2; US 7,835,430 B2; US 7,570,686 B2; US 8,238,412 B2; US 8,432,956 B2; US 7,451,379 B2; US 8,516,337 B2; US 7,979,778 B2; US 7,925,958 B2; US 8,462,835 B2; US 7,836,381 B1; US 7,844,882 B2; US 8,276,048 B2; US 8,495,473 B2; US 7,831,890 B2; . (Farnan, Brian)

1:13-cv-01835-RGA Notice has been electronically mailed to:

Brian E. Farnan bfarnan@farnanlaw.com, tfarnan@farnanlaw.com

Michael J. Farnan mfarnan@farnanlaw.com, tfarnan@farnanlaw.com

1:13-cv-01835-RGA Filer will deliver document by other means to:

The following document(s) are associated with this transaction:

From: ded_nefreply@ded.uscourts.gov
Sent: Wednesday, November 20, 2013 5:07 PM
To: ded_ecf@ded.uscourts.gov
Subject: Activity in Case 1:13-cv-01836-RGA TQ Delta LLC v. Zhone Technologies Inc.
Patent/Trademark Report to Commissioner

This is an automatic e-mail message generated by the CM/ECF system. Please **DO NOT RESPOND** to this e-mail because the mail box is unattended.

*****NOTE TO PUBLIC ACCESS USERS***** Judicial Conference of the United States policy permits attorneys of record and parties in a case (including pro se litigants) to receive one free electronic copy of all documents filed electronically, if receipt is required by law or directed by the filer. PACER access fees apply to all other users. To avoid later charges, download a copy of each document during this first viewing. However, if the referenced document is a transcript, the free copy and 30 page limit do not apply.

U.S. District Court

District of Delaware

Notice of Electronic Filing

The following transaction was entered by Farnan, Brian on 11/20/2013 at 5:07 PM EST and filed on 11/20/2013

Case Name: TQ Delta LLC v. Zhone Technologies Inc.

Case Number: 1:13-cv-01836-RGA

Filer:

Document Number: 7

Docket Text:

Report to the Commissioner of Patents and Trademarks for Patent/Trademark Number(s) US 8,090,008 B2; US 8,073,041 B1; US 7,292,627 B2; US 7,471,721 B2; US 8,218,610 B2; US 8,355,427 B2; US 7,453,881 B2; US 7,809,028 B2; US 7,978,706 B2; US 8,422,511 B2; US 7,796,705 B2; US 7,889,784 B2; US 7,835,430 B2; US 7,570,686 B2; US 8,238,412 B2; US 8,432,956 B2; US 7,451,379 B2; US 8,516,337 B2; US 7,979,778 B2; US 7,925,958 B2; US 8,462,835 B2; US 7,978,753 B2; US 6,445,730 B1; US 8,437,382 B2; US 7,836,381 B1; US 7,844,882 B2; US 8,276,048 B2; US 8,495,473 B2; US 7,831,890 B2; US 8,335,956 B2; US 8,468,411 B2; US 8,407,546 B2 . (Farnan, Brian)

1:13-cv-01836-RGA Notice has been electronically mailed to:

Brian E. Farnan bfarnan@farnanlaw.com, tfarnan@farnanlaw.com

Michael J. Farnan mfarnan@farnanlaw.com, tfarnan@farnanlaw.com

1:13-cv-01836-RGA Filer will deliver document by other means to:

AO 120 (Rev. 08/10)

TO: Mail Stop 8 Director of the U.S. Patent and Trademark Office P.O. Box 1450 Alexandria, VA 22313-1450	REPORT ON THE FILING OR DETERMINATION OF AN ACTION REGARDING A PATENT OR TRADEMARK

In Compliance with 35 U.S.C. § 290 and/or 15 U.S.C. § 1116 you are hereby advised that a court action has been filed in the U.S. District Court District of Delaware on the following
☐ Trademarks or ☒ Patents. (☐ the patent action involves 35 U.S.C. § 292.);

DOCKET NO.	DATE FILED 12/9/2013	U.S. DISTRICT COURT District of Delaware
PLAINTIFF TQ Delta, LLC		DEFENDANT ZyXEL Communications Corporation and ZyXEL Communications, Inc.
PATENT OR TRADEMARK NO.	DATE OF PATENT OR TRADEMARK	HOLDER OF PATENT OR TRADEMARK
1 See Attached		
2		
3		
4		
5		

In the above—entitled case, the following patent(s)/ trademark(s) have been included:

DATE INCLUDED	INCLUDED BY ☐ Amendment ☐ Answer ☐ Cross Bill ☐ Other Pleading		
PATENT OR TRADEMARK NO.	DATE OF PATENT OR TRADEMARK	HOLDER OF PATENT OR TRADEMARK	
1			
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3			
4			
5			

In the above—entitled case, the following decision has been rendered or judgement issued:

DECISION/JUDGEMENT		
CLERK	(BY) DEPUTY CLERK	DATE

Copy 1—Upon initiation of action, mail this copy to Director Copy 3—Upon termination of action, mail this copy to Director
Copy 2—Upon filing document adding patent(s), mail this copy to Director Copy 4—Case file copy

	PATENT OR TRADEMARK NO.	DATE OF PATENT OR TRADEMARK	HOLDER OF PATENT OR TRADEMARK
1	US 8,090,008 B2	1/3/2012	TQ Delta, LLC
2	US 8,073,041 B1	12/6/2011	TQ Delta, LLC
3	US 7,292,627 B2	11/6/2007	TQ Delta, LLC
4	US 7,471,721 B2	12/30/2008	TQ Delta, LLC
5	US 8,218,610 B2	7/10/2012	TQ Delta, LLC
6	US 8,355,427 B2	1/15/2013	TQ Delta, LLC
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10	US 8,422,511 B2	4/16/2013	TQ Delta, LLC
11	US 7,796,705 B2	9/14/2010	TQ Delta, LLC
12	US 7,889,784 B2	2/15/2011	TQ Delta, LLC
13	US 7,835,430 B2	11/16/2010	TQ Delta, LLC
14	US 7,570,686 B2	8/4/2009	TQ Delta, LLC
15	US 8,238,412 B2	8/7/2012	TQ Delta, LLC
16	US 8,432,956 B2	4/30/2013	TQ Delta, LLC
17	US 7,451,379 B2	11/11/2008	TQ Delta, LLC
18	US 8,516,337 B2	8/20/2013	TQ Delta, LLC
19	US 7,979,778 B2	7/12/2011	TQ Delta, LLC
20	US 7,925,958 B2	4/12/2011	TQ Delta, LLC
21	US 8,462,835 B2	6/11/2013	TQ Delta, LLC
22	US 7,978,753 B2	7/12/2011	TQ Delta, LLC
23	US 6,445,730 B1	9/3/2002	TQ Delta, LLC
24	US 8,437,382 B2	5/7/2013	TQ Delta, LLC
25	US 7,836,381 B1	11/16/2010	TQ Delta, LLC
26	US 7,844,882 B2	11/30/2010	TQ Delta, LLC
27	US 8,276,048 B2	9/25/2012	TQ Delta, LLC
28	US 8,495,473 B2	7/23/2013	TQ Delta, LLC
29	US 7,831,890 B2	11/9/2010	TQ Delta, LLC
30	US 8,335,956 B2	12/18/2012	TQ Delta, LLC
31	US 8,468,411 B2	6/18/2013	TQ Delta, LLC
32	US 8,407,546 B2	3/26/2013	TQ Delta, LLC

TO: Mail Stop 8 Director of the U.S. Patent and Trademark Office P.O. Box 1450 Alexandria, VA 22313-1450	REPORT ON THE FILING OR DETERMINATION OF AN ACTION REGARDING A PATENT OR TRADEMARK

In Compliance with 35 U.S.C. § 290 and/or 15 U.S.C. § 1116 you are hereby advised that a court action has been filed in the U.S. District Court Northern District of Texas, Dallas Division on the following

☒ Trademarks or ☐ Patents. (☐ the patent action involves 35 U.S.C. § 292.):

DOCKET NO. 3:12-cv-1462-L	DATE FILED 5/10/2012	U.S. DISTRICT COURT Northern District of Texas, Dallas Division
PLAINTIFF Boulle Ltd		DEFENDANT De Boulle Diamond & Jewelry Inc
PATENT OR TRADEMARK NO.	DATE OF PATENT OR TRADEMARK	HOLDER OF PATENT OR TRADEMARK
1 4,086,050	1/17/2012	Boulle Ltd
2		
3		
4		
5		

In the above—entitled case, the following patent(s)/ trademark(s) have been included:

DATE INCLUDED 12/9/2013	INCLUDED BY ☒ Amendment ☐ Answer ☐ Cross Bill ☐ Other Pleading		
PATENT OR TRADEMARK NO.	DATE OF PATENT OR TRADEMARK	HOLDER OF PATENT OR TRADEMARK	
1 3,078,625	4/11/2006	De Boulle Diamond & Jewelry Inc	
2 3,078,627	4/11/2006	De Boulle Diamond & Jewelry Inc	
3			
4			
5			

In the above—entitled case, the following decision has been rendered or judgement issued:

DECISION/JUDGEMENT		
CLERK Karen Mitchell	(BY) DEPUTY CLERK s/A. Lowe-Monserrate	DATE 12/10/2013

Copy 1—Upon initiation of action, mail this copy to Director Copy 3—Upon termination of action, mail this copy to Director
 Copy 2—Upon filing document adding patent(s), mail this copy to Director Copy 4—Case file copy

Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it displays a valid OMB control number.

POWER OF ATTORNEY TO PROSECUTE APPLICATIONS BEFORE THE USPTO

I hereby revoke all previous powers of attorney given in the application identified in the attached statement under 37 CFR 3.73(c).

I hereby appoint:

☒

Practitioners associated with Customer Number:

62574

OR

☐

Practitioner(s) named below (If more than ten patent practitioners are to be named, then a customer number must be used):

Name	Registration Number	Name	Registration Number

As attorney(s) or agent(s) to represent the undersigned before the United States Patent and Trademark Office (USPTO) in connection with any and all patent applications assigned only to the undersigned according to the USPTO assignment records or assignments documents attached to this form in accordance with 37 CFR 3.73(c).

Please change the correspondence address for the application identified in the attached statement under 37 CFR 3.73(c) to:

☒

The address associated with Customer Number:

62574

OR

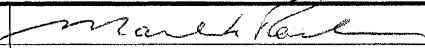
☐ Firm or Individual Name			
Address			
City	State	Zip	
Country			
Telephone			Email

Assignee Name and Address: TQ DELTA, LLC
805 Las Cimas Parkway, Suite 240
Austin, Texas 78746

A copy of this form, together with a statement under 37 CFR 3.73(c) (Form PTO/AIA/96 or equivalent) is required to be filed in each application in which this form is used. The statement under 37 CFR 3.73(c) may be completed by one of The practitioners appointed in this form, and must identify the application in which this Power of Attorney is to be filed.

SIGNATURE of Assignee of Record

The individual whose signature and title is supplied below is authorized to act on behalf of the assignee

Signature		Date	10/4/12
Name	Mark K. Roche	Telephone	512-609-1810
Title	Managing Director		

This collection of information is required by 37 CFR 1.31, 1.32 and 1.33. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.11 and 1.14. This collection is estimated to take 3 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.

If you need assistance in completing the form, call 1-800-PTO-9199 and select option 2.

Electronic Acknowledgement Receipt	
EFS ID:	14186005
Application Number:	12901699
International Application Number:	
Confirmation Number:	1676
Title of Invention:	RESOURCE SHARING IN A TELECOMMUNICATIONS ENVIRONMENT
First Named Inventor/Applicant Name:	Marcos C. Tzannes
Customer Number:	62574
Filer:	Jason Vick/Joanne Vos
Filer Authorized By:	Jason Vick
Attorney Docket Number:	6936-54-CON-3
Receipt Date:	08-NOV-2012
Filing Date:	11-OCT-2010
Time Stamp:	18:11:59
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	no				
File Listing:					
Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1		EntityStatus_373c_w_POA.pdf	417878 5071e3be61d1b8a9127d1f735535c4cc95720731	yes	4

	Multipart Description/PDF files in .zip description		
	Document Description	Start	End
	Miscellaneous Incoming Letter	1	1
	Assignee showing of ownership per 37 CFR 3.73.	2	3
	Power of Attorney	4	4
Warnings:			
Information:			
Total Files Size (in bytes):		417878	
This Acknowledgement Receipt evidences receipt on the noted date by the USPTO of the indicated documents, characterized by the applicant, and including page counts, where applicable. It serves as evidence of receipt similar to a Post Card, as described in MPEP 503.			
<u>New Applications Under 35 U.S.C. 111</u> If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application.			
<u>National Stage of an International Application under 35 U.S.C. 371</u> If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.			
<u>New International Application Filed with the USPTO as a Receiving Office</u> If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.			

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In Re the Application of: Marcos C. Tzannes	)	Issued Patent No.: 8,276,048
Application No.: 12/901,699	)	Issued Date: September 25, 2012
Filed: October 11, 2010	)	Examiner: TABONE, JR, John J.
Atty. File No.: 6936-54-CON-3	)	Confirmation No.: 1676

For: RESOURCE SHARING IN A TELECOMMUNICATIONS ENVIRONMENT

ASSERTION OF ENTITLEMENT TO SMALL ENTITY STATUS

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Madam:

In accordance with MPEP §§ 509.02 and 509.03 and 37 CFR 1.27, this document is being filed to inform the U.S. Patent Office of the change of status for the above-identified patent from large entity status to small entity status. All fees paid to date have been paid as large entity status. No fees have yet been paid as small entity status. Due to the sale of the referenced patent, the Applicant is now entitled to small entity status.

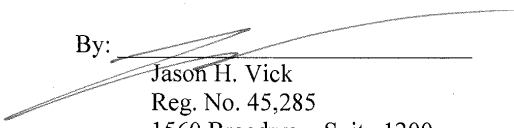
We respectfully request that small entity status be granted for the above-referenced patent.

Please contact the undersigned if there are any questions regarding this notification.

Respectfully submitted,

SHERIDAN ROSS P.C.

Date: 8/11/12

By: 
Jason H. Vick
Reg. No. 45,285
1560 Broadway, Suite 1200
Denver, Colorado 80202
Telephone: 303-863-9700

STATEMENT UNDER 37 CFR 3.73(c)

Applicant/Patent Owner: TQ DELTA, LLC
Application No./Patent No.: 8,276,048 Filed/Issue Date: September 25, 2012
Titled: RESOURCE SHARING IN A TELECOMMUNICATIONS ENVIRONMENT
TQ DELTA, LLC, a Corporation
(Name of Assignee) (Type of Assignee, e.g., corporation, partnership, university, government agency, etc.)

states that, for the patent application/patent identified above, it is (choose one of options 1, 2, 3 or 4 below):

1. ☒ The assignee of the entire right, title, and interest.
2. ☐ An assignee of less than the entire right, title, and interest (check applicable box):
- ☐ The extent (by percentage) of its ownership interest is ____%. Additional Statement(s) by the owners holding the balance of the interest must be submitted to account for 100% of the ownership interest.
- ☐ There are unspecified percentages of ownership. The other parties, including inventors, who together own the entire right, title and interest are:

Additional Statement(s) by the owner(s) holding the balance of the interest must be submitted to account for the entire right, title, and interest.

3. ☐ The assignee of an undivided interest in the entirety (a complete assignment from one of the joint inventors was made). The other parties, including inventors, who together own the entire right, title, and interest are:

Additional Statement(s) by the owner(s) holding the balance of the interest must be submitted to account for the entire right, title, and interest.

4. ☐ The recipient, via a court proceeding or the like (e.g., bankruptcy, probate), of an undivided interest in the entirety (a complete transfer of ownership interest was made). The certified document(s) showing the transfer is attached.

The interest identified in option 1, 2 or 3 above (not option 4) is evidenced by either (choose one of options A or B below):

- A. ☐ An assignment from the inventor(s) of the patent application/patent identified above. The assignment was recorded in the United States Patent and Trademark Office at Reel _____, Frame _____, or for which a copy thereof is attached.
- B. ☒ A chain of title from the inventor(s), of the patent application/patent identified above, to the current assignee as follows:

1. From: Marcos C. Tzannes, Michael Lund To: AWARE, INC.

The document was recorded in the United States Patent and Trademark Office at
Reel 017438, Frame 0094, or for which a copy thereof is attached.

2. From: AWARE, INC. To: TQ DELTA, LLC

The document was recorded in the United States Patent and Trademark Office at
Reel 029154, Frame 0937, or for which a copy thereof is attached.

[Page 1 of 2]

This collection of information is required by 37 CFR 3.73(b). The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.11 and 1.14. This collection is estimated to take 12 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

If you need assistance in completing the form, call 1-800-PTO-9199 and select option 2.

Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it displays a valid OMB control number.

STATEMENT UNDER 37 CFR 3.73(c)

3. From: _____ To: _____

The document was recorded in the United States Patent and Trademark Office at
Reel _____, Frame _____, or for which a copy thereof is attached.

4. From: _____ To: _____

The document was recorded in the United States Patent and Trademark Office at
Reel _____, Frame _____, or for which a copy thereof is attached.

5. From: _____ To: _____

The document was recorded in the United States Patent and Trademark Office at
Reel _____, Frame _____, or for which a copy thereof is attached.

6. From: _____ To: _____

The document was recorded in the United States Patent and Trademark Office at
Reel _____, Frame _____, or for which a copy thereof is attached.☐ Additional documents in the chain of title are listed on a supplemental sheet(s).☒ As required by 37 CFR 3.73(c)(1)(i), the documentary evidence of the chain of title from the original owner to the assignee was, or concurrently is being, submitted for recordation pursuant to 37 CFR 3.11.

[NOTE: A separate copy (i.e., a true copy of the original assignment document(s)) must be submitted to Assignment Division in accordance with 37 CFR Part 3, to record the assignment in the records of the USPTO. See MPEP 302.08]

The undersigned (whose title is supplied below) is authorized to act on behalf of the assignee.

Signature

Jason H. Vick

Printed or Typed Name

Date

45,285

Title or Registration Number

[Page 2 of 2]



UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	ISSUE DATE	PATENT NO.	ATTORNEY DOCKET NO.	CONFIRMATION NO.
12/901,699	09/25/2012	8276048	5550-54-CON-3	1676

62574 7590 09/05/2012

Jason H. Vick
Sheridan Ross, PC
Suite # 1200
1560 Broadway
Denver, CO 80202

ISSUE NOTIFICATION

The projected patent number and issue date are specified above.

Determination of Patent Term Adjustment under 35 U.S.C. 154 (b)
(application filed on or after May 29, 2000)

The Patent Term Adjustment is 0 day(s). Any patent to issue from the above-identified application will include an indication of the adjustment on the front page.

If a Continued Prosecution Application (CPA) was filed in the above-identified application, the filing date that determines Patent Term Adjustment is the filing date of the most recent CPA.

Applicant will be able to obtain more detailed information by accessing the Patent Application Information Retrieval (PAIR) WEB site (<http://pair.uspto.gov>).

Any questions regarding the Patent Term Extension or Adjustment determination should be directed to the Office of Patent Legal Administration at (571)-272-7702. Questions relating to issue and publication fee payments should be directed to the Application Assistance Unit (AAU) of the Office of Data Management (ODM) at (571)-272-4200.

APPLICANT(s) (Please see PAIR WEB site <http://pair.uspto.gov> for additional applicants):

Marcos C. Tzannes, Orinda, CA;
Michael Lund, West Newton, MA;

The United States represents the largest, most dynamic marketplace in the world and is an unparalleled location for business investment, innovation, and commercialization of new technologies. The USA offers tremendous resources and advantages for those who invest and manufacture goods here. Through SelectUSA, our nation works to encourage and facilitate business investment. To learn more about why the USA is the best country in the world to develop technology, manufacture products, and grow your business, visit SelectUSA.gov.

IR103 (Rev. 10/09)

Receipt date: 02/29/2012

Change(s) applied

to document,

Substitute for form 1449A/PTO

/M.C.R./

8/16/2012

**INFORMATION DISCLOSURE
STATEMENT BY APPLICANT**

				Complete if Known	
				Application Number	12/901,699
				Filing Date	October 11, 2010
				First Named Inventor	Marcos C. Tzannes
				Art Unit	2117
				Examiner Name	Tabone Jr, John J.
				Attorney Docket Number	5550-54-CON-3
Sheet	1	of	2		

U.S. PATENT DOCUMENTS

Examiner Initials*	Cite No. ¹	Document Number Number-kind Code ^{2 (if known)}	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear
	1	7200792	04-03-2007	Kim et al.	
	2	2001/0014962	08-16-2001	Obuchi et al.	

FOREIGN PATENT DOCUMENTS

Examiner Initials*	Cite No. ¹	Foreign Patent Document Country Code ³ ; Number ⁴ ; Kind Code ⁵ (if known)	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear	T ⁶
	3	JP 07-254862	10-03-1995	Sony CORP.		(includes English abstract and partial mechanical translation)
	4	JP 2003-224615	08-08-2003	SAMSUNG ELECTRONICS CO LTD.		(corresponds to US 7,200,792 cited herein)
	5	JP 2005-522963	07-28-2005	INTERDIGITAL TECHNOLOGY CORPORATION		(corresponds to WO 03/090011 cited herein)
	6	WO00/52834	~~10-30-2003~~ 09/2000	FUJITSU LIMITED		(corresponds to US2001/0014962 cited herein)
	7	WO 03/090011	10-30-2003	INTERDIGITAL TECHNOLOGY CORPORATION		
	8	EP 1041756	10-04-2000	LUCENT TECHNOLOGIES INC.		(corresponds to JP 2000-341247 previously cited by Applicants on 10-17-2011)

Examiner Signature	/John J. Tabone Jr. / (07/20/2012)	Date Considered	

*EXAMINER: Initial if reference is considered, whether or not citation is in conformance and not considered. Include copy of this form with next communication to applicant.

ALL REFERENCES CONSIDERED EXCEPT WHERE LINED THROUGH. /JJT/

Receipt date: 01/18/2012

Substitute for form 1449A/PTO INFORMATION DISCLOSURE STATEMENT BY APPLICANT				Complete if Known	
				Application Number	12/901,699
				Filing Date	October 11, 2010
				First Named Inventor	Marcos C. Tzannes
				Art Unit	2117
				Examiner Name	Tabone Jr, John J.
Sheet	1	of	1	Attorney Docket Number	5550-54-CON-3

U.S. PATENT DOCUMENTS					
Examiner Initials*	Cite No. ¹	Document Number Number-kind Code ² (if known)	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear

FOREIGN PATENT DOCUMENTS						
Examiner Initials*	Cite No. ¹	Foreign Patent Document Country Code ³ ; Number ⁴ ; Kind Code ⁵ (if known)	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear	T ⁶
/JJT/	1	GB 2389493	12/10/2003	NEC CORP		

OTHER ART (Including Author, Title, Date, Pertinent Pages, etc.)		
Examiner Initials*	Cite No. ¹	
/JJT/	2	Official Action for European Patent Application No. 10000016.5, dated Dec. 22, 2011 (Attorney Ref. No. 5550-57-PEP-DIV-2)

Examiner Signature	/John J. Tabone Jr. / (08/07/2012)	Date Considered	

*EXAMINER: Initial if reference is considered, whether or not citation is in conformance and not considered. Include copy of this form with next communication to applicant.



UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
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Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
12/901,699	10/11/2010	Marcos C. Tzannes	5550-54-CON-3	1676
62574	7590	08/10/2012	EXAMINER	
Jason H. Vick			TABONE JR, JOHN J	
Sheridan Ross, PC			ART UNIT	PAPER NUMBER
Suite # 1200			2117	
1560 Broadway			NOTIFICATION DATE	DELIVERY MODE
Denver, CO 80202			08/10/2012	ELECTRONIC

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

jvick@sheridanross.com

Response to Rule 312 Communication	Application No.	Applicant(s)
	12/901,699	TZANNES ET AL.
	Examiner	Art Unit
	JOHN J. TABONE JR	2117
-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address -- 1. ☒ The amendment filed on <u>03 August 2012</u> under 37 CFR 1.312 has been considered, and has been: a) ☒ entered. b) ☐ entered as directed to matters of form not affecting the scope of the invention. c) ☐ disapproved because the amendment was filed after the payment of the issue fee. Any amendment filed after the date the issue fee is paid must be accompanied by a petition under 37 CFR 1.313(c)(1) and the required fee to withdraw the application from issue. d) ☐ disapproved. See explanation below. e) ☐ entered in part. See explanation below. In response to the Incoming Letter from the Applicants, the IDS of 01/18/2012 has been considered by the Examiner and is attached to this this response. The Examiner did not initially considered it because it was enter into eDAN with a red X in the IDS field.		
	/JOHN J TABONE JR/ Primary Examiner, Art Unit 2117 08/07/2012	

PART B - FEE(S) TRANSMITTAL

Complete and send this form, together with applicable fee(s), to: **Mail** **Mail Stop ISSUE FEE**
Commissioner for Patents
P.O. Box 1450
Alexandria, Virginia 22313-1450
or Fax **(571)-273-2885**

INSTRUCTIONS: This form should be used for transmitting the ISSUE FEE and PUBLICATION FEE (if required). Blocks 1 through 5 should be completed where appropriate. All further correspondence including the Patent, advance orders and notification of maintenance fees will be mailed to the current correspondence address as indicated unless corrected below or directed otherwise in Block 1, by (a) specifying a new correspondence address; and/or (b) indicating a separate "FEE ADDRESS" for maintenance fee notifications.

CURRENT CORRESPONDENCE ADDRESS (Note: Use Block 1 for any change of address)

62574 7590 07/27/2012
Jason H. Vick
Sheridan Ross, PC
Suite # 1200
1560 Broadway
Denver, CO 80202

Note: A certificate of mailing can only be used for domestic mailings of the Fee(s) Transmittal. This certificate cannot be used for any other accompanying papers. Each additional paper, such as an assignment or formal drawing, must have its own certificate of mailing or transmission.

Certificate of Mailing or Transmission

I hereby certify that this Fee(s) Transmittal is being deposited with the United States Postal Service with sufficient postage for first class mail in an envelope addressed to the Mail Stop ISSUE FEE address above, or being facsimile transmitted to the USPTO (571) 273-2885, on the date indicated below.

(Depositor's name)
(Signature)
(Date)

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
12/901,699	10/11/2010	Marcos C. Tzannes	5550-54-CON-3	1676

TITLE OF INVENTION: RESOURCE SHARING IN A TELECOMMUNICATIONS ENVIRONMENT

APPLN. TYPE	SMALL ENTITY	ISSUE FEE DUE	PUBLICATION FEE DUE	PREV. PAID (ISSUE FEE)	TOTAL FEE(S) DUE	DATE DUE
nonprovisional	NO	\$1740	\$300	\$0	\$2040	10/29/2012

EXAMINER	ART UNIT	CLASS-SUBCLASS
TABONE JR, JOHN J	2117	714-774000

1. Change of correspondence address or indication of "Fee Address" (37 CFR 1.363).

- ☐ Change of correspondence address (or Change of Correspondence Address form PTO/SB/122) attached.
☐ "Fee Address" indication (or "Fee Address" Indication form PTO/SB/47; Rev 03-02 or more recent) attached. Use of a Customer Number is required.

2. For printing on the patent front page, list

- (1) the names of up to 3 registered patent attorneys or agents OR, alternatively,
(2) the name of a single firm (having as a member a registered attorney or agent) and the names of up to 2 registered patent attorneys or agents. If no name is listed, no name will be printed.

1 Jason H. Vick

2 Sheridan Ross, PC

3 _____

3. ASSIGNEE NAME AND RESIDENCE DATA TO BE PRINTED ON THE PATENT (print or type)

PLEASE NOTE: Unless an assignee is identified below, no assignee data will appear on the patent. If an assignee is identified below, the document has been filed for recordation as set forth in 37 CFR 3.11. Completion of this form is NOT a substitute for filing an assignment.

(A) NAME OF ASSIGNEE

AWARE, INC.

(B) RESIDENCE: (CITY and STATE OR COUNTRY)

Bedford, MA

Please check the appropriate assignee category or categories (will not be printed on the patent): ☐ Individual ☒ Corporation or other private group entity ☐ Government

4a. The following fee(s) are submitted:

- ☒ Issue Fee
☒ Publication Fee (No small entity discount permitted)
☐ Advance Order - # of Copies _____

4b. Payment of Fee(s): (Please first reapply any previously paid issue fee shown above)

- ☐ A check is enclosed.
☐ Payment by credit card. Form PTO-2038 is attached.
☒ The Director is hereby authorized to charge the required fee(s), any deficiency, or credit any overpayment, to Deposit Account Number 19-1970 (enclose an extra copy of this form).

5. Change in Entity Status (from status indicated above)

- ☐ a. Applicant claims SMALL ENTITY status. See 37 CFR 1.27. ☐ b. Applicant is no longer claiming SMALL ENTITY status. See 37 CFR 1.27(g)(2).

NOTE: The Issue Fee and Publication Fee (if required) will not be accepted from anyone other than the applicant; a registered attorney or agent; or the assignee or other party in interest as shown by the records of the United States Patent and Trademark Office.

Authorized Signature _____

Date 3 Aug '12

Typed or printed name Jason H. Vick

Registration No. 45,285

This collection of information is required by 37 CFR 1.311. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 12 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, Virginia 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, Virginia 22313-1450.

Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it displays a valid OMB control number.

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In Re the Application of: Marcos C. Tzannes	)	Group Art Unit: 2117
Application No.: 12/901,699	)	Examiner: TABONE JR., John J.
Filed: October 11, 2010	)	Confirmation No.: 1676
Atty. File No.: 5550-54-CON-3	)	

For: RESOURCE SHARING IN A TELECOMMUNICATIONS ENVIRONMENT

COMMENTS ON STATEMENT OF REASONS FOR ALLOWANCE

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313

Madam:

Applicant submits this Comments on Statement of Reasons for Allowance to address further the Notice of Allowability ("Notice") having a mailing date of July 27, 2012.

In the Notice, the Examiner's stated reasons for allowance were that:

The present invention relates to communication systems. More specifically, an exemplary embodiment of this invention relates to memory sharing in communication systems. Another exemplary embodiment relates to processing or coding resource sharing in a communication system.

The claimed invention as set forth in **claim 46** recites features such as:

A system that allocates shared memory comprising:
a transceiver that is capable of:
transmitting or receiving a message during initialization specifying a maximum number of bytes of memory that are available to be allocated to an interleaver;
determining an amount of memory required by the interleaver to interleave a first plurality of Reed Solomon (RS) coded data bytes within the shared memory;
allocating a first number of bytes of the shared memory to the interleaver to interleave the first plurality of Reed Solomon (RS) coded data

bytes for transmission at a first data rate, wherein the allocated memory for the interleaver does not exceed the maximum number of bytes specified in the message;

allocating a second number of bytes of the shared memory to a deinterleaver to deinterleave a second plurality of RS coded data bytes received at a second data rate; and

interleaving the first plurality of RS coded data bytes within the shared memory allocated to the interleaver and deinterleaving the second plurality of RS coded data bytes within the shared memory allocated to the deinterleaver, wherein the shared memory allocated to the interleaver is used at the same time as the shared memory allocated to the deinterleaver.

The prior arts of record, namely Fadavi-Ardekani et al. (US-6707822), teach sharing a memory between the interleavers and deinterleavers of multiple Asymmetrical Digital Subscriber Line (ADSL) sessions. (Abstract).

The prior arts of record, however, fail to teach, singly or in combination, the claimed invention as a whole, *especially transmitting or receiving a message during initialization specifying a maximum number of bytes of memory that are available to be allocated to an interleaver*. As such, modification of the prior art of record to include the claimed invention as a whole, *especially transmitting or receiving a message during initialization specifying a maximum number of bytes of memory that are available to be allocated to an interleaver* can only be motivated by hindsight reasoning, or by changing the intended use and function of the prior art themselves. Therefore, it is not clear that one of ordinary skill in the art at the time of the invention would have made the necessary modifications to the prior art of record to encompass the invention as a whole, *especially transmitting or receiving a message during initialization specifying a maximum number of bytes of memory that are available to be allocated to an interleaver* set forth in the present application. Moreover, none of the prior arts of record, taken either alone or in combination, anticipate nor render obvious the invention as a whole, *especially transmitting or receiving a message during initialization specifying a maximum number of bytes of memory that are available to be allocated to an interleaver* as set forth in **claim 46**. Independent **claim 50** recite similar patentable features and are allowable for the same reasons as **claim 46**. Hence, **claims 46-53** are allowable over the prior arts of record.

Based on the Notice, the patentability of all other independent and dependent claims is assumed to be based upon the elements as set forth in such claims and that such claims meet all criteria for patentability under §101, §102, §103 and §112.

As is clear from MPEP 1302.14,

“The statement [of reasons for allowance] is not intended to necessarily state all the reasons for allowance or all the details why claims are allowed and should not be written to specifically or impliedly state that all the reasons for allowance are set forth.”

While the stated Reasons for Allowance may be a stated reason for allowing some independent claims, Applicant submits that some independent claims have a different reason for allowance and that some independent claims have other reasons for allowance.

Specifically, the prior art fails to teach the specific combination of features as recited in the independent claims 46 and 50.

Although the Applicant believes that no fees are due for filing this Comments on Statement of Reasons for Allowance, please charge any fees deemed necessary to Deposit Account No. 19-1970.

Respectfully submitted,

SHERIDAN ROSS P.C.

Date: 3/27/12

By: _____

Jason H. Vick
Reg. No. 45,285
1560 Broadway, Suite 1200
Denver, Colorado 80202
Telephone: 303-863-9700

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In Re the Application of: Marcos C. Tzannes	}	Group Art Unit: 2117
Application No.: 12/901,699		Examiner: TABONE JR., John J.
Filed: October 11, 2010		Confirmation No.: 1676
Atty. File No.: 5550-54-CON-3		

For: RESOURCE SHARING IN A TELECOMMUNICATIONS ENVIRONMENT

AMENDMENT AFTER ALLOWANCE UNDER
37 C.F.R. 1.312

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Madam:

Applicants submit this Amendment After Allowance pursuant to 37 C.F.R. 1.312 in response to the Notice of Allowance having a mailing date of July 27, 2012. While Applicants believe that no fees are due with the filing of this response, the undersigned hereby authorizes the charge of any fees deemed necessary to Deposit Account No. 19-1970.

An amendment may be entered after the mailing of a Notice of Allowance but prior to payment of the issue fee upon recommendation of the primary Examiner. Therefore, it is respectfully requested that the above-referenced application be amended as follows:

Amendments to the Specification begin on page 2 of this paper.

Remarks begin on page 3 of this paper.

AMENDMENTS TO THE SPECIFICATION

Please replace paragraph [0001] with:

[0001] This application is a Continuation of U.S. Application No. 12/761,586, filed April 16, 2010, now U.S. Patent No. 7,844,882, which is a Continuation of U.S. Application No. 11/246,163 filed October 11, 2005, now U.S. Patent No. 7,831,890, which claims the benefit of and priority under 35 U.S.C. § 119(e) to U.S. Patent Application No. 60/618,269, filed October 12, 2004, entitled “Sharing Memory and Processing Resources in DSL Systems,” each of which are incorporated herein by reference in their entirety.

REMARKS

By this amendment, the Cross-Reference to Related Applications has been updated. No new matter is believed to be introduced by this amendment.

The Commissioner is hereby authorized to charge to deposit account number 19-1970 any fees under 37 CFR § 1.16 and 1.17 that may be required by this paper and to credit any overpayment to that Account. If any extension of time is required in connection with the filing of this paper and has not been separately requested, such extension is hereby petitioned.

Respectfully submitted,

SHERIDAN ROSS P.C.

Date: 3 Aug '12

By: _____

Jason H. Vick
Reg. No. 45,285
1560 Broadway, Suite 1200
Denver, Colorado 80202
Telephone: 303-863-9700

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In Re the Application of:	)	Group Art Unit: 2117
Marcos C. Tzannes	)	Confirmation No.: 1676
Serial No.: 12/9601,699	)	Examiner: TABONE JR., John J.
Filed: October 11, 2010	)	
Atty. File No.: 5550-54-CON-3	)	<u>REQUEST FOR CONSIDERATION OF</u>
Entitled: "RESOURCE SHARING IN A	)	<u>REFERENCES CITED IN</u>
TELECOMMUNICATIONS	)	<u>INFORMATION DISCLOSURE</u>
ENVIRONMENT"	)	<u>STATEMENT OF January 18, 2012</u>
	)	
	)	<i>Electronically Submitted</i>

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Dear Madam:

On January 18, 2012, Applicant's representative filed an Information Disclosure Statement ("IDS") pursuant to 37 CFR 1.97(c) in the above-identified patent application. A copy of the IDS is attached hereto as Exhibit A. Copies of the non-patent literature were provided to the USPTO with the IDS and may be viewed in the image file wrapper.

The Examiner issued a Notice of Allowance on July 27, 2012, the "List of References cited by applicant and considered by examiner" for the aforementioned IDS was not attached to the communication.

The IDS of January 18, 2012, was properly submitted to the USPTO pursuant to 37 CFR §§ 1.97(c). Applicants hereby respectfully request that the reference cited therein be considered by the Examiner.

Although no fees are believed due in connection with this communication, please charge any fees deemed necessary to Deposit Account No. 19-1970. If additional information is required please contact the undersigned

Respectfully submitted,

SHERIDAN ROSS P.C.

Date: 3 Aug '12

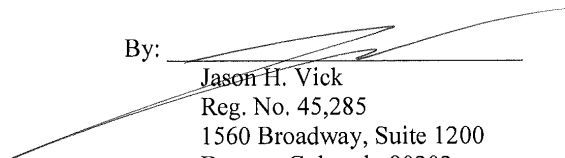
By: 
Jason H. Vick
Reg. No. 45,285
1560 Broadway, Suite 1200
Denver, Colorado 80202
Telephone: 303-863-9700

EXHIBIT A

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In Re the Application of:	)	Group Art Unit: 2117
TZANNES, Marcos C.	)	Confirmation No.: 1676
Serial No.: 12/901,699	)	Examiner: Tabone Jr, John J.
Filed: October 11, 2010	)	
Atty. File No.: 5550-54-CON-3	)	<u>SUPPLEMENTAL</u>
Entitled: "RESOURCE SHARING IN A	)	<u>INFORMATION DISCLOSURE</u>
TELECOMMUNICATIONS ENVIRONMENT"	)	<u>STATEMENT</u>
	)	Electronically Submitted

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Dear Sir:

The references cited on attached Form PTO-1449 are being called to the attention of the Examiner.

- ☒ Copies of the cited non-patent and/or foreign references are enclosed herewith.
- ☐ Copies of the cited U.S. patents and/or patent applications are enclosed herewith.
- ☐ Copies of the cited U.S. patents/patent application publications are not enclosed in accordance with 37 C.F.R. § 1.98(a).
- ☐ Copies of the cited references are not enclosed, in accordance with 37 C.F.R. § 1.98(d), because the references were cited by or submitted to the U.S. Patent and Trademark Office in prior application Serial No. _____ filed _____, which is relied upon for an earlier filing date under 35 U.S.C. § 120.
- ☐ To the best of applicants' belief, the pertinence of the foreign-language references are believed to be summarized in the attached English translations and/or in the figures, although applicants do not necessarily vouch for the accuracy of the translation.
- ☐ Examiner's attention is drawn to the following related applications:
- Serial No. _____ filed _____ (Attorney Ref. No. _____)
- Serial No. _____ filed _____ (Attorney Ref. No. _____)
- ☐ Other: _____

Submission of the above information is not intended as an admission that any item is citable under the statutes or rules to support a rejection, that any item disclosed represents analogous art, or that those skilled in the art would refer to or recognize the pertinence of any reference without the benefit of hindsight, nor should an inference be

drawn as to the pertinence of the references based on the order in which they are presented. Submission of this statement should not be taken as an indication that a search has been conducted, or that no better art exists.

It is respectfully requested that the cited information be expressly considered during the prosecution of this application and the references made of record therein.

FEES

☐	37 CFR 1.97(b): No fee is believed due in connection with this submission, because the information disclosure statement submitted herewith is satisfied by one of the following conditions ("X" indicates satisfaction): ☐ Within three months of the filing date of a national application other than a continued prosecution application under 37 CFR 1.53(d), or ☐ Within three months of the date of entry of the national stage as set forth in § 1.491 in an international application, or ☐ Before the mailing date of a first Office Action on the merits, or ☐ Before the mailing of a first Office action after the filing of a request for continued examination under 37 CFR 1.114. Although no fee is believed due, if any fee is deemed due in connection with this submission, please charge such fee to Deposit Account 19-1970.
☒	37 CFR 1.97(c): The information disclosure statement transmitted herewith is being filed after all the above conditions (37 CFR 1.97(b)), but before the mailing date of any one of the following conditions: (1) a final action under 37 C.F.R. 1.113, or (2) a notice of allowance under 37 C.F.R. 1.311, or (3) an action that otherwise closes prosecution in the application. This Information Disclosure Statement is accompanied by: ☒ A Certification (below) as specified by 37 C.F.R. 1.97(e). Although no fee is believed due, if any fee is deemed due in connection with this submission, please charge such fee to Deposit Account 19-1970. OR ☐ Please charge Deposit Account 19-1970 in the amount of \$180.00 for the fee set forth in 37 C.F.R. 1.17(p) for submission of an information disclosure statement. Please credit any overpayment or charge any underpayment to Deposit Account 19-1970.
☐	37 CFR 1.97(d): This Information Disclosure Statement is being submitted after the period specified in 37 CFR 1.97(c). ☐ This information Disclosure Statement includes a Certification (below) as specified by 37 C.F.R. 1.97(e) AND ☐ Applicants hereby requests consideration of the reference(s) disclosed herein. Please charge Deposit Account 19-1970 in the amount of \$180.00 under 37 C.F.R. 1.17(p). Please credit any overpayment or charge any underpayment to Deposit Account 19-1970. Election to pay the fee should not be taken as an indication that applicant(s) cannot execute a certification.

Certification (37 C.F.R. 1.97(e))

(Applicable only if checked)



The undersigned certifies that:

☒ Each item of information contained in this information disclosure statement was first cited in any communication from a foreign patent office in a counterpart foreign application not more than three months prior to the filing of this statement, 37 C.F.R. 1.97(e)(1).

☒ A copy of the communication from the foreign patent office is enclosed.

OR

☐ No item of information contained in this information disclosure statement was cited in a communication from a foreign patent office in a counterpart foreign application, and, to the knowledge of the undersigned after making reasonable inquiry, no item of information contained in this Information Disclosure Statement was known to any individual designated in 37 C.F.R. 1.56(c) more than three months prior to the filing of this statement, 37 C.F.R. 1.97(e)(2).

Respectfully submitted,

SHERIDAN ROSS P.C.

By: _____

Jason H. Vick
Registration No. 45,285
1560 Broadway, Suite 1200
Denver, Colorado 80202-5141
(303) 863-9700

Date: 18 Jan '12

Substitute for form 1449A/PTO				Complete if Known	
INFORMATION DISCLOSURE STATEMENT BY APPLICANT				Application Number	12/901,699
				Filing Date	October 11, 2010
				First Named Inventor	Marcos C. Tzannes
				Art Unit	2117
				Examiner Name	Tabone Jr, John J.
Sheet	1	of	1	Attorney Docket Number	5550-54-CON-3

U.S. PATENT DOCUMENTS					
Examiner Initials*	Cite No. ¹	Document Number Number-kind Code ^{2 (if known)}	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear

FOREIGN PATENT DOCUMENTS						
Examiner Initials*	Cite No. ¹	Foreign Patent Document Country Code ³ ; Number ⁴ ; Kind Code ⁵ (if known)	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear	T ⁶
	1	GB 2389493	12/10/2003	NEC CORP		

OTHER ART (Including Author, Title, Date, Pertinent Pages, etc.)		
Examiner Initials*	Cite No. ¹	
	2	Official Action for European Patent Application No. 10000016.5, dated Dec. 22, 2011 (Attorney Ref. No. 5550-57-PEP-DIV-2)

Examiner Signature		Date Considered	

*EXAMINER: Initial if reference is considered, whether or not citation is in conformance and not considered. Include copy of this form with next communication to applicant.

Electronic Acknowledgement Receipt	
EFS ID:	11866536
Application Number:	12901699
International Application Number:	
Confirmation Number:	1676
Title of Invention:	RESOURCE SHARING IN A TELECOMMUNICATIONS ENVIRONMENT
First Named Inventor/Applicant Name:	Marcos C. Tzannes
Customer Number:	62574
Filer:	Jason Vick/Amy Duarte
Filer Authorized By:	Jason Vick
Attorney Docket Number:	5550-54-CON-3
Receipt Date:	18-JAN-2012
Filing Date:	11-OCT-2010
Time Stamp:	17:21:57
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment		no			
File Listing:					
Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1		IDS_06.pdf	335533 f46002ca7b8c180e9308b4b22fcca8e7dbee5b0	yes	4

	Multipart Description/PDF files in .zip description				
	Document Description		Start	End	
	Transmittal Letter		1	3	
	Information Disclosure Statement (IDS) Form (SB08)		4	4	
Warnings:					
Information:					
2	Foreign Reference	GB2389493A.pdf	970749	no	28
			17b7179bab10ac0e84488cbf906fbae564ca4718		
Warnings:					
Information:					
3	Non Patent Literature	5550-57-PEP-DIV-2_OA_2011-12-22.pdf	95779	no	4
			b7a638eb4f8f3af97bbcdf9b81dad58be29cb5f		
Warnings:					
Information:					
4		IDS_07.pdf	329530	yes	4
			26db912057d6038b249d6332b8d7ea8b3b54cc4a		
	Multipart Description/PDF files in .zip description				
	Document Description		Start	End	
	Transmittal Letter		1	3	
	Information Disclosure Statement (IDS) Form (SB08)		4	4	
Warnings:					
Information:					
5	Non Patent Literature	5550-57-PUS_OA_2012-01-05.pdf	504513	no	14
			0f0b5ee21f015db258d58f7f50aa47e1528cf88c		
Warnings:					
Information:					
Total Files Size (in bytes):			2236104		

This Acknowledgement Receipt evidences receipt on the noted date by the USPTO of the indicated documents, characterized by the applicant, and including page counts, where applicable. It serves as evidence of receipt similar to a Post Card, as described in MPEP 503.

New Applications Under 35 U.S.C. 111

If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application.

National Stage of an International Application under 35 U.S.C. 371

If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.

New International Application Filed with the USPTO as a Receiving Office

If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.

Electronic Patent Application Fee Transmittal				
Application Number:		12901699		
Filing Date:		11-Oct-2010		
Title of Invention:		RESOURCE SHARING IN A TELECOMMUNICATIONS ENVIRONMENT		
First Named Inventor/Applicant Name:		Marcos C. Tzannes		
Filer:		Jason Vick/Joanne Vos		
Attorney Docket Number:		5550-54-CON-3		
Filed as Large Entity				
Utility under 35 USC 111(a) Filing Fees				
Description	Fee Code	Quantity	Amount	Sub-Total in USD(\$)
Basic Filing:				
Pages:				
Claims:				
Miscellaneous-Filing:				
Petition:				
Patent-Appeals-and-Interference:				
Post-Allowance-and-Post-Issuance:				
Utility Appl issue fee	1501	1	1740	1740
Publ. Fee- early, voluntary, or normal	1504	1	300	300

Description	Fee Code	Quantity	Amount	Sub-Total in USD(\$)
Extension-of-Time:				
Miscellaneous:				
Total in USD (\$)				2040

Electronic Acknowledgement Receipt	
EFS ID:	13412401
Application Number:	12901699
International Application Number:	
Confirmation Number:	1676
Title of Invention:	RESOURCE SHARING IN A TELECOMMUNICATIONS ENVIRONMENT
First Named Inventor/Applicant Name:	Marcos C. Tzannes
Customer Number:	62574
Filer:	Jason Vick/Joanne Vos
Filer Authorized By:	Jason Vick
Attorney Docket Number:	5550-54-CON-3
Receipt Date:	03-AUG-2012
Filing Date:	11-OCT-2010
Time Stamp:	12:43:09
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	yes
Payment Type	Deposit Account
Payment was successfully received in RAM	\$2040
RAM confirmation Number	9225
Deposit Account	191970
Authorized User	
The Director of the USPTO is hereby authorized to charge indicated fees and credit any overpayment as follows: Charge any Additional Fees required under 37 C.F.R. Section 1.16 (National application filing, search, and examination fees) Charge any Additional Fees required under 37 C.F.R. Section 1.17 (Patent application and reexamination processing fees)	

Charge any Additional Fees required under 37 C.F.R. Section 1.19 (Document supply fees)					
Charge any Additional Fees required under 37 C.F.R. Section 1.20 (Post Issuance fees)					
Charge any Additional Fees required under 37 C.F.R. Section 1.21 (Miscellaneous fees and charges)					
File Listing:					
Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1	Issue Fee Payment (PTO-85B)	Issue_fee_Submission.pdf	161999 139fd2fe4fef3bc57dc3f482efbf3217435d6ca	no	1
Warnings:					
Information:					
2	Post Allowance Communication - Incoming	Comments_on_Reason_for_Allowance.pdf	279515 32fd814dd2f03f73f1152fbaddb26ccfd5368130	no	3
Warnings:					
Information:					
3		Amendment_312.pdf	161764 b0d3009c98f2350b3c04798f1b3d4fda4c97427c	yes	3
	Multipart Description/PDF files in .zip description				
	Document Description		Start	End	
	Amendment after Notice of Allowance (Rule 312)		1	1	
	Specification		2	2	
	Applicant Arguments/Remarks Made in an Amendment		3	3	
Warnings:					
Information:					
4	Miscellaneous Incoming Letter	Request_for_Consideration_of_IDS.pdf	673978 3ac5ecd2a7ad0ff45693d4792f04b9d05ea8d6ef	no	10
Warnings:					
Information:					
5	Fee Worksheet (SB06)	fee-info.pdf	31852 a2077768b1b1a2506da54639b1213947e7a26fdc	no	2
Warnings:					
Information:					
Total Files Size (in bytes):			1309108		

This Acknowledgement Receipt evidences receipt on the noted date by the USPTO of the indicated documents, characterized by the applicant, and including page counts, where applicable. It serves as evidence of receipt similar to a Post Card, as described in MPEP 503.

New Applications Under 35 U.S.C. 111

If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application.

National Stage of an International Application under 35 U.S.C. 371

If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.

New International Application Filed with the USPTO as a Receiving Office

If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.



UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

NOTICE OF ALLOWANCE AND FEE(S) DUE

62574 7590 07/27/2012
Jason H. Vick
Sheridan Ross, PC
Suite # 1200
1560 Broadway
Denver, CO 80202

EXAMINER

TABONE JR, JOHN J

ART UNIT

PAPER NUMBER

2117

DATE MAILED: 07/27/2012

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
12/901,699	10/11/2010	Marcos C. Tzannes	5550-54-CON-3	1676

TITLE OF INVENTION: RESOURCE SHARING IN A TELECOMMUNICATIONS ENVIRONMENT

APPLN. TYPE	SMALL ENTITY	ISSUE FEE DUE	PUBLICATION FEE DUE	PREV. PAID ISSUE FEE	TOTAL FEE(S) DUE	DATE DUE
nonprovisional	NO	\$1740	\$300	\$0	\$2040	10/29/2012

THE APPLICATION IDENTIFIED ABOVE HAS BEEN EXAMINED AND IS ALLOWED FOR ISSUANCE AS A PATENT. PROSECUTION ON THE MERITS IS CLOSED. THIS NOTICE OF ALLOWANCE IS NOT A GRANT OF PATENT RIGHTS. THIS APPLICATION IS SUBJECT TO WITHDRAWAL FROM ISSUE AT THE INITIATIVE OF THE OFFICE OR UPON PETITION BY THE APPLICANT. SEE 37 CFR 1.313 AND MPEP 1308.

THE ISSUE FEE AND PUBLICATION FEE (IF REQUIRED) MUST BE PAID WITHIN THREE MONTHS FROM THE MAILING DATE OF THIS NOTICE OR THIS APPLICATION SHALL BE REGARDED AS ABANDONED. THIS STATUTORY PERIOD CANNOT BE EXTENDED. SEE 35 U.S.C. 151. THE ISSUE FEE DUE INDICATED ABOVE DOES NOT REFLECT A CREDIT FOR ANY PREVIOUSLY PAID ISSUE FEE IN THIS APPLICATION. IF AN ISSUE FEE HAS PREVIOUSLY BEEN PAID IN THIS APPLICATION (AS SHOWN ABOVE), THE RETURN OF PART B OF THIS FORM WILL BE CONSIDERED A REQUEST TO REAPPLY THE PREVIOUSLY PAID ISSUE FEE TOWARD THE ISSUE FEE NOW DUE.

HOW TO REPLY TO THIS NOTICE:

I. Review the SMALL ENTITY status shown above.

If the SMALL ENTITY is shown as YES, verify your current SMALL ENTITY status:

A. If the status is the same, pay the TOTAL FEE(S) DUE shown above.

B. If the status above is to be removed, check box 5b on Part B - Fee(s) Transmittal and pay the PUBLICATION FEE (if required) and twice the amount of the ISSUE FEE shown above, or

If the SMALL ENTITY is shown as NO:

A. Pay TOTAL FEE(S) DUE shown above, or

B. If applicant claimed SMALL ENTITY status before, or is now claiming SMALL ENTITY status, check box 5a on Part B - Fee(s) Transmittal and pay the PUBLICATION FEE (if required) and 1/2 the ISSUE FEE shown above.

II. PART B - FEE(S) TRANSMITTAL, or its equivalent, must be completed and returned to the United States Patent and Trademark Office (USPTO) with your ISSUE FEE and PUBLICATION FEE (if required). If you are charging the fee(s) to your deposit account, section "4b" of Part B - Fee(s) Transmittal should be completed and an extra copy of the form should be submitted. If an equivalent of Part B is filed, a request to reapply a previously paid issue fee must be clearly made, and delays in processing may occur due to the difficulty in recognizing the paper as an equivalent of Part B.

III. All communications regarding this application must give the application number. Please direct all communications prior to issuance to Mail Stop ISSUE FEE unless advised to the contrary.

IMPORTANT REMINDER: Utility patents issuing on applications filed on or after Dec. 12, 1980 may require payment of maintenance fees. It is patentee's responsibility to ensure timely payment of maintenance fees when due.

PART B - FEE(S) TRANSMITTAL

Complete and send this form, together with applicable fee(s), to: **Mail Stop ISSUE FEE**
Commissioner for Patents
P.O. Box 1450
Alexandria, Virginia 22313-1450
or Fax **(571)-273-2885**

INSTRUCTIONS: This form should be used for transmitting the ISSUE FEE and PUBLICATION FEE (if required). Blocks 1 through 5 should be completed where appropriate. All further correspondence including the Patent, advance orders and notification of maintenance fees will be mailed to the current correspondence address as indicated unless corrected below or directed otherwise in Block 1, by (a) specifying a new correspondence address; and/or (b) indicating a separate "FEE ADDRESS" for maintenance fee notifications.

CURRENT CORRESPONDENCE ADDRESS (Note: Use Block 1 for any change of address)

62574 7590 07/27/2012
Jason H. Vick
Sheridan Ross, PC
Suite # 1200
1560 Broadway
Denver, CO 80202

Note: A certificate of mailing can only be used for domestic mailings of the Fee(s) Transmittal. This certificate cannot be used for any other accompanying papers. Each additional paper, such as an assignment or formal drawing, must have its own certificate of mailing or transmission.

Certificate of Mailing or Transmission

I hereby certify that this Fee(s) Transmittal is being deposited with the United States Postal Service with sufficient postage for first class mail in an envelope addressed to the Mail Stop ISSUE FEE address above, or being facsimile transmitted to the USPTO (571) 273-2885, on the date indicated below.

(Depositor's name)
(Signature)
(Date)

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
12/901,699	10/11/2010	Marcos C. Tzannes	5550-54-CON-3	1676

TITLE OF INVENTION: RESOURCE SHARING IN A TELECOMMUNICATIONS ENVIRONMENT

APPLN. TYPE	SMALL ENTITY	ISSUE FEE DUE	PUBLICATION FEE DUE	PREV. PAID ISSUE FEE	TOTAL FEE(S) DUE	DATE DUE
nonprovisional	NO	\$1740	\$300	\$0	\$2040	10/29/2012

EXAMINER	ART UNIT	CLASS-SUBCLASS
TABONE JR, JOHN J	2117	714-774000

1. Change of correspondence address or indication of "Fee Address" (37 CFR 1.563).

- ☐ Change of correspondence address (or Change of Correspondence Address form PTO/SB/122) attached.
☐ "Fee Address" indication (or "Fee Address" Indication form PTO/SB/47; Rev 03-02 or more recent) attached. Use of a Customer Number is required.

2. For printing on the patent front page, list

- (1) the names of up to 3 registered patent attorneys or agents OR, alternatively,
(2) the name of a single firm (having as a member a registered attorney or agent) and the names of up to 3 registered patent attorneys or agents. If no name is listed, no name will be printed.

1 _____
2 _____
3 _____

3. ASSIGNEE NAME AND RESIDENCE DATA TO BE PRINTED ON THE PATENT (print or type)

PLEASE NOTE: Unless an assignee is identified below, no assignee data will appear on the patent. If an assignee is identified below, the document has been filed for recordation as set forth in 37 CFR 3.11. Completion of this form is NOT a substitute for filing an assignment.

(A) NAME OF ASSIGNEE

(B) RESIDENCE: (CITY and STATE OR COUNTRY)

Please check the appropriate assignee category or categories (will not be printed on the patent): ☐ Individual ☐ Corporation or other private group entity ☐ Government

4a. The following fee(s) are submitted:

- ☐ Issue Fee
☐ Publication Fee (No small entity discount permitted)
☐ Advance Order - # of Copies _____

4b. Payment of Fee(s): (Please first reapply any previously paid issue fee shown above)

- ☐ A check is enclosed.
☐ Payment by credit card. Form PTO-2038 is attached.
☐ The Director is hereby authorized to charge the required fee(s), any deficiency, or credit any overpayment, to Deposit Account Number _____ (enclose an extra copy of this form).

5. Change in Entity Status (from status indicated above)

- ☐ a. Applicant claims SMALL ENTITY status. See 37 CFR 1.27. ☐ b. Applicant is no longer claiming SMALL ENTITY status. See 37 CFR 1.27(g)(2).

NOTE: The Issue Fee and Publication Fee (if required) will not be accepted from anyone other than the applicant; a registered attorney or agent; or the assignee or other party in interest as shown by the records of the United States Patent and Trademark Office.

Authorized Signature _____ Date _____
Typed or printed name _____ Registration No. _____

This collection of information is required by 37 CFR 1.311. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 12 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, Virginia 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, Virginia 22313-1450.

Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it displays a valid OMB control number.



UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
12/901,699	10/11/2010	Marcos C. Tzannes	5550-54-CON-3	1676
62574	7590	07/27/2012	EXAMINER	
Jason H. Vick Sheridan Ross, PC Suite # 1200 1560 Broadway Denver, CO 80202			TABONE JR, JOHN J	
			ART UNIT	PAPER NUMBER
			2117	
DATE MAILED: 07/27/2012				

Determination of Patent Term Adjustment under 35 U.S.C. 154 (b)
(application filed on or after May 29, 2000)

The Patent Term Adjustment to date is 0 day(s). If the issue fee is paid on the date that is three months after the mailing date of this notice and the patent issues on the Tuesday before the date that is 28 weeks (six and a half months) after the mailing date of this notice, the Patent Term Adjustment will be 0 day(s).

If a Continued Prosecution Application (CPA) was filed in the above-identified application, the filing date that determines Patent Term Adjustment is the filing date of the most recent CPA.

Applicant will be able to obtain more detailed information by accessing the Patent Application Information Retrieval (PAIR) WEB site (<http://pair.uspto.gov>).

Any questions regarding the Patent Term Extension or Adjustment determination should be directed to the Office of Patent Legal Administration at (571)-272-7702. Questions relating to issue and publication fee payments should be directed to the Customer Service Center of the Office of Patent Publication at 1-(888)-786-0101 or (571)-272-4200.

Privacy Act Statement

The Privacy Act of 1974 (P.L. 93-579) requires that you be given certain information in connection with your submission of the attached form related to a patent application or patent. Accordingly, pursuant to the requirements of the Act, please be advised that: (1) the general authority for the collection of this information is 35 U.S.C. 2(b)(2); (2) furnishing of the information solicited is voluntary; and (3) the principal purpose for which the information is used by the U.S. Patent and Trademark Office is to process and/or examine your submission related to a patent application or patent. If you do not furnish the requested information, the U.S. Patent and Trademark Office may not be able to process and/or examine your submission, which may result in termination of proceedings or abandonment of the application or expiration of the patent.

The information provided by you in this form will be subject to the following routine uses:

1. The information on this form will be treated confidentially to the extent allowed under the Freedom of Information Act (5 U.S.C. 552) and the Privacy Act (5 U.S.C. 552a). Records from this system of records may be disclosed to the Department of Justice to determine whether disclosure of these records is required by the Freedom of Information Act.
2. A record from this system of records may be disclosed, as a routine use, in the course of presenting evidence to a court, magistrate, or administrative tribunal, including disclosures to opposing counsel in the course of settlement negotiations.
3. A record in this system of records may be disclosed, as a routine use, to a Member of Congress submitting a request involving an individual, to whom the record pertains, when the individual has requested assistance from the Member with respect to the subject matter of the record.
4. A record in this system of records may be disclosed, as a routine use, to a contractor of the Agency having need for the information in order to perform a contract. Recipients of information shall be required to comply with the requirements of the Privacy Act of 1974, as amended, pursuant to 5 U.S.C. 552a(m).
5. A record related to an International Application filed under the Patent Cooperation Treaty in this system of records may be disclosed, as a routine use, to the International Bureau of the World Intellectual Property Organization, pursuant to the Patent Cooperation Treaty.
6. A record in this system of records may be disclosed, as a routine use, to another federal agency for purposes of National Security review (35 U.S.C. 181) and for review pursuant to the Atomic Energy Act (42 U.S.C. 218(c)).
7. A record from this system of records may be disclosed, as a routine use, to the Administrator, General Services, or his/her designee, during an inspection of records conducted by GSA as part of that agency's responsibility to recommend improvements in records management practices and programs, under authority of 44 U.S.C. 2904 and 2906. Such disclosure shall be made in accordance with the GSA regulations governing inspection of records for this purpose, and any other relevant (i.e., GSA or Commerce) directive. Such disclosure shall not be used to make determinations about individuals.
8. A record from this system of records may be disclosed, as a routine use, to the public after either publication of the application pursuant to 35 U.S.C. 122(b) or issuance of a patent pursuant to 35 U.S.C. 151. Further, a record may be disclosed, subject to the limitations of 37 CFR 1.14, as a routine use, to the public if the record was filed in an application which became abandoned or in which the proceedings were terminated and which application is referenced by either a published application, an application open to public inspection or an issued patent.
9. A record from this system of records may be disclosed, as a routine use, to a Federal, State, or local law enforcement agency, if the USPTO becomes aware of a violation or potential violation of law or regulation.

Notice of Allowability	Application No.	Applicant(s)	
	12/901,699	TZANNES ET AL.	
	Examiner	Art Unit	
	JOHN J. TABONE JR	2117	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address--

All claims being allowable, PROSECUTION ON THE MERITS IS (OR REMAINS) CLOSED in this application. If not included herewith (or previously mailed), a Notice of Allowance (PTOL-85) or other appropriate communication will be mailed in due course. **THIS NOTICE OF ALLOWABILITY IS NOT A GRANT OF PATENT RIGHTS.** This application is subject to withdrawal from issue at the initiative of the Office or upon petition by the applicant. See 37 CFR 1.313 and MPEP 1308.

1. ☒ This communication is responsive to amendments, arguments and Terminal Disclaimers filed 07/05/2012.

2. ☐ An election was made by the applicant in response to a restriction requirement set forth during the interview on ____; the restriction requirement and election have been incorporated into this action.

3. ☒ The allowed claim(s) is/are 46-53, renumbered to 1-8.

4. ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
 a) ☐ All b) ☐ Some* c) ☐ None of the:
 1. ☐ Certified copies of the priority documents have been received.
 2. ☐ Certified copies of the priority documents have been received in Application No. _____.
 3. ☐ Copies of the certified copies of the priority documents have been received in this national stage application from the International Bureau (PCT Rule 17.2(a)).
 * Certified copies not received: _____.

Applicant has **THREE MONTHS FROM THE "MAILING DATE"** of this communication to file a reply complying with the requirements noted below. Failure to timely comply will result in ABANDONMENT of this application.
THIS THREE-MONTH PERIOD IS NOT EXTENDABLE.

5. ☐ A SUBSTITUTE OATH OR DECLARATION must be submitted. Note the attached EXAMINER'S AMENDMENT or NOTICE OF INFORMAL PATENT APPLICATION (PTO-152) which gives reason(s) why the oath or declaration is deficient.

6. ☐ CORRECTED DRAWINGS (as "replacement sheets") must be submitted.
 (a) ☐ including changes required by the Notice of Draftsperson's Patent Drawing Review (PTO-948) attached
 1) ☐ hereto or 2) ☐ to Paper No./Mail Date _____.
 (b) ☐ including changes required by the attached Examiner's Amendment / Comment or in the Office action of Paper No./Mail Date _____.
Identifying indicia such as the application number (see 37 CFR 1.84(c)) should be written on the drawings in the front (not the back) of each sheet. Replacement sheet(s) should be labeled as such in the header according to 37 CFR 1.121(d).

7. ☐ DEPOSIT OF and/or INFORMATION about the deposit of BIOLOGICAL MATERIAL must be submitted. Note the attached Examiner's comment regarding REQUIREMENT FOR THE DEPOSIT OF BIOLOGICAL MATERIAL.

Attachment(s)

1. ☐ Notice of References Cited (PTO-892) 2. ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948) 3. ☒ Information Disclosure Statements (PTO/SB/08), Paper No./Mail Date _____ 4. ☐ Examiner's Comment Regarding Requirement for Deposit of Biological Material	5. ☐ Notice of Informal Patent Application 6. ☐ Interview Summary (PTO-413), Paper No./Mail Date _____. 7. ☐ Examiner's Amendment/Comment 8. ☒ Examiner's Statement of Reasons for Allowance 9. ☐ Other _____.

/JOHN J TABONE JR/ Primary Examiner, Art Unit 2117 07/20/12	

DETAILED ACTION

1. Claims 46-53 are currently pending in the application and have been examined. Claims 1-45 have been cancelled. Claims 46-53 are newly added in a Preliminary amendment filed 10/11/2010.
2. The objections to the Specification and claims as well as the 35 USC § 112, second paragraph rejections have been withdrawn in light of amendments and arguments filed 07/05/2012.
3. The nonstatutory obviousness-type double patenting rejections have been withdrawn due to the filing of the Terminal Disclaimers

Information Disclosure Statement

4. The information disclosure statements (IDSs) submitted on 01/18/2012, 02/29/2012, 05/01/2012, 05/24/2012 and 06/19/2012 are in compliance with the provisions of 37 CFR 1.97. Accordingly, the information disclosure statements are being considered by the examiner.

Allowable Subject Matter

5. **Claims 46 and 50** would be allowable if rewritten or amended to overcome the rejection(s) under 35 U.S.C. 112, 2nd paragraph, as well as the Double Patenting rejections, set forth in this Office action.

The following is a statement of reasons for the indication of allowable subject matter:

The present invention relates to communication systems. More specifically, an exemplary embodiment of this invention relates to memory sharing in communication systems. Another exemplary embodiment relates to processing or coding resource sharing in a communication system.

The claimed invention as set forth in **claim 46** recites features such as:

A system that allocates shared memory comprising:

a transceiver that is capable of:

transmitting or receiving a message during initialization specifying a maximum number of bytes of memory that are available to be allocated to an interleaver;

determining an amount of memory required by the interleaver to interleave a first plurality of Reed Solomon (RS) coded data bytes within the shared memory;

allocating a first number of bytes of the shared memory to the interleaver to interleave the first plurality of Reed Solomon (RS) coded data bytes for transmission at a first data rate, wherein the allocated memory for the interleaver does not exceed the maximum number of bytes specified in the message;

allocating a second number of bytes of the shared memory to a deinterleaver to deinterleave a second plurality of RS coded data bytes received at a second data rate;
and

interleaving the first plurality of RS coded data bytes within the shared memory allocated to the interleaver and deinterleaving the second plurality of RS coded data

bytes within the shared memory allocated to the deinterleaver, wherein the shared memory allocated to the interleaver is used at the same time as the shared memory allocated to the deinterleaver.

The prior arts of record, namely **Fadavi-Ardekani et al.** (US-6707822), teach sharing a memory between the interleavers and deinterleavers of multiple Asymmetrical Digital Subscriber Line (ADSL) sessions. (Abstract).

The prior arts of record, however, fail to teach, singly or in combination, the claimed invention as a whole, especially *transmitting or receiving a message during initialization specifying a maximum number of bytes of memory that are available to be allocated to an interleaver*. As such, modification of the prior art of record to include the claimed invention as a whole, especially *transmitting or receiving a message during initialization specifying a maximum number of bytes of memory that are available to be allocated to an interleaver* can only be motivated by hindsight reasoning, or by changing the intended use and function of the prior art themselves. Therefore, it is not clear that one of ordinary skill in the art at the time of the invention would have made the necessary modifications to the prior art of record to encompass the invention as a whole, especially *transmitting or receiving a message during initialization specifying a maximum number of bytes of memory that are available to be allocated to an interleaver* set forth in the present application. Moreover, none of the prior arts of record, taken either alone or in combination, anticipate nor render obvious the invention as a whole, especially *transmitting or receiving a message during initialization specifying a*

maximum number of bytes of memory that are available to be allocated to an interleaver as set forth in **claim 46**. Independent **claim 50** recite similar patentable features and are allowable for the same reasons as **claim 46**. Hence, **claims 46-53** are allowable over the prior arts of record.

The Examiner favors the allowance of **claims 46-53**. Any comments considered necessary by applicant must be submitted no later than the payment of the Issue Fee and, to avoid processing delays, should preferably accompany the Issue Fee. Such submissions should be clearly labeled "Comments on Statement of Reasons for Allowance."

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to JOHN J. TABONE JR whose telephone number is (571)272-3827. The examiner can normally be reached on M-F.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Ajay Bhatia can be reached on (571) 272-3906. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/JOHN J TABONE JR/
Primary Examiner, Art Unit 2117
07/20/2012

Search Notes 	Application/Control No. 12901699	Applicant(s)/Patent Under Reexamination TZANNES ET AL.
	Examiner JOHN J TABONE JR	Art Unit 2117

SEARCHED			
Class	Subclass	Date	Examiner
714	774, 784	7/20/12	JJT
375	222	7/20/12	JJT
711	147, 157	7/20/12	JJT
709	215	7/20/12	JJT

SEARCH NOTES		
Search Notes	Date	Examiner
Assignee and Inventor Search. DP found. See OA for details.	12/31/2011	JJT
714/748,776,774,784 711/170,147,153,157,173 375/222 379/93.01 709/215 (text search only - see search history printout).	01/02/2012	JJT
714/748,776,774,784 711/170,147,153,157,173 375/222 379/93.01 709/215 (text search only - see search history printout). UPDATED.	7/20/12	JJT
Google Search. (maximum number of bytes "shared memory" interleaver deinterleaver)	7/20/12	JJT

INTERFERENCE SEARCH			
Class	Subclass	Date	Examiner
	Interference Search History Printout.	7/20/12	JJT

	/JOHN J TABONE JR/ Primary Examiner.Art Unit 2117

EAST Search History

EAST Search History (Prior Art)

Ref #	Hits	Search Query	DBs	Default Operator	Plurals	Time Stamp
S35	2	"7865796".pn.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2012/07/20 15:57
S33	9	(transceiver same (message stream data) with (allocat\$4 specify\$3 reconfigur\$5) near8 (memory buffer register) with (interleaver deinterleaver retransmission) and (interleav\$3 near5 (byte data)))	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2012/07/20 15:18
S32	8	S30 and S31	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2012/07/20 15:16
S31	9	transceiver same (message stream data) with (allocat\$4 specify\$3 reconfigur\$5) near8 (memory buffer register) with (interleaver deinterleaver retransmission)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2012/07/20 15:16
S30	19641	(714/748,776,774,784 711/170,147,153,157,173 375/222 379/93.01 709/215).ccls.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2012/07/20 15:16
S29	3	"6707822".pn.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2012/07/20 14:50
S28	4	("6775320" "6778596").pn.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2012/01/02 12:20
S27	6	transceiver same (message stream data) with (allocat\$4 specify\$3 reconfigur\$5) near8 (memory buffer register) with (interleaver deinterleaver)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2012/01/02 12:17
S26	9	transceiver same (message stream data) with (allocat\$4 specify\$3	US-PGPUB; USPAT;	OR	ON	2012/01/02 12:17

EAST Search History

		reconfigur\$5) near8 (memory buffer register) with (interleaver deinterleaver retransmission)	USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB			
S25	6	S22 and S23	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2012/01/01 20:59
S23	186	(shar\$3 near4 memory) and (packet near3 retransmission) and (interleav\$3 deinterleav\$3 de-interleav\$3)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2012/01/01 20:59
S22	187	(Tzannes-Marcos-C\$ Lund-Michael).in.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2012/01/01 20:58
S21	1	transceiver same (message stream data) with (allocat\$4 specify\$3) near8 (memory buffer) with (interleaver deinterleaver) and (allocat\$4 specify\$3) near8 ((memory buffer) near8 retransmission)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2012/01/01 14:45
S20	1	transceiver same (message stream data) with (allocat\$4 specify\$3) near8 (memory buffer) with (interleaver deinterleaver) same2 (allocat\$4 specify\$3) near8 ((memory buffer) near8 retransmission)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2012/01/01 14:42
S19	9	transceiver same (message stream data) with (allocat\$4 specify\$3) near8 (memory buffer) with (interleaver deinterleaver retransmission)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2012/01/01 14:34
S18	1	12/901699	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2011/12/31 14:40
S17	6	S14 and S15	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2011/12/31 14:34
S16	6	S13 and S15	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2011/12/31 14:34
S15	186	(shar\$3 near4 memory) and (packet near3 retransmission) and (interleav\$3	US-PGPUB; USPAT;	OR	ON	2011/12/31 14:34

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EAST Search History

		deinterleav\$3 de-interleav\$3)	USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB			
S14	174	(Tzannes-Marcos-Ç\$).in.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2011/12/31 14:32
S13	542	AWARE.as.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2011/12/31 14:31
S12	13	S10 not S11	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2011/12/31 13:04
S11	8	S9 and S8	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2011/12/31 13:03
S10	18	S9 and S4	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2011/12/31 13:03
S9	18525	(714/748,776,774,784 711/170,147,153,157,173 375/222 379/93.01 709/215).ccls.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2011/12/31 13:03
S8	9	transceiver same (message stream data) with (allocat\$4 specify\$3) near8 memory with (interleaver deinterleaver retransmission)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2011/12/31 12:53
S7	18	S4 and transceiver	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2011/12/31 12:43
S6	10	(allocat\$4 specify\$3) near8 shar\$3 near2 memory with (interleaver deinterleaver)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2011/12/31 12:42
S5	10	(allocat\$4 specify\$3) near8 shared near2 memory with (interleaver	US-PGPUB; USPAT;	OR	ON	2011/12/31 12:40

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EAST Search History

		deinterleaver)	USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB			
S4	63	(allocat\$4 specify\$3) near8 memory with (interleaver deinterleaver)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2011/12/31 12:40
S3	20	("20060088054" "7836381" "20020154600" "6707822" "6778596" "5663910" "6778589" "20030067877" "6337877" "6775320").PN.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2011/12/31 12:36
S2	7	11/246163	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2011/12/21 16:10
S1	1	12/295828	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2011/12/21 16:08

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Receipt date: 02/29/2012

Substitute for form 1449A/PTO INFORMATION DISCLOSURE STATEMENT BY APPLICANT				Complete if Known	
				Application Number	12/901,699
				Filing Date	October 11, 2010
				First Named Inventor	Marcos C. Tzannes
				Art Unit	2117
				Examiner Name	Tabone Jr, John J.
Sheet	1	of	2	Attorney Docket Number	5550-54-CON-3

U.S. PATENT DOCUMENTS					
Examiner Initials*	Cite No. ¹	Document Number Number-kind Code ^{2 (if known)}	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear
	1	7200792	04-03-2007	Kim et al.	
	2	2001/0014962	08-16-2001	Obuchi et al.	

FOREIGN PATENT DOCUMENTS						
Examiner Initials*	Cite No. ¹	Foreign Patent Document Country Code ³ ; Number ⁴ ; Kind Code ⁵ (if known)	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear	T ⁶
	3	JP 07-254862	10-03-1995	Sony CORP.		(includes English abstract and partial mechanical translation)
	4	JP 2003-224615	08-08-2003	SAMSUNG ELECTRONICS CO LTD.		(corresponds to US 7,200,792 cited herein)
	5	JP 2005-522963	07-28-2005	INTERDIGITAL TECHNOLOGY CORPORATION		(corresponds to WO 03/090011 cited herein)
	6	WO00/52834	10-30-2003	FUJITSU LIMITED		(corresponds to US2001/0014962 cited herein)
	7	WO 03/090011	10-30-2003	INTERDIGITAL TECHNOLOGY CORPORATION		
	8	EP 1041756	10-04-2000	LUCENT TECHNOLOGIES INC.		(corresponds to JP 2000-341247 previously cited by Applicants on 10-17-2011)

Examiner Signature	/John J. Tabone Jr. / (07/20/2012)	Date Considered	

*EXAMINER: Initial if reference is considered, whether or not citation is in conformance and not considered. Include copy of this form with next communication to applicant.

ALL REFERENCES CONSIDERED EXCEPT WHERE LINED THROUGH. /JJT/

Receipt date: 02/29/2012

Substitute for form 1449A/PTO INFORMATION DISCLOSURE STATEMENT BY APPLICANT				Complete if Known	
				Application Number	12/901,699
				Filing Date	October 11, 2010
				First Named Inventor	Marcos C. Tzannes
				Art Unit	2117
				Examiner Name	Tabone Jr, John J.
				Attorney Docket Number	5550-54-CON-3
Sheet	2	of	2		

OTHER ART (Including Author, Title, Date, Pertinent Pages, etc.)		
Examiner Initials*	Cite No. ¹	
	9	Official Action (including translation) for Japanese Patent Application No. 2008-264540, dispatched Dec. 12, 2011 (Attorney Ref. No. 5550-54-PJP-DIV)

Examiner Signature	/John J. Tabone Jr. / (07/20/2012)	Date Considered	

*EXAMINER: Initial if reference is considered, whether or not citation is in conformance and not considered. Include copy of this form with next communication to applicant.

ALL REFERENCES CONSIDERED EXCEPT WHERE LINED THROUGH. /JJT/

Receipt date: 01/18/2012

Substitute for form 1449A/PTO INFORMATION DISCLOSURE STATEMENT BY APPLICANT				Complete if Known	
				Application Number	12/901,699
				Filing Date	October 11, 2010
				First Named Inventor	Marcos C. Tzannes
				Art Unit	2117
				Examiner Name	Tabone Jr, John J.
Sheet	1	of	1	Attorney Docket Number	5550-54-CON-3

U.S. PATENT DOCUMENTS					
Examiner Initials*	Cite No. ¹	Document Number Number-kind Code ² (if known)	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear

FOREIGN PATENT DOCUMENTS						
Examiner Initials*	Cite No. ¹	Foreign Patent Document Country Code ³ ; Number ⁴ ; Kind Code ⁵ (if known)	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear	T ⁶

OTHER ART (Including Author, Title, Date, Pertinent Pages, etc.)		
Examiner Initials*	Cite No. ¹	
/JJT/	1	Official Action for U.S. Patent Application No. 12/295,828, mailed Jan. 5, 2012 (Attorney Ref. No. 5550-57-PUS)

Examiner Signature	/John J. Tabone Jr. / (07/20/2012)	Date Considered	

*EXAMINER: Initial if reference is considered, whether or not citation is in conformance and not considered. Include copy of this form with next communication to applicant.

Receipt date: 06/19/2012

Substitute for form 1449A/PTO INFORMATION DISCLOSURE STATEMENT BY APPLICANT				Complete if Known	
				Application Number	12/901,699
				Filing Date	October 11, 2010
				First Named Inventor	Marcos C. Tzannes
				Art Unit	2117
				Examiner Name	Tabone Jr, John J.
Sheet	1	of	1	Attorney Docket Number	5550-54-CON-3

U.S. PATENT DOCUMENTS					
Examiner Initials*	Cite No. ¹	Document Number Number-kind Code ² (if known)	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear

FOREIGN PATENT DOCUMENTS						
Examiner Initials*	Cite No. ¹	Foreign Patent Document Country Code ³ ; Number ⁴ ; Kind Code ⁵ (if known)	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear	T ⁶

OTHER ART (Including Author, Title, Date, Pertinent Pages, etc.)		
Examiner Initials*	Cite No. ¹	
/JJT/	1	Official Notification of Intent to Grant (including translation) for Mexican Patent Application No. MX/a/2008/012505, mailed April 3, 2012 (Attorney Ref. No.: 5550-57-PMX)

Examiner Signature	/John J. Tabone Jr. / (07/20/2012)	Date Considered	

*EXAMINER: Initial if reference is considered, whether or not citation is in conformance and not considered. Include copy of this form with next communication to applicant.

Receipt date: 05/01/2012

Substitute for form 1449A/PTO INFORMATION DISCLOSURE STATEMENT BY APPLICANT				Complete if Known	
				Application Number	12/901,699
				Filing Date	October 11, 2010
				First Named Inventor	Marcos C. Tzannes
				Art Unit	2117
				Examiner Name	Tabone Jr, John J.
Sheet	1	of	1	Attorney Docket Number	5550-54-CON-3

U.S. PATENT DOCUMENTS					
Examiner Initials*	Cite No. ¹	Document Number Number-kind Code ^{2 (if known)}	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear
	1	6826589	11-30-2004	Berrada	

FOREIGN PATENT DOCUMENTS						
Examiner Initials*	Cite No. ¹	Foreign Patent Document Country Code ³ ; Number ⁴ ; Kind Code ^{5 (if known)}	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear	T ⁶
	2	KR10-2000-0047827	07-25-2000	KONINCLIKE PHILIPS ELECTRONICS		(corresponds to US 6,826,589 cited herein)

OTHER ART (Including Author, Title, Date, Pertinent Pages, etc.)		
Examiner Initials*	Cite No. ¹	
	3	Notice of Allowance (including translation) for Korean Patent Application No. 10-2007-7008270, mailed March 29, 2012 (Attorney Ref. No.: 5550-54-PKR)
	4	Notice of Allowance (including translation) for Korean Patent Application No. 10-2010-7022463, mailed March 29, 2012 (Attorney Ref. No.: 5550-54-PKR-DIV)
	5	Notice of Allowance for Japanese Patent Application No. 2008-264540, mailed March 26, 2012 (Attorney Ref. No.: 5550-54-PJP-DIV)
	6	Notification of the Second Office Action (including translation) for Chinese Patent Application No. 200780012891.0, dispatched March 7, 2012 (Attorney Ref. No.: 5550-57-PCN)

Examiner Signature	/John J. Tabone Jr. / (07/20/2012)	Date Considered	

*EXAMINER: Initial if reference is considered, whether or not citation is in conformance and not considered. Include copy of this form with next communication to applicant.

ALL REFERENCES CONSIDERED EXCEPT WHERE LINED THROUGH. /JJT/

Receipt date: 05/24/2012

Substitute for form 1449A/PTO INFORMATION DISCLOSURE STATEMENT BY APPLICANT				Complete if Known	
				Application Number	12/901,699
				Filing Date	October 11, 2010
				First Named Inventor	Marcos C. Tzannes
				Art Unit	2117
				Examiner Name	Tabone Jr, John J.
Sheet	1	of	1	Attorney Docket Number	5550-54-CON-3

U.S. PATENT DOCUMENTS					
Examiner Initials*	Cite No. ¹	Document Number Number-kind Code ² (if known)	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear
	1	5524116	06-04-1996	Kalmanek, Jr., et al.	
	2	6098188	08-01-2000	Kalmanek, Jr., et al.	
	3	7164654	01-16-2007	Hunzinger et al.	
	4	7782758	08-24-2010	Wydrowski et al.	

FOREIGN PATENT DOCUMENTS						
Examiner Initials*	Cite No. ¹	Foreign Patent Document Country Code ³ ; Number ⁴ ; Kind Code ⁵ (if known)	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear	T ⁶

OTHER ART (Including Author, Title, Date, Pertinent Pages, etc.)		
Examiner Initials*	Cite No. ¹	
	5	Official Action for U.S. Patent Application No. 12/760,728, mailed April 27, 2012 (Attorney Ref. No.: 5550-57-PUS-DIV)
	6	Official Action for U.S. Patent Application No. 12/783,765, mailed May 17, 2012 (Attorney Ref. No. 5550-57-PUS-DIV-CON)

Examiner Signature	/John J. Tabone Jr. / (07/20/2012)	Date Considered	

*EXAMINER: Initial if reference is considered, whether or not citation is in conformance and not considered. Include copy of this form with next communication to applicant.

ALL REFERENCES CONSIDERED EXCEPT WHERE LINED THROUGH. /JJT/

Receipt date: 05/24/2012

Substitute for form 1449A/PTO INFORMATION DISCLOSURE STATEMENT BY APPLICANT				Complete if Known	
				Application Number	12/901,699
				Filing Date	October 11, 2010
				First Named Inventor	Marcos C. Tzannes
				Art Unit	2117
				Examiner Name	Tabone Jr, John J.
Sheet	1	of	1	Attorney Docket Number	5550-54-CON-3

U.S. PATENT DOCUMENTS					
Examiner Initials*	Cite No. ¹	Document Number Number-kind Code ² (if known)	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear

FOREIGN PATENT DOCUMENTS					
Examiner Initials*	Cite No. ¹	Foreign Patent Document Country Code ³ ; Number ⁴ ; Kind Code ⁵ (if known)	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear

OTHER ART (Including Author, Title, Date, Pertinent Pages, etc.)		
Examiner Initials*	Cite No. ¹	
/JJT/	1	Official Action (including translation) for Chinese Patent Application No. 200580032703.1, dispatched March 28, 2012 (Attorney Ref. No. 5550-54-PCN)
/JJT/	2	Decision of Final Rejection for Japanese Patent Application No. 2010-017356, dispatched April 23, 2012 (Attorney Ref. No.: 5550-57-PJP-DIV)

Examiner Signature	/John J. Tabone Jr. / (07/20/2012)	Date Considered	

*EXAMINER: Initial if reference is considered, whether or not citation is in conformance and not considered. Include copy of this form with next communication to applicant.

<i>Index of Claims</i> 	Application/Control No. 12901699	Applicant(s)/Patent Under Reexamination TZANNES ET AL.
	Examiner JOHN J TABONE JR	Art Unit 2117

✓	Rejected	-	Cancelled	N	Non-Elected	A	Appeal
=	Allowed	÷	Restricted	I	Interference	O	Objected

☐ Claims renumbered in the same order as presented by applicant				☐ CPA		☐ T.D.		☐ R.1.47	
CLAIM		DATE							
Final	Original	01/02/2012	07/20/2012						
	1	-							
	2	-							
	3	-							
	4	-							
	5	-							
	6	-							
	7	-							
	8	-							
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	33	-							
	34	-							
	35	-							
	36	-							

<i>Index of Claims</i> 	Application/Control No. 12901699	Applicant(s)/Patent Under Reexamination TZANNES ET AL.
	Examiner JOHN J TABONE JR	Art Unit 2117

✓	Rejected	-	Cancelled	N	Non-Elected	A	Appeal
=	Allowed	÷	Restricted	I	Interference	O	Objected

☐ Claims renumbered in the same order as presented by applicant				☐ CPA		☐ T.D.		☐ R.1.47	
CLAIM		DATE							
Final	Original	01/02/2012	07/20/2012						
	37	-							
	38	-							
	39	-							
	40	-							
	41	-							
	42	-							
	43	-							
	44	-							
	45	-							
1	46	✓	=						
2	47	✓	=						
3	48	✓	=						
4	49	✓	=						
5	50	✓	=						
6	51	✓	=						
7	52	✓	=						
8	53	✓	=						

Issue Classification 	Application/Control No. 12901699	Applicant(s)/Patent Under Reexamination TZANNES ET AL.
	Examiner JOHN J TABONE JR	Art Unit 2117

ORIGINAL						INTERNATIONAL CLASSIFICATION										
CLASS			SUBCLASS			CLAIMED					NON-CLAIMED					
714			774			H	0	3	M	13 / 00 (2006.01.01)						
CROSS REFERENCE(S)						H	0	4	B	1 / 38 (2006.01.01)						
						G	0	6	F	13 / 00 (2006.01.01)						
						G	0	6	F	15 / 16 (2006.01.01)						
CLASS	SUBCLASS (ONE SUBCLASS PER BLOCK)															
714	784															
375	222															
711	147	157														
709	215															

☐ Claims renumbered in the same order as presented by applicant ☐ CPA ☐ T.D. ☐ R.1.47															
Final	Original	Final	Original	Final	Original	Final	Original	Final	Original	Final	Original	Final	Original	Final	Original
	1		17		33	4	49								
	2		18		34	5	50								
	3		19		35	6	51								
	4		20		36	7	52								
	5		21		37	8	53								
	6		22		38										
	7		23		39										
	8		24		40										
	9		25		41										
	10		26		42										
	11		27		43										
	12		28		44										
	13		29		45										
	14		30	1	46										
	15		31	2	47										
	16		32	3	48										

NONE (Assistant Examiner) _____ (Date) _____ /JOHN J TABONE JR/ Primary Examiner. Art Unit 2117 (Primary Examiner) _____ (Date) _____		Total Claims Allowed: 8 O.G. Print Claim(s) O.G. Print Figure 1 1	

EAST Search History**EAST Search History (Interference)**

Ref #	Hits	Search Query	DBs	Default Operator	Plurals	Time Stamp
S34	5	(transceiver same (message stream data) with (allocat\$4 specify\$3 reconfigur\$5) near8 (memory buffer register) with (interleaver deinterleaver retransmission) and (interleav\$3 near5 (byte data))).clm.	US- PGPUB; USPAT; UPAD	OR	ON	2012/07/20 15:18

7/ 20/ 2012 5:46:28 PM**C:\Users\jtabone\Documents\EAST\Workspaces\12901699.wsp**

Application Number 	Application/Control No. 12/901,699	Applicant(s)/Patent under Reexamination TZANNES ET AL.	

Document Code - DISQ	Internal Document – DO NOT MAIL

TERMINAL DISCLAIMER	☒ APPROVED	☐ DISAPPROVED
Date Filed : 7/5/12	This patent is subject to a Terminal Disclaimer	

Approved/Disapproved by: Janice Ford three terminals approved

U.S. Patent and Trademark Office

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In Re the Application of: Marcos C. Tzannes	)	Group Art Unit: 2117
Application No.: 12/901,699	)	Examiner: TABONE JR., John J.
Filed: October 11, 2010	)	Confirmation No.: 1676
Atty. File No.: 5550-54-CON-3	)	

For: RESOURCE SHARING IN A TELECOMMUNICATIONS ENVIRONMENT

AMENDMENT AND RESPONSE

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Madam:

Applicants submit this Amendment and Response to address the Office Action having a mailing date of January 6, 2012. Please credit any overpayment or charge any underpayment to Deposit Account No. 19-1970.

Please amend the above-identified patent application as follows:

Amendments to the Specification begin on page 2 of this paper

Amendments to the Claims are shown in the listing of claims which begins on page 4 of this paper.

Remarks begin on page 6 of this paper.

Amendments to the Specification:

Please replace paragraph [0003] with the following:

[0003] U.S. Patent Nos. 6,775,320 and ~~6,778,589~~6,778,596 describe DSL systems supporting multiple applications and multiple framer/coder/interleaver FCI blocks (an FCI block is also referred to as a latency path). DSL systems carry applications that have different transmission requirements with regard to, for example, data rate, latency (delay), bit error rate (BER), and the like. For example, video typically requires a low BER ($<1E-10$) but can tolerate higher latency (>20 ms). Voice, on the other hand, typically requires a low latency (<1 ms) but can tolerate BER ($>1E-3$).

IN THE ABSTRACT:

Please replace the Abstract with the Abstract supplied herewith on a separate sheet.

ABSTRACT

A system allocates shared memory by transmitting/receiving a message specifying a maximum number of bytes of memory that are available to be allocated to an interleaver. The system determines an amount of memory required by the interleaver to interleave a first plurality of RS coded data bytes within a shared memory and allocates a first number of bytes of the shared memory to the interleaver to interleave the first plurality of RS coded data bytes for transmission at a first data rate. The system also allocates a second number of bytes of the shared memory to a deinterleaver to deinterleave a second plurality of RS coded data bytes received at a second data rate and interleaves the first plurality of RS coded data bytes within the shared memory allocated to the interleaver and deinterleaves the second plurality of RS coded data bytes within the shared memory allocated to the deinterleaver.

Amendments to the Claims:

This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims:

1.-45. (Cancelled)

46. (Currently Amended) A system that allocates shared memory comprising:
a transceiver that is capable of:

transmitting or receiving a message during initialization specifying a maximum number
of bytes of memory that are available to be allocated to an interleaver;

determining an amount of memory required by the interleaver to interleave a first
plurality of Reed Solomon (RS) coded data bytes within the shared memory;

allocating a first number of bytes of the shared memory to the interleaver to interleave the
first plurality of Reed Solomon (RS) coded data bytes for transmission at a first data rate,
wherein the allocated memory for the interleaver does not exceed the maximum number of bytes
specified in the message;

allocating a second number of bytes of the shared memory to a deinterleaver to
deinterleave a second plurality of RS coded data bytes received at a second data rate; and

interleaving the first plurality of RS coded data bytes within the shared memory allocated
to the interleaver and deinterleaving the second plurality of RS coded data bytes within the
shared memory allocated to the deinterleaver, wherein the shared memory allocated to the
interleaver is used at the same time as the shared memory allocated to the deinterleaver.

47. (Previously Presented) The system of claim 46, wherein the determining is based
on an impulse noise protection requirement.

48. (Previously Presented) The system of claim 46, wherein the determining is based
on a latency requirement.

49. (Previously Presented) The system of claim 46, wherein the determining is based on a bit error rate requirement.

50. (Currently Amended) A system that allocates shared memory comprising:
a transceiver that is capable of:

transmitting or receiving a message during initialization specifying a maximum number of bytes of memory that are available to be allocated to a deinterleaver;

determining an amount of memory required by the deinterleaver to deinterleave a first plurality of Reed Solomon (RS) coded data bytes within ~~athe~~ shared memory;

allocating a first number of bytes of the shared memory to the deinterleaver to deinterleave a first plurality of Reed Solomon (RS) coded data bytes for transmission at a first data rate, wherein the allocated memory for the deinterleaver does not exceed the maximum number of bytes specified in the message;

allocating a second number of bytes of the shared memory to an interleaver to interleave a second plurality of RS coded data bytes received at a second data rate; and

deinterleaving the first plurality of RS coded data bytes within the shared memory allocated to the deinterleaver and interleaving the second plurality of RS coded data bytes within the ~~shred~~-shared memory allocated to the interleaver, wherein the shared memory allocated to the deinterleaver is used at the same time as the shared memory allocated to the interleaver.

51. (Previously Presented) The system of claim 50, wherein the determining is based on an impulse noise protection requirement.

52. (Previously Presented) The system of claim 50, wherein the determining is based on a latency requirement.

53. (Previously Presented) The system of claim 50, wherein the determining is based on a bit error rate requirement.

REMARKS

Applicant respectfully requests reconsideration of this application as amended.

Applicant expressly thanks the Examiner for the indication of allowable subject matter.

By this amendment, the Applicant has addressed the Examiner's objections and rejections thereby placing the application in condition for allowance.

Claims 46-53 are pending.

With respect to the objection to the specification, a new Abstract is provided herewith – withdrawal of the objection is respectfully requested.

Regarding the objections to claims 46 and 50, the typographical error has been corrected and indents added as recommended by the Examiner. Withdrawal of the objection to the claims is respectfully requested.

Regarding the rejection under 35 U.S.C. §112, second paragraph, and in particular the allegation that the term “capable of” renders the claims indefinite, Applicant respectfully traverses this rejection. Specifically, Applicant respectfully submits with reference to the United States Court of Appeals for the Federal Circuit decision in ENZO BIOCHEM, INC., ENZO LIFE SCIENCES, INC., and YALE UNIVERSITY, v. APPLERA CORP. and TROPIX, INC., (2009-1281) the term “capable of” is definite.

Applicant therefore respectfully submits the claims do particularly point out and distinctly define the metes and bounds of the subject matter that will be protected by the patent grant.

By this amendment, claims 46 and 53 have been amended in accordance with the Examiner's recommendation to clarify antecedent basis for “shared memory.”

Withdrawal of the rejection of claims 46-53 is therefore respectfully requested.

Applicant further respectfully submits the double patenting rejections are moot in light of the Terminal Disclaimers filed herewith. Applicant does note however that on page 5 of the Office Action, claims 46-53 are rejected on nonstatutory obviousness-type double patenting in view of US Patent “7,848,882” – Applicant believes this is a typo and should be US Patent No.: 7,844,882. The attached Terminal Disclaimer reflects this understanding.

The provisional double patenting rejections are requested to be held in abeyance until an indication of allowable subject matter.

With all objections and rejections having been overcome, Applicant respectfully submits the application is in condition for allowance. A prompt notice of allowance is respectfully solicited.

Should the Examiner believe anything further is desirable in order to place the application in even better condition for allowance, the Examiner is encouraged to contact Applicants undersigned representative at the telephone number listed below.

The Commissioner is hereby authorized to charge to deposit account number 19-1970 any fees under 37 CFR § 1.16 and 1.17 that may be required by this paper and to credit any overpayment to that Account. If any extension of time is required in connection with the filing of this paper and has not been separately requested, such extension is hereby petitioned.

Respectfully submitted,

SHERIDAN ROSS P.C.

Date: 5/5/12

By: [Signature]
Jason H. Vick
Reg. No. 45,285
1560 Broadway, Suite 1200
Denver, Colorado 80202
Telephone: 303-863-9700

**TERMINAL DISCLAIMER TO OBTAIN A DOUBLE PATENTING
REJECTION OVER A "PRIOR" PATENT**

Docket Number (Optional)
5550-54-CON-3

In re Application of: Marcos C. Tzannes

Application No.: 12/901,699

Filed: October 11, 2010

For: RESOURCE SHARING IN A TELECOMMUNICATIONS ENVIRONMENT

The owner*, AWARE, INC., of 100 percent interest in the instant application hereby disclaims, except as provided below, the terminal part of the statutory term of any patent granted on the instant application which would extend beyond the expiration date of the full statutory term of **prior patent** No. 7,831,890 as the term of said **prior patent** is presently shortened by any terminal disclaimer. The owner hereby agrees that any patent so granted on the instant application shall be enforceable only for and during such period that it and the **prior patent** are commonly owned. This agreement runs with any patent granted on the instant application and is binding upon the grantee, its successors or assigns.

In making the above disclaimer, the owner does not disclaim the terminal part of the term of any patent granted on the instant application that would extend to the expiration date of the full statutory term of the **prior patent**, "as the term of said **prior patent** is presently shortened by any terminal disclaimer," in the event that said **prior patent** later:

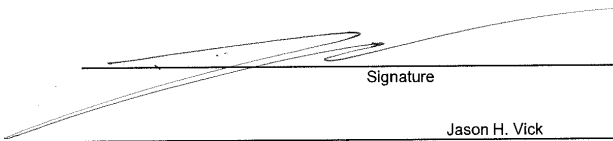
- expires for failure to pay a maintenance fee;
- is held unenforceable;
- is found invalid by a court of competent jurisdiction;
- is statutorily disclaimed in whole or terminally disclaimed under 37 CFR 1.321;
- has all claims canceled by a reexamination certificate;
- is reissued; or
- is in any manner terminated prior to the expiration of its full statutory term as presently shortened by any terminal disclaimer.

Check either box 1 or 2 below, if appropriate.

1. ☐ For submissions on behalf of a business/organization (e.g., corporation, partnership, university, government agency, etc.), the undersigned is empowered to act on behalf of the business/organization.

I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code and that such willful false statements may jeopardize the validity of the application or any patent issued thereon.

2. ☒ The undersigned is an attorney or agent of record. Reg. No. 45,285



Signature
Jason H. Vick

Typed or printed name

July 5, 2012

Date

303-863-9700

Telephone Number

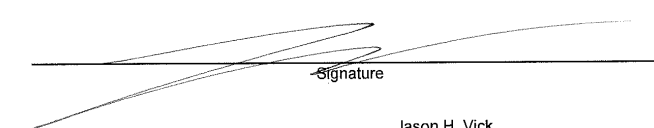
- ☒ Terminal disclaimer fee under 37 CFR 1.20(d) included.

WARNING: Information on this form may become public. Credit card information should not be included on this form. Provide credit card information and authorization on PTO-2038.

*Statement under 37 CFR 3.73(b) is required if terminal disclaimer is signed by the assignee (owner).
Form PTO/SB/96 may be used for making this certification. See MPEP § 324.

This collection of information is required by 37 CFR 1.321. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.11 and 1.14. This collection is estimated to take 12 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.

If you need assistance in completing the form, call 1-800-PTO-9199 and select option 2.

TERMINAL DISCLAIMER TO OBTAIN A DOUBLE PATENTING REJECTION OVER A "PRIOR" PATENT		Docket Number (Optional) 5550-54-CON-3
In re Application of: Marcos C. Tzannes		
Application No.: 12/901,699		
Filed: October 11, 2010		
For: RESOURCE SHARING IN A TELECOMMUNICATIONS ENVIRONMENT		
The owner*, <u>AWARE, INC.</u>, of <u>100</u> percent interest in the instant application hereby disclaims, except as provided below, the terminal part of the statutory term of any patent granted on the instant application which would extend beyond the expiration date of the full statutory term of prior patent No. <u>7,836,381</u> as the term of said prior patent is presently shortened by any terminal disclaimer. The owner hereby agrees that any patent so granted on the instant application shall be enforceable only for and during such period that it and the prior patent are commonly owned. This agreement runs with any patent granted on the instant application and is binding upon the grantee, its successors or assigns. In making the above disclaimer, the owner does not disclaim the terminal part of the term of any patent granted on the instant application that would extend to the expiration date of the full statutory term of the prior patent, "as the term of said prior patent is presently shortened by any terminal disclaimer," in the event that said prior patent later: - expires for failure to pay a maintenance fee; - is held unenforceable; - is found invalid by a court of competent jurisdiction; - is statutorily disclaimed in whole or terminally disclaimed under 37 CFR 1.321; - has all claims canceled by a reexamination certificate; - is reissued; or - is in any manner terminated prior to the expiration of its full statutory term as presently shortened by any terminal disclaimer. Check either box 1 or 2 below, if appropriate. 1. ☐ For submissions on behalf of a business/organization (e.g., corporation, partnership, university, government agency, etc.), the undersigned is empowered to act on behalf of the business/organization. I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code and that such willful false statements may jeopardize the validity of the application or any patent issued thereon. 2. ☒ The undersigned is an attorney or agent of record. Reg. No. <u>45,285</u>  _____ Signature <u>July 5, 2012</u> _____ Date <u>Jason H. Vick</u> _____ Typed or printed name <u>303-863-9700</u> _____ Telephone Number ☒ Terminal disclaimer fee under 37 CFR 1.20(d) included. WARNING: Information on this form may become public. Credit card information should not be included on this form. Provide credit card information and authorization on PTO-2038. *Statement under 37 CFR 3.73(b) is required if terminal disclaimer is signed by the assignee (owner). Form PTO/SB/96 may be used for making this certification. See MPEP § 324.		

This collection of information is required by 37 CFR 1.321. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.11 and 1.14. This collection is estimated to take 12 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.

If you need assistance in completing the form, call 1-800-PTO-9199 and select option 2.

Under the paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it displays a valid OMB control number.

PETITION FOR EXTENSION OF TIME UNDER 37 CFR 1.136(a)		Docket Number (Optional) 5550-54-CON-3	
Application Number 12/901,699		Filed October 11, 2010	
For RESOURCE SHARING IN A TELECOMMUNICATIONS ENVIRONMENT			
Art Unit 2117		Examiner TABONE JR., John J.	
This is a request under the provisions of 37 CFR 1.136(a) to extend the period for filing a reply in the above identified application.			
The requested extension and fee are as follows (check time period desired and enter the appropriate fee below):			
	<u>Fee</u>	<u>Small Entity Fee</u>	
☐ One month (37 CFR 1.17(a)(1))	\$150	\$75	\$ _____
☐ Two months (37 CFR 1.17(a)(2))	\$560	\$280	\$ _____
☒ Three months (37 CFR 1.17(a)(3))	\$1270	\$635	\$ <u>1270</u>
☐ Four months (37 CFR 1.17(a)(4))	\$1980	\$990	\$ _____
☐ Five months (37 CFR 1.17(a)(5))	\$2690	\$1345	\$ _____
☐ Applicant claims small entity status. See 37 CFR 1.27.			
☐ A check in the amount of the fee is enclosed.			
☐ Payment by credit card. Form PTO-2038 is attached.			
☒ The Director has already been authorized to charge fees in this application to a Deposit Account.			
☒ The Director is hereby authorized to charge any fees which may be required, or credit any overpayment, to Deposit Account Number <u>19-1970</u> .			
WARNING: Information on this form may become public. Credit card information should not be included on this form. Provide credit card information and authorization on PTO-2038.			
I am the ☐ applicant/inventor.			
☐ assignee of record of the entire interest. See 37 CFR 3.71. Statement under 37 CFR 3.73(b) is enclosed (Form PTO/SB/96).			
☒ attorney or agent of record. Registration Number <u>45,285</u>			
☐ attorney or agent under 37 CFR 1.34. Registration number if acting under 37 CFR 1.34 _____			
 Signature		July 5, 2012 Date	
Jason H. Vick Typed or printed name		303-863-9700 Telephone Number	
NOTE: Signatures of all the inventors or assignees of record of the entire interest or their representative(s) are required. Submit multiple forms if more than one signature is required, see below.			
☒ Total of <u>1</u> forms are submitted.			

This collection of information is required by 37 CFR 1.136(a). The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.11 and 1.14. This collection is estimated to take 6 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

If you need assistance in completing the form, call 1-800-PTO-9199 and select option 2.

Electronic Patent Application Fee Transmittal				
Application Number:		12901699		
Filing Date:		11-Oct-2010		
Title of Invention:		RESOURCE SHARING IN A TELECOMMUNICATIONS ENVIRONMENT		
First Named Inventor/Applicant Name:		Marcos C. Tzannes		
Filer:		Jason Vick/Joanne Vos		
Attorney Docket Number:		5550-54-CON-3		
Filed as Large Entity				
Utility under 35 USC 111(a) Filing Fees				
Description	Fee Code	Quantity	Amount	Sub-Total in USD(\$)
Basic Filing:				
Pages:				
Claims:				
Miscellaneous-Filing:				
Petition:				
Patent-Appeals-and-Interference:				
Post-Allowance-and-Post-Issuance:				
Extension-of-Time:				
Extension - 3 months with \$0 paid	1253	1	1270	1270

Description	Fee Code	Quantity	Amount	Sub-Total in USD(\$)
Miscellaneous:				
Statutory or terminal disclaimer	1814	3	160	480
Total in USD (\$)				1750

Electronic Acknowledgement Receipt	
EFS ID:	13186107
Application Number:	12901699
International Application Number:	
Confirmation Number:	1676
Title of Invention:	RESOURCE SHARING IN A TELECOMMUNICATIONS ENVIRONMENT
First Named Inventor/Applicant Name:	Marcos C. Tzannes
Customer Number:	62574
Filer:	Jason Vick/Joanne Vos
Filer Authorized By:	Jason Vick
Attorney Docket Number:	5550-54-CON-3
Receipt Date:	05-JUL-2012
Filing Date:	11-OCT-2010
Time Stamp:	18:42:50
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	yes
Payment Type	Deposit Account
Payment was successfully received in RAM	\$1750
RAM confirmation Number	7224
Deposit Account	191970
Authorized User	
The Director of the USPTO is hereby authorized to charge indicated fees and credit any overpayment as follows: Charge any Additional Fees required under 37 C.F.R. Section 1.16 (National application filing, search, and examination fees) Charge any Additional Fees required under 37 C.F.R. Section 1.17 (Patent application and reexamination processing fees)	

Charge any Additional Fees required under 37 C.F.R. Section 1.19 (Document supply fees)					
Charge any Additional Fees required under 37 C.F.R. Section 1.21 (Miscellaneous fees and charges)					
File Listing:					
Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1		AMEND_01.pdf	1008698	yes	11
			cd9fd61927281716a908978e59119a2cfe13935		
	Multipart Description/PDF files in .zip description				
	Document Description		Start	End	
	Amendment/Req. Reconsideration-After Non-Final Reject		1	1	
	Specification		2	2	
	Abstract		3	3	
	Claims		4	5	
	Applicant Arguments/Remarks Made in an Amendment		6	7	
	Terminal Disclaimer Filed		8	8	
	Terminal Disclaimer Filed		9	9	
	Terminal Disclaimer Filed		10	10	
	Extension of Time		11	11	
Warnings:					
Information:					
2	Fee Worksheet (SB06)	fee-info.pdf	32053	no	2
			7b42eccfda0e7e1fceb0c34b9d7a39ce34e49155		
Warnings:					
Information:					
Total Files Size (in bytes):			1040751		

This Acknowledgement Receipt evidences receipt on the noted date by the USPTO of the indicated documents, characterized by the applicant, and including page counts, where applicable. It serves as evidence of receipt similar to a Post Card, as described in MPEP 503.

New Applications Under 35 U.S.C. 111

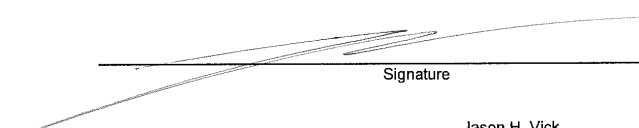
If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application.

National Stage of an International Application under 35 U.S.C. 371

If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.

New International Application Filed with the USPTO as a Receiving Office

If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.

TERMINAL DISCLAIMER TO OBTAIN A DOUBLE PATENTING REJECTION OVER A "PRIOR" PATENT	Docket Number (Optional) 5550-54-CON-3
In re Application of: Marcos C. Tzannes Application No.: 12/901,699 Filed: October 11, 2010 For: RESOURCE SHARING IN A TELECOMMUNICATIONS ENVIRONMENT The owner*, <u>AWARE, INC.</u>, of <u>100</u> percent interest in the instant application hereby disclaims, except as provided below, the terminal part of the statutory term of any patent granted on the instant application which would extend beyond the expiration date of the full statutory term of prior patent No. <u>7,844,882</u> as the term of said prior patent is presently shortened by any terminal disclaimer. The owner hereby agrees that any patent so granted on the instant application shall be enforceable only for and during such period that it and the prior patent are commonly owned. This agreement runs with any patent granted on the instant application and is binding upon the grantee, its successors or assigns. In making the above disclaimer, the owner does not disclaim the terminal part of the term of any patent granted on the instant application that would extend to the expiration date of the full statutory term of the prior patent, "as the term of said prior patent is presently shortened by any terminal disclaimer," in the event that said prior patent later: - expires for failure to pay a maintenance fee; - is held unenforceable; - is found invalid by a court of competent jurisdiction; - is statutorily disclaimed in whole or terminally disclaimed under 37 CFR 1.321; - has all claims canceled by a reexamination certificate; - is reissued; or - is in any manner terminated prior to the expiration of its full statutory term as presently shortened by any terminal disclaimer. Check either box 1 or 2 below, if appropriate. 1. ☐ For submissions on behalf of a business/organization (e.g., corporation, partnership, university, government agency, etc.), the undersigned is empowered to act on behalf of the business/organization. I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code and that such willful false statements may jeopardize the validity of the application or any patent issued thereon. 2. ☒ The undersigned is an attorney or agent of record. Reg. No. <u>45,285</u>  _____ Signature <u>July 5, 2012</u> Date <u>Jason H. Vick</u> Typed or printed name <u>303-863-9700</u> Telephone Number ☒ Terminal disclaimer fee under 37 CFR 1.20(d) included. WARNING: Information on this form may become public. Credit card information should not be included on this form. Provide credit card information and authorization on PTO-2038. *Statement under 37 CFR 3.73(b) is required if terminal disclaimer is signed by the assignee (owner). Form PTO/SB/96 may be used for making this certification. See MPEP § 324.	

This collection of information is required by 37 CFR 1.321. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.11 and 1.14. This collection is estimated to take 12 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.

If you need assistance in completing the form, call 1-800-PTO-9199 and select option 2.

Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it displays a valid OMB control number.

PATENT APPLICATION FEE DETERMINATION RECORD Substitute for Form PTO-875					Application or Docket Number 12/901,699		Filing Date 10/11/2010		☐ To be Mailed		
APPLICATION AS FILED – PART I											
(Column 1)			(Column 2)			SMALL ENTITY ☐ OR		OTHER THAN SMALL ENTITY			
FOR		NUMBER FILED	NUMBER EXTRA		RATE (\$)	FEE (\$)	OR		RATE (\$)	FEE (\$)	
☐ BASIC FEE (37 CFR 1.16(a), (b), or (c))		N/A	N/A		N/A		OR		N/A		
☐ SEARCH FEE (37 CFR 1.16(k), (l), or (m))		N/A	N/A		N/A		OR		N/A		
☐ EXAMINATION FEE (37 CFR 1.16(o), (p), or (q))		N/A	N/A		N/A		OR		N/A		
TOTAL CLAIMS (37 CFR 1.16(j))		minus 20 =	*		X \$ =		OR		X \$ =		
INDEPENDENT CLAIMS (37 CFR 1.16(h))		minus 3 =	*		X \$ =		OR		X \$ =		
☐ APPLICATION SIZE FEE (37 CFR 1.16(s))		If the specification and drawings exceed 100 sheets of paper, the application size fee due is \$250 (\$125 for small entity) for each additional 50 sheets or fraction thereof. See 35 U.S.C. 41(a)(1)(G) and 37 CFR 1.16(s).									
☐ MULTIPLE DEPENDENT CLAIM PRESENT (37 CFR 1.16(j))											
					TOTAL		OR		TOTAL		
* If the difference in column 1 is less than zero, enter "0" in column 2.											
APPLICATION AS AMENDED – PART II											
(Column 1)			(Column 2)			(Column 3)		SMALL ENTITY OR		OTHER THAN SMALL ENTITY	
AMENDMENT	07/05/2012	CLAIMS REMAINING AFTER AMENDMENT	HIGHEST NUMBER PREVIOUSLY PAID FOR	PRESENT EXTRA		RATE (\$)	ADDITIONAL FEE (\$)	OR		RATE (\$)	ADDITIONAL FEE (\$)
	Total (37 CFR 1.16(j))	* 8	Minus	** 20	= 0	X \$ =		OR		X \$60=	0
	Independent (37 CFR 1.16(h))	* 2	Minus	***3	= 0	X \$ =		OR		X \$250=	0
	☐ Application Size Fee (37 CFR 1.16(s))							OR			
	☐ FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))							OR			
						TOTAL ADD'L FEE		OR		TOTAL ADD'L FEE	0
AMENDMENT	Total (37 CFR 1.16(j))	*	Minus	**	=	X \$ =		OR		X \$ =	
	Independent (37 CFR 1.16(h))	*	Minus	***	=	X \$ =		OR		X \$ =	
	☐ Application Size Fee (37 CFR 1.16(s))							OR			
	☐ FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))							OR			
						TOTAL ADD'L FEE		OR		TOTAL ADD'L FEE	
								OR			
* If the entry in column 1 is less than the entry in column 2, write "0" in column 3. ** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 20, enter "20". *** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 3, enter "3". The "Highest Number Previously Paid For" (Total or Independent) is the highest number found in the appropriate box in column 1.											

Legal Instrument Examiner:
/Theresa Dawkins/

This collection of information is required by 37 CFR 1.16. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 12 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

If you need assistance in completing the form, call 1-800-PTO-9199 and select option 2.

Substitute for form 1449A/PTO				Complete if Known	
INFORMATION DISCLOSURE STATEMENT BY APPLICANT				Application Number	12/901,699
				Filing Date	October 11, 2010
				First Named Inventor	Marcos C. Tzannes
				Art Unit	2117
				Examiner Name	Tabone Jr, John J.
Sheet	1	of	1	Attorney Docket Number	5550-54-CON-3

U.S. PATENT DOCUMENTS					
Examiner Initials*	Cite No. ¹	Document Number Number-kind Code ² (if known)	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear

FOREIGN PATENT DOCUMENTS						
Examiner Initials*	Cite No. ¹	Foreign Patent Document Country Code ³ ; Number ⁴ ; Kind Code ⁵ (if known)	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear	T ⁶

OTHER ART (Including Author, Title, Date, Pertinent Pages, etc.)		
Examiner Initials*	Cite No. ¹	
	1	Official Notification of Intent to Grant (including translation) for Mexican Patent Application No. MX/a/2008/012505, mailed April 3, 2012 (Attorney Ref. No.: 5550-57-PMX)

Examiner Signature		Date Considered	

*EXAMINER: Initial if reference is considered, whether or not citation is in conformance and not considered. Include copy of this form with next communication to applicant.

Electronic Acknowledgement Receipt	
EFS ID:	13047483
Application Number:	12901699
International Application Number:	
Confirmation Number:	1676
Title of Invention:	RESOURCE SHARING IN A TELECOMMUNICATIONS ENVIRONMENT
First Named Inventor/Applicant Name:	Marcos C. Tzannes
Customer Number:	62574
Filer:	Jason Vick/Joanne Vos
Filer Authorized By:	Jason Vick
Attorney Docket Number:	5550-54-CON-3
Receipt Date:	19-JUN-2012
Filing Date:	11-OCT-2010
Time Stamp:	11:32:13
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	no				
File Listing:					
Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1		IDS_12.pdf	337796 0a787e3da1fe968c3d6fc85fc4d1586d41b0b16b	yes	4

Multipart Description/PDF files in .zip description					
Document Description			Start	End	
Transmittal Letter			1	3	
Information Disclosure Statement (IDS) Form (SB08)			4	4	
Warnings:					
Information:					
2	Non Patent Literature	5550-57- PMX_NOA_04-03-2012.pdf	96094 d9b4dee00d8a7805e7197605e62a054b353118c8	no	2
Warnings:					
Information:					
Total Files Size (in bytes):			433890		
This Acknowledgement Receipt evidences receipt on the noted date by the USPTO of the indicated documents, characterized by the applicant, and including page counts, where applicable. It serves as evidence of receipt similar to a Post Card, as described in MPEP 503. New Applications Under 35 U.S.C. 111 If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application. National Stage of an International Application under 35 U.S.C. 371 If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course. New International Application Filed with the USPTO as a Receiving Office If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.					

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In Re the Application of:	)	Group Art Unit: 2117
TZANNES, Marcos C.	)	Confirmation No.: 1676
Serial No.: 12/901,699	)	Examiner: Tabone Jr, John J.
Filed: October 11, 2010	)	
Atty. File No.: 5550-54-CON-3	)	<u>SUPPLEMENTAL</u>
Entitled: "RESOURCE SHARING IN A	)	<u>INFORMATION DISCLOSURE</u>
TELECOMMUNICATIONS ENVIRONMENT"	)	<u>STATEMENT</u>
	)	Electronically Submitted

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Dear Sir:

The references cited on attached Form PTO-1449 are being called to the attention of the Examiner.

- ☒ Copies of the cited non-patent and/or foreign references are enclosed herewith.
- ☐ Copies of the cited U.S. patents and/or patent applications are enclosed herewith.
- ☐ Copies of the cited U.S. patents/patent application publications are not enclosed in accordance with 37 C.F.R. § 1.98(a).
- ☐ Copies of the cited references are not enclosed, in accordance with 37 C.F.R. § 1.98(d), because the references were cited by or submitted to the U.S. Patent and Trademark Office in prior application Serial No. _____ filed _____, which is relied upon for an earlier filing date under 35 U.S.C. § 120.
- ☒ To the best of applicants' belief, the pertinence of the foreign-language references are believed to be summarized in the attached English translations and/or in the figures, although applicants do not necessarily vouch for the accuracy of the translation.

- ☐ Examiner's attention is drawn to the following related applications:
- Serial No. _____ filed _____ (Attorney Ref. No. _____)
- Serial No. _____ filed _____ (Attorney Ref. No. _____)
- ☐ Other: _____

Submission of the above information is not intended as an admission that any item is citable under the statutes or rules to support a rejection, that any item disclosed represents analogous art, or that those skilled in the art would refer to or recognize the pertinence of any reference without the benefit of hindsight, nor should an inference be

drawn as to the pertinence of the references based on the order in which they are presented. Submission of this statement should not be taken as an indication that a search has been conducted, or that no better art exists.

It is respectfully requested that the cited information be expressly considered during the prosecution of this application and the references made of record therein.

FEES

☐	37 CFR 1.97(b): No fee is believed due in connection with this submission, because the information disclosure statement submitted herewith is satisfied by one of the following conditions ("X" indicates satisfaction): ☐ Within three months of the filing date of a national application other than a continued prosecution application under 37 CFR 1.53(d), or ☐ Within three months of the date of entry of the national stage as set forth in § 1.491 in an international application, or ☐ Before the mailing date of a first Office Action on the merits, or ☐ Before the mailing of a first Office action after the filing of a request for continued examination under 37 CFR 1.114. Although no fee is believed due, if any fee is deemed due in connection with this submission, please charge such fee to Deposit Account 19-1970.
☒	37 CFR 1.97(c): The information disclosure statement transmitted herewith is being filed after all the above conditions (37 CFR 1.97(b)), but before the mailing date of any one of the following conditions: (1) a final action under 37 C.F.R. 1.113, or (2) a notice of allowance under 37 C.F.R. 1.311, or (3) an action that otherwise closes prosecution in the application. This Information Disclosure Statement is accompanied by: ☒ A Certification (below) as specified by 37 C.F.R. 1.97(e). Although no fee is believed due, if any fee is deemed due in connection with this submission, please charge such fee to Deposit Account 19-1970. OR ☐ Please charge Deposit Account 19-1970 in the amount of \$180.00 for the fee set forth in 37 C.F.R. 1.17(p) for submission of an information disclosure statement. Please credit any overpayment or charge any underpayment to Deposit Account 19-1970.
☐	37 CFR 1.97(d): This Information Disclosure Statement is being submitted after the period specified in 37 CFR 1.97(c). ☐ This information Disclosure Statement includes a Certification (below) as specified by 37 C.F.R. 1.97(e) AND ☐ Applicants hereby requests consideration of the reference(s) disclosed herein. Please charge Deposit Account 19-1970 in the amount of \$180.00 under 37 C.F.R. 1.17(p). Please credit any overpayment or charge any underpayment to Deposit Account 19-1970. Election to pay the fee should not be taken as an indication that applicant(s) cannot execute a certification.

Certification (37 C.F.R. 1.97(e))
(Applicable only if checked)

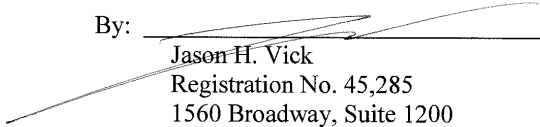
- ☒ The undersigned certifies that:
- ☒ Each item of information contained in this information disclosure statement was first cited in any communication from a foreign patent office in a counterpart foreign application not more than three months prior to the filing of this statement. 37 C.F.R. 1.97(e)(1).
 - ☒ A copy of the communication from the foreign patent office is enclosed.

OR

☐ No item of information contained in this information disclosure statement was cited in a communication from a foreign patent office in a counterpart foreign application, and, to the knowledge of the undersigned after making reasonable inquiry, no item of information contained in this Information Disclosure Statement was known to any individual designated in 37 C.F.R. 1.56(c) more than three months prior to the filing of this statement. 37 C.F.R. 1.97(e)(2).

Respectfully submitted,

SHERIDAN ROSS P.C.

By: 
Jason H. Vick
Registration No. 45,285
1560 Broadway, Suite 1200
Denver, Colorado 80202-5141
(303) 863-9700

Date: 19 Jan '12

Substitute for form 1449A/PTO				Complete if Known	
INFORMATION DISCLOSURE STATEMENT BY APPLICANT				Application Number	12/901,699
				Filing Date	October 11, 2010
				First Named Inventor	Marcos C. Tzannes
				Art Unit	2117
				Examiner Name	Tabone Jr, John J.
Sheet	1	of	1	Attorney Docket Number	5550-54-CON-3

U.S. PATENT DOCUMENTS					
Examiner Initials*	Cite No. ¹	Document Number Number-kind Code ^{2 (if known)}	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear
	1	5524116	06-04-1996	Kalmanek, Jr., et al.	
	2	6098188	08-01-2000	Kalmanek, Jr., et al.	
	3	7164654	01-16-2007	Hunzinger et al.	
	4	7782758	08-24-2010	Wydrowski et al.	

FOREIGN PATENT DOCUMENTS						
Examiner Initials*	Cite No. ¹	Foreign Patent Document Country Code ³ ; Number ⁴ ; Kind Code ⁵ (if known)	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear	T ⁶

OTHER ART (Including Author, Title, Date, Pertinent Pages, etc.)		
Examiner Initials*	Cite No. ¹	
	5	Official Action for U.S. Patent Application No. 12/760,728, mailed April 27, 2012 (Attorney Ref. No.: 5550-57-PUS-DIV)
	6	Official Action for U.S. Patent Application No. 12/783,765, mailed May 17, 2012 (Attorney Ref. No. 5550-57-PUS-DIV-CON)

Examiner Signature		Date Considered	

*EXAMINER: Initial if reference is considered, whether or not citation is in conformance and not considered. Include copy of this form with next communication to applicant.

Electronic Acknowledgement Receipt	
EFS ID:	12859937
Application Number:	12901699
International Application Number:	
Confirmation Number:	1676
Title of Invention:	RESOURCE SHARING IN A TELECOMMUNICATIONS ENVIRONMENT
First Named Inventor/Applicant Name:	Marcos C. Tzannes
Customer Number:	62574
Filer:	Jason Vick/Joanne Vos
Filer Authorized By:	Jason Vick
Attorney Docket Number:	5550-54-CON-3
Receipt Date:	24-MAY-2012
Filing Date:	11-OCT-2010
Time Stamp:	16:18:03
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	no

File Listing:

Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1		IDS_10_US_Certified.pdf	344230 f5ce3de6932118e89be337eeb1a419ca2fe7ed1	yes	4

Multipart Description/PDF files in .zip description					
Document Description			Start	End	
Transmittal Letter			1	3	
Information Disclosure Statement (IDS) Form (SB08)			4	4	
Warnings:					
Information:					
2	Non Patent Literature	5550-57-PUS-DIV_OA_04-27-2012.pdf	1361537	no	39
			5a4a357e95db117e255a428b57d061c3d3a59ff		
Warnings:					
Information:					
3	Non Patent Literature	5550-57-PUS-DIV-CON_OA_05-17-2012.pdf	1064507	no	26
			79d45f50517b0f66a3f8e825d7ccdc8f055b588		
Warnings:					
Information:					
Total Files Size (in bytes):			2770274		
This Acknowledgement Receipt evidences receipt on the noted date by the USPTO of the indicated documents, characterized by the applicant, and including page counts, where applicable. It serves as evidence of receipt similar to a Post Card, as described in MPEP 503. New Applications Under 35 U.S.C. 111 If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application. National Stage of an International Application under 35 U.S.C. 371 If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course. New International Application Filed with the USPTO as a Receiving Office If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.					

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In Re the Application of:	)	Group Art Unit: 2117
TZANNES, Marcos C.	)	Confirmation No.: 1676
Serial No.: 12/901,699	)	Examiner: Tabone Jr, John J.
Filed: October 11, 2010	)	
Atty. File No.: 5550-54-CON-3	)	<u>SUPPLEMENTAL</u>
Entitled: "RESOURCE SHARING IN A	)	<u>INFORMATION DISCLOSURE</u>
TELECOMMUNICATIONS ENVIRONMENT"	)	<u>STATEMENT</u>
	)	Electronically Submitted

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Dear Sir:

The references cited on attached Form PTO-1449 are being called to the attention of the Examiner.

- ☒ Copies of the cited non-patent and/or foreign references are enclosed herewith.
- ☐ Copies of the cited U.S. patents and/or patent applications are enclosed herewith.
- ☒ Copies of the cited U.S. patents/patent application publications are not enclosed in accordance with 37 C.F.R. § 1.98(a).
- ☐ Copies of the cited references are not enclosed, in accordance with 37 C.F.R. § 1.98(d), because the references were cited by or submitted to the U.S. Patent and Trademark Office in prior application Serial No. _____ filed _____, which is relied upon for an earlier filing date under 35 U.S.C. § 120.
- ☐ To the best of applicants' belief, the pertinence of the foreign-language references are believed to be summarized in the attached English translations and/or in the figures, although applicants do not necessarily vouch for the accuracy of the translation.
- ☐ Examiner's attention is drawn to the following related applications:
- Serial No. _____ filed _____ (Attorney Ref. No. _____)
- Serial No. _____ filed _____ (Attorney Ref. No. _____)
- ☐ Other: _____

Submission of the above information is not intended as an admission that any item is citable under the statutes or rules to support a rejection, that any item disclosed represents analogous art, or that those skilled in the art would refer to or recognize the pertinence of any reference without the benefit of hindsight, nor should an inference be

drawn as to the pertinence of the references based on the order in which they are presented. Submission of this statement should not be taken as an indication that a search has been conducted, or that no better art exists.

It is respectfully requested that the cited information be expressly considered during the prosecution of this application and the references made of record therein.

FEES

☐	37 CFR 1.97(b): No fee is believed due in connection with this submission, because the information disclosure statement submitted herewith is satisfied by one of the following conditions ("X" indicates satisfaction): ☐ Within three months of the filing date of a national application other than a continued prosecution application under 37 CFR 1.53(d), or ☐ Within three months of the date of entry of the national stage as set forth in § 1.491 in an international application, or ☐ Before the mailing date of a first Office Action on the merits, or ☐ Before the mailing of a first Office action after the filing of a request for continued examination under 37 CFR 1.114. Although no fee is believed due, if any fee is deemed due in connection with this submission, please charge such fee to Deposit Account 19-1970.
☒	37 CFR 1.97(c): The information disclosure statement transmitted herewith is being filed after all the above conditions (37 CFR 1.97(b)), but before the mailing date of any one of the following conditions: (1) a final action under 37 C.F.R. 1.113, or (2) a notice of allowance under 37 C.F.R. 1.311, or (3) an action that otherwise closes prosecution in the application. This Information Disclosure Statement is accompanied by: ☒ A Certification (below) as specified by 37 C.F.R. 1.97(e). Although no fee is believed due, if any fee is deemed due in connection with this submission, please charge such fee to Deposit Account 19-1970. OR ☐ Please charge Deposit Account 19-1970 in the amount of \$180.00 for the fee set forth in 37 C.F.R. 1.17(p) for submission of an information disclosure statement. Please credit any overpayment or charge any underpayment to Deposit Account 19-1970.
☐	37 CFR 1.97(d): This Information Disclosure Statement is being submitted after the period specified in 37 CFR 1.97(c). ☐ This information Disclosure Statement includes a Certification (below) as specified by 37 C.F.R. 1.97(e) AND ☐ Applicants hereby requests consideration of the reference(s) disclosed herein. Please charge Deposit Account 19-1970 in the amount of \$180.00 under 37 C.F.R. 1.17(p). Please credit any overpayment or charge any underpayment to Deposit Account 19-1970. Election to pay the fee should not be taken as an indication that applicant(s) cannot execute a certification.

Certification (37 C.F.R. 1.97(e))
(Applicable only if checked)



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Respectfully submitted,

SHERIDAN ROSS P.C.

By: _____

Jason H. Vick
Registration No. 45,285
1560 Broadway, Suite 1200
Denver, Colorado 80202-5141
(303) 863-9700

Date: 27 MAY '12

Substitute for form 1449A/PTO				Complete if Known	
INFORMATION DISCLOSURE STATEMENT BY APPLICANT				Application Number	12/901,699
				Filing Date	October 11, 2010
				First Named Inventor	Marcos C. Tzannes
				Art Unit	2117
				Examiner Name	Tabone Jr, John J.
Sheet	1	of	1	Attorney Docket Number	5550-54-CON-3

U.S. PATENT DOCUMENTS					
Examiner Initials*	Cite No. ¹	Document Number Number-kind Code ² (if known)	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear

FOREIGN PATENT DOCUMENTS					
Examiner Initials*	Cite No. ¹	Foreign Patent Document Country Code ³ ; Number ⁴ ; Kind Code ⁵ (if known)	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear

OTHER ART (Including Author, Title, Date, Pertinent Pages, etc.)		
Examiner Initials*	Cite No. ¹	
	1	Official Action (including translation) for Chinese Patent Application No. 200580032703.1, dispatched March 28, 2012 (Attorney Ref. No. 5550-54-PCN)
	2	Decision of Final Rejection for Japanese Patent Application No. 2010-017356, dispatched April 23, 2012 (Attorney Ref. No.: 5550-57-PJP-DIV)

Examiner Signature		Date Considered	

*EXAMINER: Initial if reference is considered, whether or not citation is in conformance and not considered. Include copy of this form with next communication to applicant.

Electronic Acknowledgement Receipt	
EFS ID:	12860027
Application Number:	12901699
International Application Number:	
Confirmation Number:	1676
Title of Invention:	RESOURCE SHARING IN A TELECOMMUNICATIONS ENVIRONMENT
First Named Inventor/Applicant Name:	Marcos C. Tzannes
Customer Number:	62574
Filer:	Jason Vick/Joanne Vos
Filer Authorized By:	Jason Vick
Attorney Docket Number:	5550-54-CON-3
Receipt Date:	24-MAY-2012
Filing Date:	11-OCT-2010
Time Stamp:	16:21:26
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	no

File Listing:

Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1		IDS_11_Foreign_Certified.pdf	337122 c1ac2ae29f9b661417f61428d59f538f62d4f260	yes	4

Multipart Description/PDF files in .zip description					
Document Description			Start	End	
Transmittal Letter			1	3	
Information Disclosure Statement (IDS) Form (SB08)			4	4	
Warnings:					
Information:					
2	Non Patent Literature	5550-54-PCN_OA_03-28-2012.pdf	660784 b0c1187723e87cb0a883e72e25592ae303998667	no	10
Warnings:					
Information:					
3	Non Patent Literature	5550-57-PJP-DIV_OA_04-23-2012.pdf	41922 4fe1314fed0e7846fcd81a1d6fc5be206fdd8853	no	1
Warnings:					
Information:					
Total Files Size (in bytes):			1039828		
This Acknowledgement Receipt evidences receipt on the noted date by the USPTO of the indicated documents, characterized by the applicant, and including page counts, where applicable. It serves as evidence of receipt similar to a Post Card, as described in MPEP 503. New Applications Under 35 U.S.C. 111 If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application. National Stage of an International Application under 35 U.S.C. 371 If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course. New International Application Filed with the USPTO as a Receiving Office If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.					

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In Re the Application of:	)	Group Art Unit: 2117
TZANNES, Marcos C.	)	Confirmation No.: 1676
Serial No.: 12/901,699	)	Examiner: Tabone Jr, John J.
Filed: October 11, 2010	)	
Atty. File No.: 5550-54-CON-3	)	<u>SUPPLEMENTAL</u>
Entitled: "RESOURCE SHARING IN A	)	<u>INFORMATION DISCLOSURE</u>
TELECOMMUNICATIONS ENVIRONMENT"	)	<u>STATEMENT</u>
	)	Electronically Submitted

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Dear Sir:

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- Serial No. _____ filed _____ (Attorney Ref. No. _____)
- Serial No. _____ filed _____ (Attorney Ref. No. _____)
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FEES

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Certification (37 C.F.R. 1.97(e))
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Respectfully submitted,

SHERIDAN ROSS P.C.

By: _____

Jason H. Vick
Registration No. 45,285
1560 Broadway, Suite 1200
Denver, Colorado 80202-5141
(303) 863-9700

Date: 24 May '12

Substitute for form 1449A/PTO				Complete if Known	
INFORMATION DISCLOSURE STATEMENT BY APPLICANT				Application Number	12/901,699
				Filing Date	October 11, 2010
				First Named Inventor	Marcos C. Tzannes
				Art Unit	2117
				Examiner Name	Tabone Jr, John J.
Sheet	1	of	1	Attorney Docket Number	5550-54-CON-3

U.S. PATENT DOCUMENTS					
Examiner Initials*	Cite No. ¹	Document Number Number-kind Code ² (if known)	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear
	1	6826589	11-30-2004	Berrada	

FOREIGN PATENT DOCUMENTS						
Examiner Initials*	Cite No. ¹	Foreign Patent Document Country Code ³ ; Number ⁴ ; Kind Code ⁵ (if known)	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear	T ⁶
	2	KR10-2000-0047827	07-25-2000	KONINCLIKE PHILIPS ELECTRONICS		(corresponds to US 6,826,589 cited herein)

OTHER ART (Including Author, Title, Date, Pertinent Pages, etc.)		
Examiner Initials*	Cite No. ¹	
	3	Notice of Allowance (including translation) for Korean Patent Application No. 10-2007-7008270, mailed March 29, 2012 (Attorney Ref. No.: 5550-54-PKR)
	4	Notice of Allowance (including translation) for Korean Patent Application No. 10-2010-7022463, mailed March 29, 2012 (Attorney Ref. No.: 5550-54-PKR-DIV)
	5	Notice of Allowance for Japanese Patent Application No. 2008-264540, mailed March 26, 2012 (Attorney Ref. No.: 5550-54-PJP-DIV)
	6	Notification of the Second Office Action (including translation) for Chinese Patent Application No. 200780012891.0, dispatched March 7, 2012 (Attorney Ref. No.: 5550-57-PCN)

Examiner Signature		Date Considered	

*EXAMINER: Initial if reference is considered, whether or not citation is in conformance and not considered. Include copy of this form with next communication to applicant.



Espacenet

Bibliographic data: KR200000047827 (A) — 2000-07-25

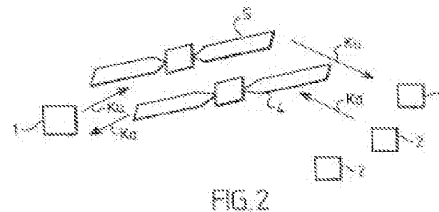
REQUEST MECHANISM FOR COMMUNICATION SYSTEM BETWEEN MASTER STATIONS AND TWO-WAY TERMINAL

Inventor(s): MARONE BERADA [NL] ±
Applicant(s): KONINCLIKE PHILIPS ELECTRONICS ±
Classification: - **international:** H04B7/212; H04B7/24; H04H1/00; H04J3/00; H04L12/56; (IPC1-7): H04B7/212
 - **European:** H04B7/212A1
Application number: KR19990054140 19991201
Priority number (s): FR19980015141 19981201
Also published as: KR100619456 (B1) EP1006681 (A1) EP1006681 (B1) US2003187981 (A1) US6826589 (B2) more

Abstract of KR200000047827 (A)

PURPOSE: A mechanism for communication system between master stations and two-way terminal is provided to enable terminals to allocate the designated numbers of reservation on transmission system by using a series of master stations and transmission systems.

CONSTITUTION: A mechanism for communication system between master station and two-way terminal includes the following steps. A series of two-way terminals (2) which communicates with a master station through transmission system(3) are set on the communication system. A series of two-way terminals(2) transmit information to the master station. Terminals(2) receive allocation which are not yet destroyed. Terminals(2) temporarily stores the allocation to a memory(10). A memory(10) considers the allocation which are already stored when a new order is received. The device enables communication systems to prevent repeatedly produce requests.



(19)대한민국특허청(KR)
(12) 등록특허공보(B1)

(51) 。 Int. Cl.
H04B 7/212 (2006.01)

(45) 공고일자 2006년09월06일
(11) 등록번호 10-0619456
(24) 등록일자 2006년08월28일

(21) 출원번호 10-1999-0054140 (65) 공개번호 10-2000-0047827
(22) 출원일자 1999년12월01일 (43) 공개일자 2000년07월25일

(30) 우선권주장 9815141 1998년12월01일 프랑스(FR)

(73) 특허권자 코닌클리케 필립스 일렉트로닉스 엔.브이.
네델란드왕국, 아인드호펜, 그로네보르스베그 1

(72) 발명자 베라다마로안느
프랑스,프레메이르94000,뤼두카프,15

(74) 대리인 이병호
정상구
신현문
이범래

심사관 : 송원환

(54) 양방향 단말들 및 마스터 스테이션 간의 통신 시스템에 대한 요청 메카니즘

요약

본 발명은 전송 매체를 통하여 마스터 스테이션(master station)과 통신하는 복수의 양방향(interactive) 단말들을 포함하는 통신 시스템에 관한 것이다. 본 발명은 특히 양방향 위성 방송 시스템들에 적용된다. 본 발명은 양방향 단말들이 마스터 스테이션에 정보를 전송하기 위해, 전송 매체 상에서 단말들에 할당되는 예약들을 갖도록 허용하는 요청 메카니즘에 관한 것이다. 단말이 아직 만료되지 않은 할당들을 수신할 때, 단말은 임시적으로 할당 메모리에 할당들을 저장한다. 새로운 요청이 전송될 때, 본 발명은 이 메모리에 포함된 할당들의 수를 고려하는 것을 포함한다. 따라서, 이미 부여 받은 할당들에 대한 요청들이 다시 정해지는 것을 방지하게 된다.

대표도

도 2

색인어

마스터 스테이션, 양방향 단말, 요청 메카니즘, 할당 메모리

명세서

도면의 간단한 설명

도 1은 본 발명에 따른 통신 시스템을 도시하는 도면.

도 2는 본 발명에 따른 위성 통신 시스템을 도시하는 도면.

도 3은 본 발명에 따른 요청 방법을 도시하는 도면.

도 4 및 도 5는 본 발명으로 얻어지는 결과들을 지시하는 도면.

도면의 주요부분에 대한 설명

3: 전송 매체 2: 양방향 단말

4: 제 1 위성 5: 제 2 위성

10: 메모리

발명의 상세한 설명

발명의 목적

발명이 속하는 기술 및 그 분야의 종래기술

본 발명은 적어도 마스터 스테이션, 및 전송 매체를 통하여 마스터 스테이션과 통신하고자 하는 복수의 단말들을 포함하는 통신 시스템에 관한 것으로서, 상기 단말들은 전송 매체 상에, 일정 수의 예약들의 할당을 요청하기 위한 수단을 포함한다. 본 발명은, 또한, 그러한 시스템에서 사용되기 위해 의도된 단말에 관한 것이고, 그러한 단말들이 전송 매체상에서 일정 수의 예약들을 할당받는 것을 허용하는 하는 요청 방법에 관한 것이다.

본 발명은, 특히, 양방향 위성 방송 시스템들에 적용된다.

네도 셀란드로니 및 에리나 페로에 의해 저술되고, 1991년 12월에, 제 12호, 39권의 통신에 대한 IEEE 회보 (transactions)에 편찬된, "FODA-TDMA 위성 접속 기법(scheme): 프레젠테이션, 시스템의 연구 및 결과들"이라는 제목의 논문은, 복수의 단말들이 마스터 스테이션과의 통신을 위한 시분할 다중 접속 메카니즘을 통하여, 전송 매체를 접속할 수 있는 통신 시스템을 기술한다. 이 메카니즘은 시간 간격들로 분할된 시간의 부-분할(sub-division)을 포함하며, 이 시간 간격들은 이들 단말들의 요청 시, 단말들로 다이나믹하게 할당된다. 따라서, 그 단말들은 요청들을 전송하고, 이 요청들은 단말들이 주어진 순간에 가지고 있어야할 시간 간격들의 수 R 을 나타낸다. 각 단말은, 단말이 요청을 하는 순간에, 전송 큐(queue) 내의 현재의 패킷들의 수를 기초로 이 수 R 을 계산한다.

발명이 이루고자 하는 기술적 과제

단말들에 의해 불필요하게 요청되는 예약들의 수를 제한하기 위하여 단말들의 요청 메카니즘을 최적화하는 방법을 제안하는 것이 본 발명의 목적이다. 따라서, 본 발명은 소스들의 분배에서 더 큰 효율성을 얻는 것을 가능하게 하고, 이는 전송 매체가 위성 채널인 경우에 특히 중요한데, 이런 종류의 매체가 특히 비용이 많이 들기 때문이다.

이 목적은, 본 출원서의 제 1 항, 제 2 항 및 제 3 항에서 각각 서술되는 것처럼 통신 시스템, 단말 및 요청 방법으로써 달성된다.

본 발명은, 어떤 통신 시스템에도 있는 전송 지연의 존재를 고려한다(특히, 위성에 의한 전송의 경우에, 전송 지연은 크다). 이 지연은 지터(jitter)되기 쉽다. 따라서, 마스터 스테이션이 단말들로 예약 할당들을 전송할때, 그 마스터 스테이션은 전송 지연의 최대값을 고려해야 한다. 이들 할당들은 그것들이 만료되기 전에(즉, 해당하는 시간 간격의 시작 전에) 도착하도록 충분히 일찍 발송되어야 한다. 일찍 도착하는 할당들은 할당들의 만료 일자까지 단말의 할당 메모리 내에 저장된다. 본 발명은 주어진 순간에 요청받은 예약들의 수를 계산하기 위하여 단말의 할당 메모리에 저장되는 할당들을 고려하는 것을

포함한다. 이 계획(strategy)은 마스터 스테이션에 의해 이미 할당된 예약들이 다시 요청되는 것을 방지하는 것을 가능하게 한다. 따라서, 본 발명은 단말들에 의해 궁극적으로(ultimately) 사용되지 않은 할당된 예약들의 수를 현저히 감소시킨다.

발명의 구성 및 작용

도 1은 전송 매체(3)를 통하여 통신하는 마스터 스테이션(1) 및 복수의 양방향 단말들(2)을 포함하는 통신 시스템의 예를 도시한다. 이 전송 매체의 상이한 유형들이 있을 수 있다. 예를 들어, 이것은 케이블 네트워크, 라디오 채널에 의한 전송, 또는 위성 채널에 의한 전송일 수 있다.

도 2에서 도면이 위성 통신 시스템을 도시하기 위하여, 예로서 선택되었고, 이것은, 전송 지연들에 관한 가장 큰 문제들을 제기하는 경우이기 때문이다. 그러나, 본 발명은 다른 전송 매체에 적용될 수 있다. 그 단말들(2)은 제 1 주파수 대역(Ka)을 사용하는 동안, 제 1 위성(4)을 통하여 마스터 스테이션(1)으로 요청들 및 데이터를 전송하고, 마스터 스테이션(1)은 제 2 주파수 대역(Ku)을 사용하는 동안 데이터 및 제어 정보를 제 2 위성(5)을 통하여 단말들(2)로 방송한다.

방금 기술된 예에서, 마스터 스테이션과 통신하기 위하여 양방향 단말들(2)은 시분할 다중 접속 메카니즘인 TDMA를 통하여 전송 매체(3)를 접속한다. 이를 위해, 그 시간은 시간 간격들로 분할되고, 시간 간격들은 상기 단말들의 요청 시, 마스터 스테이션에 의해 다이나믹하게 단말들에게 할당된다. 이것은, 전송 매체 상의 예약들이 단말들에 의하여 요청되고, 마스터 스테이션에 의하여 할당되며, 시간 간격들마다 형성된다는 것을 의미한다. 시간 간격들이 사용 가능한 상태로 있다면, 마스터 스테이션은 그 시간 간격들을 요구하지 않은 단말들에게, 시간 간격들을 자유롭게 할당할 수 있다. 단말들은, 예를 들어, 사용자 데이터 후에, 단말들에 할당된 시간 간격들 내에서 그들의 요청들을 전송한다. 이 경우에, 단말들이 통신을 시작했을 때, 그 단말들은, 마스터 스테이션이 그들에게 자유롭게 할당된 사용 가능한 시간 간격을 갖는 것을 기다려서, 요청을 전송할 수 있다.

수신된 요청들에 대해 응답하여, 마스터 스테이션은 단말들에게 일정 수의 시간 간격들을 할당한다. 이들 할당들은 단말들로 방송되고, 사용되기 위하여, 완료되기 전에 수신되어야만 한다.

각 단말(2)은 메모리(10)를 포함하고, 이 메모리(10)는 전송 큐이며, 전송되어야 하는 데이터는 패킷화되는 방식으로 전송 큐 내에 저장된다. 단말들이 일정 수의 시간 간격들을 할당받기 위하여 요청을 할때, 이 전송 메모리에 저장된 패킷들의 수(B)를 고려한다.

다양한 요청 메카니즘들이 제안되어 왔다. 예를 들어, 위에서 인용된 논문에서, 저자들은 제 1 메카니즘(X1)을 제안하며, 이 메카니즘은 주어진 순간에 단말의 전송 메모리의 내용들을 나타내는 요청들의 전송을 포함한다. 네트워크 헤드-엔드에서, 각 새로운 요청은 이전의 요청을 대체한다. 제 2 메카니즘(X2)은 르-엔코, 자항거 아이 모하메드 공저, 캐나다 오타와에서 1993년 10월 12-15일에 열린 보편적 개인용 통신들에 관한 2차 IEEE 국제 회의의 회보에 편찬된 "패킷 위성 통신들을 위한 조합된 자유/요구 할당 다중 접속(CFDAMA) 프로토콜들"이라는 논문의 2권 824부터 828페이지에서 제안되었다. 이 제 2 메카니즘(X2)은, 이미 요청되어, 단말에 부여될 예약들의 수를 계산하는 것을 포함한다. 카운터는 예약이 요청되는 단위시간만큼 증가되고, 할당이 수신되는 단위 시간만큼 감소된다. 단말에 의해 전송된 각 요청은 전송 메모리의 내용 및 이 카운터의 값 간의 차를 나타낸다. 마스터 스테이션에서, 각 새로운 요청이 이전의 요청에 가산된다.

본 발명은 사용된 요청 메카니즘에 독립적이다. 이제 설명될 것처럼, 본 발명은 요청하기 위하여 단말의 할당 메모리에서 저장되는 할당들을 고려하므로써 사용되는 요청 메카니즘의 성능의 향상을 포함한다.

어떤 전송 매체는 매체의 유형에 따라서 변화할 수 있는 다소의 지터되기 쉬운, 전송 지연을 도입한다. 이 전송 지연은 일반적으로 최대 값보다 작다. 따라서 마스터 스테이션에 의해 할당의 송신을 분리하는 지연 및 이 할당의 완료는 이 최대 값보다 크거나 동일하다. 할당들이 완료되기 전에 수신된 할당들은 사용되기 이전에 할당 메모리에 저장된다. 단말의 할당 메모리에 저장된 할당들은 이미 마스터 스테이션에 의해 부여된 요청들에 대응된다. 그러나 이들 할당들은 단말에 의해 아직 사용되지 않았다. 따라서, 데이터를 위해 할당들이 형성되고, 데이터는 전송 메모리에서 아직도 대기중이다. 이들 데이터를 위한 새로운 요청들의 형성을 방지하는 것이 본 발명의 목적이다. 따라서, 요청을 전송하기 위하여, 본 발명은 할당 메모리에 저장된 할당들의 수를 고려하는 것을 포함한다. 유익하게, 다른 종래의 요청 메카니즘의 수단에 의해 계산된 예약들의 수 R은 다음 값들 $R'=R'-A$ 에 의해 대체되고, 여기서, A는 할당 메모리에 저장된 할당들의 수를 나타낸다.

도 3은 본 발명에 따른 요청 방법을 도시한다. 상자(100)에서, 단말은 종래의 요청 계산 방법을 구현하므로써 값 R을 계산한다. 상자(110)에서, 단말은 값 $R'=R-A$ 을 계산한다. 상자(120)에서, 단말은 요청 R'을 전송한다.

도 4 및 5는 위성 통신 시스템의 경우에 발명에 의해 제공되는 향상점들의 중요한 곡선 도표들을 도시한다. 도 4는 제 1 요청 메카니즘 X1을 갖는 전송 네트워크의 부하 비율의 함수로써 사용되지 않은 할당들의 비율을 나타낸다. 그 사각형들은 본 발명으로 얻어진 결과들을 나타내고 십자선들은 본 발명없이 얻어진 결과들을 나타낸다. 도 5는, 제 2 요청 메카니즘 X2가 사용될 때, 얻어진 결과들을 나타낸다. 이들 2개의 곡선들은, 본 발명이 사용되지 않은 할당들의 비율을, 특히 중간 이하의 크기의 부하들에 대해, 현저히 감소시키는 것을 허용한다. 사용 가능한 남아있는 예약들의 수는, 마스터 스테이션이 단말들의 모든 요청들을 부여할 때, 더 높다. 마스터 스테이션은 할당들을 요구하지 않은 단말들에게 예약을 할당할 수 있다. 이것은 그 시스템의 성능을 향상시킨다; 그것은 특히, 한 주기의 비활성 이후에 통신하기 시작하는 단말을 위해 전송 메모리에서 평균 순환 지연을 감소시키는 것을 허용한다.

서술된 실시예들의 예에서, 단말들은 시간 분할 다중 접속 메카니즘을 통하여 전송 매체에 접속한다. 이것은 제한적이지 않다. 본 발명은 전송 매체를 접속하기 위한 다른 메카니즘들이 사용될 때, 예를 들어, 주파수 분할 다중 접속 메카니즘 FDMA 또는 코드 분할 다중 접속 메카니즘 CDMA와 결합된 시간 분할 다중 접속 메카니즘이 사용될 때, 응용할 수 있다. 고려하는 경우에 따라, 마스터 스테이션에 의해 할당되는 예약들은 시간 간격들, 시간 간격/반송파의 조합, 시간 간격/반송파/코드의 조합에 의해 형성된다.

발명의 효과

본 발명은 양방향 단말들이 마스터 스테이션에 정보를 전송하는 전송 매체 상에서 단말들에 할당되는 예약을 갖도록 허용하는 요청 메카니즘에 관한 것이다. 본 발명에 따르면, 단말이 아직 만료되지 않은 할당들을 수신할 때, 단말은 임시적으로 할당 메모리에 예약들을 저장하여서 새로운 요청이 전송될 때, 이 메모리에 포함된 할당들의 수를 고려하고 따라서, 이미 부여 받은 할당들에 대한 요청들이 다시 정해지는 것을 방지하도록 하게 된다.

(57) 청구의 범위

청구항 1.

적어도 하나의 마스터 스테이션(master station) 및 전송 매체를 통하여 상기 마스터 스테이션과 통신하고자 하는 복수의 단말들을 포함하고, 상기 단말들은 상기 전송 매체 상으로 일정 수의 예약들의 할당을 요청하기 위한 수단을 포함하는 통신 시스템에 있어서, 적어도 하나의 단말은,

-상기 단말에 이미 할당되어 있고, 상기 단말이 아직 사용하지 않은 예약들의 수를 나타내는 카운터, 및

-상기 카운터의 값을 고려하여, 요청될 예약들의 수를 정하는(formulating) 수단을 포함하는 것을 특징으로 하는, 통신 시스템.

청구항 2.

전송 매체를 통하여 통신 시스템의 마스터 스테이션과 통신하도록 의도되고, 상기 전송 매체 상으로 일정 수의 예약들의 할당을 요청하기 위한 수단을 포함하는 단말로서,

-상기 단말에 이미 할당되어 있고, 상기 단말이 아직 사용하지 않은 예약들의 수를 나타내는 카운터, 및

-상기 카운터의 값을 고려하여 요청될 예약들의 수를 정하는 수단을 포함하는 것을 특징으로 하는 단말.

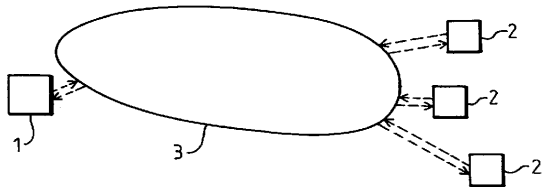
청구항 3.

전송 매체를 통해 통신 시스템의 마스터 스테이션과 통신하도록 의도된 단말이 상기 전송 매체 상에서 단말에 할당되는 일정 수의 예약들을 갖도록 할 수 있는 요청 방법으로서,

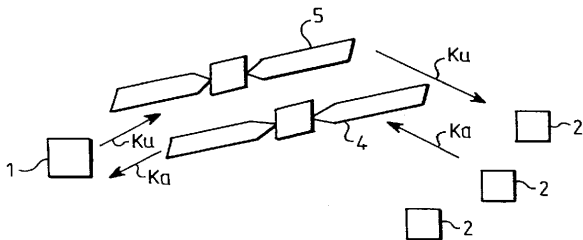
- 상기 단말에 이미 할당되어 있고, 상기 단말이 아직 사용하지 않은 예약들의 수를 나타내는 카운터를 저장하는 단계, 및
- 상기 카운터의 값을 고려하여 상기 단말에 대해 요청될 예약들의 수를 정하는 단계를 포함하는 것을 특징으로 하는 요청 방법.

도면

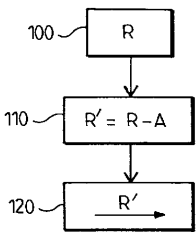
도면1



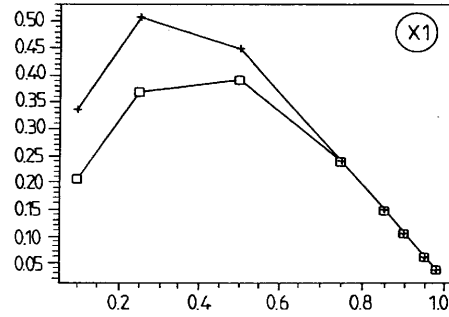
도면2



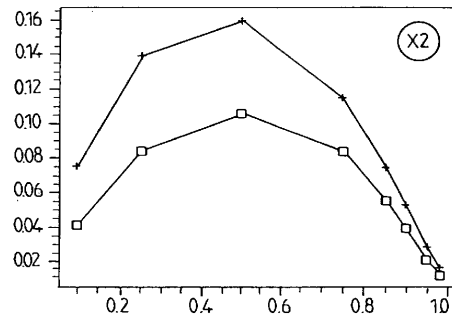
도면3



도면4



도면5



Electronic Acknowledgement Receipt	
EFS ID:	12677662
Application Number:	12901699
International Application Number:	
Confirmation Number:	1676
Title of Invention:	RESOURCE SHARING IN A TELECOMMUNICATIONS ENVIRONMENT
First Named Inventor/Applicant Name:	Marcos C. Tzannes
Customer Number:	62574
Filer:	Jason Vick/Joanne Vos
Filer Authorized By:	Jason Vick
Attorney Docket Number:	5550-54-CON-3
Receipt Date:	01-MAY-2012
Filing Date:	11-OCT-2010
Time Stamp:	16:57:36
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	no				
File Listing:					
Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1		IDS_09.pdf	358793 7ea348a0013c45e1ab36838b606faa7c177 eaa48	yes	4

	Multipart Description/PDF files in .zip description				
	Document Description		Start	End	
	Transmittal Letter		1	3	
	Information Disclosure Statement (IDS) Form (SB08)		4	4	
Warnings:					
Information:					
2	Foreign Reference	KR1020000047827.pdf	403475 1eb2e08b737f63b1b98cf7937bb3bafabc9d5c14	no	7
Warnings:					
Information:					
3	Non Patent Literature	5550-54-PKR_NOA_03-29-2012.pdf	847775 e19d832f97e517db6e02ded58df1a186f9060b36	no	4
Warnings:					
Information:					
4	Non Patent Literature	5550-54-PKR-DIV_NOA_03-29-2012.pdf	856807 b2175cb58e7fcd303526308cfb4ed963d12049d9	no	4
Warnings:					
Information:					
5	Non Patent Literature	5550-57-PCN_OA_03-07-2012.pdf	790537 72cf34d3071fbeb92aa164a6a97cb3f6242b4806	no	10
Warnings:					
Information:					
6	Non Patent Literature	5550-54-PJP-DIV_NOA_03-26-2012.pdf	56733 0c14f634e73ff4a9abfffe61f83ff096b6d48fd6	no	3
Warnings:					
Information:					
Total Files Size (in bytes):			3314120		

This Acknowledgement Receipt evidences receipt on the noted date by the USPTO of the indicated documents, characterized by the applicant, and including page counts, where applicable. It serves as evidence of receipt similar to a Post Card, as described in MPEP 503.

New Applications Under 35 U.S.C. 111

If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application.

National Stage of an International Application under 35 U.S.C. 371

If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.

New International Application Filed with the USPTO as a Receiving Office

If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In Re the Application of:	)	Group Art Unit: 2117
TZANNES, Marcos C.	)	Confirmation No.: 1676
Serial No.: 12/901,699	)	Examiner: Tabone Jr, John J.
Filed: October 11, 2010	)	
Atty. File No.: 5550-54-CON-3	)	<u>SUPPLEMENTAL</u>
Entitled: "RESOURCE SHARING IN A	)	<u>INFORMATION DISCLOSURE</u>
TELECOMMUNICATIONS ENVIRONMENT"	)	<u>STATEMENT</u>
	)	Electronically Submitted

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Dear Sir:

The references cited on attached Form PTO-1449 are being called to the attention of the Examiner.

- ☒ Copies of the cited non-patent and/or foreign references are enclosed herewith.
- ☐ Copies of the cited U.S. patents and/or patent applications are enclosed herewith.
- ☒ Copies of the cited U.S. patents/patent application publications are not enclosed in accordance with 37 C.F.R. § 1.98(a).
- ☐ Copies of the cited references are not enclosed, in accordance with 37 C.F.R. § 1.98(d), because the references were cited by or submitted to the U.S. Patent and Trademark Office in prior application Serial No. _____ filed _____, which is relied upon for an earlier filing date under 35 U.S.C. § 120.
- ☒ To the best of applicants' belief, the pertinence of the foreign-language references are believed to be summarized in the attached English translations and/or in the figures, although applicants do not necessarily vouch for the accuracy of the translation.
- ☐ Examiner's attention is drawn to the following related applications:
- Serial No. _____ filed _____ (Attorney Ref. No. _____)
- Serial No. _____ filed _____ (Attorney Ref. No. _____)
- ☐ Other: _____

Submission of the above information is not intended as an admission that any item is citable under the statutes or rules to support a rejection, that any item disclosed represents analogous art, or that those skilled in the art would refer to or recognize the pertinence of any reference without the benefit of hindsight, nor should an inference be

drawn as to the pertinence of the references based on the order in which they are presented. Submission of this statement should not be taken as an indication that a search has been conducted, or that no better art exists.

It is respectfully requested that the cited information be expressly considered during the prosecution of this application and the references made of record therein.

FEES

☐	37 CFR 1.97(b): No fee is believed due in connection with this submission, because the information disclosure statement submitted herewith is satisfied by one of the following conditions ("X" indicates satisfaction): ☐ Within three months of the filing date of a national application other than a continued prosecution application under 37 CFR 1.53(d), or ☐ Within three months of the date of entry of the national stage as set forth in § 1.491 in an international application, or ☐ Before the mailing date of a first Office Action on the merits, or ☐ Before the mailing of a first Office action after the filing of a request for continued examination under 37 CFR 1.114. Although no fee is believed due, if any fee is deemed due in connection with this submission, please charge such fee to Deposit Account 19-1970.
☒	37 CFR 1.97(c): The information disclosure statement transmitted herewith is being filed after all the above conditions (37 CFR 1.97(b)), but before the mailing date of any one of the following conditions: (1) a final action under 37 C.F.R. 1.113, or (2) a notice of allowance under 37 C.F.R. 1.311, or (3) an action that otherwise closes prosecution in the application. This Information Disclosure Statement is accompanied by: ☒ A Certification (below) as specified by 37 C.F.R. 1.97(e). Although no fee is believed due, if any fee is deemed due in connection with this submission, please charge such fee to Deposit Account 19-1970. OR ☐ Please charge Deposit Account 19-1970 in the amount of \$180.00 for the fee set forth in 37 C.F.R. 1.17(p) for submission of an information disclosure statement. Please credit any overpayment or charge any underpayment to Deposit Account 19-1970.
☐	37 CFR 1.97(d): This Information Disclosure Statement is being submitted after the period specified in 37 CFR 1.97(c). ☐ This information Disclosure Statement includes a Certification (below) as specified by 37 C.F.R. 1.97(e) AND ☐ Applicants hereby requests consideration of the reference(s) disclosed herein. Please charge Deposit Account 19-1970 in the amount of \$180.00 under 37 C.F.R. 1.17(p). Please credit any overpayment or charge any underpayment to Deposit Account 19-1970. Election to pay the fee should not be taken as an indication that applicant(s) cannot execute a certification.

Certification (37 C.F.R. 1.97(e))

(Applicable only if checked)



The undersigned certifies that:

☒ Each item of information contained in this information disclosure statement was first cited in any communication from a foreign patent office in a counterpart foreign application not more than three months prior to the filing of this statement. 37 C.F.R. 1.97(e)(1).

☒ A copy of the communication from the foreign patent office is enclosed.

OR

☐ No item of information contained in this information disclosure statement was cited in a communication from a foreign patent office in a counterpart foreign application, and, to the knowledge of the undersigned after making reasonable inquiry, no item of information contained in this Information Disclosure Statement was known to any individual designated in 37 C.F.R. 1.56(c) more than three months prior to the filing of this statement. 37 C.F.R. 1.97(e)(2).

Respectfully submitted,

SHERIDAN ROSS P.C.

By: _____

Jason H. Vick

Registration No. 45,285

1560 Broadway, Suite 1200

Denver, Colorado 80202-5141

(303) 863-9700

Date: 30 Apr '12

Substitute for form 1449A/PTO				Complete if Known	
INFORMATION DISCLOSURE STATEMENT BY APPLICANT				Application Number	12/901,699
				Filing Date	October 11, 2010
				First Named Inventor	Marcos C. Tzannes
				Art Unit	2117
				Examiner Name	Tabone Jr, John J.
Sheet	1	of	2	Attorney Docket Number	5550-54-CON-3

U.S. PATENT DOCUMENTS					
Examiner Initials*	Cite No. ¹	Document Number Number-kind Code ^{2 (if known)}	Publication Date MM-DD-YYYY	Name of Patentee of Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear
	1	7200792	04-03-2007	Kim et al.	
	2	2001/0014962	08-16-2001	Obuchi et al.	

FOREIGN PATENT DOCUMENTS						
Examiner Initials*	Cite No. ¹	Foreign Patent Document Country Code ³ ; Number ⁴ ; Kind Code ⁵ (if known)	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear	T ⁶
	3	JP 07-254862	10-03-1995	Sony CORP.		(includes English abstract and partial mechanical translation)
	4	JP 2003-224615	08-08-2003	SAMSUNG ELECTRONICS CO LTD.		(corresponds to US 7,200,792 cited herein)
	5	JP 2005-522963	07-28-2005	INTERDIGITAL TECHNOLOGY CORPORATION		(corresponds to WO 03/090011 cited herein)
	6	WO00/52834	10-30-2003	FUJITSU LIMITED		(corresponds to US2001/0014962 cited herein)
	7	WO 03/090011	10-30-2003	INTERDIGITAL TECHNOLOGY CORPORATION		
	8	EP 1041756	10-04-2000	LUCENT TECHNOLOGIES INC.		(corresponds to JP 2000-341247 previously cited by Applicants on 10-17-2011)

Examiner Signature		Date Considered	

*EXAMINER: Initial if reference is considered, whether or not citation is in conformance and not considered. Include copy of this form with next communication to applicant.

Substitute for form 1449A/PTO				Complete if Known	
INFORMATION DISCLOSURE STATEMENT BY APPLICANT				Application Number	12/901,699
				Filing Date	October 11, 2010
				First Named Inventor	Marcos C. Tzannes
				Art Unit	2117
				Examiner Name	Tabone Jr, John J.
Sheet	2	of	2	Attorney Docket Number	5550-54-CON-3

OTHER ART (Including Author, Title, Date, Pertinent Pages, etc.)		
Examiner Initials*	Cite No. ¹	
	9	Official Action (including translation) for Japanese Patent Application No. 2008-264540, dispatched Dec. 12, 2011 (Attorney Ref. No. 5550-54-PJP-DIV)

Examiner Signature		Date Considered	

*EXAMINER: Initial if reference is considered, whether or not citation is in conformance and not considered. Include copy of this form with next communication to applicant.

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(12) 公開特許公報 (A)

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H 0 4 J 13/00		27/00	E 5 K 0 1 4
H 0 4 L 1/00		H 0 4 J 13/00	A 5 K 0 2 2

審査請求 有 請求項の数103 ○L 外国語出願 (全123頁)

(21) 出願番号	特願2002-371079(P2002-371079)	(71) 出願人	390019839 三星電子株式会社 大韓民国京畿道水原市八達区梅灘洞416
(22) 出願日	平成14年12月20日 (2002. 12. 20)	(72) 発明者	金 憲基 大韓民国ソウル特別市銅雀區舍堂洞 (番地なし) 新東亜アパート406棟1006號
(31) 優先権主張番号	2 0 0 1 - 0 8 3 0 6 4	(72) 発明者	崔 鎮圭 大韓民国ソウル特別市鐘路區明倫洞 2 街 4 番地 亞南アパート101棟104號
(32) 優先日	平成13年12月21日 (2001. 12. 21)	(74) 代理人	100064908 弁理士 志賀 正武 (外1名)
(33) 優先権主張国	韓国 (K R)		

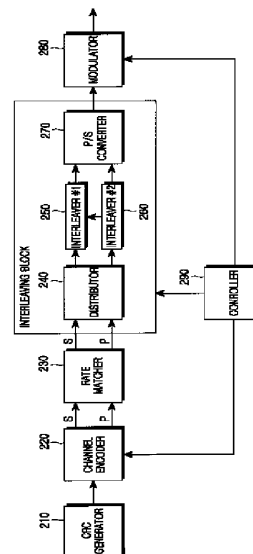
最終頁に続く

(54) 【発明の名称】 高速ダウンリンクパケットアクセス移動通信システムにおけるシンボルマッピングのためのインターリーピング装置及び方法

(57) 【要約】

【課題】 高速ダウンリンクパケットアクセス移動通信システムにおけるシンボルマッピングのためのインターリーピング装置及び方法を提供する。

【解決手段】 インターリーパは、高い重要度を有する符号化ビットと相対的に低い重要度を有する符号化ビットとの比率によってその内部に備わったバッファの領域を第1書き込み領域と第2書き込み領域に区分し、前記高い重要度を有する符号化ビットのストリームを前記第1書き込み領域内の前記列のうち一番目の列から最後の列まで行方向に順次に書き込み、前記相対的に低い重要度を有する符号化ビットのストリームを前記第2書き込み領域内の前記列のうち一番目の列から最後の列まで行方向に順次に書き込み、前記バッファ領域の前記列を所定の規則によって交換して再配列する。



【特許請求の範囲】

【請求項1】 複数の行及び列から構成されたビットを書き込む領域を有するバッファを備える移動通信システムの送信装置で、所定の符号化率によって符号化された符号化ビットをインターリーブする方法において、前記符号化ビットのうち高い重要度を有する符号化ビットと相対的に低い重要度を有する符号化ビットとの比率によって、前記バッファの領域を第1書き込み領域と第2書き込み領域に区分する過程と、前記高い重要度を有する符号化ビットのストリームを前記第1書き込み領域内の前記列のうち一番目の列から最後の列まで行方向に順次に書き込み、前記相対的に低い重要度を有する符号化ビットのストリームを前記第2書き込み領域内の前記列のうち一番目の列から最後の列まで行方向に順次に書き込む過程と、前記バッファ領域の前記列を所定の規則によって交換して再配列する過程と、前記バッファ領域の前記行を同一のサイズを有する第1読み出し領域と第2読み出し領域に両分する過程と、所定の変調方式によって決定された数だけのビットを前記第1読み出し領域及び前記第2読み出し領域から交代に読み出す動作において、前記ビットを前記それぞれの第1読み出し領域及び第2読み出し領域の行のうち一番目の行から最後の行まで列方向に順次に読み出す過程と、を含むことを特徴とする方法。

【請求項2】 前記第1読み出し領域から読み出される符号化ビットをシンボルの第1信頼度を有する位置にマッピングし、前記第2読み出し領域から読み出される符号化ビットを前記第1信頼度より低い第2信頼度を有する位置にマッピングする過程をさらに含むことを特徴とする請求項1記載の方法。

【請求項3】 前記符号化ビットを変調する方式が16QAMである場合、前記第1読み出し領域及び前記第2読み出し領域から読み出されるビットは、それぞれ2ビット単位で交代に読み出されることを特徴とする請求項1記載の方法。

【請求項4】 前記符号化ビットを変調する方式が64QAMである場合、前記第1読み出し領域及び前記第2読み出し領域から読み出されるビットは、それぞれ3ビット単位で交代に読み出されることを特徴とする請求項1記載の方法。

【請求項5】 前記符号化ビットを書き込んだ後、使用されなかった残りのバッファの領域に補助ビットを挿入することを特徴とする請求項1記載の方法。

【請求項6】 前記補助ビットは、前記第1書き込み領域と前記第2書き込み領域との間に挿入されることを特徴とする請求項5記載の方法。

【請求項7】 前記補助ビットは、前記バッファ領域内の前記第2書き込み領域の符号化ビットの次に挿入され

ることを特徴とする請求項5記載の方法。

【請求項8】 前記高い重要度を有する符号化ビットは、システムティックビットであることを特徴とする請求項1記載の方法。

【請求項9】 前記低い重要度を有する符号化ビットは、パリティビットであることを特徴とする請求項1記載の方法。

【請求項10】 前記高い重要度を有する符号化ビットと相対的に低い重要度を有する符号化ビットとの比率は、前記所定の符号化率によって決定されることを特徴とする請求項1記載の方法。

【請求項11】 複数の行及び列から構成されたビットを書き込む領域を有するバッファを備える移動通信システムの送信装置で、所定の符号化率によって符号化された符号化ビットをインターリーブする方法において、前記符号化ビットのうち高い重要度を有する符号化ビットと相対的に低い重要度を有する符号化ビットとの比率によって、前記バッファの領域を第1書き込み領域と第2書き込み領域に区分する過程と、前記高い重要度を有する符号化ビットのストリームを前記第1書き込み領域内の前記列のうち一番目の列から最後の列まで行方向に順次に書き込み、前記相対的に低い重要度を有する符号化ビットのストリームを前記第2書き込み領域内の前記列のうち一番目の列から最後の列まで行方向に順次に書き込む過程と、前記バッファ領域の前記列を所定の規則によって交換して再配列する過程と、前記バッファ領域の前記行を同一のサイズを有する第1読み出し領域と第2読み出し領域に両分する過程と、前記それぞれの第1読み出し領域及び第2読み出し領域の行のうち所定の変調方式によって決定された数だけの行を、前記第1読み出し領域と第2読み出し領域との間に交換して再配列する過程と、前記第1読み出し領域及び第2読み出し領域から構成された前記全体バッファ領域の行を一番目の行から最後の行まで列方向に順次に読み出す過程と、を含むことを特徴とする方法。

【請求項12】 前記第1読み出し領域から読み出される符号化ビットをシンボルの第1信頼度を有する位置にマッピングし、前記第2読み出し領域から読み出される符号化ビットを前記第1信頼度より低い第2信頼度を有する位置にマッピングする過程をさらに含むことを特徴とする請求項11記載の方法。

【請求項13】 前記符号化ビットを変調する方式が16QAMである場合、前記第1読み出し領域及び前記第2読み出し領域から読み出されるビットは、それぞれ2ビット単位で交代に読み出されることを特徴とする請求項11記載の方法。

【請求項14】 前記符号化ビットを変調する方式が64QAMである場合、前記第1読み出し領域及び前記第

2読み出し領域から読み出されるビットは、それぞれ3ビット単位で交代に読み出されることを特徴とする請求項1記載の方法。

【請求項15】 前記符号化ビットを書き込んだ後、使用されなかった残りのバッファの領域に補助ビットを挿入することを特徴とする請求項1記載の方法。

【請求項16】 前記補助ビットは、前記第1書き込み領域と前記第2書き込み領域との間に挿入されることを特徴とする請求項15記載の方法。

【請求項17】 前記補助ビットは、前記バッファ領域内の前記第2書き込み領域の符号化ビットの次に挿入されることを特徴とする請求項15記載の方法。

【請求項18】 前記高い重要度を有する符号化ビットは、システマティックビットであることを特徴とする請求項1記載の方法。

【請求項19】 前記低い重要度を有する符号化ビットは、パリティビットであることを特徴とする請求項1記載の方法。

【請求項20】 前記高い重要度を有する符号化ビットと相対的に低い重要度を有する符号化ビットとの比率は、前記所定の符号化率によって決定されることを特徴とする請求項1記載の方法。

【請求項21】 複数の行及び列から構成されたビットを書き込む領域を有するバッファを備える移动通信システムの送信装置で、所定の符号化率によって符号化された符号化ビットをインターリーブする方法において、前記符号化ビットのうち高い重要度を有する符号化ビットと相対的に低い重要度を有する符号化ビットとの比率によって、前記バッファの領域を第1書き込み領域と第2書き込み領域に区分する過程と、

前記高い重要度を有する符号化ビットのストリームを前記第1書き込み領域内の前記列のうち一番目の列から最後の列まで行方向に順次に書き込み、前記相対的に低い重要度を有する符号化ビットのストリームを前記第2書き込み領域内の前記列のうち最後の列から一番目の列まで行方向に逆順に書き込む動作において、前記符号化ビットのストリームを前記第2書き込み領域内の最後の行から一番目の行まで逆方向に書き込む過程と、

前記バッファ領域の前記列を所定の規則によって交換して再配列する過程と、

前記バッファ領域の前記行を同一のサイズを有する第1読み出し領域と第2読み出し領域に両分する過程と、所定の変調方式によって決定された数だけのビットを前記第1読み出し領域及び前記第2読み出し領域から交代に読み出す動作において、前記ビットを前記それぞれの第1読み出し領域及び第2読み出し領域の行のうち一番目の行から最後の行まで列方向に順次に読み出す過程と、

を含むことを特徴とする方法。

【請求項22】 前記第1読み出し領域から読み出され

る符号化ビットをシンボルの第1信頼度を有する位置にマッピングし、前記第2読み出し領域から読み出される符号化ビットを前記第1信頼度より低い第2信頼度を有する位置にマッピングする過程をさらに含むことを特徴とする請求項21記載の方法。

【請求項23】 前記符号化ビットを変調する方式が16QAMである場合、前記それぞれの第1読み出し領域及び第2読み出し領域の行は、前記バッファ領域において前記第1読み出し領域の行と前記第2読み出し領域の行がそれぞれ2行ずつ交代に配置されるように交換して再配列されることを特徴とする請求項21記載の方法。

【請求項24】 前記符号化ビットを変調する方式が64QAMである場合、前記それぞれの第1読み出し領域及び第2読み出し領域の行は、前記バッファ領域において前記第1読み出し領域の行と前記第2読み出し領域の行がそれぞれ3行ずつ交代に配置されるように交換して再配列されることを特徴とする請求項21記載の方法。

【請求項25】 前記符号化ビットを書き込んだ後、使用されなかった残りのバッファの領域に補助ビットを挿入することを特徴とする請求項21記載の方法。

【請求項26】 前記補助ビットは、前記第1書き込み領域と前記第2書き込み領域との間に挿入されることを特徴とする請求項25記載の方法。

【請求項27】 前記補助ビットは、前記バッファ領域内の前記第2書き込み領域の符号化ビットの次に挿入されることを特徴とする請求項25記載の方法。

【請求項28】 前記高い重要度を有する符号化ビットは、システマティックビットであることを特徴とする請求項21記載の方法。

【請求項29】 前記低い重要度を有する符号化ビットは、パリティビットであることを特徴とする請求項21記載の方法。

【請求項30】 前記高い重要度を有する符号化ビットと相対的に低い重要度を有する符号化ビットとの比率は、前記所定の符号化率によって決定されることを特徴とする請求項21記載の方法。

【請求項31】 複数の行及び列から構成されたビットを書き込む領域を有するバッファを備える移动通信システムの送信装置で、所定の符号化率によって符号化された符号化ビットをインターリーブする方法において、前記符号化ビットのうち高い重要度を有する符号化ビットと相対的に低い重要度を有する符号化ビットとの比率によって、前記バッファの領域を第1書き込み領域と第2書き込み領域に区分する過程と、

前記高い重要度を有する符号化ビットのストリームを前記第1書き込み領域内の前記列のうち一番目の列から最後の列まで行方向に順次に書き込み、前記相対的に低い重要度を有する符号化ビットのストリームを前記第2書き込み領域内の前記列のうち最後の列から一番目の列まで行方向に逆順に書き込む動作において、前記符号化ビ

ットのストリームを前記第2書き込み領域内の最後の行から一番目の行まで逆方向に書き込む過程と、
前記バッファ領域の前記列を所定の規則によって交換して再配列する過程と、
前記バッファ領域の前記行を同一のサイズを有する第1読み出し領域と第2読み出し領域に両分する過程と、
所定の変調方式によって決定された数だけのビットを前記第1読み出し領域及び前記第2読み出し領域から交代に読み出す動作において、前記ビットを前記それぞれの第1読み出し領域及び第2読み出し領域の行のうち一番目の行から最後の行まで列方向に順次に読み出す過程と、
を含むことを特徴とする方法。

【請求項32】 前記第1読み出し領域から読み出される符号化ビットをシンボルの第1信頼度を有する位置にマッピングし、前記第2読み出し領域から読み出される符号化ビットを前記第1信頼度より低い第2信頼度を有する位置にマッピングする過程をさらに含むことを特徴とする請求項31記載の方法。

【請求項33】 前記符号化ビットを変調する方式が16QAMである場合、前記それぞれの第1読み出し領域及び第2読み出し領域の行は、前記バッファ領域において前記第1読み出し領域の行と前記第2読み出し領域の行がそれぞれ2行ずつ交代に配置されるように交換して再配列されることを特徴とする請求項31記載の方法。

【請求項34】 前記符号化ビットを変調する方式が16QAMである場合、前記それぞれの第1読み出し領域及び第2読み出し領域の行は、前記バッファ領域において前記第1読み出し領域の行と前記第2読み出し領域の行がそれぞれ3行ずつ交代に配置されるように交換して再配列されることを特徴とする請求項31記載の方法。

【請求項35】 前記符号化ビットを書き込んだ後、使用されなかった残りのバッファの領域に補助ビットを挿入することを特徴とする請求項31記載の方法。

【請求項36】 前記補助ビットは、前記第1書き込み領域と前記第2書き込み領域との間に挿入されることを特徴とする請求項35記載の方法。

【請求項37】 前記補助ビットは、前記バッファ領域内の前記第2書き込み領域の符号化ビットの次に挿入されることを特徴とする請求項35記載の方法。

【請求項38】 前記高い重要性を有する符号化ビットは、システムティックビットであることを特徴とする請求項31記載の方法。

【請求項39】 前記低い重要性を有する符号化ビットは、パリティビットであることを特徴とする請求項31記載の方法。

【請求項40】 前記高い重要性を有する符号化ビットと相対的に低い重要性を有する符号化ビットとの比率は、前記所定の符号化率によって決定されることを特徴とする請求項31記載の方法。

【請求項41】 それぞれ複数の行及び列から構成されたビットを書き込む領域を有する2つのバッファを備える移動通信システムの送信装置で、所定の符号化率によって符号化された符号化ビットをインターリーブする方法において、

前記符号化ビットのうち高い重要性を有する符号化ビットを第1バッファに書き込み、相対的に低い重要性を有する符号化ビットを第2バッファに書き込む動作において、前記高い重要性を有する符号化ビットのストリームを前記第1バッファの前記列のうち一番目の列から最後の列まで行方向に順次に書き込み、前記相対的に低い重要性を有する符号化ビットのストリームを前記第2バッファの前記列のうち一番目の列から最後の列まで行方向に順次に書き込む過程と、

前記第1バッファ及び第2バッファの前記列を所定の規則によって交換して再配列する過程と、
所定の変調方式によって決定された数だけのビットを前記第1バッファ及び前記第2バッファから交代に読み出す動作において、前記ビットを前記それぞれの第1バッファ及び第2バッファの行のうち一番目の行から最後の行まで列方向に順次に読み出す過程と、
を含むことを特徴とする方法。

【請求項42】 前記第1バッファから読み出される符号化ビットをシンボルの第1信頼度を有する位置にマッピングし、前記第2バッファから読み出した符号化ビットを前記第1信頼度より低い第2信頼度を有する位置にマッピングする過程をさらに含むことを特徴とする請求項41記載の方法。

【請求項43】 前記符号化ビットを変調する方式が16QAMである場合、前記第1バッファから読み出されるビット及び前記第2バッファから読み出されるビットは、2ビット単位で交代に読み出されることを特徴とする請求項41記載の方法。

【請求項44】 前記符号化ビットを変調する方式が64QAMである場合、前記第1バッファから読み出されるビット及び前記第2バッファから読み出されるビットは、3ビット単位で交代に読み出されることを特徴とする請求項41記載の方法。

【請求項45】 前記符号化ビットを書き込んだ後、使用されなかった残りのバッファの領域に補助ビットを挿入することを特徴とする請求項41記載の方法。

【請求項46】 前記高い重要性を有する符号化ビットは、システムティックビットであることを特徴とする請求項41記載の方法。

【請求項47】 前記低い重要性を有する符号化ビットは、パリティビットであることを特徴とする請求項41記載の方法。

【請求項48】 前記高い重要性を有する符号化ビットと相対的に低い重要性を有する符号化ビットとの比率は、前記所定の符号化率によって決定されることを特徴

とする請求項41記載の方法。

【請求項49】 前記第1バッファのサイズが前記高い重要性度を有する符号化ビットの総数に対して足りない場合、前記高い重要性度を有する符号化ビットのうち前記第1バッファに書き込まれない符号化ビットを前記第2バッファの前記列のうち一番目の列から行方向に順次に書き込み、前記相対的に低い重要性度を有する符号化ビットのストリームを前記第2バッファ内の残りの領域内の前記列のうち一番目の列から最後の列まで行方向に順次に書き込む過程をさらに含むことを特徴とする請求項41記載の方法。

【請求項50】 前記第1バッファの書き込み領域及び前記第2バッファの書き込み領域は、同一のサイズを有することを特徴とする請求項49記載の方法。

【請求項51】 伝送しようとするデータを所定の符号化率によって高い重要性度を有する符号化ビット及び相対的に低い重要性度を有する符号化ビットから構成された符号化ビットに符号化する符号化器、及び複数の行及び列から構成されたビットを書き込む領域を有するバッファを備える移动通信システムの送信装置で、所定の符号化率によって符号化された符号化ビットをインターリーブする装置において、

高い重要性度を有する符号化ビットと相対的に低い重要性度を有する符号化ビットとの比率によってその内部に備わったバッファの領域を第1書き込み領域と第2書き込み領域に区分し、前記高い重要性度を有する符号化ビットのストリームを前記第1書き込み領域内の前記列のうち一番目の列から最後の列まで行方向に順次に書き込み、前記相対的に低い重要性度を有する符号化ビットのストリームを前記第2書き込み領域内の前記列のうち一番目の列から最後の列まで行方向に順次に書き込み、前記バッファ領域の前記列を所定の規則によって交換して再配列するインターリーブと、

前記バッファ領域の前記列を同一のサイズを有する第1読み出し領域と第2読み出し領域に分割し、所定の変調方式によって決定された数だけのビットを前記第1読み出し領域及び前記第2読み出し領域から交代に読み出す動作において、前記ビットを前記それぞれの第1読み出し領域及び第2読み出し領域の行のうち一番目の行から最後の行まで列方向に順次に読み出し、前記読み出された符号化ビットを多重化するマルチプレクサと、を含むことを特徴とする装置。

【請求項52】 前記バッファの第1読み出し領域から読み出される符号化ビットをシンボルの第1信頼度を有する位置にマッピングし、前記バッファの第2読み出し領域から読み出される符号化ビットを前記第1信頼度より低い第2信頼度を有する位置にマッピングする変調部をさらに備えることを特徴とする請求項51記載の装置。

【請求項53】 前記符号化ビットを変調する方式が1

6QAMである場合、前記インターリーブ内に備わった前記バッファの前記それぞれの第1読み出し領域及び第2読み出し領域から読み出されるビットは、2ビット単位で交代に読み出されることを特徴とする請求項51記載の装置。

【請求項54】 前記符号化ビットを変調する方式が64QAMである場合、前記インターリーブ内に備わった前記バッファの前記それぞれの第1読み出し領域及び第2読み出し領域から読み出されるビットは、3ビット単位で交代に読み出されることを特徴とする請求項51記載の装置。

【請求項55】 前記符号化ビットを書き込んだ後、使用されなかった残りのバッファ領域に補助ビットを挿入することを特徴とする請求項51記載の装置。

【請求項56】 前記インターリーブは、前記補助ビットを前記第1書き込み領域と前記第2書き込み領域との間に挿入することを特徴とする請求項55記載の装置。

【請求項57】 前記インターリーブは、前記補助ビットを前記第2書き込み領域の符号化ビットの次に挿入することを特徴とする請求項55記載の装置。

【請求項58】 前記高い重要性度を有する符号化ビットは、システムティックビットであることを特徴とする請求項51の装置。

【請求項59】 前記低い重要性度を有する符号化ビットは、パリティビットであることを特徴とする請求項51記載の装置。

【請求項60】 前記高い重要性度を有する符号化ビットと相対的に低い重要性度を有する符号化ビットとの比率は、前記所定の符号化率によって決定されることを特徴とする請求項51記載の装置。

【請求項61】 伝送しようとするデータを所定の符号化率によって高い重要性度を有する符号化ビット及び相対的に低い重要性度を有する符号化ビットから構成された符号化ビットに符号化する符号化器、及び複数の行及び列から構成されたビットを書き込む領域を有するバッファを備える移动通信システムの送信装置で、所定の符号化率によって符号化された符号化ビットをインターリーブする装置において、

高い重要性度を有する符号化ビットと相対的に低い重要性度を有する符号化ビットとの比率によって前記バッファの領域を第1書き込み領域と第2書き込み領域に区分し、前記高い重要性度を有する符号化ビットのストリームを前記第1書き込み領域内の前記列のうち一番目の列から最後の列まで行方向に順次に書き込み、前記相対的に低い重要性度を有する符号化ビットのストリームを前記第2書き込み領域内の前記列のうち一番目の列から最後の列まで行方向に順次に書き込み、前記バッファ領域の前記列を所定の規則によって交換して再配列し、前記バッファ領域の前記行を同一のサイズを有する第1読み出し領域と第2読み出し領域に分割し、前記それぞれの第1読み

出し領域及び第2読み出し領域の行のうち所定の変調方式によって決定された数だけの行を前記第1読み出し領域と第2読み出し領域との間に交換して再配列するインターリーバを含むことを特徴とする装置。

【請求項62】 前記バッファの第1読み出し領域から読み出される符号化ビットをシンボルの第1信頼度を有する位置にマッピングし、前記バッファの第2読み出し領域から読み出される符号化ビットを前記第1信頼度より低い第2信頼度を有する位置にマッピングする変調部をさらに備えることを特徴とする請求項61記載の装置。

【請求項63】 前記符号化ビットを変調する方式が16QAMである場合、前記インターリーバ内に備わった前記バッファの前記それぞれの第1読み出し領域及び第2読み出し領域から読み出されるビットは、2ビット単位で交代に読み出されることを特徴とする請求項61記載の装置。

【請求項64】 前記符号化ビットを変調する方式が64QAMである場合、前記インターリーバ内に備わった前記バッファの前記それぞれの第1読み出し領域及び第2読み出し領域から読み出されるビットは、3ビット単位で交代に読み出されることを特徴とする請求項61記載の装置。

【請求項65】 前記符号化ビットを書き込んだ後、使用されなかった残りのバッファ領域に補助ビットを挿入することを特徴とする請求項61記載の装置。

【請求項66】 前記インターリーバは、前記補助ビットを前記第1書き込み領域と前記第2書き込み領域との間に挿入することを特徴とする請求項65記載の装置。

【請求項67】 前記インターリーバは、前記補助ビットを前記第2書き込み領域の符号化ビットの次に挿入することを特徴とする請求項65記載の装置。

【請求項68】 前記高い重要性を有する符号化ビットは、システムティックビットであることを特徴とする請求項61の装置。

【請求項69】 前記低い重要性を有する符号化ビットは、パリティビットであることを特徴とする請求項61記載の装置。

【請求項70】 前記高い重要性を有する符号化ビットと相対的に低い重要性を有する符号化ビットとの比率は、前記所定の符号化率によって決定されることを特徴とする請求項61記載の装置。

【請求項71】 伝送しようとするデータを所定の符号化率によって高い重要性を有する符号化ビット及び相対的に低い重要性を有する符号化ビットから構成された符号化ビットに符号化する符号化器、及び複数の行及び列から構成されたビットを書き込む領域を有するバッファを備える移動通信システムの送信装置で、所定の符号化率によって符号化された符号化ビットをインターリーブする装置において、

高い重要性を有する符号化ビットと相対的に低い重要性を有する符号化ビットとの比率によって前記バッファの領域を第1書き込み領域と第2書き込み領域に区分し、前記高い重要性を有する符号化ビットのストリームを前記第1書き込み領域内の前記列のうち一番目の列から最後の列まで行方向に順次書き込み、前記相対的に低い重要性を有する符号化ビットのストリームを前記第2書き込み領域内の前記列のうち最後の列から一番目の列まで行方向に書き込む時、前記符号化ビットのストリームを前記第2書き込み領域内の最後の行から一番目の行まで逆方向に書き込み、前記バッファ領域の前記列を所定の規則によって交換して再配列するインターリーバと、前記バッファ領域の前記行を同一のサイズを有する第1読み出し領域と第2読み出し領域に分割し、所定の変調方式によって決定された数だけのビットを前記第1読み出し領域及び前記第2読み出し領域から交代に読み出し、前記それぞれの第1読み出し領域及び第2読み出し領域の行のうち一番目の行から最後の行まで列方向に符号化ビットを順次に読み出し、前記読み出された符号化ビットを多重化するマルチプレクサと、を含むことを特徴とする装置。

【請求項72】 前記バッファの第1読み出し領域から読み出される符号化ビットをシンボルの第1信頼度を有する位置にマッピングし、前記バッファの第2読み出し領域から読み出される符号化ビットを前記第1信頼度より低い第2信頼度を有する位置にマッピングする変調部をさらに備えることを特徴とする請求項71記載の装置。

【請求項73】 前記符号化ビットを変調する方式が16QAMである場合、前記バッファの前記第1読み出し領域及び前記第2読み出し領域の行を交換して再配列する前記インターリーバは、前記バッファ領域における前記第1読み出し領域の行及び前記第2読み出し領域の行を2行ずつ交代に配列することを特徴とする請求項71記載の装置。

【請求項74】 前記符号化ビットを変調する方式が64QAMである場合、前記バッファの前記第1読み出し領域及び前記第2読み出し領域の行を交換して再配列する前記インターリーバは、前記バッファ領域における前記第1読み出し領域の行及び前記第2読み出し領域の行を3行ずつ交代に配列することを特徴とする請求項71記載の装置。

【請求項75】 前記符号化ビットを書き込んだ後、使用されなかった残りのバッファ領域に補助ビットを挿入することを特徴とする請求項71記載の装置。

【請求項76】 前記インターリーバは、前記補助ビットを前記第1書き込み領域と前記第2書き込み領域との間に挿入することを特徴とする請求項75記載の装置。

【請求項77】 前記インターリーバは、前記補助ビットを前記第2書き込み領域の符号化ビットの次に挿入す

ることを特徴とする請求項75記載の装置。

【請求項78】 前記高い重要性度を有する符号化ビットは、システムティックビットであることを特徴とする請求項71記載の装置。

【請求項79】 前記低い重要性度を有する符号化ビットは、パリティビットであることを特徴とする請求項71記載の装置。

【請求項80】 前記高い重要性度を有する符号化ビットと相対的に低い重要性度を有する符号化ビットとの比率は、前記所定の符号化率によって決定されることを特徴とする請求項71記載の装置。

【請求項81】 伝送しようとするデータを所定の符号化率によって高い重要性度を有する符号化ビット及び相対的に低い重要性度を有する符号化ビットから構成された符号化ビットに符号化する符号化器、及び複数の行及び列から構成されたビットを書き込む領域を有するバッファを備える移動通信システムの送信装置で、所定の符号化率によって符号化された符号化ビットをインターリーブする装置において、高い重要性度を有する符号化ビットと相対的に低い重要性度を有する符号化ビットとの比率によって前記バッファの領域を第1書き込み領域と第2書き込み領域に区分し、前記高い重要性度を有する符号化ビットのストリームを前記第1書き込み領域内の前記列のうち一番目の列から最後の列まで行方向に順次書き込み、前記相対的に低い重要性度を有する符号化ビットのストリームを前記第2書き込み領域内の前記列のうち最後の列から一番目の列まで行方向に書き込む時、前記符号化ビットのストリームを前記第2書き込み領域内の最後の行から一番目の行まで逆方向に書き込み、前記バッファ領域の前記列を所定の規則によって交換して再配列し、前記バッファ領域の前記行を同一のサイズを有する第1読み出し領域及び第2読み出し領域に分割し、前記それぞれの第1読み出し領域及び第2読み出し領域の行のうち所定の変調方式によって決定された数だけの行を前記第1読み出し領域と第2読み出し領域との間に交換して再配列するインターリーバを含むことを特徴とする装置。

【請求項82】 前記バッファの第1読み出し領域から読み出される符号化ビットをシンボルの第1信頼度を有する位置にマッピングし、前記バッファの第2読み出し領域から読み出される符号化ビットを前記第1信頼度より低い第2信頼度を有する位置にマッピングする変調部をさらに備えることを特徴とする請求項81記載の装置。

【請求項83】 前記符号化ビットを変調する方式が16QAMである場合、前記バッファの前記第1読み出し領域及び前記第2読み出し領域の行を交換して再配列する前記インターリーバは、前記バッファ領域においてそれぞれ前記第1読み出し領域の行及び前記第2読み出し領域の行を2行ずつ交代に配列するを特徴とする請求項

81記載の装置。

【請求項84】 前記符号化ビットを変調する方式が64QAMである場合、前記バッファの前記第1読み出し領域及び前記第2読み出し領域の行を交換して再配列する前記インターリーバは、前記バッファ領域においてそれぞれ前記第1読み出し領域の行及び前記第2読み出し領域の行を3行ずつ交代に配列するを特徴とする請求項81記載の装置。

【請求項85】 前記符号化ビットを書き込んだ後、使用されなかった残りのバッファ領域に補助ビットを挿入することを特徴とする請求項81記載の装置。

【請求項86】 前記インターリーバは、前記補助ビットを前記第1書き込み領域と前記第2書き込み領域との間に挿入することを特徴とする請求項85記載の装置。

【請求項87】 前記インターリーバは、前記補助ビットを前記バッファ領域の前記第2書き込み領域のビットの次に挿入することを特徴とする請求項85記載の装置。

【請求項88】 前記高い重要性度を有する符号化ビットは、システムティックビットであることを特徴とする請求項81記載の装置。

【請求項89】 前記低い重要性度を有する符号化ビットは、パリティビットであることを特徴とする請求項81記載の装置。

【請求項90】 前記高い重要性度を有する符号化ビットと相対的に低い重要性度を有する符号化ビットとの比率は、前記所定の符号化率によって決定されることを特徴とする請求項81記載の装置。

【請求項91】 伝送しようとするデータを所定の符号化率によって高い重要性度を有する符号化ビット及び相対的に低い重要性度を有する符号化ビットから構成された符号化ビットに符号化する符号化器、及び複数の行及び列から構成されたビットを書き込む領域を有するバッファを備える移動通信システムの送信装置で、所定の符号化率によって符号化された符号化ビットをインターリーブする装置において、

高い重要性度を有する符号化ビットのストリームを書き込み領域内の前記列のうち一番目の列から最後の列まで行方向に順次書き込む第1バッファと、前記相対的に低い重要性度を有する符号化ビットのストリームを書き込み領域内の前記列のうち一番目の列から最後の列まで行方向に順次書き込む第2バッファを含み、前記第1バッファ及び第2バッファ内の書き込み領域の前記列を所定の規則によって交換して再配列するインターリーバと、所定の変調方式によって決定された数だけのビットを前記第1バッファの書き込み領域及び前記第2バッファの書き込み領域から交代に読み出す動作において、前記それぞれの第1バッファの書き込み領域及び第2バッファの書き込み領域の行のうち一番目の行から最後の行まで列方向に順次読み出し、前記読み出された符号化ビ

ットを多重化するマルチプレクサと、を含むことを特徴とする装置。

【請求項92】 前記第1バッファの書き込み領域から読み出される符号化ビットをシンボルの第1信頼度を有する位置にマッピングし、前記第2バッファの書き込み領域から読み出される符号化ビットを前記第1信頼度より低い第2信頼度を有する位置にマッピングする変調部をさらに備えることを特徴とする請求項91記載の装置。

【請求項93】 前記符号化ビットを変調する方式が16QAMである場合、前記インターリーブ内に備わった前記第1バッファ及び前記第2バッファから読み出されるビットは2ビット単位で交代に読み出されることを特徴とする請求項91記載の装置。

【請求項94】 前記符号化ビットを変調する方式が64QAMである場合、前記インターリーブ内に備わった前記第1バッファ及び前記第2バッファから読み出されるビットは3ビット単位で交代に読み出されることを特徴とする請求項91記載の装置。

【請求項95】 前記符号化ビットを書き込んだ後、使用されなかった残りのバッファ領域に補助ビットを挿入することを特徴とする請求項91記載の装置。

【請求項96】 前記高い重要性を有する符号化ビットは、システマティックビットであることを特徴とする請求項91記載の装置。

【請求項97】 前記低い重要性を有する符号化ビットは、パリティビットであることを特徴とする請求項91記載の装置。

【請求項98】 前記高い重要性を有する符号化ビットと相対的に低い重要性を有する符号化ビットとの比率は、前記所定の符号化率によって決定されることを特徴とする請求項91記載の装置。

【請求項99】 前記第1バッファのサイズが前記高い重要性を有する符号化ビットの総量に対して足りない場合、前記インターリーブは、前記高い重要性を有する符号化ビットのうち前記第1バッファに書き込まれなかった符号化ビットを前記第2バッファの書き込み領域内の前記列のうち一番目の列から行方向に順次に書き込み、前記相対的に低い重要性を有する符号化ビットのストリームを前記第2バッファの書き込み領域内の残りの領域内に前記列のうち一番目の列から最後の列まで行方向に順次に書き込むことを特徴とする請求項91記載の装置。

【請求項100】 前記第1バッファの書き込み領域と前記第2バッファの書き込み領域は同一のサイズを有することを特徴とする請求項91記載の装置。

【請求項101】 複数の行及び列から構成されたビットを書き込む領域を有するバッファを備える移動通信システムの受信装置で、所定の復調方式によって復調された符号化ビットをデインターリーブする方法において、

前記符号化ビットを所定の周期で逆多重化する過程と、前記バッファを同一のサイズを有する第1書き込み領域と第2書き込み領域に分割する過程と、前記逆多重化された1つの出力を前記第1書き込み領域に順次に書き込み、前記逆多重化された他の出力を前記第2書き込み領域に順次に書き込む過程と、前記符号化ビットのうち高い重要性を有する符号化ビットと相対的に低い重要性を有する符号化ビットとの比率によって前記バッファを第1読み出し領域と第2読み出し領域に区分する過程と、前記高い重要性を有する符号化ビットと前記相対的に低い重要性を有する符号化ビットとの比率によって前記第1読み出し領域及び前記第2読み出し領域から符号化ビットを読み出す過程と、を含むことを特徴とする方法。

【請求項102】 複数の行及び列から構成されたビットを書き込む領域を有するバッファを備える移動通信システムの受信装置で、所定の復調方式によって復調された符号化ビットをデインターリーブする装置において、前記バッファの使用領域を同一のサイズを有する第1書き込み領域と第2書き込み領域に分割し、前記逆多重化された1つの出力を前記第1書き込み領域に順次に書き込み、前記逆多重化された他の出力を前記第2書き込み領域に順次に書き込み、前記使用領域を前記符号化ビットのうち高い重要性を有する符号化ビットと相対的に低い重要性を有する符号化ビットとの比率によって第1読み出し領域と第2読み出し領域に区分し、前記高い重要性を有する符号化ビットと前記相対的に低い重要性を有する符号化ビットとの比率によって前記第1読み出し領域及び前記第2読み出し領域から符号化ビットを読み出し、前記読み出された符号化ビットをデインターリーブするデインターリーブを含むことを特徴とする装置。

【請求項103】 前記復号化されたビットを所定の周期で逆多重化し、前記逆多重化されたビットを前記デインターリーブに提供するデマルチプレクサをさらに備えることを特徴とする請求項102記載の装置。

【発明の詳細な説明】

【0001】

【発明の属する技術分野】本発明は、符号分割多重接続移動通信システムにおけるデータ送／受信装置及び方法に関し、特に、伝送されるデータビットの信頼度を向上させるデータ送／受信装置及び方法に関する。

【0002】

【従来の技術】通信システムにおいて、送信された信号を歪みや雑音なしで受信することは現実的に不可能である。特に、無線ネットワークを通して信号を送信及び受信する移動通信システムは、有線ネットワークを通して信号を送信及び受信する通信システムに比べて、歪みや雑音の影響を受けやすい。

【0003】従って、歪みや雑音の影響を最小化するた

めに多様な技術が提案されてきた。その代表的な技術がエラーコントロールコーディング(error control coding)技法である。前記エラーコントロールコーディング技法のために使用されるコードは、メモリレス(memoryless)コードとメモリ(memory)コードに区分される。前記メモリレスコードとしては、線形ブロックコードがあり、前記メモリコードとしては、コンボリューション(Convolutional)コード及びターボ(Turbo)コードがある。このコードを生成する装置をチャネル符号器と称し、その出力は、使用するエラーコントロールコーディング技法によってシステマティック(systematic)ビットとパリティ(parity)ビットに区別される。前記システマティックビットとパリティビットに区別して出力するエラーコントロールコーディング技法に使用される代表的なコードはターボコードがある。勿論、前記ターボコード以外にもシステマティックビットとパリティビットを区別して出力する、コンボリューションコードの一種であるシステマティックコンボリューションコードがある。ここで、前記システマティックビットは、伝送しようとする実際の信号を意味し、前記パリティビットは、伝送時に発生したエラーを復号時に補正するために追加される信号である。しかしながら、エラーコントロールコーディングされた信号であっても、システマティックビットまたはパリティビットにバーストエラー(Burst Error)が発生すると、前記バーストエラーを補正することが容易でない。このような現象は、フェーディング(fading)チャネルを信号が通過する時によく発生し、この現象を防止するためには、インターリーブ(interleaving)技術が使用される。

【0004】前記インターリーブ技術は、損傷した部分を特定の位置に集中させずに多数の位置に分散させることによって、前記バーストエラーをより効率的に克服するために使用される。

【0005】前記インターリーブされた信号は、デジタル変調器(Digital Modulator)においてシンボル単位でマッピング(mapping)される。この時、前記変調器の次数(order)が増加すると、1つのシンボルに含まれるビット数も増加する。特に、16QAM以上の高い次数(high order)の変調方式である場合、1つのシンボルは4ビット以上の情報ビットを含み、前記情報ビットは、信頼度(reliability)によって分類されることができる。ここで、送信器によって1つのシンボルを変調する過程において、シンボルがX-Y軸上で左/右側または上/下側のように大きい(macro)領域で2ビット(bits)を表現する時、前記シンボルは“高い信頼度(high reliability)”を有し、小さい(micro)領域で2ビットを表現するシンボルは“低い信頼度(low reliability)”を有する。

【0006】図1は、高速ダウンリンクパケットアクセス(High Speed Downlink Packet Access: 以下、HSD

PAと称する)無線通信システムにおける送信器の構造を示す概略図である。図1に示すように、前記送信器は、チャネル符号器、インターリーバ(interleaver)、及び変調器から構成される。

【0007】図1を参照すると、CRC部(CRC generator)110においてエラー検出用のデータであるCRC(Cyclic Redundancy Check)ビットが追加された情報ビットは、チャネル符号化部(channel encoder)120に入力され、前記チャネル符号化部120は、前記CRCビットが追加された情報ビットを所定の符号化過程を通して符号化して符号化ビットを出力する。前記符号化ビットは、システマティックビットS及びパリティビットPである。前記チャネル符号化部120は、前記情報ビットを符号化するために少なくとも1つの符号化率を有する。前記符号化率は、 $1/2$ 、 $3/4$ などがある。さらに、前記チャネル符号器120が $1/3$ または $1/5$ の符号化率を有する母符号(mother code)に基づいてシンボル穿孔またはシンボル反復を通して複数の符号化率を支援する場合、支援する複数の符号化率から使用する特定の符号化率を選択する動作が必要になる。図1において、例えば、前記チャネル符号化部120が制御部160の制御下で前記符号化率を決定する。前記符号化ビットはレートマッチング部(Rate Matcher)130によってレートマッチングされる。通常的に、前記レートマッチングは、トランスポートチャネル(transport channel)がマルチプレキシング(multiplexing)されるか、前記符号化部120の出力シンボルが無線上で伝送されるシンボルの数と一致しない場合に、前記符号化ビットに対する反復(Repetition)及び穿孔(Puncturing)を通して遂行される。前記レートマッチング部130の穿孔または反復機能は、前記チャネル符号化部120の符号化率を調節するために遂行される穿孔または反復機能と同一であり、前記機能を統合することができる。つまり、前記チャネル符号化部120及び前記レートマッチング部130は、1つのブロックで表現されることができるが、図1においては、その機能を分離して表現する。前記レートマッチング部130によってレートマッチングされた符号化ビットは、インターリーバ(Interleaver)140によってインターリーブされる。前記インターリーブ動作は、伝送中にデータ損失が発生しても、データ損失を最小化する。前記インターリーブされた符号化ビットは、変調部(Modulator)150において、QPSK(Quadrature Phase shift Keying)、8PSK(8-ary Phase shift Keying)、16QAM、64QAMなどの変調方式によってシンボルマッピングされる。制御部160は、現在の無線チャネルの状態によって前記チャネル符号化部120の符号化動作及び前記変調部150の変調方式を制御する。前記HSDPA無線通信システムにおいて、無線環境によってQPSK、8PSK、16QAM、64QAMの変調方式のいずれか1つを選択

するためにAMCS(Adaptive Modulation and Coding Scheme)を前記制御部160に対して使用する。

【0008】図示されていないが、符号分割多重接続方式を使用する移动通信システムは、伝送するデータをウォルシュ符号W及び直交符号PNを使用して拡散することによって、対応する移動端末機(User Equipment: UE)が前記データを伝送するチャネル及び前記データを伝送する基地局(Node B)を区分することができる。

【0009】前述した送信器の構造において、前記チャネル符号化部120から出力されたシステムティックビット及びパリティビットは相違なる重要度(priority)を有する。言い換えると、伝送するデータに所定の比率でエラーが発生した場合、前記システムティックビットにエラーが発生する時に比べて、前記パリティビットにエラーが発生する時に、相対的に受信器においてより正確に復号(decoding)を遂行することができる。その理由は、前述したように、実質的なデータビットはシステムティックビットであり、パリティビットは、伝送中に発生したエラーを復号時に補正するために追加されるビットであるからである。前記理由によって、シンボルマッピング(SMP)技術が提案され、前記SMP技術は、本願出願人によって2001年4月4日付けに出願された大韓民国出願番号第2001-17925号に開示されている。

【0010】前記SMP技術は、前記パリティビットより高い重要度を有するシステムティックビットのエラー確率を低減することによってシステムの性能を向上させる。つまり、前記SMP技術は、前記変調器150において所定の変調方式によってシンボルマッピング時に、高い重要度を有するシステムティックビットはシンボルを構成するビットのうち高い信頼度を有するビットにマッピングされるようにし、相対的に低い重要度を有するパリティビットは低い信頼度を有するビットにマッピングされるようにする。従って、従来の移动通信システムの送信器において、重要度に関係なく符号化ビットをインターリーブするインターリーブ140に対する改善が必要になる。つまり、前記SMP技術を適用するためには、システムティックビットとパリティビットを区分してインターリーブすることができるように、前記インターリーブ140が改善されるべきである。

【0011】

【発明が解決しようとする課題】従って、本発明の目的は、前記SMP技術のためにインターリーブを具現することにおいて、複雑度を低減し、かつ、既存のアルゴリズムとの互換性の確保する方法を提供することにある。

【0012】本発明の他の目的は、重要度によって信頼度を差別マッピングするSMP技術を具現することによって無線通信システムの性能を向上させるデータ送/受信装置及び方法を提供することにある。

【0013】本発明のまた他の目的は、無線通信システ

ムにおいて、SMPを効果的に具現する方法を提供することにある。

【0014】本発明のまた他の目的は、無線通信システムのインターリーブのアルゴリズムを提供することにある。

【0015】本発明のまた他の目的は、無線移动通信システムにおいて、SMPを具現するための装置を提供することにある。

【0016】本発明のまた他の目的は、SMPの具現において、複雑度を低減する装置及び方法を提供することにある。

【0017】

【課題を解決するための手段】前記目的を達成するために、本発明は、既存のインターリーブ方法と比較して、複雑度の増加及びアルゴリズムの変化を最小化してSMPを具現する新しい方法を提示し、さらに、その方法が適用できる条件を提供することにある。

【0018】本発明の第1特徴によると、本発明は、複数の行及び列から構成されたビットを書き込む領域を有するバッファを備える移动通信システムの送信装置において、所定の符号化率によって符号化された符号化ビットをインターリーブする方法を提供する。前記方法は、前記符号化ビットのうち高い重要度を有する符号化ビットと相対的に低い重要度を有する符号化ビットとの比率によって、前記バッファの領域を第1書き込み領域と第2書き込み領域に区分する過程と、前記高い重要度を有する符号化ビットのストリームを前記第1書き込み領域内の前記列のうち一番目の列から最後の列まで行方向に順次に書き込み、前記相対的に低い重要度を有する符号化ビットのストリームを前記第2書き込み領域内の前記列のうち一番目の列から最後の列まで行方向に順次に書き込む過程と、前記バッファ領域の前記列を所定の規則によって交換して再配列する過程と、前記バッファ領域の前記行を同一のサイズを有する第1読み出し領域と第2読み出し領域に両分する過程と、所定の変調方式によって決定された数だけのビットを前記第1読み出し領域及び前記第2読み出し領域から交代に読み出す動作において、前記ビットを前記それぞれの第1読み出し領域及び第2読み出し領域の行のうち一番目の行から最後の行まで列方向に順次に読み出す過程と、から構成される。

【0019】本発明の第2特徴によると、本発明は、複数の行及び列から構成されたビットを書き込む領域を有するバッファを備える移动通信システムの送信装置において、所定の符号化率によって符号化された符号化ビットをインターリーブする方法を提供する。前記方法は、前記符号化ビットのうち高い重要度を有する符号化ビットと相対的に低い重要度を有する符号化ビットとの比率によって、前記バッファの領域を第1書き込み領域と第2書き込み領域に区分する過程と、前記高い重要度を有する符号化ビットのストリームを前記第1書き込み領域

内の前記列のうち一番目の列から最後の列まで行方向に順次書き込み、前記相対的に低い重要度を有する符号化ビットのストリームを前記第2書き込み領域内の前記列のうち一番目の列から最後の列まで行方向に順次書き込む過程と、前記バッファ領域の前記列を所定の規則によって交換して再配列する過程と、前記バッファ領域の前記行を同一のサイズを有する第1読み出し領域と第2読み出し領域に両分する過程と、前記それぞれの第1読み出し領域及び第2読み出し領域の行のうち所定の変調方式によって決定された数だけの行を、前記第1読み出し領域と第2読み出し領域との間に交換して再配列する過程と、前記第1読み出し領域及び第2読み出し領域から構成された前記全体バッファ領域の行を一番目の行から最後の行まで列方向に順次に読み出す過程と、から構成される。

【0020】本発明の第3特徴によると、本発明は、複数の行及び列から構成されたビットを書き込む領域を有するバッファを備える移動通信システムの送信装置において、所定の符号化率によって符号化された符号化ビットをインターリーブする方法を提供する。前記方法は、前記符号化ビットのうち高い重要度を有する符号化ビットと相対的に低い重要度を有する符号化ビットとの比率によって、前記バッファの領域を第1書き込み領域と第2書き込み領域に区分する過程と、前記高い重要度を有する符号化ビットのストリームを前記第1書き込み領域内の前記列のうち一番目の列から最後の列まで行方向に順次書き込み、前記相対的に低い重要度を有する符号化ビットのストリームを前記第2書き込み領域内の前記列のうち最後の列から一番目の列まで行方向に逆順に書き込む動作において、前記符号化ビットのストリームを前記第2書き込み領域内の最後の行から一番目の行まで逆方向に書き込む過程と、前記バッファ領域の前記列を所定の規則によって交換して再配列する過程と、前記バッファ領域の前記行を同一のサイズを有する第1読み出し領域と第2読み出し領域に両分する過程と、所定の変調方式によって決定された数だけのビットを前記第1読み出し領域及び前記第2読み出し領域から交代に読み出す動作において、前記ビットを前記それぞれの第1読み出し領域及び第2読み出し領域の行のうち一番目の行から最後の行まで列方向に順次に読み出す過程と、から構成される。

【0021】本発明の第4特徴によると、本発明は、複数の行及び列から構成されたビットを書き込む領域を有するバッファを備える移動通信システムの送信装置において、所定の符号化率によって符号化された符号化ビットをインターリーブする方法を提供する。前記方法は、前記符号化ビットのうち高い重要度を有する符号化ビットと相対的に低い重要度を有する符号化ビットとの比率によって、前記バッファの領域を第1書き込み領域と第2書き込み領域に区分する過程と、前記高い重要度を有

する符号化ビットのストリームを前記第1書き込み領域内の前記列のうち一番目の列から最後の列まで行方向に順次書き込み、前記相対的に低い重要度を有する符号化ビットのストリームを前記第2書き込み領域内の前記列のうち最後の列から一番目の列まで行方向に逆順に書き込む動作において、前記符号化ビットのストリームを前記第2書き込み領域内の最後の行から一番目の行まで逆方向に書き込む過程と、前記バッファ領域の前記列を所定の規則によって交換して再配列する過程と、前記バッファ領域の前記行を同一のサイズを有する第1読み出し領域と第2読み出し領域に両分する過程と、所定の変調方式によって決定された数だけのビットを前記第1読み出し領域及び前記第2読み出し領域から交代に読み出す動作において、前記ビットを前記それぞれの第1読み出し領域及び第2読み出し領域の行のうち一番目の行から最後の行まで列方向に順次に読み出す過程と、から構成される。

【0022】本発明の第5特徴によると、本発明は、それぞれ複数の行及び列から構成されたビットを書き込む領域を有する2つのバッファを備える移動通信システムの送信装置において、所定の符号化率によって符号化された符号化ビットをインターリーブする方法を提供する。前記方法は、前記符号化ビットのうち高い重要度を有する符号化ビットを第1バッファに書き込み、相対的に低い重要度を有する符号化ビットを第2バッファに書き込む動作において、前記高い重要度を有する符号化ビットのストリームを前記第1バッファの前記列のうち一番目の列から最後の列まで行方向に順次書き込み、前記相対的に低い重要度を有する符号化ビットのストリームを前記第2バッファの前記列のうち一番目の列から最後の列まで行方向に順次書き込む過程と、前記第1バッファ及び第2バッファの前記列を所定の規則によって交換して再配列する過程と、所定の変調方式によって決定された数だけのビットを前記第1バッファ及び前記第2バッファから交代に読み出す動作において、前記ビットを前記それぞれの第1バッファ及び第2バッファの行のうち一番目の行から最後の行まで列方向に順次に読み出す過程と、から構成される。

【0023】本発明の第6特徴によると、本発明は、伝送しようとするデータを所定の符号化率によって高い重要度を有する符号化ビット及び相対的に低い重要度を有する符号化ビットから構成された符号化ビットに符号化する符号化器、及び複数の行及び列から構成されたビットを書き込む領域を有するバッファを備える移動通信システムの送信装置において、所定の符号化率によって符号化された符号化ビットをインターリーブする装置を提供する。前記装置は、高い重要度を有する符号化ビットと相対的に低い重要度を有する符号化ビットとの比率によってその内部に備わったバッファの領域を第1書き込み領域と第2書き込み領域に区分し、前記高い重要度を

有する符号化ビットのストリームを前記第1書き込み領域内の前記列のうち一番目の列から最後の列まで行方向に順次書き込み、前記相対的に低い重要度を有する符号化ビットのストリームを前記第2書き込み領域内の前記列のうち一番目の列から最後の列まで行方向に順次書き込み、前記バッファ領域の前記列を所定の規則によって交換して再配列するインターリーブと、前記バッファ領域の前記列を同一のサイズを有する第1読み出し領域と第2読み出し領域に分割し、所定の変調方式によって決定された数だけのビットを前記第1読み出し領域及び前記第2読み出し領域から交代に読み出す動作において、前記ビットを前記それぞれの第1読み出し領域及び第2読み出し領域の行のうち一番目の行から最後の行まで列方向に順次読み出し、前記読み出された符号化ビットを多重化するマルチプレクサと、から構成される。

【0024】本発明の第7特徴によると、本発明は、伝送しようとするデータを所定の符号化率によって高い重要度を有する符号化ビット及び相対的に低い重要度を有する符号化ビットから構成された符号化ビットに符号化する符号化器、及び複数の行及び列から構成されたビットを書き込む領域を有するバッファを備える移動通信システムの送信装置において、所定の符号化率によって符号化された符号化ビットをインターリーブする装置を提供する。前記装置は、高い重要度を有する符号化ビットと相対的に低い重要度を有する符号化ビットとの比率によって前記バッファの領域を第1書き込み領域と第2書き込み領域に区分し、前記高い重要度を有する符号化ビットのストリームを前記第1書き込み領域内の前記列のうち一番目の列から最後の列まで行方向に順次書き込み、前記相対的に低い重要度を有する符号化ビットのストリームを前記第2書き込み領域内の前記列のうち一番目の列から最後の列まで行方向に順次書き込み、前記バッファ領域の前記列を所定の規則によって交換して再配列し、前記バッファ領域の前記行を同一のサイズを有する第1読み出し領域と第2読み出し領域に分割し、前記それぞれの第1読み出し領域及び第2読み出し領域の行のうち所定の変調方式によって決定された数だけの行を前記第1読み出し領域と第2読み出し領域との間に交換して再配列するインターリーブを含む。

【0025】本発明の第8特徴によると、本発明は、伝送しようとするデータを所定の符号化率によって高い重要度を有する符号化ビット及び相対的に低い重要度を有する符号化ビットから構成された符号化ビットに符号化する符号化器、及び複数の行及び列から構成されたビットを書き込む領域を有するバッファを備える移動通信システムの送信装置において、所定の符号化率によって符号化された符号化ビットをインターリーブする装置を提供する。前記装置は、高い重要度を有する符号化ビットと相対的に低い重要度を有する符号化ビットとの比率によって前記バッファの領域を第1書き込み領域と第2書

き込み領域に区分し、前記高い重要度を有する符号化ビットのストリームを前記第1書き込み領域内の前記列のうち一番目の列から最後の列まで行方向に順次書き込み、前記相対的に低い重要度を有する符号化ビットのストリームを前記第2書き込み領域内の前記列のうち最後の列から一番目の列まで行方向に書き込む時、前記符号化ビットのストリームを前記第2書き込み領域内の最後の行から一番目の行まで逆方向に書き込み、前記バッファ領域の前記列を所定の規則によって交換して再配列するインターリーブと、前記バッファ領域の前記行を同一のサイズを有する第1読み出し領域と第2読み出し領域に分割し、所定の変調方式によって決定された数だけのビットを前記第1読み出し領域及び前記第2読み出し領域から交代に読み出し、前記それぞれの第1読み出し領域及び第2読み出し領域の行のうち一番目の行から最後の行まで列方向に符号化ビットを順次読み出し、前記読み出された符号化ビットを多重化するマルチプレクサと、を含む。

【0026】本発明の第9特徴によると、本発明は、伝送しようとするデータを所定の符号化率によって高い重要度を有する符号化ビット及び相対的に低い重要度を有する符号化ビットから構成された符号化ビットに符号化する符号化器、及び複数の行及び列から構成されたビットを書き込む領域を有するバッファを備える移動通信システムの送信装置において、所定の符号化率によって符号化された符号化ビットをインターリーブする装置を提供する。前記装置は、高い重要度を有する符号化ビットと相対的に低い重要度を有する符号化ビットとの比率によって前記バッファの領域を第1書き込み領域と第2書き込み領域に区分し、前記高い重要度を有する符号化ビットのストリームを前記第1書き込み領域内の前記列のうち一番目の列から最後の列まで行方向に順次書き込み、前記相対的に低い重要度を有する符号化ビットのストリームを前記第2書き込み領域内の前記列のうち最後の列から一番目の列まで行方向に書き込む時、前記符号化ビットのストリームを前記第2書き込み領域内の最後の行から一番目の行まで逆方向に書き込み、前記バッファ領域の前記列を所定の規則によって交換して再配列し、前記バッファ領域の前記行を同一のサイズを有する第1読み出し領域及び第2読み出し領域に分割し、前記それぞれの第1読み出し領域及び第2読み出し領域の行のうち所定の変調方式によって決定された数だけの行を前記第1読み出し領域と第2読み出し領域との間に交換して再配列するインターリーブを含む。

【0027】本発明の第10特徴によると、本発明は、伝送しようとするデータを所定の符号化率によって高い重要度を有する符号化ビット及び相対的に低い重要度を有する符号化ビットから構成された符号化ビットに符号化する符号化器、及び複数の行及び列から構成されたビットを書き込む領域を有するバッファを備える移動通信

システムの送信装置において、所定の符号化率によって符号化された符号化ビットをインターリーブする装置を提供する。前記装置は、高い重要度を有する符号化ビットのストリームを書き込み領域内の前記列のうち一番目の列から最後の列まで行方向に順次に書き込む第1バッファと、前記相対的に低い重要度を有する符号化ビットのストリームを書き込み領域内の前記列のうち一番目の列から最後の列まで行方向に順次に書き込む第2バッファを含み、前記第1バッファ及び第2バッファ内の書き込み領域の前記列を所定の規則によって交換して再配列するインターリーブと、所定の変調方式によって決定された数だけのビットを前記第1バッファの書き込み領域及び前記第2バッファの書き込み領域から交代に読み出す動作において、前記それぞれの第1バッファの書き込み領域及び第2バッファの書き込み領域の行のうち一番目の行から最後の行まで列方向に順次に読み出し、前記読み出された符号化ビットを多重化するマルチプレクサと、を含む。

【0028】本発明の第1特徴によると、本発明は、複数の行及び列から構成されたビットを書き込む領域を有するバッファを備える移動通信システムの受信装置において、所定の復調方式によって復調された符号化ビットをデインターリーブする方法を提供する。前記方法は、前記符号化ビットを所定の周期で逆多重化する過程と、前記バッファを同一のサイズを有する第1書き込み領域と第2書き込み領域に分割する過程と、前記逆多重化された1つの出力を前記第1書き込み領域に順次に書き込み、前記逆多重化された他の出力を前記第2書き込み領域に順次に書き込む過程と、前記符号化ビットのうち高い重要度を有する符号化ビットと相対的に低い重要度を有する符号化ビットとの比率によって前記バッファを第1読み出し領域と第2読み出し領域に区分する過程と、前記高い重要度を有する符号化ビットと前記相対的に低い重要度を有する符号化ビットとの比率によって前記第1読み出し領域及び前記第2読み出し領域から符号化ビットを読み出す過程と、から構成される。

【0029】本発明の第2特徴によると、本発明は、複数の行及び列から構成されたビットを書き込む領域を有するバッファを備える移動通信システムの受信装置において、所定の復調方式によって復調された符号化ビットをデインターリーブする装置を提供する。前記装置は、前記バッファの使用領域を同一のサイズを有する第1書き込み領域と第2書き込み領域に分割し、前記逆多重化された1つの出力を前記第1書き込み領域に順次に書き込み、前記逆多重化された他の出力を前記第2書き込み領域に順次に書き込み、前記使用領域を前記符号化ビットのうち高い重要度を有する符号化ビットと相対的に低い重要度を有する符号化ビットとの比率によって第1読み出し領域と第2読み出し領域に区分し、前記高い重要度を有する符号化ビットと前記相対的に低い重要度を

を有する符号化ビットとの比率によって前記第1読み出し領域及び前記第2読み出し領域から符号化ビットを読み出し、前記読み出された符号化ビットをデインターリーブするデインターリーブを含む。

【0030】

【発明の実施の形態】以下、本発明に従う好適な実施形態について添付図を参照しつつ詳細に説明する。下記の説明において、本発明の要旨のみを明確にする目的で、関連した公知機能または構成に関する具体的な説明は省略する。

【0031】本発明は、SMP技術を適用するために要求されるインターリーブの具現例を提供する。通常的に、移動通信システムにおいて、それぞれシンボルにマッピングされるシステムティックビットの量(数)及びパリティビットの数は、符号化率及び変調方式によって異なる。従って、前記システムティックビット及びパリティビットの数を調節するためには、変調器の入力が前記条件によって適したパターンで形成されるべきである。つまり、前記SMP技術を適用するためのインターリーブは、システムティックビット及びパリティビットを区分してインターリーブを遂行することができるように、前記インターリーブが改善されるべきである。前記変調器の前段に位置するインターリーブを具現する方法は、与えられた条件によって様々な方法がある。

【0032】前記インターリーブを改善する方法は、前記インターリーブを物理的に区分する方法及び論理的に区分する方法に分けられる。前記物理的に区分する方法は、高い重要度を有する符号化ビットをインターリーブするためのインターリーブと低い重要度を有する符号化ビットをインターリーブするためのインターリーブを別に備える方法である。前記論理的に区分する方法は、1つのインターリーブ内の備わるバッファの貯蔵領域を高い重要度を有する符号化ビットを貯蔵するための領域及び低い重要度を有する符号化ビットを貯蔵するための領域に区分して使用する方法である。

【0033】1. 物理的に区分する方法

図2は、物理的に区分された2つのインターリーブを利用してSMP技術が適用された高速パケット伝送システムの構造を示す。図2に示す構造は、物理的に区分された2つのインターリーブを備え、前記システムティックビットS及び前記パリティビットPは別のインターリーブによって区別してインターリーブされる。このために、分配部(distributor)240、2つのインターリーブ250及び260、及び並列変換部(P/S変換部)270が要求される。

【0034】図2を参照すると、前記分配部240は、入力される符号化ビットを2つのインターリーブ250及び260に適切に分配する。例えば、前記分配部240は、前記符号化ビットのうち高い重要度を有するビットは第1インターリーブ250に分配し、前記高い重要

度を有するビットより低い重要度を有するビットは第2インターリーブ260に分配する。さらに、前記分配部240は、符号化のための符号化率が非対称である場合、前記符号化ビットの重要度及び符号化率によって前記符号化ビットを前記第1インターリーブ250及び前記第2インターリーブ260に均等に分配することができる。一方、前記第1インターリーブ250及び前記第2インターリーブ260は、前記分配部240から分配される符号化ビットをそれぞれインターリーブし、前記インターリーブされた符号化ビットを並列にP/S変換部270に出力する。前記P/S変換部270は、符号化率及び変調方式によって並列に入力される前記インターリーブされた符号化ビットに適したビットストリーム(stream)の形態を有する直列データに変換する。このために、前記P/S変換部270は、前記符号化率及び前記変調方式による制御器の制御によって変調周期で前記2つの入力を選択して直列化することができるべきである。

【0035】前記物理的に区分された2つのインターリーブを利用してSMP技術を適用した例を図3乃至図5に示す。

【0036】図3を参照すると、符号化率が1/2であり、2つのインターリーブ250及び260にシステムティックビットS及びパリティビットPが適切に分配された場合、変調部280によって、前記システムティックビットはそれぞれのシンボルの高い信頼度を有するH位置に、パリティビットは低い信頼度を有するL位置にマッピングされることができる。ここで、前記分配部240は、特別な役割を遂行せずに除去されることができ、P/S変換部270は単純なマルチプレクサ(MUX)の役割を遂行する。

【0037】図4を参照すると、符号化率が3/4であり、インターリーブ250及び260がシステムティックビット及びパリティビットを十分収容する場合、図3と関連して、前記変調部280の出力パターンは、最適の形態になることができる。同様に、図4の分配部240も特別な役割を遂行せずに除去されることができる。図4に示すように、64QAMの場合に2つのパターンが必要になるので、P/S変換部270は、変調率によってその動作を制御すべきである。例えば、初期シンボルのためには5ビットのシステムティックビット当わりに1ビットのパリティビットを出力し、次のシンボルのためには、4ビットのシステムティックビット当わりに2ビットのパリティビットを出力する。変調方式及び符号化率に適した動作のために、前記P/S変換部270が大事な役割をする。

【0038】図5を参照すると、第1バッファ250のサイズがシステムティックビットの総量より小さい場合、第2バッファ260は、超過した量のシステムティックビットを収容すべきである。出力パターンからみ

て、16QAMの場合、SMPの概念に違反する出力パターンは存在しない。しかしながら、64QAMの場合、一部のパターンは、システムティックビットがパリティビットより高い信頼度を有する位置にマッピングできるように形成される。その理由は、前記第2バッファ260の入力ビットがランダムにインターリーブされた後、前記P/S変換部270が前記第2バッファ260に貯蔵されたシステムティックビット及びパリティビットを区別することができないからである。

【0039】図3乃至図5から分かるように、バッファのサイズ(バッファサイズ=システムティックビットの数+パリティビットの数)が最小になる場合、64QAMのシンボルパターンが最適にマッピングされることができない。言い換えると、物理的にインターリーブングバッファを分離する場合、高次変調方式として64QAMの変調方式が適用されると、最適のマッピングパターンを生成するために、全ての符号化率のために2つのバッファのサイズを十分大きくする必要がある。しかしながら、16QAM以下の変調方式が適用される場合は、バッファのサイズを最小化しても、最適のマッピングパターンを生成することができる。

【0040】以下、本発明の目的は、16QAM以下の変調方式が使用される場合、バッファのサイズを図5に示すように最小化し、ハードウェア構成を最小にする方法を提供することにある。さらに、本発明は、追加的に既存のインターリーブングアルゴリズムである3GPP Release 99インターリーブング方式を修正する方法を提示する。

【0041】図6は、本発明の実施形態によって、物理的に分離されたインターリーブを使用するSMP技術を適用する方法を示すフローチャートである。以下、図6を参照して、物理的に分離されたインターリーブを使用するSMP技術を適用する方法を説明する。

【0042】図6を参照すると、インターリーブングのために、列間の交換(inter-column permutationまたはcolumn permutation)をするブロックインターリーブが使用される。前記インターリーブは、 $u_{p,1}, u_{p,2}, u_{p,3}, \dots, u_{p,U}$ を受信する(段階612)。ここで、pは、物理チャネル(physical channel)の数を示し、Uは、物理チャネルのフレーム当たりのビット数を示す。

【0043】(1) まず、列(column)の総数C2を30に割り当てる(段階614)。列の番号は、左から右側に0, 1, 2, ..., C2-1である。

【0044】(2) 条件 $U \leq R2 \times C2$ を満足する行列の行(row)を示す最小の整数R2を決定する。行列の行は、上から下に0, 1, 2, ..., R2-1に番号が割り当てられる(段階616)。

【0045】(3) 前記入力 $u_{p,1}, u_{p,2}, u_{p,3}, \dots, u_{p,U}$ を0行の0列の $y_{p,1}$ から始まっ

て $R2 \times C2$ 直角行列に＜数式1＞のように行単位 (row by row) で書き込む (段階618)。

$$\begin{bmatrix} y_{p,1} & y_{p,2} & y_{p,3} & \cdots & y_{p,C2} \\ y_{p,(C2+1)} & y_{p,(C2+2)} & y_{p,(C2+3)} & \cdots & y_{p,(2 \times C2)} \\ \vdots & \vdots & \vdots & \cdots & \vdots \\ y_{p,((R2-1) \times C2+1)} & y_{p,((R2-1) \times C2+2)} & y_{p,((R2-1) \times C2+3)} & \cdots & y_{p,(R2 \times C2)} \end{bmatrix}$$

【0047】ここで、 $k=1, 2, \dots, U$ のために、 $y_{p,k} = u_{p,k}$ である。 $R2 \times C2 > U$ である場合 (段階620)、 $k=U+1, U+2, \dots, R2 \times C2$ のために、 $y_{p,k} = 0$ または1の補助ビット (dummy bit) を挿入 (段階622) する。前記補助ビットは、列間の交換 (column permutation) (段階624) の後、除去 (段階6

【0046】

【数1】

26) される。

【0048】(4) 規則によって列間の交換 (column permutation) を遂行 (段階624) した後、その結果のビットは $y'_{p,k}$ によって＜数式2＞のように表現される。

【0049】

【数2】

$$\begin{bmatrix} y'_{p,1} & y'_{p,(R2+1)} & y'_{p,(2 \times R2+1)} & \cdots & y'_{p,((C2-1) \times R2+1)} \\ y'_{p,2} & y'_{p,(R2+2)} & y'_{p,(2 \times R2+2)} & \cdots & y'_{p,((C2-1) \times R2+2)} \\ \vdots & \vdots & \vdots & \cdots & \vdots \\ y'_{p,R2} & y'_{p,(2 \times R2)} & y'_{p,(3 \times R2)} & \cdots & y'_{p,(C2 \times R2)} \end{bmatrix}$$

【0050】(5) ブロックインターリーブの出力は、列間交換された $R2 \times C2$ 行列を列単位 (column by column) で読み出す (段階628)。前記出力は、 $v_{p,1}, v_{p,2}, v_{p,3}, \dots, v_{p,U}$ によって表現される。

【0051】しかしながら、通常のSMP技術において、2つのインターリーブが物理的に分離されているので、符号化率によって変動するシステムティックビット及びパリティビットを前記2つのインターリーブから適した量に分配するための分配部が要求される。分配器が存在しない場合、前記それぞれのインターリーブは、入力される全体の符号化ビットが貯蔵できるバッファを有するべきである。その理由は、複合再伝送技術を支援する高速パケット伝送システムにおいては、場合によって、再伝送時にシステムティックビットまたはパリティビットのみを伝送することができるからである。

【0052】一方、2つのインターリーブが物理的に分離されている場合、前記分離された2つのインターリーブのそれぞれの出力を1つのビットストリームに変換するためには、外部装置からの制御信号によって制御される直／並列変換部が必須的に要求される。

【0053】2. 論理的に区分する方法の第1実施形態以下、本発明によって提案しようとする1つのインターリーブ内に備わったバッファを論理的に区分することによってSMP技術を具現する第1実施形態を説明する。

【0054】2.1 第1実施形態による送信装置の構成

図7は、第1実施形態によって、1つのインターリーブ内に備わったバッファを論理的に区分することによってSMP技術を具現しようとする送信装置の構成を示す。

【0055】図7を参照すると、インターリーブ710

は、内部に所定の領域を有するバッファを備える。前記バッファの所定の領域は、符号化部 (図示せず) から入力される符号化ビットの総数によって決定される一部領域を意味する。以下、前記符号化ビットの総数によって決定される前記所定の領域を“使用領域”と称する。前記インターリーブ710は、前記決定された使用領域を前記符号化ビットを構成する第1重要度を有するビット (以下、システムティックビットと称する) と前記第1重要度より低い第2重要度を有するビット (以下、パリティビットと称する) との比率によって2つの書き込み領域 (第1書き込み領域及び第2書き込み領域) に区分する。ここで、前記システムティックビットと前記パリティビットとの比率は、前記符号化部が使用する符号化率によって決定される。例えば、前記符号化率が $1/2$ である場合、前記使用領域は、同一のサイズを有する2つの書き込み領域に等分され、1つの書き込み領域は、第1書き込み領域として定義され、他の1つの書き込み領域は、第2書き込み領域として定義される。図8A及び図8Bは、前記第1書き込み領域及び前記第2書き込み領域のサイズが同一であるインターリーブ710の例を示す。しかしながら、前記符号化率が $3/4$ である場合、前記使用領域は、同一のサイズを有する4つの領域に等分され、前記4つの領域のうち3つの領域は、第1書き込み領域として定義され、残りの1つの領域は、第2書き込み領域として定義される。図9A及び図9Bは、前記第1書き込み領域及び前記第2書き込み領域が非対称に区分されるインターリーブ710の例を示す。図7において、前記符号化率が $1/2$ である場合、前記インターリーブ710が使用領域を第1書き込み領域と前記第2書き込み領域に区分されていることを仮定している。

【0056】前記インターリーブ710は、前記符号化部から符号化ビットを受信すると、前記符号化ビットのうち前記システムティックビットを前記第1書き込み領域に順次に書き込み、前記パリティビットを前記第2書き込み領域に順次に書き込む。ここで、前記インターリーブ710は、前記第1書き込み領域中で前記システムティックビットが書き込まれた後の残りの領域、及び前記第2書き込み領域の中で前記パリティビットが書き込まれた後の残りの領域に補助ビット(dummy bits)を挿入する。前記システムティックビットを前記第1書き込み領域に順次に書き込む例と前記パリティビットを前記第2書き込み領域に順次に書き込む例を、図8A乃至図10Dに示す。

【0057】前記インターリーブ710は、前述した動作によって前記システムティックビット及び前記パリティビットの書き込みが完了すると、前記使用領域内の貯蔵された補助ビット含む符号化ビットを列交換(column permutation)を通してインターリーブする。前記列交換は、前記使用領域内の符号化ビットを列単位(column by column)で列交換することによって、書き込まれたシステムティックビットとパリティビットがミックス(mix)されないようになる。

【0058】さらに、前記インターリーブ710は、前記書き込まれた符号化ビットを読み出すために、前記使用領域を同一のサイズの第1読み出し領域と第2読み出し領域に分割する。従って、前記符号化率が1/2である場合、前記第1読み出し領域は前記第1書き込み領域と同一であり、前記第2読み出し領域は前記第2書き込み領域と同一である。従って、前記第1読み出し領域には前記システムティックビットのみが予め書き込まれており、前記第2読み出し領域には前記パリティビットのみが予め書き込まれている。しかしながら、前記符号化率が3/4である場合、前記第1書き込み領域は、前記第1読み出し領域及び前記第2読み出し領域の一部を含み、前記第2読み出し領域の残りの部分は、前記第2書き込み領域になる。従って、前記第1読み出し領域には、前記システムティックビットのみが予め書き込まれており、前記第2読み出し領域には前記システムティックビット及び前記パリティビットが行単位(row by row)で予め書き込まれている。

【0059】前記インターリーブ710は、前記インターリーブの後、前記第1読み出し領域及び前記第2読み出し領域に書き込まれた符号化ビットを順次に読み出す。図11A及び図11Bには、前記第1読み出し領域及び前記第2読み出し領域から符号化ビットを読み出す例を示す。ここでは、インターリーブのための列交換動作及び読み出し動作を区分して説明する。しかしながら、前記読み出しの順序を交換することによって、前記列交換動作及び前記読み出し動作を1つの動作として具現できることは自明である。

【0060】前記インターリーブ710の前記第1読み出し領域及び前記第2読み出し領域から読み出した符号化ビットは、マルチプレクサ(multiplexer: MUX)720に提供される。前記MUX720は、前記第1読み出し領域及び前記第2読み出し領域からの符号化ビットを所定の比率で多重化し、1つのビットストリームを出力する。前記第1読み出し領域からの符号化ビット及び前記第2読み出し領域からの符号化ビットを多重化する比率は、変調器730によって使用される変調方式によって決定される。例えば、前記変調方式が16QAMである場合、4つの符号化ビットが1つのシンボルにマッピングされる。この場合、前記MUX720は、前記第1読み出し領域からの2ビットの符号化ビット及び前記第2読み出し領域からの2ビットの符号化ビットをそれぞれのシンボルに対して多重化する。

【0061】前記MUX720によって多重化された符号化ビットは、前記変調器730に入力される。前記変調器730は、前記多重化された符号化ビットに対してシンボルマッピングを遂行する。例えば、変調方式として16QAMを使用する場合、前記変調器730は、前記第1読み出し領域に書き込まれていた2ビットの符号化ビットを特定のシンボルの高い信頼度(以下、第1信頼度と称する)を有するビットにマッピングする。さらに、前記変調器730は、前記第2読み出し領域に書き込まれていた2ビットの符号化ビットを前記シンボルの低い信頼度(以下、第2信頼度と称する)を有するビットにマッピングする。

【0062】前述したように、本発明は、1つのインターリーブを論理的に区分することによってシステムティックビット及びパリティビットをインターリーブする方法を提供することで、前記変調器がSMP技術によるシンボルマッピングを遂行することを可能にする。

【0063】2.2 符号化ビットの書き込み

本発明の実施形態によってインターリーブ710内に備わったバッファに符号化ビットを書き込む方法は、補助ビット(dummy bits)が使用される場合及び前記補助ビットが使用されない場合に区分されることができる。前記補助ビットは、符号化部から入力される符号化ビットの総数によって決定される前記バッファの使用領域に前記符号化ビットを書き込んだ後、残りの領域を充填するために使用されるビットである。前記補助ビットは、インターリーブのための列間の交換が遂行された後、除去される。

【0064】前記符号化ビットを書き込む方法を説明する前に、前記補助ビットが使用されるか否かを決定する方法に関して説明する。前記補助ビットが使用されるか否かは、符号化部から入力される符号化ビットの総数Uが前記使用領域のバッファ行列を構成する列(column)の総数C2の整数倍であるか否かによって決定される。ここで、前記C2は、前記インターリーブ内のバッファの

サイズによって予め決定されることができる。さらに、前記使用領域を決定するために使用される行(row)の総数 $R/2$ は、前記 $C/2$ が予め決定されているので、前記符号化ビットの総数 U によって決定されることができる。従って、前記使用領域は、前記 $C/2$ と前記 $R/2$ の積($C/2 \times R/2$)によって決定される。さらに、前記補助ビットが使用されるか否かは、前記 $C/2$ と前記 $R/2$ との積と前記 U を比較することによって判断できる。例えば、前記 U が前記 $C/2$ の整数倍($R/2$)であることによって、 $U = C/2 \times R/2$ の条件を満足すると、補助ビットは使用されない。しかしながら、前記 U が前記 $C/2$ の整数倍($R/2$)でないことによって、 $U < C/2 \times R/2$ の条件を満足すると、前記補助ビットが使用される。

【0065】2. 2. 1 補助ビットを使用しない場合
図8A、図8B、図9A及び図9Bを参照して、前記補助ビットを使用しない場合に符号化ビットをインターリーブ710に書き込む例を説明する。特に、図8A及び図8Bは、前記符号化部によって使用される符号化率が $1/2$ であるケースを示し、図9A及び図9Bは、前記符号化部によって使用される符号化率が $3/4$ であるケースを示す。

【0066】まず、前記符号化部の符号化率が $1/2$ であることによって、システムティックビット及びパリティビットが同一の比率で入力されるケースを説明する。図8Aは、符号化率が $1/2$ である場合、前記パリティビットを前記使用領域の後端から書き込む方法を示し、図8Bは、符号化率が $1/2$ である場合、前記パリティビットを前記使用領域の第2書き込み領域の前部から書き込む方法を示す。

【0067】図8Aを参照すると、前記符号化部から入力される符号化ビットの総数 U によって、前記インターリーブ710内に備わるバッファの全体領域の一部の使用領域が決定される。前記使用領域の決定は、前記 U を前記定義された $C/2$ によって割った余りが存在しない場合、前記割り算によって得られた分け前を行の総数($R/2$)として決定する。しかしながら、前記余りが存在する場合は、前記分け前に1を加算して $R/2$ を決定する。前記使用領域は、図8Aに示す第1書き込み領域及び第2書き込み領域の和として決定されることができ、前記第1書き込み領域及び前記第2書き込み領域は、前記使用領域を同一のサイズに両分することによって決定される。図8Aに示す書き込み方法を使用する場合、前記第1書き込み領域及び前記第2書き込み領域を物理的に明確に区分する必要はない。その理由は、前記符号化ビットのうちシステムティックビットは前記使用領域の前部から書き込まれ(図8Aにおいて黒い矢印で表示する)、前記符号化ビットのうちパリティビットは、前記使用領域の後端から書き込まれる(図8Aにおいて白い矢印で表示する)からである。言い換えると、前記システムティックビットは、前記使用領域の(0,0)から順方向に

進行書き込まれ、前記パリティビットは、前記使用領域の($R/2-1, C/2-1$)から逆方向に書き込まれる。ここで、 $C/2$ は、前記使用領域内のバッファ行列を構成する列(column)の総数であり、 $R/2$ は、前記使用領域内のバッファ行列を構成する行(row)の総数である。従って、前記符号化ビットが前記使用領域に完全に書き込まれると、前記第1書き込み領域及び前記第2書き込み領域は、書き込まれた符号化ビットによって自然に区分される。

【0068】図8Bを参照すると、前記符号化部から入力される符号化ビットの総数 U によって、インターリーブ710内に備わるバッファの全体領域の一部の使用領域が決定される。前記使用領域は、図8Bに示す第1書き込み領域と第2書き込み領域の和として決定されることができ、前記第1書き込み領域及び前記第2書き込み領域は、前記使用領域を同一のサイズに両分することによって決定される。前記第1書き込み領域及び前記第2書き込み領域が決定された後、前記符号化ビットのうちシステムティックビットは、前記第1書き込み領域の前部から書き込まれ(図8Bにおいて黒い矢印で表示する)、前記符号化ビットのうちパリティビットは、前記第2書き込み領域の前部から書き込まれる(図8Bにおいて白い矢印で表示する)。言い換えると、前記システムティックビットは、前記使用領域の(0,0)から順方向に書き込まれ、前記パリティビットは、前記使用領域の(y, z)から順方向に書き込まれる。ここで、符号化率が $1/2$ であるので、 y は $R/2/2$ になり、 z は0になる。

【0069】次に、前記符号化部の符号化率が $3/4$ であることによって、システムティックビットとパリティビットが $3:1$ の比率で入力されるケースを説明する。図9Aは、符号化率が $3/4$ である場合、前記パリティビットを前記使用領域の後端から書き込む方法を示し、図9Bは、符号化率が $3/4$ である場合、前記パリティビットを前記使用領域の前部から書き込む方法を示す。

【0070】図9Aを参照すると、前記符号化部から入力される符号化ビットの総数 U によって、インターリーブ710内に備わるバッファの全体領域の一部の使用領域が決定される。前記使用領域の決定は、前記 U を前記定義された $C/2$ で割ることによって得られた分け前を $R/2$ として決定する。前記使用領域は、図9Aに示す第1書き込み領域と第2書き込み領域の和として決定されることができる。図9Aの書き込み方法を使用する場合、前記第1書き込み領域及び前記第2書き込み領域を物理的に明確に区分する必要はない。その理由は、前記符号化ビットのうちシステムティックビットは、前記使用領域の前部から書き込まれ(図9Aにおいて黒い矢印で表示する)、前記符号化ビットのうちパリティビットは、前記使用領域の後端から書き込まれる(図9Aにおいて白い矢印で表示する)からである。言い換えると、前記

システムティックビットは、前記使用領域の(0,0)から順方向に書き込まれ、前記パリティビットは、(R2-1, C2-1)から逆方向に書き込まれる。従って、前記使用領域に書き込まれた前記システムティックビット及び前記パリティビットは、前記第1書き込み領域と前記第2書き込み領域との間の境界地点(y, z)によって区分される。前記(y, z)は、前記第1書き込み領域と前記第2書き込み領域との間の境界地点であり、前記使用領域の特定地点を指定する座標である。前記システムティックビットの総数を前記C2で割った分け前または余りが存在する場合、前記yは、前記分け前に1を加算した値であり、前記zは、その余りである。従って、前記第1書き込み領域は、前記使用領域の(0,0)から(y, z)までの領域として定義されることができ、前記第2書き込み領域は、前記使用領域の(y, z)から(R2-1, C2-1)までの領域として定義されることができ

【0071】図9Bを参照すると、前記符号化部から入力される符号化ビットの総数Uによって、インターリーブ710内に備わるバッファの全体領域の一部の使用領域が決定される。前記使用領域は、図9Bに示す第1書き込み領域と第2書き込み領域との和として決定されることができ。前記第1書き込み領域及び前記第2書き込み領域が決定された後、前記符号化ビットのうちシステムティックビットは、前記第1書き込み領域の前部から書き込まれ(図9Bにおいて黒い矢印で表示する)、前記符号化ビットのうちパリティビットは、前記第2書き込み領域の前部、つまり、(y, z)から書き込まれる(図9Bにおいて白い矢印で表示する)。言い換えると、前記システムティックビットは、前記使用領域の(0,0)から順方向に書き込まれ、前記パリティビットは、前記使用領域の(y, z)から順方向に書き込まれる。前述したように、前記(y, z)において、システムティックビットの総数を前記C2で割って得られた分け前または余りが存在する場合、前記yは、前記分け前に1を加算した値であり、前記zは、余りである。

【0072】2.2.2 補助ビット(dummy bit)を使用する場合

以下、補助ビット(dummy bit)を使用して符号化ビットを書き込む方法を、符号化率が3/4である場合に限定して説明しているが、1/2の符号化率にも同一適用されることができるとは自明である。

【0073】前記定義されたように、前記補助ビットは、前記使用領域に前記システムティックビット及び前記パリティビットを書き込んだ後でも、使用されなかった空きの領域が存在する時に使用される。つまり、前記補助ビットは、前記Uが前記C2の整数倍でない場合に使用される。前記補助ビットが挿入される場合、補助ビットを挿入する方法は、前記使用領域の位置によって異なる具現例が提案されることができ。図10A乃至図

10Dは、前記補助ビットの位置によって符号ビットを書き込む方法を示す。前記補助ビットの位置は、前記パリティビットを第2書き込み領域に書き込む方向及び前記パリティビットの書き込み開始点によって決定されることができる。

【0074】図10Aは、前記パリティビットを逆方向に書き込み、前記第2書き込み領域の端から前記補助ビットの分だけ移動した地点を開始点と定義する場合において、符号化ビットを書き込む方法を示す。図10Bは、前記パリティビットを順方向に書き込み、前記第2書き込み領域の前部を開始点として定義する場合、符号化ビットを書き込む方法を示す。図10Cは、前記パリティビットを逆方向に書き込み、前記第2書き込み領域の端を開始点として定義する場合に、符号化ビットを書き込む方法を示す。図10Dは、前記パリティビットを順方向に書き込み、前記第2書き込み領域の前部から前記補助ビットの分だけ移動した地点を開始点として定義する場合に、符号化ビットを書き込む方法を示す。

【0075】図10Aを参照すると、前記符号化部から入力される符号化ビットの総数Uによってインターリーブ710内に備わるバッファの全体領域の一部である使用領域が決定される。前記使用領域は、図10Aに示す第1書き込み領域及び第2書き込み領域の和として定義されることができ。図10Aにおいては、前記補助ビットが前記第2書き込み領域の後端に位置する場合、前記第1書き込み領域及び前記第2書き込み領域を物理的に明確に区分する必要はない。その理由は、前記符号化ビットのうちシステムティックビットは、前記使用領域の前部から書き込まれ(図10Aにおいて黒い矢印で表示する)、前記符号化ビットのうちパリティビットは、前記使用領域の後端から書き込まれる(図10Aにおいて白い矢印で表示する)からである。言い換えると、前記システムティックビットは、前記使用領域の(0,0)から順方向に書き込まれ、前記パリティビットは、(R2-1, x)から逆方向に書き込まれる。前記xは、C2-1に対応する列から前記補助ビットの数だけ減算することによって計算されることができ。従って、前述したように、前記使用領域に書き込まれた前記システムティックビット及び前記パリティビットは、前記第1書き込み領域と前記第2書き込み領域との間の境界地点(y, z)によって区分される。

【0076】図10Bを参照すると、前記システムティックビットは、前述した方法と同一の方法によって書き込まれる。しかしながら、前記パリティビットは、前記第1書き込み領域と前記第2書き込み領域との間の境界(y, z)から始まって順方向に書き込まれる。ここで、前記(y, z)は、挿入される補助ビットを考慮して新しく定義されることができ。前記パリティビットの書き込みが完了すると、前記第2書き込み領域の後端に存在する残りの領域に前記補助ビットを挿入する。

【0077】図10Cを参照すると、前記システムティックビットは、前記第1領域の前部から順方向に書き込まれ、前記パリティビットは、前記第2書き込み領域の端から逆方向に書き込まれる。従って、前記システムティックビットが書き込まれた後の残りの領域及び前記パリティビットが書き込まれた後の残りの領域に補助ビットが挿入される。

【0078】図10Dを参照すると、前記システムティックビットは、前記第1書き込み領域の前部から順方向に書き込まれ、前記パリティビットは、予想される前記システムティックビットの書き込みが完了する地点と、前記補助ビットが挿入される地点との間の領域の後端から順方向に書き込まれる。従って、前記補助ビットは、前記第1書き込み領域の一部及び前記第2書き込み領域の一部において挿入される。

【0079】2.3 符号化ビットの読み出し
前記符号化ビットが書き込まれたインターリーブ710内のバッファの使用領域は、読み出しのために2つの仮想的な読み出し領域に区分される。前記2つの読み出し領域は、前記使用領域を同一のサイズを有する2つの領域に両分することによって区分されることができる。前記インターリーブ710は、前記区分された第1読み出し領域及び第2読み出し領域に書き込まれた符号化ビットを読み出す。

【0080】図11A及び図11Bは、前記インターリーブ710が前記第1読み出し領域及び前記第2読み出し領域から符号化ビットを読み出す方法の例を示す。特に、図11Aは、1/2の符号化率で書き込まれた符号化ビットを読み出す方法を示し、図11Bは、3/4の符号化率で書き込まれた符号化ビットを読み出す方法を示す。

【0081】図11A及び図11Bを参照すると、前記インターリーブ710は、前記第1読み出し領域に書き込まれた符号化ビットを列単位で順次に読み出す。さらに、前記インターリーブ710は、前記第2読み出し領域に書き込まれた符号化ビットも列単位で順次に読み出す。その結果として、図11Aにおいて、前記第1読み出し領域からはシステムティックビットのみが読み出され、前記第2読み出し領域からはパリティビットのみが読み出される。しかしながら、図11Bにおいては、前記第1読み出し領域からはシステムティックビットのみが

読み出され、前記第2読み出し領域からはパリティビット及びシステムティックビットが読み出される。

【0082】2.4 第1実施形態による送信装置の動作

図12は、本発明の第1実施形態によるインターリーブ過程を示すフローチャートである。つまり、図12は、システムティックビット及びパリティビットを区分して書き込み及び読み出しを遂行する変更されたアルゴリズムを示す。ここでは、理解を容易にするために、書き込み動作が図10Aにおいて提案された方式によって遂行されると仮定する。

【0083】図12を参照すると、インターリーブは、U個の符号化ビットを符号化部から受信する(段階1200)。前記符号化ビットは、 $u_{p,1}$ 、 $u_{p,2}$ 、 $u_{p,3}$ 、 $\dots$ 、 $u_{p,U}$ 及び $u_{p,U+1}$ 、 $u_{p,U+2}$ 、 $u_{p,U+3}$ 、 $\dots$ 、 $u_{p,U+U}$ で表現される。ここで、前記pは、物理チャネル番号であり、前記U_s及び前記U_pは、それぞれシステムティックビット及びパリティビットの数を示す。前記U_s及び前記U_pの和は、1つの物理チャネルのフレーム当たりのビット数である。

【0084】(1)まず、列(column)の総数C2を30に設定する。列の番号は、左側から右側に0、1、2、 $\dots$ 、C2-1である。U=U_s+U_p≤R2×C2の条件を満足する行列の行(row)を示す最小整数R2を決定する(段階1202)。行列の行は、上から下に0、1、2、 $\dots$ 、R2-1のように番号が割り当てられる(段階1204)。

【0085】(2)入力 $u_{p,1}$ 、 $u_{p,2}$ 、 $u_{p,3}$ 、 $\dots$ 、 $u_{p,U}$ は、0番目の行及び0番目の列の $y_{p,1}$ から始まって、R2×C2直角行列において行単位(row by row)で書き込まれ、 $u_{p,U+1}$ 、 $u_{p,U+2}$ 、 $u_{p,U+3}$ 、 $\dots$ 、 $u_{p,U+U}$ は、R2-1番目の行及びx-1番目の列の地点から行単位で逆方向に書き込まれる(段階1206)。ここで、xは、UをC2で割った余りを意味し、1より大きい、それとも同一であり、C2より小さい($1 \leq x < C2$)。＜数式3＞は、こういうふう生成された行列の例を示す。

【0086】

【数3】

$$\begin{bmatrix} y_{p,1} & y_{p,2} & y_{p,3} & \dots & y_{p,C2} \\ y_{p,(C2+1)} & y_{p,(C2+2)} & y_{p,(C2+3)} & \dots & y_{p,(2 \times C2)} \\ \vdots & \vdots & \vdots & \dots & \vdots \\ y_{p,((R2-1) \times C2+1)} & y_{p,((R2-1) \times C2+2)} & y_{p,((R2-1) \times C2+3)} & \dots & y_{p,(R2 \times C2)} \end{bmatrix}$$

【0087】ここで、k=1、2、 $\dots$ 、Uである場合、 $y_{p,k} = u_{p,k}$ である。R2×C2>Uであると(段階1208)、k=U+1、U+2、 $\dots$ 、R2×C2の

ために、 $y_{p,k} = 0$ または1の補助ビット(dummy bit)を挿入する(段階1210)。前記補助ビットは、列間の交換(段階1212)の後、除去される(段階121

4)。

【0088】(3)規則によって、列間の交換(column permutation)を遂行した後(段階1212)、その結果のビットは、高信頼度を有するH部分及び低い信頼度を有するL部分に分けられ、

【0089】

【数4】

$$y_{p,k}^H$$

$$\begin{bmatrix} y_{p,1}^H & y_{p,(R2/2+1)}^H & y_{p,R2+1}^H & \cdots & y_{p,((C2-1) \times R2/2+1)}^H \\ y_{p,2}^H & y_{p,(R2/2+2)}^H & y_{p,R2+2}^H & \cdots & y_{p,((C2-1) \times R2/2+2)}^H \\ \vdots & \vdots & \vdots & \cdots & \vdots \\ y_{p,R2/2}^H & y_{p,R2}^H & y_{p,3 \times R2/2}^H & \cdots & y_{p,(C2 \times R2/2)}^H \\ y_{p,1}^L & y_{p,(R2/2+1)}^L & y_{p,R2+1}^L & \cdots & y_{p,((C2-1) \times R2/2+1)}^L \\ y_{p,2}^L & y_{p,(R2/2+2)}^L & y_{p,R2+2}^L & \cdots & y_{p,((C2-1) \times R2/2+2)}^L \\ \vdots & \vdots & \vdots & \cdots & \vdots \\ y_{p,R2/2}^L & y_{p,R2}^L & y_{p,3 \times R2/2}^L & \cdots & y_{p,(C2 \times R2/2)}^L \end{bmatrix}$$

【0092】(4)ブロックインターリーブの出力は、列間交換された $R2 \times C2$ 行列を高い信頼度を有する部分及び低い信頼度を有する部分に等分することによって、列単位で2ビットずつ読み取られる(段階1216)。前記出力は、 $v_{p,1}, v_{p,2}, v_{p,3}, \dots, v_{p,U_S}$ のように表現される。

【0093】3. 論理的に区分する方法の第2実施形態
図13は、本発明の第2実施形態によって、1つのインターリーブ内に備わったバッファを論理的に区分することによってSMP技術を具現する送信装置の構成を示す。

【0094】図13を参照すると、インターリーブ1310は、内部に所定の領域を有するバッファを備える。前記バッファの所定の領域は、符号化部(図示せず)から入力される符号化ビットの総数によって決定される使用領域を定義する。前記インターリーブ1310は、前記使用領域を前記符号化ビットを構成するシステムティックビットとパリティビットとの比率によって第1書き込み領域と第2書き込み領域に区分する。ここで、前記システムティックビットと前記パリティビットとの比率は、前記符号化部によって使用される符号化率によって決定される。図13においては、前記インターリーブ1310が符号化率 $1/2$ を支援すると仮定する。

【0095】前記インターリーブ1310は、前記符号化部から符号化ビットを受信すると、前記符号化ビットのうち前記システムティックビットを前記第1書き込み領域に順次に書き込み、前記パリティビットを前記第2書き込み領域に順次に書き込む。ここで、前記インターリーブ1310は、前記第1書き込み領域に前記システムティックビットを書き込んだ後の残りの領域、及び前

及び

【0090】

【数5】

$$y_{p,k}^L$$

によって<数式6>のように表現される。

【0091】

【数6】

記第2書き込み領域のうち前記パリティビットを書き込んだ後の残りの領域に補助ビット(dummy bits)を挿入する。

【0096】前記インターリーブ1310は、前述した動作によって前記システムティックビット及び前記パリティビットの書き込みが完了すると、前記使用領域内に貯蔵された補助ビットを含む符号化ビットを列交換(column permutation)によってインターリーブする。前記列交換は、前記使用領域内の符号化ビットを列(column)単位で交換することによって、前記書き込まれたシステムティックビットとパリティビットが混合されないようにする。前記インターリーブ1310は、前記列交換の後、前記第1書き込み領域を構成する行のうち下側の半分の列と前記第2書き込み領域を構成する行のうち上側の半分の列を交換する。その結果、前記第1書き込み領域及び前記第2書き込み領域に書き込まれた符号化ビットをSMP技術によってビットストリームの形態で適切に読み出すことができる。前記行間の交換(または、行交換)の例を図14A及び図14Bに示す。特に、図14Aは、 $1/2$ の符号化率を使用する場合の行交換の例を示し、図14Bは、 $3/4$ の符号化率を使用する場合の行交換の例を示す。

【0097】一方、前記インターリーブ1310は、前記書き込まれた符号化ビットを順次に読み出す。前記インターリーブ1310によって前記符号化ビットを読み出す例は、図15A及び図15Bに示す。特に、図15Aは、 $1/2$ の符号化率を使用する場合の読み出しの例を示し、図15Bは、 $3/4$ の符号化率を使用する場合の読み出しの例を示す。

【0098】ここで、インターリーブのための列交

換動作及び読み出し動作を区分して説明する。しかしながら、前記読み出しの順序を変更することによって前記列交換動作及び前記読み出し動作を1つの動作として具現することができる。

【0099】前記インターリーブ1310によって前記読み出された符号化ビットは、SMP技術を適用するために要求される形態を有する。従って、前記インターリーブ1310から出力される符号化ビットは、変調器1320に提供されて、SMP技術によってシンボルマッピングされる。

【0100】前述したように、本発明は、システムティックビット及びパリティビットを1つのインターリーブによって論理的に区分してインターリーブすることによって、変調器がSMP技術によるシンボルマッピングを遂行することを可能にする。さらに、第1実施形態において使用されたMUXを除去するために、Re199の読み出しアルゴリズムを変更する必要がある。つまり、2つの書き込み領域に書き込まれた符号化ビットを2ビットずつ読み出すように前記アルゴリズムを変更する場合、前記MUXが除去される。言い換えると、論理的に区分されたインターリーブバッファの場合、前述したように簡単な読み出しアルゴリズムの修正によってMUXのハードウェア装置を除去することができる。以下の本発明のアルゴリズムには、前記読み出しアルゴリズムの修正が含まれる。さらに、バッファ行列のR2が4の倍数である場合、前記MUXを使用せずに行交換(row permutation)を通して前記全体のバッファを読み出す既存の読み出しアルゴリズムで具現することができる。

【0101】図15A及び図15Bは、符号化率がそれぞれ1/2及び3/4である場合に、前記行交換(row permutation)方式が提供された変調器のシンボルパターンを示す。図15A及び図15Bを参照すると、両方とも重要度によって信頼度を差別して割り当てるSMP技

術の思想を違反していない。拡張された実際のデータ量を適用する場合、第1実施形態による結果と同一の結果を得ることができる。

【0102】図16は、本発明の第2実施形態によるインターリーブ過程を示すフローチャートである。図16を参照すると、インターリーブのために列交換(column permutation)の機能を有するブロックインターリーブが使用される。前記インターリーブは、

$u_{p,1}$ 、 $u_{p,2}$ 、 $u_{p,3}$ 、 $\dots$ 、 u_{p,U_s} 及び u_{p,U_s+1} 、 u_{p,U_s+2} 、 u_{p,U_s+3} 、 $\dots$ 、 u_{p,U_s+U_p} を受信する(段階1600)。ここで、 p は、物理チャネルの番号であり、 U_s 及び U_p は、それぞれシステムティックビット及びパリティビットの数を示す。前記 U_s と前記 U_p の和は、1つの物理チャネルのフレーム当たりのビット数である。

【0103】(1)まず、列の総数C2を30に設定する。列の番号は、左側から右側に0、1、2、 $\dots$ 、C2-1である。 $U=U_s+U_p \leq R2 \times C2$ の条件を満足する行列の行を示す最小整数R2が決定される(段階1602)。行列の行は、上側から下側に0、1、2、 $\dots$ 、R2-1で番号を割り当てる(段階1604)。

【0104】(2)入力 $u_{p,1}$ 、 $u_{p,2}$ 、 $u_{p,3}$ 、 $\dots$ 、 u_{p,U_s} は、0行の0列の $y_{p,1}$ から始めて $R2 \times C2$ 直角行列に行単位(row by row)で順方向に書き込まれ、入力 u_{p,U_s+1} 、 u_{p,U_s+2} 、 u_{p,U_s+3} 、 $\dots$ 、 u_{p,U_s+U_p} は、R2-1番目の行のx-1番目の行の地点から行単位で逆方向に書き込まれる(段階1606)。ここで、xは、UをC2で割った余りを意味し、1より大きいか、それとも同一であり、C2より小さい($1 \leq x < C2$)。このような動作によって生成された行列は、<数式7>のようである。

【0105】

【数7】

$$\begin{bmatrix} y_{p,1} & y_{p,2} & y_{p,3} & \dots & y_{p,C2} \\ y_{p,(C2+1)} & y_{p,(C2+2)} & y_{p,(C2+3)} & \dots & y_{p,(2 \times C2)} \\ \vdots & \vdots & \vdots & \dots & \vdots \\ y_{p,((R2-1) \times C2+1)} & y_{p,((R2-1) \times C2+2)} & y_{p,((R2-1) \times C2+3)} & \dots & y_{p,(R2 \times C2)} \end{bmatrix}$$

【0106】ここで、 $k=1, 2, \dots, U$ である場合、 $y_{p,k} = u_{p,k}$ である。 $R2 \times 2 > U$ である場合(段階1608)、 $k=U+1, U+2, \dots, R2 \times C2$ のために、 $y_{p,k} = 0$ または 1 の補助ビット(dummy bit)を挿入する(段階1610)。

【0107】(3)規則によって列交換(column permutation)を実施(段階1612)した後、その結果のビットは、高い信頼度を有するH部分及び低い信頼度を有するL部分に分けられ、下記のように、

【0108】

【数8】

$$y_{p,k}^H$$

及び

【0109】

【数9】

$$y_{p,k}^L$$

で表現される。

【0110】

【数10】

$$\begin{bmatrix}
 y_{p,1}^H & y_{p,(R/2+1)}^H & y_{p,R/2+1}^H & \cdots & y_{p,((C/2-1) \times R/2+1)}^H \\
 y_{p,2}^H & y_{p,(R/2+2)}^H & y_{p,R/2+2}^H & \cdots & y_{p,((C/2-1) \times R/2+2)}^H \\
 \vdots & \vdots & \vdots & \cdots & \vdots \\
 y_{p,R/2}^H & y_{p,R/2}^H & y_{p,3 \times R/2}^H & \cdots & y_{p,(C/2 \times R/2)}^H \\
 y_{p,1}^L & y_{p,(R/2+1)}^L & y_{p,R/2+1}^L & \cdots & y_{p,((C/2-1) \times R/2+1)}^L \\
 y_{p,2}^L & y_{p,(R/2+2)}^L & y_{p,R/2+2}^L & \cdots & y_{p,((C/2-1) \times R/2+2)}^L \\
 \vdots & \vdots & \vdots & \cdots & \vdots \\
 y_{p,R/2}^L & y_{p,R/2}^L & y_{p,3 \times R/2}^L & \cdots & y_{p,(C/2 \times R/2)}^L
 \end{bmatrix}$$

【0111】(4)高い信頼度を有する行及び低い信頼度を有する行が2行ずつ繰り返されるように、低い信頼度を有する行と高い信頼度を有する行の位置を<数式11>のように変更する(段階1614)。前記補助ビット

は、行及び列の交換の後、削除される(段階1616)

【0112】

【数11】

$$\begin{bmatrix}
 y_{p,1}^H & y_{p,(R/2+1)}^H & y_{p,R/2+1}^H & \cdots & y_{p,((C/2-1) \times R/2+1)}^H \\
 y_{p,2}^H & y_{p,(R/2+2)}^H & y_{p,R/2+2}^H & \cdots & y_{p,((C/2-1) \times R/2+2)}^H \\
 y_{p,1}^L & y_{p,(R/2+1)}^L & y_{p,R/2+1}^L & \cdots & y_{p,((C/2-1) \times R/2+1)}^L \\
 y_{p,2}^L & y_{p,(R/2+2)}^L & y_{p,R/2+2}^L & \cdots & y_{p,((C/2-1) \times R/2+2)}^L \\
 \vdots & \vdots & \vdots & \cdots & \vdots \\
 y_{p,R/2-1}^H & y_{p,R/2-1}^H & y_{p,3 \times R/2-1}^H & \cdots & y_{p,(C/2 \times R/2-1)}^H \\
 y_{p,R/2}^H & y_{p,R/2}^H & y_{p,3 \times R/2}^H & \cdots & y_{p,(C/2 \times R/2)}^H \\
 y_{p,R/2-1}^L & y_{p,R/2-1}^L & y_{p,3 \times R/2-1}^L & \cdots & y_{p,(C/2 \times R/2-1)}^L \\
 y_{p,R/2}^L & y_{p,R/2}^L & y_{p,3 \times R/2}^L & \cdots & y_{p,(C/2 \times R/2)}^L
 \end{bmatrix}$$

【0113】(5)ブロックインターリーブの出力は、列間の交換及び行間交換された $R \times C/2$ 行列から列単位で読み取られる(段階1618)。前記出力は、 $v_{p,1}, v_{p,2}, v_{p,3}, \dots, v_{p,U}$ で表現される。

【0114】3. 本発明の実施形態による受信装置以下、本発明1つのインターリーブ内に備わったバッファを論理的に区分することによってSMP技術を具現する送信装置に対応する受信装置に関して説明する。前記受信装置は、図2に示す送信装置と対称的な構造を有する。前記受信装置のデインターリーブは、図17及び図18において説明する。

【0115】受信された信号は、送信装置の変調部によって変調されたシンボルの形態であるので、復調器によって優先的に復調された後、デインターリーブに入力される。前記デインターリーブは、図2に示すインターリーブの対称構造である。直列化したビットは、インターリーブングバッファの上段及び下段に書き込まれることができるように、並列ビットに変化されるべきである。前記論理的に区分されたバッファは、インターリーブの逆動作によってデインターリーブを遂行し、分配部は、その出力ビットをシステムティックビットとパリティビットに分類する。レートマッチング部は、送信装置によってレートマッチングされたビットの位置を判断し、前記判断された位置に0を挿入することによ

て、他のビットが復調部の適した入力端に入力できるようにする。復調部は、送信装置の符号化部によって符号化されたビットを復号する装置であり、チャネル上で発生するエラーを補正する。送信された信号が正確に受信されているか否かを判断するために、前記エラーが補正された出力に対してCRC検査部によってCRC検査が遂行される。エラーが検出された場合、前記受信装置は、再伝送を送信装置に要求する。高速パケット伝送システムは、多様な変調率(modulation order)及び符号化率(code rate)を使用するので、制御部によって各機能が調節される。

【0116】3. 1 第1実施形態による受信装置の構成

図17は、第1実施形態による受信装置の構成を示す。前記受信装置は、図7を参照して説明した送信装置に対応する。

【0117】図17を参照すると、復調部1710によって復号されたデータビットは、デマルチプレクサ(DEMUX)1720によって逆多重化される。前記DEMUX1720は、所定の数分だけの入力されたビットを変調方式によって逆多重化し、前記逆多重化されたビットをデインターリーブのバッファ1730の第1書き込み領域及び第2書き込み領域に伝送する。例えば、前記変調方式が16QAMである場合、前記DEMUX1

720は、前記入力ビットを2ビットずつ前記バッファ領域1730の第1書き込み領域及び第2書き込み領域にそれぞれ伝送する。しかしながら、前記変調方式が64QAMである場合、前記DEMUX1720は、前記入力ビットを3ビットずつ前記バッファ領域1730の第1書き込み領域及び第2書き込み領域にそれぞれ伝送する。

【0118】符号化率が1/2である場合、システムティックビット及びパリティビットが区分されて前記第1及び第2書き込み領域に伝送される。しかしながら、前記符号化率が3/4である場合は、前記第1書き込み領域にはシステムティックビットのみが提供され、前記第2書き込み領域にはシステムティックビット及びパリティビットが入力される。

【0119】前記デインターリーブのバッファ領域1730に書き込まれるデータは、前記インターリーブの逆変換過程によってデインターリーブされ、前記システムティックビット及びパリティビットを区分して生成する。

【0120】3.2 第2実施形態による受信装置の構成

図18は、本発明の第2実施形態による受信装置の構造を示す。前記受信装置は、図13を参照して説明した送信装置に対応する。

【0121】図18を参照すると、復調部1810によって復号されたビットデータは、デマルチプレクサによる逆多重化過程を遂行せずに、デインターリーブのバッファ領域1820の第1書き込み領域及び第2書き込み領域に提供される。図13において説明したように、前記バッファ領域1310に貯蔵された符号化ビットをインターリーブ過程において行交換するので、前記送信装置は、所定の読み出し方法を通してマルチプレクサなしで多重化を遂行する。同様に、前記受信装置も前記受信されたビットに対して行交換を遂行することによって、逆多重化過程を遂行せずにデインターリーブを遂行することができる。

【0122】例えば、前記変調方式が16QAMである場合、前記バッファ領域1820に書き込まれたビットは、前記第1書き込み領域と前記第2書き込み領域との間に2行ずつ行交換が遂行される。前記変調方式が64QAMである場合、前記バッファ領域1820に書き込まれたビットは、前記第1書き込み領域と前記第2書き込み領域との間に3行ずつ行交換が遂行される。

【0123】前記デインターリーブのバッファ1820に書き込まれたデータビットは、インターリーブの逆動作によってデインターリーブされ、前記システムティックビット及びパリティビットを区分して生成する。

【0124】前記デインターリーブは、インターリーブが論理的に区分される場合、本発明によって提案されたデインターリーブングアルゴリズムによって、図17及

び図18のような構造を有する。前記デインターリーブングアルゴリズムは、図19に示すようである。

【0125】3.3 本発明の実施形態による受信装置の動作

図19は、本発明の実施形態によるデインターリーブング過程を示すフローチャートである。前記デインターリーブング過程は、前記送信装置のインターリーブによって遂行されるインターリーブング過程によって多少異なって遂行される。最終的に元のシステムティックビット及びパリティビットを生成するために、前記受信されたビットは、前記送信装置によって遂行されたそれぞれの方法に対応する方法によってデインターリーブされる。

【0126】図19を参照して、本発明の実施形態による受信装置のデインターリーブの動作を説明する。前記デインターリーブは、 $u_{p,1}$ 、 $u_{p,2}$ 、 $u_{p,3}$ 、 $\dots$ 、 u_{p,U_s} 及び u_{p,U_s+1} 、 u_{p,U_s+2} 、 u_{p,U_s+3} 、 $\dots$ 、 u_{p,U_s+U_p} を受信する(段階1900)。

【0127】(1)まず、列の総数C2を30に設定する。列の番号は、左側から右側に0、1、2、 $\dots$ 、C2-1である。 $U=U_s+U_p \leq R2 \times C2$ の条件を満足する行列の行を示す最小整数R2を決定する(段階1902)。上側から下側に0、1、2、 $\dots$ 、R2-1に行番号が割り当てられる(段階1904)。

【0128】(2)入力 $u_{p,1}$ 、 $u_{p,2}$ 、 $u_{p,3}$ 、 $\dots$ 、 u_{p,U_s} は、0行及び0列の $y_{p,1}$ から始めて $R2 \times C2$ 直角行列において行単位(row by row)で書き込まれ、入力 u_{p,U_s+1} 、 u_{p,U_s+2} 、 u_{p,U_s+3} 、 $\dots$ 、 u_{p,U_s+U_p} は、R2-1番目の行及びx-1番目の列の地点から始めて行単位で逆方向に書き込まれる(段階1906)。ここで、xは、UをC2で割った余りを意味し、1より大きいか、それとも同一であり、C2より小さい($1 \leq x < C2$)。 $R2 \times C2 > U$ である場合(段階1908)、 $k=U+1$ 、 $U+2$ 、 $\dots$ 、 $R2 \times C2$ のために、 $y_{p,k}=0$ であるから1の補助ビット(dummy bit)を挿入する(段階1910)。前記補助ビットは、列交換(段階1912)された後、除去(段階1914)される。

【0129】(3)規則によって列交換(column permutation)が遂行(段階1912)された後、その結果のビットはシステムティックビットS部分とパリティビットP部分に分けられる。

【0130】(4)デインターリーブの出力は、列交換された $R2 \times C2$ 行列をシステムティックビットとパリティビットに分けることによって、2ビットずつ行単位で読み出される(段階1916)。

【0131】

【発明の効果】前述してきたように、本発明は、高い重要度を有するビットを高い信頼度を有するシンボルにマッピングすることにおいて、インターリーブング動作を

効率的に遂行する方法を提供することによって、ハードウェア複雑度の増加を防止し、既存のインターリービング方式と互換性を維持することができる。重要度によって信頼度を差別して割り当てるSMP技術は、理論的に十分な効果を奏しているため、前記SMP技術を具現することは非常に大切である。本発明は、高速パケット伝送システム、特に、HSDPAまたは1XEV-DVシステムに適用される時、その利得(gain)を維持しながら、アルゴリズムの最小変更及びハードウェアの最小追加によって具現することができる。

【図面の簡単な説明】

【図1】 従来技術による高速パケット伝送システムの構造を示すブロック図である。

【図2】 本発明の実施形態によって重要度によって信頼度を差別して割り当てるSMPを支援する高速パケット伝送システムの構造を示すブロック図である。

【図3】 本発明の実施形態によって、符号化率が1/2である場合、十分のサイズを有するように物理的に区分された2つのインターリービングバッファに同一の比率で入力されたシステムティックビット及びパリティビットが16QAMまたは64QAMのシンボルにマッピングされる過程を示すブロック図である。

【図4】 本発明の実施形態によって十分のサイズを有するように物理的に区分された2つのインターリービングバッファに異なる比率で入力されたシステムティックビット及びパリティビットが16QAMまたは64QAMのシンボルにマッピングされる過程を示すブロック図である。

【図5】 本発明の実施形態によって、符号化率が3/4である場合、最小のサイズを有するように物理的に区分された2つのインターリービングバッファに異なる比率で入力されたシステムティックビット及びパリティビットが16QAMまたは64QAMのシンボルにマッピングされる過程を示すブロック図である。

【図6】 本発明の実施形態によってインターリーバを物理的に区分することによってSMP技術を適用する過程を示すフローチャートである。

【図7】 本発明の第1実施形態による送信装置の構成を示すブロック図である。

【図8A】 本発明の第1実施形態による1/2の符号化率を使用する場合の書き込み過程の例を示す図である。

【図8B】 本発明の第1実施形態による1/2の符号化率を使用する場合の書き込み過程の例を示す図である。

【図9A】 本発明の第1実施形態による3/4の符号化率を使用する場合の書き込み過程の例を示す図である。

【図9B】 本発明の第1実施形態による3/4の符号

化率を使用する場合の書き込み過程の例を示す図である。

【図10A】 本発明の第1実施形態によって、3/4の符号化率を使用する場合、補助ビットを利用する書き込み過程の例を示す図である。

【図10B】 本発明の第1実施形態によって、3/4の符号化率を使用する場合、補助ビットを利用する書き込み過程の例を示す図である。

【図10C】 本発明の第1実施形態によって、3/4の符号化率を使用する場合、補助ビットを利用する書き込み過程の例を示す図である。

【図10D】 本発明の第1実施形態によって、3/4の符号化率を使用する場合、補助ビットを利用する書き込み過程の例を示す図である。

【図11A】 本発明の第1実施形態による符号化ビットの読み出し過程の例を示す図である。

【図11B】 本発明の第1実施形態による符号化ビットの読み出し過程の例を示す図である。

【図12】 本発明の第1実施形態によるインターリーバを論理的に区分することによってSMP技術を適用する過程を示すフローチャートである。

【図13】 本発明の第2実施形態による送信装置の構成を示すブロック図である。

【図14A】 本発明の第2実施形態による書き込み過程の例を示す図である。

【図14B】 本発明の第2実施形態による書き込み過程の例を示す図である。

【図15A】 本発明の第2実施形態による読み出し過程の例を示す図である。

【図15B】 本発明の第2実施形態による読み出し過程の例を示す図である。

【図16】 本発明の第2実施形態によってインターリーバを論理的に区分することによってSMP技術を適用する過程を示すフローチャートである。

【図17】 本発明の第1実施形態による送信装置に対応する受信装置の構造を示すブロック図である。

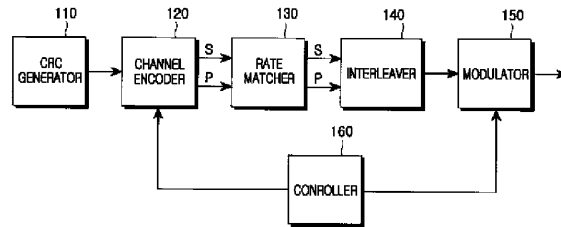
【図18】 本発明の第2実施形態による送信装置に対応する受信装置の構造を示すブロック図である。

【図19】 本発明の実施形態による受信装置の動作を示すフローチャートである。

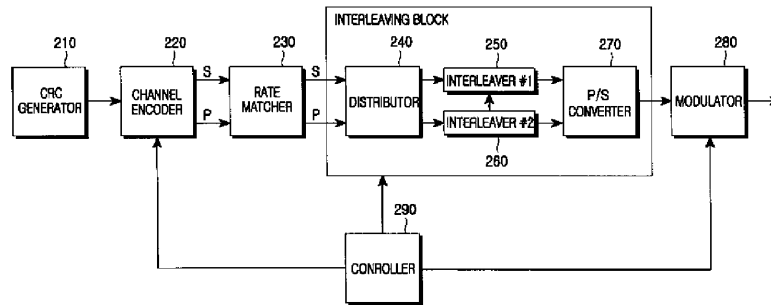
【符号の説明】

240 分配部
250・260 インターリーバ
270 並/直列変換部(P/S変換部)
280 変調部
710 インターリーバ
720 マルチプレクサ
730 変調器

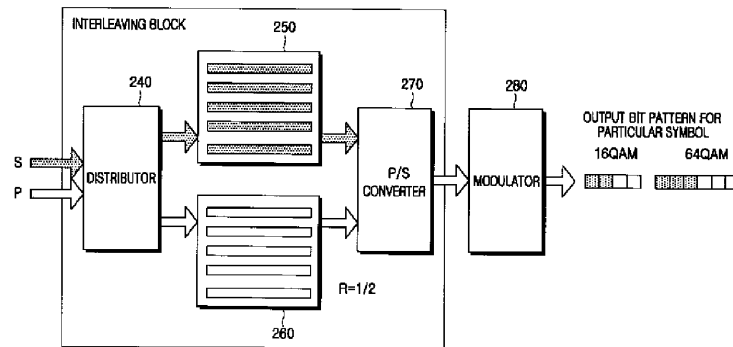
【図1】



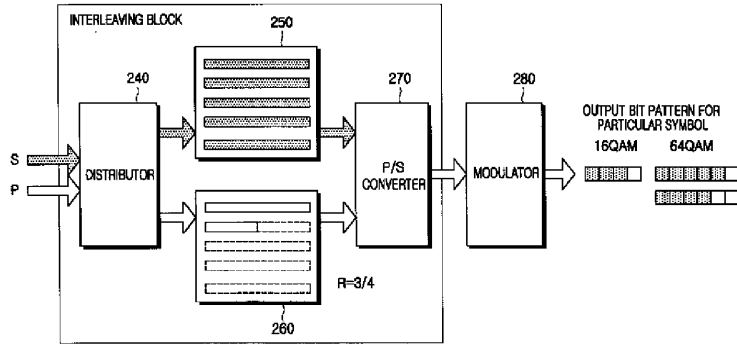
【図2】



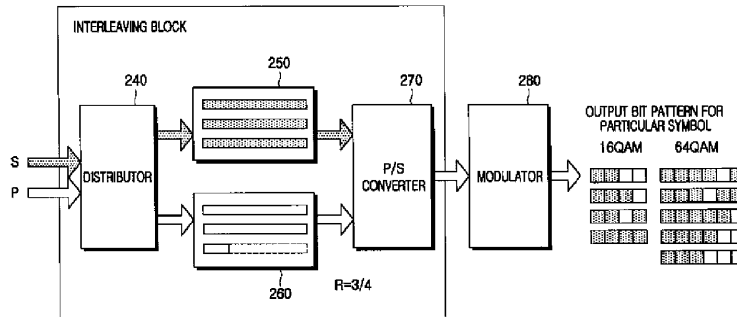
【図3】



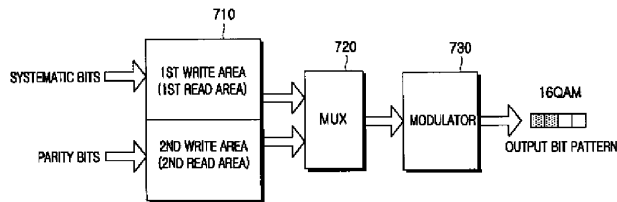
【図4】



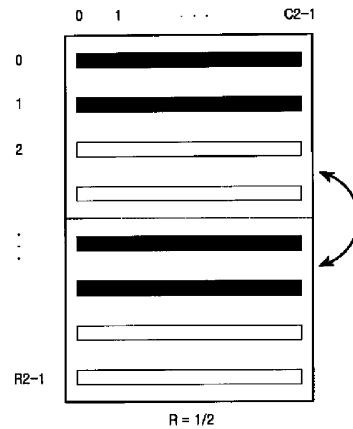
【図5】



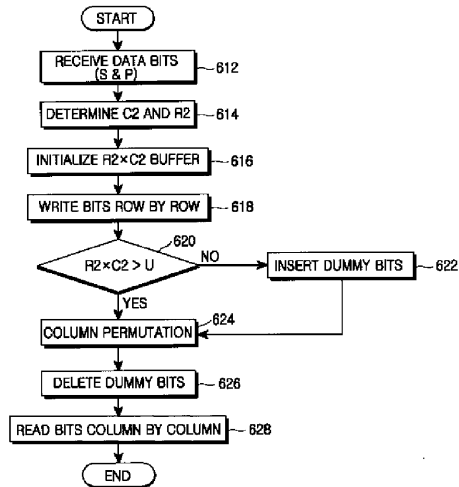
【図7】



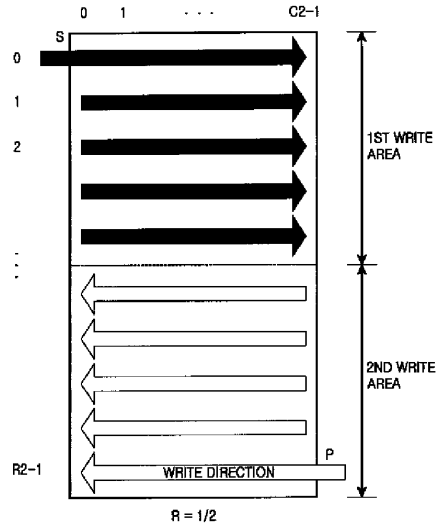
【図14A】



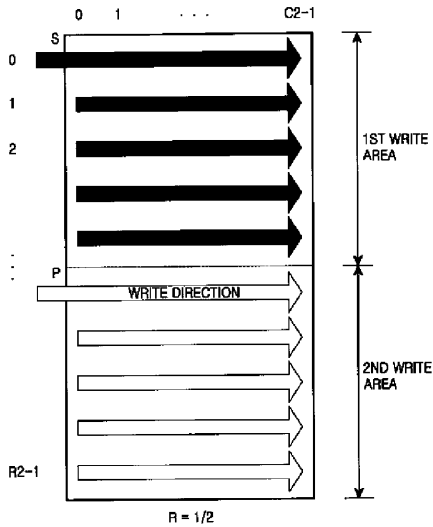
【図6】



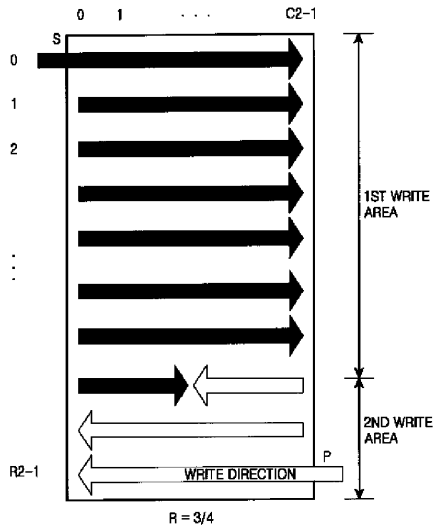
【図8A】



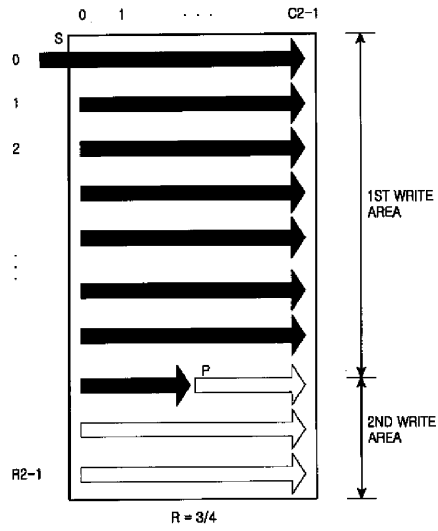
【図8B】



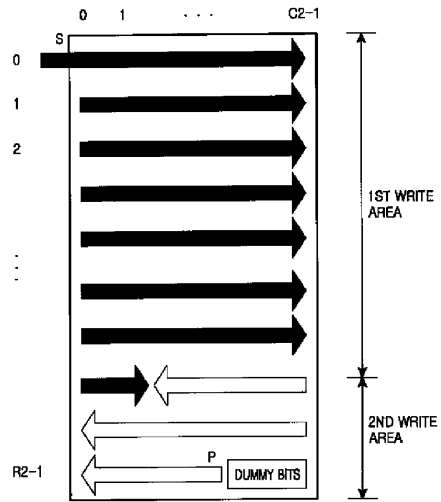
【図9A】



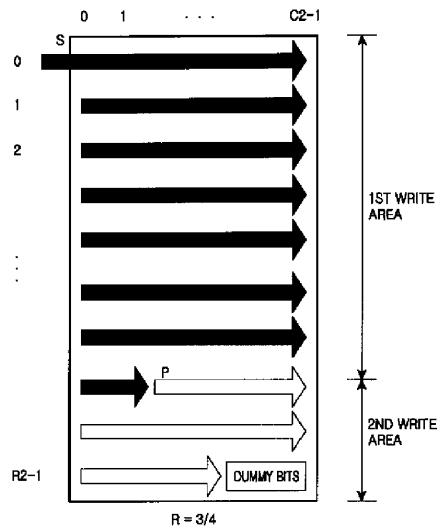
【図9B】



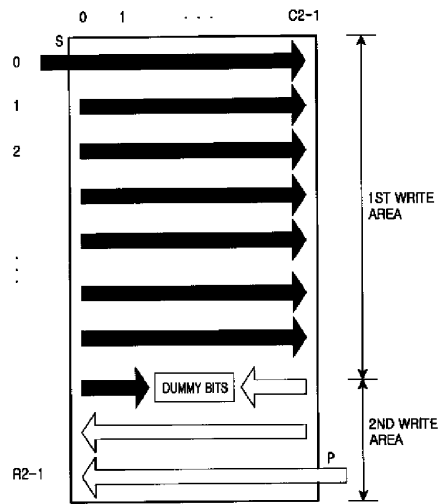
【図10A】



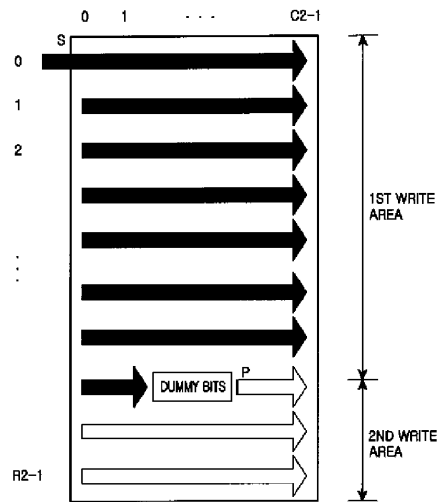
【図10B】



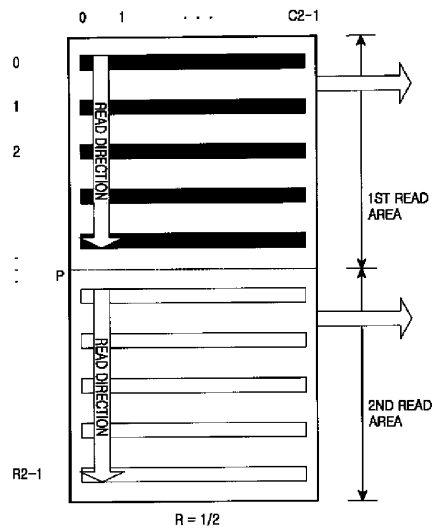
【図10C】



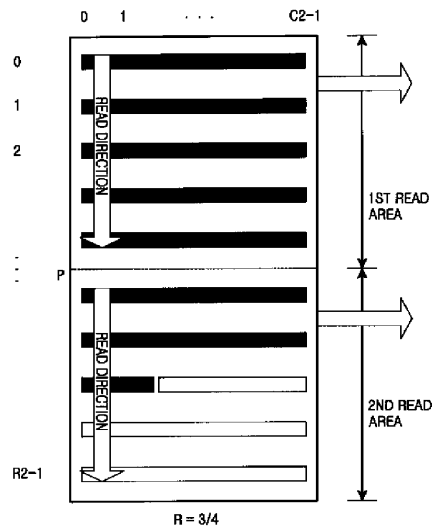
【図10D】



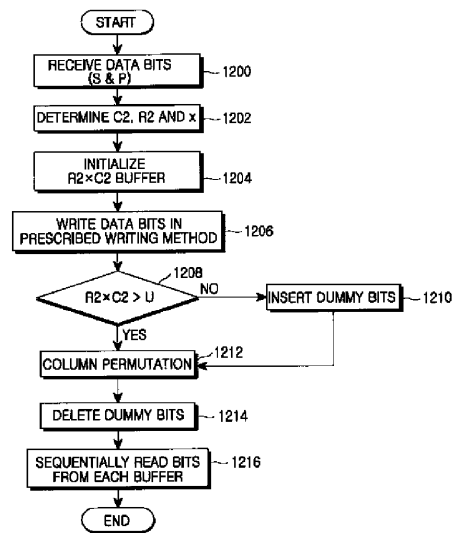
【図11A】



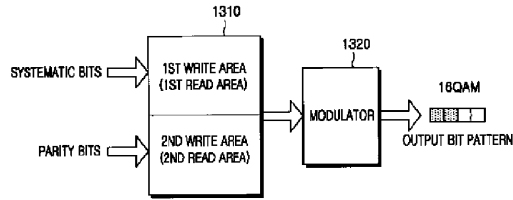
【図11B】



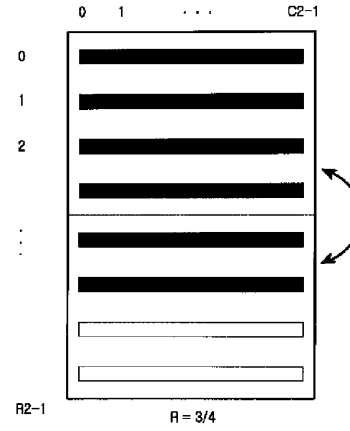
【図12】



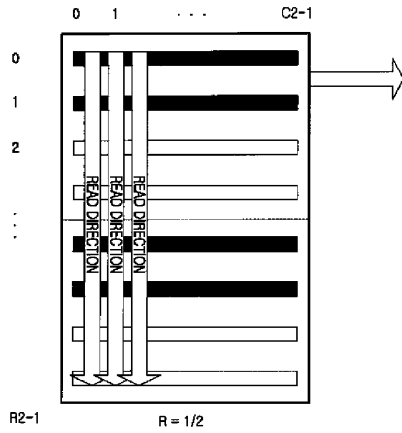
【図13】



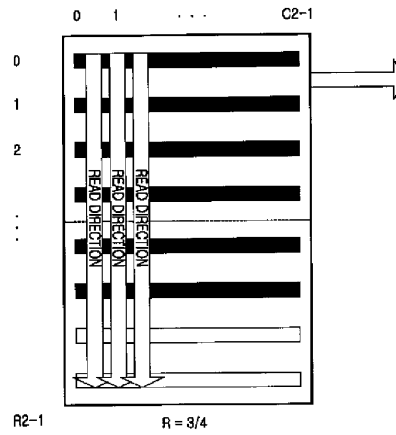
【図14B】



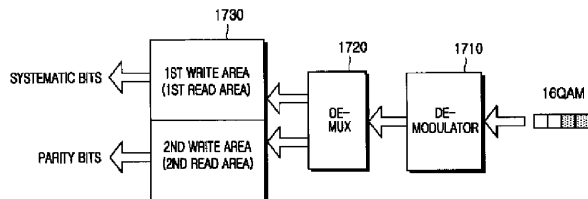
【図15A】



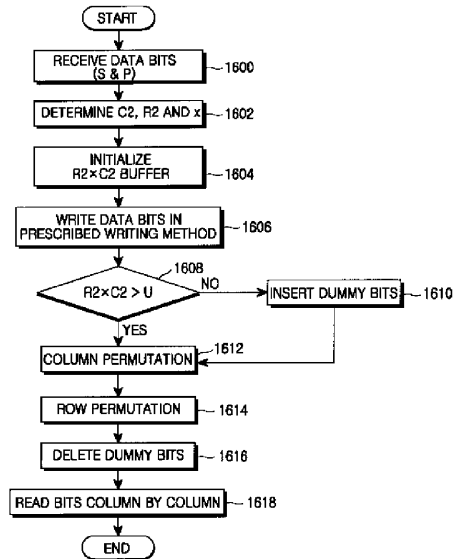
【図15B】



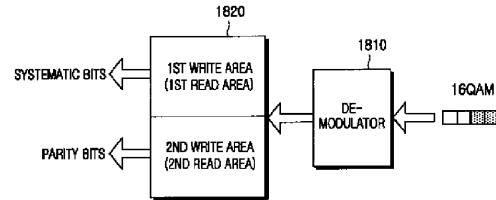
【図17】



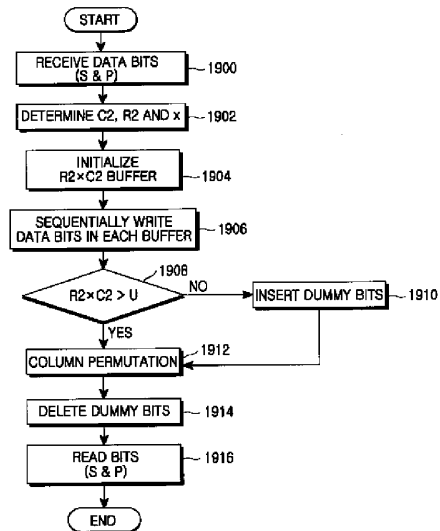
【図16】



【図18】



【図19】



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【外国語明細書】

1 Title of Invention

**INTERLEAVING APPARATUS AND METHOD FOR SYMBOL
MAPPING IN AN HSDPA MOBILE COMMUNICATION SYSTEM**

2 Claims

1. A method for interleaving coded bits encoded at a prescribed code rate in a transmitter of a mobile communication system having a buffer comprised of a plurality of rows and columns, for writing the coded bits, the method comprising the steps of:

separating the buffer into a first write area and a second write area according to a ratio of coded bits with higher priority among the coded bits to coded bits with lower priority;

sequentially writing a stream of the coded bits with higher priority in a row direction from a first column to a last column among the columns in the first write area, and sequentially writing a stream of the coded bits with lower priority in a row direction from a first column to a last column among the columns in the second write area;

permuting the columns in the buffer according to a given rule;

dividing the rows in the buffer into a first read area and a second read area having equal size; and

alternately reading a number of bits equal to a number determined by a prescribed modulation technique from the first read area and the second read area in such a manner that the bits are sequentially read in a column direction from a first row to a last row among the rows of each of the first read area and the second read area.

2. The method of claim 1, further comprising the step of mapping coded bits read from the first read area to a position with a first reliability of a symbol, and mapping coded bits read from the second read area to a position with a second reliability, the second reliability being lower than the first reliability.

3. The method of claim 1, wherein if the modulation technique for

modulating the coded bits is 16QAM (16-ary Quadrature Amplitude Modulation), the bits read from the first read area and the bits read from the second read area are alternately read 2 bits at a time.

4. The method of claim 1, wherein if the modulation technique for modulating the coded bits is 64QAM, the bits read from the first read area and the bits read from the second read area are alternately read 3 bits at a time.

5. The method of claim 1, wherein dummy bits are inserted in buffer locations remaining unused after writing the coded bits.

6. The method of claim 5, wherein the dummy bits are inserted between the first write area and the second write area.

7. The method of claim 5, wherein the dummy bits are inserted after the coded bits of the second write area.

8. The method of claim 1, wherein the coded bits with higher priority are systematic bits.

9. The method of claim 1, wherein the coded bits with lower priority are parity bits.

10. The method of claim 1, wherein the ratio of the coded bits with higher priority to the coded bits with lower priority is determined according to the prescribed code rate.

11. A method for interleaving coded bits encoded at a prescribed code rate in a transmitter of a mobile communication system having a buffer comprised of a plurality of rows and columns, for writing the coded bits, the

method comprising the steps of:

separating the buffer into a first write area and a second write area according to a ratio of coded bits with higher priority among the coded bits to coded bits with lower priority;

sequentially writing a stream of the coded bits with higher priority in a row direction from a first column to a last column among the columns in the first write area, and sequentially writing a stream of the coded bits with lower priority in a row direction from a first column to a last column among the columns in the second write area;

permuting the columns in the buffer according to a given rule;

dividing the rows in the buffer into a first read area and a second read area having equal size;

permuting, between the first read area and the second read area, a number of rows equal to a number determined by a prescribed modulation technique among the rows of each of the first read area and the second read area; and

sequentially reading the rows in the entire buffer in a column direction from a first row to a last row.

12. The method of claim 11, further comprising the step of mapping coded bits read from the first read area to a position with a first reliability of a symbol, and mapping coded bits read from the second read area to a position with a second reliability, the second reliability being lower than the first reliability.

13. The method of claim 11, wherein if the modulation technique for modulating the coded bits is 16QAM (16-ary Quadrature Amplitude Modulation), the bits read from the first read area and the bits read from the second read area are alternately read 2 bits at a time.

14. The method of claim 11, wherein if the modulation technique for modulating the coded bits is 64QAM, the bits read from the first read area and the bits read from the second read area are alternately read 3 bits at a time.

15. The method of claim 11, wherein dummy bits are inserted in buffer locations remaining unused after writing the coded bits.

16. The method of claim 15, wherein the dummy bits are inserted between the first write area and the second write area.

17. The method of claim 15, wherein the dummy bits are inserted after the coded bits of the second write area.

18. The method of claim 11, wherein the coded bits with higher priority are systematic bits.

19. The method of claim 11, wherein the coded bits with lower priority are parity bits.

20. The method of claim 11, wherein the ratio of the coded bits with higher priority to the coded bits with lower priority is determined according to the prescribed code rate.

21. A method for interleaving coded bits encoded at a prescribed code rate in a transmitter of a mobile communication system having a buffer comprised of a plurality of rows and columns, for writing the coded bits, the method comprising the steps of:

separating the buffer into a first write area and a second write area according to a ratio of coded bits with higher priority among the coded bits to coded bits with lower priority;

sequentially writing a stream of the coded bits with higher priority in a

row direction from a first column to a last column among the columns in the first write area, and writing a stream of the coded bits with lower priority in a row direction from a last column to a first column among the columns in the second write area in such a manner that the stream of coded bits is written in a reverse direction from a last row to a first row in the second write area;

permuting the columns in the buffer according to a given rule;

dividing the rows in the buffer into a first read area and a second read area having equal size; and

alternately reading a number of bits equal to a number determined by a prescribed modulation technique from the first read area and the second read area in such a manner that the bits are sequentially read in a column direction from a first row to a last row among the rows of each of the first read area and the second read area.

22. The method of claim 21, further comprising the step of mapping coded bits read from the first read area to a position with a first reliability of a symbol, and mapping coded bits read from the second read area to a position with a second reliability, the second reliability being lower than the first reliability.

23. The method of claim 21, wherein if the modulation technique for modulating the coded bits is 16QAM (16-ary Quadrature Amplitude Modulation), the rows of each of the first read area and the second read area are permuted such that the rows of the first read area and the rows of the second read area are alternately arranged in the buffer area 2 rows at a time.

24. The method of claim 21, wherein if the modulation technique for modulating the coded bits is 64QAM, the rows of each of the first read area and the second read area are permuted such that the rows of the first read area and the rows of the second read area are alternately arranged in the buffer area 3 rows at

a time.

25. The method of claim 21, wherein if dummy bits are inserted in buffer locations remaining unused after writing the coded bits.

26. The method of claim 25, wherein the dummy bits are inserted between the first write area and the second write area.

27. The method of claim 25, wherein the dummy bits are inserted after the coded bits of the second write area.

28. The method of claim 21, wherein the coded bits with higher priority are systematic bits.

29. The method of claim 21, wherein the coded bits with lower priority are parity bits.

30. The method of claim 21, wherein the ratio of the coded bits with higher priority to the coded bits with lower priority is determined according to the prescribed code rate.

31. A method for interleaving coded bits encoded at a prescribed code rate in a transmitter of a mobile communication system having a buffer comprised of a plurality of rows and columns, for writing the coded bits, the method comprising the steps of:

separating the buffer into a first write area and a second write area according to a ratio of coded bits with higher priority among the coded bits to coded bits with lower priority;

sequentially writing a stream of the coded bits with higher priority in a row direction from a first column to a last column among the columns in the first

write area, and writing a stream of the coded bits with lower priority in a row direction from a last column to a first column among the columns in the second write area in such a manner that the stream of coded bits is written in a reverse direction from a last row to a first row in the second write area;

permuting the columns in the buffer according to a given rule;

dividing the rows in the buffer into a first read area and a second read area having equal size;

permuting, between the first read area and the second read area, a number of rows equal to a number determined by a prescribed modulation technique among the rows of each of the first read area and the second read area; and

sequentially reading the rows in the entire buffer in a column direction from a first row to a last row.

32. The method of claim 31, further comprising the step of mapping coded bits read from the first read area to a position with a first reliability of a symbol, and mapping coded bits read from the second read area to a position with a second reliability, the second reliability being lower than the first reliability.

33. The method of claim 31, wherein if the modulation technique for modulating the coded bits is 16QAM (16-ary Quadrature Amplitude Modulation), the rows of each of the first read area and the second read area are permuted such that the rows of the first read area and the rows of the second read area are alternately arranged in the buffer area 2 rows at a time.

34. The method of claim 31, wherein if the modulation technique for modulating the coded bits is 64QAM, the rows of each of the first read area and the second read area are permuted such that the rows of the first read area and the rows of the second read area are alternately arranged in the buffer area 3 rows at

a time.

35. The method of claim 31, wherein dummy bits are inserted in buffer locations remaining unused after writing the coded bits.

36. The method of claim 35, wherein the dummy bits are inserted between the first write area and the second write area.

37. The method of claim 35, wherein the dummy bits are inserted after the coded bits of the second write area.

38. The method of claim 31, wherein the coded bits with higher priority are systematic bits.

39. The method of claim 31, wherein the coded bits with lower priority are parity bits.

40. The method of claim 31, wherein the ratio of the coded bits with higher priority to the coded bits with lower priority is determined according to the prescribed code rate.

41. A method for interleaving coded bits encoded at a prescribed code rate in a transmitter of a mobile communication system having two buffers each comprised of a plurality of rows and columns, for writing the coded bits, the method comprising the steps of:

writing coded bits with higher priority among the coded bits in a first buffer and writing coded bits with lower priority in a second buffer, in such a manner that a stream of the coded bits with higher priority is sequentially written in a row direction from a first column to a last column among the columns of the first buffer and a stream of the coded with lower priority is sequentially written in

a row direction from a first column to a last column among the columns of the second buffer;

permuting the columns of the the first buffer and the second buffer according to a given rule; and

alternately reading a number of bits equal to a number determined by a prescribed modulation technique from the first buffer and the the second buffer in such a manner that the bits are sequentially read in a column direction from a first row to a last row among the rows of each of the first buffer and the second buffer.

42. The method of claim 41, further comprising the step of mapping coded bits read from the first buffer to a position with a first reliability of a symbol, and mapping coded bits read from the second buffer to a position with a second reliability, the second reliability being lower than the first reliability.

43. The method of claim 41, wherein if the modulation technique for modulating the coded bits is 16QAM (16-ary Quadrature Amplitude Modulation), the bits read from the first buffer and the bits read from the second buffer are alternately read 2 bits at a time.

44. The method of claim 41, wherein if the modulation technique for modulating the coded bits is 64QAM, the bits read from the first buffer and the bits read from the second buffer are alternately read 3 bits at a time.

45. The method of claim 41, wherein dummy bits are inserted in buffer locations remaining unused after writing the coded bits.

46. The method of claim 41, wherein the coded bits with higher priority are systematic bits.

47. The method of claim 41, wherein the coded bits with lower priority are parity bits.

48. The method of claim 41, wherein the ratio of the coded bits with higher priority to the coded bits with lower priority is determined according to the prescribed code rate.

49. The method of claim 41, further comprising the step of sequentially writing, if a size of the first buffer is insufficient for a total number of the coded bits with higher priority, coded bits unwritten in the first buffer among the coded bits with higher priority in a row direction from a first column among the columns of the second buffer, and sequentially writing a stream of the coded bits with lower priority in a row direction from a first column to a last column among the columns in a remaining area within the second buffer.

50. The method of claim 49, wherein the write area of the first buffer is identical in size to the write area of the second buffer.

51. An apparatus for interleaving coded bits encoded at a prescribed code rate in a transmitter of a mobile communication system having an encoder for encoding transmission data into coded bits at the prescribed code rate, the coded bits including coded bits with higher priority and coded bits with lower priority, and a buffer having a plurality of rows and columns, for writing the coded bits, the apparatus comprising:

an interleaver for separating the area of the buffer included therein into a first write area and a second write area according to a ratio of the coded bits with higher priority to the coded bits with lower priority, sequentially writing a stream of the coded bits with higher priority in a row direction from a first column to a last column among the columns in the first write area, and sequentially writing a stream of the coded bits with lower priority in a row direction from a first column

to a last column among the columns in the second write area, and permuting the columns in the buffer area according to a given rule; and

a multiplexer for dividing the rows in the buffer area into a first read area and a second read area having equal size, and alternately reading a number of bits equal to a number determined by a prescribed modulation technique from the first read area and the second read area in such a manner that the bits are sequentially read in a column direction from a first row to a last row among the rows of each of the first read area and the second read area, and multiplexing the read coded bits.

52. The apparatus of claim 51, further comprising a modulator for mapping coded bits read from the first read area of the buffer to a position with a first reliability of a symbol, and mapping coded bits read from the second read area of the buffer to a position with a second reliability, the second reliability being lower than the first reliability.

53. The apparatus of claim 51, wherein if the modulation technique for modulating the coded bits is 16QAM (16-ary Quadrature Amplitude Modulation), the bits read from each of the first read area and the second read area of the buffer included in the interleaver are alternately read 2 bits at a time.

54. The apparatus of claim 51, wherein if the modulation technique for modulating the coded bits is 64QAM, the bits read from each of the first read area and the second read area of the buffer included in the interleaver are alternately read 3 bits at a time.

55. The apparatus of claim 51, wherein dummy bits are inserted in buffer locations remaining unused after writing the coded bits.

56. The apparatus of claim 55, wherein the interleaver inserts the

dummy bits between the first write area and the second write area.

57. The apparatus of claim 55, wherein the interleaver inserts the dummy bits after the coded bits of the second write area.

58. The apparatus of claim 51, wherein the coded bits with higher priority are systematic bits.

59. The apparatus of claim 51, wherein the coded bits with lower priority are parity bits.

60. The apparatus of claim 51, wherein the ratio of the coded bits with higher priority to the coded bits with lower priority is determined according to the prescribed code rate.

61. An apparatus for interleaving coded bits encoded at a prescribed code rate in a transmitter of a mobile communication system having an encoder for encoding transmission data into coded bits at the prescribed code rate, the coded bits including coded bits with higher priority and coded bits with lower priority, and a buffer a plurality of rows and columns, for writing the coded bits, the apparatus comprising:

an interleaver for separating the area of the buffer into a first write area and a second write area according to a ratio of coded bits with higher priority to coded bits with lower priority, sequentially writing a stream of the coded bits with higher priority in a row direction from a first column to a last column among the columns in the first write area, and sequentially writing a stream of the coded bits with lower priority in a row direction from a first column to a last column among the columns in the second write area, permuting the columns in the buffer area according to a given rule, dividing the rows in the buffer area into a first read area and a second read area having equal size, and permuting, between the first

read area and the second read area, a number of rows equal to a number determined by a prescribed modulation technique among the rows of each of the first read area and the second read area.

62. The apparatus of claim 61, further comprising a modulator for mapping coded bits read from the first read area of the buffer to a position with a first reliability of a symbol, and mapping coded bits read from the second read area of the buffer to a position with a second reliability, the second reliability being lower than the first reliability.

63. The apparatus of claim 61, wherein if the modulation technique for modulating the coded bits is 16QAM (16-ary Quadrature Amplitude Modulation), the bits read from each of the first read area and the second read area of the buffer included in the interleaver are alternately read 2 bits at a time.

64. The apparatus of claim 61, wherein if the modulation technique for modulating the coded bits is 64QAM, the bits read from each of the first read area and the second read area of the buffer included in the interleaver are alternately read 3 bits at a time.

65. The apparatus of claim 61, wherein dummy bits are inserted in buffer locations remaining unused after writing the coded bits.

66. The apparatus of claim 65, wherein the interleaver inserts the dummy bits between the first write area and the second write area.

67. The apparatus of claim 65, wherein the interleaver inserts the dummy bits after the coded bits of the second write area.

68. The apparatus of claim 61, wherein the coded bits with higher

priority are systematic bits.

69. The apparatus of claim 61, wherein the coded bits with lower priority are parity bits.

70. The apparatus of claim 71, wherein the ratio of the coded bits with higher priority to the coded bits with lower priority is determined according to the prescribed code rate.

71. An apparatus for interleaving coded bits encoded at a prescribed code rate in a transmitter of a mobile communication system having an encoder for encoding transmission data into coded bits at the prescribed code rate, the coded bits including coded bits with higher priority and coded bits with lower priority, and a buffer having a plurality of rows and columns, for writing the coded bits, the apparatus comprising:

an interleaver for separating the area of the buffer into a first write area and a second write area according to a ratio of the coded bits with higher priority to the coded bits with lower priority, sequentially writing a stream of the coded bits with higher priority in a row direction from a first column to a last column among the columns in the first write area, and writing a stream of the coded bits with lower priority in a row direction from a last column to a first column among the columns in the second write area in such a manner that the stream of coded bits is written in a reverse direction from a last row to a first row in the second write area, and permuting the columns in the buffer area according to a given rule; and

a multiplexer for dividing the rows in the buffer area into a first read area and a second read area having equal size, alternately reading a number of bits equal to a number determined by a prescribed modulation technique from the first write area and the second write area, and sequentially reading coded bits in a column direction from a first row to a last row among the rows in the first read

area and the second read area, and multiplexing the read coded bits.

72. The apparatus of claim 71, further comprising a modulator for mapping coded bits read from the first read area of the buffer to a position with a first reliability of a symbol, and mapping coded bits read from the second read area of the buffer to a position with a second reliability, the second reliability being lower than the first reliability.

73. The apparatus of claim 71, wherein if the modulation technique for modulating the coded bits is 16QAM (16-ary Quadrature Amplitude Modulation), the interleaver for permuting rows of the first read area and the second read area of the buffer alternately arranges the rows of each of the first read area and the second read area in the buffer area 2 rows at a time.

74. The apparatus of claim 71, wherein if the modulation technique for modulating the coded bits is 64QAM, the interleaver for permuting rows of the first read area and the second read area of the buffer alternately arranges the rows of each of the first read area and the second read area in the buffer area 3 rows at a time.

75. The apparatus of claim 71, wherein dummy bits are inserted in buffer locations remaining unused after writing the coded bits.

76. The apparatus of claim 75, wherein the interleaver inserts the dummy bits between the first write area and the second write area.

77. The apparatus of claim 75, wherein the interleaver insets the dummy bits after the coded bits of the second write area.

78. The apparatus of claim 71, wherein the coded bits with higher

priority are systematic bits.

79. The apparatus of claim 71, wherein the coded bits with lower priority are parity bits.

80. The apparatus of claim 71, wherein the ratio of the coded bits with higher priority to the coded bits with lower priority is determined according to the prescribed code rate.

81. An apparatus for interleaving coded bits encoded at a prescribed code rate in a transmitter of a mobile communication system having an encoder for encoding transmission data into coded bits at the prescribed code rate, the coded bits including coded bits with higher priority and coded bits with lower priority, and a buffer having a plurality of rows and columns, for writing the coded bits, the apparatus comprising:

an interleaver for separating the area of the buffer into a first write area and a second write area according to a ratio of coded bits with higher priority to coded bits with lower priority, sequentially writing a stream of the coded bits with higher priority in a row direction from a first column to a last column among the columns in the first write area, and writing a stream of the coded bits with lower priority in a row direction from a last column to a first column among the columns in the second write area in such a manner that the stream of coded bits is written in a reverse direction from a last row to a first row in the second write area, permuting the columns in the buffer area according to a given rule, dividing the rows in the buffer area into a first read area and a second read area having equal size, and permuting, between the first read area and the second read area, a number of rows equal to a number determined by a prescribed modulation technique among the rows of each of the first read area and the second read area.

82. The apparatus of claim 81, further comprising a modulator for

mapping coded bits read from the first read area of the buffer to a position with a first reliability of a symbol, and mapping coded bits read from the second read area of the buffer to a position with a second reliability, the second reliability being lower than the first reliability.

83. The apparatus of claim 81, wherein if the modulation technique for modulating the coded bits is 16QAM (16-ary Quadrature Amplitude Modulation), the interleaver for permuting rows of the first read area and the second read area of the buffer alternately arranges the rows of each of the first read area and the second read area in the buffer area 2 rows at a time.

84. The apparatus of claim 81, wherein if the modulation technique for modulating the coded bits is 64QAM, the interleaver for permuting rows of the first read area and the second read area of the buffer alternately arranges the rows of each of the first read area and the second read area in the buffer area 3 rows at a time.

85. The apparatus of claim 81, wherein dummy bits are inserted in buffer locations remaining unused after writing the coded bits.

86. The apparatus of claim 85, wherein the interleaver inserts the dummy bits between the first write area and the second write area.

87. The apparatus of claim 85, wherein the interleaver inserts the dummy bits after the bits of the second write area in the buffer area.

88. The apparatus of claim 81, wherein the coded bits with higher priority are systematic bits.

89. The apparatus of claim 81, wherein the coded bits with lower

priority are parity bits.

90. The apparatus of claim 81, wherein the ratio of the coded bits with higher priority to the coded bits with lower priority is determined according to the prescribed code rate.

91. An apparatus for interleaving coded bits encoded at a prescribed code rate in a transmitter of a mobile communication system having an encoder for encoding transmission data into coded bits at the prescribed code rate, the coded bits including coded bits with higher priority and coded bits with lower priority, and buffers each having a plurality of rows and columns, for writing the coded bits, the apparatus comprising:

an interleaver having a first buffer for sequentially writing a stream of the coded bits with higher priority in a row direction from a first column to a last column among the columns in the write area thereof, and a second buffer for sequentially writing a stream of the coded bits with lower priority in a row direction from a first column to a last column among the columns in the write area thereof, the interleaver permuting the columns of the write areas in the first buffer and the second buffer according to a given rule; and

a multiplexer for alternately reading a number of bits equal to a number determined by a prescribed modulation technique from the write area of the first buffer and the write area of the second buffer in such a manner that the bits are sequentially read in a column direction from a first row to a last row among the rows of the write areas in each of the first buffer and the second buffer, and multiplexing the read coded bits.

92. The apparatus of claim 91, further comprising a modulator for mapping coded bits read from the write area of the first buffer to a position with a first reliability of a symbol, and mapping coded bits read from the write area of the second buffer to a position with a second reliability, the second reliability

being lower than the first reliability.

93. The apparatus of claim 91, wherein if the modulation technique for modulating the coded bits is 16QAM (16-ary Quadrature Amplitude Modulation), the bits read from the first buffer and the second buffer included in the interleaver are alternately read 2 bits at a time.

94. The apparatus of claim 91, wherein if the modulation technique for modulating the coded bits is 64QAM, the bits read from the first buffer and the second buffer included in the interleaver are alternately read 3 bits at a time.

95. The apparatus of claim 91, wherein dummy bits are inserted in buffer locations remaining unused after writing the coded bits.

96. The apparatus of claim 91, wherein the coded bits with higher priority are systematic bits.

97. The apparatus of claim 91, wherein the coded bits with lower priority are parity bits.

98. The apparatus of claim 91, wherein the ratio of the coded bits with higher priority to the coded bits with lower priority is determined according to the prescribed code rate.

99. The apparatus of claim 91, wherein if a size of the first buffer is insufficient for storing a total number of the coded bits with higher priority, the interleaver sequentially writes coded bits unwritten in the first buffer among the coded bits with higher priority in a row direction from a first column among the columns in the write area of the second buffer, and sequentially writes a stream of the coded bits with lower priority in a row direction from a first column to a last column among the columns in a remaining area within the write area of the

second buffer.

100. The apparatus of claim 91, wherein the write area of the first buffer is identical in size to the write area of the second buffer.

101. A method for deinterleaving coded bits demodulated by a prescribed demodulation technique in a receiver of a mobile communication system having a buffer comprised of rows and columns, for writing the coded bits, the method comprising the steps of:

demultiplexing the coded bits at prescribed periods;

separating the buffer into a first write area and a second write area having equal size;

sequentially writing one demultiplexed output into the first write area and sequentially writing another demultiplexed output into the second write area;

dividing the buffer into a first read area and a second read area according to a ratio of coded bits with higher priority among the coded bits to coded bits with lower priority; and

reading coded bits from the first read area and the second read area according to the ratio of the coded bits with higher priority to the coded bits with lower priority.

102. An apparatus for deinterleaving coded bits demodulated by a prescribed demodulation technique in a receiver of a mobile communication system having a buffer comprised of rows and columns, for writing the coded bits, the apparatus comprising:

a deinterleaver for separating a use area of the buffer into a first write area and a second write area having equal size, sequentially writing one demultiplexed output into the first write area and sequentially writing another demultiplexed output into the second write area, dividing the use area into a first read area and a second read area according to a ratio of coded bits with higher

priority among the coded bits to coded bits with lower priority, and reading coded bits from the first read area and the second read area according to the ratio of the coded bits with higher priority to the coded bits with lower priority, and deinterleaving the read coded bits.

103. The apparatus of claim 102, further comprising a demultiplexer for demultiplexing the demodulated bits at prescribed period, and providing the demultiplexed bits to the deinterleaver.

3 Detailed Description of Invention

PRIORITY

This application claims priority to an application entitled "Interleaving Apparatus and Method for Symbol Mapping in an HSDPA Mobile Communication System" filed in the Korean Industrial Property Office on December 21, 2001 and assigned Serial No. 2001-83064, the contents of which are incorporated herein by reference.

BACKGROUND OF THE INVENTION

1. Field of the Invention

The present invention relates generally to a data transmission/reception apparatus and method in a CDMA (Code Division Multiple Access) mobile communication system, and in particular, to a data transmission/reception apparatus and method for improving reliability of transmission data bits.

2. Description of the Related Art

In reality, in a communication system, it is impossible to receive a transmitted signal without any distortion or noise. Particularly, a mobile communication system that transmits and receives signals through a wireless network is more susceptible to the distortion or noise, compared with a communication system that transmits and receives signals through a wired network.

Therefore, various techniques for minimizing the influence of the distortion or noise have been proposed, and an error control coding technique is one of the typical proposed techniques. Codes used for the error control coding

technique are classified into memoryless codes and memory codes. The memoryless codes include linear block codes, and the memory codes include convolutional codes and turbo codes. A device for creating such codes is called a "channel encoder," and its outputs can be divided into systematic bits and parity bits according to the error control coding technique in use. The turbo codes are typically used for the error control coding technique for separately outputting the systematic bits and the parity bits. Of course, in addition to the turbo codes, systematic convolutional codes, a kind of the convolutional codes, are used to separately output the systematic bits and the parity bits. Here, the systematic bits mean actual signals to be transmitted, and the parity bits are signals added to correct a possible transmission error of the systematic bits during decoding. However, even in the case of the error control-coded signals, if a burst error occurs in the systematic bits or parity bits, it is not easy to correct the burst error. Such a phenomenon frequently occurs when a signal passes through a fading channel, and an interleaving technique is typically used to prevent this phenomenon.

The interleaving technique is used to more efficiently overcome the burst error by dispersing a defective part into several positions instead of concentrating the defective part on a particular position.

The interleaved signal undergoes symbol mapping in a digital modulator. Here, if an order of the modulator is increased, the number of bits included in one symbol is also increased. Particularly, in the case of a high-order modulation technique of over 16QAM (16-ary Quadrature Amplitude Modulation), one symbol includes 4 or more information bits, and the information bits can be classified according to their reliability. Here, as to the reliability, in a process of modulating one symbol by a transmitter, a symbol representing two bits in a macro region like the left/right quadrants or upper/lower quadrants on the X/Y-axis has "high reliability," and a symbol representing two bits in a micro region

has "low reliability."

FIG. 1 schematically illustrates a structure of a transmitter in an HSDPA (High Speed Downlink Packet Access) mobile communication system. As illustrated, the transmitter includes a channel encoder, an interleaver and a modulator.

Referring to FIG. 1, input information bits to which CRC (Cyclic Redundancy Check) bits, or error detection data, are added in a CRC generator 110, are provided to a channel encoder 120, and the channel encoder 120 encodes the CRC bit-added input information bits through a predetermined coding process, and outputs coded bits, i.e., systematic bits S and parity bits P. The channel encoder 120 has at least one code rate in order to encode the information bits. The code rate may become 1/2 or 3/4. In addition, when the channel encoder 120 supports a plurality of code rates through symbol puncturing or symbol repetition based on a rate R=1/3 or 1/5 mode code, an operation of selecting a particular code rate from the supportable code rates is required. In FIG. 1, for example, the channel encoder 120 determines a code rate under the control of a controller 160. The coded bits are subject to rate matching in a rate matcher 130. Commonly, the rate matching is performed through repetition and/or puncturing on the coded bits, when a transport channel is subject to multiplexing or the output symbols of the channel encoder 120 are not identical in number to the symbols transmitted over the air. The puncturing or repetition function of the rate matcher 130 is identical to the puncturing or repetition function performed to adjust a code rate of the channel encoder 120, the functions can be united. That is, the channel encoder 120 and the rate matcher 130 can be integrated into one block, but they are separately illustrated in FIG. 1, for the sake of convenience. The coded bits rate-matched by the rate matcher 130 are subject to interleaving in an interleaver 140. The interleaving operation is performed to minimize a data loss even though data is lost during transmission. The interleaved coded bits are

subject to symbol mapping in a modulator 150 according to a modulation technique of QPSK (Quadrature Phase Shift Keying), 8PSK (8-ary Phase Shift Keying), 16QAM (16-ary Quadrature Amplitude Modulation) or 64QAM. The controller 160 controls a coding operation of the channel encoder 120 and a modulation technique of the modulator 150 according to a current state of a radio channel. In the HSDPA mobile communication system, AMCS (Adaptive Modulation and Coding Scheme) is used for the controller 160 in order to adaptively select one of the modulation techniques QPSK, 8PSK, 16QAM and 64QAM according to the radio environment.

Though not illustrated in the drawing, a CDMA mobile communication system spreads transmission data with a Walsh code W and a PN (Pseudo Noise) orthogonal code (PN) so that a corresponding UE (User Equipment), or a mobile terminal, can identify a channel over which the data is transmitted, and a Node B, or a base station, which transmits the data.

In the transmitter structure stated above, as a matter of course, systematic bits and parity bits output from the channel encoder 120 have different priorities. In other words, in the case where errors occur in transmission data at a certain rate, the transmission data can be decoded more correctly at a receiver when the errors occur in the parity bits, compared with when the errors occur in the systematic bits. The reason is because, as stated above, the systematic bits are the actual data bits, while the parity bits are the bits added to correct the transmission errors during decoding. For this, a symbol mapping (SMP) technique has been proposed, and the SMP technique is disclosed in Korean patent application No. 2001-17925, filed by the applicant on April 4, 2001 the contents of which are incorporated herein by reference.

The SMP technique is a technique for increasing system performance by reducing an error probability of the systematic bits having higher priority than

the parity bits. That is, the SMP technique enables the modulator 150 to map the systematic bits with higher priority to the bits with higher reliability among the bits constituting a symbol, and map the parity bits with lower priority to the bits with lower reliability, during symbol mapping based on a predetermined modulation technique. Therefore, in the transmitter of the conventional mobile communication system, it is necessary to improve the interleaver 140 which interleaves coded bits regardless of their priority. That is, in order to apply the SMP technique, the interleaver 140 must be improved such that it can separately interleave the systematic bits and the parity bits.

SUMMARY OF THE INVENTION

It is, therefore, an object of the present invention to provide a method for reducing complexity and securing compatibility with an existing algorithm in realizing an interleaver for a SMP technique.

It is another object of the present invention to provide a data transmission/reception apparatus and method for improving performance of a mobile communication system by realizing an SMP technique for differentially mapping reliabilities according to priority.

It is further another object of the present invention to provide a method for efficiently realizing SMP in a mobile communication system.

It is yet another object of the present invention to provide an algorithm for an interleaver in a mobile communication system.

It is still another object of the present invention to provide an apparatus for realizing SMP in a mobile communication system.

It is still another object of the present invention to provide an apparatus and method for reducing complexity in realizing SMP.

To achieve the above and other objects, the present invention provides a new method for realizing SMP with a minimized increase in complexity and minor modification of the algorithm, compared with an existing interleaving algorithm. Further, the present invention proposes a condition to which the method can be applied.

According to a first aspect of the present invention, the present invention provides a method for interleaving coded bits encoded at a prescribed code rate in a transmitter for a mobile communication system including a buffer having an area comprised of a plurality of rows and columns, for writing the coded bits. The method comprises separating the area of the buffer into a first write area and a second write area according to a ratio of coded bits with higher priority among the coded bits to coded bits with lower priority; sequentially writing a stream of the coded bits with higher priority in a row direction from a first column to a last column among the columns in the first write area, and sequentially writing a stream of the coded bits with lower priority in a row direction from a first column to a last column among the columns in the second write area; permuting the columns in the buffer area according to a given rule; dividing the rows in the buffer area into a first read area and a second read area having the same size; and alternately reading as many bits as a number determined based on a prescribed modulation technique from the first read area and the second read area in such a manner that the bits are sequentially read in a column direction from a first row to a last row among the rows of each of the first read area and the second read area.

According to a second aspect of the present invention, the present invention provides a method for interleaving coded bits encoded at a prescribed

code rate in a transmitter for a mobile communication system including a buffer having an area comprised of a plurality of rows and columns, for writing the coded bits. The method comprises separating the area of the buffer into a first write area and a second write area according to a ratio of coded bits with higher priority among the coded bits to coded bits with lower priority; sequentially writing a stream of the coded bits with higher priority in a row direction from a first column to a last column among the columns in the first write area, and sequentially writing a stream of the coded bits with lower priority in a row direction from a first column to a last column among the columns in the second write area; permuting the columns in the buffer area according to a given rule; dividing the rows in the buffer area into a first read area and a second read area having the same size; permuting, between the first read area and the second read area, as many rows as a number determined based on a prescribed modulation technique among the rows of each of the first read area and the second read area; and sequentially reading the rows in the entire buffer area comprised of the first read area and the second read area, in a column direction from a first row to a last row.

According to a third aspect of the present invention, the present invention provides a method for interleaving coded bits encoded at a prescribed code rate in a transmitter for a mobile communication system including a buffer having an area comprised of a plurality of rows and columns, for writing the coded bits. The method comprises separating the area of the buffer into a first write area and a second write area according to a ratio of coded bits with higher priority among the coded bits to coded bits with lower priority; sequentially writing a stream of the coded bits with higher priority in a row direction from a first column to a last column among the columns in the first write area, and writing a stream of the coded bits with lower priority in a row direction from a last column to a first column among the columns in the second write area in such a manner that the stream of coded bits is written in a reverse direction from a last

row to a first row in the second write area; permuting the columns in the buffer area according to a given rule; dividing the rows in the buffer area into a first read area and a second read area having the same size; and alternately reading as many bits as a number determined based on a prescribed modulation technique from the first read area and the second read area in such a manner that the bits are sequentially read in a column direction from a first row to a last row among the rows of each of the first read area and the second read area.

According to a fourth aspect of the present invention, the present invention provides a method for interleaving coded bits encoded at a prescribed code rate in a transmitter for a mobile communication system including a buffer having an area comprised of a plurality of rows and columns, for writing the coded bits. The method comprises separating the area of the buffer into a first write area and a second write area according to a ratio of coded bits with higher priority among the coded bits to coded bits with lower priority; sequentially writing a stream of the coded bits with higher priority in a row direction from a first column to a last column among the columns in the first write area, and writing a stream of the coded bits with lower priority in a row direction from a last column to a first column among the columns in the second write area in such a manner that the stream of coded bits is written in a reverse direction from a last row to a first row in the second write area; permuting the columns in the buffer area according to a given rule; dividing the rows in the buffer area into a first read area and a second read area having the same size; permuting, between the first read area and the second read area, as many rows as a number determined based on a prescribed modulation technique among the rows of each of the first read area and the second read area; and sequentially reading the rows in the entire buffer area comprised of the first read area and the second read area, in a column direction from a first row to a last row.

According to a fifth aspect of the present invention, the present invention

provides a method for interleaving coded bits encoded at a prescribed code rate in a transmitter for a mobile communication system including two buffers each having an area comprised of a plurality of rows and columns, for writing the coded bits. The method comprises writing coded bits with higher priority among the coded bits in a first buffer and writing coded bits with lower priority in a second buffer, in such a manner that a stream of the coded bits with higher priority is sequentially written in a row direction from a first column to a last column among the columns in the write area of the first buffer and a stream of the coded bits with lower priority is sequentially written in a row direction from a first column to a last column among the columns in the write area of the second buffer; permuting the columns of the write areas in the first buffer and the second buffer according to a given rule; and alternately reading as many bits as a number determined based on a prescribed modulation technique from the write area of the first buffer and the write area of the second buffer in such a manner that the bits are sequentially read in a column direction from a first row to a last row among the rows of the write areas in each of the first buffer and the second buffer.

According to a sixth aspect of the present invention, the present invention provides an apparatus for interleaving coded bits encoded at a prescribed code rate in a transmitter for a mobile communication system including an encoder for encoding transmission data into coded bits at the prescribed code rate, the coded bits including coded bits with higher priority and coded bits with lower priority, and a buffer having an area comprised of a plurality of rows and columns, for writing the coded bits. The apparatus comprises an interleaver for separating the area of the buffer included therein into a first write area and a second write area according to a ratio of the coded bits with higher priority to the coded bits with lower priority, sequentially writing a stream of the coded bits with higher priority in a row direction from a first column to a last column among the columns in the first write area, and sequentially writing a stream of the coded bits with lower priority in a row

direction from a first column to a last column among the columns in the second write area, and permuting the columns in the buffer area according to a given rule. Further, the apparatus comprises a multiplexer for dividing the rows in the buffer area into a first read area and a second read area having the same size, and alternately reading as many bits as a number determined based on a prescribed modulation technique from the first read area and the second read area in such a manner that the bits are sequentially read in a column direction from a first row to a last row among the rows of each of the first read area and the second read area, and multiplexing the read coded bits.

According to a seventh aspect of the present invention, the present invention provides an apparatus for interleaving coded bits encoded at a prescribed code rate in a transmitter for a mobile communication system including an encoder for encoding transmission data into coded bits at the prescribed code rate, the coded bits including coded bits with higher priority and coded bits with lower priority, and a buffer having an area comprised of a plurality of rows and columns, for writing the coded bits. The apparatus comprises an interleaver for separating the area of the buffer into a first write area and a second write area according to a ratio of coded bits with higher priority to coded bits with lower priority; sequentially writing a stream of the coded bits with higher priority in a row direction from a first column to a last column among the columns in the first write area, and sequentially writing a stream of the coded bits with lower priority in a row direction from a first column to a last column among the columns in the second write area; permuting the columns in the buffer area according to a given rule; dividing the rows in the buffer area into a first read area and a second read area having the same size; and permuting, between the first read area and the second read area, as many rows as a number determined based on a prescribed modulation technique among the rows of each of the first read area and the second read area.

According to an eighth aspect of the present invention, the present invention provides an apparatus for interleaving coded bits encoded at a prescribed code rate in a transmitter for a mobile communication system including an encoder for encoding transmission data into coded bits at the prescribed code rate, the coded bits including coded bits with higher priority and coded bits with lower priority, and a buffer having an area comprised of a plurality of rows and columns, for writing the coded bits. The apparatus comprises an interleaver for separating the area of the buffer into a first write area and a second write area according to a ratio of the coded bits with higher priority to the coded bits with lower priority, sequentially writing a stream of the coded bits with higher priority in a row direction from a first column to a last column among the columns in the first write area, and writing a stream of the coded bits with lower priority in a row direction from a last column to a first column among the columns in the second write area in such a manner that the stream of coded bits is written in a reverse direction from a last row to a first row in the second write area, and permuting the columns in the buffer area according to a given rule. Further, the apparatus comprises a multiplexer for dividing the rows in the buffer area into a first read area and a second read area having the same size, alternately reading as many bits as a number determined based on a prescribed modulation technique from the first write area and the second write area, and sequentially reading coded bits in a column direction from a first row to a last row among the rows in the first read area and the second read area, and multiplexing the read coded bits.

According to a ninth aspect of the present invention, the present invention provides an apparatus for interleaving coded bits encoded at a prescribed code rate in a transmitter for a mobile communication system including an encoder for encoding transmission data into coded bits at the prescribed code rate, the coded bits including coded bits with higher priority and coded bits with lower priority, and a buffer having an area comprised of a

plurality of rows and columns, for writing the coded bits. The apparatus comprises an interleaver for separating the area of the buffer into a first write area and a second write area according to a ratio of coded bits with higher priority to coded bits with lower priority; sequentially writing a stream of the coded bits with higher priority in a row direction from a first column to a last column among the columns in the first write area, and writing a stream of the coded bits with lower priority in a row direction from a last column to a first column among the columns in the second write area in such a manner that the stream of coded bits is written in a reverse direction from a last row to a first row in the second write area; permuting the columns in the buffer area according to a given rule; dividing the rows in the buffer area into a first read area and a second read area having the same size; and permuting, between the first read area and the second read area, as many rows as a number determined based on a prescribed modulation technique among the rows of each of the first read area and the second read area.

According to a tenth aspect of the present invention, the present invention provides an apparatus for interleaving coded bits encoded at a prescribed code rate in a transmitter for a mobile communication system including an encoder for encoding transmission data into coded bits at the prescribed code rate, the coded bits including coded bits with higher priority and coded bits with lower priority, and buffers each having an area comprised of a plurality of rows and columns, for writing the coded bits. The apparatus comprises an interleaver including a first buffer for sequentially writing a stream of the coded bits with higher priority in a row direction from a first column to a last column among the columns in the write area thereof, and a second buffer for sequentially writing a stream of the coded bits with lower priority in a row direction from a first column to a last column among the columns in the write area thereof, the interleaver permuting the columns of the write areas in the first buffer and the second buffer according to a given rule; and a multiplexer for

alternately reading as many bits as a number determined based on a prescribed modulation technique from the write area of the first buffer and the write area of the second buffer in such a manner that the bits are sequentially read in a column direction from a first row to a last row among the rows of the write areas in each of the first buffer and the second buffer, and multiplexing the read coded bits.

According to a eleventh aspect of the present invention, the present invention provides a method for deinterleaving coded bits demodulated by a prescribed demodulation technique in a receiver for a mobile communication system including a buffer having an area comprised of rows and columns, for writing the coded bits. The method comprises demultiplexing the coded bits at prescribed periods; separating a use area of the buffer into a first write area and a second write area having the same size; sequentially writing one demultiplexed output into the first write area and sequentially writing another demultiplexed output into the second write area; dividing the use area into a first read area and a second read area according to a ratio of coded bits with higher priority among the coded bits to coded bits with lower priority; and reading coded bits from the first read area and the second read area according to the ratio of the coded bits with higher priority to the coded bits with lower priority.

According to a twelfth aspect of the present invention, the present invention provides an apparatus for deinterleaving coded bits demodulated by a prescribed demodulation technique in a receiver for a mobile communication system including a buffer having an area comprised of rows and columns, for writing the coded bits. The apparatus comprises a deinterleaver for separating a use area of the buffer into a first write area and a second write area having the same size; sequentially writing one demultiplexed output into the first write area and sequentially writing another demultiplexed output into the second write area; dividing the use area into a first read area and a second read area according to a ratio of coded bits with higher priority among the coded bits to coded bits with

lower priority; and reading coded bits from the first read area and the second read area according to the ratio of the coded bits with higher priority to the coded bits with lower priority, and deinterleaving the read coded bits.

BRIEF DESCRIPTION OF THE DRAWINGS

The above and other objects, features and advantages of the present invention will become more apparent from the following detailed description when taken in conjunction with the accompanying drawings in which:

FIG. 1 is a block diagram illustrating a structure of a high-speed packet transmission system according to the prior art;

FIG. 2 is a block diagram illustrating a structure of a high-speed packet transmission system supporting SMP for differentially mapping reliabilities according to priority, according to an embodiment of the present invention;

FIG. 3 is a block diagram illustrating a process of mapping systematic bits and parity bits, applied in the same ratio to two physically separated interleaving buffers having a sufficient size, to a 16QAM or 64QAM-modulated symbol in the case where a code rate is 1/2, according to an embodiment of the present invention;

FIG. 4 is a block diagram illustrating a process of mapping systematic bits and parity bits, applied in a different ratio to two physically separated interleaving buffers having a sufficient size, to a 16QAM or 64QAM-modulated symbol in the case where a code rate is 3/4, according to an embodiment of the present invention;

FIG. 5 is a block diagram illustrating a process of mapping systematic bits and parity bits, applied in a different ratio to two physically separated interleaving buffers having a minimum size, to a 16QAM or 64QAM-modulated symbol in the case where a code rate is 3/4, according to an embodiment of the present invention;

FIG. 6 is a flowchart illustrating a process of applying an SMP technique

by physically separating an interleaver according to an embodiment of the present invention;

FIG. 7 is a block diagram illustrating a structure of a transmitter according to a first embodiment of the present invention;

FIGs. 8A and 8B illustrate examples of a writing process for a code rate 1/2 according to a first embodiment of the present invention;

FIGs. 9A and 9B illustrate examples of a writing process for a code rate 3/4 according to the first embodiment of the present invention;

FIGs. 10A to 10D illustrate examples of a writing process for a code rate 3/4, using dummy bits, according to the first embodiment of the present invention;

FIGs. 11A and 11B illustrate examples of a process of reading coded bits according to the first embodiment of the present invention;

FIG. 12 is a flowchart illustrating a process of applying an SMP technique by logically separating an interleaver according to the first embodiment of the present invention;

FIG. 13 is a block diagram illustrating a structure of a transmitter according to a second embodiment of the present invention;

FIGs. 14A and 14B illustrate examples of a writing process according to the second embodiment of the present invention;

FIGs. 15A and 15B illustrate examples of a read process according to the second embodiment of the present invention;

FIG. 16 is a flowchart illustrating a process of applying an SMP technique by logically separating an interleaver according to the second embodiment of the present invention;

FIG. 17 is a block diagram illustrating a structure of a receiver corresponding to the transmitter according to the first embodiment of the present invention;

FIG. 18 is a block diagram illustrating a structure of a receiver corresponding to the transmitter according to the second embodiment of the

present invention; and

FIG. 19 is a flowchart illustrating an operation of the receiver according to an embodiment of the present invention.

DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENT

A preferred embodiment of the present invention will be described herein below with reference to the accompanying drawings. In the following description, well-known functions or constructions are not described in detail since they would obscure the invention in unnecessary detail.

The present invention provides examples for an interleaver required for applying the SMP technique. Commonly, in a mobile communication system, an amount of (or the number of) systematic bits and the number of parity bits, mapped to each symbol, are different according to a code rate and a modulation technique. Therefore, in order to adjust the number of systematic bits and parity bits, an input of a modulator must be formed in a proper pattern according to the above condition. That is, an interleaver for applying the SMP technique must be improved such that it can separately interleave the systematic bits and the parity bits. There are several methods for realizing such an interleaver arranged in front of the modulator according to a given condition.

The method for improving an interleaver can be divided into one method for separating the interleaver physically and another method for separating the interleaver logically. The physical separation method separates the interleaver into an interleaver for interleaving coded bits with higher priority and an interleaver for interleaving coded bits with lower priority. The logical separation method separates a storage area of a buffer included in one interleaver into an area for storing coded bits with higher priority and an area for storing coded bits with lower priority.

1. Physical Separation Method

FIG. 2 illustrates a structure of a high-speed packet transmission system to which the SMP technique is applied using two physically-separated interleavers. The structure of FIG. 2 includes two physically-separated interleavers, and the systematic bits S and the parity bits P are separately interleaved by the different interleavers. To this end, an interleaving block includes a distributor 240, two interleavers 250 and 260, and a parallel-to-serial (P/S) converter 270.

Referring to FIG. 2, the distributor 240 properly distributes input coded bits to the two interleavers 250 and 260. For example, the distributor 240 distributes the bits with higher priority among the coded bits to the first interleaver 250, and the bits with lower priority to the second interleaver 260. In addition, if a code rate for encoding is asymmetric, the distributor 240 can uniformly distribute the coded bits to the first interleaver 250 and the second interleaver 260 according to priority of the coded bits and the code rate. Meanwhile, the first interleaver 250 and the second interleaver 260 separately interleave the coded bits distributed from the distributor 240, and provide the interleaved coded bits in parallel to the P/S converter 270. The P/S converter 270 converts the interleaved coded bits provided in parallel into serial data in the form of a proper bit stream according to a code rate and a modulation technique. To this end, the P/S converter 270 should be able to select the two inputs in series for a variable period according to the code rate and the modulation technique under the control of a controller.

Meanwhile, examples of applying the SMP technique using the two physically-separated interleavers are illustrated in FIGs. 3 to 5.

Referring to FIG. 3, in the case where a code rate is $1/2$, and the

systematic (S) bits and the parity (P) bits are properly distributed to the two interleavers 250 and 260, the systematic bits and the parity bits can be mapped to H positions with higher reliability and L positions with lower reliability of each symbol by a modulator 280, respectively. Here, the distributor 240 is optional, and the P/S converter 270 simply serves as a multiplexer (MUX).

Referring to FIG. 4, in the case where a code rate is 3/4, and the two interleavers 250 and 260 sufficiently receive the systematic bits and the parity bits, an output pattern of the modulator 280 can become optimal as described in conjunction with FIG. 3. Likewise, the distributor 240 in FIG. 4 is also optional. As illustrated in FIG. 4, since two patterns are required for 64QAM, the P/S converter 270 must control its operation according to a modulation order. For example, the P/S converter 270 outputs 1 parity bit per 5 systematic bits for an initial symbol, and outputs 2 parity bits for 4 systematic bits for the next symbol. For an operation proper to the modulation technique and the code rate, the P/S converter 270 plays an important role.

Referring to FIG. 5, in the case where a size of a first buffer 250 is smaller than the total number of systematic bits, a second buffer 260 must accept the excessive number of systematic bits. As illustrated, in the case of 16QAM, there is no output pattern which violates a general idea of SMP. However, in the case of 64QAM, some patterns are formed such that the systematic bits can be mapped to the bit positions having higher reliability than the parity bits. The reason is because after the input bits of the second buffer 260 are randomly interleaved, the P/S converter 270 cannot distinguish the systematic bits and the parity bits stored in the second buffer 260.

As can be understood from FIGs. 3 to 5, if the size of the buffer (buffer size = {the number of systematic bits} + {the number of parity bits}) is minimized, a symbol pattern for the 64QAM cannot be optimally mapped. In

other words, in the case where the interleaving buffer is physically separated, if a high-order modulation technique of 64QAM is applied, it is necessary to sufficiently increase the sizes of the two buffers for all code rates, in order to create optimal mapping patterns. However, in the case of the modulation technique with a modulation order of below 16QAM, the optimal mapping patterns can be generated even though the size of the buffer is minimized.

Herein, the present invention provides a method for minimizing a size of the buffer to minimize hardware complexity as described in conjunction with FIG. 5, in the case where the modulation technique with a modulation order of below 16QAM is used. In addition, the present invention provides a method for modifying the existing 3GPP Rel99 interleaving algorithm.

FIG. 6 is a flowchart illustrating a method for applying an SMP technique using physically-separated interleavers according to an embodiment of the present invention. With reference to FIG. 6, a method for applying the SMP technique using physically-separated interleavers will be described.

Referring to FIG. 6, a block interleaver with an inter-column permutation (or column permutation) function is used for interleaving. The interleaver receives $u_{p,1}, u_{p,2}, u_{p,3}, \dots, u_{p,U}$ (Step 612). Here, p represents the number of physical channels, and U represents the number of bits per frame of a physical channel.

(1) First, the total number of columns $C2$ is set to 30 (Step 614). The columns are assigned column numbers $0, 1, 2, \dots, C2-1$ from left to right.

(2) The minimum integer indicating a row of a matrix $R2$, satisfying a condition of $U \leq R2 \times C2$, is determined. The rows of the matrix are assigned row

numbers 0, 1, 2, ..., R2-1 from top to bottom (Step 616).

(3) The inputs $u_{p,1}$, $u_{p,2}$, $u_{p,3}$, ..., $u_{p,U}$ are written row by row in an $R2 \times C2$ rectangular matrix beginning at position $y_{p,1}$ in a 0th row and a 0th column (Step 618), in accordance with Equation (1).

Equation (1)

$$\begin{bmatrix} y_{p,1} & y_{p,2} & y_{p,3} & \cdots & y_{p,C2} \\ y_{p,(C2+1)} & y_{p,(C2+2)} & y_{p,(C2+3)} & \cdots & y_{p,(C2+C2)} \\ \vdots & \vdots & \vdots & \cdots & \vdots \\ y_{p,((R2-1) \times C2+1)} & y_{p,((R2-1) \times C2+2)} & y_{p,((R2-1) \times C2+3)} & \cdots & y_{p,(R2 \times C2)} \end{bmatrix}$$

Here, $y_{p,k} = u_{p,k}$ for $k = 1, 2, \dots, U$. If $R2 \times C2 > U$ (Step 620), then dummy bits of $y_{p,k} = 0$ or 1 (for $k = U+1, U+2, \dots, R2 \times C2$) are inserted (Step 622). The dummy bits are deleted (Step 626) after being subject to column permutation (Step 624).

(4) After the column permutation is performed according to a rule (Step 624), the resulting bits $y'_{p,k}$ are expressed as

Equation (2)

$$\begin{bmatrix} y'_{p,1} & y'_{p,(R2+1)} & y'_{p,(2 \times R2+1)} & \cdots & y'_{p,((C2-1) \times R2+1)} \\ y'_{p,2} & y'_{p,(R2+2)} & y'_{p,(2 \times R2+2)} & \cdots & y'_{p,((C2-1) \times R2+2)} \\ \vdots & \vdots & \vdots & \cdots & \vdots \\ y'_{p,R2} & y'_{p,(2 \times R2)} & y'_{p,(3 \times R2)} & \cdots & y'_{p,(C2 \times R2)} \end{bmatrix}$$

(5) Outputs of the block interleaver are read column by column from the column-permuted $R2 \times C2$ matrix (Step 628). The outputs are represented by $v_{p,1}$, $v_{p,2}$, $v_{p,3}$, ..., $v_{p,U}$.

However, in the normal SMP technique, since two interleavers are physically separated, a distributor for properly distributing systematic bits and parity bits, the number of which is variable according to the code rate, to the two interleavers is necessarily required. If the distributor is not provided, each of the interleavers must have a buffer capable of storing the entire input coded bits. The reason is because in a high-speed packet transmission system supporting an HARQ (Hybrid Automatic Retransmission Request) technique, only systematic bits or parity bits can be transmitted during retransmission when occasion demands.

Meanwhile, in the case where the two interleavers are physically separated, in order to convert outputs from each of the two separated interleavers into one bit stream, a serial-to-parallel (S/P) converter controlled by a control signal from an external device is necessarily required.

2. First Embodiment of Logical Separation Method

Now, a first embodiment for realizing the SMP technique by logically separating a buffer included in one interleaver will be described.

2.1 Structure of Transmitter According to First Embodiment

FIG. 7 illustrates a structure of a transmitter for realizing the SMP technique by logically separating a buffer included in one interleaver according to the first embodiment of the present invention.

Referring to FIG. 7, an interleaver 710 includes a buffer having a prescribed area therein. The prescribed area of the buffer means a partial area determined by the total number of coded bits received from an encoder (not shown). Hereinafter, the prescribed area determined by the total number of coded bits will be referred to as "use area" (or an area in use). The interleaver 710 divides the determined use area into two virtual write areas of a first write area

and a second write area according to a ratio of the bits with first priority (hereinafter, referred to as "systematic bits") to the bits with second priority (hereinafter, referred to as "parity bits"), constituting the coded bits. Here, the ratio of the systematic bits to the parity bits is determined depending on a code rate used by the encoder. For example, if the code rate is $1/2$, the use area is equally divided into two virtual write areas having the same size, and one of the two areas is defined as the first write area and the other area is defined as the second write area. FIGs. 8A and 8B illustrate an example of the interleaver 710 in which the first write area and the second write area are equal in size. However, if the code rate is $3/4$, the use area is equally divided into four areas having the same size, and three of the four areas are defined as a first write area and the remaining one area is defined as a second write area. FIGs. 9A and 9B illustrate an example of the interleaver 710 in which the first write area and the second write area are asymmetric in size. It is assumed in FIG. 7 that the interleaver 710 equally divides the use area into the first write area and the second write area, for the code rate $1/2$.

Upon receiving coded bits from the encoder, the interleaver 710 sequentially writes the systematic bits among the coded bits in the first write area, and sequentially writes the parity bits in the second write area. Here, the interleaver 710 inserts dummy bits into an area left over after writing the systematic bits in the first write area, and inserts the dummy bits into an area left over after writing the parity bits in the second write area. Exemplary methods of writing the systematic bits and exemplary methods of writing the parity bits are illustrated in FIGs. 8A to 10D.

After completion of writing the systematic bits and the parity bits in this manner, the interleaver 710 interleaves the coded bits including the dummy bits stored in the use area through column permutation. The column permutation permutes the coded bits in the use area column by column, so that the written

systematic bits are never mixed with the parity bits.

Further, the interleaver 710 equally divides the use area into a first read area and a second read area in order to read the written coded bits. Therefore, if the code rate is $1/2$, the first read area is identical to the first write area, and the second read area is identical to the second write area. Thus, only the systematic bits are previously written in the first read area, and only the parity bits are previously written in the second read area. However, if the code rate is $3/4$, the first write area includes the first read area and a part of the second read area, and the remaining part of the second read area becomes the second write area. Thus, only the systematic bits are previously written in the first read area, and the systematic bits and the parity bits are previously written in the second read area row by row.

After interleaving, the interleaver 710 sequentially reads the coded bits written in the first read area and the second read area. Exemplary methods of reading the coded bits from the first read area and the second read area are illustrated in FIGs. 11A and 11B. Herein, the column permutation operation and the reading operation for interleaving have been separately described. However, it would be obvious to those skilled in the art that the column permutation operation and the reading operation can be united into one operation by changing the order of reading.

The coded bits read from the first read area and the second read area of the interleaver 710, are provided to a multiplexer (MUX) 720. The MUX 720 multiplexes the coded bits from the first read area and the second read area in a prescribed ratio, and outputs one bit stream. The ratio for multiplexing the coded bits from the first read area and the coded bits from the second read area is determined depending on the modulation technique used by a modulator 730. For example, if the modulation technique is 16QAM, 4 coded bits are mapped to one

symbol. In this case, the MUX 720 multiplexes the 2 coded bits from the first read area and the 2 coded bits from the second read area, for each symbol.

The coded bits multiplexed by the MUX 720 are applied to the modulator 730. The modulator 730 performs symbol mapping on the multiplexed coded bits. For example, when using a modulation technique of 16QAM, the modulator 730 maps 2 coded bits read from the first read area to the bits with higher reliability (hereinafter, referred to as "first reliability") of a particular symbol. Further, the modulator 730 maps 2 coded bits read from the second read area to the bits with lower reliability (hereinafter, referred to as "second reliability") of the symbol.

As stated above, the present invention provides a method for interleaving the systematic bits and the parity bits by logically separating one interleaver, so that the modulator can perform symbol mapping by the SMP technique.

2.2 Writing of Coded Bits

A method of writing coded bits in the buffer included in the interleaver 710 according to an embodiment of the present invention can be divided into one case where dummy bits are used and another case where the dummy bits are not used. The dummy bits are used to fill an area left over after writing coded bits in the use area of the buffer, determined depending on the total number of the coded bits provided from the encoder. The dummy bits are deleted after being subject to column permutation for interleaving.

Before a description of the methods for writing the coded bits, a method for determining whether to use the dummy bits will be described.

Whether to use the dummy bits is determined according to whether the total number U of the coded bits received from the encoder is a multiple of the

total number $C2$ of columns constituting a buffer matrix for the use area. Here, the $C2$ can be previously determined according to a size of a buffer in the interleaver. Further, the total number $R2$ of rows, used to determine the use area, can be determined according to the total number U of the coded bits, as the $C2$ is previously determined. Therefore, the use area is determined by the product of the $C2$ and the $R2$ ($C2 \times R2$). In addition, whether to use the dummy bits can be determined by comparing the product of the $C2$ and the $R2$ with the U . For example, if a condition of $U = C2 \times R2$ is satisfied as the U is a multiple of the $C2$, then the dummy bits are not used. However, if a condition of $U < C2 \times R2$ is satisfied as the U is not a multiple ($R2$) of the $C2$, then the dummy bits are used.

2.2.1 No Dummy Bit Used

FIGs. 8A, 8B, 9A and 9B illustrate exemplary methods of writing coded bits in the interleaver 710 in the case where the dummy bits are not used. Specifically, FIGs. 8A and 8B illustrate a case where a code rate used by the encoder is $1/2$, and FIGs. 9A and 9B illustrate a case where a code rate used by the encoder is $3/4$.

First, a description will be made of a case where systematic bits and parity bits are received in the same ratio, as the code rate of the encoder is $1/2$.

FIG. 8A illustrates a method of writing the parity bits beginning at the end of the use area in the case where the code rate is $1/2$, and FIG. 8B illustrates a method of writing the parity bits beginning at the head of the second write area of the use area in the case where the code rate is $1/2$.

Referring to FIG. 8A, the use area, a part of the entire area for the buffer included in the interleaver 710, is determined depending on the total number U of coded bits received from the encoder. The use area is determined in such a manner

that if no remainder exists after dividing the U by the predefined $C2$, a quotient obtained by the division is defined as the total number $R2$ of rows. However, if a remainder exists after the division, the $R2$ is determined by adding 1 to the quotient. The use area can be defined as the sum of a first write area and a second write area illustrated in FIG. 8A, and the first write area and the second write area are determined by equally dividing the use area into two areas. In the writing method of FIG. 8A, it is not necessary to physically definitely separate the first write area and the second write area. The reason is because the systematic bits out of the coded bits are written beginning at the head of the use area (represented by black arrows), while the parity bits among the coded bits are written beginning at the end of the use area (represented by white arrows). In other words, the systematic bits are written in a forward direction beginning at $(0,0)$ of the use area, and the parity bits are written in a reverse direction beginning at $(R2-1, C2-1)$ of the use area. Here, $C2$ represents the total number of columns constituting a buffer matrix in the use area, and $R2$ represents the total number of rows constituting the buffer matrix in the use area. Therefore, when the coded bits are completely written in the use area, the first write area and the second write area can be naturally separated by the coded bits written therein.

Referring to FIG. 8B, the use area, a part of the entire area for the buffer included in the interleaver 710, is determined depending on the total number U of coded bits received from the encoder. The use area can be defined as the sum of a first write area and a second write area illustrated in FIG. 8B, and the first write area and the second write area are determined by equally dividing the use area into two areas. After the first write area and the second write area are determined, the systematic bits out of the coded bits are written beginning at the head of the first write area (represented by black arrows), and the parity bits out of the coded bits are written beginning at the head of the second write area (represented by white arrows). In other words, the systematic bits are written in a forward direction beginning at $(0,0)$ of the use area, and the parity bits are written in a

forward direction beginning at (y,z) of the use area. Here, since the code rate is $1/2$, $y=R2/2$ and $z=0$.

Next, a description will be made of a case where systematic bits and parity bits are received in a ratio of 3:1, as the code rate of the encoder is $3/4$.

FIG. 9A illustrates a method of writing the parity bits beginning at the end of the use area in the case where the code rate is $3/4$, and FIG. 9B illustrates a method of writing the parity bits beginning at the head of the second write area of the use area in the case where the code rate is $3/4$.

Referring to FIG. 9A, the use area, a part of the entire area for the buffer included in the interleaver 710, is determined depending on the total number U of coded bits received from the encoder. The use area is determined in such a manner that a quotient obtained by dividing the U by the predefined $C2$ is defined as $R2$. The use area can be defined as the sum of a first write area and a second write area illustrated in FIG. 9A. In the writing method of FIG. 9A, it is not necessary to physically definitely separate the first write area and the second write area. The reason is because the systematic bits out of the coded bits are written beginning at the head of the use area (represented by black arrows), while the parity bits out of the coded bits are written beginning at the end of the use area (represented by white arrows). In other words, the systematic bits are written in a forward direction beginning at (0,0) of the use area, and the parity bits are written in a reverse direction beginning at ($R2-1$, $C2-1$) of the use area. The systematic bits and the parity bits written in the use area are separated by a boundary point (y,z) between the first write area and the second write area. The (y,z), a boundary point between the first write area and the second write area, is a coordinate designating a particular point in the use area. If there exists a quotient or a remainder obtained by dividing the total number of systematic bits by the $C2$, the y is defined as a value determined by adding 1 to the quotient, and the z becomes

the remainder. Therefore, the first write area can be defined as an area from the (0,0) to the (y,z) of the use area, and the second write area can be defined as an area from the (y,z) to the (R2-1,C2-1) of the use area.

Referring to FIG. 9B, the use area, a part of the entire area for the buffer included in the interleaver 710, is determined depending on the total number U of coded bits received from the encoder. The use area can be defined as the sum of a first write area and a second write area illustrated in FIG. 9B. After the first write area and the second write area are determined, the systematic bits out of the coded bits are written beginning at the head of the first write area (represented by black arrows), and the parity bits out of the coded bits are written beginning at the head of the second write area, i.e., beginning at the (y,z) (represented by white arrows). In other words, the systematic bits are written in a forward direction beginning at (0,0) of the use area, and the parity bits are written in a forward direction beginning at (y,z) of the use area. As stated above, if there exists a quotient or a remainder obtained by dividing the total number of systematic bits by the C2, the y is defined as a value determined by adding 1 to the quotient, and the z becomes the remainder.

2.2.2 Dummy Bits Used

Although a method of writing the coded bits using the dummy bits will be described with reference to a code rate 3/4, it would be obvious to those skilled in the art that the same method can be applied even to a code rate 1/2.

As defined above, the dummy bits are used when there remains an empty area even after the systematic bits and the parity bits are completely written in the use area. That is, the dummy bits are used when the U is not a multiple of the C2. A method of inserting the dummy bits is realized in different ways according to a position in the use area, where the dummy bits are to be inserted. FIGs. 10A to 10D illustrate methods of writing the coded bits according to a position of the

dummy bits. The position of the dummy bits can be determined depending on a direction in which the parity bits are written in the second write area, and a write starting point of the parity bits.

FIG. 10A illustrates a method of writing coded bits in the case where the dummy bits are written in a reverse direction and a point shifted from an end of the second write area by the dummy bits is defined as a starting point. FIG. 10B illustrates a method of writing coded bits in the case where the dummy bits are written in a forward direction and a head of the second write area is defined as a starting point. FIG. 10C illustrates a method of writing coded bits in the case where the dummy bits are written in a reverse direction and an end of the second write area is defined as a starting point. FIG. 10D illustrates a method of writing coded bits in the case where the dummy bits are written in a forward direction and a point shifted from a head of the second write area by the dummy bits is defined as a starting point.

Referring to FIG. 10A, the use area, a part of the entire area for the buffer included in the interleaver 710, is determined depending on the total number U of coded bits received from the encoder. The use area can be defined as the sum of a first write area and a second write area illustrated in FIG. 10A. In the writing method of FIG. 10A where the dummy bits are located at the end of the second write area, it is not necessary to physically definitely separate the first write area and the second write area. The reason is because the systematic bits out of the coded bits are written beginning at the head of the use area (represented by black arrows), while the parity bits out of the coded bits are written beginning at the end of the use area (represented by white arrows). In other words, the systematic bits are written in a forward direction beginning at $(0,0)$ of the use area, and the parity bits are written in a reverse direction beginning at $(R2-1,x)$ of the use area. The x can be calculated by subtracting the number of the dummy bits from a column number corresponding to the $C2-1$.

Therefore, as stated above, the systematic bits and the parity bits written in the use area are separated by a boundary point (y,z) between the first write area and the second write area.

Referring to FIG. 10B, the systematic bits are written in the same way as described in the above methods. However, the parity bits are written in a forward direction beginning at a boundary (y,z) between the first write area and the second write area. Here, the (y,z) can be newly defined taking into account the dummy bits to be inserted. After the parity bits are completely written, the dummy bits are inserted in a remaining area existing at the end of the second write area.

Referring to FIG. 10C, the systematic bits are written in a forward direction beginning at the head of the first write area, and the parity bits are written in a reverse direction beginning at the end of the second write area. Thereafter, the dummy bits are inserted in an area left over after the systematic bits are written and an area left over after the parity bits are written.

Referring to FIG. 10D, the systematic bits are written in a forward direction beginning at the head of the first write area, and the parity bits are written in a forward direction beginning at an end of an area between a point where writing of the systematic bits is expected to be completed and a point where the dummy bits are to be inserted. Therefore, the dummy bits are inserted in a part of the first write area and a part of the second write area.

2.3 Reading of Coded Bits

The use area of a buffer in the interleaver 710, in which the coded bits are written, is separated into two virtual read areas for reading. The two read areas can be separated by equally dividing the use area into two areas with the same size. The interleaver 710 reads the coded bits written in the separated first

read area and second read area.

FIGs. 11A and 11B illustrate exemplary methods of reading coded bits from the first read area and the second read area by the interleaver 710. Specifically, FIG. 11A illustrates a method of reading the coded bits written at a code rate 1/2, and FIG. 11B illustrates a method of reading the coded bits written at a code rate 3/4.

Referring to FIGs. 11A and 11B, the interleaver 710 sequentially reads coded bits written in the first read area column by column. In addition, the interleaver 710 sequentially reads coded bits written in the second read area as well, column by column. As a result, in the case of FIG. 11A, only the systematic bits are read from the first read area and only the parity bits are read from the second read area. However, in the case of FIG. 11B, only the systematic bits are read from the first read area, and the systematic bits and the parity bits are read from second read area.

2.4 Operation of Transmitter According to First Embodiment

FIG. 12 is a flowchart illustrating an interleaving process according to the first embodiment of the present invention. That is, FIG. 12 illustrates a modified interleaving algorithm for separately writing and reading systematic bits and parity bits. It will be assumed herein that the writing operation is performed in the manner described in conjunction with FIG. 10A, for convenience.

Referring to FIG. 12, the interleaver receives U coded bits from an encoder (Step 1200). The coded bits are represented by $u_{p,1}, u_{p,2}, u_{p,3}, \dots, u_{p,U_s}$ and $u_{p,U_s+1}, u_{p,U_s+2}, u_{p,U_s+3}, \dots, u_{p,U_s+U_p}$. Here, p represents a physical channel number, and U_s and U_p represent the number of systematic bits and the number of parity

bits, respectively. The sum of the U_s and U_p is equal to the number of bits per frame of one physical channel.

(1) First, the total number of columns $C2$ is set to 30. The columns are assigned column numbers 0, 1, 2, ..., $C2-1$ from left to right. The minimum integer indicating a row of a matrix $R2$, satisfying a condition of $U_s + U_p \leq R2 \times C2$, is determined (Step 1202). The rows of the matrix are assigned row numbers 0, 1, 2, ..., $R2-1$ from top to bottom (Step 1204).

(2) The inputs $u_{p,1}, u_{p,2}, u_{p,3}, \dots, u_{p,U_s}$ are written in a forward direction row by row in an $R2 \times C2$ rectangular matrix beginning at $y_{p,1}$ in a 0th row and a 0th column, and the inputs $u_{p,U_s+1}, u_{p,U_s+2}, u_{p,U_s+3}, \dots, u_{p,U_s+U_p}$ are written in a reverse direction row by row beginning at a point in an $(R2-1)^{th}$ row and a $(x-1)^{th}$ column (Step 1206). Here, x means a remainder obtained by dividing the U by the $C2$, and is larger than or equal to 1 and smaller than $C2$ ($1 \leq x < C2$). Equation (3) shows an example of the matrix generated in this manner.

Equation (3)

$$\begin{bmatrix} y_{p,1} & y_{p,2} & y_{p,3} & \dots & y_{p,C2} \\ y_{p,(C2+1)} & y_{p,(C2+2)} & y_{p,(C2+3)} & \dots & y_{p,(2 \times C2)} \\ \vdots & \vdots & \vdots & \dots & \vdots \\ y_{p,(R2-1) \times C2+1} & y_{p,(R2-1) \times C2+2} & y_{p,(R2-1) \times C2+3} & \dots & y_{p,R2 \times C2} \end{bmatrix}$$

Here, $y_{p,k} = u_{p,k}$ for $k = 1, 2, \dots, U$. If $R2 \times C2 > U$ (Step 1208), then dummy bits of $y_{p,k} = 0$ or 1 (for $k = U+1, U+2, \dots, R2 \times C2$) are inserted (Step 1210). The dummy bits are deleted (Step 1214) after being subject to column permutation (Step 1212).

(3) After the column permutation is performed according to a rule (Step

1212), the resulting bits are divided into an H part with higher reliability and an L part with lower reliability, and expressed with $y_{p,k}^H$ and $y_{p,k}^L$, as follows.

Equation (4)

$$\begin{bmatrix} y_{p,1}^H & y_{p,(R/2+1)}^H & y_{p,R/2+1}^H & \cdots & y_{p,(C/2-1) \times R/2+1}^H \\ y_{p,2}^H & y_{p,(R/2+2)}^H & y_{p,R/2+2}^H & \cdots & y_{p,(C/2-1) \times R/2+2}^H \\ \vdots & \vdots & \vdots & \cdots & \vdots \\ y_{p,N/2}^H & y_{p,R/2}^H & y_{p,N/2}^H & \cdots & y_{p,(C/2-1) \times R/2}^H \\ y_{p,1}^L & y_{p,(R/2+1)}^L & y_{p,R/2+1}^L & \cdots & y_{p,(C/2-1) \times R/2+1}^L \\ y_{p,2}^L & y_{p,(R/2+2)}^L & y_{p,R/2+2}^L & \cdots & y_{p,(C/2-1) \times R/2+2}^L \\ \vdots & \vdots & \vdots & \cdots & \vdots \\ y_{p,N/2}^L & y_{p,R/2}^L & y_{p,N/2}^L & \cdots & y_{p,(C/2-1) \times R/2}^L \end{bmatrix}$$

(4) Outputs of the block interleaver are read by two bits column by column by equally dividing the column-permuted $R \times C/2$ matrix into a part with higher reliability and a part with lower reliability (Step 1216). The outputs are represented by $v_{p,1}, v_{p,2}, v_{p,3}, \dots, v_{p,1/2}$.

3. Second Embodiment of Logical Separation Method

FIG. 13 illustrates a structure of a transmitter for realizing the SMP technique by logically separating a buffer included in one interleaver according to a second embodiment of the present invention.

Referring to FIG. 13, an interleaver 1310 includes a buffer having a prescribed area therein. The prescribed area of the buffer defines a use area determined by the total number of coded bits received from an encoder (not shown). The interleaver 1310 divides the use area into a first write area and a second write area according to a ratio of systematic bits to parity bits, constituting the coded bits. Here, the ratio of the systematic bits to the parity bits is determined depending on a code rate used by the encoder. It is assumed in FIG.

13 that the interleaver 1310 is designed to support a code rate $1/2$.

Upon receiving coded bits from the encoder, the interleaver 1310 sequentially writes the systematic bits among the coded bits in the first write area, and sequentially writes the parity bits in the second write area. Here, the interleaver 1310 inserts dummy bits into an area left over after writing the systematic bits in the first write area, and inserts the dummy bits into an area left over after writing the parity bits in the second write area.

After completion of writing the systematic bits and the parity bits in this manner, the interleaver 1310 interleaves the coded bits including the dummy bits stored in the use area through column permutation. The column permutation permutes the coded bits in the use area column by column, so that the written systematic bits are never mixed with the written parity bits. After the column permutation, the interleaver 1310 permutes lower half columns among rows constituting the first write area with upper half columns among rows constituting the second write area. As a result, the coded bits written in the first write area and

the second write area can be properly read in the form of a bit stream according to the SMP technique. Examples of the inter-row permutation (or row permutation) are illustrated in FIGs. 14A and 14B. Specifically, FIG. 14A illustrates row permutation for a code rate $1/2$, and FIG. 14B illustrates row permutation for a code rate $3/4$.

Thereafter, the interleaver 1310 sequentially reads the written coded bits. Exemplary methods of reading the coded bits by the interleaver 1310 are illustrated in FIGs. 15A and 15B. Specifically, FIG. 15A illustrates a method for reading the coded bits in the case where the code rate $1/2$ is used, and FIG. 15B illustrates a method for reading the coded bits in the case where the code rate $3/4$ is used.

Herein, the column permutation operation and the reading operation for interleaving have been separately described. However, it would be obvious to those skilled in the art that the column permutation operation and the reading operation can be united into one operation by changing the order of reading.

As stated above, the coded bits read by the interleaver 1310 have a format required for applying the SMP technique. Therefore, the coded bits output from the interleaver 1310 are provided to a modulator 1320, where they are subject to symbol mapping by the SMP technique.

As described above, the present invention interleaves systematic bits and parity bits by logically separating one interleaver so that a modulator can perform symbol mapping by the SMP technique. Further, in order to exclude the MUX used in the first embodiment, it is necessary to modify a Rel99 reading algorithm. That is, the MUX can be excluded, if the algorithm is changed such that the coded bits written in the two write areas should be read by two bits. In other words, in the case of logically separated interleaving buffers, it is possible to exclude a hardware device for the MUX by simply modifying the reading algorithm in the above-stated manner. A novel algorithm which will be described herein below includes modification of the reading algorithm. In addition, in the case where R2 of a buffer matrix is a multiple of 4, it is possible to realize the existing reading algorithm for reading the entire buffer in the interleaver, through row permutation in stead of using the MUX.

FIGs. 15A and 15B illustrate symbol patterns of a modulator based on the row permutation, for the code rates 1/2 and 3/4, respectively. Referring to FIGs. 15A and 15B, both patterns do not violate an idea of the SMP technique that differentially maps reliabilities according to priority. When an extended amount of actual data is applied, it is possible to obtain the same result as the result obtained by the first embodiment.

FIG. 16 is a flowchart illustrating an interleaving process according to the second embodiment of the present invention. Referring to FIG. 16, a block interleaver with a column permutation function is used for interleaving. The interleaver receives $u_{p,1}$, $u_{p,2}$, $u_{p,3}$, ..., u_{p,U_s} and u_{p,U_s+1} , u_{p,U_s+2} , u_{p,U_s+3} , ..., u_{p,U_s+U_p} (Step 1600). Here, p represents a physical channel number, and U_s and U_p represent the number of systematic bits and the number of parity bits, respectively. The sum of the U_s and U_p is equal to the number of bits per frame of one physical channel.

(1) First, the total number of columns $C2$ is set to 30. The columns are assigned column numbers 0, 1, 2, ..., $C2-1$ from left to right. The minimum integer indicating a row of a matrix $R2$, satisfying a condition of $U=U_s+U_p \leq R2 \times C2$, is determined (Step 1602). The rows of the matrix are assigned row numbers 0, 1, 2, ..., $R2-1$ from top to bottom (Step 1604).

(2) The inputs $u_{p,1}$, $u_{p,2}$, $u_{p,3}$, ..., u_{p,U_s} are written in a forward direction row by row in an $R2 \times C2$ rectangular matrix beginning at $y_{p,1}$ in a 0th row and a 0th column, and the inputs u_{p,U_s+1} , u_{p,U_s+2} , u_{p,U_s+3} , ..., u_{p,U_s+U_p} are written in a reverse direction row by row beginning at a point in an $(R2-1)$ th row and a $(x-1)$ th column (Step 1606). Here, x means a remainder obtained by dividing the U by the $C2$, and is larger than or equal to 1 and smaller than $C2$ ($1 \leq x < C2$). Equation (5) shows an example of the matrix generated in this manner.

Equation (5)

$$\begin{bmatrix} y_{p,1} & y_{p,2} & y_{p,3} & \cdots & y_{p,C2} \\ y_{p,(C2+1)} & y_{p,(C2+2)} & y_{p,(C2+3)} & \cdots & y_{p,(2 \times C2)} \\ \vdots & \vdots & \vdots & \cdots & \vdots \\ y_{p,((R2-1) \times C2+1)} & y_{p,((R2-1) \times C2+2)} & y_{p,((R2-1) \times C2+3)} & \cdots & y_{p,(R2 \times C2)} \end{bmatrix}$$

Here, $y_{p,k} = u_{p,k}$ for $k = 1, 2, \dots, U$. If $R2 \times C2 > U$ (Step 1608), then dummy bits of $y_{p,k} = 0$ or 1 (for $k = U+1, U+2, \dots, R2 \times C2$) are inserted (Step 1610).

(3) After the column permutation is performed according to a rule (Step 1612), the resulting bits are divided into an H part with higher reliability and an L part with lower reliability, and expressed with $y_{p,k}^H$ and $y_{p,k}^L$, as follows.

Equation (6)

$$\begin{bmatrix} y_{p,1}^H & y_{p,(R2/2+1)}^H & y_{p,R2+1}^H & \dots & y_{p,((C2-1) \times R2/2+1)}^H \\ y_{p,2}^H & y_{p,(R2/2+2)}^H & y_{p,R2+2}^H & \dots & y_{p,((C2-1) \times R2/2+2)}^H \\ \vdots & \vdots & \vdots & \dots & \vdots \\ y_{p,R2/2}^H & y_{p,R2}^H & y_{p,3 \times R2/2}^H & \dots & y_{p,(C2 \times R2/2)}^H \\ y_{p,1}^L & y_{p,(R2/2+1)}^L & y_{p,R2+1}^L & \dots & y_{p,((C2-1) \times R2/2+1)}^L \\ y_{p,2}^L & y_{p,(R2/2+2)}^L & y_{p,R2+2}^L & \dots & y_{p,((C2-1) \times R2/2+2)}^L \\ \vdots & \vdots & \vdots & \dots & \vdots \\ y_{p,R2/2}^L & y_{p,R2}^L & y_{p,3 \times R2/2}^L & \dots & y_{p,(C2 \times R2/2)}^L \end{bmatrix}$$

(4) Rows with lower reliability are permuted with rows with higher reliability so that rows with higher reliability bits and rows with lower reliability bits should be repeated by two rows, as follows (Step 1614). The dummy bits are deleted (Step 1616) after being subject to row column permutation (Step 1614).

Equation (7)

$$\begin{bmatrix}
 Y_{p,1}^H & Y_{p,(R2/2+1)}^H & Y_{p,R2+1}^H & \cdots & Y_{p,((C2-1) \times R2/2+1)}^H \\
 Y_{p,2}^H & Y_{p,(R2/2+2)}^H & Y_{p,R2+2}^H & \cdots & Y_{p,((C2-1) \times R2/2+2)}^H \\
 Y_{p,1}^L & Y_{p,(R2/2+1)}^L & Y_{p,R2+1}^L & \cdots & Y_{p,((C2-1) \times R2/2+1)}^L \\
 Y_{p,2}^L & Y_{p,(R2/2+2)}^L & Y_{p,R2+2}^L & \cdots & Y_{p,((C2-1) \times R2/2+2)}^L \\
 \vdots & \vdots & \vdots & \cdots & \vdots \\
 Y_{p,R2/2-1}^H & Y_{p,R2-1}^H & Y_{p,3 \times R2/2-1}^H & \cdots & Y_{p,(C2 \times R2/2-1)}^H \\
 Y_{p,R2/2}^H & Y_{p,R2}^H & Y_{p,3 \times R2/2}^H & \cdots & Y_{p,(C2 \times R2/2)}^H \\
 Y_{p,R2/2-1}^L & Y_{p,R2-1}^L & Y_{p,3 \times R2/2-1}^L & \cdots & Y_{p,(C2 \times R2/2-1)}^L \\
 Y_{p,R2/2}^L & Y_{p,R2}^L & Y_{p,3 \times R2/2}^L & \cdots & Y_{p,(C2 \times R2/2)}^L
 \end{bmatrix}$$

(5) Outputs of the block interleaver are read column by column from the column-permuted, row-permuted $R2 \times C2$ matrix (Step 1618). The outputs are represented by $v_{p,1}, v_{p,2}, v_{p,3}, \dots, v_{p,13}$.

3. Receiver According to Invention

Now, a description will be made of a receiver corresponding to the transmitter that realizes the SMP technique by logically separating a buffer included in one interleaver. The receiver has a symmetrical structure of the transmitter illustrated in FIG. 2. A deinterleaver for the receiver is illustrated in FIGs. 17 and 18.

Since a received signal is in the form of a symbol modulated by a modulator in the transmitter, the received signal is first demodulated by a demodulator and then provided to a deinterleaver. The deinterleaver has a symmetrical structure of the interleaver illustrated in FIG. 2. The serial input bits must be converted to parallel bits, so that they can be written in upper and lower areas of the interleaving buffer. The logically separated buffers perform deinterleaving in a reverse operation of the interleaver, and a distributor distributes the output bits into systematic bits and parity bits. A rate matcher determines positions of the bits rate-matched by the transmitter and inserts 0's in the determined positions, so that other bits can be applied to a proper input

terminal of the demodulator. The demodulator, a device for decoding the bits encoded by an encoder in the transmitter, corrects errors occurring on a channel. The error-corrected output undergoes CRC checking by a CRC checker in order to determine whether the transmitted signal is correctly received. If an error is detected, the receiver sends a retransmission request to the transmitter. Since a high-speed packet transmission system uses various modulation orders and code rates, each element is controlled by a controller.

3.1 Structure of Receiver According to First Embodiment

FIG. 17 illustrates a structure of a receiver according to a first embodiment of the present invention. The receiver corresponds to the transmitter described in conjunction with FIG. 7.

Referring to FIG. 17, data bits decoded by a demodulator 1710 are demultiplexed by a demultiplexer (DEMUX) 1720. The DEMUX 1720 demultiplexes as many input bits as a prescribed number according to a modulation technique, and provides the demultiplexed bits to a first write area and a second write area in a buffer 1730 of the deinterleaver. For example, if the modulation technique is 16QAM, the DEMUX 1720 provides the input bits by 2 bits to each of the first and second write areas in the buffer 1730. However, if the modulation technique is 64QAM, the DEMUX 1720 provides the input bits by 3 bits to each of the first and second write areas.

If the code rate is $1/2$, systematic bits and parity bits are separately provided to the first and second write areas. However, if the code rate is $3/4$, only the systematic bits are provided to the first write area, and the systematic bits and parity bits are provided to the second write area.

The data bits written in the buffer 1730 of the deinterleaver are deinterleaved in a reverse operation of the interleaver, separately generating the

systematic bits and the parity bits.

3.2 Structure of Receiver According to Second Embodiment

FIG. 18 illustrates a structure of a receiver according to the second embodiment of the present invention. The receiver corresponds to the transmitter described in conjunction with FIG. 13.

Referring to FIG. 18, data bits decoded by a demodulator 1810 are provided to a first write area and a second write area in a buffer 1820 of the deinterleaver, without being demultiplexed by a demultiplexer. As described in conjunction with FIG. 13, since the coded bits stored in the buffer 1310 are subject to row permutation in the interleaving process, the transmitter performs multiplexing through a prescribed reading method, without a multiplexer. Likewise, the receiver also can perform deinterleaving without a demultiplexing process, by performing row permutation on the received bits.

For example, if the modulation technique is 16QAM, the bits written in the buffer 1820 undergo row permutation by two rows between the first write area and the second write area. However, if the modulation technique is 64QAM, the bits written in the buffer 1820 undergo row permutation by three rows between the first write area and the second write area.

The data bits written in the buffer 1820 of the deinterleaver are deinterleaved in a reverse operation of the interleaver, separately generating the systematic bits and the parity bits.

When the interleaver is logically separated, the deinterleaver has the structures illustrated in FIGs. 17 and 18, based on a deinterleaving algorithm proposed by the present invention. The deinterleaving algorithm is illustrated in FIG. 19.

3.3 Operation of Receiver According to Invention

FIG. 19 is a flowchart illustrating a deinterleaving process according to an embodiment of the present invention. The deinterleaving process is performed somewhat differently according to the interleaving processes performed by the interleaver in the transmitter. In order to finally create the original systematic bits and parity bits, the received bits are deinterleaved in a method corresponding to each method performed by the transmitter.

With reference to FIG. 19, a description will be made of an operation of the deinterleaver in the receiver according to an embodiment of the present invention. The deinterleaver receives $u_{p,1}$, $u_{p,2}$, $u_{p,3}$, ..., u_{p,U_s} and u_{p,U_s+1} , u_{p,U_s+2} , u_{p,U_s+3} , ..., u_{p,U_s+U_p} (Step 1900).

(1) First, the total number of columns C2 is set to 30. The columns are assigned column numbers 0, 1, 2, ..., C2-1 from left to right. The minimum integer indicating a row of a matrix R2, satisfying a condition of $U=U_s+U_p \leq R2 \times C2$, is determined (Step 1902). The rows of the matrix are assigned row numbers 0, 1, 2, ..., R2-1 from top to bottom (Step 1904).

(2) The inputs $u_{p,1}$, $u_{p,2}$, $u_{p,3}$, ..., u_{p,U_s} are written in a forward direction row by row in an $R2 \times C2$ rectangular matrix beginning at $y_{p,1}$ in a 0th row and a 0th column, and the inputs u_{p,U_s+1} , u_{p,U_s+2} , u_{p,U_s+3} , ..., u_{p,U_s+U_p} are written in a reverse direction row by row beginning at a point in an $(R2-1)$ th row and a $(x-1)$ th column (Step 1906). Here, x means a remainder obtained by dividing the U by the C2, and is larger than or equal to 1 and smaller than C2 ($1 \leq x < C2$). If $R2 \times C2 > U$ (Step 1908), then dummy bits of $y_{p,k} = 0$ or 1 (for $k = U+1, U+2, \dots, R2 \times C2$) are inserted (Step 1910). The dummy bits are deleted (Step 1914) after being subject to column permutation (Step 1912).

($\oplus 5$) 03-224615 (P2003-15)

(3) After the column permutation is performed according to a rule (Step 1912), the resulting bits are divided into a systematic bit (S) part and a parity bit (P) part.

(4) Outputs of the deinterleaver are read by two bits column by column, by dividing the column-permuted $R2 \times C2$ matrix into a systematic bit part and a parity bit part (Step 1916).

As described above, the present invention provides a method for efficiently performing interleaving in mapping the bits with higher priority to the position with higher reliability of a symbol, thereby preventing an increase in hardware complexity and maintaining compatibility with an existing interleaving technique. Since the SMP technique for differentially mapping reliabilities according to priority shows theoretically sufficient effects, it is very important to realize the SMP technique. The present invention, when applied to a high-speed packet transmission system, especially HSDPA or 1xEV-DV system, can be realized through minor modification of an algorithm and minor addition of hardware, while maintaining its gain.

While the invention has been shown and described with reference to a certain preferred embodiment thereof, it will be understood by those skilled in the art that various changes in form and details may be made therein without departing from the spirit and scope of the invention as defined by the appended claims.

4 Brief Description of Drawings

FIG. 1 is a block diagram illustrating a structure of a high-speed packet transmission system according to the prior art;

FIG. 2 is a block diagram illustrating a structure of a high-speed packet transmission system supporting SMP for differentially mapping reliabilities according to priority, according to an embodiment of the present invention;

FIG. 3 is a block diagram illustrating a process of mapping systematic bits and parity bits, applied in the same ratio to two physically separated interleaving buffers having a sufficient size, to a 16QAM or 64QAM-modulated symbol in the case where a code rate is $1/2$, according to an embodiment of the present invention;

FIG. 4 is a block diagram illustrating a process of mapping systematic bits and parity bits, applied in a different ratio to two physically separated interleaving buffers having a sufficient size, to a 16QAM or 64QAM-modulated symbol in the case where a code rate is $3/4$, according to an embodiment of the present invention;

FIG. 5 is a block diagram illustrating a process of mapping systematic bits and parity bits, applied in a different ratio to two physically separated interleaving buffers having a minimum size, to a 16QAM or 64QAM-modulated symbol in the case where a code rate is $3/4$, according to an embodiment of the present invention;

FIG. 6 is a flowchart illustrating a process of applying an SMP technique by physically separating an interleaver according to an embodiment of the present invention;

FIG. 7 is a block diagram illustrating a structure of a transmitter according to a first embodiment of the present invention;

FIGs. 8A and 8B illustrate examples of a writing process for a code rate $1/2$ according to a first embodiment of the present invention;

FIGs. 9A and 9B illustrate examples of a writing process for a code rate $3/4$ according to the first embodiment of the present invention;

FIGs. 10A to 10D illustrate examples of a writing process for a code rate $3/4$, using dummy bits, according to the first embodiment of the present invention;

FIGs. 11A and 11B illustrate examples of a process of reading coded bits according to the first embodiment of the present invention;

FIG. 12 is a flowchart illustrating a process of applying an SMP technique by logically separating an interleaver according to the first embodiment of the present invention;

FIG. 13 is a block diagram illustrating a structure of a transmitter according to a second embodiment of the present invention;

FIGs. 14A and 14B illustrate examples of a writing process according to the second embodiment of the present invention;

FIGs. 15A and 15B illustrate examples of a read process according to the second embodiment of the present invention;

FIG. 16 is a flowchart illustrating a process of applying an SMP technique by logically separating an interleaver according to the second embodiment of the present invention;

FIG. 17 is a block diagram illustrating a structure of a receiver corresponding to the transmitter according to the first embodiment of the present invention;

FIG. 18 is a block diagram illustrating a structure of a receiver corresponding to the transmitter according to the second embodiment of the present invention; and

FIG. 19 is a flowchart illustrating an operation of the receiver according to an embodiment of the present invention.

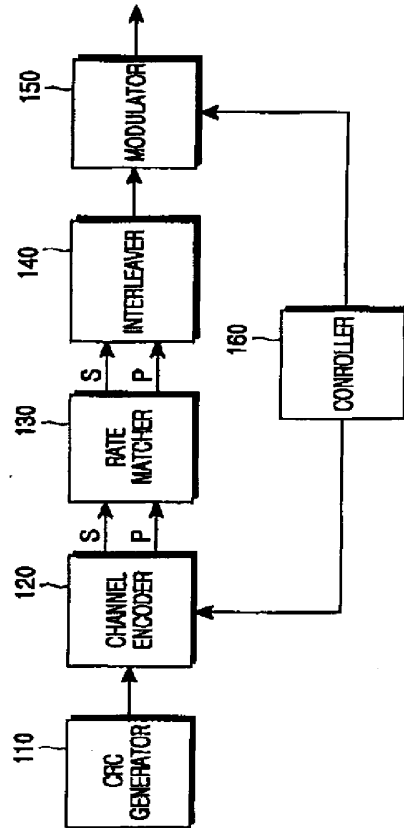


FIG.1

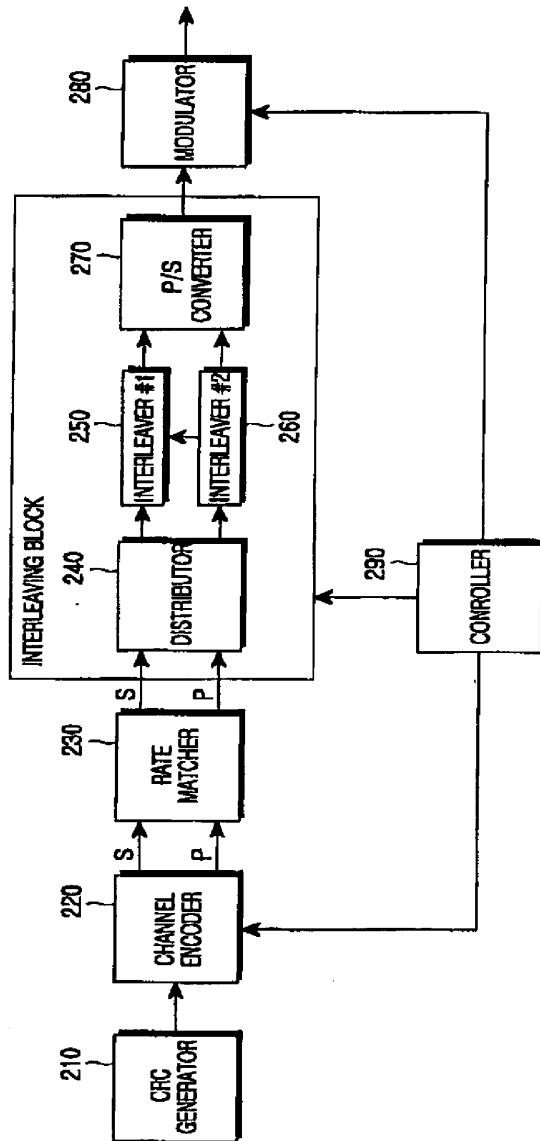


FIG.2

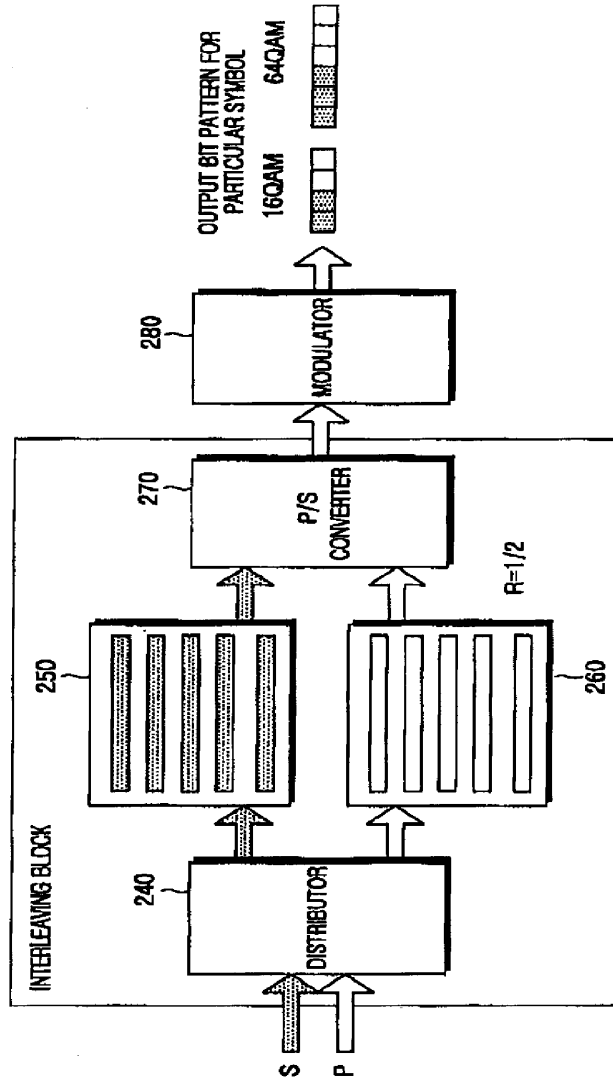


FIG.3

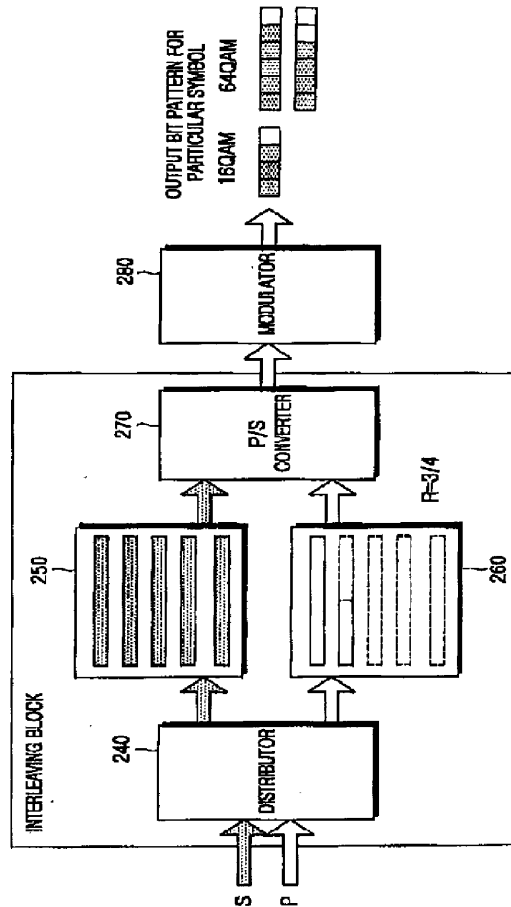


FIG. 4

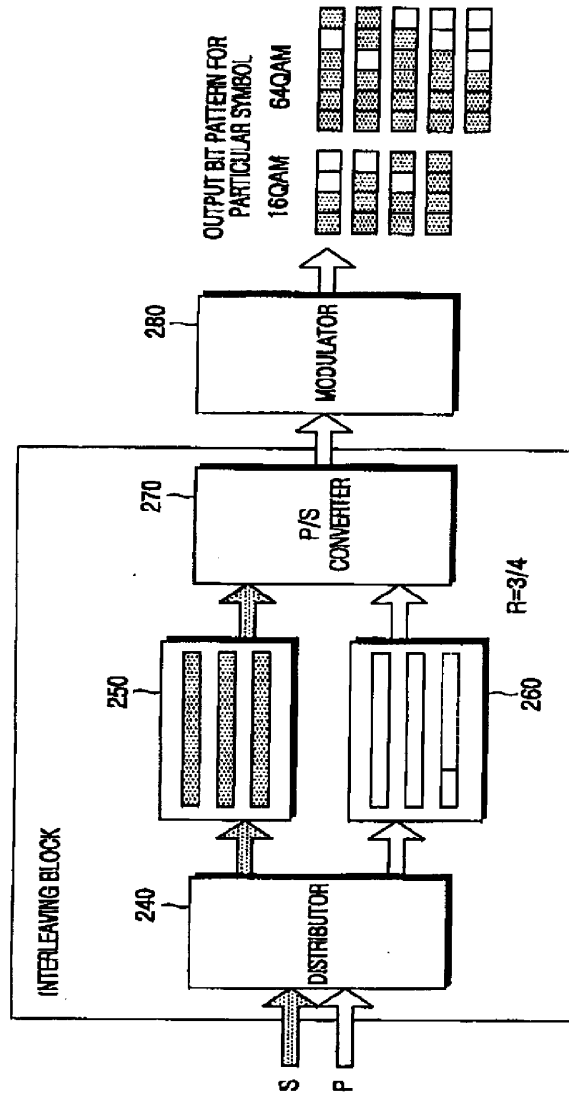


FIG.5

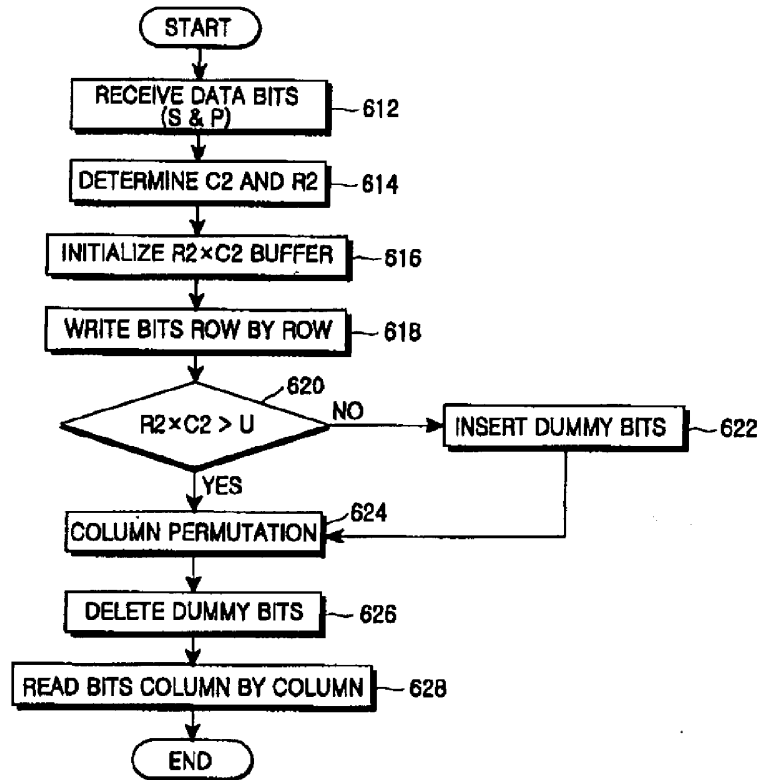


FIG.6

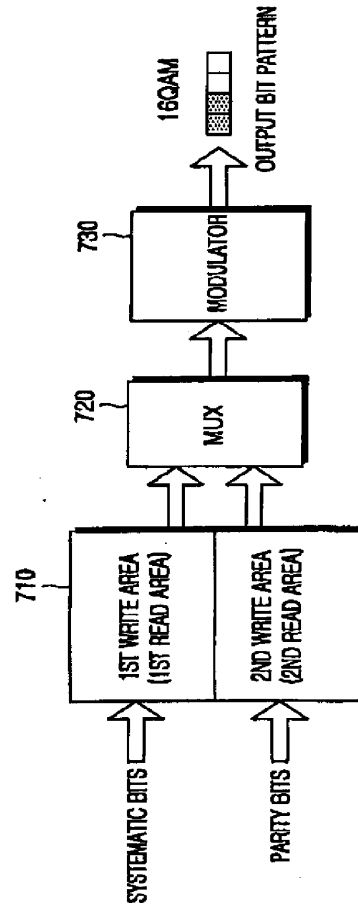


FIG.7

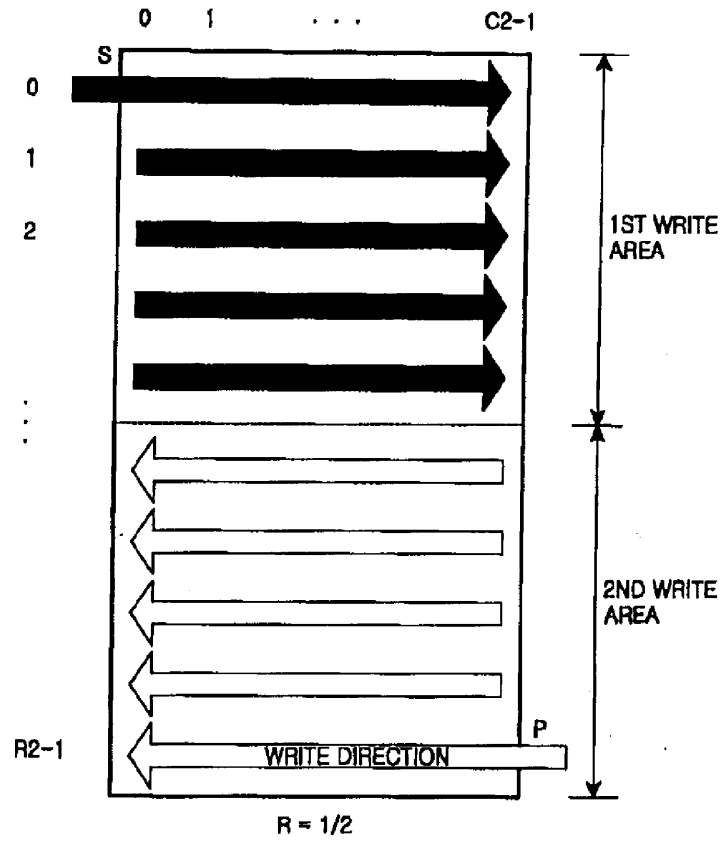


FIG.8A

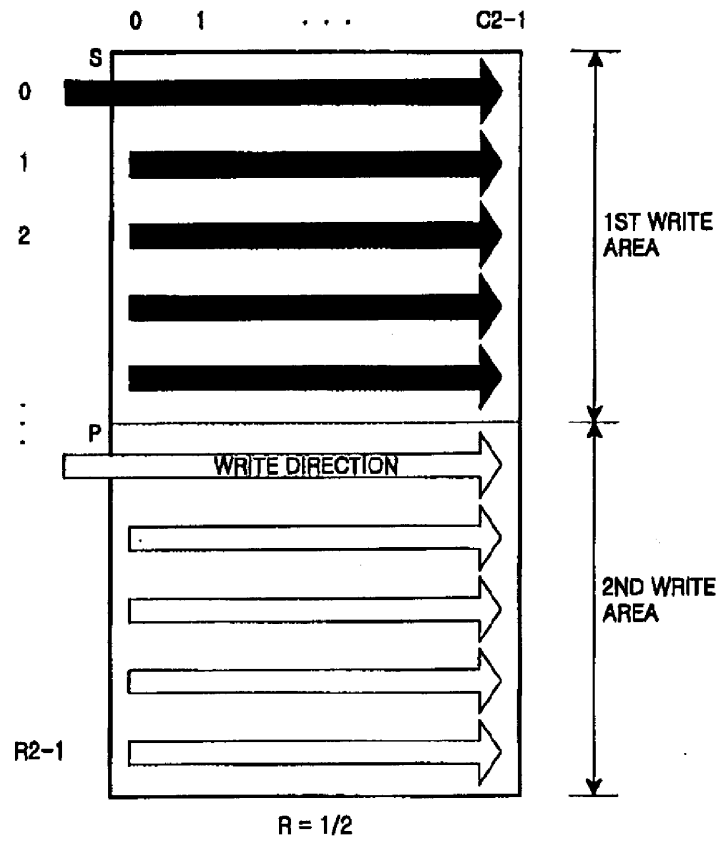


FIG.8B

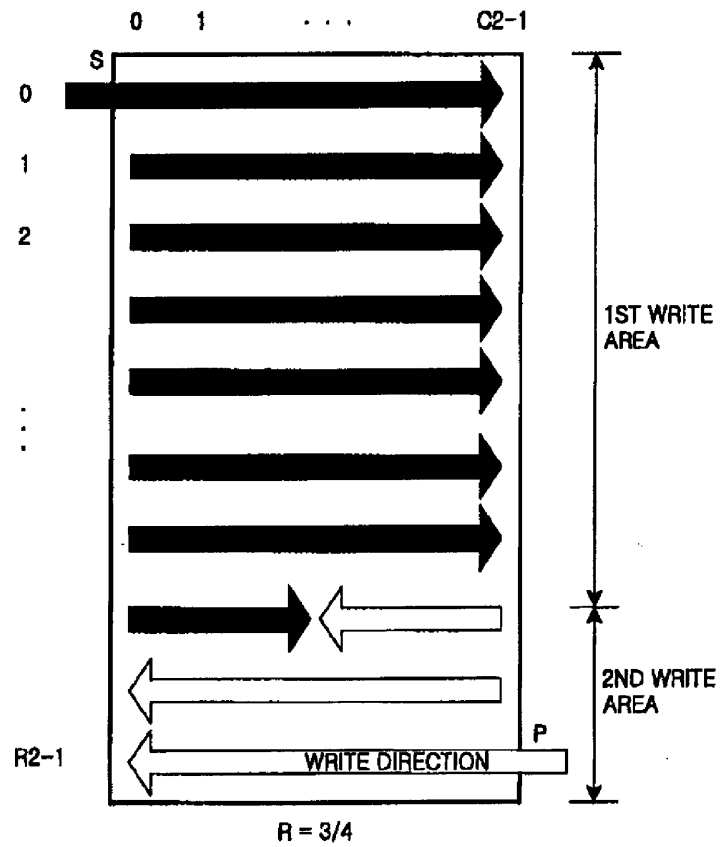


FIG.9A

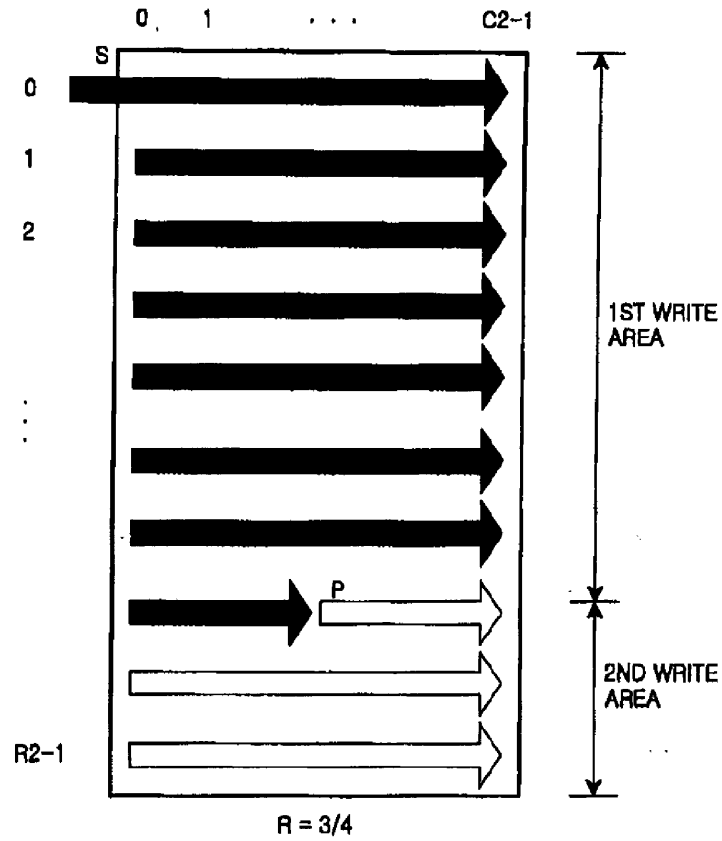


FIG.9B

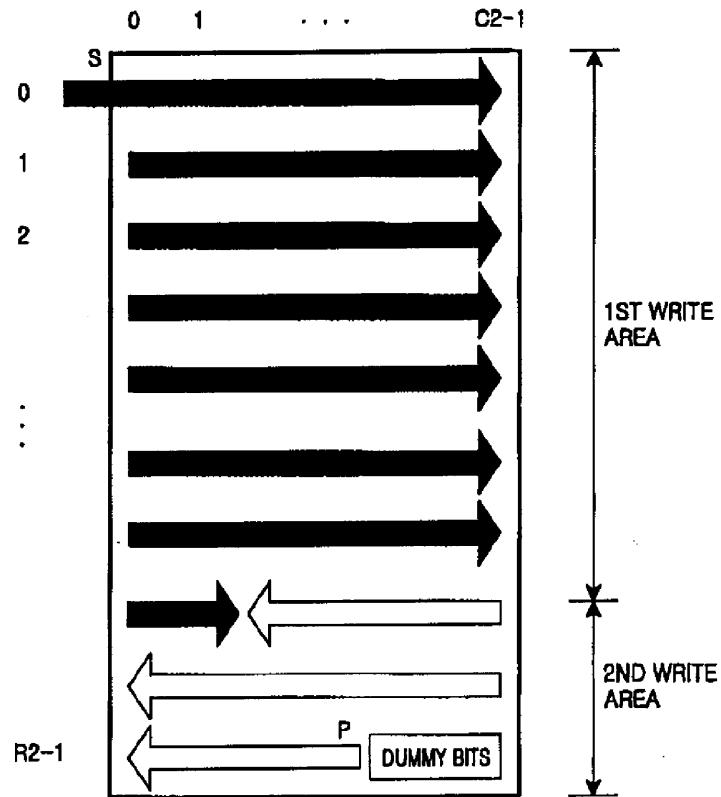


FIG.10A

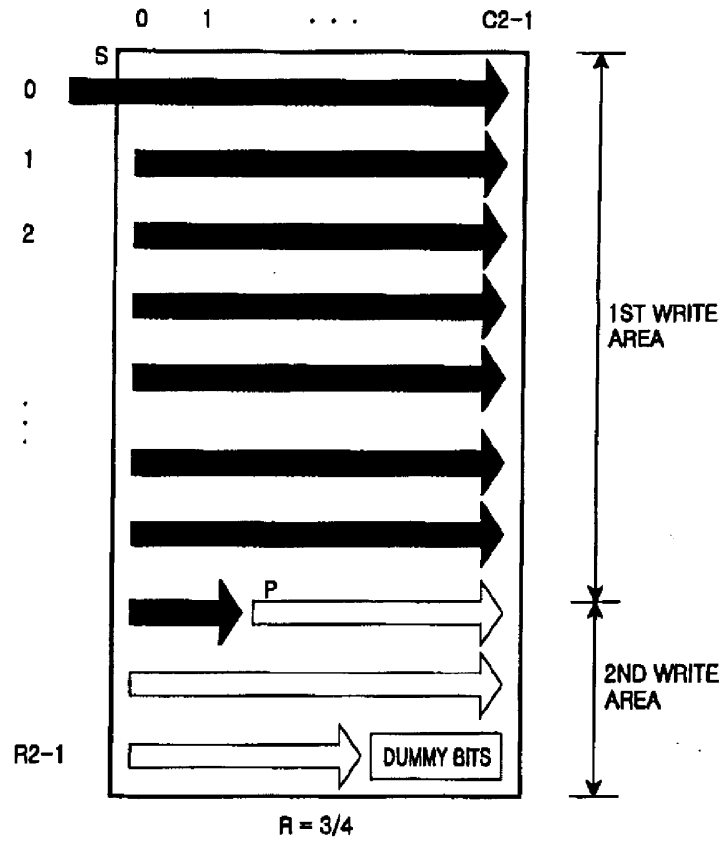


FIG.10B

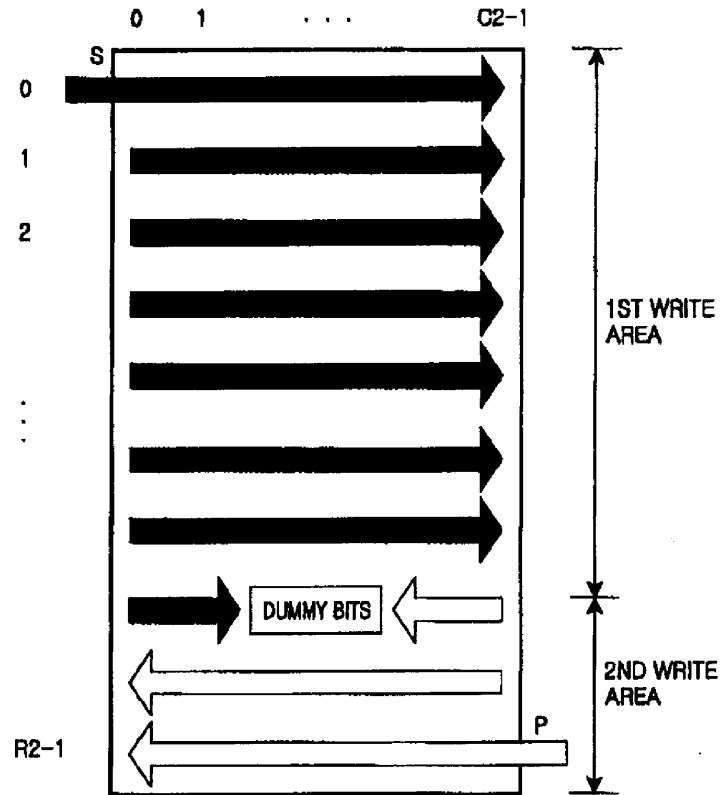


FIG.10C

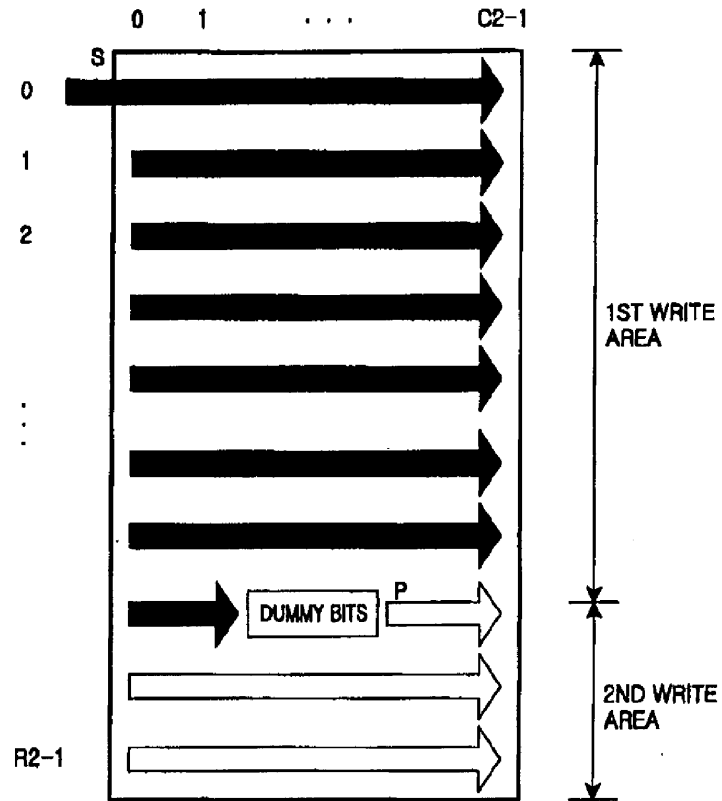


FIG.10D

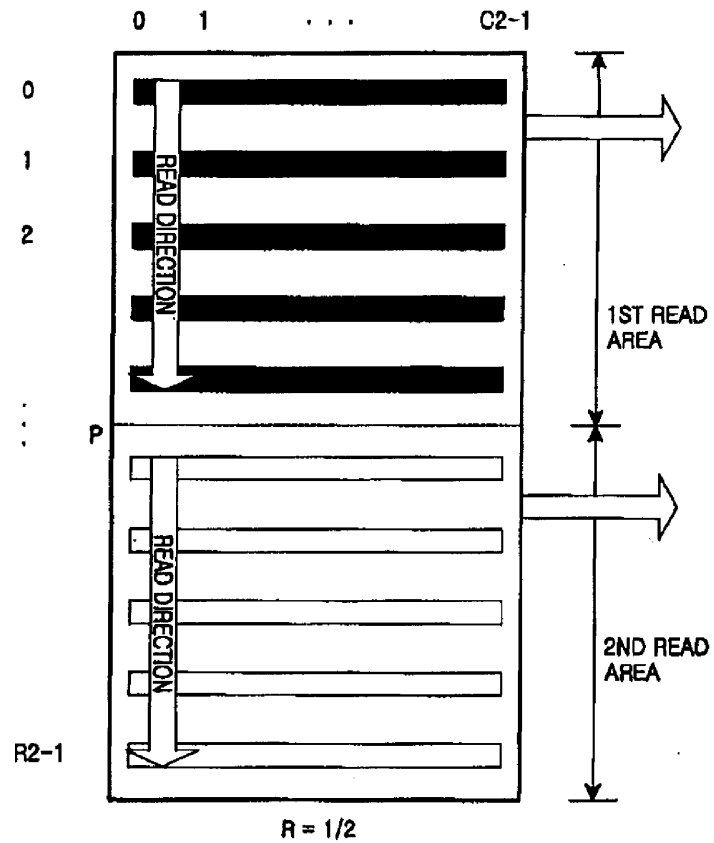


FIG.11A

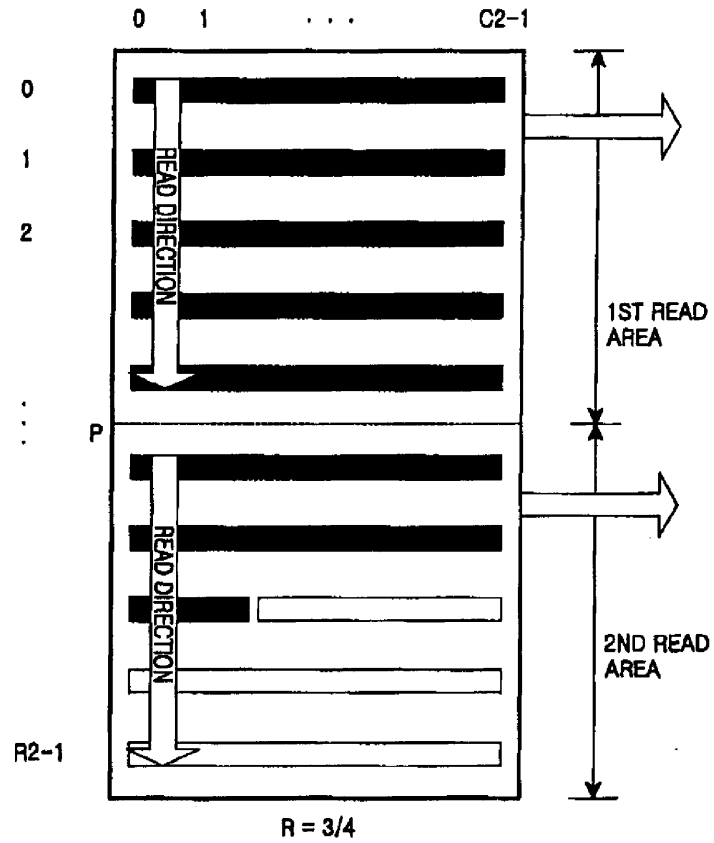


FIG.11B

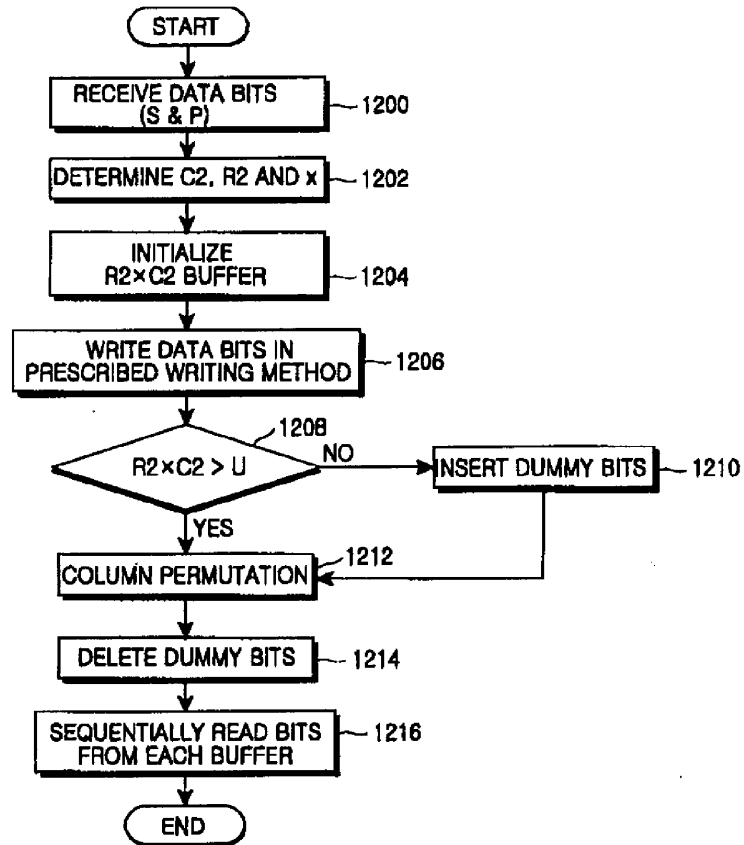


FIG.12

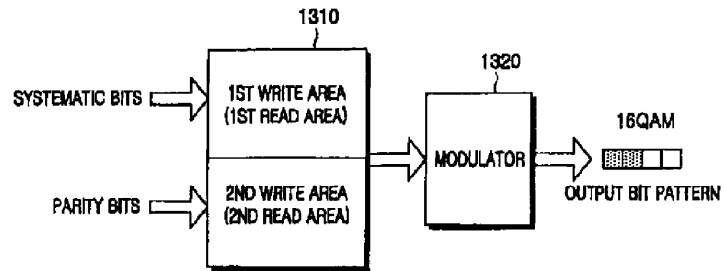


FIG.13

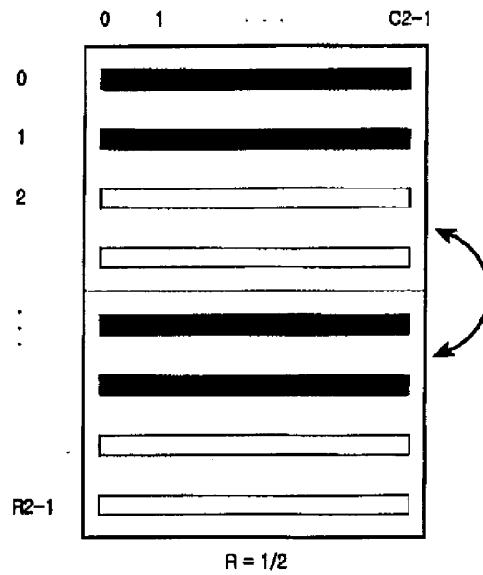


FIG.14A

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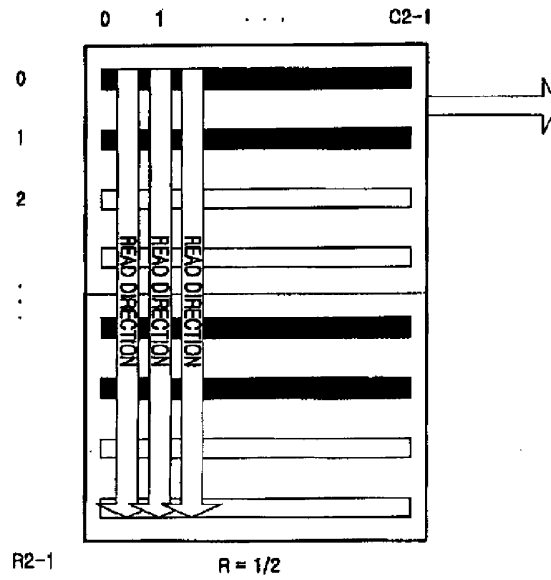


FIG.15A

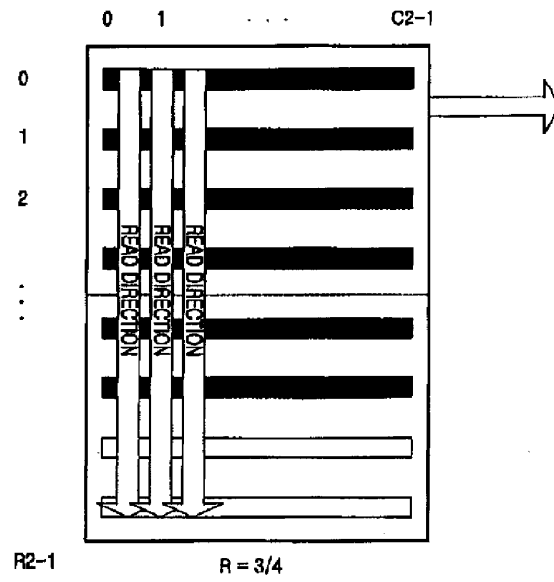


FIG. 15B

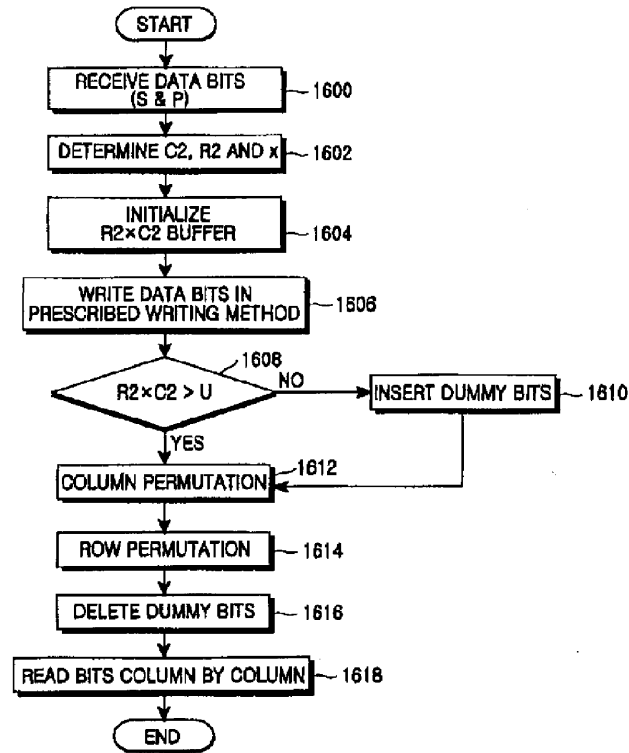


FIG.16

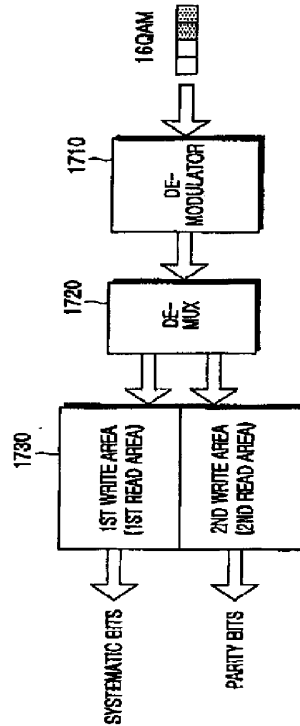


FIG.17

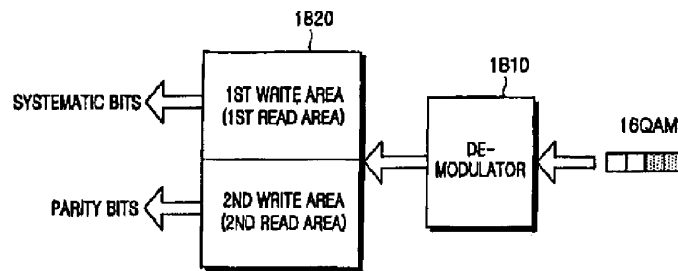


FIG.18

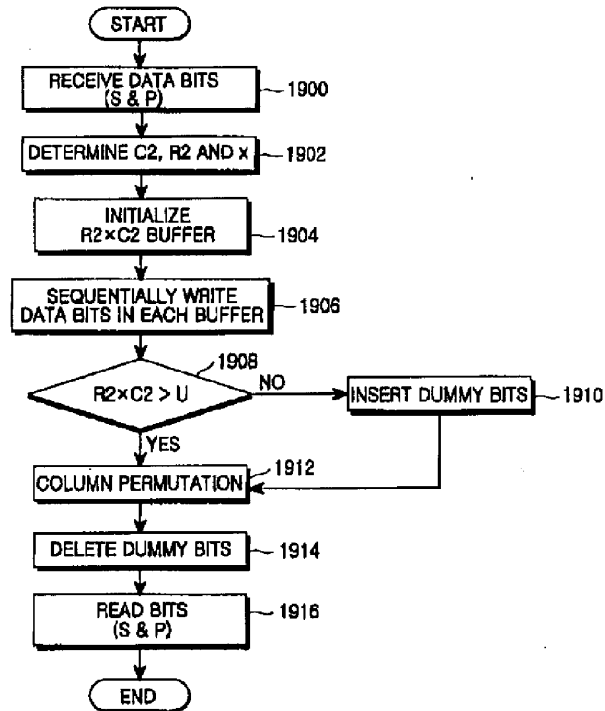


FIG.19

1 Abstract

An interleaver separates an area of a buffer included therein into a first write area and a second write area according to a ratio of coded bits with higher priority to coded bits with lower priority, sequentially writes a stream of the coded bits with higher priority in a row direction from a first column to a last column among the columns in the first write area, and sequentially writes a stream of the coded bits with lower priority in a row direction from a first column to a last column among the columns in the second write area, and permutes the columns in the buffer area according to a given rule. A multiplexer divides rows in the buffer area into a first read area and a second read area having the same size, and alternately reads as many bits as a number determined based on a prescribed modulation technique from the first read area and the second read area in such a manner that the bits are sequentially read in a column direction from a first row to a last row among the rows of each of the first read area and the second read area, and multiplexes the read coded bits.

2 Representative Drawing

Fig. 2

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(11) 特許出願公表番号

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 (31) 優先権主張番号 60/372,763
 (32) 優先日 平成14年4月15日 (2002.4.15)
 (33) 優先権主張国 米国 (US)

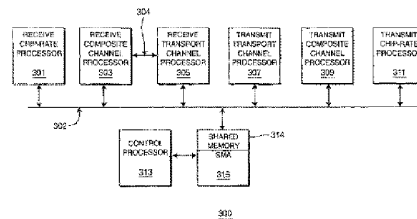
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 弁理士 谷 義一
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最終頁に続く

(54) 【発明の名称】 物理レイヤ処理において使用するためのソフトウェアパラメータ化可能な制御ブロック

(57) 【要約】

無線通信システムにおいて使用される物理レイヤトランスポート複合処理システム。複数の互いに接続された処理ブロックが提供される。ブロックは、データ読み取りバス、データ書き込みバス、および制御バスで互いに接続される。ブロックには、トランスポートチャネル処理ブロック (303、307)、複合チャネル処理ブロック (305、309)、およびチップレート処理ブロック (301、311) が含まれる。ブロックの少なくとも2つは、複数の無線フォーマット向けにデータを処理することができる。特定の無線モード向けに第1のパラメータのセットが、ブロック群にプログラミングされる。ブロック群は、特定の無線フォーマットモードでデータを処理するように動作させられる。



【特許請求の範囲】**【請求項1】**

時分割双方向（TDD）モードと周波数分割双方向（FDD）モードの両方で動作することができる無線ユーザ装置であって、

TDDモードまたはFDDモードの送信のためのネットワークデータを受け取り、該受け取られたネットワークデータを処理するための送信トランスポートチャネルプロセッサと、

該処理されたトランスポートチャネルを受け取り、TDDモードで動作している場合、リソースユニットを生成し、FDDモードで動作している場合、物理チャネルを生成するための送信複合チャネルプロセッサと、

該生成された物理チャネルを無線インタフェースを介して伝送するためにフォーマットするためのFDD送信チップレートプロセッサと、

該生成されたリソースユニットを前記無線インタフェースを介して伝送するためにフォーマットするためのTDD送信チップレートプロセッサとを含むことを特徴とする装置。

【請求項2】

前記送信トランスポートチャネルプロセッサ、前記送信複合チャネルプロセッサ、前記FDD送信チップレートプロセッサ、前記TDD送信チップレートプロセッサ、FDD受信チップレートプロセッサ、TDD送信チップレートプロセッサ、受信複合チャネルプロセッサ、および、受信トランスポートチャネルプロセッサは、システムバスに結合されることを特徴とする請求項1に記載の無線ユーザ装置。

【請求項3】

システムバスは、共通のデータ読み取りバス、データ書き込みバス、および、制御バスを含むことを特徴とする請求項1に記載の無線ユーザ装置。

【請求項4】

前記送信トランスポートチャネルプロセッサは、CRC付加、トランスポートブロック連結／符号ブロックセグメント化、チャネル符号化、無線フレームセグメント化、第1のインターリーブ、および、無線フレーム等化をTDDモードおよびFDDモードで実行することを特徴とする請求項1に記載の無線ユーザ装置。

【請求項5】

前記送信複合チャネルプロセッサは、レートマッチング、トラフィックチャネル多重化、ビットスクランブル、物理チャネルセグメント化、第2のインターリーブ、および、物理チャネルマッピングをTDDモードおよびFDDモードで実行することを特徴とする請求項1に記載の無線ユーザ装置。

【請求項6】

前記送信チップレートプロセッサは、拡散、スクランブル、パルス整形フィルタリング、および、周波数補正を実行することを特徴とする請求項1に記載の無線ユーザ装置。

【請求項7】

前記送信トランスポートチャネルプロセッサおよび前記送信複合チャネルプロセッサは、FDDモードとTDDモードの両方で動作し、対応するモードで動作するようにソフトウェアによってパラメータ化されることを特徴とする請求項1に記載の無線ユーザ装置。

【請求項8】

前記生成されたリソースユニットおよび前記生成された物理チャネルを前記無線インタフェースを介して送信するための無線周波数トランスミッタをさらに含むことを特徴とする請求項1に記載の無線ユーザ装置。

【請求項9】

時分割双方向（TDD）モードと周波数分割双方向（FDD）モードの両方で動作することができる無線ユーザ装置であって、

FDDフォーマットで受信された信号を物理チャネルにフォーマットするためのFDD

受信チップレートプロセッサと、

TDDフォーマットで受信された信号をリソースユニットにフォーマットするためのTDD受信チップレートプロセッサと、

TDDモードで動作している場合、リソースユニットを受け取り、FDDモードで動作している場合、物理チャネルを受け取り、トランスポートチャネルを生成するための受信複合チャネルプロセッサと、

TDDモードまたはFDDモードで動作している場合に受け取られた該生成したトランスポートチャネルを処理し、前記受け取られたトランスポートチャネルを処理してネットワークデータを生成するための受信トランスポートチャネルプロセッサとを含むことを特徴とする装置。

【請求項10】

前記受信チップレートプロセッサ、前記TDD受信チップレートプロセッサ、前記受信複合チャネルプロセッサ、および、前記受信トランスポートチャネルプロセッサは、システムバスに結合されることを特徴とする請求項9に記載の無線ユーザ装置。

【請求項11】

システムバスは、共通のデータ読み取りバス、データ書き込みバス、および、制御バスを含むことを特徴とする請求項9に記載の無線ユーザ装置。

【請求項12】

前記受信トランスポートチャネルプロセッサは、TDDモードで、CRC付加、トラフィックブロック連結／符号ブロックセグメント化、チャネル符号化、無線フレーム等化、第1のインターリーブ、および、無線フレームセグメント化の逆を実行し、FDDモードで、CRC付加、トラフィックブロック連結／符号ブロックセグメント化、チャネル符号化、レートマッチング、第1の不連続送信インジケータの挿入、第1のインターリーブ、無線フレームセグメント化、および、トラフィックチャネル多重化の逆を実行することを特徴とする請求項9に記載の無線ユーザ装置。

【請求項13】

前記受信複合チャネルプロセッサは、TDDモードで、トラフィックチャネル多重化、ビットスクランブル、物理チャネルセグメント化、第2のインターリーブ、および、物理チャネルマッピングの逆を実行し、FDDモードで、第2の不連続送信インジケータの挿入、物理チャネルセグメント化、第2のインターリーブ、および、物理チャネルマッピングの逆を実行することを特徴とする請求項9に記載の無線ユーザ装置。

【請求項14】

前記受信チップレートプロセッサは、拡散、スクランブル、パルス整形フィルタリング、および、周波数補正の逆を実行することを特徴とする請求項9に記載の無線ユーザ装置。

【請求項15】

前記受信トランスポートチャネルプロセッサおよび前記受信複合チャネルプロセッサは、FDDモードとTDDモードの両方で動作し、対応するモードで動作するようにソフトウェアによってパラメータ化されることを特徴とする請求項9に記載の無線ユーザ装置。

【請求項16】

前記受信チップレートプロセッサに入力するために無線インタフェースを介してリソースユニットおよび物理チャネルを受信するための無線周波数レシーバをさらに含むことを特徴とする請求項9に記載の無線ユーザ装置。

【請求項17】

時分割双方向(TDD)モードと周波数分割双方向(FDD)モードの両方で動作することができる無線ノードB／基地局であって、

TDDモードまたはFDDモードの送信のためのネットワークデータを受け取り、該受け取られたネットワークデータを処理するための送信トランスポートチャネルプロセッサと、

該処理されたトランスポートチャネルを受け取り、TDDモードで動作している場合、

リソースユニットを生成し、FDDモードで動作している場合、物理チャネルを生成するための送信複合チャネルプロセッサと、

該生成された物理チャネルを無線インタフェースを介して伝送するためにフォーマットするためのFDD送信チップレートプロセッサと、

該生成されたリソースユニットを前記無線インタフェースを介して伝送するためにフォーマットするためのTDD送信チップレートプロセッサとを含むことを特徴とする無線ノードB／基地局。

【請求項18】

前記送信トランスポートチャネルプロセッサ、前記送信複合チャネルプロセッサ、前記FDD送信チップレートプロセッサ、前記TDD送信チップレートプロセッサ、FDD受信チップレートプロセッサ、TDD送信チップレートプロセッサ、受信複合チャネルプロセッサ、および、受信トランスポートチャネルプロセッサは、システムバスに結合されることを特徴とする請求項17に記載の無線ノードB／基地局。

【請求項19】

システムバスは、共通のデータ読み取りバス、データ書き込みバス、および、制御バスを含むことを特徴とする請求項17に記載の無線ノードB／基地局。

【請求項20】

前記送信トランスポートチャネルプロセッサは、TDDモードで、CRC付加、トラフィックブロック連結／符号ブロックセグメント化、チャネル符号化、無線フレーム等化、第1のインターリーブ、および、無線フレームセグメント化を実行し、FDDモードで、CRC付加、トラフィックブロック連結／符号ブロックセグメント化、チャネル符号化、レートマッチング、第1の不連続送信指示の挿入、第1のインターリーブ、無線フレームセグメント化、および、トラフィックチャネル多重化を実行することを特徴とする請求項17に記載の無線ノードB／基地局。

【請求項21】

前記送信複合チャネルプロセッサは、TDDモードで、トラフィックチャネル多重化、ビットスクランブル、物理チャネルセグメント化、第2のインターリーブ、および物理チャネルマッピングを実行し、FDDモードで、第2の不連続送信インジケータの挿入、物理チャネルセグメント化、第2のインターリーブ、および、物理チャネルマッピングを実行することを特徴とする請求項17に記載の無線ノードB／基地局。

【請求項22】

前記送信チップレートプロセッサは、拡散、スクランブル、パルス整形フィルタリング、および、周波数補正を実行することを特徴とする請求項17に記載の無線ノードB／基地局。

【請求項23】

前記送信トランスポートチャネルプロセッサおよび前記送信複合チャネルプロセッサは、FDDモードとTDDモードの両方で動作し、対応するモードで動作するようにソフトウェアによってパラメータ化されることを特徴とする請求項17に記載の無線ノードB／基地局。

【請求項24】

前記生成されたリソースユニットおよび前記生成された物理チャネルを前記無線インタフェースを介して送信するための無線周波数トランスミッタをさらに含むことを特徴とする請求項17に記載の無線ノードB／基地局。

【請求項25】

広帯域符号分割多重アクセスの時分割双方向（TDD）モードと周波数分割双方向（FDD）モードの両方で動作することができる無線ノードB／基地局であって、

FDDフォーマットで受信された信号を物理チャネルにフォーマットするためのFDD受信チップレートプロセッサと、

TDDフォーマットで受信された信号をリソースユニットにフォーマットするためのTDD受信チップレートプロセッサと、

TDDモードで動作している場合、リソースユニットを受け取り、FDDモードで動作している場合、物理チャネルを受け取り、トランスポートチャネルを生成するための受信複合チャネルプロセッサと、

TDDモードまたはFDDモードで動作している場合に受け取られた該生成したトランスポートチャネルを処理し、該受け取られたトランスポートチャネルを処理してネットワークデータを生成するための受信トランスポートチャネルプロセッサとを含むことを特徴とする無線ノードB／基地局。

【請求項26】

前記受信チップレートプロセッサ、前記TDD受信チップレートプロセッサ、前記受信複合チャネルプロセッサ、および、前記受信トランスポートチャネルプロセッサは、システムバスに結合されることを特徴とする請求項25に記載の無線ノードB／基地局。

【請求項27】

システムバスは、共通のデータ読み取りバス、データ書き込みバス、および、制御バスを含むことを特徴とする請求項25に記載の無線ノードB／基地局。

【請求項28】

前記受信トランスポートチャネルプロセッサは、CRC付加、トランスポートブロック連結／符号ブロックセグメント化、チャネル符号化、無線フレームセグメント化、第1のインターリーブ、および、無線フレーム等化の逆をTDDモードおよびFDDモードで実行することを特徴とする請求項25に記載の無線ノードB／基地局。

【請求項29】

前記受信複合チャネルプロセッサは、レートマッチング、トラフィックチャネル多重化、ビットスクランブル、物理チャネルセグメント化、第2のインターリーブ、および、物理チャネルマッピングの逆をTDDモードおよびFDDモードで実行することを特徴とする請求項25に記載の無線ノードB／基地局。

【請求項30】

前記受信チップレートプロセッサは、拡散、スクランブル、パルス整形フィルタリング、および、周波数補正の逆を実行することを特徴とする請求項25に記載の無線ノードB／基地局。

【請求項31】

前記受信トランスポートチャネルプロセッサ、前記受信複合チャネルプロセッサは、FDDモードとTDDモードの両方で動作し、対応するモードで動作するようにソフトウェアによってパラメータ化されることを特徴とする請求項25に記載の無線ノードB／基地局。

【請求項32】

前記受信チップレートプロセッサに入力するために無線インタフェースを介してリソースユニットおよび物理チャネルを受信するための無線周波数レシーバをさらに含むことを特徴とする請求項25に記載の無線ノードB／基地局。

【請求項33】

無線通信システムにおいて使用するための複数のソフトウェアパラメータ化可能な制御ブロックおよび共有メモリにおけるデータ伝送を調整する共有メモリアービタ(SMA)であって、

物理レイヤトランスポート複合処理システム内の前記複数のソフトウェアパラメータ化可能な制御ブロックにパラメータおよびデータの伝送をロードするためのデータバスと、

前記共有メモリと前記複数のソフトウェアパラメータ化可能な制御ブロックの間でパラメータおよびデータの伝送を要求するための複数のチャネル要求と、

前記複数のソフトウェアパラメータ化可能な制御ブロックの間でデータおよびパラメータの伝送を許すSMAからの複数の認可と、

アドレスレジスタのインクリメントおよびデクリメントを行うデータストロープとを含むことを特徴とする共有メモリアービタ(SMA)。

【請求項34】

ソフトウェアパラメータ化可能な制御ブロック読み取りは、
前記ソフトウェアパラメータ化可能な制御ブロックの少なくとも1つが、チャネル要求をアサートする、

ソフトウェアパラメータ化可能な制御ブロックの前記少なくとも1つが、前記SMAからの認可信号を待つ、

前記少なくともソフトウェアパラメータ化可能な制御ブロックが、前記共有メモリからデータをストローブして前記データストローブがローカルレジスタに入るようにする、および、

前記SMAが、アドレスレジスタをインクリメントする
ことを備えることを特徴とする請求項33に記載のSMA。

【請求項35】

ソフトウェアパラメータ化可能な制御ブロック書き込みは、

前記ソフトウェアパラメータ化可能な制御ブロックの少なくとも1つが、チャネル要求をアサートする、

前記SMAレジスタが、前記少なくとも1つのソフトウェアパラメータ化可能な制御ブロックからデータを書き込む、

前記SMAが、認可信号をアサートする、

前記SMAが、メインメモリにデータを書き込み、アドレスレジスタをインクリメントする、

前記少なくとも1つのソフトウェアパラメータ化可能な制御ブロックが、前記少なくとも1つのソフトウェアパラメータ化可能な制御ブロックによって提供されたデータがメモリに書き込まれたことを示すSMAからの前記認可信号を待つ
ことを備えることを特徴とする請求項33に記載のSMA。

【請求項36】

ソフトウェアパラメータ化可能な制御ブロックポインタ読み取り書き込みは、

少なくとも1つのソフトウェアパラメータ化可能な制御ブロックが、読み取り要求およびデータ要求を同時にアサートする、

前記SMAが、制御チャネルアドレスレジスタの中に現在、入っている第1のアドレスを使用して前記共有メモリから32ビット語を読み取る、

前記SMAが、前記制御チャネルアドレスレジスタをインクリメントし、読み取られた値を第1のデータアドレスレジスタの中に格納する、および、

前記SMAが、認可信号をアサートして肯定応答する (acknowledge)

ことを備えることを特徴とする請求項33に記載のSMA。

【請求項37】

前記SMAは、複数の制御プロセッサの少なくとも1つに接続されることを特徴とする請求項33に記載のSMA。

【請求項38】

少なくとも制御プロセッサは、デジタル信号プロセッサ (DSP) であることを特徴とする請求項33に記載のSMA。

【請求項39】

少なくとも制御プロセッサは、アドバンストRISCマシン (ARM) であることを特徴とする請求項33に記載のSMA。

【請求項40】

制御プロセッサ読み取りは、

制御プロセッサが、前記SMAに対して要求をアサートする、

前記SMAが、プロセッサ読み取り要求をアサートし、アドレス値を制御プロセッサに送る、

前記SMA、指示、プロセッサ要求が、読み取り要求である、および、

前記SMAが、データのブロックを読み取る

ことを備えることを特徴とする請求項33に記載のSMA。

【請求項41】

制御プロセッサ書き込みが、
制御プロセッサが、前記SMAに対して要求をアサートする、
前記SMAが、プロセッサ書き込み要求をアサートし、アドレス値を前記制御プロセッサに送る、
前記SMA、指示、プロセッサ要求が、書き込み要求である、および、
前記SMAが、データのブロックを書き込む
ことを備えることを特徴とする請求項33に記載のSMA。

【請求項42】

無線通信を処理する際に使用するための物理レイヤトランスポート複合処理のための方法であって、
トランスポートチャネルごとにデータを処理するためのトランスポートチャネル処理ブロック、複合チャネルごとにデータを処理するための複合チャネル処理ブロック、および、無線インタフェースに関連するデータを処理するためのチップレート処理ブロックを含み、前記処理ブロックの少なくとも2つが、複数の無線フォーマット向けにデータを処理することができる、システムバスによって互いに接続された複数の相互接続された処理ブロックを提供すること、
特定の無線フォーマット向けに第1のパラメータのセットを前記複数の相互接続された処理ブロックにプログラミングすること、および、
前記相互接続された処理ブロックを動作させて、前記特定の無線フォーマットのデータを処理すること
を含むことを特徴とする方法。

【請求項43】

前記システムバスは、データ書き込みバス、データ読み取りバス、および、制御バスを含むことを特徴とする請求項42に記載の方法。

【請求項44】

前記無線インタフェースを介して信号を受信するための受信レシーバと、前記無線インタフェースを介してデータを送信するための送信トランスミッタとをさらに含むことを特徴とする請求項42に記載の方法。

【請求項45】

無線通信を処理する際に使用するための物理レイヤトランスポート複合プロセッサであって、
トランスポートチャネルごとにデータを処理するためのトランスポートチャネル処理ブロック、複合チャネルごとにデータを処理するための複合チャネル処理ブロック、および、無線インタフェースに関連するデータを処理するためのチップレート処理ブロックを含み、前記処理ブロックの少なくとも2つが、複数の無線フォーマット向けにデータを処理することができる、システムバスによって互いに接続された複数の相互接続された処理ブロックと、
特定の無線フォーマット向けに前記複数の相互接続された処理ブロックにプログラミングされる第1のパラメータのセットと、
前記相互接続された処理ブロックが、前記特定の無線フォーマットのデータを処理するように動作せられること
を含むことを特徴とするプロセッサ。

【請求項46】

前記システムバスは、データ書き込みバス、データ読み取りバス、および、制御バスを含むことを特徴とする請求項45に記載の物理レイヤトランスポート複合プロセッサ。

【請求項47】

前記無線インタフェースを介して信号を受信するためのレシーバと、前記無線インタフェースを介してデータを送信するためのトランスミッタとをさらに含むことを特徴とする請求項45に記載の物理レイヤトランスポート複合プロセッサ。

【請求項48】

広帯域符号分割多重アクセスの時分割双方向 (TDD) モードと周波数分割双方向 (FDD) モードの両方で動作することができる無線ユーザ装置のための方法であって、

TDDモードまたはFDDモードで送信するために複数のネットワークデータを受け取ること、

該受け取られたネットワークデータの第1のトランスポートチャネルのセットを送信トランスポートチャネルプロセッサにおいて処理すること、

該処理された第1のトランスポートチャネルのセットを受け取り、TDDモードで動作している場合、第1のリソースユニットのセットを生成し、FDDモードで動作している場合、第1の物理チャネルのセットを生成することを送信複合チャネルプロセッサにおいて行うこと、

該生成された第1の物理チャネルのセットを伝送のためにFDD送信チップレートプロセッサにおいてフォーマットすること、

該生成された第1のリソースユニットのセットをTDD送信チップレートプロセッサにおいてフォーマットすること、

該生成された物理チャネルおよび該生成されたリソースユニットを無線周波数トランスミッタにおいて無線インタフェースを介して送信すること、

無線周波数レシーバにおいて前記無線インタフェースから信号を受信すること、

FDDフォーマットで受信された該受信信号をFDD受信チップレートプロセッサにおいて第2の物理チャネルのセットにフォーマットすること、

TDDフォーマットで受信された該受信信号をTDD受信チップレートプロセッサにおいて第2のリソースユニットのセットにフォーマットすること、

TDDモードで動作している場合、前記第2のリソースユニットのセットを受信し、FDDモードで動作している場合、前記第2の物理チャネルのセットを受信し、第2のセットのトランスポートチャネルを生成することを受信複合チャネルプロセッサで行うこと、および、

TDDモードまたはFDDモードで動作している場合に受信され生成された第2のトランスポートチャネルのセットを処理して、ネットワークデータを生成することを受信トランスポートチャネルプロセッサで行うこと

を含むことを特徴とする方法。

【請求項49】

共通のデータ読み取り、データ書き込み、および、制御バスを前記送信トランスポートチャネルプロセッサ、前記送信複合チャネルプロセッサ、前記FDD送信チップレートプロセッサ、前記TDD送信チップレートプロセッサ、前記FDD受信チップレートプロセッサ、前記TDD受信チップレートプロセッサ、前記受信複合チャネルプロセッサ、および、前記受信トランスポートチャネルプロセッサに結合することをさらに含むことを特徴とする請求項48に記載の方法。

【発明の詳細な説明】

【技術分野】

【0001】

本発明は、一般に、無線通信システムに関する。詳細には、本発明は、そのようなシステムのために物理レイヤにおいてデータを処理することに関する。

【背景技術】

【0002】

無線通信システムでは、ネットワークから受信されたデータが、無線インタフェースを介して伝送するためにフォーマットされる。逆に、無線インタフェースを介して受信されたデータは、元のネットワークデータを回復するように処理される。このデータの処理が、物理レイヤ処理と呼ばれる。

【0003】

物理レイヤにおいてデータを処理することは、無線通信システムにおける複雑な操作である。図1は、提案される第3世代パートナーシッププロジェクト (3GPP) の広帯域

符号分割多重アクセス (W-CDMA) の提案される時分割双方向 (TDD) モードに関する物理レイヤ処理の概念図である。処理は、トランスミッタに関して示している。同様の逆の形で、データは、レシーバにおいて処理される。ただし、レシーバにおける物理レイヤ処理との1つの違いは、レシーバが、通常、ソフトシンボルを処理し、処理要件が複雑になることである。また、図1は、W-CDMAの周波数分割双方向 (FDD) モードのアップリンクにも概念的に関連する。ただし、各ブロックによって使用されるパラメータは、TDDとFDDでは異なる。

【0004】

トランスポートブロックは、無線インタフェースを介する伝送のために着信する。トランスポートブロックは、トランスポートブロックのセットで着信する。セットは、伝送時間間隔 (TTI) として知られる指定された時間間隔で受信される。TDDモード、およびFDDモードの場合、可能なTTIの長さは、1つ、2つ、4つ、および8つの無線フレームにそれぞれ対応する10ミリ秒、20ミリ秒、40ミリ秒、および80ミリ秒である。巡回冗長符号 (CRC) 付加ブロック42が、CRCビットを各トランスポートブロックに付加する。CRCビットは、レシーバにおける誤り検出のために使用される。CRCビット長は、より高位のレイヤから通知される。

【0005】

トランスポートブロック (TrB1k) は、TrB1k連結/符号ブロックセグメント化ブロック44によって順次に連結される。連結されたブロックのビットの数が、符号ブロックに許された最大サイズより大きい場合、連結されたブロックは、セグメント化される。チャネル符号化ブロック46誤り訂正が、畳み込み符号化、ターボ符号化などにより、符号ブロックを符号化する。符号化された後、符号ブロックは、一緒に連結される。連結された符号ブロックを最小限の数の等しいサイズのセグメント (フレーム) にセグメント化することができない場合、無線フレームセグメント化ブロック50によって追加の任意のビットを連結することにより、無線フレーム等化が行われる。

【0006】

第1のインターリーブ48が、すべての連結済みのデータをインターリーブする。その後、インターリーブ済みのデータが、無線フレームセグメント化ブロック50によって無線フレームにセグメント化される。レートマッチングブロック52が、ビットをバンクチャリングするか、または繰り返す。バンクチャリングおよび繰り返すにより、各物理チャネル上で伝送されるデータが、そのチャネルの最大ビット伝送速度に等しいことが確実になる。各トランスポートチャネル (TrCH) に関するレートマッチング属性は、より高位のレイヤによって通知される。

【0007】

TrCH多重化ブロック54が、各トランスポートチャネルに関する1つのフレームのデータを受け取る。各TrCHに関して受け取られたデータは、符号化複合トランスポートチャネル (CCTrCH) 上に順次に多重化される。ビットスクランプリングブロック65が、そのCCTrCHビットをスクランブルする。

【0008】

物理チャネルセグメント化ブロック58が、多重化されたデータを物理チャネル上にマップする。第2のインターリーブ60が、無線フレーム全体にわたって、または各タイムスロットにわたってスクランブルデータをインターリーブする。第2のインターリーブ後、インターリーブ済みのデータが、物理チャネルマッピングブロック62により、無線インタフェースを介して伝送するために物理チャネルにセグメント化される。

【0009】

各物理チャネルに関するデータは、拡散ブロック64によってそれぞれの符号を使用して拡散される。拡散済みのデータが、スクランプリングブロック66を使用して、基地局に関連する符号でスクランブルされる。もたらされたそれぞれのスクランブル済みのチップが、パルス整形フィルタ68によってパルス整形される。周波数補正ブロック70が、結果の信号の周波数を調整する。周波数補正済みの信号が、無線インタフェースを介して

放射される。

【0010】

やはり図1に示すFDDモードのダウンリンクの場合、処理は、概念的に同様の形で実行される。ただし、いくつかの違いが存在する。FDDダウンリンクでは、レートマッチングは、レートマッチングブロック52によってチャネル符号化後に実行される。この結果、無線フレーム等化は、実行されない。不連続な送信をサポートするため、第1の不連続送信(DTX)指示が、第1のDTX指示ブロック72によって第1のインターリーブに先行して挿入され、第2のDTX指示が、第2のDTX指示ブロック74によって物理チャネルマッピングに先行して挿入される。

【0011】

物理チャネル処理を実行するための2つのアプローチは、ソフトウェアベースのアプローチとハードウェアベースのアプローチである。ソフトウェアベースのアプローチでは、物理チャネル処理の大部分が、ソフトウェアによって実行される。ソフトウェアベースのアプローチは、高い柔軟性を可能にする。物理チャネル処理のパラメータをソフトウェア改訂によって容易に変更することができる。

【発明の開示】

【発明が解決しようとする課題】

【0012】

ソフトウェアベースのアプローチが抱える2つの欠点は、1)マイクロプロセッサまたはDSPなどのプロセッサが、カスタマイズされたソリューションより高い電力を使用すること、および2)すべての要求される機能を実行するのにいくつかのプロセッサが必要とされる可能性があることである。

【0013】

ハードウェアベースのソリューションは、要求される総チップ面積を小さくし、電力消費を低減することを可能にする。特定の環境向けにハードウェアをカスタマイズし、構成すると、データ処理のnのより高い効率。しかし、そのようなアプローチは、設計の柔軟性を小さくする。物理レイヤ処理の再構成は、初期設計において提供されるパラメータに限定される。

【0014】

よって、高い処理速度と柔軟性を可能にする物理レイヤ処理を得ることが望ましい。

【課題を解決するための手段】

【0015】

無線通信システムにおいて使用される物理レイヤトランスポート複合処理システム。複数の互いに接続された処理ブロックが提供される。ブロックは、データ読み取りバス、データ書き込みバス、および制御バスで互いに接続される。ブロックには、トランスポートチャネル処理ブロック、複合チャネル処理ブロック、およびチップレート処理ブロックが含まれる。ブロックの少なくとも2つが、複数の無線フォーマットに関してデータを処理することができる。特定の無線モード用に第1のパラメータのセットが、ブロックにプログラムされる。ブロックは、特定の無線フォーマットモードでデータを処理するように動作させられる。

【発明を実施するための最良の形態】

【0016】

本発明は、すべての図で同様の符号が同様の要素を表している図を参照して説明する。物理レイヤ処理は、主に3GPPのTDDモードおよびFDDモードの好ましい実施形態に関連して説明するが、時間分割同期符号分割多重アクセス(TD-SCDMA)、TSM、CDMA2000、その他などの他のシステムにも適用可能である。

【0017】

好ましい物理レイヤシステムアーキテクチャ300の概要を図2に示している。この物理レイヤシステムは、無線通信システムの基地局/ノードBにおいてか、またはユーザ装置において使用することができる。この好ましいアーキテクチャにより、提案される3G

PPのW-CDMAシステムおよびGSMのTDDモード、FDDモードなどの異なる無線環境にわたる物理レイヤ処理の設計の柔軟性が可能になる。

【0018】

ブロック301、303、305、307、309、および311は、一式のソフトウェアパラメータ化可能なレバレッジ (leveraged) された組み込みプロセッサを表しており、仮想回路 (VC) としても知られている。受信チップレートプロセッサ301が、データ読み取りバス、データ書き込みバス、および制御バスに接続され、これら3つを、以降、システムバス302と呼ぶ。受信複合チャネルプロセッサ303ブロックおよび受信トランスポートチャネルプロセッサ305ブロックも、システムバス302に接続される。さらに、これら2つのブロックは、いずれのデータブロックがトランスポートチャネル処理の準備ができているかを受信トランスポートチャネルプロセッサ305に報告する連番バス (sequential number bus) も有する。送信トランスポートチャネルプロセッサ307ブロック、送信複合チャネルプロセッサ309ブロック、および送信チップレートプロセッサ311ブロックも、システムバス302に接続される。共有メモリ/共有メモリアービタ (SMA) 315ブロックが、システムバス302および制御プロセッサ313ブロックに接続される。好ましい実施形態では、ブロックの機能は、3GPPのTDDモード、FDDモード、またはその両方のモードの物理レイヤ処理を実行するように設計されるが、他の実施形態では、他の物理レイヤ処理アプローチが、ブロックによって実行されることも可能である。

【0019】

制御プロセッサ313は、SMA315を介して共有メモリ314の中のコントロールキューを通じて処理ブロックと通信する。制御プロセッサ313は、セットアップデータおよび制御データを、各制御ブロックに関するデータレジスタとして作用する特定の共有メモリ域に入れる。また、共有メモリは、処理ブロック間でデータを伝送するためのデータブロックアドレスホルダとしても利用される。これは、好ましくは、データをブロックで伝送するリンクリストを介して達せられ、各ブロックの最後の要素は、次のデータブロックのアドレスであるか、データ終了インジケータである。この技術により、物理レイヤプロセッサにおけるバッファリングが少なくなる。制御プロセッサ313は、好ましくは、アドバンスRISCマシン (ARM) プロセッサである。代替として、プロセッサ313は、任意の組み込みプロセッサであることが可能である。

【0020】

共有メモリアービタ (SMA) 315は、メインVCおよび制御プロセッサ313によって共有されるメモリへのアクセスを制御するハードウェアだけの仮想回路 (VC) である。SMAユニットは、VCのすべて、およびプロセッサ群がメモリへのアクセスを効率的に共有することを可能にするのに必要なアドレスレジスタおよび順序付けロジックを含む。

【0021】

SMAの高レベルのブロック図を図12で示している。SMAユニットは、VCのすべて、およびプロセッサ群が共有メモリ314へのアクセスを効率的に共有することを可能にするのに必要なアドレスレジスタ601および順序付けロジックを含む。SMAは、保留中の要求が存在するという条件で、毎クロックサイクルに1つの要求をバイフラインに受け入れる。SMAアドレスジェネレータが、チャネル上で実行される次のメモリアクセスのアドレスを含む各SMAチャネルに関するレジスタを保持する。それらのレジスタは、アクセスされるメモリブロックの最初のメモリアドレスに初期設定されなければならない。各アドレスレジスタは、各アクセス後にアドレスポインタがインクリメントされるか、またはデクリメントされるかを示す、ソフトウェアによって構成される関連するコントロールビットを有する。

【0022】

次の3つのタイプのメモリチャネルが存在する。すなわち、1) 読み取りチャネルデータが、共有メモリから要求側のユニットに伝送される、2) 書き込みチャネルデータが、

要求側のユニットから共有メモリに伝送される、3)制御チャネル群(特別な読み取りチャネル群)が、2つのタイプのメモリアクセス、通常の読み取りチャネルに関する読み取りアクセス、およびロードアクセスをサポートする。ロードアクセスは、共有メモリからSMAの中のアドレスレジスタの1つにメモリポインタを伝送するのに使用される。これにより、リンクリストの効率的な実施が可能になる。

【0023】

各ハードウェアコンポーネントには、1つまたは複数のSMAチャネルが割り当てられ、メモリへの伝送、およびメモリからの伝送は、各SMAチャネル上の要求/許可ハンドシェイクによって制御される。要求信号には、重要なバス上の適時のアクセスを保証するために優先順位が付けられる。要求がパイプラインに入ると、許可が送られるまで、同一の要求はパイプラインの中に受け入れられない。

【0024】

受信チップレートプロセッサ301は、処理を完了した時点で、要求603をSMAに送る。SMA315は、その要求603に優先順位を付け、共有メモリ314に関するアドレスレジスタ601を介してメモリアドレスを割り当てる。次に、SMAは、書き込み許可605を要求側のソースに送り、データ伝送を開始させる。

【0025】

物理レイヤ処理システムの1つの可能な実施形態は、3GPPシステムのTDDモードとFDDモードのいずれか、または両方を処理することである。そのような実施形態では、図1を再び参照すると、様々な処理ブロックが、トランスポートチャネル処理400、複合チャネル処理402、およびチップレート処理404という3つの一般的なプロセスに分けられる。トランスポートチャネル処理400は、トランスポートチャネル上で実行される。複合チャネル処理402は、複合チャネル上で実行されて、フレームごとに実行され、チップレート処理404も、タイムスロットごとに実行される。

【0026】

TDDおよびFDDのアップリンク処理に関して図1に示すとおり、トランスポートチャネル処理は、CRC付加42、トランスポートブロック連結44、チャネル符号化46、無線フレーム等化47、第1のインターリーブ48、および無線フレームセグメント化50の機能を実行する。

【0027】

FDDダウンリンクに関して、トランスポートチャネル処理400は、CRC付加42、トランスポートブロック連結44、チャネル符号化46、レートマッチング52、第1のDTX指示挿入72、第1のインターリーブ48、無線フレームセグメント化50、およびトランスポートチャネル多重化54を含む。TDDモードでは、レートマッチング解除(de-rate matching)52は、トランスポートプロセッサ内部または複合プロセッサ内部で実行されることが可能であることに留意されたい。

【0028】

TDDモードおよびFDDリンクに関して、複合チャネル処理402は、レートマッチング52、トランスポートチャネル多重化54、物理チャネルセグメント化58、ビットスクランブル55、第2のインターリーブ60、および物理チャネルマッピング62の機能を実行する。FDDダウンリンクに関して、複合チャネル処理402は、第2のDTX指示挿入74、物理チャネルセグメント化58、第2のインターリーブ60、および物理チャネルマッピング62の機能を実行する。TDDモード、ならびにFDDモードのアップリンクとダウンリンクの両方に関して、チップレート処理404は、拡散64、スクランブル66、パルス整形フィルタリング68、および周波数補正70の機能を実行する。

【0029】

図1に示すとおり、好ましくは、TDD処理400およびFDD処理403は、次の3つのセクションによって扱われる。すなわち、1)トランスポートチャネル処理401セクション、2)複合チャネル処理402セクション、および3)チップレート処理403セクションである。

【0030】

図2に示した好ましいアーキテクチャでは、送信動作および受信動作について以上のセクションのそれぞれに関して制御ブロックが作成され、合計で6つの処理ブロック（3つの送信と3つの受信）が作成される。以上の制御ブロックの動作は、パラメータ化される。この結果、以上のブロックが動作する形は、ソフトウェアによって変更することができる。これにより、異なる無線環境において同一のハードウェア制御ブロック群を使用することが可能になる。ソフトウェアが存在する無線システムに基づき、ソフトウェアを使用して制御ブロック群のパラメータ変更が行われる。

【0031】

制御ブロック群の柔軟性の例を図4に示し、物理レイヤプロセッサが、3GPPのFDDモードとTDDモードの両方で処理を行うことができる。物理レイヤプロセッサがTDDモードで動作しているか、FDDモードで動作しているかに関わらず、受信複合チャネルプロセッサ303、受信トランスポートチャネルプロセッサ305、送信トランスポートチャネルプロセッサ307、送信複合チャネルプロセッサ309、制御プロセッサ313（ARMプロセッサ、DSPプロセッサ、またはRISCプロセッサなどの）、および共有メモリ/SMA315がすべて利用される。ただし、以上のブロックのそれぞれの機能は、物理レイヤプロセッサ動作モードに応じて変化する。したがって、動作モードがTDDであるか、FDDであるか、またはTSMであるかに依存して、モード変更を可能にする新たなパラメータがブロック群に送られる。

【0032】

TDDとFDDでは送信フォーマットが異なるので、物理レイヤプロセッサは、2つの送信ブロック、TDD送信チップレートプロセッサ311およびFDD送信チップレートプロセッサ306を有する。同様に受信側でも、2つの受信ブロック、TDDチップレートプロセッサ301およびFDD受信チップレートプロセッサ304が使用される。TDDチップレートプロセッサ301は、マルチユーザ検出デバイスを使用することなどにより、TDDフォーマットの信号を検出する。FDDチップレートプロセッサ304は、Rakeレシーバを使用することなどにより、FDDフォーマットの信号を検出する。

【0033】

物理レイヤプロセッサがTDDモードで動作している場合、TDD受信チップレートプロセッサ301およびTDD送信チップレートプロセッサ311が、その他の6つの共通で利用されるコンポーネントとともに利用される。物理レイヤプロセッサがFDDモードで動作している場合、FDD受信チップレートプロセッサ304およびFDD送信チップレートプロセッサ306が、その他の6つの共通で利用されるコンポーネントとともに利用される。

【0034】

TDDモードとFDDモードの間で要求されるハードウェアの違いは、チップレートレシーバ301、304、およびトランスミッタ311、306だけなので、実質的に同一のハードウェアブロック群を使用することにより、FDD物理レイヤプロセッサ、TDD物理レイヤプロセッサ、またはFDD/TDD両方の物理レイヤプロセッサを実装することができる。類似した形で、これらのハードウェアブロック群を3GPPのTDDモードおよびFDDモード以外の無線システムのために利用することもできる。

【0035】

TDDモードだけを実行する物理レイヤプロセッサを実装するため、図4のハードウェアブロック群をFDD受信チップレートプロセッサ304およびFDD送信チップレートプロセッサ306なしで使うことができる。逆に、FDDモードだけを実行する物理レイヤプロセッサを実装するため、図4のハードウェアブロック群をTDD受信チップレートプロセッサ301およびTDD送信チップレートプロセッサ311なしで使うことができる。この結果、受信複合チャネルプロセッサ303、受信トランスポートチャネルプロセッサ305、送信トランスポートチャネルプロセッサ、および送信複合チャネルプロセッサ307のハードウェア実施形態を様々な無線環境において使うことができ

る。

【0036】

図4は、好ましいFDDモードのユーザ装置（UE）または基地局／ノードBに関するハードウェアコンポーネント群の図である。セル探索316は、UEだけに関することに留意されたい。ユーザ装置／ノードBのアンテナ317またはアンテナアレイを介して信号が受信される。RFレシーバ316が、受信信号の同相のベースバンドサンプルおよび直交位相のベースバンドサンプルを生成する。

【0037】

FDD受信チップレートプロセッサ301は、セル探索－レイク(Rake)フィンガロケータ(Rake finger locator)316、レイク(Rake)フィンガ312、およびデータエスティメータ(estimator)314を含む。セル探索－レイク(Rake)フィンガロケータ316は、セル選択を実行し、受信された通信のパスを探し出して、レイク(Rake)フィンガ312の位相遅延を特定する。レイク(Rake)フィンガ312は、受信信号の複数のパスのエネルギーを収集する。データ推定314が、複合処理のために受信信号のソフトシンボルを生成する。

【0038】

受信複合チャネルプロセッサ303が、データ推定314によって生成されたソフトシンボルに対して複合処理を実行する。受信トランスポートチャネルプロセッサ307は、デインターリーブ(de-interleaver)／デレートマッチャ(de-rate matcher)52、ターボデコーダ41、ビタビデコーダ43、およびCRCデコーダ42を含む。デインターリーブ／デレートマッチャは、第1のインターリーブおよび第2のインターリーブの逆、ならびにレートマッチングの逆を実行する。ターボエンコーダ41は、ターボ符号化された信号を復号化し、ビタビデコーダは、畳み込み符号化された信号43を復号化する。CRCデコーダ42は、受信信号のCRCを復号化する。制御プロセッサ313およびSMA315コントロール316の指示の下で、FDD受信チップレートプロセッサ301、受信複合チャネルプロセッサ303、およびトランスポートチャネルプロセッサ305を使用して、受信信号からネットワークデータが回復される。

【0039】

送信側で、ネットワークデータが、送信トランスポートチャネルプロセッサ307、送信複合チャネルプロセッサ309、およびFDD送信チップレートプロセッサ311によって処理されて、同相の信号および直交位相の信号が生成される。送信トランスポートチャネルプロセッサ307、送信複合チャネルプロセッサ309、およびFDD送信チップレートプロセッサ311は、制御プロセッサ313およびMEM/SMAコントローラ316によって指示されて適切な処理を実行する。同相の信号および直交位相の信号は、RFモジュレータ308によって変調されたRF信号に変換され、無線インタフェースを介してアンテナ317Aまたはアンテナアレイによって放射される。

【0040】

図6は、データが、送信のために、どのように共有メモリ314と複合ブロック群の間で伝送されるかを示している。受信の場合、このプロセスは、逆向きに実行される。例えば、時間伝送間隔(TTI)が4に設定された場合、処理されるべきデータの4つの伝送ブロック、TrB1k0 251~TrB1k3 257が存在する。SMA315は、メモリを共有メモリ314の送信バッファ265の中に入れる。10ミリ秒である各フレーム時間において、SMA315は、データのブロックをトランスポートチャネルプロセッサ307に伝送し、プロセッサ307において、CRC付加およびチャネル符号化などの処理が行われる。処理が完了した時点で、またはほとんど終わった時点で、SMA315は、処理済みのデータブロックを共有メモリ314内部の第1のインターリーブバッファ267の中に移動させる。TTIは、この例では40ミリ秒に設定されているので、SMA315は、10ミリ秒(1フレーム)ごとにインターリーブバッファ267の4分の1を複合チャネルプロセッサ309に伝送する。処理が完了した後、またはほぼ完了した後、SMA315は、結果を共有メモリ314内部の物理チャネルバッファ269の中に

入れる。次に、フレーム分のデータは、SMA315を介してチップレートプロセッサ311に伝送される。処理済みのデータは、RFモジュレータに送られて、無線インタフェースを介して放射される。

【0041】

図7は、3GPPによる、長さ10ミリ秒のフレームに対する上述の送信処理に関するパイプラインタイミングを示している。2つのトランスポートチャンネル、および関連する符号化された複合チャンネルが、フレームN-2 295内で構成され、それらのチャンネル上でデータが即時に送信される。送信フレームコンポーネント群が、フレームN-1 296内のデータを処理し、送信チップレート処理が、符号化済みの複合トランスポートチャンネル_1 (CCTrch_1) の最初の無線 (over-the-air) フレームであるフレームN 297内で行われる。各水平領域は、システム内の計算コンポーネントを表し、パイプラインにおける段階である。各プロセッサの活動は、それぞれ、ボックス401~482で表している。各水平領域内の複数の活動ボックスは、それらがシステム内で通常、出現する順序で現れる。矢印を有する破線は、時間依存関係を表す。例えば、1つのプロセッサが処理タスクを終了した場合、そのプロセッサは、別のプロセッサが自らの処理タスクを開始することができるように別のプロセッサに通信する。

【0042】

時刻N-2 295に、構成トランスポートチャンネル1メッセージが、送信フレームソフトウェア401によって受領される。さらに、構成CCTrchチャンネル1 402メッセージ、構成トランスポートチャンネル2 403メッセージが、送信フレームソフトウェアによって受領される。トランスポートチャンネル1 406の送信データ、およびトランスポートチャンネル_2 407の送信データは、送信フレームソフトウェアによって受領される。

【0043】

時刻N-1 296に、新たな構成が、アクティブなデータベースにマージされる409。送信フレームソフトウェアが、トランスポートチャンネル1に関する制御ブロックを共有メモリに書き込み、次に、処理411を開始するように送信トランスポートプロセッサに告げる。送信フレームソフトウェアは、トランスポートチャンネル2に関する制御ブロックを共有メモリに書き込み、次に、新たな制御ブロックをトランスポートチャンネル1に関する制御ブロックにリンクするか、または処理413を開始するように送信トランスポートプロセッサに告げる。送信フレームソフトウェアが、CCTrch1に関する送信複合制御ブロックを共有メモリに書き込み、処理415を開始するように送信複合プロセッサに告げる。送信チップソフトウェアが、フレームNのタイムスロット1に関する制御ブロックを共有メモリに書き込む。

【0044】

時刻N 297に、送信チップソフトウェアが、フレームNのタイムスロット2に関する制御ブロックを共有メモリ419に書き込む。送信フレームソフトウェアは、cctrch1に関する送信複合制御ブロックを共有メモリに書き込むことを開始し、処理421を開始するように送信複合プロセッサに告げる。送信チップソフトウェアは、送信フレームソフトウェアを中断し、フレームNのタイムスロット2に関する制御ブロックを共有メモリ423に書き込む。送信フレームソフトウェアは、cctrch1に関する送信複合制御ブロックを共有メモリに書き込むことを完了させ、処理425を開始するように送信複合プロセッサに告げる。

【0045】

送信トランスポートが、トランスポートチャンネル1に関するトランスポートデータを読み取り、インターリーブされたデータの4つのフレームを共有メモリ440に出力する。送信トランスポートは、制御ブロックおよびトランスポートデータをトランスポートチャンネル2に関する共有メモリから読み取り、インターリーブされたデータの4つのフレームを共有メモリ442に出力する。

【0046】

送信複合プロセッサが、制御ブロック、トランスポートチャネル1の出力データの第1のフレーム、およびトランスポートチャネル2の出力データの第1のフレームを読み取る。送信複合プロセッサは、このデータを処理し、リソースユニットデータを共有メモリに書き込む。送信複合プロセッサは、送信トランスポートプロセッサが、トランスポートチャネル1およびトランスポートチャネル2の両方に関するインターリーブされたデータ460を書き込むことを完了するまで、待たなければならない。送信複合プロセッサは、制御ブロック、トランスポートチャネル1の出力データの第2のフレーム、およびトランスポートチャネル2の出力データの第2のフレームを読み取る。送信複合プロセッサは、このデータを処理して、リソースユニットデータを共有メモリ462に書き込む。

【0047】

チップレートプロセッサが、`cctrch1`の第1のOTAフレームの第1のタイムスロットに関するリソースユニットデータを読み取り、ソフトシンボル480を出力する。送信チップレートプロセッサが、`cctrch1`の第1のOTAフレームの第2のタイムスロットに関するリソースユニットデータを読み取る。これに続き、送信チップレートプロセッサは、`cctrch1`の第1のOTAフレームの第3のタイムスロットに関するリソースユニットデータを読み取り、ソフトシンボル482を出力する。

【0048】

好ましいソフトウェア設計は、送信フレームが、図8に最上レベルの状態図で示すメッセージベースのイベント駆動型システムであることであり、このシステムは、メッセージループ待ち201で開始する。着信する構成メッセージにより、メッセージループ待ち201の状態変化が生じさせられ、データベースの中にデータを入れる、またはデータベースの中のデータを更新するサービスへのコールがもたらされる。例えば、システムは、ハードウェア初期設定を要し、状態変化が、メッセージループ201待ちで検出され、ハードウェアを初期設定する209コールが実行される。コールからリターンすると、保留中データベース更新233ファンクションが呼び出され、妥当なデータベースへのハードウェア構成データ伝送が行われる。すべての構成変更およびデータ伝送が行われた時点で、メッセージループ待ち201が、実行(N)225ファンクションを呼び出す。このファンクションは、最後のフレームティック(tick)203以来、いずれのデータベースが更新または変更されているかに関する情報を保持するデータベースレジスタを生じさせる。

【0049】

フレームティックは、上記の3GPPの例では、10ミリ秒ごとに生じ、メッセージループ待ち201によって検出される。システムは、フレームティック203サブルーチンに入る。前述した実行(n)225ファンクションからデータベースレジスタの中でセマフォが設定された(semaphored)データベース群が、更新され205、データ処理のセットアップおよび開始207が実行される。

【0050】

`TrCh`構成209、`TrCh`解放211、無線リンク構成215、無線リンク解放217、物理チャネル解放219のさらなる状態は、メッセージループ201が探すその他のルーチンの例である。`TrCh`データ221ルーチンは、ブロック伝送をセットアップするサブルーチンである。

【0051】

図5は、制御ブロック群、および共有メモリアクセススキームを使用する本発明のリンクリストスキームの図である。ハードウェアレジスタ151が、メモリ制御ブロック155の開始アドレスを含む。パラメータおよびデータが2つ以上のブロックにわたる場合、リンクリストメカニズムにより、シームレスな伝送が可能になる。例えば、制御ブロック155が、リンクリストとしてメモリの中に存在し、リストの最後のエントリ、第2の制御ブロック165へのポインタが存在する。

【0052】

メモリアクセスが、プロセッサ313またはSMA315によって提供される。例えば、ハードウェアレジスタ151が、パラメータおよびデータがロードされた制御ブロック

155の開始アドレスを有する。動作の際、SMA315またはプロセッサ313による連続的なメモリアクセスにより、複合ブロック群へのデータ伝送、および複合ブロック群からのデータ伝送が可能になる。

【0053】

例えば、制御ブロック155内の最初のセットのパラメータ154は、アドレス0100hで始まる。メモリアドレスポインタがまず、0100hに設定され、パラメータ154が伝送される。メモリアドレスポインタは、0104hである次のメモリアドレスにインクリメントされ、パラメータ157が伝送される。メモリアドレス指定がアドレス0118hに達するまで、このプロセスが繰り返される。

【0054】

011Chで、プロセッサ313またはSMA315が、初期セットアップによるか、または011C8hに位置するデータの中のフラグにより、メモリアドレスポインタをデータブロック_1 162の最初のアドレスと入れ替える。次に、データブロック_1内のデータが、順次に伝送される。伝送が完了すると、メモリアドレスポインタは、元に戻るように入れ替えられ、インクリメントされて、制御ブロック155のアドレス0120hをポイントし、これにより、メモリアドレスポインタがやはり入れ替えられて、データブロック_2 164の追加のデータを順次に獲得する。

【0055】

データブロック_2 164から戻ると、メモリアドレスポインタは、Next_Chain_Address160である0124hにある。このアドレスに位置するデータは、パラメータ166、ならびにデータブロック176~180をそれぞれポイントするデータブロックアドレス168~174も含む次の制御ブロック165の最初のアドレスである。このリンクリストの終りには、リンクリストの終りを示すフラグ174が存在する。

【0056】

共有メモリ315からの好ましいブロックロードプロセスの例を図10に示している。通常の実施形態では、デュアルポートメモリ群への書き込みアクセスに関連するタイミング問題が存在する。特に書き込み操作を実行している際、2つ以上のエンティティが同一のメモリ域にアクセスしようと試みた場合、競合が生じる。この問題を解決する1つの可能な好ましいアプローチは、複合/トランスポートプロセッサがアイドルである場合に制御ブロック書き込みを許すことである。

【0057】

新たなブロックが利用可能になると202、複合/トランスポートプロセッサがアイドル204であるかどうかを調べる検査が行われる。複合/トランスポートプロセッサがビジーである場合、チェーンポインタが上書きされ208、制御は、プロセッサのステータスを調べる検査を行うことにループして戻る。複合/トランスポートプロセッサがアイドルである場合、共有メモリアクセス(SMA)ポインタが書き込まれ206、データ書き込みが開始される210。さらなる制御ブロックの検査212が実行される。さらなる制御ブロックが存在する場合、制御は、プロセッサステータス検査202にループして戻る。さらなる制御ブロックが存在する場合、ブロックロードが完了し、システムは戻る214。

【0058】

TDDモードにおける送信のための物理レイヤ処理の好ましい実施形態を、制御ブロック群のパラメータ化を例示するために以下のとおり説明する。送信可能なデータを生成するため、制御ブロック群、送信トランスポートチャネルプロセッサ307、送信複合チャネルプロセッサ309、および送信チップレートプロセッサ311が利用される。データの最初のブロック群が、共有メモリ315から送信トランスポートチャネルプロセッサ307に送られる。トランスポートブロックが生成され、巡回冗長検査(CRC)がCRC付加プロセッサ42においてそれぞれの新たなトランスポートブロックに追加される。好ましい実施形態では、0ビット、8ビット、12ビット、16ビット、および24ビット

のCRCを含む通常のCRCタイプが生成される。

【0059】

表1は、送信トランスポートチャネルプロセッサ307ブロックにロードされるソフトウェアパラメータのリストである。

【0060】

【表1】

制御ブロック パラメータ	コメント／説明
サービス品質 (Quality of Service)	CRC CRCビット数/4 符号化タイプ 00=なし 01=ターボ 10=1/2conv 11=1/3conv インターリーブレート 00=10ミリ秒 01=20ミリ秒 10=40ミリ秒 11=80ミリ秒
モード	NCOL-P (インターリーブマトリックス内の列の数) 00=P 01=P+1 10=P+1およびK=C*R 11=P-1 MACヘッダ埋め込みビット
連番	各トランスポートチャネルを特定するのに使用される
トランスポートブロック 数	トランスポートチャネルにおけるトランスポートブロック数
トランスポートブロック サイズ	最後の32ビットの入力語におけるビット数 0は32を意味する トランスポートブロック当たりのビット数 32の次の倍数に切り上げられた
エンコーダ入力サイズ	エンコーダに入力されたビットの総数から1を引いた数
エンコーダ出力サイズ	第1のインターリーブパから出力された32ビット語の総数
符号化ブロックサイズ	エンコーダブロック当たりのビット数
符号化ブロック充填ビッ ト	第1の符号ブロック内の充填ビットの数
ターボインターリーブ制 御	トランスポートチャネルにおける行の数 原始根 素数
ターボインターリーブ素 数テーブル	ターボインターリーブ用の素数テーブル(10語)
インターリーブメモリア ドレス	TTIにかかわらず8つのアドレスであるフレーム宛先アドレス
トランスポートブロック メモリアドレス	トランスポートブロックソースアドレス トランスポートブロック当たりに1つ
次のT r C H制御ブロッ クアドレス／終了	次のトランスポートチャネル(処理すべきさらなるチャネルが存在 する場合)に関する制御ブロックに対するポインタ ビット31が設定されたNULL(0の値)ポインタにより、もはやトラン スポートチャネルが存在しないことが示される(すなわち、最後の トランスポートチャネルを示すのに0x80000000という値が常に使 用される)

表 1

【0061】

T r B l k連結／符号ブロックセグメント化プロセッサ44が、伝送時間間隔(T T I

）分のトランスポートブロックを作成し、ただし、ブロックの数は、特定の送信チャネル向けに選択されたトランスポートフォーマットに依存する。また、セグメント化プロセッサ44は、ブロックを連結して単一のエンティティにすることも行う。

【0062】

所与のトランスポートチャネルに関する符号ブロックが、チャネルコーダプロセッサ46に送られる。入力データファイルの中で指定された所与のトランスポートチャネルに関する符号化タイプに依存して、符号ブロックは、適切なチャネルコーダファンクションに送られる。表1を参照すると、ビット10およびビット11が、所望されるタイプの符号化に設定されている。これらのビットが00に設定されている場合、符号化は、全く行われない。これらのビットが01、10、および11に設定されている場合、符号化は、それぞれ、レート1/2畳み込み符号化、レート1/3畳み込み符号化、およびターボ符号化である。好ましい実施形態において可能な符号化のタイプは、3GPP TSG-RANの「多重化およびチャネル符号化」3GPP TS 25. 212によって定義される。このパラメータ化可能なハードウェアベースのアプローチにより、高い性能レベルで、例えば、畳み込み符号化の場合はビット当たり1クロック、ターボ符号化の場合はビット当たり2クロックで符号化を行うことが可能になる。これは、同一の機能が通常どおり、（クロックレート当たり）ソフトウェアで実行された場合よりも10倍ないし100倍速い。

【0063】

チャネル符号化後、符号化済みのブロックが、無線フレーム等化45プロセスにおいてレートマッチングプロセスによって順次に処理される。これにより、符号化済みのブロックの連結が実質的に実施される。次に、出力が、第1のインターリーブ50プロセスに送られる。インターリーブは、やはり表1の中のソフトウェアパラメータであるTTIインターリーブレートに依存する。例えば、10ミリ秒のインターリーブの場合、00が、サービス品質（Quality of Service）レジスタのビット8およびビット9に設定される。20ミリ秒、40ミリ秒、および80ミリ秒のTTIの場合、それぞれ01、10、および11という値が、ビット8およびビット9に設定される。データは、無線フレームセグメント化プロセス50においてセグメント化され、送信複合チャネルプロセッサ309ブロックに準備ができて共有メモリ315に戻される。

【0064】

送信複合チャネルプロセッサ309ブロックは、共有メモリ315から制御パラメータとならんでデータを抽出し、物理チャネルデータを生成する。無線フレーム分のデータが、所与のトランスポートチャネルに関する先行するブロックの第1のインターリーブから出力されたデータから集められる。

【0065】

表2は、送信複合チャネルプロセッサ309の制御ブロックのフォーマットパラメータテーブルである。

【0066】

【表2】

TrCH制御ブロック パラメータ	説明
Number Bits Before Rate Matching This Trch	そのTrCHに関する第1のインターリーブバッファの現在の列 (フレーム)内のビット数
Number Leftover Bits This Trch	バンクチャリングまたは繰り返しが考慮されないトランス ポートチャネルの末尾のビット数 ターボバンクチャのために使用される、P2ビット
Rate Matching Direction	ビットシーケンスが{S, P1, P2} (順方向)であるか、または {P2, P1, S} (逆方向)であるかを示す。 ターボバンクチャのために使用される、P2ビット
Rate Matching Type	TURBO_PUNCTURE、REPEAT、NON_TURBO_PUNCTURE、またはNONE を示す
Rate Matching Column Top	列内の最初のビットがシステマティック(S)ビットであるか、 パリティ1(P1)ビットであるか、またはパリティ2(P2)ビットで あるかを示す
std_e_init1	第1のシーケンスに関するレートマッチングパラメータの初期 値
std_e_plus1	ビットがバンクチャリングされる、または繰り返される場合の 誤りに対するインクリメント値
std_e_minus1	ビットが第1のインターリーブバッファから読み取られる場合 の誤りに対するデクリメント値
std_e_init2	第2のシーケンスに関するレートマッチングパラメータの初期 値 ターボバンクチャのために使用される、P2ビット
std_e_plus2	ビットがバンクチャリングされる、または繰り返される場合の 誤りに対するインクリメント値 ターボバンクチャのために使用される、P2ビット
std_e_minus2	ビットが第1のインターリーブバッファから読み取られる場合 の誤りに対するデクリメント値 ターボバンクチャのために使用される、P2ビット
Start Address This Trch	トランスポートチャネルの開始メモリアドレス

表 2

【0067】

例えば、レートマッチングパラメータが、ビット28および29を使用する。これらのビットが00に設定されている場合、これは、TURBO_PUNCTUREモードを示す。同様に、REPEAT、NON_TURBO_PUNCTURE、およびNONEが、パラメータレジスタのビット位置28および29に01、10、および11をそれぞれ入れることによって表される。

【0068】

データは、トランスポートチャネル(TrCH)多重化プロセス54において他のチャネルで多重化される前に、レートマッチングプロセス52によってレートマッチングが行われる。トランスポートチャネル多重化プロセッサ54の出力が、物理チャネル(PyC

H) 57プロセッサにおいて物理チャネルにセグメント化される。第2のインターリーブが、第2のインターリーブプロセッサ46によって実行され、物理チャネルプロセッサ62において物理チャネルにマップされる。次に、送信チャネル処理済みのデータが、送信チップレートプロセッサによるさらなる処理のために共有メモリ315に戻される。

【0069】

次に、送信チップレートプロセッサ311ブロックが、共有メモリ315からデータおよび制御パラメータを抽出する。好ましいTDD実施形態では、ブロック311は、拡散、スクランブル、利得の印加、フォーマット、プリアンブル挿入、RRCフィルタリングを実行し、タイムスロットあたりに1ないし16のリソースユニットを生成する。送信のための送信チップレートプロセッサ311のI出力およびQ出力。

【0070】

図11は、好ましい送信構成タイムライン500を示し、パラメータ変更可能なハードウェア実施形態の利点を示している。フレームは、メッセージタイムライン502上のフレームマーカー503によって境界が定められている。フレームN409で信号を送信するため、Execute_N510で処理が開始される前に、送信のためのデータが、フレームN-2505中に構成されなければならない。フレームNに関するデータは、フレームN-1中に処理され、フレームマーカー503(n)までに完全に処理され、送信される準備ができていなければならない。

【0071】

データベースタイムライン504上の時刻N-2505に、送信チャネルのフレームハードウェアが構成される。時刻N-1507に、開始制御信号がSMA313から送られ、データベースからのブロック処理が開始される。処理は、送信フレーム受領プロセッサ群を構成する送信トランスポートチャネルプロセッサ307および送信複合チャネルプロセッサ309において実行される。時刻N509には、送信チッププロセッサ311が、データベースから受け取ったデータを処理している。

【0072】

物理チャネル処理を通るデータの流れを示すため、図12は、FDD送信に関するデータの好ましい流れの図である。図12で、トランスポートチャネルが、符号化され、4でインターリーブされて2つの物理チャネルに入れられる。トランスポートチャネル1102およびトランスポートチャネル2104に関するデータが、トランスポートチャネル処理106にSMA伝送されて、処理106においてCRCが追加され、データが符号ブロックにセグメント化される。ブロックが符号化され、レートマッチングが行われ、第1のインターリーブが実行される。送信チャネルデータ108~122のブロックとしてのデータが、共有メモリに送られる。次に、データは、複合チャネル処理124に送られ、処理124において、フレーム当たり1回のレートでレートマッチングが行われ、第2のインターリーブが行われ、物理チャネルにセグメント化される。物理チャネルデータは、フレーム別の物理チャネル126~128として並べられて共有メモリに送られる。次に、フレームデータ別の物理チャネルは、チップレート処理130に送られ、処理130において、フレームごとに拡散、スクランブルが行われ、フィルタ処理される。制御チャネルもそれぞれの生成されたフレームに付加される。

【0073】

各チャネルプロセッサに関する一連の「ジョブ」が、ソフトウェアによってスケジュール設定され、共有メモリの中に保持されるリンクリストキューを介してプロセッサ群に与えられる。各処理ユニットは、共有メモリの中に存在する制御ブロック群を介して「ジョブ」を受け取る。各制御ブロックの内容は、そのブロックが制御を行うユニットの機能である。データ、およびデータの順序は、各ユニットの機能および仕様によって定義される。各制御ブロックにおけるエントリには、ユニットに関する制御パラメータ、ならびに入力データをポイントするアドレス、および出力データ位置に対するアドレスが含まれる。制御ブロックは、一緒にリンクして制御プロセッサのオーバーヘッドを小さくすることができる。

【0074】

TDDモードにおける受信信号の物理レイヤ処理に関して、好ましいパラメータテーブルを表3に示す。

【0075】

【表3】

名 前	説明
il2 Disable	第2のインターリーブ無効
Descr Disable	デスクランブラ (Descrambler) 無効
Number TrCH	CCTrCHにおけるTrCHの数
Number Interleaver Blocks	CCTrCHにおけるILBの数
Interleaver Block Size	そのILB内のビット数
Number Ts Blocks	ILB内のタイムスロット数
Number Full Columns	第2のインターリーブマトリックス内の全列 (full columns) の数
Number Rows	30列のインターリーブアレイにおける行の数
Ts Block Size	ビット数単位のタイムスロットデータブロックサイズ
Number resource units (Rus)	タイムスロット内のRUの数
RU Size	RUデータブロックサイズ (ソフト決定 (soft decision) の数)
RU ConsecutiveSize	RUから読み取られた連続するソフトビットの数
RU Offset	逆の順序でデータがマップされているRUの最初のデータ語の先頭からのオフセット
RU Address	RUデータの開始アドレス
RU Direction	RUに関するデータは、進む順序にも逆の順序にもマップすることができる

表 3

【0076】

例えば、第2のインターリーブを無効にするのに、「il2 Disable」のビット16を1に設定する。制御パラメータおよびデータのブロックが、共有メモリ315から受信複合チャネルプロセッサ303ブロックに伝送される。

【0077】

図13は、受信構成タイムライン700を表している。フレームは、メッセージタイムライン702上のフレームマーカー703によって境界を定められている。受信信号がフレームN705でキャプチャされた場合、受信されたデータは、フレームN+1711およびフレームN+2713のフレーム中に処理される。フレームN+3で、受信されたデータは、高位レイヤの処理に準備ができています。

【0078】

時刻N-1703に、特定の受信されたフレームに関するハードウェア構成のためのソフトウェアパラメータが、保留中のデータベースの中で用意されていなければならない。時刻N709に、受信チップレートプロセッサ301が、そのデータをデータベースに入れる。時刻N+1711に、受信複合チャネルプロセッサ303および受信トランスポートチャネルプロセッサ305から成る受信フレームプロセッサが、受信されたデータ

を処理し、次に、そのデータをより高位のレイヤに送る。

【図面の簡単な説明】

【0079】

【図1】第3世代パートナーシッププロジェクト（3GPP）の広帯域符号分割多重アクセス（W-CDMA）の標準の時分割双方向（TDD）モードおよび周波数分割双方向（FDD）モードに関する物理レイヤ処理を示す概念図である。

【図2】物理レイヤプロセッサを示す簡略図である。

【図3】共有メモリアービタレータ（SMA）を示す高レベルのブロック図である。

【図4】FDDモードおよびTDDモードで機能することができる物理レイヤプロセッサを示す簡略図である。

【図5】FDDユーザ装置またはノードB／基地局を示す簡略図である。

【図6】データがどのように共有メモリから送信プロセッサに移動されるかを示す図である。

【図7】10ミリ秒時間間隔の構成限度を示すタイムラインのタイミング図である。

【図8】送信フレームソフトウェア構造を示す状態図である。

【図9】通常の制御ブロックの共有メモリアービタ（SMA）ハードウェアレジスタおよび擬似メモリマップを示す図である。

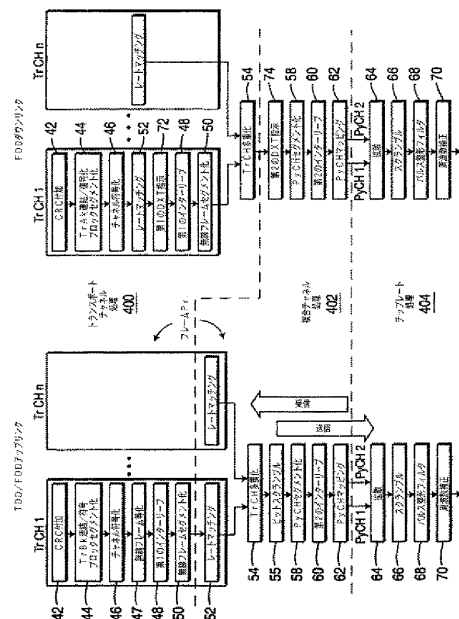
【図10】制御プロセッサから共有メモリへのブロックローディングプロセスを示す流れ図である。

【図11】送信構成タイムラインを示すタイミング図である。

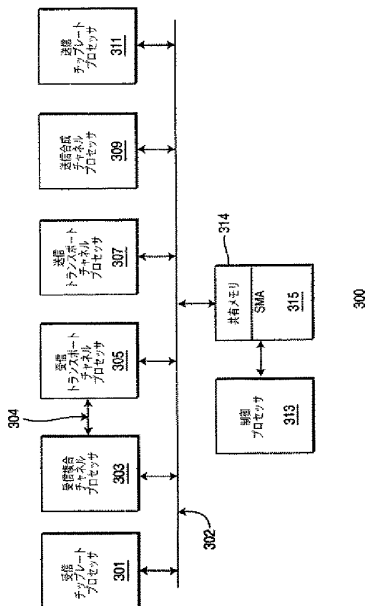
【図12】送信チャネル処理、複合チャネル処理、およびチップレート処理の間のデータフローを示す図である。

【図13】受信構成タイムラインを示すタイミング図である。

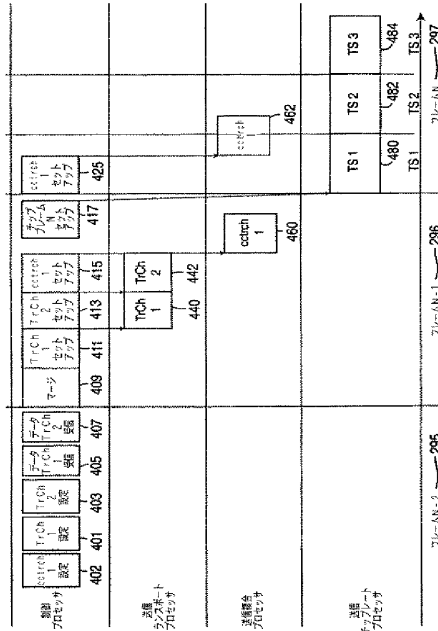
【図1】



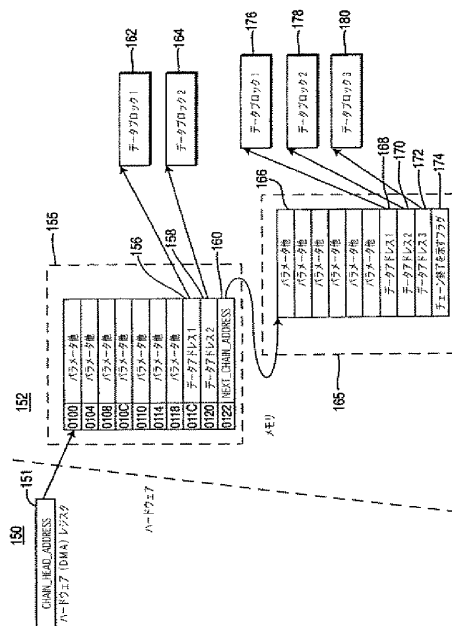
【図2】



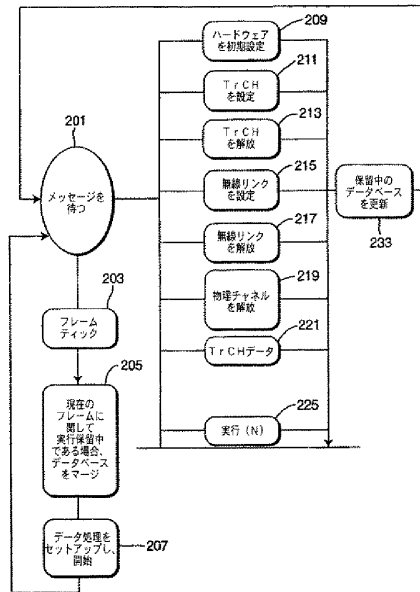
【☒7】



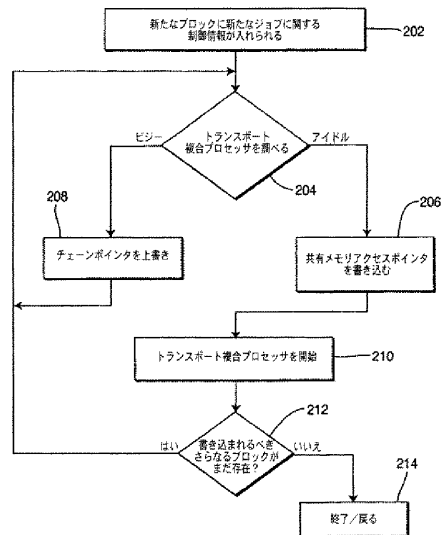
【☒9】



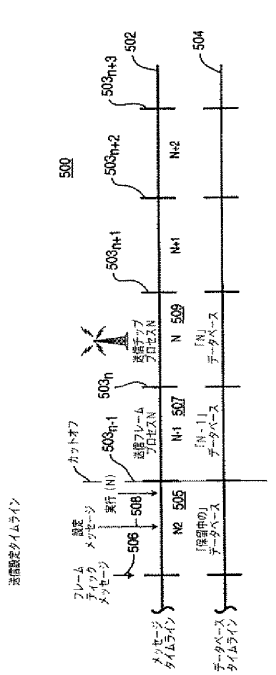
【例8】



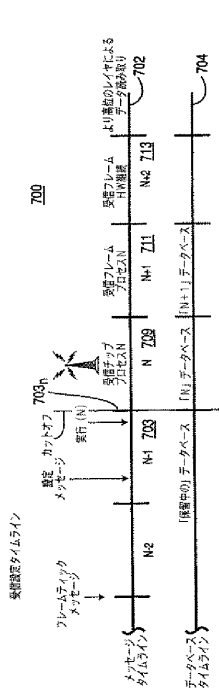
【 ㊦10 】



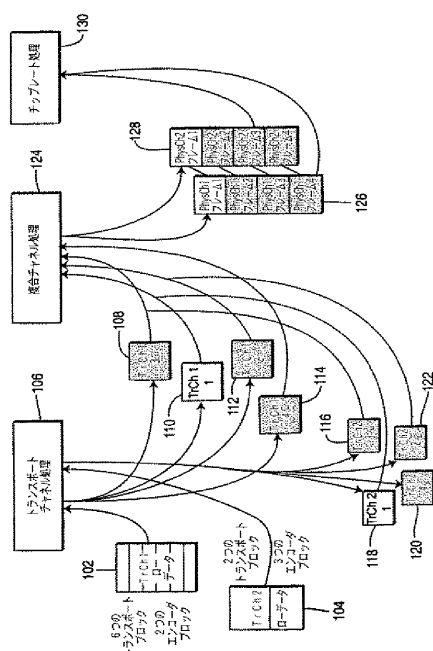
【図11】



【図13】



【図12】



INTERNATIONAL SEARCH REPORT		International application No. PCT/US05/11415												
A. CLASSIFICATION OF SUBJECT MATTER IPC(7) : H04J 4/00 US CL : 370/277 According to International Patent Classification (IPC) or to both national classification and IPC														
B. FIELDS SEARCHED Minimum documentation searched (classification system followed by classification symbols) U.S. : 370/277 Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)														
C. DOCUMENTS CONSIDERED TO BE RELEVANT														
Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.												
A	US 5,987,010 A (SCHNIZLEIN) 16 NOVEMBER 1999, ALL	1-49												
A	US 6,094,421 A (SCOTT) 25 JULY 2000, ALL	1-49												
☐ Further documents are listed in the continuation of Box C. ☐ See patent family annex.														
<table border="0"> <tr> <td>* Special categories of cited documents:</td> <td>"T" Inter document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention</td> </tr> <tr> <td>"A" document defining the general state of the art which is not considered to be of particular relevance</td> <td>"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone</td> </tr> <tr> <td>"E" earlier document published on or after the international filing date</td> <td>"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art</td> </tr> <tr> <td>"L" document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reasons (as specified)</td> <td>"A" document member of the same patent family</td> </tr> <tr> <td>"O" document referring to an oral disclosure, use, exhibition or other means</td> <td></td> </tr> <tr> <td>"P" document published prior to the international filing date but later than the priority date claimed</td> <td></td> </tr> </table>			* Special categories of cited documents:	"T" Inter document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention	"A" document defining the general state of the art which is not considered to be of particular relevance	"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone	"E" earlier document published on or after the international filing date	"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art	"L" document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reasons (as specified)	"A" document member of the same patent family	"O" document referring to an oral disclosure, use, exhibition or other means		"P" document published prior to the international filing date but later than the priority date claimed	
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Form PCT/ISA/210 (second sheet) (July 1998)*

INTERNATIONAL SEARCH REPORT

International application No.
PCT/US08/11415

Box I Observations where certain claims were found unsearchable (Continuation of item 1 of first sheet)

This international report has not been established in respect of certain claims under Article 17(2)(a) for the following reasons:

1. ☐ Claims Nos.:
because they relate to subject matter not required to be searched by this Authority, namely:

2. ☐ Claims Nos.:
because they relate to parts of the international application that do not comply with the prescribed requirements to
such an extent that no meaningful international search can be carried out, specifically:

3. ☐ Claims Nos.:
because they are dependent claims and are not drafted in accordance with the second and third sentences of Rule 6.4(a).

Box II Observations where unity of invention is lacking (Continuation of item 2 of first sheet)

This International Searching Authority found multiple inventions in this international application, as follows:

1. ☐ As all required additional search fees were timely paid by the applicant, this international search report covers all
searchable claims.
2. ☐ As all searchable claims could be searched without effort justifying an additional fee, this Authority did not invite payment
of any additional fee.
3. ☐ As only some of the required additional search fees were timely paid by the applicant, this international search report
covers only those claims for which fees were paid, specifically claims Nos.:

4. ☐ No required additional search fees were timely paid by the applicant. Consequently, this international search report is
restricted to the invention first mentioned in the claims; it is covered by claims Nos.:

Remark on Protest

- ☐ The additional search fees were accompanied by the applicant's protest.
☐ No protest accompanied the payment of additional search fees.

Form PCT/ISA/210 (continuation of first sheet(1)) (July 1998)*

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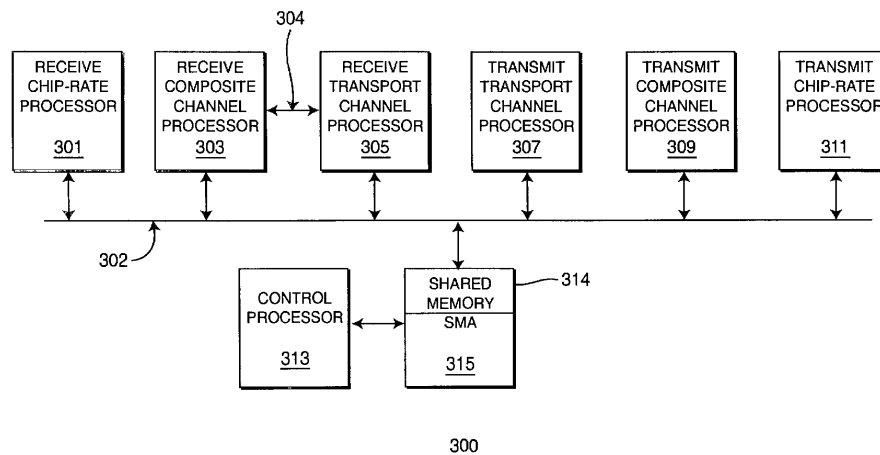
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(54) Title: SOFTWARE PARAMETERIZABLE CONTROL BLOCKS FOR USE IN PHYSICAL LAYER PROCESSING



(57) Abstract: A physical layer transport composite processing system used in a wireless communication system. A plurality of interconnected processing blocks are provided. The blocks are interconnected by a read data bus, a write data bus and a control bus. The blocks include a transport channel processing block, a composite channel processing block and a chip rate processing block. At least two of the blocks are capable of processing data for a plurality of wireless formats. A first set of parameters is programmed into the blocks for a particular wireless mode. The blocks are operated to process data in the particular wireless format mode.

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[0001] SOFTWARE PARAMETERIZABLE CONTROL
BLOCKS FOR USE IN PHYSICAL LAYER PROCESSING

[0002] BACKGROUND OF THE INVENTION

[0003] The invention generally relates to wireless communication systems. In particular, the invention relates to processing data at the physical layer for such systems.

[0004] In wireless communication systems, data received from the network is formatted for transfer over the wireless interface. Conversely, data received over the wireless interface is processed to recover the original network data. The processing of this data is referred to as physical layer processing.

[0005] Processing data at the physical layer is a complex operation in wireless communication systems. Figure 1 is a conceptual illustration of physical layer processing for the proposed time division duplex (TDD) mode for wideband code division multiple access (W-CDMA) of the proposed third generation partnership project (3GPP). The processing is shown for the transmitter. In an analogous reverse manner, the data is processed at the receiver. However, one difference with physical layer processing at the receiver is that the receiver typically processes soft symbols complicating the processing requirements. Figure 1 also pertains conceptually to the uplink of the frequency division duplex (FDD) mode of W-CDMA. However, the parameters used by each block differ between TDD and FDD.

[0006] Transport blocks arrive for transport over the wireless interface. The transport blocks arrive in sets of transport block sets. The sets are received in a specified time interval, known as transmission time interval (TTI). For the TDD mode, and FDD mode the possible TTI lengths are 10ms, 20ms, 40ms and 80ms, which correspond to 1, 2, 4 and 8 radio frames, respectively. A circular redundancy code (CRC) attachment block 42 attaches CRC bits to each transport block. The CRC bits are used for error detection at the receiver. The CRC bit length is signaled from higher layers.

[0007] The transport blocks (TrBlks) are serially concatenated by the TrBlk concatenation/code block segmentation block 44. If the number of bits of the concatenated blocks is larger than the maximum size allowed for a code block, the concatenated blocks are segmented. A channel coding block 46 error correction encodes the code blocks, such as by convolutional coding, turbo coding. After encoding, the code blocks are concatenated together. If the concatenated code blocks can not be segmented into a minimum number of equal sized segments (frames), radio frame equalization is performed by concatenating additional arbitrary bits by a radio frame segmentation block 50.

[0008] A first interleaver 48 interleaves all the concatenated data. Subsequently, the interleaved data is segmented into radio frames by a radio frame segmentation block 50. A rate matching block 52 punctures or repeats bits. The puncturing and repeating assures data transmitted on each physical channel equals the maximum bit rate for that channel. The rate matching attributes for each transport channel (TrCH) is signaled by higher layers.

[0009] The TrCH multiplexing block 54 receives one frame's data for each transport channel. The received data for each TrCH is serially multiplexed onto a coded composite transport channel (CCTrCH). A bit scrambling block 65 scrambles the CCTrCH bits.

[0010] A physical channel segmentation block 58 maps the multiplexed data onto the physical channels. A second interleaver 60 interleaves the scramble data either over the entire radio frame or over each time slot. After second interleaving, the interleaved data is segmented into the physical channels for transport over the air interface by a physical channel mapping block 62.

[0011] The data for each physical channel is spread using a respective code by a spreading block 64. The spread data is scrambled using a scrambling block 66 with a code associated with the base station. Each resulting scrambled chip is pulse shaped by a pulse shape filter 68. A frequency correction block 70 adjusts the frequency of the resulting signal. The frequency corrected signal is radiated through the wireless interface.

[0012] For the downlink of FDD mode as also shown in Figure 1, the processing is performed in a similar manner conceptually. However, there are some differences. In the FDD downlink, rate matching is performed after the channel coding by a rate matching block 52. As a result, radio frame equalization is not performed. To support discontinuous transmission, a first discontinuous transmission (DTX) indication is inserted prior to first interleaving by a first DTX indication block 72 and a second DTX indication is inserted prior to physical channel mapping by a second DTX indication block 74.

[0013] Two approaches for performing physical layer processing are a software based approach and a hardware based approach. In a software based approach, the bulk of the physical layer processing is performed by software. A software based approach allows for great flexibility. Parameters of the physical layer processing can be easily changed by software revisions.

[0014] Two drawbacks with a software based approach are that: 1) processors, such as microprocessors or DSPs use higher power than customized solutions, and 2) several processors may be needed to carry out all the required functionality.

[0015] A hardware based solution allows for a reduction in total chip area required and reduced power consumption. Customizing and configuring the hardware for a particular environment, the n better efficiencies in the data processing. However, such an approach reduces the flexibility of the design. Reconfiguration of the physical layer processing is limited to parameters made available in the initial design.

[0016] Accordingly, it is desirable to have a physical layer processing which allows for high processing speed and flexibility.

[0017] SUMMARY

[0018] A physical layer transport composite processing system used in a wireless communication system. A plurality of interconnected processing blocks are provided. The blocks are interconnected by a read data bus, a write data bus and a control bus. The blocks include a transport channel processing block, a

composite channel processing block and a chip rate processing block. At least two of the blocks are capable of processing data for a plurality of wireless formats. A first set of parameters is programmed into the blocks for a particular wireless mode. The blocks are operated to process data in the particular wireless format mode.

[0019] BRIEF DESCRIPTION OF THE DRAWING(S)

[0020] Figure 1 is a conceptual illustration of physical layer processing for the standard time division duplex (TDD) and frequency division duplex (FDD) modes for wideband code division multiple access (W-CDMA) of the third generation partnership project (3GPP).

[0021] Figure 2 is a simplified diagram of a physical layer processor.

[0022] Figure 3 is a high level block diagram of the shared memory arbitrator (SMA).

[0023] Figure 4 is a simplified diagram of a physical layer processor capable of functioning in FDD and TDD modes.

[0024] Figure 5 is a simplified diagram of a FDD user equipment or Node-B/base station.

[0025] Figure 6 illustrates how data is moved from shared memory to transmit processors.

[0026] Figure 7 is a timeline illustrating the 10 millisecond time interval configuration limit.

[0027] Figure 8 is a state diagram of the transmit frame software structure.

[0028]

[0029] Figure 9 is a diagram of a shared memory arbiter (SMA) hardware register and a pseudo memory map of typical control blocks.

[0030] Figure 10 is a flowchart of the block loading process from the control processor to shared memory.

[0031] Figure 11 is a timing diagram of the transmit configuration timeline.

[0032] Figure 12 is an illustration of data flow between transmit channel processing, composite channel processing and chip rate processing.

[0033] Figure 13 is a timing diagram of the receive configuration timeline.

[0034] DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENT(S)

[0035] The present invention will be described with reference to the drawing figures wherein like numerals represent like elements throughout. Although the physical layer processing is primarily described in conjunction with the preferred implementation of the TDD and FDD modes of 3GPP, the physical layer processing is applicable to other systems, such as time division synchronous code division multiple access (TD-SCDMA), TSM, CDMA 2000 as well as others.

[0036] An overview of the preferred physical layer system architecture 300 is illustrated in Figure 2. The physical layer system can be used at either a base station/Node-B of a wireless communication system or at a user equipment. The preferred architecture allows for flexibility in design of the physical layer processing across differing wireless environments, such as TDD, FDD modes of the proposed 3GPP W-CDMA system and GSM.

[0037] Blocks 301, 303, 305, 307, 309 and 311 represent a suite of software parametizable leveraged embedded processors and are also known as virtual circuits (VCs). A receive chip-rate processor 301 is connected to a data read bus, a data write bus and a control bus, hereinafter the three are to be known as the system bus 302. The receive composite channel processor 303 block and receive transport channel processor 305 block are also connected to the system bus 302. In addition, the two blocks also have a sequential number bus that reports to the receive transport channel processor 305 which data block is ready for transport channel processing. The transmit transport channel processor 307, transmit composite channel processor 309 and transmit chip-rate processor 311 blocks are also connected to the system bus 302. The shared memory/ shared memory arbiter (SMA) 315 block is connected to the system bus 302 and to the control processor 313 block. In the preferred implementation, the block's functionality is

designed to perform the physical layer processing of either TDD, FDD or both modes of the 3GPP, although in other implementations other physical layer processing approaches may be performed by the blocks.

[0038] The control processor 313 communicates with processing blocks via control queues in the shared memory 314 via the SMA 315. The control processor 313 places set-up and control data into specific shared memory locations to act as data registers for each control block. The shared memory is also utilized as a data block place holder to transfer data amongst the processing blocks. This is preferably achieved through linked lists which transfers data in blocks, with the last element of each block being an address of a next data block or an end of data indicator. This technique reduces buffering in the physical layer processor. The control processor 313 is preferably an advance RISC machine (ARM) processor. Alternately, it may be any embedded processor.

[0039] The Shared Memory Arbiter (SMA) 315 is a hardware only virtual circuit (VC) that controls access to a memory shared by the main VCs and the control processor 313. The SMA unit contains address registers and the sequencing logic necessary to allow all of the VCs and the processors to efficiently share access to the memory.

[0040] A high level block diagram of a SMA is illustrated by Figure 12. The SMA unit contains address registers 601 and the sequencing logic necessary to allow all of the VCs and the processors to efficiently share access to the shared memory 314. The SMA accepts one request into its pipeline every clock cycle , provided there are pending request(s). The SMA address generator maintains a register for each SMA channel containing the address for the next memory access to be performed on that channel. These registers must be initialized to the first memory address of the memory block to be accessed. Each address register has an associated control bit that is configured by software to indicate if an address pointer is to be incremented or decremented after each access.

[0041] There are three types of memory channels: 1) read channel data is transferred from shared memory to the requesting unit, 2) write channel data is transferred from the requesting unit to the shared memory, and 3) control

channels (special read channels) support two types of memory access, read access, as for a normal read channel and load access. Load access is used to transfer a memory pointer from shared memory into one of the address registers in the SMA. This allows an efficient implementation of a linked list.

[0042] Each hardware component is assigned one or more SMA channels, and transfers to and from memory are controlled by a request/grant handshake on each SMA channel. Request signals are prioritized in order to guarantee timely access on critical paths. Once a request is in the pipeline, the same request will not be accepted into the pipeline again, until the grant is sent.

[0043] When a receive chip rate processor 301 has completed its processing, it will send a request 603 to the SMA. The SMA 315 will prioritize the request 603 and allocate a memory address via the address register 601 for the shared memory 314. The SMA will then send a write grant 605 to the requesting source, to begin data transfer.

[0044] One potential implementation for the physical layer processing system is to process either or both the TDD and FDD modes of a 3GPP system. In such an implementation, referring back to Figure 1, the various processing blocks are divided into three general processes, transport channel processing 400, composite channel processing 402 and chip rate processing 404. Transport channel processing 400 is performed on the transport channels. Composite channel processing 402 is performed on the composite channels and is performed on a frame by frame basis and chip rate processing 404 is also performed on a timeslot by timeslot basis.

[0045] As shown in Figure 1 for TDD and FDD uplink processing, the transport channel processing performs the functions of CRC attachment 42, transport block concatenation 44, channel coding 46, radio frame equalization 47, first interleaving 48 and radio frame segmentation 50.

[0046] For the FDD downlink, the transport channel processing 400 includes the functions of CRC attachment 42, transport block concatenation 44, channel coding 46, rate matching 52, first DTX indication insertion 72, first interleaving 48, radio frame segmentation 50 and transport channel multiplexing

54. It should be noted that in TDD mode, the de-rate matching 52 may be performed in wither the transport or composite processor.

[0047] For the TDD mode and the FDD uplink, the composite channel processing 402 performs the functions of rate matching 52, transport channel multiplexing 54, physical channel segmentation 58, bit scrambling 55, second interleaving 60 and physical channel mapping 62. For the FDD downlink, the composite channel processing 402 performs the functions of second DTX indication insertion 74, physical channel segmentation 58, second interleaving 60 and physical channel mapping 62. For the TDD mode and both the uplink and downlink of FDD mode, the chip rate processing 404 performs the functions of spreading 64, scrambling 66, pulse shape filtering 68 and frequency correction 70.

[0048] As shown in Figure 1, preferably TDD and FDD processing 400, 403 is handled by three sections: 1) a transport channel processing 401 section, 2) a composite channel processing 402 section, and 3) a chip rate processing 403 section.

[0049] In the preferred architecture as shown in Figure 2, control blocks are created for each of these sections for the transmit and receive operations, totaling six processing blocks (three transmit and three receive). The operations of these controls blocks is parametrized. As a result, the manner at which these blocks operate can be changed by software. This allows for the same hardware control blocks to be used in differing wireless environments. Software is used to reparameterize the control blocks based on the wireless system it resides.

[0050] An illustration of the flexibility of the control blocks is shown in Figure 4, the physical layer processor capable of processing in both 3GPP FDD and TDD modes. The receive composite channel processor 303, receive transport channel processor 305, transmit transport channel processor 307, transmit composite channel processor 309, the control processor 313 (such as a ARM, DSP or RISC processor) and shared memory/ SMA 315 are all utilized whether the physical layer processor is operating in TDD or FDD mode. However, the functions of each of these blocks are changed depending on the physical layer

processor operating mode. Therefore depending whether the mode of operation is TDD, FDD or TSM, new reparameters are sent to the blocks allowing mode change.

[0051] Since the transmission formats in TDD and FDD differ, the physical layer processor has two transmit blocks, a TDD transmit chip-rate processor 311 and an FDD transmit chip-rate processor 306. Similarly, on the receive side, two receiver blocks are used, a TDD chip-rate processor 301 and a FDD receive chip-rate processor 304. The TDD chip rate processor 301 detects TDD formatted signals, such as by using a multi-user detection device. The FDD chip rate processor 304 detects FDD formatted signals, such as by using a Rake receiver.

[0052] When the physical layer processor is operating in TDD mode, the TDD receive chip-rate processor 301 and the TDD transmit chip-rate processor 311 are utilized along with the other six commonly utilized components. When the physical layer processor is operating in FDD mode, the FDD receive chip-rate processor 304 and the FDD transmit chip-rate processor 306 are utilized along with the other six commonly utilized components.

[0053] Since the only hardware difference required between the TDD and FDD modes is the chip-rate receivers 301, 304 and transmitters 311, 306, by using substantially the same hardware blocks either an FDD, TDD or both FDD/TDD physical layer processor can be implemented. In an analogous manner, these hardware blocks could be utilized for wireless systems other than the TDD and FDD modes of the 3GPP.

[0054] To implement a physical layer processor performing only TDD mode, the hardware blocks of Figure 4 can be used without the FDD receive and transmit chip rate processors 304, 306. Conversely, to implement a physical layer processor performing only FDD mode, the hardware blocks of Figure 4 can be used without the TDD receive and transmit chip rate processors 301, 311. As a result, the receive composite channel processor 303, receive transport channel processor 305, transmit transport channel processor and transmit composite channel processor 307 hardware implementations can be used in various wireless environments.

[0055] Figure 4 is an illustration of the hardware components for either a preferred FDD mode user equipment (UE) or base station/Node-B. It should be noted that the cell search 316 is only for UEs. Signals are received over an antenna 317 or an antenna array of the user equipment/Node-B. An RF receiver 316 produces in-phase and quadrature baseband samples of the received signals.

[0056] The FDD receive chip-rate processor 301 comprises a cell search and Rake finger locator 316, Rake fingers 312 and data estimator 314. The cell search and Rake finger locator 316 performs cell selection and locates the paths of received communications to identify the phase delays for the Rake fingers 312. The Rake fingers 312 collect the energy of the multiple paths of the received signals. The data estimation 314 produces soft symbols of the received signals for composite processing.

[0057] The receive composite channel processor 303 performs the composite processing on the soft symbols produced by the data estimation 314. The receive transport channel processor 307 comprises a de-interleaver/de-rate matcher 52, a turbo decoder 41, a Viterbi decoder 43 and a CRC decoder 42. The de-interleaver/de-rate matcher performs an inverse of the first and second interleaving as well as an inverse of the rate matching. The turbo decoder 41 decodes turbo encoded signals and the Viterbi decoder decodes convolutionally encoded signals 43. The CRC decoder 42 decodes the CRCs of the received signals. Under the direction of the control processor 313 and SMA 315 control 316, the network data is recovered from the received signals using the FDD receive chip rate processor 301, the receive composite channel processor 303 and transport channel processor 305.

[0058] On the transmit side, the network data is processed by a transmit transport channel processor 307, transmit composite channel processor 309 and FDD transmit chip rate processor 311 to produce an in-phase and quadrature signal. The transmit transport channel processor 307, transmit composite channel processor 309 and FDD transmit chip rate processor 311 are directed by the control processor 313 and MEM/SMA controller 316 to perform the proper processing. The in-phase and quadrature signals are converted to a modulated

RF signal by a RF modulator 308 and radiated by an antenna 317A or antenna array through the wireless interface.

[0059] Figure 6 illustrates how data is transferred between the shared memory 314 and the composite blocks for transmission. For reception, the process is performed in the reverse. For example, if the time transmission interval (TTI) is set to 4, there are four transmit blocks TrBlk0 – TrBlk3 251 – 257 of data to be processed. The SMA 315 places the memory into the transmit buffer 265 of the shared memory 314. At each frame time, which is 10 ms, the SMA 315 transfers the blocks of data to the transport channel processor 307, where processing such as CRC attachment and channel coding occurs. When processing is complete or just about finished, the SMA 315 moves the processed data blocks into a first interleaver buffer 267 within the shared memory 314. Since the TTI is set to 40 ms In this example, the SMA 315 transfers one-quarter of the interleaver buffer 267 each 10 ms. (one frame) to the composite channel processor 309. After processing is complete or just about completed, the SMA 315 places the results into a physical channel buffer 269 in the shared memory 314. The frame's worth of data is then transferred into the chip rate processor 311 via the SMA 315. The processed data is sent to an RF modulator to be radiated through a wireless interface

[0060] Figure 7 illustrates the pipeline timing for the above transmit processing with frames of ten milliseconds in length, as per 3GPP. Two transport channels and an associated coded composite channel are configured in frame N-2 295 and data is immediately sent on the channels. The transmit frame components process data in frame N-1 296 and the transmit chiprate processing operates in frame N 297, the first over-the-air (OTA) frame for coded composite transport channel_1 (CCTrCh_1). Each horizontal region represents a computational component in the system and is a stage in the pipeline. The activity of each processor is represented by boxes 401 – 482, respectively. The activity boxes in each horizontal region appear in the order in which they will typically occur in the system. The dotted lines with arrows represent time dependencies. For example, when one processor ends a processing task, it

communicates to another processor so that the latter may begin its processing task.

[0061] At time N-2 295, the configure transport channel 1 message is received by transmit frame software 401. In addition the configure CCTrCh channel 1 402, configure transport channel 2 403 messages are received by transmit frame software. The transmit data for transport channel 1 406 and transmit data for transport channel_2 407 are received by transmit frame software.

[0062] At time N-1 296, the new configurations are merged into active database 409. The transmit frame software writes a control block for transport channel 1 to shared memory and then tells transmit transport processor to begin processing 411. The transmit frame software writes control block for transport channel 2 to shared memory, then either links the new control block to the one for transport channel 1 or tells transmit transport processor to begin processing 413. The transmit frame software writes transmit composite control blocks for CCTrCh 1 to shared memory and tells transmit Composite processor to begin processing 415. The Transmit chip software writes control block for time slot 1 of frame N to shared memory.

[0063] At time N 297, the transmit chip software writes control block for time slot 2 of frame N to shared memory 419. The transmit frame software begins to write transmit Composite control blocks for cctrch 1 to shared memory and tells transmit Composite processor to begin processing 421. The transmit chip software interrupts transmit Frame software and writes control block for time slot 2 of frame N to shared memory 423. The transmit frame software completes writing Transmit composite control blocks for cctrch 1 to shared memory and tells transmit composite processor to begin processing 425.

[0064] The transmit transport reads transport data for transport channel 1 and outputs four frames of interleaved data to shared memory 440. The transmit transport reads control block and transport data from shared memory for transport channel 2 and outputs four frames of interleaved data to shared memory 442.

[0065] The transmit composite processor reads control blocks, 1st frame of transport channel 1's output data, and 1st frame of transport channel 2's output data. It processes the data and writes resource unit data into shared memory. The transmit composite processor must wait until the transmit transport processor has completed writing interleaved data for both transport channel 1 and transport channel 2 460. The transmit composite processor reads control blocks, 2nd frame of transport channel 1's output data, and 2nd frame of transport channel 2's output data. It processes the data and writes resource unit data into shared memory 462.

[0066] The chip rate processor reads resource unit data for the first timeslot of the first OTA frame of cctrch 1 and outputs soft symbols 480. The transmit chip rate processor reads resource unit data for the second timeslot of the first OTA frame of cctrch 1 and outputs soft symbols. This is followed by the transmit chip rate processor reading resource unit data for the third timeslot of the first OTA frame of cctrch 1 and outputs soft symbols 482.

[0067] The preferred software design is for the transmit frame to be a message based, event driven system, as shown in the top level state diagram in Figure 8, with the system starting in wait for message loop 201. An arriving configuration messages cause a state change in the wait for message loop 201, bringing about a call to a service routine which places or updates data in a database. For example, the system requires a hardware initialization, the state change is detected in wait for message loop 201 and a call to initialize hardware 209 is performed. Upon return from the call, the update pending database 233 function is called and the hardware configuration data transfer to the pertinent database is carried out. When all configuration changes and data transfers are carried out, the wait for message loop 201 calls the execute(N) 225 function. This function causes a database register which holds information regarding what database have been updated or changed since the last frame tick 203.

[0068] A frame tick occurs every 10 ms. in this 3GPP example and is detected by the wait for message loop 201. The system goes into a frame tick 203 subroutine. The databases that are semaphored in the database register from

the above execute(n) 225 function are updated 205 and a setup and start of the data processing 207 is performed.

[0069] The additional states of configure TrCh 209, release TrCh 211, configure radio link 215, release radio link 217, release physical channels 219 are examples of other routines the message loop 201 look for. The TrCh Data 221 routine is the subroutine that sets up the block transfers.

[0070] Figure 5 is an illustration of control blocks and a linked list scheme using a shared memory access scheme and of the present invention. A hardware register 151 contains the beginning address of a memory control block 155. When parameters and data span over two or more blocks, a linked list mechanism allows for seamless transfers. For example, control block 155 resides in memory as a linked list, its last entry there is a pointer to a second control block 165.

[0071] Memory access is provided by the processor 313 or the SMA 315. For example, the hardware register 151 has the beginning address of control block 155, which is loaded with parameters and data. In operation, consecutive memory accesses by the SMA 315 or the processor 315 allow data transfers to and from the composite blocks.

[0072] For example, the first set of parameters 154 in control block 155 start at address 0100h. A memory address pointer is first set to 0100h and parameters 154 are transferred. The memory address pointer is incremented to the next memory address, which is 0104h and parameters 157 are transferred. This process is repeated until the memory addressing reaches address 0118h.

[0073] At 011Ch the processor 313 or SMA 315 either by initial set up or a by a flag in the data located at 011C8h, and, swaps the memory address pointer with the first address of data block_1 162. The data in data block_1 is then sequentially transferred. Upon completion of the transfer, the memory address pointer is then swapped back and incremented and points to address 0120h of control block 155, which also swaps the memory address pointers to sequentially acquire additional data from data block_2 164.

[0074] Upon returning from data block₂ 164, the memory address pointer is at 0124h which is the Next_Chain_Address 160. The data located at this address is the first address of to the next control block 165, which also comprises parameters 166 and data block addresses 168-174 pointing to data blocks 176-180, respectively. At the end of this linked list is a flag 174 indicating the end of the link lists.

[0075] An illustration of a preferred block loading process from the shared memory 315 is illustrated in Figure 10. In typical implementations, there are timing issues associated with write accesses to dual port memories. Contentions come about when two or more entities try to access the same memory region, especially when performing a write operation. One possible preferred approach to resolve this problem is to allow control block writes when the composite/transport processor is idle.

[0076] As a new block becomes available 202, a check is made to see if the composite/transport processor is idle 204. If the composite/transport processor is busy, the chain pointer is overwritten 208 and the control loops back checking to check the status of the processor. If composite/transport processor is idle, a shared memory access (SMA) pointer is written 206 and the data write is started 210. A check for more control blocks 212 is performed. If there are more control blocks, control loops back to the check processor status 202. If there are more control blocks, the block loading is complete and the system will return 214.

[0077] A preferred embodiment for physical layer processing for transmission in TDD mode is described as follows to illustrate the parameterization of the control blocks. To generate transmittable data, the control blocks transmit transport channel processor 307, transmit composite channel processor 309, and transmit chip-rate processor 311 are utilized. First blocks of data are sent to the transmit transport channel processor 307 block from the shared memory 315. Transport blocks are generated and a cyclical redundancy check (CRC) is added at CRC attachment processor 42 to each new transport block. In the preferred implementation, typical CRC types are generated, including none, 8, 12, 16 and 24 bit CRCs.

[0078] Table 1 is a list of software parameters which is loaded into transmit transport channel processor 307 block.

Control Block Parameters	Comments/Description
Quality of Service	CRC. Number of CRC bits / 4 coding type. 00 = none. 01 = turbo 10 = 1/2 conv. 11 = 1/3 conv. : interleave rate. 00=10ms. 01=20ms. 10=40ms. 11=80ms.
Mode	: NCOL-P (number of columns in the interleaver matrix) 00=P. 01=P+1. 10=P+1 and K=C*R. 11=P-1. : MAC header pad bits
Sequence Number	: used to identify each transport channel.
Number of Transport Blocks	: Number of transport blocks in transport channel.
Transport Block Size	: Number of bits in last 32-bit input word. 0 means 32. : Number of bits per transport block. Rounded up to the next multiple of 32.
Coder Input Size	: Number of total bits input to the coder minus one.
Coder Output Size	: Number of total 32-bit words output from the first interleaver.
Coding Block Size	Number of bits per coder block.
Coding Block Filler Bits	: Number of filler bits in the first code block.
Turbo Interleaver Control	: the Number of rows in the transport channel. : Primitive Root. : Prime Number.
Turbo Interleaver Prime Number Table	Prime Number table for the turbo interleaver (10 words).
Interleaver Memory Addresses	Frame destination addresses, 8 addresses regardless of TTI.
Transport Block Memory Addresses	Transport block source addresses. One per transport block.
Next TrCH Control Block Address/End	Pointer to the control block for the next transport channel (if there are more to process). A NULL (value of 0) pointer with bit 31 set indicates that there are no more transport channels (i.e. a value of 0x80000000 is always used to indicate the last transport channel).

Table 1

[0079] The TrBlk concatenation/code block segmentation processor 44 creates a transmission time interval's (TTI's) worth of transport blocks, where the number of the blocks depends on the transport format selected for a particular Transmit channel. The segmentation processor 44 also concatenates the blocks into a single entity.

[0080] Code blocks for the given transport channel are delivered to the channel coder processor 46. Depending on the coding type for the given transport channel, specified in the input data file, they are delivered to the appropriate channel coder function. Referring to Table 1, bits 10 and 11 are set to the desired type of coding. If the bits are set to 00, there is no coding. If the bits are set to 01, 10 and 11, the coding is Rate 1/2 convolutional, Rate 1/3 convolutional and Turbo, respectfully. The types of coding which are possible in the preferred embodiment are defined by the 3GPP TSG-RAN "Multiplexing and Channel Coding" 3GPP TS 25.212. This parameterizable hardware based approach allows for coding at a high performance level, for example, one clock per bit for convolutional encoding and two clocks per bit for Turbo Encoding. This is ten to one-hundred times faster (per clock rate) than the same function is typically performed in software.

[0081] After channel coding, the coded blocks are processed in sequence by a rate matching process in the radio frame equalization 45 process. This effectively implements a concatenation of encoded blocks. The output is then sent to a first interleaver 50 process. The interleaving depends on the TTI interleaver rate which is also a software parameter in Table 1. For example, a 00 is set into bits 8 and 9 of the Quality of Service register for an interleave of 10 milliseconds. For 20, 40 and 80 ms TTIs, values of 01, 10 and 11, respectively, are set into bits 8 and 9. The data is segmented in the radio frame segmentation process 50 and returned to the shared memory 315 ready for the transmit composite channel processor 309 block.

[0082] The transmit composite channel processor 309 block extracts data from the shared memory 315 along with control parameters and produces physical channel data. A radio frame's worth of data is compiled from the data

output from the previous block's first interleaver for the given transport channel.

[0083] Table 2 is a format parameter table of the transmit composite channel processor's 309 control block.

TrCH Control Block Parameters	Description
Number Bits Before Rate Matching This Trch	The Number of bits in the current column (frame) of the First Interleaver Buffer for this TrCH.
Number Leftover Bits This Trch	The Number of bits at the tail of the transport channel that are not considered for puncturing or repeating. Used for Turbo puncture, P2 bits.
Rate Matching Direction	Indicates whether the bit sequences is {S,P1,P2} (forward) or {P2,P1,S} (reverse) Used for Turbo puncture, P2 bits.
Rate Matching Type	Indicates TURBO_PUNCTURE, REPEAT, NON_TURBO_PUNCTURE, or NONE.
Rate Matching Column Top	Indicates whether the first bit in the column is a systematic (S), parity 1(P1), or parity 2 (P2) bit.
std_e_init1	The initial value of the rate matching parameter for the first sequence.
std_e_plus1	The increment value to the error when a bit is punctured or repeated.
std_e_minus1	The decrement value to the error when a bit is read from the First Interleaver Buffer.
std_e_init2	The initial value of the rate matching parameter for the second sequence. Used for Turbo puncture, P2 bits.
std_e_plus2	The increment value to the error when a bit is punctured or repeated. Used for Turbo puncture, P2 bits.
std_e_minus2	The decrement value to the error when a bit is read from the First Interleaver Buffer. Used for Turbo puncture, P2 bits.
Start Address This Trch	The starting memory address of the transport channel.

Table 2

[0084] For example, the rate matching type parameter uses bits 28 and 29. When these bits are set to 00, this indicates TURBO_PUNCTURE mode.

Likewise, REPEAT, NON_TURBO_PUNCTURE, and NONE are represented by placing 01, 10 and 11, respectively into bit locations 28 and 29 of the parameter register.

[0085] The data is rate matched by rate matching process 52 before it is multiplexed with other channels at the transport channel (TrCH) multiplexing process 54. The output of the multiplex transport channel processor 54 is segmented into physical channels in the physical channel (PyCH) 57 processor. A second interleaving is performed by the second interleaving processor 46 and mapped into physical channels at the physical channel processor 62. The transmit channel processed data is then returned to the shared memory 315 for further processing by the transmit chip-rate processor.

[0086] The transmit chip-rate processor 311 block then extracts data and control parameters from the shared memory 315. In the preferred TDD implementation, the block 311 performs spreading, scrambling, gain application, formatting, preamble insertion, RRC filtering and produces one to sixteen resource units per time slot. The I and Q output of the transmit chip-rate processor 311 for transmission.

[0087] Figure 11 illustrates a preferred transmit configuration timeline 500 and show the advantages of the reparamatizable hardware implementation. The frames are bound by Frame Markers 503 on the Message Timeline 502. To transmit a signal at Frame N 409, the data for the transmission must be configured during Frame N-2 505 before the processing is started at Execute_N 510. The data for Frame N is processed during Frame N-1 and must be completely finished processing and ready to transmit by Frame Marker 503(n).

[0088] At time N-2 505 on the database timeline 504, the frame hardware of the transmit channel is configured. At time N-1 507 the start control signal is sent from the SMA 313 to start the block processing from the database. The processing is performed in the transmit transport channel processor 307 and transmit composite channel processor 309, which make up the transmit frame receive processors. At time N 509, the transmit chip processor 311 is processing the data it received from the database.

[0089] To illustrate the flow of data through physical channel processing, Figure 12 is an illustration of a preferred flow of data for FDD transmission. In Figure 12, the transport channel is encoded and interleaved by a factor of four into two physical channels. The raw data for transport channel_1 102 and transport channel_2 104 are SMA transferred to the transport channel processing 106 where the CRC is added and the data is segmented into code blocks. The blocks are encoded, rate matched and a first interleaving is performed. The data as blocks of transmit channel data 108 - 122 are sent to the shared memory.

The data is then sent to composite channel processing 124 where it is rate matched, second interleaved and segmented into physical channels at the rate of once per frame. The Physical Channel data is sent to the shared memory ordered as physical channels by frame 126 - 128. The physical channels by frame data is then sent to the Chip Rate Processing 130 where it is spread scrambled and filtered on a per frame basis. A control channel is also appended to each generated frame.

[0090] A series of "jobs" for each channel processor are scheduled by software and presented to the processors via linked list job queues maintained in the shared memory. Each processing unit receives "jobs" via control blocks that reside in the shared memory. The content of each control block is a function of the unit for which it controls. The data and the order of the data is defined by the functionality and the specifications of each unit. Entries in each control block include control parameters for the unit and addresses which point to input data and addresses to output data locations. Control blocks can be linked together reducing control processor overhead.

[0091] With respect to the physical layer processing of received signals in TDD mode, a preferred parameters table is shown in Table 3.

Name	Description
il2 Disable	Second Interleaver disable.
Descr Disable	Descrambler disable.
Number TrCH	Number of TrCH in the CCTrCH.
Number Interleaver Blocks	Number of ILBs in the CCTrCH.
Interleaver Block Size	Number of bits in this ILB.
Number Ts Blocks	Number of time slots in the ILB.
Number Full Columns	Number of full columns in the second interleaver matrix.
Number Rows	Number of rows in the interleaver array of 30 columns.
Ts Block Size	Time slot data block size in bits.
Number resource units (RUs)	Number of RUs in the time slot.
RU Size	RU data block size (number of soft decisions).
RU ConsecutiveSize	Number of consecutive soft bits read from RU.
RU Offset	Offset from the start of the first data word of an RU which has data mapped in reverse order.
RU Address	Start address of the RU data.
RU Direction	Data for an RU can be mapped in Forward or Reverse order.

Table 3

[0092] For example, to disable the second interleaving, bit 16 of the “l2 Disable” would be set to a 1. Control parameters and blocks of data are transferred from the shared memory 315 to the receive composite channel processor 303 block.

[0093] Figure 13 represents the receive configuration timeline 700. The frames are bound by frame markers 703 on the message timeline 702. When a received signal is captured at Frame N 705, the received data is processed during frames Frame N+1 711 and Frame N+2 713. At Frame N+3 the received data is ready for high layer processing.

[0094] At time N-1 703, the software parameters for hardware configuration for a particular received frame must be available in the pending database. At time N 709, the receive chip rate processor 301 places the data into the database. At time N+1 711, the received frame processor, which are comprised of the receive composite channel processor 303 and receive transport channel processor 305 process the received data and subsequently sends the data on to higher layers.

CLAIMS

What is claimed is:

1. A wireless user equipment capable of operating in both a time division duplex (TDD) and frequency division duplex (FDD) modes, the user equipment comprising:

a transmit transport channel processor for receiving network data for transmission in either a TDD or FDD mode and processing transport channels of the received network data;

a transmit composite channel processor for receiving the processed transport channels and producing either resource units when operating in the TDD mode and physical channels when operating in a FDD mode;

a FDD transmit chip rate processor for formatting the produced physical channels for transfer over a wireless interface; and

a TDD transmit chip rate processor for formatting the produced resource units for transfer over the wireless interface.

2. The wireless user equipment of claim 1 wherein the transmit transport channel processor, the transmit composite channel processor, the FDD transmit chip rate processor, the TDD transmit chip rate processor, the FDD receive chip rate processor, the TDD transmit chip rate processor, the receive composite channel processor and the receive transport channel processor are coupled to a system bus.

3. The wireless user equipment of claim 1 wherein the system bus comprises a common data read bus, data write bus and control bus.

4. The wireless user equipment of claim 1 wherein the transmit transport channel processor performs CRC attachment, transport block concatenation/code block segmentation, channel coding, radio frame segmentation, first interleaving and radio frame equalization in TDD and FDD modes.

5. The wireless user equipment of claim 1 wherein the transmit composite channel processor performs rate matching, traffic channel multiplexing, bit scrambling, physical channel segmentation, second interleaving and physical channel mapping in TDD and FDD modes.

6. The wireless user equipment of claim 1 wherein the transmit chip rate processor performs spreading, scrambling, pulse shape filtering and frequency correction.

7. The wireless user equipment of claim 1 wherein the transmit transport channel processor, the transmit composite channel processor operate in both FDD and TDD modes and are parameterized by software to operate in a corresponding mode.

8. The wireless user equipment of claim 1 further comprising a radio frequency transmitter for transmitting the produced resource units and produced physical channels through the wireless interface.

9. A wireless user equipment capable of operating in both a time division duplex (TDD) and frequency division duplex (FDD) modes, the user equipment comprising:

- a FDD receive chip rate processor for formatting signals received in a FDD format into physical channels;

- a TDD receive chip rate processor for formatting signals received in a TDD format into resource units;

- a receive composite channel processor for receiving either resource units when operating in TDD mode and physical channels when operating in FDD mode and producing transport channels; and

- a receive transport channel processor for processing the produced transport channels received when operating in either a TDD or FDD mode and processing the received transport channels to produce network data.

10. The wireless user equipment of claim 9 wherein the FDD receive chip rate processor, the TDD receive chip rate processor, the receive composite channel processor and the receive transport channel processor are coupled to a system bus.

11. The wireless user equipment of claim 9 wherein the system bus comprises a common data read bus, data write bus and control bus.

12. The wireless user equipment of claim 9 wherein the receive transport channel processor performs in TDD mode an inverse of CRC attachment, traffic block concatenation/code block segmentation, channel coding, radio frame equalization, first interleaving and radio frame segmentation and in FDD mode an inverse of CRC attachment, traffic block concatenation/code block segmentation, channel coding, rate matching, first discontinuous transmission indication insertion, first interleaving, radio frame segmentation and traffic channel multiplexing.

13. The wireless user equipment of claim 9 wherein the receive composite channel processor performs in TDD mode an inverse of traffic channel multiplexing, bit scrambling, physical channel segmentation, second interleaving and physical channel mapping and in FDD mode an inverse of second discontinuous transmission indicator insertion, physical channel segmentation, second interleaving and physical channel mapping.

14. The wireless user equipment of claim 9 wherein the receive chip rate processor performs an inverse of spreading, scrambling, pulse shape filtering and frequency correction.

15. The wireless user equipment of claim 9 wherein the receive transport channel processor, the receive composite channel processor operate in

both FDD and TDD modes and are parameterized by software to operate in a corresponding mode.

16. The wireless user equipment of claim 9 further comprising a radio frequency receiver for receiving resource units and physical channels over the wireless interface for input into the receive chip rate processor.

17. A wireless Node-B/base station capable of operating in both a time division duplex (TDD) and frequency division duplex (FDD) modes, the user equipment comprising:

- a transmit transport channel processor for receiving network data for transmission in either a TDD or FDD mode and processing transport channels of the received network data;

- a transmit composite channel processor for receiving the processed transport channels and producing either resource units when operating in the TDD mode and physical channels when operating in a FDD mode;

- a FDD transmit chip rate processor for formatting the produced physical channels for transfer over a wireless interface; and

- a TDD transmit chip rate processor for formatting the produced resource units for transfer over the wireless interface.

18. The wireless Node-B/base station of claim 17 wherein the transmit transport channel processor, the transmit composite channel processor, the FDD transmit chip rate processor, the TDD transmit chip rate processor, the FDD receive chip rate processor, the TDD transmit chip rate processor, the receive composite channel processor and the receive transport channel processor are coupled to a system bus.

19. The wireless Node-B/base station of claim 17 wherein the system bus comprises a common data read bus, data write bus and control bus.

20. The wireless Node-B/base station of claim 17 wherein the transmit transport channel processor performs in TDD mode CRC attachment, traffic block concatenation/code block segmentation, channel coding, radio frame equalization, first interleaving and radio frame segmentation and in FDD mode CRC attachment, traffic block concatenation/code block segmentation, channel coding, rate matching, first discontinuous transmission indication insertion, first interleaving, radio frame segmentation and traffic channel multiplexing.

21. The wireless Node-B/base station of claim 17 wherein the transmit composite channel processor performs in TDD mode traffic channel multiplexing, bit scrambling, physical channel segmentation, second interleaving and physical channel mapping and in FDD mode second discontinuous transmission indicator insertion, physical channel segmentation, second interleaving and physical channel mapping.

22. The wireless Node-B/base station of claim 17 wherein the transmit chip rate processor performs spreading, scrambling, pulse shape filtering and frequency correction.

23. The wireless Node-B/base station of claim 17 wherein the transmit transport channel processor, the transmit composite channel processor operate in both FDD and TDD modes and are parameterized by software to operate in a corresponding mode.

24. The wireless Node-B/base station of claim 17 further comprising a radio frequency transmitter for transmitting the produced resource units and produced physical channels through the wireless interface.

25. A wireless Node-B/base station capable of operating in both a time division duplex (TDD) and frequency division duplex (FDD) modes of wideband code division multiple access, the user equipment comprising:

a FDD receive chip rate processor for formatting signals received in a FDD format into physical channels;

a TDD receive chip rate processor for formatting signals received in a TDD format into resource units;

a receive composite channel processor for receiving either resource units when operating in TDD mode and physical channels when operating in FDD mode and producing transport channels; and

a receive transport channel processor for processing the produced transport channels received when operating in either a TDD or FDD mode and processing the received transport channels to produce network data.

26. The wireless Node-B/base station of claim 25 wherein the FDD receive chip rate processor, the TDD receive chip rate processor, the receive composite channel processor and the receive transport channel processor are coupled to a system bus.

27. The wireless Node-B/base station of claim 25 wherein the system bus comprises a common data read bus, data write bus and control bus.

28. The wireless Node-B/base station of claim 25 wherein the receive transport channel processor performs an inverse of CRC attachment, transport block concatenation/code block segmentation, channel coding, radio frame segmentation, first interleaving and radio frame equalization in TDD and FDD modes.

29. The wireless Node-B/base station of claim 25 wherein the receive composite channel processor performs an inverse of rate matching, traffic channel multiplexing, bit scrambling, physical channel segmentation, second interleaving and physical channel mapping in TDD and FDD modes.

30. The wireless Node-B/base station of claim 25 wherein the receive chip rate processor performs an inverse of spreading, scrambling, pulse shape filtering and frequency correction.

31. The wireless Node-B/base station of claim 25 wherein the receive transport channel processor, the receive composite channel processor operate in both FDD and TDD modes and are parameterized by software to operate in a corresponding mode.

32. The wireless Node-B/base station of claim 25 further comprising a radio frequency receiver for receiving resource units and physical channels over the wireless interface for input into the receive chip rate processor.

33. A shared memory arbitrator (SMA) which coordinates data transfers in a plurality of software parameterizable control blocks and a shared memory for use in a wireless communication system, comprising:

- a data bus for loading parameters and data transference in said plurality of software parameterizable control blocks in a physical layer transport composite processing system;

- a plurality of channel requests for requesting parameters and data transference amongst the shared memory and said plurality of software parameterizable control blocks;

- a plurality of grants from the SMA to allow data and parameters transference amongst said plurality of software parameterizable control blocks;
- and

- a data strobe to increment and decrement an address register.

34. The SMA of claim 33, wherein a software parameterizable control block read comprises;

- at least one of said software parameterizable control blocks asserts a channel request;

said at least one of software parameterizable control blocks waits for a grant signal from said SMA;
said at least software parameterizable control blocks strobes data from said shared memory with said data strobe into a local register; and
said SMA increments an address register.

35. The SMA of claim 33, wherein a software parameterizable control block write comprises:

at least one of said software parameterizable control block asserts a channel request;

said SMA registers write data from said at least one software parameterizable control block;

said SMA asserts a grant signal;

said SMA writes data into main memory and increments an address register; and

said at least one software parameterizable control block waits for the grant signal from SMA indicating that data provided by the said at least one software parameterizable control block has been written into memory.

36. The SMA of claim 33, wherein a software parameterizable control block pointer read write comprises:

at least one software parameterizable control block simultaneously asserts a read request and a data request;

said SMA reads a 32-bit word from said shared memory using a first address currently in a control channel address register;

said SMA increments the control channel address register and stores the value read into a first data address register; and

said SMA asserts a grant signal to acknowledge

37. The SMA of claim 33, wherein said SMA is connected to at least one of a plurality of control processors.

38. The SMA of claim 33, wherein said at least control processor is a digital signal processor (DSP).

39. The SMA of claim 33, wherein said at least control processor is an advanced RISC machine (ARM).

40. The SMA of claim 33, wherein a control processor read comprises:
said control processor asserts a request to the SMA;
said SMA asserts a processor read request and sends an address value to the control processor;
said SMA indicatives said processor request is a read request; and
said SMA reads a block of data.

41. The SMA of claim 33, wherein a control processor write comprises:
said control processor asserts a request to the SMA;
said SMA asserts a processor write request and sends an address value to the control processor;
said SMA indicatives said processor request is a write request; and
said SMA writes a block of data.

42. A method for a physical layer transport composite processing for use in processing wireless communications, the method comprising:
providing a plurality of interconnected processing blocks interconnected by a system bus, the plurality of interconnected blocks including a transport channel processing block for processing data on a transport channel basis, a composite channel processing block for processing data on a composite channel basis and a chip rate processing block for processing data associated with

a wireless interface, at least two of the processing blocks capable of processing data for a plurality of wireless formats;

programming a first set of parameters into said plurality of interconnected processing blocks for a particular wireless format; and

operating the interconnected processing blocks to process data in the particular wireless format.

43. The method of claim 42, wherein the system bus comprises a write data bus, a read data bus and a control bus.

44. The wireless user equipment of claim 42 further includes, a receive receiver for receiving signals over the wireless interface and a transmit transmitter for transmitting data over the wireless interface.

45. A physical layer transport composite processor for use in processing wireless communications, comprising:

a plurality of interconnected processing blocks interconnected by a system bus, the plurality of interconnected blocks including a transport channel processing block for processing data on a transport channel basis, a composite channel processing block for processing data on a composite channel basis and a chip rate processing block for processing data associated with a wireless interface, at least two of the processing blocks capable of processing data for a plurality of wireless formats;

a first set of parameters programmed into said plurality of interconnected processing blocks for a particular wireless format; and

said interconnected processing blocks are operated to process data in the particular wireless format.

46. The physical layer transport composite processor of claim 45, wherein the system bus comprises a write data bus, a read data bus and a control bus.

47. The physical layer transport composite processor of claim 45, further including a receiver for receiving signals over the wireless interface and a transmitter for transmitting data over the wireless interface.

48. A method for a wireless user equipment which is capable of operating in both a time division duplex (TDD) and frequency division duplex (FDD) modes of wideband code division multiple access, the user equipment comprises:

- receiving a plurality of network data for transmission in either a TDD or FDD mode;

- processing a first set of transport channels of the received network data in a transmit transport channel processor;

- receiving the processed first set of transport channels and producing either a first set of resource units when operating in the TDD mode and a first set of physical channels when operating in FDD mode in a transmit composite channel processor;

- formatting the produced first set of physical channels for transfer in a FDD transmit chip rate processor;

- formatting the produced first set of resource units in a TDD transmit chip rate processor;

- transmitting the produced physical channels and resource units over a wireless interface in a radio frequency transmitter;

- receiving signals from the wireless interface in a radio frequency receiver;

- formatting the received signals received in a FDD format into a second set of physical channels in a FDD receive chip rate processor;

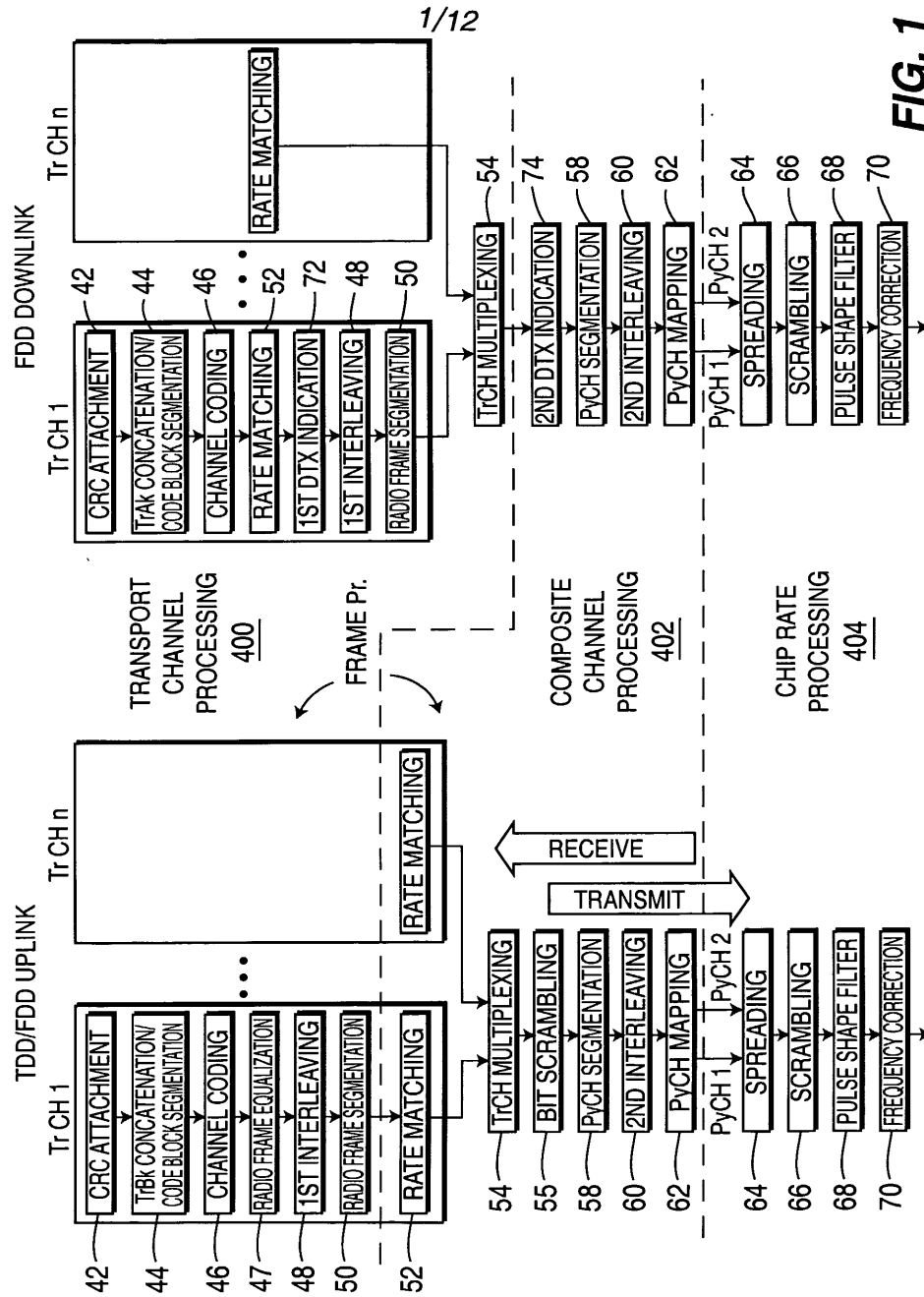
- formatting the received signals received in a TDD format into a second set of resource units in a TDD receive chip rate processor;

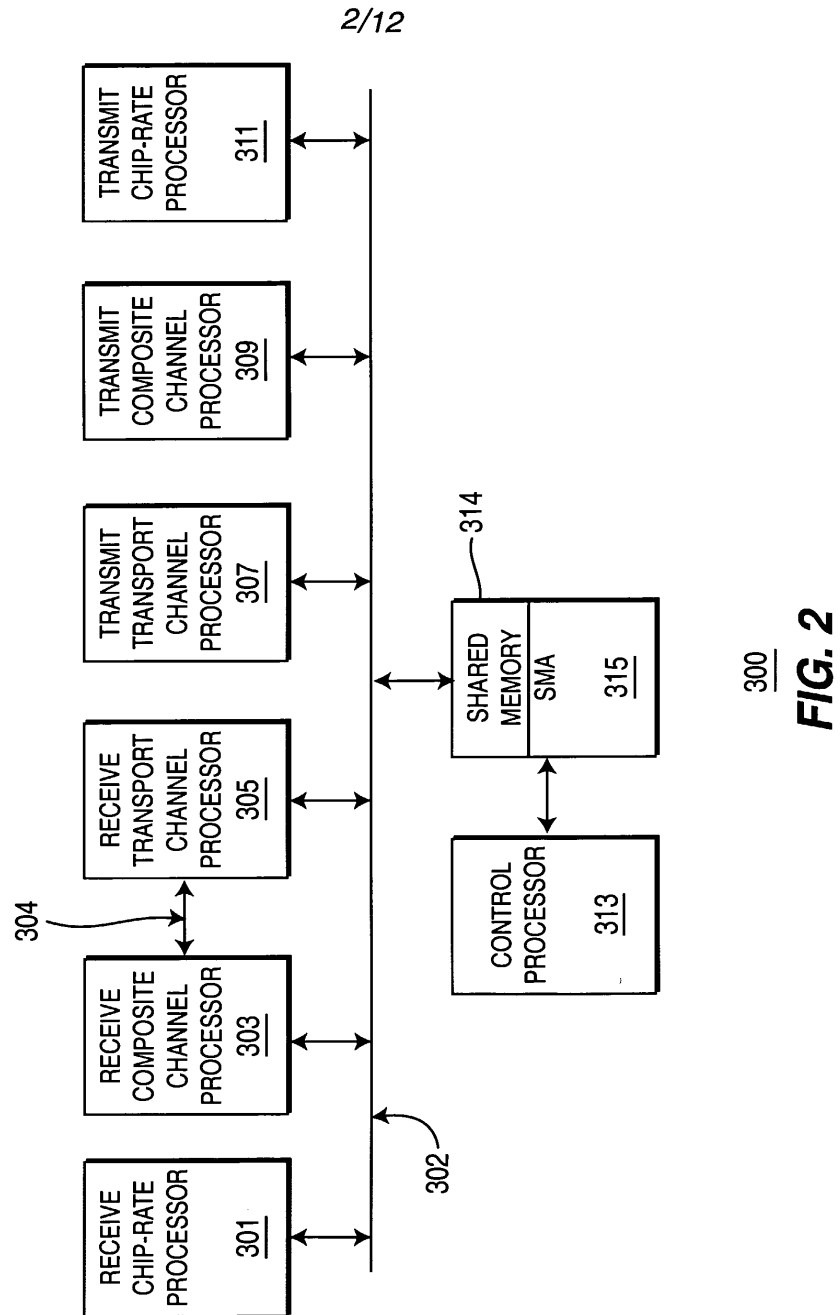
- receiving either the second set of resource units when operating in TDD mode and the second set of physical channels when operating in FDD mode and

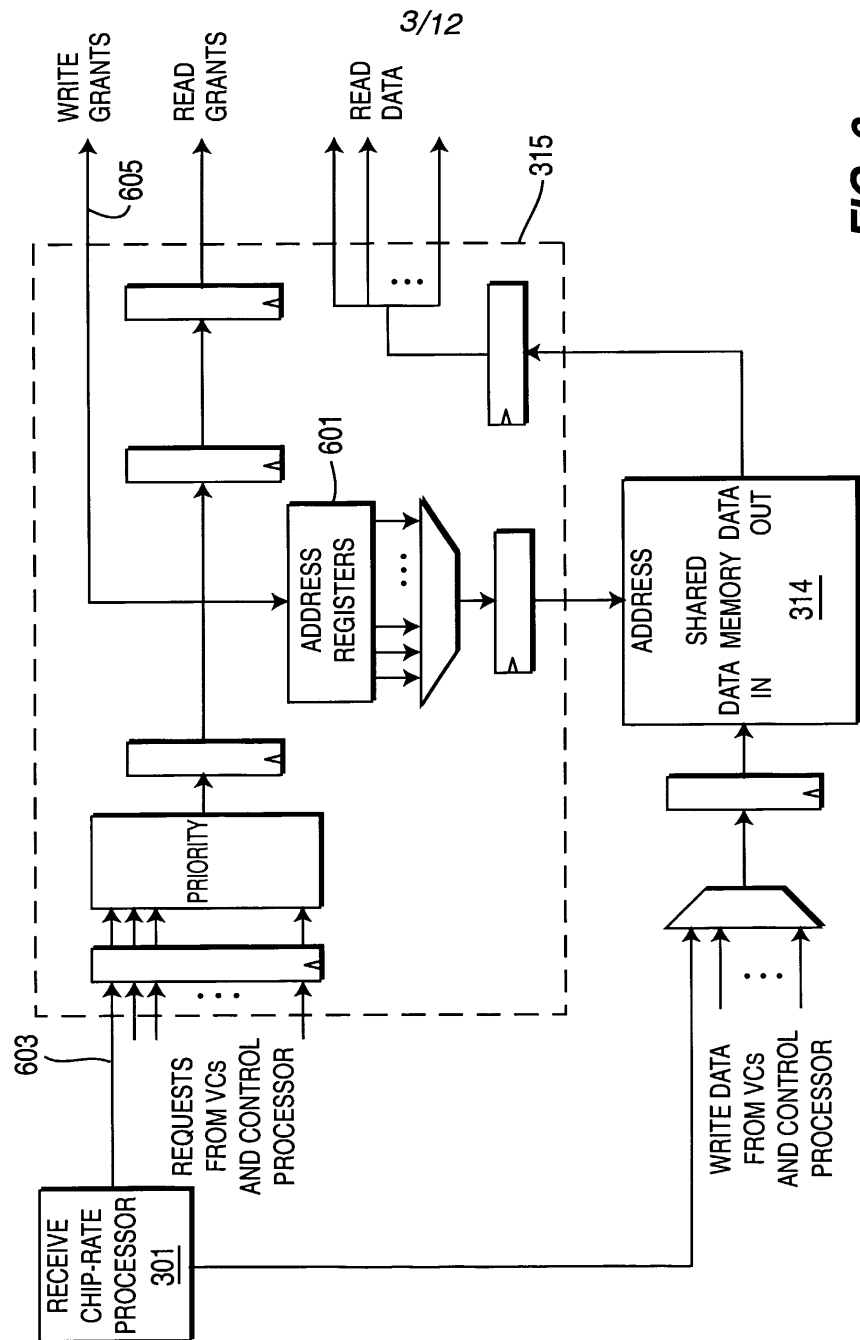
producing a second set of transport channels in a receive composite channel processor; and

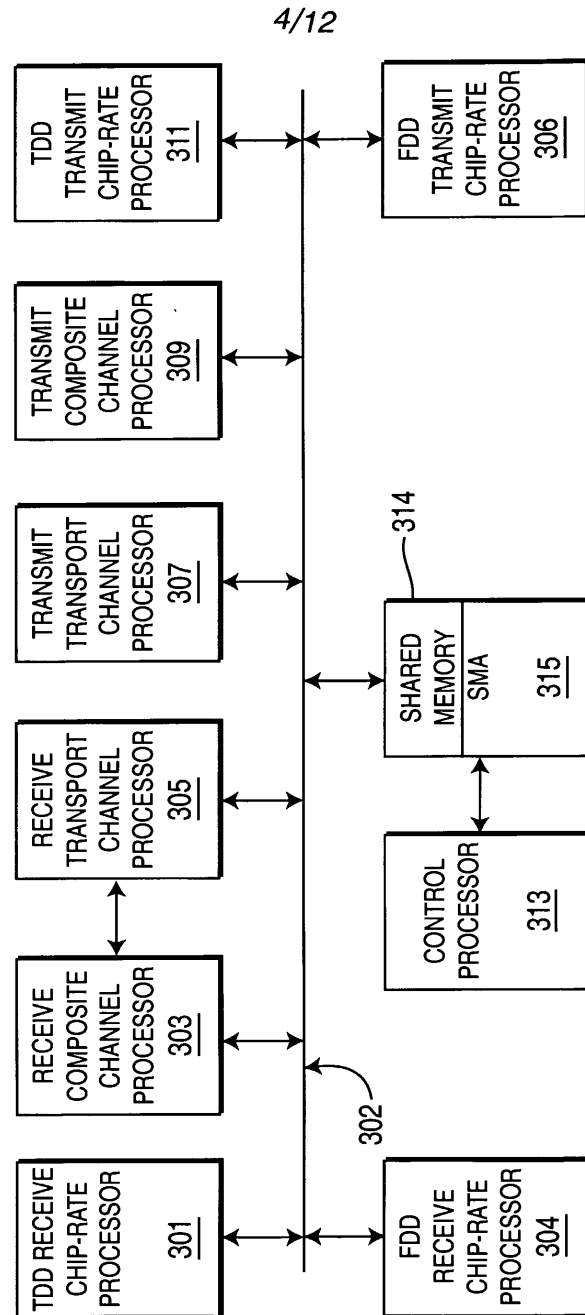
processing the produced second set of transport channels received when operating in either a TDD or FDD mode to produce network data in a receive transport channel processor.

49. The method of claim 48 further comprising coupling a common data read, data write and control bus to the transmit transport channel processor, the transmit composite channel processor, the FDD transmit chip rate processor, the TDD transmit chip rate processor, the FDD receive chip rate processor, the TDD transmit chip rate processor, the receive composite channel processor and the receive transport channel processor.





**FIG. 3**

**FIG. 4**

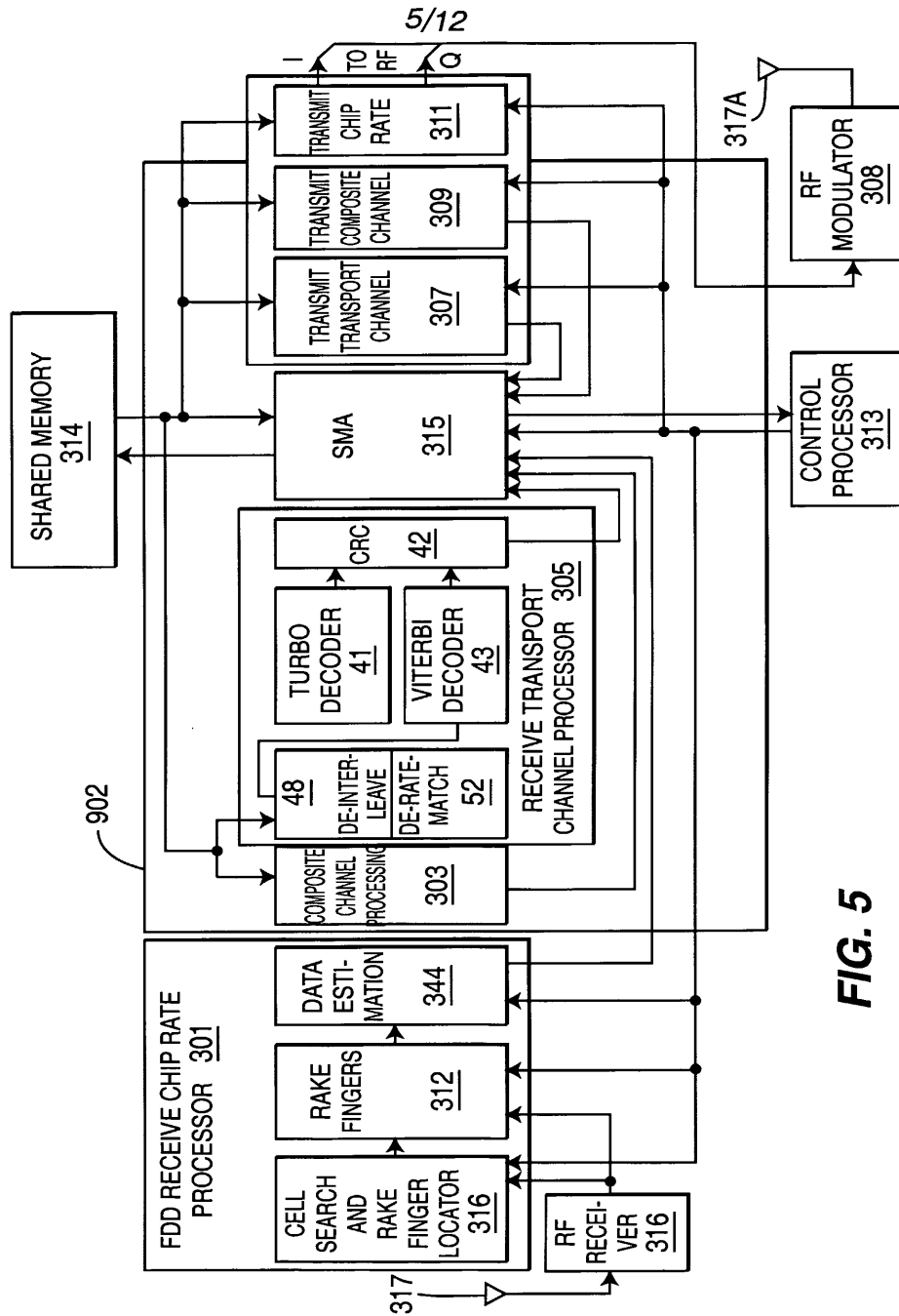


FIG. 5

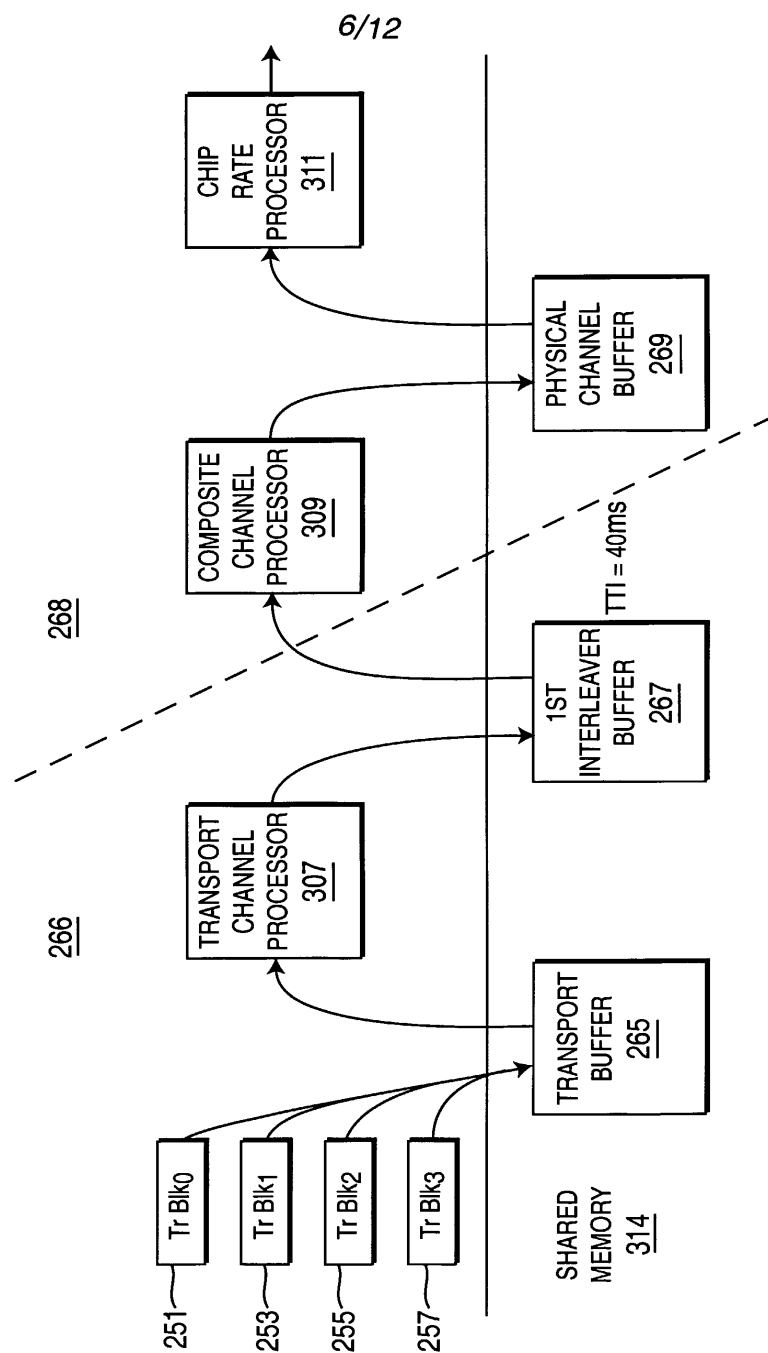


FIG. 6

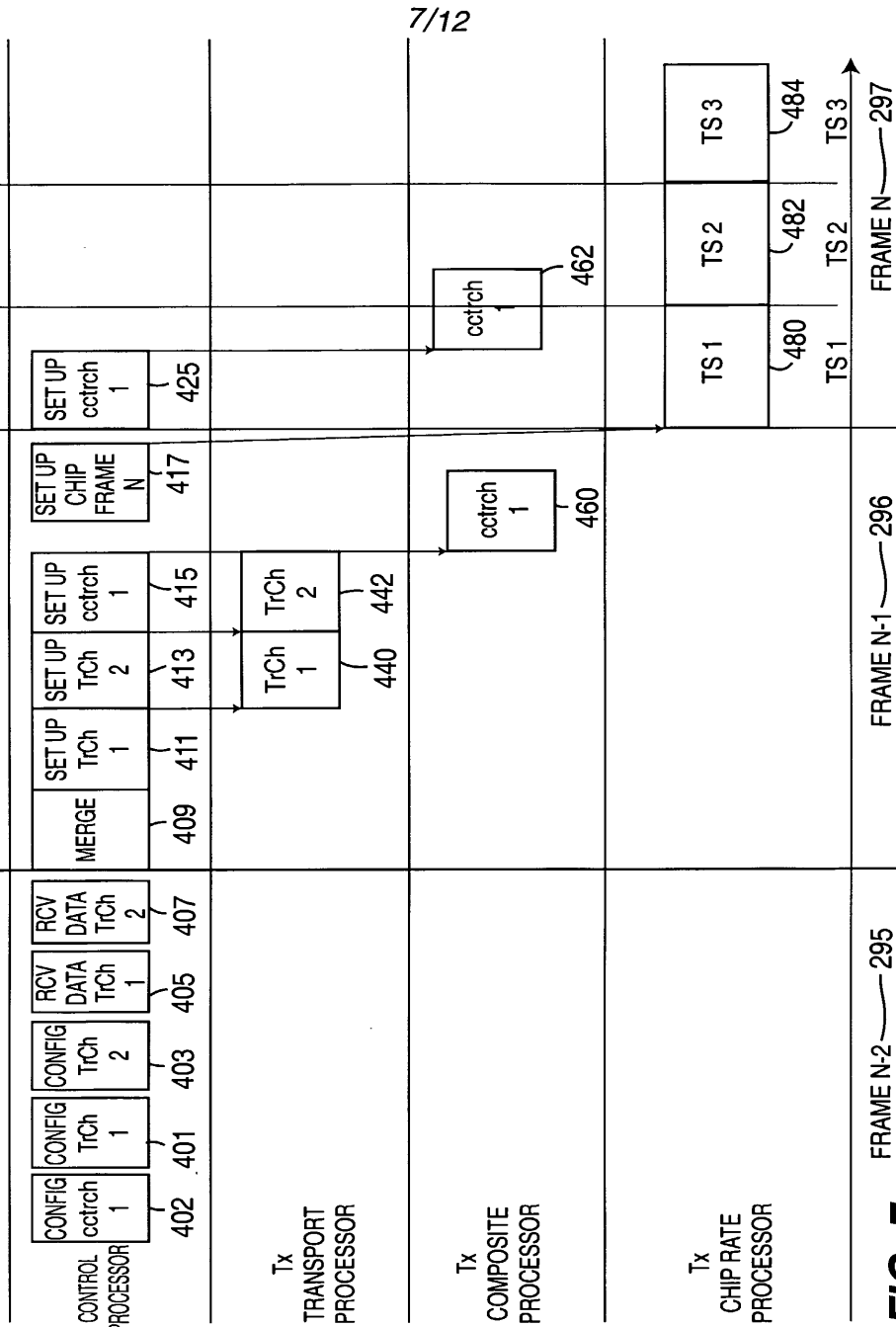
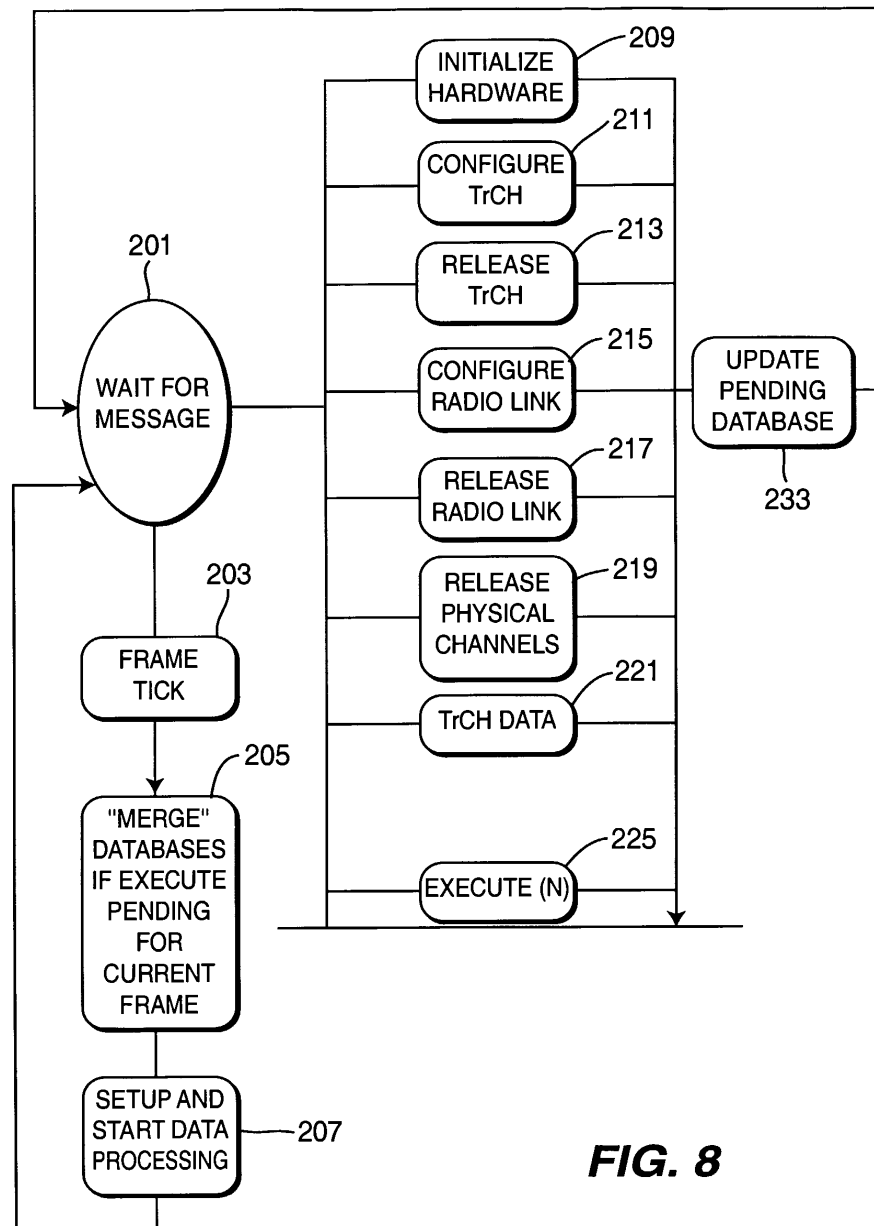
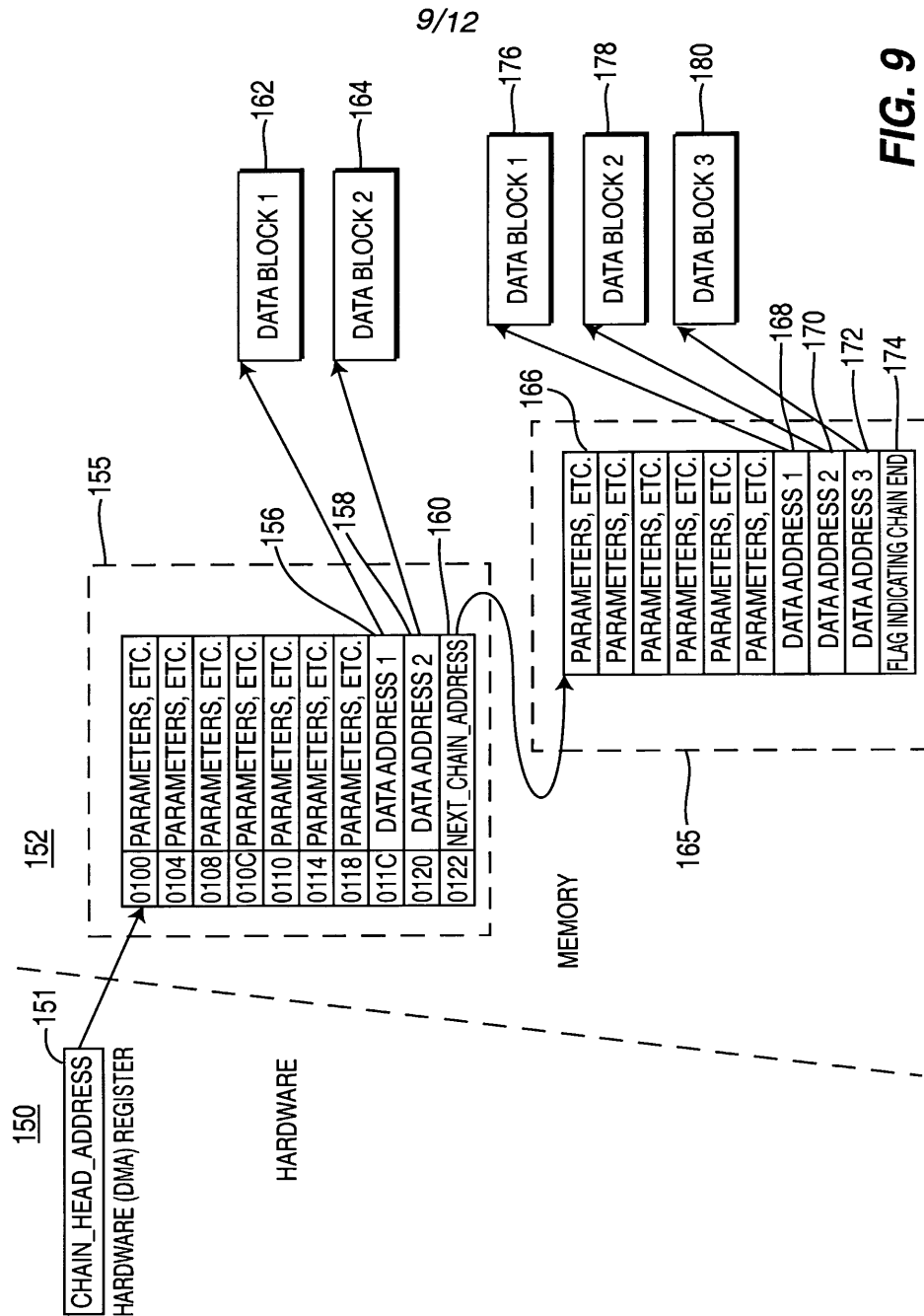


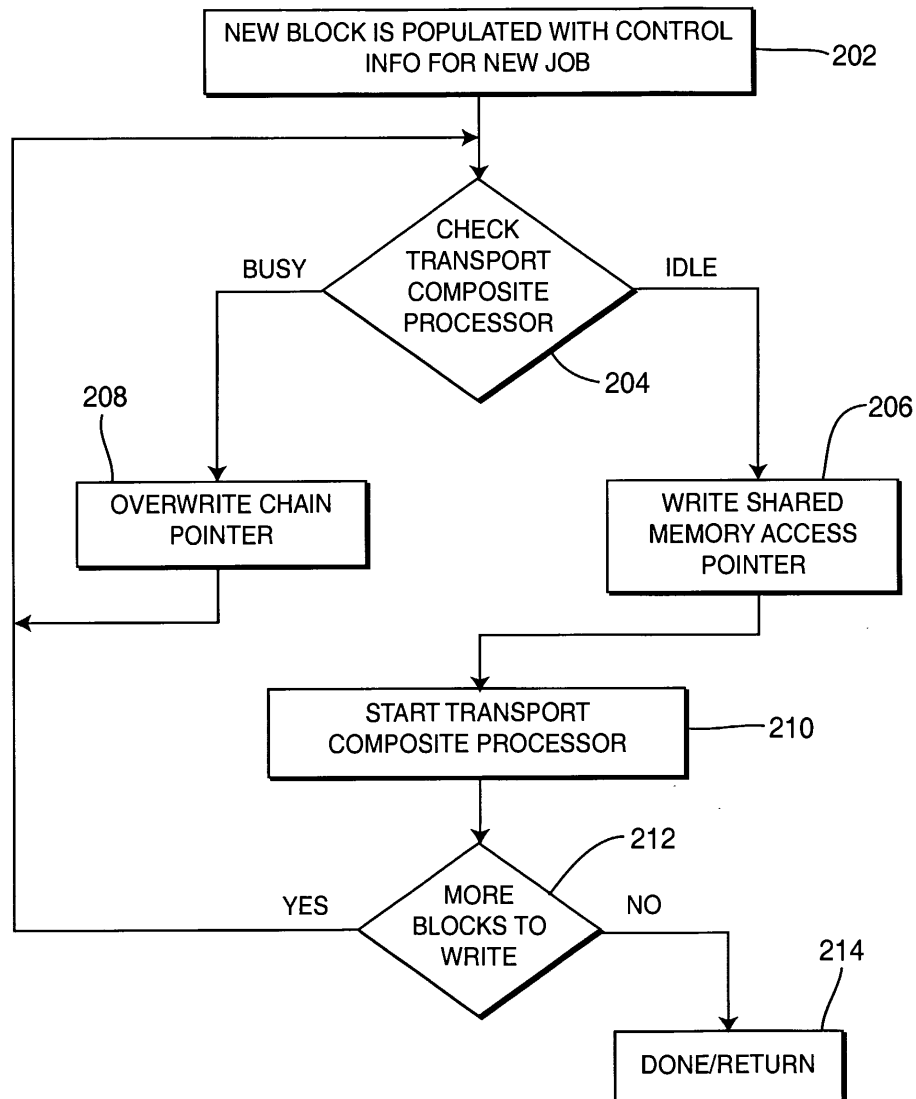
FIG. 7

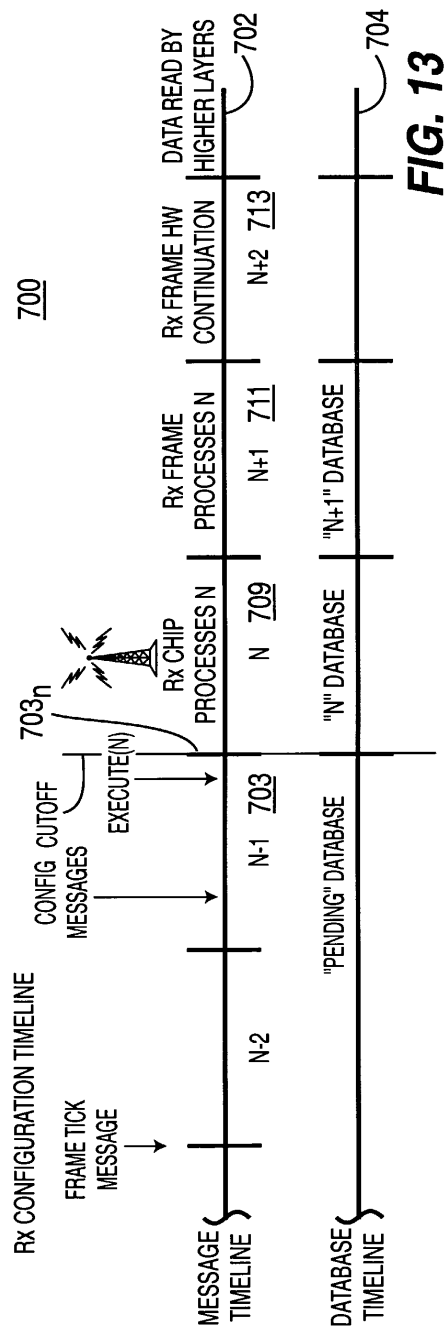
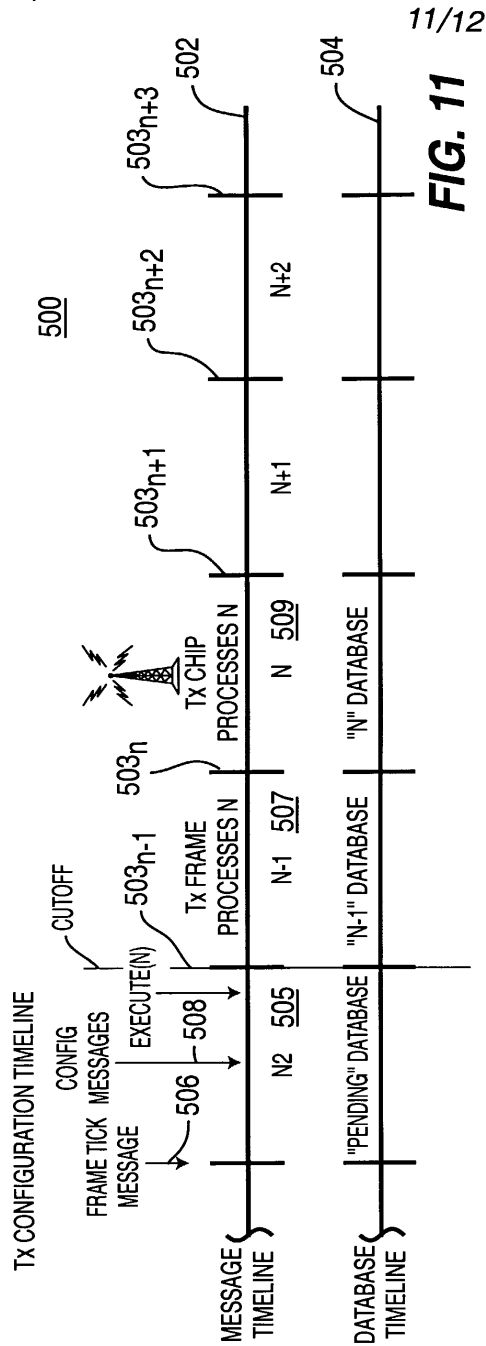
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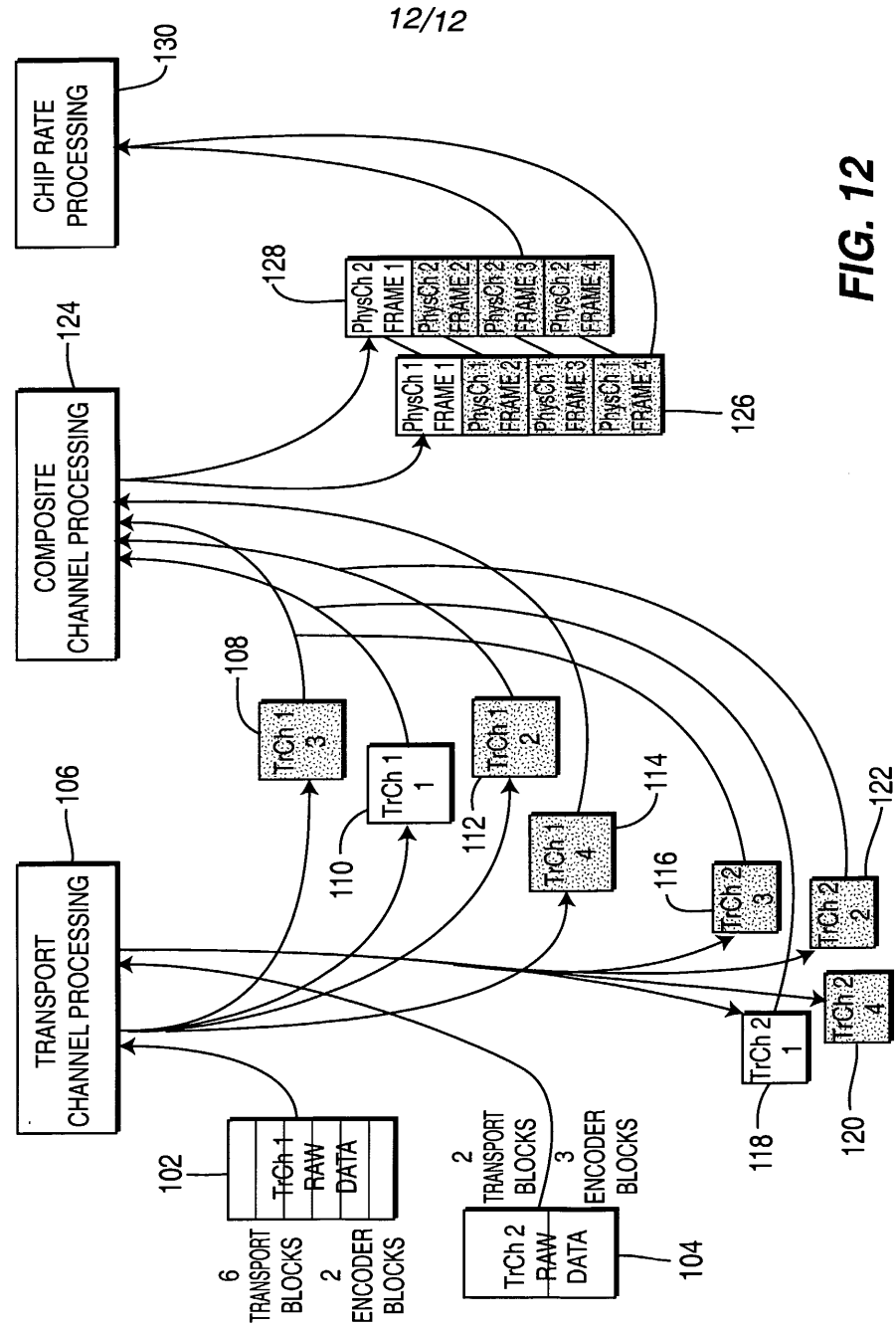
**FIG. 8**

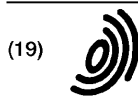


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**FIG. 10**



**FIG. 12**



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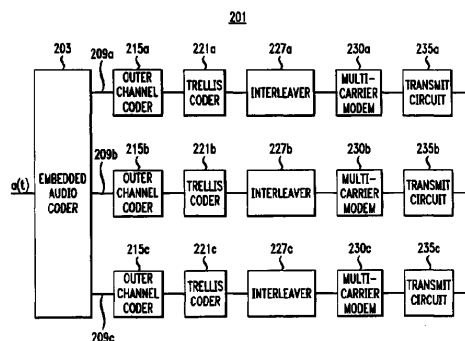
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(54) Multistream-in-band-on-channel transmission system

(57) Methods and apparatus for processing information, e.g., audio, speech, video or image information, for transmission in a communication system. In an illustrative embodiment, a set of bit streams are generated from an audio information signal. The set of bit streams may be, e.g., a total of four bit streams generated by separating each of two multiple description bit streams, corresponding to separate representations of the audio information signal, into first and second class bit streams. The first and second class bit streams associated with the first multiple description bit stream may then be transmitted in respective first and second subbands of a first sideband of an FM host carrier, while the first and second class bit streams associated with the second multiple description bit stream are transmitted in respective first and second subbands of a second sideband of the FM host carrier. The first class bit streams may be provided with a different level of error protection than the second class bit streams, e.g., by utilizing different portions of a non-uniform power profile for the corresponding subbands, or by placement of the bit streams in subbands having different susceptibility to interference. Delay may be introduced between at least a subset of the bit streams in order to provide improved performance, e.g., in the presence of fading.

FIG. 2



Description

Related Application

[0001] The present application is a continuation-in-part of U.S. Patent Application Serial No. 09/280,280, filed March 29, 1999 in the name of inventors Hui-Ling Lou, Deepen Sinha and Carl-Erik W. Sundberg and entitled "Technique for Effectively Communicating Multiple Digital Representations of a Signal," which is assigned to the assignee of the present application and incorporated by reference herein.

Field of the Invention

[0002] The present invention relates generally to digital audio broadcasting (DAB) and other techniques for transmitting information, and more particularly to techniques for implementing hybrid in-band on-channel (IBOC) systems for DAB and other applications.

Background of the Invention

[0003] The explosive growth of digital communications technology has resulted in an ever-increasing demand for bandwidth for communicating digital audio information, video information and/or data. For example, to efficiently utilize bandwidth to communicate digital audio information, a perceptual audio coding (PAC) technique has been developed. For details on the PAC technique, one may refer to U.S. Patent No. 5,285,498 issued February 8, 1994 to Johnston; and U.S. Patent No. 5,040,217 issued August 13, 1991 to Brandenburg et al., both of which are incorporated by reference herein. In accordance with such a PAC technique, each of a succession of time domain blocks of an audio signal representing audio information is coded in the frequency domain. Specifically, the frequency domain representation of each block is divided into coder bands, each of which is individually coded, based on psychoacoustic criteria, in such a way that the audio information is significantly compressed, thereby requiring a smaller number of bits to represent the audio information than would be the case if the audio information were represented in a more simplistic digital format, such as the PCM format.

[0004] Recently, the industry turned its focus to the idea of utilizing preexisting analog amplitude-modulation (AM) frequency band more efficiently to accommodate digital communications as well. However, it is required that any adjustment to the AM band to provide the additional capacity for digital communications does not significantly affect the analog AM signals currently generated by radio stations on the same band for AM radio broadcast. In the United States, adjacent geographic areas covered by AM radio broadcast are assigned different AM carrier frequencies, which are at least 20 kHz apart. Specifically, when they are exactly

20 kHz apart, the AM carrier assigned to the adjacent area is referred to as a "second adjacent carrier." Similarly, when they are 10 kHz apart, the AM carrier assigned to the adjacent area is referred to as a "first adjacent carrier."

[0005] An in-band on channel AM (IBOC-AM) (also known as "hybrid IBOC-AM") scheme utilizing bandwidth of the AM band to communicate digital audio information has been proposed. In accordance with the proposed scheme, digitally modulated signals representing the audio information populate, e.g., a 30 kHz digital band centered at an analog host AM carrier. The power levels of the spectrums of the digitally modulated signals are allowed to be equally high across a 10 kHz subband in the digital band on each end thereof.

[0006] However, in implementation, it is likely that two such IBOC-AM schemes would be respectively employed in two adjacent areas, to which the host AM carriers assigned are 20 kHz apart. In that case, the 30 kHz digital bands for digital communications centered at the respective host AM carriers overlap each other by 10 kHz, thereby causing undesirable "adjacent channel interference" to each area. In particular, such interference is referred to as "second adjacent channel interference," as the dominant interfering carrier in this instance consists of a second adjacent carrier. For example, the second adjacent channel interference degrades the digital communications in each of the adjacent areas, especially in the parts of the areas which are close to their common border. Similar concerns arise in other types of IBOC systems, e.g., frequency-modulation (FM) IBOC systems, also known as IBOC-FM systems or hybrid IBOC-FM systems, satellite broadcasting systems, Internet radio systems, TV broadcasting systems, etc.

[0007] Accordingly, there exists a need for a technique, e.g., based on the PAC technique, for effectively utilizing an existing transmission band, e.g., an AM, FM or other band, for digital communications and treating adjacent channel interference in adjacent areas where IBOC schemes are employed.

Summary of the Invention

[0008] The present invention provides methods and apparatus for multistream transmission and/or reception of information in IBOC digital audio broadcasting and other applications. In accordance with the invention, multiple bit streams are generated from an information signal, and the bit streams are transmitted using frequency bands associated with a host carrier signal, e.g., an AM or FM host carrier signal. The manner in which the multiple bit streams are generated and transmitted may be based on factors such as, e.g., multidescriptive coding, a core/enhancement type of embedded coding, a lower basic coding rate in one frequency band relative to another frequency band, bit error sensitivity classification for unequal error protection (UEP), a non-uniform

power profile on the bands, an increased total frequency band power, and an increase in frequency band and bit stream time diversity by introducing delay between bit streams in different bands and/or within the same band. The individual bit streams may be encoded using an outer code, e.g., a CRC code, RS code, BCH code, or other linear block code, and an inner code, e.g., a convolutional code, turbo code, or trellis coded modulation.

[0009] In an illustrative embodiment, a set of bit streams are generated from an audio information signal. The set of bit streams may be, e.g., a total of four bit streams generated by separating each of two multiple description bit streams, corresponding to separate representations of the audio information signal, into first and second class bit streams. The first and second class bit streams associated with the first multiple description bit stream may then be transmitted in respective first and second subbands of a first sideband of an FM host carrier, while the first and second class bit streams associated with the second multiple description bit stream are transmitted in respective first and second subbands of a second sideband of the FM host carrier. The first class bit streams may be provided with a different level of error protection than the second class bit streams, e.g., by utilizing different portions of a non-uniform power profile for the corresponding subbands, or by placement of the bit streams in subbands having different susceptibility to interference. Delay may be introduced between at least a subset of the four bit streams in order to provide improved performance. e.g., in the presence of fading.

[0010] The invention provides a number of other significant advantages over conventional systems, including, for example, improved coverage area and reduced memory requirements. The invention may be implemented in numerous applications, such as simultaneous multiple program listening and/or recording, simultaneous delivery of audio and data, etc. In addition, one or more of the techniques of the invention can be applied to other types of digital information, including, for example, speech, data, video and image information. Moreover, the invention is applicable not only to perceptual coders but also to other types of source encoders using other compression techniques operating over a wide range of bit rates, and can be used with transmission channels other than radio broadcasting channels.

Brief Description of the Drawings

[0011]

FIG. 1 illustrates a power profile of digitally modulated signals representing multiple bit streams transmitted over corresponding subbands of a frequency band in accordance with the invention.

FIG. 2 is a block diagram of a transmitter for transmitting multiple bit streams containing audio information through subbands of a frequency band in accordance with the invention.

FIG. 3 is a block diagram of a receiver for recovering the audio information transmitted using the transmitter of FIG. 2.

FIG. 4 is a table illustrating the configuration of a number of different multistream FM hybrid in-band on-channel (IBOC-FM) systems in accordance with the invention.

FIG. 5 shows a set of power profiles which may be used in a multistream IBOC-FM system in accordance with the invention.

FIGS. 6 and 7 illustrate the operation of multistream IBOC-FM systems 7 and 9, respectively, of FIG. 4.

FIG. 8 is a table showing blend modes in a four-stream IBOC-FM system in accordance with the invention.

FIG. 9 shows examples of rate-1/2 codes that may be utilized in the multistream IBOC-FM systems of the invention.

FIGS. 10 through 13 are tables illustrating performance gains in an exemplary multistream IBOC-FM system in accordance with the invention.

Detailed Description of the Invention

[0012] The invention will be described below in conjunction with exemplary multistream techniques for use in the transmission and reception of audio information bits, e.g., audio bits generated by an audio coder such as the perceptual audio coder (PAC) described in D. Sinha, J.D. Johnston, S. Dorward and S.R. Quackenbush, "The Perceptual Audio Coder," in Digital Audio, Section 42, pp. 42-1 to 42-18, CRC Press, 1998. It should be understood, however, that the multistream techniques of the invention may be applied to many other types of information, e.g., video or image information, and other types of coding devices. In addition, the invention may be utilized in a wide variety of different types of communication applications, including communications over the Internet and other computer networks, and over cellular multimedia, satellite, wireless cable, wireless local loop, high-speed wireless access and other types of communication systems. The invention may be utilized with any desired type of communication channel or channels, such as, for example, frequency channels, time slots, code division multiple access (CDMA) slots, and virtual connections in asynchronous transfer mode (ATM) or other packet-based

transmission systems.

[0013] The invention is directed to techniques for digital communications over multiple frequency bands including, e.g., parts of an amplitude-modulation (AM) or frequency-modulation (FM) frequency band which is currently used by radio stations for respective AM or FM radio broadcast. A system in accordance with the invention may be used to effectively communicate digitally modulated signals representing, e.g., audio information, over an AM or FM frequency band in a geographic area which is assigned an analog host AM or FM carrier whose frequency is f_c , despite any adjacent channel interference affecting the digitally modulated signals.

[0014] To effectively communicate the audio information and treat any adjacent channel interference, in particular, second adjacent channel interference, in accordance with the invention, multistream coding is implemented in an IBOC system to generate multiple bit streams representing an audio signal containing the audio information, and the bit streams are respectively transmitted through individual subbands within a digital sideband. The audio signal may be recovered using all of the bit streams received or a subset thereof if some of the subbands are severely affected by the adjacent channel interference and/or other adverse channel conditions. The audio quality, e.g., based on a signal-to-noise ratio (SNR) or preferably perceptually based measure, of the recovered signal varies with the underlying, received bit streams used. In general, the more received bit streams are used, the higher the audio quality of the recovered signal. Advantageously, with respect to prior art systems, the inventive system affords increased robustness against adverse channel conditions, and more graceful degradation of digital communications when such conditions occur.

[0015] For example, in an illustrative embodiment suitable for use in an IBOC-AM system, three bit streams are used to communicate an audio signal containing audio information. In accordance with the invention, one of the bit streams represents core audio information and is referred to as a "C-stream." The other two bit streams represent first and second enhancement audio information, and are referred to as "E₁-stream" and "E₂-stream," respectively. Because of the design of the multistream coding described below, the audio signal recovered based on the C-stream alone, although viable, has the minimum acceptable quality; the audio signal recovered based on the C-stream in combination with either E₁-stream or E₂-stream has relatively high quality; the audio signal recovered based on the C-stream in combination with both E₁-stream and E₂-stream has the highest quality. However, any audio signal recovered based only on the E₁-stream and/or E₂-stream is not viable.

[0016] Thus, in accordance with an aspect of the invention, the C-stream representing the minimal core audio information is transmitted through subband 103 in FIG. 1 between $f_c - 5$ kHz and $f_c + 5$ kHz which is

immune to second adjacent channel interference; the E₁-stream representing first enhancement audio information is transmitted through subband 105 between $f_c - 15$ kHz and $f_c - 5$ kHz which is subject to second adjacent channel interference; and the E₂-stream representing second enhancement audio information is transmitted through subband 107 between $f_c + 5$ kHz and $f_c + 15$ kHz which is also subject to second adjacent channel interference. As such, the minimal core audio information would be recoverable despite any second adjacent channel interference, and enhanced by any of E₁-stream and E₂-stream depending on whether the respective subbands 105 and 107 are severely affected by the second adjacent channel interference.

[0017] FIG. 2 illustrates transmitter 201 in an IBOC-AM communications system embodying the principles of the invention. An analog audio signal $a(t)$ containing audio information to be transmitted by transmitter 201 is fed to embedded audio coder 203 which is fully described below. It suffices to know for now that coder 203 based on the multistream coding generates the aforementioned C-stream, E₁-stream and E₂-stream representing the analog signal on leads 209a, 209b and 209c, respectively. The bit rates for the C-stream, E₁-stream and E₂-stream, thus generated, are M kb/sec, S1 kb/sec and S2 kb/sec, respectively. For example, if coder 203 is a 48 kb/sec audio coder, M, S1 and S2 in that case may be set to be 16, 16 and 16, respectively. These bit rates are selected such that if all of the streams are successfully received, the quality of the resulting recovered signal is close to that of a single stream generated by a conventional non-embedded audio coder at M + S1 + S2 kb/sec. Similarly, the quality of the resulting signal recovered based on a combination of the C-stream with the E₁-stream or E₂-stream is close to that of a single stream generated by the conventional non-embedded audio coder at M + S1 kb/sec or M + S2 kb/sec. In addition, the resulting quality corresponding to the combination of the C-stream with the E₁-stream or E₂-stream is significantly higher than the analog AM quality.

[0018] The C-stream on lead 209a, E₁-stream on lead 209b and E₂-stream on lead 209c are fed to outer channel coder 215a, outer channel coder 215b and outer channel coder 215c, respectively. Outer channel coder 215a encodes the C-stream according to a well known forward error correction coding technique, e.g., the Reed-Solomon (RS) coding technique in this instance, or alternatively a cyclic redundancy check (CRC) binary block coding technique, to afford correction and/or detection of errors in the C-stream after its transmission. The C-stream is processed by coder 215a on a block by block basis, with each block having a predetermined number of bits. In a conventional manner, coder 215a appends the RS check symbols resulting from the encoding to each corresponding block. Similarly, coders 215b and 215c respectively processes the E₁-stream and E₂-stream on a block by block basis, and

append RS check symbols to each corresponding block of the streams for error correction and/or detection purposes.

[0019] The RS coded C-stream, RS coded E_1 -stream and RS coded E_2 -stream are fed to trellis coders 221a, 221b and 221c, respectively. Trellis coder 221a processes the received RS coded C-stream on a symbol (different from a RS check symbol) interval by symbol interval basis, where the symbol interval has a predetermined duration T_1 .

[0020] In a well known manner, coder 221a encodes the received bit stream in accordance with a trellis code to provide the communications system with a so-called "coding gain" which manifests itself in the form of enhance immunity to such random channel impairments as additive noise, without sacrificing the source bit rate or additional broadcast bandwidth. Specifically, coder 221a introduces redundancy into the received bit stream in accordance with the trellis code to allow use of a maximum likelihood decoding technique at receiver 301 in FIG. 3 to be described. This redundancy takes the form of one or more additional bits. During each symbol interval, coder 221a forms an encoded word, which includes redundancy bits and bits from the received RS coded C-stream and is used to select a symbol from a signal constellation of conventional design. The selected symbols from coder 221a are interleaved by interleaver 227a to pseudo-randomize the symbols. During each time frame which is $K_1 T_1$ long, multicarrier modem 230a processes K_1 symbols from interleaver 227a in accordance with the well known orthogonal frequency division multiplexed (OFDM) scheme, where K_1 is a predetermined number. In a well known manner, modem 230a generates K_1 pulse shaping carriers or digitally modulated signals corresponding to the K_1 symbols. The resulting pulse shaping carriers are transmitted by transmit circuit 235a through a sub-band 303 with power profile 309. Transmit circuit 235a may include, e.g., a radio-frequency (RF) up-converter, a power amplifier and an antenna, all of conventional design.

[0021] Similarly, during each symbol interval T_2 , trellis coder 221b forms an encoded word, which includes redundancy bits and bits from the received RS coded E_1 -stream and is used to select a symbol from a second predetermined signal constellation, where T_2 represents a predetermined duration. The resulting sequence of selected symbols are interleaved by interleaver 227b to pseudo-randomize the symbols. During each time frame which is $K_2 T_2$ long, multicarrier modem 230b processes K_2 symbols from interleaver 227b in accordance with the well known OFDM scheme, where K_2 is a predetermined number. In a well known manner, modem 230b generates K_2 pulse shaping carriers or digitally modulated signals corresponding to the K_2 symbols. The resulting pulse shaping carriers are transmitted by transmit circuit 235b through subband 105 with power profile 111.

[0022] In addition, during each symbol interval T_3 , trellis coder 221c similarly forms an encoded word, which includes redundancy bits and bits from the received RS coded E_2 -stream and is used to select a symbol from a third predetermined signal constellation, where T_3 represents a predetermined duration. The resulting sequence of selected symbols are interleaved by interleaver 227c to pseudo-randomize the symbols. During each time frame which is $K_3 T_3$ long, multicarrier modem 230c transmits K_3 symbols from interleaver 227b in accordance with the well known OFDM scheme, where K_3 is a predetermined number. In a well known manner, modem 230b generates K_3 pulse shaping carriers or digitally modulated signals corresponding to the K_3 symbols. The resulting pulse shaping carriers are transmitted by transmit circuit 235c through sub-band 107 with power profile 113. If the E_1 -stream and E_2 -stream are equivalent and $S_1 = S_2$, which is the case in this instance, $T_2 = T_3$ and $K_2 = K_3$.

[0023] Referring to FIG. 3, receiver 301 receives signals transmitted by transmitter 201 through sub-bands 103, 105 and 107, respectively. The received signals corresponding to the C-stream, E_1 -stream and E_2 -stream are processed by receive circuits 307a, 307b and 307c, which perform inverse functions to above-described transmit circuits 235a, 235b and 235c, respectively. The output of circuit 307a comprises the K_1 pulse shaping carriers as transmitted, which are fed to demodulator 309a. Accordingly, demodulator 309a generates a sequence of symbols containing the core audio information. The generated symbols are de-interleaved by de-interleaver 313a which performs the inverse function to interleaver 227a described above. Based on the de-interleaved symbols and the signal constellation used in trellis coder 221a, trellis decoder 317a in a conventional manner determines what the most likely transmitted symbols are in accordance with the well known Viterbi algorithm, thereby recovering the C-stream incorporating RS check symbols therein, i.e., the RS coded C-stream. Outer channel decoder 319a extracts the RS check symbols from blocks of the RS coded C-stream bits, and examines the RS check symbols in connection with the corresponding blocks of C-stream bits. Each block of C-stream bits may contain errors because of the channel imperfection, e.g., interference with the transmitted signals in subband 103. If the number of errors in each block is smaller than a threshold whose value depends on the actual RS coding technique used, decoder 319a corrects the errors in the block. However, if the number of errors in each block is larger than the threshold and the errors are detected by decoder 319a, the latter issues, to blending processor 327 described below, a first flag indicating the error detection. Decoder 319a then provides the recovered C-stream to embedded audio decoder 330.

[0024] Similarly, the output of circuit 307b comprises the K_2 pulse shaping carriers corresponding to the E_1 -stream, which are fed to demodulator 309b. Accord-

ingly, demodulator 309b generates a sequence of symbols containing the first enhancement audio information. The generated symbols are de-interleaved by de-interleaver 313b which performs the inverse function to interleaver 227b described above. Based on the deinterleaved symbols and the signal constellation used in trellis coder 221b, trellis decoder 317b in a conventional manner determines what the most likely transmitted symbols are in accordance with the Viterbi algorithm, thereby recovering the E_1 -stream incorporating RS check symbols therein, i.e., the RS coded E_1 -stream. Outer channel decoder 319b extracts the RS check symbols from blocks of the RS coded E_1 -stream bits, and examines the RS check symbols in connection with the corresponding blocks of E_1 -stream bits. Each block of E_1 -stream bits may contain errors because of the channel imperfection, e.g., second adjacent channel interference with the transmitted signals in subband 105. If the number of errors in each block is smaller than the aforementioned threshold, decoder 319b corrects the errors in the block. However, if the number of errors in each block is larger than the threshold and the errors are detected by decoder 319b, the latter issues, to blending processor 327, a second flag indicating the error detection. Decoder 319b then provides the recovered E_1 -stream to embedded audio decoder 330.

[0025] In addition, the output of circuit 307c comprises the K_3 pulse shaping carriers corresponding the E_2 -stream, which are fed to demodulator 309c. Accordingly, demodulator 309c generates a sequence of symbols containing the second enhancement audio information. The generated symbols are de-interleaved by de-interleaver 313c which performs the inverse function to interleaver 227c described above. Based on the deinterleaved symbols and the signal constellation used in trellis coder 221c, trellis decoder 317c in a conventional manner determines what the most likely transmitted symbols are in accordance with the Viterbi algorithm, thereby recovering the E_2 -stream incorporating RS check symbols therein, i.e., the RS coded E_2 -stream. Outer channel decoder 319c extracts the RS check symbols from blocks of the RS coded E_2 -stream bits, and examines the RS check symbols in connection with the corresponding blocks of E_2 -stream bits. Each block of E_2 -stream bits may contain errors because of the channel imperfection, e.g., second adjacent channel interference with the transmitted signals in subband 107. If the number of errors in each block is smaller than the aforementioned threshold, decoder 319c corrects the errors in the block. However, if the number of errors in each block is larger than the threshold and the errors are detected by decoder 319c, the latter issues, to blending processor 327, a third flag indicating the error detection. Decoder 319c then provides the recovered E_2 -stream to embedded audio decoder 330.

[0026] Embedded audio decoder 330 performs the inverse function to embedded audio coder 203 described above and is capable of blending the

received C-stream, E_1 -stream and E_2 -stream to recover an audio signal corresponding to a(t). However, blending processor 327 determines any of the E_1 -stream and E_2 -stream to be blended with the C-stream in decoder 330. Such a determination is based on measures of data integrity of the E_1 -stream and E_2 -stream. Blending processor 327 may also determine the viability of the C-stream based on a measure of its data integrity, and control any audio signal output based on the C-stream from receiver 303. To that end, processor 327 provides first, second and third control signals indicative of the determinations of use of the C-stream, E_1 -stream and E_2 -stream, respectively, in decoder 330 to recover the audio signal. In response to such control signals, decoder 330 accordingly (a) operates at the full rate and utilizes all three streams to recover the audio signal, (b) blends to a lower bit rate and utilizes the C-stream in combination with the E_1 -stream or E_2 -stream to recover the audio signal, (c) operates at the lowest bit rate and utilizes only the C-stream to recover the audio signal, or (d) recovers no audio signal based on the C-stream. To avoid event (d), although rare, remedial methodologies may be implemented, including transmitting the audio signal through the AM band as a conventional analog AM signal, and recovering the audio signal based on the analog AM signal in the receiver when event (d) occurs.

[0027] The measures based on which processor 327 determines whether any of the C-stream, E_1 -stream and E_2 -stream is used in recovering the audio signal include, e.g., the frequencies of the first, second and third flags received by processor 327, which are indicative of bit errors in the received C-stream, E_1 -stream and E_2 -stream, respectively. The actual frequency threshold beyond which the corresponding stream is rejected or "muted" depends on bit rate of the stream, output quality requirements, etc.

[0028] The aforementioned measures may also include an estimate of a signal-to-interference ratio concerning each subband obtained during periodic training of each of modems 230a, 230b and 230c. Since these modems implement multilevel signaling and operate in varying channel conditions, a training sequence with known symbols is used for equalization and level adjustments in demodulators 309a, 309b and 309c periodically. Such a training sequence can be used to estimate the signal-to-interference ratio. When such an estimate goes below an acceptable threshold, blending processor 327 receives an exceptional signal from the corresponding demodulator. In response to the exceptional signal, and depending on other measures, processor 327 may issue a control signal concerning the stream associated with the demodulator to cause decoder 330 to mute the stream. As the exceptional signal needs to be time aligned with the portion of the stream affected by the substandard signal-to-interference ratio, delay element 335 is employed to compensate for the delay imparted to such a stream portion in traversing the deinterleaver and intervening decoders.

[0029] The foregoing hybrid IBOC-AM embodiment merely illustrates the principles of the invention. It will thus be appreciated that those skilled in the art will be able to devise numerous other arrangements which embody the principles of the invention and are thus within its spirit and scope.

[0030] For example, in the disclosed embodiment, three streams, i.e., the C-stream, E_1 -stream and E_2 -stream are used to represent the audio information to be transmitted. However, it will be appreciated that the number of such streams used may be higher or lower than three.

[0031] In addition, as mentioned before, an audio signal with digital quality can only be regenerated when the C-stream is viable. However, it will be appreciated that the audio signal may also be transmitted through the AM band as a host analog AM signal according to a mixed blending approach. In that approach, if the C-stream is lost and at least one E_i -stream is recovered in the receiver, the E_i -stream may be used to enhance the analog audio signal output, where i generically represents an integer greater than or equal to one. For example, the E_i -stream can be used to add high frequency content and/or stereo components to the analog signal. If all of the E_i - and C-streams are lost, the receiver would afford only the analog audio signal output.

[0032] In addition, in the disclosed embodiment, complementary quantizers are used to generate equivalent enhancement bit streams, e.g., E_1 -stream and E_2 -stream, for communications. However, based on the disclosure heretofore, it is apparent that a person skilled in the art may use similar complementary quantizers to generate equivalent C-streams, e.g., C_1 -stream and C_2 -stream, for communications. In an alternative embodiment, for instance, $a(t)$ may be coded in accordance with the invention to yield an enhancement bit stream, and C_1 - and C_2 -streams at 8 kb/sec, 20 kb/sec and 20 kb/sec, respectively.

[0033] Further, in the disclosed embodiment, for example, subband 103 is used to transmit the C-stream. It will be appreciated that one may further subdivide, e.g., subband 103 equally for transmission of duplicate versions of the C-stream, or equivalent C-streams, to afford additional robustness to the core audio information.

[0034] In addition, the multistream coding schemes described above are applicable to various sizes of digital bands surrounding an analog host AM carrier at f_c , e.g., $f_c \pm 5$ kHz, $f_c \pm 10$ kHz, $f_c \pm 15$ kHz, $f_c \pm 20$ kHz, etc.

[0035] Further, the multistream coding schemes described above are applicable to communications of not only audio information, but also information concerning text, graphics, video, etc.

[0036] Still further, the multistream coding schemes, and the mixed blending technique described above are applicable not only to the hybrid IBOC-AM systems, but also other systems, e.g., hybrid IBOC-FM systems, satellite broadcasting systems, Internet radio

systems, TV broadcasting systems, etc.

[0037] Moreover, the multistream coding schemes can be used with any other well known channel coding different than the RS coding described above such as the Bose-Chandhuri-Hocquenghem (BCH) coding, etc., with or without unequal error protection (UEP) sensitivity classifications.

[0038] In addition, in the disclosed embodiment, multicarrier modems 230a, 230b and 230c illustratively implement an OFDM scheme. It will be appreciated that a person skilled in the art may utilize in such a modem any other scheme such as a frequency division multiplexed tone scheme, time division multiplexed (TDM) scheme, or code division multiplexed (CDM), instead.

[0039] Further, the frequency subbands for transmission of individual bit streams in the multistream coding approach need not be contiguous. In addition, the channel coding and interleaving techniques applied to different subbands may not be identical.

[0040] Still further, each frequency subband may be used for transmission of multiple bit streams in the multistream coding approach by time-sharing the frequency subband in accordance with a well known time division multiple access (TDMA) scheme, or by code-sharing the frequency subband in accordance with a well known code division multiple access (CDMA) scheme, or by sharing the frequency subband in another manner in accordance with a similar implicit partitioning of the subband.

[0041] Yet still further, the power profiles of the digitally modulated signals in the multistream coding approach may not be uniform across the transmission band.

[0042] Finally, transmitter 201 and receiver 301 are disclosed herein in a form in which various transmitter and receiver functions are performed by discrete functional blocks. However, any one or more of these functions could equally well be embodied in an arrangement in which the functions of any one or more of those blocks or indeed, all of the functions thereof, are realized, for example, by one or more appropriately programmed processors.

[0043] As noted previously, the multistream transmission and reception techniques described in conjunction with FIGS. 1 through 3 above are applicable to IBOC-FM systems as well as other types of digital broadcasting systems. FIG. 4 lists a number of examples of multistream IBOC-FM systems in accordance with the invention. For each of the systems, the table in FIG. 4 specifies the audio coder rate on each of two sidebands, the one sideband channel code rate, the two sideband channel code rate, a power profile, a source coder type (if applicable), a channel code type, and a number of streams (MS). As will be described in greater detail below, the illustrative embodiments of the present invention provide improved performance through the use of multistream coding and bit placement, transmission with introduction of time diversity, and non-uniform

power profiles for different frequency bands or within a given frequency band. These features of the invention can provide significant advantages, including, for example, improved coverage area and reduced memory requirements relative to conventional systems.

[0044] Each of the systems listed in FIG. 4 utilizes both a channel code, also referred to as an inner code, and an outer code. Inner codes that may be used in the systems of FIG. 4 or other systems of the invention include block or convolutional codes, so-called "turbo" codes, and coding associated with trellis coded modulation. Examples of outer codes that may be used include CRCs, RS codes, BACH. codes, and other types of linear block codes.

[0045] System 1 in FIG. 4 is a baseline system which uses 96 kb/sec audio coding in a single stream transmission configuration over two sidebands with OFDM modulation. The two frequency sidebands for digital audio are transmitted on each side of a host analog FM signal. A uniform power profile, i.e., profile *a* in FIG. 5, is used. The channel coding is rate 4/5, memory 6 on each sideband with a total of rate 2/5, memory 6 in a complementary punctured pair convolutional (CPPC) channel coding configuration with both sidebands. Optimum bit placement (OBP) is used in conjunction with the channel code. CPPC codes and OBP techniques suitable for use in the IBOC-FM systems of the invention are described in, e.g., U.S. Patent Application Serial No. 09/217,655, filed December 21, 1998 in the name of inventors Brian Chen and Carl-Erik W. Sundberg and entitled "Optimal Complementary Punctured Convolutional Codes," which is assigned to the assignee of the present application and incorporated by reference herein.

[0046] A significant difficulty with system 1 is projected limited coverage for the digital transmission, particularly when only one sideband is available to the receiver, e.g., due to severe interference. This difficulty remains significant even if soft combining is used.

[0047] System 2 through 9 in FIG. 4 utilize one or more of the following techniques in order to provide improved signal-to-noise ratio, and thus better digital signal coverage, relative to the baseline system 1: multistream transmission, multidescriptive (MD) audio coding, a core/enhancement type of embedded audio coding such as that described above in conjunction with FIGS. 2 and 3, a lower basic audio coding rate in one sideband, bit error sensitivity classification for unequal error protection (UEP), modified power profile on the sidebands, and an increased total sideband power. For example, lowering the PAC audio coding rate per sideband to 64 kb/sec provides sufficient additional bandwidth to permit utilization of lower rate channel codes. In systems 2 through 9 of FIG. 4, using an audio coding rate of 64 kb/sec on at least one of the sidebands allows a considerably more powerful channel code, i.e., a rate 1/2 convolutional channel code, to be used in place of the rate 4/5 code of the baseline system 1.

[0048] Other techniques in accordance with the invention may also be used to further improve performance. For example, an increase in frequency band and bit stream time diversity may be provided in one or more of the systems of FIG. 4 by introducing delay between bit streams in different sidebands and/or within the same sideband. Such an arrangement may be used to provide improved performance in the presence of fading. Time diversity techniques suitable for use with the present invention are described in greater detail in U.S. Patent Application Serial No. 09/102,776, filed June 23, 1998 in the name of inventors Robert L. Cupo et al. and entitled "Broadcast Method Having Time and Frequency Diversity," which is assigned to the assignee of the present application and incorporated by reference herein.

[0049] Generation of multiple source coded streams may be achieved using multistream PAC encoding techniques such as bit-stream partitioning, multidescriptive coding, and embedded coding. A particular multistream transmission system may employ one or more of these techniques for producing a multistream representation of a source signal. In bit-stream partitioning, source bits are partitioned into two or more classes of differing sensitivity to bit errors, each of which may be provided with a different level of error protection in accordance with a UEP technique. The invention may be utilized with UEP techniques such as those described in U.S. Patent Application Serial No. 09/022,114, filed February 11, 1998 in the name of inventors Deepen Sinha and Carl-Erik W. Sundberg and entitled "Unequal Error Protection For Perceptual Audio Coders," and U.S. Patent Application Serial No. 09/163,656, filed September 30, 1998 in the name of inventors Deepen Sinha and Carl-Erik W. Sundberg and entitled "Unequal Error Protection for Digital Broadcasting Using Channel Classification," both of which are assigned to the assignee of the present application and incorporated by reference herein.

[0050] In multidescriptive coding, source bits are encoded into two or more equivalent streams such that any of these streams may be decoded independently as well as in combination with other substreams to provide different levels of recovered audio quality. In embedded coding, source bits are encoded with a core or essential bit stream and one or more enhancement bit streams. Exemplary multidescriptive and embedded coding techniques suitable for use with the present invention are described in U.S. Patent Application Serial No. 09/280,785, filed March 29, 1999 in the name of inventors Peter Kroon and Deepen Sinha and entitled "Multirate Embedded Coding of Speech and Audio Signals," which is assigned to the assignee of the present application and incorporated by reference herein.

[0051] The power profiles listed in FIG. 4 are illustrated in FIG. 5. The power profiles referred to herein as *a*⁺ and *a*⁺ correspond to power profiles *a* and *a*⁺, respectively, with a uniform power increase of 3 dB over

the entire sideband. FIG. 5 shows only a single sideband of each of the power profiles, and it should be understood that the other sideband may be configured in the same manner. Increased power levels within the profiles are referenced to a power level P , and expressed as a multiple of P , e.g., $2.5P$ is the increased level in profile b . The increased power levels are also expressed in dB relative to level P , i.e., level P corresponds to 0 dB. The power profiles shown in FIG. 5 are examples only, and numerous other types of profiles may be used. The particular profile selected will generally depend on certain application-specific factors, such as, e.g., the nature of interference effects such as self-interference and/or adjacent channel interference. Additional details regarding non-uniform power profiles suitable for use with the present invention may be found in U.S. Patent Application Serial No. 09/064,938, filed April 22, 1998 in the name of inventors Brian Chen and Carl-Erik W. Sundberg and entitled "Technique for Communicating Digitally Modulated Signals Over an Amplitude-Modulation Frequency Band," which is assigned to the assignee of the present application and incorporated by reference herein.

[0052] FIGS. 6 and 7 illustrate in greater detail the operation of systems 7 and 9 of FIG. 4. Systems 7 and 9 represent preferred embodiments of an IBOC-FM system in accordance with the invention. Both of these systems utilize an overall source coder rate of 128 kb/sec, a rate $1/2$ convolutional channel code, multidescriptive coding, two-level UEP and at least four bit streams. Referring to FIG. 6, an audio signal is first encoded using a multidescriptive coding technique to produce two streams S_1 and S_2 at 64 kb/sec each. The streams S_1 and S_2 are transmitted on a host FM signal 602 as sidebands 604 and 606, respectively. The transmission of multidescriptive streams S_1 and S_2 in different frequency bands provides both information diversity and frequency diversity in accordance with the invention. Although FIG. 4 indicates that system 7 may utilize power profile b , c , d or e of FIG. 5, the embodiment illustrated in FIG. 6 uses power profile b . This profile includes subbands A, B and C in each of the two sidebands 604 and 606, as shown.

[0053] The two streams S_1 and S_2 in FIG. 6 are divided into two classes, class I and class II, using a bit stream classifier. Class I bits represent the more important audio bits, and are provided with a higher level of error protection by associating them with the high-power subband B of the non-uniform power profile b . Class II bits, of lesser importance to reconstructed audio quality than the class I bits, are provided with a lower level by associating them with the lower-power subbands A and C of the power profile b . The subbands A, B and C of each sideband 604 and 606 are encoded for transmission using an inner rate $1/2$ convolutional code, and a CRC outer code. The system 7 transmission may utilize a four-stream implementation or a six-stream implementation.

[0054] It should be noted that the total gain for bits of class I with power profile b is on the order of 8 to 9.4 dB on a Gaussian channel. These gain numbers are expected to be higher for fading channels. In certain applications, a power profile of type c in FIG. 5 may be used in order to better maintain a proper balance between classes I and II.

[0055] FIG. 6 also shows a portion of a receiver for decoding the multiple streams of system 7. The receiver includes rate $1/2$ Viterbi decoders 612, 614, 616 and CRC decoders 632, 634 and 636 for use in decoding the respective inner and outer code for stream S_1 , and rate $1/2$ Viterbi decoders 622, 624, 626 and CRC decoders 642, 644 and 646 for use in decoding the respective inner code and outer code for stream S_2 . In the four-stream implementation, illustrated by solid lines in FIG. 6, subbands A and C of sideband 604 are decoded in Viterbi decoder 612 and CRC decoder 632, subband B of sideband 604 is decoded in Viterbi decoder 614 and CRC decoder 634, subbands A and C of sideband 606 are decoded in Viterbi decoder 622 and CRC decoder 642, and subband B of sideband 606 is decoded in Viterbi decoder 624 and CRC decoder 644. The decoders 616, 626, 636 and 646, shown in dashed outline in FIG. 6, are not used in this implementation, and may be eliminated from the receiver. It should be noted that, in the systems illustrated in FIGS. 6 and 7, the CRC block length may be optimized using conventional techniques. List Viterbi algorithms, which are well known in the art, may also be used in the decoding process.

[0056] The six-stream implementation of the receiver for system 7 decodes subband C of sideband 604 in Viterbi decoder 616 and CRC decoder 636, and subband A of sideband 606 in Viterbi decoder 626 and CRC decoder 646. As in the previous implementation, subband A of sideband 604 is decoded in Viterbi decoder 612 and CRC decoder 632, and subband C of sideband 606 is decoded in Viterbi decoder 622 and CRC decoder 642. In either of these example implementations, the outputs of the CRC decoders are applied to a PAC decoder 650, which generates reconstructed audio output signals for applications to speakers 652, 654.

[0057] Referring now to FIG. 7, an audio signal is first encoded using a multidescriptive coding technique to produce two streams S_1 and S_2 at 64 kb/sec each. The streams S_1 and S_2 are transmitted on a host FM signal 702 as sidebands 704 and 706, respectively. Although FIG. 4 indicates that system 7 may utilize power profile a or $a+$ of FIG. 5, the embodiment illustrated in FIG. 7 uses power profile $a+$. This profile includes subbands A' and B' in each of the two sidebands 704 and 706, as shown.

[0058] As in system 7, the two streams S_1 and S_2 in system 9 are divided into two classes, class I and class II, using a bit stream classifier. Class I bits represent the more important audio bits, and are provided with a

higher level of error protection by associating them with subband B' of the non-uniform power profile a_+ . The subband B' represents the subband of the power profile which is less susceptible to interference, e.g., first adjacent channel interference. Class II bits, of lesser importance to reconstructed audio quality than the class I bits, are provided with a lower power level by associating them with the subband A' of the power profile a_+ . In other words, the most sensitive bits are transmitted in subband B' on both sides of the host and the least sensitive bits are transmitted in subband A' on both sides. This UEP arrangement makes use of the fact that first adjacent interferers generally cause a higher level of interference in subband A' than in subband B'. Performance gains are thus obtained from this type of frequency division UEP by exploiting interference variations across the sidebands. The subbands A' and B' of each sideband 704 and 706 are encoded for transmission using an inner rate 1/2 convolutional code, and a CRC outer code. The system 9 transmission utilizes a four-stream implementation.

[0059] FIG. 7 also shows a portion of a receiver for decoding the multiple streams of system 9. The receiver includes rate 1/2 Viterbi decoders 712, 714 and CRC decoders 732, 734 for use in decoding the respective inner and outer code for stream S_1 , and rate 1/2 Viterbi decoders 722, 724 and CRC decoders 742, 744 for use in decoding the respective inner code and outer code for stream S_2 . In the four-stream implementation subband A' of sideband 704 is decoded in Viterbi decoder 712 and CRC decoder 732, subband B' of sideband 704 is decoded in Viterbi decoder 714 and CRC decoder 734, subband A' of sideband 706 is decoded in Viterbi decoder 722 and CRC decoder 742, and subband B' of sideband 706 is decoded in Viterbi decoder 724 and CRC decoder 744. The outputs of the CRC decoders 732, 734, 742 and 744 are applied to a PAC decoder 750, which generates reconstructed audio output signals for applications to speakers 752, 754. It should be noted that the exemplary systems illustrated in FIGS. 6 and 7 may be configured to introduce delay between the various multiple bit streams, in accordance with the previously-mentioned time diversity techniques.

[0060] Systems 7 and 9 as described above include several built-in digital blend modes that provide graceful degradation in the presence of interference or other types of transmission and/or reception problems. FIG. 8 is a table summarizing these blend modes for a four-stream IBOC-FM system, such as the four-stream implementations of systems 7 and 9. For purposes of FIG. 8, the class I and class II streams associated with one of the sidebands are designated as class I' and class II' streams, respectively, in order to distinguish them from the class I and II bits associated with the other sideband. It is assumed in this example that any delay introduced between the bit streams for time diversity purposes has been removed by the receiver.

[0061] The first column of the table in FIG. 8 speci-

fies the available streams, i.e., which streams can be received without significant degradation in a given transmission situation, and the second column indicates the corresponding quality of the reconstructed audio. For example, if streams corresponding to classes I, II, I' and II' are available, the resultant reconstructed audio quality is on the order of 96 kb/sec single-stream PAC quality. Availability of streams corresponding to classes (I + II + II') or classes (II + I' + II') results in better than 64 kb/sec single-stream PAC quality. Availability of streams corresponding to classes (I + II) or classes (I' + II') results in better than analog FM quality. The quality level associated with availability of streams corresponding to classes (I + I') is unknown, while the quality level associated with availability of streams corresponding to classes I or I' is expected to be severely degraded.

[0062] FIG. 9 is a table providing examples of rate 1/2 channel codes that may be used in systems 2 through 9. M is the code memory and d_f is the free Hamming distance. The code generators are given in octal form and weight spectra (a_d event, c_d bit) are also given. It should be noted that the rate 1/2 codes with $M = 7$ and $M = 9$ have particularly low weights. It is estimated that a choice of $M = 8$, i.e., 256 states, represents a reasonable complexity level for the channel code choice. A number of the rate 1/2 codes shown in the table of FIG. 9 are from T. Ottosson, "Coding, Modulation and Multiuser Decoding for DS-CDMA Systems," Ph.D. thesis, Chalmers University of Technology, Gothenburg, Sweden, November 1997. Of course, many other types and arrangements of codes could be used in the multistream IBOC-FM systems of the invention.

[0063] FIGS. 10 through 13 illustrate performance improvements in an exemplary multistream IBOC-FM system in accordance with the invention. FIGS. 10, 11 and 12 show gains in signal-to-noise ratio (SNR) resulting from the use of rate 1/2, rate 2/3 and rate 3/4 codes, respectively, relative to the rate 4/5, $M = 6$ code in the baseline system 1. Uniform power profile a of FIG. 5 and a Gaussian channel is assumed in each case. In FIG. 10, the gains are shown for the one-sided rate 4/5 system with $d_f = 4$, and for the corresponding double-sided rate 2/5 system with $d_f = 11$. The rate 2/3 and rate 3/4 codes are from G.C. Clark Jr. and J.B. Cain, "Error Correction Coding for Digital Communication," Plenum Press, New York, 1981.

[0064] It should be noted that the audio coder rate for a system in which the baseline rate is changed to rate 1/2 on one sideband, with all other parameters unchanged, is 60 kb/sec. Utilizing an audio coder rate of 64 kb/sec in such a system will require a channel code rate of 8/15. Although such codes are available, these codes are generally optimized with rate compatible punctured code (RCPC) constraints from puncturing a mother code of rate 1/3. Codes providing better performance may be obtained using another mother code, e.g., a rate 1/2 mother code.

[0065] It can be seen from FIG. 10 that the one-sided 60 kb/sec, rate 1/2 system with $M = 6$ is comparable in SNR performance to the double-sided 96 kb/sec, rate 2/5 system with $M = 6$. It is also apparent that the rate 1/2 systems with $M \geq 8$ are superior to the rate 2/5 systems with $M = 6$. In addition, the double-sided 120 kb/sec, rate 1/2, $M = 6$ system is comparable to the 96 kb/sec, rate 2/5, $M = 6$ system in asymptotic error rate performance for the Gaussian channel. Embodiments of the invention in which there is insufficient bandwidth for a rate 1/2 code may utilize, e.g., a rate 8/15 code instead, resulting in somewhat smaller gains in SNR. A straightforward code search may be performed to determine acceptable rate 8/15 codes for such an embodiment.

[0066] FIG 13 summarizes performance measurements based on simulations of the above-described multistream IBOC-FM systems. For the Gaussian channel, the simulations predict a gain of approximately 8 dB in subband B with a rate 1/2 code and a 60 kb/sec audio coder. In subbands A and C, the SNR gain is approximately 4 dB over the baseline 96 kb/sec, rate 4/5 code with uniform power profile *a*. FIG. 13 shows the estimated gains in channel SNR ($E_b N_0$) over the baseline rate 4/5 system 1. The two UEP error probabilities in subband B (or B') and in subbands A plus C (or A') are denoted as P_I and P_{II} , respectively.

[0067] FIG. 13 indicates that, for power profile *b*, the two error rate probabilities P_I and P_{II} are about 4 dB apart. It is believed that the overall system in this case will be performance limited by P_{II} . With power profile *c*, the two error rate probabilities are closer (and both better) than with profile *b*. Power profile *c* may therefore be a preferable solution in applications in which the interference levels are acceptable. The shape of profile *c* can also be further modified as necessary in a particular application. One such possible modification is profile *d* of FIG. 5, which has a lower total sideband power increase than profile *c* and P_I and P_{II} values which are even closer together than those for profile *c*. The optimization of the shape of the power profile may be based on a number of factors, including interference to the host signal, first adjacent interference levels and FCC emission masks or other requirements. For fading channels, the gains in FIG. 13 may be viewed as lower bounds.

[0068] The two-level UEP in the simulations summarized in FIG. 13 is obtained using the same rate 1/2 code in both classes I and II with different average power levels in the two classes. Thus, there is no UEP gain with this approach for the uniform power profile *a*. In other embodiments of the invention, a UEP gain can be obtained by employing two separate channel codes with rates higher (class II) and lower (class I) than 1/2, with an average rate of 1/2. Such an approach can be used, e.g., with a uniform 3 dB power increase over the entire sideband, i.e., power profile *a+*, leading to a similar result as that provided by power profile *d*. The chan-

nel codes in such an embodiment can be found by code search. Alternatively, a frequency division UEP approach can be utilized, such that the same rate 1/2 code is used in subbands B and (A+C). In this case there is no gain on a uniform noise channel, but gains are achieved, e.g., for first adjacent interference type of channels. Additional details regarding this frequency division UEP approach can be found in the above-cited U.S. Patent Application Serial No. 09/163,656.

[0069] There are a number of different options for the number of tones and structure of OFDM modem(s) for use in the illustrative multistream systems listed in FIG. 4. One possible implementation uses two 70 kHz sidebands with about 90 tones on each side. A single 512 fast Fourier transform (FFT) is used in this example implementation, and the number of tones per kHz is 1.29. Another implementation uses twice as many tones, i.e., about 180 tones per sideband, and a single 1024 FFT with zero padding. The symbol time in this implementation is twice as long as in the previous example. In addition, for the same multipath, the relative overhead for the cyclic extension is reduced by a factor of two. The number of tones per kHz in this implementation is 2.57. Yet another option is to use two separate OFDM modems for the upper and lower sideband. With, e.g., two separate 256 FFTs, the cyclic extension overhead is now even less than with the single 1024 FFT with zero padding. The number of tones per kHz in this case is 3.66. Although the FFTs are simpler, two modems have to be used.

[0070] When using the non-uniform power profiles of FIG. 5, it is important that the interleaver design take into account the power profile, even if the channel is a Gaussian channel. This is because different symbols may have different power levels in the OFDM tones. If an entire error event of the convolutional code is associated with only symbols transmitted on low power level tones, the performance is degraded. To obtain the "average power level" behavior of the code, the error events should typically consist of a mixture of high and low power levels. Fortunately, dominating convolutional code error events are typically short in nature. Additional considerations in the interleaver design include time-selective and frequency-selective fading. Short of doing joint convolutional code and interleaver design, there is no absolute guarantee that the average power level behavior will be achieved, and it is possible that a small loss may be incurred.

[0071] Alternative embodiments of the invention can utilize other types of outer codes, e.g., RS, BCH or other linear block codes, other types of inner codes, e.g., various types of convolutional codes, turbo codes, or coding associated with trellis coded modulation, and a variety of different types of interleaving, e.g., block interleaving, convolutional interleaving, or random interleaving. The alternative embodiments could also utilize only an inner code and no outer code, or vice-versa. Embodiments which utilize an RS, BCH or other similar

type of error correcting outer code can of course use the code for error correction.

[0072] It should be noted that one or more of the frequency bands associated with a given host carrier signal in an embodiment of the invention may be arranged so as to overlap with the carrier. Such an embodiment may utilize the precancellation techniques described in, e.g., U.S. Patent Application Serial No. 08/704,470 filed August 22, 1996 in the names of inventors Haralabos C. Papadopolous and Carl-Erik W. Sundberg and entitled "Technique for Simultaneous Communications of Analog Frequency-Modulated and Digitally Modulated Signals Using Precanceling Scheme," and U.S. Patent Application Serial No. 08/834,541 filed March 18, 1997 in the names of inventors Brian Chen and Carl-Erik W. Sundberg and entitled "Band Insertion and Precancellation Technique for Simultaneous Communications of Analog Frequency-Modulated and Digitally Modulated Signals," both of which are assigned to the assignee of the present application and incorporated by reference herein.

[0073] The invention can be applied to decoding of a wide variety of frame formats, including time division multiplexed (TDM), frequency division multiplexed (FDM) and code division multiplexed (CDM) formats, as well as combinations of TDM, FDM, CDM and other types of frame formats. Furthermore, although not described in detail herein, numerous different types of modulation techniques may be used in conjunction with the invention, including, e.g., single-carrier modulation in every channel, or multi-carrier modulation, e.g., OFDM in every channel. A given carrier can be modulated using any desired type of modulation technique, including, e.g., a technique such as m -QAM, m -PSK or trellis coded modulation.

[0074] As previously noted, one or more of the techniques of the invention can be applied to the transmission of digital information other than audio, such as speech, data, video, images and other types of information. Although the illustrative embodiments use audio information, such as that generated by a PAC encoder, the invention is more generally applicable to digital information in any form and generated by any type of compression technique. For example, the embedded audio coder in the exemplary transmitter 201 of FIG. 2 may alternatively be implemented as a multiple description audio coder, or as a combination of a multiple description audio coder and an embedded audio coder. The invention may be implemented in numerous applications, such as simultaneous multiple program listening and/or recording, simultaneous delivery of audio and data, etc. These and numerous other alternative embodiments and implementations within the scope of the following claims will be apparent to those skilled in the art.

Claims

1. A method of processing at least one information signal for transmission in a communication system, the method comprising the steps of:
 - generating a plurality of bit streams from the information signal, each of at least a subset of the bit streams corresponding to a separate representation of at least a portion of the information signal; and
 - transmitting the bit streams in corresponding portions of one or more frequency bands associated with a host carrier signal.
2. The method of claim 1 wherein the host carrier signal is an FM carrier signal.
3. The method of claim 1 wherein the information signal comprises an audio signal.
4. The method of claim 1 wherein the transmitting step includes transmitting the bit streams such that at least one of the bit streams is transmitted with a different transmission characteristic than another of the bit streams.
5. The method of claim 4 wherein the different transmission characteristic includes at least one of a different level of error protection and a different portion of a non-uniform transmission power profile.
6. The method of claim 1 wherein the generating step includes generating first and second multiple description bit streams representative of the information signal.
7. The method of claim 6 wherein the transmitting step further includes transmitting the first multiple description bit stream on a first sideband of the host carrier signal, and transmitting the second multiple description bit stream on a second sideband of the host carrier signal.
8. The method of claim 7 wherein the generating step further includes separating each of the first and second multiple description bit streams into at least first and second class bit streams, wherein each of the first and second class bit streams corresponds to a different level of error protection.
9. The method of claim 8 wherein the transmitting step further includes transmitting the first and second class bit streams associated with the first multiple description bit stream in respective first and second subbands of the first sideband, and transmitting the first and second class bit streams associated with

- the second multiple description bit stream in respective first and second subbands of the second sideband.
10. The method of claim 9 wherein each of the subbands of at least one of the first and second sidebands is associated with a different level of error protection. 5
 11. The method of claim 9 wherein each of the subbands of at least one of the first and second sidebands is associated with at least one of a different portion of a non-uniform transmission power profile and a different susceptibility to interference. 10
 12. The method of claim 1 wherein the generating step includes generating at least a first bit stream having a first coding rate and a second bit stream having a coding rate lower than the first coding rate, and wherein the transmitting step includes transmitting at least the first bit stream in a first sideband of the host carrier signal and the second bit stream in a second sideband of the host carrier signal. 15
 13. The method of claim 1 further including the step of introducing delay between at least a subset of the bit streams prior to the transmitting step in order to provide time diversity in the system. 20
 14. An apparatus for processing at least one information signal for transmission in a communication system, the apparatus comprising: 25
 - a transmitter operative: (i) to generate a plurality of bit streams from the information signal, each of at least a subset of the bit streams corresponding to a separate representation of at least a portion of the information signal, and (ii) to transmit each of the bit streams in corresponding portions of one or more frequency bands associated with a host carrier signal. 30
 15. The apparatus of claim 14 wherein the host carrier signal is an FM carrier signal. 35
 16. The apparatus of claim 14 wherein the information signal comprises an audio signal. 40
 17. The apparatus of claim 14 wherein at least one of the bit streams is transmitted with a different transmission characteristic than another of the bit streams. 45
 18. The apparatus of claim 17 wherein the different transmission characteristic includes at least one of a different level of error protection and a different portion of a non-uniform transmission power profile. 50
 19. The apparatus of claim 14 wherein the transmitter is further operative to generate first and second multiple description bit streams representative of the information signal. 55
 20. The apparatus of claim 19 wherein the transmitter is further operative to transmit the first multiple description bit stream on a first sideband of the host carrier signal, and to transmit the second multiple description bit stream on a second sideband of the host carrier signal.
 21. The apparatus of claim 20 wherein the transmitter is further operative to separate each of the first and second multiple description bit streams into at least first and second class bit streams, wherein each of the first and second class bit streams corresponds to a different level of error protection.
 22. The apparatus of claim 21 wherein the transmitter is further operative to transmit the first and second class bit streams associated with the first multiple description bit stream in respective first and second subbands of the first sideband, and to transmit the first and second class bit streams associated with the second multiple description bit stream in respective first and second subbands of the second sideband.
 23. The apparatus of claim 22 wherein each of the subbands of at least one of the first and second sidebands is associated with a different level of error protection.
 24. The apparatus of claim 22 wherein each of the subbands of at least one of the first and second sidebands is associated with at least one of a different portion of a non-uniform transmission power profile and a different susceptibility to interference.
 25. The apparatus of claim 14 wherein the transmitter is further operative to generate at least a first bit stream having a first coding rate and a second bit stream having a coding rate lower than the first coding rate, and to transmit at least the first bit stream in a first sideband of the host carrier signal and the second bit stream in a second sideband of the host carrier signal.
 26. The apparatus of claim 14 wherein the transmitter is further operative to introduce delay between at least a subset of the bit streams prior to transmission in order to provide time diversity in the system.
 27. An apparatus for processing at least one information signal for transmission in a communication system, the apparatus comprising:

means for generating a plurality of bit streams from the information signal, each of at least a subset of the bit streams corresponding to a separate representation of at least a portion of the information signal; and

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means for transmitting the bit streams in corresponding portions of one or more frequency bands associated with a host carrier signal.

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28. A method of processing at least one information signal in a communication system, the method comprising the steps of:

receiving a plurality of bit streams, each of at least a subset of the bit streams corresponding to a separate representation of at least a portion of the information signal, wherein the bit streams are transmitted in corresponding portions of one or more frequency bands associated with a host carrier signal; and
reconstructing the information signal from the received bit streams.

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29. An apparatus for processing at least one information signal in a communication system, the apparatus comprising:

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a receiver operative: (i) to receive a plurality of bit streams, each of at least a subset of the bit streams corresponding to a separate representation of at least a portion of the information signal, wherein the bit streams are transmitted in corresponding portions of one or more frequency bands associated with a host carrier signal, and (ii) to reconstruct the information signal from the received bit streams.

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30. An apparatus for processing an encoded signal, said encoded signal being produced by generating a plurality of bit streams from an input signal, each of at least a subset of the bit streams corresponding to a separate representation of at least a portion of the input signal, said bit streams being transmitted through a communications channel in corresponding portions of one or more frequency bands associated with a host carrier signal, the apparatus comprising:

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means for receiving said encoded signal from said communications channel;

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means for decoding said received encoded signal; and

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means for recovering said input signal from said decoded signal.

FIG. 1

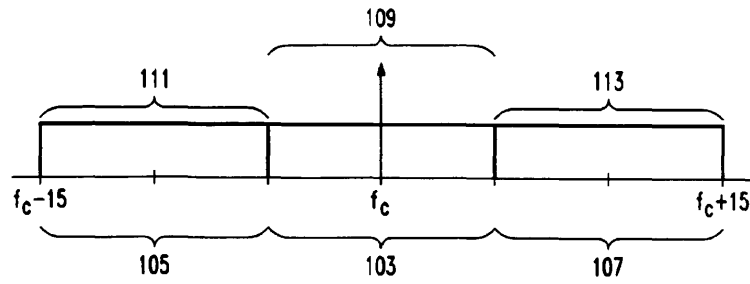


FIG. 2

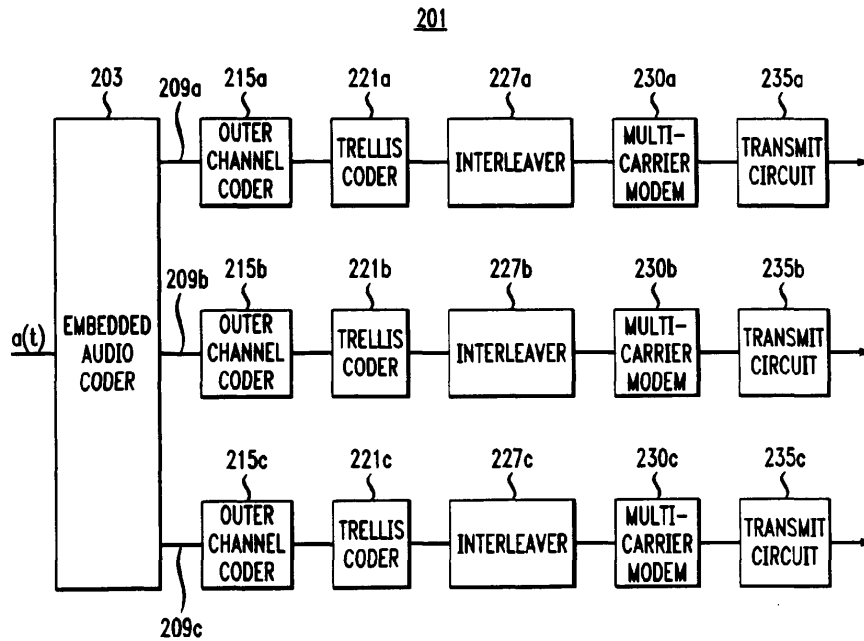


FIG. 3

301

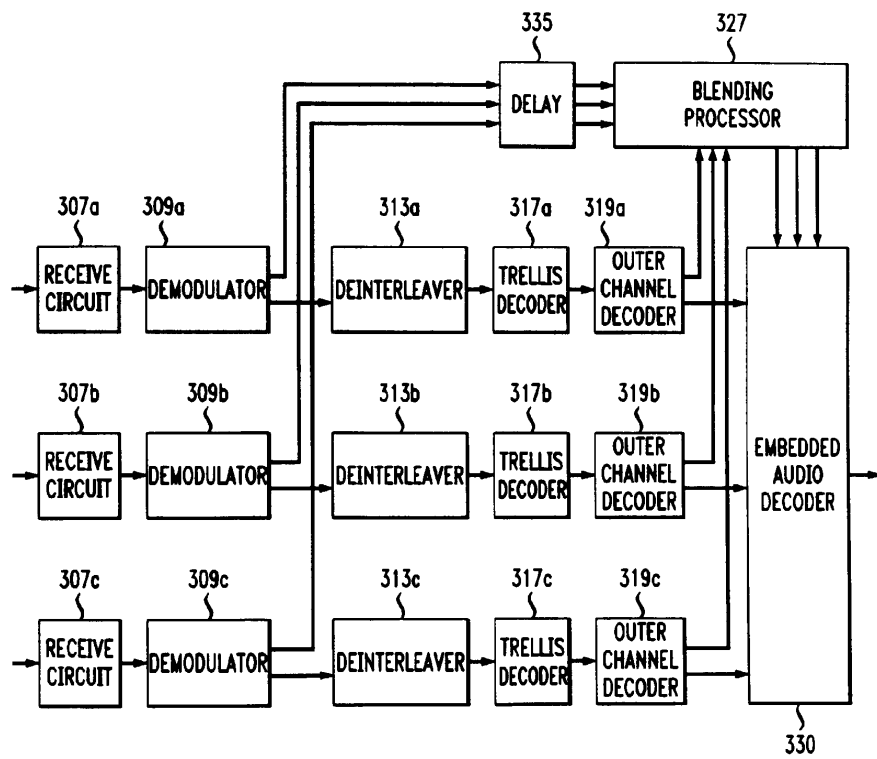


FIG. 4

SYSTEM #	AUDIO CODER RATE kb/s ONE/TWO SIDEBANDS	CHANNEL CODE RATE ONE SIDEBAND	CHANNEL CODE RATE TWO SIDEBAND	POWER PROFILE	SOURCE CODER TYPE	CHANNEL CODE TYPE	MS
1	96/96	4/5	2/5	a		OBP CPPC	1
2	64/64	1/2	1/4	a		OBP CPPC	1
3	64/128	1/2	1/2	a,a+	MD	CC	2
4	64/64	1/2	1/4	b,c,d,e		OBP CPPC	1
5	64/128	1/2	1/2	b,c,d,e	MD	CC	2
6	64/128	1/2	1/2	b,c,d,e	MD C/E	CC	3
7	64/128	1/2	1/2	b,c,d,e	MD UEP2	CC	4/6
8	64/128	1/2	1/2	b,c,d,e	MD C/E	CC	4/6
9	64/128	1/2	1/2	a,a+	MD UEP2	CC	4

FIG. 5

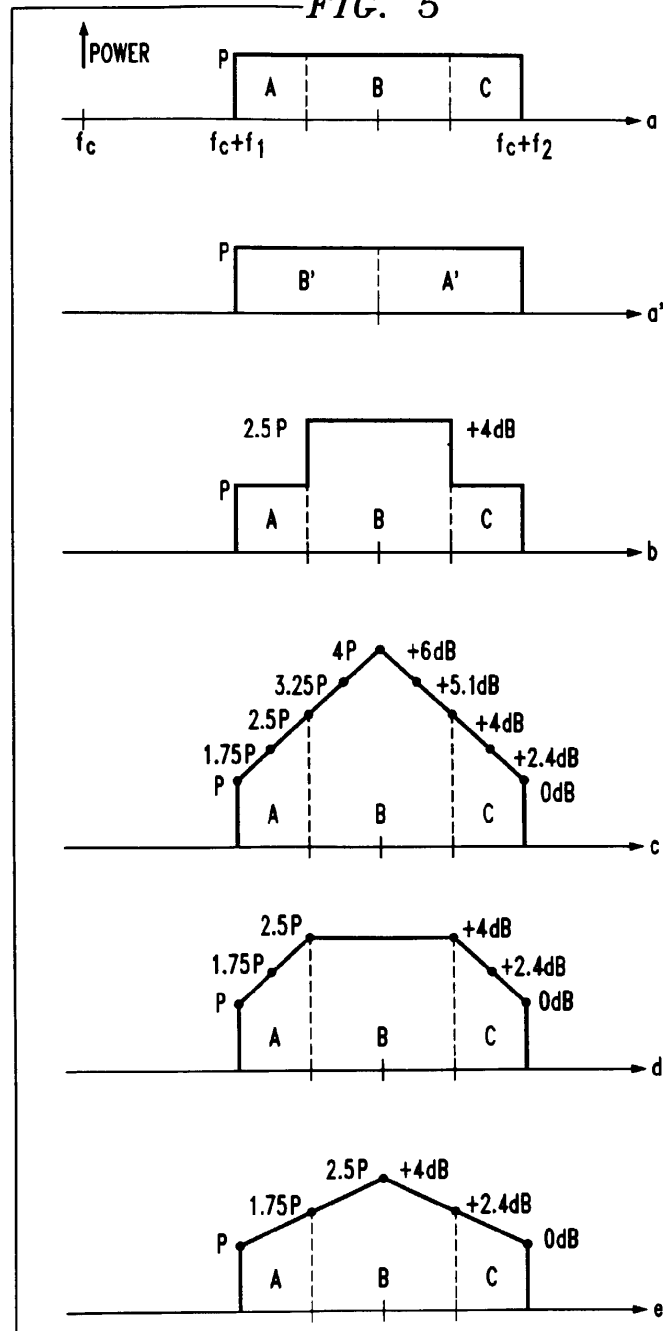


FIG. 6

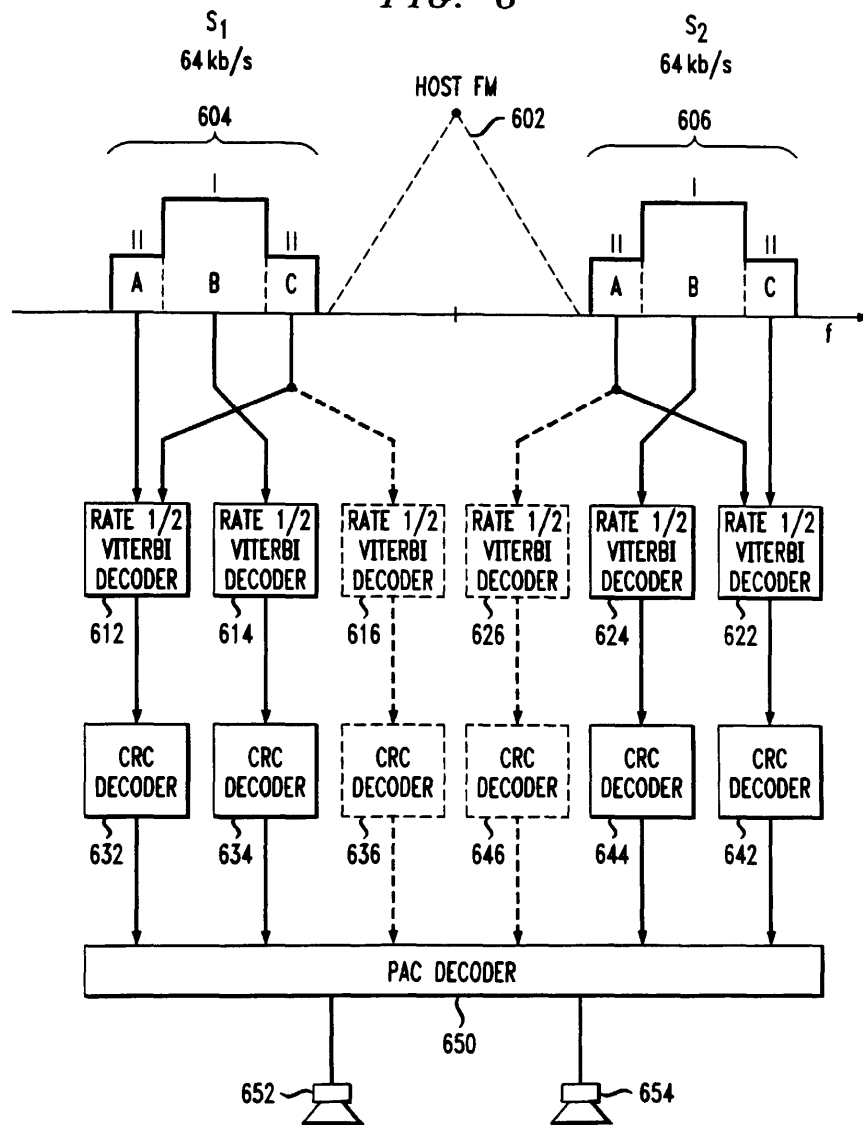


FIG. 7

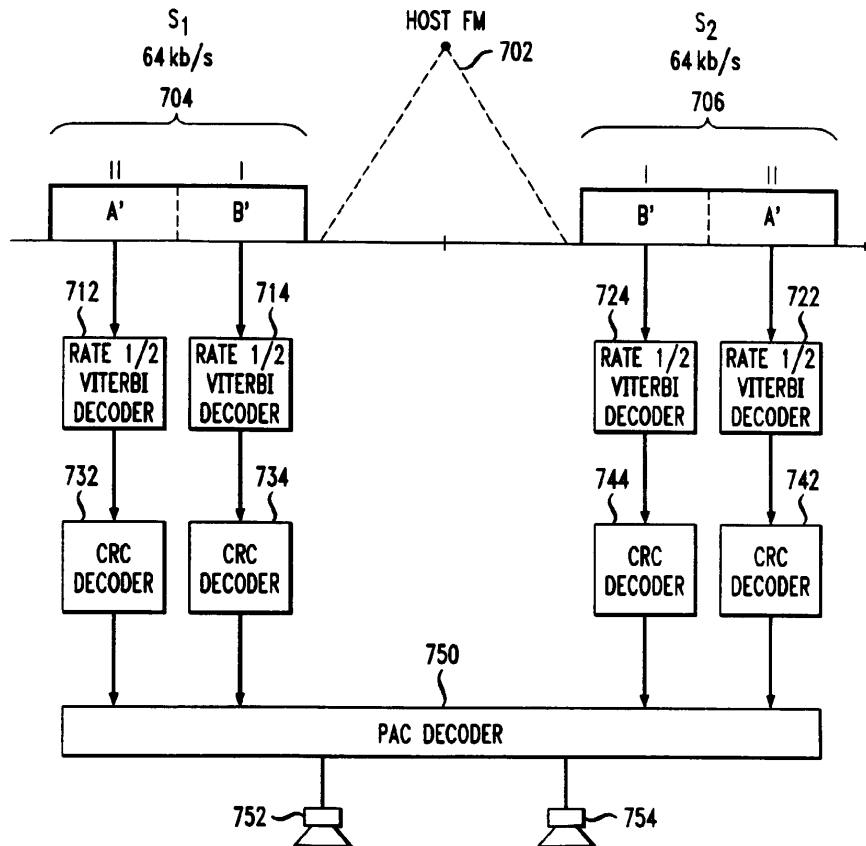


FIG. 8

AVAILABLE STREAMS	CORRESPONDING QUALITY
$I + I' + II + II'$	96 kbps SINGLE STREAM PAC
$(I + II + II') \text{ OR } (I' + II' + II)$	BETTER THAN 64 kbps PAC
$(I + II) \text{ OR } (I' + II')$	BETTER THAN ANALOG FM
$(I + I')$	UNKNOWN
$I \text{ OR } I'$	—

FIG. 9

M + 1	GENERATORS	d_f	$(a_d, d = d_f, d_f + 1, \dots, d_f + 19)$ $[c_d, d = d_f, d_f + 1, \dots, d_f + 19]$
7	133, 171	10	$(11, 0, 38, 0, 193, 0, 1331, 0, 7275, 0, 40406, 0, 234969, 0, 1337714, 0,$ $7594819, 0, 43375588, 0)$ $[36, 0, 211, 0, 1404, 0, 11633, 0, 77433, 0, 502690, 0, 3322763, 0,$ $21292910, 0, 134365911, 0, 843425871, 0]$
8	247, 371	10	$(1, 6, 12, 26, 52, 132, 317, 730, 1823, 4446, 10739, 25358, 60773, 146396,$ $350399, 842174, 2021290, 4853474, 11648661, 27945646)$ $[2, 22, 60, 148, 340, 1008, 2642, 6748, 18312, 48478, 126364, 320062,$ $821350, 2102864, 5335734, 13549068, 34254388,$ $86441848, 217480314, 545858054]$
9	561, 753	12	$(11, 0, 50, 0, 286, 0, 1630, 0, 9639, 0, 55152, 0, 320782, 0, 1859184, 0,$ $10777264, 0, 62423710, 0)$ $[33, 0, 281, 0, 2179, 0, 15035, 0, 105166, 0, 692330, 0, 4580007, 0,$ $29692894, 0, 190453145, 0, 1208999091, 0]$
10	1151, 1753	12	$(1, 7, 19, 28, 69, 185, 411, 1010, 2492, 5963, 14192, 34584, 83567, 200343,$ $483393, 1165406, 2809777, 6773483, 16324253, 39351344)$ $[2, 21, 100, 186, 474, 1419, 3542, 9774, 25950, 66831, 171594, 447372,$ $1152976, 2938087, 7497956, 19072552, 48400420, 122452387,$ $309085546, 778801868]$
11	3345, 3613	14	$(14, 0, 92, 0, 426, 0, 2595, 0, 15221, 0, 87694, 0, 509876, 0, 2975097, 0,$ $17303477, 0, 100650003, 0)$ $[56, 0, 656, 0, 3708, 0, 27503, 0, 185997, 0, 1220645, 0, 7966761, 0,$ $51581661, 0, 329655865, 0, 2089605350, 0]$
12	5261, 7173	15	$(14, 21, 34, 101, 249, 597, 1373, 3317, 8014, 19559, 47302, 113723,$ $274266, 662666, 1600334, 3857052, 9308986, 22473832,$ $54226452, 130860787)$ $[66, 98, 220, 788, 2083, 5424, 13771, 35966, 93970, 246720, 635694,$ $1623432, 4149988, 10599534, 26964102, 68271886, 172723512,$ $436205306, 1098861232, 2763565986]$
13	12767, 16461	16	$(14, 38, 35, 108, 342, 724, 1604, 4020, 9825, 23899, 57724, 138584,$ $335272, 808236, 1952588, 4714596, 11375389, 27462352,$ $66275890, 159940379)$ $[60, 188, 288, 952, 2754, 6628, 16606, 44640, 116712, 304987, 785180,$ $2002076, 5132496, 13067080, 33236580, 84264272, 213035502,$ $537722506, 1354359096, 3404955291]$

FIG. 10

RATE 1/2 CODES M d _f		GAIN IN SNR RELATIVE TO M = 6, R = 4/5*	GAIN IN SNR RELATIVE TO M = 6, R = 2/5**
6	10	4.0 dB	-0.4 dB
8	12	4.8 dB	0.4 dB
10	14	5.4 dB	1.0 dB
12	16	6.0 dB	1.5 dB

*d_f = 4**d_f = 11*FIG. 11*

RATE 2/3 CODES M d _f		GAIN IN SNR RELATIVE TO M = 6, R = 4/5
6	6	1.8 dB
8	8	3.0 dB

FIG. 12

RATE 3/4 CODES M d _f		GAIN IN SNR RELATIVE TO M = 6, R = 4/5
6	5	1.0 dB
8	6	1.8 dB

FIG. 13

OFDM POWER PROFILE	BANDS B, (B') P _I	BANDS A + C, (A') P _{II}	TOTAL SIDEBAND POWER INCREASE
a, a'	4 dB	4 dB	0 dB
a+, a'+	7 dB	7 dB	3 dB
b	8 dB	4 dB	2.4 dB
c	9.1 dB	6.4 dB	4.0 dB
d	8 dB	6.4 dB	3.3 dB
e	7.3 dB	5.4 dB	2.4 dB

PATENT ABSTRACTS OF JAPAN

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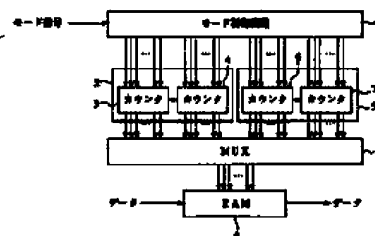
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MIYATO YOSHIKAZU****(54) INTERLEAVE CIRCUIT AND DEINTERLEAVE CIRCUIT**

(57)Abstract:

PURPOSE: To interleave/deinterleave data of plural kinds of interleave formats by one circuit.

CONSTITUTION: Data to be interleaved is inputted to a RAM 9. The mode signal which includes information related to the frame length and the depth of interleave of data inputted to the RAM 9 is inputted to a mode control circuit 1. In an address generator 2 or 5, a write address or a read address to the RAM 9 is generated in accordance with the mode signal. Data is written in or read out from the RAM 9 in accordance with the write address or the read address.



* NOTICES *

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- 1.This document has been translated by computer. So the translation may not reflect the original precisely.
- 2.**** shows the word which can not be translated.
- 3.In the drawings, any words are not translated.

CLAIMS

[Claim(s)]

[Claim 1]An interleave circuit being an interleave circuit which interleaves and outputs inputted data, changing frame length or the depth of interleave corresponding to a predetermined mode signal, and interleaving the aforementioned data.

[Claim 2]The interleave circuit according to claim 1 which is provided with the following and characterized by the aforementioned memory measure outputting the aforementioned data memorized to an address which the aforementioned reading address shows to it while memorizing the aforementioned data to an address which the aforementioned writing address shows.

A calculating means which searches for interleave information which is information about frame length and the depth which interleave the aforementioned data based on the aforementioned predetermined mode signal.

A memory measure which memorizes the aforementioned data.

A generating means which generates a writing address and a reading address to the aforementioned memory measure based on the aforementioned interleave information.

[Claim 3]Have the following and said 1st depth counting means, Count up, when said 1st frame length counting means counts even the greatest aforementioned frame length, and said 2nd frame length counting means, Count up, when said 2nd depth counting means counts even the greatest aforementioned depth, and the aforementioned writing address, Make counted value of said 1st depth counting means or each 1st frame length counting means into an upper address or a lower address, and the aforementioned reading address, The interleave circuit according to claim 2 being what makes counted value of said 2nd depth counting means or each 2nd frame length counting means an upper address or a lower address.

A frame length difference which is a difference with frame length in case the aforementioned interleave information interleaves greatest frame length and the aforementioned data of interleave, And the 1st and the 2nd frame length counting means among which it becomes with a depth difference which is a difference with the depth when interleaving the greatest depth and the aforementioned data of interleave, and the aforementioned generating means counts even the greatest frame length [difference / aforementioned / frame length] of interleave repeatedly.

The 1st and the 2nd depth counting means which count even the greatest depth [difference / aforementioned / depth] of interleave repeatedly.

[Claim 4]The Di interleave circuit which is the Di interleave circuit which carries out the DIINTA reeve of the inputted data, and outputs it, and is characterized by changing frame length or the depth of a DIINTA reeve, and performing a DIINTA reeve of the aforementioned data corresponding to a predetermined mode signal.

[Claim 5]The Di interleave circuit according to claim 4 which is provided with the following and characterized by the aforementioned memory measure outputting the aforementioned data memorized to an address which the aforementioned reading address shows to it while memorizing the aforementioned data to an address which the aforementioned writing address shows.

A calculating means which searches for DIINTA reeve information which is information about frame length and the depth which carry out the DIINTA reeve of the aforementioned data based on the aforementioned predetermined mode signal.

A memory measure which memorizes the aforementioned data.

A generating means which generates a writing address and a reading address to the aforementioned memory measure based on the aforementioned DIINTA reeve information.

[Claim 6]Have the following and said 1st depth counting means, Count up, whenever said 1st frame length counting means counts even the greatest aforementioned frame length, and said 2nd frame length counting means, Count up, whenever said 2nd depth counting means counts even the greatest aforementioned depth, and the aforementioned writing address, Make counted value of said 2nd depth counting means or each 2nd frame length counting means into an upper address or a lower address, and the aforementioned reading address, The Di interleave circuit according to claim 5 being what makes counted value of said 1st depth counting means or each 1st frame length counting means an upper address or a lower address.

A frame length difference which is a difference with frame length in case the aforementioned DIINTA reeve information carries out the DIINTA reeve of greatest frame length and the aforementioned data of a DIINTA reeve, And the 1st and the 2nd frame length counting means among which it becomes with a depth difference which is a difference with the depth when carrying out the DIINTA reeve of the greatest depth and the aforementioned data of a DIINTA reeve, and the aforementioned generating means counts from the aforementioned frame length difference to the greatest frame length of a DIINTA reeve repeatedly.

The 1st and the 2nd depth counting means which count from the aforementioned depth difference to the greatest depth of a DIINTA reeve repeatedly.

DETAILED DESCRIPTION

[Detailed Description of the Invention]

[0001]

[Industrial Application]This invention relates digital data to interleave, the interleave circuit which carries out a DIINTA reeve, and the Di interleave circuit.

[0002]

[Description of the Prior Art]For example, when transmitting digital information (digital data), the error correction in consideration of the error in the inside of a transmission line is performed. In this case, the system coded, for example with block codes, such as a Reed Solomon code, as error correcting system, Generally the systems using a convolutional code or these systems (for example, syste

m etc. which is further convolutional-code-ized after coding with a block code) that were combined are used.

[0003]In the case of transmission of digital data, in order to prevent an error occurring burstily, interleave of digital data besides an error correction is also performed.

[0004]In [according to interleave, in the transmitting side, replace the turn of digital data transmit, and] a receiving side, Since the burst error generated by returning the turn in order of origin in the transmission line can be seemingly made in to a random error, generating of a fatal error can be prevented.

[0005]Drawing 5 shows the composition of an example of the conventional interleave circuit. The data which should be transmitted is inputted into RAM14 and written in according to the writing address supplied via the multiplexer 13 from the writing address counter 11. As shown in drawing 6 now, supposing the address of the memory space for interleave of RAM14 is arranged, the writing address counter 11, it is made as [output / like 0, 1, ..., L-1, L, L+1, ..., x(D-1) L-1, / synchronizing with the timing as which data is inputted into RAM14, / it / increment a writing address every / 1 / and].

[0006]As a result, the inputted data is written in the transverse direction one by one, as shown in drawing 7 (a), and thereby, one lines [D] which becomes by L data are written in RAM14. A block of data of this LxD individual is one unit of data interleaved.

Hereafter, it is called an interleave block.

[0007]According to the reading address which will be outputted via the multiplexer 13 in an interleave block from the read address counter 12 if all the data is written in, the data memorized by RAM14 is read to a lengthwise direction one by one, as shown in drawing 7 (b). By this, the data with which turn (time series) was replaced will be outputted.

[0008]And completion of read-out of the data within an interleave block will perform interleave to the following interleave block like the case where it mentions above.

[0009]At the time of the timing to which the multiplexer 13 should write data in RAM14, The writing address from the counter 11 is outputted to RAM14, and it is made as [output / to RAM14 / the reading address from the counter 12] at the time of the timing which should read data from RAM14.

[0010]Next, drawing 8 shows the composition of an example of the Di interleave circuit which carries out the DIINTA reeve of the data interleaved in the interleave circuit of drawing 5. In the Di interleave circuit, to RAM24 constituted like RAM14 of the interleave circuit shown in drawing 5, reading and writing are performed conversely and reading and writing of the data at the time of interleave are made as [return / the turn of the replaced data].

[0011]That is, the interleaved data is inputted into RAM24, and according to the writing address supplied via the multiplexer 23 from the writing address counter 21, as shown in drawing 9 (a), it is written in a lengthwise direction one by one.

[0012]And if all the data is written in in interleave Brock (DIINTA reeve block), According to the reading address outputted via the multiplexer 23 from the read address counter 22, the data memorized by RAM14 will be read to a transverse direction one by one, as shown in drawing 9 (b), and the data in which turn (time series) returned by this will be outputted.

[0013]And completion of read-out of the data in interleave Brock will perform the DIINTA reeve to next interleave Brock like the case where it mentions above.

[0014]At the time of the timing for which the multiplexer 24 should write data in RAM24 like the multiplexer 14 shown in drawing 5, The writing address from the counter 21 is outputted to RAM24, and it is made as [output / to RAM24 / the r

reading address from the counter 22] at the time of the timing which should read data from RAM24.

[0015]On the other hand, as a transmission line used for transmission and reception of data, it roughly divides and there are radio and a cable. There are a satellite system which uses artificial satellites (for example, a communications satellite, a broadcasting satellite, etc.), for example, a ground system using a terrestrial wave, etc. in the transmission line of radio. There are a cable system etc. which are transmitted, for example using a cable in the transmission line of a cable.

[0016]Usually, since a transmission condition changes with transmission lines (transmission medium), in the case of transmission and reception of data, the modulation method doubled with the transmission line to be used is used.

[0017]That is, when a satellite system is used, for example, a receiving level is small, therefore since it is easy to produce a transmission error, it is strong by noise, for example, BPSK, QPSK, etc. are used for a modulation method. On the other hand, in a ground system or a cable system, since a large carrier-to-noise ratio (C/N) can be taken compared with a satellite system, the modulation method of a multiple value like 16QAM is used, for example.

[0018]The thing corresponding to a transmission condition is similarly used about error correcting system or the conditions of interleave besides a modulation method.

[0019]

[Problem to be solved by the invention]By the way, about digital transmission of a television signal etc., the distribution service which used the plurality of various transmission lines (transmission medium), i.e., satellite connection which was mentioned above, a terrestrial wave, the cables, etc. can be considered with diversification of media in recent years.

[0020]However, since a modulation method and an error correcting code usually differ also from the conditions of interleave when transmission lines differ as mentioned above, In order to receive diversified digital data (digital data from a different transmission line), the demodulator corresponding to each system (transmission system) is needed. That is, in order to receive three services, a satellite system, a ground system, and a cable system, for example, the demodulator circuit corresponding to each, a decoder circuit, the Di interleave circuit, etc. are needed.

[0021]About the counter 21 of the Di interleave circuit of drawing 8 mentioned above, When interleave FOMATTO (interleave Brock's format) differs (i.e., when the frame length and the depth of interleave (DIINTA reeve) differ from each other), Since a changed part of the address of the lengthwise direction of the memory space shown in drawing 6 changes, corresponding to each interleave format, two or more things from which count width (they are increment or a value which carries out a decrement about counted value) differs are needed.

[0022]Here, the frame length of interleave (DIINTA reeve) means length L beside an interleave block, and the depth of interleave (DIINTA reeve) means length D of the length of an interleave block.

[0023]Therefore, the problem which the Di interleave circuit enlarges and complicates occurred.

[0024]The counter 12 into which count width was changed for every (every transmission line to be used) service had to be formed also about the interleave circuit of drawing 5, and the problem to which low cost-ization by mass production becomes difficult occurred.

[0025]This invention is made in view of such a situation, suppresses enlargement of a circuit, and complication to the minimum, and enables it to correspond to two or more interleave formats.

[0026]

[Means for solving problem]The interleave circuit according to claim 1 is an interleave circuit which interleaves and outputs the inputted data, changes the frame length or the depth of interleave corresponding to a predetermined mode signal, and interleaves data.

[0027]The calculating means (for example, mode control circuit 1 shown in drawing 1) which searches for the interleave information which is information about the frame length and the depth in which the interleave circuit according to claim 2 interleaves data based on a predetermined mode signal, Based on the memory measure (for example, RAM9 shown in drawing 1) which memorizes data, and interleave information, Have a generating means (for example, address generators 2 and 5 shown in drawing 1) which generates the writing address and reading address to a memory measure, and while memorizing data to the address which a writing address shows, a memory measure, The data memorized to the address which a reading address shows is outputted.

[0028]The frame length difference whose interleave circuit according to claim 3 is a difference with frame length in case interleave information interleaves the greatest frame length and data of interleave, And it becomes with the depth difference which is a difference with the depth when interleaving the greatest depth and data of interleave, The 1st and the 2nd frame length counting means (for example, counters 3 and 7 shown in drawing 1) among which a generating means counts even the greatest frame length [difference / frame length] of interleave repeatedly, The 1st and the 2nd depth counting means which count even the greatest depth [difference / depth] of interleave repeatedly. (For example, counters 4 and 6 shown in drawing 1) Have and the 1st depth counting means, It counts up, whenever the 1st frame length counting means counts even the greatest frame length, The 2nd frame length counting means counts up, whenever the 2nd depth counting means counts even the greatest depth, A writing address makes counted value of the 1st depth counting means or each 1st frame length counting means an upper address or a lower address, and it a reading address, It is characterized by being what makes counted value of the 2nd depth counting means or each 2nd frame length counting means an upper address or a lower address.

[0029]The DI interleave circuit according to claim 4, It is the DI interleave circuit which carries out the DIINTA reeve of the inputted data, and outputs it, the frame length or the depth of a DIINTA reeve is changed corresponding to a predetermined mode signal, and the DIINTA reeve of data is performed.

[0030]The DI interleave circuit according to claim 5, The calculating means (for example, mode control circuit 101 shown in drawing 4) which searches for the DIINTA reeve information which is information about the frame length and the depth which carry out the DIINTA reeve of the data based on a predetermined mode signal, The memory measure (for example, RAM109 shown in drawing 4) which memorizes data, The generating means which generates the writing address and reading address to a memory measure based on DIINTA reeve information. (For example, address generators 102 and 105 shown in drawing 4) It has, and a memory measure outputs the data memorized to the address which a reading address shows to it, while memorizing data to the address which a writing address shows.

[0031]The DI interleave circuit according to claim 6, The frame length difference which is a difference with frame length in case DIINTA reeve information carries out the DIINTA reeve of the greatest frame length and data of a DIINTA reeve, And it becomes with the depth difference which is a difference with the depth when carrying out the DIINTA reeve of the greatest depth and data of a DIINTA reeve, The 1st and the 2nd frame length counting means (for example, counters 1

03 and 107 shown in drawing 4) among which a generating means counts from a frame length difference to the greatest frame length of a DIINTA reeve repeatedly, The 1st and the 2nd depth counting means which count from a depth difference to the greatest depth of a DIINTA reeve repeatedly. (For example, counters 104 and 106 shown in drawing 4) Have and the 1st depth counting means, It counts up, whenever the 1st frame length counting means counts even the greatest frame length, The 2nd frame length counting means counts up, whenever the 2nd depth counting means counts even the greatest depth, A writing address is what makes counted value of the 2nd depth counting means or each 2nd frame length counting means an upper address or a lower address, A reading address is characterized by being what makes counted value of the 1st depth counting means or each 1st frame length counting means an upper address or a lower address.

[0032]

[Function]In the interleave circuit according to claim 1, since the frame length or the depth of interleave is changed and data is interleaved corresponding to a predetermined mode signal, enlargement of a circuit can be suppressed to the minimum and it can respond to two or more interleave formats.

[0033]In the interleave circuit according to claim 2, interleave information is searched for based on a predetermined mode signal, and the writing address and reading address to a memory measure are generated based on the interleave information. And while making the address which a writing address shows memorize data, the data memorized to the address which a reading address shows is made to output to a memory measure. Therefore, enlargement of a circuit can be suppressed to the minimum and it can respond to two or more interleave formats.

[0034]In the interleave circuit according to claim 3, The 1st depth counting means counts up, whenever the 1st frame length counting means counts even the greatest frame length, Whenever the 2nd frame length counting means counts [the 2nd depth counting means] even the greatest depth, while counting up, by the 1st and 2nd frame length counting means, While even the greatest frame length [difference / frame length] of interleave counts repeatedly, even the greatest depth [difference / depth] of interleave counts by the 1st and 2nd depth counting means repeatedly. And the counted value of the 1st depth counting means or each 1st frame length counting means, It is considered as the upper address of a writing address, or a lower address, and let counted value of the 2nd depth counting means or each 2nd frame length counting means be an upper address of a reading address, or a lower address. Therefore, it can respond to two or more interleave formats, without changing the count width of the 1st, 2nd frame length counting means, 1st, and 2nd depth counting means.

[0035]In the Di interleave circuit according to claim 4, Since the frame length or the depth of a DIINTA reeve is changed and the DIINTA reeve of data is performed corresponding to a predetermined mode signal, enlargement of a circuit can be suppressed to the minimum and it can respond to two or more interleave formats.

[0036]In the Di interleave circuit according to claim 5, DIINTA reeve information is searched for based on a predetermined mode signal, and the writing address and reading address to a memory measure are generated based on the DIINTA reeve information. And while making the address which a writing address shows memorize data, the data memorized to the address which a reading address shows is made to output to a memory measure. Therefore, enlargement of a circuit can be suppressed to the minimum and it can respond to two or more interleave formats.

[0037]In the Di interleave circuit according to claim 6, The 1st depth counting m

means counts up, whenever the 1st frame length counting means counts even the greatest frame length, Whenever the 2nd frame length counting means counts [the 2nd depth counting means] even the greatest depth, while counting up, by the 1st and 2nd frame length counting means, While even the greatest frame length [difference / frame length] of interleave counts repeatedly, even the greatest depth [difference / depth] of interleave counts by the 1st and 2nd depth counting means repeatedly. And the counted value of the 2nd depth counting means or each 2nd frame length counting means, It is considered as the upper address of a writing address, or a lower address, and let counted value of the 1st depth counting means or each 1st frame length counting means be an upper address of a reading address, or a lower address. Therefore, it can respond to two or more interleave formats, without changing the count width of the 1st, 2nd frame length counting means, 1st, and 2nd depth counting means.

[0038]

[Working example] Drawing 1 is a block diagram showing the composition of one working example of the interleave circuit of this invention. In this interleave circuit, the data which should be interleaved to RAM9 is inputted and it is made as [interleave / data] in RAM9 by performing writing of data as shown in drawing 7 mentioned above, and read-out. What has the data storage capacity of LMAXx DMAX described below is used for RAM9.

[0039] Before data is supplied at the same time as data is supplied to RAM9 or, it is made as [supply / from the circuit which is not illustrated / to the mode control circuit 1 / a mode signal]. Here, the frame length L at the time of interleaving the data inputted into RAM9 and depth D are contained in the mode signal. The mode control circuit 1 receives a mode signal, and computes difference SL of frame length, or difference SD of the depth according to a following formula.

$SL = LMAX - LSD = DMAX - D$ [0040] The value of BEKI ** of 2 in which LMAX or DMAX is larger respectively here than the frame length or the depth of the greatest (you are going to make it interleave) interleave block it is going to make correspond to this interleave circuit. (LMAX or DMAX is hereafter called suitably the greatest frame length or depth of interleave, respectively.) -- it is .

[0041] That is, when frame length shall be the maximum and shall respond, for example to the interleave block of 15, LMAX needs to set this interleave circuit to 16 (=24>15), for example (32 (=25), 64 (=26), etc. may be sufficient). The depth is the maximum, and when it shall respond, for example to the interleave block of 24, DMAX needs to set this interleave circuit to 32 (=25>24), for example (64 (=26), 128 (=27), etc. may be sufficient).

[0042] Difference SL of frame length and difference SD of the depth which were computed in the mode control circuit 1 are made as [read / by the address generators 2 and 5].

[0043] The address generator 2 comprises the counters 3 and 4, and the address generator 5 comprises the counters 6 and 7. The counters 3 and 7 are made as [count /, for example / even the greatest frame length / 0 / LMAX / incrementing the counted value every / 1 / repeatedly].

The counters 4 and 6 are made as [count /, for example / even the greatest depth DMAX / 0 / incrementing the counted value every / 1 / repeatedly].

[0044] At the time of the operation start of a circuit, the counters 3 and 7 read difference SL of frame length from the mode control circuit 1, initialize counted value to the value, and start a count to it. The counters 4 and 6 read difference DL of the depth from the mode control circuit 1, initialize counted value to the value, and start a count to it.

[0045] The counters 3, 4, 6, and 7 are own ripple carries (after being set to LMAX or DMAX, counted value by counting up only further 1 (increment)). it is uncou

table in person -- be alike with the signal which shows that wind going up arose to initialize counted value as follows -- now, it is.

[0046] That is, if a ripple carry occurs in self, the counters 3 and 7 will read difference SL of frame length from the mode control circuit 1, and will initialize counted value to the value. Therefore, as mentioned above depending on the counters 3 and 7, even the greatest frame length [$SL / \text{of frame length} / \text{difference}$] LMAX will count repeatedly.

[0047] If a ripple carry occurs in self, the counters 4 and 6 will read difference SD of the depth from the mode control circuit 1, and will initialize counted value to the value. Therefore, as mentioned above depending on the counters 4 and 6, even the greatest depth DMAX [$SD / \text{of the depth} / \text{difference}$] will count repeatedly.

[0048] The counter 3 is made as [increment / counted value / every / 1] synchronizing with timing to which data which should be interleaved to RAM9 is supplied.

The counter 4 is made as [increment / counted value / every / 1], if a ripple carry (the sign C shows a figure) arises at the counter 3.

[0049] The counted value of the counters 3 and 4 is supplied to the multiplexer 8. The multiplexer 8 is made as [output / the counted value from the counters 3 and 4 / to RAM9 / as a writing address] at the time of the timing which should write data in RAM9. In this case, the writing address is made as [constitute /, respectively / as a lower address or an upper address] in the counted value of the counter 3 or 4.

[0050] For example, now if $LMAX=DMAX=256 (=28)$, the address of memory space as shown in drawing 2 depending on an above-mentioned writing address can be expressed. In drawing 2, hexa (hexadecimal number) has shown the address.

[0051] And if an interleave block is set to 253×254 in this case, for example, That is, if the frame length L at the time of interleaving the data inputted into RAM9 or depth D is set to 253 or 254, respectively, difference SL of frame length or difference SD of the depth will be set to 3 (= $256-253$) or 2 (= $256-254$), respectively. Therefore, at the counter 3, it synchronizes with the entry-of-data timing (clock which controls entry-of-data timing) of RAM9 in this case, A count is started from the initial value (difference of frame length) 03H, and the count is performed like 04H, ..., 0EH, 0FH, 10H, ..., FDH, FEH, and FFH. On the other hand, although a count is started from the initial value (difference of the depth) 02H in the counter 4, While the counter 3 counts from 03H to FFH since counted value is not changed until a ripple carry occurs from the counter 3 as mentioned above, 02H is outputted as the counted value.

[0052] Therefore, this case -- RAM9 -- the counter 3 or 4 -- each counted value was made into the lower address or the upper address -- Address 0203H-0204H of the top line of the memory space enclosed with having been square in drawing 2, ..., 020EH, 020FH, 0210H, ..., 02FDH, 02FEH, and 02FFH will be given one by one as a writing address.

[0053] Then, in the counter 3, if count-up from the counted value FFH is performed, a ripple carry will be generated and the counted value will turn into the initial value 03H which is a difference of frame length as mentioned above. If a ripple carry is generated at the counter 3, as mentioned above, only 1 will increment the counted value and the counter 4 will set it to 03H. In the counter 3, since the count from 03H is performed again, in this case to RAM9, Address 0303H-0304H [of the memory space enclosed with having been square in drawing 2] of the 2nd line, ..., 030EH, 030FH, 0310H, ..., 03FDH, 03FEH, and 03FFH will be given one by one as a writing address.

[0054]Hereafter, even address FF03H of the lowermost row of the memory space enclosed with having been square in drawing 2, FF04H, ..., FF0EH, FF0FH, FF10H, ..., FFFDH, FFFE H, and FFFFH are given to RAM9 one by one as a writing address in a similar manner.

[0055]Therefore, as shown in drawing 7 (a), it is written in the memory space of 253x254 which the inputted data was square in drawing 2, and surrounded one by one in the transverse direction, and one lines [254] which becomes by 253 data by this are memorized by RAM9. That is, the data of an interleave block of 253x254 is memorized.

[0056]In the counter 4, if that counted value is set to FFH and this count-up from FFH is performed, a ripple carry will be generated. When a ripple carry occurs at the counter 4, the counted value is set to 02H which is a difference of the depth as mentioned above, and the writing address to next interleave Block will be generated by this.

[0057]If the data of 253x254 is written in in one interleave block, i.e., this case, as mentioned above, the multiplexer 8 will output the counted value of the counters 6 and 7 of the address generator 5 to RAM9 as a reading address. In this case, the reading address is made as [constitute /, respectively / as an upper address or a lower address] in the counted value of the counter 6 or 7.

[0058]The counter 6 is made as [increment / counted value / every / 1] synchronizing with timing which should output data interleaved from RAM9.

The counter 7 is made as [increment / counted value / every / 1], if a ripple carry (the sign C shows a figure) arises at the counter 6.

[0059]In now, as mentioned above, difference SL of frame length or difference SD of the depth, Since it is 3 or 2, respectively, in the counter 6, It synchronizes with the output timing (clock which controls the output timing of data) of the data from RAM9, A count is started from the initial value (difference of the depth) 02H, and the count is performed like 03H, 04H, ..., 0EH, 0FH, 10H, ..., FDH, FEH, and FFFH. On the other hand, although a count is started from the initial value (difference of frame length) 03H in the counter 7, While the counter 6 counts from 02H to FFFH since counted value is not changed until a ripple carry occurs from the counter 6 as mentioned above, 03H is outputted as the counted value.

[0060]therefore, this case -- RAM9 -- the counter 6 or 7 -- let each counted value be an upper address or a lower address -- Address 0203H-0303H-0403H of the leftmost sequence of the memory space where the data of 253x254 which should be interleaved enclosed with having been square in drawing 2 was written in, ..., 0E03H, 0F03H-1003H, ..., FD03H, FE03H, and FF03H, It will be given one by one as a reading address.

[0061]Then, in the counter 6, if count-up from the counted value FFFH is performed, a ripple carry will be generated and the counted value will turn into the initial value 02H which is a difference of frame length as mentioned above. If a ripple carry is generated at the counter 6, as mentioned above, only 1 will increment the counted value and the counter 7 will set it to 04H. In the counter 6, since the count from 02H is performed again, in this case to RAM9, Address 0204H-0304H-0404H of the 2nd row, ..., 0E04H, 0F04H-1004H, ..., FD04H, FE04H, and FF04H will be given one by one as a reading address from the left of the memory space enclosed with having been square in drawing 2.

[0062]Even address 02FFH of the rightmost sequence of the memory space which it was square in drawing 2 to RAM9, and was hereafter surrounded to it similarly, 03FFH, 04FFH, ..., 0EFFH, 0FFFH, 10FFH, ..., FDFFH, FEFFH, and FFFFH, It is given one by one as a reading address.

[0063]Therefore, from RAM9, the data of 253x254 enclosed with being square in drawing 2 written in there is read to the lengthwise direction one by one, as shown

own in drawing 7 (b), and one rows [253] which become by 254 data by this are outputted. By this, the data with which turn (time series) was replaced, i.e., the interleaved data, will be obtained.

[0064]In the counter 7, if that counted value is set to FFH and this count-up from FFH is performed, a ripple carry will be generated. When a ripple carry occurs at the counter 7, the counted value is set to 03H which is a difference of frame length as mentioned above, and the reading address to the following interleave block will be generated by this.

[0065]02H thru/or FFH of the memory spaces of 0000H thru/or FFFFH of RAM9 is made into an upper address as mentioned above, the portion expressed in the address which makes 03H thru/or FFH a lower address is used, and interleave is performed.

[0066]Next, drawing 3 shows the situation of interleave at the time of expressing the frame length or the depth at the time of interleaving the data inputted into RAM9 as L or D, respectively. Also in this case, interleave is performed using the portion of LxD which it is square and has been surrounded among the figure of the memory spaces of RAM9 like the case where it mentions above.

[0067]As mentioned above, by changing difference SL of the frame length as an initial value which gives the counters 3 and 7, and difference SD of the depth as an initial value given to the counters 4 and 6 according to the interleave circuit shown in drawing 1, It can respond to various interleave formats (transmission system). That is, by changing a mode signal, interleave Brock's frame length and the depth can be changed (selection), and data can be interleaved. Therefore, simplification (miniaturization of circuit structure) of circuitry can be attained as compared with the case where the counter which gives an address for every interleave format is formed.

[0068]Since it is not necessary to change the increase (variation) of the counted value which the counters 3, 4, 6, and 7 count in this case, that control is easy and high cost-ization of a circuit can be prevented.

[0069]Next, drawing 4 shows the composition of one working example of the Di interleave circuit of this invention. This Di interleave circuit is made as [carry out / the DIINTA reeve of the data of the various interleave formats interleaved in other circuits besides the data by which interleave was carried out in the interleave circuit of drawing 1 mentioned above]. Namely, even if the data of what kind of interleave format which should be carried out a DIINTA reeve to RAM109 is inputted in this interleave circuit, In RAM109, it is made as [carry out / the DIINTA reeve of the data] by performing writing of data as shown in drawing 9 mentioned above, and read-out.

[0070]Mode control circuit 101, address generator 102,105, multiplexer 108, or RAM109 is constituted respectively like mode control circuit [of the interleave circuit shown in drawing 1] 1, address generator 2 and 5, multiplexer 8, or RAM9. The counter 103 or 104 which constitutes the address generator 102 is constituted respectively like the counter 3 or 4 which constitutes the address generator 2 of drawing 1.

The counter 106 or 107 which constitutes the address generator 105 is constituted respectively like the counter 6 or 7 which constitutes the address generator 5 of drawing 1.

It is made as [supply / to the mode control circuit 101 / the mode signal which contains depth D with the frame length L when the data inputted into RAM109 is interleaved].

[0071]And the address which the address generator 5 which gives the reading address of drawing 1, and the address generator 105 constituted similarly generate is made as [supply / via the multiplexer 108 / as a writing address / RAM109]. The address which the address generator 2 which gives the writing address of

drawing 1, and the address generator 102 constituted similarly generate is made as [supply / via the multiplexer 108 / as a reading address / RAM109].

[0072]That is, in this Di interleave circuit, the address generated as a writing address or a reading address in the interleave circuit of drawing 1 is made as [generate /, respectively / as a reading address or a writing address].

[0073]Therefore, it corresponds to depth D with the frame length L when it is interleave-formatted, namely, the inputted data is interleaved in RAM109. As shown in drawing 9 (a) mentioned above and (drawing 7 (b)), after the writing of data is made, as shown in drawing 9 (b) and (drawing 7 (a)), read-out of data will be performed, and the data in which turn (time series) returned by this will be outputted.

[0074]As mentioned above, by this Di interleave circuit as well as the case in the interleave circuit of drawing 1, It can respond to various interleave formats (transmission system) by changing difference SL of the frame length as an initial value which gives the counters 103 and 107, and difference SD of the depth as an initial value given to the counters 104 and 106. That is, by changing a mode signal, by one Di interleave circuit shown in drawing 4, interleave Brock's frame length and the depth can be changed (selection), and the DIINTA receive of data can be performed. Therefore, simplification (miniaturization of circuit structure) of circuitry can be attained as compared with the case where the counter which gives an address for every interleave format is formed.

[0075]Since it is not necessary to change the increase (variation) of the counted value which the counters 103,104,106 and 107 count also in this case, that control is easy and high cost-ization of a circuit can be prevented.

[0076]As a result, when it applies to the receiving set for receiving service of plurality, such as a satellite system which mentioned this Di interleave circuit above, a ground system, and a cable system, enlargement of that equipment and high cost-ization can be prevented.

[0077]Although the thing containing interleave Brock's frame length and the depth was used as a mode signal in this example, Since an interleave format is determined in relation to a modulation method in many cases, usually in such a case, Interleave Brock's frame length and the depth which are used for a modulation method and its modulation method combining are matched, and the signal which can identify a modulation method can be made into a mode signal. In this case, in the mode control circuit 1 (and 101), a modulation method is discriminated from a mode signal and the difference of frame length or the difference of the depth is computed, respectively from the frame length or the depth further matched with that modulation method.

[0078]In this example, although the circuit of drawing 1 was explained as an interleave circuit (it is the Di interleave circuit about the circuit of drawing 4), this circuit can be made into the circuit interleave and both for a DIINTA receive. In this case, when making it operate as an interleave circuit. Each address which the address generator 2 or 5 outputs by the multiplexer 8 as mentioned above When making it give RAM9 as a writing address or a reading address and making it operate as a Di interleave circuit, What is necessary is just to give each address which the address generator 2 or 5 outputs to RAM9 as a reading address or a writing address by the multiplexer 8.

[0079]Therefore, when providing the final controlling element and the control signal input terminal in order to switch operation of the multiplexer 8 as mentioned above for example, Since the same circuit can be used now for both interleave and a DIINTA receive, reduction of a manufacturing cost can be attained.

[0080]In this example, although the counted value of the counters 3 (103), 4 (104), 6 (106), and 7 (107) was incremented every [1] from the difference of the frame length which is an initial value, and the difference of the depth, For example

e, a decrement can be carried out every [1] from interleave Brock's frame length, and the depth. In this case, after counted value is set to 0, it is made to be initialized by frame length or the depth again, and it is made just to generate a ripple carry at this time. By doing in this way, a portion and a portion symmetrical with a point square and shown among the figure of the memory spaces shown in drawing 2 or drawing 3, are used, and interleave (DIINTA reeve) is performed.

[0081]

[Effect of the Invention]Like the above, according to the interleave circuit and the Di interleave circuit of this invention, enlargement of a circuit can be suppressed to the minimum and it can respond to two or more interleave formats.

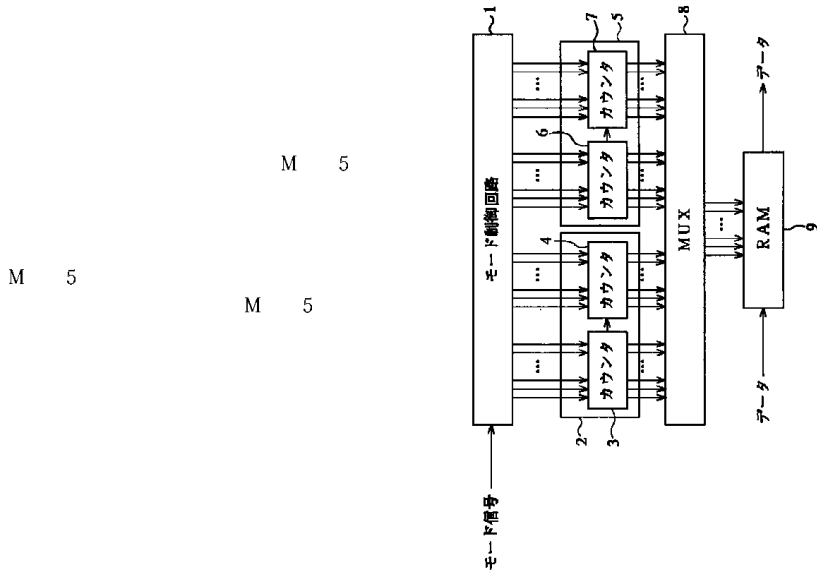
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特開平7-254862
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H 0 4 L 1/00	F			

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(54)【発明の名称】 インターリーブ回路およびディインターリーブ回路



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M 5

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9

W

5

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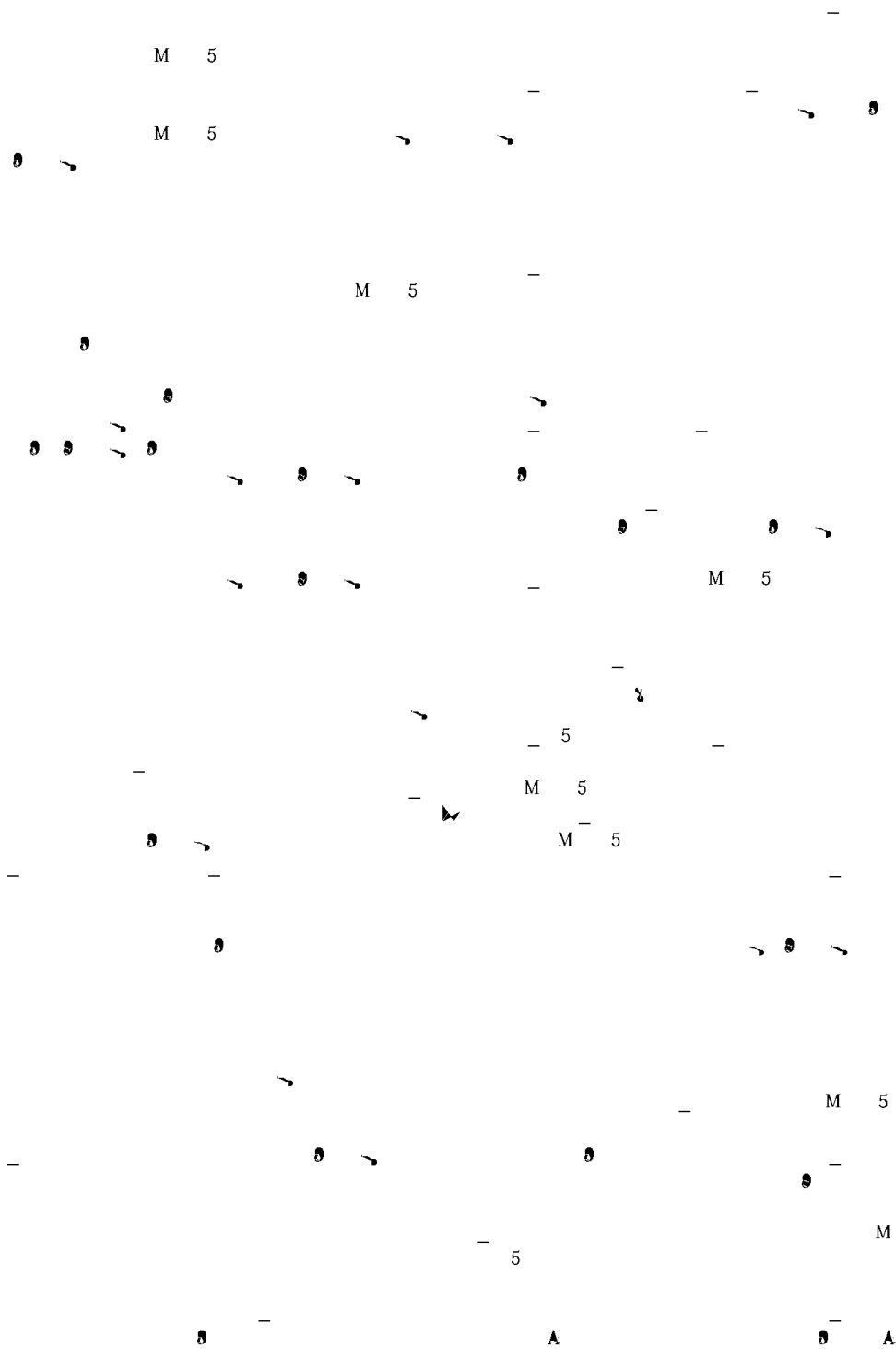
—

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M 5

M 5

5

9
M 5

9 A

M 5

M 5

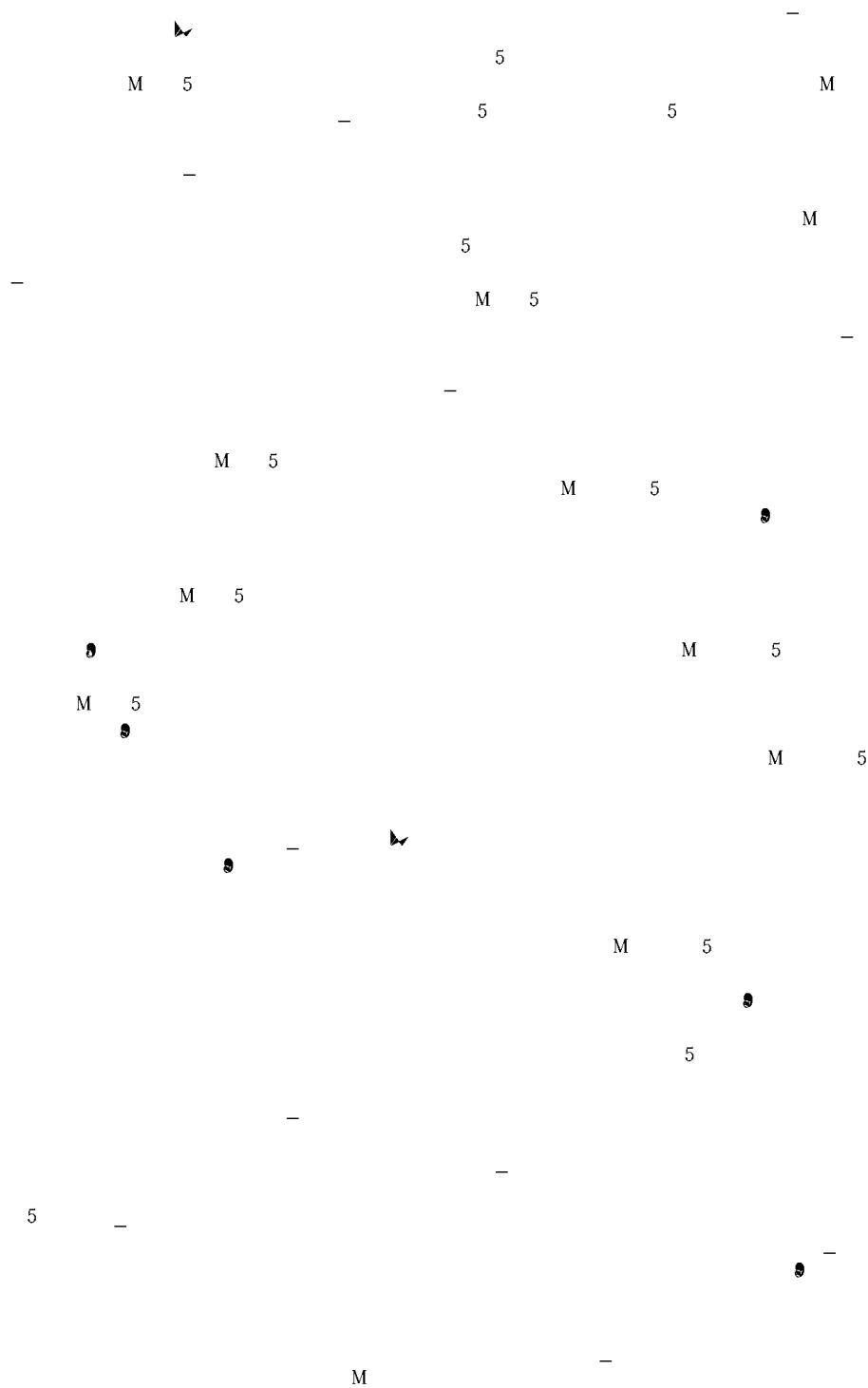
M 5

Three small black and white photographs showing different views of a person's face. The first is a profile view, the second is a frontal view, and the third is a frontal view with a slight smile.

M 5

M 5





M



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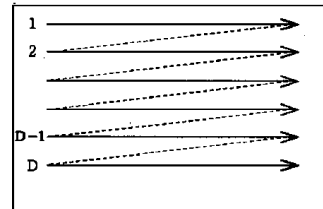
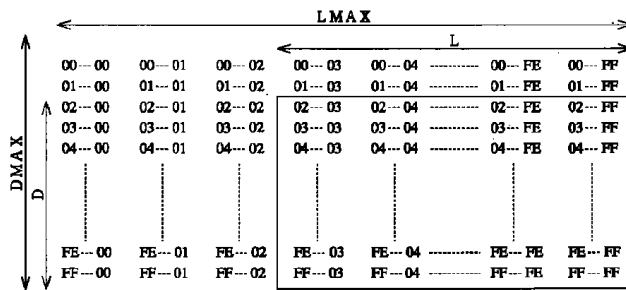
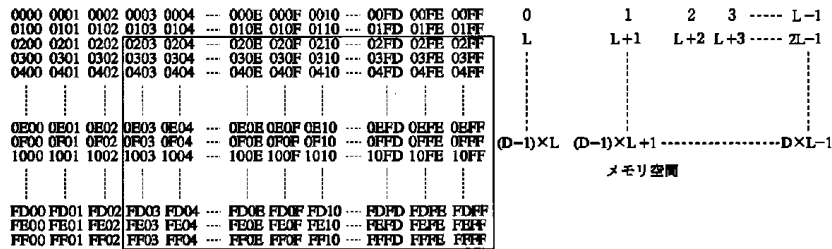
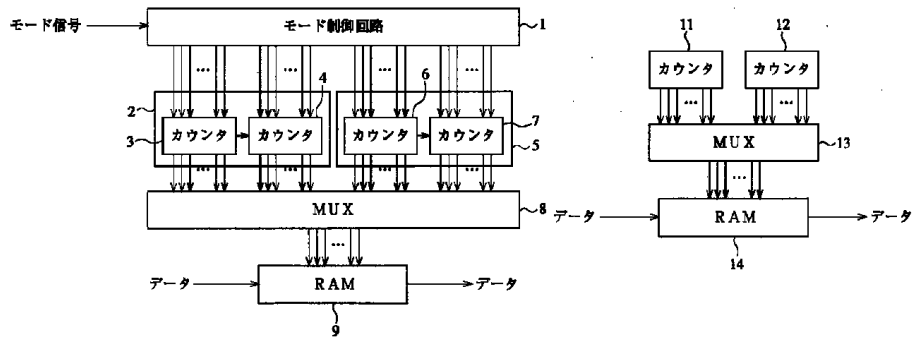
M 5

M 5

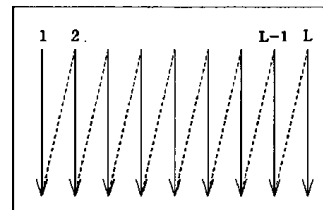
5

5 M

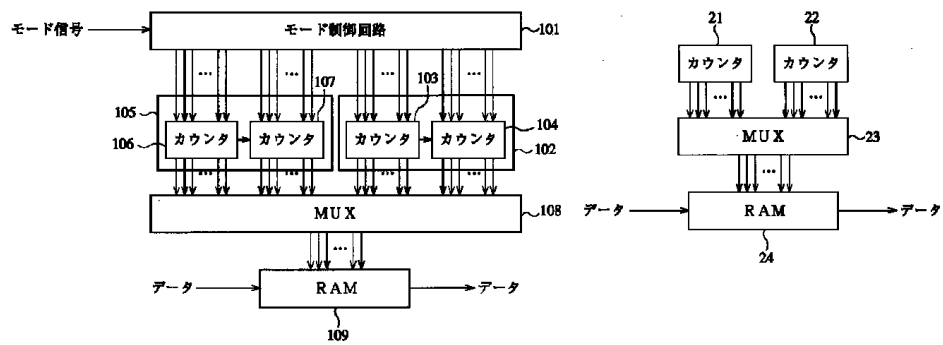
5 M



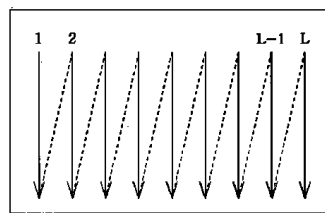
(a)



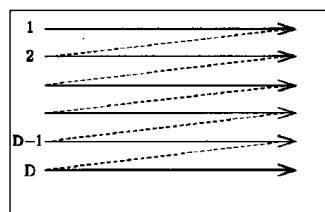
(b)



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(a)



(b)



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(54)Title: TURBO DECODER AND INTERLEAVE / DE-INTERLEAVE APPARATUS (54)発明の名称 ターボ復号装置及びインタリーブ・デインタリーブ装置 10 ... SWITCH CONTROL 6 ... COUNTER FOR GENERATING 0-386 71 ... INTERLEAVE PATTERN ROM 111 ... COUNTER 112 ... MONITOR (57) Abstract A device such as a turbo decoder that requires interleaving and de-interleaving comprises a memory section (5) and a memory control section (12) for changing the sequence in which data are written into or read from the memory section (5) depending on whether to perform interleaving or de-interleaving. The single memory section (5) functions as both an interleaver and a de-interleaver, resulting in a reduction in the cost and size of the device.		

(57)要約

ターボ復号装置などのインタリーブとデインタリーブとを行なう必要がある装置において、メモリ部（５）と、データをインタリーブする場合とデインタリーブする場合とでこのメモリ部（５）に対するデータの書き込み順序及び読み出し順序を変えるメモリ制御部（１２）とをそなえることで、１つのメモリ部（５）でインタリーブ及びデインタリーブとしての機能を実現して、装置規模、コストを低減できるようにする。

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明 細 書

ターボ復号装置及びインタリーブ・デインタリーブ装置

5 技術分野

本発明は、例えば、移動体通信システム等の通信システムに用いて好適な、ターボ復号装置及びインタリーブ・デインタリーブ装置に関する。

背景技術

10 従来より、移動体通信等の無線通信分野では、特定のデータ列部分に連続して発生するバースト誤りをデータ並べ替えにより訂正しやすい形の誤りにする目的でインタリーブ及びそれに応じたデインタリーブが使用される。即ち、送信側において送信信号をインタリーブでインタリーブして送信し、受信側においてその信号をデインタリーブでデインタリーブするといった具合である。

15 以下、従来のインタリーブ及びデインタリーブについて説明する。

図6 (A) は従来のインタリーブの構成を示すブロック図で、この図6 (A) に示すインタリーブ100は、インタリーブRAM101、書き込み用カウンタ102、読み出し用カウンタ103及び読み出しアドレス変換回路104をそなえて構成されている。ただし、この図6 (A) に示すインタリーブ100は、2
20 $4 \times 16 = 384$ 個の入力データ列 (D000, D001, D002, ..., D383) をインタリーブする (つまり、インタリーブ・サイズ = 24×16) ことを前提にしている。

ここで、インタリーブRAM101 (以下、単に「RAM101」と表記する) は、インタリーブ対象の入力データ列 (D000, D001, D002, ..., D383) を記憶するものであり、書き込み用カウンタ102は、0 ~ 383を順にカウントしてその
25 カウント値をRAM101用の書き込みアドレス (A000, A001, A002, ..., A383) として出力するもので、この書き込みアドレス (A000 ~ A383) に従って入力データ列がRAM101のアドレスA000からアドレスA383まで順に書き込まれるようになっている。

また、読み出し用カウンタ103は、RAM101用の読み出しアドレスを生

成するために0～383をカウントするものであり、読み出しアドレス変換回路104は、この読み出し用カウンタ103からのカウント値 x ($=0\sim383$)に対して $x*16 \pmod{383}$ なる演算を施すことにより、読み出し用カウンタ103からのカウント値 x が16おきとなるように変換するもので、これにより、RAM101の読み出しアドレスが、A000, A016, A032, ..., A368, A001, A017, A033, ..., $A_{n*16 \pmod{383}}$, ..., A351, A367, A383 といった具合に16おきに指定されるようになっている。

上述のごとく構成されたインタリーブ100では、図6(B)に示すように、書き込み時には、書き込み用カウンタ102のカウント値がそのまま書き込みアドレスとなり、入力データ列(D000, D001, D002, ..., D383)が順番にRAM101の該当アドレス領域に書き込まれてゆく。一方、読み出し時には、読み出しアドレス変換回路104から16おきに出力される読み出しアドレスで指定されるアドレス領域からデータが順に読み出されてゆく。

この結果、入力データ列(D000, D001, D002, ..., D383)は、D000, D016, D032, ..., D368, D001, D017, ..., $D_{n*16 \pmod{383}}$, ..., D351, D367, D383 というようにデータ並べ替え(インタリーブ)が行なわれて出力されることになる。

つまり、本インタリーブ100は、イメージ的には、例えば図7に示すように、 $24 \times 16 = 384$ 個の入力データ列を矢印A方向に順番にRAM101に書き込んでゆき、読み出し時には矢印B方向に書き込まれた入力データ列を順番に読み出してゆくことで、インタリーブを行なうようになっているのである(このようなインタリーブをブロックインタリーブという)。

一方、図8(A)は従来のデインタリーブの構成を示すブロック図で、この図8(A)に示すデインタリーブ200は、デインタリーブRAM201、書き込み用カウンタ202、読み出し用カウンタ203及び読み出しアドレス変換回路204をそなえて構成されている。ただし、この図8(A)に示すデインタリーブ200は、 $16 \times 24 = 384$ 個の入力データ列(D0, D1, D2, ..., D383)をデインタリーブすることを前提にしている。

ここで、デインタリーブRAM201(以下、単に「RAM201」と表記する)は、デインタリーブ対象の入力データ列(D000, D001, D002, ..., D383)を記憶

するものであり、書き込み用カウンタ202は、0～383を順にカウントしてそのカウント値をRAM201用の書き込みアドレス(A000, A001, A002, ..., A383)として出力するもので、この書き込みアドレス(A000～A383)に従って入力データ列がRAM201のアドレスA000からアドレスA383まで順に書き込まれるようになっている。

また、読み出し用カウンタ203は、RAM201用の読み出しアドレスを生成するために0～383をカウントするものであり、読み出しアドレス変換回路204は、この読み出し用カウンタ203からのカウント値 x ($=0\sim383$)に対して $x*24 \pmod{383}$ なる演算を施すことにより、読み出し用カウンタ203からのカウント値 x が24おきとなるように変換するもので、これにより、RAM201の読み出しアドレスが、A000, A024, A048, ..., A360, A001, A002, ..., A $n*24 \pmod{383}$, ..., A335, A359, A383といった具合に24おきに指定されるようになっている。

上述のごとく構成されたデインタリーバ200では、図8(B)に示すように、書き込み時には、書き込み用カウンタ202のカウント値がそのまま書き込みアドレスとなり、入力データ列(D000, D001, D002, ..., D383)が順番にRAM201の該当アドレス領域に書き込まれてゆく。一方、読み出し時には、読み出しアドレス生成回路204から24おきに出力される読み出しアドレスで指定されるアドレス領域からデータが順に読み出されてゆく。

この結果、入力データ列(D000, D001, D002, ..., D383)は、D000, D024, D048, ..., D360, D001, D025, ..., D $n*24 \pmod{383}$, ..., D335, D359, D383 というようにデータ並べ替えが行なわれて出力されることになる。つまり、本デインタリーバ200は動作的には、 16×24 サイズのインタリーブを行なっていることになる。即ち例えば図9に示すように、 $16 \times 24 = 384$ 個の入力データ系列を矢印A方向に順番にRAM201に書き込んでゆき、読み出し時には矢印B方向に入力データ系列をRAM201から順番に読み出してゆくようになっているのである。

従って、本デインタリーバ200への入力データ列として、上記のインタリーブ100によって 24×16 インタリーブされた出力データ列(D000, D016, D032, ..., D368, D001, D017, ..., D $n*16 \pmod{383}$, ..., D351, D367, D383)を入力すると、図

8 (C) に示すように、まず、書き込み時には、上記の順序でその出力データ列が順番に RAM 202 に書き込まれてゆき、読み出し時には、24 アドレスおきにデータ列が読み出されてゆくので、結果的に、出力データ列は、インタリーブ前の元のデータ列となる（つまり、デインタリーブされる）。

5 ところで、近年、新しい誤り訂正方式として「ターボ符号化・復号方式」と呼ばれる方式が登場している。この「ターボ符号化・復号方式」を適用した通信システムでは、送信側（ターボ符号器）において、送信情報をインタリーブを介して複数の誤り訂正符号（再帰的組織畳み込み符号がよく用いられる）で符号化し、受信側（ターボ復号器）において、受信情報に対して、インタリーブ、デインタリーブ及び複数の誤り訂正（軟出力）復号器を用いて、インタリーブ、軟出力復号及びデインタリーブを繰り返し施すことによって、通信路で送信情報に付加された誤りを極力小さくして元の送信情報を復元することが行なわれる。

図10は上記の「ターボ符号化・復号方式」を適用した通信システムの要部の構成例を示すブロック図で、この図10に示す通信システムは、送信側にターボ符号器300をそなえ、所望の通信路（無線回線等）500を介した受信側にターボ復号器（ターボ復号装置）400をそなえている。そして、ターボ符号器300は、それぞれ排他的論理和素子（EX-OR）311～313及び遅延素子（フリップフロップ：FF）314、315を有する2組の再帰的組織畳み込み符号器（以下、単に「畳み込み符号器」という）301、302と、送信情報uをインタリーブするインタリーブ（ π ）303とをそなえて構成されており、ターボ復号器400は、軟出力復号器（DEC）401、402、インタリーブ（ π ）403及びデインタリーブ（ π^{-1} ）404をそなえて構成されている。

ここで、ターボ符号器300において、畳み込み符号器301は、送信情報uを畳み込み符号化して得られた符号化情報を誤り訂正符号 y_1 として受信側へ送出するものであり、インタリーブ303は、上記のインタリーブ100と同様の動作原理により、送信情報uをインタリーブするものであり、畳み込み符号器302は、このインタリーブ303でインタリーブされた送信情報 u' を畳み込み符号化して得られた符号化情報を誤り訂正符号 y_2 として受信側へ送出するものである。

つまり、ターボ符号器 300 は、送信情報（被復号情報） u 自身と、インタリーブ前の送信情報 u についての誤り訂正符号 y_1 と、インタリーブ後の送信情報 u についての誤り訂正符号 y_2 とをターボ符号として受信側へ送信するようになっているのである。

5 一方、ターボ復号器 400 において、DEC 401 は、受信ターボ符号〔ただし、送信情報 u ，誤り訂正符号 y_1 ， y_2 は、それぞれ、通信路 500 から雑音（誤り）を受けて受信情報 U ，誤り訂正符号 Y_1 ， Y_2 となっていると仮定する〕のうち、1 番始めは受信情報 U を誤り訂正符号 Y_1 を用いて軟出力復号して受信情報 U' を得、その後は、受信情報 U' をインタリーブ 403 によりインタ
10 リーブした信号を DEC 402 で誤り訂正符号 Y_2 を用いて軟出力復号し、その復号結果（受信情報 U'' ）をデインタリーブ 404 でデインタリーブして得られる信号について誤り訂正符号 Y_1 を用いて再度軟出力復号することを繰り返す行なうものである。なお、この軟出力復号には、例えば、MAP (Maximum A Posteriori probability) 復号や SOVA (Soft-Output Viterbi Algorithm) 復号等が
15 用いられる。

また、インタリーブ 403 も、上記のインタリーブ 100 と同様の動作原理により、この DEC 401 からの復号結果をインタリーブするものであり、このインタリーブにより、DEC 401 からの復号結果のデータ列が DEC 402 での軟出力復号に用いられる誤り訂正符号 Y_2 のデータ列と揃った状態で DEC 40
20 2 に入力されることになる。

さらに、DEC 402 は、インタリーブ後の復号結果を誤り訂正符号 Y_2 を用いてさらに軟出力復号（例えば、MAP 復号や SOVA 復号等）するものであり、デインタリーブ 404 は、上記のデインタリーブ 200 と同様の動作原理により、この DEC 402 からの復号結果をデインタリーブして元のデータ列に戻すもの
25 で、このデインタリーブにより、DEC 402 からの復号結果のデータ列が誤り訂正符号 Y_1 のデータ列と揃った状態で DEC 401 に入力され、DEC 401 において、再度、誤り訂正符号 Y_1 を用いた軟出力復号が行なわれることになる。

つまり、ターボ復号器 400 では、次のような演算を繰り返せば繰り返すほど送信情報 u に付加された誤りが低減され、元の送信情報 u をできる限り忠実に復

元することができるようになっているのである。

1. U と Y_1 とで軟出力復号 $\rightarrow U'$
 2. U' と Y_2 とで軟出力復号 $\rightarrow U''$ (ターボ繰り返し 1 回の出力)
 3. U'' と Y_1 とで軟出力復号 $\rightarrow U'^3$
 - 5 4. U'^3 と Y_2 とで軟出力復号 $\rightarrow U'^4$ (ターボ繰り返し 2 回の出力)
 5. U'^4 と Y_1 とで軟出力復号 $\rightarrow U'^5$
 6. U'^5 と Y_2 とで軟出力復号 $\rightarrow U'^6$ (ターボ繰り返し 3 回の出力)
- (以下、同様)

ただし、繰り返し回数は、飽和回数 (例えば、16 回程度) 以下に設定される。

- 10 このように、ターボ復号器 400 では、DEC 401, 402 とインタリーブ 403 とデインタリーブ 404 とを用いて、軟出力復号、インタリーブ及びデインタリーブを繰り返し行なうことによって、ターボ符号の復号を行なうようになっている。なお、「ターボ符号化・復号方式」の詳細については、例えば、米国特許 No. 5,446,747 等に記載されている。

- 15 ところが、上記のターボ復号器 400 では、インタリーブとデインタリーブとをそれぞれ個別のインタリーブ 403 とデインタリーブ 404 とで行なっているため、その回路規模が非常に大きくなってしまっているという課題がある。

- 特に、実際の通信では、復号結果であるデータ列 (インタリーブもしくはデインタリーブ対象のデータ列) の 1 単位 (例えば、前記の D000~D383 のそれぞれに
- 20 相当する) が十数ビット分になることがあり、このような場合には、インタリーブ (デインタリーブ) ・サイズ (つまり、メモリサイズ) が数千ビット分にもなるので、上記のような課題が顕著になる。

- また、ターボ復号器 400 に限らず、例えば、インタリーブとそれに応じたデ
- インタリーブとを用いて通信を行なう送受信機などでも、現状では、インタリー
- 25 バ 100 とデインタリーブ 200 とを個別にそなえるしかなく、同様に、装置規模が非常に大きくなってしまふ。

本発明は、このような課題に鑑み創案されたもので、1つのメモリ部でインタリーブ及びデインタリーブとしての機能を実現して、装置規模を大幅に削減できるようにした、ターボ復号装置およびインタリーブ・デインタリーブ装置を提供

することを目的とする。

発明の開示

上記の目的を達成するために、本発明のターボ復号装置は、少なくとも、被復
5 号情報と、送信側でのインタリーブ前のその被復号情報についての誤り訂正符号
と、上記の送信側でのインタリーブ後の上記被復号情報についての誤り訂正符号
とを有するターボ符号を、誤り訂正復号とインタリーブとデインタリーブとを繰
り返し施して復号するためのものであって、上記の各誤り訂正符号のいずれか一
方と過去の誤り訂正復号結果とに基づいて被復号情報を誤り訂正復号しうる誤り
10 訂正復号部と、この誤り訂正復号部からの誤り訂正復号結果をインタリーブもし
くはデインタリーブして過去の誤り訂正復号結果として誤り訂正復号部へ出力す
るためのメモリ部と、上記の誤り訂正復号部で用いられる誤り訂正符号に応じて
誤り訂正復号結果をインタリーブもしくはデインタリーブすべく上記メモリ部に
15 対する誤り訂正復号結果の書き込み順及び読み出し順を制御するメモリ制御部と
をそなえて構成されたことを特徴としている。

従って、本発明のターボ復号装置では、誤り訂正復号部で用いられる誤り訂正
符号に応じてメモリ部に対する誤り訂正復号結果の書き込み順及び読み出し順を
制御することで、誤り訂正復号結果をインタリーブもしくはデインタリーブする
ことができるので、インタリーブ及びデインタリーブを個別にそなえる必要がな
20 く、これにより、ターボ復号装置の小型化、低コスト化に大いに寄与する。

ここで、上記のメモリ制御部は、次の各部をそなえていてもよい。

(1) 上記メモリ部用のアドレスを所定の順序で生成する第1のアドレス生成
部

(2) この第1のアドレス生成部のアドレス生成順序とは異なる順序でメモリ
25 部用のアドレスを生成する第2のアドレス生成部

(3) これらの各アドレス生成部の各出力のうちのいずれか一方をメモリ部用
の書き込みアドレス、他方をメモリ部用の読み出しアドレスとして選択出力しう
るアドレス選択部

(4) 上記の誤り訂正復号部で用いられる誤り訂正符号が上記の送信側でのイ

インタリーブ前の被復号情報についてのものかインタリーブ後の被復号情報についてのものかを判別するインタリーブ判別部

(5) このインタリーブ判別部において、上記の誤り訂正符号がインタリーブ前の被復号情報についてのものであると判別されると、一方のアドレス生成部の出力が書き込みアドレス、他方のアドレス生成部の出力が読み出しアドレスとしてそれぞれ選択され、上記の誤り訂正符号がインタリーブ後の被復号情報についてのものであると判別されると、上記他方のアドレス生成部の出力が書き込みアドレス、上記一方のアドレス生成部の出力が読み出しアドレスとしてそれぞれ選択されるようアドレス選択部を制御するアドレス選択制御部

10 これにより、本発明のターボ復号装置では、上記の第1のアドレス生成部及び第2のアドレス生成部の各出力を選択制御するだけで、メモリ部に対する誤り訂正復号結果の書き込み順及び読み出し順をインタリーブ及びデインタリーブに応じた順序に制御することができるので、極めて簡素な構成で、本ターボ復号装置を実現することができる。

15 なお、上記第2のアドレス生成部に、上記第1のアドレス生成部で生成されたアドレスをランダムに並び替えて出力するためのランダムパターン情報を保持するランダムパターン保持部をそなえれば、ランダムパターン情報をインタリーブ用及びデインタリーブ用に2種類用意する必要が無い（上記第1のアドレス生成部をインタリーブ時とデインタリーブ時とで共用できる）ので、ランダムパターン情報を予め演算により求める場合の作業負担が大幅に軽減されるとともに、ターボ復号装置のさらなる小型化、低コスト化に大いに寄与する。

次に、本発明のインタリーブ・デインタリーブ装置は、所望のデータをインタリーブもしくはデインタリーブするためにデータを記憶するメモリ部と、このメモリ部用のアドレスを所定の順序で生成する第1のアドレス生成部と、この第1
25 のアドレス生成部のアドレス生成順序とは異なる順序でメモリ部用のアドレスを生成する第2のアドレス生成部と、上記の各アドレス生成部の各出力のうちのいずれか一方をメモリ部用の書き込みアドレス、他方をメモリ部用の読み出しアドレスとして選択出力しうるアドレス選択部と、上記のデータをインタリーブする場合とデインタリーブする場合とで異なるアドレス生成部の出力が書き込みアド

レス及び読み出しアドレスとして選択されるようアドレス選択部を制御するアドレス選択制御部とをそなえて構成されたことを特徴としている。

従って、本発明のインタリーブ・デインタリーブ装置によれば、上記のデータをインタリーブする場合とデインタリーブする場合とで異なるアドレス生成部の出力（生成順の異なる２種のアドレス）が書き込みアドレス及び読み出しアドレスとして選択されるので、１つのメモリ部でインタリーブとしての機能とデインタリーブとしての機能を実現することができる。この結果、データをインタリーブ、デインタリーブするのにインタリーブ及びデインタリーブを個別にそなえる必要がなく、装置規模、コストの削減に大いに寄与する。

ここで、上記のアドレス選択制御部は、上記のデータをインタリーブする場合には、上記第１のアドレス生成部の出力が書き込みアドレス、上記第２のアドレス生成部の出力が読み出しアドレスとしてそれぞれ選択され、上記のデータをデインタリーブする場合には、上記第２のアドレス生成部の出力が書き込みアドレス、上記第１のアドレス生成部の出力が読み出しアドレスとしてそれぞれ選択されるよう上記のアドレス選択部を制御するように構成されていてもよい。

また、上記のアドレス選択制御部は、逆に、上記のデータをインタリーブする場合には、上記第２のアドレス生成部の出力が書き込みアドレス、上記第１のアドレス生成部の出力が読み出しアドレスとしてそれぞれ選択され、上記のデータをデインタリーブする場合には、上記第１のアドレス生成部の出力が書き込みアドレス、上記第２のアドレス生成部の出力が読み出しアドレスとしてそれぞれ選択されるようアドレス選択部を制御するように構成されていてもよい。

いずれの場合も、上記の各アドレス生成部の出力の選択を切り替えるだけで、インタリーブとしての機能とデインタリーブとしての機能が切り替えられるので、極めて簡素な構成で、本装置を実現することができる。

なお、本インタリーブ・デインタリーブ装置についても、上記第２のアドレス生成部に、上記第１のアドレス生成部で生成されたアドレスをランダムに並び替えて出力するためのランダムパターン情報を保持するランダムパターン保持部をそなえれば、この場合も、ランダムパターン情報をインタリーブ用及びデインタリーブ用に２種類用意する必要が無い（上記第１のアドレス生成部をインタリー

ブ時とデインタリーブ時とで共用できる) ので、ランダムパターン情報を予め演算により求める場合の作業負担が大幅に軽減されるとともに、本装置の小型化、低コスト化に大いに寄与する。

5 図面の簡単な説明

図1は本発明の一実施形態としてのターボ復号器(ターボ復号装置)の構成を示すブロック図である。

図2(A)～図2(H)はいずれも本実施形態のターボ復号器の動作を説明するためのタイムチャートである。

10 図3は本実施形態のターボ復号器に適用されたインタリーブ・デインタリーブ装置に着目した構成を示すブロック図である。

図4(A)は本実施形態にかかるデインタリーブの構成を示すブロック図である。

15 図4(B)及び図4(C)はいずれも図4(A)に示すデインタリーブの動作を説明するためのアドレス出力及び入出力データ例を示す図である。

図5は本実施形態のインタリーブ・デインタリーブ装置の他の構成を示すブロック図である。

図6(A)は従来のインタリーブの構成を示すブロック図である。

20 図6(B)は図6(A)に示すインタリーブの動作を説明するためのアドレス出力及びデータ入出力例を示す図である。

図7は図6(A)に示すインタリーブの動作イメージを説明するための図である。

図8(A)は従来のデインタリーブの構成を示すブロック図である。

25 図8(B)及び図8(C)はいずれも図8(A)に示すデインタリーブの動作を説明するためのアドレス出力及び入出力データ例を示す図である。

図9は図8(A)に示すデインタリーブの動作イメージを説明するための図である。

図10は従来の「ターボ符号化・復号方式」を適用した通信システムの要部の構成例を示すブロック図である。

発明を実施するための最良の形態

以下、図面を参照して本発明の実施の形態を説明する。

図1は本発明の一実施形態としてのターボ復号器（ターボ復号装置）の構成を示すブロック図で、この図1に示すターボ復号器1も、図10により前述したターボ復号器400と同様に、ターボ符号器300で符号化されたターボ符号を復号するもので、本実施形態では、RAM2-1～2-3、RAM切り替えスイッチ3、軟出力復号器（DEC）4、インタリーブ・デインタリーブRAM（ π - π) 5、アドレス生成カウンタ6、アドレス生成部7、書き込みアドレス切り替えスイッチ（SW1）8-1、読み出しアドレス切り替えスイッチ（SW2）8-2、出力切り替えスイッチ9及びスイッチ制御部10をそなえて構成されている。

なお、本実施形態では、「ターボ符号化・復号方式」をCDMA(Code Division Multiple Access)を利用した移動体通信システムに適用し、例えば、ターボ符号器300は、送信側において1次変調（例えば、QPSK等）及びスペクトラム拡散変調前の送信情報uを入力とする位置に設けられ、ターボ復号器1は、受信側においてスペクトラム拡散復調後の受信情報Uを入力とする位置に設けられることを想定する。

ここで、上記のRAM2-1～2-3は、ターボ符号器300から送信されて通信路500（図10参照）で誤りを受けたターボ符号〔受信情報（被復号情報）U、誤り訂正符号 Y_1 、 Y_2 〕を記憶するためのものであり、本実施形態では、アドレス生成カウンタ6のカウント値に従って、これらの受信情報U、誤り訂正符号 Y_1 、 Y_2 の書き込み及び読み出しが制御されるようになっている。

ただし、本実施形態では、説明の便宜上、図6（A）、図6（B）、図7、図8（A）～図8（C）及び図9により前述したのと同様に、受信情報U、誤り訂正符号 Y_1 、 Y_2 及びDEC4での軟出力復号結果の各データ列をそれぞれ16×24=384（D0～D383）個と仮定する。このため、アドレス生成カウンタ6のカウント値は0～383であり、後述するようにターボ復号もこのデータ列単位（周期）で行なわれることになる。

また、本実施形態でも、上記の誤り訂正符号 Y_1 は、ターボ符号器300において送信情報 u をインタリーブ303でインタリーブする前に畳み込み符号化して得られたもの（即ち、ターボ符号器300でのインタリーブ前の送信情報 u についての誤り訂正符号）であり、誤り訂正符号 Y_2 は、ターボ符号器300において送信情報 u をインタリーブ303でインタリーブした後に畳み込み符号化して得られたもの（即ち、ターボ符号器300でのインタリーブ後の送信情報 u についての誤り訂正符号）である。

次に、RAM切り替えスイッチ3は、これらの各RAM2-1～2-3のうちRAM2-2の出力（即ち、誤り訂正符号 Y_1 ）とRAM2-3の出力（即ち、誤り訂正符号 Y_2 ）とを切り替えるためのもので、本実施形態では、スイッチ制御部10によりA側とB側とに交互に切り替えられるようになっている。

さらに、DEC（誤り訂正復号部）4は、図10により前述したDEC401やDEC402と同様のもので、ここでは、RAM切り替えスイッチ3の切り替えにより入力される、各誤り訂正符号 Y_1 、 Y_2 のいずれか一方と過去の軟出力復号結果（誤り訂正復号結果） U' （ただし、1番最初は除く）とに基づいて受信情報 U を軟出力復号（誤り訂正復号：例えば、MAP復号）しうようになっている。つまり、本実施形態のターボ復号器1は、RAM切り替えスイッチ3をそなえることで、従来のターボ復号器400のDEC401、402の共通化を可能にしているのである。

また、インタリーブ・デインタリーブRAM（メモリ部）5は、DEC4からの軟出力復号結果（以下、単に「復号結果」という）をインタリーブもしくはデインタリーブするために記憶するもので、インタリーブもしくはデインタリーブ後の復号結果は上記過去の復号結果 U' としてDEC4へ帰還出力されるようになっている。

さらに、アドレス生成カウンタ（第1のアドレス生成部）6は、0～383のカウンタ値を順にカウントすることにより、そのカウンタ値をインタリーブ・デインタリーブRAM5（以下、単に「RAM5」と表記する）用のアドレス（A000～A383）として生成するものであり、アドレス変換部（第2のアドレス生成部）7は、このアドレス生成カウンタ6のアドレス生成順序とは異なる順序でR

RAM 5用のアドレスを生成するもので、ここでは、例えば、アドレス生成カウンタ 6 でのアドレス生成順 (A000~A383) を 16 おきに変換した (並び替えた) もの (A000, A016, A032, ..., $A_{n \times 16 \pmod{383}}$, ..., A351, A367, A383) を RAM 5 用のアドレスとして出力するようになっている。

- 5 このために、アドレス変換部 7 は、アドレス生成順変換用のインタリーブパターン情報 [具体的には、例えば、アドレス生成カウンタ 6 のカウント値を x としたときに、 $x \times 16 \pmod{383}$ なる演算を実現するような情報 : ランダムパターン情報 (つまりはアドレス変換テーブル)] を保持したインタリーブパターン ROM (アドレス生成パターン保持部) 71 (以下、単に「ROM 71」と表記する) をそなえて構成されている。

- 10 さらに、書き込みアドレス切り替えスイッチ 8-1 は、アドレス生成カウンタ 6 の出力 (アドレス) とアドレス変換部 7 の出力 (アドレス) とを切り替えることにより、各アドレスのいずれか一方を RAM 5 用の書き込みアドレスとして選択するもので、ここでは、図 1 中に示すように、このスイッチ 8-1 が A 側に切り
15 替えられるとアドレス生成カウンタ 6 の出力が書き込みアドレスとして選択され、B 側に切り替えられるとアドレス変換部 7 の出力が書き込みアドレスとして選択されるようになっている。

- 20 一方、読み出しアドレス切り替えスイッチ 8-2 は、アドレス生成カウンタ 6 の出力 (アドレス) とアドレス変換部 7 の出力 (アドレス) とを切り替えることにより、各アドレスのいずれか一方を RAM 5 用の読み出しアドレスとして選択するもので、図 1 中に示すように、このスイッチ 8-2 が A 側に切り替えられるとアドレス変換部 7 の出力が読み出しアドレスとして選択され、B 側に切り替え
25 られるとアドレス生成カウンタ 6 の出力が読み出しアドレスとして選択されるようになっている。

- 25 ただし、これらの各スイッチ 8-1, 8-2 は、本実施形態では、スイッチ制御部 10 により、A 側及び B 側のいずれかに同時に切り替えられるようになっている (スイッチ 8-1 が A 側でスイッチ 8-2 が B 側、もしくはその逆に切り替えられることはない)。つまり、各スイッチ 8-1, 8-2 は、上記のアドレス生成カウンタ 6 及びアドレス変換部 7 の各出力のうちのいずれか一方を RAM 5

用の書き込みアドレス、他方をRAM 5用の読み出しアドレスとして選択出力し
うるアドレス選択部として機能するのである。

さらに、出力切り替えスイッチ9は、ターボ復号完了後に復号結果を出力する
際にON状態となるもので、例えば、DEC 4での繰り返し復号による飽和回数
5 に達すると、スイッチ制御部10によりON状態に制御されるようになっている。

なお、上記の飽和回数は、本実施形態では、DEC 4での復号が2回繰り返し
で図10に示すDEC 401及びDEC 402での復号1回分に相当するので、
例えば、DEC 4にMAP復号を適用すれば16（図10に示す構成での飽和回
数） $\times 2 = 32$ 回程度となる。

10 そして、スイッチ制御部10は、上記の各スイッチ3、8-1、8-2及び9
の切り替えを統括的に制御するもので、本実施形態の要部である各スイッチ3、
8-1、8-2に対しては、次のようなスイッチ制御を行なうようになっている。

（1）スイッチ3をA側に切り替えるとき（即ち、DEC 4での復号に誤り訂
正符号Y₁を用いるとき）、スイッチ8-1、8-2もそれぞれA側に切り替え
15 る。すると、RAM 5、アドレス生成カウンタ6及びアドレス変換部7の接続構
成が、図6（A）に示すインタリーブ100と同様になる。この結果、DEC 4
からの復号結果（D000～D383）は、アドレス生成カウンタ6からの順列アドレス
（A000～A383）に従ってRAM 5に書き込まれた後、アドレス変換部7からの1
6おきのアドレスに従って読み出されて、インタリーブされる。

20 （2）スイッチ3をB側に切り替えるとき（即ち、DEC 4での復号に誤り訂
正符号Y₂を用いるとき）、スイッチ8-1、8-2もそれぞれB側に切り替え
る。すると、RAM 5、アドレス生成カウンタ6及びアドレス変換部7の接続構
成は、図4（A）に示すようになる。これにより、DEC 4からの復号結果は、
アドレス変換部7からの16おきのアドレスに従って書き込まれた後、アドレス
25 生成カウンタ6からの順列アドレス（A000～A383）に従って順に読み出されるこ
とになる。

従って、入力データ列がD000～D383の順であれば、そのデータ列は、図4（
B）に示すような順序で書き込み及び読み出しが行なわれることになるが、図4
（A）に示す構成において、入力データ列を上記のインタリーブ後のデータ列と

すると、図4（C）に示すような順序で書き込み及び読み出しが行なわれることになり、RAM5の出力データ列は上記インタリーブ前の状態に戻る（即ち、デインタリーブされる）。

つまり、本実施形態のターボ復号器1は、スイッチ制御部10によってスイッチ8-1、8-2の切り替えを制御することで、RAM5、アドレス生成カウンタ6及びアドレス変換部7からなる部分をインタリーブとしてもデインタリーブとしても使用できるようになっている（即ち、例えば図3に示すようなインタリーブ・デインタリーブ装置11をそなえている）のである。

そして、スイッチ制御部10は、上記のようなスイッチ制御を行なうために、例えば、スイッチ制御用カウンタ111とカウント値監視部112とをそなえて構成されている。

ここで、スイッチ制御用カウンタ111は、アドレス生成カウンタ6のカウント値に基づいてスイッチ制御用のカウント値をカウントするもので、本実施形態では、DEC4による復号処理遅延を考慮して、例えば、アドレス生成カウンタ6のカウント周期（0～383）を1周期として3周期毎に0から1ずつカウントアップを行なうようになっている。

また、カウント値監視部112は、このカウンタ111のカウント値を監視するもので、ここでは、例えば、そのカウント値の偶数／奇数を判別し、偶数（ただし、0も含む）のときにはスイッチ3、8-1、8-2がそれぞれA側に切り替えられ、奇数のときにはスイッチ3、8-1、8-2がそれぞれB側に切り替えられるようになっている。

なお、このカウント値監視部112は、カウンタ111のカウント値が例えば31になる（つまり、DEC4の繰り返し復号回数が飽和回数である32回に達する）とターボ復号が完了したものと判別して、出力切り替えスイッチ9をON状態に切り替えるようになっている。

以下、上述のごとく構成された本実施形態のターボ復号器1の動作について、図2（A）～図2（H）に示すタイムチャートを参照しながら詳述する。

まず、スイッチ制御部10は、1回目の復号では、受信情報Uを誤り訂正符号Y₁を用いて軟出力復号すべく、RAM切り替えスイッチ3をA側に切り替える

(スイッチ9はOFF状態)。これにより、アドレス生成カウンタ6のカウン
値〔図2(A)参照〕に従ってRAM2-1, 2-2からそれぞれ受信情報U,
誤り訂正符号Y₁が順に読み出されて〔図2(A)及び図2(B)の時点T0～
T1参照〕、DEC4に入力される。

5 DEC4では、入力された誤り訂正符号Y₁に基づいて受信情報Uを軟出力復
号する(時点T1～T2)。一方、このとき、スイッチ制御部10では、カウ
ント値監視部112がカウンタ111のカウンタ値が0(偶数)であることを認識
するので、スイッチ8-1, 8-2はそれぞれA側に切り替えられている〔図2
(H)参照〕。

10 これにより、DEC4の復号結果は、アドレス生成カウンタ6からの順列アド
レスに従ってRAM5に書き込まれた〔図2(F)の時点T2～T3参照〕後、
アドレス変換部7からの16おきのアドレスに従って読み出されて〔図2(G)
の時点T3～T4参照〕、インタリーブされる。

 ここまでの処理で、カウンタ111のカウンタ値が1(奇数)になる〔図2
15 (A)の時点T3参照〕ので、スイッチ制御部10が、スイッチ3, 8-1, 8
-2を今度はそれぞれB側に切り替える。

 すると、DEC4に、インタリーブ後の復号結果(過去の復号結果U')、受
信情報U、誤り訂正符号Y₂が入力され、DEC4は、これらの入力情報に基づ
いて2回目の軟出力復号を行なう(時点T4～T5)。なお、このとき、受信情
20 報Uを再度入力するのは、過去の復号結果U'と受信情報Uとの差分をとり、以
降の復号はその差分と誤り訂正符号Y₁, Y₂とに基づいて行なうためである。従
って、例えば、DEC4に、この受信情報Uを保持しておくメモリがそなえられ
ていれば、毎回、受信情報UをDEC4に入力する必要はない。

 次に、DEC4の復号結果は、RAM5に入力されるが、このとき、スイッチ
25 8-1, 8-2がそれぞれB側に切り替えられている〔図2(H)の時点T5参
照〕ので、アドレス変換部7からの16おきのアドレスに従ってRAM5に書き
込まれた〔図2(F)の時点T5～T6参照〕後、アドレス生成カウンタ6から
の順列アドレスに従って順に読み出されて〔図2(G)の時点T6～T7参照〕、
デインタリーブされる。

以降、同様にして、スイッチ 3, 8-1, 8-2 が交互に切り替えられて、3 回目、4 回目、・・・の復号が繰り返し行なわれてゆき、例えば、カウンタ 11 1 のカウント値が 3 1 になった時点（つまり、3 2 回目の復号が終了した時点）でスイッチ 9 が ON 状態に制御され、復号結果が出力される。

5 つまり、上記のアドレス生成カウンタ 6, アドレス変換部 7, スイッチ 8-1, 8-2 及びスイッチ制御部 10 は、DEC 4 で用いた誤り訂正符号 Y_1 , Y_2 に応じて復号結果をインタリーブもしくはデインタリーブすべく RAM 5 に対する復号結果の書き込み順及び読み出し順を制御するメモリ制御部 12 としての機能を果たしているのである。

10 このために、カウント値監視部 112 は、DEC 4 で用いられた誤り訂正符号がターボ符号器 300 でのインタリーブ前の送信情報 u についてのもの (Y_1) かインタリーブ後の送信情報 u についてのもの (Y_2) かを判別するインタリーブ判別部として機能している。

15 そして、スイッチ制御部 10 は、このカウント値監視部 112 において、DEC 4 で用いられる誤り訂正符号が Y_1 であると判別されると、アドレス生成カウンタ 6 の出力が書き込みアドレス、アドレス変換部 7 の出力が読み出しアドレスとしてそれぞれ選択され、DEC 4 で用いられる誤り訂正符号が Y_2 であると判別されると、アドレス変換部 7 の出力が書き込みアドレス、アドレス生成カウンタ 6 の出力が読み出しアドレスとしてそれぞれ選択されるようスイッチ 8-1, 20 8-2 を制御するアドレス選択制御部として機能している。

25 つまり、このスイッチ制御部 10 は、インタリーブ・デインタリーブ装置 11 (図 3 参照) において、データ (復号結果) をインタリーブする場合とデインタリーブする場合とで異なるアドレス生成部 6, 7 の出力が書き込みアドレス及び読み出しアドレスとして選択されるようスイッチ 8-1, 8-2 を制御するのである。

以上のように本実施形態のターボ復号器 1 によれば、上述のごとくスイッチ制御部 10 が DEC 4 で用いられる誤り訂正符号 Y_1 , Y_2 に応じてスイッチ 8-1, 8-2 の切り替えを制御して、RAM 5 に対する DEC 4 の復号結果の書き込み順及び読み出し順を制御することで、その復号結果をインタリーブもしくはデ

インタリーブすることができるので、従来のようにインタリーブ及びデインタリーブを個別にそなえる必要がない。

従って、従来のおよそ半分の回路規模でターボ復号器 1 を実現でき、ターボ復号器 1 の大幅な小型化、低コスト化が実現されている。特に、本実施形態では、
5 RAM切り替えスイッチ 3 をそなえることで、1 つの DEC 4 で、従来のターボ復号器 400 と同等の動作を実現できているので、その規模、コストがさらに削減されている。

また、本実施形態では、上述のごとくスイッチ制御部 10 が復号結果（データ）をインタリーブする場合とデインタリーブする場合とで異なるアドレス生成部 6、7 の出力（アドレス）が RAM 5 の書き込みアドレス及び読み出しアドレスとして選択されるようスイッチ 8-1、8-2 の切り替えを制御するという極めて簡素な構成で、1 つの RAM 5 によるインタリーブ及びデインタリーブが実現されているので、制御の簡素化、ターボ復号器 1 のさらなる小型化に大いに寄与している。

15 さらに、本実施形態では、アドレス生成カウンタ 6 の出力（アドレス）をランダム（上述した例では 16 おき）に並び替えるためのランダムパターン情報を保持した ROM 7 1 をそなえることで、ランダムパターン情報をインタリーブ用及びデインタリーブ用に 2 種類用意する必要が無い（アドレス生成カウンタ 6 をインタリーブ時とデインタリーブ時とで共用できる）。

20 従って、ランダムパターン情報を予め演算により求める場合の作業負担が大幅に軽減されるとともに、本ターボ復号器 1 のさらなる小型化、低コスト化に大いに寄与している。

特に、実際に「ターボ符号化・復号方式」で用いられるインタリーブ（デインタリーブ）は「ランダムインタリーブ（デインタリーブ）」と呼ばれる複雑なインタリーブ（デインタリーブ）である（上記のように 16 おきといった単純な規則ではない）ため、このようにランダムパターン情報を 1 種類用意するだけでよいことは、非常に有効である。

なお、上述した実施形態では、DEC 4 で用いる各誤り訂正符号 Y_1 、 Y_2 を誤り訂正符号 Y_1 から交互に切り替える（スイッチ 3 を A 側から交互に切り替え

る) になっているが、逆に、誤り訂正符号 Y_2 から交互に切り替える (スイッチ 3 を B 側から交互に切り替える) ようにしても、上記と同様の作用効果が得られることはいうまでもない。

ただし、この場合、スイッチ制御部 10 は、上述した実施形態とは逆に、DE
5 C 4 の復号結果のインタリーブ/デインタリーブをデインタリーブから始めて交互に切り替える必要があるので、スイッチ 8-1, 8-2 をそれぞれ B 側から交互に切り替えることになる。

また、上述した実施形態では、インタリーブ・デインタリーブ装置 11 において、データ (復号結果) 読み出し時 (スイッチ 8-1, 8-2 を A 側に切り替えた時) にアドレス変換部 7 のランダムパターン情報を用いたデータの並び替え
10 (インタリーブ) が行なわれ、データ書き込み時 (スイッチ 8-1, 8-2 を B 側に切り替えた時) に同じランダムパターン情報を用いたデータの並び替え (デインタリーブ) が行なわれているが、逆にすることも可能である。

即ち、例えば図 5 に示すように、上記の $x * 16 \pmod{383}$ に代えて x
15 $* 24 \pmod{383}$ なる演算を実現するようなランダムパターン情報を ROM 71 に保持させておけば、スイッチ 8-1, 8-2 をそれぞれ B 側に切り替えたときに、アドレス変換部 7 で 24 おきに生成されるアドレスに従ってデータが書き込まれ、アドレス生成カウンタ 6 で順列に生成されるアドレスに従ってデータが読み出されるので、図 5 に示すインタリーブ・デインタリーブ装置 11' は
20 書き込み時にデータの並び替えを行なうインタリーブバとして動作する。

逆に、スイッチ 8-1, 8-2 をそれぞれ A 側に切り替えれば、アドレス生成カウンタ 6 で順列に生成されるアドレスに従ってデータが書き込まれ、アドレス生成カウンタ 7 で 24 おきに生成されるアドレスに従ってデータが読み出されるので、インタリーブ・デインタリーブ装置 11' は読み出し時にデータの並び替
25 えを行なうデインタリーブバとして動作する。

従って、ROM 71 に $x * 24 \pmod{383}$ のランダムパターン情報を保持させた場合 (図 5 に示すインタリーブ・デインタリーブ装置 11' をターボ復号器 1 に適用した場合)、スイッチ制御部 10 は、データ (復号結果) をインタリーブする場合 (スイッチ 3 を A 側に切り替えるとき) はアドレス変換部 7 の出

力が書き込みアドレス、アドレス生成カウンタ 6 の出力が読み出しアドレスとしてそれぞれ選択されるようスイッチ 8-1, 8-2 をそれぞれ B 側に切り替え、データをデインタリーブする場合（スイッチ 3 を B 側に切り替えるとき）は、アドレス生成カウンタ 6 の出力が書き込みアドレス、アドレス変換部 7 の出力が読み出しアドレスとしてそれぞれ選択されるようスイッチ 8-1, 8-2 をそれぞれ A 側に切り替え制御することになる。

なお、この場合も、上述した実施形態と同様の作用効果が得られることはいうまでもない。

・その他

10 上述した実施形態では、インタリーブ・デインタリーブ装置 11（もしくは 11'）がターボ復号器 1 に適用されている場合を例にして説明したが、勿論、インタリーブ・デインタリーブ装置 11（11'）は、ターボ復号器 1 に限らず、インタリーブとそれに応じたデインタリーブとの両方を行なう必要がある箇所であれば同様に適用することができ、この場合も、適用箇所の大幅な小型化を図ることが可能である。

また、上述した実施形態では、インタリーブ及びデインタリーブ対象の入力データ列の個数を、便宜上、384 個（D000～D383）とし、インタリーブ及びデインタリーブ時に用いるランダムパターン情報を $x * 16 \pmod{383}$ （もしくは、 $x * 24 \pmod{383}$ ）としたが、本発明はこれに限定されず、勿論、20 上記以外の個数の入力データ列であっても、上記以外のランダムパターン情報であっても、上述した実施形態と同様の作用効果が得られることはいうまでもない。

さらに、図 1 に示したターボ復号器 1 の構成はあくまでも一例であり、少なくとも図 2（A）～図 2（H）のタイムチャートに示す動作を実現できる構成であれば、どのような構成をとってもよい。

25 また、上述した実施形態では、CDMA を利用した移動体通信システムに本発明が適用されることを例にして説明を行なったが、本発明はこれに限定されず、例えば、FDMA (Frequency Division Multiple Access), TDMA (Time Division Multiple Access) 等の他の方式を利用した多重無線通信システムや、その他の所要の通信システムにも同様に適用され、上述した実施形態と同様の作用効

果が得られる。

そして、本発明は上述した実施形態に限定されるものではなく、本発明の趣旨を逸脱しない範囲で種々変形して実施することができる。

5 産業上の利用可能性

以上のように、本発明によれば、1つのメモリ部でインタリーバ及びデインタリーバとしての機能を実現することができるので、移動体通信システム等においてインタリーバとデインタリーバとを個別にそなえる必要がなくなるので、インタリーバ及びデインタリーバを行なう通信機器の大幅な小型化、低コスト化が可

10 能になり、その有用性は極めて高いものと考えられる。

請求の範囲

1. 少なくとも、被復号情報(U)と、送信側(300)でのインタリーブ前の該被復号情報(U)についての誤り訂正符号(Y_1)と、該送信側(300)でのインタリーブ後の該被復号情報(U)についての誤り訂正符号(Y_2)とを有するターボ符号を、誤り訂正復号とインタリーブとデインタリーブとを繰り返し施して復号するターボ復号装置(1)であって、

上記の各誤り訂正符号(Y_1 , Y_2)のいずれか一方と過去の誤り訂正復号結果とに基づいて該被復号情報(U)を誤り訂正復号しうる誤り訂正復号部(4)と、
10 該誤り訂正復号部(4)からの誤り訂正復号結果をインタリーブもしくはデインタリーブして該過去の誤り訂正復号結果として該誤り訂正復号部(4)へ出力するためのメモリ部(5)と、

該誤り訂正復号部(4)で用いられる誤り訂正符号(Y_1 , Y_2)に応じて該誤り訂正復号結果をインタリーブもしくはデインタリーブすべく該メモリ部(4)に
15 対する該誤り訂正復号結果の書き込み順及び読み出し順を制御するメモリ制御部(12)とをそなえて構成されたことを特徴とする、ターボ復号装置。

2. 該メモリ制御部(12)が、

該メモリ部(5)用のアドレスを所定の順序で生成する第1のアドレス生成部
20 (6)と、

該第1のアドレス生成部(6)のアドレス生成順序とは異なる順序で該メモリ部用のアドレスを生成する第2のアドレス生成部(7)と、

上記の各アドレス生成部(6, 7)の各出力のうちのいずれか一方を該メモリ部(5)用の書き込みアドレス、他方を該メモリ部(5)用の読み出しアドレス
25 として選択出力しうるアドレス選択部(8-1, 8-2)と、

該誤り訂正復号部(4)で用いられる誤り訂正符号が送信側でのインタリーブ前の被復号情報(U)についてのものかインタリーブ後の被復号情報(U)についてのものかを判別するインタリーブ判別部(112)と、

該インタリーブ判別部(112)において、該誤り訂正符号がインタリーブ前

- の被復号情報についてのものであると判別されると、一方のアドレス生成部（６又は７）の出力が該書き込みアドレス、他方のアドレス生成部（７又は６）の出力が該読み出しアドレスとしてそれぞれ選択され、該誤り訂正符号がインタリーブ後の被復号情報についてのものであると判別されると、上記他方のアドレス生成部（７又は６）の出力が該書き込みアドレス、上記一方のアドレス生成部（６又は７）の出力が該読み出しアドレスとしてそれぞれ選択されるよう該アドレス選択部を制御するアドレス選択制御部（１０）とをそなえていることを特徴とする、請求の範囲第１項記載のターボ復号装置。
- 10 3. 該第２のアドレス生成部（７）が、
該第１のアドレス生成部（６）で生成されたアドレスをランダムに並び替えて出力するためのランダムパターン情報を保持するランダムパターン保持部（７１）をそなえていることを特徴とする、請求の範囲第１項記載のターボ復号装置。
- 15 4. 所望のデータをインタリーブもしくはデインタリーブするために該データを記憶するメモリ部（５）と、
該メモリ部（５）用のアドレスを所定の順序で生成する第１のアドレス生成部（６）と、
該第１のアドレス生成部（６）のアドレス生成順序とは異なる順序で該メモリ
20 部（５）用のアドレスを生成する第２のアドレス生成部（７）と、
上記の各アドレス生成部（６，７）の各出力のうちのいずれか一方を該メモリ部（５）用の書き込みアドレス、他方を該メモリ部（５）用の読み出しアドレスとして選択出力するアドレス選択部（８－１，８－２）と、
該データをインタリーブする場合とデインタリーブする場合とで異なるアドレ
25 ス生成部（６，７）の出力が該書き込みアドレス及び該読み出しアドレスとして選択されるよう該アドレス選択部（８－１，８－２）を制御するアドレス選択制御部（１０）とをそなえて構成されたことを特徴とする、インタリーブ・デインタリーブ装置。

5. 該アドレス選択制御部（10）が、

該データをインタリーブする場合は、該第1のアドレス生成部（6）の出力が該書き込みアドレス、該第2のアドレス生成部（7）の出力が該読み出しアドレスとしてそれぞれ選択され、該データをデインタリーブする場合は、該第2のアドレス生成部（7）の出力が該書き込みアドレス、該第1のアドレス生成部（6）の出力が該読み出しアドレスとしてそれぞれ選択されるよう該アドレス選択部（8-1, 8-2）を制御するように構成されたことを特徴とする、請求の範囲第4項記載のインタリーブ・デインタリーブ装置。

10 6. 該アドレス選択制御部（10）が、

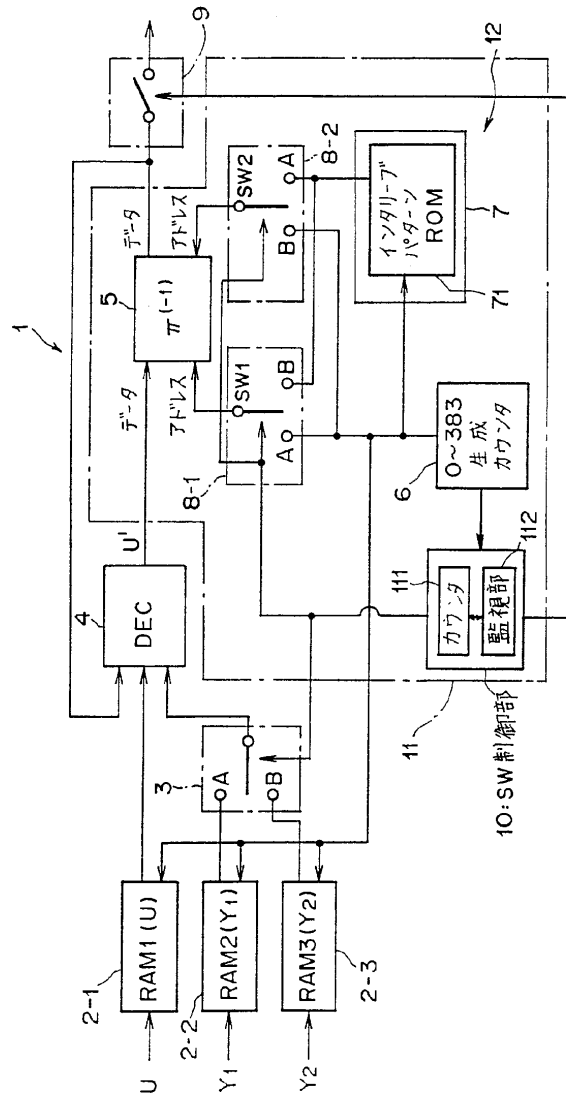
該データをインタリーブする場合は、該第2のアドレス生成部（7）の出力が該書き込みアドレス、該第1のアドレス生成部（6）の出力が該読み出しアドレスとしてそれぞれ選択され、該データをデインタリーブする場合は、該第1のアドレス生成部（6）の出力が該書き込みアドレス、該第2のアドレス生成部（7）の出力が該読み出しアドレスとしてそれぞれ選択されるよう該アドレス選択部（8-1, 8-2）を制御するように構成されたことを特徴とする、請求の範囲第4項記載のインタリーブ・デインタリーブ装置。

7. 該第2のアドレス生成部（7）が、

20 該第1のアドレス生成部（6）で生成されたアドレスをランダムに並び替えて出力するためのランダムパターン情報を保持するランダムパターン保持部（71）をそなえていることを特徴とする、請求の範囲第4項記載のインタリーブ・デインタリーブ装置。

25

図 1



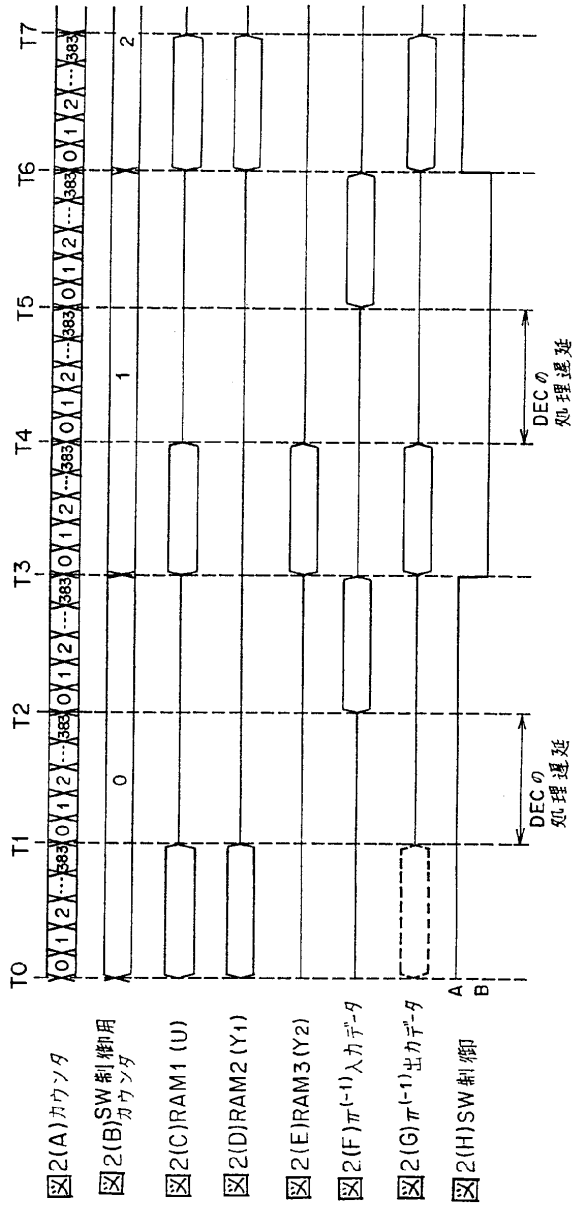
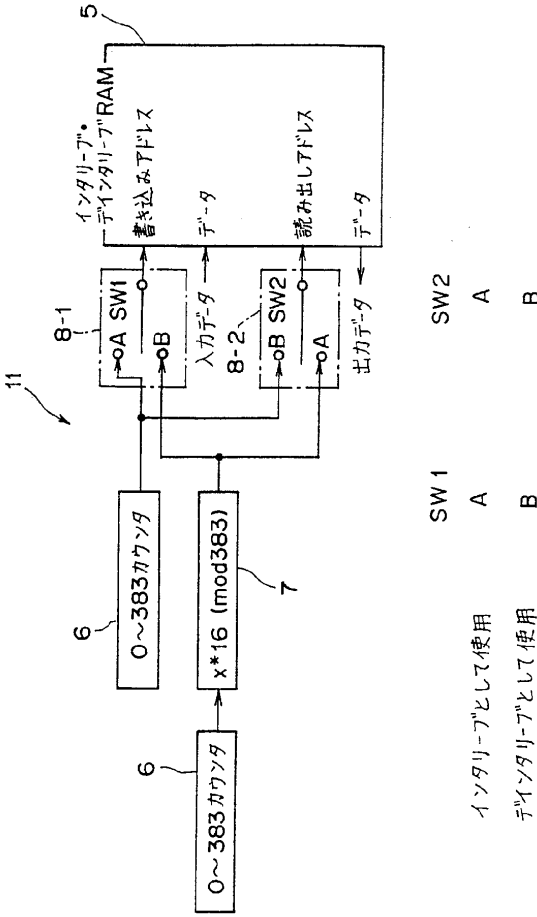


図 3



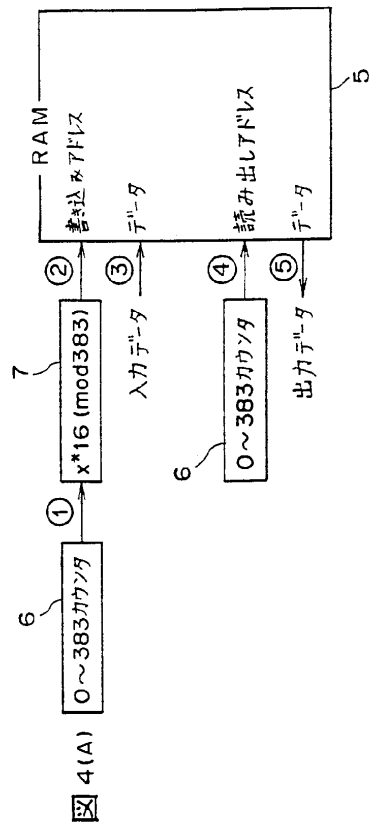


図 4(B)

①	000	001	002	...	023	024	025	...	n	...	381	382	383
②	A000	A016	A032	...	A368	A001	A017	...	$A_n*16 \pmod{383}$	...	A351	A367	A383
③	D000	D001	D002	...	D023	D024	D025	...	Dn	...	D381	D382	D383
④	A000	A001	A002	...	A015	A016	A017	...	An	...	A381	A382	A383
⑤	D000	D024	D048	...	D360	D001	D025	...	$D_n*24 \pmod{383}$	...	D335	D359	D383

書き込み
読み出し

図 4(C)

インターリーブ後のデータを入力すると

①	000	001	002	...	023	024	025	...	n	...	381	382	383
②	A000	A016	A032	...	A368	A001	A017	...	$A_n*16 \pmod{383}$	...	A351	A367	A383
③	D000	D016	D032	...	D368	D001	D017	...	$D_n*16 \pmod{383}$	...	D351	D367	D383
④	A000	A001	A002	...	A015	A016	A017	...	An	...	A381	A382	A383
⑤	D000	D001	D002	...	D015	D016	D017	...	Dn	...	D381	D382	D383

書き込み
読み出し

図 5

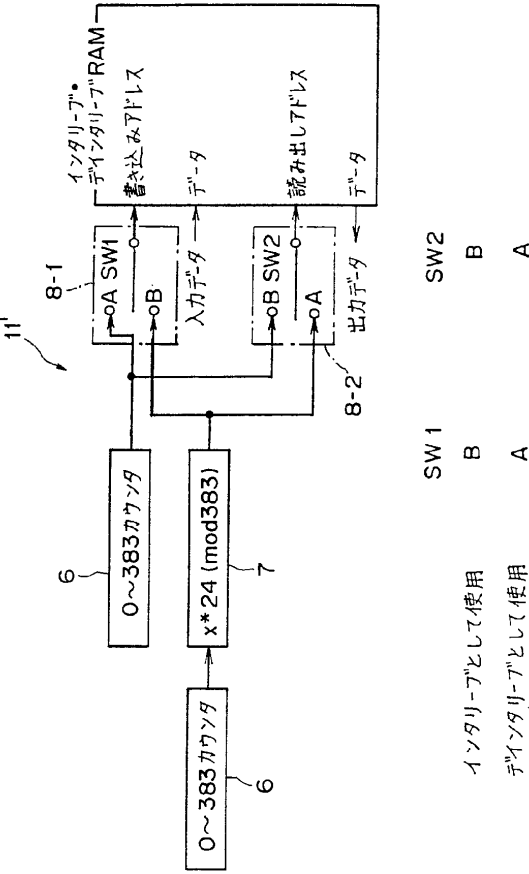


図 6(A)

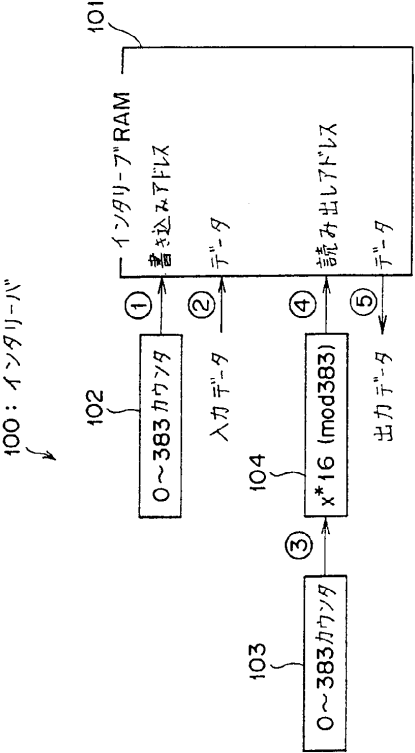
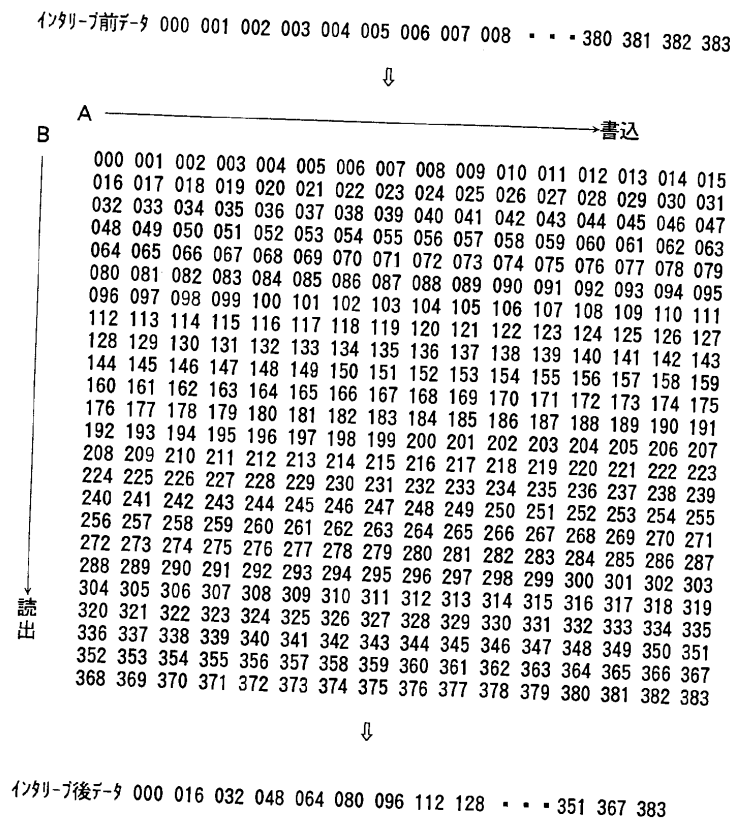


図 6(B)

①	A000	A001	A002	A003	A004	A005	A006	A007	...	An	...	A380	A381	A382	A383
②	D000	D001	D002	D003	D004	D005	D006	D007	...	Dn	...	D380	D381	D382	D383
③	000	001	002	...	023	024	025	...	n	...	...	381	382	383	
④	A000	A016	A032	...	A368	A001	A017	...	An*16(mod 383)	...	...	A351	A367	A383	
⑤	D000	D016	D032	...	D368	D001	D017	...	Dn*16(mod 383)	...	...	D351	D367	D383	

図 7



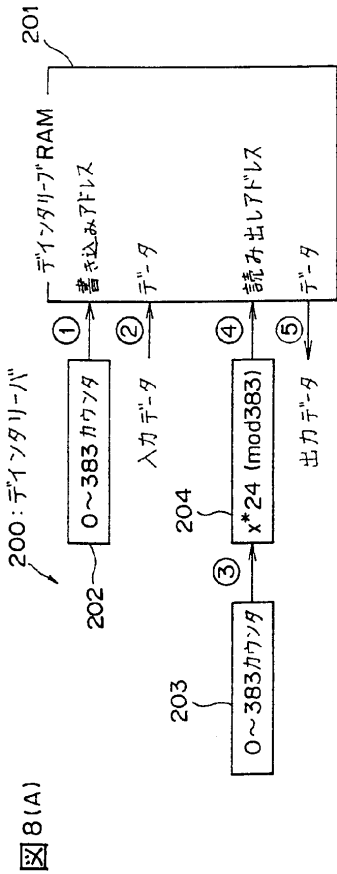


図 8(B)

①	A000	A001	A002	A003	A004	A005	A006	A007	...	An	...	A380	A381	A382	A383
②	D000	D001	D002	D003	D004	D005	D006	D007	...	Dn	...	D380	D381	D382	D383
③	000	001	002	...	015	016	017	...	n	...	...	381	382	383	
④	A000	A024	A048	...	A360	A001	A025	$An \cdot 24 \pmod{383}$	...	A335	A359	A383			
⑤	D000	D024	D048	...	D360	D001	D025	$Dn \cdot 24 \pmod{383}$	...	D335	D359	D383			

インタリ-バ 100 で⁰ インタリ-ブされたデータを入力すると

書込

①	A000	A001	A002	...	A023	A024	A025	...	An	...	A381	A382	A383
②	D000	D016	D032	...	D368	D001	D017	...	$Dn \cdot 16 \pmod{383}$	...	D351	D367	D383
読出													
③	000	001	002	...	015	016	017	...	n	...	381	382	383
④	A000	A024	A048	...	A360	A001	A025	...	$An \cdot 24 \pmod{383}$	...	A335	A359	A383
⑤	D000	D001	D002	...	D015	D016	D017	...	Dn	...	D381	D382	D383

図 8(C)

図 9

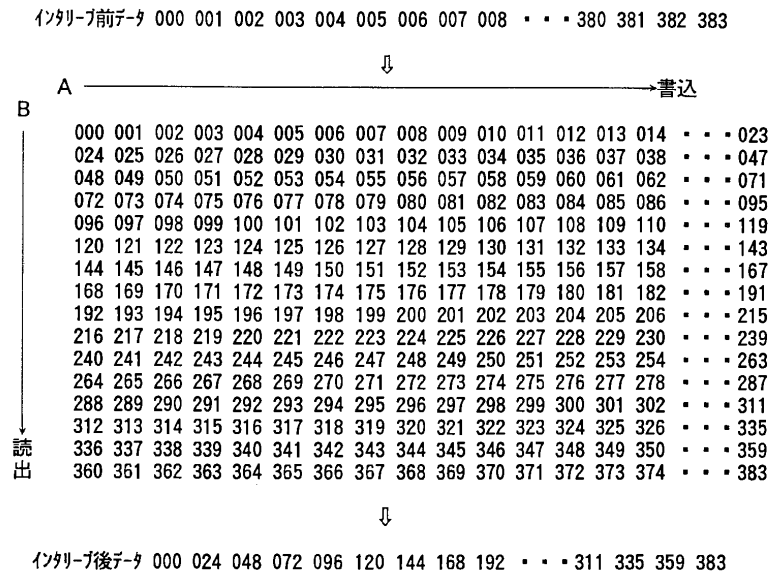
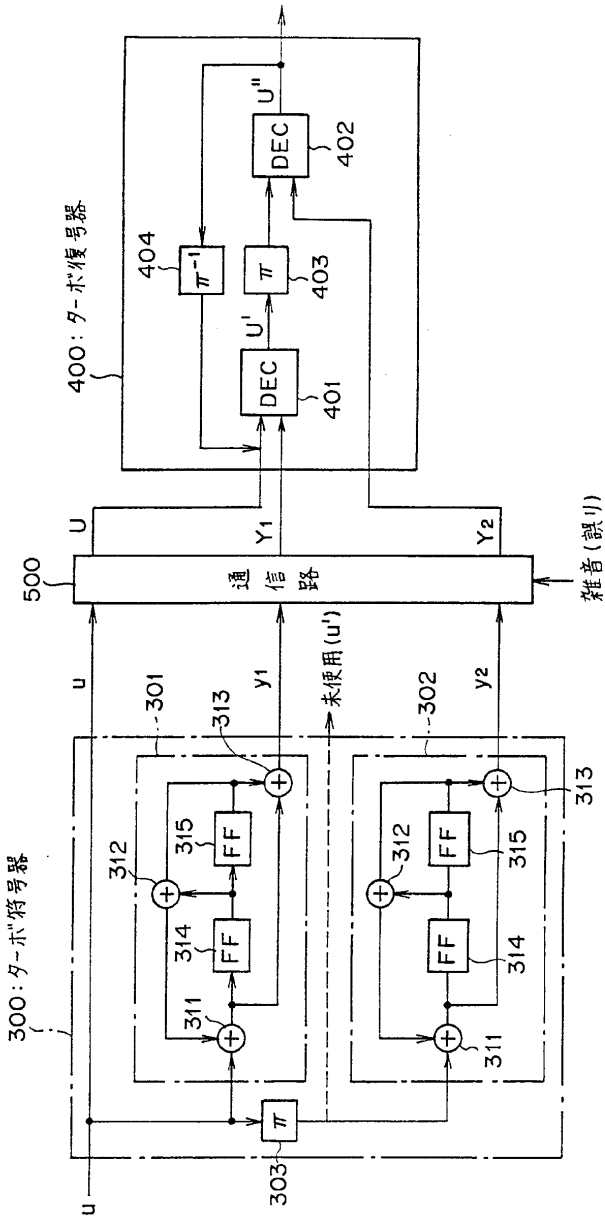


図 10



INTERNATIONAL SEARCH REPORT

International application No.

PCT/JP99/00934

A. CLASSIFICATION OF SUBJECT MATTER
Int.Cl.⁶ H03M13/22, H03M13/12

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
Int.Cl.⁶ H03M13/00-13/22

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched
Jitsuyo Shinan Koho 1926-1996 Toroku Jitsuyo Shinan Koho 1994-1998
Kokai Jitsuyo Shinan Koho 1971-1998 Jitsuyo Shinan Toroku Koho 1996-1998

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
Y	US, 5737252, A (U.S. Phillips), April 7, 1998 (07. 04. 98), Column 5, lines 24 to 26, 32 to 36 ; column 6, lines 10 to 13 ; column 8, lines 26 to 31 & JP, 09-511606, A	1-7
Y	JP, 07-254862, A (Sony Corp.), 3 October, 1995 (03. 10. 95), Par. Nos. [0078], [0079] (Family: none)	1-7
A	US, 5446747, A (France Telecom), August 29, 1995 (29. 08. 95), Fig. 1 & EP, 511141, A1 & FR, 2675971, A1 & DE, 69215743, E	1-3

☒ Further documents are listed in the continuation of Box C. ☐ See patent family annex.

* Special categories of cited documents: "A" document defining the general state of the art which is not considered to be of particular relevance "E" earlier document but published on or after the international filing date "L" document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified) "O" document referring to an oral disclosure, use, exhibition or other means "P" document published prior to the international filing date but later than the priority date claimed	"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention "X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone "Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art "&" document member of the same patent family

Date of the actual completion of the international search
13 May, 1999 (13. 05. 99)

Date of mailing of the international search report
1 June, 1999 (01. 06. 99)

Name and mailing address of the ISA/
Japanese Patent Office

Authorized officer

Facsimile No.

Telephone No.

Form PCT/ISA/210 (second sheet) (July 1992)

INTERNATIONAL SEARCH REPORT

International application No.

PCT/JP99/00934

C (Continuation). DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
A	Small World Communications, "Iterative decoding of parallel concatenated convolutional codes", Version 1.4, 13 Jan. 1999, Australia, pp.1-12, Figure 3, Figure 8 ; page 4, right column, 3rd to 1st line from the bottom ; page 5, right column, lines 29 to 31 ; page 8, right column, line 14 to page 9, right column, line 18	1-7

Form PCT/ISA/210 (continuation of second sheet) (July 1992)

国際調査報告		国際出願番号 PCT/J P 99/00934
A. 発明の属する分野の分類 (国際特許分類 (IPC))		
Int. Cl ⁶ H03M13/22, H03M13/12		
B. 調査を行った分野		
調査を行った最小限資料 (国際特許分類 (IPC))		
Int. Cl ⁶ H03M13/00-13/22		
最小限資料以外の資料で調査を行った分野に含まれるもの 日本国実用新案公報 1926-1996年 日本国公開実用新案公報 1971-1998年 日本国登録実用新案公報 1994-1998年 日本国実用新案登録公報 1996-1998年		
国際調査で使用した電子データベース (データベースの名称、調査に使用した用語)		
C. 関連すると認められる文献		
引用文献の カテゴリー*	引用文献名 及び一部の箇所が関連するときは、その関連する箇所の表示	関連する 請求の範囲の番号
Y	US, 5737252, A (U. S. Phillips) Apr. 7, 1998 (07. 04. 98) 第5欄第24~26行, 第5欄第32~36行, 第6欄第10~13行, 第8欄第26~31行。 & JP, 09-511606, A	1-7
Y	JP, 07-254862, A (ソニー株式会社) 3. 10月. 1995 (03. 10. 95) 段落【0078】 - 【0079】 (ファミリーなし)	1-7
A	US, 5446747, A (France Telecom) Aug. 29, 1995 (29. 08. 95) 第1図。 & EP, 511141, A1 & FR, 2675971, A1 & DE, 69215743, E	1-3
☒ C欄の続きにも文献が列挙されている。 ☐ パテントファミリーに関する別紙を参照。		
* 引用文献のカテゴリー 「A」 特に関連のある文献ではなく、一般的技術水準を示すもの 「E」 国際出願日前の出願または特許であるが、国際出願日以後に公表されたもの 「L」 優先権主張に疑義を提起する文献又は他の文献の発行日若しくは他の特別な理由を確立するために引用する文献 (理由を付す) 「O」 口頭による開示、使用、展示等に言及する文献 「P」 国際出願日前で、かつ優先権の主張の基礎となる出願日の後に公表された文献 「T」 国際出願日又は優先日後に公表された文献であって出願と矛盾するものではなく、発明の原理又は理論の理解のために引用するもの 「X」 特に関連のある文献であって、当該文献のみで発明の新規性又は進歩性がないと考えられるもの 「Y」 特に関連のある文献であって、当該文献と他の1以上の文献との、当業者にとって自明である組合せによって進歩性がないと考えられるもの 「&」 同一パテントファミリー文献		
国際調査を完了した日 13. 05. 99	国際調査報告の発送日 01.06.99	
国際調査機関の名称及びあて先 日本国特許庁 (ISA/J P) 郵便番号 100-8915 東京都千代田区霞が関三丁目4番3号	特許庁審査官 (権限のある職員) 稲葉 和生 印 電話番号 03-3581-1101 内線 3595	

様式 PCT/ISA/210 (第2ページ) (1998年7月)

C (続き) . 関連すると認められる文献		
引用文献の カテゴリー*	引用文献名 及び一部の箇所が関連するときは、その関連する箇所の表示	関連する 請求の範囲の番号
A	Small World Communications, "Iterative decoding of parallel concatenated convolutional codes ", Version 1.4, 13 Jan. 1999, Australia, pp. 1-12, Figure 3, Figure 8, 第4頁右欄下から第3～1行, 第5頁右欄第29-31行, 第8頁右欄第14-第9頁右欄第18行。	1-7

様式PCT/ISA/210 (第2ページの続き) (1998年7月)

Electronic Acknowledgement Receipt	
EFS ID:	12196285
Application Number:	12901699
International Application Number:	
Confirmation Number:	1676
Title of Invention:	RESOURCE SHARING IN A TELECOMMUNICATIONS ENVIRONMENT
First Named Inventor/Applicant Name:	Marcos C. Tzannes
Customer Number:	62574
Filer:	Jason Vick/Joanne Vos
Filer Authorized By:	Jason Vick
Attorney Docket Number:	5550-54-CON-3
Receipt Date:	29-FEB-2012
Filing Date:	11-OCT-2010
Time Stamp:	19:02:14
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	no

File Listing:

Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1		IDS_08.pdf	412229 95975a10490fe3a56eac9e4e78d3513918a8bbe6	yes	5

	Multipart Description/PDF files in .zip description				
	Document Description		Start	End	
	Transmittal Letter		1	3	
	Information Disclosure Statement (IDS) Form (SB08)		4	5	
Warnings:					
Information:					
2	Foreign Reference	JP2003224615.pdf	3636306	no	123
			7e78fb8675084ebfbcb34091e6feafad0a4848bf		
Warnings:					
Information:					
3	Foreign Reference	JP2005522963.pdf	1172060	no	29
			263e8cd1c7ce7b39bd1aa8bb3ec066e4d75fca		
Warnings:					
Information:					
4	Foreign Reference	WO03090011.pdf	1840337	no	47
			e43f3626e7561a14e40892f5c58f0471dc8a12		
Warnings:					
Information:					
5	Foreign Reference	EP1041756.pdf	1405051	no	22
			71137eb7fe64961d64fd1bf6c7e545193f001e9		
Warnings:					
Information:					
6	Non Patent Literature	5550-54-PJP-DIV_OA_2011-12-12.pdf	82852	no	4
			7e0a2b3704b5049e9135153b0b40b5f5102203fb		
Warnings:					
Information:					
7	Foreign Reference	JP7_254862.pdf	347817	no	24
			c4cfa8bf5e4641c9153685dc3769e38692231d5		
Warnings:					
Information:					
8	Foreign Reference	WO0052834.pdf	1619380	no	40
			25b6e57b041e6bb478a259d56aeb6cb712b3279		
Warnings:					
Information:					
Total Files Size (in bytes):			10516032		

This Acknowledgement Receipt evidences receipt on the noted date by the USPTO of the indicated documents, characterized by the applicant, and including page counts, where applicable. It serves as evidence of receipt similar to a Post Card, as described in MPEP 503.

New Applications Under 35 U.S.C. 111

If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application.

National Stage of an International Application under 35 U.S.C. 371

If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.

New International Application Filed with the USPTO as a Receiving Office

If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In Re the Application of:	)	Group Art Unit: 2117
TZANNES, Marcos C.	)	Confirmation No.: 1676
Serial No.: 12/901,699	)	Examiner: Tabone Jr, John J.
Filed: October 11, 2010	)	
Atty. File No.: 5550-54-CON-3	)	<u>SUPPLEMENTAL</u>
Entitled: "RESOURCE SHARING IN A	)	<u>INFORMATION DISCLOSURE</u>
TELECOMMUNICATIONS ENVIRONMENT"	)	<u>STATEMENT</u>
	)	Electronically Submitted

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Dear Sir:

The references cited on attached Form PTO-1449 are being called to the attention of the Examiner.

- ☒ Copies of the cited non-patent and/or foreign references are enclosed herewith.
- ☐ Copies of the cited U.S. patents and/or patent applications are enclosed herewith.
- ☒ Copies of the cited U.S. patents/patent application publications are not enclosed in accordance with 37 C.F.R. § 1.98(a).
- ☐ Copies of the cited references are not enclosed, in accordance with 37 C.F.R. § 1.98(d), because the references were cited by or submitted to the U.S. Patent and Trademark Office in prior application Serial No. _____ filed _____, which is relied upon for an earlier filing date under 35 U.S.C. § 120.
- ☒ To the best of applicants' belief, the pertinence of the foreign-language references are believed to be summarized in the attached English translations and/or in the figures, although applicants do not necessarily vouch for the accuracy of the translation.
- ☐ Examiner's attention is drawn to the following related applications:
- Serial No. _____ filed _____ (Attorney Ref. No. _____)
- Serial No. _____ filed _____ (Attorney Ref. No. _____)
- ☐ Other: _____

Submission of the above information is not intended as an admission that any item is citable under the statutes or rules to support a rejection, that any item disclosed represents analogous art, or that those skilled in the art would refer to or recognize the pertinence of any reference without the benefit of hindsight, nor should an inference be

drawn as to the pertinence of the references based on the order in which they are presented. Submission of this statement should not be taken as an indication that a search has been conducted, or that no better art exists.

It is respectfully requested that the cited information be expressly considered during the prosecution of this application and the references made of record therein.

FEES

☐	37 CFR 1.97(b): No fee is believed due in connection with this submission, because the information disclosure statement submitted herewith is satisfied by one of the following conditions ("X" indicates satisfaction): ☐ Within three months of the filing date of a national application other than a continued prosecution application under 37 CFR 1.53(d), or ☐ Within three months of the date of entry of the national stage as set forth in § 1.491 in an international application, or ☐ Before the mailing date of a first Office Action on the merits, or ☐ Before the mailing of a first Office action after the filing of a request for continued examination under 37 CFR 1.114. Although no fee is believed due, if any fee is deemed due in connection with this submission, please charge such fee to Deposit Account 19-1970.
☒	37 CFR 1.97(c): The information disclosure statement transmitted herewith is being filed after all the above conditions (37 CFR 1.97(b)), but before the mailing date of any one of the following conditions: (1) a final action under 37 C.F.R. 1.113, or (2) a notice of allowance under 37 C.F.R. 1.311, or (3) an action that otherwise closes prosecution in the application. This Information Disclosure Statement is accompanied by: ☒ A Certification (below) as specified by 37 C.F.R. 1.97(e). Although no fee is believed due, if any fee is deemed due in connection with this submission, please charge such fee to Deposit Account 19-1970. OR ☐ Please charge Deposit Account 19-1970 in the amount of \$180.00 for the fee set forth in 37 C.F.R. 1.17(p) for submission of an information disclosure statement. Please credit any overpayment or charge any underpayment to Deposit Account 19-1970.
☐	37 CFR 1.97(d): This Information Disclosure Statement is being submitted after the period specified in 37 CFR 1.97(c). ☐ This information Disclosure Statement includes a Certification (below) as specified by 37 C.F.R. 1.97(e) AND ☐ Applicants hereby requests consideration of the reference(s) disclosed herein. Please charge Deposit Account 19-1970 in the amount of \$180.00 under 37 C.F.R. 1.17(p). Please credit any overpayment or charge any underpayment to Deposit Account 19-1970. Election to pay the fee should not be taken as an indication that applicant(s) cannot execute a certification.

Certification (37 C.F.R. 1.97(e))
(Applicable only if checked)



The undersigned certifies that:

☒ Each item of information contained in this information disclosure statement was first cited in any communication from a foreign patent office in a counterpart foreign application not more than three months prior to the filing of this statement. 37 C.F.R. 1.97(e)(1).

☒ A copy of the communication from the foreign patent office is enclosed.

OR

☐ No item of information contained in this information disclosure statement was cited in a communication from a foreign patent office in a counterpart foreign application, and, to the knowledge of the undersigned after making reasonable inquiry, no item of information contained in this Information Disclosure Statement was known to any individual designated in 37 C.F.R. 1.56(c) more than three months prior to the filing of this statement. 37 C.F.R. 1.97(e)(2).

Respectfully submitted,

SHERIDAN ROSS P.C.

By: _____

Jason H. Vick
Registration No. 45,285
1560 Broadway, Suite 1200
Denver, Colorado 80202-5141
(303) 863-9700

Date: 29 Feb '12

Substitute for form 1449A/PTO				Complete if Known	
INFORMATION DISCLOSURE STATEMENT BY APPLICANT				Application Number	12/901,699
				Filing Date	October 11, 2010
				First Named Inventor	Marcos C. Tzannes
				Art Unit	2117
				Examiner Name	Tabone Jr, John J.
Sheet	1	of	1	Attorney Docket Number	5550-54-CON-3

U.S. PATENT DOCUMENTS					
Examiner Initials*	Cite No. ¹	Document Number Number-kind Code ² (if known)	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear

FOREIGN PATENT DOCUMENTS						
Examiner Initials*	Cite No. ¹	Foreign Patent Document Country Code ³ ; Number ⁴ ; Kind Code ⁵ (if known)	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear	T ⁶

OTHER ART (Including Author, Title, Date, Pertinent Pages, etc.)		
Examiner Initials*	Cite No. ¹	
	1	Official Action for U.S. Patent Application No. 12/295,828, mailed Jan. 5, 2012 (Attorney Ref. No. 5550-57-PUS)

Examiner Signature		Date Considered	

*EXAMINER: Initial if reference is considered, whether or not citation is in conformance and not considered. Include copy of this form with next communication to applicant.

Electronic Acknowledgement Receipt	
EFS ID:	11866536
Application Number:	12901699
International Application Number:	
Confirmation Number:	1676
Title of Invention:	RESOURCE SHARING IN A TELECOMMUNICATIONS ENVIRONMENT
First Named Inventor/Applicant Name:	Marcos C. Tzannes
Customer Number:	62574
Filer:	Jason Vick/Amy Duarte
Filer Authorized By:	Jason Vick
Attorney Docket Number:	5550-54-CON-3
Receipt Date:	18-JAN-2012
Filing Date:	11-OCT-2010
Time Stamp:	17:21:57
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	no

File Listing:

Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1		IDS_06.pdf	335533 f46002ca7b8c180e9308b4b22fcca8e7dba b5b0	yes	4

	Multipart Description/PDF files in .zip description				
	Document Description		Start	End	
	Transmittal Letter		1	3	
	Information Disclosure Statement (IDS) Form (SB08)		4	4	
Warnings:					
Information:					
2	Foreign Reference	GB2389493A.pdf	970749	no	28
			17b7179bab10ac0e84488cbf906bae564ca4718		
Warnings:					
Information:					
3	Non Patent Literature	5550-57-PEP-DIV-2_OA_2011-12-22.pdf	95779	no	4
			b7a638eb4f8f3af97bbcdf9b81dadfb58be29cb5f		
Warnings:					
Information:					
4		IDS_07.pdf	329530	yes	4
			26db912057d6038b249d6332b8d7ea8b3b54cc4a		
	Multipart Description/PDF files in .zip description				
	Document Description		Start	End	
	Transmittal Letter		1	3	
	Information Disclosure Statement (IDS) Form (SB08)		4	4	
Warnings:					
Information:					
5	Non Patent Literature	5550-57-PUS_OA_2012-01-05.pdf	504513	no	14
			0f0b5ee21f015d8258d58f7f50aa47e1528cf a8c		
Warnings:					
Information:					
Total Files Size (in bytes):			2236104		

This Acknowledgement Receipt evidences receipt on the noted date by the USPTO of the indicated documents, characterized by the applicant, and including page counts, where applicable. It serves as evidence of receipt similar to a Post Card, as described in MPEP 503.

New Applications Under 35 U.S.C. 111

If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application.

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If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.

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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In Re the Application of:	)	Group Art Unit: 2117
TZANNES, Marcos C.	)	Confirmation No.: 1676
Serial No.: 12/901,699	)	Examiner: Tabone Jr, John J.
Filed: October 11, 2010	)	
Atty. File No.: 5550-54-CON-3	)	<u>SUPPLEMENTAL</u>
Entitled: "RESOURCE SHARING IN A	)	<u>INFORMATION DISCLOSURE</u>
TELECOMMUNICATIONS ENVIRONMENT"	)	<u>STATEMENT</u>
	)	Electronically Submitted

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Dear Sir:

The references cited on attached Form PTO-1449 are being called to the attention of the Examiner.

- ☒ Copies of the cited non-patent and/or foreign references are enclosed herewith.
- ☐ Copies of the cited U.S. patents and/or patent applications are enclosed herewith.
- ☐ Copies of the cited U.S. patents/patent application publications are not enclosed in accordance with 37 C.F.R. § 1.98(a).
- ☐ Copies of the cited references are not enclosed, in accordance with 37 C.F.R. § 1.98(d), because the references were cited by or submitted to the U.S. Patent and Trademark Office in prior application Serial No. _____ filed _____, which is relied upon for an earlier filing date under 35 U.S.C. § 120.
- ☐ To the best of applicants' belief, the pertinence of the foreign-language references are believed to be summarized in the attached English translations and/or in the figures, although applicants do not necessarily vouch for the accuracy of the translation.
- ☐ Examiner's attention is drawn to the following related applications:
- Serial No. _____ filed _____ (Attorney Ref. No. _____)
- Serial No. _____ filed _____ (Attorney Ref. No. _____)
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It is respectfully requested that the cited information be expressly considered during the prosecution of this application and the references made of record therein.

FEES

☐	37 CFR 1.97(b): No fee is believed due in connection with this submission, because the information disclosure statement submitted herewith is satisfied by one of the following conditions ("X" indicates satisfaction): ☐ Within three months of the filing date of a national application other than a continued prosecution application under 37 CFR 1.53(d), or ☐ Within three months of the date of entry of the national stage as set forth in § 1.491 in an international application, or ☐ Before the mailing date of a first Office Action on the merits, or ☐ Before the mailing of a first Office action after the filing of a request for continued examination under 37 CFR 1.114. Although no fee is believed due, if any fee is deemed due in connection with this submission, please charge such fee to Deposit Account 19-1970.
☒	37 CFR 1.97(c): The information disclosure statement transmitted herewith is being filed after all the above conditions (37 CFR 1.97(b)), but before the mailing date of any one of the following conditions: (1) a final action under 37 C.F.R. 1.113, or (2) a notice of allowance under 37 C.F.R. 1.311, or (3) an action that otherwise closes prosecution in the application. This Information Disclosure Statement is accompanied by: ☒ A Certification (below) as specified by 37 C.F.R. 1.97(e). Although no fee is believed due, if any fee is deemed due in connection with this submission, please charge such fee to Deposit Account 19-1970. OR ☐ Please charge Deposit Account 19-1970 in the amount of \$180.00 for the fee set forth in 37 C.F.R. 1.17(p) for submission of an information disclosure statement. Please credit any overpayment or charge any underpayment to Deposit Account 19-1970.
☐	37 CFR 1.97(d): This Information Disclosure Statement is being submitted after the period specified in 37 CFR 1.97(c). ☐ This information Disclosure Statement includes a Certification (below) as specified by 37 C.F.R. 1.97(e) AND ☐ Applicants hereby requests consideration of the reference(s) disclosed herein. Please charge Deposit Account 19-1970 in the amount of \$180.00 under 37 C.F.R. 1.17(p). Please credit any overpayment or charge any underpayment to Deposit Account 19-1970. Election to pay the fee should not be taken as an indication that applicant(s) cannot execute a certification.

Certification (37 C.F.R. 1.97(e))
(Applicable only if checked)



The undersigned certifies that:

☒ Each item of information contained in this information disclosure statement was first cited in any communication from a foreign patent office in a counterpart foreign application not more than three months prior to the filing of this statement. 37 C.F.R. 1.97(e)(1).

☒ A copy of the communication from the foreign patent office is enclosed.

OR

☐ No item of information contained in this information disclosure statement was cited in a communication from a foreign patent office in a counterpart foreign application, and, to the knowledge of the undersigned after making reasonable inquiry, no item of information contained in this Information Disclosure Statement was known to any individual designated in 37 C.F.R. 1.56(c) more than three months prior to the filing of this statement. 37 C.F.R. 1.97(e)(2).

Respectfully submitted,

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				First Named Inventor	Marcos C. Tzannes
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U.S. PATENT DOCUMENTS					
Examiner Initials*	Cite No. ¹	Document Number Number-kind Code ² (if known)	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear

FOREIGN PATENT DOCUMENTS						
Examiner Initials*	Cite No. ¹	Foreign Patent Document Country Code ³ ; Number ⁴ ; Kind Code ⁵ (if known)	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear	T ⁶
	1	GB 2389493	12/10/2003	NEC CORP		

OTHER ART (Including Author, Title, Date, Pertinent Pages, etc.)		
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	2	Official Action for European Patent Application No. 10000016.5, dated Dec. 22, 2011 (Attorney Ref. No. 5550-57-PEP-DIV-2)

Examiner Signature		Date Considered	

*EXAMINER: Initial if reference is considered, whether or not citation is in conformance and not considered. Include copy of this form with next communication to applicant.

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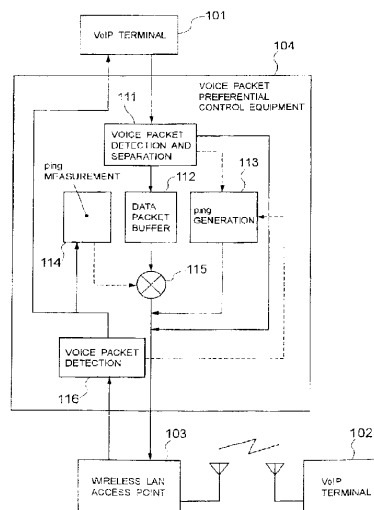
(56) Documents Cited:
GB 2344029 A **GB 2166320 A**
WO 2002/058293 A2 **WO 2002/032097 A2**
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(54) Abstract Title: **Voice packet preferential control equipment**

(57) Voice packet preferential control equipment 104 adapted to be added to media conversion equipment 103 (in one embodiment a wireless LAN access point) connecting a high-speed and low-speed communication circuit, the control equipment being adapted to function such that: when a voice packet is detected 111 from packet information on a communication circuit, said control equipment preferentially transmits a voice packet and interrupts and buffers 112 transmission of data packets from said high-speed circuit; and subsequently, said control equipment checks traffic of said low-speed circuit, continues to buffer said data packets when the traffic is in a congestion state, and terminates said buffering and resumes data packet transmission when the traffic is in a non-congestion state. The congestion state may be determined using ping packets 113 to measure a round trip period and may be compared to a preset value (threshold). The added control equipment therefore enables quality of service (QoS) requirements to be introduced in an access point in a VoIP (or VoIPoW) system which would otherwise not support QoS.

FIG. 1



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FIG. 1

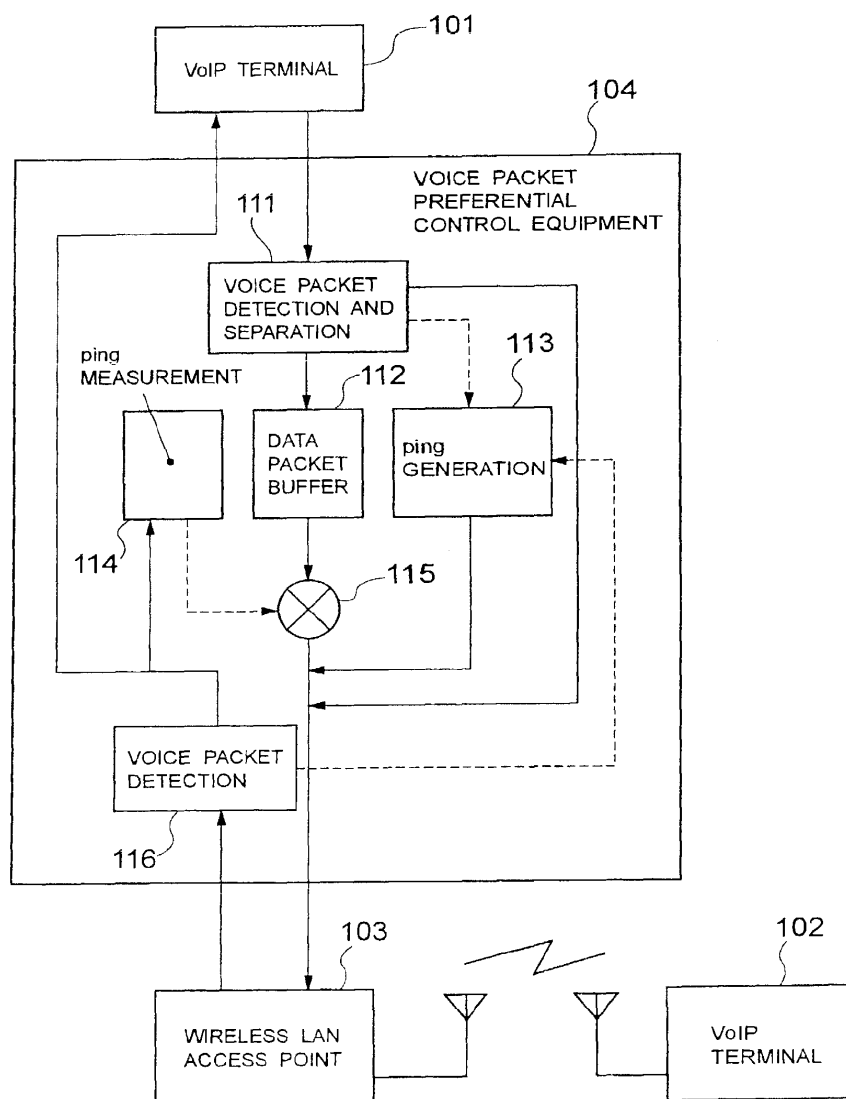
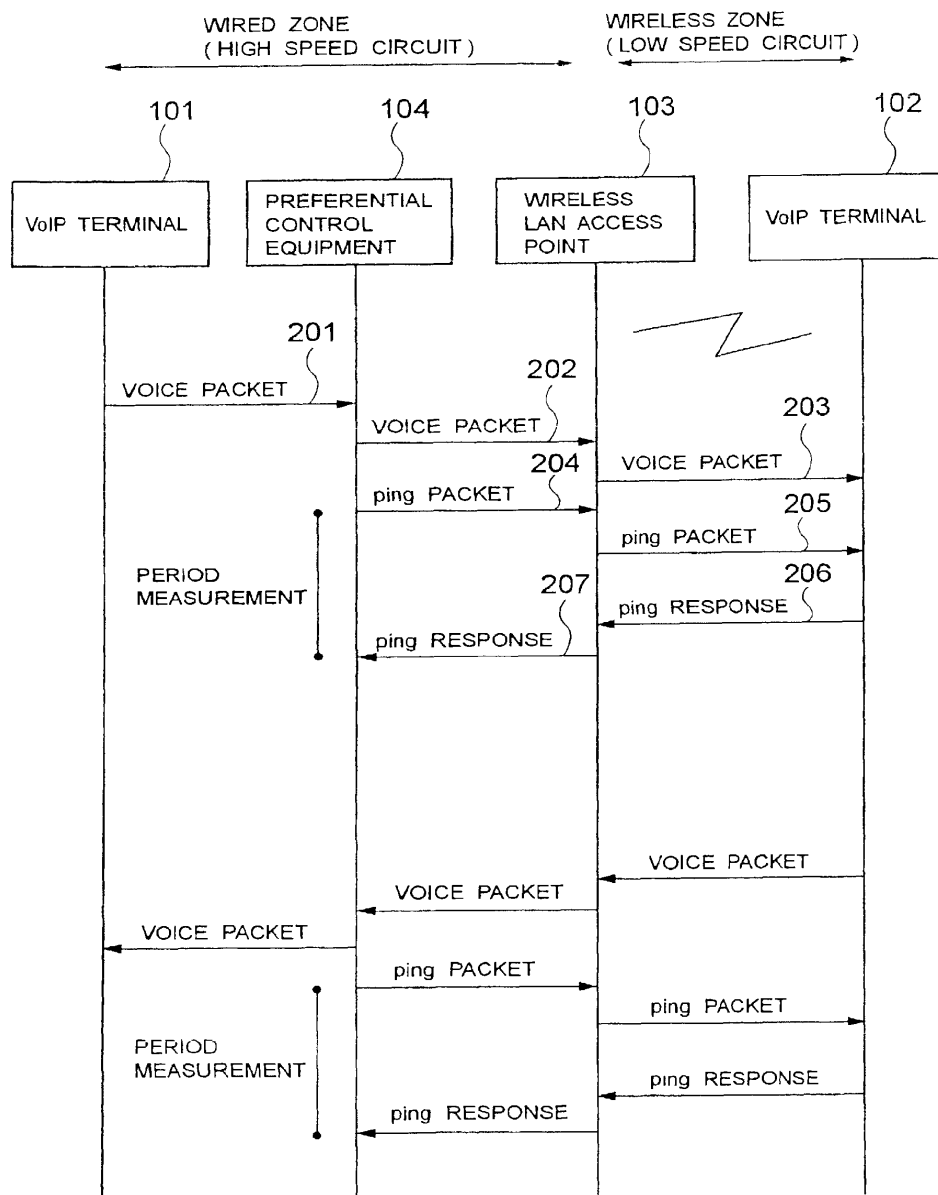


FIG. 2



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```

    tmp                = 0x20000000 - ((phaseAcc[31:0] & 0xffffffff)
>> 15) * bankFactor
    tmp                = MAX([0, tmp])
5    xmtPhaseTmp[4:0]  = tmp >> phaseShift
    xmtPhase[3:0]      = LIMIT(xmtPhaseTmp[4:0], 0, 15)
    alphaTmp[31:0]     = tmp - (xmtPhase[3:0] << phaseShift)
    alpha[8:0]         = alphaTmp >> (phaseShift - nInterpBits)
    c0Ptr              = coeffPtr + (xmtPhase[3:0] * nCoeffs)
10    c1Ptr             = c0Ptr + nCoeffs
    coeffs[k]          = c0Ptr + ((c1Ptr[k] - c0Ptr[k]) * alpha[8:0]) >>
nInterpBits

```

NOTE:

15 coeffPtr is a pointer to the fixed set of 17 banks of coefficients.

The phaseInc and bankFactor parameters should be updated atomically in order to ensure that there are no glitches in the xmtPhase computation. A new input sample is shifted into transmit re-sampler 122 delay line with every other increment of the phase accumulator 309.

20 The ATUR receiver continuously extracts timing information from the received signal and updates the control signals 350 352 and 354 in order to track any clock drift that may occur in the system.

25 There are several different ways to update the timing of the re-samplers: 1) through use of a phase tweak (periodically adjust the phase accumulator), 2) through update of the phase increment, or 3) using a combination of 1) and 2). In the former case, the phase tweak is applied in conjunction with the phase increment when incrementing the phase accumulator 309. If Δ represents the adjustment to be applied to the phase accumulator 309, it is performed by using a phase tweak given by

$$\text{phaseTweak}[31:0] = \text{phaseInc}[31:0] + \frac{\Delta}{2}$$

35 for 2 consecutive phase increments (the phase tweak acts as the phase increment for 2 consecutive phase increments). The phase tweak must be limited to be less than 2^{29} otherwise it would be possible to wrap twice modulo 2^{29} with a single increment of the phase accumulator 309. The use of

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the common phase accumulator 309 shared between the receive re-sampler 116 and transmit re-sampler 122 ensures that receive and transmit timing is locked.

5 III. Copying DMA With Two Separate Strides Selected by a Modulo-n Counter to Perform Convolutional De-interleaving.

 In a communication system employing convolutional interleaving (such as an ADSL), it is necessary for the receiver to de-interleave the decoded data stream. A data buffer is used to implement the de-interleaving process. For each codeword-sized interleaved data block decoded and written
10 into the data buffer, a single de-interleaved codeword is read from the data buffer. Because the data buffer requires substantial storage capacity, up to 16 KB for an ADSL system, it is desirable to share a single physical memory between the de-interleaving data buffer, other receiver system I/O buffers, and program and data storage. This type of shared memory architecture is known
15 as a unified memory architecture (UMA).

 The problem, however, with using traditional UMAs is that the codeword-sized blocks written to the de-interleaving data buffer are not an integer multiple of the width of the shared physical memory. This complicates the write interface to the shared memory by requiring it to perform alignment
20 of the codeword-sized block and partial word writes in order to append the block to the existing data buffer contents. The second stride is also adjusted to account for a dummy byte added at the input to the interleaver (to make the interleaved block size relatively prime to the interleave depth) but not transmitted, as in systems like ADSL. The write interface is further
25 complicated by the need to re-insert a dummy byte added at the input to the interleaver (to make the interleaved block size relatively prime to the interleave depth) but not transmitted. As a solution, the present invention uses a DMA scheme with two separate strides to copy codewords from the de-interleaving data buffer..

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FIG. 4 is an illustration of a more detailed block diagram of the control processor 205, shown in FIG. 2. The control processor 205 is an example of a control processor, or DPS, suitable for implementing the DMA scheme of the present invention. In FIG. 4, the control processor 205 includes a central processing unit (CPU) 400, a memory 402, and an input/output interface 403. The DMA engine 404, responsible for implementing the DMA functions, includes a DMA memory storage area 406.

The DMA storage area 406 includes an exemplary de-interleaving data buffer 408, along with other DMA related storage locations. The DMA scheme is implemented using a DMA engine 404 to execute the overall DMA operations associated with the control processor 205. Thus, the DMA engine 404 receives data, via the control processor 205, based upon a received signal, such as the digitized signal 112. The received data is then placed into the data buffer 408 for de-interleaving. The data is read from the data buffer 408, or de-interleaved, in accordance with the DMA engine 404, selected DMA parameters (discussed in greater detail below), and a modulo counting scheme. The modulo counting scheme is accomplished using an exemplary modulo counter 410.

In the present invention, the use of two separate strides, for placing the data into the data buffer 408 allows the codeword-sized blocks, written to the buffer, to be appended with dummy bytes. This padding enables the codeword sized blocks to be translated to a size, or format, that is an integer multiple of the shared physical memory width. The size conversion simplifies the write interface by eliminating the need for data alignment and partial word writes into the shared memory.

The first stride specifies the increment between codeword elements necessary to perform the basic de-interleaving operation. The second stride allows the DMA engine 404 to skip over the dummy padding every codeword-size bytes. The wrapping of a modulo-n counter indicates when the second stride should be used to perform the skip.

FIG. 5 is an illustration of an exemplary decoded serial byte stream 500, segmented into codeword-sized data blocks A-G. The byte stream 500

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includes a plurality of individual interleaved bytes, as shown, and is representative of a typical byte stream received as an input to the CPU 400 and processed by the DMA engine 404. Such byte streams are normally interleaved on the transmitter side in order to provide features such as robustness and security and thus require de-interleaving at the receiver side.

5 In the example of FIG. 5, and for purposes of illustration only, the byte stream 500 has a de-interleave depth (D) of "4" and a block size value (N) of "5." The de-interleave depth (D) controls the amount of time each byte is delayed. The block size value (N) specifies the number of bytes in each
10 codeword. Thus, in the example of the byte stream 500, each of the individual bytes is delayed by four time slots. In the present invention, the DMA engine 404 is configured to efficiently place the originally transmitted bytes of the data stream 500 back into their original order (1, 2, 3, 4, 5, 6...) instead of the interleaved order (0, -, -, -, 1, 5, etc.), illustrated in FIG. 5. FIG. 6 illustrates
15 the first step in the process of re-ordering the bytes of the data stream 500, i.e., copying each of the codeword-size blocks A-G into the data buffer 408.

In FIG. 6 the input buffer 408, shown vertically arrayed, is partitioned into separate memory locations 600 – 608. For purposes of illustration, the memory locations 600-608 correspond to the exemplary data blocks A-E. In
20 the example of FIG. 6, each of the memory locations 600-608 has a memory width (W) of four bytes. The DMA engine 404 must respectively copy the codeword-size data blocks A-E into the memory locations 600-608. In a first stage of de-interleaving the byte stream 500, the DMA engine 404 writes the first block A, is indexed 0, -, -, -, 1, into the memory location 600 in the
25 manner illustrated in FIG. 6.

A common requirement on many different types of memories is that data must be written to the memory in integer multiples of the memory width (W). Although exceptions to this requirement are possible, the exceptions provide inefficient, overly complex schemes that sacrifice speed and power
30 and erode other valuable system resources. Therefore, in the present invention, the DMA engine 404 will copy the five bytes of the data block A,

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and all of the other five byte codeword-size blocks B-G, into the buffer 408 in multiples of four bytes at a time.

Since the data blocks A-E are five bytes in width, and thus not a multiple of the memory width (W) of four bytes, the data blocks A-G must be
5 appended, or padded, with three dummy padding bytes 610-618 respectively. This padding artificially converts the length of each of the blocks A-E to eight bytes, a multiple of the memory width (W) four. With all of the exemplary data blocks A-E, including the appended padding bytes 610-618, now having been stored in the respective memory locations 600-608, the DMA engine 404
10 must now perform the de-interleaving.

FIG. 7 is an illustration of essential parameters used by the DMA engine 404 to de-interleave the now padded data blocks A-E, stored in the memory locations 600-608 of the buffer 408. The DMA parameters shown in FIG. 7 are typically stored in DMA registers or storage areas, such as the
15 DMA memory storage area 406. As noted above with reference to FIGs. 5 and 6, the byte stream 500 and the DMA parameters of FIG. 7 are for the exemplary case where the interleave depth (D) is 4 and the byte size (N) is 5. traditional DMA engines use many other DMA parameters to perform de-interleaving. The present invention also uses some of these other DMA
20 parameters. For purposes of clarity, however, the present application will not address these other parameters since their use remains unchanged in the present invention. Instead, the description of the present invention will focus on the DMA parameters shown in FIG. 7.

The STRIDE is the first of the DMA parameters listed in FIG. 7, and is
25 has a value of 4. In the present invention, the STRIDE is the distance from one byte, that requires copying to memory, to the next byte requiring copying. STRIDE2, with a value of 4+3, is similar to the STRIDE, plus the number of padding bytes, such as the three bytes of padding 610 stored in the memory location 600. Thus, in the case of STRIDE 2, the DMA engine will skip over
30 the padding bytes 610 in addition to the interleave depth. The number of padding bytes is referred to as the PADSIZ.

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In the example of FIGs. 6 and 7, the STRIDE increments through all of the values of the block A (0,-,-, and 1) to obtain the value "1." And the "3" in the STRIDE2 implies skipping over the "5" and the two dashes that follow the "5" of the block B, to get to the "2" value of the block B. Also included in the DMA parameters are the values of OFFSET, OFFSET INC, and OFFSET MOD, discussed in greater detail below.

The following is an exemplary approach to initializing the DMA parameters shown in FIG. 7 of the instant invention:

```

10      stride      = floor(D / N) * (N + PADSIZ) + (D mod N)
      stride2     = stride + PADSIZ
      offset      = 0
      offsetInc   = D mod N
      offsetMod   = N

```

where D is interleave depth
 N is interleave length (i.e. including any pre-interleave padding)
 PADSIZ is number of padding bytes per codeword (including any pre-interleave padding not transmitted which is negative)

The DMA computes each address to copy from as follows:

```

      offset += offsetInc
      if (offset >= offsetMod) then
25          offset -= offsetMod
          address += stride2
      else
          address += stride

```

FIG. 8 is an illustration of an exemplary DMA address sequence for determining the order in which the de-interleaved data bytes of the blocks A-E are read from the buffer 408. In FIG. 8, step 0 represents the reading of address A, which is the beginning of the buffer 408, where the bytes are numbered from left to right. Thus, the DMA engine 404 will first read the value "0" at address A. Address A corresponds to the first byte of the first row of the memory location 600 of the buffer 408. Next, in step 1, the DMA engine 404 will increment the address by the STRIDE value of "4." Thus, address A+4 of the buffer 408 will be read, which contains the value "1." The

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address A+4 corresponds to the first byte of the second row of the memory location 600.

In step 2 of FIG. 8, the STRIDE2 of FIG. 7 will be used instead of the STRIDE, which represents an increment of 7. Thus, the DMA engine 404 will skip over 7 values to obtain the value of "2," shown in byte position four of the memory location 602. The DMA engine 404 will continue to read the remaining contents of the memory locations 602-608 to finally produce a de-interleaved byte stream sequenced as 0,1,2,3,4,5....

In any particular read cycle, the DMA engine 404 will use STRIDE or STRIDE2, but not both at the same time. Thus, the DMA engine 404 must know apriorily whether to use STRIDE or STRIDE2. The values of the OFFSET column of FIG. 8 determine whether the DMA engine 404 will use STRIDE or STRIDE2. The values of the OFFSET column operate based upon a modulo-n counting scheme. The modulo-n counting scheme controls the OFFSET, OFFSET INC, and OFFSET MOD (the modulo of how the offset of FIG. 8 is incremented) of the DMA parameters shown in FIG. 7.

The offset of FIG. 8 initially begins at 0, and for each step, is incremented by the OFFSET INC value. If the offset is initially 0, it will ordinarily be incremented by 4 each time. However, the offset counts by modulo. Therefore, in the example of FIGs. 5 -8, the only legal numerical values are 0-4, since the present example is based on modulo-5. The OFFSET MOD value corresponds to the byte size (N). Thus, in FIG. 8 at step 0, the offset is 0, and then the DMA engine 404 increments by 4. In step 1, the offset is 4. In step 2, the DMA engine 404 increments by 4 again, and so it would ordinarily be 8. The value, however, gets reduced because the counting is based on modulo-5, which in-turn, produces the offset value of 3. The remaining values of the offset column of FIG. 8 are determined in this manner and this process continues until the entire byte stream 500 is completely de-interleaved.

Thus, in accordance with the present invention, the DMA engine 404 uses two strides to facilitate an efficient implementation of a UMA memory technique. This technique ensures that codeword-size data blocks can be

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written into memories in cases where the originally transmitted data blocks are not an integer multiple of the width (W) of the input buffer memory. In so doing, this process eliminates the need to perform alignment and partial word writes of the data blocks, which provides significant savings of system resources.

IV. Conditional One's-complement of Partial Address to Map Butterfly Address Generation to FFT/IFFT Post-/Preprocessing Pass Address Generation.

Processors, such as the control processor 205 of FIG. 2, support FFT/IFFT functions through use of standard radix-2 butterfly operations. These butterfly operations are specific implementations of an FFT algorithm in cases where the number of input samples is a power of 2. In order to implement these FFT/IFFT functions, the processor 205 includes address generation logic to access the input and output operand pairs (address pairs) of each butterfly.

One way of generating the butterfly input and output address pairs is to use a pointer and a fixed offset to access the operands at addresses 'pointer' and 'pointer+offset', incrementing the pointer through each recursion in the FFT/IFFT stage. A preferred approach would be to support optimized implementations of the FFT/IFFT for real-valued FFT inputs and IFFT outputs using standard post and pre-processing steps. Using standard post and pre-processing steps, however, the inputs to the butterfly operations of the post-and pre-processing steps are not separated by a fixed offset, and thus cannot use the normal operand addressing logic.

As a solution, the present invention uses an exemplary circuit implementation to conditionally invert the $n-1$ least-significant bits (LSBs) of the butterfly operand addresses provided for an N -point FFT/IFFT, where $N = 2^n$. The $n-1$ LSBs are inverted when the n 'th operand address bit (address[n-1] where the LSB is address[0]) is 1, otherwise the LSBs are unchanged. This effectively reverses the last $N/2$ inputs to the real-valued FFT post-processing

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pass or IFFT pre-processing pass, yielding un-unfixed offset between the inputs to the butterfly operations of the pass.

FIG. 9 is an illustration of a conventional 512 point FFT implementation 900. In FIG. 9, pairs of 512 real-valued inputs 902 are represented in the form of a 256 point (pre-processing) complex FFT 904. Using a traditional FFT approach, the 256 point complex FFT values are processed in the stage 904. Next, a conventional FFT post-processing stage 906 is implemented to produce 256 complex outputs 908. FIGs. 10 and 11 provide more detailed illustrations of the complex FFT operation 904 and the FFT post-processing stage 906.

In FIG. 10, a complex FFT operation, such as the pre-processing FFT operation 904, is implemented using a standard radix-2 butterfly 1000. A butterfly is a computational technique that takes a pair of real-valued FFT inputs and produces a pair of complex outputs. While the FFT operation 904 of FIG. 9 is a 256 point FFT, for purposes of simplification, the butterfly technique 1000 is demonstrated using an 8 point FFT.

In the illustration of FIG. 10, 8 complex value inputs 1002 (representative of 16 real-valued inputs) are provided as inputs to the butterfly 910. Outputs 1004 of the butterfly 1000 are represented as output addresses B0-B3. The output address B0 is associated with complex value inputs 0 and 4, which are provided as inputs to a first butterfly calculation (of the butterfly 1000). The output address B1 is associated with inputs 1 and 5, which were provided as inputs to a second butterfly calculation, the address B2 is associated with inputs 2 and 6, and so on, as illustrated in the step/address table 1006, also shown in FIG. 10. A point of interest with regard to the output addresses B0-B3, is that distances 1008-1012 (or offsets) between the addresses B0-B3 are fixed, with respect to each of the butterfly calculations of the butterfly 1000.

In FIG. 11, a standard post-processing operation, such as the post-processing operation 906, is implemented using a butterfly 1100. The butterfly 1100 receives inputs pairs 1102 and produces outputs 1104, shown as addresses C0-C2. In the post-processing butterfly 1100, however, offsets

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1106-1110, associated with the inputs 1102, are not fixed. That is, the offsets 1106-1110 decrease in length for each of the butterfly calculations associated with the butterfly 1100. In an exemplary embodiment of the present invention, FFT pre-processing output addresses having fixed offsets, such as the exemplary addresses B0-B3, are transformed into FFT post-processing addresses having decreasing offsets, such as the exemplary addresses C0-C2.

FIG. 12 is a block diagram illustration of an exemplary circuit 1200 be configurable to transform the addresses output from an FFT pre-processing stage into addresses representative of an FFT post-processing stage. The circuit 1200 can be inserted into the logic path of a DSP controller, such as the controller 205 of FIG. 2, to perform this address transformation.

The circuit 1200 is coupled to an output of a conventional FFT address generator 1201. The address generator 1201 is included as part of an FFT intermediate processing FFT algorithm, such as the operation 904, and produces FFT complex values, such as those that would be provided to the post-processing operation 906. At a high level, the circuit 1200 is configured to perform a conditional one's complement of the address output from the address generator 1201.

The circuit 1200 includes a mask generator 1204 and a logic gate 1206 configured to perform a complementing operation. In the embodiment of FIG. 12, the logic gate is an exclusive OR gate, although other suitable logic circuits can be used. A value (n) specifies the number of address lines or bits output from the FFT address generator 1201. Another value (N) represents the size of the FFT operation to be performed, such as 256 point or 512 points, and is provided as an input to the mask generator 1204.

The mask generator 1204 allows the circuit 1200 to function with FFTs of different sizes. The mask generator 1204 also determines how many of the bits, output from the address generator 1201, should be complemented. A pre/post processing enabling signal 1208 is provided as input to the mask generator 1204. The signal 1208 enables the circuit 1200 when an FFT computation reaches the post-processing stage 906. The function of the circuit 1200 is explained in greater detail below, in relation to FIG. 13.

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FIG. 13 is a detailed illustration of exemplary outputs 1300 of the FFT generator 1201. FIG. 13 also illustrates exemplary masks 1302. Each row of the masks 1302 is associated with a corresponding one of the rows of the outputs 1300, as indicated by the arrows. As noted above, the value (N) specifies the size of the FFT operation to be implemented. The example of FIG. 10, where (N) is 8, corresponds to the first two rows of the outputs 1300. An (N) value of 16 corresponds to the third and fourth rows of the addresses 1300 and masks 1302. In the example where (N) is 8, there is only one bit of the FFT generator 1201 that will control one of two output values of its corresponding mask within the mask values 1302.

When the signal 1208 indicates that the FFT post-processing is occurring, the mask generator 1204 is enabled. The output of the mask generator 1204 is then exclusively OR'd with the addresses having fixed offsets, output from the address generator 1201. The output of the circuit 1200 is a conditionally inverted address sequence having decreasing outputs, as discussed above. FIG. 14 is a more detailed illustration of the output of the circuit 1200.

In FIG. 14, steps 2-255 are shown, each corresponding to one of the addresses within an address sequence 1402. The address sequence 1402 is provided as an output from the address generator 1201 and includes fixed offsets (1/128, 2/129, 3/130, etc.). The circuit 1200, however, transforms the address sequence 1402, as described above, into the address sequence 1404 having decreasing offsets (1/255, 2/254, 3/254, etc.).

The present invention, therefore, provides significant economies by enabling the calculation of the post-processing FFT address sequence directly from the output of the FFT address generator 1201. This calculation is achieved through the use of simple logic circuit that performs a one's complement of the fixed offset addresses and a mask of the address. Thus, the techniques of the present invention facilitate savings of significant hardware resources that would ordinarily be dedicated to performing FFT post processing address.

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V. Definition and Implementation of SLICE Instructions on a Programmable SIMD Processor Data Path.

An important function in digital communication receivers is the 'slicing' of a received data symbol to determine the nearest point (or phase state) on a constellation grid. That is, the digital communication receivers must be able to closet grid point, from a standpoint of distance, that a particular received symbol value is associated with when it was transmitted. Put more simply, the receiver use slicing to determine precisely what was originally transmitted.

One commonly used approach to perform slicing in a DSP is through execution of a sequence of conventional instructions. The slicing function can also be implemented in dedicated logic, but this approach is inflexible and requires additional hardware resources. Dedicated logic, however, is unnecessary in systems where data paths of a SIMD based programmable DSP, such as the controller 205 of FIG. 2, can be modified to perform the slicing functions.

The instant invention provides an approach for slicing operations to be more efficiently and upported directly on a programmable DSP. This more efficient approach is facilitated through extensions to the instruction set, modifications to internal data paths, and use of control logic. The slicing operations are implemented using the data path logic that is provided for other basic operations.

DSPs typically provide functional units for multiplication, addition (accumulation) and result scaling. Many DSPs provide multiple sets of such units, controlled with a SIMD scheme to enhance performance. Slicing can be efficiently implemented using pairs of such units processing the in-phase and quadrature phase (I and Q) components of a received symbol. A more detailed discussion of preferred embodiments of the present invention is provided below in relation to a description of FIGs. 15-20.

FIG. 15 is a block diagram illustration of a conventional three stage DSP functional SIMD based data module 1500, having first and second

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parallel paths 1502 and 1504. Since the first and second data paths 1502 and 1504 include identical functional modules, the discussion of the first parallel path 1502 will apply equally to the parallel path 1504. The conventional data module 1500 includes a first pipeline stage 1506 including a multiplier 1507, a second pipeline stage 1508 including an adder 1509, and a third stage 1510 including a scalar 1511. Also included are registers 1512 for holding addresses or instructions used for manipulation of data passed through each of the stages of the data module 1500.

In the conventional functional data module 1500 illustrated in FIG. 15, input operands OP1n and OP2n are received, from general registers, as inputs to the stage 1506 of the first path 1502 during a current timing cycle. The input operand OP1n might, for example, be representative of the "I" component of a received data point in the exemplary form of a 16 bit data word. The operand OP2n is traditionally representative of a scaling factor. The operands OP1n and OP2n are multiplied together in the multiplier 1507.

Next, the product of the multiplier 1507 is provided to the input of the adder 1509 in accordance with, for example, instructions stored in one of the registers 1512. In the module 1500, the second data path 1504 is configured to receive symbol data associated with the symbol's "Q" component, as discussed above. Further, while the first stage 1506 process the input from the current timing cycle, the stage 1508 is simultaneously processing an input from a previous timing cycle and the stage 1510 is simultaneously processing an input from an even earlier timing cycle.

A rounding value, provided as an input to a mutiplexer 1514, is added to the first product of the multiplier 1507 during the noted timing cycle. For subsequent products output from the multiplier 1507, the multiplexer 1514 selects its lower path such that the products are added with previous sums. A rounding value is provided so that when scaling is performed in the third stage 1510, the scaling will be performed on a sum having a fixed number of data bits.

Next, the result from the adder 1509 is scaled in the third stage 1510 by a scalar 1511. The scalar 1511 multiplies the result, output from the adder

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1509, times $2^{(-k)}$, where (k) is specified by the DSP instructions. The output of the scalar 1511, labeled as RSLTn, is then provided as an overall output of the data module 1500. As previously noted, FIG. 15 is an illustration of a conventional SIMD processor data path. FIG. 16, however, is an illustration of modifications, in accordance with the present invention, to the conventional data path of FIG. 15. This modification enables the data path to more efficiently support symbol slicing instructions.

In general terms, FIG. 16 provides a block diagram illustration of an exemplary data path module 1600 capable of performing symbol slicing instructions as part of its instruction set, i.e., performing the slice instruction as a primitive instruction. An advantage of the approach of the present invention is a reduction in the number of input cycles required to execute slice instructions. In a conventional DSP, slice instructions can require 20 or more cycles for execution. In the exemplary embodiment of FIG. 16, however, slice instructions can be executed within about two cycles.

More specifically, FIG. 16 includes a data path module 1600 including conventional components, such as the multiplier 1507, the adder 1509, and the scalar 1511, shown in FIG. 15. The module 1600, however, also includes an additional operand path 1602 and an additional multiplexer 1604.

A constants generator 1606 is provided to scale the bit stream associated with OP1 (the I or Q component) into a format that has its binary point in a fixed position. The scaling directly supports the slicing function and scales each of the I and Q components to a fixed format by multiplying OP1 by $2^{(k-b)}$, where k is a constant chosen based on the data path precision and b, an instruction parameter or operand, indicates the number of fractional bits in, for example, the 16 bit data stream of the I or Q component.

When control logic of the DSP detects that the data module 1600 is executing a slicing instruction instead of standard DSP instructions, the multiplexer 1604 selects its operand path 1602 (lower path). When the path 1602 is selected, OP1 is received and is multiplied by the expression $2^{(k-b)}$ and is thus scaled into the fixed binary point format. The use of a fixed format simplifies subsequent processing.

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Next, OP1n and the fixed format value (output from the constants generator 1606) are multiplied together in the multiplier 1507. The product of the multiplier 1507 is provided as an input to another multiplexer 1608. Also provided as an input to the multiplexer, are boundary constraints 1610 which are output from a slice decoder 1700, illustrated in FIG. 17. The slice decoder 1700 and the boundary constraints 1610 are discussed in greater detail below and in relation to FIG. 17.

FIG. 17 is an illustration of an exemplary slice decoder 1700. The slice decoder 1700 is conventional logic that is configured to receive the sign bits of the I and Q components associated with the received symbol data. The decoder 1700 also receives data representative of the particular constellation grid associated with the transmitted symbol data. The output of the decoder 1700 is a set of I and Q limit values 1610 (boundary constraints) and a set of I and Q load enable conditions 1702. The limit values 1610 and the enable conditions 1702 are a function of the location of the received symbol on a particular constellation grid, such as the grid shown in FIG. 18.

FIG. 18 is a graph of a conventional 4 x 4 constellation grid 1800. Constellation grids are representative of accepted communications standards and include two-dimensional displays of the baseband I and Q values of transmitted and received data symbols, as measured at a particular point in time. A vector from the center of the diagram to a specific constellation point is representative of the amplitude of the symbol. When symbol data is originally transmitted, its I and Q components have specific coordinates within a constellation grid. Due to noise, transmission error, and other factors, the symbol's receive constellation grid values often differ from its transmission constellation grid values. As noted above, the present invention is an efficient technique to determine the original transmitted constellation grid values of the originally transmitted data symbol.

Although the constellation grid of FIG. 18 is a 4 x 4 representation, the present invention can operate with constellation grids of other sizes, such as 2 x 2, 8 x 8, or diagrams that are not square. In FIG. 18, the points "A" and "B" are representative of the I and Q components of bits that combine to form a

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transmitted data symbol. When the points "A" and "B" were originally transmitted, they were associated with specific coordinates, or points, on the grid 1800. During transmission, however, the points moved off of their original grid coordinates as shown.

5 Therefore, the DSP, using instructions within the data module 1600, must slice the received symbol data to determine which of the coordinates on the grid that the points "A" and "B" were originally transmitted on. With reference to FIG. 17, the limit values 1610 are representative of the limits of the I and Q axis of the grid. In the exemplary grid 1800, the limits of the I
10 axis are +3 and -3, and the limits of the Q axis are also +3 and -3. These limits define a ring of grid points. The I and Q conditions 1702, on the other hand, are associated with whether the "A" and "B" points are actually within the ring of points.

 Referring back to FIG. 16, the product of the multiplier 1507 is
15 representative of an actual I or Q component of one of the A and B points. This product is received as an input to the multiplexer 1608. The multiplexer 1608 then alternately provides the product of the multiplier 1507 and the I and Q limit values 1610 to the adder 1509, which in the present invention, is used
20 as a comparator. The output of the adder 1509 is used to determine whether the points A and B are within the ring of I and Q points (finite grid) or outside the ring of points (infinite grid). As seen in FIG. 18, A is within the ring of points and B is outside.

 The output of the adder 1509 is provided as an input to a quantizer
25 circuit 1612. The quantizer circuit 1612 essentially forces the points A and B to the nearest point on the infinite grid. Subsequent cycles use the adders to implement boundary clamping via per-quadrant min/max operations that conditionally load the result registers (accumulators) based on comparisons performed by the adders (with possible auxillary comparisons). The constants
30 can be read from a table indexed by an instruction operand or directly specified by the operand. Additional details of the circuit 1612 are provided in the discussion concerning FIG. 19.

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In FIG. 19, the quantizer circuit 1612 includes an OR gate 1900 and an AND gate 1902 coupled to the OR gate 1900. A quantize signal is provided by the DSP control logic as a control signal to activate the quantizer 1612. At a more detailed level, the quantizer masks the k LSBs of the symbol data prior to storage in a results register 1614 (accumulator) to implement the quantization of each component when enabled. Also added to the results register 1614 are the I and Q conditions (load enable) 1702 from the slice decoder 1702 shown in FIG. 17. The quantized components are compared against constants determined by the constellation size and sign of the component in the accumulator register 1614. In other words, the accumulator results register 1614 compares the results of the quantizer with the actual I and Q input data symbol conditions.

The quantizer 1612 essentially forces the LSBs of the receive symbol data, to zero. The k-1 bits go through the AND gate 1902 and the next bits are received by the OR gate 1900. The most significant bits, which are left over, simply pass through the quantizer 1612 and remain unchanged. When the quantizer 1612 is in use, the adder 1509 can be used to implement symmetric rounding (about the point origin) and/or offset adjustment for constellations that aren't centered about the point origin.

Finally, an output from the results register 1614 is provided to the scalar 1511. The results scalar 1511 is used to divide each component by $2^{(k-b)}$ to return the components to the input format. The output of the scalar 1511 is a determination of the nearest grid points to the points A and B, within the constellation grid 1800. An exemplary slicing sequence implemented by the data module 1600 will be described in relation to a description of FIG. 20.

FIG. 20 is an exemplary table 2000 representative of two input cycles of the data module 1600. In FIG. 20, data points A and B are shown along a vertical column to the left. A "cycle" column shows two input cycles of the data path module 1600 for receiving input symbol data related to data points A and B. In cycle 1, the table 2000 shows that a quantize enable signal is "set" to activate the quantizer 1612. Since the quantize signal is present, the

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limits and conditions, included in the table 2000, are not used. Thus, the module 1600 will select the nearest grid point in infinite grid.

The grid 1800 illustrates that the nearest grid point in infinite grid of the I and Q coordinates, for point A, are -1 and -1. In cycle 2, the quantization has already been accomplished so the quantization signal is not set. Thus, the next comparison of the input symbol data is against the limits. Here, the I limit is -3 and a condition of "less than." The conditions of "less than" or "greater than" are a function of the quadrant that the point appeared in.

Similarly, for Q, the limit is -3, with a condition of "less than." Since in this case, the nearest point on infinite grid was within the actual 4 x 4 grid, the second cycle did not make any changes. Therefore, the result of the symbol slicing in this case was -1 and -1 for both the I and Q components, which correspond with a point on the grid 1800. The results for the point B, however, are slightly different.

The table 2000 illustrates that for the cycle 1, the quantize control signal is set. Therefore, the first step will be to quantize the symbol data associated with B onto the infinite grid. In this case, the output coordinates for I and Q are 1 and -5 respectively. The first arrow pointing away from point B on the grid 1800, points to the coordinates 1 and -5 for I and Q respectively. During cycle 2, the point B is compared against the limit of the finite grid. This comparison illustrates that the data point B is outside of this limit. Here, therefore, the result of cycle 2 is 1 and -3 for the I and Q limits, respectively. Thus, both points A and point B have now been associated with their nearest points in infinite grid, and consequently, associated with their original constellation grid coordinates.

The present invention, therefore, provides an approach for slicing operations to be more efficiently supported directly on a programmable DSP. The approach of the invention is facilitated through extensions to the instruction set, modifications to internal data paths, and use of control logic. The slicing operations are implemented using the data path logic that is provided for other basic operations. This approach facilitates performing the

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slice instruction as a primitive instruction. An advantage of the approach of the present invention is a reduction in the input cycles required to execute a slice instruction. The present invention reduces the required cycles from 20 to 2 or 3 cycles.

5 VI. Program Synchronization of A Processor and DMA Using Ownership Flags.

A processor DSP is often paired with a DMA engine and two working memories so that processor execution on data in one memory can overlap DMA transfers to and from the other memory. Higher performance processors
10 require more bandwidth than can be provided by a single working memory; additional bandwidth can be supplied by additional working memories. A synchronization mechanism is required to ensure that a given working memory is only in use by either the processor or the DMA at any given time, and to provide flow control of data passed between the processor and DMA
15 engine.

FIG. 21 is a block diagram illustration of an exemplary processor/DMA memory sharing scheme 2100. In FIG. 21, the memory sharing scheme 2100 includes another exemplary DMA engine 2102, a processor 2104, memories A-D, and associated ownership flags 2106.

20 FIG. 22 is an illustration of exemplary DMA program instructions 2200 and processor program instructions 2202, used in connection with the DMA engine 2102, the processor 2104, and the memories A-D.

Finally, FIG. 23 is an illustration of management and execution of the DMA program instruction 2200 and the processor program instructions 2202
25 based upon specific settings of the ownership flags 2106.

Systems with two or more working memories, such as the memories A-D, typically have the DMA engine 2102 and processor 2102 wait for each other upon completion of the tasks 2200 and 2202, shown in FIG. 22. When both the DMA engine 2102 and the processor 2104 have finished, the roles of
30 the memories A-D are swapped and the DMA engine 2102 and the processor

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2104 continue with the next set of tasks. This process is repeated for each set of tasks.

5 The ownership flags 2106 are provided to indicate, for each of the memories A-D, whether its use is controlled by the DMA engine 2102 or processor 2104. Specific instruction sets are provided for both the DMA engine 2102 and the processor 2104 for testing and setting the flags 2106. One instruction, from within the instruction set 2102, waits for the specified set of ownership flags to indicate ownership by the DMA engine 2102 or the processor 2104 executing the instruction. The other instruction sets the
10 specified set of ownership flags 2106 to indicate ownership by the DMA engine 2102 or the processor 2104 not executing the instruction.

The memory sharing scheme 2100, along with software convention, allows programs running on the DMA engine 2102 and the processor 2104. The scheme 2100 avoids simultaneous use of the exemplary working
15 memories A-D by transferring ownership of the memories, when finished with the memory, and waiting for ownership before accessing the memory. Similarly flow control is implemented by waiting for ownership of the memory containing the data being transferred before operating on it.

20 The present invention has been described above with the aid of functional building blocks illustrating the performance of specified functions and relationships thereof. The boundaries of these functional building blocks have been arbitrarily defined herein for the convenience of the description. Alternate boundaries can be defined so long as the specified functions and relationships thereof are appropriately performed.

25 Any such alternate boundaries are thus within the scope and spirit of the claimed invention. One skilled in the art will recognize that these functional building blocks can be implemented by analog and/or digital circuits, discrete components, application specific integrated circuits, firmware, processors executing appropriate software and the like or any
30 combination thereof. Thus, the breadth and scope of the present invention should not be limited by any of the above-described exemplary embodiments,

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but should be defined only in accordance with the following claims and their equivalents.

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WHAT IS CLAIMED IS:

- 5 1. A modem, comprising:
 one or more processing paths; and
 a number of interconnected modules sequentially arrayed along the one
 or more of the processing paths, each module being configured to (i) process
 signals passed along the paths in accordance with the sequence and (ii)
 implement unique functions to perform the processing;
10 wherein each of the modules has a particular degree of functional
 programmability; and
 wherein the degrees of functional programmability monotonically vary
 in accordance with the sequence.
- 15 2. The modem of claim 1, wherein the modem is an asymmetric
 digital subscriber logic (ADSL) modem.
3. The modem of claim 2, wherein the one or more processing
 paths include a receive path and a transmit path.
20
4. The modem of claim 3, wherein the interconnected modules
 includes at least one of an analog front end, a discrete multi-tone
 module/frequency domain equalizer and a direct memory access engine.
- 25 5. The modem of claim 1, wherein the predetermined functions
 include at least one of resampling, echo cancellation, fourier processing, and
 error correcting.
- 30 6. The modem of claim 5, wherein the functional programmability
 includes non-programmable hardware, programmable hardware, firmware,
 and software.

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7. The modem of claim 5, wherein the variations are representative of monotonic increases.

5 8. A modem comprising:
a receiver associated with a receive timing scheme;
a transmitter associated with a transmit timing scheme; and
only one timing mechanism (i) electrically coupled to the receiver and
the transmitter and (ii) configured to synchronize the receive and transmit
timing schemes.

10

9. The modem of claim 9, wherein the receiver includes a receive
re-sampler and the transmitter includes an transmit re-sampler.

15 10. The modem of claim 9, wherein the modem is an asymmetric
digital subscriber line (ADSL) modem.

11. The modem of claim 10, wherein the timing mechanism
includes a phase accumulator.

20 12. The modem of claim 10, wherein the timing mechanism
includes a coefficient generator and a phase accumulator.

25 13. A modem comprising:
a receive re-sampler configured to receive input signals in accordance
with a receive timing scheme;
a transmit re-sampler connected, at least indirectly, to the receive re-
sampler, the transmit re-sampler being configured to transmit output signals in
accordance with a transmit timing scheme; and
only one timing mechanism electrically coupled to the receive re-
30 sampler and the transmit re-sampler;
wherein the timing mechanism is configured to synchronize the receive
timing scheme and the transmit timing scheme.

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14. The modem of claim 13, wherein the modem is an asymmetric digital subscriber line (ADSL) modem.

5 15. The modem of claim 14, wherein the receive input signals includes digitized input signals.

10 16. The modem of claim 15, wherein the receive re-sampler produces interpolated signals based upon the received input signals and first timing coefficients.

15 17. The modem of claim 16, wherein the transmitted output signals include digitized output signals.

18. The modem of claim 16, wherein the transmitted output signals include second timing coefficients.

20 19. The modem of claim 18, wherein the first and second timing coefficients are produced based upon linear interpolation, the linear interpolation being a function of phase increment and phase accumulator.

25 20. The modem of claim 19, wherein the timing mechanism includes a phase accumulator.

21. The modem of claim 19, wherein the timing mechanism includes a phase accumulator and a coefficient generator.

30 22. The modem of claim 16, further comprising a timing tracking mechanism configured to receive the interpolated signal and produce timing data therefrom.

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23. The modem of claim 22, wherein the phase accumulator is configured to (i) receive the timing data and (ii) update the first and second timing coefficients based upon the received timing data.

24. A method for synchronizing timing in a modem having a receiver configured to receive an input data signal and a transmitter configured to produce an output data signal, the output data signal having timing characteristics based upon a transmit coefficient signal, the method comprising:

receiving (i) the input data signal and (ii) a receive coefficient signal in the receiver;

re-sampling the input data signal based upon the received coefficient signal to produce an interpolated signal thereby;

producing signal phase data based upon the interpolated signal; and

updating the receive coefficient signal and the transmit coefficient signal based upon the signal phase data.

25. The method of claim 24, wherein the signal phase data includes a phase increment, a phase tweak, and a coefficient factor.

26. The method of claim 24, wherein the updating includes adjusting a phase of the receive coefficient signal and transmit coefficient signal.

27. A method for de-interleaving a data stream stored in a buffer having a plurality of memory locations, each location having a memory width of (W) bytes, the data stream being formed of a number of data words each including (N) number of data bytes, wherein (N) is a non-integer multiple of the width (W), the method comprising:

storing the data words into respective memory locations;

appending each of the stored data words with number (X) of dummy bytes, a sum of (N) + (X) being an integer multiple of the width (W); and

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storing the appended dummy bytes into the respective memory locations.

5 28. The method of claim 27, wherein the data words include codeword-size data blocks.

 29. The method of claim 28, wherein the interleaved data stream includes an interleave depth (D); and
 wherein the method is implemented based upon operation of a direct
10 memory access (DMA) engine.

 30. The method of claim 29, further comprising de-interleaving the data bytes stored in the respective memory locations based upon operation of the DMA engine and a number of parameters;
15 wherein the parameters include first and second memory strides, an offset increment value, and an offset modulo value.

 31. A method for storing a data stream in a modem buffer having a plurality of memory locations, each location having a memory width of (W) bytes, the data stream being formed of a number of data words each including (N) number of data bytes, wherein (N) is a non-integer multiple of the width (W), the method comprising:

 (a) copying the (N) data bytes of a first data word into a first [(n)(W)] bytes of a first location, where (n) is an integer that (i) equals one when $W > N$ and (ii) is a smallest among all integers satisfying the expression $[(n)(W) > N]$
25 when $W < N$;

 (b) appending the first number (N) of copied bytes with (X) number of dummy bytes, a sum of $(X) + (N)$ being an integer multiple of the width W; and

30 (c) copying the appended dummy bytes (X) into the first (n)(W) bytes of the first location.

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32. The method of claim 31, wherein the copied first number (N) of data bytes and the copied (X) dummy bytes correspond to the first data word.

5 33. The method of claim 31, further comprising copying the (N) data bytes a remaining number of the data words into the remaining memory locations in accordance with (a) through (c).

10 34. The method of claim 33, wherein the interleaved data stream includes an interleave depth (D) and the method includes a memory access technique having at least first and second memory strides.

15 35. The method of claim 34, further comprising de-interleaving the data bytes in the memory based upon operation of the DMA engine, the DMA engine ignoring the dummy bytes (X).

36. The method of claim 35, wherein the de-interleaving is based upon operation of the DMA engine and at least the first and second strides.

20 37. The method of claim 36, wherein the de-interleaving occurs based upon the operation of the DMA engine, values of the first and second strides, an offset increment value, and an offset modulo value.

25 38. The method of claim 37, wherein a value of the first stride is equal to the interleave depth, and a value of the second stride is equal to the interleave depth plus (X).

30 39. The method of claim 38, wherein the second stride is used instead of the first stride; and wherein the second stride is used based a modulo of the offset increment value.

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40. An apparatus for de-interleaving a data stream stored in a buffer having a plurality of memory locations, each location having a memory width of (W) bytes, the data stream being formed of a number of data words each including (N) number of data bytes, wherein (N) is a non-integer multiple of the width (W), the apparatus comprising:

means for storing the data words into respective memory locations;

means for appending each of the stored data words with number (X) of dummy bytes, a sum of (N) + (X) being an integer multiple of the width (W); and

means for storing the appended dummy bytes into the respective memory locations.

41. The apparatus of claim 40, wherein the data words include codeword-size data blocks.

42. The apparatus of claim 41, wherein the interleaved data stream includes an interleave depth (D); and

wherein the apparatus is implemented based upon operation of a direct memory access (DMA) engine.

43. The apparatus of claim 42, further means for comprising de-interleaving the data bytes stored in the respective memory locations based upon operation of the DMA engine and a number of parameters;

wherein the parameters include first and second memory strides, an offset increment value, and an offset modulo value.

44. A circuit, comprising:

a fast fourier transform (FFT) address generator configured to produce a complex FFT address sequence, the complex FFT address sequence having fixed offsets; and

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a conversion mechanism configured to (i) receive the complex FFT address sequence and (ii) convert the received sequence into an address sequence having varying offsets.

5 45. The circuit of claim 44, wherein the circuit is included in a modem.

 46. The circuit of claim 45, wherein the modem is an asymmetric digital subscriber line (ADSL) modem.

10

 47. The circuit of claim 44, wherein the conversion mechanism is an FFT post-processing module.

 48. The circuit of claim 44, wherein the varying offsets vary in a decreasing direction.

15

 49. The circuit of claim 44, wherein the conversion mechanism performs the converting in lieu of FFT-post-processing.

20 50. The circuit of claim 44, wherein the conversion mechanism includes:

 a logic gate having first and second input ports and an output port, the first input port being coupled to an address generator output port, the output port being configured to output the address sequence having the varying offsets; and

25

 a mask generator having a third input port and an output port, the third input port being coupled to the address generator output port, and the mask generator output port being coupled to the second input.

30 51. The circuit claim 50, wherein the logic gate is an exclusive OR gate.

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52. A method for determining a fast fourier transform (FFT) post processing address sequence of an N-point FFT in a digital signal processor, the method comprising:

5 producing a complex FFT address sequence in response to N received complex FFT input samples, the complex FFT address sequence being representative of N/2 output address pairs having fixed offsets, the sequence including a bit stream having (n) data bits representative of a memory address of the output pairs, (N) being equal to 2^n ;

selecting particular ones of the data bits for complementing; and

10 performing an arithmetic operation between the selected particular ones of the bits and the complex FFT address sequence, the complement operation producing output address pairs having un-fixed offsets.

53. The method of claim 52, wherein the particular ones of the data
15 bits include an (n-1) least significant bit (LSB).

54. The method of claim 53, wherein an LSB address[0] is 1.

55. The method of claim 52, wherein selecting is implemented
20 based upon a masking operation.

56. The method of claim 52, wherein the arithmetic operation is a one's complement operation.

25 57. An apparatus for determining a fast fourier transform (FFT) post processing address sequence of an N-point FFT in a digital signal processor, the apparatus comprising:

means for producing a complex FFT address sequence in response to N received complex FFT input samples, the complex FFT address sequence
30 being representative of (N/2) output address pairs having fixed offsets, the sequence including a bit stream having (n) data bits representative of a memory address of the output pairs, (N) being equal to 2^n ;

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means for selecting particular ones of the data bits for complementing;
and

means for performing a arithmetic operation between the selected
particular ones of the bits and the complex FFT address sequence, the
5 complement operation producing output address pairs having un-fixed offsets.

58. The apparatus of claim 57, wherein the particular ones of the
data bits include an (n-1) least significant bit (LSB).

10 59. The apparatus of claim 57, wherein an LSB address[0] is 1.

60. The apparatus of claim 57, wherein the selecting is
implemented based upon a masking operation.

15 61. The apparatus of claim 57, wherein the arithmetic operation is a
one's complement operation.

20 62. A method for implementing a SLICE operation in a
programmable digital signal processor (DSP) as a primitive instruction in one
or more data paths of at least one of (i) a single instruction single data scheme
and (ii) a single instruction multiple data scheme.

25 63. The method of claim 62, wherein the SLICE instruction is
executed in three or less input cycles.

64. The method of claim 62, wherein the SLICE operation includes
an input symbol slicing stage and a quantization stage.

30 65. The method of claim 64, wherein the input symbol slicing stage
occurs during a first input cycle and the quantization stage occurs during a
second input cycle.

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66. The method of claim 65, wherein the SLICE operation is configured to associate input symbol data with a particular point of a constellation grid, the constellation grid being stored in a memory of the DSP

5 67. A computer readable medium carrying one or more sequences of one or more instructions for execution by one or more processors to perform a method for implementing a SLICE operation in a programmable digital signal processor (DSP) as a primitive instruction in one or more data paths of a single instruction multiple data scheme.

10 68. A digital signal processor (DSP) including a number of single instruction multiple data (SIMD) path logic units, each logic unit including (i) a multiplier having two or more input ports, one of the input ports being configured to receive input symbol data, the multiplier being configured to produce a multiplier output, (ii) an adder configured to receive the output product and produce an adder output therefrom, and (iii) a scalar configured to scale the adder output, the DSP comprising:

15 20 a constants generator coupled to another one of the number of multiplier input ports and being configured to produce a fixed format signal based upon the input symbol data, the multiplier output being representative of a product of the received input symbol data and the fixed format signal;

25 wherein the adder is configured to (i) receive boundary constraints representative of a first component of predetermined symbol standards and (ii) compare the multiplier output with the boundary constraints, the adder output being representative of the comparison; and

a quantizer configured to (i) receive the adder output and (ii) associate the received adder output with a second component of the predetermined symbol standard, the quantizer producing a quantized output.

30 69. The DSP of claim 68, wherein the DSP includes a number of data paths, each of the logic units being respectively arrayed along one of the paths.

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5 70. The DSP of claim 68, wherein the constants generator produces the fixed format signal in accordance with the expression $2^{(k-b)}$, where (k) is a predetermined constant, and where (b) is indicative of fractional bits associated with the symbol data.

10 71. The DSP of claim 70, wherein the symbol standards are associated with a constellation grid; and
 wherein the constellation grid is formed of an infinite grid and a finite grid.

 72. The DSP of claim 71, wherein the first component is the finite grid.

15 73. The DSP of claim 72, wherein the bit stream includes least significant bits (LSBs) and the quantizer sets the LSBs to zero.

 74. The DSP of claim 73, wherein the quantizer includes a logic array.

20 75. The DSP of claim 13, wherein the quantizer includes a first logic gate having first and second input ports and a first output port, one of the first and second input ports being configured to receive the output sum and the other of the first and second input ports being configured to receive a control
25 logic signal; and

 a second logic gate having third and fourth input ports and a second output port, one of the third and fourth input ports being coupled to the first input port and the other of the third and fourth input ports being coupled to the second input port, the second output port being coupled to the first output port.

30 76. The DSP of claim 75, wherein the first logic gate is an OR gate; and

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wherein the second logic gate is an AND gate.

77. The DSP of claim 76, wherein the second component is a nearest point within the infinite grid.

78. The DPS of claim 77, further comprising an accumulator configured to (i) receive condition data representative of a location of the input symbol data and (ii) update the quantized output based upon the received condition data.

79. A method of slicing a receive data symbol in a digital signal processor including a number of single instruction multiple data path logic units, each logic unit including (i) a multiplier having two or more input ports, one of the input ports being configured to receive input symbol data, the multiplier being configured to produce a multiplier output, and (ii) an adder configured to receive the output product and produce an adder output therefrom, the method comprising:

producing a fixed format signal based upon the input symbol data, the fixed format signal being multiplied by the input symbol data to produce the multiplier output;

comparing the boundary constraints with the multiplier output, a result of the comparing being representative of the adder output; and

associating with a second component of the predetermined symbol standard.

80. The method of claim 79, wherein the fixed signal format is produced in accordance with the expression $2^{(k-b)}$, where (k) is a predetermined constant, and where (b) is indicative of fractional bits associated with the symbol data.

81. The method of claim 79, wherein the fixed format signal is formed of a bit stream having a fixed binary point.

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82. The method of claim 79, wherein the input signal includes a phase component and a magnitude component.

5 83. The method of claim 79, wherein the symbol standards are associated with a constellation grid.

 84. The method of claim 83, wherein the constellation grid is formed of an infinite grid and a finite grid.

10 85. The method of claim 84, wherein the first component is the finite grid.

 86. A method for sharing one or more memories between one or more processors, each memory being associated with a respective ownership flag, the method comprising:

 associating each of the processors with a particular value of the flag;
 and
 assigning use of the memories to a corresponding one of the processors
20 when the respective ownership flag is set to the particular value.

 87. The method of claim 86, wherein each of the processors is associated with a different particular value.

25 88. The method of claim 87, wherein the particular values are changeable in association with selected processor cycles.

 89. The method of claim 88, wherein the use of a particular memory includes ownership of the memory during the during the selected
30 processor cycle.

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90. The method of claim 89, wherein each memory is assigned to only one processor during any one of the processor cycles.

5 91. An apparatus for sharing one or more memories between one or more processors, each memory being associated with a respective ownership flag, the apparatus comprising:

means for associating each of the processors with a particular value of the flag; and

10 means for assigning use of the memories to a corresponding one of the processors when the respective ownership flag is set to the particular value.

92. The apparatus of 91, wherein each of the processors is associated with a different particular value.

15 93. The apparatus of claim 92, wherein the particular values are changeable in association with selected processor cycles.

20 94. The apparatus of claim 93, wherein the use of a particular memory includes ownership of the memory during the during the selected processor cycle.

95. The apparatus of claim 94, wherein each memory is assigned to only one processor during any one of the processor cycles.

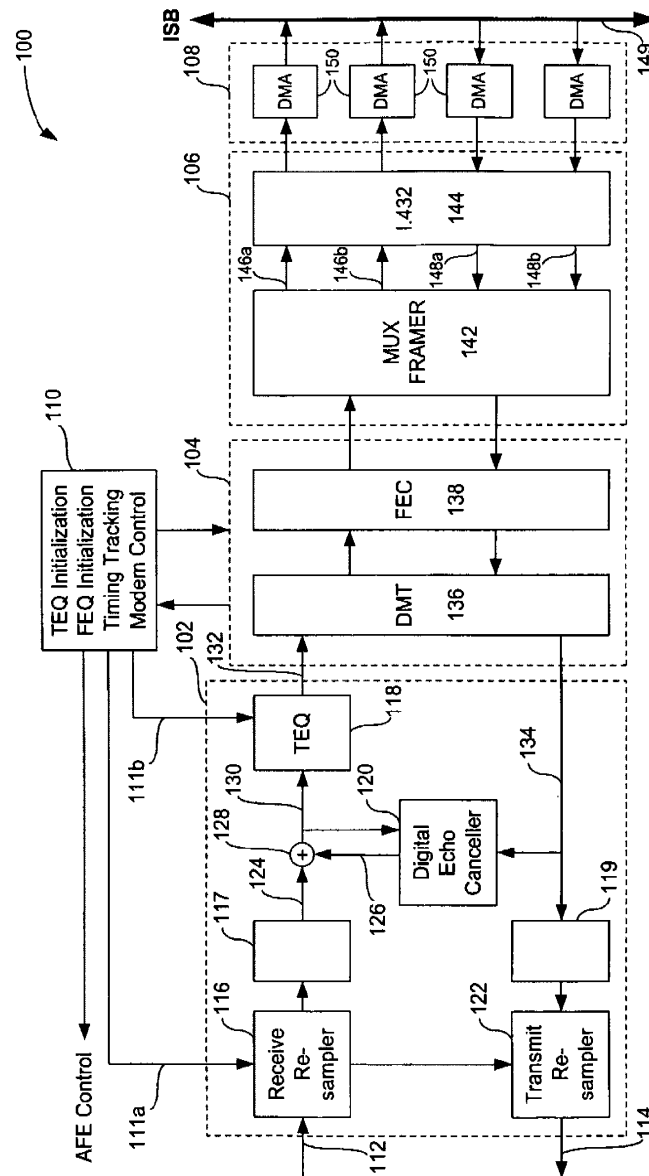


FIG. 1

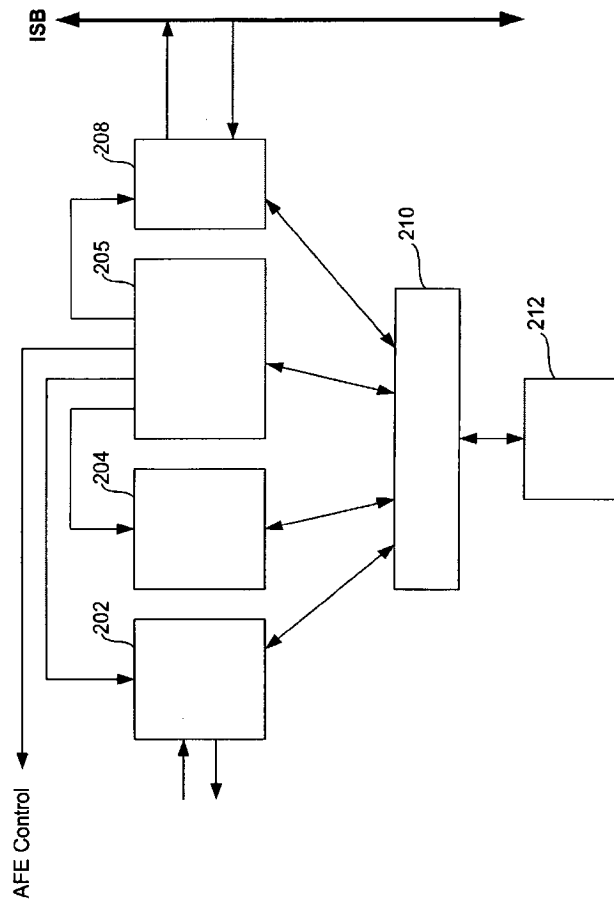
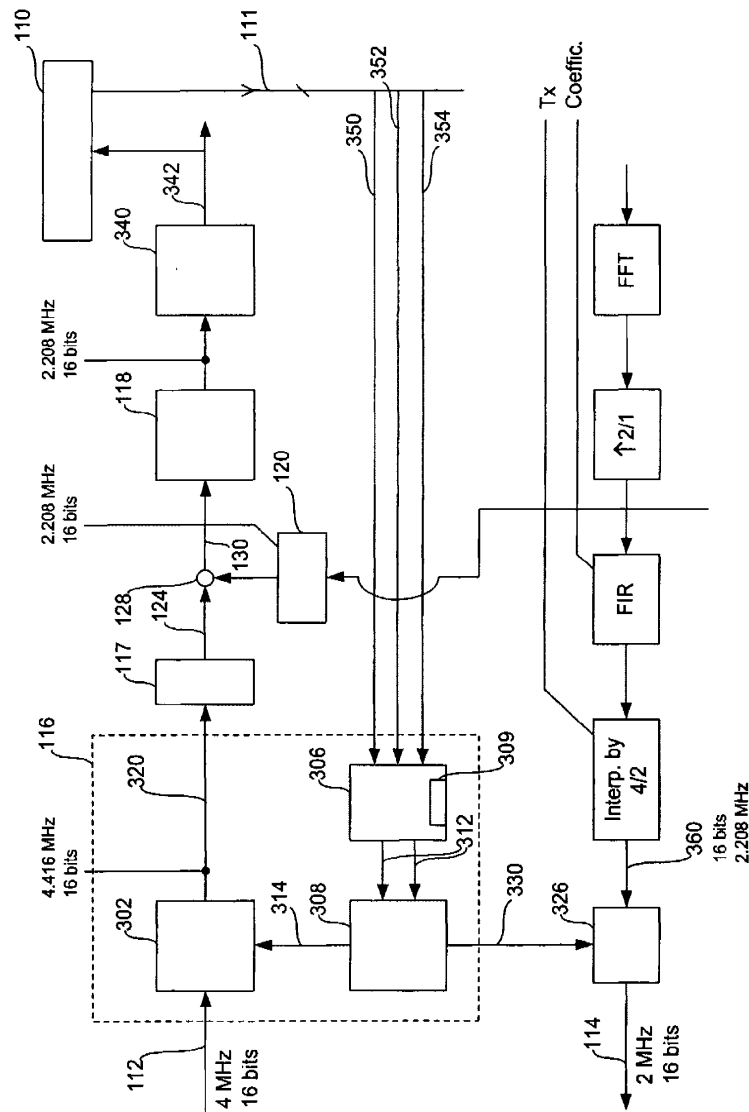


FIG. 2



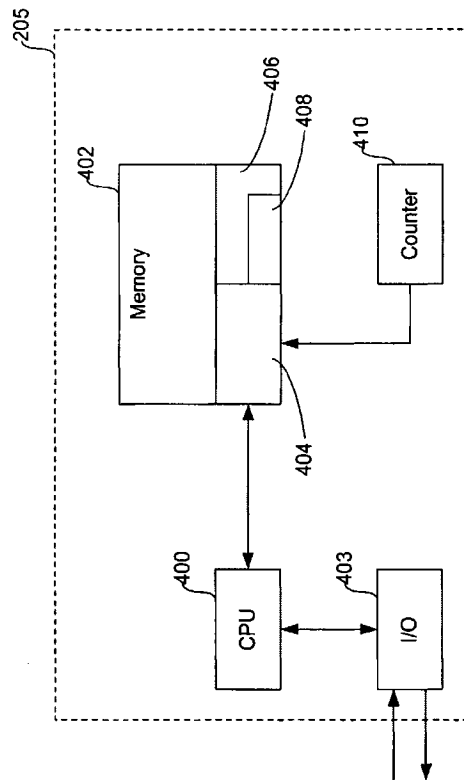


FIG. 4

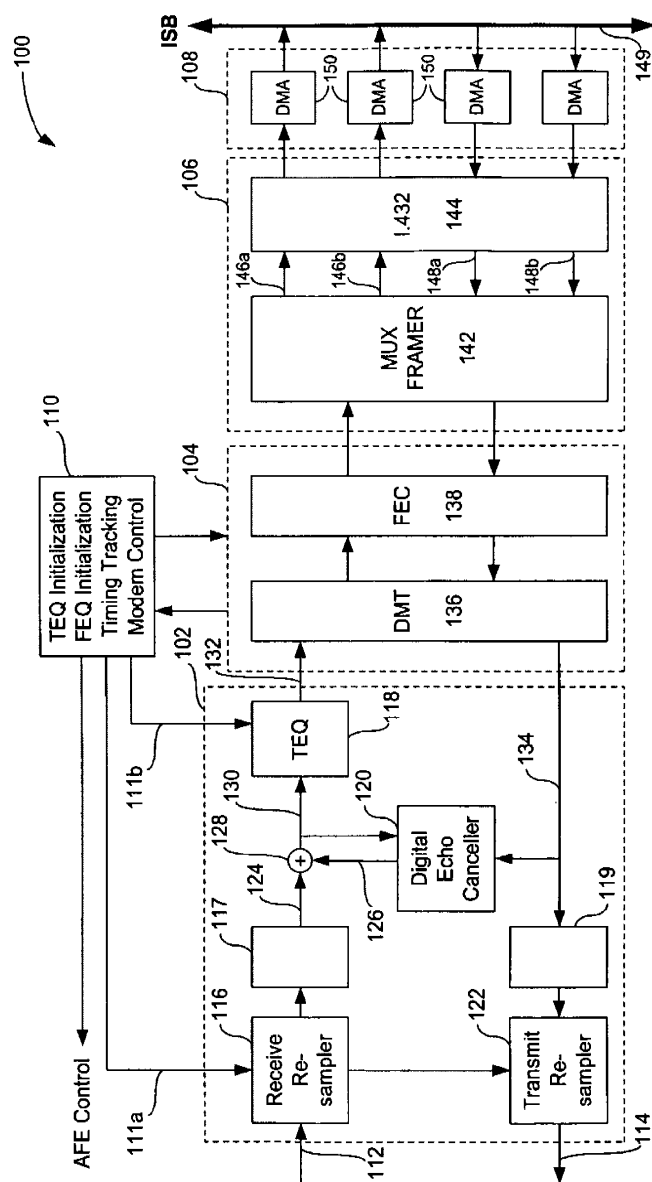
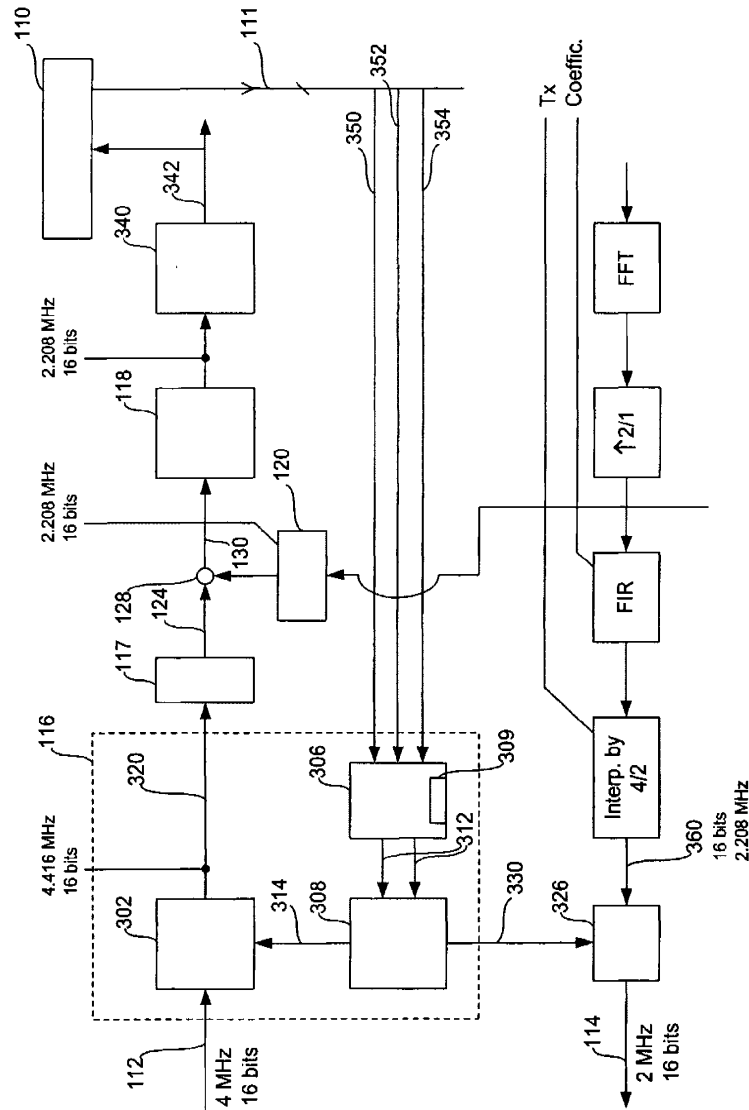


FIG. 1



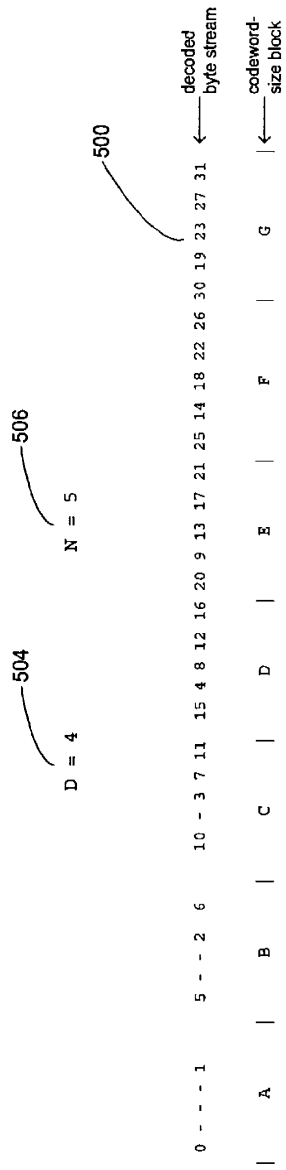


FIG. 5

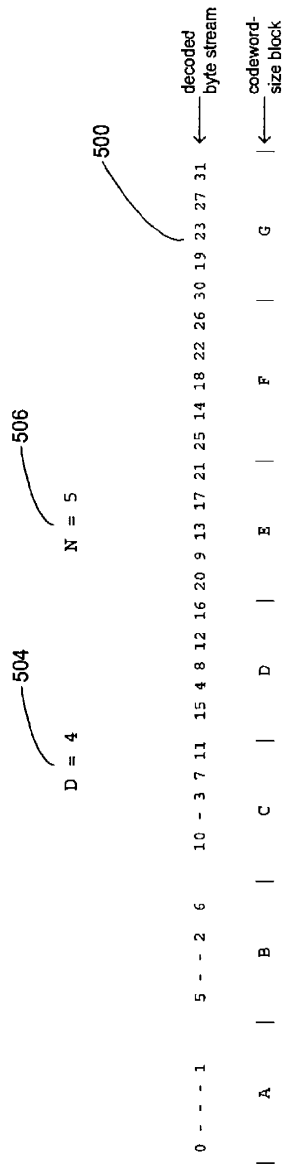


FIG. 5

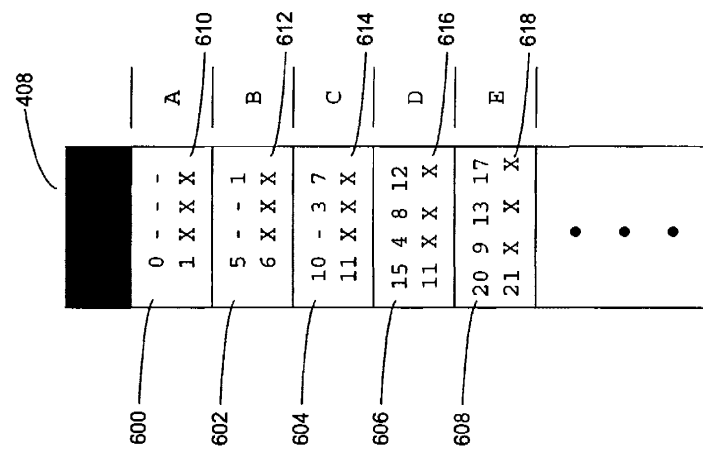


FIG. 6

DMA Parameters: Stride = 4
 Stride2 = 4 + 3 = 7
 Offset = 0
 Offset INC = 4
 Offset Mod = 5

FIG. 7

DMA Address Sequence:

<u>Step</u>	<u>Offset</u>	<u>Address</u>
0	0	A
1	4	A+4
2	3	A+11
3	2	A+18
4	1	A+25

FIG. 8

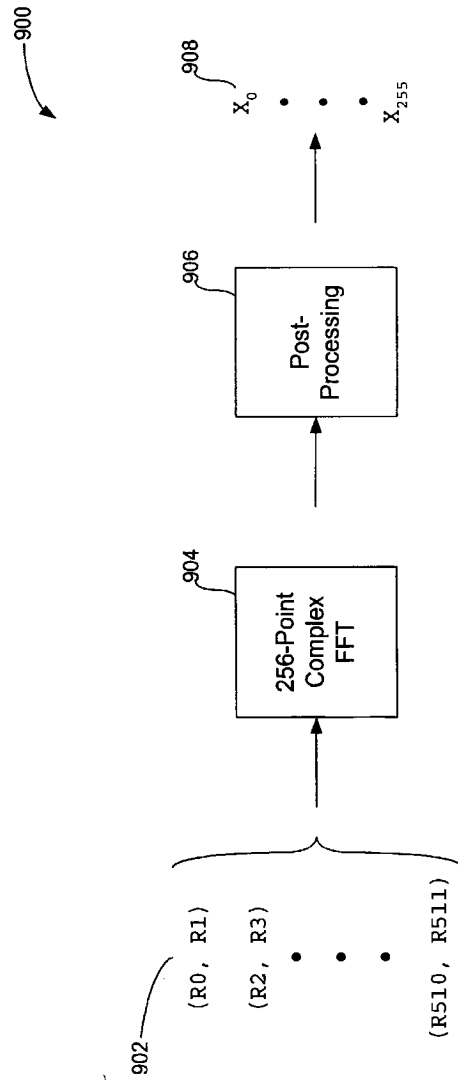


FIG. 9
(conventional)

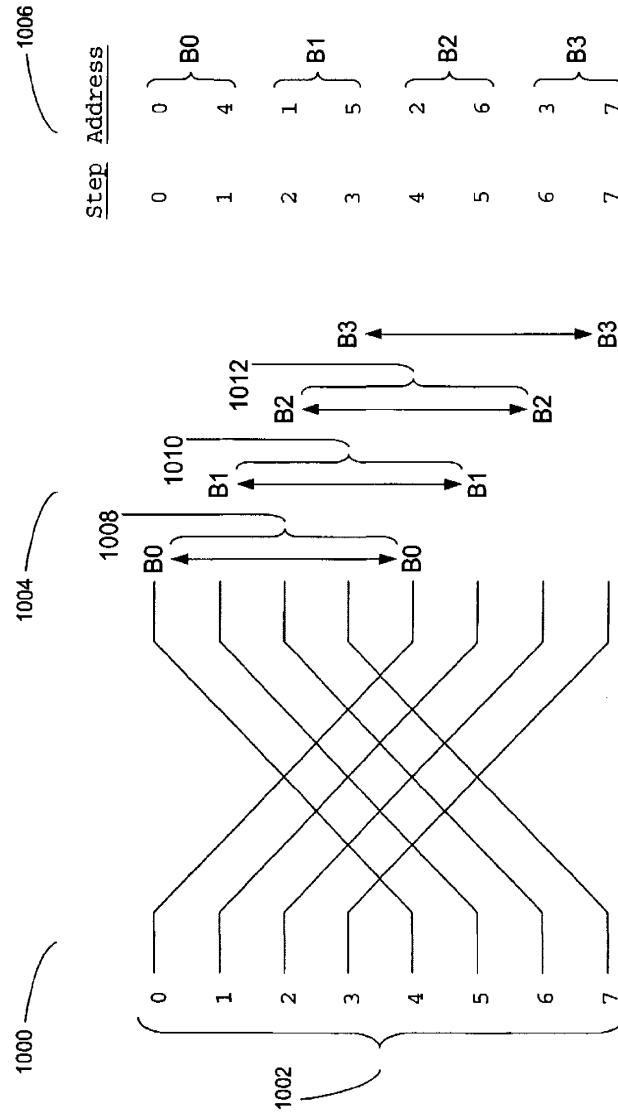


FIG. 10
(conventional)

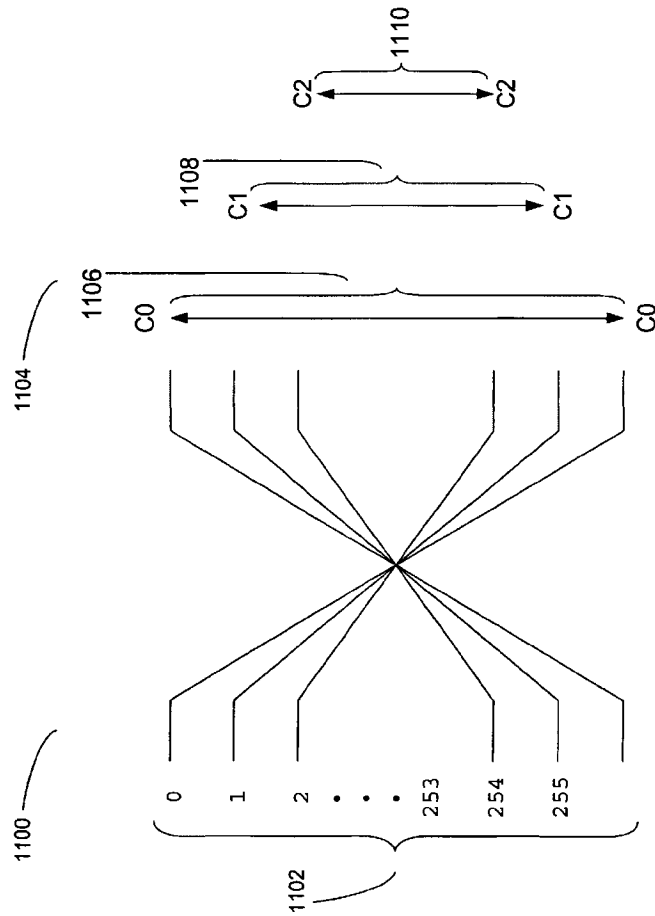
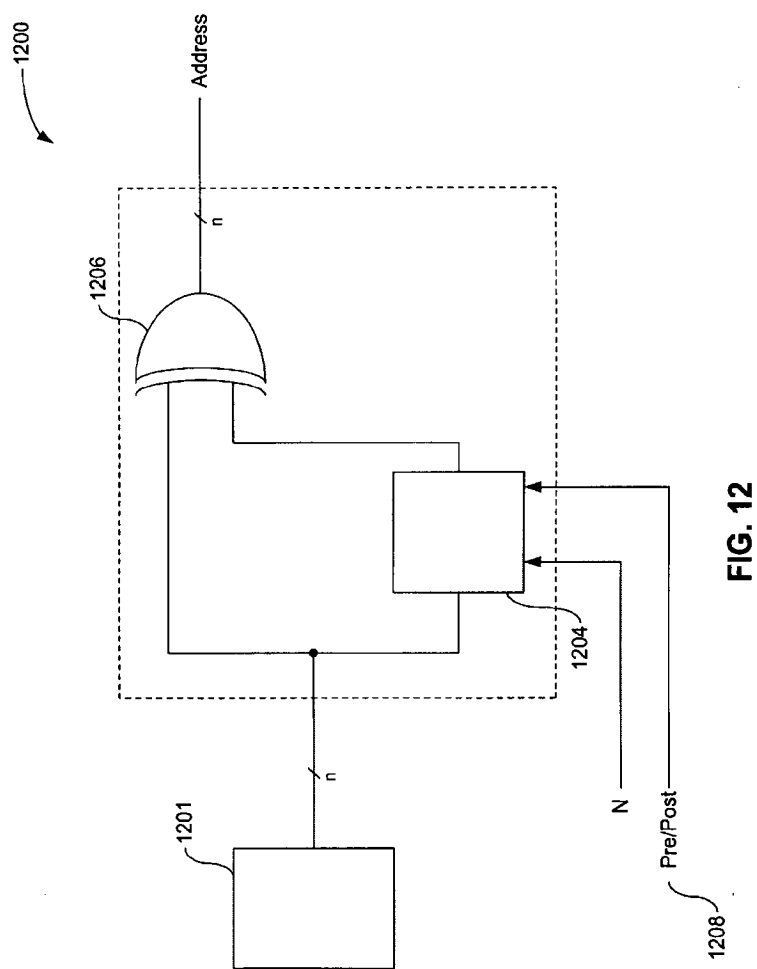


FIG. 11
(conventional)



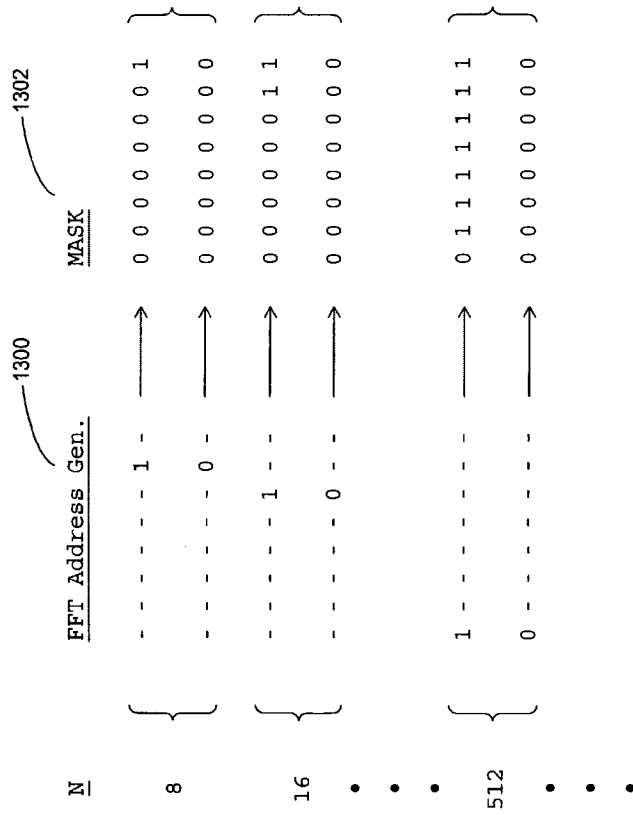


FIG. 13

STEP	1402		1404
	FFT Address Gen.	Conditionally Inverted Address	
2	1	1	
3	128	255	
4	2	2	
5	127	254	
6	3	3	
7	130	253	
•			
•			
•			
254	127	127	
255	254	129	

FIG. 14

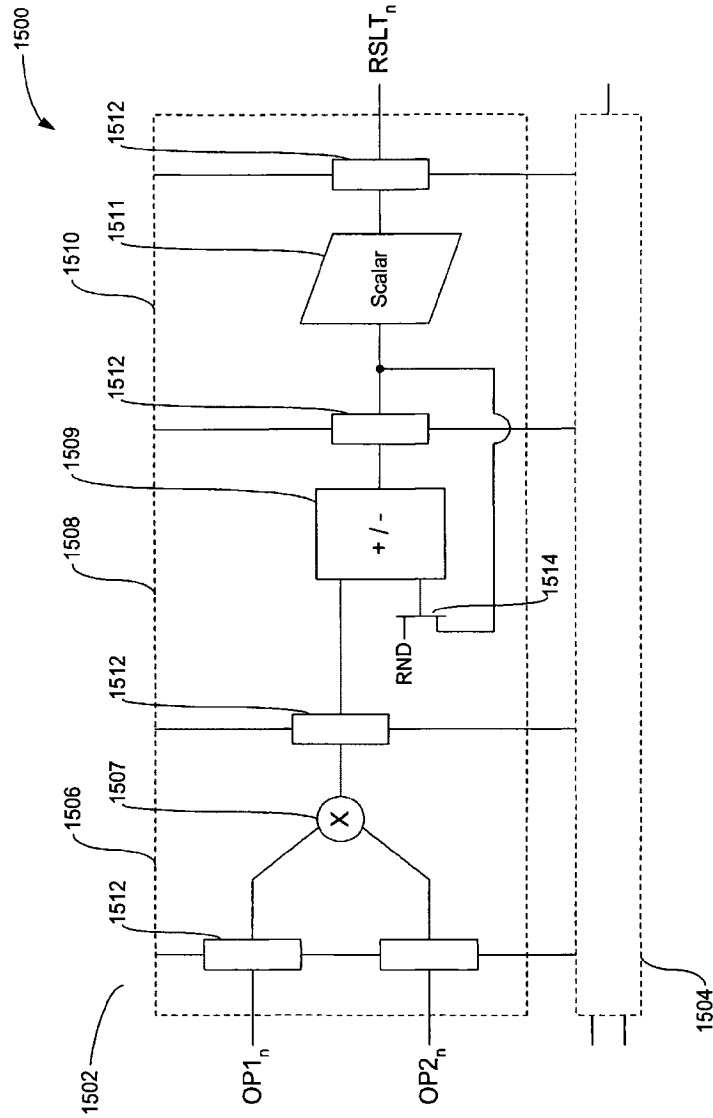


FIG. 15
(conventional)

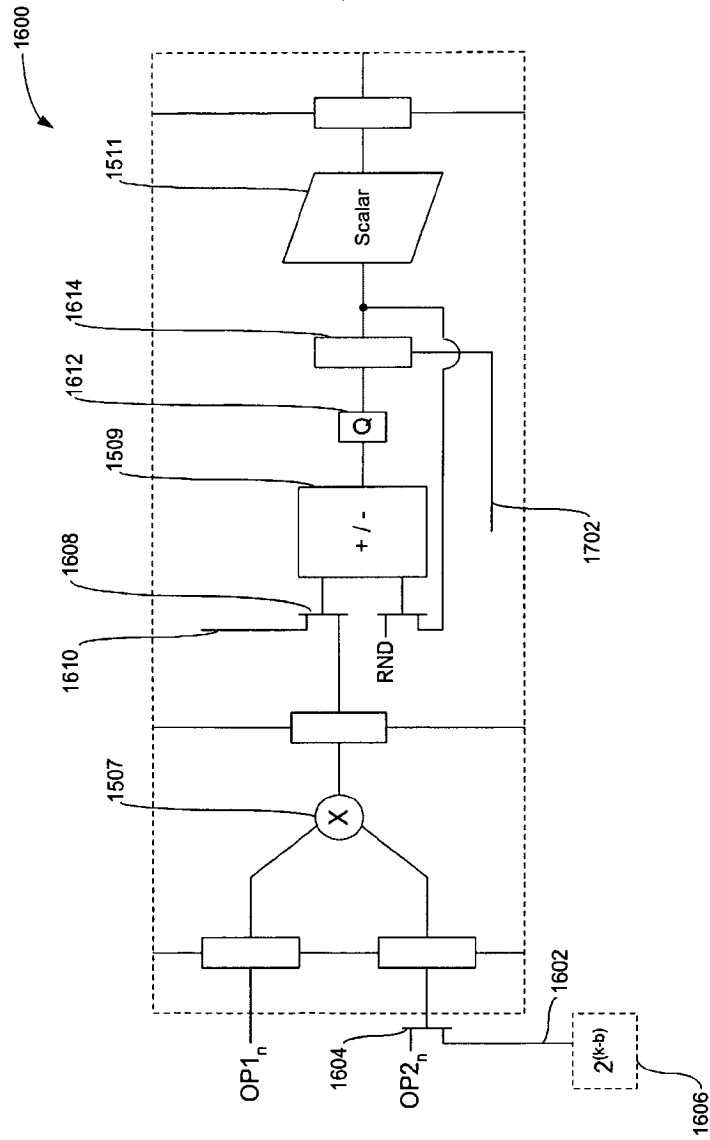


FIG. 16

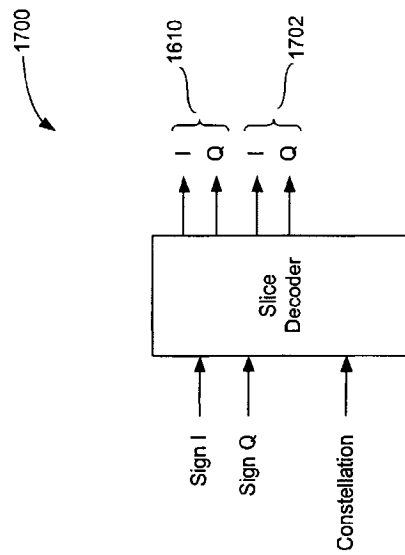


FIG. 17

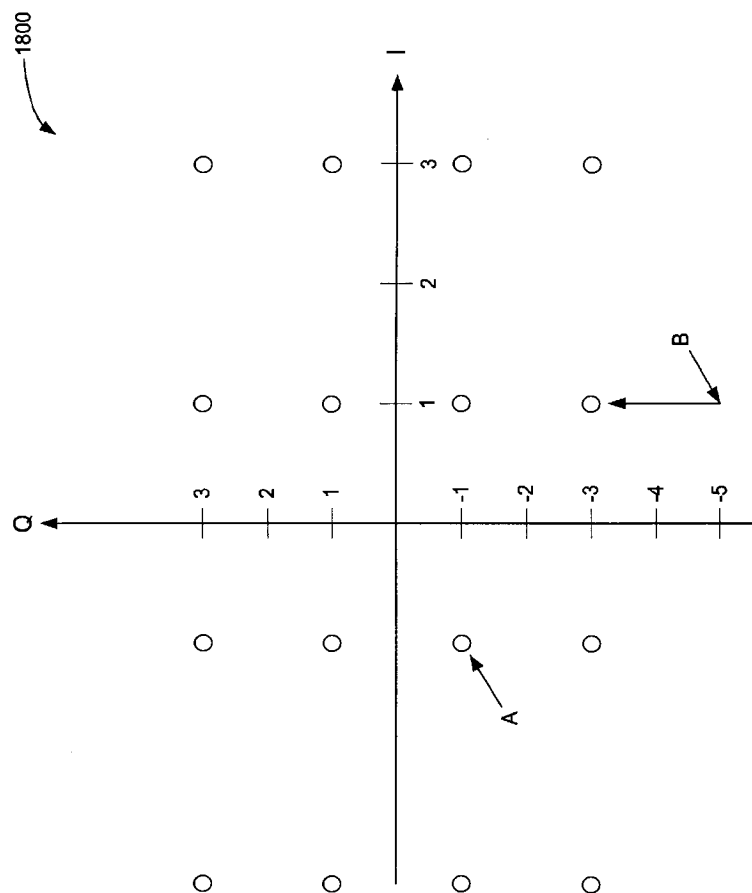


FIG. 18

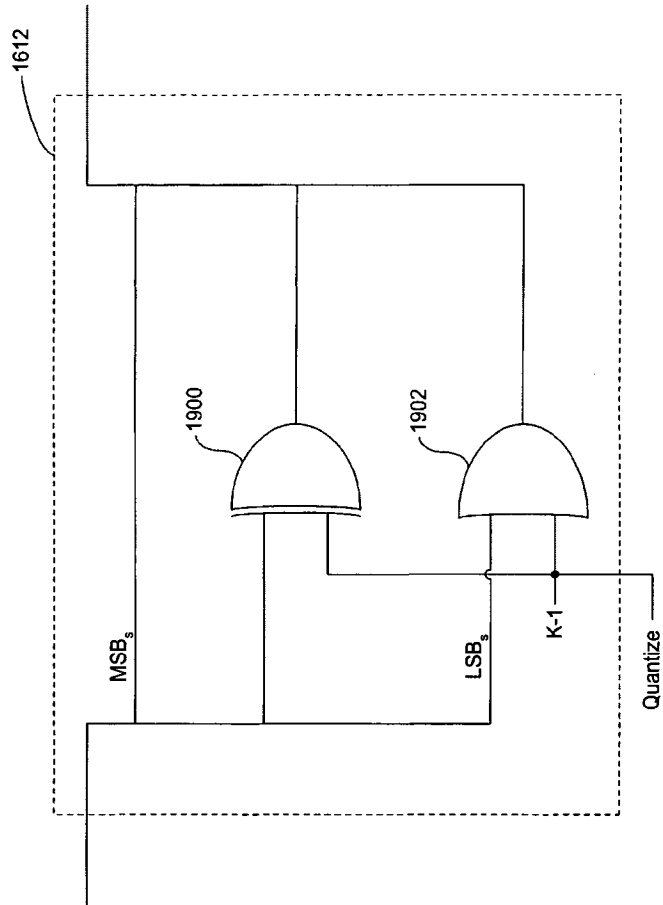


FIG. 19

		<u>Cycle</u>	<u>Quantize</u>	<u>I Limit</u>	<u>I Condition</u>	<u>Q Limit</u>	<u>Q Condition</u>	<u>Acc I</u>	<u>Acc Q</u>
'A'	1	Yes	-	-	-	-	-	-1	-1
	2	No	-3	<	<	-3	<	-1	-1
'B'	1	Yes	-	-	-	-	-	-1	-5
	2	No	3	≥	≥	-3	<	-1	-3

FIG. 20

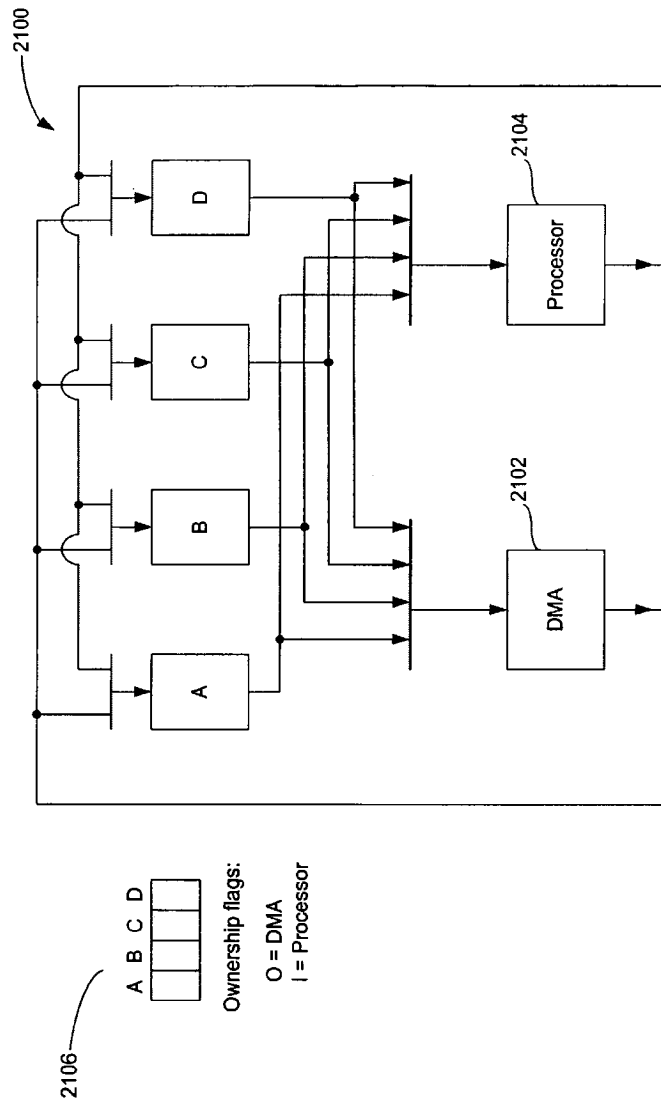


FIG. 21

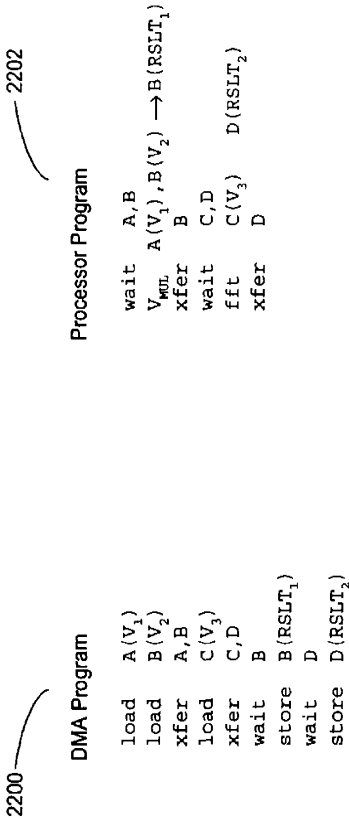


FIG. 22

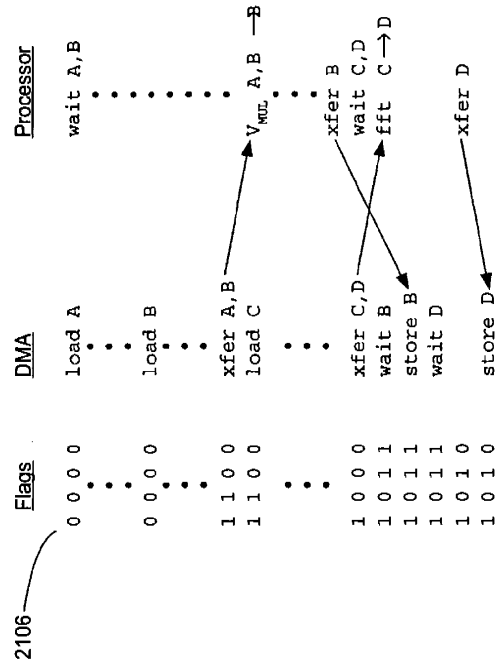


FIG. 23

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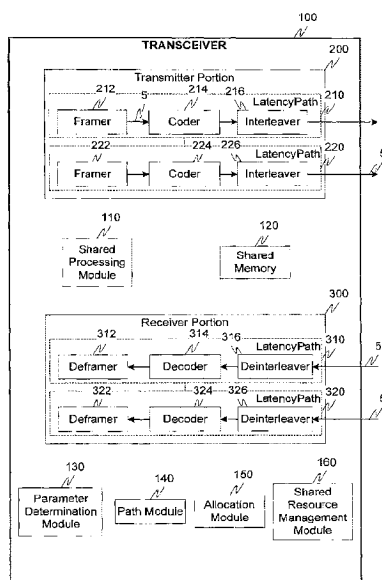
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(54) Title: RESOURCE SHARING IN A TELECOMMUNICATIONS ENVIRONMENT



(57) Abstract: A transceiver is designed to share memory and processing power amongst a plurality of transmitter and/or receiver latency paths, in a communications transceiver that carries or supports multiple applications. For example, the transmitter and/or receiver latency paths of the transceiver can share an interleaver/deinterleaver memory. This allocation can be done based on the data rate, latency, BER, impulse noise protection requirements of the application, data or information being transported over each latency path, or in general any parameter associated with the communications system.

WO 2006/044227 A1



For two-letter codes and other abbreviations, refer to the "Guidance Notes on Codes and Abbreviations" appearing at the beginning of each regular issue of the PCT Gazette.

RESOURCE SHARING IN A TELECOMMUNICATIONS ENVIRONMENTRELATED APPLICATION DATA

[0001] This application claims the benefit of and priority under 35 U.S.C. § 119(e) to U.S. Patent Application No. 60/618,269, filed October 12, 2004, entitled “Sharing Memory and Processing Resources in DSL Systems,” which is incorporated herein by reference in its entirety.

BACKGROUNDField of the Invention

[0002] This invention generally relates to communication systems. More specifically, an exemplary embodiment of this invention relates to memory sharing in communication systems. Another exemplary embodiment relates to processing or coding resource sharing in a communication system.

Description of Related Art

[0003] U.S. Patent Nos. 6,775,320 and 6,778,589, which are both incorporated herein by reference in their entirety, describe DSL systems supporting multiple applications and multiple framer/coder/interleaver FCI blocks (an FCI block is also referred to as a latency path). DSL systems carry applications that have different transmission requirements with regard to, for example, data rate, latency (delay), bit error rate (BER), and the like. For example, video typically requires a low BER ($<1\text{E-}10$) but can tolerate higher latency (>20 ms). Voice, on the other hand, typically requires a low latency (<1 ms) but can tolerate BER ($>1\text{E-}3$).

[0004] As described in U.S. Patent No. 6,775,320, different applications can use different latency paths in order to satisfy the different application requirements of the communication system. As a result a transceiver must support multiple latency paths in order to support applications such as video, Internet access and voice telephony. When implemented in a transceiver, each of the latency paths will have a framer, coder, and interleaver block with different capabilities that depend on the application requirements.

SUMMARY

[0005] One difficulty with implementing multiple latency paths in a transceiver is the fact that a latency path is a complicated digital circuit that requires a large amount of memory and processing power. An interleaver within a latency path can consume a large amount of memory in order to provide error correcting capability. For example, a typical DSL transceiver will have at least one latency path with approximately 16 kbytes of memory for the interleaver. Likewise, the coding block, for example, a Reed Solomon coder, consumes a large amount of processing power. In general, as the number of latency paths increase, the memory and processing power requirements for a communication system become larger.

[0006] Accordingly, an exemplary aspect of this invention relates to sharing memory between one or more interleavers and/or deinterleavers in a transceiver. More particularly, an exemplary aspect of this invention relates to shared latency path memory in a transceiver.

[0007] Additional aspects of this invention relate to configuring and initializing shared memory in a communication system. More particularly, an exemplary aspect of this invention relates to configuring and initializing interleaver/deinterleaver memory in a communication system.

[0008] Additional aspects of the invention relate to determining the amount of memory that can be allocated to a particular component by a communication system. More specifically, an exemplary aspect of the invention relates to determining the maximum amount of shared memory that can be allocated to one or more interleaves or deinterleavers.

[0009] According to another exemplary aspect of the invention, processing power is shared between a number of transceiver modules. More specifically, and in accordance with an exemplary embodiment of the invention, a coding module is shared between one or more coders and/or decoders.

[0010] Another exemplary embodiment of the invention relates to transitioning from a fixed memory configuration to a shared memory configuration during one or more of initialization and SHOWTIME (user data transmission).

[0011] An additional exemplary aspect of the invention relates to dynamically updating one or more of shared memory and processing resources based on changing communication conditions.

[0012] An additional exemplary aspect of the invention relates to updating one or more of shared memory and processing resources based on an updated communication parameter.

[0013] An additional exemplary aspect of the invention relates to updating the allocation of one or more of shared memory and processing resources based on an updated communication parameter(s).

[0014] Additional aspects of the invention relate to exchanging shared resource allocations between transceivers.

[0015] Additional exemplary aspects relate to a method of allocating shared memory in a transceiver comprising allocating the shared memory to a plurality of modules, wherein each of the plurality of modules comprise at least one interleaver, at least one deinterleaver or a combination thereof.

[0016] Still further aspects relate to the above method wherein the plurality of modules comprise interleavers.

[0017] Still further aspects relate to the above method wherein the plurality of modules comprise deinterleavers.

[0018] Still further aspects relate to the above method wherein the plurality of modules comprise at least one interleaver and at least one deinterleaver.

[0019] Additional exemplary aspects relate to a transceiver comprising a plurality of modules each including at least one interleaver, at least one deinterleaver or a

combination thereof and a shared memory designed to be allocated to a plurality of the modules.

[0020] Still further aspects relate to the above transceiver wherein the plurality of modules comprise interleavers.

[0021] Still further aspects relate to the above transceiver wherein the plurality of modules comprise deinterleavers.

[0022] Still further aspects relate to the above transceiver wherein the plurality of modules comprise at least one interleaver and at least one deinterleaver.

[0023] These and other features and advantages of this invention are described in, or are apparent from, the following description of the embodiments.

BRIEF DESCRIPTION OF THE DRAWINGS

[0024] The embodiments of the invention will be described in detail, with reference to the following figures, wherein:

[0025] Fig. 1 is a functional block diagram illustrating an exemplary transceiver according to this invention;

[0026] Fig. 2 is a flowchart outlining an exemplary method of sharing resources according to this invention;

[0027] Fig. 3 is a flowchart outlining an exemplary method of determining a maximum amount of shared memory according to this invention; and

[0028] Fig. 4 is a flowchart outlining an exemplary resource sharing methodology according to this invention.

DETAILED DESCRIPTION

[0029] The exemplary embodiments of this invention will be described in relation to sharing resources in a wired and/or wireless communications environment. However, it should be appreciated, that in general, the systems and methods of this invention will work equally well for any type of communication system in any environment.

[0030] The exemplary systems and methods of this invention will also be described in relation to multicarrier modems, such as DSL modems and VDSL modems, and associated communication hardware, software and communication channels. However, to avoid unnecessarily obscuring the present invention, the following description omits well-known structures and devices that may be shown in block diagram form or otherwise summarized.

[0031] For purposes of explanation, numerous details are set forth in order to provide a thorough understanding of the present invention. It should be appreciated however that the present invention may be practiced in a variety of ways beyond the specific details set forth herein.

[0032] Furthermore, while the exemplary embodiments illustrated herein show the various components of the system collocated, it is to be appreciated that the various components of the system can be located at distant portions of a distributed

network, such as a telecommunications network and/or the Internet, or within a dedicated secure, unsecured and/or encrypted system. Thus, it should be appreciated that the components of the system can be combined into one or more devices, such as a modem, or collocated on a particular node of a distributed network, such as a telecommunications network. As will be appreciated from the following description, and for reasons of computational efficiency, the components of the system can be arranged at any location within a distributed network without affecting the operation of the system. For example, the various components can be located in a Central Office modem (CO, ATU-C, VTU-O), a Customer Premises modem (CPE, ATU-R, VTU-R), a DSL management device, or some combination thereof. Similarly, one or more functional portions of the system could be distributed between a modem and an associated computing device.

[0033] Furthermore, it should be appreciated that the various links, including communications channel 5, connecting the elements can be wired or wireless links, or any combination thereof, or any other known or later developed element(s) that is capable of supplying and/or communicating data to and from the connected elements. The term module as used herein can refer to any known or later developed hardware, software, firmware, or combination thereof that is capable of performing the functionality associated with that element. The terms determine, calculate and compute, and variations thereof, as used herein are used interchangeably and include any type of methodology, process, mathematical operation or technique. FCI block and latency path are used interchangeably herein as well as transmitting modem and transmitting transceiver. Receiving modem and receiving transceiver are also used

interchangeably.

[0034] Fig. 1 illustrates an exemplary embodiment of a transceiver 100 that utilizes shared resources. It should be appreciated that numerous functional components of the transceiver have been omitted for clarity. However, the transceiver 100 can also include the standard components found in typical communications device(s) in which the technology of the subject invention is implemented into.

[0035] According to an exemplary embodiment of the invention, memory and processing power can be shared among a plurality of transmitter and/or receiver latency paths, in a communications transceiver that carries or supports multiple applications. For example, the transmitter and/or receiver latency paths of the transceiver can share an interleaver/deinterleaver memory and the shared memory can be allocated to the interleaver and/or deinterleaver of each latency path. This allocation can be done based on the data rate, latency, BER, impulse noise protection requirements of the application, data or information being transported over each latency path, or in general any parameter associated with the communications system.

[0036] Likewise, for example, the transmitter and/or receiver latency paths can share a Reed-Solomon coder/decoder processing module and the processing power of this module can be allocated to each encoder and/or decoder. This allocation can be done based on the data rate/latency, BER, impulse noise protection requirements of the application data or information being transported over each latency path, or in general based on any parameter associated with the communication system.

[0037] In accordance with an exemplary operational embodiment, a first transceiver and a second transceiver transmit to one another messages during, for example, initialization which contain information on the total and/or shared memory capabilities of each transceiver and optionally information about the one or more latency paths. This information can be transmitted prior to determining how to configure the latency paths to support the application requirements. Based on this information, one of the modems can select an FCI configuration parameter(s) that meets the transmission requirements of each application being transported over each latency paths. While an exemplary of the embodiment of the invention will be described in relation to the operation of the invention and characteristics thereof being established during initialization, it should be appreciated that the sharing of resources can be modified and messages transmitted between a two transceivers at any time during initialization and/or user data transmission, i.e., SHOWTIME.

[0038] Fig. 1 illustrates an exemplary embodiment of a transceiver 100. The transceiver 100 includes a transmitter portion 200 and a receiver portion 300. The transmitter portion 200 includes one or more latency paths 210, 220, ... Similarly, the receiver portion 300 includes one or more latency paths 310, 320, ... Each of the latency paths in the transmitter portion 200 includes a framer, coder, and interleaver designated as 212, 214, 216 and 222, 224 and 226, respectively. Each of the latency paths in the receiver portion includes a deframer, decoder, and deinterleaver designated as 312, 314, 316 and 322, 324, and 326, respectively. The transceiver 100 further includes a shared processing module 110, a shared memory 120, a parameter

determination module 130, a path module 140, an allocation module 150, and a shared resource management module 160, all interconnected by one or more links (not shown).

[0039] In this exemplary embodiment, the transceiver 100 is illustrated with four total transmitter portion and receiver portion latency paths, i.e., 210, 220, 310, and 320. The shared memory 120 is shared amongst the two transmitter portion interleavers 216 and 226 and two receiver portion deinterleavers 316 and 326. The shared processing module 110, such as a shared coding module, is shared between the two transmitter portion coders 214 and 224 and the two receiver portion decoders 314 and 324.

[0040] While the exemplary embodiment of the invention will be described in relation to a transceiver having a number of transmitter portion latency paths and receiver portion latency paths, it should be appreciated that this invention can be applied to any transceiver having any number of latency paths. Moreover, it should be appreciated that the sharing of resources can be allocated such that one or more of the transmitter portion latency paths are sharing a shared resource, one or more of the receiver portion latency paths are sharing a shared resource, or a portion of the transmitter portion latency paths and a portion of the receiver portion latency paths are sharing shared resources. Moreover, any one or more of the latency paths, or portions thereof, could also be assigned to a fixed resource while, for example, another portion of the latency path(s) assigned to a shared resource. For example, in latency path 210, the interleaver 216 could be allocated a portion of the shared

memory 120, while the coder 214 could be allocated to a dedicated processing module, vice versa, or the like.

[0041] In accordance with the exemplary embodiment, a plurality of transmitter portion or receiver portion latency paths share an interleaver/deinterleaver memory, such as shared memory 120, and a coding module, such as shared processing module 110. For example, the interleaver/deinterleaver memory can be allocated to different interleavers and/or deinterleavers. This allocation can be based on parameters associated with the communication systems such as data rate, latency, BER, impulse noise protection, and the like, of the applications being transported. Similarly, a coding module, which can be a portion of the shared processing module 110, can be shared between any one or more of the latency paths. This sharing can be based on requirements such as data rate, latency, BER, impulse noise protection, and the like, of the applications being transported.

[0042] For example, an exemplary transceiver could comprise a shared interleaver/deinterleaver memory and could be designed to allocate a first portion of the shared memory 120 to an interleaver, such as interleaver 216 in the transmitter portion of the transceiver and allocate a second portion of the shared memory 120 to a deinterleaver, such as 316, in the receiver portion of the transceiver.

[0043] Alternatively, for example, an exemplary transceiver can comprise a shared interleaver/deinterleaver memory, such as shared memory 120, and be designed to allocate a first portion of shared memory 120 to a first interleaver, e.g.,

216, in the transmitter portion of the transceiver and allocate a second portion of the shared memory to a second interleaver, e.g., 226, in the transmitter portion of the transceiver.

[0044] Alternatively, for example, an exemplary transceiver can comprise a shared interleaver/deinterleaver memory and be designed to allocate a first portion of the shared memory 120 to a first deinterleaver, e.g., 316, in the receiver portion of the transceiver and allocate a second portion of the shared memory to a second deinterleaver, e.g., 326, in the receiver portion of the transceiver. Regardless of the configuration, in general any interleaver or deinterleaver, or grouping thereof, be it in a transmitter portion or receiver portion of the transceiver, can be associated with a portion of the shared memory 120.

[0045] Establishment, configuration and usage of shared resources is performed in the following exemplary manner. First, and in cooperation with the path module 140, the number of transmitter and receiver latency paths (N) is determined. The parameter determination module 130 then analyses one or more parameters such as data rate, transmitter data rate, receiver data rate, impulse noise protection, bit error rate, latency, or the like. Based on one or more of these parameters, the allocation module 150 allocates a portion of the shared memory 120 to one or more of the interleaver and/or deinterleavers, or groupings thereof. This process continues until the memory allocation has been determined and assigned to each of the N latency paths.

[0046] Having determined the memory allocation for each of the latency paths, and in conjunction with the shared resource management 160, the transceiver 100 transmits to a second transceiver one or more of the number of latency paths (N), the maximum interleaver memory for any one or more of the latency paths and/or the maximum total and/or shared memory for all of the latency paths.

[0047] Three examples of sharing interleaver/deinterleaver memory and coding processing in a transceiver are described below. The latency paths in these examples can be in the transmitter portion of the transceiver or the receiver portion of the transceiver.

[0048] Example #1

A first transmitter portion or receiver portion latency path may carry data from a video application, which needs a very low BER but can tolerate higher latency. In this case, the video will be transported using an latency path that has a large amount of interleaving/deinterleaving and coding (also known as Forward Error Correction (FEC) coding). For example, the latency path may be configured with Reed-Solomon coding using a codeword size of 255 bytes ($N=255$) with 16 checkbytes ($R=16$) and interleaving/deinterleaving using an interleaver depth of 64 ($D=64$). This latency path will require $N \cdot D = 16 \cdot 255 = 16\text{Kbytes}$ of interleaver memory at the transmitter (or de-interleaver memory at the receiver). This latency path will be able to correct a burst of errors that is less than 512 bytes in duration.

[0049] A second transmitter portion or receiver portion latency path may carry an

internet access application that requires a medium BER and a medium amount of latency. In this case, the internet access application will be transported using a latency path that has a medium amount of interleaving and coding. For example, the latency path may be configured with Reed-Solomon coding using a codeword size of 128 bytes ($N=128$) with 8 checkbytes ($R=8$) and interleaving using an interleaver depth of 16 ($D=32$). This latency path will require $N*D=128*32=4$ Kbytes of interleaver memory and the same amount of deinterleaver memory. This latency path will be able to correct a burst of errors that is less than 128 bytes in duration.

[0050] A third transmitter portion or receiver portion latency path may carry a voice telephony application, which needs a very low latency but can tolerate BER. In this case, the video will be transported using an latency path that has a large amount of interleaving and coding. For example, the third transmitter portion or receiver portion latency path may be configured with no interleaving or coding which will result in the lowest possible latency through the latency path but will provide no error correction capability.

[0051] According to the principles of this invention, a system carrying the three applications described above in Example #1, would have three latency paths that share one memory space containing at least $(16+4)=20$ Kbytes. The three latency paths also share a common coding block that is able to simultaneously encode (in the transmitter portion) or decode (in a receiver portion) two codewords with $N=255/R=16$ and $N=128/R=8$.

[0052] According to an exemplary embodiment of this invention, the latency paths can be reconfigured at initialization or during data transmission mode (also known as SHOWTIME in ADSL and VDSL transceivers). This would occur if, for example, the applications or application requirements were to change.

[0053] Example #2

If instead of 1 video application, 1 internet application and 1 voice application, there were 3 internet access applications then the transmitter portion and/or receiver portion latency paths would be reconfigured to utilize the shared memory and coding module in a different way. For example, the system could be reconfigured to have 3 transmitter portion or receiver portion latency paths, with each latency path being configured with Reed-Solomon coding using a codeword size of 128 bytes ($N=128$) with 8 checkbytes ($R=8$) and interleaving using an interleaver depth of 16 ($D=32$). Each latency path will require $N*D=128*32=4$ Kbytes of interleaver memory and each block will be able to correct a burst of errors that is less than 128 bytes in duration. Based on the example of carrying the three internet access applications described, the three latency path share one memory space containing at least $3*4=12$ Kbytes. Also the three latency paths share a common coding block that is able to simultaneously encode (on the transmitter side) or decode (on the receiver side) three codewords with $N=128/R=16$, $N=128/R=8$ and $N=128/R=8$.

[0054] Example #3

The system could be configured to carry yet another set of applications. For example, the latency paths could be configured to carry 2 video applications. In this case only

2 transmitter portion or receiver portion latency paths are needed, which means that the third latency path could be simply disabled. Also, assuming that the memory is constrained based on the first example above, then the maximum shared memory for these 2 latency paths is 20 kBytes. In this case, the system could be reconfigured to have 2 latency paths, with each block being configured with Reed-Solomon coding using a codeword size of 200 bytes ($N=200$) with 10 checkbytes ($R=10$) and interleaving/deinterleaving using an interleaver depth of 50 ($D=50$). Each latency path will require $N*D=200*50=10\text{Kbytes}$ of interleaver memory and each block will be able to correct a burst of errors that is less than 250 bytes in duration. This configuration results in 20K of shared memory for both latency paths, which is the same as in the first example. In order to stay within the memory constraints of the latency paths, the error correction capability for each latency path is decreased to 250 bytes from 512 bytes in Example #1.

[0055] Another aspect of this invention is the how FCI configuration information is transmitted between a first modem and a second modem. FCI configuration information will depend on the requirements of the applications being transported over the DSL connection. This information may need to be forwarded during initialization in order to initially configure the DSL connection. This information may also need to be forwarded during SHOWTIME in order to reconfigure the DSL connection based on a change in applications or the application requirements.

[0056] According to one embodiment, a first modem determines the specific FCI configuration parameters, e.g., N , D , R as defined above, needed to meet specific

application requirements, such as latency, burst error correction capability, etc. In order to determine the FCI configuration parameters, the first modem must know what are the capabilities of a second modem. For example, the first modem must know how many latency paths (FCI blocks) the second modem can support. Also the first modem must know the maximum amount of interleaver memory for each transmitter latency path. In addition, since the transmitter latency paths may share a common memory space the first modem must know the total shared memory for all transmitter latency paths. This way the first modem will be able to choose a configuration that can meet application requirements and also meet the transmitter portion latency path capabilities of the second modem.

[0057] For example, using values from examples above, a first transceiver could send a message to a second transceiver during initialization or during SHOWTIME containing the following information:

- Number of supported transmitter and receiver latency paths = 3
- Max Interleaver Memory for latency path #1= 16 Kbytes
- Max Interleaver Memory for latency path #2= 16 Kbytes
- Max Interleaver Memory for latency path #3= 16 Kbytes
- Maximum total/shared memory for all latency paths = 20 kBytes

Based on this information, and the application requirements, the first transceiver would select latency path settings. For example, if the applications are 1 video, 1 internet access and 1 voice application, the first transceiver could configure 3 latency paths as follows:

latency path #1 – Video: N=255, R=16, D=64

latency path #2 – Video: N=128, R=8, D=32

latency path #3 – Video: N=0, R=0, D=1 (no coding or interleaving)

[0058] This would result in a total interleaver memory of 20 kbytes.

[0059] Alternatively, if for example, there are only 2 video applications, the first transceiver could configure 2 latency paths as follows:

latency path #1 – Video: N=200, R=10, D=50

latency path #2 – Video: N=200, R=10, D=50

latency path #3 – Video: N=0, R=0, D=1 (no coding or interleaving)

[0060] This would also result in a total interleaver memory of 20 kbytes.

[0061] Alternatively, the second transceiver can determine the specific FCI configuration parameters, e.g., N, D, R as defined above, needed to meet specific application requirements, such as latency, burst error correction capability, etc. As described above for the first transceiver, in order to determine the FCI configuration parameters, the second transceiver must first know what are the capabilities of the first transceiver. In this case, the first transceiver would send a message to the second transceiver containing the information described above and based on this information and the application requirements the second transceiver would select latency path settings.

[0062] Fig. 2 outlines an exemplary method of allocating shared memory in a transceiver. More specifically, control begins in step S200 and continues to step S210. In step S210, one or more of shared interleaver/deinterleaver memory and/or shared coder/decoder processing resources are allocated to one or more latency paths, in a transceiver. Control then continues to step S220 where the control sequence ends.

[0063] Fig. 3 outlines an exemplary method of exchanging shared resource allocations according to an exemplary embodiment of this invention. In particular, control begins in step S310. In step S310, a maximum amount of shared memory that can be allocated to a specific interleaver or deinterleaver of a plurality of interleavers or deinterleavers in a transceiver is determined. Next, in step S320, the determined maximum amount for one or more of the deinterleavers and/or interleavers is transmitted to another transceiver. Messages containing additional information can also be transmitted to the other transceiver and/or received from the other transceiver. Control then continues to step S330 where the control sequence ends.

[0064] Fig. 4 outlines an exemplary procedure for resource sharing according to an exemplary embodiment of this invention. In particular, control begins in step S400 and continues to step S410. In step S410, the number of latency paths are determined. Then, in step S420, the latency path information (FCI block information) is transmitted to another transceiver. Messages containing additional information can also be transmitted to the other transceiver and/or received from the other transceiver. This information can be used to, for example, assist with the determination of

memory allocation in the transceiver. Moreover, the messages received from the other transceiver could specify what the memory allocation is to be based on, for example, the number of latency paths, memory allocation in the remote transceiver and required applications. Control then continues to step S430.

[0065] In step S430, and for each latency path, the steps in step 440 are performed.

[0066] In step S440, and while monitoring of allocation of resources is being performed, steps 450 and 460 are performed. More specifically, in step S450, one or more parameters associated with the communication system are determined. Then, in step S460, shared resources are allocated based on one or more of the communication parameters. Control then continues to step S470.

[0067] In step S470, the allocation of shared resources is communicated to another transceiver. Next, in step S480, a determination is made as to whether there is a change in communications that would require the adjustment of the shared resource allocation. Examples of changes in communications conditions include a change in applications being transported over the system and/or changes in the channel condition, etc. If adjustments are required, control jumps back to step S410. Otherwise, control jumps to step S490 where the control sequence ends.

[0068] The above-described system can be implemented on wired and/or wireless telecommunications devices, such a modem, a multicarrier modem, a DSL modem, an

ADSL modem, an XDSL modem, a VDSL modem, a linecard, test equipment, a multicarrier transceiver, a wired and/or wireless wide/local area network system, a satellite communication system, a modem equipped with diagnostic capabilities, or the like, or on a separate programmed general purpose computer having a communications device or in conjunction with any of the following communications protocols: CDSL, ADSL2, ADSL2+, VDSL1, VDSL2, HDSL, DSL Lite, IDSL, RADSL, SDSL, UDSL or the like.

[0069] Additionally, the systems, methods and protocols of this invention can be implemented on a special purpose computer, a programmed microprocessor or microcontroller and peripheral integrated circuit element(s), an ASIC or other integrated circuit, a digital signal processor, a hard-wired electronic or logic circuit such as discrete element circuit, a programmable logic device such as PLD, PLA, FPGA, PAL, a modem, a transmitter/receiver, any comparable means, or the like. In general, any device capable of implementing a state machine that is in turn capable of implementing the methodology illustrated herein can be used to implement the various communication methods, protocols and techniques according to this invention.

[0070] Furthermore, the disclosed methods may be readily implemented in software using object or object-oriented software development environments that provide portable source code that can be used on a variety of computer or workstation platforms. Alternatively, the disclosed system may be implemented partially or fully in hardware using standard logic circuits or VLSI design. Whether software or

hardware is used to implement the systems in accordance with this invention is dependent on the speed and/or efficiency requirements of the system, the particular function, and the particular software or hardware systems or microprocessor or microcomputer systems being utilized. The communication systems, methods and protocols illustrated herein can be readily implemented in hardware and/or software using any known or later developed systems or structures, devices and/or software by those of ordinary skill in the applicable art from the functional description provided herein and with a general basic knowledge of the computer and telecommunications arts.

[0071] Moreover, the disclosed methods may be readily implemented in software that can be stored on a storage medium, executed on programmed general-purpose computer with the cooperation of a controller and memory, a special purpose computer, a microprocessor, or the like. In these instances, the systems and methods of this invention can be implemented as program embedded on personal computer such as an applet, JAVA® or CGI script, as a resource residing on a server or computer workstation, as a routine embedded in a dedicated communication system or system component, or the like. The system can also be implemented by physically incorporating the system and/or method into a software and/or hardware system, such as the hardware and software systems of a communications transceiver.

[0072] It is therefore apparent that there has been provided, in accordance with the present invention, systems and methods for sharing resources. While this invention has been described in conjunction with a number of embodiments, it is

evident that many alternatives, modifications and variations would be or are apparent to those of ordinary skill in the applicable arts. Accordingly, it is intended to embrace all such alternatives, modifications, equivalents and variations that are within the spirit and scope of this invention.

Claims:

1. A method for sharing resources in a transceiver comprising:
allocating a first portion of shared memory to a first latency path and
allocating a second portion of the shared memory to a second latency path.
2. The method of claim 1, wherein the first latency path includes an interleaver and the second latency path includes an interleaver.
3. The method of claim 1, wherein the first latency path includes an interleaver and the second latency path includes a deinterleaver.
4. The method of claim 1, wherein the first latency path includes a deinterleaver and the second latency path includes a deinterleaver.
5. The method of claim 1, further comprising transmitting to another transceiver information that is used to determine a maximum amount of shared memory that can be allocated.
6. The method of claim 1, further comprising receiving from another transceiver information that is used to determine a maximum amount of shared memory that can be allocated.
7. The method of claim 1, further comprising allocating a shared processing module to a plurality of coding and/or decoding modules.
8. The method of claim 1, wherein the allocating of at least one portion of the shared memory is based on one or more communication parameters.
9. The method of claim 8, wherein at least one of the communication parameters is a data rate, a latency, an INP value or a bit error rate (BER).

10. A transceiver comprising:
a first portion of shared memory that is allocated to a first latency path;
and
a second portion of the shared memory that is allocated to a second latency path.
11. The transceiver of claim 10, further comprising:
an allocation module designed to allocate the shared memory based on one or more communication parameters.
12. The transceiver of claim 11, wherein at least one of the communication parameters is a data rate, a latency, an INP value or a Bit Error Rate (BER).
13. The transceiver of claim 10, wherein the first latency path includes an interleaver and the second latency path includes an interleaver.
14. The transceiver of claim 10, wherein the first latency path includes an interleaver and the second latency path includes a deinterleaver.
15. The transceiver of claim 10, wherein the first latency path includes a deinterleaver and the second latency path includes a deinterleaver.
16. The transceiver of claim 10, further comprising a shared resource management module designed to determine information that is transmitted to another transceiver, wherein the information is used to determine a maximum amount of shared memory that can be allocated.
17. The transceiver of claim 10, further comprising a shared resource management module designed to utilize information that is received from another transceiver, wherein the information is used to determine a maximum amount of shared memory that can be allocated.

18. The transceiver of claim 10, further comprising a shared processing module designed to provide processing resources to a plurality of coding and/or decoding modules.
19. A system for sharing resources in a transceiver comprising:
means for allocating a first portion of shared memory to a first latency path and means for allocating a second portion of the shared memory to a second latency path.
20. The system of claim 19, wherein the first latency path includes an interleaver and the second latency path includes an interleaver.
21. The system of claim 19, wherein the first latency path includes an interleaver and the second latency path includes a deinterleaver.
22. The system of claim 19, wherein the first latency path includes a deinterleaver and the second latency path includes a deinterleaver.
23. The system of claim 19, further comprising means for transmitting to another transceiver information that is used to determine a maximum amount of shared memory that can be allocated.
24. The system of claim 19, further comprising means for receiving from another transceiver information that is used to determine a maximum amount of shared memory that can be allocated.
25. The system of claim 19, further comprising means for allocating a shared processing module to a plurality of coding and/or decoding modules.
26. The system of claim 19, wherein the allocating of at least one portion

of the shared memory is based on one or more communication parameters.

27. The system of claim 26, wherein at least one of the communication parameters is a data rate, a latency, an INP value or a bit error rate (BER).

28. A protocol for sharing resources in a transceiver comprising:
allocating a first portion of shared memory to a first latency path and
allocating a second portion of the shared memory to a second latency path.

29. The protocol of claim 28, wherein the first latency path includes an interleaver and the second latency path includes an interleaver.

30. The protocol of claim 28, wherein the first latency path includes an interleaver and the second latency path includes a deinterleaver.

31. The protocol of claim 28, wherein the first latency path includes a deinterleaver and the second latency path includes a deinterleaver.

32. The protocol of claim 28, further comprising transmitting to another transceiver information that is used to determine a maximum amount of shared memory that can be allocated.

33. The protocol of claim 28, further comprising receiving from another transceiver information that is used to determine a maximum amount of shared memory that can be allocated.

34. The protocol of claim 28, further comprising allocating a shared processing module to a plurality of coding and/or decoding modules.

35. The protocol of claim 28, wherein the allocating of at least one portion of the shared memory is based on one or more communication parameters.

36. The protocol of claim 35, wherein at least one of the communication parameters is a data rate, a latency, an INP value or a bit error rate (BER).

37. An information storage media having stored thereon information that when executed allows sharing of resources in a transceiver comprising:

information that allocates a first portion of shared memory to a first latency path and information that allocates a second portion of the shared memory to a second latency path.

38. The media of claim 37, wherein the first latency path includes an interleaver and the second latency path includes an interleaver.

39. The media of claim 37, wherein the first latency path includes an interleaver and the second latency path includes a deinterleaver.

40. The media of claim 37, wherein the first latency path includes a deinterleaver and the second latency path includes a deinterleaver.

41. The media of claim 37, further comprising information that transmits to another transceiver information that is used to determine a maximum amount of shared memory that can be allocated.

42. The media of claim 37, further comprising information that receives from another transceiver information that is used to determine a maximum amount of shared memory that can be allocated.

43. The media of claim 37, further comprising information that allocates a shared processing module to a plurality of coding and/or decoding modules.

44. The media of claim 37, wherein the allocating of at least one portion of

the shared memory is based on one or more communication parameters.

45. The media of claim 44, wherein at least one of the communication parameters is a data rate, a latency, an INP value or a bit error rate (BER).

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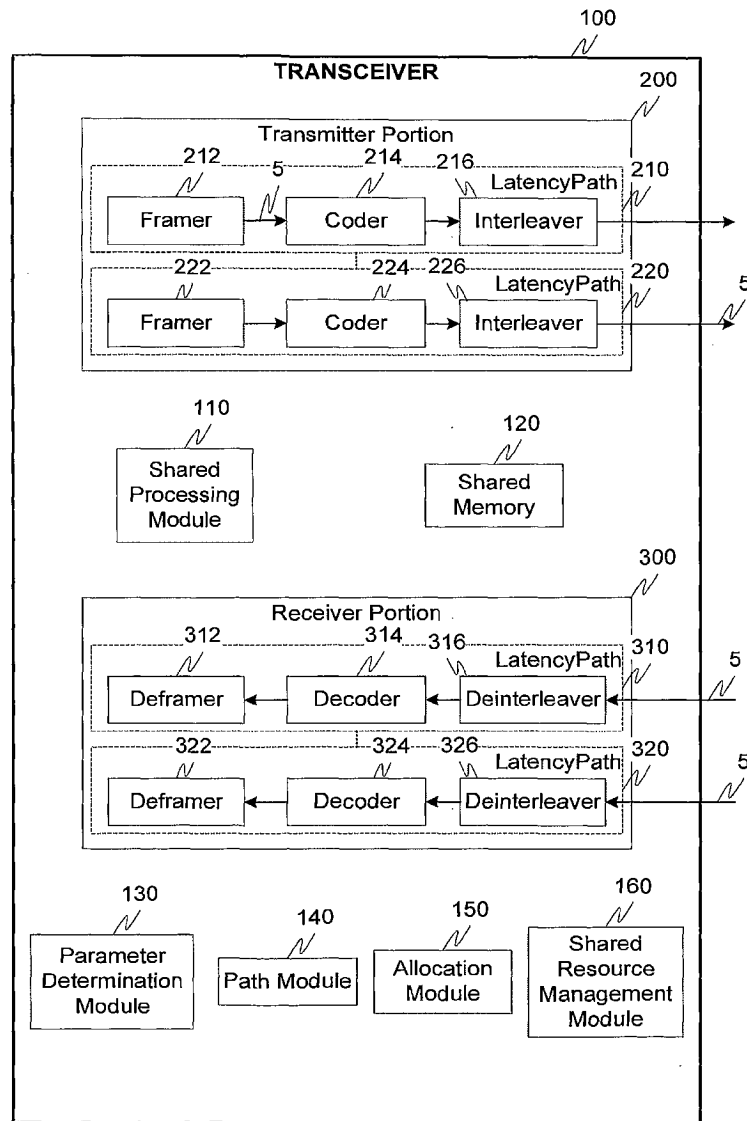


Fig. 1

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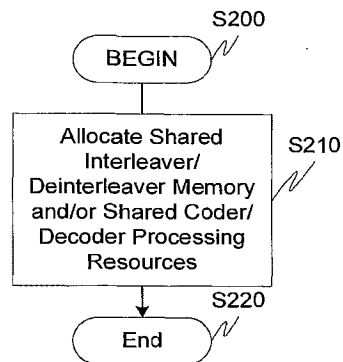


Fig. 2

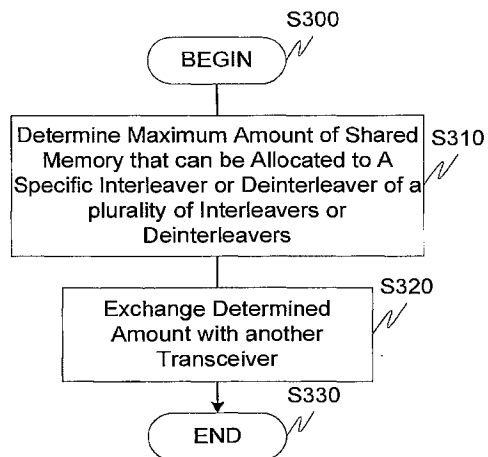


Fig. 3

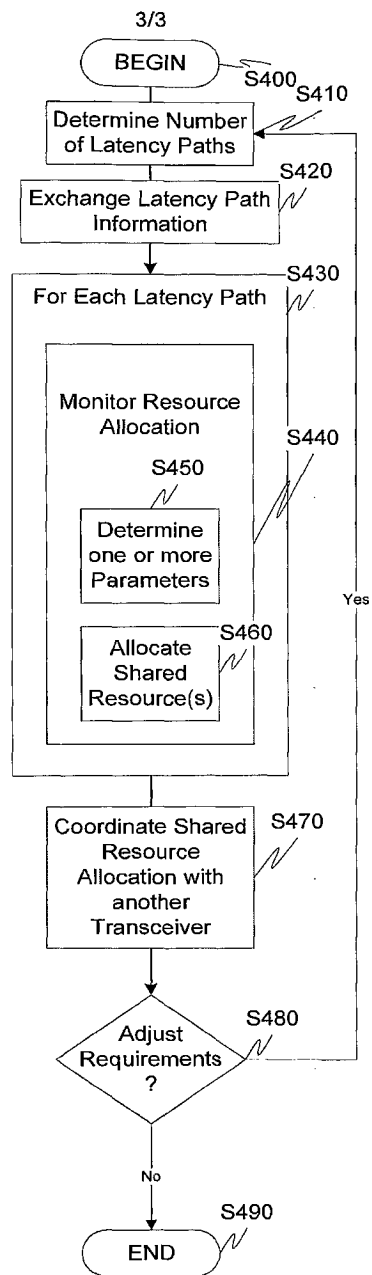


Fig. 4

INTERNATIONAL SEARCH REPORT

International application No
PCT/US2005/036015

A. CLASSIFICATION OF SUBJECT MATTER H04L1/00 H04L27/26		
According to International Patent Classification (IPC) or to both national classification and IPC		
B. FIELDS SEARCHED Minimum documentation searched (classification system followed by classification symbols) H04L		
Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched		
Electronic data base consulted during the International search (name of data base and, where practical, search terms used) EPO-Internal, WPI Data		
C. DOCUMENTS CONSIDERED TO BE RELEVANT		
Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	US 6 707 822 B1 (FADAVI-ARDEKANI JALIL ET AL) 16 March 2004 (2004-03-16) column 1, line 7 - column 2, line 59 column 3, line 5 - column 4, line 21 column 5, line 23 - column 7, line 33 column 8, line 4 - column 9, line 23 figure 2	1-45
A	WO 03/063060 A (BROADCOM CORPORATION) 31 July 2003 (2003-07-31) page 1, line 5 - page 2, line 27 page 17, line 4 - page 18, line 25 figures 1,4 page 7, line 13 - page 9, line 16 ----- -/--	1-45
☒ Further documents are listed in the continuation of Box C. ☒ See patent family annex.		
* Special categories of cited documents : * A* document defining the general state of the art which is not considered to be of particular relevance * E* earlier document but published on or after the international filing date * L* document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified) * O* document referring to an oral disclosure, use, exhibition or other means * P* document published prior to the international filing date but later than the priority date claimed * T* later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention * X* document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone * Y* document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art. * &* document member of the same patent family		
Date of the actual completion of the international search 18 January 2006		Date of mailing of the international search report 08/02/2006
Name and mailing address of the ISA/ European Patent Office, P.B. 5818 Patentlaan 2 NL - 2280 LV Rijswijk Tel. (+31-70) 340-2040, Tx. 31 651 epo nl, Fax: (+31-70) 340-3016		Authorized officer Marzenke, M

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page 1 of 2

INTERNATIONAL SEARCH REPORT

International application No
PCT/US2005/036015

C(Continuation). DOCUMENTS CONSIDERED TO BE RELEVANT		
Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
A	US 6 337 877 B1 (COLE TERRY L ET AL) 8 January 2002 (2002-01-08) column 3, line 21 - column 4, line 29 column 7, line 49 - column 8, line 67 figures 3,10	1-45
A	"SunSet xDSL: Prequalification of ADSL Circuits with ATU-C Emulation" 2001, SUNRISE TELECOM INC., APPLICATION SERIES , SAN JOSE, USA , XP002363272 Retrieved from the Internet: URL:http://www.sunrisetelecom.com/technote s/APP-xDSL-8B.pdf> 'retrieved on 2006-01-17! page 3, right-hand column, paragraph 1	1-45

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page 2 of 2

INTERNATIONAL SEARCH REPORT

Information on patent family members

International application No

PCT/US2005/036015

Patent document cited in search report		Publication date	Patent family member(s)	Publication date
US 6707822	B1	16-03-2004	NONE	
WO 03063060	A	31-07-2003	EP 1476978 A2	17-11-2004
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			WO 0013387 A1	09-03-2000

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INTERNATIONAL SEARCH REPORT

International application No
PCT/US2005/036015

A. CLASSIFICATION OF SUBJECT MATTER H04L1/00 H04L27/26		
According to International Patent Classification (IPC) or to both national classification and IPC		
B. FIELDS SEARCHED		
Minimum documentation searched (classification system followed by classification symbols) H04L		
Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched		
Electronic data base consulted during the international search (name of data base and, where practical, search terms used) EPO-Internal, WPI Data		
C. DOCUMENTS CONSIDERED TO BE RELEVANT		
Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	US 6 707 822 B1 (FADAVI-ARDEKANI JALIL ET AL) 16 March 2004 (2004-03-16) column 1, line 7 - column 2, line 59 column 3, line 5 - column 4, line 21 column 5, line 23 - column 7, line 33 column 8, line 4 - column 9, line 23 figure 2	1-45
A	WO 03/063060 A (BROADCOM CORPORATION) 31 July 2003 (2003-07-31) page 1, line 5 - page 2, line 27 page 17, line 4 - page 18, line 25 figures 1,4 page 7, line 13 - page 9, line 16 ----- -/--	1-45
☒ Further documents are listed in the continuation of Box C. ☒ See patent family annex.		
* Special categories of cited documents:		
A document defining the general state of the art which is not considered to be of particular relevance		
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X document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone		
Y document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art		
Z document member of the same patent family		
Date of the actual completion of the international search 18 January 2006		Date of mailing of the international search report 08/02/2006
Name and mailing address of the ISA/ European Patent Office, P.B. 5818 Patentlaan 2 NL - 2280 HV Rijswijk Tel: (+31-70) 340-2040, Tx. 31 651 epo nl, Fax: (+31-70) 340-3076		Authorized officer Marzenke, M

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page 1 of 2

INTERNATIONAL SEARCH REPORT

International application No
PCT/US2005/036015

C(Continuation). DOCUMENTS CONSIDERED TO BE RELEVANT		
Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
A	US 6 337 877 B1 (COLE TERRY L ET AL) 8 January 2002 (2002-01-08) column 3, line 21 - column 4, line 29 column 7, line 49 - column 8, line 67 figures 3,10	1-45
A	"SunSet xDSL: Prequalification of ADSL Circuits with ATU-C Emulation" 2001, SUNRISE TELECOM INC., APPLICATION SERIES, SAN JOSE, USA, XP002363272 Retrieved from the Internet: URL: http://www.sunrisetelecom.com/technote/s/APP-xDSL-8B.pdf 'retrieved on 2006-01-17! page 3, right-hand column, paragraph 1	1-45

Form PCT/ISA/210 (continuation of second sheet) (April 2005)

page 2 of 2

INTERNATIONAL SEARCH REPORT

Information on patent family members

International application No

PCT/US2005/036015

Patent document cited in search report		Publication date	Patent family member(s)	Publication date
US 6707822	B1	16-03-2004	NONE	
WO 03063060	A	31-07-2003	EP 1476978 A2	17-11-2004
US 6337877	B1	08-01-2002	EP 1125408 A1	22-08-2001
			WO 0013387 A1	09-03-2000

Form PCT/ISA/210 (patent family annex) (April 2005)

PATENT COOPERATION TREATY

From the
INTERNATIONAL SEARCHING AUTHORITY

To:

see form PCT/ISA/220

PCT

WRITTEN OPINION OF THE
INTERNATIONAL SEARCHING AUTHORITY
(PCT Rule 43bis.1)

Date of mailing
(day/month/year) see form PCT/ISA/210 (second sheet)

Applicant's or agent's file reference
see form PCT/ISA/220

FOR FURTHER ACTION
See paragraph 2 below

International application No
PCT/US2005/036015

International filing date (day/month/year)
11.10.2005

Priority date (day/month/year)
12.10.2004

International Patent Classification (IPC) or both national classification and IPC
H04L1/00, H04L27/26

Applicant
AWARE, INC.

1. This opinion contains indications relating to the following items:

- ☒ Box No. I Basis of the opinion
- ☐ Box No. II Priority
- ☐ Box No. III Non-establishment of opinion with regard to novelty, inventive step and industrial applicability
- ☐ Box No. IV Lack of unity of invention
- ☒ Box No. V Reasoned statement under Rule 43bis 1(a)(i) with regard to novelty, inventive step or industrial applicability; citations and explanations supporting such statement
- ☐ Box No. VI Certain documents cited
- ☒ Box No. VII Certain defects in the international application
- ☒ Box No. VIII Certain observations on the international application

2. **FURTHER ACTION**

If a demand for international preliminary examination is made, this opinion will usually be considered to be a written opinion of the International Preliminary Examining Authority ("IPEA"). However, this does not apply where the applicant chooses an Authority other than this one to be the IPEA and the chosen IPEA has notified the International Bureau under Rule 66.1bis(b) that written opinions of this International Searching Authority will not be so considered.

If this opinion is, as provided above, considered to be a written opinion of the IPEA, the applicant is invited to submit to the IPEA a written reply together, where appropriate, with amendments, before the expiration of three months from the date of mailing of Form PCT/ISA/220 or before the expiration of 22 months from the priority date, whichever expires later.

For further options, see Form PCT/ISA/220.

3. For further details, see notes to Form PCT/ISA/220

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DATE 8-12-06
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Marzenke, M

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Form (PCT/ISA237) (Cover Sheet) (January 2004)

**WRITTEN OPINION OF THE
INTERNATIONAL SEARCHING AUTHORITY**

International application No.
PCT/US2005/036015

Box No. I Basis of the opinion

1. With regard to the **language**, this opinion has been established on the basis of the international application in the language in which it was filed, unless otherwise indicated under this item.
 - ☐ This opinion has been established on the basis of a translation from the original language into the following language , which is the language of a translation furnished for the purposes of international search (under Rules 12.3 and 23.1(b)).
2. With regard to any **nucleotide and/or amino acid sequence** disclosed in the international application and necessary to the claimed invention, this opinion has been established on the basis of:
 - a. type of material:
 - ☐ a sequence listing
 - ☐ table(s) related to the sequence listing
 - b. format of material:
 - ☐ in written format
 - ☐ in computer readable form
 - c. time of filing/furnishing:
 - ☐ contained in the international application as filed.
 - ☐ filed together with the international application in computer readable form.
 - ☐ furnished subsequently to this Authority for the purposes of search.
3. ☐ In addition, in the case that more than one version or copy of a sequence listing and/or table relating thereto has been filed or furnished, the required statements that the information in the subsequent or additional copies is identical to that in the application as filed or does not go beyond the application as filed, as appropriate, were furnished.
4. Additional comments:

**WRITTEN OPINION OF THE
INTERNATIONAL SEARCHING AUTHORITY**

International application No.
PCT/US2005/036015

Box No. V Reasoned statement under Rule 43*bis*.1(a)(i) with regard to novelty, inventive step or industrial applicability; citations and explanations supporting such statement

1. Statement

Novelty (N)	Yes: Claims	5,6,16,17,23,24,32,33,41,42
	No: Claims	1-4, 7-15, 18-22, 25-31, 34-40,43-45
Inventive step (IS)	Yes: Claims	
	No: Claims	5,6,16,17,23,24,32,33,41,42
Industrial applicability (IA)	Yes: Claims	1-45
	No: Claims	

2. Citations and explanations

see separate sheet

Box No. VII Certain defects in the international application

The following defects in the form or contents of the international application have been noted:

see separate sheet

Box No. VIII Certain observations on the international application

The following observations on the clarity of the claims, description, and drawings or on the question whether the claims are fully supported by the description, are made:

see separate sheet

V. Reasoned Statement with regard to novelty, inventive step and industrial applicability; citations and explanations supporting such statement

I

The following documents are referenced for the first time in this written opinion; the numbering will be adhered to in the rest of the procedure:

D1: US-B1-6 707 822

D2: WO 03/063060 A

D3: US-B1-6 337 877

D4: "SunSet xDSL: Prequalification of ADSL Circuits with ATU-C Emulation", 2001, SUNRISE TELECOM INC., APPLICATION SERIES, XP002363272 Retrieved from the Internet: URL: <http://www.sunrisetelecom.com/technotes/APP-xDSL-8B.pdf> [retrieved on 2006-01-17]

II

- 1.1 The present broad formulation of independent method Claim 1 is such that its subject-matter can be read onto prior art Document D1 which discloses according to the wording of Claim 1 (the corresponding features in D1 are given in brackets):

A method for sharing resources (*abstract; column 2, lines 57-59; column 9, lines 10-23*) in a transceiver (*column 5, lines 23-30; fig. 2*), comprising:
allocating a first portion of shared memory (*fig. 2: IDIM RAM 230; column 3, lines 16-20*) to a first latency path (*e.g. to any interleave path for G.lite or standard ADSL, see column 6, line 66 to column 7, line 17*) and allocating a second portion of the shared memory to a second latency path (*column 6, lines 55-62 and column 7, lines 17-30: additional 4K dedicated memory space are allocated to any fast path*).

Consequently, the features of independent Claim 1 are already known from Document D1 and thus the subject-matter of Claim 1 is not novel. Claim 1 therefore does not meet the requirements of Articles 33(1) and (2) PCT.

- 1.2 It should be noted that even if the Applicant were to interpret Claim 1 in such a manner as to enable him to allege that its subject-matter were novel, based on minor differences between the features of this claim and those disclosed in D1, the subject matter of Claim 1 would still not involve an inventive step, Articles 33(1) and (3) of the PCT, with respect to the disclosure of D1 especially as this document discloses the same object and the same type of solution as claimed.
2. The subject-matter of Claims 10, 19, 28 and 37 corresponds in terms of transceiver, system, protocol and storage media features respectively to that of Claim 1. Therefore, the objections raised in the previous paragraphs apply equally to Claims 10, 19, 28 and 37 which do consequently not meet the requirements of Articles 33(1) and (2) PCT for lack of novelty.
3. The dependent claims do not appear at present to contain any feature which in combination with the subject-matter of the independent claim to which the respective dependent claim is appended would result in novel and inventive subject-matter, these additional features being either disclosed or rendered obvious by the above cited documents, or being minor details obvious to a person skilled in the art based on common general knowledge of the art (Article 33(1) PCT). In particular, it is noted:

Claims 2-4, 13-15, 20-22, 29-31, 38-40: Use of interleaving/de-interleaving in two latency paths is known from D1. The latter teaches that depending on the used interleaving depth, several interleaved sessions or paths can be supported using the shared memory (*see column 7, lines 1-5 and 30-33*);

Claims 5, 6, 16, 17, 23, 24, 32, 33, 41, 42: Exchanging various information between two modems for determining resources that are available for a connection to be set up represents general common knowledge for the skilled person in the field of xDSL communications. It is therefore considered to be a straightforward design measure for a skilled person having knowledge of the shared memory transceivers in D1 to specifically exchange information regarding the maximum available interleaver memory size in order to accommodate a plurality of latency paths. D1 clearly teaches the skilled person that the memory size is a critical resource in terms of the number of

sessions/paths that can be supported contemporaneously (see column 7, lines 1-33). It does therefore not go beyond what can generally be expected from the skilled person in the light of D1 to exchange and use information specifying said critical amount of available shared memory;

Claim 7, 18, 25, 34, 43: Allocating a shared FCI module to perform the processing of two coder/decoder modules of two latency paths respectively is known from D1 (*see column 6, lines 11-17; fig. 2: FCI 226 writes encoded data for different latency paths into RAM 230 and reads decoded data for different latency paths from it: column 8, line 62 to column 9, line 3*);

Claims 8, 9, 11, 12, 26, 27, 35, 36, 44, 45: D1 teaches allocating a portion of memory to a path according to its latency (see column 6, lines 17-18: "Interleave and Fast Path"; column 7, lines 5-20: It is implicit to the skilled person from what is expressly said in D1 that the *interleaved* G.lite path requiring 4 Kbytes of memory imposes a higher processing latency than the fast path requiring only 256 bytes; on this point, the Applicant is also referred to D4 for information, see page 3, right-hand column, "Selecting the Path: Fast vs. Interleaved").

VII. Certain defects in the international application

1. To meet the requirements of Rule 6.3(b) PCT the independent claims should be cast in the two-part form, with those features known in combination from the prior art (see document D1) being placed in a preamble (Rule 6.3(b)(i) PCT) and with the remaining features being included in a characterising part (Rule 6.3(b)(ii) PCT).
2. To fulfil the requirements of Rule 5.1(a)(ii) PCT, document D1 should be identified in the description and the relevant background art disclosed therein briefly discussed.
3. The opening part of the description should be brought into conformity with any amended independent claims (Rule 5.1(a)(iii) PCT).
4. Furthermore, following the disclosure of document D1, the statement indicating the

technical problem to be solved by the invention (see page 2, paragraphs [0005] and [0006]), requires revision, which should be effected taking the requirements of Rule 5.1(a)(iii) PCT into account.

5. Reference signs placed in parentheses should be inserted into all the claims to increase their intelligibility (Rule 6.2(b) PCT). This applies to both the preamble and the characterising portion.
6. The reference to the "spirit" of the invention should be deleted (see page 23, last line) (Article 6 PCT and PCT-Guidelines 5.30).
7. The expression "herein incorporated by reference" (see page 1, par. [0001] and [0003]) should be removed from the description (see the PCT-Guidelines, 4.26).
8. The description (see page 7, par. [0033]) refers to "**later** developed hardware, software or firmware". By definition, it is however unclear what this hardware, software and/or firmware will effectively look like in the future. This formulation, implying in general terms that the extent of protection maybe expanded in some vague and not precisely defined way, should be deleted in accordance with Article 6 PCT and the PCT Guidelines 5.30.

The same applies to the formulation "later developed systems or structures, devices and/or software" on page 22, paragraph [0070].

9. The description on page 14, paragraph [0050] describes a third latency path for "a voice telephony application, which needs a very low latency but can tolerate BER".

The next sentence however contradicts the above statement: "In this case, the **video** [not voice ?] will be transported using an latency path that has a **large** amount of interleaving and coding [i.e. resulting in a high latency and thus contradicting the previously mentioned requirements for voice telephony ?]". Subsequently, this is again contradicted by the last sentence in paragraph [0050] stipulating that "**no** interleaving or coding" would be applied to said third latency path, further corroborated by the calculation in the following paragraph [0051] clearly assuming **no** interleaver memory and **no** encoding for the third path.

The second sentence of paragraph [0050] should thus be deleted for clarification.

10. The Applicant should remove the parentheses around the expression "BER" in Claims 9, 12, 27, 36 and 45 as this term does not represent a reference sign in the sense of Rule 6.2(b) PCT (see also the PCT-Guidelines 5.11).

VIII. Certain observations on the international application

The following objections are raised with respect to Article 6 PCT:

1. Independent Claim 28 (and its dependent Claims 29-36) repeat - word by word - the subject-matter already defined in Claim 1 (and its dependent Claims 2-9), thus contravening the requirement of Article 6 PCT that the claims shall be concise.

The generic terms "method" and "protocol" used in Claims 1 and 28 respectively belong to the same category "activity" as defined in the Guidelines 5.12 and can be used interchangeably. In fact, a protocol does not consist of anything more than a number of technical method steps.

The claims need to be recast to include only the minimum necessary number of independent claims in any one category (see Rule 6.1(a) PCT and the PCT-Guidelines, A5.42). In the present case it is considered appropriate to use only one independent claim in the "activity" (method) category.

Claim 28 and its dependent Claims 29-36 should thus be deleted.

2. Independent Claim 37 refers to "information that **when executed allows** sharing of resources in a transceiver, comprising information that allocates ...".

In its present wording, the claimed information is construed to be **suitable**, when executed, to share resources. The sharing of resources is thus not limiting the scope of the claim and the claimed information thus does not produce any technical effect whatsoever in terms of technical method steps being performed as a result of the

information (or program code) being executed.

It is also unclear, where or on which physical entity the information (or program code) is being executed on. Indeed, the claimed information can only bring about a technical effect in conjunction with a physical device on which it is run or executed. Otherwise, it merely represents program code per se.

The same objections apply to dependent Claims 38-45.

Claim 37 should thus be clarified to read: "An information storage medium comprising information which, when executed on a computer, performs the method as defined in any one of Claims 1 to 9." Claims 39-45 should be deleted.

3. The category of *method* Claims 2-4 is unclear as their additional features solely relate to constituent *means* of the latency paths. It is indeed unclear, which steps of the claimed *method* are effectively to be construed from the claimed (de)interleavers.

The same objection applies to Claims 29-31 and 38-40.

4. The abbreviation "INP" as presented in Claims 9, 12, 27, 36 and 45 is not clear from the wording of the claim alone and should be replaced by "impulse noise protection" in the light of the description (see page 11, mid-paragraph [0041]).
5. Claim 7 refers to "allocating a shared processing module to a plurality of coding and/or decoding modules". It is unclear, whether or not and if so, to what extent, these modules are part of the transceiver referred to in Claim 1.

The same lack of clarity arises in Claims 18, 25, 34 and 43.

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PATENT COOPERATION TREATY

PCT/US2005/036015

From the INTERNATIONAL BUREAU

SHERIDAN ACCORD

PCT

NOTIFICATION CONCERNING
TRANSMITTAL OF COPY OF INTERNATIONAL
PRELIMINARY REPORT ON PATENTABILITY
(CHAPTER I OF THE PATENT COOPERATION
TREATY)
(PCT Rule 44bis.1(c))

To:

VICK, Jason, H.
Miles & Stockbridge P.C.
1751 Pinnacle Dr.
Suite 500
McLean, VA 22102
ETATS-UNIS D'AMERIQUE

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MAY 04 2007

MILES & STOCKBRIDGE PC
TYSONS CORNER

Date of mailing (day/month/year) 26 April 2007 (26.04.2007)		
Applicant's or agent's file reference T3653-9285WO01		IMPORTANT NOTICE
International application No. PCT/US2005/036015 ✓	International filing date (day/month/year) 11 October 2005 (11.10.2005) ✓	Priority date (day/month/year) 12 October 2004 (12.10.2004) ✓
Applicant AWARE, INC. ✓		
The International Bureau transmits herewith a copy of the international preliminary report on patentability (Chapter I of the Patent Cooperation Treaty)		
The International Bureau of WIPO 34, chemin des Colombettes 1211 Geneva 20, Switzerland		Authorized officer Athina Nickitas-Etienne
Facsimile No. +41 22 338 82 70		e-mail: pt04.pct@wipo.int

Form PCT/IB/326 (January 2004)

PATENT COOPERATION TREATY

PCT

INTERNATIONAL PRELIMINARY REPORT ON PATENTABILITY

(Chapter I of the Patent Cooperation Treaty)

(PCT Rule 44bis)

Applicant's or agent's file reference T3653-9285WO01	FOR FURTHER ACTION		See item 4 below
International application No. PCT/US2005/036015	International filing date (<i>day/month/year</i>) 11 October 2005 (11.10.2005)	Priority date (<i>day/month/year</i>) 12 October 2004 (12.10.2004)	
International Patent Classification (8th edition unless older edition indicated) See relevant information in Form PCT/ISA/237			
Applicant AWARE, INC.			

1. This international preliminary report on patentability (Chapter I) is issued by the International Bureau on behalf of the International Searching Authority under Rule 44 <i>bis</i>.1(a). 2. This REPORT consists of a total of 10 sheets, including this cover sheet. In the attached sheets, any reference to the written opinion of the International Searching Authority should be read as a reference to the international preliminary report on patentability (Chapter I) instead.																
3. This report contains indications relating to the following items: <table> <tr> <td>☒ Box No. I</td> <td>Basis of the report</td> </tr> <tr> <td>☐ Box No. II</td> <td>Priority</td> </tr> <tr> <td>☐ Box No. III</td> <td>Non-establishment of opinion with regard to novelty, inventive step and industrial applicability</td> </tr> <tr> <td>☐ Box No. IV</td> <td>Lack of unity of invention</td> </tr> <tr> <td>☒ Box No. V</td> <td>Reasoned statement under Article 35(2) with regard to novelty, inventive step or industrial applicability; citations and explanations supporting such statement</td> </tr> <tr> <td>☐ Box No. VI</td> <td>Certain documents cited</td> </tr> <tr> <td>☒ Box No. VII</td> <td>Certain defects in the international application</td> </tr> <tr> <td>☒ Box No. VIII</td> <td>Certain observations on the international application</td> </tr> </table> 4. The International Bureau will communicate this report to designated Offices in accordance with Rules 44bis.3(c) and 93bis.1 but not, except where the applicant makes an express request under Article 23(2), before the expiration of 30 months from the priority date (Rule 44bis .2).	☒ Box No. I	Basis of the report	☐ Box No. II	Priority	☐ Box No. III	Non-establishment of opinion with regard to novelty, inventive step and industrial applicability	☐ Box No. IV	Lack of unity of invention	☒ Box No. V	Reasoned statement under Article 35(2) with regard to novelty, inventive step or industrial applicability; citations and explanations supporting such statement	☐ Box No. VI	Certain documents cited	☒ Box No. VII	Certain defects in the international application	☒ Box No. VIII	Certain observations on the international application
☒ Box No. I	Basis of the report															
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☐ Box No. VI	Certain documents cited															
☒ Box No. VII	Certain defects in the international application															
☒ Box No. VIII	Certain observations on the international application															

The International Bureau of WIPO 34, chemin des Colombettes 1211 Geneva 20, Switzerland Facsimile No. +41 22 338 82 70	Date of issuance of this report 17 April 2007 (17.04.2007)
	Authorized officer Athina Nickitas-Etienne e-mail: pt04.pct@wipo.int

Form PCT/IB/373 (January 2004)

PATENT COOPERATION TREATY

From the
INTERNATIONAL SEARCHING AUTHORITY

REC'D 07 FEB 2006

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PCT

To:

see form PCT/ISA/220

PT04

WRITTEN OPINION OF THE INTERNATIONAL SEARCHING AUTHORITY (PCT Rule 43bis.1)

Date of mailing
(day/month/year) see form PCT/ISA/210 (second sheet)

Applicant's or agent's file reference
see form PCT/ISA/220

FOR FURTHER ACTION
See paragraph 2 below

International application No.
PCT/JS2005/036015

International filing date (day/month/year)
11.10.2005

Priority date (day/month/year)
12.10.2004

International Patent Classification (IPC) or both national classification and IPC
H04L1/00, H04L27/26

Applicant
AWARE, INC.

1. This opinion contains indications relating to the following items:

- ☒ Box No. I Basis of the opinion
- ☐ Box No. II Priority
- ☐ Box No. III Non-establishment of opinion with regard to novelty, inventive step and industrial applicability
- ☐ Box No. IV Lack of unity of invention
- ☒ Box No. V Reasoned statement under Rule 43bis.1(a)(i) with regard to novelty, inventive step or industrial applicability; citations and explanations supporting such statement
- ☐ Box No. VI Certain documents cited
- ☒ Box No. VII Certain defects in the international application
- ☒ Box No. VIII Certain observations on the international application

2. FURTHER ACTION

If a demand for international preliminary examination is made, this opinion will usually be considered to be a written opinion of the International Preliminary Examining Authority ("IPEA"). However, this does not apply where the applicant chooses an Authority other than this one to be the IPEA and the chosen IPEA has notified the International Bureau under Rule 66.1bis(b) that written opinions of this International Searching Authority will not be so considered.

If this opinion is, as provided above, considered to be a written opinion of the IPEA, the applicant is invited to submit to the IPEA a written reply together, where appropriate, with amendments, before the expiration of three months from the date of mailing of Form PCT/ISA/220 or before the expiration of 22 months from the priority date, whichever expires later.

For further options, see Form PCT/ISA/220.

3. For further details, see notes to Form PCT/ISA/220.

Name and mailing address of the ISA:



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Authorized Officer

Marzenke, M

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Form (PCT/ISA/237) (Cover Sheet) (January 2004)

**WRITTEN OPINION OF THE
INTERNATIONAL SEARCHING AUTHORITY**

International application No.
PCT/US2005/036015

Box No. I Basis of the opinion

1. With regard to the **language**, this opinion has been established on the basis of the international application in the language in which it was filed, unless otherwise indicated under this item.
 - ☐ This opinion has been established on the basis of a translation from the original language into the following language , which is the language of a translation furnished for the purposes of international search (under Rules 12.3 and 23.1(b)).
2. With regard to any **nucleotide and/or amino acid sequence** disclosed in the international application and necessary to the claimed invention, this opinion has been established on the basis of:
 - a. type of material:
 - ☐ a sequence listing
 - ☐ table(s) related to the sequence listing
 - b. format of material:
 - ☐ in written format
 - ☐ in computer readable form
 - c. time of filing/furnishing:
 - ☐ contained in the international application as filed.
 - ☐ filed together with the international application in computer readable form.
 - ☐ furnished subsequently to this Authority for the purposes of search.
3. ☐ In addition, in the case that more than one version or copy of a sequence listing and/or table relating thereto has been filed or furnished, the required statements that the information in the subsequent or additional copies is identical to that in the application as filed or does not go beyond the application as filed, as appropriate, were furnished.
4. Additional comments:

**WRITTEN OPINION OF THE
INTERNATIONAL SEARCHING AUTHORITY**

International application No.
PCT/US2005/036015

Box No. V Reasoned statement under Rule 43bis.1(a)(i) with regard to novelty, inventive step or industrial applicability; citations and explanations supporting such statement

1. Statement

Novelty (N)	Yes: Claims	5,6,16,17,23,24,32,33,41,42
	No: Claims	1-4, 7-15, 18-22, 25-31, 34-40,43-45
Inventive step (IS)	Yes: Claims	
	No: Claims	5,6,16,17,23,24,32,33,41,42
Industrial applicability (IA)	Yes: Claims	1-45
	No: Claims	

2. Citations and explanations

see separate sheet

Box No. VII Certain defects in the international application

The following defects in the form or contents of the international application have been noted:

see separate sheet

Box No. VIII Certain observations on the international application

The following observations on the clarity of the claims, description, and drawings or on the question whether the claims are fully supported by the description, are made:

see separate sheet

V. Reasoned Statement with regard to novelty, inventive step and industrial applicability; citations and explanations supporting such statement

I

The following documents are referenced for the first time in this written opinion; the numbering will be adhered to in the rest of the procedure:

- D1: US-B1-6 707 822
- D2: WO 03/063060 A
- D3: US-B1-6 337 877
- D4: "SunSet xDSL: Prequalification of ADSL Circuits with ATU-C Emulation", 2001, SUNRISE TELECOM INC., APPLICATION SERIES, XP002363272 Retrieved from the Internet: URL:<http://www.sunrisetelecom.com/technotes/APP-xDSL-8B.pdf> [retrieved on 2006-01-17]

II

- 1.1 The present broad formulation of independent method Claim 1 is such that its subject-matter can be read onto prior art Document D1 which discloses according to the wording of Claim 1 (the corresponding features in D1 are given in brackets):

A method for sharing resources (*abstract; column 2, lines 57-59; column 9, lines 10-23*) in a transceiver (*column 5, lines 23-30; fig. 2*), comprising:
allocating a first portion of shared memory (*fig. 2: IDIM RAM 230; column 3, lines 16-20*) to a first latency path (*e.g. to any interleave path for G.lite or standard ADSL, see column 6, line 66 to column 7, line 17*) and allocating a second portion of the shared memory to a second latency path (*column 6, lines 55-62 and column 7, lines 17-30: additional 4K dedicated memory space are allocated to any fast path*).

Consequently, the features of independent Claim 1 are already known from Document D1 and thus the subject-matter of Claim 1 is not novel. Claim 1 therefore does not meet the requirements of Articles 33(1) and (2) PCT.

**WRITTEN OPINION OF THE
INTERNATIONAL SEARCHING
AUTHORITY (SEPARATE SHEET)**

International application No.

PCT/US2005/036015

- 1.2 It should be noted that even if the Applicant were to interpret Claim 1 in such a manner as to enable him to allege that its subject-matter were novel, based on minor differences between the features of this claim and those disclosed in D1, the subject matter of Claim 1 would still not involve an inventive step, Articles 33(1) and (3) of the PCT, with respect to the disclosure of D1 especially as this document discloses the same object and the same type of solution as claimed.
2. The subject-matter of Claims 10, 19, 28 and 37 corresponds in terms of transceiver, system, protocol and storage media features respectively to that of Claim 1. Therefore, the objections raised in the previous paragraphs apply equally to Claims 10, 19, 28 and 37 which do consequently not meet the requirements of Articles 33(1) and (2) PCT for lack of novelty.
3. The dependent claims do not appear at present to contain any feature which in combination with the subject-matter of the independent claim to which the respective dependent claim is appended would result in novel and inventive subject-matter, these additional features being either disclosed or rendered obvious by the above cited documents, or being minor details obvious to a person skilled in the art based on common general knowledge of the art (Article 33(1) PCT). In particular, it is noted:

Claims 2-4, 13-15, 20-22, 29-31, 38-40: Use of interleaving/de-interleaving in two latency paths is known from D1. The latter teaches that depending on the used interleaving depth, several interleaved sessions or paths can be supported using the shared memory (*see column 7, lines 1-5 and 30-33*);

Claims 5, 6, 16, 17, 23, 24, 32, 33, 41, 42: Exchanging various information between two modems for determining resources that are available for a connection to be set up represents general common knowledge for the skilled person in the field of xDSL communications. It is therefore considered to be a straightforward design measure for a skilled person having knowledge of the shared memory transceivers in D1 to specifically exchange information regarding the maximum available interleaver memory size in order to accommodate a plurality of latency paths. D1 clearly teaches the skilled person that the memory size is a critical resource in terms of the number of

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sessions/paths that can be supported contemporaneously (see column 7, lines 1-33). It does therefore not go beyond what can generally be expected from the skilled person in the light of D1 to exchange and use information specifying said critical amount of available shared memory;

Claim 7, 18, 25, 34, 43: Allocating a shared FCI module to perform the processing of two coder/decoder modules of two latency paths respectively is known from D1 (see column 6, lines 11-17; fig. 2: FCI 226 writes encoded data for different latency paths into RAM 230 and reads decoded data for different latency paths from it: column 8, line 62 to column 9, line 3);

Claims 8, 9, 11, 12, 26, 27, 35, 36, 44, 45: D1 teaches allocating a portion of memory to a path according to its latency (see column 6, lines 17-18: "Interleave and Fast Path"; column 7, lines 5-20: It is implicit to the skilled person from what is expressly said in D1 that the *interleaved* G.lite path requiring 4 Kbytes of memory imposes a higher processing latency than the fast path requiring only 256 bytes; on this point, the Applicant is also referred to D4 for information, see page 3, right-hand column, "Selecting the Path: Fast vs. Interleaved").

VII. Certain defects in the international application

1. To meet the requirements of Rule 6.3(b) PCT the independent claims should be cast in the two-part form, with those features known in combination from the prior art (see document D1) being placed in a preamble (Rule 6.3(b)(i) PCT) and with the remaining features being included in a characterising part (Rule 6.3(b)(ii) PCT).
2. To fulfil the requirements of Rule 5.1(a)(ii) PCT, document D1 should be identified in the description and the relevant background art disclosed therein briefly discussed.
3. The opening part of the description should be brought into conformity with any amended independent claims (Rule 5.1(a)(iii) PCT).
4. Furthermore, following the disclosure of document D1, the statement indicating the

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technical problem to be solved by the invention (see page 2, paragraphs [0005] and [0006]), requires revision, which should be effected taking the requirements of Rule 5.1(a)(iii) PCT into account.

5. Reference signs placed in parentheses should be inserted into all the claims to increase their intelligibility (Rule 6.2(b) PCT). This applies to both the preamble and the characterising portion.
6. The reference to the "spirit" of the invention should be deleted (see page 23, last line) (Article 6 PCT and PCT-Guidelines 5.30).
7. The expression "herein incorporated by reference" (see page 1, par. [0001] and [0003]) should be removed from the description (see the PCT-Guidelines, 4.26).
8. The description (see page 7, par. [0033]) refers to "**later** developed hardware, software or firmware". By definition, it is however unclear what this hardware, software and/or firmware will effectively look like in the future. This formulation, implying in general terms that the extent of protection may be expanded in some vague and not precisely defined way, should be deleted in accordance with Article 6 PCT and the PCT Guidelines 5.30.

The same applies to the formulation "later developed systems or structures, devices and/or software" on page 22, paragraph [0070].

9. The description on page 14, paragraph [0050] describes a third latency path for "a voice telephony application, which needs a very low latency but can tolerate BER".

The next sentence however contradicts the above statement: "In this case, the **video** [not voice ?] will be transported using an latency path that has a **large** amount of interleaving and coding [i.e. resulting in a high latency and thus contradicting the previously mentioned requirements for voice telephony ?]". Subsequently, this is again contradicted by the last sentence in paragraph [0050] stipulating that "no interleaving or coding" would be applied to said third latency path, further corroborated by the calculation in the following paragraph [0051] clearly assuming **no** interleaver memory and **no** encoding for the third path.

The second sentence of paragraph [0050] should thus be deleted for clarification.

10. The Applicant should remove the parentheses around the expression "BER" in Claims 9, 12, 27, 36 and 45 as this term does not represent a reference sign in the sense of Rule 6.2(b) PCT (see also the PCT-Guidelines 5.11).

VIII. Certain observations on the international application

The following objections are raised with respect to Article 6 PCT:

1. Independent Claim 28 (and its dependent Claims 29-36) repeat - word by word - the subject-matter already defined in Claim 1 (and its dependent Claims 2-9), thus contravening the requirement of Article 6 PCT that the claims shall be concise.

The generic terms "method" and "protocol" used in Claims 1 and 28 respectively belong to the same category "activity" as defined in the Guidelines 5.12 and can be used interchangeably. In fact, a protocol does not consist of anything more than a number of technical method steps.

The claims need to be recast to include only the minimum necessary number of independent claims in any one category (see Rule 6.1(a) PCT and the PCT-Guidelines, A5.42). In the present case it is considered appropriate to use only one independent claim in the "activity" (method) category.

Claim 28 and its dependent Claims 29-36 should thus be deleted.

2. Independent Claim 37 refers to "information that *when executed allows* sharing of resources in a transceiver, comprising information that allocates ...".

In its present wording, the claimed information is construed to be *suitable*, when executed, to share resources. The sharing of resources is thus not limiting the scope of the claim and the claimed information thus does not produce any technical effect whatsoever in terms of technical method steps being performed as a result of the

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information (or program code) being executed.

It is also unclear, where or on which physical entity the information (or program code) is being executed on. Indeed, the claimed information can only bring about a technical effect in conjunction with a physical device on which it is run or executed. Otherwise, it merely represents program code per se.

The same objections apply to dependent Claims 38-45.

Claim 37 should thus be clarified to read: "An information storage medium comprising information which, when executed on a computer, performs the method as defined in any one of Claims 1 to 9." Claims 39-45 should be deleted.

3. The category of *method* Claims 2-4 is unclear as their additional features solely relate to constituent *means* of the latency paths. It is indeed unclear, which steps of the claimed *method* are effectively to be construed from the claimed (de)interleavers.

The same objection applies to Claims 29-31 and 38-40.

4. The abbreviation "INP" as presented in Claims 9, 12, 27, 36 and 45 is not clear from the wording of the claim alone and should be replaced by "impulse noise protection" in the light of the description (see page 11, mid-paragraph [0041]).
5. Claim 7 refers to "allocating a shared processing module to a plurality of coding and/or decoding modules". It is unclear, whether or not and if so, to what extent, these modules are part of the transceiver referred to in Claim 1.

The same lack of clarity arises in Claims 18, 25, 34 and 43.

Electronic Acknowledgement Receipt	
EFS ID:	9199730
Application Number:	12901699
International Application Number:	
Confirmation Number:	1676
Title of Invention:	RESOURCE SHARING IN A TELECOMMUNICATIONS ENVIRONMENT
First Named Inventor/Applicant Name:	Marcos C. Tzannes
Customer Number:	62574
Filer:	Jason Vick/Nancy Davis
Filer Authorized By:	Jason Vick
Attorney Docket Number:	5550-54-CON-3
Receipt Date:	10-JAN-2011
Filing Date:	11-OCT-2010
Time Stamp:	16:08:14
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	no				
File Listing:					
Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1		IDS_01.pdf	566019 53043:99670c12566056769d864c04a3053 64r0k	yes	6

Multipart Description/PDF files in .zip description					
Document Description			Start	End	
Transmittal Letter			1	3	
Information Disclosure Statement (IDS) Filed (SB/08)			4	6	
Warnings:					
Information:					
2	Foreign Reference	EP1225735A1.pdf	3319471 nb5e96001141a0a10b6c205c87ac59cadf92ed1	no	30
Warnings:					
Information:					
3	Foreign Reference	EP1246409A1.pdf	4522291 bf0232471ba2a9d6e7c8db6d21a099e58283e	no	38
Warnings:					
Information:					
4	Foreign Reference	WO2003063060A2.pdf	2430819 c8fb5b302275e9e56acafdc0c30006c03345e36c	no	75
Warnings:					
Information:					
5	NPL Documents	WO2006044227A1.pdf	1310271 c4a14474104208b981c05c08a6a10b0b1968ba	no	37
Warnings:					
Information:					
6	NPL Documents	Shoji_WIRELESS_ACCESS_MET HOD_TO_ENSURE.pdf	1414514 e83281e015c9e4830594f8ec1232d0704b8c0314	no	14
Warnings:					
Information:					
7	NPL Documents	ITU- T_Recommendation_G992_5- 05-2003.pdf	3754491 12d286f0ed8ba48c6b97c43c6da7ca90a9811d	no	92
Warnings:					
Information:					
8	NPL Documents	ITU- T_Recommendation_G992_3- 01-2005.pdf	7371505 ed553373c7c854022481a11ef8724b4394ee075d	no	436
Warnings:					
Information:					

9	NPL Documents	ITU-T_Recommendation_G993_2-02-2006.pdf	14525041	no	252
c91a12cc3242c4fc1216c1c50046fa1a1fa1f457					
Warnings:					
Information:					
10	NPL Documents	Sunset_xDSL_Prequalification_of_ADSL_Circuits_with_ATU-C_Emulation.pdf	439680	no	4
e9560587c2f3d115c38a6df/9804610015d00e9f3					
Warnings:					
Information:					
11	NPL Documents	5550-54-PCT_ISR_2-8-2006.pdf	93073	no	3
8e385f5536a8c16ba027f3d7c71dca956d18190					
Warnings:					
Information:					
12	NPL Documents	5550-54-PCT_Written_Opinion.pdf	983104	no	9
cb475ef6041b1b8f9142a18cda91ef74fb8592ee					
Warnings:					
Information:					
13	NPL Documents	5550-54-PCT_IPRP.pdf	1236891	no	11
4eca88b11bc3e36dce8fa91bc2d83a113a3a914					
Warnings:					
Information:					
14	NPL Documents	5550-54-PAU_OA_6-24-09.pdf	1621631	no	30
cedbcea1107bdececf628ca73d2fa04039aac					
Warnings:					
Information:					
15	NPL Documents	5550-54-PCN_OA_9-25-09.pdf	811648	no	13
107a3f516c5d4a1e8d1fe4d4998d17dce02a0031					
Warnings:					
Information:					
16	NPL Documents	5550-54_OA_2-24-09.pdf	865943	no	23
fa34782bc1d83ae1256676ebdae09ff75b97b9					
Warnings:					
Information:					
17	NPL Documents	5550-54_OA_12-9-09.pdf	911747	no	25
c08dca7bd031d1dc396793652122798a8713637b					
Warnings:					
Information:					

18	NPL Documents	5550-54-CON_NOA_10-6-2010.pdf	319429 Bcd4c3d8f8f19ad6dea485b079c114f182666	no	8
Warnings:					
Information:					
19	NPL Documents	5550-54-CON-2_NOA_10-6-2010.pdf	269129 a78c4d42cc6dc704f83f1492f3e5a8849a257817	no	7
Warnings:					
Information:					
20	NPL Documents	5550-54_NOA_9-7-2010.pdf	326176 76b76548f16d839a5eeea4036cc873ba9b75c22b	no	8
Warnings:					
Information:					
Total Files Size (in bytes):			47092873		
This Acknowledgement Receipt evidences receipt on the noted date by the USPTO of the indicated documents, characterized by the applicant, and including page counts, where applicable. It serves as evidence of receipt similar to a Post Card, as described in MPEP 503. New Applications Under 35 U.S.C. 111 If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application. National Stage of an International Application under 35 U.S.C. 371 If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course. New International Application Filed with the USPTO as a Receiving Office If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.					

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In Re the Application of:	)	Group Art Unit: 2447
Marcos C. Tzannes	)	Confirmation No.: 1676
Serial No.: 12/901,699	)	Examiner: Not Yet Assigned
Filed: October 11, 2010	)	
Atty. File No.: 5550-54-CON-3	)	<u>INFORMATION DISCLOSURE</u>
Entitled: "RESOURCE SHARING IN A	)	<u>STATEMENT</u>
TELECOMMUNICATIONS ENVIRONMENT"	)	Electronically Submitted

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Dear Sir:

The references cited on attached Form PTO-1449 are being called to the attention of the Examiner.

- ☒ Copies of the cited non-patent and/or foreign references are enclosed herewith.
- ☐ Copies of the cited U.S. patents and/or patent applications are enclosed herewith.
- ☒ Copies of the cited U.S. patents/patent application publications are not enclosed in accordance with 37 C.F.R. § 1.98(a).
- ☐ Copies of the cited references are not enclosed, in accordance with 37 C.F.R. § 1.98(d), because the references were cited by or submitted to the U.S. Patent and Trademark Office in prior application Serial No. _____ filed _____, which is relied upon for an earlier filing date under 35 U.S.C. § 120.
- ☐ To the best of applicants' belief, the pertinence of the foreign-language references are believed to be summarized in the attached English abstracts and in the figures, although applicants do not necessarily vouch for the accuracy of the translation.
- ☒ Examiner's attention is drawn to the following related applications:

- Serial No. 11/246,163 filed 10-11-2005 now U.S. Patent No. 7,831,890 (Attorney's Ref. No. 5550-54)
- Serial No. 12/761,586 filed 04-16-2010 now U.S. Patent No. 7,844,882 (Attorney's Ref. No. 5550-54-CON)
- Serial No. 12/853,020 filed 08-09-2010 now U.S. Patent No. 7,836,381 (Attorney's Ref. No. 5550-54-CON-2)
- Serial No. 12/295,828 filed 10-02-2008 (Attorney's Ref. No. 5550-57-PUS)
- Serial No. 12/760,728 filed 04-15-2010 (Attorney's Ref. No. 5550-57-PUS-DIV)

- Serial No. 12/783,758 filed 05-20-2010 (Attorney's Ref. No. 5550-57-PUS-CON)
- Serial No. 12/783,765 filed 05-20-2010 (Attorney's Ref. No. 5550-57-PUS-DIV-CON)

☐ Other: _____

Submission of the above information is not intended as an admission that any item is citable under the statutes or rules to support a rejection, that any item disclosed represents analogous art, or that those skilled in the art would refer to or recognize the pertinence of any reference without the benefit of hindsight, nor should an inference be drawn as to the pertinence of the references based on the order in which they are presented. Submission of this statement should not be taken as an indication that a search has been conducted, or that no better art exists.

It is respectfully requested that the cited information be expressly considered during the prosecution of this application and the references made of record therein.

FEES

☒	37 CFR 1.97(b): No fee is believed due in connection with this submission, because the information disclosure statement submitted herewith is satisfied by one of the following conditions ("X" indicates satisfaction): ☒ Within three months of the filing date of a national application other than a continued prosecution application under 37 CFR 1.53(d), or ☐ Within three months of the date of entry into the national stage of an international application as set forth in 37 CFR 1.491 or ☐ Before the mailing date of a first Office Action on the merits, or ☐ Before the mailing of a first Office action after the filing of a request for continued examination under 37 CFR 1.114. Although no fee is believed due, if any fee is deemed due in connection with this submission, please charge such fee to Deposit Account 19-1970.
☐	37 CFR 1.97(c): The information disclosure statement transmitted herewith is being filed after all the above conditions (37 CFR 1.97(b)), but before the mailing date of one of the following conditions: (1) a final action under 37 C.F.R. 1.113 or (2) a notice of allowance under 37 C.F.R. 1.311, or (3) an action that otherwise closes prosecution in the application. This Information Disclosure Statement is accompanied by: ☐ A Certification (below) as specified by 37 C.F.R. 1.97(c). Although no fee is believed due, if any fee is deemed due in connection with this submission, please charge such fee to Deposit Account 19-1970. OR ☐ Please charge Deposit Account 19-1970 in the amount of \$180.00 for the fee set forth in 37 C.F.R. 1.17(p) for submission of an information disclosure statement. Please credit any overpayment or charge any underpayment to Deposit Account 19-1970.
☐	37 CFR 1.97(d): This Information Disclosure Statement is being submitted after the period specified in 37 CFR 1.97(c). ☐ This information Disclosure Statement includes a Certification (below) as specified by 37 C.F.R. 1.97(c) AND ☐ Applicants hereby requests consideration of the reference(s) disclosed herein. Please charge Deposit Account 19-1970 in the amount of \$180.00 under 37 C.F.R. 1.17(p). Please credit any overpayment or charge any underpayment to Deposit Account 19-1970. Election to pay the fee should not be taken as an indication that applicant(s) cannot execute a certification.

Certification (37 C.F.R. 1.97(e))
(Applicable only if checked)

☐

The undersigned certifies that:

- ☐ Each item of information contained in this information disclosure statement was first cited in any communication from a foreign patent office in a counterpart foreign application not more than three months prior to the filing of this statement. 37 C.F.R. 1.97(e)(1).
- ☐ A copy of the communication from the foreign patent office is enclosed.

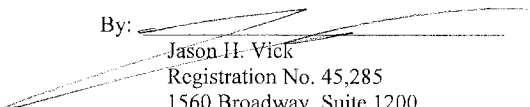
OR

- ☐ No item of information contained in this information disclosure statement was cited in a communication from a foreign patent office in a counterpart foreign application, and, to the knowledge of the undersigned after making reasonable inquiry, no item of information contained in this Information Disclosure Statement was known to any individual designated in 37 C.F.R. 1.56(e) more than three months prior to the filing of this statement. 37 C.F.R. 1.97(e)(2).

Respectfully submitted,

SHERIDAN ROSS P.C.

By:


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Date: 10 Jan '11



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APPLICATION NUMBER	FILING or 371(c) DATE	GRIPART UNIT	FIL FEE REC'D	ATTY DOCKET NO	TOT CLAIMS	IND CLAIMS
12/901,699	10/11/2010	2189	1090	5550-54-CON-3	8	2

CONFIRMATION NO. 1676

FILING RECEIPT



0000000044120447

62574
Jason H. Vick
Sheridan Ross, PC
Suite # 1200
1560 Broadway
Denver, CO 80202

Date Mailed: 10/25/2010

Receipt is acknowledged of this non-provisional patent application. The application will be taken up for examination in due course. Applicant will be notified as to the results of the examination. Any correspondence concerning the application must include the following identification information: the U.S. APPLICATION NUMBER, FILING DATE, NAME OF APPLICANT, and TITLE OF INVENTION. Fees transmitted by check or draft are subject to collection. Please verify the accuracy of the data presented on this receipt. **If an error is noted on this Filing Receipt, please submit a written request for a Filing Receipt Correction. Please provide a copy of this Filing Receipt with the changes noted thereon. If you received a "Notice to File Missing Parts" for this application, please submit any corrections to this Filing Receipt with your reply to the Notice. When the USPTO processes the reply to the Notice, the USPTO will generate another Filing Receipt incorporating the requested corrections**

Applicant(s)

Marcos C. Tzannes, Orinda, CA;
Michael Lund, West Newton, MA;

Assignment For Published Patent Application

AWARE, INC., Bedford, MA

Power of Attorney: The patent practitioners associated with Customer Number 62574

Domestic Priority data as claimed by applicant

This application is a CON of 12/761,586 04/16/2010
which is a CON of 11/246,163 10/11/2005 PAT 7,831,890
which claims benefit of 60/618,269 10/12/2004

Foreign Applications

If Required, Foreign Filing License Granted: 10/21/2010

The country code and number of your priority application, to be used for filing abroad under the Paris Convention,
is **US 12/901,699**

Projected Publication Date: 02/03/2011

Non-Publication Request: No

Early Publication Request: No

Title

RESOURCE SHARING IN A TELECOMMUNICATIONS ENVIRONMENT

Preliminary Class

711

PROTECTING YOUR INVENTION OUTSIDE THE UNITED STATES

Since the rights granted by a U.S. patent extend only throughout the territory of the United States and have no effect in a foreign country, an inventor who wishes patent protection in another country must apply for a patent in a specific country or in regional patent offices. Applicants may wish to consider the filing of an international application under the Patent Cooperation Treaty (PCT). An international (PCT) application generally has the same effect as a regular national patent application in each PCT-member country. The PCT process **simplifies** the filing of patent applications on the same invention in member countries, but **does not result** in a grant of "an international patent" and does not eliminate the need of applicants to file additional documents and fees in countries where patent protection is desired.

Almost every country has its own patent law, and a person desiring a patent in a particular country must make an application for patent in that country in accordance with its particular laws. Since the laws of many countries differ in various respects from the patent law of the United States, applicants are advised to seek guidance from specific foreign countries to ensure that patent rights are not lost prematurely.

Applicants also are advised that in the case of inventions made in the United States, the Director of the USPTO must issue a license before applicants can apply for a patent in a foreign country. The filing of a U.S. patent application serves as a request for a foreign filing license. The application's filing receipt contains further information and guidance as to the status of applicant's license for foreign filing.

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For information on preventing theft of your intellectual property (patents, trademarks and copyrights), you may wish to consult the U.S. Government website, <http://www.stopfakes.gov>. Part of a Department of Commerce initiative, this website includes self-help "toolkits" giving innovators guidance on how to protect intellectual property in specific countries such as China, Korea and Mexico. For questions regarding patent enforcement issues, applicants may call the U.S. Government hotline at 1-866-999-HALT (1-866-999-4158).

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page 2 of 3

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APPLICATION NUMBER	FILING OR 371(C) DATE	FIRST NAMED APPLICANT	ATTY. DOCKET NO./TITLE
12/901,699	10/11/2010	Marcos C. Tzannes	5550-54-CON-3

CONFIRMATION NO. 1676

POA ACCEPTANCE LETTER



62574
Jason H. Vick
Sheridan Ross, PC
Suite # 1200
1560 Broadway
Denver, CO 80202

Date Mailed: 10/25/2010

NOTICE OF ACCEPTANCE OF POWER OF ATTORNEY

This is in response to the Power of Attorney filed 10/11/2010.

The Power of Attorney in this application is accepted. Correspondence in this application will be mailed to the above address as provided by 37 CFR 1.33.

/gmhtsun/

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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In Re the Application of: TZANNES et al.	)	Group Art Unit:
Application No.:	)	Examiner:
Filed: Herewith	)	Confirmation No.:
Atty. File No.: 5550-54-CON-3	)	

For: RESOURCE SHARING IN A TELECOMMUNICATIONS ENVIRONMENT

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313

PRELIMINARY AMENDMENT

Dear Sir:

Prior to the initial review of the above-identified patent application by the Examiner, please enter the following Preliminary Amendment. Although Applicants do not believe that any fees are due based upon the filing of this Preliminary Amendment, please charge any such fees to Deposit Account 19-1970.

Please amend the above-identified patent application as follows:

Amendments to the Specification begin on page 2 of this paper.

Amendments to the Claims are shown in the listing of claims which begin on page 4 of this paper.

Remarks begin on page 6 of this paper.

AMENDMENTS TO THE SPECIFICATION

Please replace paragraph [0001] with:

[0001] This application is a Continuation of U.S. Application No. 12/761,586, filed April 16, 2010, which is a Continuation of U.S. Application No. 11/246,163 filed October 11, 2005, which This application claims the benefit of and priority under 35 U.S.C. § 119(e) to U.S. Patent Application No. 60/618,269, filed October 12, 2004, entitled “Sharing Memory and Processing Resources in DSL Systems,” each of which are incorporated herein by reference in their entirety.

Please replace paragraph [0003] with:

[0003] U.S. Patent Nos. 6,775,320 and 6,778,589, ~~which are both incorporated herein by reference in their entirety,~~ describe DSL systems supporting multiple applications and multiple framer/coder/interleaver FCI blocks (an FCI block is also referred to as a latency path). DSL systems carry applications that have different transmission requirements with regard to, for example, data rate, latency (delay), bit error rate (BER), and the like. For example, video typically requires a low BER ($<1E-10$) but can tolerate higher latency (>20 ms). Voice, on the other hand, typically requires a low latency (<1 ms) but can tolerate BER ($>1E-3$).

Please replace paragraph [0006] with:

[0006] Accordingly, an exemplary aspect of this invention relates to sharing memory between one or more interleavers and/or ~~deinterleavers~~ deinterleavers in a transceiver. More particularly, an exemplary aspect of this invention relates to shared latency path memory in a transceiver.

Please replace paragraph [0048] with:

[0048] Example #1

A first transmitter portion or receiver portion latency path may carry data from a video application, which needs a very low BER but can tolerate higher latency. In this case, the video will be transported using an latency path that has a large amount of interleaving/deinterleaving and coding (also known as Forward Error Correction (FEC) coding). For example, the latency path may be configured with Reed-Solomon coding using a codeword size of 255 bytes ($N=255$) with 16 checkbytes ($R=16$) and interleaving/deinterleaving using an interleaver depth of 64 ($D=64$). This latency path will require ~~$N \cdot D = 16 \cdot 255 = 16\text{Kbytes}$~~ $N \cdot D = 255 \cdot 64 = 16\text{Kbytes}$ of interleaver memory at the transmitter (or de-interleaver memory at the receiver). This latency path will be able to correct a burst of errors that is less than 512 bytes in duration.

AMENDMENTS TO THE CLAIMS

This listing of claims will replace all prior versions, and listings, of claims in the application.

Listing of Claims:

1.-45. (Cancelled)

46. (New) A system that allocates shared memory comprising:
a transceiver that is capable of:
transmitting or receiving a message during initialization specifying a maximum number of bytes of memory that are available to be allocated to an interleaver;
determining an amount of memory required by the interleaver to interleave a first plurality of Reed Solomon (RS) coded data bytes within a shared memory;
allocating a first number of bytes of the shared memory to the interleaver to interleave the first plurality of Reed Solomon (RS) coded data bytes for transmission at a first data rate, wherein the allocated memory for the interleaver does not exceed the maximum number of bytes specified in the message;
allocating a second number of bytes of the shared memory to a deinterleaver to deinterleave a second plurality of RS coded data bytes received at a second data rate; and
interleaving the first plurality of RS coded data bytes within the shared memory allocated to the interleaver and deinterleaving the second plurality of RS coded data bytes within the shared memory allocated to the deinterleaver, wherein the shared memory allocated to the interleaver is used at the same time as the shared memory allocated to the deinterleaver.

47. (New) The system of claim 46, wherein the determining is based on an impulse noise protection requirement.

48. (New) The system of claim 46, wherein the determining is based on a latency requirement.

49. (New) The system of claim 46, wherein the determining is based on a bit error rate requirement.

50. (New) A system that allocates shared memory comprising:
a transceiver that is capable of:

transmitting or receiving a message during initialization specifying a maximum number of bytes of memory that are available to be allocated to a deinterleaver;
determining an amount of memory required by the deinterleaver to deinterleave a first plurality of Reed Solomon (RS) coded data bytes within a shared memory;
allocating a first number of bytes of the shared memory to the deinterleaver to deinterleave a first plurality of Reed Solomon (RS) coded data bytes for transmission at a first data rate, wherein the allocated memory for the deinterleaver does not exceed the maximum number of bytes specified in the message;

allocating a second number of bytes of the shared memory to an interleaver to interleave a second plurality of RS coded data bytes received at a second data rate; and
deinterleaving the first plurality of RS coded data bytes within the shared memory allocated to the deinterleaver and interleaving the second plurality of RS coded data bytes within the shared memory allocated to the interleaver, wherein the shared memory allocated to the deinterleaver is used at the same time as the shared memory allocated to the interleaver.

51. (New) The system of claim 50, wherein the determining is based on an impulse noise protection requirement.

52. (New) The system of claim 50, wherein the determining is based on a latency requirement.

53. (New) The system of claim 50, wherein the determining is based on a bit error rate requirement.

REMARKS/ARGUMENTS

By this amendment, claims 1-45 are canceled without prejudice or disclaimer and new claims 46-53 are added.

Additionally, the continuity data has been updated and the specification amended in a similar manner as the parent application.

Applicants request examination on the merits.

Applicants believe that the pending claims are in condition for allowance and such disposition is respectfully requested. In the event that a telephone conversation would further prosecution and/or expedite allowance, the Examiner is invited to contact the undersigned.

The Commissioner is hereby authorized to charge to Deposit Account No. 19-1970 any fees under 37 C.F.R. §§ 1.16 and 1.17 that may be required by this paper and to credit any overpayment to that Account. If any extension of time is required in connection with the filing of this paper and has not been separately requested, such extension is hereby Petitioned.

Respectfully submitted,

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Date: 11 Oct '10

RESOURCE SHARING IN A TELECOMMUNICATIONS ENVIRONMENT

RELATED APPLICATION DATA

[0001] This application claims the benefit of and priority under 35 U.S.C. § 119(c) to U.S. Patent Application No. 60/618,269, filed October 12, 2004, entitled “Sharing Memory and Processing Resources in DSL Systems,” which is incorporated herein by reference in its entirety.

BACKGROUND

Field of the Invention

[0002] This invention generally relates to communication systems. More specifically, an exemplary embodiment of this invention relates to memory sharing in communication systems. Another exemplary embodiment relates to processing or coding resource sharing in a communication system.

Description of Related Art

[0003] U.S. Patent Nos. 6,775,320 and 6,778,589, which are both incorporated herein by reference in their entirety, describe DSL systems supporting multiple applications and multiple framer/coder/interleaver FCI blocks (an FCI block is also referred to as a latency path). DSL systems carry applications that have different transmission requirements with regard to, for example, data rate, latency (delay), bit error rate (BER), and the like. For example, video typically requires a low BER ($<1E-10$) but can tolerate higher latency (>20 ms). Voice, on the other hand, typically requires a low latency (<1 ms) but can tolerate BER ($>1E-3$).

[0004] As described in U.S. Patent No. 6,775,320, different applications can use different latency paths in order to satisfy the different application requirements of the communication system. As a result a transceiver must support multiple latency paths in order to support applications such as video, Internet access and voice telephony. When implemented in a transceiver, each of the latency paths will have a framer, coder, and interleaver block with different capabilities that depend on the application requirements.

SUMMARY

[0005] One difficulty with implementing multiple latency paths in a transceiver is the fact that a latency path is a complicated digital circuit that requires a large amount of memory and processing power. An interleaver within a latency path can consume a large amount of memory in order to provide error correcting capability. For example, a typical DSL transceiver will have at least one latency path with approximately 16 kbytes of memory for the interleaver. Likewise, the coding block, for example, a Reed Solomon coder, consumes a large amount of processing power. In general, as the number of latency paths increase, the memory and processing power requirements for a communication system become larger.

[0006] Accordingly, an exemplary aspect of this invention relates to sharing memory between one or more interleavers and/or deinterleavers in a transceiver. More particularly, an exemplary aspect of this invention relates to shared latency path memory in a transceiver.

[0007] Additional aspects of this invention relate to configuring and initializing shared memory in a communication system. More particularly, an exemplary aspect of this invention relates to configuring and initializing interleaver/deinterleaver memory in a communication system.

[0008] Additional aspects of the invention relate to determining the amount of memory that can be allocated to a particular component by a communication system. More specifically, an exemplary aspect of the invention relates to determining the maximum amount of shared memory that can be allocated to one or more interleaves or deinterleavers.

[0009] According to another exemplary aspect of the invention, processing power is shared between a number of transceiver modules. More specifically, and in accordance with an exemplary embodiment of the invention, a coding module is shared between one or more coders and/or decoders.

[0010] Another exemplary embodiment of the invention relates to transitioning from a fixed memory configuration to a shared memory configuration during one or more of initialization and SHOWTIME (user data transmission).

[0011] An additional exemplary aspect of the invention relates to dynamically updating one or more of shared memory and processing resources based on changing communication conditions.

[0012] An additional exemplary aspect of the invention relates to updating one or more of shared memory and processing resources based on an updated communication parameter.

[0013] An additional exemplary aspect of the invention relates to updating the allocation of one or more of shared memory and processing resources based on an updated communication parameter(s).

[0014] Additional aspects of the invention relate to exchanging shared resource allocations between transceivers.

[0015] Additional exemplary aspects relate to a method of allocating shared memory in a transceiver comprising allocating the shared memory to a plurality of modules, wherein each of the plurality of modules comprise at least one interleaver, at least one deinterleaver or a combination thereof.

[0016] Still further aspects relate to the above method wherein the plurality of modules comprise interleavers.

[0017] Still further aspects relate to the above method wherein the plurality of modules comprise deinterleavers.

[0018] Still further aspects relate to the above method wherein the plurality of modules comprise at least one interleaver and at least one deinterleaver.

[0019] Additional exemplary aspects relate to a transceiver comprising a plurality of modules each including at least one interleaver, at least one deinterleaver or a

combination thereof and a shared memory designed to be allocated to a plurality of the modules.

[0020] Still further aspects relate to the above transceiver wherein the plurality of modules comprise interleavers.

[0021] Still further aspects relate to the above transceiver wherein the plurality of modules comprise deinterleavers.

[0022] Still further aspects relate to the above transceiver wherein the plurality of modules comprise at least one interleaver and at least one deinterleaver.

[0023] These and other features and advantages of this invention are described in, or are apparent from, the following description of the embodiments.

BRIEF DESCRIPTION OF THE DRAWINGS

[0024] The embodiments of the invention will be described in detail, with reference to the following figures, wherein:

[0025] Fig. 1 is a functional block diagram illustrating an exemplary transceiver according to this invention;

[0026] Fig. 2 is a flowchart outlining an exemplary method of sharing resources according to this invention;

[0027] Fig. 3 is a flowchart outlining an exemplary method of determining a maximum amount of shared memory according to this invention; and

[0028] Fig. 4 is a flowchart outlining an exemplary resource sharing methodology according to this invention.

DETAILED DESCRIPTION

[0029] The exemplary embodiments of this invention will be described in relation to sharing resources in a wired and/or wireless communications environment. However, it should be appreciated, that in general, the systems and methods of this invention will work equally well for any type of communication system in any environment.

[0030] The exemplary systems and methods of this invention will also be described in relation to multicarrier modems, such as DSL modems and VDSL modems, and associated communication hardware, software and communication channels. However, to avoid unnecessarily obscuring the present invention, the following description omits well-known structures and devices that may be shown in block diagram form or otherwise summarized.

[0031] For purposes of explanation, numerous details are set forth in order to provide a thorough understanding of the present invention. It should be appreciated however that the present invention may be practiced in a variety of ways beyond the specific details set forth herein.

[0032] Furthermore, while the exemplary embodiments illustrated herein show the various components of the system collocated, it is to be appreciated that the various components of the system can be located at distant portions of a distributed

network, such as a telecommunications network and/or the Internet, or within a dedicated secure, unsecured and/or encrypted system. Thus, it should be appreciated that the components of the system can be combined into one or more devices, such as a modem, or collocated on a particular node of a distributed network, such as a telecommunications network. As will be appreciated from the following description, and for reasons of computational efficiency, the components of the system can be arranged at any location within a distributed network without affecting the operation of the system. For example, the various components can be located in a Central Office modem (CO, ATU-C, VTU-O), a Customer Premises modem (CPE, ATU-R, VTU-R), a DSL management device, or some combination thereof. Similarly, one or more functional portions of the system could be distributed between a modem and an associated computing device.

[0033] Furthermore, it should be appreciated that the various links, including communications channel 5, connecting the elements can be wired or wireless links, or any combination thereof, or any other known or later developed element(s) that is capable of supplying and/or communicating data to and from the connected elements. The term module as used herein can refer to any known or later developed hardware, software, firmware, or combination thereof that is capable of performing the functionality associated with that element. The terms determine, calculate and compute, and variations thereof, as used herein are used interchangeably and include any type of methodology, process, mathematical operation or technique. FCI block and latency path are used interchangeably herein as well as transmitting modem and transmitting transceiver. Receiving modem and receiving transceiver are also used

interchangably.

[0034] Fig. 1 illustrates an exemplary embodiment of a transceiver 100 that utilizes shared resources. It should be appreciated that numerous functional components of the transceiver have been omitted for clarity. However, the transceiver 100 can also include the standard components found in typical communications device(s) in which the technology of the subject invention is implemented into.

[0035] According to an exemplary embodiment of the invention, memory and processing power can be shared among a plurality of transmitter and/or receiver latency paths, in a communications transceiver that carries or supports multiple applications. For example, the transmitter and/or receiver latency paths of the transceiver can share an interleaver/deinterleaver memory and the shared memory can be allocated to the interleaver and/or deinterleaver of each latency path. This allocation can be done based on the data rate, latency, BER, impulse noise protection requirements of the application, data or information being transported over each latency path, or in general any parameter associated with the communications system.

[0036] Likewise, for example, the transmitter and/or receiver latency paths can share a Reed-Solomon coder/decoder processing module and the processing power of this module can be allocated to each encoder and/or decoder. This allocation can be done based on the data rate/latency, BER, impulse noise protection requirements of the application data or information being transported over each latency path, or in general based on any parameter associated with the communication system.

[0037] In accordance with an exemplary operational embodiment, a first transceiver and a second transceiver transmit to one another messages during, for example, initialization which contain information on the total and/or shared memory capabilities of each transceiver and optionally information about the one or more latency paths. This information can be transmitted prior to determining how to configure the latency paths to support the application requirements. Based on this information, one of the modems can select an FCI configuration parameter(s) that meets the transmission requirements of each application being transported over each latency paths. While an exemplary of the embodiment of the invention will be described in relation to the operation of the invention and characteristics thereof being established during initialization, it should be appreciated that the sharing of resources can be modified and messages transmitted between a two transceivers at any time during initialization and/or user data transmission, i.e., SHOWTIME.

[0038] Fig. 1 illustrates an exemplary embodiment of a transceiver 100. The transceiver 100 includes a transmitter portion 200 and a receiver portion 300. The transmitter portion 200 includes one or more latency paths 210, 220, ... Similarly, the receiver portion 300 includes one or more latency paths 310, 320, ... Each of the latency paths in the transmitter portion 200 includes a framer, coder, and interleaver designated as 212, 214, 216 and 222, 224 and 226, respectively. Each of the latency paths in the receiver portion includes a deframer, decoder, and deinterleaver designated as 312, 314, 316 and 322, 324, and 326, respectively. The transceiver 100 further includes a shared processing module 110, a shared memory 120, a parameter

determination module 130, a path module 140, an allocation module 150, and a shared resource management module 160, all interconnected by one or more links (not shown).

[0039] In this exemplary embodiment, the transceiver 100 is illustrated with four total transmitter portion and receiver portion latency paths, i.e., 210, 220, 310, and 320. The shared memory 120 is shared amongst the two transmitter portion interleavers 216 and 226 and two receiver portion deinterleavers 316 and 326. The shared processing module 110, such as a shared coding module, is shared between the two transmitter portion coders 214 and 224 and the two receiver portion decoders 314 and 324.

[0040] While the exemplary embodiment of the invention will be described in relation to a transceiver having a number of transmitter portion latency paths and receiver portion latency paths, it should be appreciated that this invention can be applied to any transceiver having any number of latency paths. Moreover, it should be appreciated that the sharing of resources can be allocated such that one or more of the transmitter portion latency paths are sharing a shared resource, one or more of the receiver portion latency paths are sharing a shared resource, or a portion of the transmitter portion latency paths and a portion of the receiver portion latency paths are sharing shared resources. Moreover, any one or more of the latency paths, or portions thereof, could also be assigned to a fixed resource while, for example, another portion of the latency path(s) assigned to a shared resource. For example, in latency path 210, the interleaver 216 could be allocated a portion of the shared

memory 120, while the coder 214 could be allocated to a dedicated processing module, vice versa, or the like.

[0041] In accordance with the exemplary embodiment, a plurality of transmitter portion or receiver portion latency paths share an interleaver/deinterleaver memory, such as shared memory 120, and a coding module, such as shared processing module 110. For example, the interleaver/deinterleaver memory can be allocated to different interleavers and/or deinterleavers. This allocation can be based on parameters associated with the communication systems such as data rate, latency, BER, impulse noise protection, and the like, of the applications being transported. Similarly, a coding module, which can be a portion of the shared processing module 110, can be shared between any one or more of the latency paths. This sharing can be based on requirements such as data rate, latency, BER, impulse noise protection, and the like, of the applications being transported.

[0042] For example, an exemplary transceiver could comprise a shared interleaver/deinterleaver memory and could be designed to allocate a first portion of the shared memory 120 to an interleaver, such as interleaver 216 in the transmitter portion of the transceiver and allocate a second portion of the shared memory 120 to a deinterleaver, such as 316, in the receiver portion of the transceiver.

[0043] Alternatively, for example, an exemplary transceiver can comprise a shared interleaver/deinterleaver memory, such as shared memory 120, and be designed to allocate a first portion of shared memory 120 to a first interleaver, e.g.,

216, in the transmitter portion of the transceiver and allocate a second portion of the shared memory to a second interleaver, e.g., 226, in the transmitter portion of the transceiver.

[0044] Alternatively, for example, an exemplary transceiver can comprise a shared interleaver/deinterleaver memory and be designed to allocate a first portion of the shared memory 120 to a first deinterleaver, e.g., 316, in the receiver portion of the transceiver and allocate a second portion of the shared memory to a second deinterleaver, e.g., 326, in the receiver portion of the transceiver. Regardless of the configuration, in general any interleaver or deinterleaver, or grouping thereof, be it in a transmitter portion or receiver portion of the transceiver, can be associated with a portion of the shared memory 120.

[0045] Establishment, configuration and usage of shared resources is performed in the following exemplary manner. First, and in cooperation with the path module 140, the number of transmitter and receiver latency paths (N) is determined. The parameter determination module 130 then analyses one or more parameters such as data rate, transmitter data rate, receiver data rate, impulse noise protection, bit error rate, latency, or the like. Based on one or more of these parameters, the allocation module 150 allocates a portion of the shared memory 120 to one or more of the interleaver and/or deinterleavers, or groupings thereof. This process continues until the memory allocation has been determined and assigned to each of the N latency paths.

[0046] Having determined the memory allocation for each of the latency paths, and in conjunction with the shared resource management 160, the transceiver 100 transmits to a second transceiver one or more of the number of latency paths (N), the maximum interleaver memory for any one or more of the latency paths and/or the maximum total and/or shared memory for all of the latency paths.

[0047] Three examples of sharing interleaver/deinterleaver memory and coding processing in a transceiver are described below. The latency paths in these examples can be in the transmitter portion of the transceiver or the receiver portion of the transceiver.

[0048] Example #1

A first transmitter portion or receiver portion latency path may carry data from a video application, which needs a very low BER but can tolerate higher latency. In this case, the video will be transported using an latency path that has a large amount of interleaving/deinterleaving and coding (also known as Forward Error Correction (FEC) coding). For example, the latency path may be configured with Reed-Solomon coding using a codeword size of 255 bytes ($N=255$) with 16 checkbytes ($R=16$) and interleaving/deinterleaving using an interleaver depth of 64 ($D=64$). This latency path will require $N*D=16*255=16\text{Kbytes}$ of interleaver memory at the transmitter (or de-interleaver memory at the receiver). This latency path will be able to correct a burst of errors that is less than 512 bytes in duration.

[0049] A second transmitter portion or receiver portion latency path may carry an

internet access application that requires a medium BER and a medium amount of latency. In this case, the internet access application will be transported using a latency path that has a medium amount of interleaving and coding. For example, the latency path may be configured with Reed-Solomon coding using a codeword size of 128 bytes ($N=128$) with 8 checkbytes ($R=8$) and interleaving using an interleaver depth of 16 ($D=32$). This latency path will require $N \cdot D = 128 \cdot 32 = 4$ Kbytes of interleaver memory and the same amount of deinterleaver memory. This latency path will be able to correct a burst of errors that is less than 128 bytes in duration.

[0050] A third transmitter portion or receiver portion latency path may carry a voice telephony application, which needs a very low latency but can tolerate BER. In this case, the video will be transported using an latency path that has a large amount of interleaving and coding. For example, the third transmitter portion or receiver portion latency path may be configured with no interleaving or coding which will result in the lowest possible latency through the latency path but will provide no error correction capability.

[0051] According to the principles of this invention, a system carrying the three applications described above in Example #1, would have three latency paths that share one memory space containing at least $(16+4)=20$ Kbytes. The three latency paths also share a common coding block that is able to simultaneously encode (in the transmitter portion) or decode (in a receiver portion) two codewords with $N=255/R=16$ and $N=128/R=8$.

[0052] According to an exemplary embodiment of this invention, the latency paths can be reconfigured at initialization or during data transmission mode (also known as SHOWTIME in ADSL and VDSL transceivers). This would occur if, for example, the applications or application requirements were to change.

[0053] Example #2

If instead of 1 video application, 1 internet application and 1 voice application, there were 3 internet access applications then the transmitter portion and/or receiver portion latency paths would be reconfigured to utilize the shared memory and coding module in a different way. For example, the system could be reconfigured to have 3 transmitter portion or receiver portion latency paths, with each latency path being configured with Reed-Solomon coding using a codeword size of 128 bytes ($N=128$) with 8 checkbytes ($R=8$) and interleaving using an interleaver depth of 16 ($D=32$). Each latency path will require $N*D=128*32=4\text{Kbytes}$ of interleaver memory and each block will be able to correct a burst of errors that is less than 128 bytes in duration. Based on the example of carrying the three internet access applications described, the three latency path share one memory space containing at least $3*4=12\text{ Kbytes}$. Also the three latency paths share a common coding block that is able to simultaneously encode (on the transmitter side) or decode (on the receiver side) three codewords with $N=128/R=16$, $N=128/R=8$ and $N=128/R=8$.

[0054] Example #3

The system could be configured to carry yet another set of applications. For example, the latency paths could be configured to carry 2 video applications. In this case only

2 transmitter portion or receiver portion latency paths are needed, which means that the third latency path could be simply disabled. Also, assuming that the memory is constrained based on the first example above, then the maximum shared memory for these 2 latency paths is 20 kBytes. In this case, the system could be reconfigured to have 2 latency paths, with each block being configured with Reed-Solomon coding using a codeword size of 200 bytes ($N=200$) with 10 checkbytes ($R=10$) and interleaving/deinterleaving using an interleaver depth of 50 ($D=50$). Each latency path will require $N*D=200*50=10\text{Kbytes}$ of interleaver memory and each block will be able to correct a burst of errors that is less than 250 bytes in duration. This configuration results in 20K of shared memory for both latency paths, which is the same as in the first example. In order to stay within the memory constraints of the latency paths, the error correction capability for each latency path is decreased to 250 bytes from 512 bytes in Example #1.

[0055] Another aspect of this invention is the how FCI configuration information is transmitted between a first modem and a second modem. FCI configuration information will depend on the requirements of the applications being transported over the DSL connection. This information may need to be forwarded during initialization in order to initially configure the DSL connection. This information may also need to be forwarded during SHOWTIME in order to reconfigure the DSL connection based on a change in applications or the application requirements.

[0056] According to one embodiment, a first modem determines the specific FCI configuration parameters, e.g., N , D , R as defined above, needed to meet specific

application requirements, such as latency, burst error correction capability, etc. In order to determine the FCI configuration parameters, the first modem must know what are the capabilities of a second modem. For example, the first modem must know how many latency paths (FCI blocks) the second modem can support. Also the first modem must know the maximum amount of interleaver memory for each transmitter latency path. In addition, since the transmitter latency paths may share a common memory space the first modem must know the total shared memory for all transmitter latency paths. This way the first modem will be able to choose a configuration that can meet application requirements and also meet the transmitter portion latency path capabilities of the second modem.

[0057] For example, using values from examples above, a first transceiver could send a message to a second transceiver during initialization or during SHOWTIME containing the following information:

- Number of supported transmitter and receiver latency paths = 3
- Max Interleaver Memory for latency path #1= 16 Kbytes
- Max Interleaver Memory for latency path #2= 16 Kbytes
- Max Interleaver Memory for latency path #3= 16 Kbytes
- Maximum total/shared memory for all latency paths = 20 kBytes

Based on this information, and the application requirements, the first transceiver would select latency path settings. For example, if the applications are 1 video, 1 internet access and 1 voice application, the first transceiver could configure 3 latency paths as follows:

latency path #1 – Video: N=255, R=16, D=64

latency path #2 – Video: N=128, R=8, D=32

latency path #3 – Video: N=0, R=0, D=1 (no coding or interleaving)

[0058] This would result in a total interleaver memory of 20 kbytes.

[0059] Alternatively, if for example, there are only 2 video applications, the first transceiver could configure 2 latency paths as follows:

latency path #1 – Video: N=200, R=10, D=50

latency path #2 – Video: N=200, R=10, D=50

latency path #3 – Video: N=0, R=0, D=1 (no coding or interleaving)

[0060] This would also result in a total interleaver memory of 20 kbytes.

[0061] Alternatively, the second transceiver can determine the specific FCI configuration parameters, e.g., N, D, R as defined above, needed to meet specific application requirements, such as latency, burst error correction capability, etc. As described above for the first transceiver, in order to determine the FCI configuration parameters, the second transceiver must first know what are the capabilities of the first transceiver. In this case, the first transceiver would send a message to the second transceiver containing the information described above and based on this information and the application requirements the second transceiver would select latency path settings.

[0062] Fig. 2 outlines an exemplary method of allocating shared memory in a

transceiver. More specifically, control begins in step S200 and continues to step S210. In step S210, one or more of shared interleaver/deinterleaver memory and/or shared coder/decoder processing resources are allocated to one or more latency paths, in a transceiver. Control then continues to step S220 where the control sequence ends.

[0063] Fig. 3 outlines an exemplary method of exchanging shared resource allocations according to an exemplary embodiment of this invention. In particular, control begins in step S310. In step S310, a maximum amount of shared memory that can be allocated to a specific interleaver or deinterleaver of a plurality of interleavers or deinterleavers in a transceiver is determined. Next, in step S320, the determined maximum amount for one or more of the deinterleavers and/or interleavers is transmitted to another transceiver. Messages containing additional information can also be transmitted to the other transceiver and/or received from the other transceiver. Control then continues to step S330 where the control sequence ends.

[0064] Fig. 4 outlines an exemplary procedure for resource sharing according to an exemplary embodiment of this invention. In particular, control begins in step S400 and continues to step S410. In step S410, the number of latency paths are determined. Then, in step S420, the latency path information (FCI block information) is transmitted to another transceiver. Messages containing additional information can also be transmitted to the other transceiver and/or received from the other transceiver. This information can be used to, for example, assist with the determination of memory allocation in the transceiver. Moreover, the messages received from the

other transceiver could specify what the memory allocation is to be based on, for example, the number of latency paths, memory allocation in the remote transceiver and required applications. Control then continues to step S430.

[0065] In step S430, and for each latency path, the steps in step 440 are performed.

[0066] In step S440, and while monitoring of allocation of resources is being performed, steps 450 and 460 are performed. More specifically, in step S450, one or more parameters associated with the communication system are determined. Then, in step S460, shared resources are allocated based on one or more of the communication parameters. Control then continues to step S470.

[0067] In step S470, the allocation of shared resources is communicated to another transceiver. Next, in step S480, a determination is made as to whether there is a change in communications that would require the adjustment of the shared resource allocation. Examples of changes in communications conditions include a change in applications being transported over the system and/or changes in the channel condition, etc. If adjustments are required, control jumps back to step S410. Otherwise, control jumps to step S490 where the control sequence ends.

[0068] The above-described system can be implemented on wired and/or wireless telecommunications devices, such a modem, a multicarrier modem, a DSL modem, an ADSL modem, an XDSL modem, a VDSL modem, a linecard, test equipment, a

multicarrier transceiver, a wired and/or wireless wide/local area network system, a satellite communication system, a modem equipped with diagnostic capabilities, or the like, or on a separate programmed general purpose computer having a communications device or in conjunction with any of the following communications protocols: CDSL, ADSL2, ADSL2+, VDSL1, VDSL2, HDSL, DSL Lite, IDSL, RADSL, SDSL, UDSL or the like.

[0069] Additionally, the systems, methods and protocols of this invention can be implemented on a special purpose computer, a programmed microprocessor or microcontroller and peripheral integrated circuit element(s), an ASIC or other integrated circuit, a digital signal processor, a hard-wired electronic or logic circuit such as discrete element circuit, a programmable logic device such as PLD, PLA, FPGA, PAL, a modem, a transmitter/receiver, any comparable means, or the like. In general, any device capable of implementing a state machine that is in turn capable of implementing the methodology illustrated herein can be used to implement the various communication methods, protocols and techniques according to this invention.

[0070] Furthermore, the disclosed methods may be readily implemented in software using object or object-oriented software development environments that provide portable source code that can be used on a variety of computer or workstation platforms. Alternatively, the disclosed system may be implemented partially or fully in hardware using standard logic circuits or VLSI design. Whether software or hardware is used to implement the systems in accordance with this invention is

dependent on the speed and/or efficiency requirements of the system, the particular function, and the particular software or hardware systems or microprocessor or microcomputer systems being utilized. The communication systems, methods and protocols illustrated herein can be readily implemented in hardware and/or software using any known or later developed systems or structures, devices and/or software by those of ordinary skill in the applicable art from the functional description provided herein and with a general basic knowledge of the computer and telecommunications arts.

[0071] Moreover, the disclosed methods may be readily implemented in software that can be stored on a storage medium, executed on programmed general-purpose computer with the cooperation of a controller and memory, a special purpose computer, a microprocessor, or the like. In these instances, the systems and methods of this invention can be implemented as program embedded on personal computer such as an applet, JAVA[®] or CGI script, as a resource residing on a server or computer workstation, as a routine embedded in a dedicated communication system or system component, or the like. The system can also be implemented by physically incorporating the system and/or method into a software and/or hardware system, such as the hardware and software systems of a communications transceiver.

[0072] It is therefore apparent that there has been provided, in accordance with the present invention, systems and methods for sharing resources. While this invention has been described in conjunction with a number of embodiments, it is evident that many alternatives, modifications and variations would be or are apparent

to those of ordinary skill in the applicable arts. Accordingly, it is intended to embrace all such alternatives, modifications, equivalents and variations that are within the spirit and scope of this invention.

Claims:

1. A method for sharing resources in a transceiver comprising:
allocating a first portion of shared memory to a first latency path and
allocating a second portion of the shared memory to a second latency path.
2. The method of claim 1, wherein the first latency path includes an interleaver and the second latency path includes an interleaver.
3. The method of claim 1, wherein the first latency path includes an interleaver and the second latency path includes a deinterleaver.
4. The method of claim 1, wherein the first latency path includes a deinterleaver and the second latency path includes a deinterleaver.
5. The method of claim 1, further comprising transmitting to another transceiver information that is used to determine a maximum amount of shared memory that can be allocated.
6. The method of claim 1, further comprising receiving from another transceiver information that is used to determine a maximum amount of shared memory that can be allocated.
7. The method of claim 1, further comprising allocating a shared processing module to a plurality of coding and/or decoding modules.
8. The method of claim 1, wherein the allocating of at least one portion of the shared memory is based on one or more communication parameters.
9. The method of claim 8, wherein at least one of the communication parameters is a data rate, a latency, an INP value or a bit error rate (BER).

10. A transceiver comprising:
a first portion of shared memory that is allocated to a first latency path;
and
a second portion of the shared memory that is allocated to a second latency path.
11. The transceiver of claim 10, further comprising:
an allocation module designed to allocate the shared memory based on one or more communication parameters.
12. The transceiver of claim 11, wherein at least one of the communication parameters is a data rate, a latency, an INP value or a Bit Error Rate (BER).
13. The transceiver of claim 10, wherein the first latency path includes an interleaver and the second latency path includes an interleaver.
14. The transceiver of claim 10, wherein the first latency path includes an interleaver and the second latency path includes a deinterleaver.
15. The transceiver of claim 10, wherein the first latency path includes a deinterleaver and the second latency path includes a deinterleaver.
16. The transceiver of claim 10, further comprising a shared resource management module designed to determine information that is transmitted to another transceiver, wherein the information is used to determine a maximum amount of shared memory that can be allocated.
17. The transceiver of claim 10, further comprising a shared resource management module designed to utilize information that is received from another transceiver, wherein the information is used to determine a maximum amount of shared memory that can be allocated.

18. The transceiver of claim 10, further comprising a shared processing module designed to provide processing resources to a plurality of coding and/or decoding modules.

19. A system for sharing resources in a transceiver comprising:
means for allocating a first portion of shared memory to a first latency path and means for allocating a second portion of the shared memory to a second latency path.

20. The system of claim 19, wherein the first latency path includes an interleaver and the second latency path includes an interleaver.

21. The system of claim 19, wherein the first latency path includes an interleaver and the second latency path includes a deinterleaver.

22. The system of claim 19, wherein the first latency path includes a deinterleaver and the second latency path includes a deinterleaver.

23. The system of claim 19, further comprising means for transmitting to another transceiver information that is used to determine a maximum amount of shared memory that can be allocated.

24. The system of claim 19, further comprising means for receiving from another transceiver information that is used to determine a maximum amount of shared memory that can be allocated.

25. The system of claim 19, further comprising means for allocating a shared processing module to a plurality of coding and/or decoding modules.

26. The system of claim 19, wherein the allocating of at least one portion

of the shared memory is based on one or more communication parameters.

27. The system of claim 26, wherein at least one of the communication parameters is a data rate, a latency, an INP value or a bit error rate (BER).

28. A protocol for sharing resources in a transceiver comprising:
allocating a first portion of shared memory to a first latency path and
allocating a second portion of the shared memory to a second latency path.

29. The protocol of claim 28, wherein the first latency path includes an interleaver and the second latency path includes an interleaver.

30. The protocol of claim 28, wherein the first latency path includes an interleaver and the second latency path includes a deinterleaver.

31. The protocol of claim 28, wherein the first latency path includes a deinterleaver and the second latency path includes a deinterleaver.

32. The protocol of claim 28, further comprising transmitting to another transceiver information that is used to determine a maximum amount of shared memory that can be allocated.

33. The protocol of claim 28, further comprising receiving from another transceiver information that is used to determine a maximum amount of shared memory that can be allocated.

34. The protocol of claim 28, further comprising allocating a shared processing module to a plurality of coding and/or decoding modules.

35. The protocol of claim 28, wherein the allocating of at least one portion of the shared memory is based on one or more communication parameters.

36. The protocol of claim 35, wherein at least one of the communication parameters is a data rate, a latency, an INP value or a bit error rate (BER).

37. An information storage media having stored thereon information that when executed allows sharing of resources in a transceiver comprising:
information that allocates a first portion of shared memory to a first latency path and information that allocates a second portion of the shared memory to a second latency path.

38. The media of claim 37, wherein the first latency path includes an interleaver and the second latency path includes an interleaver.

39. The media of claim 37, wherein the first latency path includes an interleaver and the second latency path includes a deinterleaver.

40. The media of claim 37, wherein the first latency path includes a deinterleaver and the second latency path includes a deinterleaver.

41. The media of claim 37, further comprising information that transmits to another transceiver information that is used to determine a maximum amount of shared memory that can be allocated.

42. The media of claim 37, further comprising information that receives from another transceiver information that is used to determine a maximum amount of shared memory that can be allocated.

43. The media of claim 37, further comprising information that allocates a shared processing module to a plurality of coding and/or decoding modules.

44. The media of claim 37, wherein the allocating of at least one portion of

the shared memory is based on one or more communication parameters.

45. The media of claim 44, wherein at least one of the communication parameters is a data rate, a latency, an INP value or a bit error rate (BER).

ABSTRACT

A transceiver is designed to share memory and processing power amongst a plurality of transmitter and/or receiver latency paths, in a communications transceiver that carries or supports multiple applications. For example, the transmitter and/or receiver latency paths of the transceiver can share an interleaver/deinterleaver memory. This allocation can be done based on the data rate, latency, BER, impulse noise protection requirements of the application, data or information being transported over each latency path, or in general any parameter associated with the communications system.

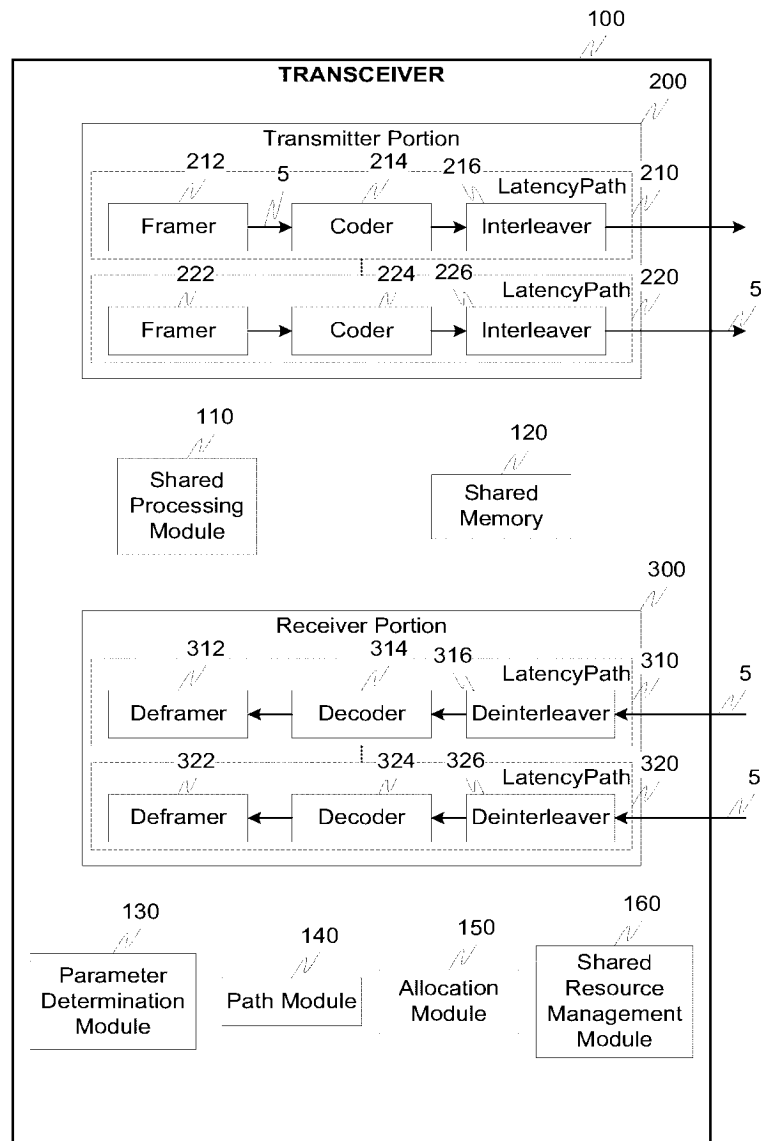


Fig. 1

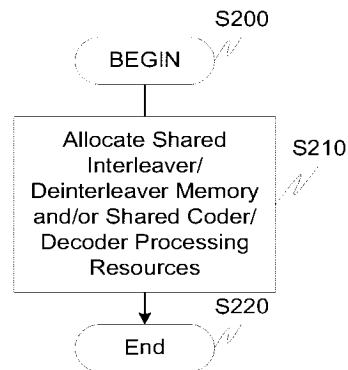


Fig. 2

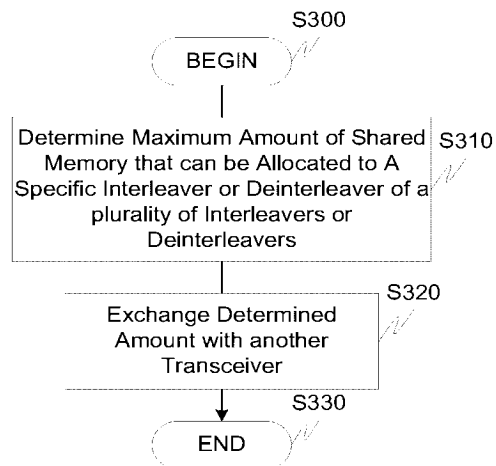


Fig. 3

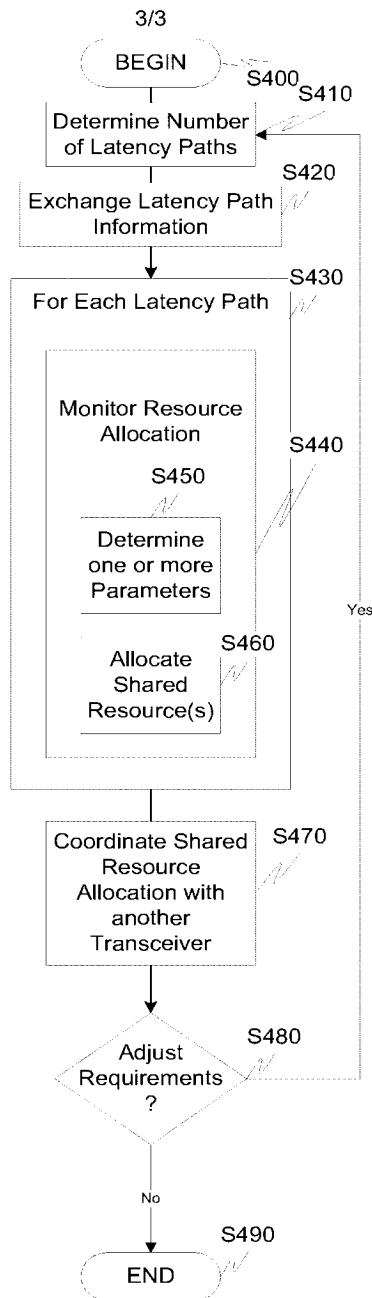


Fig. 4

RESOURCE SHARING IN A TELECOMMUNICATIONS ENVIRONMENT

RELATED APPLICATION DATA

[0001] This application is a Continuation of U.S. Application No. 12/761,586, filed April 16, 2010, which is a Continuation of U.S. Application No. 11/246,163 filed October 11, 2005, which ~~This application~~ claims the benefit of and priority under 35 U.S.C. § 119(e) to U.S. Patent Application No. 60/618,269, filed October 12, 2004, entitled “Sharing Memory and Processing Resources in DSL Systems,” each of which ~~are~~ is incorporated herein by reference in their~~its~~ entirety.

BACKGROUND

Field of the Invention

[0002] This invention generally relates to communication systems. More specifically, an exemplary embodiment of this invention relates to memory sharing in communication systems. Another exemplary embodiment relates to processing or coding resource sharing in a communication system.

Description of Related Art

[0003] U.S. Patent Nos. 6,775,320 and 6,778,589, ~~which are both incorporated herein by reference in their entirety,~~ describe DSL systems supporting multiple applications and multiple framer/coder/interleaver FCI blocks (an FCI block is also referred to as a latency path). DSL systems carry applications that have different transmission requirements with regard to, for example, data rate, latency (delay), bit error rate (BER), and the like. For example, video typically requires a low BER (<1E-10) but can tolerate higher latency (>20 ms). Voice, on the other hand, typically

requires a low latency (<1 ms) but can tolerate BER ($>1E-3$).

[0004] As described in U.S. Patent No. 6,775,320, different applications can use different latency paths in order to satisfy the different application requirements of the communication system. As a result a transceiver must support multiple latency paths in order to support applications such as video, Internet access and voice telephony. When implemented in a transceiver, each of the latency paths will have a framer, coder, and interleaver block with different capabilities that depend on the application requirements.

SUMMARY

[0005] One difficulty with implementing multiple latency paths in a transceiver is the fact that a latency path is a complicated digital circuit that requires a large amount of memory and processing power. An interleaver within a latency path can consume a large amount of memory in order to provide error correcting capability. For example, a typical DSL transceiver will have at least one latency path with approximately 16 kbytes of memory for the interleaver. Likewise, the coding block, for example, a Reed Solomon coder, consumes a large amount of processing power. In general, as the number of latency paths increase, the memory and processing power requirements for a communication system become larger.

[0006] Accordingly, an exemplary aspect of this invention relates to sharing memory between one or more interleavers and/or ~~deinterleavers~~ deinterleavers in a transceiver. More particularly, an exemplary aspect of this invention relates to shared

latency path memory in a transceiver.

[0007] Additional aspects of this invention relate to configuring and initializing shared memory in a communication system. More particularly, an exemplary aspect of this invention relates to configuring and initializing interleaver/deinterleaver memory in a communication system.

[0008] Additional aspects of the invention relate to determining the amount of memory that can be allocated to a particular component by a communication system. More specifically, an exemplary aspect of the invention relates to determining the maximum amount of shared memory that can be allocated to one or more interleaves or deinterleavers.

[0009] According to another exemplary aspect of the invention, processing power is shared between a number of transceiver modules. More specifically, and in accordance with an exemplary embodiment of the invention, a coding module is shared between one or more coders and/or decoders.

[0010] Another exemplary embodiment of the invention relates to transitioning from a fixed memory configuration to a shared memory configuration during one or more of initialization and SHOWTIME (user data transmission).

[0011] An additional exemplary aspect of the invention relates to dynamically updating one or more of shared memory and processing resources based on changing

communication conditions.

[0012] An additional exemplary aspect of the invention relates to updating one or more of shared memory and processing resources based on an updated communication parameter.

[0013] An additional exemplary aspect of the invention relates to updating the allocation of one or more of shared memory and processing resources based on an updated communication parameter(s).

[0014] Additional aspects of the invention relate to exchanging shared resource allocations between transceivers.

[0015] Additional exemplary aspects relate to a method of allocating shared memory in a transceiver comprising allocating the shared memory to a plurality of modules, wherein each of the plurality of modules comprise at least one interleaver, at least one deinterleaver or a combination thereof.

[0016] Still further aspects relate to the above method wherein the plurality of modules comprise interleavers.

[0017] Still further aspects relate to the above method wherein the plurality of modules comprise deinterleavers.

[0018] Still further aspects relate to the above method wherein the plurality of modules comprise at least one interleaver and at least one deinterleaver.

[0019] Additional exemplary aspects relate to a transceiver comprising a plurality

of modules each including at least one interleaver, at least one deinterleaver or a combination thereof and a shared memory designed to be allocated to a plurality of the modules.

[0020] Still further aspects relate to the above transceiver wherein the plurality of modules comprise interleavers.

[0021] Still further aspects relate to the above transceiver wherein the plurality of modules comprise deinterleavers.

[0022] Still further aspects relate to the above transceiver wherein the plurality of modules comprise at least one interleaver and at least one deinterleaver.

[0023] These and other features and advantages of this invention are described in, or are apparent from, the following description of the embodiments.

BRIEF DESCRIPTION OF THE DRAWINGS

[0024] The embodiments of the invention will be described in detail, with reference to the following figures, wherein:

[0025] Fig. 1 is a functional block diagram illustrating an exemplary transceiver according to this invention;

[0026] Fig. 2 is a flowchart outlining an exemplary method of sharing resources according to this invention;

[0027] Fig. 3 is a flowchart outlining an exemplary method of determining a maximum amount of shared memory according to this invention; and

[0028] Fig. 4 is a flowchart outlining an exemplary resource sharing methodology according to this invention.

DETAILED DESCRIPTION

[0029] The exemplary embodiments of this invention will be described in relation to sharing resources in a wired and/or wireless communications environment. However, it should be appreciated, that in general, the systems and methods of this invention will work equally well for any type of communication system in any environment.

[0030] The exemplary systems and methods of this invention will also be described in relation to multicarrier modems, such as DSL modems and VDSL modems, and associated communication hardware, software and communication channels. However, to avoid unnecessarily obscuring the present invention, the following description omits well-known structures and devices that may be shown in block diagram form or otherwise summarized.

[0031] For purposes of explanation, numerous details are set forth in order to provide a thorough understanding of the present invention. It should be appreciated however that the present invention may be practiced in a variety of ways beyond the specific details set forth herein.

[0032] Furthermore, while the exemplary embodiments illustrated herein show the various components of the system collocated, it is to be appreciated that the various components of the system can be located at distant portions of a distributed

network, such as a telecommunications network and/or the Internet, or within a dedicated secure, unsecured and/or encrypted system. Thus, it should be appreciated that the components of the system can be combined into one or more devices, such as a modem, or collocated on a particular node of a distributed network, such as a telecommunications network. As will be appreciated from the following description, and for reasons of computational efficiency, the components of the system can be arranged at any location within a distributed network without affecting the operation of the system. For example, the various components can be located in a Central Office modem (CO, ATU-C, VTU-O), a Customer Premises modem (CPE, ATU-R, VTU-R), a DSL management device, or some combination thereof. Similarly, one or more functional portions of the system could be distributed between a modem and an associated computing device.

[0033] Furthermore, it should be appreciated that the various links, including communications channel 5, connecting the elements can be wired or wireless links, or any combination thereof, or any other known or later developed element(s) that is capable of supplying and/or communicating data to and from the connected elements. The term module as used herein can refer to any known or later developed hardware, software, firmware, or combination thereof that is capable of performing the functionality associated with that element. The terms determine, calculate and compute, and variations thereof, as used herein are used interchangeably and include any type of methodology, process, mathematical operation or technique. FCI block and latency path are used interchangeably herein as well as transmitting modem and transmitting transceiver. Receiving modem and receiving transceiver are also used

interchangeably.

[0034] Fig. 1 illustrates an exemplary embodiment of a transceiver 100 that utilizes shared resources. It should be appreciated that numerous functional components of the transceiver have been omitted for clarity. However, the transceiver 100 can also include the standard components found in typical communications device(s) in which the technology of the subject invention is implemented into.

[0035] According to an exemplary embodiment of the invention, memory and processing power can be shared among a plurality of transmitter and/or receiver latency paths, in a communications transceiver that carries or supports multiple applications. For example, the transmitter and/or receiver latency paths of the transceiver can share an interleaver/deinterleaver memory and the shared memory can be allocated to the interleaver and/or deinterleaver of each latency path. This allocation can be done based on the data rate, latency, BER, impulse noise protection requirements of the application, data or information being transported over each latency path, or in general any parameter associated with the communications system.

[0036] Likewise, for example, the transmitter and/or receiver latency paths can share a Reed-Solomon coder/decoder processing module and the processing power of this module can be allocated to each encoder and/or decoder. This allocation can be done based on the data rate/latency, BER, impulse noise protection requirements of the application data or information being transported over each latency path, or in general based on any parameter associated with the communication system.

[0037] In accordance with an exemplary operational embodiment, a first transceiver and a second transceiver transmit to one another messages during, for example, initialization which contain information on the total and/or shared memory capabilities of each transceiver and optionally information about the one or more latency paths. This information can be transmitted prior to determining how to configure the latency paths to support the application requirements. Based on this information, one of the modems can select an FCI configuration parameter(s) that meets the transmission requirements of each application being transported over each latency paths. While an exemplary of the embodiment of the invention will be described in relation to the operation of the invention and characteristics thereof being established during initialization, it should be appreciated that the sharing of resources can be modified and messages transmitted between a two transceivers at any time during initialization and/or user data transmission, i.e., SHOWTIME.

[0038] Fig. 1 illustrates an exemplary embodiment of a transceiver 100. The transceiver 100 includes a transmitter portion 200 and a receiver portion 300. The transmitter portion 200 includes one or more latency paths 210, 220, ... Similarly, the receiver portion 300 includes one or more latency paths 310, 320, ... Each of the latency paths in the transmitter portion 200 includes a framer, coder, and interleaver designated as 212, 214, 216 and 222, 224 and 226, respectively. Each of the latency paths in the receiver portion includes a deframer, decoder, and deinterleaver designated as 312, 314, 316 and 322, 324, and 326, respectively. The transceiver 100 further includes a shared processing module 110, a shared memory 120, a parameter

determination module 130, a path module 140, an allocation module 150, and a shared resource management module 160, all interconnected by one or more links (not shown).

[0039] In this exemplary embodiment, the transceiver 100 is illustrated with four total transmitter portion and receiver portion latency paths, i.e., 210, 220, 310, and 320. The shared memory 120 is shared amongst the two transmitter portion interleavers 216 and 226 and two receiver portion deinterleavers 316 and 326. The shared processing module 110, such as a shared coding module, is shared between the two transmitter portion coders 214 and 224 and the two receiver portion decoders 314 and 324.

[0040] While the exemplary embodiment of the invention will be described in relation to a transceiver having a number of transmitter portion latency paths and receiver portion latency paths, it should be appreciated that this invention can be applied to any transceiver having any number of latency paths. Moreover, it should be appreciated that the sharing of resources can be allocated such that one or more of the transmitter portion latency paths are sharing a shared resource, one or more of the receiver portion latency paths are sharing a shared resource, or a portion of the transmitter portion latency paths and a portion of the receiver portion latency paths are sharing shared resources. Moreover, any one or more of the latency paths, or portions thereof, could also be assigned to a fixed resource while, for example, another portion of the latency path(s) assigned to a shared resource. For example, in latency path 210, the interleaver 216 could be allocated a portion of the shared

memory 120, while the coder 214 could be allocated to a dedicated processing module, vice versa, or the like.

[0041] In accordance with the exemplary embodiment, a plurality of transmitter portion or receiver portion latency paths share an interleaver/deinterleaver memory, such as shared memory 120, and a coding module, such as shared processing module 110. For example, the interleaver/deinterleaver memory can be allocated to different interleavers and/or deinterleavers. This allocation can be based on parameters associated with the communication systems such as data rate, latency, BER, impulse noise protection, and the like, of the applications being transported. Similarly, a coding module, which can be a portion of the shared processing module 110, can be shared between any one or more of the latency paths. This sharing can be based on requirements such as data rate, latency, BER, impulse noise protection, and the like, of the applications being transported.

[0042] For example, an exemplary transceiver could comprise a shared interleaver/deinterleaver memory and could be designed to allocate a first portion of the shared memory 120 to an interleaver, such as interleaver 216 in the transmitter portion of the transceiver and allocate a second portion of the shared memory 120 to a deinterleaver, such as 316, in the receiver portion of the transceiver.

[0043] Alternatively, for example, an exemplary transceiver can comprise a shared interleaver/deinterleaver memory, such as shared memory 120, and be designed to allocate a first portion of shared memory 120 to a first interleaver, e.g.,

216, in the transmitter portion of the transceiver and allocate a second portion of the shared memory to a second interleaver, e.g., 226, in the transmitter portion of the transceiver.

[0044] Alternatively, for example, an exemplary transceiver can comprise a shared interleaver/deinterleaver memory and be designed to allocate a first portion of the shared memory 120 to a first deinterleaver, e.g., 316, in the receiver portion of the transceiver and allocate a second portion of the shared memory to a second deinterleaver, e.g., 326, in the receiver portion of the transceiver. Regardless of the configuration, in general any interleaver or deinterleaver, or grouping thereof, be it in a transmitter portion or receiver portion of the transceiver, can be associated with a portion of the shared memory 120.

[0045] Establishment, configuration and usage of shared resources is performed in the following exemplary manner. First, and in cooperation with the path module 140, the number of transmitter and receiver latency paths (N) is determined. The parameter determination module 130 then analyses one or more parameters such as data rate, transmitter data rate, receiver data rate, impulse noise protection, bit error rate, latency, or the like. Based on one or more of these parameters, the allocation module 150 allocates a portion of the shared memory 120 to one or more of the interleaver and/or deinterleavers, or groupings thereof. This process continues until the memory allocation has been determined and assigned to each of the N latency paths.

[0046] Having determined the memory allocation for each of the latency paths, and in conjunction with the shared resource management 160, the transceiver 100 transmits to a second transceiver one or more of the number of latency paths (N), the maximum interleaver memory for any one or more of the latency paths and/or the maximum total and/or shared memory for all of the latency paths.

[0047] Three examples of sharing interleaver/deinterleaver memory and coding processing in a transceiver are described below. The latency paths in these examples can be in the transmitter portion of the transceiver or the receiver portion of the transceiver.

[0048] Example #1

A first transmitter portion or receiver portion latency path may carry data from a video application, which needs a very low BER but can tolerate higher latency. In this case, the video will be transported using an latency path that has a large amount of interleaving/deinterleaving and coding (also known as Forward Error Correction (FEC) coding). For example, the latency path may be configured with Reed-Solomon coding using a codeword size of 255 bytes (N=255) with 16 checkbytes (R=16) and interleaving/deinterleaving using an interleaver depth of 64 (D=64). This latency path will require $N \cdot D = 16 \cdot 255 = 16\text{Kbytes}$ ~~$N \cdot D = 255 \cdot 64 = 16\text{Kbytes}$~~ of interleaver memory at the transmitter (or de-interleaver memory at the receiver). This latency path will be able to correct a burst of errors that is less than 512 bytes in duration.

[0049] A second transmitter portion or receiver portion latency path may carry an

internet access application that requires a medium BER and a medium amount of latency. In this case, the internet access application will be transported using a latency path that has a medium amount of interleaving and coding. For example, the latency path may be configured with Reed-Solomon coding using a codeword size of 128 bytes ($N=128$) with 8 checkbytes ($R=8$) and interleaving using an interleaver depth of 16 ($D=32$). This latency path will require $N*D=128*32=4$ Kbytes of interleaver memory and the same amount of deinterleaver memory. This latency path will be able to correct a burst of errors that is less than 128 bytes in duration.

[0050] A third transmitter portion or receiver portion latency path may carry a voice telephony application, which needs a very low latency but can tolerate BER. In this case, the video will be transported using a latency path that has a large amount of interleaving and coding. For example, the third transmitter portion or receiver portion latency path may be configured with no interleaving or coding which will result in the lowest possible latency through the latency path but will provide no error correction capability.

[0051] According to the principles of this invention, a system carrying the three applications described above in Example #1, would have three latency paths that share one memory space containing at least $(16+4)=20$ Kbytes. The three latency paths also share a common coding block that is able to simultaneously encode (in the transmitter portion) or decode (in a receiver portion) two codewords with $N=255/R=16$ and $N=128/R=8$.

[0052] According to an exemplary embodiment of this invention, the latency paths can be reconfigured at initialization or during data transmission mode (also known as SHOWTIME in ADSL and VDSL transceivers). This would occur if, for example, the applications or application requirements were to change.

[0053] Example #2

If instead of 1 video application, 1 internet application and 1 voice application, there were 3 internet access applications then the transmitter portion and/or receiver portion latency paths would be reconfigured to utilize the shared memory and coding module in a different way. For example, the system could be reconfigured to have 3 transmitter portion or receiver portion latency paths, with each latency path being configured with Reed-Solomon coding using a codeword size of 128 bytes ($N=128$) with 8 checkbytes ($R=8$) and interleaving using an interleaver depth of 16 ($D=32$). Each latency path will require $N*D=128*32=4\text{Kbytes}$ of interleaver memory and each block will be able to correct a burst of errors that is less than 128 bytes in duration. Based on the example of carrying the three internet access applications described, the three latency path share one memory space containing at least $3*4=12\text{ Kbytes}$. Also the three latency paths share a common coding block that is able to simultaneously encode (on the transmitter side) or decode (on the receiver side) three codewords with $N=128/R=16$, $N=128/R=8$ and $N=128/R=8$.

[0054] Example #3

The system could be configured to carry yet another set of applications. For example, the latency paths could be configured to carry 2 video applications. In this case only

2 transmitter portion or receiver portion latency paths are needed, which means that the third latency path could be simply disabled. Also, assuming that the memory is constrained based on the first example above, then the maximum shared memory for these 2 latency paths is 20 kBytes. In this case, the system could be reconfigured to have 2 latency paths, with each block being configured with Reed-Solomon coding using a codeword size of 200 bytes ($N=200$) with 10 checkbytes ($R=10$) and interleaving/deinterleaving using an interleaver depth of 50 ($D=50$). Each latency path will require $N*D=200*50=10\text{Kbytes}$ of interleaver memory and each block will be able to correct a burst of errors that is less than 250 bytes in duration. This configuration results in 20K of shared memory for both latency paths, which is the same as in the first example. In order to stay within the memory constraints of the latency paths, the error correction capability for each latency path is decreased to 250 bytes from 512 bytes in Example #1.

[0055] Another aspect of this invention is the how FCI configuration information is transmitted between a first modem and a second modem. FCI configuration information will depend on the requirements of the applications being transported over the DSL connection. This information may need to be forwarded during initialization in order to initially configure the DSL connection. This information may also need to be forwarded during SHOWTIME in order to reconfigure the DSL connection based on a change in applications or the application requirements.

[0056] According to one embodiment, a first modem determines the specific FCI configuration parameters, e.g., N , D , R as defined above, needed to meet specific

application requirements, such as latency, burst error correction capability, etc. In order to determine the FCI configuration parameters, the first modem must know what are the capabilities of a second modem. For example, the first modem must know how many latency paths (FCI blocks) the second modem can support. Also the first modem must know the maximum amount of interleaver memory for each transmitter latency path. In addition, since the transmitter latency paths may share a common memory space the first modem must know the total shared memory for all transmitter latency paths. This way the first modem will be able to choose a configuration that can meet application requirements and also meet the transmitter portion latency path capabilities of the second modem.

[0057] For example, using values from examples above, a first transceiver could send a message to a second transceiver during initialization or during SHOWTIME containing the following information:

- Number of supported transmitter and receiver latency paths = 3
- Max Interleaver Memory for latency path #1= 16 Kbytes
- Max Interleaver Memory for latency path #2= 16 Kbytes
- Max Interleaver Memory for latency path #3= 16 Kbytes
- Maximum total/shared memory for all latency paths = 20 kBytes

Based on this information, and the application requirements, the first transceiver would select latency path settings. For example, if the applications are 1 video, 1 internet access and 1 voice application, the first transceiver could configure 3 latency paths as follows:

latency path #1 – Video: N=255, R=16, D=64

latency path #2 – Video: $N=128$, $R=8$, $D=32$

latency path #3 – Video: $N=0$, $R=0$, $D=1$ (no coding or interleaving)

[0058] This would result in a total interleaver memory of 20 kbytes.

[0059] Alternatively, if for example, there are only 2 video applications, the first transceiver could configure 2 latency paths as follows:

latency path #1 – Video: $N=200$, $R=10$, $D=50$

latency path #2 – Video: $N=200$, $R=10$, $D=50$

latency path #3 – Video: $N=0$, $R=0$, $D=1$ (no coding or interleaving)

[0060] This would also result in a total interleaver memory of 20 kbytes.

[0061] Alternatively, the second transceiver can determine the specific FCI configuration parameters, e.g., N , D , R as defined above, needed to meet specific application requirements, such as latency, burst error correction capability, etc. As described above for the first transceiver, in order to determine the FCI configuration parameters, the second transceiver must first know what are the capabilities of the first transceiver. In this case, the first transceiver would send a message to the second transceiver containing the information described above and based on this information and the application requirements the second transceiver would select latency path settings.

[0062] Fig. 2 outlines an exemplary method of allocating shared memory in a

transceiver. More specifically, control begins in step S200 and continues to step S210. In step S210, one or more of shared interleaver/deinterleaver memory and/or shared coder/decoder processing resources are allocated to one or more latency paths, in a transceiver. Control then continues to step S220 where the control sequence ends.

[0063] Fig. 3 outlines an exemplary method of exchanging shared resource allocations according to an exemplary embodiment of this invention. In particular, control begins in step S310. In step S310, a maximum amount of shared memory that can be allocated to a specific interleaver or deinterleaver of a plurality of interleavers or deinterleavers in a transceiver is determined. Next, in step S320, the determined maximum amount for one or more of the deinterleavers and/or interleavers is transmitted to another transceiver. Messages containing additional information can also be transmitted to the other transceiver and/or received from the other transceiver. Control then continues to step S330 where the control sequence ends.

[0064] Fig. 4 outlines an exemplary procedure for resource sharing according to an exemplary embodiment of this invention. In particular, control begins in step S400 and continues to step S410. In step S410, the number of latency paths are determined. Then, in step S420, the latency path information (FCI block information) is transmitted to another transceiver. Messages containing additional information can also be transmitted to the other transceiver and/or received from the other transceiver. This information can be used to, for example, assist with the determination of memory allocation in the transceiver. Moreover, the messages received from the

other transceiver could specify what the memory allocation is to be based on, for example, the number of latency paths, memory allocation in the remote transceiver and required applications. Control then continues to step S430.

[0065] In step S430, and for each latency path, the steps in step 440 are performed.

[0066] In step S440, and while monitoring of allocation of resources is being performed, steps 450 and 460 are performed. More specifically, in step S450, one or more parameters associated with the communication system are determined. Then, in step S460, shared resources are allocated based on one or more of the communication parameters. Control then continues to step S470.

[0067] In step S470, the allocation of shared resources is communicated to another transceiver. Next, in step S480, a determination is made as to whether there is a change in communications that would require the adjustment of the shared resource allocation. Examples of changes in communications conditions include a change in applications being transported over the system and/or changes in the channel condition, etc. If adjustments are required, control jumps back to step S410. Otherwise, control jumps to step S490 where the control sequence ends.

[0068] The above-described system can be implemented on wired and/or wireless telecommunications devices, such a modem, a multicarrier modem, a DSL modem, an ADSL modem, an XDSL modem, a VDSL modem, a linecard, test equipment, a

multicarrier transceiver, a wired and/or wireless wide/local area network system, a satellite communication system, a modem equipped with diagnostic capabilities, or the like, or on a separate programmed general purpose computer having a communications device or in conjunction with any of the following communications protocols: CDSL, ADSL2, ADSL2+, VDSL1, VDSL2, HDSL, DSL Lite, IDSL, RADSL, SDSL, UDSL or the like.

[0069] Additionally, the systems, methods and protocols of this invention can be implemented on a special purpose computer, a programmed microprocessor or microcontroller and peripheral integrated circuit element(s), an ASIC or other integrated circuit, a digital signal processor, a hard-wired electronic or logic circuit such as discrete element circuit, a programmable logic device such as PLD, PLA, FPGA, PAL, a modem, a transmitter/receiver, any comparable means, or the like. In general, any device capable of implementing a state machine that is in turn capable of implementing the methodology illustrated herein can be used to implement the various communication methods, protocols and techniques according to this invention.

[0070] Furthermore, the disclosed methods may be readily implemented in software using object or object-oriented software development environments that provide portable source code that can be used on a variety of computer or workstation platforms. Alternatively, the disclosed system may be implemented partially or fully in hardware using standard logic circuits or VLSI design. Whether software or hardware is used to implement the systems in accordance with this invention is

dependent on the speed and/or efficiency requirements of the system, the particular function, and the particular software or hardware systems or microprocessor or microcomputer systems being utilized. The communication systems, methods and protocols illustrated herein can be readily implemented in hardware and/or software using any known or later developed systems or structures, devices and/or software by those of ordinary skill in the applicable art from the functional description provided herein and with a general basic knowledge of the computer and telecommunications arts.

[0071] Moreover, the disclosed methods may be readily implemented in software that can be stored on a storage medium, executed on programmed general-purpose computer with the cooperation of a controller and memory, a special purpose computer, a microprocessor, or the like. In these instances, the systems and methods of this invention can be implemented as program embedded on personal computer such as an applet, JAVA® or CGI script, as a resource residing on a server or computer workstation, as a routine embedded in a dedicated communication system or system component, or the like. The system can also be implemented by physically incorporating the system and/or method into a software and/or hardware system, such as the hardware and software systems of a communications transceiver.

[0072] It is therefore apparent that there has been provided, in accordance with the present invention, systems and methods for sharing resources. While this invention has been described in conjunction with a number of embodiments, it is evident that many alternatives, modifications and variations would be or are apparent

to those of ordinary skill in the applicable arts. Accordingly, it is intended to embrace all such alternatives, modifications, equivalents and variations that are within the spirit and scope of this invention.

ABSTRACT

A transceiver is designed to share memory and processing power amongst a plurality of transmitter and/or receiver latency paths, in a communications transceiver that carries or supports multiple applications. For example, the transmitter and/or receiver latency paths of the transceiver can share an interleaver/deinterleaver memory. This allocation can be done based on the data rate, latency, BER, impulse noise protection requirements of the application, data or information being transported over each latency path, or in general any parameter associated with the communications system.

RESOURCE SHARING IN A TELECOMMUNICATIONS ENVIRONMENT

RELATED APPLICATION DATA

[0001] This application is a Continuation of U.S. Application No. 12/761,586, filed April 16, 2010, which is a Continuation of U.S. Application No. 11/246,163 filed October 11, 2005, which claims the benefit of and priority under 35 U.S.C. § 119(e) to U.S. Patent Application No. 60/618,269, filed October 12, 2004, entitled “Sharing Memory and Processing Resources in DSL Systems,” each of which are incorporated herein by reference in their entirety.

BACKGROUND

Field of the Invention

[0002] This invention generally relates to communication systems. More specifically, an exemplary embodiment of this invention relates to memory sharing in communication systems. Another exemplary embodiment relates to processing or coding resource sharing in a communication system.

Description of Related Art

[0003] U.S. Patent Nos. 6,775,320 and 6,778,589 describe DSL systems supporting multiple applications and multiple framer/coder/interleaver FCI blocks (an FCI block is also referred to as a latency path). DSL systems carry applications that have different transmission requirements with regard to, for example, data rate, latency (delay), bit error rate (BER), and the like. For example, video typically requires a low BER ($<1E-10$) but can tolerate higher latency (>20 ms). Voice, on the other hand, typically requires a low latency (<1 ms) but can tolerate BER ($>1E-3$).

[0004] As described in U.S. Patent No. 6,775,320, different applications can use different latency paths in order to satisfy the different application requirements of the communication system. As a result a transceiver must support multiple latency paths in order to support applications such as video, Internet access and voice telephony. When implemented in a transceiver, each of the latency paths will have a framer, coder, and interleaver block with different capabilities that depend on the application requirements.

SUMMARY

[0005] One difficulty with implementing multiple latency paths in a transceiver is the fact that a latency path is a complicated digital circuit that requires a large amount of memory and processing power. An interleaver within a latency path can consume a large amount of memory in order to provide error correcting capability. For example, a typical DSL transceiver will have at least one latency path with approximately 16 kbytes of memory for the interleaver. Likewise, the coding block, for example, a Reed Solomon coder, consumes a large amount of processing power. In general, as the number of latency paths increase, the memory and processing power requirements for a communication system become larger.

[0006] Accordingly, an exemplary aspect of this invention relates to sharing memory between one or more interleavers and/or deinterleavers in a transceiver. More particularly, an exemplary aspect of this invention relates to shared latency path memory in a transceiver.

[0007] Additional aspects of this invention relate to configuring and initializing shared memory in a communication system. More particularly, an exemplary aspect of this invention relates to configuring and initializing interleaver/deinterleaver memory in a communication system.

[0008] Additional aspects of the invention relate to determining the amount of memory that can be allocated to a particular component by a communication system. More specifically, an exemplary aspect of the invention relates to determining the maximum amount of shared memory that can be allocated to one or more interleaves or deinterleavers.

[0009] According to another exemplary aspect of the invention, processing power is shared between a number of transceiver modules. More specifically, and in accordance with an exemplary embodiment of the invention, a coding module is shared between one or more coders and/or decoders.

[0010] Another exemplary embodiment of the invention relates to transitioning from a fixed memory configuration to a shared memory configuration during one or more of initialization and SHOWTIME (user data transmission).

[0011] An additional exemplary aspect of the invention relates to dynamically updating one or more of shared memory and processing resources based on changing communication conditions.

[0012] An additional exemplary aspect of the invention relates to updating one or more of shared memory and processing resources based on an updated communication parameter.

[0013] An additional exemplary aspect of the invention relates to updating the allocation of one or more of shared memory and processing resources based on an updated communication parameter(s).

[0014] Additional aspects of the invention relate to exchanging shared resource allocations between transceivers.

[0015] Additional exemplary aspects relate to a method of allocating shared memory in a transceiver comprising allocating the shared memory to a plurality of modules, wherein each of the plurality of modules comprise at least one interleaver, at least one deinterleaver or a combination thereof.

[0016] Still further aspects relate to the above method wherein the plurality of modules comprise interleavers.

[0017] Still further aspects relate to the above method wherein the plurality of modules comprise deinterleavers.

[0018] Still further aspects relate to the above method wherein the plurality of modules comprise at least one interleaver and at least one deinterleaver.

[0019] Additional exemplary aspects relate to a transceiver comprising a plurality of modules each including at least one interleaver, at least one deinterleaver or a

combination thereof and a shared memory designed to be allocated to a plurality of the modules.

[0020] Still further aspects relate to the above transceiver wherein the plurality of modules comprise interleavers.

[0021] Still further aspects relate to the above transceiver wherein the plurality of modules comprise deinterleavers.

[0022] Still further aspects relate to the above transceiver wherein the plurality of modules comprise at least one interleaver and at least one deinterleaver.

[0023] These and other features and advantages of this invention are described in, or are apparent from, the following description of the embodiments.

BRIEF DESCRIPTION OF THE DRAWINGS

[0024] The embodiments of the invention will be described in detail, with reference to the following figures, wherein:

[0025] Fig. 1 is a functional block diagram illustrating an exemplary transceiver according to this invention;

[0026] Fig. 2 is a flowchart outlining an exemplary method of sharing resources according to this invention;

[0027] Fig. 3 is a flowchart outlining an exemplary method of determining a maximum amount of shared memory according to this invention; and

[0028] Fig. 4 is a flowchart outlining an exemplary resource sharing methodology according to this invention.

DETAILED DESCRIPTION

[0029] The exemplary embodiments of this invention will be described in relation to sharing resources in a wired and/or wireless communications environment. However, it should be appreciated, that in general, the systems and methods of this invention will work equally well for any type of communication system in any environment.

[0030] The exemplary systems and methods of this invention will also be described in relation to multicarrier modems, such as DSL modems and VDSL modems, and associated communication hardware, software and communication channels. However, to avoid unnecessarily obscuring the present invention, the following description omits well-known structures and devices that may be shown in block diagram form or otherwise summarized.

[0031] For purposes of explanation, numerous details are set forth in order to provide a thorough understanding of the present invention. It should be appreciated however that the present invention may be practiced in a variety of ways beyond the specific details set forth herein.

[0032] Furthermore, while the exemplary embodiments illustrated herein show the various components of the system collocated, it is to be appreciated that the various components of the system can be located at distant portions of a distributed network, such as a telecommunications network and/or the Internet, or within a

dedicated secure, unsecured and/or encrypted system. Thus, it should be appreciated that the components of the system can be combined into one or more devices, such as a modem, or collocated on a particular node of a distributed network, such as a telecommunications network. As will be appreciated from the following description, and for reasons of computational efficiency, the components of the system can be arranged at any location within a distributed network without affecting the operation of the system. For example, the various components can be located in a Central Office modem (CO, ATU-C, VTU-O), a Customer Premises modem (CPE, ATU-R, VTU-R), a DSL management device, or some combination thereof. Similarly, one or more functional portions of the system could be distributed between a modem and an associated computing device.

[0033] Furthermore, it should be appreciated that the various links, including communications channel 5, connecting the elements can be wired or wireless links, or any combination thereof, or any other known or later developed element(s) that is capable of supplying and/or communicating data to and from the connected elements. The term module as used herein can refer to any known or later developed hardware, software, firmware, or combination thereof that is capable of performing the functionality associated with that element. The terms determine, calculate and compute, and variations thereof, as used herein are used interchangeably and include any type of methodology, process, mathematical operation or technique. FCI block and latency path are used interchangeably herein as well as transmitting modem and transmitting transceiver. Receiving modem and receiving transceiver are also used interchangeably.

[0034] Fig. 1 illustrates an exemplary embodiment of a transceiver 100 that utilizes shared resources. It should be appreciated that numerous functional components of the transceiver have been omitted for clarity. However, the transceiver 100 can also include the standard components found in typical communications device(s) in which the technology of the subject invention is implemented into.

[0035] According to an exemplary embodiment of the invention, memory and processing power can be shared among a plurality of transmitter and/or receiver latency paths, in a communications transceiver that carries or supports multiple applications. For example, the transmitter and/or receiver latency paths of the transceiver can share an interleaver/deinterleaver memory and the shared memory can be allocated to the interleaver and/or deinterleaver of each latency path. This allocation can be done based on the data rate, latency, BER, impulse noise protection requirements of the application, data or information being transported over each latency path, or in general any parameter associated with the communications system.

[0036] Likewise, for example, the transmitter and/or receiver latency paths can share a Reed-Solomon coder/decoder processing module and the processing power of this module can be allocated to each encoder and/or decoder. This allocation can be done based on the data rate/latency, BER, impulse noise protection requirements of the application data or information being transported over each latency path, or in general based on any parameter associated with the communication system.

[0037] In accordance with an exemplary operational embodiment, a first transceiver and a second transceiver transmit to one another messages during, for example, initialization which contain information on the total and/or shared memory capabilities of each transceiver and optionally information about the one or more latency paths. This information can be transmitted prior to determining how to configure the latency paths to support the application requirements. Based on this information, one of the modems can select an FCI configuration parameter(s) that meets the transmission requirements of each application being transported over each latency paths. While an exemplary of the embodiment of the invention will be described in relation to the operation of the invention and characteristics thereof being established during initialization, it should be appreciated that the sharing of resources can be modified and messages transmitted between a two transceivers at any time during initialization and/or user data transmission, i.e., SHOWTIME.

[0038] Fig. 1 illustrates an exemplary embodiment of a transceiver 100. The transceiver 100 includes a transmitter portion 200 and a receiver portion 300. The transmitter portion 200 includes one or more latency paths 210, 220, ... Similarly, the receiver portion 300 includes one or more latency paths 310, 320, ... Each of the latency paths in the transmitter portion 200 includes a framer, coder, and interleaver designated as 212, 214, 216 and 222, 224 and 226, respectively. Each of the latency paths in the receiver portion includes a deframer, decoder, and deinterleaver designated as 312, 314, 316 and 322, 324, and 326, respectively. The transceiver 100 further includes a shared processing module 110, a shared memory 120, a parameter determination module 130, a path module 140, an allocation module 150, and a shared

resource management module 160, all interconnected by one or more links (not shown).

[0039] In this exemplary embodiment, the transceiver 100 is illustrated with four total transmitter portion and receiver portion latency paths, i.e., 210, 220, 310, and 320. The shared memory 120 is shared amongst the two transmitter portion interleavers 216 and 226 and two receiver portion deinterleavers 316 and 326. The shared processing module 110, such as a shared coding module, is shared between the two transmitter portion coders 214 and 224 and the two receiver portion decoders 314 and 324.

[0040] While the exemplary embodiment of the invention will be described in relation to a transceiver having a number of transmitter portion latency paths and receiver portion latency paths, it should be appreciated that this invention can be applied to any transceiver having any number of latency paths. Moreover, it should be appreciated that the sharing of resources can be allocated such that one or more of the transmitter portion latency paths are sharing a shared resource, one or more of the receiver portion latency paths are sharing a shared resource, or a portion of the transmitter portion latency paths and a portion of the receiver portion latency paths are sharing shared resources. Moreover, any one or more of the latency paths, or portions thereof, could also be assigned to a fixed resource while, for example, another portion of the latency path(s) assigned to a shared resource. For example, in latency path 210, the interleaver 216 could be allocated a portion of the shared memory 120, while the coder 214 could be allocated to a dedicated processing

module, vice versa, or the like.

[0041] In accordance with the exemplary embodiment, a plurality of transmitter portion or receiver portion latency paths share an interleaver/deinterleaver memory, such as shared memory 120, and a coding module, such as shared processing module 110. For example, the interleaver/deinterleaver memory can be allocated to different interleavers and/or deinterleavers. This allocation can be based on parameters associated with the communication systems such as data rate, latency, BER, impulse noise protection, and the like, of the applications being transported. Similarly, a coding module, which can be a portion of the shared processing module 110, can be shared between any one or more of the latency paths. This sharing can be based on requirements such as data rate, latency, BER, impulse noise protection, and the like, of the applications being transported.

[0042] For example, an exemplary transceiver could comprise a shared interleaver/deinterleaver memory and could be designed to allocate a first portion of the shared memory 120 to an interleaver, such as interleaver 216 in the transmitter portion of the transceiver and allocate a second portion of the shared memory 120 to a deinterleaver, such as 316, in the receiver portion of the transceiver.

[0043] Alternatively, for example, an exemplary transceiver can comprise a shared interleaver/deinterleaver memory, such as shared memory 120, and be designed to allocate a first portion of shared memory 120 to a first interleaver, e.g., 216, in the transmitter portion of the transceiver and allocate a second portion of the

shared memory to a second interleaver, e.g., 226, in the transmitter portion of the transceiver.

[0044] Alternatively, for example, an exemplary transceiver can comprise a shared interleaver/deinterleaver memory and be designed to allocate a first portion of the shared memory 120 to a first deinterleaver, e.g., 316, in the receiver portion of the transceiver and allocate a second portion of the shared memory to a second deinterleaver, e.g., 326, in the receiver portion of the transceiver. Regardless of the configuration, in general any interleaver or deinterleaver, or grouping thereof, be it in a transmitter portion or receiver portion of the transceiver, can be associated with a portion of the shared memory 120.

[0045] Establishment, configuration and usage of shared resources is performed in the following exemplary manner. First, and in cooperation with the path module 140, the number of transmitter and receiver latency paths (N) is determined. The parameter determination module 130 then analyses one or more parameters such as data rate, transmitter data rate, receiver data rate, impulse noise protection, bit error rate, latency, or the like. Based on one or more of these parameters, the allocation module 150 allocates a portion of the shared memory 120 to one or more of the interleaver and/or deinterleavers, or groupings thereof. This process continues until the memory allocation has been determined and assigned to each of the N latency paths.

[0046] Having determined the memory allocation for each of the latency paths,

and in conjunction with the shared resource management 160, the transceiver 100 transmits to a second transceiver one or more of the number of latency paths (N), the maximum interleaver memory for any one or more of the latency paths and/or the maximum total and/or shared memory for all of the latency paths.

[0047] Three examples of sharing interleaver/deinterleaver memory and coding processing in a transceiver are described below. The latency paths in these examples can be in the transmitter portion of the transceiver or the receiver portion of the transceiver.

[0048] Example #1

A first transmitter portion or receiver portion latency path may carry data from a video application, which needs a very low BER but can tolerate higher latency. In this case, the video will be transported using an latency path that has a large amount of interleaving/deinterleaving and coding (also known as Forward Error Correction (FEC) coding). For example, the latency path may be configured with Reed-Solomon coding using a codeword size of 255 bytes ($N=255$) with 16 checkbytes ($R=16$) and interleaving/deinterleaving using an interleaver depth of 64 ($D=64$). This latency path will require $N*D=255*64=16\text{Kbytes}$ of interleaver memory at the transmitter (or de-interleaver memory at the receiver). This latency path will be able to correct a burst of errors that is less than 512 bytes in duration.

[0049] A second transmitter portion or receiver portion latency path may carry an internet access application that requires a medium BER and a medium amount of

latency. In this case, the internet access application will be transported using a latency path that has a medium amount of interleaving and coding. For example, the latency path may be configured with Reed-Solomon coding using a codeword size of 128 bytes ($N=128$) with 8 checkbytes ($R=8$) and interleaving using an interleaver depth of 16 ($D=32$). This latency path will require $N*D=128*32=4\text{Kbytes}$ of interleaver memory and the same amount of deinterleaver memory. This latency path will be able to correct a burst of errors that is less than 128 bytes in duration.

[0050] A third transmitter portion or receiver portion latency path may carry a voice telephony application, which needs a very low latency but can tolerate BER. In this case, the video will be transported using an latency path that has a large amount of interleaving and coding. For example, the third transmitter portion or receiver portion latency path may be configured with no interleaving or coding which will result in the lowest possible latency through the latency path but will provide no error correction capability.

[0051] According to the principles of this invention, a system carrying the three applications described above in Example #1, would have three latency paths that share one memory space containing at least $(16+4)=20$ Kbytes. The three latency paths also share a common coding block that is able to simultaneously encode (in the transmitter portion) or decode (in a receiver portion) two codewords with $N=255/R=16$ and $N=128/R=8$.

[0052] According to an exemplary embodiment of this invention, the latency

paths can be reconfigured at initialization or during data transmission mode (also known as SHOWTIME in ADSL and VDSL transceivers). This would occur if, for example, the applications or application requirements were to change.

[0053] Example #2

If instead of 1 video application, 1 internet application and 1 voice application, there were 3 internet access applications then the transmitter portion and/or receiver portion latency paths would be reconfigured to utilize the shared memory and coding module in a different way. For example, the system could be reconfigured to have 3 transmitter portion or receiver portion latency paths, with each latency path being configured with Reed-Solomon coding using a codeword size of 128 bytes ($N=128$) with 8 checkbytes ($R=8$) and interleaving using an interleaver depth of 16 ($D=32$). Each latency path will require $N*D=128*32=4$ Kbytes of interleaver memory and each block will be able to correct a burst of errors that is less than 128 bytes in duration. Based on the example of carrying the three internet access applications described, the three latency path share one memory space containing at least $3*4=12$ Kbytes. Also the three latency paths share a common coding block that is able to simultaneously encode (on the transmitter side) or decode (on the receiver side) three codewords with $N=128/R=16$, $N=128/R=8$ and $N=128/R=8$.

[0054] Example #3

The system could be configured to carry yet another set of applications. For example, the latency paths could be configured to carry 2 video applications. In this case only 2 transmitter portion or receiver portion latency paths are needed, which means that

the third latency path could be simply disabled. Also, assuming that the memory is constrained based on the first example above, then the maximum shared memory for these 2 latency paths is 20 kBytes. In this case, the system could be reconfigured to have 2 latency paths, with each block being configured with Reed-Solomon coding using a codeword size of 200 bytes ($N=200$) with 10 checkbytes ($R=10$) and interleaving/deinterleaving using an interleaver depth of 50 ($D=50$). Each latency path will require $N*D=200*50=10\text{Kbytes}$ of interleaver memory and each block will be able to correct a burst of errors that is less than 250 bytes in duration. This configuration results in 20K of shared memory for both latency paths, which is the same as in the first example. In order to stay within the memory constraints of the latency paths, the error correction capability for each latency path is decreased to 250 bytes from 512 bytes in Example #1.

[0055] Another aspect of this invention is the how FCI configuration information is transmitted between a first modem and a second modem. FCI configuration information will depend on the requirements of the applications being transported over the DSL connection. This information may need to be forwarded during initialization in order to initially configure the DSL connection. This information may also need to be forwarded during SHOWTIME in order to reconfigure the DSL connection based on a change in applications or the application requirements.

[0056] According to one embodiment, a first modem determines the specific FCI configuration parameters, e.g., N , D , R as defined above, needed to meet specific application requirements, such as latency, burst error correction capability, etc. In

order to determine the FCI configuration parameters, the first modem must know what are the capabilities of a second modem. For example, the first modem must know how many latency paths (FCI blocks) the second modem can support. Also the first modem must know the maximum amount of interleaver memory for each transmitter latency path. In addition, since the transmitter latency paths may share a common memory space the first modem must know the total shared memory for all transmitter latency paths. This way the first modem will be able to choose a configuration that can meet application requirements and also meet the transmitter portion latency path capabilities of the second modem.

[0057] For example, using values from examples above, a first transceiver could send a message to a second transceiver during initialization or during SHOWTIME containing the following information:

- Number of supported transmitter and receiver latency paths = 3
- Max Interleaver Memory for latency path #1= 16 Kbytes
- Max Interleaver Memory for latency path #2= 16 Kbytes
- Max Interleaver Memory for latency path #3= 16 Kbytes
- Maximum total/shared memory for all latency paths = 20 kBytes

Based on this information, and the application requirements, the first transceiver would select latency path settings. For example, if the applications are 1 video, 1 internet access and 1 voice application, the first transceiver could configure 3 latency paths as follows:

latency path #1 – Video: N=255, R=16, D=64

latency path #2 – Video: N=128, R=8, D=32

latency path #3 – Video: N=0, R=0, D=1 (no coding or interleaving)

[0058] This would result in a total interleaver memory of 20 kbytes.

[0059] Alternatively, if for example, there are only 2 video applications, the first transceiver could configure 2 latency paths as follows:

latency path #1 – Video: N=200, R=10, D=50

latency path #2 – Video: N=200, R=10, D=50

latency path #3 – Video: N=0, R=0, D=1 (no coding or interleaving)

[0060] This would also result in a total interleaver memory of 20 kbytes.

[0061] Alternatively, the second transceiver can determine the specific FCI configuration parameters, e.g., N, D, R as defined above, needed to meet specific application requirements, such as latency, burst error correction capability, etc. As described above for the first transceiver, in order to determine the FCI configuration parameters, the second transceiver must first know what are the capabilities of the first transceiver. In this case, the first transceiver would send a message to the second transceiver containing the information described above and based on this information and the application requirements the second transceiver would select latency path settings.

[0062] Fig. 2 outlines an exemplary method of allocating shared memory in a transceiver. More specifically, control begins in step S200 and continues to step

S210. In step S210, one or more of shared interleaver/deinterleaver memory and/or shared coder/decoder processing resources are allocated to one or more latency paths, in a transceiver. Control then continues to step S220 where the control sequence ends.

[0063] Fig. 3 outlines an exemplary method of exchanging shared resource allocations according to an exemplary embodiment of this invention. In particular, control begins in step S310. In step S310, a maximum amount of shared memory that can be allocated to a specific interleaver or deinterleaver of a plurality of interleavers or deinterleavers in a transceiver is determined. Next, in step S320, the determined maximum amount for one or more of the deinterleavers and/or interleavers is transmitted to another transceiver. Messages containing additional information can also be transmitted to the other transceiver and/or received from the other transceiver. Control then continues to step S330 where the control sequence ends.

[0064] Fig. 4 outlines an exemplary procedure for resource sharing according to an exemplary embodiment of this invention. In particular, control begins in step S400 and continues to step S410. In step S410, the number of latency paths are determined. Then, in step S420, the latency path information (FCI block information) is transmitted to another transceiver. Messages containing additional information can also be transmitted to the other transceiver and/or received from the other transceiver. This information can be used to, for example, assist with the determination of memory allocation in the transceiver. Moreover, the messages received from the other transceiver could specify what the memory allocation is to be based on, for

example, the number of latency paths, memory allocation in the remote transceiver and required applications. Control then continues to step S430.

[0065] In step S430, and for each latency path, the steps in step 440 are performed.

[0066] In step S440, and while monitoring of allocation of resources is being performed, steps 450 and 460 are performed. More specifically, in step S450, one or more parameters associated with the communication system are determined. Then, in step S460, shared resources are allocated based on one or more of the communication parameters. Control then continues to step S470.

[0067] In step S470, the allocation of shared resources is communicated to another transceiver. Next, in step S480, a determination is made as to whether there is a change in communications that would require the adjustment of the shared resource allocation. Examples of changes in communications conditions include a change in applications being transported over the system and/or changes in the channel condition, etc. If adjustments are required, control jumps back to step S410. Otherwise, control jumps to step S490 where the control sequence ends.

[0068] The above-described system can be implemented on wired and/or wireless telecommunications devices, such a modem, a multicarrier modem, a DSL modem, an ADSL modem, an XDSL modem, a VDSL modem, a linecard, test equipment, a multicarrier transceiver, a wired and/or wireless wide/local area network system, a

satellite communication system, a modem equipped with diagnostic capabilities, or the like, or on a separate programmed general purpose computer having a communications device or in conjunction with any of the following communications protocols: CDSL, ADSL2, ADSL2+, VDSL1, VDSL2, HDSL, DSL Lite, IDSL, RADSL, SDSL, UDSL or the like.

[0069] Additionally, the systems, methods and protocols of this invention can be implemented on a special purpose computer, a programmed microprocessor or microcontroller and peripheral integrated circuit element(s), an ASIC or other integrated circuit, a digital signal processor, a hard-wired electronic or logic circuit such as discrete element circuit, a programmable logic device such as PLD, PLA, FPGA, PAL, a modem, a transmitter/receiver, any comparable means, or the like. In general, any device capable of implementing a state machine that is in turn capable of implementing the methodology illustrated herein can be used to implement the various communication methods, protocols and techniques according to this invention.

[0070] Furthermore, the disclosed methods may be readily implemented in software using object or object-oriented software development environments that provide portable source code that can be used on a variety of computer or workstation platforms. Alternatively, the disclosed system may be implemented partially or fully in hardware using standard logic circuits or VLSI design. Whether software or hardware is used to implement the systems in accordance with this invention is dependent on the speed and/or efficiency requirements of the system, the particular

function, and the particular software or hardware systems or microprocessor or microcomputer systems being utilized. The communication systems, methods and protocols illustrated herein can be readily implemented in hardware and/or software using any known or later developed systems or structures, devices and/or software by those of ordinary skill in the applicable art from the functional description provided herein and with a general basic knowledge of the computer and telecommunications arts.

[0071] Moreover, the disclosed methods may be readily implemented in software that can be stored on a storage medium, executed on programmed general-purpose computer with the cooperation of a controller and memory, a special purpose computer, a microprocessor, or the like. In these instances, the systems and methods of this invention can be implemented as program embedded on personal computer such as an applet, JAVA® or CGI script, as a resource residing on a server or computer workstation, as a routine embedded in a dedicated communication system or system component, or the like. The system can also be implemented by physically incorporating the system and/or method into a software and/or hardware system, such as the hardware and software systems of a communications transceiver.

[0072] It is therefore apparent that there has been provided, in accordance with the present invention, systems and methods for sharing resources. While this invention has been described in conjunction with a number of embodiments, it is evident that many alternatives, modifications and variations would be or are apparent to those of ordinary skill in the applicable arts. Accordingly, it is intended to embrace

all such alternatives, modifications, equivalents and variations that are within the spirit and scope of this invention.

ABSTRACT

A transceiver is designed to share memory and processing power amongst a plurality of transmitter and/or receiver latency paths, in a communications transceiver that carries or supports multiple applications. For example, the transmitter and/or receiver latency paths of the transceiver can share an interleaver/deinterleaver memory. This allocation can be done based on the data rate, latency, BER, impulse noise protection requirements of the application, data or information being transported over each latency path, or in general any parameter associated with the communications system.

Electronic Patent Application Fee Transmittal				
Application Number:				
Filing Date:				
Title of Invention:		Resource Sharing in a Telecommunications Environment		
First Named Inventor/Applicant Name:		Marcos C. Tzannes		
Filer:		Jason Vick/Joanne Vos		
Attorney Docket Number:		5550-54-CON-3		
Filed as Large Entity				
Utility under 35 USC 111(a) Filing Fees				
Description	Fee Code	Quantity	Amount	Sub-Total in USD(\$)
Basic Filing:				
Utility application filing	1011	1	330	330
Utility Search Fee	1111	1	540	540
Utility Examination Fee	1311	1	220	220
Pages:				
Claims:				
Miscellaneous-Filing:				
Petition:				
Patent-Appeals-and-Interference:				

Description	Fee Code	Quantity	Amount	Sub-Total in USD(\$)
Post-Allowance-and-Post-Issuance:				
Extension-of-Time:				
Miscellaneous:				
Total in USD (\$)				1090

Electronic Acknowledgement Receipt	
EFS ID:	8598221
Application Number:	12901699
International Application Number:	
Confirmation Number:	1676
Title of Invention:	Resource Sharing in a Telecommunications Environment
First Named Inventor/Applicant Name:	Marcos C. Tzannes
Customer Number:	62574
Filer:	Jason Vick/Joanne Vos
Filer Authorized By:	Jason Vick
Attorney Docket Number:	5550-54-CON-3
Receipt Date:	11-OCT-2010
Filing Date:	
Time Stamp:	14:06:19
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	yes
Payment Type	Deposit Account
Payment was successfully received in RAM	\$1090
RAM confirmation Number	9244
Deposit Account	191970
Authorized User	
The Director of the USPTO is hereby authorized to charge indicated fees and credit any overpayment as follows: Charge any Additional Fees required under 37 C.F.R. Section 1.16 (National application filing, search, and examination fees) Charge any Additional Fees required under 37 C.F.R. Section 1.17 (Patent application and reexamination processing fees)	

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Charge any Additional Fees required under 37 C.F.R. Section 1.20 (Post Issuance fees)					
Charge any Additional Fees required under 37 C.F.R. Section 1.21 (Miscellaneous fees and charges)					
File Listing:					
Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1	Application Data Sheet	ADS.pdf	1031615 2b02ad33a517a021784c39ecf96c88aef36c b3f9	no	5
Warnings:					
Information:					
2	Oath or Declaration filed	Executed_Declaration.pdf	68832 4fa55931a03ee1c0095613ab7b15a94c333aef 874a5	no	1
Warnings:					
Information:					
3		AMEND_PRELIM_01.pdf	433308 a2c1779933f7331aa5413b712e300031a8311 0b66	yes	6
	Multipart Description/PDF files in .zip description				
	Document Description		Start	End	
	Preliminary Amendment		1	1	
	Specification		2	3	
	Claims		4	5	
	Applicant Arguments/Remarks Made in an Amendment		6	6	
Warnings:					
Information:					
4		Specification.pdf	158115 a232204b8c9c4ab5c3df572626f3ca8320a 7040	yes	30
	Multipart Description/PDF files in .zip description				
	Document Description		Start	End	
	Specification		1	23	
	Claims		24	29	
	Abstract		30	30	
Warnings:					

Information:					
5	Drawings-only black and white line drawings	Figures_Final.pdf	29302	no	3
			914c8c5d7bce1b8cf5e5fcc337a8b7944b61d397		
Warnings:					
Information:					
6		Substitute_Spec_Marked_Up_Verson.pdf	150768	yes	24
			aad567efb03cc7b118092eb1f94115c182158e97		
	Multipart Description/PDF files in .zip description				
	Document Description		Start	End	
	Specification		1	23	
	Abstract		24	24	
Warnings:					
Information:					
7		Substitute_Spec_Clean_Verson.pdf	148644	yes	24
			6c69e1138b3cfe19fbb0cb18256e8a6da382960		
	Multipart Description/PDF files in .zip description				
	Document Description		Start	End	
	Specification		1	23	
	Abstract		24	24	
Warnings:					
Information:					
8	Fee Worksheet (PTO-875)	fee-info.pdf	32502	no	2
			21744b0b76a94f51444d007cc56008ae270cad73c		
Warnings:					
Information:					
Total Files Size (in bytes):			2053086		

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New Applications Under 35 U.S.C. 111

If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application.

National Stage of an International Application under 35 U.S.C. 371

If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.

New International Application Filed with the USPTO as a Receiving Office

If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.

Electronic Acknowledgement Receipt	
EFS ID:	8598221
Application Number:	12901699
International Application Number:	
Confirmation Number:	1676
Title of Invention:	Resource Sharing in a Telecommunications Environment
First Named Inventor/Applicant Name:	Marcos C. Tzannes
Customer Number:	62574
Filer:	Jason Vick/Joanne Vos
Filer Authorized By:	Jason Vick
Attorney Docket Number:	5550-54-CON-3
Receipt Date:	11-OCT-2010
Filing Date:	
Time Stamp:	14:06:19
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	yes
Payment Type	Deposit Account
Payment was successfully received in RAM	\$1090
RAM confirmation Number	9244
Deposit Account	191970
Authorized User	
The Director of the USPTO is hereby authorized to charge indicated fees and credit any overpayment as follows: Charge any Additional Fees required under 37 C.F.R. Section 1.16 (National application filing, search, and examination fees) Charge any Additional Fees required under 37 C.F.R. Section 1.17 (Patent application and reexamination processing fees)	

Charge any Additional Fees required under 37 C.F.R. Section 1.19 (Document supply fees)					
Charge any Additional Fees required under 37 C.F.R. Section 1.20 (Post Issuance fees)					
Charge any Additional Fees required under 37 C.F.R. Section 1.21 (Miscellaneous fees and charges)					
File Listing:					
Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1	Application Data Sheet	ADS.pdf	1031615 2b02ad33a517a02178dc37ecf96c88aef36c b3f9	no	5
Warnings:					
Information:					
2	Oath or Declaration filed	Executed_Declaration.pdf	68832 4fa55931a03ce1c0095613ab7b15a94c333aef 874a5	no	1
Warnings:					
Information:					
3		AMEND_PRELIM_01.pdf	433308 a2c1779933f7331aa5413b712e300031a8311 0b66	yes	6
	Multipart Description/PDF files in .zip description				
	Document Description	Start	End		
	Preliminary Amendment	1	1		
	Specification	2	3		
	Claims	4	5		
	Applicant Arguments/Remarks Made in an Amendment	6	6		
Warnings:					
Information:					
4		Specification.pdf	158115 a232204b8c9c4ab5c3df572626f3ca8320a 7040	yes	30
	Multipart Description/PDF files in .zip description				
	Document Description	Start	End		
	Specification	1	23		
	Claims	24	29		
	Abstract	30	30		
Warnings:					

Information:					
5	Drawings-only black and white line drawings	Figures_Final.pdf	29302	no	3
			914c85d0fbc1b8cf5e5fcc337a8b9948b61d99f		
Warnings:					
Information:					
6		Substitute_Spec_Marked_Up_Verson.pdf	150768	yes	24
			aad567efb03cc7b118092eb1f94115c182158697		
	Multipart Description/PDF files in .zip description				
	Document Description		Start	End	
	Specification		1	23	
	Abstract		24	24	
Warnings:					
Information:					
7		Substitute_Spec_Clean_Verson.pdf	148644	yes	24
			6c69e1138b3cfe19fbb0cb18256e8afda382960		
	Multipart Description/PDF files in .zip description				
	Document Description		Start	End	
	Specification		1	23	
	Abstract		24	24	
Warnings:					
Information:					
8	Fee Worksheet (PTO-875)	fee-info.pdf	32502	no	2
			21744b0b076a94f51444d0017c56008ae270cad73c		
Warnings:					
Information:					
Total Files Size (in bytes):			2053086		

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New International Application Filed with the USPTO as a Receiving Office

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Application Data Sheet 37 CFR 1.76		Attorney Docket Number	5550-54-CON-3
		Application Number	
Title of Invention	RESOURCE SHARING IN A TELECOMMUNICATIONS ENVIRONMENT		
The application data sheet is part of the provisional or nonprovisional application for which it is being submitted. The following form contains the bibliographic data arranged in a format specified by the United States Patent and Trademark Office as outlined in 37 CFR 1.76. This document may be completed electronically and submitted to the Office in electronic format using the Electronic Filing System (EFS) or the document may be printed and included in a paper filed application.			

Secrecy Order 37 CFR 5.2

☐ Portions or all of the application associated with this Application Data Sheet may fall under a Secrecy Order pursuant to 37 CFR 5.2. (Paper filers only. Applications that fall under Secrecy Order may not be filed electronically.)

Applicant Information:

Applicant 1					Remove		
Applicant Authority		☒ Inventor		☐ Legal Representative under 35 U.S.C. 117		☐ Party of Interest under 35 U.S.C. 118	
Prefix	Given Name	Middle Name	Family Name		Suffix		
	Marcos	C.	Tzannes				
Residence Information (Select One)		☒ US Residency ☐ Non US Residency ☐ Active US Military Service					
City	Orinda	State/Province	CA	Country of Residence i	US		
Citizenship under 37 CFR 1.41(b) i		US					
Mailing Address of Applicant:							
Address 1		121 La Espiral					
Address 2							
City	Orinda	State/Province	CA				
Postal Code	94563	Country i	US				
Applicant 2					Remove		
Applicant Authority		☒ Inventor		☐ Legal Representative under 35 U.S.C. 117		☐ Party of Interest under 35 U.S.C. 118	
Prefix	Given Name	Middle Name	Family Name		Suffix		
	Michael		Lund				
Residence Information (Select One)		☒ US Residency ☐ Non US Residency ☐ Active US Military Service					
City	West Newton	State/Province	MA	Country of Residence i	US		
Citizenship under 37 CFR 1.41(b) i		US					
Mailing Address of Applicant:							
Address 1		110 Prospect Street					
Address 2							
City	West Newton	State/Province	MA				
Postal Code	02465	Country i	US				
All Inventors Must Be Listed - Additional Inventor Information blocks may be generated within this form by selecting the Add button.							

Correspondence Information:

Enter either Customer Number or complete the Correspondence Information section below.
For further information see 37 CFR 1.33(a).

☐ An Address is being provided for the correspondence information of this application.

Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it contains a valid OMB control number.

Application Data Sheet 37 CFR 1.76		Attorney Docket Number	5550-54-CON-3
		Application Number	
Title of Invention	RESOURCE SHARING IN A TELECOMMUNICATIONS ENVIRONMENT		
Customer Number	62574		
Email Address	jvick@sheridanross.com	Add Email	Remove Email

Application Information:

Title of the Invention	RESOURCE SHARING IN A TELECOMMUNICATIONS ENVIRONMENT		
Attorney Docket Number	5550-54-CON-3	Small Entity Status Claimed	☐
Application Type	Nonprovisional		
Subject Matter	Utility		
Suggested Class (if any)		Sub Class (if any)	
Suggested Technology Center (if any)			
Total Number of Drawing Sheets (if any)	3	Suggested Figure for Publication (if any)	

Publication Information:
☐ Request Early Publication (Fee required at time of Request 37 CFR 1.219)

Request Not to Publish. I hereby request that the attached application not be published under 35 U.S. C. 122(b) and certify that the invention disclosed in the attached application **has not and will not** be the subject of an application filed in another country, or under a multilateral international agreement, that requires publication at eighteen months after filing.

Representative Information:

Representative information should be provided for all practitioners having a power of attorney in the application. Providing this information in the Application Data Sheet does not constitute a power of attorney in the application (see 37 CFR 1.32). Enter either Customer Number or complete the Representative Name section below. If both sections are completed the Customer Number will be used for the Representative Information during processing.

Please Select One:	☒ Customer Number	☐ US Patent Practitioner	☐ Limited Recognition (37 CFR 11.9)
Customer Number	62574		

Domestic Benefit/National Stage Information:

This section allows for the applicant to either claim benefit under 35 U.S.C. 119(e), 120, 121, or 365(c) or indicate National Stage entry from a PCT application. Providing this information in the application data sheet constitutes the specific reference required by 35 U.S.C. 119(e) or 120, and 37 CFR 1.78(a)(2) or CFR 1.78(a)(4), and need not otherwise be made part of the specification.

Prior Application Status	Pending	Remove	
Application Number	Continuity Type	Prior Application Number	Filing Date (YYYY-MM-DD)
	Continuation of	12/761586	2010-04-16
Prior Application Status	Pending	Remove	
Application Number	Continuity Type	Prior Application Number	Filing Date (YYYY-MM-DD)
12/761586	Continuation of	11/246163	2005-10-11

Application Data Sheet 37 CFR 1.76		Attorney Docket Number	5550-54-CON-3
		Application Number	
Title of Invention	RESOURCE SHARING IN A TELECOMMUNICATIONS ENVIRONMENT		

Prior Application Status	Expired	Remove	
Application Number	Continuity Type	Prior Application Number	Filing Date (YYYY-MM-DD)
11/246163	non provisional of	60/618269	2004-10-12
Additional Domestic Benefit/National Stage Data may be generated within this form by selecting the Add button.			Add

Foreign Priority Information:

This section allows for the applicant to claim benefit of foreign priority and to identify any prior foreign application for which priority is not claimed. Providing this information in the application data sheet constitutes the claim for priority as required by 35 U.S.C. 119(b) and 37 CFR 1.55(a).			
			Remove
Application Number	Country ⁱ	Parent Filing Date (YYYY-MM-DD)	Priority Claimed
			☐ Yes ☒ No
Additional Foreign Priority Data may be generated within this form by selecting the Add button.			Add

Assignee Information:

Providing this information in the application data sheet does not substitute for compliance with any requirement of part 3 of Title 37 of the CFR to have an assignment recorded in the Office.			
			Remove
Assignee 1			
If the Assignee is an Organization check here. ☒			
Organization Name	AWARE, INC.		
Mailing Address Information:			
Address 1	40 Middlesex Turnpike		
Address 2			
City	Bedford	State/Province	MA
Country ⁱ	US	Postal Code	01730
Phone Number		Fax Number	
Email Address			
Additional Assignee Data may be generated within this form by selecting the Add button.			Add

Signature:

A signature of the applicant or representative is required in accordance with 37 CFR 1.33 and 10.18. Please see 37 CFR 1.4(d) for the form of the signature.					
Signature	/Jason H. Vick/			Date (YYYY-MM-DD)	2010-10-11
First Name	Jason H.	Last Name	Vick	Registration Number	45285

Application Data Sheet 37 CFR 1.76		Attorney Docket Number	5550-54-CON-3
		Application Number	
Title of Invention	RESOURCE SHARING IN A TELECOMMUNICATIONS ENVIRONMENT		

This collection of information is required by 37 CFR 1.76. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 23 minutes to complete, including gathering, preparing, and submitting the completed application data sheet form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

Privacy Act Statement

The Privacy Act of 1974 (P.L. 93-579) requires that you be given certain information in connection with your submission of the attached form related to a patent application or patent. Accordingly, pursuant to the requirements of the Act, please be advised that: (1) the general authority for the collection of this information is 35 U.S.C. 2(b)(2); (2) furnishing of the information solicited is voluntary; and (3) the principal purpose for which the information is used by the U.S. Patent and Trademark Office is to process and/or examine your submission related to a patent application or patent. If you do not furnish the requested information, the U.S. Patent and Trademark Office may not be able to process and/or examine your submission, which may result in termination of proceedings or abandonment of the application or expiration of the patent.

The information provided by you in this form will be subject to the following routine uses:

1. The information on this form will be treated confidentially to the extent allowed under the Freedom of Information Act (5 U.S.C. 552) and the Privacy Act (5 U.S.C. 552a). Records from this system of records may be disclosed to the Department of Justice to determine whether the Freedom of Information Act requires disclosure of these records.
2. A record from this system of records may be disclosed, as a routine use, in the course of presenting evidence to a court, magistrate, or administrative tribunal, including disclosures to opposing counsel in the course of settlement negotiations.
3. A record in this system of records may be disclosed, as a routine use, to a Member of Congress submitting a request involving an individual, to whom the record pertains, when the individual has requested assistance from the Member with respect to the subject matter of the record.
4. A record in this system of records may be disclosed, as a routine use, to a contractor of the Agency having need for the information in order to perform a contract. Recipients of information shall be required to comply with the requirements of the Privacy Act of 1974, as amended, pursuant to 5 U.S.C. 552a(m).
5. A record related to an International Application filed under the Patent Cooperation Treaty in this system of records may be disclosed, as a routine use, to the International Bureau of the World Intellectual Property Organization, pursuant to the Patent Cooperation Treaty.
6. A record in this system of records may be disclosed, as a routine use, to another federal agency for purposes of National Security review (35 U.S.C. 181) and for review pursuant to the Atomic Energy Act (42 U.S.C. 218(c)).
7. A record from this system of records may be disclosed, as a routine use, to the Administrator, General Services, or his/her designee, during an inspection of records conducted by GSA as part of that agency's responsibility to recommend improvements in records management practices and programs, under authority of 44 U.S.C. 2904 and 2906. Such disclosure shall be made in accordance with the GSA regulations governing inspection of records for this purpose, and any other relevant (i.e., GSA or Commerce) directive. Such disclosure shall not be used to make determinations about individuals.
8. A record from this system of records may be disclosed, as a routine use, to the public after either publication of the application pursuant to 35 U.S.C. 122(b) or issuance of a patent pursuant to 35 U.S.C. 151. Further, a record may be disclosed, subject to the limitations of 37 CFR 1.14, as a routine use, to the public if the record was filed in an application which became abandoned or in which the proceedings were terminated and which application is referenced by either a published application, an application open to public inspections or an issued patent.
9. A record from this system of records may be disclosed, as a routine use, to a Federal, State, or local law enforcement agency, if the USPTO becomes aware of a violation or potential violation of law or regulation.



PTO/SB01A (09-04)
 Approved for use through 07/31/2006 OMB 0651-0032
 U.S. Patent and Trademark Office, U.S. DEPARTMENT OF COMMERCE
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 Docket No. T3653-9285US01

DECLARATION (37 CFR 1.63) FOR UTILITY OR DESIGN APPLICATION USING AN APPLICATION DATA SHEET (37 CFR 1.76)

Title of
Invention

RESOURCE SHARING IN A TELECOMMUNICATIONS ENVIRONMENT

As the below named inventor(s), I/we declare that:

This declaration is directed to:

- ☐ The attached application, or
☒ Application No. 11/246,163, filed on October 11, 2005
☐ as amended on _____ (if applicable):

I/we believe that I/we am/are the original and first inventor(s) of the subject matter which is claimed and for which a patent is sought;

I/we have reviewed and understand the contents of the above-identified application, including the claims, as amended by any amendment specifically referred to above;

I/we acknowledge the duty to disclose to the United States Patent and Trademark Office all information known to me/us to be material to patentability as defined in 37 CFR 1.56, including for continuation-in-part applications, material information which became available between the filing date of the prior application and the national or PCT International filing date of the continuation-in-part application.

All statements made herein of my/own knowledge are true, all statements made herein on information and belief are believed to be true, and further that these statements were made with the knowledge that willful false statements and the like are punishable by fine or imprisonment, or both, under 18 U.S.C. 1001, and may jeopardize the validity of the application or any patent issuing thereon.

FULL NAME OF INVENTOR(S)

Inventor one: Marcos C. TZANNES

Signature: [Signature] Citizen of: U.S.A.

Inventor two: Michael LUND

Signature: [Signature] Citizen of: U.S.A.

Inventor three: _____

Signature: _____ Citizen of: _____

Inventor four: _____

Signature: _____ Citizen of: _____

☐ Additional inventors or a legal representative are being named on _____ additional form(s) attached hereto.

This collection of information is required by 37 U.S.C. 115 and 37 CFR 1.63. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.11 and 1.14. This collection is estimated to take 1 minute to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.

*AGE 2/5 * RCVD AT 1/5/2006 11:05:03 AM [Eastern Standard Time] * SVR: TYSOFAX/0 * DNIS: 9994 * CSID: 17816870430 * DURATION (mm:ss): 02:14

POWER OF ATTORNEY TO PROSECUTE APPLICATIONS BEFORE THE USPTO

I hereby revoke all previous powers of attorney given in the application identified in the attached statement under 37 CFR 3.73(b).

I hereby appoint:

☒ Practitioners associated with the Customer Number: 62574

OR

☐ Practitioner(s) named below (if more than ten patent practitioners are to be named, then a customer number must be used):

Name	Registration Number	Name	Registration Number

as attorney(s) or agent(s) to represent the undersigned before the United States Patent and Trademark Office (USPTO) in connection with any and all patent applications assigned only to the undersigned according to the USPTO assignment records or assignment documents attached to this form in accordance with 37 CFR 3.73(b).

Please change the correspondence address for the application identified in the attached statement under 37 CFR 3.73(b) to:

☒ The address associated with Customer Number: 62574

OR

☐ Firm or Individual Name			
Address			
City	State	Zip	
Country			
Telephone			Email

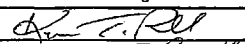
Assignee Name and Address:

AWARE, INC.
40 Middlesex Turnpike
Bedford, MA 07130-1423

A copy of this form, together with a statement under 37 CFR 3.73(b) (Form PTO/SB/96 or equivalent) is required to be filed in each application in which this form is used. The statement under 37 CFR 3.73(b) may be completed by one of the practitioners appointed in this form if the appointed practitioner is authorized to act on behalf of the assignee, and must identify the application in which this Power of Attorney is to be filed.

SIGNATURE of Assignee of Record

The individual whose signature and title is supplied below is authorized to act on behalf of the assignee

Signature		Date	11/8/09
Name	Kevin T. Russell	Telephone	781-657-8335
Title	V.P. General Counsel		

This collection of information is required by 37 CFR 1.31, 1.32 and 1.33. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 36 U.S.C. 122 and 37 CFR 1.11 and 1.14. This collection is estimated to take 3 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1460, Alexandria, VA 22313-1460. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. SEND TO: Commissioner for Patents, P.O. Box 1460, Alexandria, VA 22313-1460.

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Electronic Acknowledgement Receipt	
EFS ID:	8598548
Application Number:	12901699
International Application Number:	
Confirmation Number:	1676
Title of Invention:	RESOURCE SHARING IN A TELECOMMUNICATIONS ENVIRONMENT
First Named Inventor/Applicant Name:	Marcos C. Tzannes
Customer Number:	62574
Filer:	Jason Vick/Joanne Vos
Filer Authorized By:	Jason Vick
Attorney Docket Number:	5550-54-CON-3
Receipt Date:	11-OCT-2010
Filing Date:	
Time Stamp:	14:33:59
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	no				
File Listing:					
Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1		Statement_under_373b_w_PO A.pdf	249478 d4129973f08c8162cb36fa70b4697c0dc274c c0f09	yes	2

Multipart Description/PDF files in .zip description		
Document Description	Start	End
Assignee showing of ownership per 37 CFR 3.73(b).	1	1
Power of Attorney	2	2

Warnings:

Information:

Total Files Size (in bytes):	249478

This Acknowledgement Receipt evidences receipt on the noted date by the USPTO of the indicated documents, characterized by the applicant, and including page counts, where applicable. It serves as evidence of receipt similar to a Post Card, as described in MPEP 503.

New Applications Under 35 U.S.C. 111
If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application.

National Stage of an International Application under 35 U.S.C. 371
If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.

New International Application Filed with the USPTO as a Receiving Office
If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.

STATEMENT UNDER 37 CFR 3.73(b)

Applicant/Patent Owner: AWARE, INC.

Application No./Patent No.: 12/901,699

Filed/Issue Date: October 11, 2010

Titled: RESOURCE SHARING IN A TELECOMMUNICATIONS ENVIRONMENT

AWARE, INC., a Corporation

(Name of Assignee)

(Type of Assignee, e.g., corporation, partnership, university, government agency, etc.)

states that it is:

1. ☒ the assignee of the entire right, title, and interest in;
2. ☐ an assignee of less than the entire right, title, and interest in
(The extent (by percentage) of its ownership interest is _____ %); or
3. ☐ the assignee of an undivided interest in the entirety of (a complete assignment from one of the joint inventors was made)

the patent application/patent identified above, by virtue of either:

- A. ☒ An assignment from the inventor(s) of the patent application/patent identified above. The assignment was recorded in the United States Patent and Trademark Office at Reel 017438, Frame 0094, or for which a copy therefore is attached.

OR

- B. ☐ A chain of title from the inventor(s), of the patent application/patent identified above, to the current assignee as follows:

1. From: _____ To: _____

The document was recorded in the United States Patent and Trademark Office at

Reel _____, Frame _____, or for which a copy thereof is attached.

2. From: _____ To: _____

The document was recorded in the United States Patent and Trademark Office at

Reel _____, Frame _____, or for which a copy thereof is attached.

3. From: _____ To: _____

The document was recorded in the United States Patent and Trademark Office at

Reel _____, Frame _____, or for which a copy thereof is attached.

- ☐ Additional documents in the chain of title are listed on a supplemental sheet(s).

- ☒ As required by 37 CFR 3.73(b)(1)(i), the documentary evidence of the chain of title from the original owner to the assignee was, or concurrently is being, submitted for recordation pursuant to 37 CFR 3.11.

[NOTE: A separate copy (i.e., a true copy of the original assignment document(s)) must be submitted to Assignment Division in accordance with 37 CFR Part 3, to record the assignment in the records of the USPTO. See MPEP 302.08]

The undersigned (whose title is supplied below) is authorized to act on behalf of the assignee.

Signature

11 OCT '10
Date

Jason H. Vick

Attorney for Assignee

Printed or Typed Name

Title

This collection of information is required by 37 CFR 3.73(b). The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.11 and 1.14. This collection is estimated to take 12 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.

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Date: 10/11/10

Approved for use through 7/31/2006. OMB 0651-0032

U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE

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PATENT APPLICATION FEE DETERMINATION RECORD Substitute for Form PTO-875					Application or Docket Number 12/901,699	
APPLICATION AS FILED – PART I						
(Column 1)		(Column 2)		SMALL ENTITY		OR
FOR	NUMBER FILED	NUMBER EXTRA	RATE (\$)	FEE (\$)	RATE (\$)	FEE (\$)
BASIC FEE (37 CFR 1.16(a), (b), or (c))	N/A	N/A	N/A		N/A	330
SEARCH FEE (37 CFR 1.16(k), (l), or (m))	N/A	N/A	N/A		N/A	540
EXAMINATION FEE (37 CFR 1.16(o), (p), or (q))	N/A	N/A	N/A		N/A	220
1 (37 CFR 1.16(i))	8	minus 20 =	x\$26		x\$52	
INDEPENDENT CLAIMS (37 CFR 1.16(h))	2	minus 3 = *	x\$110		x\$220	
APPLICATION SIZE FEE (37 CFR 1.16(s))	If the specification and drawings exceed 100 sheets of paper, the application size fee due is \$270 (\$135 for small entity) for each additional 50 sheets or fraction thereof. See 35 U.S.C. 41(a)(1)(G) and 37 CFR					
MULTIPLE DEPENDENT CLAIM PRESENT (37 CFR 1.16(j))			195		390	
* If the difference in column 1 is less than zero, enter "0" in column 2.			TOTAL		TOTAL	1090
APPLICATION AS AMENDED – PART II						
(Column 1)		(Column 2)		(Column 3)		SMALL ENTITY
AMENDMENT A	CLAIMS REMAINING AFTER AMENDMENT	HIGHEST NUMBER PREVIOUSLY PAID FOR	PRESENT EXTRA	RATE (\$)	ADDITIONAL FEE (\$)	RATE (\$)
	Total (37 CFR 1.16(i))	Minus **	=	X =		X =
	Independent (37 CFR 1.16(h))	Minus ***	=	X =		X =
	Application Size Fee (37 CFR 1.16(s))					
	FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))			N/A		N/A
			TOTAL ADD'T FEE		TOTAL ADD'T FEE	
(Column 1)		(Column 2)		(Column 3)		SMALL ENTITY
AMENDMENT B	CLAIMS REMAINING AFTER AMENDMENT	HIGHEST NUMBER PREVIOUSLY PAID FOR	PRESENT EXTRA	RATE (\$)	ADDITIONAL FEE (\$)	RATE (\$)
	Total (37 CFR 1.16(i))	Minus **	=	X =		X =
	Independent (37 CFR 1.16(h))	Minus ***	=	X =		X =
	Application Size Fee (37 CFR 1.16(s))					
	FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))			N/A		N/A
			TOTAL ADD'T FEE		TOTAL ADD'T FEE	
* If the entry in column 1 is less than the entry in column 2, write "0" in column 3. ** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 20, enter "20". *** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 3, enter "3". The "Highest Number Previously Paid For" (Total or Independent) is the highest number found in the appropriate box in column 1.						

This collection of information is required by 37 CFR 1.16. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 12 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comment on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.

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PATENT APPLICATION FEE DETERMINATION RECORD Substitute for Form PTO-875					Application or Docket Number 12/901,699		Filing Date 10/11/2010		☐ To be Mailed	
APPLICATION AS FILED – PART I										
(Column 1)			(Column 2)		SMALL ENTITY ☐ OR			OTHER THAN SMALL ENTITY		
FOR		NUMBER FILED	NUMBER EXTRA		RATE (\$)	FEE (\$)			RATE (\$)	FEE (\$)
☐ BASIC FEE (37 CFR 1.16(a), (b), or (c))		N/A	N/A		N/A				N/A	
☐ SEARCH FEE (37 CFR 1.16(k), (l), or (m))		N/A	N/A		N/A				N/A	
☐ EXAMINATION FEE (37 CFR 1.16(o), (p), or (q))		N/A	N/A		N/A				N/A	
TOTAL CLAIMS (37 CFR 1.16(j))		minus 20 =	*		X \$ =		OR		X \$ =	
INDEPENDENT CLAIMS (37 CFR 1.16(h))		minus 3 =	*		X \$ =				X \$ =	
☐ APPLICATION SIZE FEE (37 CFR 1.16(s))		If the specification and drawings exceed 100 sheets of paper, the application size fee due is \$250 (\$125 for small entity) for each additional 50 sheets or fraction thereof. See 35 U.S.C. 41(a)(1)(G) and 37 CFR 1.16(s).								
☐ MULTIPLE DEPENDENT CLAIM PRESENT (37 CFR 1.16(j))										
					TOTAL				TOTAL	
APPLICATION AS AMENDED – PART II										
(Column 1)		(Column 2)		(Column 3)		SMALL ENTITY OR			OTHER THAN SMALL ENTITY	
AMENDMENT	10/11/2010	CLAIMS REMAINING AFTER AMENDMENT		HIGHEST NUMBER PREVIOUSLY PAID FOR	PRESENT EXTRA	RATE (\$)	ADDITIONAL FEE (\$)		RATE (\$)	ADDITIONAL FEE (\$)
	Total (37 CFR 1.16(o))	* 8	Minus	** 20	= 0	X \$ =		OR	X \$52=	0
	Independent (37 CFR 1.16(h))	* 2	Minus	*** 3	= 0	X \$ =		OR	X \$220=	0
	☐ Application Size Fee (37 CFR 1.16(s))									
	☐ FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))									
						TOTAL ADD'L FEE		OR	TOTAL ADD'L FEE	0
AMENDMENT		CLAIMS REMAINING AFTER AMENDMENT		HIGHEST NUMBER PREVIOUSLY PAID FOR	PRESENT EXTRA	RATE (\$)	ADDITIONAL FEE (\$)		RATE (\$)	ADDITIONAL FEE (\$)
	Total (37 CFR 1.16(o))	*	Minus	**	=	X \$ =		OR	X \$ =	
	Independent (37 CFR 1.16(h))	*	Minus	***	=	X \$ =		OR	X \$ =	
	☐ Application Size Fee (37 CFR 1.16(s))									
	☐ FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))									
						TOTAL ADD'L FEE		OR	TOTAL ADD'L FEE	
* If the entry in column 1 is less than the entry in column 2, write "0" in column 3. ** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 20, enter "20". *** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 3, enter "3". The "Highest Number Previously Paid For" (Total or Independent) is the highest number found in the appropriate box in column 1. Legal Instrument Examiner: /YOLANDA CHADWICK/										

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- 16 -

```

    tmp          = 0x20000000 - ((phaseAcc[31:0] & 0xffffffff)
>> 15) * bankFactor
    tmp          = MAX([0, tmp])
5    xmtPhaseTmp[4:0] = tmp >> phaseShift
    xmtPhase[3:0] = LIMIT(xmtPhaseTmp[4:0], 0, 15)
    alphaTmp[31:0] = tmp - (xmtPhase[3:0] << phaseShift)
    alpha[8:0]     = alphaTmp >> (phaseShift - nInterpBits)
    c0Ptr          = coeffPtr + (xmtPhase[3:0] * nCoeffs)
10    c1Ptr        = c0Ptr + nCoeffs
    coeffs[k]      = c0Ptr + ((c1Ptr[k] - c0Ptr[k]) * alpha[8:0]) >>
nInterpBits

```

15 NOTE:
 coeffPtr is a pointer to the fixed set of 17 banks of coefficients.

The phaseInc and bankFactor parameters should be updated atomically in order to ensure that there are no glitches in the xmtPhase computation. A new input sample is shifted into transmit re-sampler 122 delay line with every other increment of the phase accumulator 309.

20 The ATUR receiver continuously extracts timing information from the received signal and updates the control signals 350 352 and 354 in order to track any clock drift that may occur in the system.

25 There are several different ways to update the timing of the re-samplers: 1) through use of a phase tweak (periodically adjust the phase accumulator), 2) through update of the phase increment, or 3) using a combination of 1) and 2). In the former case, the phase tweak is applied in conjunction with the phase increment when incrementing the phase accumulator 309. If Δ represents the adjustment to be applied to the phase accumulator 309, it is performed by using a phase tweak given by

$$\text{phaseTweak}[31:0] = \text{phaseInc}[31:0] + \frac{\Delta}{2}$$

35 for 2 consecutive phase increments (the phase tweak acts as the phase increment for 2 consecutive phase increments). The phase tweak must be limited to be less than 2^{29} otherwise it would be possible to wrap twice modulo 2^{29} with a single increment of the phase accumulator 309. The use of

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the common phase accumulator 309 shared between the receive re-sampler 116 and transmit re-sampler 122 ensures that receive and transmit timing is locked.

5 III. Copying DMA With Two Separate Strides Selected by a Modulo-n Counter to Perform Convolutional De-interleaving.

 In a communication system employing convolutional interleaving (such as an ADSL), it is necessary for the receiver to de-interleave the decoded data stream. A data buffer is used to implement the de-interleaving process. For each codeword-sized interleaved data block decoded and written
10 into the data buffer, a single de-interleaved codeword is read from the data buffer. Because the data buffer requires substantial storage capacity, up to 16 KB for an ADSL system, it is desirable to share a single physical memory between the de-interleaving data buffer, other receiver system I/O buffers, and program and data storage. This type of shared memory architecture is known
15 as a unified memory architecture (UMA).

 The problem, however, with using traditional UMAs is that the codeword-sized blocks written to the de-interleaving data buffer are not an integer multiple of the width of the shared physical memory. This complicates the write interface to the shared memory by requiring it to perform alignment
20 of the codeword-sized block and partial word writes in order to append the block to the existing data buffer contents. The second stride is also adjusted to account for a dummy byte added at the input to the interleaver (to make the interleaved block size relatively prime to the interleave depth) but not transmitted, as in systems like ADSL. The write interface is further
25 complicated by the need to re-insert a dummy byte added at the input to the interleaver (to make the interleaved block size relatively prime to the interleave depth) but not transmitted. As a solution, the present invention uses a DMA scheme with two separate strides to copy codewords from the de-interleaving data buffer..

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FIG. 4 is an illustration of a more detailed block diagram of the control processor 205, shown in FIG. 2. The control processor 205 is an example of a control processor, or DPS, suitable for implementing the DMA scheme of the present invention. In FIG. 4, the control processor 205 includes a central processing unit (CPU) 400, a memory 402, and an input/output interface 403. The DMA engine 404, responsible for implementing the DMA functions, includes a DMA memory storage area 406.

The DMA storage area 406 includes an exemplary de-interleaving data buffer 408, along with other DMA related storage locations. The DMA scheme is implemented using a DMA engine 404 to execute the overall DMA operations associated with the control processor 205. Thus, the DMA engine 404 receives data, via the control processor 205, based upon a received signal, such as the digitized signal 112. The received data is then placed into the data buffer 408 for de-interleaving. The data is read from the data buffer 408, or de-interleaved, in accordance with the DMA engine 404, selected DMA parameters (discussed in greater detail below), and a modulo counting scheme. The modulo counting scheme is accomplished using an exemplary modulo counter 410.

In the present invention, the use of two separate strides, for placing the data into the data buffer 408 allows the codeword-sized blocks, written to the buffer, to be appended with dummy bytes. This padding enables the codeword sized blocks to be translated to a size, or format, that is an integer multiple of the shared physical memory width. The size conversion simplifies the write interface by eliminating the need for data alignment and partial word writes into the shared memory.

The first stride specifies the increment between codeword elements necessary to perform the basic de-interleaving operation. The second stride allows the DMA engine 404 to skip over the dummy padding every codeword-size bytes. The wrapping of a modulo-n counter indicates when the second stride should be used to perform the skip.

FIG. 5 is an illustration of an exemplary decoded serial byte stream 500, segmented into codeword-sized data blocks A-G. The byte stream 500

- 19 -

includes a plurality of individual interleaved bytes, as shown, and is representative of a typical byte stream received as an input to the CPU 400 and processed by the DMA engine 404. Such byte streams are normally interleaved on the transmitter side in order to provide features such as robustness and security and thus require de-interleaving at the receiver side.

5 In the example of FIG. 5, and for purposes of illustration only, the byte stream 500 has a de-interleave depth (D) of "4" and a block size value (N) of "5." The de-interleave depth (D) controls the amount of time each byte is delayed. The block size value (N) specifies the number of bytes in each
10 codeword. Thus, in the example of the byte stream 500, each of the individual bytes is delayed by four time slots. In the present invention, the DMA engine 404 is configured to efficiently place the originally transmitted bytes of the data stream 500 back into their original order (1, 2, 3, 4, 5, 6...) instead of the interleaved order (0, -, -, -, 1, 5, etc.), illustrated in FIG. 5. FIG. 6 illustrates
15 the first step in the process of re-ordering the bytes of the data stream 500, i.e., copying each of the codeword-size blocks A-G into the data buffer 408.

In FIG. 6 the input buffer 408, shown vertically arrayed, is partitioned into separate memory locations 600 – 608. For purposes of illustration, the memory locations 600-608 correspond to the exemplary data blocks A-E. In
20 the example of FIG. 6, each of the memory locations 600-608 has a memory width (W) of four bytes. The DMA engine 404 must respectively copy the codeword-size data blocks A-E into the memory locations 600-608. In a first stage of de-interleaving the byte stream 500, the DMA engine 404 writes the first block A, is indexed 0, -, -, -, 1, into the memory location 600 in the
25 manner illustrated in FIG. 6.

A common requirement on many different types of memories is that data must be written to the memory in integer multiples of the memory width (W). Although exceptions to this requirement are possible, the exceptions provide inefficient, overly complex schemes that sacrifice speed and power
30 and erode other valuable system resources. Therefore, in the present invention, the DMA engine 404 will copy the five bytes of the data block A,

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and all of the other five byte codeword-size blocks B-G, into the buffer 408 in multiples of four bytes at a time.

Since the data blocks A-E are five bytes in width, and thus not a multiple of the memory width (W) of four bytes, the data blocks A-G must be
5 appended, or padded, with three dummy padding bytes 610-618 respectively. This padding artificially converts the length of each of the blocks A-E to eight bytes, a multiple of the memory width (W) four. With all of the exemplary data blocks A-E, including the appended padding bytes 610-618, now having been stored in the respective memory locations 600-608, the DMA engine 404
10 must now perform the de-interleaving.

FIG. 7 is an illustration of essential parameters used by the DMA engine 404 to de-interleave the now padded data blocks A-E, stored in the memory locations 600-608 of the buffer 408. The DMA parameters shown in FIG. 7 are typically stored in DMA registers or storage areas, such as the
15 DMA memory storage area 406. As noted above with reference to FIGs. 5 and 6, the byte stream 500 and the DMA parameters of FIG. 7 are for the exemplary case where the interleave depth (D) is 4 and the byte size (N) is 5. traditional DMA engines use many other DMA parameters to perform de-interleaving. The present invention also uses some of these other DMA
20 parameters. For purposes of clarity, however, the present application will not address these other parameters since their use remains unchanged in the present invention. Instead, the description of the present invention will focus on the DMA parameters shown in FIG. 7.

The STRIDE is the first of the DMA parameters listed in FIG. 7, and is
25 has a value of 4. In the present invention, the STRIDE is the distance from one byte, that requires copying to memory, to the next byte requiring copying. STRIDE2, with a value of 4+3, is similar to the STRIDE, plus the number of padding bytes, such as the three bytes of padding 610 stored in the memory location 600. Thus, in the case of STRIDE 2, the DMA engine will skip over
30 the padding bytes 610 in addition to the interleave depth. The number of padding bytes is referred to as the PADSIZ.

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In the example of FIGs. 6 and 7, the STRIDE increments through all of the values of the block A (0,-,-, and 1) to obtain the value "1." And the "3" in the STRIDE2 implies skipping over the "5" and the two dashes that follow the "5" of the block B, to get to the "2" value of the block B. Also included in the DMA parameters are the values of OFFSET, OFFSET INC, and OFFSET MOD, discussed in greater detail below.

The following is an exemplary approach to initializing the DMA parameters shown in FIG. 7 of the instant invention:

```

10      stride      = floor(D / N) * (N + PADSIZ) + (D mod N)
      stride2     = stride + PADSIZ
      offset      = 0
      offsetInc   = D mod N
      offsetMod   = N

```

where D is interleave depth
 N is interleave length (i.e. including any pre-interleave padding)
 PADSIZ is number of padding bytes per codeword (including any pre-interleave padding not transmitted which is negative)

The DMA computes each address to copy from as follows:

```

      offset += offsetInc
      if (offset >= offsetMod) then
25          offset -= offsetMod
          address += stride2
      else
          address += stride

```

FIG. 8 is an illustration of an exemplary DMA address sequence for determining the order in which the de-interleaved data bytes of the blocks A-E are read from the buffer 408. In FIG. 8, step 0 represents the reading of address A, which is the beginning of the buffer 408, where the bytes are numbered from left to right. Thus, the DMA engine 404 will first read the value "0" at address A. Address A corresponds to the first byte of the first row of the memory location 600 of the buffer 408. Next, in step 1, the DMA engine 404 will increment the address by the STRIDE value of "4." Thus, address A+4 of the buffer 408 will be read, which contains the value "1." The

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address A+4 corresponds to the first byte of the second row of the memory location 600.

In step 2 of FIG. 8, the STRIDE2 of FIG. 7 will be used instead of the STRIDE, which represents an increment of 7. Thus, the DMA engine 404 will skip over 7 values to obtain the value of "2," shown in byte position four of the memory location 602. The DMA engine 404 will continue to read the remaining contents of the memory locations 602-608 to finally produce a de-interleaved byte stream sequenced as 0,1,2,3,4,5....

In any particular read cycle, the DMA engine 404 will use STRIDE or STRIDE2, but not both at the same time. Thus, the DMA engine 404 must know apriorily whether to use STRIDE or STRIDE2. The values of the OFFSET column of FIG. 8 determine whether the DMA engine 404 will use STRIDE or STRIDE2. The values of the OFFSET column operate based upon a modulo-n counting scheme. The modulo-n counting scheme controls the OFFSET, OFFSET INC, and OFFSET MOD (the modulo of how the offset of FIG. 8 is incremented) of the DMA parameters shown in FIG. 7.

The offset of FIG. 8 initially begins at 0, and for each step, is incremented by the OFFSET INC value. If the offset is initially 0, it will ordinarily be incremented by 4 each time. However, the offset counts by modulo. Therefore, in the example of FIGs. 5 -8, the only legal numerical values are 0-4, since the present example is based on modulo-5. The OFFSET MOD value corresponds to the byte size (N). Thus, in FIG. 8 at step 0, the offset is 0, and then the DMA engine 404 increments by 4. In step 1, the offset is 4. In step 2, the DMA engine 404 increments by 4 again, and so it would ordinarily be 8. The value, however, gets reduced because the counting is based on modulo-5, which in-turn, produces the offset value of 3. The remaining values of the offset column of FIG. 8 are determined in this manner and this process continues until the entire byte stream 500 is completely de-interleaved.

Thus, in accordance with the present invention, the DMA engine 404 uses two strides to facilitate an efficient implementation of a UMA memory technique. This technique ensures that codeword-size data blocks can be

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written into memories in cases where the originally transmitted data blocks are not an integer multiple of the width (W) of the input buffer memory. In so doing, this process eliminates the need to perform alignment and partial word writes of the data blocks, which provides significant savings of system resources.

IV. Conditional One's-complement of Partial Address to Map Butterfly Address Generation to FFT/IFFT Post-/Preprocessing Pass Address Generation.

Processors, such as the control processor 205 of FIG. 2, support FFT/IFFT functions through use of standard radix-2 butterfly operations. These butterfly operations are specific implementations of an FFT algorithm in cases where the number of input samples is a power of 2. In order to implement these FFT/IFFT functions, the processor 205 includes address generation logic to access the input and output operand pairs (address pairs) of each butterfly.

One way of generating the butterfly input and output address pairs is to use a pointer and a fixed offset to access the operands at addresses 'pointer' and 'pointer+offset', incrementing the pointer through each recursion in the FFT/IFFT stage. A preferred approach would be to support optimized implementations of the FFT/IFFT for real-valued FFT inputs and IFFT outputs using standard post and pre-processing steps. Using standard post and pre-processing steps, however, the inputs to the butterfly operations of the post-and pre-processing steps are not separated by a fixed offset, and thus cannot use the normal operand addressing logic.

As a solution, the present invention uses an exemplary circuit implementation to conditionally invert the $n-1$ least-significant bits (LSBs) of the butterfly operand addresses provided for an N -point FFT/IFFT, where $N = 2^n$. The $n-1$ LSBs are inverted when the n 'th operand address bit (address[n-1] where the LSB is address[0]) is 1, otherwise the LSBs are unchanged. This effectively reverses the last $N/2$ inputs to the real-valued FFT post-processing

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pass or IFFT pre-processing pass, yielding un-unfixed offset between the inputs to the butterfly operations of the pass.

FIG. 9 is an illustration of a conventional 512 point FFT implementation 900. In FIG. 9, pairs of 512 real-valued inputs 902 are represented in the form of a 256 point (pre-processing) complex FFT 904. Using a traditional FFT approach, the 256 point complex FFT values are processed in the stage 904. Next, a conventional FFT post-processing stage 906 is implemented to produce 256 complex outputs 908. FIGs. 10 and 11 provide more detailed illustrations of the complex FFT operation 904 and the FFT post-processing stage 906.

In FIG. 10, a complex FFT operation, such as the pre-processing FFT operation 904, is implemented using a standard radix-2 butterfly 1000. A butterfly is a computational technique that takes a pair of real-valued FFT inputs and produces a pair of complex outputs. While the FFT operation 904 of FIG. 9 is a 256 point FFT, for purposes of simplification, the butterfly technique 1000 is demonstrated using an 8 point FFT.

In the illustration of FIG. 10, 8 complex value inputs 1002 (representative of 16 real-valued inputs) are provided as inputs to the butterfly 910. Outputs 1004 of the butterfly 1000 are represented as output addresses B0-B3. The output address B0 is associated with complex value inputs 0 and 4, which are provided as inputs to a first butterfly calculation (of the butterfly 1000). The output address B1 is associated with inputs 1 and 5, which were provided as inputs to a second butterfly calculation, the address B2 is associated with inputs 2 and 6, and so on, as illustrated in the step/address table 1006, also shown in FIG. 10. A point of interest with regard to the output addresses B0-B3, is that distances 1008-1012 (or offsets) between the addresses B0-B3 are fixed, with respect to each of the butterfly calculations of the butterfly 1000.

In FIG. 11, a standard post-processing operation, such as the post-processing operation 906, is implemented using a butterfly 1100. The butterfly 1100 receives inputs pairs 1102 and produces outputs 1104, shown as addresses C0-C2. In the post-processing butterfly 1100, however, offsets

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1106-1110, associated with the inputs 1102, are not fixed. That is, the offsets 1106-1110 decrease in length for each of the butterfly calculations associated with the butterfly 1100. In an exemplary embodiment of the present invention, FFT pre-processing output addresses having fixed offsets, such as the exemplary addresses B0-B3, are transformed into FFT post-processing addresses having decreasing offsets, such as the exemplary addresses C0-C2.

FIG. 12 is a block diagram illustration of an exemplary circuit 1200 be configurable to transform the addresses output from an FFT pre-processing stage into addresses representative of an FFT post-processing stage. The circuit 1200 can be inserted into the logic path of a DSP controller, such as the controller 205 of FIG. 2, to perform this address transformation.

The circuit 1200 is coupled to an output of a conventional FFT address generator 1201. The address generator 1201 is included as part of an FFT intermediate processing FFT algorithm, such as the operation 904, and produces FFT complex values, such as those that would be provided to the post-processing operation 906. At a high level, the circuit 1200 is configured to perform a conditional one's complement of the address output from the address generator 1201.

The circuit 1200 includes a mask generator 1204 and a logic gate 1206 configured to perform a complementing operation. In the embodiment of FIG. 12, the logic gate is an exclusive OR gate, although other suitable logic circuits can be used. A value (n) specifies the number of address lines or bits output from the FFT address generator 1201. Another value (N) represents the size of the FFT operation to be performed, such as 256 point or 512 points, and is provided as an input to the mask generator 1204.

The mask generator 1204 allows the circuit 1200 to function with FFTs of different sizes. The mask generator 1204 also determines how many of the bits, output from the address generator 1201, should be complemented. A pre/post processing enabling signal 1208 is provided as input to the mask generator 1204. The signal 1208 enables the circuit 1200 when an FFT computation reaches the post-processing stage 906. The function of the circuit 1200 is explained in greater detail below, in relation to FIG. 13.

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FIG. 13 is a detailed illustration of exemplary outputs 1300 of the FFT generator 1201. FIG. 13 also illustrates exemplary masks 1302. Each row of the masks 1302 is associated with a corresponding one of the rows of the outputs 1300, as indicated by the arrows. As noted above, the value (N) specifies the size of the FFT operation to be implemented. The example of FIG. 10, where (N) is 8, corresponds to the first two rows of the outputs 1300. An (N) value of 16 corresponds to the third and fourth rows of the addresses 1300 and masks 1302. In the example where (N) is 8, there is only one bit of the FFT generator 1201 that will control one of two output values of its corresponding mask within the mask values 1302.

When the signal 1208 indicates that the FFT post-processing is occurring, the mask generator 1204 is enabled. The output of the mask generator 1204 is then exclusively OR'd with the addresses having fixed offsets, output from the address generator 1201. The output of the circuit 1200 is a conditionally inverted address sequence having decreasing outputs, as discussed above. FIG. 14 is a more detailed illustration of the output of the circuit 1200.

In FIG. 14, steps 2-255 are shown, each corresponding to one of the addresses within an address sequence 1402. The address sequence 1402 is provided as an output from the address generator 1201 and includes fixed offsets (1/128, 2/129, 3/130, etc.). The circuit 1200, however, transforms the address sequence 1402, as described above, into the address sequence 1404 having decreasing offsets (1/255, 2/254, 3/254, etc.).

The present invention, therefore, provides significant economies by enabling the calculation of the post-processing FFT address sequence directly from the output of the FFT address generator 1201. This calculation is achieved through the use of simple logic circuit that performs a one's complement of the fixed offset addresses and a mask of the address. Thus, the techniques of the present invention facilitate savings of significant hardware resources that would ordinarily be dedicated to performing FFT post processing address.

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V. Definition and Implementation of SLICE Instructions on a Programmable SIMD Processor Data Path.

An important function in digital communication receivers is the 'slicing' of a received data symbol to determine the nearest point (or phase state) on a constellation grid. That is, the digital communication receivers must be able to closet grid point, from a standpoint of distance, that a particular received symbol value is associated with when it was transmitted. Put more simply, the receiver use slicing to determine precisely what was originally transmitted.

One commonly used approach to perform slicing in a DSP is through execution of a sequence of conventional instructions. The slicing function can also be implemented in dedicated logic, but this approach is inflexible and requires additional hardware resources. Dedicated logic, however, is unnecessary in systems where data paths of a SIMD based programmable DSP, such as the controller 205 of FIG. 2, can be modified to perform the slicing functions.

The instant invention provides an approach for slicing operations to be more efficiently and upported directly on a programmable DSP. This more efficient approach is facilitated through extensions to the instruction set, modifications to internal data paths, and use of control logic. The slicing operations are implemented using the data path logic that is provided for other basic operations.

DSPs typically provide functional units for multiplication, addition (accumulation) and result scaling. Many DSPs provide multiple sets of such units, controlled with a SIMD scheme to enhance performance. Slicing can be efficiently implemented using pairs of such units processing the in-phase and quadrature phase (I and Q) components of a received symbol. A more detailed discussion of preferred embodiments of the present invention is provided below in relation to a description of FIGs. 15-20.

FIG. 15 is a block diagram illustration of a conventional three stage DSP functional SIMD based data module 1500, having first and second

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parallel paths 1502 and 1504. Since the first and second data paths 1502 and 1504 include identical functional modules, the discussion of the first parallel path 1502 will apply equally to the parallel path 1504. The conventional data module 1500 includes a first pipeline stage 1506 including a multiplier 1507, a second pipeline stage 1508 including an adder 1509, and a third stage 1510 including a scalar 1511. Also included are registers 1512 for holding addresses or instructions used for manipulation of data passed through each of the stages of the data module 1500.

In the conventional functional data module 1500 illustrated in FIG. 15, input operands OP1n and OP2n are received, from general registers, as inputs to the stage 1506 of the first path 1502 during a current timing cycle. The input operand OP1n might, for example, be representative of the "I" component of a received data point in the exemplary form of a 16 bit data word. The operand OP2n is traditionally representative of a scaling factor. The operands OP1n and OP2n are multiplied together in the multiplier 1507.

Next, the product of the multiplier 1507 is provided to the input of the adder 1509 in accordance with, for example, instructions stored in one of the registers 1512. In the module 1500, the second data path 1504 is configured to receive symbol data associated with the symbol's "Q" component, as discussed above. Further, while the first stage 1506 process the input from the current timing cycle, the stage 1508 is simultaneously processing an input from a previous timing cycle and the stage 1510 is simultaneously processing an input from an even earlier timing cycle.

A rounding value, provided as an input to a mutiplexer 1514, is added to the first product of the multiplier 1507 during the noted timing cycle. For subsequent products output from the multiplier 1507, the multiplexer 1514 selects its lower path such that the products are added with previous sums. A rounding value is provided so that when scaling is performed in the third stage 1510, the scaling will be performed on a sum having a fixed number of data bits.

Next, the result from the adder 1509 is scaled in the third stage 1510 by a scalar 1511. The scalar 1511 multiplies the result, output from the adder

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1509, times $2^{(-k)}$, where (k) is specified by the DSP instructions. The output of the scalar 1511, labeled as RSLTn, is then provided as an overall output of the data module 1500. As previously noted, FIG. 15 is an illustration of a conventional SIMD processor data path. FIG. 16, however, is an illustration of modifications, in accordance with the present invention, to the conventional data path of FIG. 15. This modification enables the data path to more efficiently support symbol slicing instructions.

In general terms, FIG. 16 provides a block diagram illustration of an exemplary data path module 1600 capable of performing symbol slicing instructions as part of its instruction set, i.e., performing the slice instruction as a primitive instruction. An advantage of the approach of the present invention is a reduction in the number of input cycles required to execute slice instructions. In a conventional DSP, slice instructions can require 20 or more cycles for execution. In the exemplary embodiment of FIG. 16, however, slice instructions can be executed within about two cycles.

More specifically, FIG. 16 includes a data path module 1600 including conventional components, such as the multiplier 1507, the adder 1509, and the scalar 1511, shown in FIG. 15. The module 1600, however, also includes an additional operand path 1602 and an additional multiplexer 1604.

A constants generator 1606 is provided to scale the bit stream associated with OP1 (the I or Q component) into a format that has its binary point in a fixed position. The scaling directly supports the slicing function and scales each of the I and Q components to a fixed format by multiplying OP1 by $2^{(k-b)}$, where k is a constant chosen based on the data path precision and b, an instruction parameter or operand, indicates the number of fractional bits in, for example, the 16 bit data stream of the I or Q component.

When control logic of the DSP detects that the data module 1600 is executing a slicing instruction instead of standard DSP instructions, the multiplexer 1604 selects its operand path 1602 (lower path). When the path 1602 is selected, OP1 is received and is multiplied by the expression $2^{(k-b)}$ and is thus scaled into the fixed binary point format. The use of a fixed format simplifies subsequent processing.

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Next, OP1n and the fixed format value (output from the constants generator 1606) are multiplied together in the multiplier 1507. The product of the multiplier 1507 is provided as an input to another multiplexer 1608. Also provided as an input to the multiplexer, are boundary constraints 1610 which are output from a slice decoder 1700, illustrated in FIG. 17. The slice decoder 1700 and the boundary constraints 1610 are discussed in greater detail below and in relation to FIG. 17.

FIG. 17 is an illustration of an exemplary slice decoder 1700. The slice decoder 1700 is conventional logic that is configured to receive the sign bits of the I and Q components associated with the received symbol data. The decoder 1700 also receives data representative of the particular constellation grid associated with the transmitted symbol data. The output of the decoder 1700 is a set of I and Q limit values 1610 (boundary constraints) and a set of I and Q load enable conditions 1702. The limit values 1610 and the enable conditions 1702 are a function of the location of the received symbol on a particular constellation grid, such as the grid shown in FIG. 18.

FIG. 18 is a graph of a conventional 4 x 4 constellation grid 1800. Constellation grids are representative of accepted communications standards and include two-dimensional displays of the baseband I and Q values of transmitted and received data symbols, as measured at a particular point in time. A vector from the center of the diagram to a specific constellation point is representative of the amplitude of the symbol. When symbol data is originally transmitted, its I and Q components have specific coordinates within a constellation grid. Due to noise, transmission error, and other factors, the symbol's receive constellation grid values often differ from its transmission constellation grid values. As noted above, the present invention is an efficient technique to determine the original transmitted constellation grid values of the originally transmitted data symbol.

Although the constellation grid of FIG. 18 is a 4 x 4 representation, the present invention can operate with constellation grids of other sizes, such as 2 x 2, 8 x 8, or diagrams that are not square. In FIG. 18, the points "A" and "B" are representative of the I and Q components of bits that combine to form a

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transmitted data symbol. When the points "A" and "B" were originally transmitted, they were associated with specific coordinates, or points, on the grid 1800. During transmission, however, the points moved off of their original grid coordinates as shown.

5 Therefore, the DSP, using instructions within the data module 1600, must slice the received symbol data to determine which of the coordinates on the grid that the points "A" and "B" were originally transmitted on. With reference to FIG. 17, the limit values 1610 are representative of the limits of the I and Q axis of the grid. In the exemplary grid 1800, the limits of the I
10 axis are +3 and -3, and the limits of the Q axis are also +3 and -3. These limits define a ring of grid points. The I and Q conditions 1702, on the other hand, are associated with whether the "A" and "B" points are actually within the ring of points.

 Referring back to FIG. 16, the product of the multiplier 1507 is
15 representative of an actual I or Q component of one of the A and B points. This product is received as an input to the multiplexer 1608. The multiplexer 1608 then alternately provides the product of the multiplier 1507 and the I and Q limit values 1610 to the adder 1509, which in the present invention, is used
20 as a comparator. The output of the adder 1509 is used to determine whether the points A and B are within the ring of I and Q points (finite grid) or outside the ring of points (infinite grid). As seen in FIG. 18, A is within the ring of points and B is outside.

 The output of the adder 1509 is provided as an input to a quantizer
25 circuit 1612. The quantizer circuit 1612 essentially forces the points A and B to the nearest point on the infinite grid. Subsequent cycles use the adders to implement boundary clamping via per-quadrant min/max operations that conditionally load the result registers (accumulators) based on comparisons performed by the adders (with possible auxillary comparisons). The constants
30 can be read from a table indexed by an instruction operand or directly specified by the operand. Additional details of the circuit 1612 are provided in the discussion concerning FIG. 19.

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In FIG. 19, the quantizer circuit 1612 includes an OR gate 1900 and an AND gate 1902 coupled to the OR gate 1900. A quantize signal is provided by the DSP control logic as a control signal to activate the quantizer 1612. At a more detailed level, the quantizer masks the k LSBs of the symbol data prior to storage in a results register 1614 (accumulator) to implement the quantization of each component when enabled. Also added to the results register 1614 are the I and Q conditions (load enable) 1702 from the slice decoder 1702 shown in FIG. 17. The quantized components are compared against constants determined by the constellation size and sign of the component in the accumulator register 1614. In other words, the accumulator results register 1614 compares the results of the quantizer with the actual I and Q input data symbol conditions.

The quantizer 1612 essentially forces the LSBs of the receive symbol data, to zero. The k-1 bits go through the AND gate 1902 and the next bits are received by the OR gate 1900. The most significant bits, which are left over, simply pass through the quantizer 1612 and remain unchanged. When the quantizer 1612 is in use, the adder 1509 can be used to implement symmetric rounding (about the point origin) and/or offset adjustment for constellations that aren't centered about the point origin.

Finally, an output from the results register 1614 is provided to the scalar 1511. The results scalar 1511 is used to divide each component by $2^{(k-b)}$ to return the components to the input format. The output of the scalar 1511 is a determination of the nearest grid points to the points A and B, within the constellation grid 1800. An exemplary slicing sequence implemented by the data module 1600 will be described in relation to a description of FIG. 20.

FIG. 20 is an exemplary table 2000 representative of two input cycles of the data module 1600. In FIG. 20, data points A and B are shown along a vertical column to the left. A "cycle" column shows two input cycles of the data path module 1600 for receiving input symbol data related to data points A and B. In cycle 1, the table 2000 shows that a quantize enable signal is "set" to activate the quantizer 1612. Since the quantize signal is present, the

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limits and conditions, included in the table 2000, are not used. Thus, the module 1600 will select the nearest grid point in infinite grid.

The grid 1800 illustrates that the nearest grid point in infinite grid of the I and Q coordinates, for point A, are -1 and -1. In cycle 2, the quantization has already been accomplished so the quantization signal is not set. Thus, the next comparison of the input symbol data is against the limits. Here, the I limit is -3 and a condition of "less than." The conditions of "less than" or "greater than" are a function of the quadrant that the point appeared in.

Similarly, for Q, the limit is -3, with a condition of "less than." Since in this case, the nearest point on infinite grid was within the actual 4 x 4 grid, the second cycle did not make any changes. Therefore, the result of the symbol slicing in this case was -1 and -1 for both the I and Q components, which correspond with a point on the grid 1800. The results for the point B, however, are slightly different.

The table 2000 illustrates that for the cycle 1, the quantize control signal is set. Therefore, the first step will be to quantize the symbol data associated with B onto the infinite grid. In this case, the output coordinates for I and Q are 1 and -5 respectively. The first arrow pointing away from point B on the grid 1800, points to the coordinates 1 and -5 for I and Q respectively. During cycle 2, the point B is compared against the limit of the finite grid. This comparison illustrates that the data point B is outside of this limit. Here, therefore, the result of cycle 2 is 1 and -3 for the I and Q limits, respectively. Thus, both points A and point B have now been associated with their nearest points in infinite grid, and consequently, associated with their original constellation grid coordinates.

The present invention, therefore, provides an approach for slicing operations to be more efficiently supported directly on a programmable DSP. The approach of the invention is facilitated through extensions to the instruction set, modifications to internal data paths, and use of control logic. The slicing operations are implemented using the data path logic that is provided for other basic operations. This approach facilitates performing the

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slice instruction as a primitive instruction. An advantage of the approach of the present invention is a reduction in the input cycles required to execute a slice instruction. The present invention reduces the required cycles from 20 to 2 or 3 cycles.

5 VI. Program Synchronization of A Processor and DMA Using Ownership Flags.

A processor DSP is often paired with a DMA engine and two working memories so that processor execution on data in one memory can overlap DMA transfers to and from the other memory. Higher performance processors
10 require more bandwidth than can be provided by a single working memory; additional bandwidth can be supplied by additional working memories. A synchronization mechanism is required to ensure that a given working memory is only in use by either the processor or the DMA at any given time, and to provide flow control of data passed between the processor and DMA
15 engine.

FIG. 21 is a block diagram illustration of an exemplary processor/DMA memory sharing scheme 2100. In FIG. 21, the memory sharing scheme 2100 includes another exemplary DMA engine 2102, a processor 2104, memories A-D, and associated ownership flags 2106.

20 FIG. 22 is an illustration of exemplary DMA program instructions 2200 and processor program instructions 2202, used in connection with the DMA engine 2102, the processor 2104, and the memories A-D.

Finally, FIG. 23 is an illustration of management and execution of the DMA program instruction 2200 and the processor program instructions 2202
25 based upon specific settings of the ownership flags 2106.

Systems with two or more working memories, such as the memories A-D, typically have the DMA engine 2102 and processor 2102 wait for each other upon completion of the tasks 2200 and 2202, shown in FIG. 22. When both the DMA engine 2102 and the processor 2104 have finished, the roles of
30 the memories A-D are swapped and the DMA engine 2102 and the processor

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2104 continue with the next set of tasks. This process is repeated for each set of tasks.

5 The ownership flags 2106 are provided to indicate, for each of the memories A-D, whether its use is controlled by the DMA engine 2102 or processor 2104. Specific instruction sets are provided for both the DMA engine 2102 and the processor 2104 for testing and setting the flags 2106. One instruction, from within the instruction set 2102, waits for the specified set of ownership flags to indicate ownership by the DMA engine 2102 or the processor 2104 executing the instruction. The other instruction sets the
10 specified set of ownership flags 2106 to indicate ownership by the DMA engine 2102 or the processor 2104 not executing the instruction.

 The memory sharing scheme 2100, along with software convention, allows programs running on the DMA engine 2102 and the processor 2104. The scheme 2100 avoids simultaneous use of the exemplary working
15 memories A-D by transferring ownership of the memories, when finished with the memory, and waiting for ownership before accessing the memory. Similarly flow control is implemented by waiting for ownership of the memory containing the data being transferred before operating on it.

 The present invention has been described above with the aid of
20 functional building blocks illustrating the performance of specified functions and relationships thereof. The boundaries of these functional building blocks have been arbitrarily defined herein for the convenience of the description. Alternate boundaries can be defined so long as the specified functions and relationships thereof are appropriately performed.

25 Any such alternate boundaries are thus within the scope and spirit of the claimed invention. One skilled in the art will recognize that these functional building blocks can be implemented by analog and/or digital circuits, discrete components, application specific integrated circuits, firmware, processors executing appropriate software and the like or any
30 combination thereof. Thus, the breadth and scope of the present invention should not be limited by any of the above-described exemplary embodiments,

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but should be defined only in accordance with the following claims and their equivalents.

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WHAT IS CLAIMED IS:

1. A modem, comprising:
5 one or more processing paths; and
a number of interconnected modules sequentially arrayed along the one or more of the processing paths, each module being configured to (i) process signals passed along the paths in accordance with the sequence and (ii) implement unique functions to perform the processing;
10 wherein each of the modules has a particular degree of functional programmability; and
wherein the degrees of functional programmability monotonically vary in accordance with the sequence.
- 15 2. The modem of claim 1, wherein the modem is an asymmetric digital subscriber logic (ADSL) modem.
3. The modem of claim 2, wherein the one or more processing paths include a receive path and a transmit path.
20
4. The modem of claim 3, wherein the interconnected modules includes at least one of an analog front end, a discrete multi-tone module/frequency domain equalizer and a direct memory access engine.
- 25 5. The modem of claim 1, wherein the predetermined functions include at least one of resampling, echo cancellation, fourier processing, and error correcting.
- 30 6. The modem of claim 5, wherein the functional programmability includes non-programmable hardware, programmable hardware, firmware, and software.

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7. The modem of claim 5, wherein the variations are representative of monotonic increases.

5 8. A modem comprising:
a receiver associated with a receive timing scheme;
a transmitter associated with a transmit timing scheme; and
only one timing mechanism (i) electrically coupled to the receiver and
the transmitter and (ii) configured to synchronize the receive and transmit
timing schemes.

10

9. The modem of claim 9, wherein the receiver includes a receive
re-sampler and the transmitter includes an transmit re-sampler.

15 10. The modem of claim 9, wherein the modem is an asymmetric
digital subscriber line (ADSL) modem.

11. The modem of claim 10, wherein the timing mechanism
includes a phase accumulator.

20 12. The modem of claim 10, wherein the timing mechanism
includes a coefficient generator and a phase accumulator.

25 13. A modem comprising:
a receive re-sampler configured to receive input signals in accordance
with a receive timing scheme;
a transmit re-sampler connected, at least indirectly, to the receive re-
sampler, the transmit re-sampler being configured to transmit output signals in
accordance with a transmit timing scheme; and
only one timing mechanism electrically coupled to the receive re-
30 sampler and the transmit re-sampler;
wherein the timing mechanism is configured to synchronize the receive
timing scheme and the transmit timing scheme.

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14. The modem of claim 13, wherein the modem is an asymmetric digital subscriber line (ADSL) modem.

5 15. The modem of claim 14, wherein the receive input signals includes digitized input signals.

10 16. The modem of claim 15, wherein the receive re-sampler produces interpolated signals based upon the received input signals and first timing coefficients.

15 17. The modem of claim 16, wherein the transmitted output signals include digitized output signals.

18. The modem of claim 16, wherein the transmitted output signals include second timing coefficients.

20 19. The modem of claim 18, wherein the first and second timing coefficients are produced based upon linear interpolation, the linear interpolation being a function of phase increment and phase accumulator.

25 20. The modem of claim 19, wherein the timing mechanism includes a phase accumulator.

21. The modem of claim 19, wherein the timing mechanism includes a phase accumulator and a coefficient generator.

30 22. The modem of claim 16, further comprising a timing tracking mechanism configured to receive the interpolated signal and produce timing data therefrom.

- 40 -

23. The modem of claim 22, wherein the phase accumulator is configured to (i) receive the timing data and (ii) update the first and second timing coefficients based upon the received timing data.

24. A method for synchronizing timing in a modem having a receiver configured to receive an input data signal and a transmitter configured to produce an output data signal, the output data signal having timing characteristics based upon a transmit coefficient signal, the method comprising:

receiving (i) the input data signal and (ii) a receive coefficient signal in the receiver;

re-sampling the input data signal based upon the received coefficient signal to produce an interpolated signal thereby;

producing signal phase data based upon the interpolated signal; and

updating the receive coefficient signal and the transmit coefficient signal based upon the signal phase data.

25. The method of claim 24, wherein the signal phase data includes a phase increment, a phase tweak, and a coefficient factor.

26. The method of claim 24, wherein the updating includes adjusting a phase of the receive coefficient signal and transmit coefficient signal.

27. A method for de-interleaving a data stream stored in a buffer having a plurality of memory locations, each location having a memory width of (W) bytes, the data stream being formed of a number of data words each including (N) number of data bytes, wherein (N) is a non-integer multiple of the width (W), the method comprising:

storing the data words into respective memory locations;

appending each of the stored data words with number (X) of dummy bytes, a sum of (N) + (X) being an integer multiple of the width (W); and

- 41 -

storing the appended dummy bytes into the respective memory locations.

5 28. The method of claim 27, wherein the data words include codeword-size data blocks.

 29. The method of claim 28, wherein the interleaved data stream includes an interleave depth (D); and
 wherein the method is implemented based upon operation of a direct
10 memory access (DMA) engine.

 30. The method of claim 29, further comprising de-interleaving the data bytes stored in the respective memory locations based upon operation of the DMA engine and a number of parameters;
15 wherein the parameters include first and second memory strides, an offset increment value, and an offset modulo value.

 31. A method for storing a data stream in a modem buffer having a plurality of memory locations, each location having a memory width of (W) bytes, the data stream being formed of a number of data words each including (N) number of data bytes, wherein (N) is a non-integer multiple of the width (W), the method comprising:

 (a) copying the (N) data bytes of a first data word into a first [(n)(W)] bytes of a first location, where (n) is an integer that (i) equals one when $W > N$ and (ii) is a smallest among all integers satisfying the expression $[(n)(W) > N]$ when $W < N$;

 (b) appending the first number (N) of copied bytes with (X) number of dummy bytes, a sum of $(X) + (N)$ being an integer multiple of the width W; and

30 (c) copying the appended dummy bytes (X) into the first (n)(W) bytes of the first location.

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32. The method of claim 31, wherein the copied first number (N) of data bytes and the copied (X) dummy bytes correspond to the first data word.

5 33. The method of claim 31, further comprising copying the (N) data bytes a remaining number of the data words into the remaining memory locations in accordance with (a) through (c).

10 34. The method of claim 33, wherein the interleaved data stream includes an interleave depth (D) and the method includes a memory access technique having at least first and second memory strides.

15 35. The method of claim 34, further comprising de-interleaving the data bytes in the memory based upon operation of the DMA engine, the DMA engine ignoring the dummy bytes (X).

36. The method of claim 35, wherein the de-interleaving is based upon operation of the DMA engine and at least the first and second strides.

20 37. The method of claim 36, wherein the de-interleaving occurs based upon the operation of the DMA engine, values of the first and second strides, an offset increment value, and an offset modulo value.

25 38. The method of claim 37, wherein a value of the first stride is equal to the interleave depth, and a value of the second stride is equal to the interleave depth plus (X).

30 39. The method of claim 38, wherein the second stride is used instead of the first stride; and wherein the second stride is used based a modulo of the offset increment value.

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40. An apparatus for de-interleaving a data stream stored in a buffer having a plurality of memory locations, each location having a memory width of (W) bytes, the data stream being formed of a number of data words each including (N) number of data bytes, wherein (N) is a non-integer multiple of the width (W), the apparatus comprising:

means for storing the data words into respective memory locations;

means for appending each of the stored data words with number (X) of dummy bytes, a sum of (N) + (X) being an integer multiple of the width (W); and

means for storing the appended dummy bytes into the respective memory locations.

41. The apparatus of claim 40, wherein the data words include codeword-size data blocks.

42. The apparatus of claim 41, wherein the interleaved data stream includes an interleave depth (D); and

wherein the apparatus is implemented based upon operation of a direct memory access (DMA) engine.

43. The apparatus of claim 42, further means for comprising de-interleaving the data bytes stored in the respective memory locations based upon operation of the DMA engine and a number of parameters;

wherein the parameters include first and second memory strides, an offset increment value, and an offset modulo value.

44. A circuit, comprising:

a fast fourier transform (FFT) address generator configured to produce a complex FFT address sequence, the complex FFT address sequence having fixed offsets; and

- 44 -

a conversion mechanism configured to (i) receive the complex FFT address sequence and (ii) convert the received sequence into an address sequence having varying offsets.

5 45. The circuit of claim 44, wherein the circuit is included in a modem.

 46. The circuit of claim 45, wherein the modem is an asymmetric digital subscriber line (ADSL) modem.

10

 47. The circuit of claim 44, wherein the conversion mechanism is an FFT post-processing module.

 48. The circuit of claim 44, wherein the varying offsets vary in a decreasing direction.

15

 49. The circuit of claim 44, wherein the conversion mechanism performs the converting in lieu of FFT-post-processing.

20 50. The circuit of claim 44, wherein the conversion mechanism includes:

 a logic gate having first and second input ports and an output port, the first input port being coupled to an address generator output port, the output port being configured to output the address sequence having the varying offsets; and

25

 a mask generator having a third input port and an output port, the third input port being coupled to the address generator output port, and the mask generator output port being coupled to the second input.

30 51. The circuit claim 50, wherein the logic gate is an exclusive OR gate.

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52. A method for determining a fast fourier transform (FFT) post processing address sequence of an N-point FFT in a digital signal processor, the method comprising:

5 producing a complex FFT address sequence in response to N received complex FFT input samples, the complex FFT address sequence being representative of N/2 output address pairs having fixed offsets, the sequence including a bit stream having (n) data bits representative of a memory address of the output pairs, (N) being equal to 2^n ;

selecting particular ones of the data bits for complementing; and

10 performing an arithmetic operation between the selected particular ones of the bits and the complex FFT address sequence, the complement operation producing output address pairs having un-fixed offsets.

53. The method of claim 52, wherein the particular ones of the data
15 bits include an (n-1) least significant bit (LSB).

54. The method of claim 53, wherein an LSB address[0] is 1.

55. The method of claim 52, wherein selecting is implemented
20 based upon a masking operation.

56. The method of claim 52, wherein the arithmetic operation is a one's complement operation.

25 57. An apparatus for determining a fast fourier transform (FFT) post processing address sequence of an N-point FFT in a digital signal processor, the apparatus comprising:

means for producing a complex FFT address sequence in response to N received complex FFT input samples, the complex FFT address sequence
30 being representative of (N/2) output address pairs having fixed offsets, the sequence including a bit stream having (n) data bits representative of a memory address of the output pairs, (N) being equal to 2^n ;

- 46 -

means for selecting particular ones of the data bits for complementing;
and

means for performing a arithmetic operation between the selected
particular ones of the bits and the complex FFT address sequence, the
5 complement operation producing output address pairs having un-fixed offsets.

58. The apparatus of claim 57, wherein the particular ones of the
data bits include an (n-1) least significant bit (LSB).

10 59. The apparatus of claim 57, wherein an LSB address[0] is 1.

60. The apparatus of claim 57, wherein the selecting is
implemented based upon a masking operation.

15 61. The apparatus of claim 57, wherein the arithmetic operation is a
one's complement operation.

20 62. A method for implementing a SLICE operation in a
programmable digital signal processor (DSP) as a primitive instruction in one
or more data paths of at least one of (i) a single instruction single data scheme
and (ii) a single instruction multiple data scheme.

25 63. The method of claim 62, wherein the SLICE instruction is
executed in three or less input cycles.

64. The method of claim 62, wherein the SLICE operation includes
an input symbol slicing stage and a quantization stage.

30 65. The method of claim 64, wherein the input symbol slicing stage
occurs during a first input cycle and the quantization stage occurs during a
second input cycle.

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66. The method of claim 65, wherein the SLICE operation is configured to associate input symbol data with a particular point of a constellation grid, the constellation grid being stored in a memory of the DSP

5 67. A computer readable medium carrying one or more sequences of one or more instructions for execution by one or more processors to perform a method for implementing a SLICE operation in a programmable digital signal processor (DSP) as a primitive instruction in one or more data paths of a single instruction multiple data scheme.

10 68. A digital signal processor (DSP) including a number of single instruction multiple data (SIMD) path logic units, each logic unit including (i) a multiplier having two or more input ports, one of the input ports being configured to receive input symbol data, the multiplier being configured to produce a multiplier output, (ii) an adder configured to receive the output product and produce an adder output therefrom, and (iii) a scalar configured to scale the adder output, the DSP comprising:

15 a constants generator coupled to another one of the number of multiplier input ports and being configured to produce a fixed format signal based upon the input symbol data, the multiplier output being representative of a product of the received input symbol data and the fixed format signal;

20 wherein the adder is configured to (i) receive boundary constraints representative of a first component of predetermined symbol standards and (ii) compare the multiplier output with the boundary constraints, the adder output being representative of the comparison; and

25 a quantizer configured to (i) receive the adder output and (ii) associate the received adder output with a second component of the predetermined symbol standard, the quantizer producing a quantized output.

30 69. The DSP of claim 68, wherein the DSP includes a number of data paths, each of the logic units being respectively arrayed along one of the paths.

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5 70. The DSP of claim 68, wherein the constants generator produces the fixed format signal in accordance with the expression $2^{(k-b)}$, where (k) is a predetermined constant, and where (b) is indicative of fractional bits associated with the symbol data.

10 71. The DSP of claim 70, wherein the symbol standards are associated with a constellation grid; and
 wherein the constellation grid is formed of an infinite grid and a finite grid.

 72. The DSP of claim 71, wherein the first component is the finite grid.

15 73. The DSP of claim 72, wherein the bit stream includes least significant bits (LSBs) and the quantizer sets the LSBs to zero.

 74. The DSP of claim 73, wherein the quantizer includes a logic array.

20 75. The DSP of claim 13, wherein the quantizer includes a first logic gate having first and second input ports and a first output port, one of the first and second input ports being configured to receive the output sum and the other of the first and second input ports being configured to receive a control
25 logic signal; and

 a second logic gate having third and fourth input ports and a second output port, one of the third and fourth input ports being coupled to the first input port and the other of the third and fourth input ports being coupled to the second input port, the second output port being coupled to the first output port.

30 76. The DSP of claim 75, wherein the first logic gate is an OR gate; and

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wherein the second logic gate is an AND gate.

77. The DSP of claim 76, wherein the second component is a nearest point within the infinite grid.

78. The DPS of claim 77, further comprising an accumulator configured to (i) receive condition data representative of a location of the input symbol data and (ii) update the quantized output based upon the received condition data.

79. A method of slicing a receive data symbol in a digital signal processor including a number of single instruction multiple data path logic units, each logic unit including (i) a multiplier having two or more input ports, one of the input ports being configured to receive input symbol data, the multiplier being configured to produce a multiplier output, and (ii) an adder configured to receive the output product and produce an adder output therefrom, the method comprising:

producing a fixed format signal based upon the input symbol data, the fixed format signal being multiplied by the input symbol data to produce the multiplier output;

comparing the boundary constraints with the multiplier output, a result of the comparing being representative of the adder output; and

associating with a second component of the predetermined symbol standard.

80. The method of claim 79, wherein the fixed signal format is produced in accordance with the expression $2^{(k-b)}$, where (k) is a predetermined constant, and where (b) is indicative of fractional bits associated with the symbol data.

81. The method of claim 79, wherein the fixed format signal is formed of a bit stream having a fixed binary point.

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82. The method of claim 79, wherein the input signal includes a phase component and a magnitude component.

5 83. The method of claim 79, wherein the symbol standards are associated with a constellation grid.

 84. The method of claim 83, wherein the constellation grid is formed of an infinite grid and a finite grid.

10 85. The method of claim 84, wherein the first component is the finite grid.

 86. A method for sharing one or more memories between one or more processors, each memory being associated with a respective ownership flag, the method comprising:

 associating each of the processors with a particular value of the flag;
 and
 assigning use of the memories to a corresponding one of the processors
20 when the respective ownership flag is set to the particular value.

 87. The method of claim 86, wherein each of the processors is associated with a different particular value.

25 88. The method of claim 87, wherein the particular values are changeable in association with selected processor cycles.

 89. The method of claim 88, wherein the use of a particular memory includes ownership of the memory during the during the selected
30 processor cycle.

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90. The method of claim 89, wherein each memory is assigned to only one processor during any one of the processor cycles.

5 91. An apparatus for sharing one or more memories between one or more processors, each memory being associated with a respective ownership flag, the apparatus comprising:

means for associating each of the processors with a particular value of the flag; and

10 means for assigning use of the memories to a corresponding one of the processors when the respective ownership flag is set to the particular value.

92. The apparatus of 91, wherein each of the processors is associated with a different particular value.

15 93. The apparatus of claim 92, wherein the particular values are changeable in association with selected processor cycles.

20 94. The apparatus of claim 93, wherein the use of a particular memory includes ownership of the memory during the during the selected processor cycle.

95. The apparatus of claim 94, wherein each memory is assigned to only one processor during any one of the processor cycles.

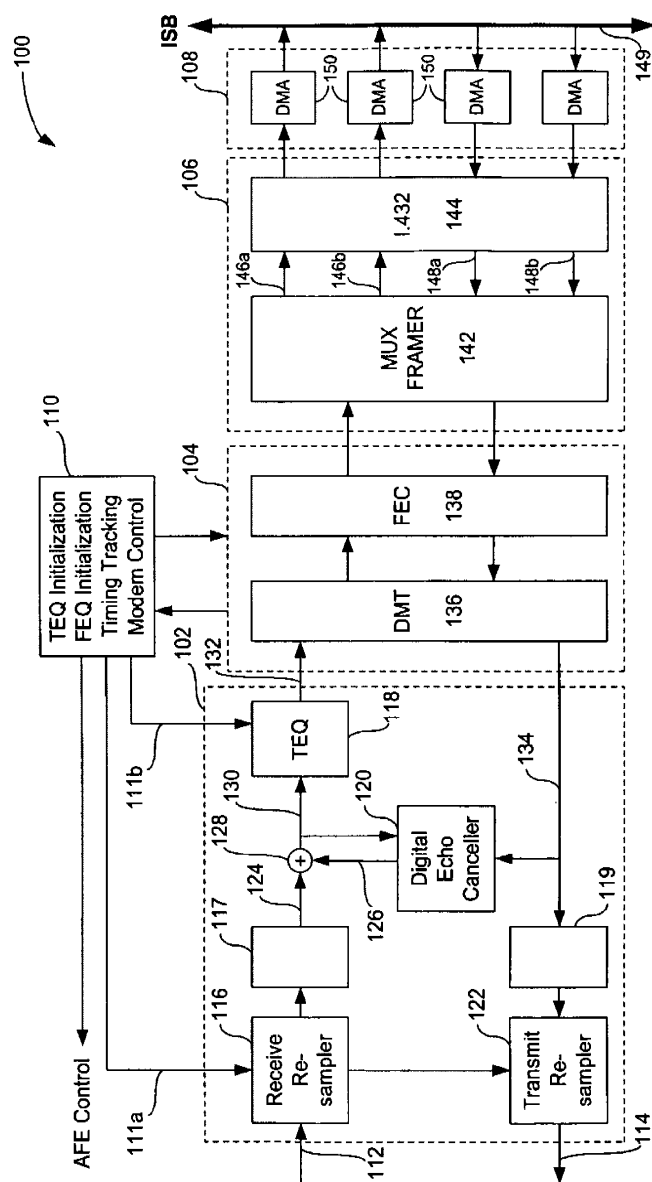


FIG. 1

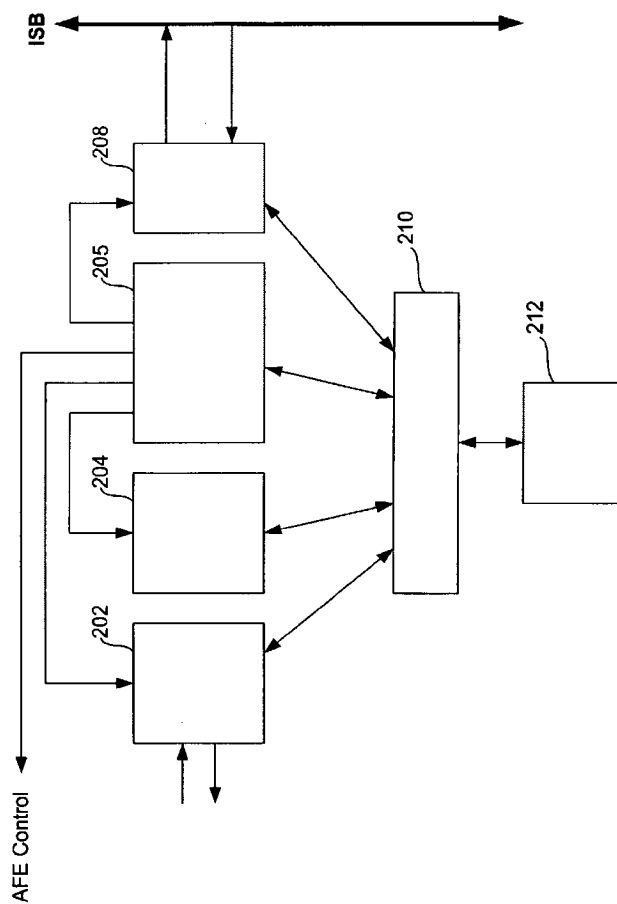


FIG. 2

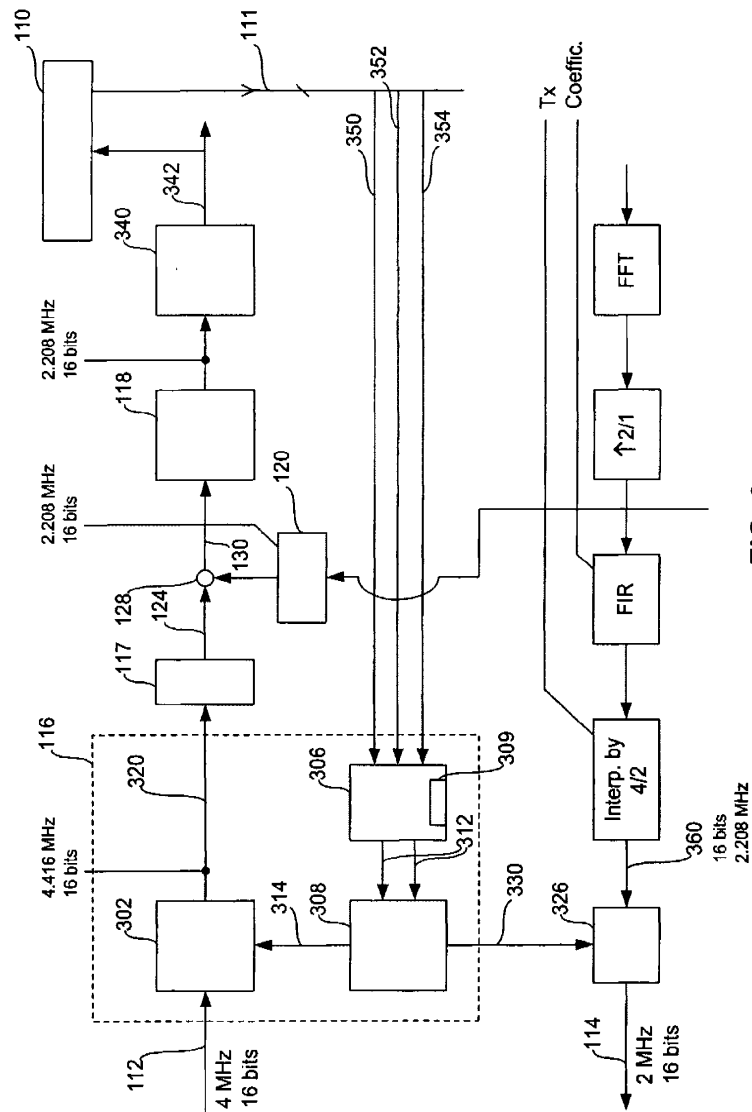


FIG. 3

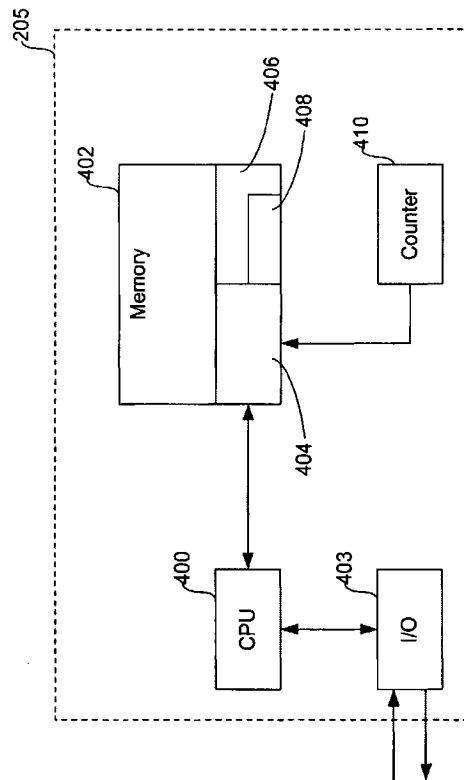


FIG. 4

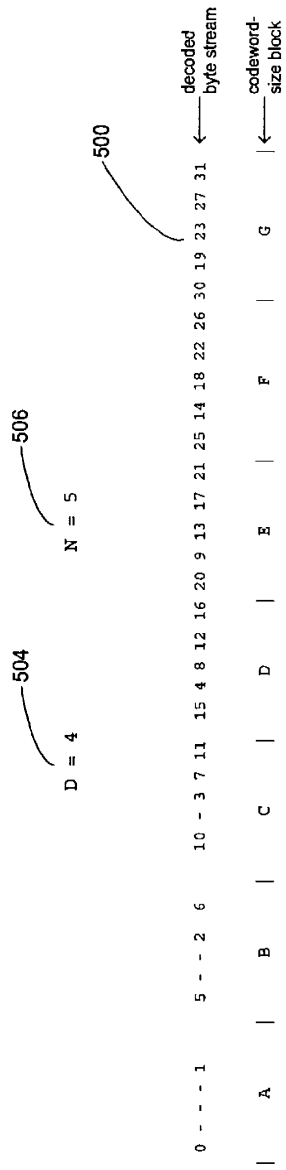


FIG. 5

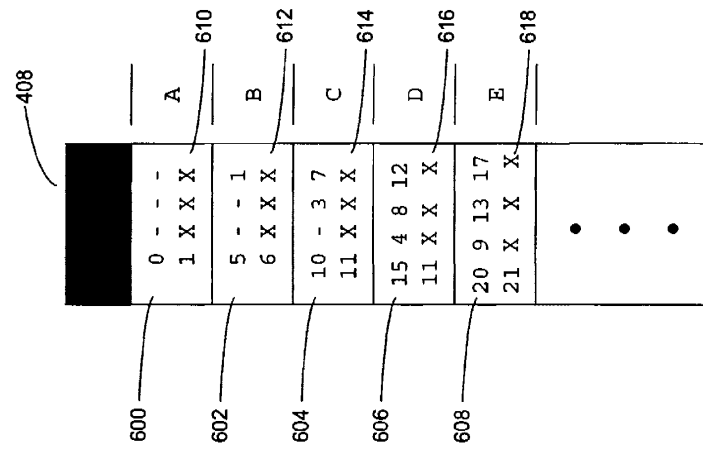


FIG. 6

DMA Parameters: Stride = 4
 Stride2 = 4 + 3 = 7
 Offset = 0
 Offset INC = 4
 Offset Mod = 5

FIG. 7

DMA Address Sequence:

<u>Step</u>	<u>Offset</u>	<u>Address</u>
0	0	A
1	4	A+4
2	3	A+11
3	2	A+18
4	1	A+25

FIG. 8

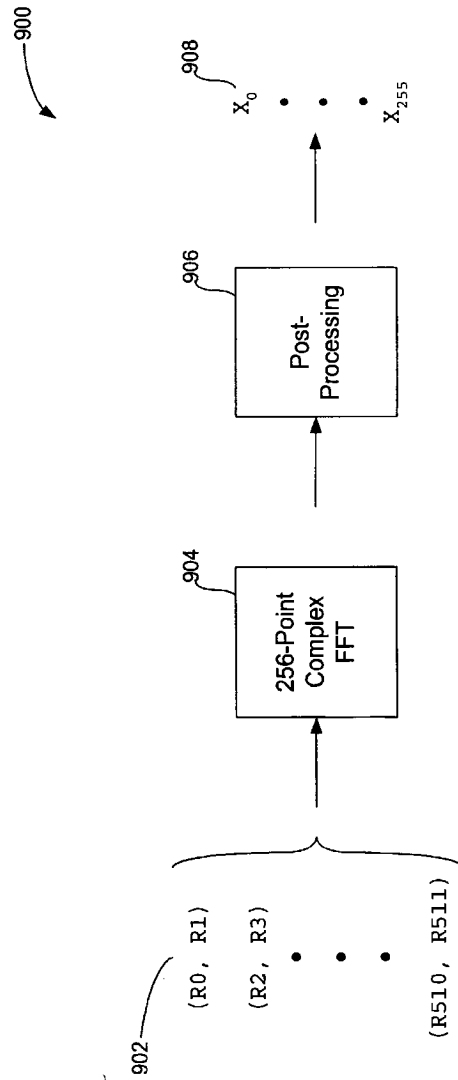


FIG. 9
(conventional)

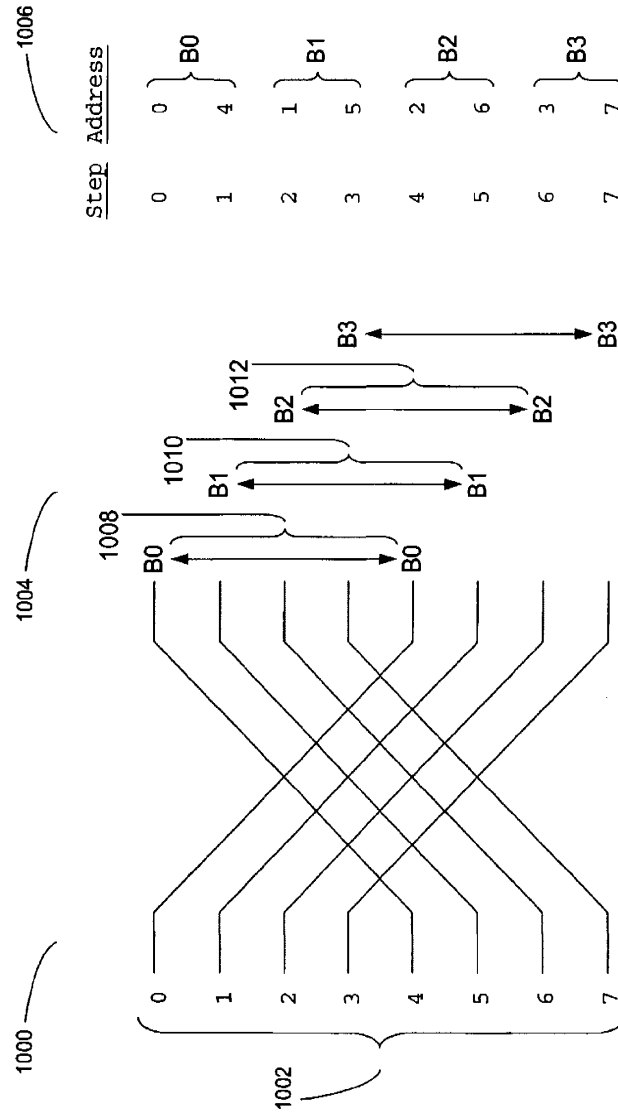


FIG. 10
(conventional)

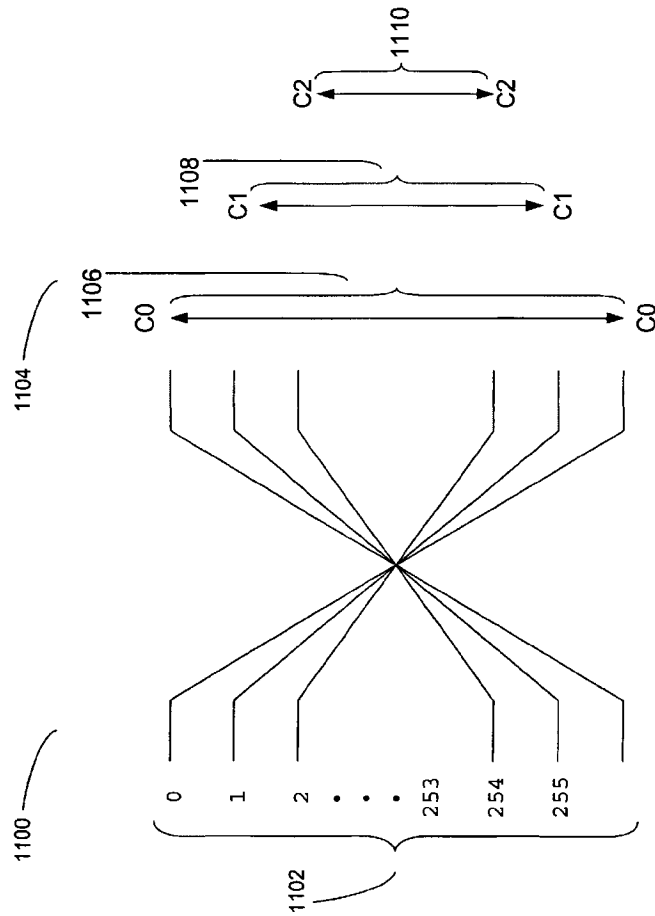
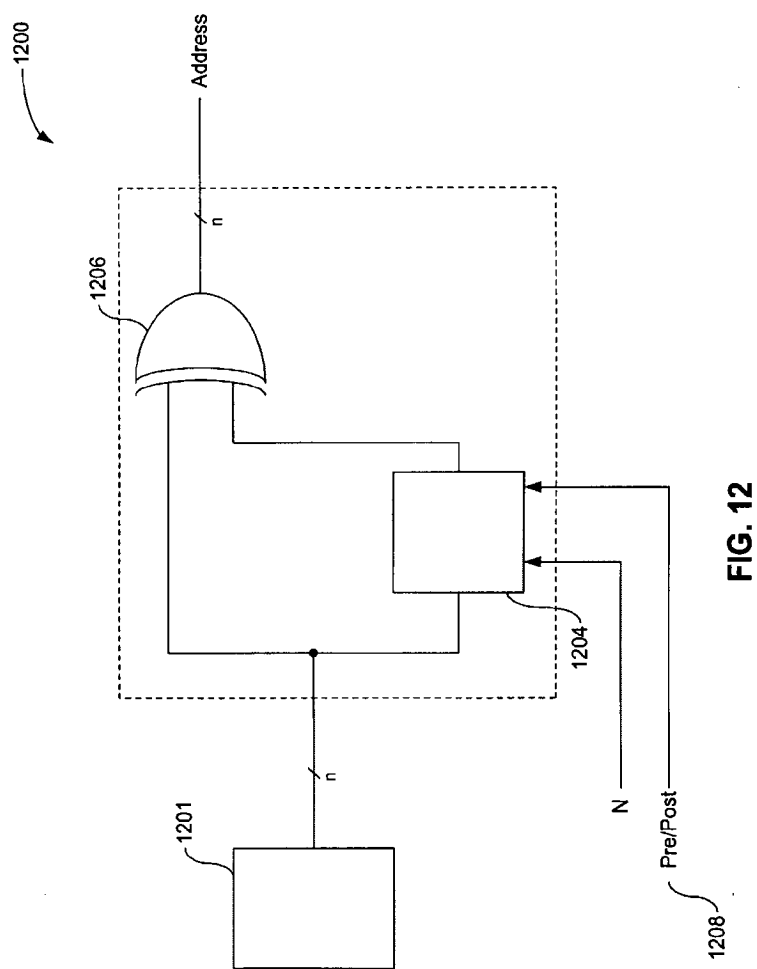


FIG. 11
(conventional)



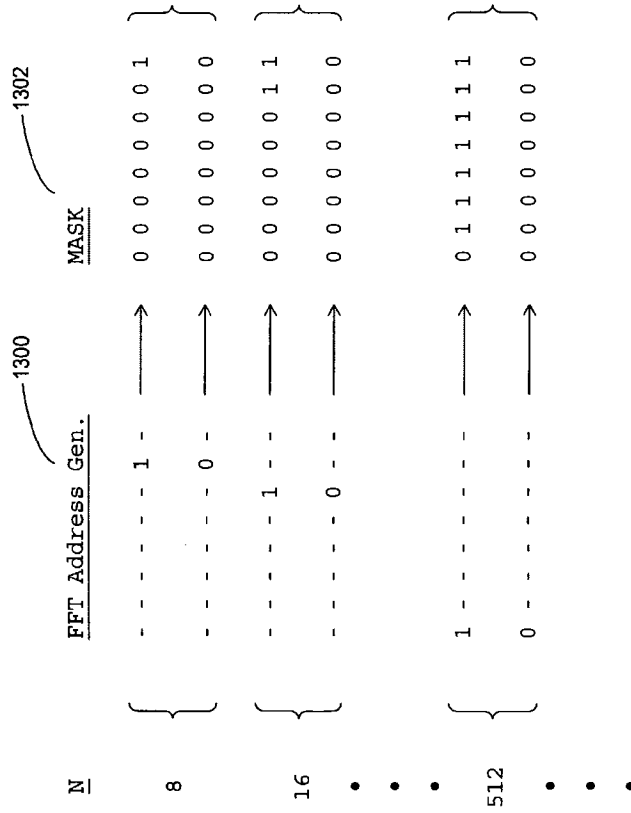


FIG. 13

STEP	1402		1404
	<u>FFT Address Gen.</u>	<u>Conditionally Inverted Address</u>	
2	1	1	
3	128	255	
4	2	2	
5	127	254	
6	3	3	
7	130	253	
•			
•			
•			
254	127	127	
255	254	129	

FIG. 14

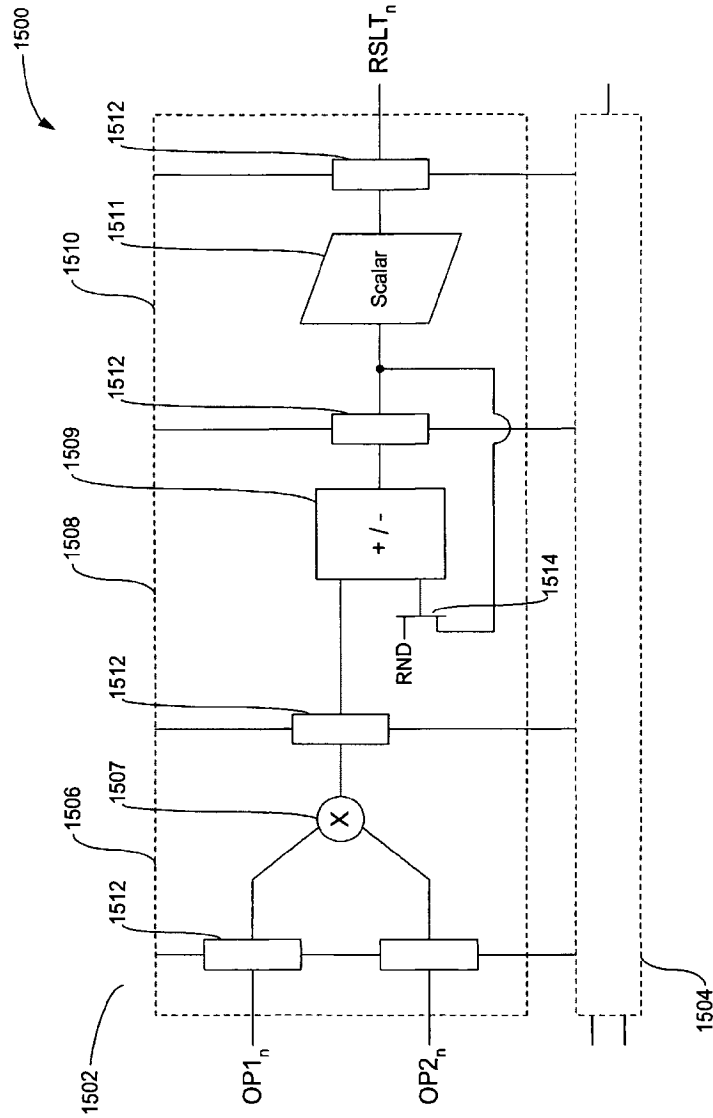


FIG. 15
(conventional)

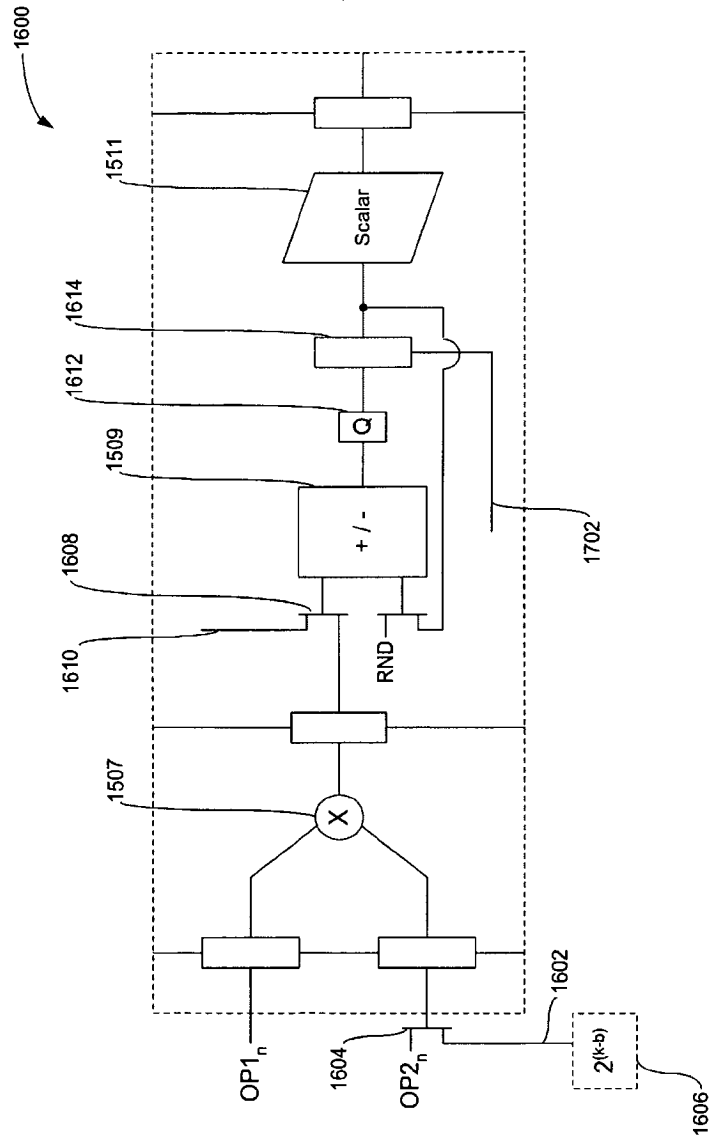


FIG. 16

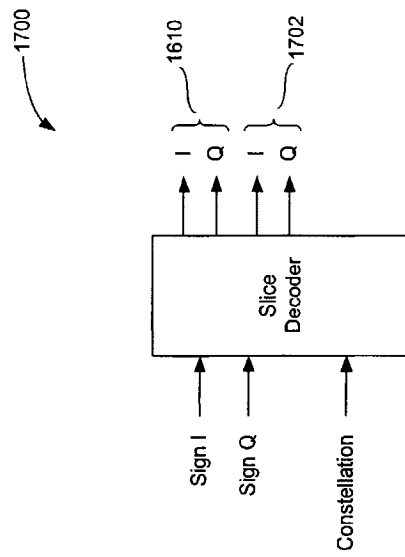
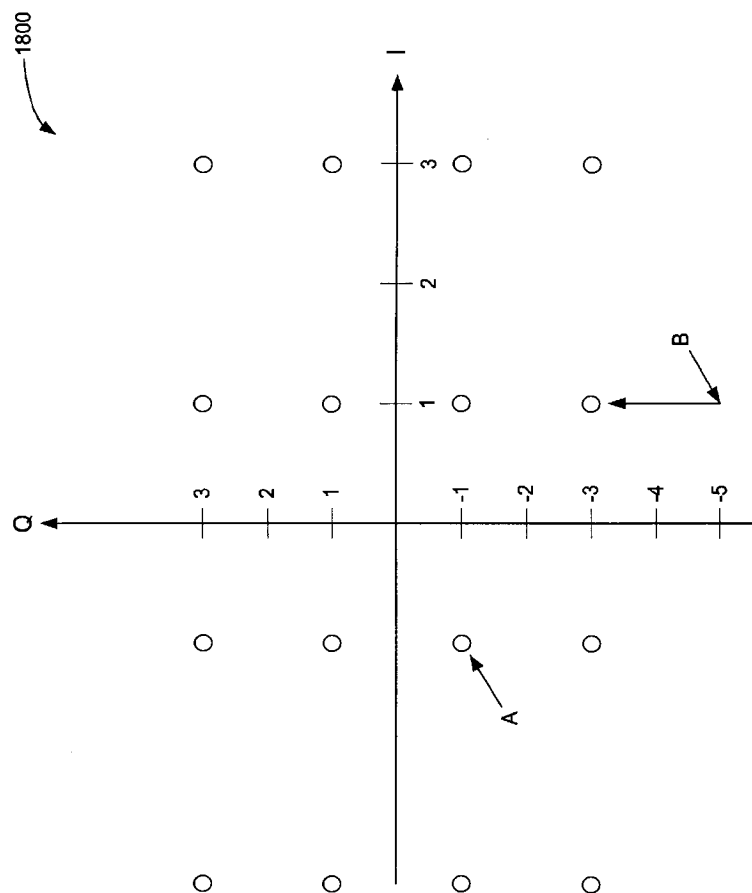


FIG. 17



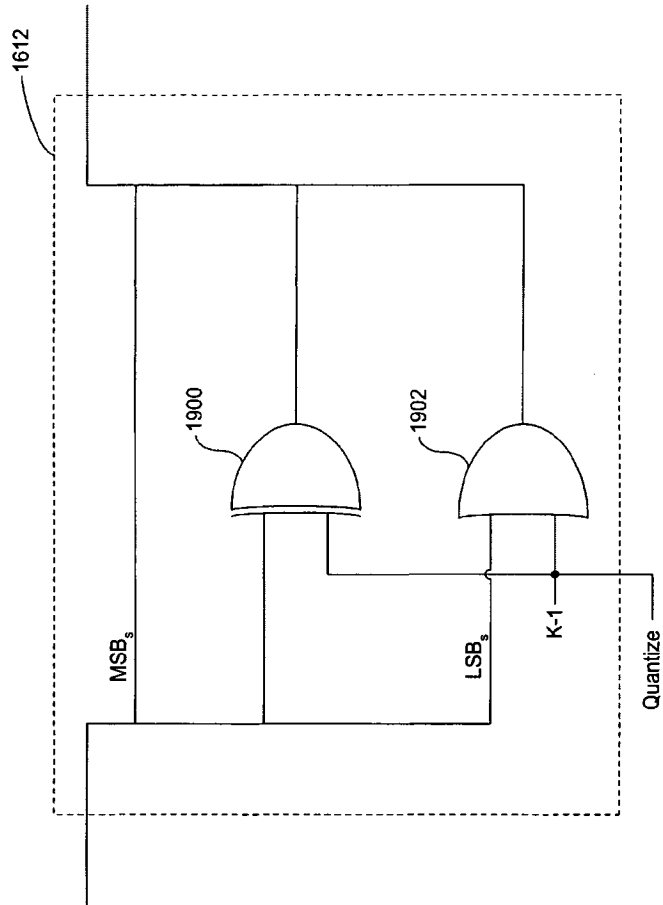


FIG. 19

		<u>Cycle</u>	<u>Quantize</u>	<u>I Limit</u>	<u>I Condition</u>	<u>Q Limit</u>	<u>Q Condition</u>	<u>Acc I</u>	<u>Acc Q</u>
'A'	1	Yes	-	-	-	-	-	-1	-1
	2	No	-3	<	<	-3	<	-1	-1
'B'	1	Yes	-	-	-	-	-	-1	-5
	2	No	3	≥	≥	-3	<	-1	-3

FIG. 20

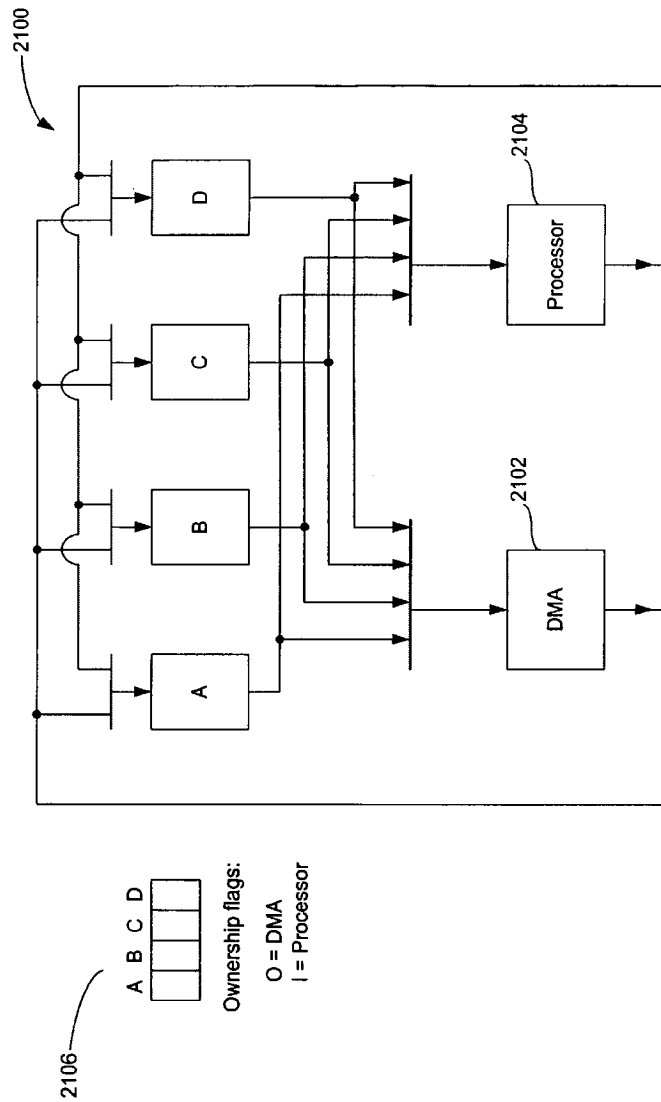


FIG. 21

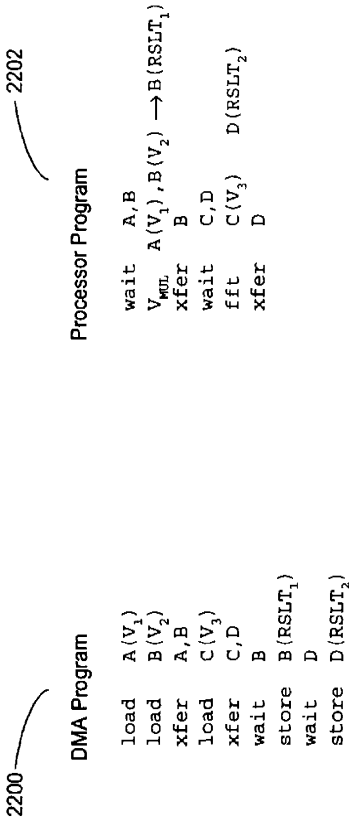


FIG. 22

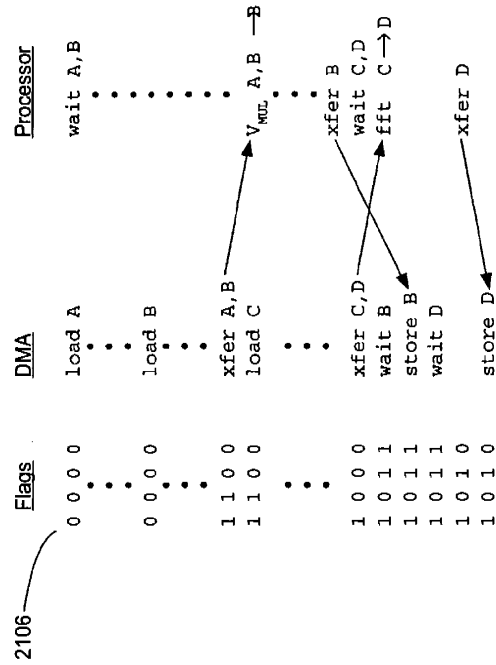


FIG. 23

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- (74) Agent: VICK, Jason, H.; Miles & Stockbridge P.C., 1751 Pinnacle Dr., Suite 500, McLean, VA 22102 (US).

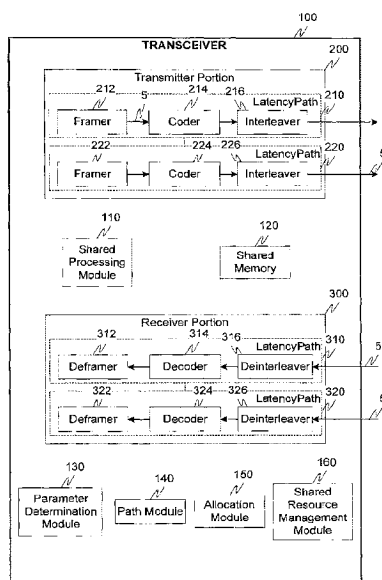
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Published:
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{Continued on next page}

(54) Title: RESOURCE SHARING IN A TELECOMMUNICATIONS ENVIRONMENT



(57) Abstract: A transceiver is designed to share memory and processing power amongst a plurality of transmitter and/or receiver latency paths, in a communications transceiver that carries or supports multiple applications. For example, the transmitter and/or receiver latency paths of the transceiver can share an interleaver/deinterleaver memory. This allocation can be done based on the data rate, latency, BER, impulse noise protection requirements of the application, data or information being transported over each latency path, or in general any parameter associated with the communications system.

WO 2006/044227 A1



For two-letter codes and other abbreviations, refer to the "Guidance Notes on Codes and Abbreviations" appearing at the beginning of each regular issue of the PCT Gazette.

RESOURCE SHARING IN A TELECOMMUNICATIONS ENVIRONMENTRELATED APPLICATION DATA

[0001] This application claims the benefit of and priority under 35 U.S.C. § 119(e) to U.S. Patent Application No. 60/618,269, filed October 12, 2004, entitled “Sharing Memory and Processing Resources in DSL Systems,” which is incorporated herein by reference in its entirety.

BACKGROUNDField of the Invention

[0002] This invention generally relates to communication systems. More specifically, an exemplary embodiment of this invention relates to memory sharing in communication systems. Another exemplary embodiment relates to processing or coding resource sharing in a communication system.

Description of Related Art

[0003] U.S. Patent Nos. 6,775,320 and 6,778,589, which are both incorporated herein by reference in their entirety, describe DSL systems supporting multiple applications and multiple framer/coder/interleaver FCI blocks (an FCI block is also referred to as a latency path). DSL systems carry applications that have different transmission requirements with regard to, for example, data rate, latency (delay), bit error rate (BER), and the like. For example, video typically requires a low BER ($<1\text{E-}10$) but can tolerate higher latency (>20 ms). Voice, on the other hand, typically requires a low latency (<1 ms) but can tolerate BER ($>1\text{E-}3$).

[0004] As described in U.S. Patent No. 6,775,320, different applications can use different latency paths in order to satisfy the different application requirements of the communication system. As a result a transceiver must support multiple latency paths in order to support applications such as video, Internet access and voice telephony. When implemented in a transceiver, each of the latency paths will have a framer, coder, and interleaver block with different capabilities that depend on the application requirements.

SUMMARY

[0005] One difficulty with implementing multiple latency paths in a transceiver is the fact that a latency path is a complicated digital circuit that requires a large amount of memory and processing power. An interleaver within a latency path can consume a large amount of memory in order to provide error correcting capability. For example, a typical DSL transceiver will have at least one latency path with approximately 16 kbytes of memory for the interleaver. Likewise, the coding block, for example, a Reed Solomon coder, consumes a large amount of processing power. In general, as the number of latency paths increase, the memory and processing power requirements for a communication system become larger.

[0006] Accordingly, an exemplary aspect of this invention relates to sharing memory between one or more interleavers and/or deinterleavers in a transceiver. More particularly, an exemplary aspect of this invention relates to shared latency path memory in a transceiver.

[0007] Additional aspects of this invention relate to configuring and initializing shared memory in a communication system. More particularly, an exemplary aspect of this invention relates to configuring and initializing interleaver/deinterleaver memory in a communication system.

[0008] Additional aspects of the invention relate to determining the amount of memory that can be allocated to a particular component by a communication system. More specifically, an exemplary aspect of the invention relates to determining the maximum amount of shared memory that can be allocated to one or more interleaves or deinterleavers.

[0009] According to another exemplary aspect of the invention, processing power is shared between a number of transceiver modules. More specifically, and in accordance with an exemplary embodiment of the invention, a coding module is shared between one or more coders and/or decoders.

[0010] Another exemplary embodiment of the invention relates to transitioning from a fixed memory configuration to a shared memory configuration during one or more of initialization and SHOWTIME (user data transmission).

[0011] An additional exemplary aspect of the invention relates to dynamically updating one or more of shared memory and processing resources based on changing communication conditions.

[0012] An additional exemplary aspect of the invention relates to updating one or more of shared memory and processing resources based on an updated communication parameter.

[0013] An additional exemplary aspect of the invention relates to updating the allocation of one or more of shared memory and processing resources based on an updated communication parameter(s).

[0014] Additional aspects of the invention relate to exchanging shared resource allocations between transceivers.

[0015] Additional exemplary aspects relate to a method of allocating shared memory in a transceiver comprising allocating the shared memory to a plurality of modules, wherein each of the plurality of modules comprise at least one interleaver, at least one deinterleaver or a combination thereof.

[0016] Still further aspects relate to the above method wherein the plurality of modules comprise interleavers.

[0017] Still further aspects relate to the above method wherein the plurality of modules comprise deinterleavers.

[0018] Still further aspects relate to the above method wherein the plurality of modules comprise at least one interleaver and at least one deinterleaver.

[0019] Additional exemplary aspects relate to a transceiver comprising a plurality of modules each including at least one interleaver, at least one deinterleaver or a

combination thereof and a shared memory designed to be allocated to a plurality of the modules.

[0020] Still further aspects relate to the above transceiver wherein the plurality of modules comprise interleavers.

[0021] Still further aspects relate to the above transceiver wherein the plurality of modules comprise deinterleavers.

[0022] Still further aspects relate to the above transceiver wherein the plurality of modules comprise at least one interleaver and at least one deinterleaver.

[0023] These and other features and advantages of this invention are described in, or are apparent from, the following description of the embodiments.

BRIEF DESCRIPTION OF THE DRAWINGS

[0024] The embodiments of the invention will be described in detail, with reference to the following figures, wherein:

[0025] Fig. 1 is a functional block diagram illustrating an exemplary transceiver according to this invention;

[0026] Fig. 2 is a flowchart outlining an exemplary method of sharing resources according to this invention;

[0027] Fig. 3 is a flowchart outlining an exemplary method of determining a maximum amount of shared memory according to this invention; and

[0028] Fig. 4 is a flowchart outlining an exemplary resource sharing methodology according to this invention.

DETAILED DESCRIPTION

[0029] The exemplary embodiments of this invention will be described in relation to sharing resources in a wired and/or wireless communications environment. However, it should be appreciated, that in general, the systems and methods of this invention will work equally well for any type of communication system in any environment.

[0030] The exemplary systems and methods of this invention will also be described in relation to multicarrier modems, such as DSL modems and VDSL modems, and associated communication hardware, software and communication channels. However, to avoid unnecessarily obscuring the present invention, the following description omits well-known structures and devices that may be shown in block diagram form or otherwise summarized.

[0031] For purposes of explanation, numerous details are set forth in order to provide a thorough understanding of the present invention. It should be appreciated however that the present invention may be practiced in a variety of ways beyond the specific details set forth herein.

[0032] Furthermore, while the exemplary embodiments illustrated herein show the various components of the system collocated, it is to be appreciated that the various components of the system can be located at distant portions of a distributed

network, such as a telecommunications network and/or the Internet, or within a dedicated secure, unsecured and/or encrypted system. Thus, it should be appreciated that the components of the system can be combined into one or more devices, such as a modem, or collocated on a particular node of a distributed network, such as a telecommunications network. As will be appreciated from the following description, and for reasons of computational efficiency, the components of the system can be arranged at any location within a distributed network without affecting the operation of the system. For example, the various components can be located in a Central Office modem (CO, ATU-C, VTU-O), a Customer Premises modem (CPE, ATU-R, VTU-R), a DSL management device, or some combination thereof. Similarly, one or more functional portions of the system could be distributed between a modem and an associated computing device.

[0033] Furthermore, it should be appreciated that the various links, including communications channel 5, connecting the elements can be wired or wireless links, or any combination thereof, or any other known or later developed element(s) that is capable of supplying and/or communicating data to and from the connected elements. The term module as used herein can refer to any known or later developed hardware, software, firmware, or combination thereof that is capable of performing the functionality associated with that element. The terms determine, calculate and compute, and variations thereof, as used herein are used interchangeably and include any type of methodology, process, mathematical operation or technique. FCI block and latency path are used interchangeably herein as well as transmitting modem and transmitting transceiver. Receiving modem and receiving transceiver are also used

interchangeably.

[0034] Fig. 1 illustrates an exemplary embodiment of a transceiver 100 that utilizes shared resources. It should be appreciated that numerous functional components of the transceiver have been omitted for clarity. However, the transceiver 100 can also include the standard components found in typical communications device(s) in which the technology of the subject invention is implemented into.

[0035] According to an exemplary embodiment of the invention, memory and processing power can be shared among a plurality of transmitter and/or receiver latency paths, in a communications transceiver that carries or supports multiple applications. For example, the transmitter and/or receiver latency paths of the transceiver can share an interleaver/deinterleaver memory and the shared memory can be allocated to the interleaver and/or deinterleaver of each latency path. This allocation can be done based on the data rate, latency, BER, impulse noise protection requirements of the application, data or information being transported over each latency path, or in general any parameter associated with the communications system.

[0036] Likewise, for example, the transmitter and/or receiver latency paths can share a Reed-Solomon coder/decoder processing module and the processing power of this module can be allocated to each encoder and/or decoder. This allocation can be done based on the data rate/latency, BER, impulse noise protection requirements of the application data or information being transported over each latency path, or in general based on any parameter associated with the communication system.

[0037] In accordance with an exemplary operational embodiment, a first transceiver and a second transceiver transmit to one another messages during, for example, initialization which contain information on the total and/or shared memory capabilities of each transceiver and optionally information about the one or more latency paths. This information can be transmitted prior to determining how to configure the latency paths to support the application requirements. Based on this information, one of the modems can select an FCI configuration parameter(s) that meets the transmission requirements of each application being transported over each latency paths. While an exemplary of the embodiment of the invention will be described in relation to the operation of the invention and characteristics thereof being established during initialization, it should be appreciated that the sharing of resources can be modified and messages transmitted between a two transceivers at any time during initialization and/or user data transmission, i.e., SHOWTIME.

[0038] Fig. 1 illustrates an exemplary embodiment of a transceiver 100. The transceiver 100 includes a transmitter portion 200 and a receiver portion 300. The transmitter portion 200 includes one or more latency paths 210, 220, ... Similarly, the receiver portion 300 includes one or more latency paths 310, 320, ... Each of the latency paths in the transmitter portion 200 includes a framer, coder, and interleaver designated as 212, 214, 216 and 222, 224 and 226, respectively. Each of the latency paths in the receiver portion includes a deframer, decoder, and deinterleaver designated as 312, 314, 316 and 322, 324, and 326, respectively. The transceiver 100 further includes a shared processing module 110, a shared memory 120, a parameter

determination module 130, a path module 140, an allocation module 150, and a shared resource management module 160, all interconnected by one or more links (not shown).

[0039] In this exemplary embodiment, the transceiver 100 is illustrated with four total transmitter portion and receiver portion latency paths, i.e., 210, 220, 310, and 320. The shared memory 120 is shared amongst the two transmitter portion interleavers 216 and 226 and two receiver portion deinterleavers 316 and 326. The shared processing module 110, such as a shared coding module, is shared between the two transmitter portion coders 214 and 224 and the two receiver portion decoders 314 and 324.

[0040] While the exemplary embodiment of the invention will be described in relation to a transceiver having a number of transmitter portion latency paths and receiver portion latency paths, it should be appreciated that this invention can be applied to any transceiver having any number of latency paths. Moreover, it should be appreciated that the sharing of resources can be allocated such that one or more of the transmitter portion latency paths are sharing a shared resource, one or more of the receiver portion latency paths are sharing a shared resource, or a portion of the transmitter portion latency paths and a portion of the receiver portion latency paths are sharing shared resources. Moreover, any one or more of the latency paths, or portions thereof, could also be assigned to a fixed resource while, for example, another portion of the latency path(s) assigned to a shared resource. For example, in latency path 210, the interleaver 216 could be allocated a portion of the shared

memory 120, while the coder 214 could be allocated to a dedicated processing module, vice versa, or the like.

[0041] In accordance with the exemplary embodiment, a plurality of transmitter portion or receiver portion latency paths share an interleaver/deinterleaver memory, such as shared memory 120, and a coding module, such as shared processing module 110. For example, the interleaver/deinterleaver memory can be allocated to different interleavers and/or deinterleavers. This allocation can be based on parameters associated with the communication systems such as data rate, latency, BER, impulse noise protection, and the like, of the applications being transported. Similarly, a coding module, which can be a portion of the shared processing module 110, can be shared between any one or more of the latency paths. This sharing can be based on requirements such as data rate, latency, BER, impulse noise protection, and the like, of the applications being transported.

[0042] For example, an exemplary transceiver could comprise a shared interleaver/deinterleaver memory and could be designed to allocate a first portion of the shared memory 120 to an interleaver, such as interleaver 216 in the transmitter portion of the transceiver and allocate a second portion of the shared memory 120 to a deinterleaver, such as 316, in the receiver portion of the transceiver.

[0043] Alternatively, for example, an exemplary transceiver can comprise a shared interleaver/deinterleaver memory, such as shared memory 120, and be designed to allocate a first portion of shared memory 120 to a first interleaver, e.g.,

216, in the transmitter portion of the transceiver and allocate a second portion of the shared memory to a second interleaver, e.g., 226, in the transmitter portion of the transceiver.

[0044] Alternatively, for example, an exemplary transceiver can comprise a shared interleaver/deinterleaver memory and be designed to allocate a first portion of the shared memory 120 to a first deinterleaver, e.g., 316, in the receiver portion of the transceiver and allocate a second portion of the shared memory to a second deinterleaver, e.g., 326, in the receiver portion of the transceiver. Regardless of the configuration, in general any interleaver or deinterleaver, or grouping thereof, be it in a transmitter portion or receiver portion of the transceiver, can be associated with a portion of the shared memory 120.

[0045] Establishment, configuration and usage of shared resources is performed in the following exemplary manner. First, and in cooperation with the path module 140, the number of transmitter and receiver latency paths (N) is determined. The parameter determination module 130 then analyses one or more parameters such as data rate, transmitter data rate, receiver data rate, impulse noise protection, bit error rate, latency, or the like. Based on one or more of these parameters, the allocation module 150 allocates a portion of the shared memory 120 to one or more of the interleaver and/or deinterleavers, or groupings thereof. This process continues until the memory allocation has been determined and assigned to each of the N latency paths.

[0046] Having determined the memory allocation for each of the latency paths, and in conjunction with the shared resource management 160, the transceiver 100 transmits to a second transceiver one or more of the number of latency paths (N), the maximum interleaver memory for any one or more of the latency paths and/or the maximum total and/or shared memory for all of the latency paths.

[0047] Three examples of sharing interleaver/deinterleaver memory and coding processing in a transceiver are described below. The latency paths in these examples can be in the transmitter portion of the transceiver or the receiver portion of the transceiver.

[0048] Example #1

A first transmitter portion or receiver portion latency path may carry data from a video application, which needs a very low BER but can tolerate higher latency. In this case, the video will be transported using an latency path that has a large amount of interleaving/deinterleaving and coding (also known as Forward Error Correction (FEC) coding). For example, the latency path may be configured with Reed-Solomon coding using a codeword size of 255 bytes ($N=255$) with 16 checkbytes ($R=16$) and interleaving/deinterleaving using an interleaver depth of 64 ($D=64$). This latency path will require $N \cdot D = 16 \cdot 255 = 16\text{Kbytes}$ of interleaver memory at the transmitter (or de-interleaver memory at the receiver). This latency path will be able to correct a burst of errors that is less than 512 bytes in duration.

[0049] A second transmitter portion or receiver portion latency path may carry an

internet access application that requires a medium BER and a medium amount of latency. In this case, the internet access application will be transported using a latency path that has a medium amount of interleaving and coding. For example, the latency path may be configured with Reed-Solomon coding using a codeword size of 128 bytes ($N=128$) with 8 checkbytes ($R=8$) and interleaving using an interleaver depth of 16 ($D=32$). This latency path will require $N*D=128*32=4\text{Kbytes}$ of interleaver memory and the same amount of deinterleaver memory. This latency path will be able to correct a burst of errors that is less than 128 bytes in duration.

[0050] A third transmitter portion or receiver portion latency path may carry a voice telephony application, which needs a very low latency but can tolerate BER. In this case, the video will be transported using an latency path that has a large amount of interleaving and coding. For example, the third transmitter portion or receiver portion latency path may be configured with no interleaving or coding which will result in the lowest possible latency through the latency path but will provide no error correction capability.

[0051] According to the principles of this invention, a system carrying the three applications described above in Example #1, would have three latency paths that share one memory space containing at least $(16+4)=20\text{ Kbytes}$. The three latency paths also share a common coding block that is able to simultaneously encode (in the transmitter portion) or decode (in a receiver portion) two codewords with $N=255/R=16$ and $N=128/R=8$.

[0052] According to an exemplary embodiment of this invention, the latency paths can be reconfigured at initialization or during data transmission mode (also known as SHOWTIME in ADSL and VDSL transceivers). This would occur if, for example, the applications or application requirements were to change.

[0053] Example #2

If instead of 1 video application, 1 internet application and 1 voice application, there were 3 internet access applications then the transmitter portion and/or receiver portion latency paths would be reconfigured to utilize the shared memory and coding module in a different way. For example, the system could be reconfigured to have 3 transmitter portion or receiver portion latency paths, with each latency path being configured with Reed-Solomon coding using a codeword size of 128 bytes ($N=128$) with 8 checkbytes ($R=8$) and interleaving using an interleaver depth of 16 ($D=32$). Each latency path will require $N*D=128*32=4$ Kbytes of interleaver memory and each block will be able to correct a burst of errors that is less than 128 bytes in duration. Based on the example of carrying the three internet access applications described, the three latency path share one memory space containing at least $3*4=12$ Kbytes. Also the three latency paths share a common coding block that is able to simultaneously encode (on the transmitter side) or decode (on the receiver side) three codewords with $N=128/R=16$, $N=128/R=8$ and $N=128/R=8$.

[0054] Example #3

The system could be configured to carry yet another set of applications. For example, the latency paths could be configured to carry 2 video applications. In this case only

2 transmitter portion or receiver portion latency paths are needed, which means that the third latency path could be simply disabled. Also, assuming that the memory is constrained based on the first example above, then the maximum shared memory for these 2 latency paths is 20 kBytes. In this case, the system could be reconfigured to have 2 latency paths, with each block being configured with Reed-Solomon coding using a codeword size of 200 bytes ($N=200$) with 10 checkbytes ($R=10$) and interleaving/deinterleaving using an interleaver depth of 50 ($D=50$). Each latency path will require $N*D=200*50=10\text{Kbytes}$ of interleaver memory and each block will be able to correct a burst of errors that is less than 250 bytes in duration. This configuration results in 20K of shared memory for both latency paths, which is the same as in the first example. In order to stay within the memory constraints of the latency paths, the error correction capability for each latency path is decreased to 250 bytes from 512 bytes in Example #1.

[0055] Another aspect of this invention is the how FCI configuration information is transmitted between a first modem and a second modem. FCI configuration information will depend on the requirements of the applications being transported over the DSL connection. This information may need to be forwarded during initialization in order to initially configure the DSL connection. This information may also need to be forwarded during SHOWTIME in order to reconfigure the DSL connection based on a change in applications or the application requirements.

[0056] According to one embodiment, a first modem determines the specific FCI configuration parameters, e.g., N , D , R as defined above, needed to meet specific

application requirements, such as latency, burst error correction capability, etc. In order to determine the FCI configuration parameters, the first modem must know what are the capabilities of a second modem. For example, the first modem must know how many latency paths (FCI blocks) the second modem can support. Also the first modem must know the maximum amount of interleaver memory for each transmitter latency path. In addition, since the transmitter latency paths may share a common memory space the first modem must know the total shared memory for all transmitter latency paths. This way the first modem will be able to choose a configuration that can meet application requirements and also meet the transmitter portion latency path capabilities of the second modem.

[0057] For example, using values from examples above, a first transceiver could send a message to a second transceiver during initialization or during SHOWTIME containing the following information:

- Number of supported transmitter and receiver latency paths = 3
- Max Interleaver Memory for latency path #1= 16 Kbytes
- Max Interleaver Memory for latency path #2= 16 Kbytes
- Max Interleaver Memory for latency path #3= 16 Kbytes
- Maximum total/shared memory for all latency paths = 20 kBytes

Based on this information, and the application requirements, the first transceiver would select latency path settings. For example, if the applications are 1 video, 1 internet access and 1 voice application, the first transceiver could configure 3 latency paths as follows:

latency path #1 – Video: N=255, R=16, D=64

latency path #2 – Video: N=128, R=8, D=32

latency path #3 – Video: N=0, R=0, D=1 (no coding or interleaving)

[0058] This would result in a total interleaver memory of 20 kbytes.

[0059] Alternatively, if for example, there are only 2 video applications, the first transceiver could configure 2 latency paths as follows:

latency path #1 – Video: N=200, R=10, D=50

latency path #2 – Video: N=200, R=10, D=50

latency path #3 – Video: N=0, R=0, D=1 (no coding or interleaving)

[0060] This would also result in a total interleaver memory of 20 kbytes.

[0061] Alternatively, the second transceiver can determine the specific FCI configuration parameters, e.g., N, D, R as defined above, needed to meet specific application requirements, such as latency, burst error correction capability, etc. As described above for the first transceiver, in order to determine the FCI configuration parameters, the second transceiver must first know what are the capabilities of the first transceiver. In this case, the first transceiver would send a message to the second transceiver containing the information described above and based on this information and the application requirements the second transceiver would select latency path settings.

[0062] Fig. 2 outlines an exemplary method of allocating shared memory in a transceiver. More specifically, control begins in step S200 and continues to step S210. In step S210, one or more of shared interleaver/deinterleaver memory and/or shared coder/decoder processing resources are allocated to one or more latency paths, in a transceiver. Control then continues to step S220 where the control sequence ends.

[0063] Fig. 3 outlines an exemplary method of exchanging shared resource allocations according to an exemplary embodiment of this invention. In particular, control begins in step S310. In step S310, a maximum amount of shared memory that can be allocated to a specific interleaver or deinterleaver of a plurality of interleavers or deinterleavers in a transceiver is determined. Next, in step S320, the determined maximum amount for one or more of the deinterleavers and/or interleavers is transmitted to another transceiver. Messages containing additional information can also be transmitted to the other transceiver and/or received from the other transceiver. Control then continues to step S330 where the control sequence ends.

[0064] Fig. 4 outlines an exemplary procedure for resource sharing according to an exemplary embodiment of this invention. In particular, control begins in step S400 and continues to step S410. In step S410, the number of latency paths are determined. Then, in step S420, the latency path information (FCI block information) is transmitted to another transceiver. Messages containing additional information can also be transmitted to the other transceiver and/or received from the other transceiver. This information can be used to, for example, assist with the determination of

memory allocation in the transceiver. Moreover, the messages received from the other transceiver could specify what the memory allocation is to be based on, for example, the number of latency paths, memory allocation in the remote transceiver and required applications. Control then continues to step S430.

[0065] In step S430, and for each latency path, the steps in step 440 are performed.

[0066] In step S440, and while monitoring of allocation of resources is being performed, steps 450 and 460 are performed. More specifically, in step S450, one or more parameters associated with the communication system are determined. Then, in step S460, shared resources are allocated based on one or more of the communication parameters. Control then continues to step S470.

[0067] In step S470, the allocation of shared resources is communicated to another transceiver. Next, in step S480, a determination is made as to whether there is a change in communications that would require the adjustment of the shared resource allocation. Examples of changes in communications conditions include a change in applications being transported over the system and/or changes in the channel condition, etc. If adjustments are required, control jumps back to step S410. Otherwise, control jumps to step S490 where the control sequence ends.

[0068] The above-described system can be implemented on wired and/or wireless telecommunications devices, such a modem, a multicarrier modem, a DSL modem, an

ADSL modem, an XDSL modem, a VDSL modem, a linecard, test equipment, a multicarrier transceiver, a wired and/or wireless wide/local area network system, a satellite communication system, a modem equipped with diagnostic capabilities, or the like, or on a separate programmed general purpose computer having a communications device or in conjunction with any of the following communications protocols: CDSL, ADSL2, ADSL2+, VDSL1, VDSL2, HDSL, DSL Lite, IDSL, RADSL, SDSL, UDSL or the like.

[0069] Additionally, the systems, methods and protocols of this invention can be implemented on a special purpose computer, a programmed microprocessor or microcontroller and peripheral integrated circuit element(s), an ASIC or other integrated circuit, a digital signal processor, a hard-wired electronic or logic circuit such as discrete element circuit, a programmable logic device such as PLD, PLA, FPGA, PAL, a modem, a transmitter/receiver, any comparable means, or the like. In general, any device capable of implementing a state machine that is in turn capable of implementing the methodology illustrated herein can be used to implement the various communication methods, protocols and techniques according to this invention.

[0070] Furthermore, the disclosed methods may be readily implemented in software using object or object-oriented software development environments that provide portable source code that can be used on a variety of computer or workstation platforms. Alternatively, the disclosed system may be implemented partially or fully in hardware using standard logic circuits or VLSI design. Whether software or

hardware is used to implement the systems in accordance with this invention is dependent on the speed and/or efficiency requirements of the system, the particular function, and the particular software or hardware systems or microprocessor or microcomputer systems being utilized. The communication systems, methods and protocols illustrated herein can be readily implemented in hardware and/or software using any known or later developed systems or structures, devices and/or software by those of ordinary skill in the applicable art from the functional description provided herein and with a general basic knowledge of the computer and telecommunications arts.

[0071] Moreover, the disclosed methods may be readily implemented in software that can be stored on a storage medium, executed on programmed general-purpose computer with the cooperation of a controller and memory, a special purpose computer, a microprocessor, or the like. In these instances, the systems and methods of this invention can be implemented as program embedded on personal computer such as an applet, JAVA® or CGI script, as a resource residing on a server or computer workstation, as a routine embedded in a dedicated communication system or system component, or the like. The system can also be implemented by physically incorporating the system and/or method into a software and/or hardware system, such as the hardware and software systems of a communications transceiver.

[0072] It is therefore apparent that there has been provided, in accordance with the present invention, systems and methods for sharing resources. While this invention has been described in conjunction with a number of embodiments, it is

evident that many alternatives, modifications and variations would be or are apparent to those of ordinary skill in the applicable arts. Accordingly, it is intended to embrace all such alternatives, modifications, equivalents and variations that are within the spirit and scope of this invention.

Claims:

1. A method for sharing resources in a transceiver comprising:
allocating a first portion of shared memory to a first latency path and
allocating a second portion of the shared memory to a second latency path.
2. The method of claim 1, wherein the first latency path includes an interleaver and the second latency path includes an interleaver.
3. The method of claim 1, wherein the first latency path includes an interleaver and the second latency path includes a deinterleaver.
4. The method of claim 1, wherein the first latency path includes a deinterleaver and the second latency path includes a deinterleaver.
5. The method of claim 1, further comprising transmitting to another transceiver information that is used to determine a maximum amount of shared memory that can be allocated.
6. The method of claim 1, further comprising receiving from another transceiver information that is used to determine a maximum amount of shared memory that can be allocated.
7. The method of claim 1, further comprising allocating a shared processing module to a plurality of coding and/or decoding modules.
8. The method of claim 1, wherein the allocating of at least one portion of the shared memory is based on one or more communication parameters.
9. The method of claim 8, wherein at least one of the communication parameters is a data rate, a latency, an INP value or a bit error rate (BER).

10. A transceiver comprising:
a first portion of shared memory that is allocated to a first latency path;
and
a second portion of the shared memory that is allocated to a second latency path.
11. The transceiver of claim 10, further comprising:
an allocation module designed to allocate the shared memory based on one or more communication parameters.
12. The transceiver of claim 11, wherein at least one of the communication parameters is a data rate, a latency, an INP value or a Bit Error Rate (BER).
13. The transceiver of claim 10, wherein the first latency path includes an interleaver and the second latency path includes an interleaver.
14. The transceiver of claim 10, wherein the first latency path includes an interleaver and the second latency path includes a deinterleaver.
15. The transceiver of claim 10, wherein the first latency path includes a deinterleaver and the second latency path includes a deinterleaver.
16. The transceiver of claim 10, further comprising a shared resource management module designed to determine information that is transmitted to another transceiver, wherein the information is used to determine a maximum amount of shared memory that can be allocated.
17. The transceiver of claim 10, further comprising a shared resource management module designed to utilize information that is received from another transceiver, wherein the information is used to determine a maximum amount of shared memory that can be allocated.

18. The transceiver of claim 10, further comprising a shared processing module designed to provide processing resources to a plurality of coding and/or decoding modules.
19. A system for sharing resources in a transceiver comprising:
means for allocating a first portion of shared memory to a first latency path and means for allocating a second portion of the shared memory to a second latency path.
20. The system of claim 19, wherein the first latency path includes an interleaver and the second latency path includes an interleaver.
21. The system of claim 19, wherein the first latency path includes an interleaver and the second latency path includes a deinterleaver.
22. The system of claim 19, wherein the first latency path includes a deinterleaver and the second latency path includes a deinterleaver.
23. The system of claim 19, further comprising means for transmitting to another transceiver information that is used to determine a maximum amount of shared memory that can be allocated.
24. The system of claim 19, further comprising means for receiving from another transceiver information that is used to determine a maximum amount of shared memory that can be allocated.
25. The system of claim 19, further comprising means for allocating a shared processing module to a plurality of coding and/or decoding modules.
26. The system of claim 19, wherein the allocating of at least one portion

of the shared memory is based on one or more communication parameters.

27. The system of claim 26, wherein at least one of the communication parameters is a data rate, a latency, an INP value or a bit error rate (BER).

28. A protocol for sharing resources in a transceiver comprising:
allocating a first portion of shared memory to a first latency path and
allocating a second portion of the shared memory to a second latency path.

29. The protocol of claim 28, wherein the first latency path includes an interleaver and the second latency path includes an interleaver.

30. The protocol of claim 28, wherein the first latency path includes an interleaver and the second latency path includes a deinterleaver.

31. The protocol of claim 28, wherein the first latency path includes a deinterleaver and the second latency path includes a deinterleaver.

32. The protocol of claim 28, further comprising transmitting to another transceiver information that is used to determine a maximum amount of shared memory that can be allocated.

33. The protocol of claim 28, further comprising receiving from another transceiver information that is used to determine a maximum amount of shared memory that can be allocated.

34. The protocol of claim 28, further comprising allocating a shared processing module to a plurality of coding and/or decoding modules.

35. The protocol of claim 28, wherein the allocating of at least one portion of the shared memory is based on one or more communication parameters.

36. The protocol of claim 35, wherein at least one of the communication parameters is a data rate, a latency, an INP value or a bit error rate (BER).

37. An information storage media having stored thereon information that when executed allows sharing of resources in a transceiver comprising:

information that allocates a first portion of shared memory to a first latency path and information that allocates a second portion of the shared memory to a second latency path.

38. The media of claim 37, wherein the first latency path includes an interleaver and the second latency path includes an interleaver.

39. The media of claim 37, wherein the first latency path includes an interleaver and the second latency path includes a deinterleaver.

40. The media of claim 37, wherein the first latency path includes a deinterleaver and the second latency path includes a deinterleaver.

41. The media of claim 37, further comprising information that transmits to another transceiver information that is used to determine a maximum amount of shared memory that can be allocated.

42. The media of claim 37, further comprising information that receives from another transceiver information that is used to determine a maximum amount of shared memory that can be allocated.

43. The media of claim 37, further comprising information that allocates a shared processing module to a plurality of coding and/or decoding modules.

44. The media of claim 37, wherein the allocating of at least one portion of

the shared memory is based on one or more communication parameters.

45. The media of claim 44, wherein at least one of the communication parameters is a data rate, a latency, an INP value or a bit error rate (BER).

1/3

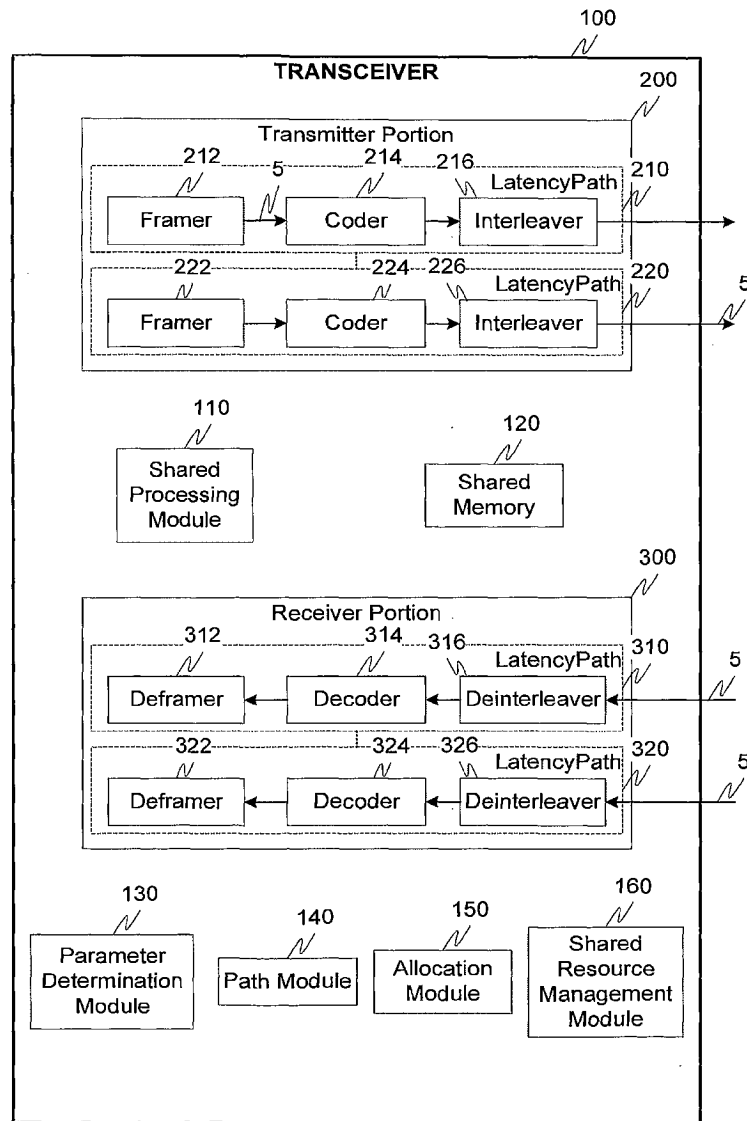


Fig. 1

2/3

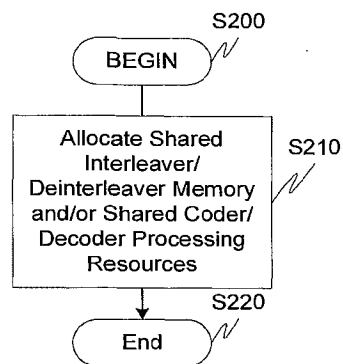


Fig. 2

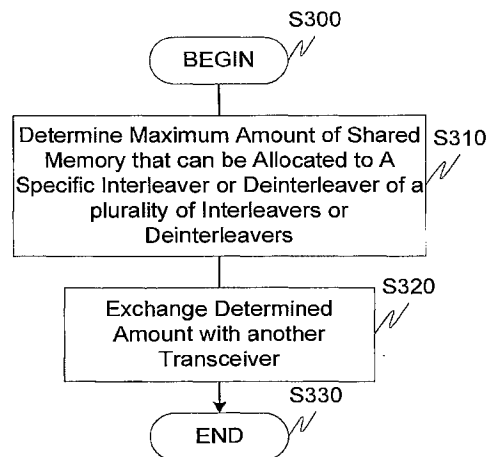


Fig. 3

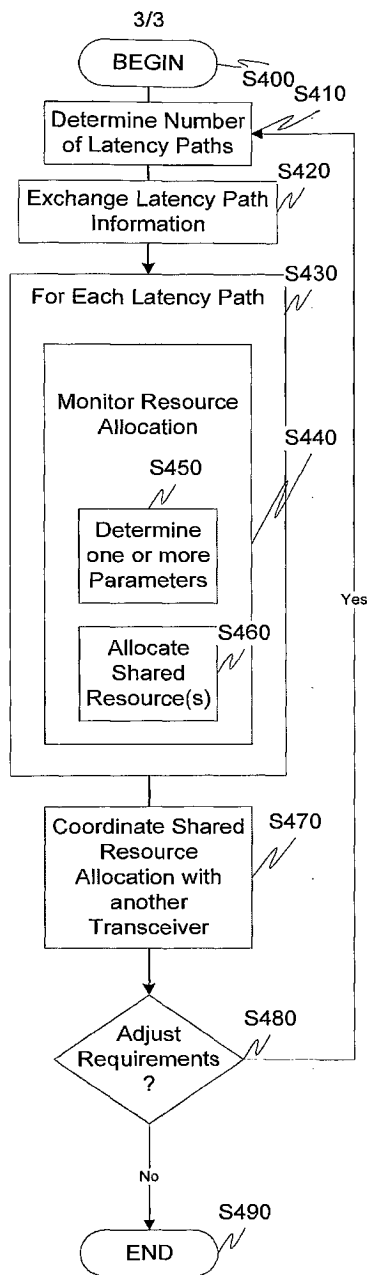


Fig. 4

INTERNATIONAL SEARCH REPORT

International application No
PCT/US2005/036015

A. CLASSIFICATION OF SUBJECT MATTER H04L1/00 H04L27/26		
According to International Patent Classification (IPC) or to both national classification and IPC		
B. FIELDS SEARCHED Minimum documentation searched (classification system followed by classification symbols) H04L		
Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched		
Electronic data base consulted during the International search (name of data base and, where practical, search terms used) EPO-Internal, WPI Data		
C. DOCUMENTS CONSIDERED TO BE RELEVANT		
Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	US 6 707 822 B1 (FADAVI-ARDEKANI JALIL ET AL) 16 March 2004 (2004-03-16) column 1, line 7 - column 2, line 59 column 3, line 5 - column 4, line 21 column 5, line 23 - column 7, line 33 column 8, line 4 - column 9, line 23 figure 2	1-45
A	WO 03/063060 A (BROADCOM CORPORATION) 31 July 2003 (2003-07-31) page 1, line 5 - page 2, line 27 page 17, line 4 - page 18, line 25 figures 1,4 page 7, line 13 - page 9, line 16 ----- -/--	1-45
☒ Further documents are listed in the continuation of Box C. ☒ See patent family annex.		
* Special categories of cited documents : * A* document defining the general state of the art which is not considered to be of particular relevance * E* earlier document but published on or after the international filing date * L* document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified) * O* document referring to an oral disclosure, use, exhibition or other means * P* document published prior to the international filing date but later than the priority date claimed * T* later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention * X* document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone * Y* document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art. * &* document member of the same patent family		
Date of the actual completion of the international search 18 January 2006		Date of mailing of the international search report 08/02/2006
Name and mailing address of the ISA/ European Patent Office, P.B. 5818 Patentlaan 2 NL - 2280 LV Rijswijk Tel. (+31-70) 340-2040, Tx. 31 651 epo nl, Fax: (+31-70) 340-3016		Authorized officer Marzenke, M

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page 1 of 2

INTERNATIONAL SEARCH REPORT

International application No
PCT/US2005/036015

C(Continuation). DOCUMENTS CONSIDERED TO BE RELEVANT		
Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
A	US 6 337 877 B1 (COLE TERRY L ET AL) 8 January 2002 (2002-01-08) column 3, line 21 - column 4, line 29 column 7, line 49 - column 8, line 67 figures 3,10	1-45
A	"SunSet xDSL: Prequalification of ADSL Circuits with ATU-C Emulation" 2001, SUNRISE TELECOM INC., APPLICATION SERIES , SAN JOSE, USA , XP002363272 Retrieved from the Internet: URL:http://www.sunrisetelecom.com/technote s/APP-xDSL-8B.pdf> 'retrieved on 2006-01-17! page 3, right-hand column, paragraph 1	1-45

Form PCT/ISA/210 (continuation of second sheet) (April 2005)

page 2 of 2

INTERNATIONAL SEARCH REPORT

Information on patent family members

International application No

PCT/US2005/036015

Patent document cited in search report		Publication date	Patent family member(s)	Publication date
US 6707822	B1	16-03-2004	NONE	
WO 03063060	A	31-07-2003	EP 1476978 A2	17-11-2004
US 6337877	B1	08-01-2002	EP 1125408 A1	22-08-2001
			WO 0013387 A1	09-03-2000

Form PCT/ISA/210 (patent family annex) (April 2005)

INTERNATIONAL SEARCH REPORT

International application No
PCT/US2005/036015

A. CLASSIFICATION OF SUBJECT MATTER H04L1/00 H04L27/26		
According to International Patent Classification (IPC) or to both national classification and IPC		
B. FIELDS SEARCHED		
Minimum documentation searched (classification system followed by classification symbols) H04L		
Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched		
Electronic data base consulted during the international search (name of data base and, where practical, search terms used) EPO-Internal, WPI Data		
C. DOCUMENTS CONSIDERED TO BE RELEVANT		
Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	US 6 707 822 B1 (FADAVI-ARDEKANI JALIL ET AL) 16 March 2004 (2004-03-16) column 1, line 7 - column 2, line 59 column 3, line 5 - column 4, line 21 column 5, line 23 - column 7, line 33 column 8, line 4 - column 9, line 23 figure 2	1-45
A	WO 03/063060 A (BROADCOM CORPORATION) 31 July 2003 (2003-07-31) page 1, line 5 - page 2, line 27 page 17, line 4 - page 18, line 25 figures 1,4 page 7, line 13 - page 9, line 16 ----- -/--	1-45
☒ Further documents are listed in the continuation of Box C. ☒ See patent family annex.		
* Special categories of cited documents : *A* document defining the general state of the art which is not considered to be of particular relevance *E* earlier document but published on or after the international filing date *L* document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified) *O* document referring to an oral disclosure, use, exhibition or other means *P* document published prior to the international filing date but later than the priority date claimed *T* later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention *X* document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone *Y* document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art *Z* document member of the same patent family		
Date of the actual completion of the international search 18 January 2006		Date of mailing of the international search report 08/02/2006
Name and mailing address of the ISA/ European Patent Office, P.B. 5818 Patentlaan 2 NL - 2280 HV Rijswijk Tel: (+31-70) 340-2040, Tx. 31 651 epo nl, Fax: (+31-70) 340-3076		Authorized officer Marzenke, M

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page 1 of 2

INTERNATIONAL SEARCH REPORT

International application No
PCT/US2005/036015

C(Continuation). DOCUMENTS CONSIDERED TO BE RELEVANT		
Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
A	US 6 337 877 B1 (COLE TERRY L ET AL) 8 January 2002 (2002-01-08) column 3, line 21 - column 4, line 29 column 7, line 49 - column 8, line 67 figures 3,10	1-45
A	"SunSet xDSL: Prequalification of ADSL Circuits with ATU-C Emulation" 2001, SUNRISE TELECOM INC., APPLICATION SERIES, SAN JOSE, USA, XP002363272 Retrieved from the Internet: URL:http://www.sunrisetelecom.com/technote s/APP-xDSL-8B.pdf> 'retrieved on 2006-01-17! page 3, right-hand column, paragraph 1	1-45

Form PCT/ISA/210 (continuation of second sheet) (April 2005)

page 2 of 2

INTERNATIONAL SEARCH REPORT

Information on patent family members

International application No

PCT/US2005/036015

Patent document cited in search report		Publication date	Patent family member(s)	Publication date
US 6707822	B1	16-03-2004	NONE	
WO 03063060	A	31-07-2003	EP 1476978 A2	17-11-2004
US 6337877	B1	08-01-2002	EP 1125408 A1	22-08-2001
			WO 0013387 A1	09-03-2000

Form PCT/ISA/210 (patent family annex) (April 2005)

PATENT COOPERATION TREATY

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INTERNATIONAL SEARCHING AUTHORITY

To:

see form PCT/ISA/220

PCT

WRITTEN OPINION OF THE INTERNATIONAL SEARCHING AUTHORITY (PCT Rule 43bis.1)

Date of mailing
(day/month/year) see form PCT/ISA/210 (second sheet)

Applicant's or agent's file reference
see form PCT/ISA/220

FOR FURTHER ACTION
See paragraph 2 below

International application No
PCT/US2005/036015

International filing date (day/month/year)
11.10.2005

Priority date (day/month/year)
12.10.2004

International Patent Classification (IPC) or both national classification and IPC
H04L1/00, H04L27/26

Applicant
AWARE, INC.

1. This opinion contains indications relating to the following items:

- ☒ Box No. I Basis of the opinion
- ☐ Box No. II Priority
- ☐ Box No. III Non-establishment of opinion with regard to novelty, inventive step and industrial applicability
- ☐ Box No. IV Lack of unity of invention
- ☒ Box No. V Reasoned statement under Rule 43bis 1(a)(i) with regard to novelty, inventive step or industrial applicability; citations and explanations supporting such statement
- ☐ Box No. VI Certain documents cited
- ☒ Box No. VII Certain defects in the international application
- ☒ Box No. VIII Certain observations on the international application

2 FURTHER ACTION

If a demand for international preliminary examination is made, this opinion will usually be considered to be a written opinion of the International Preliminary Examining Authority ("IPEA"). However, this does not apply where the applicant chooses an Authority other than this one to be the IPEA and the chosen IPEA has notified the International Bureau under Rule 66.1bis(b) that written opinions of this International Searching Authority will not be so considered.

If this opinion is, as provided above, considered to be a written opinion of the IPEA, the applicant is invited to submit to the IPEA a written reply together, where appropriate, with amendments, before the expiration of three months from the date of mailing of Form PCT/ISA/220 or before the expiration of 22 months from the priority date, whichever expires later.

For further options, see Form PCT/ISA/220.

3 For further details, see notes to Form PCT/ISA/220

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my
DATE 8-12-06
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Name and mailing address of the ISA.



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D-80298 Munich
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Authorized Officer

Marzenke, M

Telephone No. +49 89 2399-8810



**WRITTEN OPINION OF THE
INTERNATIONAL SEARCHING AUTHORITY**

International application No.
PCT/US2005/036015

Box No. I Basis of the opinion

1. With regard to the **language**, this opinion has been established on the basis of the international application in the language in which it was filed, unless otherwise indicated under this item.
 - ☐ This opinion has been established on the basis of a translation from the original language into the following language , which is the language of a translation furnished for the purposes of international search (under Rules 12.3 and 23.1(b)).
2. With regard to any **nucleotide and/or amino acid sequence** disclosed in the international application and necessary to the claimed invention, this opinion has been established on the basis of:
 - a. type of material:
 - ☐ a sequence listing
 - ☐ table(s) related to the sequence listing
 - b. format of material:
 - ☐ in written format
 - ☐ in computer readable form
 - c. time of filing/furnishing:
 - ☐ contained in the international application as filed.
 - ☐ filed together with the international application in computer readable form.
 - ☐ furnished subsequently to this Authority for the purposes of search.
3. ☐ In addition, in the case that more than one version or copy of a sequence listing and/or table relating thereto has been filed or furnished, the required statements that the information in the subsequent or additional copies is identical to that in the application as filed or does not go beyond the application as filed, as appropriate, were furnished.
4. Additional comments:

**WRITTEN OPINION OF THE
INTERNATIONAL SEARCHING AUTHORITY**

International application No.
PCT/US2005/036015

Box No. V Reasoned statement under Rule 43*bis*.1(a)(i) with regard to novelty, inventive step or industrial applicability; citations and explanations supporting such statement

1. Statement

Novelty (N)	Yes: Claims	5,6,16,17,23,24,32,33,41,42
	No: Claims	1-4, 7-15, 18-22, 25-31, 34-40,43-45
Inventive step (IS)	Yes: Claims	
	No: Claims	5,6,16,17,23,24,32,33,41,42
Industrial applicability (IA)	Yes: Claims	1-45
	No: Claims	

2. Citations and explanations

see separate sheet

Box No. VII Certain defects in the international application

The following defects in the form or contents of the international application have been noted:

see separate sheet

Box No. VIII Certain observations on the international application

The following observations on the clarity of the claims, description, and drawings or on the question whether the claims are fully supported by the description, are made:

see separate sheet

V. Reasoned Statement with regard to novelty, inventive step and industrial applicability; citations and explanations supporting such statement

I

The following documents are referenced for the first time in this written opinion; the numbering will be adhered to in the rest of the procedure:

D1: US-B1-6 707 822

D2: WO 03/063060 A

D3: US-B1-6 337 877

D4: "SunSet xDSL: Prequalification of ADSL Circuits with ATU-C Emulation", 2001, SUNRISE TELECOM INC., APPLICATION SERIES, XP002363272 Retrieved from the Internet: URL: <http://www.sunrisetelecom.com/technotes/APP-xDSL-8B.pdf> [retrieved on 2006-01-17]

II

- 1.1 The present broad formulation of independent method Claim 1 is such that its subject-matter can be read onto prior art Document D1 which discloses according to the wording of Claim 1 (the corresponding features in D1 are given in brackets):

A method for sharing resources (*abstract; column 2, lines 57-59; column 9, lines 10-23*) in a transceiver (*column 5, lines 23-30; fig. 2*), comprising:
allocating a first portion of shared memory (*fig. 2: IDIM RAM 230; column 3, lines 16-20*) to a first latency path (*e.g. to any interleave path for G.lite or standard ADSL, see column 6, line 66 to column 7, line 17*) and allocating a second portion of the shared memory to a second latency path (*column 6, lines 55-62 and column 7, lines 17-30: additional 4K dedicated memory space are allocated to any fast path*).

Consequently, the features of independent Claim 1 are already known from Document D1 and thus the subject-matter of Claim 1 is not novel. Claim 1 therefore does not meet the requirements of Articles 33(1) and (2) PCT.

- 1.2 It should be noted that even if the Applicant were to interpret Claim 1 in such a manner as to enable him to allege that its subject-matter were novel, based on minor differences between the features of this claim and those disclosed in D1, the subject matter of Claim 1 would still not involve an inventive step, Articles 33(1) and (3) of the PCT, with respect to the disclosure of D1 especially as this document discloses the same object and the same type of solution as claimed.
2. The subject-matter of Claims 10, 19, 28 and 37 corresponds in terms of transceiver, system, protocol and storage media features respectively to that of Claim 1. Therefore, the objections raised in the previous paragraphs apply equally to Claims 10, 19, 28 and 37 which do consequently not meet the requirements of Articles 33(1) and (2) PCT for lack of novelty.
3. The dependent claims do not appear at present to contain any feature which in combination with the subject-matter of the independent claim to which the respective dependent claim is appended would result in novel and inventive subject-matter, these additional features being either disclosed or rendered obvious by the above cited documents, or being minor details obvious to a person skilled in the art based on common general knowledge of the art (Article 33(1) PCT). In particular, it is noted:

Claims 2-4, 13-15, 20-22, 29-31, 38-40: Use of interleaving/de-interleaving in two latency paths is known from D1. The latter teaches that depending on the used interleaving depth, several interleaved sessions or paths can be supported using the shared memory (*see column 7, lines 1-5 and 30-33*);

Claims 5, 6, 16, 17, 23, 24, 32, 33, 41, 42: Exchanging various information between two modems for determining resources that are available for a connection to be set up represents general common knowledge for the skilled person in the field of xDSL communications. It is therefore considered to be a straightforward design measure for a skilled person having knowledge of the shared memory transceivers in D1 to specifically exchange information regarding the maximum available interleaver memory size in order to accommodate a plurality of latency paths. D1 clearly teaches the skilled person that the memory size is a critical resource in terms of the number of

sessions/paths that can be supported contemporaneously (see column 7, lines 1-33). It does therefore not go beyond what can generally be expected from the skilled person in the light of D1 to exchange and use information specifying said critical amount of available shared memory;

Claim 7, 18, 25, 34, 43: Allocating a shared FCI module to perform the processing of two coder/decoder modules of two latency paths respectively is known from D1 (*see column 6, lines 11-17; fig. 2: FCI 226 writes encoded data for different latency paths into RAM 230 and reads decoded data for different latency paths from it: column 8, line 62 to column 9, line 3*);

Claims 8, 9, 11, 12, 26, 27, 35, 36, 44, 45: D1 teaches allocating a portion of memory to a path according to its latency (see column 6, lines 17-18: "Interleave and Fast Path"; column 7, lines 5-20: It is implicit to the skilled person from what is expressly said in D1 that the *interleaved* G.lite path requiring 4 Kbytes of memory imposes a higher processing latency than the fast path requiring only 256 bytes; on this point, the Applicant is also referred to D4 for information, see page 3, right-hand column, "Selecting the Path: Fast vs. Interleaved").

VII. Certain defects in the international application

1. To meet the requirements of Rule 6.3(b) PCT the independent claims should be cast in the two-part form, with those features known in combination from the prior art (see document D1) being placed in a preamble (Rule 6.3(b)(i) PCT) and with the remaining features being included in a characterising part (Rule 6.3(b)(ii) PCT).
2. To fulfil the requirements of Rule 5.1(a)(ii) PCT, document D1 should be identified in the description and the relevant background art disclosed therein briefly discussed.
3. The opening part of the description should be brought into conformity with any amended independent claims (Rule 5.1(a)(iii) PCT).
4. Furthermore, following the disclosure of document D1, the statement indicating the

technical problem to be solved by the invention (see page 2, paragraphs [0005] and [0006]), requires revision, which should be effected taking the requirements of Rule 5.1(a)(iii) PCT into account.

5. Reference signs placed in parentheses should be inserted into all the claims to increase their intelligibility (Rule 6.2(b) PCT). This applies to both the preamble and the characterising portion.
6. The reference to the "spirit" of the invention should be deleted (see page 23, last line) (Article 6 PCT and PCT-Guidelines 5.30).
7. The expression "herein incorporated by reference" (see page 1, par. [0001] and [0003]) should be removed from the description (see the PCT-Guidelines, 4.26).
8. The description (see page 7, par. [0033]) refers to "**later** developed hardware, software or firmware". By definition, it is however unclear what this hardware, software and/or firmware will effectively look like in the future. This formulation, implying in general terms that the extent of protection maybe expanded in some vague and not precisely defined way, should be deleted in accordance with Article 6 PCT and the PCT Guidelines 5.30.

The same applies to the formulation "later developed systems or structures, devices and/or software" on page 22, paragraph [0070].

9. The description on page 14, paragraph [0050] describes a third latency path for "a voice telephony application, which needs a very low latency but can tolerate BER".

The next sentence however contradicts the above statement: "In this case, the **video** [not voice ?] will be transported using an latency path that has a **large** amount of interleaving and coding [i.e. resulting in a high latency and thus contradicting the previously mentioned requirements for voice telephony ?]". Subsequently, this is again contradicted by the last sentence in paragraph [0050] stipulating that "**no** interleaving or coding" would be applied to said third latency path, further corroborated by the calculation in the following paragraph [0051] clearly assuming **no** interleaver memory and **no** encoding for the third path.

The second sentence of paragraph [0050] should thus be deleted for clarification.

10. The Applicant should remove the parentheses around the expression "BER" in Claims 9, 12, 27, 36 and 45 as this term does not represent a reference sign in the sense of Rule 6.2(b) PCT (see also the PCT-Guidelines 5.11).

VIII. Certain observations on the international application

The following objections are raised with respect to Article 6 PCT:

1. Independent Claim 28 (and its dependent Claims 29-36) repeat - word by word - the subject-matter already defined in Claim 1 (and its dependent Claims 2-9), thus contravening the requirement of Article 6 PCT that the claims shall be concise.

The generic terms "method" and "protocol" used in Claims 1 and 28 respectively belong to the same category "activity" as defined in the Guidelines 5.12 and can be used interchangeably. In fact, a protocol does not consist of anything more than a number of technical method steps.

The claims need to be recast to include only the minimum necessary number of independent claims in any one category (see Rule 6.1(a) PCT and the PCT-Guidelines, A5.42). In the present case it is considered appropriate to use only one independent claim in the "activity" (method) category.

Claim 28 and its dependent Claims 29-36 should thus be deleted.

2. Independent Claim 37 refers to "information that **when executed allows** sharing of resources in a transceiver, comprising information that allocates ...".

In its present wording, the claimed information is construed to be **suitable**, when executed, to share resources. The sharing of resources is thus not limiting the scope of the claim and the claimed information thus does not produce any technical effect whatsoever in terms of technical method steps being performed as a result of the

information (or program code) being executed.

It is also unclear, where or on which physical entity the information (or program code) is being executed on. Indeed, the claimed information can only bring about a technical effect in conjunction with a physical device on which it is run or executed. Otherwise, it merely represents program code per se.

The same objections apply to dependent Claims 38-45.

Claim 37 should thus be clarified to read: "An information storage medium comprising information which, when executed on a computer, performs the method as defined in any one of Claims 1 to 9." Claims 39-45 should be deleted.

3. The category of *method* Claims 2-4 is unclear as their additional features solely relate to constituent *means* of the latency paths. It is indeed unclear, which steps of the claimed *method* are effectively to be construed from the claimed (de)interleavers.

The same objection applies to Claims 29-31 and 38-40.

4. The abbreviation "INP" as presented in Claims 9, 12, 27, 36 and 45 is not clear from the wording of the claim alone and should be replaced by "impulse noise protection" in the light of the description (see page 11, mid-paragraph [0041]).
5. Claim 7 refers to "allocating a shared processing module to a plurality of coding and/or decoding modules". It is unclear, whether or not and if so, to what extent, these modules are part of the transceiver referred to in Claim 1.

The same lack of clarity arises in Claims 18, 25, 34 and 43.

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PATENT COOPERATION TREATY

PCT/US2005/036015

From the INTERNATIONAL BUREAU

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NOTIFICATION CONCERNING
TRANSMITTAL OF COPY OF INTERNATIONAL
PRELIMINARY REPORT ON PATENTABILITY
(CHAPTER I OF THE PATENT COOPERATION
TREATY)

(PCT Rule 44bis.1(c))

To:

VICK, Jason, H.
Miles & Stockbridge P.C.
1751 Pinnacle Dr.
Suite 500
McLean, VA 22102
ETATS-UNIS D'AMERIQUE

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MAY 04 2007

MILES & STOCKBRIDGE PC
TYSONS CORNER

Date of mailing (day/month/year) 26 April 2007 (26.04.2007)		
Applicant's or agent's file reference T3653-9285WO01		IMPORTANT NOTICE
International application No. PCT/US2005/036015 ✓	International filing date (day/month/year) 11 October 2005 (11.10.2005) ✓	Priority date (day/month/year) 12 October 2004 (12.10.2004) ✓
Applicant AWARE, INC. ✓		
The International Bureau transmits herewith a copy of the international preliminary report on patentability (Chapter I of the Patent Cooperation Treaty)		
The International Bureau of WIPO 34, chemin des Colombettes 1211 Geneva 20, Switzerland		Authorized officer Athina Nickitas-Etienne
Facsimile No. +41 22 338 82 70		e-mail: pt04.pct@wipo.int

Form PCT/IB/326 (January 2004)

PATENT COOPERATION TREATY

PCT

INTERNATIONAL PRELIMINARY REPORT ON PATENTABILITY

(Chapter I of the Patent Cooperation Treaty)

(PCT Rule 44bis)

Applicant's or agent's file reference T3653-9285WO01	FOR FURTHER ACTION See item 4 below	
International application No. PCT/US2005/036015	International filing date (<i>day/month/year</i>) 11 October 2005 (11.10.2005)	Priority date (<i>day/month/year</i>) 12 October 2004 (12.10.2004)
International Patent Classification (8th edition unless older edition indicated) See relevant information in Form PCT/ISA/237		
Applicant AWARE, INC.		

1. This international preliminary report on patentability (Chapter I) is issued by the International Bureau on behalf of the International Searching Authority under Rule 44 <i>bis</i>.1(a). 2. This REPORT consists of a total of 10 sheets, including this cover sheet. In the attached sheets, any reference to the written opinion of the International Searching Authority should be read as a reference to the international preliminary report on patentability (Chapter I) instead.																
3. This report contains indications relating to the following items: <table> <tr> <td>☒ Box No. I</td> <td>Basis of the report</td> </tr> <tr> <td>☐ Box No. II</td> <td>Priority</td> </tr> <tr> <td>☐ Box No. III</td> <td>Non-establishment of opinion with regard to novelty, inventive step and industrial applicability</td> </tr> <tr> <td>☐ Box No. IV</td> <td>Lack of unity of invention</td> </tr> <tr> <td>☒ Box No. V</td> <td>Reasoned statement under Article 35(2) with regard to novelty, inventive step or industrial applicability; citations and explanations supporting such statement</td> </tr> <tr> <td>☐ Box No. VI</td> <td>Certain documents cited</td> </tr> <tr> <td>☒ Box No. VII</td> <td>Certain defects in the international application</td> </tr> <tr> <td>☒ Box No. VIII</td> <td>Certain observations on the international application</td> </tr> </table> 4. The International Bureau will communicate this report to designated Offices in accordance with Rules 44bis.3(c) and 93bis.1 but not, except where the applicant makes an express request under Article 23(2), before the expiration of 30 months from the priority date (Rule 44bis .2).	☒ Box No. I	Basis of the report	☐ Box No. II	Priority	☐ Box No. III	Non-establishment of opinion with regard to novelty, inventive step and industrial applicability	☐ Box No. IV	Lack of unity of invention	☒ Box No. V	Reasoned statement under Article 35(2) with regard to novelty, inventive step or industrial applicability; citations and explanations supporting such statement	☐ Box No. VI	Certain documents cited	☒ Box No. VII	Certain defects in the international application	☒ Box No. VIII	Certain observations on the international application
☒ Box No. I	Basis of the report															
☐ Box No. II	Priority															
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☐ Box No. IV	Lack of unity of invention															
☒ Box No. V	Reasoned statement under Article 35(2) with regard to novelty, inventive step or industrial applicability; citations and explanations supporting such statement															
☐ Box No. VI	Certain documents cited															
☒ Box No. VII	Certain defects in the international application															
☒ Box No. VIII	Certain observations on the international application															

The International Bureau of WIPO 34, chemin des Colombettes 1211 Geneva 20, Switzerland Facsimile No. +41 22 338 82 70	Date of issuance of this report 17 April 2007 (17.04.2007)
	Authorized officer Athina Nickitas-Etienne e-mail: pt04.pct@wipo.int

Form PCT/IB/373 (January 2004)

PATENT COOPERATION TREATY

From the
INTERNATIONAL SEARCHING AUTHORITY

REC'D 07 FEB 2006

PCT

WIPO

PCT

To:

see form PCT/ISA/220

PT04

WRITTEN OPINION OF THE INTERNATIONAL SEARCHING AUTHORITY (PCT Rule 43bis.1)

Date of mailing
(day/month/year) see form PCT/ISA/210 (second sheet)

Applicant's or agent's file reference
see form PCT/ISA/220

FOR FURTHER ACTION
See paragraph 2 below

International application No.
PCT/JS2005/036015

International filing date (day/month/year)
11.10.2005

Priority date (day/month/year)
12.10.2004

International Patent Classification (IPC) or both national classification and IPC
H04L1/00, H04L27/26

Applicant
AWARE, INC.

1. This opinion contains indications relating to the following items:

- ☒ Box No. I Basis of the opinion
- ☐ Box No. II Priority
- ☐ Box No. III Non-establishment of opinion with regard to novelty, inventive step and industrial applicability
- ☐ Box No. IV Lack of unity of invention
- ☒ Box No. V Reasoned statement under Rule 43bis.1(a)(i) with regard to novelty, inventive step or industrial applicability; citations and explanations supporting such statement
- ☐ Box No. VI Certain documents cited
- ☒ Box No. VII Certain defects in the international application
- ☒ Box No. VIII Certain observations on the international application

2. FURTHER ACTION

If a demand for international preliminary examination is made, this opinion will usually be considered to be a written opinion of the International Preliminary Examining Authority ("IPEA"). However, this does not apply where the applicant chooses an Authority other than this one to be the IPEA and the chosen IPEA has notified the International Bureau under Rule 66.1bis(b) that written opinions of this International Searching Authority will not be so considered.

If this opinion is, as provided above, considered to be a written opinion of the IPEA, the applicant is invited to submit to the IPEA a written reply together, where appropriate, with amendments, before the expiration of three months from the date of mailing of Form PCT/ISA/220 or before the expiration of 22 months from the priority date, whichever expires later.

For further options, see Form PCT/ISA/220.

3. For further details, see notes to Form PCT/ISA/220.

Name and mailing address of the ISA:



European Patent Office
D-80298 Munich
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Form (PCT/ISA/237) (Cover Sheet) (January 2004)

**WRITTEN OPINION OF THE
INTERNATIONAL SEARCHING AUTHORITY**

International application No.
PCT/US2005/036015

Box No. I Basis of the opinion

1. With regard to the **language**, this opinion has been established on the basis of the international application in the language in which it was filed, unless otherwise indicated under this item.
 - ☐ This opinion has been established on the basis of a translation from the original language into the following language , which is the language of a translation furnished for the purposes of international search (under Rules 12.3 and 23.1(b)).
2. With regard to any **nucleotide and/or amino acid sequence** disclosed in the international application and necessary to the claimed invention, this opinion has been established on the basis of:
 - a. type of material:
 - ☐ a sequence listing
 - ☐ table(s) related to the sequence listing
 - b. format of material:
 - ☐ in written format
 - ☐ in computer readable form
 - c. time of filing/furnishing:
 - ☐ contained in the international application as filed.
 - ☐ filed together with the international application in computer readable form.
 - ☐ furnished subsequently to this Authority for the purposes of search.
3. ☐ In addition, in the case that more than one version or copy of a sequence listing and/or table relating thereto has been filed or furnished, the required statements that the information in the subsequent or additional copies is identical to that in the application as filed or does not go beyond the application as filed, as appropriate, were furnished.
4. Additional comments:

**WRITTEN OPINION OF THE
INTERNATIONAL SEARCHING AUTHORITY**

International application No.
PCT/US2005/036015

Box No. V Reasoned statement under Rule 43bis.1(a)(i) with regard to novelty, inventive step or industrial applicability; citations and explanations supporting such statement

1. Statement

Novelty (N)	Yes: Claims	5,6,16,17,23,24,32,33,41,42
	No: Claims	1-4, 7-15, 18-22, 25-31, 34-40,43-45
Inventive step (IS)	Yes: Claims	
	No: Claims	5,6,16,17,23,24,32,33,41,42
Industrial applicability (IA)	Yes: Claims	1-45
	No: Claims	

2. Citations and explanations

see separate sheet

Box No. VII Certain defects in the international application

The following defects in the form or contents of the international application have been noted:

see separate sheet

Box No. VIII Certain observations on the international application

The following observations on the clarity of the claims, description, and drawings or on the question whether the claims are fully supported by the description, are made:

see separate sheet

V. Reasoned Statement with regard to novelty, inventive step and industrial applicability; citations and explanations supporting such statement

I

The following documents are referenced for the first time in this written opinion; the numbering will be adhered to in the rest of the procedure:

- D1: US-B1-6 707 822
- D2: WO 03/063060 A
- D3: US-B1-6 337 877
- D4: "SunSet xDSL: Prequalification of ADSL Circuits with ATU-C Emulation", 2001, SUNRISE TELECOM INC., APPLICATION SERIES, XP002363272 Retrieved from the Internet: URL:<http://www.sunrisetelecom.com/technotes/APP-xDSL-8B.pdf> [retrieved on 2006-01-17]

II

- 1.1 The present broad formulation of independent method Claim 1 is such that its subject-matter can be read onto prior art Document D1 which discloses according to the wording of Claim 1 (the corresponding features in D1 are given in brackets):

A method for sharing resources (*abstract; column 2, lines 57-59; column 9, lines 10-23*) in a transceiver (*column 5, lines 23-30; fig. 2*), comprising:
allocating a first portion of shared memory (*fig. 2: IDIM RAM 230; column 3, lines 16-20*) to a first latency path (*e.g. to any interleave path for G.lite or standard ADSL, see column 6, line 66 to column 7, line 17*) and allocating a second portion of the shared memory to a second latency path (*column 6, lines 55-62 and column 7, lines 17-30: additional 4K dedicated memory space are allocated to any fast path*).

Consequently, the features of independent Claim 1 are already known from Document D1 and thus the subject-matter of Claim 1 is not novel. Claim 1 therefore does not meet the requirements of Articles 33(1) and (2) PCT.

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- 1.2 It should be noted that even if the Applicant were to interpret Claim 1 in such a manner as to enable him to allege that its subject-matter were novel, based on minor differences between the features of this claim and those disclosed in D1, the subject matter of Claim 1 would still not involve an inventive step, Articles 33(1) and (3) of the PCT, with respect to the disclosure of D1 especially as this document discloses the same object and the same type of solution as claimed.
2. The subject-matter of Claims 10, 19, 28 and 37 corresponds in terms of transceiver, system, protocol and storage media features respectively to that of Claim 1. Therefore, the objections raised in the previous paragraphs apply equally to Claims 10, 19, 28 and 37 which do consequently not meet the requirements of Articles 33(1) and (2) PCT for lack of novelty.
3. The dependent claims do not appear at present to contain any feature which in combination with the subject-matter of the independent claim to which the respective dependent claim is appended would result in novel and inventive subject-matter, these additional features being either disclosed or rendered obvious by the above cited documents, or being minor details obvious to a person skilled in the art based on common general knowledge of the art (Article 33(1) PCT). In particular, it is noted:

Claims 2-4, 13-15, 20-22, 29-31, 38-40: Use of interleaving/de-interleaving in two latency paths is known from D1. The latter teaches that depending on the used interleaving depth, several interleaved sessions or paths can be supported using the shared memory (*see column 7, lines 1-5 and 30-33*);

Claims 5, 6, 16, 17, 23, 24, 32, 33, 41, 42: Exchanging various information between two modems for determining resources that are available for a connection to be set up represents general common knowledge for the skilled person in the field of xDSL communications. It is therefore considered to be a straightforward design measure for a skilled person having knowledge of the shared memory transceivers in D1 to specifically exchange information regarding the maximum available interleaver memory size in order to accommodate a plurality of latency paths. D1 clearly teaches the skilled person that the memory size is a critical resource in terms of the number of

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PCT/US2005/036015

sessions/paths that can be supported contemporaneously (see column 7, lines 1-33). It does therefore not go beyond what can generally be expected from the skilled person in the light of D1 to exchange and use information specifying said critical amount of available shared memory;

Claim 7, 18, 25, 34, 43: Allocating a shared FCI module to perform the processing of two coder/decoder modules of two latency paths respectively is known from D1 (see column 6, lines 11-17; fig. 2: FCI 226 writes encoded data for different latency paths into RAM 230 and reads decoded data for different latency paths from it: column 8, line 62 to column 9, line 3);

Claims 8, 9, 11, 12, 26, 27, 35, 36, 44, 45: D1 teaches allocating a portion of memory to a path according to its latency (see column 6, lines 17-18: "Interleave and Fast Path"; column 7, lines 5-20: It is implicit to the skilled person from what is expressly said in D1 that the *interleaved* G.lite path requiring 4 Kbytes of memory imposes a higher processing latency than the fast path requiring only 256 bytes; on this point, the Applicant is also referred to D4 for information, see page 3, right-hand column, "Selecting the Path: Fast vs. Interleaved").

VII. Certain defects in the international application

1. To meet the requirements of Rule 6.3(b) PCT the independent claims should be cast in the two-part form, with those features known in combination from the prior art (see document D1) being placed in a preamble (Rule 6.3(b)(i) PCT) and with the remaining features being included in a characterising part (Rule 6.3(b)(ii) PCT).
2. To fulfil the requirements of Rule 5.1(a)(ii) PCT, document D1 should be identified in the description and the relevant background art disclosed therein briefly discussed.
3. The opening part of the description should be brought into conformity with any amended independent claims (Rule 5.1(a)(iii) PCT).
4. Furthermore, following the disclosure of document D1, the statement indicating the

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technical problem to be solved by the invention (see page 2, paragraphs [0005] and [0006]), requires revision, which should be effected taking the requirements of Rule 5.1(a)(iii) PCT into account.

5. Reference signs placed in parentheses should be inserted into all the claims to increase their intelligibility (Rule 6.2(b) PCT). This applies to both the preamble and the characterising portion.
6. The reference to the "spirit" of the invention should be deleted (see page 23, last line) (Article 6 PCT and PCT-Guidelines 5.30).
7. The expression "herein incorporated by reference" (see page 1, par. [0001] and [0003]) should be removed from the description (see the PCT-Guidelines, 4.26).
8. The description (see page 7, par. [0033]) refers to "**later** developed hardware, software or firmware". By definition, it is however unclear what this hardware, software and/or firmware will effectively look like in the future. This formulation, implying in general terms that the extent of protection may be expanded in some vague and not precisely defined way, should be deleted in accordance with Article 6 PCT and the PCT Guidelines 5.30.

The same applies to the formulation "later developed systems or structures, devices and/or software" on page 22, paragraph [0070].

9. The description on page 14, paragraph [0050] describes a third latency path for "a voice telephony application, which needs a very low latency but can tolerate BER".

The next sentence however contradicts the above statement: "In this case, the **video** [not voice ?] will be transported using an latency path that has a **large** amount of interleaving and coding [i.e. resulting in a high latency and thus contradicting the previously mentioned requirements for voice telephony ?]". Subsequently, this is again contradicted by the last sentence in paragraph [0050] stipulating that "no interleaving or coding" would be applied to said third latency path, further corroborated by the calculation in the following paragraph [0051] clearly assuming **no** interleaver memory and **no** encoding for the third path.

The second sentence of paragraph [0050] should thus be deleted for clarification.

10. The Applicant should remove the parentheses around the expression "BER" in Claims 9, 12, 27, 36 and 45 as this term does not represent a reference sign in the sense of Rule 6.2(b) PCT (see also the PCT-Guidelines 5.11).

VIII. Certain observations on the international application

The following objections are raised with respect to Article 6 PCT:

1. Independent Claim 28 (and its dependent Claims 29-36) repeat - word by word - the subject-matter already defined in Claim 1 (and its dependent Claims 2-9), thus contravening the requirement of Article 6 PCT that the claims shall be concise.

The generic terms "method" and "protocol" used in Claims 1 and 28 respectively belong to the same category "activity" as defined in the Guidelines 5.12 and can be used interchangeably. In fact, a protocol does not consist of anything more than a number of technical method steps.

The claims need to be recast to include only the minimum necessary number of independent claims in any one category (see Rule 6.1(a) PCT and the PCT-Guidelines, A5.42). In the present case it is considered appropriate to use only one independent claim in the "activity" (method) category.

Claim 28 and its dependent Claims 29-36 should thus be deleted.

2. Independent Claim 37 refers to "information that *when executed allows* sharing of resources in a transceiver, comprising information that allocates ...".

In its present wording, the claimed information is construed to be *suitable*, when executed, to share resources. The sharing of resources is thus not limiting the scope of the claim and the claimed information thus does not produce any technical effect whatsoever in terms of technical method steps being performed as a result of the

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information (or program code) being executed.

It is also unclear, where or on which physical entity the information (or program code) is being executed on. Indeed, the claimed information can only bring about a technical effect in conjunction with a physical device on which it is run or executed. Otherwise, it merely represents program code per se.

The same objections apply to dependent Claims 38-45.

Claim 37 should thus be clarified to read: "An information storage medium comprising information which, when executed on a computer, performs the method as defined in any one of Claims 1 to 9." Claims 39-45 should be deleted.

3. The category of *method* Claims 2-4 is unclear as their additional features solely relate to constituent *means* of the latency paths. It is indeed unclear, which steps of the claimed *method* are effectively to be construed from the claimed (de)interleavers.

The same objection applies to Claims 29-31 and 38-40.

4. The abbreviation "INP" as presented in Claims 9, 12, 27, 36 and 45 is not clear from the wording of the claim alone and should be replaced by "impulse noise protection" in the light of the description (see page 11, mid-paragraph [0041]).
5. Claim 7 refers to "allocating a shared processing module to a plurality of coding and/or decoding modules". It is unclear, whether or not and if so, to what extent, these modules are part of the transceiver referred to in Claim 1.

The same lack of clarity arises in Claims 18, 25, 34 and 43.

Electronic Acknowledgement Receipt	
EFS ID:	9199730
Application Number:	12901699
International Application Number:	
Confirmation Number:	1676
Title of Invention:	RESOURCE SHARING IN A TELECOMMUNICATIONS ENVIRONMENT
First Named Inventor/Applicant Name:	Marcos C. Tzannes
Customer Number:	62574
Filer:	Jason Vick/Nancy Davis
Filer Authorized By:	Jason Vick
Attorney Docket Number:	5550-54-CON-3
Receipt Date:	10-JAN-2011
Filing Date:	11-OCT-2010
Time Stamp:	16:08:14
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	no				
File Listing:					
Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1		IDS_01.pdf	566019 53043:99670c12566056769d864c04a3053 64r0k	yes	6

Multipart Description/PDF files in .zip description					
Document Description			Start	End	
Transmittal Letter			1	3	
Information Disclosure Statement (IDS) Filed (SB/08)			4	6	
Warnings:					
Information:					
2	Foreign Reference	EP1225735A1.pdf	3319471 nb5e96001141a0a10bfcd205c87ac59cadf92ed1	no	30
Warnings:					
Information:					
3	Foreign Reference	EP1246409A1.pdf	4522291 bf0232d471ba2a9d6eefc8db6d21a099e58283e	no	38
Warnings:					
Information:					
4	Foreign Reference	WO2003063060A2.pdf	2430819 c8fb5b302275e9e56acafdc0c30006c03345e36c	no	75
Warnings:					
Information:					
5	NPL Documents	WO2006044227A1.pdf	1310271 c4a14474104208b98fc05d78a6fa10b0bf968ba	no	37
Warnings:					
Information:					
6	NPL Documents	Shoji_WIRELESS_ACCESS_MET HOD_TO_ENSURE.pdf	1414514 e83281e015c9e4830594f8ec1232d0704b8c0314	no	14
Warnings:					
Information:					
7	NPL Documents	ITU- T_Recommendation_G992_5- 05-2003.pdf	3754491 12d286f0cd8ba48c6b97c43ccda7ca90a6811d	no	92
Warnings:					
Information:					
8	NPL Documents	ITU- T_Recommendation_G992_3- 01-2005.pdf	7371505 ed553373c7c854022481a11ef8724b4394ee075d	no	436
Warnings:					
Information:					

9	NPL Documents	ITU-T_Recommendation_G993_2-02-2006.pdf	14525041 c91a12cca242c4cde1216c1c50046fa1a1fa1f457	no	252
Warnings:					
Information:					
10	NPL Documents	Sunset_xDSL_Prequalification_of_ADSL_Circuits_with_ATU-C_Emulation.pdf	439680 e9560587c2f3d115c38a6dffa9054610015d00e9f3	no	4
Warnings:					
Information:					
11	NPL Documents	5550-54-PCT_ISR_2-8-2006.pdf	93073 8e385f5536a8c16ba027f3d7c71dca956d18190	no	3
Warnings:					
Information:					
12	NPL Documents	5550-54-PCT_Written_Opinion.pdf	983104 cb475ef6041b1b8f9142a18cda91ef74fb8592ec	no	9
Warnings:					
Information:					
13	NPL Documents	5550-54-PCT_IPRP.pdf	1236891 4eca8811bc3e36ddecfa91bc2d83a113a3a914	no	11
Warnings:					
Information:					
14	NPL Documents	5550-54-PAU_OA_6-24-09.pdf	1621631 cedbcea1107bdeceacf628ca73d2fa040390ac	no	30
Warnings:					
Information:					
15	NPL Documents	5550-54-PCN_OA_9-25-09.pdf	811648 107a3f916c5d4a1e8d16e4d4998d17dce02a0031	no	13
Warnings:					
Information:					
16	NPL Documents	5550-54_OA_2-24-09.pdf	865943 fa34782bc1d83ae1256676ebdae09ff75b97b9	no	23
Warnings:					
Information:					
17	NPL Documents	5550-54_OA_12-9-09.pdf	911747 c08dca7bd91911dc396793652122798a8713637b	no	25
Warnings:					
Information:					

18	NPL Documents	5550-54-CON_NOA_10-6-2010.pdf	319429 Bcd4c3d8f8f19ad6dea485b079c114f182606	no	8
Warnings:					
Information:					
19	NPL Documents	5550-54-CON-2_NOA_10-6-2010.pdf	269129 a78c4d42cc6dc704f83f1492f3e5a8849a257817	no	7
Warnings:					
Information:					
20	NPL Documents	5550-54_NOA_9-7-2010.pdf	326176 76b76548f16d839a5eeea4036cc873baa8b75c22b	no	8
Warnings:					
Information:					
Total Files Size (in bytes):			47092873		
This Acknowledgement Receipt evidences receipt on the noted date by the USPTO of the indicated documents, characterized by the applicant, and including page counts, where applicable. It serves as evidence of receipt similar to a Post Card, as described in MPEP 503. New Applications Under 35 U.S.C. 111 If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application. National Stage of an International Application under 35 U.S.C. 371 If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course. New International Application Filed with the USPTO as a Receiving Office If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.					

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In Re the Application of:	)	Group Art Unit: 2447
Marcos C. Tzannes	)	Confirmation No.: 1676
Serial No.: 12/901,699	)	Examiner: Not Yet Assigned
Filed: October 11, 2010	)	
Atty. File No.: 5550-54-CON-3	)	<u>INFORMATION DISCLOSURE</u>
Entitled: "RESOURCE SHARING IN A	)	<u>STATEMENT</u>
TELECOMMUNICATIONS ENVIRONMENT"	)	Electronically Submitted

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Dear Sir:

The references cited on attached Form PTO-1449 are being called to the attention of the Examiner.

- ☒ Copies of the cited non-patent and/or foreign references are enclosed herewith.
- ☐ Copies of the cited U.S. patents and/or patent applications are enclosed herewith.
- ☒ Copies of the cited U.S. patents/patent application publications are not enclosed in accordance with 37 C.F.R. § 1.98(a).
- ☐ Copies of the cited references are not enclosed, in accordance with 37 C.F.R. § 1.98(d), because the references were cited by or submitted to the U.S. Patent and Trademark Office in prior application Serial No. _____ filed _____, which is relied upon for an earlier filing date under 35 U.S.C. § 120.
- ☐ To the best of applicants' belief, the pertinence of the foreign-language references are believed to be summarized in the attached English abstracts and in the figures, although applicants do not necessarily vouch for the accuracy of the translation.
- ☒ Examiner's attention is drawn to the following related applications:

- Serial No. 11/246,163 filed 10-11-2005 now U.S. Patent No. 7,831,890 (Attorney's Ref. No. 5550-54)
- Serial No. 12/761,586 filed 04-16-2010 now U.S. Patent No. 7,844,882 (Attorney's Ref. No. 5550-54-CON)
- Serial No. 12/853,020 filed 08-09-2010 now U.S. Patent No. 7,836,381 (Attorney's Ref. No. 5550-54-CON-2)
- Serial No. 12/295,828 filed 10-02-2008 (Attorney's Ref. No. 5550-57-PUS)
- Serial No. 12/760,728 filed 04-15-2010 (Attorney's Ref. No. 5550-57-PUS-DIV)

- Serial No. 12/783,758 filed 05-20-2010 (Attorney's Ref. No. 5550-57-PUS-CON)
- Serial No. 12/783,765 filed 05-20-2010 (Attorney's Ref. No. 5550-57-PUS-DIV-CON)

☐ Other: _____

Submission of the above information is not intended as an admission that any item is citable under the statutes or rules to support a rejection, that any item disclosed represents analogous art, or that those skilled in the art would refer to or recognize the pertinence of any reference without the benefit of hindsight, nor should an inference be drawn as to the pertinence of the references based on the order in which they are presented. Submission of this statement should not be taken as an indication that a search has been conducted, or that no better art exists.

It is respectfully requested that the cited information be expressly considered during the prosecution of this application and the references made of record therein.

FEES

☒	37 CFR 1.97(b): No fee is believed due in connection with this submission, because the information disclosure statement submitted herewith is satisfied by one of the following conditions ("X" indicates satisfaction): ☒ Within three months of the filing date of a national application other than a continued prosecution application under 37 CFR 1.53(d), or ☐ Within three months of the date of entry into the national stage of an international application as set forth in 37 CFR 1.491 or ☐ Before the mailing date of a first Office Action on the merits, or ☐ Before the mailing of a first Office action after the filing of a request for continued examination under 37 CFR 1.114. Although no fee is believed due, if any fee is deemed due in connection with this submission, please charge such fee to Deposit Account 19-1970.
☐	37 CFR 1.97(c): The information disclosure statement transmitted herewith is being filed after all the above conditions (37 CFR 1.97(b)), but before the mailing date of one of the following conditions: (1) a final action under 37 C.F.R. 1.113 or (2) a notice of allowance under 37 C.F.R. 1.311, or (3) an action that otherwise closes prosecution in the application. This Information Disclosure Statement is accompanied by: ☐ A Certification (below) as specified by 37 C.F.R. 1.97(c). Although no fee is believed due, if any fee is deemed due in connection with this submission, please charge such fee to Deposit Account 19-1970. OR ☐ Please charge Deposit Account 19-1970 in the amount of \$180.00 for the fee set forth in 37 C.F.R. 1.17(p) for submission of an information disclosure statement. Please credit any overpayment or charge any underpayment to Deposit Account 19-1970.
☐	37 CFR 1.97(d): This Information Disclosure Statement is being submitted after the period specified in 37 CFR 1.97(c). ☐ This information Disclosure Statement includes a Certification (below) as specified by 37 C.F.R. 1.97(c) AND ☐ Applicants hereby requests consideration of the reference(s) disclosed herein. Please charge Deposit Account 19-1970 in the amount of \$180.00 under 37 C.F.R. 1.17(p). Please credit any overpayment or charge any underpayment to Deposit Account 19-1970. Election to pay the fee should not be taken as an indication that applicant(s) cannot execute a certification.

Certification (37 C.F.R. 1.97(e))
(Applicable only if checked)

☐

The undersigned certifies that:

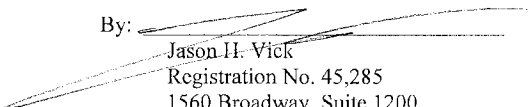
- ☐ Each item of information contained in this information disclosure statement was first cited in any communication from a foreign patent office in a counterpart foreign application not more than three months prior to the filing of this statement. 37 C.F.R. 1.97(e)(1).
- ☐ A copy of the communication from the foreign patent office is enclosed.

OR

- ☐ No item of information contained in this information disclosure statement was cited in a communication from a foreign patent office in a counterpart foreign application, and, to the knowledge of the undersigned after making reasonable inquiry, no item of information contained in this Information Disclosure Statement was known to any individual designated in 37 C.F.R. 1.56(e) more than three months prior to the filing of this statement. 37 C.F.R. 1.97(e)(2).

Respectfully submitted,

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Date: 10 Jan '11



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APPLICATION NUMBER	FILING or 371(c) DATE	GR/PART UNIT	FIL FEE REC'D	ATTY DOCKET NO	TOT CLAIMS	IND CLAIMS
12/901,699	10/11/2010	2189	1090	5550-54-CON-3	8	2

CONFIRMATION NO. 1676

FILING RECEIPT



0000000044120447

62574
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Date Mailed: 10/25/2010

Receipt is acknowledged of this non-provisional patent application. The application will be taken up for examination in due course. Applicant will be notified as to the results of the examination. Any correspondence concerning the application must include the following identification information: the U.S. APPLICATION NUMBER, FILING DATE, NAME OF APPLICANT, and TITLE OF INVENTION. Fees transmitted by check or draft are subject to collection. Please verify the accuracy of the data presented on this receipt. **If an error is noted on this Filing Receipt, please submit a written request for a Filing Receipt Correction. Please provide a copy of this Filing Receipt with the changes noted thereon. If you received a "Notice to File Missing Parts" for this application, please submit any corrections to this Filing Receipt with your reply to the Notice. When the USPTO processes the reply to the Notice, the USPTO will generate another Filing Receipt incorporating the requested corrections**

Applicant(s)

Marcos C. Tzannes, Orinda, CA;
Michael Lund, West Newton, MA;

Assignment For Published Patent Application

AWARE, INC., Bedford, MA

Power of Attorney: The patent practitioners associated with Customer Number 62574

Domestic Priority data as claimed by applicant

This application is a CON of 12/761,586 04/16/2010
which is a CON of 11/246,163 10/11/2005 PAT 7,831,890
which claims benefit of 60/618,269 10/12/2004

Foreign Applications

If Required, Foreign Filing License Granted: 10/21/2010

The country code and number of your priority application, to be used for filing abroad under the Paris Convention, is **US 12/901,699**

Projected Publication Date: 02/03/2011

Non-Publication Request: No

Early Publication Request: No

Title

RESOURCE SHARING IN A TELECOMMUNICATIONS ENVIRONMENT

Preliminary Class

711

PROTECTING YOUR INVENTION OUTSIDE THE UNITED STATES

Since the rights granted by a U.S. patent extend only throughout the territory of the United States and have no effect in a foreign country, an inventor who wishes patent protection in another country must apply for a patent in a specific country or in regional patent offices. Applicants may wish to consider the filing of an international application under the Patent Cooperation Treaty (PCT). An international (PCT) application generally has the same effect as a regular national patent application in each PCT-member country. The PCT process **simplifies** the filing of patent applications on the same invention in member countries, but **does not result** in a grant of "an international patent" and does not eliminate the need of applicants to file additional documents and fees in countries where patent protection is desired.

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For information on preventing theft of your intellectual property (patents, trademarks and copyrights), you may wish to consult the U.S. Government website, <http://www.stopfakes.gov>. Part of a Department of Commerce initiative, this website includes self-help "toolkits" giving innovators guidance on how to protect intellectual property in specific countries such as China, Korea and Mexico. For questions regarding patent enforcement issues, applicants may call the U.S. Government hotline at 1-866-999-HALT (1-866-999-4158).

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Title 35, United States Code, Section 184

Title 37, Code of Federal Regulations, 5.11 & 5.15

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page 2 of 3

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APPLICATION NUMBER	FILING OR 371(C) DATE	FIRST NAMED APPLICANT	ATTY. DOCKET NO./TITLE
12/901,699	10/11/2010	Marcos C. Tzannes	5550-54-CON-3

CONFIRMATION NO. 1676

POA ACCEPTANCE LETTER



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Date Mailed: 10/25/2010

NOTICE OF ACCEPTANCE OF POWER OF ATTORNEY

This is in response to the Power of Attorney filed 10/11/2010.

The Power of Attorney in this application is accepted. Correspondence in this application will be mailed to the above address as provided by 37 CFR 1.33.

/gmhtsun/

Office of Data Management, Application Assistance Unit (571) 272-4000, or (571) 272-4200, or 1-888-786-0101

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In Re the Application of: TZANNES et al.	)	Group Art Unit:
Application No.:	)	Examiner:
Filed: Herewith	)	Confirmation No.:
Atty. File No.: 5550-54-CON-3	)	

For: RESOURCE SHARING IN A TELECOMMUNICATIONS ENVIRONMENT

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313

PRELIMINARY AMENDMENT

Dear Sir:

Prior to the initial review of the above-identified patent application by the Examiner, please enter the following Preliminary Amendment. Although Applicants do not believe that any fees are due based upon the filing of this Preliminary Amendment, please charge any such fees to Deposit Account 19-1970.

Please amend the above-identified patent application as follows:

Amendments to the Specification begin on page 2 of this paper.

Amendments to the Claims are shown in the listing of claims which begin on page 4 of this paper.

Remarks begin on page 6 of this paper.

AMENDMENTS TO THE SPECIFICATION

Please replace paragraph [0001] with:

[0001] This application is a Continuation of U.S. Application No. 12/761,586, filed April 16, 2010, which is a Continuation of U.S. Application No. 11/246,163 filed October 11, 2005, which This application claims the benefit of and priority under 35 U.S.C. § 119(e) to U.S. Patent Application No. 60/618,269, filed October 12, 2004, entitled “Sharing Memory and Processing Resources in DSL Systems,” each of which ~~are~~ incorporated herein by reference in ~~their~~ its entirety.

Please replace paragraph [0003] with:

[0003] U.S. Patent Nos. 6,775,320 and 6,778,589, ~~which are both incorporated herein by reference in their entirety,~~ describe DSL systems supporting multiple applications and multiple framer/coder/interleaver FCI blocks (an FCI block is also referred to as a latency path). DSL systems carry applications that have different transmission requirements with regard to, for example, data rate, latency (delay), bit error rate (BER), and the like. For example, video typically requires a low BER ($<1E-10$) but can tolerate higher latency (>20 ms). Voice, on the other hand, typically requires a low latency (<1 ms) but can tolerate BER ($>1E-3$).

Please replace paragraph [0006] with:

[0006] Accordingly, an exemplary aspect of this invention relates to sharing memory between one or more interleavers and/or ~~deinterleavers~~ deinterleavers in a transceiver. More particularly, an exemplary aspect of this invention relates to shared latency path memory in a transceiver.

Please replace paragraph [0048] with:

[0048] Example #1

A first transmitter portion or receiver portion latency path may carry data from a video application, which needs a very low BER but can tolerate higher latency. In this case, the video will be transported using an latency path that has a large amount of interleaving/deinterleaving and coding (also known as Forward Error Correction (FEC) coding). For example, the latency path may be configured with Reed-Solomon coding using a codeword size of 255 bytes ($N=255$) with 16 checkbytes ($R=16$) and interleaving/deinterleaving using an interleaver depth of 64 ($D=64$). This latency path will require ~~$N \cdot D = 16 \cdot 255 = 16\text{Kbytes}$~~ $N \cdot D = 255 \cdot 64 = 16\text{Kbytes}$ of interleaver memory at the transmitter (or de-interleaver memory at the receiver). This latency path will be able to correct a burst of errors that is less than 512 bytes in duration.

AMENDMENTS TO THE CLAIMS

This listing of claims will replace all prior versions, and listings, of claims in the application.

Listing of Claims:

1.-45. (Cancelled)

46. (New) A system that allocates shared memory comprising:
a transceiver that is capable of:
transmitting or receiving a message during initialization specifying a maximum number of bytes of memory that are available to be allocated to an interleaver;
determining an amount of memory required by the interleaver to interleave a first plurality of Reed Solomon (RS) coded data bytes within a shared memory;
allocating a first number of bytes of the shared memory to the interleaver to interleave the first plurality of Reed Solomon (RS) coded data bytes for transmission at a first data rate, wherein the allocated memory for the interleaver does not exceed the maximum number of bytes specified in the message;
allocating a second number of bytes of the shared memory to a deinterleaver to deinterleave a second plurality of RS coded data bytes received at a second data rate; and
interleaving the first plurality of RS coded data bytes within the shared memory allocated to the interleaver and deinterleaving the second plurality of RS coded data bytes within the shared memory allocated to the deinterleaver, wherein the shared memory allocated to the interleaver is used at the same time as the shared memory allocated to the deinterleaver.

47. (New) The system of claim 46, wherein the determining is based on an impulse noise protection requirement.

48. (New) The system of claim 46, wherein the determining is based on a latency requirement.

49. (New) The system of claim 46, wherein the determining is based on a bit error rate requirement.

50. (New) A system that allocates shared memory comprising:
a transceiver that is capable of:

transmitting or receiving a message during initialization specifying a maximum number of bytes of memory that are available to be allocated to a deinterleaver;
determining an amount of memory required by the deinterleaver to deinterleave a first plurality of Reed Solomon (RS) coded data bytes within a shared memory;
allocating a first number of bytes of the shared memory to the deinterleaver to deinterleave a first plurality of Reed Solomon (RS) coded data bytes for transmission at a first data rate, wherein the allocated memory for the deinterleaver does not exceed the maximum number of bytes specified in the message;

allocating a second number of bytes of the shared memory to an interleaver to interleave a second plurality of RS coded data bytes received at a second data rate; and
deinterleaving the first plurality of RS coded data bytes within the shared memory allocated to the deinterleaver and interleaving the second plurality of RS coded data bytes within the shared memory allocated to the interleaver, wherein the shared memory allocated to the deinterleaver is used at the same time as the shared memory allocated to the interleaver.

51. (New) The system of claim 50, wherein the determining is based on an impulse noise protection requirement.

52. (New) The system of claim 50, wherein the determining is based on a latency requirement.

53. (New) The system of claim 50, wherein the determining is based on a bit error rate requirement.

REMARKS/ARGUMENTS

By this amendment, claims 1-45 are canceled without prejudice or disclaimer and new claims 46-53 are added.

Additionally, the continuity data has been updated and the specification amended in a similar manner as the parent application.

Applicants request examination on the merits.

Applicants believe that the pending claims are in condition for allowance and such disposition is respectfully requested. In the event that a telephone conversation would further prosecution and/or expedite allowance, the Examiner is invited to contact the undersigned.

The Commissioner is hereby authorized to charge to Deposit Account No. 19-1970 any fees under 37 C.F.R. §§ 1.16 and 1.17 that may be required by this paper and to credit any overpayment to that Account. If any extension of time is required in connection with the filing of this paper and has not been separately requested, such extension is hereby Petitioned.

Respectfully submitted,

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By: _____

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Date: 11 Oct '10

RESOURCE SHARING IN A TELECOMMUNICATIONS ENVIRONMENT

RELATED APPLICATION DATA

[0001] This application claims the benefit of and priority under 35 U.S.C. § 119(c) to U.S. Patent Application No. 60/618,269, filed October 12, 2004, entitled “Sharing Memory and Processing Resources in DSL Systems,” which is incorporated herein by reference in its entirety.

BACKGROUND

Field of the Invention

[0002] This invention generally relates to communication systems. More specifically, an exemplary embodiment of this invention relates to memory sharing in communication systems. Another exemplary embodiment relates to processing or coding resource sharing in a communication system.

Description of Related Art

[0003] U.S. Patent Nos. 6,775,320 and 6,778,589, which are both incorporated herein by reference in their entirety, describe DSL systems supporting multiple applications and multiple framer/coder/interleaver FCI blocks (an FCI block is also referred to as a latency path). DSL systems carry applications that have different transmission requirements with regard to, for example, data rate, latency (delay), bit error rate (BER), and the like. For example, video typically requires a low BER ($<1E-10$) but can tolerate higher latency (>20 ms). Voice, on the other hand, typically requires a low latency (<1 ms) but can tolerate BER ($>1E-3$).

[0004] As described in U.S. Patent No. 6,775,320, different applications can use different latency paths in order to satisfy the different application requirements of the communication system. As a result a transceiver must support multiple latency paths in order to support applications such as video, Internet access and voice telephony. When implemented in a transceiver, each of the latency paths will have a framer, coder, and interleaver block with different capabilities that depend on the application requirements.

SUMMARY

[0005] One difficulty with implementing multiple latency paths in a transceiver is the fact that a latency path is a complicated digital circuit that requires a large amount of memory and processing power. An interleaver within a latency path can consume a large amount of memory in order to provide error correcting capability. For example, a typical DSL transceiver will have at least one latency path with approximately 16 kbytes of memory for the interleaver. Likewise, the coding block, for example, a Reed Solomon coder, consumes a large amount of processing power. In general, as the number of latency paths increase, the memory and processing power requirements for a communication system become larger.

[0006] Accordingly, an exemplary aspect of this invention relates to sharing memory between one or more interleavers and/or deinterleavers in a transceiver. More particularly, an exemplary aspect of this invention relates to shared latency path memory in a transceiver.

[0007] Additional aspects of this invention relate to configuring and initializing shared memory in a communication system. More particularly, an exemplary aspect of this invention relates to configuring and initializing interleaver/deinterleaver memory in a communication system.

[0008] Additional aspects of the invention relate to determining the amount of memory that can be allocated to a particular component by a communication system. More specifically, an exemplary aspect of the invention relates to determining the maximum amount of shared memory that can be allocated to one or more interleaves or deinterleavers.

[0009] According to another exemplary aspect of the invention, processing power is shared between a number of transceiver modules. More specifically, and in accordance with an exemplary embodiment of the invention, a coding module is shared between one or more coders and/or decoders.

[0010] Another exemplary embodiment of the invention relates to transitioning from a fixed memory configuration to a shared memory configuration during one or more of initialization and SHOWTIME (user data transmission).

[0011] An additional exemplary aspect of the invention relates to dynamically updating one or more of shared memory and processing resources based on changing communication conditions.

[0012] An additional exemplary aspect of the invention relates to updating one or more of shared memory and processing resources based on an updated communication parameter.

[0013] An additional exemplary aspect of the invention relates to updating the allocation of one or more of shared memory and processing resources based on an updated communication parameter(s).

[0014] Additional aspects of the invention relate to exchanging shared resource allocations between transceivers.

[0015] Additional exemplary aspects relate to a method of allocating shared memory in a transceiver comprising allocating the shared memory to a plurality of modules, wherein each of the plurality of modules comprise at least one interleaver, at least one deinterleaver or a combination thereof.

[0016] Still further aspects relate to the above method wherein the plurality of modules comprise interleavers.

[0017] Still further aspects relate to the above method wherein the plurality of modules comprise deinterleavers.

[0018] Still further aspects relate to the above method wherein the plurality of modules comprise at least one interleaver and at least one deinterleaver.

[0019] Additional exemplary aspects relate to a transceiver comprising a plurality of modules each including at least one interleaver, at least one deinterleaver or a

combination thereof and a shared memory designed to be allocated to a plurality of the modules.

[0020] Still further aspects relate to the above transceiver wherein the plurality of modules comprise interleavers.

[0021] Still further aspects relate to the above transceiver wherein the plurality of modules comprise deinterleavers.

[0022] Still further aspects relate to the above transceiver wherein the plurality of modules comprise at least one interleaver and at least one deinterleaver.

[0023] These and other features and advantages of this invention are described in, or are apparent from, the following description of the embodiments.

BRIEF DESCRIPTION OF THE DRAWINGS

[0024] The embodiments of the invention will be described in detail, with reference to the following figures, wherein:

[0025] Fig. 1 is a functional block diagram illustrating an exemplary transceiver according to this invention;

[0026] Fig. 2 is a flowchart outlining an exemplary method of sharing resources according to this invention;

[0027] Fig. 3 is a flowchart outlining an exemplary method of determining a maximum amount of shared memory according to this invention; and

[0028] Fig. 4 is a flowchart outlining an exemplary resource sharing methodology according to this invention.

DETAILED DESCRIPTION

[0029] The exemplary embodiments of this invention will be described in relation to sharing resources in a wired and/or wireless communications environment. However, it should be appreciated, that in general, the systems and methods of this invention will work equally well for any type of communication system in any environment.

[0030] The exemplary systems and methods of this invention will also be described in relation to multicarrier modems, such as DSL modems and VDSL modems, and associated communication hardware, software and communication channels. However, to avoid unnecessarily obscuring the present invention, the following description omits well-known structures and devices that may be shown in block diagram form or otherwise summarized.

[0031] For purposes of explanation, numerous details are set forth in order to provide a thorough understanding of the present invention. It should be appreciated however that the present invention may be practiced in a variety of ways beyond the specific details set forth herein.

[0032] Furthermore, while the exemplary embodiments illustrated herein show the various components of the system collocated, it is to be appreciated that the various components of the system can be located at distant portions of a distributed

network, such as a telecommunications network and/or the Internet, or within a dedicated secure, unsecured and/or encrypted system. Thus, it should be appreciated that the components of the system can be combined into one or more devices, such as a modem, or collocated on a particular node of a distributed network, such as a telecommunications network. As will be appreciated from the following description, and for reasons of computational efficiency, the components of the system can be arranged at any location within a distributed network without affecting the operation of the system. For example, the various components can be located in a Central Office modem (CO, ATU-C, VTU-O), a Customer Premises modem (CPE, ATU-R, VTU-R), a DSL management device, or some combination thereof. Similarly, one or more functional portions of the system could be distributed between a modem and an associated computing device.

[0033] Furthermore, it should be appreciated that the various links, including communications channel 5, connecting the elements can be wired or wireless links, or any combination thereof, or any other known or later developed element(s) that is capable of supplying and/or communicating data to and from the connected elements. The term module as used herein can refer to any known or later developed hardware, software, firmware, or combination thereof that is capable of performing the functionality associated with that element. The terms determine, calculate and compute, and variations thereof, as used herein are used interchangeably and include any type of methodology, process, mathematical operation or technique. FCI block and latency path are used interchangeably herein as well as transmitting modem and transmitting transceiver. Receiving modem and receiving transceiver are also used

interchangably.

[0034] Fig. 1 illustrates an exemplary embodiment of a transceiver 100 that utilizes shared resources. It should be appreciated that numerous functional components of the transceiver have been omitted for clarity. However, the transceiver 100 can also include the standard components found in typical communications device(s) in which the technology of the subject invention is implemented into.

[0035] According to an exemplary embodiment of the invention, memory and processing power can be shared among a plurality of transmitter and/or receiver latency paths, in a communications transceiver that carries or supports multiple applications. For example, the transmitter and/or receiver latency paths of the transceiver can share an interleaver/deinterleaver memory and the shared memory can be allocated to the interleaver and/or deinterleaver of each latency path. This allocation can be done based on the data rate, latency, BER, impulse noise protection requirements of the application, data or information being transported over each latency path, or in general any parameter associated with the communications system.

[0036] Likewise, for example, the transmitter and/or receiver latency paths can share a Reed-Solomon coder/decoder processing module and the processing power of this module can be allocated to each encoder and/or decoder. This allocation can be done based on the data rate/latency, BER, impulse noise protection requirements of the application data or information being transported over each latency path, or in general based on any parameter associated with the communication system.

[0037] In accordance with an exemplary operational embodiment, a first transceiver and a second transceiver transmit to one another messages during, for example, initialization which contain information on the total and/or shared memory capabilities of each transceiver and optionally information about the one or more latency paths. This information can be transmitted prior to determining how to configure the latency paths to support the application requirements. Based on this information, one of the modems can select an FCI configuration parameter(s) that meets the transmission requirements of each application being transported over each latency paths. While an exemplary of the embodiment of the invention will be described in relation to the operation of the invention and characteristics thereof being established during initialization, it should be appreciated that the sharing of resources can be modified and messages transmitted between a two transceivers at any time during initialization and/or user data transmission, i.e., SHOWTIME.

[0038] Fig. 1 illustrates an exemplary embodiment of a transceiver 100. The transceiver 100 includes a transmitter portion 200 and a receiver portion 300. The transmitter portion 200 includes one or more latency paths 210, 220, ... Similarly, the receiver portion 300 includes one or more latency paths 310, 320, ... Each of the latency paths in the transmitter portion 200 includes a framer, coder, and interleaver designated as 212, 214, 216 and 222, 224 and 226, respectively. Each of the latency paths in the receiver portion includes a deframer, decoder, and deinterleaver designated as 312, 314, 316 and 322, 324, and 326, respectively. The transceiver 100 further includes a shared processing module 110, a shared memory 120, a parameter

determination module 130, a path module 140, an allocation module 150, and a shared resource management module 160, all interconnected by one or more links (not shown).

[0039] In this exemplary embodiment, the transceiver 100 is illustrated with four total transmitter portion and receiver portion latency paths, i.e., 210, 220, 310, and 320. The shared memory 120 is shared amongst the two transmitter portion interleavers 216 and 226 and two receiver portion deinterleavers 316 and 326. The shared processing module 110, such as a shared coding module, is shared between the two transmitter portion coders 214 and 224 and the two receiver portion decoders 314 and 324.

[0040] While the exemplary embodiment of the invention will be described in relation to a transceiver having a number of transmitter portion latency paths and receiver portion latency paths, it should be appreciated that this invention can be applied to any transceiver having any number of latency paths. Moreover, it should be appreciated that the sharing of resources can be allocated such that one or more of the transmitter portion latency paths are sharing a shared resource, one or more of the receiver portion latency paths are sharing a shared resource, or a portion of the transmitter portion latency paths and a portion of the receiver portion latency paths are sharing shared resources. Moreover, any one or more of the latency paths, or portions thereof, could also be assigned to a fixed resource while, for example, another portion of the latency path(s) assigned to a shared resource. For example, in latency path 210, the interleaver 216 could be allocated a portion of the shared

memory 120, while the coder 214 could be allocated to a dedicated processing module, vice versa, or the like.

[0041] In accordance with the exemplary embodiment, a plurality of transmitter portion or receiver portion latency paths share an interleaver/deinterleaver memory, such as shared memory 120, and a coding module, such as shared processing module 110. For example, the interleaver/deinterleaver memory can be allocated to different interleavers and/or deinterleavers. This allocation can be based on parameters associated with the communication systems such as data rate, latency, BER, impulse noise protection, and the like, of the applications being transported. Similarly, a coding module, which can be a portion of the shared processing module 110, can be shared between any one or more of the latency paths. This sharing can be based on requirements such as data rate, latency, BER, impulse noise protection, and the like, of the applications being transported.

[0042] For example, an exemplary transceiver could comprise a shared interleaver/deinterleaver memory and could be designed to allocate a first portion of the shared memory 120 to an interleaver, such as interleaver 216 in the transmitter portion of the transceiver and allocate a second portion of the shared memory 120 to a deinterleaver, such as 316, in the receiver portion of the transceiver.

[0043] Alternatively, for example, an exemplary transceiver can comprise a shared interleaver/deinterleaver memory, such as shared memory 120, and be designed to allocate a first portion of shared memory 120 to a first interleaver, e.g.,

216, in the transmitter portion of the transceiver and allocate a second portion of the shared memory to a second interleaver, e.g., 226, in the transmitter portion of the transceiver.

[0044] Alternatively, for example, an exemplary transceiver can comprise a shared interleaver/deinterleaver memory and be designed to allocate a first portion of the shared memory 120 to a first deinterleaver, e.g., 316, in the receiver portion of the transceiver and allocate a second portion of the shared memory to a second deinterleaver, e.g., 326, in the receiver portion of the transceiver. Regardless of the configuration, in general any interleaver or deinterleaver, or grouping thereof, be it in a transmitter portion or receiver portion of the transceiver, can be associated with a portion of the shared memory 120.

[0045] Establishment, configuration and usage of shared resources is performed in the following exemplary manner. First, and in cooperation with the path module 140, the number of transmitter and receiver latency paths (N) is determined. The parameter determination module 130 then analyses one or more parameters such as data rate, transmitter data rate, receiver data rate, impulse noise protection, bit error rate, latency, or the like. Based on one or more of these parameters, the allocation module 150 allocates a portion of the shared memory 120 to one or more of the interleaver and/or deinterleavers, or groupings thereof. This process continues until the memory allocation has been determined and assigned to each of the N latency paths.

[0046] Having determined the memory allocation for each of the latency paths, and in conjunction with the shared resource management 160, the transceiver 100 transmits to a second transceiver one or more of the number of latency paths (N), the maximum interleaver memory for any one or more of the latency paths and/or the maximum total and/or shared memory for all of the latency paths.

[0047] Three examples of sharing interleaver/deinterleaver memory and coding processing in a transceiver are described below. The latency paths in these examples can be in the transmitter portion of the transceiver or the receiver portion of the transceiver.

[0048] Example #1

A first transmitter portion or receiver portion latency path may carry data from a video application, which needs a very low BER but can tolerate higher latency. In this case, the video will be transported using an latency path that has a large amount of interleaving/deinterleaving and coding (also known as Forward Error Correction (FEC) coding). For example, the latency path may be configured with Reed-Solomon coding using a codeword size of 255 bytes ($N=255$) with 16 checkbytes ($R=16$) and interleaving/deinterleaving using an interleaver depth of 64 ($D=64$). This latency path will require $N*D=16*255=16\text{Kbytes}$ of interleaver memory at the transmitter (or de-interleaver memory at the receiver). This latency path will be able to correct a burst of errors that is less than 512 bytes in duration.

[0049] A second transmitter portion or receiver portion latency path may carry an

internet access application that requires a medium BER and a medium amount of latency. In this case, the internet access application will be transported using a latency path that has a medium amount of interleaving and coding. For example, the latency path may be configured with Reed-Solomon coding using a codeword size of 128 bytes ($N=128$) with 8 checkbytes ($R=8$) and interleaving using an interleaver depth of 16 ($D=32$). This latency path will require $N*D=128*32=4\text{Kbytes}$ of interleaver memory and the same amount of deinterleaver memory. This latency path will be able to correct a burst of errors that is less than 128 bytes in duration.

[0050] A third transmitter portion or receiver portion latency path may carry a voice telephony application, which needs a very low latency but can tolerate BER. In this case, the video will be transported using an latency path that has a large amount of interleaving and coding. For example, the third transmitter portion or receiver portion latency path may be configured with no interleaving or coding which will result in the lowest possible latency through the latency path but will provide no error correction capability.

[0051] According to the principles of this invention, a system carrying the three applications described above in Example #1, would have three latency paths that share one memory space containing at least $(16+4)=20$ Kbytes. The three latency paths also share a common coding block that is able to simultaneously encode (in the transmitter portion) or decode (in a receiver portion) two codewords with $N=255/R=16$ and $N=128/R=8$.

[0052] According to an exemplary embodiment of this invention, the latency paths can be reconfigured at initialization or during data transmission mode (also known as SHOWTIME in ADSL and VDSL transceivers). This would occur if, for example, the applications or application requirements were to change.

[0053] Example #2

If instead of 1 video application, 1 internet application and 1 voice application, there were 3 internet access applications then the transmitter portion and/or receiver portion latency paths would be reconfigured to utilize the shared memory and coding module in a different way. For example, the system could be reconfigured to have 3 transmitter portion or receiver portion latency paths, with each latency path being configured with Reed-Solomon coding using a codeword size of 128 bytes ($N=128$) with 8 checkbytes ($R=8$) and interleaving using an interleaver depth of 16 ($D=32$). Each latency path will require $N*D=128*32=4\text{Kbytes}$ of interleaver memory and each block will be able to correct a burst of errors that is less than 128 bytes in duration. Based on the example of carrying the three internet access applications described, the three latency path share one memory space containing at least $3*4=12\text{ Kbytes}$. Also the three latency paths share a common coding block that is able to simultaneously encode (on the transmitter side) or decode (on the receiver side) three codewords with $N=128/R=16$, $N=128/R=8$ and $N=128/R=8$.

[0054] Example #3

The system could be configured to carry yet another set of applications. For example, the latency paths could be configured to carry 2 video applications. In this case only

2 transmitter portion or receiver portion latency paths are needed, which means that the third latency path could be simply disabled. Also, assuming that the memory is constrained based on the first example above, then the maximum shared memory for these 2 latency paths is 20 kBytes. In this case, the system could be reconfigured to have 2 latency paths, with each block being configured with Reed-Solomon coding using a codeword size of 200 bytes ($N=200$) with 10 checkbytes ($R=10$) and interleaving/deinterleaving using an interleaver depth of 50 ($D=50$). Each latency path will require $N*D=200*50=10\text{Kbytes}$ of interleaver memory and each block will be able to correct a burst of errors that is less than 250 bytes in duration. This configuration results in 20K of shared memory for both latency paths, which is the same as in the first example. In order to stay within the memory constraints of the latency paths, the error correction capability for each latency path is decreased to 250 bytes from 512 bytes in Example #1.

[0055] Another aspect of this invention is the how FCI configuration information is transmitted between a first modem and a second modem. FCI configuration information will depend on the requirements of the applications being transported over the DSL connection. This information may need to be forwarded during initialization in order to initially configure the DSL connection. This information may also need to be forwarded during SHOWTIME in order to reconfigure the DSL connection based on a change in applications or the application requirements.

[0056] According to one embodiment, a first modem determines the specific FCI configuration parameters, e.g., N , D , R as defined above, needed to meet specific

application requirements, such as latency, burst error correction capability, etc. In order to determine the FCI configuration parameters, the first modem must know what are the capabilities of a second modem. For example, the first modem must know how many latency paths (FCI blocks) the second modem can support. Also the first modem must know the maximum amount of interleaver memory for each transmitter latency path. In addition, since the transmitter latency paths may share a common memory space the first modem must know the total shared memory for all transmitter latency paths. This way the first modem will be able to choose a configuration that can meet application requirements and also meet the transmitter portion latency path capabilities of the second modem.

[0057] For example, using values from examples above, a first transceiver could send a message to a second transceiver during initialization or during SHOWTIME containing the following information:

- Number of supported transmitter and receiver latency paths = 3
- Max Interleaver Memory for latency path #1= 16 Kbytes
- Max Interleaver Memory for latency path #2= 16 Kbytes
- Max Interleaver Memory for latency path #3= 16 Kbytes
- Maximum total/shared memory for all latency paths = 20 kBytes

Based on this information, and the application requirements, the first transceiver would select latency path settings. For example, if the applications are 1 video, 1 internet access and 1 voice application, the first transceiver could configure 3 latency paths as follows:

latency path #1 – Video: N=255, R=16, D=64

latency path #2 – Video: N=128, R=8, D=32

latency path #3 – Video: N=0, R=0, D=1 (no coding or interleaving)

[0058] This would result in a total interleaver memory of 20 kbytes.

[0059] Alternatively, if for example, there are only 2 video applications, the first transceiver could configure 2 latency paths as follows:

latency path #1 – Video: N=200, R=10, D=50

latency path #2 – Video: N=200, R=10, D=50

latency path #3 – Video: N=0, R=0, D=1 (no coding or interleaving)

[0060] This would also result in a total interleaver memory of 20 kbytes.

[0061] Alternatively, the second transceiver can determine the specific FCI configuration parameters, e.g., N, D, R as defined above, needed to meet specific application requirements, such as latency, burst error correction capability, etc. As described above for the first transceiver, in order to determine the FCI configuration parameters, the second transceiver must first know what are the capabilities of the first transceiver. In this case, the first transceiver would send a message to the second transceiver containing the information described above and based on this information and the application requirements the second transceiver would select latency path settings.

[0062] Fig. 2 outlines an exemplary method of allocating shared memory in a

transceiver. More specifically, control begins in step S200 and continues to step S210. In step S210, one or more of shared interleaver/deinterleaver memory and/or shared coder/decoder processing resources are allocated to one or more latency paths, in a transceiver. Control then continues to step S220 where the control sequence ends.

[0063] Fig. 3 outlines an exemplary method of exchanging shared resource allocations according to an exemplary embodiment of this invention. In particular, control begins in step S310. In step S310, a maximum amount of shared memory that can be allocated to a specific interleaver or deinterleaver of a plurality of interleavers or deinterleavers in a transceiver is determined. Next, in step S320, the determined maximum amount for one or more of the deinterleavers and/or interleavers is transmitted to another transceiver. Messages containing additional information can also be transmitted to the other transceiver and/or received from the other transceiver. Control then continues to step S330 where the control sequence ends.

[0064] Fig. 4 outlines an exemplary procedure for resource sharing according to an exemplary embodiment of this invention. In particular, control begins in step S400 and continues to step S410. In step S410, the number of latency paths are determined. Then, in step S420, the latency path information (FCI block information) is transmitted to another transceiver. Messages containing additional information can also be transmitted to the other transceiver and/or received from the other transceiver. This information can be used to, for example, assist with the determination of memory allocation in the transceiver. Moreover, the messages received from the

other transceiver could specify what the memory allocation is to be based on, for example, the number of latency paths, memory allocation in the remote transceiver and required applications. Control then continues to step S430.

[0065] In step S430, and for each latency path, the steps in step 440 are performed.

[0066] In step S440, and while monitoring of allocation of resources is being performed, steps 450 and 460 are performed. More specifically, in step S450, one or more parameters associated with the communication system are determined. Then, in step S460, shared resources are allocated based on one or more of the communication parameters. Control then continues to step S470.

[0067] In step S470, the allocation of shared resources is communicated to another transceiver. Next, in step S480, a determination is made as to whether there is a change in communications that would require the adjustment of the shared resource allocation. Examples of changes in communications conditions include a change in applications being transported over the system and/or changes in the channel condition, etc. If adjustments are required, control jumps back to step S410. Otherwise, control jumps to step S490 where the control sequence ends.

[0068] The above-described system can be implemented on wired and/or wireless telecommunications devices, such a modem, a multicarrier modem, a DSL modem, an ADSL modem, an XDSL modem, a VDSL modem, a linecard, test equipment, a

multicarrier transceiver, a wired and/or wireless wide/local area network system, a satellite communication system, a modem equipped with diagnostic capabilities, or the like, or on a separate programmed general purpose computer having a communications device or in conjunction with any of the following communications protocols: CDSL, ADSL2, ADSL2+, VDSL1, VDSL2, HDSL, DSL Lite, IDSL, RADSL, SDSL, UDSL or the like.

[0069] Additionally, the systems, methods and protocols of this invention can be implemented on a special purpose computer, a programmed microprocessor or microcontroller and peripheral integrated circuit element(s), an ASIC or other integrated circuit, a digital signal processor, a hard-wired electronic or logic circuit such as discrete element circuit, a programmable logic device such as PLD, PLA, FPGA, PAL, a modem, a transmitter/receiver, any comparable means, or the like. In general, any device capable of implementing a state machine that is in turn capable of implementing the methodology illustrated herein can be used to implement the various communication methods, protocols and techniques according to this invention.

[0070] Furthermore, the disclosed methods may be readily implemented in software using object or object-oriented software development environments that provide portable source code that can be used on a variety of computer or workstation platforms. Alternatively, the disclosed system may be implemented partially or fully in hardware using standard logic circuits or VLSI design. Whether software or hardware is used to implement the systems in accordance with this invention is

dependent on the speed and/or efficiency requirements of the system, the particular function, and the particular software or hardware systems or microprocessor or microcomputer systems being utilized. The communication systems, methods and protocols illustrated herein can be readily implemented in hardware and/or software using any known or later developed systems or structures, devices and/or software by those of ordinary skill in the applicable art from the functional description provided herein and with a general basic knowledge of the computer and telecommunications arts.

[0071] Moreover, the disclosed methods may be readily implemented in software that can be stored on a storage medium, executed on programmed general-purpose computer with the cooperation of a controller and memory, a special purpose computer, a microprocessor, or the like. In these instances, the systems and methods of this invention can be implemented as program embedded on personal computer such as an applet, JAVA[®] or CGI script, as a resource residing on a server or computer workstation, as a routine embedded in a dedicated communication system or system component, or the like. The system can also be implemented by physically incorporating the system and/or method into a software and/or hardware system, such as the hardware and software systems of a communications transceiver.

[0072] It is therefore apparent that there has been provided, in accordance with the present invention, systems and methods for sharing resources. While this invention has been described in conjunction with a number of embodiments, it is evident that many alternatives, modifications and variations would be or are apparent

to those of ordinary skill in the applicable arts. Accordingly, it is intended to embrace all such alternatives, modifications, equivalents and variations that are within the spirit and scope of this invention.

Claims:

1. A method for sharing resources in a transceiver comprising:
allocating a first portion of shared memory to a first latency path and
allocating a second portion of the shared memory to a second latency path.
2. The method of claim 1, wherein the first latency path includes an interleaver and the second latency path includes an interleaver.
3. The method of claim 1, wherein the first latency path includes an interleaver and the second latency path includes a deinterleaver.
4. The method of claim 1, wherein the first latency path includes a deinterleaver and the second latency path includes a deinterleaver.
5. The method of claim 1, further comprising transmitting to another transceiver information that is used to determine a maximum amount of shared memory that can be allocated.
6. The method of claim 1, further comprising receiving from another transceiver information that is used to determine a maximum amount of shared memory that can be allocated.
7. The method of claim 1, further comprising allocating a shared processing module to a plurality of coding and/or decoding modules.
8. The method of claim 1, wherein the allocating of at least one portion of the shared memory is based on one or more communication parameters.
9. The method of claim 8, wherein at least one of the communication parameters is a data rate, a latency, an INP value or a bit error rate (BER).

10. A transceiver comprising:
a first portion of shared memory that is allocated to a first latency path;
and
a second portion of the shared memory that is allocated to a second latency path.
11. The transceiver of claim 10, further comprising:
an allocation module designed to allocate the shared memory based on one or more communication parameters.
12. The transceiver of claim 11, wherein at least one of the communication parameters is a data rate, a latency, an INP value or a Bit Error Rate (BER).
13. The transceiver of claim 10, wherein the first latency path includes an interleaver and the second latency path includes an interleaver.
14. The transceiver of claim 10, wherein the first latency path includes an interleaver and the second latency path includes a deinterleaver.
15. The transceiver of claim 10, wherein the first latency path includes a deinterleaver and the second latency path includes a deinterleaver.
16. The transceiver of claim 10, further comprising a shared resource management module designed to determine information that is transmitted to another transceiver, wherein the information is used to determine a maximum amount of shared memory that can be allocated.
17. The transceiver of claim 10, further comprising a shared resource management module designed to utilize information that is received from another transceiver, wherein the information is used to determine a maximum amount of shared memory that can be allocated.

18. The transceiver of claim 10, further comprising a shared processing module designed to provide processing resources to a plurality of coding and/or decoding modules.

19. A system for sharing resources in a transceiver comprising:
means for allocating a first portion of shared memory to a first latency path and means for allocating a second portion of the shared memory to a second latency path.

20. The system of claim 19, wherein the first latency path includes an interleaver and the second latency path includes an interleaver.

21. The system of claim 19, wherein the first latency path includes an interleaver and the second latency path includes a deinterleaver.

22. The system of claim 19, wherein the first latency path includes a deinterleaver and the second latency path includes a deinterleaver.

23. The system of claim 19, further comprising means for transmitting to another transceiver information that is used to determine a maximum amount of shared memory that can be allocated.

24. The system of claim 19, further comprising means for receiving from another transceiver information that is used to determine a maximum amount of shared memory that can be allocated.

25. The system of claim 19, further comprising means for allocating a shared processing module to a plurality of coding and/or decoding modules.

26. The system of claim 19, wherein the allocating of at least one portion

of the shared memory is based on one or more communication parameters.

27. The system of claim 26, wherein at least one of the communication parameters is a data rate, a latency, an INP value or a bit error rate (BER).

28. A protocol for sharing resources in a transceiver comprising:
allocating a first portion of shared memory to a first latency path and
allocating a second portion of the shared memory to a second latency path.

29. The protocol of claim 28, wherein the first latency path includes an interleaver and the second latency path includes an interleaver.

30. The protocol of claim 28, wherein the first latency path includes an interleaver and the second latency path includes a deinterleaver.

31. The protocol of claim 28, wherein the first latency path includes a deinterleaver and the second latency path includes a deinterleaver.

32. The protocol of claim 28, further comprising transmitting to another transceiver information that is used to determine a maximum amount of shared memory that can be allocated.

33. The protocol of claim 28, further comprising receiving from another transceiver information that is used to determine a maximum amount of shared memory that can be allocated.

34. The protocol of claim 28, further comprising allocating a shared processing module to a plurality of coding and/or decoding modules.

35. The protocol of claim 28, wherein the allocating of at least one portion of the shared memory is based on one or more communication parameters.

36. The protocol of claim 35, wherein at least one of the communication parameters is a data rate, a latency, an INP value or a bit error rate (BER).

37. An information storage media having stored thereon information that when executed allows sharing of resources in a transceiver comprising:
information that allocates a first portion of shared memory to a first latency path and information that allocates a second portion of the shared memory to a second latency path.

38. The media of claim 37, wherein the first latency path includes an interleaver and the second latency path includes an interleaver.

39. The media of claim 37, wherein the first latency path includes an interleaver and the second latency path includes a deinterleaver.

40. The media of claim 37, wherein the first latency path includes a deinterleaver and the second latency path includes a deinterleaver.

41. The media of claim 37, further comprising information that transmits to another transceiver information that is used to determine a maximum amount of shared memory that can be allocated.

42. The media of claim 37, further comprising information that receives from another transceiver information that is used to determine a maximum amount of shared memory that can be allocated.

43. The media of claim 37, further comprising information that allocates a shared processing module to a plurality of coding and/or decoding modules.

44. The media of claim 37, wherein the allocating of at least one portion of

the shared memory is based on one or more communication parameters.

45. The media of claim 44, wherein at least one of the communication parameters is a data rate, a latency, an INP value or a bit error rate (BER).

ABSTRACT

A transceiver is designed to share memory and processing power amongst a plurality of transmitter and/or receiver latency paths, in a communications transceiver that carries or supports multiple applications. For example, the transmitter and/or receiver latency paths of the transceiver can share an interleaver/deinterleaver memory. This allocation can be done based on the data rate, latency, BER, impulse noise protection requirements of the application, data or information being transported over each latency path, or in general any parameter associated with the communications system.

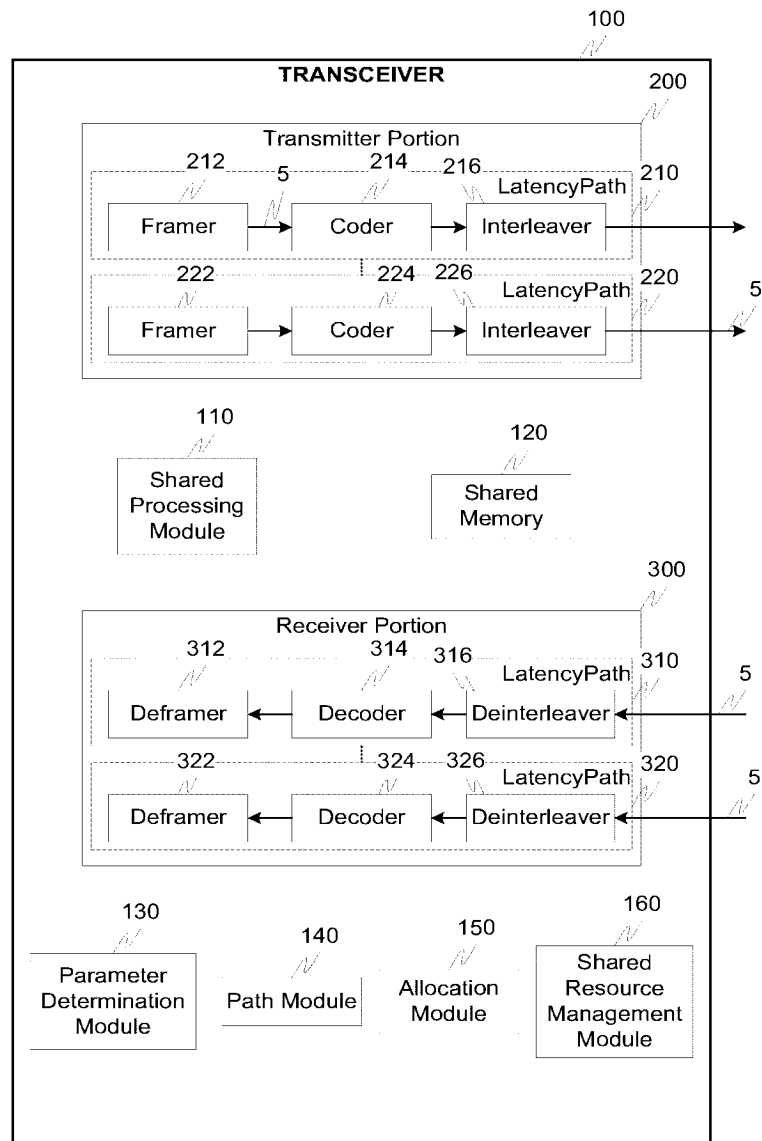


Fig. 1

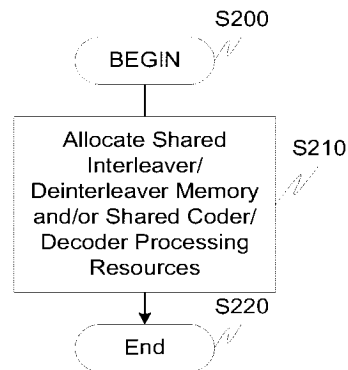


Fig. 2

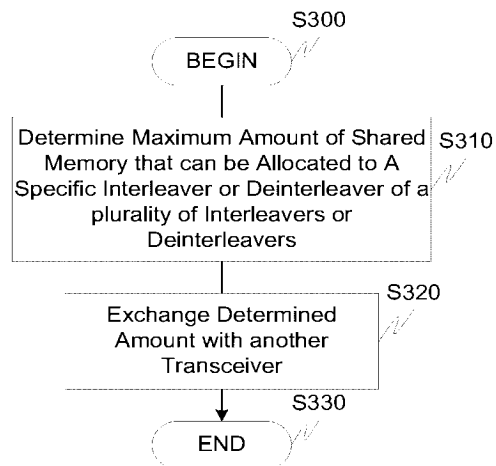


Fig. 3

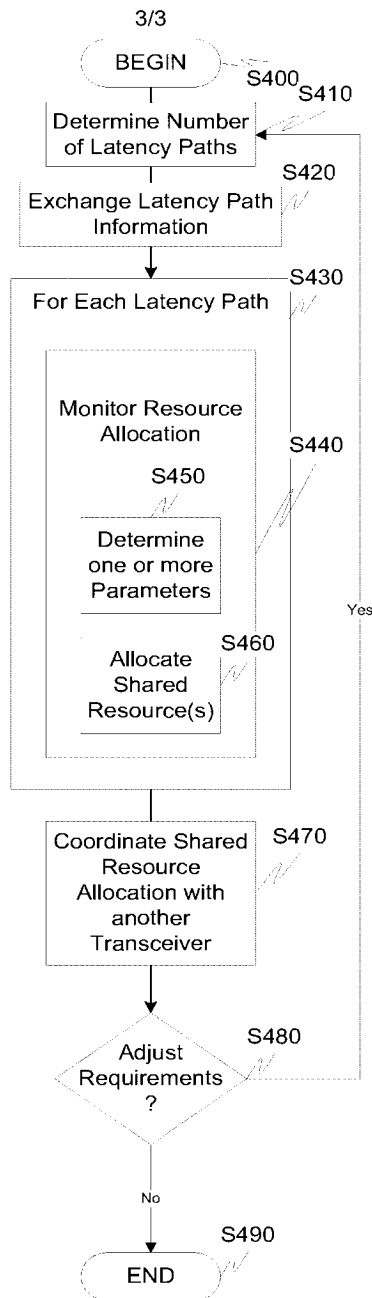


Fig. 4

RESOURCE SHARING IN A TELECOMMUNICATIONS ENVIRONMENT

RELATED APPLICATION DATA

[0001] This application is a Continuation of U.S. Application No. 12/761,586, filed April 16, 2010, which is a Continuation of U.S. Application No. 11/246,163 filed October 11, 2005, which ~~This application~~ claims the benefit of and priority under 35 U.S.C. § 119(e) to U.S. Patent Application No. 60/618,269, filed October 12, 2004, entitled “Sharing Memory and Processing Resources in DSL Systems,” each of which ~~are~~ is incorporated herein by reference in their~~its~~ entirety.

BACKGROUND

Field of the Invention

[0002] This invention generally relates to communication systems. More specifically, an exemplary embodiment of this invention relates to memory sharing in communication systems. Another exemplary embodiment relates to processing or coding resource sharing in a communication system.

Description of Related Art

[0003] U.S. Patent Nos. 6,775,320 and 6,778,589, ~~which are both incorporated herein by reference in their entirety,~~ describe DSL systems supporting multiple applications and multiple framer/coder/interleaver FCI blocks (an FCI block is also referred to as a latency path). DSL systems carry applications that have different transmission requirements with regard to, for example, data rate, latency (delay), bit error rate (BER), and the like. For example, video typically requires a low BER (<1E-10) but can tolerate higher latency (>20 ms). Voice, on the other hand, typically

requires a low latency (<1 ms) but can tolerate BER ($>1E-3$).

[0004] As described in U.S. Patent No. 6,775,320, different applications can use different latency paths in order to satisfy the different application requirements of the communication system. As a result a transceiver must support multiple latency paths in order to support applications such as video, Internet access and voice telephony. When implemented in a transceiver, each of the latency paths will have a framer, coder, and interleaver block with different capabilities that depend on the application requirements.

SUMMARY

[0005] One difficulty with implementing multiple latency paths in a transceiver is the fact that a latency path is a complicated digital circuit that requires a large amount of memory and processing power. An interleaver within a latency path can consume a large amount of memory in order to provide error correcting capability. For example, a typical DSL transceiver will have at least one latency path with approximately 16 kbytes of memory for the interleaver. Likewise, the coding block, for example, a Reed Solomon coder, consumes a large amount of processing power. In general, as the number of latency paths increase, the memory and processing power requirements for a communication system become larger.

[0006] Accordingly, an exemplary aspect of this invention relates to sharing memory between one or more interleavers and/or ~~deinterleavers~~ deinterleavers in a transceiver. More particularly, an exemplary aspect of this invention relates to shared

latency path memory in a transceiver.

[0007] Additional aspects of this invention relate to configuring and initializing shared memory in a communication system. More particularly, an exemplary aspect of this invention relates to configuring and initializing interleaver/deinterleaver memory in a communication system.

[0008] Additional aspects of the invention relate to determining the amount of memory that can be allocated to a particular component by a communication system. More specifically, an exemplary aspect of the invention relates to determining the maximum amount of shared memory that can be allocated to one or more interleaves or deinterleavers.

[0009] According to another exemplary aspect of the invention, processing power is shared between a number of transceiver modules. More specifically, and in accordance with an exemplary embodiment of the invention, a coding module is shared between one or more coders and/or decoders.

[0010] Another exemplary embodiment of the invention relates to transitioning from a fixed memory configuration to a shared memory configuration during one or more of initialization and SHOWTIME (user data transmission).

[0011] An additional exemplary aspect of the invention relates to dynamically updating one or more of shared memory and processing resources based on changing

communication conditions.

[0012] An additional exemplary aspect of the invention relates to updating one or more of shared memory and processing resources based on an updated communication parameter.

[0013] An additional exemplary aspect of the invention relates to updating the allocation of one or more of shared memory and processing resources based on an updated communication parameter(s).

[0014] Additional aspects of the invention relate to exchanging shared resource allocations between transceivers.

[0015] Additional exemplary aspects relate to a method of allocating shared memory in a transceiver comprising allocating the shared memory to a plurality of modules, wherein each of the plurality of modules comprise at least one interleaver, at least one deinterleaver or a combination thereof.

[0016] Still further aspects relate to the above method wherein the plurality of modules comprise interleavers.

[0017] Still further aspects relate to the above method wherein the plurality of modules comprise deinterleavers.

[0018] Still further aspects relate to the above method wherein the plurality of modules comprise at least one interleaver and at least one deinterleaver.

[0019] Additional exemplary aspects relate to a transceiver comprising a plurality

of modules each including at least one interleaver, at least one deinterleaver or a combination thereof and a shared memory designed to be allocated to a plurality of the modules.

[0020] Still further aspects relate to the above transceiver wherein the plurality of modules comprise interleavers.

[0021] Still further aspects relate to the above transceiver wherein the plurality of modules comprise deinterleavers.

[0022] Still further aspects relate to the above transceiver wherein the plurality of modules comprise at least one interleaver and at least one deinterleaver.

[0023] These and other features and advantages of this invention are described in, or are apparent from, the following description of the embodiments.

BRIEF DESCRIPTION OF THE DRAWINGS

[0024] The embodiments of the invention will be described in detail, with reference to the following figures, wherein:

[0025] Fig. 1 is a functional block diagram illustrating an exemplary transceiver according to this invention;

[0026] Fig. 2 is a flowchart outlining an exemplary method of sharing resources according to this invention;

[0027] Fig. 3 is a flowchart outlining an exemplary method of determining a maximum amount of shared memory according to this invention; and

[0028] Fig. 4 is a flowchart outlining an exemplary resource sharing methodology according to this invention.

DETAILED DESCRIPTION

[0029] The exemplary embodiments of this invention will be described in relation to sharing resources in a wired and/or wireless communications environment. However, it should be appreciated, that in general, the systems and methods of this invention will work equally well for any type of communication system in any environment.

[0030] The exemplary systems and methods of this invention will also be described in relation to multicarrier modems, such as DSL modems and VDSL modems, and associated communication hardware, software and communication channels. However, to avoid unnecessarily obscuring the present invention, the following description omits well-known structures and devices that may be shown in block diagram form or otherwise summarized.

[0031] For purposes of explanation, numerous details are set forth in order to provide a thorough understanding of the present invention. It should be appreciated however that the present invention may be practiced in a variety of ways beyond the specific details set forth herein.

[0032] Furthermore, while the exemplary embodiments illustrated herein show the various components of the system collocated, it is to be appreciated that the various components of the system can be located at distant portions of a distributed

network, such as a telecommunications network and/or the Internet, or within a dedicated secure, unsecured and/or encrypted system. Thus, it should be appreciated that the components of the system can be combined into one or more devices, such as a modem, or collocated on a particular node of a distributed network, such as a telecommunications network. As will be appreciated from the following description, and for reasons of computational efficiency, the components of the system can be arranged at any location within a distributed network without affecting the operation of the system. For example, the various components can be located in a Central Office modem (CO, ATU-C, VTU-O), a Customer Premises modem (CPE, ATU-R, VTU-R), a DSL management device, or some combination thereof. Similarly, one or more functional portions of the system could be distributed between a modem and an associated computing device.

[0033] Furthermore, it should be appreciated that the various links, including communications channel 5, connecting the elements can be wired or wireless links, or any combination thereof, or any other known or later developed element(s) that is capable of supplying and/or communicating data to and from the connected elements. The term module as used herein can refer to any known or later developed hardware, software, firmware, or combination thereof that is capable of performing the functionality associated with that element. The terms determine, calculate and compute, and variations thereof, as used herein are used interchangeably and include any type of methodology, process, mathematical operation or technique. FCI block and latency path are used interchangeably herein as well as transmitting modem and transmitting transceiver. Receiving modem and receiving transceiver are also used

interchangeably.

[0034] Fig. 1 illustrates an exemplary embodiment of a transceiver 100 that utilizes shared resources. It should be appreciated that numerous functional components of the transceiver have been omitted for clarity. However, the transceiver 100 can also include the standard components found in typical communications device(s) in which the technology of the subject invention is implemented into.

[0035] According to an exemplary embodiment of the invention, memory and processing power can be shared among a plurality of transmitter and/or receiver latency paths, in a communications transceiver that carries or supports multiple applications. For example, the transmitter and/or receiver latency paths of the transceiver can share an interleaver/deinterleaver memory and the shared memory can be allocated to the interleaver and/or deinterleaver of each latency path. This allocation can be done based on the data rate, latency, BER, impulse noise protection requirements of the application, data or information being transported over each latency path, or in general any parameter associated with the communications system.

[0036] Likewise, for example, the transmitter and/or receiver latency paths can share a Reed-Solomon coder/decoder processing module and the processing power of this module can be allocated to each encoder and/or decoder. This allocation can be done based on the data rate/latency, BER, impulse noise protection requirements of the application data or information being transported over each latency path, or in general based on any parameter associated with the communication system.

[0037] In accordance with an exemplary operational embodiment, a first transceiver and a second transceiver transmit to one another messages during, for example, initialization which contain information on the total and/or shared memory capabilities of each transceiver and optionally information about the one or more latency paths. This information can be transmitted prior to determining how to configure the latency paths to support the application requirements. Based on this information, one of the modems can select an FCI configuration parameter(s) that meets the transmission requirements of each application being transported over each latency paths. While an exemplary of the embodiment of the invention will be described in relation to the operation of the invention and characteristics thereof being established during initialization, it should be appreciated that the sharing of resources can be modified and messages transmitted between a two transceivers at any time during initialization and/or user data transmission, i.e., SHOWTIME.

[0038] Fig. 1 illustrates an exemplary embodiment of a transceiver 100. The transceiver 100 includes a transmitter portion 200 and a receiver portion 300. The transmitter portion 200 includes one or more latency paths 210, 220, ... Similarly, the receiver portion 300 includes one or more latency paths 310, 320, ... Each of the latency paths in the transmitter portion 200 includes a framer, coder, and interleaver designated as 212, 214, 216 and 222, 224 and 226, respectively. Each of the latency paths in the receiver portion includes a deframer, decoder, and deinterleaver designated as 312, 314, 316 and 322, 324, and 326, respectively. The transceiver 100 further includes a shared processing module 110, a shared memory 120, a parameter

determination module 130, a path module 140, an allocation module 150, and a shared resource management module 160, all interconnected by one or more links (not shown).

[0039] In this exemplary embodiment, the transceiver 100 is illustrated with four total transmitter portion and receiver portion latency paths, i.e., 210, 220, 310, and 320. The shared memory 120 is shared amongst the two transmitter portion interleavers 216 and 226 and two receiver portion deinterleavers 316 and 326. The shared processing module 110, such as a shared coding module, is shared between the two transmitter portion coders 214 and 224 and the two receiver portion decoders 314 and 324.

[0040] While the exemplary embodiment of the invention will be described in relation to a transceiver having a number of transmitter portion latency paths and receiver portion latency paths, it should be appreciated that this invention can be applied to any transceiver having any number of latency paths. Moreover, it should be appreciated that the sharing of resources can be allocated such that one or more of the transmitter portion latency paths are sharing a shared resource, one or more of the receiver portion latency paths are sharing a shared resource, or a portion of the transmitter portion latency paths and a portion of the receiver portion latency paths are sharing shared resources. Moreover, any one or more of the latency paths, or portions thereof, could also be assigned to a fixed resource while, for example, another portion of the latency path(s) assigned to a shared resource. For example, in latency path 210, the interleaver 216 could be allocated a portion of the shared

memory 120, while the coder 214 could be allocated to a dedicated processing module, vice versa, or the like.

[0041] In accordance with the exemplary embodiment, a plurality of transmitter portion or receiver portion latency paths share an interleaver/deinterleaver memory, such as shared memory 120, and a coding module, such as shared processing module 110. For example, the interleaver/deinterleaver memory can be allocated to different interleavers and/or deinterleavers. This allocation can be based on parameters associated with the communication systems such as data rate, latency, BER, impulse noise protection, and the like, of the applications being transported. Similarly, a coding module, which can be a portion of the shared processing module 110, can be shared between any one or more of the latency paths. This sharing can be based on requirements such as data rate, latency, BER, impulse noise protection, and the like, of the applications being transported.

[0042] For example, an exemplary transceiver could comprise a shared interleaver/deinterleaver memory and could be designed to allocate a first portion of the shared memory 120 to an interleaver, such as interleaver 216 in the transmitter portion of the transceiver and allocate a second portion of the shared memory 120 to a deinterleaver, such as 316, in the receiver portion of the transceiver.

[0043] Alternatively, for example, an exemplary transceiver can comprise a shared interleaver/deinterleaver memory, such as shared memory 120, and be designed to allocate a first portion of shared memory 120 to a first interleaver, e.g.,

216, in the transmitter portion of the transceiver and allocate a second portion of the shared memory to a second interleaver, e.g., 226, in the transmitter portion of the transceiver.

[0044] Alternatively, for example, an exemplary transceiver can comprise a shared interleaver/deinterleaver memory and be designed to allocate a first portion of the shared memory 120 to a first deinterleaver, e.g., 316, in the receiver portion of the transceiver and allocate a second portion of the shared memory to a second deinterleaver, e.g., 326, in the receiver portion of the transceiver. Regardless of the configuration, in general any interleaver or deinterleaver, or grouping thereof, be it in a transmitter portion or receiver portion of the transceiver, can be associated with a portion of the shared memory 120.

[0045] Establishment, configuration and usage of shared resources is performed in the following exemplary manner. First, and in cooperation with the path module 140, the number of transmitter and receiver latency paths (N) is determined. The parameter determination module 130 then analyses one or more parameters such as data rate, transmitter data rate, receiver data rate, impulse noise protection, bit error rate, latency, or the like. Based on one or more of these parameters, the allocation module 150 allocates a portion of the shared memory 120 to one or more of the interleaver and/or deinterleavers, or groupings thereof. This process continues until the memory allocation has been determined and assigned to each of the N latency paths.

[0046] Having determined the memory allocation for each of the latency paths, and in conjunction with the shared resource management 160, the transceiver 100 transmits to a second transceiver one or more of the number of latency paths (N), the maximum interleaver memory for any one or more of the latency paths and/or the maximum total and/or shared memory for all of the latency paths.

[0047] Three examples of sharing interleaver/deinterleaver memory and coding processing in a transceiver are described below. The latency paths in these examples can be in the transmitter portion of the transceiver or the receiver portion of the transceiver.

[0048] Example #1

A first transmitter portion or receiver portion latency path may carry data from a video application, which needs a very low BER but can tolerate higher latency. In this case, the video will be transported using an latency path that has a large amount of interleaving/deinterleaving and coding (also known as Forward Error Correction (FEC) coding). For example, the latency path may be configured with Reed-Solomon coding using a codeword size of 255 bytes (N=255) with 16 checkbytes (R=16) and interleaving/deinterleaving using an interleaver depth of 64 (D=64). This latency path will require $N \cdot D = 16 \cdot 255 = 16\text{Kbytes}$ ~~$N \cdot D = 255 \cdot 64 = 16\text{Kbytes}$~~ of interleaver memory at the transmitter (or de-interleaver memory at the receiver). This latency path will be able to correct a burst of errors that is less than 512 bytes in duration.

[0049] A second transmitter portion or receiver portion latency path may carry an

internet access application that requires a medium BER and a medium amount of latency. In this case, the internet access application will be transported using a latency path that has a medium amount of interleaving and coding. For example, the latency path may be configured with Reed-Solomon coding using a codeword size of 128 bytes ($N=128$) with 8 checkbytes ($R=8$) and interleaving using an interleaver depth of 16 ($D=32$). This latency path will require $N*D=128*32=4$ Kbytes of interleaver memory and the same amount of deinterleaver memory. This latency path will be able to correct a burst of errors that is less than 128 bytes in duration.

[0050] A third transmitter portion or receiver portion latency path may carry a voice telephony application, which needs a very low latency but can tolerate BER. In this case, the video will be transported using a latency path that has a large amount of interleaving and coding. For example, the third transmitter portion or receiver portion latency path may be configured with no interleaving or coding which will result in the lowest possible latency through the latency path but will provide no error correction capability.

[0051] According to the principles of this invention, a system carrying the three applications described above in Example #1, would have three latency paths that share one memory space containing at least $(16+4)=20$ Kbytes. The three latency paths also share a common coding block that is able to simultaneously encode (in the transmitter portion) or decode (in a receiver portion) two codewords with $N=255/R=16$ and $N=128/R=8$.

[0052] According to an exemplary embodiment of this invention, the latency paths can be reconfigured at initialization or during data transmission mode (also known as SHOWTIME in ADSL and VDSL transceivers). This would occur if, for example, the applications or application requirements were to change.

[0053] Example #2

If instead of 1 video application, 1 internet application and 1 voice application, there were 3 internet access applications then the transmitter portion and/or receiver portion latency paths would be reconfigured to utilize the shared memory and coding module in a different way. For example, the system could be reconfigured to have 3 transmitter portion or receiver portion latency paths, with each latency path being configured with Reed-Solomon coding using a codeword size of 128 bytes ($N=128$) with 8 checkbytes ($R=8$) and interleaving using an interleaver depth of 16 ($D=32$). Each latency path will require $N*D=128*32=4$ Kbytes of interleaver memory and each block will be able to correct a burst of errors that is less than 128 bytes in duration. Based on the example of carrying the three internet access applications described, the three latency path share one memory space containing at least $3*4=12$ Kbytes. Also the three latency paths share a common coding block that is able to simultaneously encode (on the transmitter side) or decode (on the receiver side) three codewords with $N=128/R=16$, $N=128/R=8$ and $N=128/R=8$.

[0054] Example #3

The system could be configured to carry yet another set of applications. For example, the latency paths could be configured to carry 2 video applications. In this case only

2 transmitter portion or receiver portion latency paths are needed, which means that the third latency path could be simply disabled. Also, assuming that the memory is constrained based on the first example above, then the maximum shared memory for these 2 latency paths is 20 kBytes. In this case, the system could be reconfigured to have 2 latency paths, with each block being configured with Reed-Solomon coding using a codeword size of 200 bytes ($N=200$) with 10 checkbytes ($R=10$) and interleaving/deinterleaving using an interleaver depth of 50 ($D=50$). Each latency path will require $N*D=200*50=10\text{Kbytes}$ of interleaver memory and each block will be able to correct a burst of errors that is less than 250 bytes in duration. This configuration results in 20K of shared memory for both latency paths, which is the same as in the first example. In order to stay within the memory constraints of the latency paths, the error correction capability for each latency path is decreased to 250 bytes from 512 bytes in Example #1.

[0055] Another aspect of this invention is the how FCI configuration information is transmitted between a first modem and a second modem. FCI configuration information will depend on the requirements of the applications being transported over the DSL connection. This information may need to be forwarded during initialization in order to initially configure the DSL connection. This information may also need to be forwarded during SHOWTIME in order to reconfigure the DSL connection based on a change in applications or the application requirements.

[0056] According to one embodiment, a first modem determines the specific FCI configuration parameters, e.g., N , D , R as defined above, needed to meet specific

application requirements, such as latency, burst error correction capability, etc. In order to determine the FCI configuration parameters, the first modem must know what are the capabilities of a second modem. For example, the first modem must know how many latency paths (FCI blocks) the second modem can support. Also the first modem must know the maximum amount of interleaver memory for each transmitter latency path. In addition, since the transmitter latency paths may share a common memory space the first modem must know the total shared memory for all transmitter latency paths. This way the first modem will be able to choose a configuration that can meet application requirements and also meet the transmitter portion latency path capabilities of the second modem.

[0057] For example, using values from examples above, a first transceiver could send a message to a second transceiver during initialization or during SHOWTIME containing the following information:

- Number of supported transmitter and receiver latency paths = 3
- Max Interleaver Memory for latency path #1= 16 Kbytes
- Max Interleaver Memory for latency path #2= 16 Kbytes
- Max Interleaver Memory for latency path #3= 16 Kbytes
- Maximum total/shared memory for all latency paths = 20 kBytes

Based on this information, and the application requirements, the first transceiver would select latency path settings. For example, if the applications are 1 video, 1 internet access and 1 voice application, the first transceiver could configure 3 latency paths as follows:

latency path #1 – Video: N=255, R=16, D=64

latency path #2 – Video: $N=128$, $R=8$, $D=32$

latency path #3 – Video: $N=0$, $R=0$, $D=1$ (no coding or interleaving)

[0058] This would result in a total interleaver memory of 20 kbytes.

[0059] Alternatively, if for example, there are only 2 video applications, the first transceiver could configure 2 latency paths as follows:

latency path #1 – Video: $N=200$, $R=10$, $D=50$

latency path #2 – Video: $N=200$, $R=10$, $D=50$

latency path #3 – Video: $N=0$, $R=0$, $D=1$ (no coding or interleaving)

[0060] This would also result in a total interleaver memory of 20 kbytes.

[0061] Alternatively, the second transceiver can determine the specific FCI configuration parameters, e.g., N , D , R as defined above, needed to meet specific application requirements, such as latency, burst error correction capability, etc. As described above for the first transceiver, in order to determine the FCI configuration parameters, the second transceiver must first know what are the capabilities of the first transceiver. In this case, the first transceiver would send a message to the second transceiver containing the information described above and based on this information and the application requirements the second transceiver would select latency path settings.

[0062] Fig. 2 outlines an exemplary method of allocating shared memory in a

transceiver. More specifically, control begins in step S200 and continues to step S210. In step S210, one or more of shared interleaver/deinterleaver memory and/or shared coder/decoder processing resources are allocated to one or more latency paths, in a transceiver. Control then continues to step S220 where the control sequence ends.

[0063] Fig. 3 outlines an exemplary method of exchanging shared resource allocations according to an exemplary embodiment of this invention. In particular, control begins in step S310. In step S310, a maximum amount of shared memory that can be allocated to a specific interleaver or deinterleaver of a plurality of interleavers or deinterleavers in a transceiver is determined. Next, in step S320, the determined maximum amount for one or more of the deinterleavers and/or interleavers is transmitted to another transceiver. Messages containing additional information can also be transmitted to the other transceiver and/or received from the other transceiver. Control then continues to step S330 where the control sequence ends.

[0064] Fig. 4 outlines an exemplary procedure for resource sharing according to an exemplary embodiment of this invention. In particular, control begins in step S400 and continues to step S410. In step S410, the number of latency paths are determined. Then, in step S420, the latency path information (FCI block information) is transmitted to another transceiver. Messages containing additional information can also be transmitted to the other transceiver and/or received from the other transceiver. This information can be used to, for example, assist with the determination of memory allocation in the transceiver. Moreover, the messages received from the

other transceiver could specify what the memory allocation is to be based on, for example, the number of latency paths, memory allocation in the remote transceiver and required applications. Control then continues to step S430.

[0065] In step S430, and for each latency path, the steps in step 440 are performed.

[0066] In step S440, and while monitoring of allocation of resources is being performed, steps 450 and 460 are performed. More specifically, in step S450, one or more parameters associated with the communication system are determined. Then, in step S460, shared resources are allocated based on one or more of the communication parameters. Control then continues to step S470.

[0067] In step S470, the allocation of shared resources is communicated to another transceiver. Next, in step S480, a determination is made as to whether there is a change in communications that would require the adjustment of the shared resource allocation. Examples of changes in communications conditions include a change in applications being transported over the system and/or changes in the channel condition, etc. If adjustments are required, control jumps back to step S410. Otherwise, control jumps to step S490 where the control sequence ends.

[0068] The above-described system can be implemented on wired and/or wireless telecommunications devices, such a modem, a multicarrier modem, a DSL modem, an ADSL modem, an XDSL modem, a VDSL modem, a linecard, test equipment, a

multicarrier transceiver, a wired and/or wireless wide/local area network system, a satellite communication system, a modem equipped with diagnostic capabilities, or the like, or on a separate programmed general purpose computer having a communications device or in conjunction with any of the following communications protocols: CDSL, ADSL2, ADSL2+, VDSL1, VDSL2, HDSL, DSL Lite, IDSL, RADSL, SDSL, UDSL or the like.

[0069] Additionally, the systems, methods and protocols of this invention can be implemented on a special purpose computer, a programmed microprocessor or microcontroller and peripheral integrated circuit element(s), an ASIC or other integrated circuit, a digital signal processor, a hard-wired electronic or logic circuit such as discrete element circuit, a programmable logic device such as PLD, PLA, FPGA, PAL, a modem, a transmitter/receiver, any comparable means, or the like. In general, any device capable of implementing a state machine that is in turn capable of implementing the methodology illustrated herein can be used to implement the various communication methods, protocols and techniques according to this invention.

[0070] Furthermore, the disclosed methods may be readily implemented in software using object or object-oriented software development environments that provide portable source code that can be used on a variety of computer or workstation platforms. Alternatively, the disclosed system may be implemented partially or fully in hardware using standard logic circuits or VLSI design. Whether software or hardware is used to implement the systems in accordance with this invention is

dependent on the speed and/or efficiency requirements of the system, the particular function, and the particular software or hardware systems or microprocessor or microcomputer systems being utilized. The communication systems, methods and protocols illustrated herein can be readily implemented in hardware and/or software using any known or later developed systems or structures, devices and/or software by those of ordinary skill in the applicable art from the functional description provided herein and with a general basic knowledge of the computer and telecommunications arts.

[0071] Moreover, the disclosed methods may be readily implemented in software that can be stored on a storage medium, executed on programmed general-purpose computer with the cooperation of a controller and memory, a special purpose computer, a microprocessor, or the like. In these instances, the systems and methods of this invention can be implemented as program embedded on personal computer such as an applet, JAVA® or CGI script, as a resource residing on a server or computer workstation, as a routine embedded in a dedicated communication system or system component, or the like. The system can also be implemented by physically incorporating the system and/or method into a software and/or hardware system, such as the hardware and software systems of a communications transceiver.

[0072] It is therefore apparent that there has been provided, in accordance with the present invention, systems and methods for sharing resources. While this invention has been described in conjunction with a number of embodiments, it is evident that many alternatives, modifications and variations would be or are apparent

to those of ordinary skill in the applicable arts. Accordingly, it is intended to embrace all such alternatives, modifications, equivalents and variations that are within the spirit and scope of this invention.

ABSTRACT

A transceiver is designed to share memory and processing power amongst a plurality of transmitter and/or receiver latency paths, in a communications transceiver that carries or supports multiple applications. For example, the transmitter and/or receiver latency paths of the transceiver can share an interleaver/deinterleaver memory. This allocation can be done based on the data rate, latency, BER, impulse noise protection requirements of the application, data or information being transported over each latency path, or in general any parameter associated with the communications system.

RESOURCE SHARING IN A TELECOMMUNICATIONS ENVIRONMENT

RELATED APPLICATION DATA

[0001] This application is a Continuation of U.S. Application No. 12/761,586, filed April 16, 2010, which is a Continuation of U.S. Application No. 11/246,163 filed October 11, 2005, which claims the benefit of and priority under 35 U.S.C. § 119(e) to U.S. Patent Application No. 60/618,269, filed October 12, 2004, entitled “Sharing Memory and Processing Resources in DSL Systems,” each of which are incorporated herein by reference in their entirety.

BACKGROUND

Field of the Invention

[0002] This invention generally relates to communication systems. More specifically, an exemplary embodiment of this invention relates to memory sharing in communication systems. Another exemplary embodiment relates to processing or coding resource sharing in a communication system.

Description of Related Art

[0003] U.S. Patent Nos. 6,775,320 and 6,778,589 describe DSL systems supporting multiple applications and multiple framer/coder/interleaver FCI blocks (an FCI block is also referred to as a latency path). DSL systems carry applications that have different transmission requirements with regard to, for example, data rate, latency (delay), bit error rate (BER), and the like. For example, video typically requires a low BER ($<1E-10$) but can tolerate higher latency (>20 ms). Voice, on the other hand, typically requires a low latency (<1 ms) but can tolerate BER ($>1E-3$).

[0004] As described in U.S. Patent No. 6,775,320, different applications can use different latency paths in order to satisfy the different application requirements of the communication system. As a result a transceiver must support multiple latency paths in order to support applications such as video, Internet access and voice telephony. When implemented in a transceiver, each of the latency paths will have a framer, coder, and interleaver block with different capabilities that depend on the application requirements.

SUMMARY

[0005] One difficulty with implementing multiple latency paths in a transceiver is the fact that a latency path is a complicated digital circuit that requires a large amount of memory and processing power. An interleaver within a latency path can consume a large amount of memory in order to provide error correcting capability. For example, a typical DSL transceiver will have at least one latency path with approximately 16 kbytes of memory for the interleaver. Likewise, the coding block, for example, a Reed Solomon coder, consumes a large amount of processing power. In general, as the number of latency paths increase, the memory and processing power requirements for a communication system become larger.

[0006] Accordingly, an exemplary aspect of this invention relates to sharing memory between one or more interleavers and/or deinterleavers in a transceiver. More particularly, an exemplary aspect of this invention relates to shared latency path memory in a transceiver.

[0007] Additional aspects of this invention relate to configuring and initializing shared memory in a communication system. More particularly, an exemplary aspect of this invention relates to configuring and initializing interleaver/deinterleaver memory in a communication system.

[0008] Additional aspects of the invention relate to determining the amount of memory that can be allocated to a particular component by a communication system. More specifically, an exemplary aspect of the invention relates to determining the maximum amount of shared memory that can be allocated to one or more interleaves or deinterleavers.

[0009] According to another exemplary aspect of the invention, processing power is shared between a number of transceiver modules. More specifically, and in accordance with an exemplary embodiment of the invention, a coding module is shared between one or more coders and/or decoders.

[0010] Another exemplary embodiment of the invention relates to transitioning from a fixed memory configuration to a shared memory configuration during one or more of initialization and SHOWTIME (user data transmission).

[0011] An additional exemplary aspect of the invention relates to dynamically updating one or more of shared memory and processing resources based on changing communication conditions.

[0012] An additional exemplary aspect of the invention relates to updating one or more of shared memory and processing resources based on an updated communication parameter.

[0013] An additional exemplary aspect of the invention relates to updating the allocation of one or more of shared memory and processing resources based on an updated communication parameter(s).

[0014] Additional aspects of the invention relate to exchanging shared resource allocations between transceivers.

[0015] Additional exemplary aspects relate to a method of allocating shared memory in a transceiver comprising allocating the shared memory to a plurality of modules, wherein each of the plurality of modules comprise at least one interleaver, at least one deinterleaver or a combination thereof.

[0016] Still further aspects relate to the above method wherein the plurality of modules comprise interleavers.

[0017] Still further aspects relate to the above method wherein the plurality of modules comprise deinterleavers.

[0018] Still further aspects relate to the above method wherein the plurality of modules comprise at least one interleaver and at least one deinterleaver.

[0019] Additional exemplary aspects relate to a transceiver comprising a plurality of modules each including at least one interleaver, at least one deinterleaver or a

combination thereof and a shared memory designed to be allocated to a plurality of the modules.

[0020] Still further aspects relate to the above transceiver wherein the plurality of modules comprise interleavers.

[0021] Still further aspects relate to the above transceiver wherein the plurality of modules comprise deinterleavers.

[0022] Still further aspects relate to the above transceiver wherein the plurality of modules comprise at least one interleaver and at least one deinterleaver.

[0023] These and other features and advantages of this invention are described in, or are apparent from, the following description of the embodiments.

BRIEF DESCRIPTION OF THE DRAWINGS

[0024] The embodiments of the invention will be described in detail, with reference to the following figures, wherein:

[0025] Fig. 1 is a functional block diagram illustrating an exemplary transceiver according to this invention;

[0026] Fig. 2 is a flowchart outlining an exemplary method of sharing resources according to this invention;

[0027] Fig. 3 is a flowchart outlining an exemplary method of determining a maximum amount of shared memory according to this invention; and

[0028] Fig. 4 is a flowchart outlining an exemplary resource sharing methodology according to this invention.

DETAILED DESCRIPTION

[0029] The exemplary embodiments of this invention will be described in relation to sharing resources in a wired and/or wireless communications environment. However, it should be appreciated, that in general, the systems and methods of this invention will work equally well for any type of communication system in any environment.

[0030] The exemplary systems and methods of this invention will also be described in relation to multicarrier modems, such as DSL modems and VDSL modems, and associated communication hardware, software and communication channels. However, to avoid unnecessarily obscuring the present invention, the following description omits well-known structures and devices that may be shown in block diagram form or otherwise summarized.

[0031] For purposes of explanation, numerous details are set forth in order to provide a thorough understanding of the present invention. It should be appreciated however that the present invention may be practiced in a variety of ways beyond the specific details set forth herein.

[0032] Furthermore, while the exemplary embodiments illustrated herein show the various components of the system collocated, it is to be appreciated that the various components of the system can be located at distant portions of a distributed network, such as a telecommunications network and/or the Internet, or within a

dedicated secure, unsecured and/or encrypted system. Thus, it should be appreciated that the components of the system can be combined into one or more devices, such as a modem, or collocated on a particular node of a distributed network, such as a telecommunications network. As will be appreciated from the following description, and for reasons of computational efficiency, the components of the system can be arranged at any location within a distributed network without affecting the operation of the system. For example, the various components can be located in a Central Office modem (CO, ATU-C, VTU-O), a Customer Premises modem (CPE, ATU-R, VTU-R), a DSL management device, or some combination thereof. Similarly, one or more functional portions of the system could be distributed between a modem and an associated computing device.

[0033] Furthermore, it should be appreciated that the various links, including communications channel 5, connecting the elements can be wired or wireless links, or any combination thereof, or any other known or later developed element(s) that is capable of supplying and/or communicating data to and from the connected elements. The term module as used herein can refer to any known or later developed hardware, software, firmware, or combination thereof that is capable of performing the functionality associated with that element. The terms determine, calculate and compute, and variations thereof, as used herein are used interchangeably and include any type of methodology, process, mathematical operation or technique. FCI block and latency path are used interchangeably herein as well as transmitting modem and transmitting transceiver. Receiving modem and receiving transceiver are also used interchangeably.

[0034] Fig. 1 illustrates an exemplary embodiment of a transceiver 100 that utilizes shared resources. It should be appreciated that numerous functional components of the transceiver have been omitted for clarity. However, the transceiver 100 can also include the standard components found in typical communications device(s) in which the technology of the subject invention is implemented into.

[0035] According to an exemplary embodiment of the invention, memory and processing power can be shared among a plurality of transmitter and/or receiver latency paths, in a communications transceiver that carries or supports multiple applications. For example, the transmitter and/or receiver latency paths of the transceiver can share an interleaver/deinterleaver memory and the shared memory can be allocated to the interleaver and/or deinterleaver of each latency path. This allocation can be done based on the data rate, latency, BER, impulse noise protection requirements of the application, data or information being transported over each latency path, or in general any parameter associated with the communications system.

[0036] Likewise, for example, the transmitter and/or receiver latency paths can share a Reed-Solomon coder/decoder processing module and the processing power of this module can be allocated to each encoder and/or decoder. This allocation can be done based on the data rate/latency, BER, impulse noise protection requirements of the application data or information being transported over each latency path, or in general based on any parameter associated with the communication system.

[0037] In accordance with an exemplary operational embodiment, a first transceiver and a second transceiver transmit to one another messages during, for example, initialization which contain information on the total and/or shared memory capabilities of each transceiver and optionally information about the one or more latency paths. This information can be transmitted prior to determining how to configure the latency paths to support the application requirements. Based on this information, one of the modems can select an FCI configuration parameter(s) that meets the transmission requirements of each application being transported over each latency paths. While an exemplary of the embodiment of the invention will be described in relation to the operation of the invention and characteristics thereof being established during initialization, it should be appreciated that the sharing of resources can be modified and messages transmitted between a two transceivers at any time during initialization and/or user data transmission, i.e., SHOWTIME.

[0038] Fig. 1 illustrates an exemplary embodiment of a transceiver 100. The transceiver 100 includes a transmitter portion 200 and a receiver portion 300. The transmitter portion 200 includes one or more latency paths 210, 220, ... Similarly, the receiver portion 300 includes one or more latency paths 310, 320, ... Each of the latency paths in the transmitter portion 200 includes a framer, coder, and interleaver designated as 212, 214, 216 and 222, 224 and 226, respectively. Each of the latency paths in the receiver portion includes a deframer, decoder, and deinterleaver designated as 312, 314, 316 and 322, 324, and 326, respectively. The transceiver 100 further includes a shared processing module 110, a shared memory 120, a parameter determination module 130, a path module 140, an allocation module 150, and a shared

resource management module 160, all interconnected by one or more links (not shown).

[0039] In this exemplary embodiment, the transceiver 100 is illustrated with four total transmitter portion and receiver portion latency paths, i.e., 210, 220, 310, and 320. The shared memory 120 is shared amongst the two transmitter portion interleavers 216 and 226 and two receiver portion deinterleavers 316 and 326. The shared processing module 110, such as a shared coding module, is shared between the two transmitter portion coders 214 and 224 and the two receiver portion decoders 314 and 324.

[0040] While the exemplary embodiment of the invention will be described in relation to a transceiver having a number of transmitter portion latency paths and receiver portion latency paths, it should be appreciated that this invention can be applied to any transceiver having any number of latency paths. Moreover, it should be appreciated that the sharing of resources can be allocated such that one or more of the transmitter portion latency paths are sharing a shared resource, one or more of the receiver portion latency paths are sharing a shared resource, or a portion of the transmitter portion latency paths and a portion of the receiver portion latency paths are sharing shared resources. Moreover, any one or more of the latency paths, or portions thereof, could also be assigned to a fixed resource while, for example, another portion of the latency path(s) assigned to a shared resource. For example, in latency path 210, the interleaver 216 could be allocated a portion of the shared memory 120, while the coder 214 could be allocated to a dedicated processing

module, vice versa, or the like.

[0041] In accordance with the exemplary embodiment, a plurality of transmitter portion or receiver portion latency paths share an interleaver/deinterleaver memory, such as shared memory 120, and a coding module, such as shared processing module 110. For example, the interleaver/deinterleaver memory can be allocated to different interleavers and/or deinterleavers. This allocation can be based on parameters associated with the communication systems such as data rate, latency, BER, impulse noise protection, and the like, of the applications being transported. Similarly, a coding module, which can be a portion of the shared processing module 110, can be shared between any one or more of the latency paths. This sharing can be based on requirements such as data rate, latency, BER, impulse noise protection, and the like, of the applications being transported.

[0042] For example, an exemplary transceiver could comprise a shared interleaver/deinterleaver memory and could be designed to allocate a first portion of the shared memory 120 to an interleaver, such as interleaver 216 in the transmitter portion of the transceiver and allocate a second portion of the shared memory 120 to a deinterleaver, such as 316, in the receiver portion of the transceiver.

[0043] Alternatively, for example, an exemplary transceiver can comprise a shared interleaver/deinterleaver memory, such as shared memory 120, and be designed to allocate a first portion of shared memory 120 to a first interleaver, e.g., 216, in the transmitter portion of the transceiver and allocate a second portion of the

shared memory to a second interleaver, e.g., 226, in the transmitter portion of the transceiver.

[0044] Alternatively, for example, an exemplary transceiver can comprise a shared interleaver/deinterleaver memory and be designed to allocate a first portion of the shared memory 120 to a first deinterleaver, e.g., 316, in the receiver portion of the transceiver and allocate a second portion of the shared memory to a second deinterleaver, e.g., 326, in the receiver portion of the transceiver. Regardless of the configuration, in general any interleaver or deinterleaver, or grouping thereof, be it in a transmitter portion or receiver portion of the transceiver, can be associated with a portion of the shared memory 120.

[0045] Establishment, configuration and usage of shared resources is performed in the following exemplary manner. First, and in cooperation with the path module 140, the number of transmitter and receiver latency paths (N) is determined. The parameter determination module 130 then analyses one or more parameters such as data rate, transmitter data rate, receiver data rate, impulse noise protection, bit error rate, latency, or the like. Based on one or more of these parameters, the allocation module 150 allocates a portion of the shared memory 120 to one or more of the interleaver and/or deinterleavers, or groupings thereof. This process continues until the memory allocation has been determined and assigned to each of the N latency paths.

[0046] Having determined the memory allocation for each of the latency paths,

and in conjunction with the shared resource management 160, the transceiver 100 transmits to a second transceiver one or more of the number of latency paths (N), the maximum interleaver memory for any one or more of the latency paths and/or the maximum total and/or shared memory for all of the latency paths.

[0047] Three examples of sharing interleaver/deinterleaver memory and coding processing in a transceiver are described below. The latency paths in these examples can be in the transmitter portion of the transceiver or the receiver portion of the transceiver.

[0048] Example #1

A first transmitter portion or receiver portion latency path may carry data from a video application, which needs a very low BER but can tolerate higher latency. In this case, the video will be transported using an latency path that has a large amount of interleaving/deinterleaving and coding (also known as Forward Error Correction (FEC) coding). For example, the latency path may be configured with Reed-Solomon coding using a codeword size of 255 bytes ($N=255$) with 16 checkbytes ($R=16$) and interleaving/deinterleaving using an interleaver depth of 64 ($D=64$). This latency path will require $N*D=255*64=16\text{Kbytes}$ of interleaver memory at the transmitter (or de-interleaver memory at the receiver). This latency path will be able to correct a burst of errors that is less than 512 bytes in duration.

[0049] A second transmitter portion or receiver portion latency path may carry an internet access application that requires a medium BER and a medium amount of

latency. In this case, the internet access application will be transported using a latency path that has a medium amount of interleaving and coding. For example, the latency path may be configured with Reed-Solomon coding using a codeword size of 128 bytes ($N=128$) with 8 checkbytes ($R=8$) and interleaving using an interleaver depth of 16 ($D=32$). This latency path will require $N*D=128*32=4\text{Kbytes}$ of interleaver memory and the same amount of deinterleaver memory. This latency path will be able to correct a burst of errors that is less than 128 bytes in duration.

[0050] A third transmitter portion or receiver portion latency path may carry a voice telephony application, which needs a very low latency but can tolerate BER. In this case, the video will be transported using an latency path that has a large amount of interleaving and coding. For example, the third transmitter portion or receiver portion latency path may be configured with no interleaving or coding which will result in the lowest possible latency through the latency path but will provide no error correction capability.

[0051] According to the principles of this invention, a system carrying the three applications described above in Example #1, would have three latency paths that share one memory space containing at least $(16+4)=20\text{ Kbytes}$. The three latency paths also share a common coding block that is able to simultaneously encode (in the transmitter portion) or decode (in a receiver portion) two codewords with $N=255/R=16$ and $N=128/R=8$.

[0052] According to an exemplary embodiment of this invention, the latency

paths can be reconfigured at initialization or during data transmission mode (also known as SHOWTIME in ADSL and VDSL transceivers). This would occur if, for example, the applications or application requirements were to change.

[0053] Example #2

If instead of 1 video application, 1 internet application and 1 voice application, there were 3 internet access applications then the transmitter portion and/or receiver portion latency paths would be reconfigured to utilize the shared memory and coding module in a different way. For example, the system could be reconfigured to have 3 transmitter portion or receiver portion latency paths, with each latency path being configured with Reed-Solomon coding using a codeword size of 128 bytes ($N=128$) with 8 checkbytes ($R=8$) and interleaving using an interleaver depth of 16 ($D=32$). Each latency path will require $N*D=128*32=4\text{Kbytes}$ of interleaver memory and each block will be able to correct a burst of errors that is less than 128 bytes in duration. Based on the example of carrying the three internet access applications described, the three latency path share one memory space containing at least $3*4=12\text{ Kbytes}$. Also the three latency paths share a common coding block that is able to simultaneously encode (on the transmitter side) or decode (on the receiver side) three codewords with $N=128/R=16$, $N=128/R=8$ and $N=128/R=8$.

[0054] Example #3

The system could be configured to carry yet another set of applications. For example, the latency paths could be configured to carry 2 video applications. In this case only 2 transmitter portion or receiver portion latency paths are needed, which means that

the third latency path could be simply disabled. Also, assuming that the memory is constrained based on the first example above, then the maximum shared memory for these 2 latency paths is 20 kBytes. In this case, the system could be reconfigured to have 2 latency paths, with each block being configured with Reed-Solomon coding using a codeword size of 200 bytes ($N=200$) with 10 checkbytes ($R=10$) and interleaving/deinterleaving using an interleaver depth of 50 ($D=50$). Each latency path will require $N*D=200*50=10\text{Kbytes}$ of interleaver memory and each block will be able to correct a burst of errors that is less than 250 bytes in duration. This configuration results in 20K of shared memory for both latency paths, which is the same as in the first example. In order to stay within the memory constraints of the latency paths, the error correction capability for each latency path is decreased to 250 bytes from 512 bytes in Example #1.

[0055] Another aspect of this invention is the how FCI configuration information is transmitted between a first modem and a second modem. FCI configuration information will depend on the requirements of the applications being transported over the DSL connection. This information may need to be forwarded during initialization in order to initially configure the DSL connection. This information may also need to be forwarded during SHOWTIME in order to reconfigure the DSL connection based on a change in applications or the application requirements.

[0056] According to one embodiment, a first modem determines the specific FCI configuration parameters, e.g., N , D , R as defined above, needed to meet specific application requirements, such as latency, burst error correction capability, etc. In

order to determine the FCI configuration parameters, the first modem must know what are the capabilities of a second modem. For example, the first modem must know how many latency paths (FCI blocks) the second modem can support. Also the first modem must know the maximum amount of interleaver memory for each transmitter latency path. In addition, since the transmitter latency paths may share a common memory space the first modem must know the total shared memory for all transmitter latency paths. This way the first modem will be able to choose a configuration that can meet application requirements and also meet the transmitter portion latency path capabilities of the second modem.

[0057] For example, using values from examples above, a first transceiver could send a message to a second transceiver during initialization or during SHOWTIME containing the following information:

- Number of supported transmitter and receiver latency paths = 3
- Max Interleaver Memory for latency path #1= 16 Kbytes
- Max Interleaver Memory for latency path #2= 16 Kbytes
- Max Interleaver Memory for latency path #3= 16 Kbytes
- Maximum total/shared memory for all latency paths = 20 kBytes

Based on this information, and the application requirements, the first transceiver would select latency path settings. For example, if the applications are 1 video, 1 internet access and 1 voice application, the first transceiver could configure 3 latency paths as follows:

latency path #1 – Video: N=255, R=16, D=64

latency path #2 – Video: N=128, R=8, D=32

latency path #3 – Video: $N=0$, $R=0$, $D=1$ (no coding or interleaving)

[0058] This would result in a total interleaver memory of 20 kbytes.

[0059] Alternatively, if for example, there are only 2 video applications, the first transceiver could configure 2 latency paths as follows:

latency path #1 – Video: $N=200$, $R=10$, $D=50$

latency path #2 – Video: $N=200$, $R=10$, $D=50$

latency path #3 – Video: $N=0$, $R=0$, $D=1$ (no coding or interleaving)

[0060] This would also result in a total interleaver memory of 20 kbytes.

[0061] Alternatively, the second transceiver can determine the specific FCI configuration parameters, e.g., N , D , R as defined above, needed to meet specific application requirements, such as latency, burst error correction capability, etc. As described above for the first transceiver, in order to determine the FCI configuration parameters, the second transceiver must first know what are the capabilities of the first transceiver. In this case, the first transceiver would send a message to the second transceiver containing the information described above and based on this information and the application requirements the second transceiver would select latency path settings.

[0062] Fig. 2 outlines an exemplary method of allocating shared memory in a transceiver. More specifically, control begins in step S200 and continues to step

S210. In step S210, one or more of shared interleaver/deinterleaver memory and/or shared coder/decoder processing resources are allocated to one or more latency paths, in a transceiver. Control then continues to step S220 where the control sequence ends.

[0063] Fig. 3 outlines an exemplary method of exchanging shared resource allocations according to an exemplary embodiment of this invention. In particular, control begins in step S310. In step S310, a maximum amount of shared memory that can be allocated to a specific interleaver or deinterleaver of a plurality of interleavers or deinterleavers in a transceiver is determined. Next, in step S320, the determined maximum amount for one or more of the deinterleavers and/or interleavers is transmitted to another transceiver. Messages containing additional information can also be transmitted to the other transceiver and/or received from the other transceiver. Control then continues to step S330 where the control sequence ends.

[0064] Fig. 4 outlines an exemplary procedure for resource sharing according to an exemplary embodiment of this invention. In particular, control begins in step S400 and continues to step S410. In step S410, the number of latency paths are determined. Then, in step S420, the latency path information (FCI block information) is transmitted to another transceiver. Messages containing additional information can also be transmitted to the other transceiver and/or received from the other transceiver. This information can be used to, for example, assist with the determination of memory allocation in the transceiver. Moreover, the messages received from the other transceiver could specify what the memory allocation is to be based on, for

example, the number of latency paths, memory allocation in the remote transceiver and required applications. Control then continues to step S430.

[0065] In step S430, and for each latency path, the steps in step 440 are performed.

[0066] In step S440, and while monitoring of allocation of resources is being performed, steps 450 and 460 are performed. More specifically, in step S450, one or more parameters associated with the communication system are determined. Then, in step S460, shared resources are allocated based on one or more of the communication parameters. Control then continues to step S470.

[0067] In step S470, the allocation of shared resources is communicated to another transceiver. Next, in step S480, a determination is made as to whether there is a change in communications that would require the adjustment of the shared resource allocation. Examples of changes in communications conditions include a change in applications being transported over the system and/or changes in the channel condition, etc. If adjustments are required, control jumps back to step S410. Otherwise, control jumps to step S490 where the control sequence ends.

[0068] The above-described system can be implemented on wired and/or wireless telecommunications devices, such a modem, a multicarrier modem, a DSL modem, an ADSL modem, an XDSL modem, a VDSL modem, a linecard, test equipment, a multicarrier transceiver, a wired and/or wireless wide/local area network system, a

satellite communication system, a modem equipped with diagnostic capabilities, or the like, or on a separate programmed general purpose computer having a communications device or in conjunction with any of the following communications protocols: CDSL, ADSL2, ADSL2+, VDSL1, VDSL2, HDSL, DSL Lite, IDSL, RADSL, SDSL, UDSL or the like.

[0069] Additionally, the systems, methods and protocols of this invention can be implemented on a special purpose computer, a programmed microprocessor or microcontroller and peripheral integrated circuit element(s), an ASIC or other integrated circuit, a digital signal processor, a hard-wired electronic or logic circuit such as discrete element circuit, a programmable logic device such as PLD, PLA, FPGA, PAL, a modem, a transmitter/receiver, any comparable means, or the like. In general, any device capable of implementing a state machine that is in turn capable of implementing the methodology illustrated herein can be used to implement the various communication methods, protocols and techniques according to this invention.

[0070] Furthermore, the disclosed methods may be readily implemented in software using object or object-oriented software development environments that provide portable source code that can be used on a variety of computer or workstation platforms. Alternatively, the disclosed system may be implemented partially or fully in hardware using standard logic circuits or VLSI design. Whether software or hardware is used to implement the systems in accordance with this invention is dependent on the speed and/or efficiency requirements of the system, the particular

function, and the particular software or hardware systems or microprocessor or microcomputer systems being utilized. The communication systems, methods and protocols illustrated herein can be readily implemented in hardware and/or software using any known or later developed systems or structures, devices and/or software by those of ordinary skill in the applicable art from the functional description provided herein and with a general basic knowledge of the computer and telecommunications arts.

[0071] Moreover, the disclosed methods may be readily implemented in software that can be stored on a storage medium, executed on programmed general-purpose computer with the cooperation of a controller and memory, a special purpose computer, a microprocessor, or the like. In these instances, the systems and methods of this invention can be implemented as program embedded on personal computer such as an applet, JAVA® or CGI script, as a resource residing on a server or computer workstation, as a routine embedded in a dedicated communication system or system component, or the like. The system can also be implemented by physically incorporating the system and/or method into a software and/or hardware system, such as the hardware and software systems of a communications transceiver.

[0072] It is therefore apparent that there has been provided, in accordance with the present invention, systems and methods for sharing resources. While this invention has been described in conjunction with a number of embodiments, it is evident that many alternatives, modifications and variations would be or are apparent to those of ordinary skill in the applicable arts. Accordingly, it is intended to embrace

all such alternatives, modifications, equivalents and variations that are within the spirit and scope of this invention.

ABSTRACT

A transceiver is designed to share memory and processing power amongst a plurality of transmitter and/or receiver latency paths, in a communications transceiver that carries or supports multiple applications. For example, the transmitter and/or receiver latency paths of the transceiver can share an interleaver/deinterleaver memory. This allocation can be done based on the data rate, latency, BER, impulse noise protection requirements of the application, data or information being transported over each latency path, or in general any parameter associated with the communications system.

Electronic Patent Application Fee Transmittal				
Application Number:				
Filing Date:				
Title of Invention:		Resource Sharing in a Telecommunications Environment		
First Named Inventor/Applicant Name:		Marcos C. Tzannes		
Filer:		Jason Vick/Joanne Vos		
Attorney Docket Number:		5550-54-CON-3		
Filed as Large Entity				
Utility under 35 USC 111(a) Filing Fees				
Description	Fee Code	Quantity	Amount	Sub-Total in USD(\$)
Basic Filing:				
Utility application filing	1011	1	330	330
Utility Search Fee	1111	1	540	540
Utility Examination Fee	1311	1	220	220
Pages:				
Claims:				
Miscellaneous-Filing:				
Petition:				
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Post-Allowance-and-Post-Issuance:				
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Electronic Acknowledgement Receipt	
EFS ID:	8598221
Application Number:	12901699
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First Named Inventor/Applicant Name:	Marcos C. Tzannes
Customer Number:	62574
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File Listing:					
Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1	Application Data Sheet	ADS.pdf	1031615 2b02ad33a517a02178dc37ecf96c88aef36c b3f9	no	5
Warnings:					
Information:					
2	Oath or Declaration filed	Executed_Declaration.pdf	68832 4fa5f993a03ce1c0d956f3ab0fb15a94c333aef 874a5	no	1
Warnings:					
Information:					
3		AMEND_PRELIM_01.pdf	433308 a2c1779933f7331aa5413b712e300031a8311 0b66	yes	6
	Multipart Description/PDF files in .zip description				
	Document Description		Start	End	
	Preliminary Amendment		1	1	
	Specification		2	3	
	Claims		4	5	
	Applicant Arguments/Remarks Made in an Amendment		6	6	
Warnings:					
Information:					
4		Specification.pdf	158115 a232204b8c9c4ab5c3df572626f3ca8320a 7040	yes	30
	Multipart Description/PDF files in .zip description				
	Document Description		Start	End	
	Specification		1	23	
	Claims		24	29	
	Abstract		30	30	
Warnings:					

Information:					
5	Drawings-only black and white line drawings	Figures_Final.pdf	29302	no	3
			914c85d0fbc1b8cf5e5fcc337a8b9948b61d99f		
Warnings:					
Information:					
6		Substitute_Spec_Marked_Up_Verson.pdf	150768	yes	24
			a9d567efb03cc7b118092eb1f94115c182158697		
	Multipart Description/PDF files in .zip description				
	Document Description		Start	End	
	Specification		1	23	
	Abstract		24	24	
Warnings:					
Information:					
7		Substitute_Spec_Clean_Verson.pdf	148644	yes	24
			6c69e1138b3cfe19fbb0cb18256e8afda382960		
	Multipart Description/PDF files in .zip description				
	Document Description		Start	End	
	Specification		1	23	
	Abstract		24	24	
Warnings:					
Information:					
8	Fee Worksheet (PTO-875)	fee-info.pdf	32502	no	2
			21744b0b76a94f51444d007cc56008ae270cad73c		
Warnings:					
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If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.

New International Application Filed with the USPTO as a Receiving Office

If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.

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File Listing:					
Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1	Application Data Sheet	ADS.pdf	1031615 2b02ad33a517a02178dc37ecf96c88aef36c b3f9	no	5
Warnings:					
Information:					
2	Oath or Declaration filed	Executed_Declaration.pdf	68832 4fa55931a03ee1c6095613ab7b15a94c333aef 874a5	no	1
Warnings:					
Information:					
3		AMEND_PRELIM_01.pdf	433308 a2c1779933f7331aa5413b712e300031a8311 0b66	yes	6
	Multipart Description/PDF files in .zip description				
	Document Description	Start	End		
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Warnings:					
Information:					
4		Specification.pdf	158115 a232204b8c9c4ab5c3df572626f3ca8320a 7040	yes	30
	Multipart Description/PDF files in .zip description				
	Document Description	Start	End		
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			914c8c5d7bce1b8cf5e5fcc337a8b9948b61d997		
Warnings:					
Information:					
6		Substitute_Spec_Marked_Up_Verson.pdf	150768	yes	24
			aad567efb03cc7b118092eb1f94115c182158e97		
	Multipart Description/PDF files in .zip description				
	Document Description		Start	End	
	Specification		1	23	
	Abstract		24	24	
Warnings:					
Information:					
7		Substitute_Spec_Clean_Verson.pdf	148644	yes	24
			6c69e1138b3cfe19fbb0cb18256e8afda382960		
	Multipart Description/PDF files in .zip description				
	Document Description		Start	End	
	Specification		1	23	
	Abstract		24	24	
Warnings:					
Information:					
8	Fee Worksheet (PTO-875)	fee-info.pdf	32502	no	2
			21744b0b76a94f51444d007cc56008ae270cad73c		
Warnings:					
Information:					
Total Files Size (in bytes):			2053086		

This Acknowledgement Receipt evidences receipt on the noted date by the USPTO of the indicated documents, characterized by the applicant, and including page counts, where applicable. It serves as evidence of receipt similar to a Post Card, as described in MPEP 503.

New Applications Under 35 U.S.C. 111

If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application.

National Stage of an International Application under 35 U.S.C. 371

If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.

New International Application Filed with the USPTO as a Receiving Office

If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.

Application Data Sheet 37 CFR 1.76		Attorney Docket Number	5550-54-CON-3
		Application Number	
Title of Invention	RESOURCE SHARING IN A TELECOMMUNICATIONS ENVIRONMENT		
The application data sheet is part of the provisional or nonprovisional application for which it is being submitted. The following form contains the bibliographic data arranged in a format specified by the United States Patent and Trademark Office as outlined in 37 CFR 1.76. This document may be completed electronically and submitted to the Office in electronic format using the Electronic Filing System (EFS) or the document may be printed and included in a paper filed application.			

Secrecy Order 37 CFR 5.2

☐ Portions or all of the application associated with this Application Data Sheet may fall under a Secrecy Order pursuant to 37 CFR 5.2. (Paper filers only. Applications that fall under Secrecy Order may not be filed electronically.)

Applicant Information:

Applicant 1						Remove
Applicant Authority ☒ Inventor ☐ Legal Representative under 35 U.S.C. 117 ☐ Party of Interest under 35 U.S.C. 118						
Prefix	Given Name	Middle Name	Family Name	Suffix		
	Marcos	C.	Tzannes			
Residence Information (Select One) ☒ US Residency ☐ Non US Residency ☐ Active US Military Service						
City	Orinda	State/Province	CA	Country of Residence i	US	
Citizenship under 37 CFR 1.41(b) i US						
Mailing Address of Applicant:						
Address 1		121 La Espiral				
Address 2						
City	Orinda	State/Province	CA			
Postal Code	94563	Country i	US			
Applicant 2						Remove
Applicant Authority ☒ Inventor ☐ Legal Representative under 35 U.S.C. 117 ☐ Party of Interest under 35 U.S.C. 118						
Prefix	Given Name	Middle Name	Family Name	Suffix		
	Michael		Lund			
Residence Information (Select One) ☒ US Residency ☐ Non US Residency ☐ Active US Military Service						
City	West Newton	State/Province	MA	Country of Residence i	US	
Citizenship under 37 CFR 1.41(b) i US						
Mailing Address of Applicant:						
Address 1		110 Prospect Street				
Address 2						
City	West Newton	State/Province	MA			
Postal Code	02465	Country i	US			
All Inventors Must Be Listed - Additional Inventor Information blocks may be generated within this form by selecting the Add button.						Add

Correspondence Information:

Enter either Customer Number or complete the Correspondence Information section below.
For further information see 37 CFR 1.33(a).

☐ An Address is being provided for the correspondence information of this application.

Application Data Sheet 37 CFR 1.76		Attorney Docket Number	5550-54-CON-3
		Application Number	
Title of Invention	RESOURCE SHARING IN A TELECOMMUNICATIONS ENVIRONMENT		
Customer Number	62574		
Email Address	jvick@sheridanross.com	Add Email	Remove Email

Application Information:

Title of the Invention	RESOURCE SHARING IN A TELECOMMUNICATIONS ENVIRONMENT		
Attorney Docket Number	5550-54-CON-3	Small Entity Status Claimed	☐
Application Type	Nonprovisional		
Subject Matter	Utility		
Suggested Class (if any)		Sub Class (if any)	
Suggested Technology Center (if any)			
Total Number of Drawing Sheets (if any)	3	Suggested Figure for Publication (if any)	

Publication Information:

☐ Request Early Publication (Fee required at time of Request 37 CFR 1.219)

☐ **Request Not to Publish.** I hereby request that the attached application not be published under 35 U.S.C. 122(b) and certify that the invention disclosed in the attached application **has not and will not** be the subject of an application filed in another country, or under a multilateral international agreement, that requires publication at eighteen months after filing.

Representative Information:

Representative information should be provided for all practitioners having a power of attorney in the application. Providing this information in the Application Data Sheet does not constitute a power of attorney in the application (see 37 CFR 1.32). Enter either Customer Number or complete the Representative Name section below. If both sections are completed the Customer Number will be used for the Representative Information during processing.

Please Select One:	☒ Customer Number	☐ US Patent Practitioner	☐ Limited Recognition (37 CFR 11.9)
Customer Number	62574		

Domestic Benefit/National Stage Information:

This section allows for the applicant to either claim benefit under 35 U.S.C. 119(e), 120, 121, or 365(c) or indicate National Stage entry from a PCT application. Providing this information in the application data sheet constitutes the specific reference required by 35 U.S.C. 119(e) or 120, and 37 CFR 1.78(a)(2) or CFR 1.78(a)(4), and need not otherwise be made part of the specification.

Prior Application Status	Pending	Remove	
Application Number	Continuity Type	Prior Application Number	Filing Date (YYYY-MM-DD)
	Continuation of	12/761586	2010-04-16
Prior Application Status	Pending	Remove	
Application Number	Continuity Type	Prior Application Number	Filing Date (YYYY-MM-DD)
12/761586	Continuation of	11/246163	2005-10-11

Application Data Sheet 37 CFR 1.76		Attorney Docket Number	5550-54-CON-3
		Application Number	
Title of Invention	RESOURCE SHARING IN A TELECOMMUNICATIONS ENVIRONMENT		

Prior Application Status	Expired	Remove	
Application Number	Continuity Type	Prior Application Number	Filing Date (YYYY-MM-DD)
11/246163	non provisional of	60/618269	2004-10-12
Additional Domestic Benefit/National Stage Data may be generated within this form by selecting the Add button.			Add

Foreign Priority Information:

This section allows for the applicant to claim benefit of foreign priority and to identify any prior foreign application for which priority is not claimed. Providing this information in the application data sheet constitutes the claim for priority as required by 35 U.S.C. 119(b) and 37 CFR 1.55(a).			
			Remove
Application Number	Country ⁱ	Parent Filing Date (YYYY-MM-DD)	Priority Claimed
			☐ Yes ☒ No
Additional Foreign Priority Data may be generated within this form by selecting the Add button.			Add

Assignee Information:

Providing this information in the application data sheet does not substitute for compliance with any requirement of part 3 of Title 37 of the CFR to have an assignment recorded in the Office.			
			Remove
Assignee 1			
If the Assignee is an Organization check here. ☒			
Organization Name	AWARE, INC.		
Mailing Address Information:			
Address 1	40 Middlesex Turnpike		
Address 2			
City	Bedford	State/Province	MA
Country ⁱ	US	Postal Code	01730
Phone Number		Fax Number	
Email Address			
Additional Assignee Data may be generated within this form by selecting the Add button.			Add

Signature:

A signature of the applicant or representative is required in accordance with 37 CFR 1.33 and 10.18. Please see 37 CFR 1.4(d) for the form of the signature.					
Signature	/Jason H. Vick/			Date (YYYY-MM-DD)	2010-10-11
First Name	Jason H.	Last Name	Vick	Registration Number	45285

Application Data Sheet 37 CFR 1.76		Attorney Docket Number	5550-54-CON-3
		Application Number	
Title of Invention	RESOURCE SHARING IN A TELECOMMUNICATIONS ENVIRONMENT		

This collection of information is required by 37 CFR 1.76. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 23 minutes to complete, including gathering, preparing, and submitting the completed application data sheet form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

Privacy Act Statement

The Privacy Act of 1974 (P.L. 93-579) requires that you be given certain information in connection with your submission of the attached form related to a patent application or patent. Accordingly, pursuant to the requirements of the Act, please be advised that: (1) the general authority for the collection of this information is 35 U.S.C. 2(b)(2); (2) furnishing of the information solicited is voluntary; and (3) the principal purpose for which the information is used by the U.S. Patent and Trademark Office is to process and/or examine your submission related to a patent application or patent. If you do not furnish the requested information, the U.S. Patent and Trademark Office may not be able to process and/or examine your submission, which may result in termination of proceedings or abandonment of the application or expiration of the patent.

The information provided by you in this form will be subject to the following routine uses:

1. The information on this form will be treated confidentially to the extent allowed under the Freedom of Information Act (5 U.S.C. 552) and the Privacy Act (5 U.S.C. 552a). Records from this system of records may be disclosed to the Department of Justice to determine whether the Freedom of Information Act requires disclosure of these records.
2. A record from this system of records may be disclosed, as a routine use, in the course of presenting evidence to a court, magistrate, or administrative tribunal, including disclosures to opposing counsel in the course of settlement negotiations.
3. A record in this system of records may be disclosed, as a routine use, to a Member of Congress submitting a request involving an individual, to whom the record pertains, when the individual has requested assistance from the Member with respect to the subject matter of the record.
4. A record in this system of records may be disclosed, as a routine use, to a contractor of the Agency having need for the information in order to perform a contract. Recipients of information shall be required to comply with the requirements of the Privacy Act of 1974, as amended, pursuant to 5 U.S.C. 552a(m).
5. A record related to an International Application filed under the Patent Cooperation Treaty in this system of records may be disclosed, as a routine use, to the International Bureau of the World Intellectual Property Organization, pursuant to the Patent Cooperation Treaty.
6. A record in this system of records may be disclosed, as a routine use, to another federal agency for purposes of National Security review (35 U.S.C. 181) and for review pursuant to the Atomic Energy Act (42 U.S.C. 218(c)).
7. A record from this system of records may be disclosed, as a routine use, to the Administrator, General Services, or his/her designee, during an inspection of records conducted by GSA as part of that agency's responsibility to recommend improvements in records management practices and programs, under authority of 44 U.S.C. 2904 and 2906. Such disclosure shall be made in accordance with the GSA regulations governing inspection of records for this purpose, and any other relevant (i.e., GSA or Commerce) directive. Such disclosure shall not be used to make determinations about individuals.
8. A record from this system of records may be disclosed, as a routine use, to the public after either publication of the application pursuant to 35 U.S.C. 122(b) or issuance of a patent pursuant to 35 U.S.C. 151. Further, a record may be disclosed, subject to the limitations of 37 CFR 1.14, as a routine use, to the public if the record was filed in an application which became abandoned or in which the proceedings were terminated and which application is referenced by either a published application, an application open to public inspections or an issued patent.
9. A record from this system of records may be disclosed, as a routine use, to a Federal, State, or local law enforcement agency, if the USPTO becomes aware of a violation or potential violation of law or regulation.



PTO/SB01A (09-04)
 Approved for use through 07/31/2006 OMB 0651-0032
 U.S. Patent and Trademark Office, U.S. DEPARTMENT OF COMMERCE
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 Docket No. T3653-9285US01

DECLARATION (37 CFR 1.63) FOR UTILITY OR DESIGN APPLICATION USING AN APPLICATION DATA SHEET (37 CFR 1.76)

Title of
Invention

RESOURCE SHARING IN A TELECOMMUNICATIONS ENVIRONMENT

As the below named inventor(s), I/we declare that:

This declaration is directed to:

- ☐ The attached application, or
☒ Application No. 11/246,163, filed on October 11, 2005
☐ as amended on _____ (if applicable):

I/we believe that I/we am/are the original and first inventor(s) of the subject matter which is claimed and for which a patent is sought;

I/we have reviewed and understand the contents of the above-identified application, including the claims, as amended by any amendment specifically referred to above;

I/we acknowledge the duty to disclose to the United States Patent and Trademark Office all information known to me/us to be material to patentability as defined in 37 CFR 1.56, including for continuation-in-part applications, material information which became available between the filing date of the prior application and the national or PCT International filing date of the continuation-in-part application.

All statements made herein of my/own knowledge are true, all statements made herein on information and belief are believed to be true, and further that these statements were made with the knowledge that willful false statements and the like are punishable by fine or imprisonment, or both, under 18 U.S.C. 1001, and may jeopardize the validity of the application or any patent issuing thereon.

FULL NAME OF INVENTOR(S)

Inventor one: Marcos C. TZANNES

Signature: [Signature] Citizen of: U.S.A.

Inventor two: Michael LUND

Signature: [Signature] Citizen of: U.S.A.

Inventor three: _____

Signature: _____ Citizen of: _____

Inventor four: _____

Signature: _____ Citizen of: _____

☐ Additional inventors or a legal representative are being named on _____ additional form(s) attached hereto.

This collection of information is required by 37 U.S.C. 115 and 37 CFR 1.63. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.11 and 1.14. This collection is estimated to take 1 minute to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.

*AGE 2/5 * RCVD AT 1/5/2006 11:05:03 AM [Eastern Standard Time] * SVR: TYSOFAX/0 * DNIS: 9994 * CSID: 17816870430 * DURATION (mm:ss): 02:14

POWER OF ATTORNEY TO PROSECUTE APPLICATIONS BEFORE THE USPTO

I hereby revoke all previous powers of attorney given in the application identified in the attached statement under 37 CFR 3.73(b).

I hereby appoint:

☒ Practitioners associated with the Customer Number: 62574

OR

☐ Practitioner(s) named below (if more than ten patent practitioners are to be named, then a customer number must be used):

Name	Registration Number	Name	Registration Number

as attorney(s) or agent(s) to represent the undersigned before the United States Patent and Trademark Office (USPTO) in connection with any and all patent applications assigned only to the undersigned according to the USPTO assignment records or assignment documents attached to this form in accordance with 37 CFR 3.73(b).

Please change the correspondence address for the application identified in the attached statement under 37 CFR 3.73(b) to:

☒ The address associated with Customer Number: 62574

OR

☐ Firm or Individual Name			
Address			
City	State	Zip	
Country			
Telephone			Email

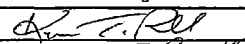
Assignee Name and Address:

AWARE, INC.
40 Middlesex Turnpike
Bedford, MA 07130-1423

A copy of this form, together with a statement under 37 CFR 3.73(b) (Form PTO/SB/96 or equivalent) is required to be filed in each application in which this form is used. The statement under 37 CFR 3.73(b) may be completed by one of the practitioners appointed in this form if the appointed practitioner is authorized to act on behalf of the assignee, and must identify the application in which this Power of Attorney is to be filed.

SIGNATURE of Assignee of Record

The individual whose signature and title is supplied below is authorized to act on behalf of the assignee

Signature		Date	11/8/09
Name	Kevin T. Russell	Telephone	781-657-8335
Title	V.P. General Counsel		

This collection of information is required by 37 CFR 1.31, 1.32 and 1.33. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 36 U.S.C. 122 and 37 CFR 1.11 and 1.14. This collection is estimated to take 3 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1460, Alexandria, VA 22313-1460. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. SEND TO: Commissioner for Patents, P.O. Box 1460, Alexandria, VA 22313-1460.

If you need assistance in completing the form, call 1-800-PTO-9199 and select option 2.

Electronic Acknowledgement Receipt	
EFS ID:	8598548
Application Number:	12901699
International Application Number:	
Confirmation Number:	1676
Title of Invention:	RESOURCE SHARING IN A TELECOMMUNICATIONS ENVIRONMENT
First Named Inventor/Applicant Name:	Marcos C. Tzannes
Customer Number:	62574
Filer:	Jason Vick/Joanne Vos
Filer Authorized By:	Jason Vick
Attorney Docket Number:	5550-54-CON-3
Receipt Date:	11-OCT-2010
Filing Date:	
Time Stamp:	14:33:59
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	no				
File Listing:					
Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1		Statement_under_373b_w_PO A.pdf	249478 d4129973f08c8162cb36fa70b4697c0dc274c c0f09	yes	2

Multipart Description/PDF files in .zip description		
Document Description	Start	End
Assignee showing of ownership per 37 CFR 3.73(b).	1	1
Power of Attorney	2	2

Warnings:

Information:

Total Files Size (in bytes):	249478

This Acknowledgement Receipt evidences receipt on the noted date by the USPTO of the indicated documents, characterized by the applicant, and including page counts, where applicable. It serves as evidence of receipt similar to a Post Card, as described in MPEP 503.

New Applications Under 35 U.S.C. 111
If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application.

National Stage of an International Application under 35 U.S.C. 371
If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.

New International Application Filed with the USPTO as a Receiving Office
If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.

STATEMENT UNDER 37 CFR 3.73(b)

Applicant/Patent Owner: AWARE, INC.

Application No./Patent No.: 12/901,699

Filed/Issue Date: October 11, 2010

Titled: RESOURCE SHARING IN A TELECOMMUNICATIONS ENVIRONMENT

AWARE, INC., a Corporation

(Name of Assignee)

(Type of Assignee, e.g., corporation, partnership, university, government agency, etc.)

states that it is:

1. ☒ the assignee of the entire right, title, and interest in;
2. ☐ an assignee of less than the entire right, title, and interest in
(The extent (by percentage) of its ownership interest is _____ %); or
3. ☐ the assignee of an undivided interest in the entirety of (a complete assignment from one of the joint inventors was made)

the patent application/patent identified above, by virtue of either:

A. ☒ An assignment from the inventor(s) of the patent application/patent identified above. The assignment was recorded in the United States Patent and Trademark Office at Reel 017438, Frame 0094, or for which a copy therefore is attached.

OR

B. ☐ A chain of title from the inventor(s), of the patent application/patent identified above, to the current assignee as follows:

1. From: _____ To: _____

The document was recorded in the United States Patent and Trademark Office at

Reel _____, Frame _____, or for which a copy thereof is attached.

2. From: _____ To: _____

The document was recorded in the United States Patent and Trademark Office at

Reel _____, Frame _____, or for which a copy thereof is attached.

3. From: _____ To: _____

The document was recorded in the United States Patent and Trademark Office at

Reel _____, Frame _____, or for which a copy thereof is attached.

☐ Additional documents in the chain of title are listed on a supplemental sheet(s).

☒ As required by 37 CFR 3.73(b)(1)(i), the documentary evidence of the chain of title from the original owner to the assignee was, or concurrently is being, submitted for recordation pursuant to 37 CFR 3.11.

[NOTE: A separate copy (i.e., a true copy of the original assignment document(s)) must be submitted to Assignment Division in accordance with 37 CFR Part 3, to record the assignment in the records of the USPTO. See MPEP 302.08]

The undersigned (whose title is supplied below) is authorized to act on behalf of the assignee.

Signature

11 OCT '10
Date

Jason H. Vick

Attorney for Assignee

Printed or Typed Name

Title

This collection of information is required by 37 CFR 3.73(b). The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.11 and 1.14. This collection is estimated to take 12 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.

If you need assistance in completing the form, call 1-800-PTO-9199 and select option 2.

Date: 10/11/10

Approved for use through 7/31/2006. OMB 0651-0032

U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE

Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it displays a valid OMB control number.

PATENT APPLICATION FEE DETERMINATION RECORD Substitute for Form PTO-875					Application or Docket Number 12/901,699	
APPLICATION AS FILED – PART I						
(Column 1)		(Column 2)		SMALL ENTITY		OR
FOR	NUMBER FILED	NUMBER EXTRA	RATE (\$)	FEE (\$)	RATE (\$)	FEE (\$)
BASIC FEE (37 CFR 1.16(a), (b), or (c))	N/A	N/A	N/A		N/A	330
SEARCH FEE (37 CFR 1.16(k), (l), or (m))	N/A	N/A	N/A		N/A	540
EXAMINATION FEE (37 CFR 1.16(o), (p), or (q))	N/A	N/A	N/A		N/A	220
1 (37 CFR 1.16(i))	8	minus 20 =	x\$26		x\$52	
INDEPENDENT CLAIMS (37 CFR 1.16(h))	2	minus 3 = *	x\$110		x\$220	
APPLICATION SIZE FEE (37 CFR 1.16(s))	If the specification and drawings exceed 100 sheets of paper, the application size fee due is \$270 (\$135 for small entity) for each additional 50 sheets or fraction thereof. See 35 U.S.C. 41(a)(1)(G) and 37 CFR					
MULTIPLE DEPENDENT CLAIM PRESENT (37 CFR 1.16(j))			195		390	
* If the difference in column 1 is less than zero, enter "0" in column 2.			TOTAL		TOTAL	1090
APPLICATION AS AMENDED – PART II						
(Column 1)		(Column 2)		(Column 3)		SMALL ENTITY
AMENDMENT A	CLAIMS REMAINING AFTER AMENDMENT	HIGHEST NUMBER PREVIOUSLY PAID FOR	PRESENT EXTRA	RATE (\$)	ADDITIONAL FEE (\$)	RATE (\$)
	Total (37 CFR 1.16(i))	Minus **	=	X =		X =
	Independent (37 CFR 1.16(h))	Minus ***	=	X =		X =
	Application Size Fee (37 CFR 1.16(s))					
	FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))			N/A		N/A
			TOTAL ADD'T FEE		TOTAL ADD'T FEE	
(Column 1)		(Column 2)		(Column 3)		SMALL ENTITY
AMENDMENT B	CLAIMS REMAINING AFTER AMENDMENT	HIGHEST NUMBER PREVIOUSLY PAID FOR	PRESENT EXTRA	RATE (\$)	ADDITIONAL FEE (\$)	RATE (\$)
	Total (37 CFR 1.16(i))	Minus **	=	X =		X =
	Independent (37 CFR 1.16(h))	Minus ***	=	X =		X =
	Application Size Fee (37 CFR 1.16(s))					
	FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))			N/A		N/A
			TOTAL ADD'T FEE		TOTAL ADD'T FEE	
* If the entry in column 1 is less than the entry in column 2, write "0" in column 3. ** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 20, enter "20". *** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 3, enter "3". The "Highest Number Previously Paid For" (Total or Independent) is the highest number found in the appropriate box in column 1.						

This collection of information is required by 37 CFR 1.16. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 12 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comment on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.

If you need assistance in completing the form, call 1-800-PTO-9199 and select option 2.

Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it displays a valid OMB control number.

PATENT APPLICATION FEE DETERMINATION RECORD Substitute for Form PTO-875					Application or Docket Number 12/901,699		Filing Date 10/11/2010		☐ To be Mailed	
APPLICATION AS FILED – PART I										
(Column 1)			(Column 2)		SMALL ENTITY ☐		OR		OTHER THAN SMALL ENTITY	
FOR	NUMBER FILED	NUMBER EXTRA	RATE (\$)	FEE (\$)			RATE (\$)	FEE (\$)		
☐ BASIC FEE (37 CFR 1.16(a), (b), or (c))	N/A	N/A	N/A				N/A			
☐ SEARCH FEE (37 CFR 1.16(k), (l), or (m))	N/A	N/A	N/A				N/A			
☐ EXAMINATION FEE (37 CFR 1.16(o), (p), or (q))	N/A	N/A	N/A				N/A			
TOTAL CLAIMS (37 CFR 1.16(j))	minus 20 =	*	X \$ =		OR		X \$ =			
INDEPENDENT CLAIMS (37 CFR 1.16(h))	minus 3 =	*	X \$ =				X \$ =			
☐ APPLICATION SIZE FEE (37 CFR 1.16(s))	If the specification and drawings exceed 100 sheets of paper, the application size fee due is \$250 (\$125 for small entity) for each additional 50 sheets or fraction thereof. See 35 U.S.C. 41(a)(1)(G) and 37 CFR 1.16(s).									
☐ MULTIPLE DEPENDENT CLAIM PRESENT (37 CFR 1.16(j))										
* If the difference in column 1 is less than zero, enter "0" in column 2.			TOTAL				TOTAL			
APPLICATION AS AMENDED – PART II										
(Column 1)			(Column 2)		(Column 3)		SMALL ENTITY		OR OTHER THAN SMALL ENTITY	
AMENDMENT	10/11/2010	CLAIMS REMAINING AFTER AMENDMENT		HIGHEST NUMBER PREVIOUSLY PAID FOR	PRESENT EXTRA	RATE (\$)	ADDITIONAL FEE (\$)		RATE (\$)	ADDITIONAL FEE (\$)
	Total (37 CFR 1.16(o))	* 8	Minus	** 20	= 0	X \$ =		OR	X \$52=	0
	Independent (37 CFR 1.16(h))	* 2	Minus	*** 3	= 0	X \$ =		OR	X \$220=	0
	☐ Application Size Fee (37 CFR 1.16(s))							OR		
	☐ FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))							OR		
						TOTAL ADD'L FEE		OR	TOTAL ADD'L FEE	0
AMENDMENT		CLAIMS REMAINING AFTER AMENDMENT		HIGHEST NUMBER PREVIOUSLY PAID FOR	PRESENT EXTRA	RATE (\$)	ADDITIONAL FEE (\$)		RATE (\$)	ADDITIONAL FEE (\$)
	Total (37 CFR 1.16(o))	*	Minus	**	=	X \$ =		OR	X \$ =	
	Independent (37 CFR 1.16(h))	*	Minus	***	=	X \$ =		OR	X \$ =	
	☐ Application Size Fee (37 CFR 1.16(s))							OR		
	☐ FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))							OR		
						TOTAL ADD'L FEE		OR	TOTAL ADD'L FEE	
* If the entry in column 1 is less than the entry in column 2, write "0" in column 3. ** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 20, enter "20". *** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 3, enter "3". The "Highest Number Previously Paid For" (Total or Independent) is the highest number found in the appropriate box in column 1.										

This collection of information is required by 37 CFR 1.16. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 12 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.
If you need assistance in completing the form, call 1-800-PTO-9199 and select option 2.