506432155 01/04/2021

PATENT ASSIGNMENT COVER SHEET

Electronic Version v1.1
Stylesheet Version v1.2

EPAS ID: PAT6478922

SUBMISSION TYPE:	NEW ASSIGNMENT
NATURE OF CONVEYANCE:	AMENDED AND RESTATED INTELLECTUAL PROPERTY SECURITY AGREEMENT

CONVEYING PARTY DATA

Name	Execution Date
TQ DELTA LLC	12/31/2020

RECEIVING PARTY DATA

Name:	ALTER DOMUS (US) LLC
Street Address:	225 W. WASHINGTON ST., 9TH FLOOR
City:	CHICAGO
State/Country:	ILLINOIS
Postal Code:	60606

PROPERTY NUMBERS Total: 227

Property Type	Number
Patent Number:	5497398
Patent Number:	5631610
Patent Number:	5636246
Patent Number:	5715280
Patent Number:	5751716
Patent Number:	5832030
Patent Number:	6445730
Patent Number:	6731695
Patent Number:	6748016
Patent Number:	6760373
Patent Number:	6801570
Patent Number:	6870888
Patent Number:	6961369
Patent Number:	7180938
Patent Number:	7292627
Patent Number:	7451379
Patent Number:	7453881
Patent Number:	7471721
Patent Number:	7558329
Patent Number:	7570686

Property Type	Number
Patent Number:	7636389
Patent Number:	7656976
Patent Number:	7697598
Patent Number:	7769104
Patent Number:	7796705
Patent Number:	7809028
Patent Number:	7831890
Patent Number:	7835430
Patent Number:	7836381
Patent Number:	7844882
Patent Number:	7889784
Patent Number:	7925958
Patent Number:	7978706
Patent Number:	7978753
Patent Number:	7979778
Patent Number:	8073041
Patent Number:	8090008
Patent Number:	8102909
Patent Number:	8218610
Patent Number:	8238412
Patent Number:	8276048
Patent Number:	8335271
Patent Number:	8335956
Patent Number:	8355427
Patent Number:	8374226
Patent Number:	8391191
Patent Number:	8407546
Patent Number:	8422511
Patent Number:	8432956
Patent Number:	8437382
Patent Number:	8462835
Patent Number:	8468411
Patent Number:	8495473
Patent Number:	8516337
Patent Number:	8594162
Patent Number:	8595577
Patent Number:	8607126
Patent Number:	8611404

Property Type	Number
Patent Number:	8625660
Patent Number:	8634449
Patent Number:	8645784
Patent Number:	8649305
Patent Number:	8718158
Patent Number:	8743931
Patent Number:	8743932
Patent Number:	8750352
Patent Number:	8782498
Patent Number:	8792574
Patent Number:	8793553
Patent Number:	8831031
Patent Number:	8837610
Patent Number:	8913649
Patent Number:	8929423
Patent Number:	8929470
Patent Number:	8937988
Patent Number:	8984366
Patent Number:	9014193
Patent Number:	9014243
Patent Number:	9065886
Patent Number:	9069718
Patent Number:	9094268
Patent Number:	9094348
Patent Number:	9154354
Patent Number:	9191039
Patent Number:	9264533
Patent Number:	9276612
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Patent Number:	9300324
Patent Number:	9300601
Patent Number:	9319512
Patent Number:	9479637
Patent Number:	9485055
Patent Number:	9485128
Patent Number:	9521003
Patent Number:	9547608
Patent Number:	9621198

Property Type	Number
Patent Number:	9749235
Patent Number:	9755876
Patent Number:	9838531
Patent Number:	9893921
Patent Number:	9894014
Patent Number:	9898220
Patent Number:	9973624
Patent Number:	10044473
Patent Number:	10049003
Patent Number:	10187240
Patent Number:	10264119
Patent Number:	10341261
Patent Number:	10346243
Patent Number:	10409510
Patent Number:	10419059
Patent Number:	10484140
Patent Number:	10498495
Patent Number:	10567112
Patent Number:	10579291
Patent Number:	10623559
Patent Number:	10708104
Patent Number:	10805040
Patent Number:	10833809
Application Number:	09768275
Application Number:	09836295
Application Number:	09882046
Application Number:	10175815
Application Number:	10202688
Application Number:	10597482
Application Number:	10631745
Application Number:	10743946
Application Number:	10778083
Application Number:	10802867
Application Number:	10834193
Application Number:	11058289
Application Number:	11090183
Application Number:	11140246
Application Number:	11200002

Property Type	Number
Application Number:	11242024
Application Number:	11289516
Application Number:	11430251
Application Number:	11434249
Application Number:	11616630
Application Number:	11748806
Application Number:	11972340
Application Number:	12383056
Application Number:	12478577
Application Number:	12615077
Application Number:	12640838
Application Number:	12783733
Application Number:	12783737
Application Number:	12783744
Application Number:	12783755
Application Number:	12783788
Application Number:	12783796
Application Number:	12783801
Application Number:	12783825
Application Number:	12783839
Application Number:	13330943
Application Number:	13467392
Application Number:	14285911
Application Number:	14485937
Application Number:	14577769
Application Number:	14724345
Application Number:	14757630
Application Number:	14865966
Application Number:	14932599
Application Number:	15054499
Application Number:	15077506
Application Number:	15084788
Application Number:	15180274
Application Number:	15298817
Application Number:	15304920
Application Number:	15479866
Application Number:	16428232
Application Number:	16544003

Property Type	Number
Application Number:	16561835
Application Number:	16569144
Application Number:	16781802
Application Number:	17027196
Application Number:	60072447
Application Number:	60090891
Application Number:	60109876
Application Number:	60144562
Application Number:	60164134
Application Number:	60172343
Application Number:	60174865
Application Number:	60177944
Application Number:	60197727
Application Number:	60212233
Application Number:	60224308
Application Number:	60241468
Application Number:	60241664
Application Number:	60278936
Application Number:	60283467
Application Number:	60287968
Application Number:	60293034
Application Number:	60309631
Application Number:	60327440
Application Number:	60400550
Application Number:	60549804
Application Number:	60555982
Application Number:	60613594
Application Number:	60618269
Application Number:	60619618
Application Number:	60792236
Application Number:	60849650
Application Number:	60989542
Application Number:	61011267
Application Number:	61183845
Application Number:	61985168
PCT Number:	US0019247
PCT Number:	US0030958
PCT Number:	US0100418

Property Type	Number
PCT Number:	US0102341
PCT Number:	US0112555
PCT Number:	US0132503
PCT Number:	US0141015
PCT Number:	US0209411
PCT Number:	US0224326
PCT Number:	US0231649
PCT Number:	US0323965
PCT Number:	US0533922
PCT Number:	US0536015
PCT Number:	US9406713
PCT Number:	US9515115
PCT Number:	US9708209
PCT Number:	US9708222
PCT Number:	US9708549
PCT Number:	US9708756
PCT Number:	US9914467

CORRESPONDENCE DATA

Fax Number: (202)887-4288

Correspondence will be sent to the e-mail address first; if that is unsuccessful, it will be sent using a fax number, if provided; if that is unsuccessful, it will be sent via US Mail.

Phone: 2028874000
Email: dlee@akingump.com
Correspondent Name: DAVID C. LEE
Address Line 1: 2001 K STREET N.W.
Address Line 2: AKIN GUMP STRAUSS HAUER & FELD LLP
Address Line 4: WASHINGTON, D.C. 20006

ATTORNEY DOCKET NUMBER:	697820.0023
NAME OF SUBMITTER:	DAVID C. LEE
SIGNATURE:	/David C. Lee/
DATE SIGNED:	01/04/2021
	This document serves as an Oath/Declaration (37 CFR 1.63).

Total Attachments: 25
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AMENDED AND RESTATED INTELLECTUAL PROPERTY SECURITY AGREEMENT

This AMENDED AND RESTATED INTELLECTUAL PROPERTY SECURITY AGREEMENT (as amended, restated, amended and restated, supplemented or otherwise modified from time to time, the "**IP Security Agreement**"), dated as of December 31, 2020, is made by each undersigned grantor (each, a "**Grantor**", and, collectively, the "**Grantors**") in favor of ALTER DOMUS (US) LLC, a Delaware limited liability company, as collateral agent for its own benefit and the benefit of the Lenders (as defined in the Credit Agreement defined below) (in such capacity, together with its successor and assigns in such capacity, the "**Collateral Agent**"). Capitalized terms used herein and not otherwise defined herein shall have the meanings assigned to such terms in the Credit Agreement or the Security Agreement (as defined below), as applicable.

WHEREAS, the Borrower, ALTER DOMUS (US) LLC, as Administrative Agent (as defined therein), the Collateral Agent and the Lenders from time party thereto, are each party to that certain Amended and Restated Credit Agreement, dated as of December 31, 2020 (as amended, restated, amended and restated, supplemented or otherwise modified from time to time, the "**Credit Agreement**"), pursuant to which the Lenders have agreed, among other things, to continue the existing term loan and extend further credit to the Borrower in the form of delayed draw term loans upon the terms and subject to the conditions specified therein;

WHEREAS, in connection with the Credit Agreement, each Grantor has entered into the Amended and Restated Security Agreement, dated as of December 31, 2020 (as amended, restated, amended and restated, supplemented or otherwise modified from time to time, the "**Security Agreement**") in order to induce the Lenders to make and continue to make, as applicable, Loans; and

WHEREAS, under the terms of the Security Agreement, each Grantor has granted to the Collateral Agent, for the ratable benefit of the Credit Parties, a security interest in, among other property, certain intellectual property of such Grantor, and has agreed as a condition thereof to execute this IP Security Agreement for recording with the United States Patent and Trademark Office and the United States Copyright Office, as the case may be.

NOW, THEREFORE, for good and valuable consideration, the receipt and sufficiency of which are hereby acknowledged, each Grantor agrees as follows:

(a) Grant of Security Interest. As security for the prompt and complete payment or performance, as the case may be, in full of the Secured Obligations, each Grantor hereby grants to the Collateral Agent for itself and the ratable benefit of the Credit Parties, a security interest in all of its right, title and interest in and to all of the following personal property, whether now owned by or owing to or hereafter acquired by or arising in favor of such Grantor (collectively, the "**IP Collateral**"):

(i) all Trademark registrations and applications for Trademark registration in the United States Patent and Trademark Office listed on Schedule I hereto;

(ii) all issued Patents and pending Patent applications in the United States Patent and Trademark Office listed on Schedule II hereto;

(iii) all Copyright registrations and pending applications for Copyright registration in the United States Copyright Office listed on Schedule III; and

(iv) all Proceeds and products of any and all of the foregoing and all supporting obligations, collateral security and guarantees given by any Person with respect to any of the foregoing;

provided, however, that notwithstanding any of the other provisions herein (and notwithstanding any recording of the Collateral Agent's Lien made in the United States Patent and Trademark Office, United States Copyright Office, or other registry office in any other jurisdiction), this Short-Form IP Security Agreement shall not constitute a grant of a security interest in any Trademark applications filed in the United States Patent and Trademark Office on the basis of such Grantor's "intent-to-use" such trademark, unless and until acceptable evidence of use of the Trademark has been filed with and accepted by the United States Patent and Trademark Office pursuant to Section 1(c) or Section 1(d) of the Lanham Act (15 U.S.C. 1051, et seq.), to the extent that granting a lien in such Trademark application prior to such filing would adversely affect the enforceability or validity of such Trademark application.

(b) Security for Secured Obligations. The grant of a security interest in the IP Collateral by each Grantor under this IP Security Agreement secures the payment of all Secured Obligations of such Grantor now or hereafter existing under or in respect of the Loan Documents, whether direct or indirect, absolute or contingent, and whether for principal, reimbursement obligations, interest, premiums, penalties, fees, indemnifications, contract causes of action, costs, expenses or otherwise, subject to the terms and provisions thereof.

(c) Recordation. This IP Security Agreement has been executed and delivered by each Grantor for the purpose of recording the grant of security interest herein with the United States Patent and Trademark Office and the United States Copyright Office, as the case may be. Each Grantor authorizes and requests that the Register of Copyrights, the Commissioner for Patents and the Commissioner for Trademarks and any other applicable government officer record this IP Security Agreement.

(d) Execution in Counterparts. This IP Security Agreement may be executed in any number of counterparts, each of which when so executed shall be deemed to be an original and all of which taken together shall constitute one and the same agreement.

(e) Grants, Rights and Remedies. This IP Security Agreement has been entered into in conjunction with the provisions of the Security Agreement. The Grantor does hereby acknowledge and confirm that the grant of the security interest hereunder to, and the rights and remedies of, the Collateral Agent with respect to the Collateral are more fully set forth in the Security Agreement, the terms and provisions of which are incorporated herein by reference as if fully set forth herein. In the event of any conflict between the terms of this IP Security Agreement and the terms of the Security Agreement, the terms of the Security Agreement shall govern.

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(f) Governing Law. THIS IP SECURITY AGREEMENT SHALL BE GOVERNED BY, AND CONSTRUED IN ACCORDANCE WITH, THE LAW OF THE STATE OF NEW YORK.

(g) General. Sections 10.04, 10.14(b) and 10.15 of the Credit Agreement are hereby incorporated by reference into this IP Security Agreement *mutatis mutandis* and shall apply hereto.

(h) Severability. In case any one or more of the provisions contained in this IP Security Agreement should be held invalid, illegal or unenforceable in any respect, the validity, legality and enforceability of the remaining provisions contained herein and in the Security Agreement shall not in any way be affected or impaired thereby (it being understood that the invalidity of a particular provision in a particular jurisdiction shall not in and of itself affect the validity of such provision in any other jurisdiction). The parties hereto shall endeavor in good-faith negotiations to replace the invalid, illegal or unenforceable provisions with valid provisions the economic effect of which comes as close as possible to that of the invalid, illegal or unenforceable provisions.

(i) Amendment and Restatement. This IP Security Agreement is an amendment and restatement but not a novation of that certain Intellectual Property Security Agreement, dated as of October 5, 2018, in favor of the Collateral Agent (as amended, modified or supplemented prior to the date hereof, the "**Original IP Security Agreement**"). All Liens and security interests securing payment of the Secured Obligations under the Original IP Security Agreement are hereby collectively, renewed, extended, ratified and brought forward as security for the payment and performance of the Secured Obligations. Each Grantor hereby (i) reaffirms each Lien, pledge and security interest granted to the Collateral Agent under or in connection with the Original IP Security Agreement, (ii) agrees that after giving effect to this IP Security Agreement such Liens, pledges and security interests shall continue in full force and effect, and (iii) agrees that such Liens, pledges and security interests continue to secure the full and prompt payment and performance of all of the Secured Obligations.

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CommScope, Inc.
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IN WITNESS WHEREOF, each Grantor has caused this IP Security Agreement to be duly executed and delivered by its officer thereunto duly authorized as of the date first above written.

TQ DELTA LLC, as Grantor

By: TQCAP GP, LLC, its manager

By: TECHQUITY CAPITAL MANAGEMENT, LLC, its sole member

By: _____
Name: Abha Divine
Title: Managing Director

[Signature Page to A&R IP Security Agreement]

ACCEPTED AND AGREED
as of the date first above written.

ALTER DOMUS (US) LLC,
as Collateral Agent

By: _____
Name: Jon Kirschmeier
Title: Associate Counsel

CommScope, Inc.
IPR2023-00064, Ex. 1035
Page 13 of 531

Schedule I

Trademarks

UNITED STATES TRADEMARKS:
Registrations / Applications:

OWNER	REGISTRATION/ APPLICATION NUMBER	TRADEMARK
TQ Delta LLC	5110447	TQ DELTA

Schedule II

Patents

(see attached)

TQ DELTA, LLC
Privileged and Confidential / Attorney Client Communication

Reference #	Title	Country ID	Status	Serial #	Filed Date	Publication #	Patent #	Issue Date	Expiration Date
6936-2-CON-2	Systems and Methods for Establishing a Diagnostic Transmission Mode and Communicating Over the Same	US	ISSUED	10/619,691	7/16/03	US 2004-0202237 A1	7,570,686	8/4/09	10/1/22
6936-2-CON-2-1	Multicarrier Modulation Messaging for Frequency Domain Received Idle Channel Noise Information	US	ISSUED	12/477,742	6/3/09	US 2009-0238254 A1	7,835,430	11/16/10	1/8/21
6936-2-CON-2-1-1	Multicarrier Modulation Messaging for Power Level Per Subchannel Information	US	EXPIRED	12/779,660	5/13/10	US 2010-0226418 A1	8,238,412	8/7/12	4/7/20
6936-2-CON-2-1-2	Multicarrier Modulation Messaging for SNR Per Subchannel During Showtime Information	US	ISSUED	12/779,708	5/13/10	US 2010-0220775 A1	7,889,784	2/15/11	1/8/21
6936-2-CON-2-1-3	Systems and Methods for Establishing a Diagnostic Transmission Mode and Communicating Over the Same	US	ISSUED	13/004,254	1/11/11	US 2011-0103443 A1	8,634,449	1/21/14	7/4/21
6936-2-CON-2-1-4	Multicarrier Modulation Messaging for Power Level Per Subchannel Information	US	ISSUED	13/476,310	5/21/12	US 2012-0230476 A1	8,432,956	4/30/13	1/8/21
6936-2-CON-2-1-5	Systems and Methods for a Transceiver to Transmit or Receive Test Information Over a Communication Channel Using Multicarrier Modulation	US	ISSUED	13/873,892	4/30/13	US 2013-0243049 A1	8,743,931	6/3/14	1/8/21
6936-2-CON-2-1-6	Systems and Methods for Establishing a Diagnostic Transmission Mode and Communicating Over the Same	US	ISSUED	14/153,282	1/13/14	US 2014-0126616 A1	8,929,423	1/6/15	1/8/21
8303-2-CON-2-1-7	Systems and Methods for Establishing a Diagnostic Transmission Mode and Communicating Over the Same	US	ISSUED	14/282,254	5/20/14	US 2014-0254645 A1	9,319,512	4/19/16	1/8/21
8303-2-CON-2-1-8	Systems and Methods for Establishing a Diagnostic Transmission Mode and Communicating Over the Same	US	ABANDONED	14/577,769	12/19/14	US 2015-0103936 A1			2/16/16
8303-2-CON-2-1-9	SYSTEMS AND METHODS FOR ESTABLISHING A DIAGNOSTIC TRANSMISSION MODE AND COMMUNICATING OVER THE SAME	US	ISSUED	14/818,731	8/5/15	US 2015-0341488 A1	9,264,533	2/16/16	1/8/21
8303-2-CON-2-1-10	SYSTEMS AND METHODS FOR ESTABLISHING A DIAGNOSTIC TRANSMISSION MODE AND COMMUNICATING OVER THE SAME	US	ISSUED	14/991,431	1/8/16	US 2016-0127537 A1	9,479,637	10/25/16	1/8/21
6936-2-CON-2-1-11	SYSTEMS AND METHODS FOR ESTABLISHING A DIAGNOSTIC TRANSMISSION MODE AND COMMUNICATING OVER THE SAME	US	ISSUED	15/016,432	2/5/16	US 2016-0165042 A1	9,973,624	5/15/18	1/8/21
6936-2-CON-2-1-12	SYSTEMS AND METHODS FOR ESTABLISHING A DIAGNOSTIC TRANSMISSION MODE AND COMMUNICATING OVER THE SAME	US	ISSUED	15/098,932	4/14/16	US 2016-0227026 A1	10,264,119	4/16/19	1/8/21
6936-2-CON-2-1-13	SYSTEMS AND METHODS FOR ESTABLISHING A DIAGNOSTIC TRANSMISSION MODE AND COMMUNICATING OVER THE SAME	US	ISSUED	15/295,602	10/17/16	US 2017-0034343 A1	9,838,531	12/5/17	1/8/21
6936-2-CON-2-1-14	SYSTEMS AND METHODS FOR ESTABLISHING A DIAGNOSTIC TRANSMISSION MODE AND COMMUNICATING OVER THE SAME	US	ISSUED	15/958,878	4/20/18	US 2018-0249001 A1	10,623,559	4/14/20	1/8/21
6936-2-PAU-4-DIV	SYSTEMS AND METHODS FOR ESTABLISHING A DIAGNOSTIC TRANSMISSION MODE AND COMMUNICATING OVER THE SAME	AU	ISSUED	2008203520	1/8/01	AU 2008203520	2008203520	11/5/09	1/8/21
6936-2-PAU-4-DIV-2	Diagnostic Methods and Systems for Multicarrier Modems	AU	ABANDONED	2009222537	1/8/01	AU 2009222537	2009222537	12/22/11	1/4/17
6936-2-PAU-4-DIV-3	SYSTEMS AND METHODS FOR ESTABLISHING A DIAGNOSTIC TRANSMISSION MODE AND COMMUNICATING OVER THE SAME	AU	ABANDONED	2011247879	1/8/01		2011247879	9/18/14	1/4/17
6936-2-PAU-4-DIV-4	SYSTEMS AND METHODS FOR ESTABLISHING A DIAGNOSTIC TRANSMISSION MODE AND COMMUNICATING OVER THE SAME	AU	ABANDONED	2014208320	1/8/01		2014208320	3/12/15	1/4/17
8303-2-PAU-4-DIV-5	DIAGNOSTIC METHODS AND SYSTEMS FOR MULTICARRIER MODEMS	AU	ABANDONED	2015200087	1/8/01				2/28/17
8303-2-PAU-4-DIV-6	DIAGNOSTIC METHODS AND SYSTEMS FOR MULTICARRIER MODEMS	AU	ABANDONED	2017201226	1/8/01		2017201226	9/7/17	12/6/19
8303-2-PAU-4-DIV-7	DIAGNOSTIC METHODS AND SYSTEMS FOR MULTICARRIER MODEMS	AU	ABANDONED	2017210489	1/8/01				12/6/19
6936-2-PCA	Diagnostic Methods and Systems for Multicarrier Modems	CA	ISSUED	2,394,491	1/8/01	CA 2394491	2,394,491	3/29/11	1/8/21
6936-2-PCA-DIV	Diagnostic Methods and Systems for Multicarrier Modems	CA	ABANDONED	2,726,826	1/8/01	CA 2726826	2,726,826	11/20/12	12/23/16
6936-2-PCA-DIV-2	Diagnostic Methods and Systems for Multicarrier Modems	CA	EXPIRED	2,788,662	1/8/01		2,788,662	1/3/17	1/8/20
6936-2-PCA-DIV-3	Diagnostic Methods and Systems for Multicarrier Modems	CA	ISSUED	2,948,960	1/8/01		2,948,960	6/23/20	1/8/21
6936-2-PCT	SYSTEMS AND METHODS FOR ESTABLISHING A DIAGNOSTIC TRANSMISSION MODE AND COMMUNICATING OVER THE SAME	WO	NAT PHASE	PCT/US01/00418	1/8/01	WO 2001/52516			

6936-2-PEP-5	SYSTEMS AND METHODS FOR ESTABLISHING A DIAGNOSTIC TRANSMISSION MODE AND COMMUNICATING OVER THE SAME	EP	ISSUED	06022008.4	1/8/01	1755253	1755253	7/13/11	1/8/21
6936-2-PEP-5-BE	SYSTEMS AND METHODS FOR ESTABLISHING A DIAGNOSTIC TRANSMISSION MODE AND COMMUNICATING OVER THE SAME	BE	ISSUED	06022008.4	1/8/01	N/A	1755253	7/13/11	1/8/21
6936-2-PEP-5-CH	SYSTEMS AND METHODS FOR ESTABLISHING A DIAGNOSTIC TRANSMISSION MODE AND COMMUNICATING OVER THE SAME	CH	ISSUED	06022008.4	1/8/01	N/A	1755253	7/13/11	1/8/21
6936-2-PEP-5-DE	SYSTEMS AND METHODS FOR ESTABLISHING A DIAGNOSTIC TRANSMISSION MODE AND COMMUNICATING OVER THE SAME	DE	ISSUED	06022008.4	1/8/01	N/A	1755253	7/13/11	1/8/21
6936-2-PEP-5-ES	SYSTEMS AND METHODS FOR ESTABLISHING A DIAGNOSTIC TRANSMISSION MODE AND COMMUNICATING OVER THE SAME	ES	ISSUED	06022008.4	1/8/01	N/A	1755253	7/13/11	1/8/21
6936-2-PEP-5-FR	SYSTEMS AND METHODS FOR ESTABLISHING A DIAGNOSTIC TRANSMISSION MODE AND COMMUNICATING OVER THE SAME	FR	ISSUED	06022008.4	1/8/01	N/A	1755253	7/13/11	1/8/21
6936-2-PEP-5-GB	SYSTEMS AND METHODS FOR ESTABLISHING A DIAGNOSTIC TRANSMISSION MODE AND COMMUNICATING OVER THE SAME	GB	ISSUED	06022008.4	1/8/01	N/A	1755253	7/13/11	1/8/21
6936-2-PEP-5-GR	SYSTEMS AND METHODS FOR ESTABLISHING A DIAGNOSTIC TRANSMISSION MODE AND COMMUNICATING OVER THE SAME	GR	ABANDONED	06022008.4	1/8/01	N/A	1755253	7/13/11	12/6/19
6936-2-PEP-5-HK	SYSTEMS AND METHODS FOR ESTABLISHING A DIAGNOSTIC TRANSMISSION MODE AND COMMUNICATING OVER THE SAME	HK	ABANDONED	07108499.2	1/8/01	HK 1100379			8/4/11
6936-2-PEP-5-IE	SYSTEMS AND METHODS FOR ESTABLISHING A DIAGNOSTIC TRANSMISSION MODE AND COMMUNICATING OVER THE SAME	IE	ISSUED	06022008.4	1/8/01	N/A	1755253	7/13/11	1/8/21
6936-2-PEP-5-IT	SYSTEMS AND METHODS FOR ESTABLISHING A DIAGNOSTIC TRANSMISSION MODE AND COMMUNICATING OVER THE SAME	IT	ISSUED	06022008.4	1/8/01	N/A	1755253	7/13/11	1/8/21
6936-2-PEP-5-NL	SYSTEMS AND METHODS FOR ESTABLISHING A DIAGNOSTIC TRANSMISSION MODE AND COMMUNICATING OVER THE SAME	NL	ISSUED	06022008.4	1/8/01	N/A	1755253	7/13/11	1/8/21
6936-2-PEP-5-DIV-1	SYSTEMS AND METHODS FOR ESTABLISHING A DIAGNOSTIC TRANSMISSION MODE AND COMMUNICATING OVER THE SAME	EP	ISSUED	10011985.8	1/8/01	2276182	2276182	2/26/20	1/8/21
6936-2-PEP-5-DIV-1-DE	SYSTEMS AND METHODS FOR ESTABLISHING A DIAGNOSTIC TRANSMISSION MODE AND COMMUNICATING OVER THE SAME	DE	ISSUED	10011985.8	1/8/01	2276182	60151242.1	2/26/20	1/8/21
6936-2-PEP-5-DIV-1-FR	SYSTEMS AND METHODS FOR ESTABLISHING A DIAGNOSTIC TRANSMISSION MODE AND COMMUNICATING OVER THE SAME	FR	ISSUED	10011985.8	1/8/01		2276182	2/26/20	1/8/21
6936-2-PEP-5-DIV-1-GB	SYSTEMS AND METHODS FOR ESTABLISHING A DIAGNOSTIC TRANSMISSION MODE AND COMMUNICATING OVER THE SAME	GB	ISSUED	10011985.8	1/8/01		2276182	2/26/20	1/8/21
6936-2-PEP-5-DIV-1-HK	SYSTEMS AND METHODS FOR ESTABLISHING A DIAGNOSTIC TRANSMISSION MODE AND COMMUNICATING OVER THE SAME	HK	ABANDONED	11101591.8	1/8/01	HK 1147612			12/5/19
6936-2-PEP-5-DIV-2	SYSTEMS AND METHODS FOR ESTABLISHING A DIAGNOSTIC TRANSMISSION MODE AND COMMUNICATING OVER THE SAME	EP	ABANDONED	10011983.3	1/8/01	2293459			12/12/19
6936-2-PEP-5-DIV-2-HK	SYSTEMS AND METHODS FOR ESTABLISHING A DIAGNOSTIC TRANSMISSION MODE AND COMMUNICATING OVER THE SAME	HK	ABANDONED	11103980.3	1/8/01	HK 1149982			12/12/19
6936-2-PEP-5-DIV-3	SYSTEMS AND METHODS FOR ESTABLISHING A DIAGNOSTIC TRANSMISSION MODE AND COMMUNICATING OVER THE SAME	EP	ISSUED	10011984.1	1/8/01	2317684	2317684	2/26/20	1/8/21
6936-2-PEP-5-DIV-3-DE	SYSTEMS AND METHODS FOR ESTABLISHING A DIAGNOSTIC TRANSMISSION MODE AND COMMUNICATING OVER THE SAME	DE	ISSUED	10011984.1	1/8/01	2317684	60151241.3	2/26/20	1/8/21
6936-2-PEP-5-DIV-3-FR	SYSTEMS AND METHODS FOR ESTABLISHING A DIAGNOSTIC TRANSMISSION MODE AND COMMUNICATING OVER THE SAME	FR	ISSUED	10011984.1	1/8/01		2317684	2/26/20	1/8/21
6936-2-PEP-5-DIV-3-GB	SYSTEMS AND METHODS FOR ESTABLISHING A DIAGNOSTIC TRANSMISSION MODE AND COMMUNICATING OVER THE SAME	GB	ISSUED	10011984.1	1/8/01		2317684	2/26/20	1/8/21
6936-2-PEP-5-DIV-3-HK	SYSTEMS AND METHODS FOR ESTABLISHING A DIAGNOSTIC TRANSMISSION MODE AND COMMUNICATING OVER THE SAME	HK	ABANDONED	11106469.6	1/8/01	1152597			11/11/19

6936-2-PEP-5-DIV-3-NL	SYSTEMS AND METHODS FOR ESTABLISHING A DIAGNOSTIC TRANSMISSION MODE AND COMMUNICATING OVER THE SAME	NL	ISSUED	10011984.1	1/8/01		2317684	2/26/20	1/8/21
6936-2-PEP-5-DIV-4	SYSTEMS AND METHODS FOR ESTABLISHING A DIAGNOSTIC TRANSMISSION MODE AND COMMUNICATING OVER THE SAME	EP	ISSUED	10011982.5	1/8/01	2270996	2270996	3/7/18	1/8/21
6936-2-PEP-5-DIV-4-DE	SYSTEMS AND METHODS FOR ESTABLISHING A DIAGNOSTIC TRANSMISSION MODE AND COMMUNICATING OVER THE SAME	DE	ISSUED	10011982.5	1/8/01		2270996	3/7/18	1/8/21
6936-2-PEP-5-DIV-4-FR	SYSTEMS AND METHODS FOR ESTABLISHING A DIAGNOSTIC TRANSMISSION MODE AND COMMUNICATING OVER THE SAME	FR	ISSUED	10011982.5	1/8/01		2270996	3/7/18	1/8/21
6936-2-PEP-5-DIV-4-GB	SYSTEMS AND METHODS FOR ESTABLISHING A DIAGNOSTIC TRANSMISSION MODE AND COMMUNICATING OVER THE SAME	GB	ISSUED	10011982.5	1/8/01		2270996	3/7/18	1/8/21
6936-2-PEP-5-DIV-4-HK	SYSTEMS AND METHODS FOR ESTABLISHING A DIAGNOSTIC TRANSMISSION MODE AND COMMUNICATING OVER THE SAME	HK	ISSUED	11101590.0	1/8/01	HK 1147611	HK 1147611	9/21/18	1/8/21
6936-2-PEP-5-DIV-5	SYSTEMS AND METHODS FOR ESTABLISHING A DIAGNOSTIC TRANSMISSION MODE AND COMMUNICATING OVER THE SAME	EP	ABANDONED	18159847.5	1/8/01	3349386			12/12/19
6936-2-PEP-5-DIV-5-HK	SYSTEMS AND METHODS FOR ESTABLISHING A DIAGNOSTIC TRANSMISSION MODE AND COMMUNICATING OVER THE SAME	HK	ABANDONED	18113502.4	1/8/01	1254420			1/14/20
6936-2-PJP	SYSTEMS AND METHODS FOR ESTABLISHING A DIAGNOSTIC TRANSMISSION MODE AND COMMUNICATING OVER THE SAME	JP	ABANDONED	2001-552611	1/8/01	JP 2003/520504			7/13/11
6936-2-PJP-DIV	SYSTEMS AND METHODS FOR ESTABLISHING A DIAGNOSTIC TRANSMISSION MODE AND COMMUNICATING OVER THE SAME	JP	ISSUED	2008-191051	1/8/01	2009-027721	4722972	4/15/11	1/8/21
6936-2-PJP-DIV-2	SYSTEMS AND METHODS FOR ESTABLISHING A DIAGNOSTIC TRANSMISSION MODE AND COMMUNICATING OVER THE SAME	JP	ABANDONED	2011-012155	1/8/01	2011-151808			6/21/13
6936-2-PROV-1	MULTICARRIER MODULATION SYSTEM WITH REMOTE DIAGNOSTIC TRANSMISSION MODE	US	EXPIRED	60/174,865	1/7/00	N/A			1/7/01
6936-2-PROV-2	CHARACTERIAZTION OF TRANSMISSION LINES USING BROADBAND SIGNALS IN A MULTI-CARRIER DSL SYSTEM	US	EXPIRED	60/224,308	8/10/00	N/A			8/10/01
6936-16	SYSTEMS AND METHODS FOR MULTI-PAIR ATM OVER DSL	US	ISSUED	10/264,258	10/4/02	US 2003-0091053 A1	7,453,881	11/18/08	7/24/25
6936-16-CON	SYSTEMS AND METHODS FOR MULTI-PAIR OVER DSL	US	ISSUED	12/247,741	10/8/08	US 2009-0028158 A1	7,809,028	10/5/10	10/4/22
6936-16-CON-2	Combining Multiple DSL Tansceivers for a High Data Rate Connection	US	ISSUED	12/769,277	4/28/10	US 2010-0208737 A1	7,978,706	7/12/11	10/4/22
6936-16-CON-3	Systems and Methods for Multi-Pair ATM Over DSL	US	ISSUED	12/783,777	5/20/10	US 2010-0290471 A1	8,422,511	4/16/13	10/4/22
6936-16-CON-4	Systems and Methods for Multi-Pair ATM Over DSL	US	ISSUED	13/863,058	4/15/13	US 2013-0223453	8,831,031	9/9/14	10/4/22
6936-16-CON-5	BONDING DEVICE AND METHOD	US	ISSUED	14/465,502	8/21/14	US 2014-0362863 A1	9,014,193	4/21/15	10/4/22
6936-16-CON-6	BONDING DEVICE AND METHOD	US	ISSUED	14/682,435	4/9/15	US 2015-0215239 A1	9,300,601	3/29/16	10/4/22
6936-16-CON-7	BONDING DEVICE AND METHOD	US	ISSUED	15/057,741	3/1/16	US 2016-0182406 A1	9,894,014	2/13/18	10/4/22
6936-16-CON-8	BONDING DEVICE AND METHOD	US	ISSUED	15/882,619	1/29/18	US 2018-0152395 A1	10,341,261	7/2/19	10/4/22
6936-16-PCA	SYSTEMS AND METHODS FOR MULTI-PAIR ATM OVER DSL	CA	ISSUED	2,461,320	10/4/02	CA 2461320	2,461,320	10/25/11	10/4/22
6936-16-PCT	SYSTEMS AND METHODS FOR MULTI-PAIR ATM OVER DSL	WO	NAT PHASE	PCT/US02/31649	10/4/02	WO 2003/032555			
6936-16-PEP	SYSTEMS AND METHODS FOR MULTI-PAIR ATM OVER DSL	EP	ISSUED	02778433.9	10/4/02	1433277	1433277	7/25/12	10/4/22
6936-16-PEPBE	SYSTEMS AND METHODS FOR MULTI-PAIR ATM OVER DSL	BE	ISSUED	02778433.9	10/4/02		1433277	7/25/12	10/4/22
6936-16-PEPDE	SYSTEMS AND METHODS FOR MULTI-PAIR ATM OVER DSL	DE	ISSUED	02778433.9	10/4/02		1433277	7/25/12	10/4/22
6936-16-PEPFR	SYSTEMS AND METHODS FOR MULTI-PAIR ATM OVER DSL	FR	ISSUED	02778433.9	10/4/02		1433277	7/25/12	10/4/22
6936-16-PEPGB	SYSTEMS AND METHODS FOR MULTI-PAIR ATM OVER DSL	GB	ISSUED	02778433.9	10/4/02		1433277	7/25/12	10/4/22
6936-16-PEP-DIV	SYSTEMS AND METHODS FOR MULTI-PAIR ATM OVER DSL	EP	ISSUED	12002728.9	10/4/02	2506508	2506508	5/2/18	10/4/22
6936-16-PEP-DIV-DE	SYSTEMS AND METHODS FOR MULTI-PAIR ATM OVER DSL	DE	ISSUED	12002728.9	10/4/02		2506508	5/2/18	10/4/22
6936-16-PEP-DIV-FR	SYSTEMS AND METHODS FOR MULTI-PAIR ATM OVER DSL	FR	ISSUED	12002728.9	10/4/02		2506508	5/2/18	10/4/22
6936-16-PEP-DIV-GB	SYSTEMS AND METHODS FOR MULTI-PAIR ATM OVER DSL	GB	ISSUED	12002728.9	10/4/02		2506508	5/2/18	10/4/22
6936-16-PEP-DIV-2	SYSTEMS AND METHODS FOR MULTI-PAIR ATM OVER DSL	EP	ISSUED	18170134.3	10/4/02	3386128	3386128	7/24/19	10/4/22
6936-16-PEP-DIV-2-DE	SYSTEMS AND METHODS FOR MULTI-PAIR ATM OVER DSL	DE	ISSUED	18170134.3	10/4/02	3386128	DE60249960.7	7/24/19	10/4/22
6936-16-PEP-DIV-2-FR	SYSTEMS AND METHODS FOR MULTI-PAIR ATM OVER DSL	FR	ISSUED	18170134.3	10/4/02		3386128	7/24/19	10/4/22
6936-16-PEP-DIV-2-GB	SYSTEMS AND METHODS FOR MULTI-PAIR ATM OVER DSL	GB	ISSUED	18170134.3	10/4/02		3386128	7/24/19	10/4/22

6936-16-PEP-DIV-2-NL	SYSTEMS AND METHODS FOR MULTI-PAIR ATM OVER DSL	NL	ISSUED	18170134.3	10/4/02		3386128	7/24/19	10/4/22
6936-16-PROV	MULIT-PAIR ATM OVER DSL	US	EXPIRED	60/327,440	10/5/01	N/A			10/5/02
6936-54	RESOURCE SHARING IN A TELECOMMUNICATIONS ENVIRONMENT	US	ISSUED	11/246,163	10/11/05	US 2006-0088054 A1	7,831,890	11/9/10	11/7/28
6936-54-CON	RESOURCE SHARING IN A TELECOMMUNICATIONS ENVIRONMENT	US	ISSUED	12/761,586	4/16/10	US 2010-0228924 A1	7,844,882	11/30/10	10/11/25
6936-54-CON-2	Computer Readable Medium with Instructions for Resource Sharing in a Telecommunications Environment	US	ISSUED	12/853,020	8/9/10	US 2010-0306628 A1	7,836,381	11/16/10	10/11/25
6936-54-CON-3	RESOURCE SHARING IN A TELECOMMUNICATIONS ENVIRONMENT	US	ISSUED	12/901,699	10/11/10	US 2011-0029844 A1	8,276,048	9/25/12	10/11/25
6936-54-CON-4	RESOURCE SHARING IN A TELECOMMUNICATIONS ENVIRONMENT	US	ISSUED	13/567,261	8/6/12	US 2012-0297148 A1	8,495,473	7/23/13	10/11/25
6936-54-CON-5	RESOURCE SHARING IN A TELECOMMUNICATIONS ENVIRONMENT	US	ISSUED	13/942,938	7/16/13	US 2013-0308689 A1	8,607,126	12/10/13	10/11/25
6936-54-CON-6	RESOURCE SHARING IN A TELECOMMUNICATIONS ENVIRONMENT	US	ISSUED	14/081,469	11/15/13	US 2014-0075128 A1	9,069,718	6/30/15	10/11/25
6936-54-CON-7	RESOURCE SHARING IN A TELECOMMUNICATIONS ENVIRONMENT	US	ISSUED	14/730,874	6/4/15	US 2015-0268863 A1	9,286,251	3/15/16	10/11/25
6936-54-CON-8	RESOURCE SHARING IN A TELECOMMUNICATIONS ENVIRONMENT	US	ISSUED	15/046,821	2/18/16	US 2016-0179389 A1	9,547,608	1/17/17	10/11/25
6936-54-CON-9	RESOURCE SHARING IN A TELECOMMUNICATIONS ENVIRONMENT	US	ISSUED	15/372,841	12/8/16	US 2017-0090811 A1	9,898,220	2/20/18	10/11/25
6936-54-CON-10	RESOURCE SHARING IN A TELECOMMUNICATIONS ENVIRONMENT	US	ISSUED	15/874,277	1/18/18	US 2018-0157436 A1	10,409,510	9/10/19	10/11/25
6936-54-CON-10-DIV	RESOURCE SHARING IN A TELECOMMUNICATIONS ENVIRONMENT	US	ISSUED	16/261,109	1/29/19	US 2019-0155530 A1	10,579,291	3/3/20	10/11/25
6936-54-CON-11	RESOURCE SHARING IN A TELECOMMUNICATIONS ENVIRONMENT	US	PUBLISHED	16/544,003	8/19/19	US 2019-0369891 A1			10/11/25
6936-54-PAU	Resource Sharing in a Telecommunications Environment	AU	ABANDONED	2005296086	10/11/05	AU 2005296086			4/6/11
6936-54-PAU-DIV	Resource Sharing in a Telecommunications Environment	AU	ABANDONED	2011201250	10/11/05	AU 2011201250			2/25/15
6936-54-PAU-DIV-2	Resource Sharing in a Telecommunications Environment	AU	ISSUED	2015200618	10/11/05		2015200618	11/12/15	10/11/25
6936-54-PCA	Resource Sharing in a Telecommunications Environment	CA	ISSUED	2,580,280	10/11/05	CA 2580280	2,580,280	3/10/15	10/11/25
6936-54-PCA-DIV	Resource Sharing in a Telecommunications Environment	CA	ABANDONED	2,869,452	10/11/05		2,869,452	1/19/16	9/25/17
6936-54-PCA-DIV-2	Resource Sharing in a Telecommunications Environment	CA	ABANDONED	2,909,150	10/11/05		2,909,150	11/7/17	9/4/20
6936-54-PCA-DIV-3	Resource Sharing in a Telecommunications Environment	CA	ISSUED	2,980,607	10/11/05		2,980,607	4/7/20	10/11/25
6936-54-PCN	Resource Sharing in a Telecommunications Environment	CN	ABANDONED	200580032703.1	10/11/05	CN101057438A			7/14/15
6936-54-PCN-DIV	Resource Sharing in a Telecommunications Environment	CN	ISSUED	201510413116.2	10/11/05	104993912	ZL201510413116.2	12/3/19	10/11/25
6936-54-PCT	RESOURCE SHARING IN A TELECOMMUNICATIONS ENVIRONMENT	WO	NAT PHASE	PCT/US05/36015	10/11/05	WO 2006/044227 A1			
6936-54-PEP	RESOURCE SHARING IN A TELECOMMUNICATIONS ENVIRONMENT	EP	ISSUED	05807443.6	10/11/05	EP 1832028	1832028	1/31/18	10/11/25
6936-54-PEPDE	RESOURCE SHARING IN A TELECOMMUNICATIONS ENVIRONMENT	DE	ISSUED	05807443.6	10/11/05		1832028	1/31/18	10/11/25
6936-54-PEPFR	RESOURCE SHARING IN A TELECOMMUNICATIONS ENVIRONMENT	FR	ISSUED	05807443.6	10/11/05		1832028	1/31/18	10/11/25
6936-54-PEPGB	RESOURCE SHARING IN A TELECOMMUNICATIONS ENVIRONMENT	GB	ISSUED	05807443.6	10/11/05		1832028	1/31/18	10/11/25
6936-54-PEPHK	RESOURCE SHARING IN A TELECOMMUNICATIONS ENVIRONMENT	HK	ISSUED	07110121.4	10/11/05	HK 1102043	HK 1102043	7/6/18	10/11/25
6936-54-PEP-DIV	RESOURCE SHARING IN A TELECOMMUNICATIONS ENVIRONMENT	EP	PUBLISHED	18153945.3	10/11/05	3340511			10/11/25
6936-54-PEP-DIV-HK	RESOURCE SHARING IN A TELECOMMUNICATIONS ENVIRONMENT	HK	PUBLISHED	18113503.3	10/11/05	1254421			10/11/25
6936-54-PIN	Resource Sharing in a Telecommunications Environment	IN	ABANDONED	1208/KOLNP/2007	10/11/05	IN 1208/KOLNP/2007			10/12/24
6936-54-PJP	Resource Sharing in a Telecommunications Environment	JP	ISSUED	2007-535818	10/11/05	2008-516533	4889646	12/22/11	10/11/25
6936-54-PJP-DIV	Resource Sharing in a Telecommunications Environment	JP	ABANDONED	2008-264540	10/11/05	2009-065692	4976359	4/20/12	2/21/17
6936-54-PKR	Method and System for Allocating Shared Memory in a Transceiver	KR	ISSUED	10-2007-7008270	10/11/05	10-2007-0065369	10-1160717	6/21/12	10/11/25
6936-54-PKR-DIV	Method for Allocating Memory in a Transceiver	KR	ABANDONED	10-2010-7022463	10/11/05	10-2010/0116234	10-1160765	6/21/12	3/10/17
6936-54-PROV	RESOURCE SHARING IN A TELECOMMUNICATIONS ENVIRONMENT	US	EXPIRED	60/618,269	10/12/04	N/A			10/12/05

6936-47	SYSTEM AND METHOD FOR SCRAMBLING THE PHASE OF THE CARRIERS IN A MULTICARRIER COMMUNICATIONS SYSTEM	US	ISSUED	09/710,310	11/9/00	N/A	6,961,369	11/1/05	7/28/23
6936-47-CON	SYSTEM AND METHOD FOR SCRAMBLING THE PHASE OF THE CARRIERS IN A MULTICARRIER COMMUNICATIONS SYSTEM	US	EXPIRED	11/211,535	8/26/05	US 2006-0002454 A1	7,292,627	11/6/07	11/9/20
6936-47-CON-2	System and Method for Scrambling the Phase of the Carriers in a Multicarrier Communications System	US	EXPIRED	11/863,581	9/28/07	US 2008-0069253 A1	7,471,721	12/30/08	11/9/20
6936-47-CON-3	System and Method for Scrambling the Phase of the Carriers in a Multicarrier Communications System	US	EXPIRED	12/255,713	10/22/08	US 2009-0110105 A1	7,769,104	8/3/10	11/9/20
6936-47-CON-4	System and Method for Scrambling the Phase of the Carriers in a Multicarrier Communications System	US	EXPIRED	12/783,725	5/20/10	US 2010-0290507 A1	8,090,008	1/3/12	11/9/20
6936-47-CON-5	System and Method for Scrambling the Phase of the Carriers in a Multicarrier Communications System	US	EXPIRED	13/303,417	11/23/11	US 2012-0069878 A1	8,718,158	5/6/14	11/18/20
6936-47-CON-6	System and Method for Scrambling the Phase of the Carriers in a Multicarrier Communications System	US	EXPIRED	14/256,677	4/18/14	US 2014-0226737 A1	8,929,470	1/6/15	11/9/20
6936-47-CON-7	System and Method for Scrambling the Phase of the Carriers in a Multicarrier Communications System	US	EXPIRED	14/540,332	11/13/14	US 2015-0071385 A1	9,755,876	9/5/17	11/9/20
6936-47-CON-8	System and Method for Scrambling the Phase of the Carriers in a Multicarrier Communications System	US	EXPIRED	15/693,914	9/1/17	US 2018-0013599 A1	10,187,240	1/22/19	11/9/20
6936-47-CON-DIV	System and Method for Descrambling the Phase of the Carriers in a Multicarrier Communications System	US	ISSUED	11/860,080	9/24/07		8,073,041	12/6/11	11/5/23
6936-47-CON-DIV-CON	System and method for descrambling the phase of carriers in a multicarrier communications system	US	EXPIRED	13/284,549	10/28/11	US 2012-0044977 A1	8,218,610	7/10/12	11/9/20
6936-47-CON-DIV-CON-2	System and Method for Descrambling the Phase of Carriers in a Multicarrier Communications System	US	EXPIRED	13/439,605	4/4/12	US 2012-0195353 A1	8,355,427	1/15/13	11/9/20
6936-47-CON-DIV-CON-3	System and Method for Scrambling Using a Bit Scrambler and a Phase Scrambler	US	EXPIRED	13/718,016	12/18/12	US 2013-0136160-A1	9,014,243	4/21/15	11/9/20
6936-47-CON-DIV-CON-4	SYSTEM AND METHOD FOR SCRAMBLING USING A BIT SCRAMBLER AND A PHASE SCRAMBLER	US	EXPIRED	14/684,737	4/13/15	US 2015-0222467 A1	9,485,128	11/1/16	11/9/20
6936-47-CON-DIV-CON-5	SYSTEM AND METHOD FOR SCRAMBLING USING A BIT SCRAMBLER AND A PHASE SCRAMBLER	US	PUBLISHED	15/298,817	10/20/16	US 2017-0041173 A1			11/9/20
6936-47-PAU	SYSTEM AND METHOD FOR SCRAMBLING THE PHASE OF THE CARRIERS IN A MULTICARRIER COMMUNICATIONS SYSTEM	AU	ABANDONED	15964/01	11/9/00	AU 1596401			11/9/20
6936-47-PCA	SYSTEM AND METHOD FOR SCRAMBLING THE PHASE OF THE CARRIERS IN A MULTICARRIER COMMUNICATIONS SYSTEM	CA	ABANDONED	2,387,812	11/9/00	CA2387812			11/9/20
6936-47-PCT	SYSTEM AND METHOD FOR SCRAMBLING THE PHASE OF THE CARRIERS IN A MULTICARRIER COMMUNICATIONS SYSTEM	WO	NAT PHASE	PCT/US00/030958	11/9/00	WO 2001/035591			
6936-47-PEP	SYSTEM AND METHOD FOR SCRAMBLING THE PHASE OF THE CARRIERS IN A MULTICARRIER COMMUNICATIONS SYSTEM	EP	ABANDONED	00978507.2	11/9/00	EP 1228615			11/9/20
6936-47-PJP	SYSTEM AND METHOD FOR SCRAMBLING THE PHASE OF THE CARRIERS IN A MULTICARRIER COMMUNICATIONS SYSTEM	JP	ABANDONED	2001-537217	11/9/00	2003-514444A			11/9/20
6936-47-PJP-DIV	System and Method for Scrambling the Phase of the Carriers in a Multicarrier Communications System	JP	ABANDONED	2006-345675	11/9/00	JP 2007/129755			11/9/20
6936-47-PKR	SYSTEM AND METHOD FOR SCRAMBLING THE PHASE OF THE CARRIERS IN A MULTICARRIER COMMUNICATIONS SYSTEM	KR	ABANDONED	2002-7005830	11/9/00	10-2002-0049025			11/9/20
6936-47-PROV	SYSTEM AND METHOD FOR SCRAMBLING THE PHASE OF THE CARRIERS IN A MULTICARRIER COMMUNICATIONS SYSTEM	US	EXPIRED	60/164,134	11/9/99	N/A			11/9/00
6936-53	CRC COUNTER NORMALIZATION	US	ISSUED	11/232,899	9/23/05	US 2006-0069980 A1	7,451,379	11/11/08	3/8/27
6936-53-CON	CRC COUNTER NORMALIZATION	US	ISSUED	12/236,902	9/24/08	US 2009-0019346	7,925,958	4/12/11	5/4/26
6936-53-CON-2	CRC COUNTER NORMALIZATION	US	ISSUED	12/783,771	5/20/10	US 2010-0293444 A1	7,979,778	7/12/11	9/23/25
6936-53-CON-3	CRC COUNTER NORMALIZATION	US	ISSUED	13/156,098	6/8/11	US 2011-0239087 A1	8,516,337	8/20/13	9/23/25
6936-53-CON-4	CRC COUNTER NORMALIZATION	US	ISSUED	13/968,880	8/16/13	US 2013-0339828 A1	8,793,553	7/29/14	9/23/25
6936-53-CON-5	CRC COUNTER NORMALIZATION	US	ISSUED	14/338,503	7/23/14	US 2014-0337683 A1	8,984,366	3/17/15	9/23/25
6936-53-CON-6	CRC COUNTER NORMALIZATION	US	ISSUED	14/638,889	3/4/15	US 2015-0180508 A1	9,300,324	3/29/16	9/23/25
6936-53-CON-7	CRC COUNTER NORMALIZATION	US	ISSUED	15/062,522	3/7/16	US 2016-0188403 A1	10,049,003	8/14/18	9/23/25
6936-53-CON-8	CRC COUNTER NORMALIZATION	US	ISSUED	16/037,825	7/17/18	US 2018-0341544 A1	10,346,243	7/9/19	9/23/25
6936-53-CON-9	CRC COUNTER NORMALIZATION	US	PUBLISHED	16/428,232	5/31/19	US 2019-0286514 A1			9/23/25
6936-53-PAU	CRC COUNTER NORMALIZATION	AU	ISSUED	2005289753	9/23/05	AU 2005289753	2005289753	3/19/09	9/23/25
6936-53-PAU-DIV	CRC COUNTER NORMALIZATION	AU	ABANDONED	2009200784	9/23/05	AU 2009200784			6/27/11
6936-53-PCA	CRC COUNTER NORMALIZATION	CA	ISSUED	2,550,263	9/23/05	CA 2550263	2,550,263	11/2/10	9/23/25

6936-53-PCA-DIV	CRC COUNTER NORMALIZATION	CA	ABANDONED	2,711,718	9/23/05	CA 2711718	2,711,718	3/24/15	7/28/20
6936-53-PCA-DIV-2	CRC COUNTER NORMALIZATION	CA	ABANDONED	2,876,137	9/23/05		2,876,137	9/13/16	9/12/18
6936-53-PCA-DIV-3	CRC COUNTER NORMALIZATION	CA	ABANDONED	2,935,980	9/23/05		2,935,980	1/8/19	7/28/20
6936-53-PCA-DIV-4	CRC COUNTER NORMALIZATION	CA	ABANDONED	3,023,907	9/23/05		3,023,907	6/4/19	7/28/20
6936-53-PCN	CRC COUNTER NORMALIZATION	CN	ISSUED	200580008869.X	9/23/05	CN1934817A	200580008869.X	5/16/12	9/23/25
6936-53-PCN-DIV	CRC COUNTER NORMALIZATION	CN	ABANDONED	201210063701.0	9/23/05	CN 102624488	201210063701.0	11/25/15	7/25/17
6936-53-PCN-DIV-HK	A Method and a system for Cyclic Redundancy Checksum (CRC) Anomaly Counter Normalization, and a Module Performing the Method	HK	ABANDONED	13101408.9	9/23/05	HK1174752			3/22/16
6936-53-PCT	CRC COUNTER NORMALIZATION	WO	NAT PHASE	PCT/US05/033922	9/23/05	WO 2006/036723 A1			
6936-53-PEP	CRC COUNTER NORMALIZATION	EP	ISSUED	05799765.2	9/23/05	1792430	1792430	7/20/11	9/23/25
6936-53-PEPBE	CRC COUNTER NORMALIZATION	BE	ABANDONED	05799765.2	9/23/05	N/A	1792430	7/20/11	8/4/20
6936-53-PEPCH	CRC COUNTER NORMALIZATION	CH	ABANDONED	05799765.2	9/23/05	N/A	1792430	7/20/11	8/4/20
6936-53-PEPDE	CRC COUNTER NORMALIZATION	DE	ISSUED	05799765.2	9/23/05	N/A	1792430	7/20/11	9/23/25
6936-53-PEPDK	CRC COUNTER NORMALIZATION	DK	ABANDONED	05799765.2	9/23/05	N/A	1792430	7/20/11	8/4/20
6936-53-PEPFR	CRC COUNTER NORMALIZATION	FR	ISSUED	05799765.2	9/23/05	N/A	1792430	7/20/11	9/23/25
6936-53-PEPGB	CRC COUNTER NORMALIZATION	GB	ABANDONED	05799765.2	9/23/05	N/A	1792430	7/20/11	8/6/19
6936-53-PEPHK	CRC COUNTER NORMALIZATION	HK	ABANDONED	07110654.9	9/23/05	HK 1102488			8/4/11
6936-53-PEPIE	CRC COUNTER NORMALIZATION	IE	ABANDONED	05799765.2	9/23/05	N/A	1792430	7/20/11	8/4/20
6936-53-PEPNL	CRC COUNTER NORMALIZATION	NL	ISSUED	05799765.2	9/23/05	N/A	1792430	7/20/11	9/23/25
6936-53-PEPSE	CRC COUNTER NORMALIZATION	SE	ABANDONED	05799765.2	9/23/05	N/A	1792430	7/20/11	8/4/20
6936-53-PEP-DIV	CRC COUNTER NORMALIZATION	EP	ISSUED	11005906.0	9/23/05	EP2381610A1	2381610	12/21/16	9/23/25
6936-53-PEP-DIV-DE	CRC COUNTER NORMALIZATION	DE	ISSUED	11005906.0	9/23/05		2381610	12/21/16	9/23/25
6936-53-PEP-DIV-FR	CRC COUNTER NORMALIZATION	FR	ISSUED	11005906.0	9/23/05		2381610	12/21/16	9/23/25
6936-53-PEP-DIV-GB	CRC COUNTER NORMALIZATION	GB	ISSUED	11005906.0	9/23/05		2381610	12/21/16	9/23/25
6936-53-PEP-DIV-2	CRC COUNTER NORMALIZATION	EP	ISSUED	16020487.1	9/23/05	3176973	3176973	6/17/20	9/23/25
6936-53-PEP-DIV-2-DE	CRC COUNTER NORMALIZATION	DE	ISSUED	16020487.1	9/23/05		3176973	6/17/20	9/23/25
6936-53-PEP-DIV-2-FR	CRC COUNTER NORMALIZATION	FR	ISSUED	16020487.1	9/23/05		3176973	6/17/20	9/23/25
6936-53-PEP-DIV-2-GB	CRC COUNTER NORMALIZATION	GB	ISSUED	16020487.1	9/23/05		3176973	6/17/20	9/23/25
6936-53-PIN	CRC COUNTER NORMALIZATION	IN	ABANDONED	1601/KOLNP/2006	9/23/05	IN 1601/KOLNP/2006			9/23/25
6936-53-PJP	CRC COUNTER NORMALIZATION	JP	ABANDONED	2006-551651	9/23/05	2007-519382			10/12/11
6936-53-PJP-DIV	CRC COUNTER NORMALIZATION	JP	ABANDONED	2006-345676	9/23/05	JP 2007/151145			10/12/11
6936-53-PJP-DIV-2	CRC COUNTER NORMALIZATION	JP	ISSUED	2010-042193	9/23/05	2010-178353	5237317	4/5/13	9/23/25
6936-53-PJP-DIV-3	CRC COUNTER NORMALIZATION	JP	ISSUED	2012-194723	9/23/05	2013-009417	5823936	10/16/15	9/23/25
6936-53-PJP-DIV-4	CRC COUNTER NORMALIZATION	JP	ISSUED	2015-105633	9/23/05	2015-167401	6215254	9/29/17	9/23/25
6936-53-PJP-DIV-5	CRC COUNTER NORMALIZATION	JP	ISSUED	2016-162059	9/23/05	2016-220241	6335230	5/11/18	9/23/25
6936-53-PKR	CRC COUNTER NORMALIZATION	KR	ISSUED	10-2006-7011697	9/23/05	10-2007-0072425	10-0955190	4/20/10	9/23/25
6936-53-PKR-DIV	CRC COUNTER NORMALIZATION	KR	ABANDONED	10-2010-7005285	9/23/05	10-2010/0035665			9/23/25
6936-53-PKR-DIV-2	CRC COUNTER NORMALIZATION	KR	ABANDONED	10-2010-7024190	9/23/05	10-2010-0120722			9/23/25
6936-53-PROV	CRC COUNTER NORMALIZATION METHOD AND SYSTEM	US	EXPIRED	60/613,594	9/25/04	N/A			9/25/05
6936-52-PCA	Impulse Noise Management	CA	ISSUED	2,555,757	3/3/05	CA 2555757	2,555,757	1/20/15	3/3/25
6936-52-PCA-REI	Impulse Noise Management	CA	ISSUED	2,555,757R	3/3/05		2,555,757	3/27/18	3/3/25
6936-52-PCN	On-Line Impulse Noise Protection (INP) Adaptation	CN	ABANDONED	200580006738.8	3/3/05	CN1926794A			11/10/11
6936-52-PCT	ON-LINE IMPULSE NOISE PROTECTION (INP) ADAPTATION	WO	NAT PHASE	PCT/US05/06842	3/3/05	WO 2005/086405 A3			
6936-52-PEP	Impulse Noise Management	EP	ABANDONED	05724394.1	3/3/05	EP 1721403			3/3/25
6936-52-PEPHK	ON-LINE IMPULSE NOISE PROTECTION (INP) ADAPTATION	HK	ABANDONED	07105041.1	3/3/05	HK 1097672			8/23/12
6936-52-PEP-DIV	Impulse Noise Management	EP	ABANDONED	10006702.4	3/3/05	2228936			3/7/11
6936-52-PEP-DIV-HK	Impulse Noise Management	HK	ABANDONED	10110020.1	3/3/05	HK 1143672			8/23/12
6936-52-PIN	ON-LINE IMPULSE NOISE PROTECTION (INP) ADAPTATION	IN	ABANDONED	2155/KOLNP/2006	7/31/06	IN 2137/KOLNP/2006			7/31/26
6936-52-PROV	ON-LINE IMPULSE NOISE PROTECTION (INP) ADAPTATION	US	EXPIRED	60/549,804	3/3/04	N/A			3/3/05
6936-52-PROV-2	IMPULSE NOISE PROTECTION (INP) TRAINING	US	EXPIRED	60/555,982	3/24/04	N/A			3/24/05
6936-52-PUS	Impulse Noise Management	US	ABANDONED	10/597,482	7/27/06	US 2008-0232444 A1			10/14/11
6936-52-PUS-CON	Impulse Noise Management	US	ISSUED	12/769,193	4/28/10	US 2010-0220771 A1	8,462,835	6/11/13	3/3/25
6936-52-PUS-CON-2	Impulse Noise Management	US	ISSUED	13/914,852	6/11/13	US 2013-0272355 A1	8,594,162	11/26/13	3/3/25
6936-52-PUS-CON-3	Impulse Noise Management	US	ISSUED	14/075,077	11/8/13	US 2014-0064343 A1	8,743,932	6/3/14	3/3/25
6936-52-PUS-CON-4	Impulse Noise Management	US	ABANDONED	14/285,911	5/23/14	US 2014-0254643 A1			2/11/16
6936-52-PUS-CON-5	IMPULSE NOISE MANAGEMENT	US	ABANDONED	14/757,630	12/23/15	US 2016-0127079 A1			9/10/18
6936-52-PUS-CON-6	IMPULSE NOISE MANAGEMENT	US	ISSUED	16/126,027	9/10/18	US 2019-0007164 A1	10,567,112	2/18/20	3/3/25
6936-52-PUS-CON-6-DIV	IMPULSE NOISE MANAGEMENT	US	ISSUED	16/448,939	6/21/19	US 2019-0312667 A1	10,805,040	10/13/20	3/3/25
6936-52-PUS-CON-7	IMPULSE NOISE MANAGEMENT	US	PUBLISHED	16/781,802	2/4/20	US 2020-0177304 A1			3/3/25
6936-28	MULTICARRIER TRANSMISSION SYSTEM WITH LOW POWER SLEEP MODE AND RAPID-ON CAPABILITY	US	EXPIRED	09/581,400	6/13/00	N/A	6,445,730	9/3/02	1/26/19
6936-28-CON	MULTICARRIER TRANSMISSION SYSTEM WITH LOW POWER SLEEP MODE AND RAPID-ON CAPABILITY	US	ABANDONED	10/175,815	6/21/02	US 2002-0150152			5/17/04
6936-28-CON-1	MULTICARRIER TRANSMISSION SYSTEM WITH LOW POWER SLEEP MODE AND RAPID-ON CAPABILITY	US	ABANDONED	10/778,083	2/17/04	US 2004-0160906			5/30/05
6936-28-CON-2	MULTICARRIER TRANSMISSION SYSTEM WITH LOW POWER SLEEP MODE AND RAPID-ON CAPABILITY	US	ABANDONED	11/090,183	3/28/05	US 2005-0185726 A1			3/12/06
6936-28-CON-3	MULTICARRIER TRANSMISSION SYSTEM WITH LOW POWER SLEEP MODE AND RAPID-ON CAPABILITY	US	ABANDONED	11/289,516	11/30/05	US 2006-0078060 A1			

6936-28-CON-4	MULTICARRIER TRANSMISSION SYSTEM WITH LOW POWER SLEEP MODE AND RAPID-ON CAPABILITY	US	EXPIRED	11/425,507	6/21/06	US 2006-0233273 A1	7,697,598	4/13/10	1/26/19
6936-28-CON-5	Multicarrier Transmission System with Low Power Sleep Mode and Rapid-on Capability	US	ABANDONED	12/615,946	11/10/09	US 2010-0054312 A1	7,978,753	7/12/11	12/12/18
6936-28-CON-6	Multicarrier Transmission System with Low Power Sleep Mode and Rapid-On Capability	US	EXPIRED	13/152,558	6/3/11	US 2011-0235691 A1	8,437,382	5/7/13	1/26/19
6936-28-CON-7	Multicarrier Transmission System with Low Power Sleep Mode and Rapid-On Capability	US	EXPIRED	13/887,889	5/6/13	US 2013-0243051-A1	8,611,404	12/17/13	1/26/19
6936-28-CON-8	Multicarrier Transmission System with Low Power Sleep Mode and Rapid-On Capability	US	EXPIRED	14/092,248	11/27/13	US 2014-0086287 A1	8,750,352	6/10/14	1/26/19
6936-28-CON-9	Multicarrier Transmission System with Low Power Sleep Mode and Rapid-On Capability	US	ABANDONED	14/295,981	6/4/14	US 2014-0286379 A1	9,094,268	7/28/15	12/12/18
6936-28-CON-10	MULTICARRIER TRANSMISSION SYSTEM WITH LOW POWER SLEEP MODE AND RAPID-ON CAPABILITY	US	EXPIRED	14/798,014	7/13/15	US 2015-0326404 A1	9,521,003	12/13/16	1/26/19
6936-28-CON-11	MULTICARRIER TRANSMISSION SYSTEM WITH LOW POWER SLEEP MODE AND RAPID-ON CAPABILITY	US	ABANDONED	15/180,274	6/13/16	US 2016-0286493 A1			11/19/18
6936-28-PAU	MULTICARRIER TRANSMISSION SYSTEM WITH LOW POWER SLEEP MODE AND RAPID-ON CAPABILITY	AU	EXPIRED	23409/99	1/26/99	AU 2340999	764933	12/18/03	1/26/19
6936-28-PAU-2	MULTICARRIER TRANSMISSION SYSTEM WITH LOW POWER SLEEP MODE AND RAPID-ON CAPABILITY	AU	ABANDONED	2003266426	12/4/03	AU 2003266429			3/10/05
6936-28-PCA	MULTICARRIER TRANSMISSION SYSTEM WITH LOW POWER SLEEP MODE AND RAPID-ON CAPABILITY	CA	EXPIRED	2,357,551	1/26/99	CA 2357551	2,357,551	9/30/08	1/26/19
6936-28-PCA-DIV	Multicarrier Transmission System With Low Power Sleep Mode and Rapid-On Capability	CA	ABANDONED	2,633,064	1/26/99	CA 2633064	2,633,064	4/2/13	12/23/16
6936-28-PCA-DIV-2	Multicarrier Transmission System With Low Power Sleep Mode and Rapid-On Capability	CA	EXPIRED	2,800,005	1/26/99		2,800,005	3/14/17	1/26/19
6936-28-PCT	MULTICARRIER TRANSMISSION SYSTEM WITH LOW POWER SLEEP MODE AND RAPID-ON CAPABILITY	WO	NAT PHASE	PCT/US99/01539	1/26/99	WO 2000/045559			
6936-28-PEP	MULTICARRIER TRANSMISSION SYSTEM WITH LOW POWER SLEEP MODE AND RAPID-ON CAPABILITY	EP	EXPIRED	99903370.7	1/26/99	1145518	1145518	11/24/04	1/26/19
6936-28-PEPGB	MULTICARRIER TRANSMISSION SYSTEM WITH LOW POWER SLEEP MODE AND RAPID-ON CAPABILITY	GB	EXPIRED	99903370.7	1/26/99	N/A	1145518	11/24/04	1/26/19
6936-28-PEP-2	MULTICARRIER TRANSMISSION SYSTEM WITH LOW POWER SLEEP MODE AND RAPID-ON CAPABILITY	EP	EXPIRED	04022871.0	1/26/99	1524812	1524812	10/31/07	1/26/19
6936-28-PEP-2-DE	MULTICARRIER TRANSMISSION SYSTEM WITH LOW POWER SLEEP MODE AND RAPID-ON CAPABILITY	DE	EXPIRED	04022871.0	1/26/99	N/A	1524812	10/31/07	1/26/19
6936-28-PEP-2-FR	MULTICARRIER TRANSMISSION SYSTEM WITH LOW POWER SLEEP MODE AND RAPID-ON CAPABILITY	FR	EXPIRED	04022871.0	1/26/99	N/A	1524812	10/31/07	1/26/19
6936-28-PEP-2-GB	MULTICARRIER TRANSMISSION SYSTEM WITH LOW POWER SLEEP MODE AND RAPID-ON CAPABILITY	GB	EXPIRED	04022871.0	1/26/99	N/A	1524812	10/31/07	1/26/19
6936-28-PEP-3	Multicarrier Transmission System with Low Power Sleep Mode and Rapid-on-Capability	EP	EXPIRED	07021150.3	1/26/99	1901512	1901512	11/23/11	1/26/19
6936-28-PEP-3-DE	Multicarrier Transmission System with Low Power Sleep Mode and Rapid-on-Capability	DE	EXPIRED	07021150.3	1/26/99	N/A	1901512	11/23/11	1/26/19
6936-28-PEP-3-FR	Multicarrier Transmission System with Low Power Sleep Mode and Rapid-on-Capability	FR	EXPIRED	07021150.3	1/26/99	N/A	1901512	11/23/11	1/26/19
6936-28-PEP-3-GB	Multicarrier Transmission System with Low Power Sleep Mode and Rapid-on-Capability	GB	EXPIRED	07021150.3	1/26/99	N/A	1901512	11/23/11	1/26/19
6936-28-PEP-3-HK	Multicarrier Transmission System with Low Power Sleep Mode and Rapid-on-Capability	HK	ABANDONED	08110349.9	1/26/99	HK 1117978			7/28/11
6936-28-PEP-3-DIV-1	Multicarrier Transmission System with Low Power Sleep Mode and Rapid-on-Capability	EP	EXPIRED	10011996.5	1/26/99	2302857	2302857	9/2/15	1/26/19
6936-28-PEP-3-DIV-1-DE	Multicarrier Transmission System with Low Power Sleep Mode and Rapid-on-Capability	DE	EXPIRED	10011996.5	1/26/99		2302857	9/2/15	1/26/19
6936-28-PEP-3-DIV-1-FR	Multicarrier Transmission System with Low Power Sleep Mode and Rapid-on-Capability	FR	EXPIRED	10011996.5	1/26/99		2302857	9/2/15	1/26/19
6936-28-PEP-3-DIV-1-GB	Multicarrier Transmission System with Low Power Sleep Mode and Rapid-on-Capability	GB	EXPIRED	10011996.5	1/26/99		2302857	9/2/15	1/26/19
6936-28-PEP-3-DIV-2	Multicarrier Transmission System with Low Power Sleep Mode and Rapid-on-Capability	EP	EXPIRED	10012013.8	1/26/99	2330749	2330749	4/30/14	1/26/19
6936-28-PEP-3-DIV-2-DE	Multicarrier Transmission System with Low Power Sleep Mode and Rapid-on-Capability	DE	EXPIRED	10012013.8	1/26/99		2330749	4/30/14	1/26/19
6936-28-PEP-3-DIV-2-FR	Multicarrier Transmission System with Low Power Sleep Mode and Rapid-on-Capability	FR	EXPIRED	10012013.8	1/26/99		2330749	4/30/14	1/26/19

6936-28-PEP-3-DIV-2-GB	Multicarrier Transmission System with Low Power Sleep Mode and Rapid-on-Capability	GB	EXPIRED	10012013.8	1/26/99		2330749	4/30/14	1/26/19
6936-28-PJP	MULTICARRIER TRANSMISSION SYSTEM WITH LOW POWER SLEEP MODE AND RAPID-ON CAPABILITY	JP	EXPIRED	2000-596705	1/26/99	2003-518341	4282907	3/27/09	1/26/19
6936-28-PJP-DIV	MULTICARRIER TRANSMISSION SYSTEM WITH LOW POWER SLEEP MODE AND RAPID-ON CAPABILITY	JP	ABANDONED	2008-323651	1/26/99	N/A			1/26/19
6936-28-PKR	MULTICARRIER TRANSMISSION SYSTEM WITH LOW POWER SLEEP MODE AND RAPID-ON CAPABILITY	KR	ABANDONED	7009402/2001	1/26/99	10-2001-0108132			5/15/06
6936-28-PROV	MULTICARRIER TRANSMISSION SYSTEM WITH LOW POWER SLEEP MODE AND RAPID-ON CAPABILITY	US	EXPIRED	60/072,447	1/26/98	N/A			1/26/99
6936-55-PAU	Initialization in the Presence of Impulse Noise	AU	ISSUED	2005295758	10/14/05	AU 2005295758	2005295758	7/9/10	10/14/25
6936-55-PAU-2	Initialization in the Presence of Impulse Noise	AU	ABANDONED	2010202626	10/14/05	AU 2010202626			6/27/11
6936-55-PCA	DMT Symbol Repetition in the Presence of Impluse Noise	CA	ISSUED	2,582,106	10/14/05	2,582,106	2,582,106	4/28/15	10/14/25
6936-55-PCA-DIV	DMT Symbol Repetition in the Presence of Impluse Noise	CA	ABANDONED	2,881,036	10/14/05		2,881,036	12/22/15	9/8/20
6936-55-PCA-DIV-2	DMT Symbol Repetition in the Presence of Impluse Noise	CA	ABANDONED	2,906,478	10/14/05		2,906,478	1/8/19	10/14/25
6936-55-PCN	Initialization in the Presence of Impulse Noise	CN	ISSUED	200580034464.3	10/14/05	CN101040480A	200580034464.3	8/31/11	10/14/25
6936-55-PCN-HK	DMT Symbol Repetition in the Presence of Impulse Noise	HK	ISSUED	08102934.7	10/14/05	HK 1108783	HK1108783	12/16/11	10/14/25
6936-55-PCT	DMT Symbol Repetition in the Presence of Impluse Noise	WO	NAT PHASE	PCT/US05/36815	10/14/05	WO 2006/044533 A1			
6936-55-PEP	DMT SYMBOL REPETITION IN THE PRESENCE OF IMPULSE NOISE	EP	ISSUED	05810124.7	10/14/05	1800427	1800427	6/20/12	10/14/25
6936-55-PEPBE	Initialization in the Presence of Impulse Noise	BE	ISSUED	05810124.7	10/14/05		1800427	6/20/12	10/14/25
6936-55-PEPCH	Initialization in the Presence of Impulse Noise	CH	ABANDONED	05810124.7	10/14/05		1800427	6/20/12	9/8/20
6936-55-PEPDE	Initialization in the Presence of Impulse Noise	DE	ISSUED	05810124.7	10/14/05		1800427	6/20/12	10/14/25
6936-55-PEPDK	Initialization in the Presence of Impulse Noise	DK	ABANDONED	05810124.7	10/14/05		1800427	6/20/12	10/14/25
6936-55-PEPES	Initialization in the Presence of Impulse Noise	ES	ISSUED	05810124.7	10/14/05		1800427	6/20/12	10/14/25
6936-55-PEPFR	Initialization in the Presence of Impulse Noise	FR	ISSUED	05810124.7	10/14/05		1800427	6/20/12	10/14/25
6936-55-PEPGB	Initialization in the Presence of Impulse Noise	GB	ISSUED	05810124.7	10/14/05		1800427	6/20/12	10/14/25
6936-55-PEPHK	Initialization in the Presence of Impulse Noise	HK	ISSUED	07112380.6	10/14/05	HK 1103889	1103889	12/28/12	10/14/25
6936-55-PEPIT	Initialization in the Presence of Impulse Noise	IT	ISSUED	05810124.7	10/14/05		1800427	6/20/12	10/14/25
6936-55-PEPNL	Initialization in the Presence of Impulse Noise	NL	ISSUED	05810124.7	10/14/05		1800427	6/20/12	10/14/25
6936-55-PEPSE	Initialization in the Presence of Impulse Noise	SE	ABANDONED	05810124.7	10/14/05		1800427	6/20/12	10/14/25
6936-55-PEP-DIV	Initialization in the Presence of Impulse Noise	EP	ISSUED	11000980.0	10/14/05	2312784	2312784	2/1/17	10/14/25
6936-55-PEP-DIV-DE	Initialization in the Presence of Impulse Noise	DE	ISSUED	11000980.0	10/14/05		2312784	2/1/17	10/14/25
6936-55-PEP-DIV-FR	Initialization in the Presence of Impulse Noise	FR	ISSUED	11000980.0	10/14/05		2312784	2/1/17	10/14/25
6936-55-PEP-DIV-GB	Initialization in the Presence of Impulse Noise	GB	ISSUED	11000980.0	10/14/05		2312784	2/1/17	10/14/25
6936-55-PEP-DIV-2	Initialization in the Presence of Impulse Noise	EP	PUBLISHED	17020039.8	10/14/05	3220567			10/14/25
6936-55-PEP-DIV-2-HK	Initialization in the Presence of Impulse Noise	HK	PUBLISHED	18100419.3	10/14/15	1241167			10/14/35
6936-55-PIN	Initialization in the Presence of Impulse Noise	IN	ABANDONED	1209/KOLNP/2007	10/14/05	IN 1209/KOLNP/2007			10/15/24
6936-55-PJP	DMT Symbol Repetition in the Presense of Impulse Noise	JP	ABANDONED	2007-536883	10/14/05	2008-517535			4/15/13
6936-55-PJP-DIV	DMT Symbol Repetition in the Presense of Impulse Noise	JP	ABANDONED	2008-264567	10/14/05	2009-081862			4/15/13
6936-55-PKR	DMT SYMBOL REPETITION IN THE PRESENCE OF IMPULSE NOISE	KR	ISSUED	10-2007-7008275	10/14/05	10-2007-0061867	10-1272404	5/31/13	10/14/25
6936-55-PKR-DIV	DMT Symbol Repetition in the Presence of Impulse Noise	KR	ISSUED	10-2010-7022479	10/14/05	10-2010/0121542	10-1314976	9/27/13	10/14/25
6936-55-PKR-DIV-2	DMT Symbol Repetition in the Presence of Impulse Noise	KR	ABANDONED	10-2012-7021605	10/14/05				4/16/13
6936-55-PROV	XDSL INITIALIZATION IN THE PRESENCE OF IMPULSE NOISE	US	EXPIRED	60/619,618	10/15/04	N/A			10/15/05
6936-55-PUS	DMT Symbol Repetition in the Presence of Impulse Noise	US	ISSUED	11/575,598	3/20/07	US 2007-0217491 A1	7,796,705	9/14/10	8/22/27
6936-55-PUS-CON	Impulse Noise Protection During Initialization	US	ISSUED	12/769,747	4/29/10	US 2010-0208842 A1	8,913,649	12/16/14	10/14/25
6936-55-PUS-CON-2	DMT Symbol Repetition in the Presence of Impulse Noise	US	ISSUED	14/559,156	12/3/14	US 2015-0146821 A1	9,621,198	4/11/17	10/14/25
6936-55-PUS-CON-3	DMT SYMBOL REPETITION IN THE PRESENCE OF IMPULSE NOISE	US	ABANDONED	15/479,866	4/5/17	US 2017-0214487 A1			9/12/19
6936-55-PUS-CON-4	DMT SYMBOL REPETITION IN THE PRESENCE OF IMPULSE NOISE	US	PUBLISHED	16/569,144	9/12/19	US 2020-0007268 A1			10/14/25
6936-57-PAU	Packet Retransmission and Memory Sharing	AU	ABANDONED	2007257055	4/12/07	AU 2007257055			4/12/27
6936-57-PBR	Packet Retransmission and Memory Sharing	BR	ISSUED	PI-0709871-5	4/12/07	BR PI0709871	PI 0709871-5	10/15/19	10/15/29
6936-57-PCA	Packet Retransmission and Memory Sharing	CA	ISSUED	2,647,589	4/12/07	CA 2647589	2,647,589	8/21/18	4/12/27

6936-57-PCA-DIV	Packet Retransmission and Memory Sharing	CA	PENDING	3,011,163	4/12/07				4/12/27
6936-57-PCN	Packet Retransmission and Memory Sharing	CN	ABANDONED	200780012891.0	4/12/07	CN101421992A			4/16/13
6936-57-PCN-HK	Packet Retransmission and Memory Sharing	HK	ABANDONED	09109954.6	4/12/07	HK 1133132			4/16/13
6936-57-PCO	Packet Retransmission and Memory Sharing	CO	ABANDONED	08-109.377	4/12/07	08-109.377			4/12/27
6936-57-PCT	Packet Retransmission and Memory Sharing	WO	NAT PHASE	PCT/US07/66522	4/12/07	WO 2007/143277			
6936-57-PEP	Packet Retransmission and Memory Sharing	EP	ISSUED	07811844.5	4/12/07	2005674	2005674	9/28/16	4/12/27
6936-57-PEP-DE	Packet Retransmission and Memory Sharing	DE	ISSUED	07811844.5	4/12/07		2005674	9/28/16	4/12/27
6936-57-PEP-FR	Packet Retransmission and Memory Sharing	FR	ISSUED	07811844.5	4/12/07		2005674	9/28/16	4/12/27
6936-57-PEP-GB	Packet Retransmission and Memory Sharing	GB	ISSUED	07811844.5	4/12/07		2005674	9/28/16	4/12/27
6936-57-PEP-DIV	Packet Retransmission and Memory Sharing	EP	ISSUED	10000017.3	4/12/07	2178254	2178254	2/8/17	4/12/27
6936-57-PEP-DIV-DE	Packet Retransmission and Memory Sharing	DE	ISSUED	10000017.3	4/12/07		2178254	2/8/17	4/12/27
6936-57-PEP-DIV-FR	Packet Retransmission and Memory Sharing	FR	ISSUED	10000017.3	4/12/07		2178254	2/8/17	4/12/27
6936-57-PEP-DIV-GB	Packet Retransmission and Memory Sharing	GB	ISSUED	10000017.3	4/12/07		2178254	2/8/17	4/12/27
6936-57-PEP-DIV-HK	Packet Retransmission and Memory Sharing	HK	ABANDONED	10104429.1	4/12/07	HK 1136723			10/26/16
6936-57-PEP-DIV-2	Packet Retransmission and Memory Sharing	EP	ISSUED	10000016.5	4/12/07	2173071	2173071	6/26/13	4/12/27
6936-57-PEP-DIV-2-BE	Packet Retransmission and Memory Sharing	BE	ABANDONED	10000016.5	4/12/07		2173071	6/26/13	1/13/17
6936-57-PEP-DIV-2-DE	Packet Retransmission and Memory Sharing	DE	ABANDONED	10000016.5	4/12/07		2173071	6/26/13	1/13/17
6936-57-PEP-DIV-2-FR	Packet Retransmission and Memory Sharing	FR	ABANDONED	10000016.5	4/12/07		2173071	6/26/13	1/13/17
6936-57-PEP-DIV-2-GB	Packet Retransmission and Memory Sharing	GB	ABANDONED	10000016.5	4/12/07		2173071	6/26/13	1/13/17
6936-57-PEP-DIV-2-HK	Packet Retransmission and Memory Sharing	HK	ABANDONED	10103698.7	4/12/07	HK 1135537	1135537	11/15/13	1/13/17
6936-57-PEP-DIV-3	Packet Retransmission and Memory Sharing	EP	ISSUED	17020026.5	4/12/07	3190756	3190756	10/31/18	4/12/27
6936-57-PEP-DIV-3-DE	Packet Retransmission and Memory Sharing	DE	ISSUED	17020026.5	4/12/07		3190756	10/31/18	4/12/27
6936-57-PEP-DIV-3-FR	Packet Retransmission and Memory Sharing	FR	ISSUED	17020026.5	4/12/07		3190756	10/31/18	4/12/27
6936-57-PEP-DIV-3-GB	Packet Retransmission and Memory Sharing	GB	ISSUED	17020026.5	4/12/07		3190756	10/31/18	4/12/27
6936-57-PEP-DIV-4	Packet Retransmission and Memory Sharing	EP	PUBLISHED	17020525.6	4/12/07	3301871			4/12/27
6936-57-PEP-DIV-4-HK	Packet Retransmission and Memory Sharing	HK	PENDING	18110134.6	4/12/07				4/12/27
6936-57-PIN	Packet Retransmission and Memory Sharing	IN	ABANDONED	4084/KOLNP/2008	4/12/07	IN 4084/KOLNP/2008			4/12/27
6936-57-PJP	6936and Memory Sharing	JP	ABANDONED	2009-505623	4/12/07	2009-533973			2/27/12
6936-57-PJP-DIV	Packet Retransmission and Memory Sharing	JP	ABANDONED	2010-017356	4/12/07	2010-136427			10/2/12
6936-57-PJP-DIV-2	Packet Retransmission and Memory Sharing	JP	ISSUED	2012-042978	4/12/07	2012-151863	5486621	2/28/14	4/12/27
6936-57-PJP-DIV-3	Packet Retransmission and Memory Sharing	JP	ISSUED	2013-246257	4/12/07	2014-090433	5948307	6/10/16	4/12/27
6936-57-PKR	Packet Retransmission and Memory Sharing	KR	ISSUED	10-2008-7024792	4/12/07	10-2008-0108127	10-1736999	5/11/17	4/12/27
6936-57-PKR-DIV	Packet Retransmission and Memory Sharing	KR	ABANDONED	10-2014-7005299	4/12/07				6/20/16
6936-57-PKR-DIV-2	Packet Retransmission and Memory Sharing	KR	ABANDONED	10-2017-7012757	4/12/07				1/12/18
6936-57-PKR-DIV-3	Packet Retransmission and Memory Sharing	KR	ISSUED	10-2017-7036067	4/12/07		10-1952812	2/21/19	4/12/27
6936-57-PKR-DIV-4	Packet Retransmission and Memory Sharing	KR	ISSUED	10-2019-7005116	4/12/07		10-2151398	8/28/20	4/12/27
6936-57-PMX	Packet Retransmission and Memory Sharing	MX	ISSUED	MX/a/2008/012505	4/12/07	MX 2008012505	301471	7/18/12	4/12/27
6936-57-PMX-DIV	Packet Retransmission and Memory Sharing	MX	ABANDONED	MX/a/2011/005751	4/12/07				4/12/27
6936-57-PROV	XDSL PACKET RETRANSMISSION MECHANISM	US	EXPIRED	60/792,236	4/12/06	N/A			4/12/07
6936-57-PUS	Packet Retransmission and Memory Sharing	US	ISSUED	12/295,828	10/2/08	US 2009-0300450 A1	8,335,956	12/18/12	10/11/25
6936-57-PUS-CON	Packet Retransmission and Memory Sharing	US	ISSUED	12/783,758	5/20/10	US 2011-0002331 A1	8,407,546	3/26/13	7/23/28
6936-57-PUS-CON-2	Packet Retransmission and Memory Sharing	US	ISSUED	13/766,059	2/13/13	US 2013-0163592 A1	8,645,784	2/4/14	4/12/27
6936-57-PUS-CON-3	Packet Retransmission and Memory Sharing	US	ISSUED	14/159,125	1/20/14	US 2014-0133491 A1	9,485,055	11/1/16	4/12/27
6936-57-PUS-CON-4	PACKET RETRANSMISSION AND MEMORY SHARING	US	ISSUED	15/298,526	10/20/16	US 2017-0041224 A1	10,044,473	8/7/18	4/12/27
6936-57-PUS-CON-5	PACKET RETRANSMISSION AND MEMORY SHARING	US	ISSUED	16/046,494	7/26/18	US 2018-0331790 A1	10,484,140	11/19/19	10/11/25
6936-57-PUS-CON-6	PACKET RETRANSMISSION AND MEMORY SHARING	US	PUBLISHED	16/561,835	9/5/19	US 2019-0393991 A1			4/12/27
6936-57-PUS-DIV	Packet Retransmission	US	ISSUED	12/760,728	4/15/10	US 2010-0205501 A1	8,595,577	11/26/13	8/28/27
6936-57-PUS-DIV-CON	Packet Retransmission	US	ISSUED	12/783,765	5/20/10	US 2010-0332935 A1	8,468,411	6/18/13	10/11/25
6936-57-PUS-DIV-CON-2	Packet Retransmission	US	ISSUED	14/075,194	11/8/13	US 2014-0068366 A1	9,094,348	7/28/15	4/12/27
6936-57-PUS-DIV-CON-3	Packet Retransmission	US	ISSUED	14/742,334	6/17/15	US 2015-0312001 A1	9,749,235	8/29/17	4/12/27

6936-57-PUS-DIV-CON-4	Packet Retransmission	US	ISSUED	15/678,870	8/16/17	US 2017-0373971 A1	10,498,495	12/3/19	4/12/27
6936-57-PUS-DIV-CON-5	TECHNIQUES FOR PACKET AND MESSAGE COMMUNICATION IN A MULTICARRIER TRANSCEIVER ENVIRONMENT	US	ISSUED	16/701,343	12/3/19	US 2020-0106558 A1	10,833,809	11/10/20	4/12/27
6936-57-PUS-DIV-CON-6	PACKET RETRANSMISSION	US	PENDING	17/027,196	9/21/20				4/12/27
6936-59-PROV	xDSL Packet Retransmission Mechanism With Examples	US	EXPIRED	60/849,650	10/5/06	N/A			10/5/07
6936-26	SYSTEMS AND METHODS FOR A MULTICARRIER MODULATION SYSTEM WITH A VARIABLE MARGIN	US	ABANDONED	09/836,295	4/18/01	US 2002-0009155			10/4/05
6936-26-CON	SYSTEMS AND METHODS FOR A MULTICARRIER MODULATION SYSTEM WITH A VARIABLE MARGIN	US	ABANDONED	11/242,024	10/4/05	US 2006-0018395 A1			4/18/21
6936-26-CON-2	Systems and Methods for a Multicarrier Modulation System with a Variable Margin	US	ABANDONED	11/972,340	1/10/08	US 2008-0107204 A1			7/27/11
6936-26-CON-3	Systems and Methods for a Multicarrier Modulation System with a Variable Margin	US	ISSUED	12/694,143	1/26/10	US 2010-0128810 A1	8,374,226	2/12/13	7/3/21
6936-26-CON-4	Systems and Methods for a Multicarrier Modulation System with a Variable Margin	US	ABANDONED	13/467,392	5/9/12	US 2012-0219047 A1			4/18/21
6936-26-CON-5	Systems and Methods for a Multicarrier Modulation System with a Variable Margin	US	ISSUED	13/764,529	2/11/13	US 2013-0148708 A1	8,625,660	1/7/14	4/18/21
6936-26-CON-6	Systems and Methods for a Multicarrier Modulation System with a Variable Margin	US	ISSUED	14/079,285	11/13/13	US 2014-0072062 A1	8,937,988	1/20/15	4/18/21
6936-26-CON-7	Systems and Methods for a Multicarrier Modulation System with a Variable Margin	US	ISSUED	14/591,612	1/7/15	US 2015-0117557 A1	9,154,354	10/6/15	4/18/21
6936-26-CON-8	SYSTEMS AND METHODS FOR A MULTICARRIER MODULATION SYSTEM WITH A VARIABLE MARGIN	US	ABANDONED	14/865,966	9/25/15	US 2016-0013962 A1			12/13/16
6936-26-CON-9	SYSTEMS AND METHODS FOR A MULTICARRIER MODULATION SYSTEM WITH A VARIABLE MARGIN	US	ISSUED	15/348,372	11/10/16	US 2017-0078129 A1	9,893,921	2/13/18	4/18/21
6936-26-CON-10	SYSTEMS AND METHODS FOR A MULTICARRIER MODULATION SYSTEM WITH A VARIABLE MARGIN	US	ISSUED	15/886,295	2/1/18	US 2018-0159711 A1	10,708,104	7/7/20	4/18/21
6936-26-PAU	MULTICARRIER MODULATION SYSTEM WITH VARIABLE MARGIN TO ACCOUNT FORTIME VARYING IMPAIRMENTS	AU	ABANDONED	2001257081	4/18/01	N/A			
6936-26-PAU-CON	Data Allocation with Variable SNR Margins	AU	ISSUED	2007200448	4/18/01	AU 2007200448	2007200448	8/6/09	4/18/21
6936-26-PAU-CON-2	Data Allocation with Variable SNR Margins	AU	ABANDONED	2009202880	4/18/05	AU 2009202880			10/18/11
6936-26-PCA	MULTICARRIER MODULATION SYSTEM WITH VARIABLE MARGIN TO ACCOUNT FORTIME VARYING IMPAIRMENTS	CA	ISSUED	2,406,151	4/18/01	CA 2405151	2,406,151	4/13/10	4/18/21
6936-26-PCA-2	DATA ALLOCATION WITH VARIABLE SNR MARGINS	CA	ABANDONED	2,689,952	4/18/01	CA 689952			2/24/11
6936-26-PCT	MULTICARRIER MODULATION SYSTEM WITH VARIABLE MARGIN TO ACCOUNT FORTIME VARYING IMPAIRMENTS	WO	NAT PHASE	PCT/US01/12555	4/18/01	WO 2001/080510			
6936-26-PEP	MULTICARRIER MODULATION SYSTEM WITH VARIABLE MARGIN TO ACCOUNT FORTIME VARYING IMPAIRMENTS	EP	ABANDONED	01930554.9	4/18/01	EP 1275229	1275229	3/21/07	4/18/21
6936-26-PEPBE	Data Allocation With Variable SNR Margins	BE	ABANDONED	01930554.9	4/18/01	N/A	1275229	3/21/07	4/18/21
6936-26-PEPDE	Data Allocation With Variable SNR Margins	DE	ABANDONED	01930554.9	4/18/01	N/A	1275229	3/21/07	4/18/21
6936-26-PEPFR	Data Allocation With Variable SNR Margins	FR	ABANDONED	01930554.9	4/18/01	N/A	1275229	3/21/07	4/18/21
6936-26-PEPGB	Data Allocation With Variable SNR Margins	GB	ABANDONED	01930554.9	4/18/01	N/A	1275229	3/21/07	4/18/21
6936-26-PEP-DIV	Data Allocation With Variable SNR Margins	EP	ISSUED	07005676.7	4/18/01	1830535	1830535	6/15/11	4/18/21
6936-26-PEP-DIV-BE	Data Allocation With Variable SNR Margins	BE	ISSUED	07005676.7	4/18/01	N/A	1830535	9/5/07	4/18/21
6936-26-PEP-DIV-DE	Data Allocation With Variable SNR Margins	DE	ISSUED	07005676.7	4/18/01		1830535	6/15/11	4/18/21
6936-26-PEP-DIV-FR	Data Allocation With Variable SNR Margins	FR	ISSUED	07005676.7	4/18/01	N/A	1830535	9/5/07	4/18/21
6936-26-PEP-DIV-GB	Data Allocation With Variable SNR Margins	GB	ISSUED	07005676.7	4/18/01	N/A	1830535	9/5/07	4/18/21
6936-26-PEP-DIV-2	MULTICARRIER MODULATION SYSTEM WITH VARIABLE MARGIN TO ACCOUNT FORTIME VARYING IMPAIRMENTS	EP	ABANDONED	10011998.1	4/18/01	2267963			4/18/21
6936-26-PJP	MULTICARRIER MODULATION SYSTEM WITH VARIABLE MARGIN TO ACCOUNT FORTIME VARYING IMPAIRMENTS	JP	ABANDONED	2001-576639	4/18/01	2004-501535			4/18/21
6936-26-PKR	MULTICARRIER MODULATION SYSTEM WITH VARIABLE MARGIN TO ACCOUNT FORTIME VARYING IMPAIRMENTS	KR	ABANDONED	2002-7013983	4/18/01	10-2002-087990			4/18/21
6936-26-PROV	MULTICARRIER MODULATION SYSTEM WITH VARIABLE MARGIN TO ACCOUNT FORTIME VARYING IMPAIRMENTS	US	EXPIRED	60/197,727	4/18/00	N/A			4/18/01

6936-7-CON	MULTICARRIER COMMUNICATION WITH VARIABLE OVERHEAD RATE	US	ABANDONED	10/202,688	7/25/02	US 2003-0007509			7/13/06
6936-7-PAU	MULTICARRIER COMMUNICATION WITH VARIABLE OVERHEAD RATE	AU	EXPIRED	48339/99	6/25/99	AU 4833999	750898	11/21/02	6/25/19
6936-7-PAU-2	MULTICARRIER COMMUNICATION WITH VARIABLE OVERHEAD RATE	AU	EXPIRED	2002301627	6/25/99	AU 2002301627	2002301627	8/6/04	6/25/19
6936-7-PAU-3	MULTICARRIER COMMUNICATION WITH VARIABLE OVERHEAD RATE	AU	ABANDONED	2004203322	6/25/99	AU 2004203322	2004203322	10/11/07	5/4/17
6936-7-PAU-4	Multicarrier Communication With Variable Overhead Rate	AU	ABANDONED	2007202930	6/25/99	AU 2007202930			6/25/19
6936-7-PAU-4-DIV	Multicarrier Communication With Variable Overhead Rate	AU	ABANDONED	2010249199	6/25/99	AU 2010249199			6/25/19
6936-7-PCA	MULTICARRIER COMMUNICATION WITH VARIABLE OVERHEAD RATE	CA	ABANDONED	2,335,865	6/25/99	CA 2335865	2,335,865	12/16/08	3/10/17
6936-7-PCA-DIV	MULTICARRIER COMMUNICATION WITH VARIABLE OVERHEAD RATE	CA	EXPIRED	2,641,978	6/25/99	CA 2641978	2,641,978	1/6/15	6/25/19
6936-7-PCA-DIV-2	MULTICARRIER COMMUNICATION WITH VARIABLE OVERHEAD RATE	CA	EXPIRED	2,867,539	6/25/99		2,867,539	3/14/17	6/25/19
6936-7-PCT	MULTICARRIER COMMUNICATION WITH VARIABLE OVERHEAD RATE	WO	NAT PHASE	PCT/US99/14467	6/25/99	WO 2000/001127			
6936-7-PEP-2	MULTICARRIER COMMUNICATION WITH VARIABLE OVERHEAD RATE	EP	EXPIRED	04012683.1	6/25/99	1453268	1453268	3/8/06	6/25/19
6936-7-PEPAT-2	MULTICARRIER COMMUNICATION WITH VARIABLE OVERHEAD RATE	AT	EXPIRED	04012683.1	6/25/99	N/A	1453268	3/8/06	6/25/19
6936-7-PEPBE-2	MULTICARRIER COMMUNICATION WITH VARIABLE OVERHEAD RATE	BE	EXPIRED	04012683.1	6/25/99	N/A	1453268	3/8/06	6/25/19
6936-7-PEPCH-2	MULTICARRIER COMMUNICATION WITH VARIABLE OVERHEAD RATE	CH	EXPIRED	04012683.1	6/25/99	N/A	1453268	3/8/06	6/25/19
6936-7-PEPDE-2	Multicarrier Communication With Variable Overhead Rate	DE	EXPIRED	04012683.1	6/25/99	N/A	1453268	3/8/06	6/25/19
6936-7-PEPES-2	MULTICARRIER COMMUNICATION WITH VARIABLE OVERHEAD RATE	ES	EXPIRED	04012683.1	6/25/99	N/A	1453268	3/8/06	6/25/19
6936-7-PEPFI-2	MULTICARRIER COMMUNICATION WITH VARIABLE OVERHEAD RATE	FI	EXPIRED	04012683.1	6/25/99	N/A	1453268	3/8/06	6/25/19
6936-7-PEPFR-2	MULTICARRIER COMMUNICATION WITH VARIABLE OVERHEAD RATE	FR	EXPIRED	04012683.1	6/25/99	N/A	1453268	3/8/06	6/25/19
6936-7-PEPGB-2	MULTICARRIER COMMUNICATION WITH VARIABLE OVERHEAD RATE	GB	EXPIRED	04012683.1	6/25/99	N/A	1453268	3/8/06	6/25/19
6936-7-PEPGR-2	MULTICARRIER COMMUNICATION WITH VARIABLE OVERHEAD RATE	GR	EXPIRED	04012683.1	6/25/99	N/A	1453268	3/8/06	6/25/19
6936-7-PEPHK-2	MULTICARRIER COMMUNICATION WITH VARIABLE OVERHEAD RATE	HK	EXPIRED	05101665.7	6/25/99	HK 1068080	HK1068080	5/6/06	6/25/19
6936-7-PEPIE-2	MULTICARRIER COMMUNICATION WITH VARIABLE OVERHEAD RATE	IE	EXPIRED	04012683.1	6/25/99	N/A	1453268	3/8/06	6/25/19
6936-7-PEPIT-2	MULTICARRIER COMMUNICATION WITH VARIABLE OVERHEAD RATE	IT	EXPIRED	04012683.1	6/25/99	N/A	1453268	3/8/06	6/25/19
6936-7-PEPNL-2	MULTICARRIER COMMUNICATION WITH VARIABLE OVERHEAD RATE	NL	EXPIRED	04012683.1	6/25/99	N/A	1453268	3/8/06	6/25/19
6936-7-PEPSE-2	MULTICARRIER COMMUNICATION WITH VARIABLE OVERHEAD RATE	SE	EXPIRED	04012683.1	6/25/99	N/A	1453268	3/8/06	6/25/19
6936-7-PEP-3	MULTICARRIER COMMUNICATION WITH VARIABLE OVERHEAD RATE	EP	EXPIRED	06004566.3	6/25/99	EP 1667392	1667392	1/10/18	6/25/19
6936-7-PEP-3-DE	MULTICARRIER COMMUNICATION WITH VARIABLE OVERHEAD RATE	DE	EXPIRED	06004566.3	6/25/99		1667392	1/10/18	6/25/19
6936-7-PEP-3-FR	MULTICARRIER COMMUNICATION WITH VARIABLE OVERHEAD RATE	FR	EXPIRED	06004566.3	6/25/99		1667392	1/10/18	6/25/19
6936-7-PEP-3-GB	MULTICARRIER COMMUNICATION WITH VARIABLE OVERHEAD RATE	GB	EXPIRED	06004566.3	6/25/99		1667392	1/10/18	6/25/19
6936-7-PEP-3-HK	MULTICARRIER COMMUNICATION WITH VARIABLE OVERHEAD RATE	HK	EXPIRED	06112790.1	6/25/99	1091070	HK1091070	6/22/18	6/25/19
6936-7-PEP-3-DIV-1	MULTICARRIER COMMUNICATION WITH VARIABLE OVERHEAD RATE	EP	EXPIRED	10011974.2	6/25/99	2278765	2278765	11/7/18	6/25/19
6936-7-PEP-3-DIV-1-AT	MULTICARRIER COMMUNICATION WITH VARIABLE OVERHEAD RATE	AT	EXPIRED	10011974.2	6/25/99		2278765	11/7/18	6/25/19
6936-7-PEP-3-DIV-1-BE	MULTICARRIER COMMUNICATION WITH VARIABLE OVERHEAD RATE	BE	EXPIRED	10011974.2	6/25/99		2278765	11/7/18	6/25/19
6936-7-PEP-3-DIV-1-CH	MULTICARRIER COMMUNICATION WITH VARIABLE OVERHEAD RATE	CH	EXPIRED	10011974.2	6/25/99		2278765	11/7/18	6/25/19
6936-7-PEP-3-DIV-1-DE	MULTICARRIER COMMUNICATION WITH VARIABLE OVERHEAD RATE	DE	EXPIRED	10011974.2	6/25/99	2278765	DE 699 45 900.1	11/7/18	6/25/19
6936-7-PEP-3-DIV-1-ES	MULTICARRIER COMMUNICATION WITH VARIABLE OVERHEAD RATE	ES	EXPIRED	10011974.2	6/25/99		2278765	11/7/18	6/25/19
6936-7-PEP-3-DIV-1-FI	MULTICARRIER COMMUNICATION WITH VARIABLE OVERHEAD RATE	FI	EXPIRED	10011974.2	6/25/99		2278765	11/7/18	6/25/19
6936-7-PEP-3-DIV-1-FR	MULTICARRIER COMMUNICATION WITH VARIABLE OVERHEAD RATE	FR	EXPIRED	10011974.2	6/25/99		2278765	11/7/18	6/25/19
6936-7-PEP-3-DIV-1-GB	MULTICARRIER COMMUNICATION WITH VARIABLE OVERHEAD RATE	GB	EXPIRED	10011974.2	6/25/99		2278765	11/7/18	6/25/19
6936-7-PEP-3-DIV-1-GR	MULTICARRIER COMMUNICATION WITH VARIABLE OVERHEAD RATE	GR	EXPIRED	10011974.2	6/25/99		2278765	11/7/18	6/25/19
6936-7-PEP-3-DIV-1-IE	MULTICARRIER COMMUNICATION WITH VARIABLE OVERHEAD RATE	IE	EXPIRED	10011974.2	6/25/99		2278765	11/7/18	6/25/19
6936-7-PEP-3-DIV-1-IT	MULTICARRIER COMMUNICATION WITH VARIABLE OVERHEAD RATE	IT	EXPIRED	10011974.2	6/25/99		2278765	11/7/18	6/25/19
6936-7-PEP-3-DIV-1-NL	MULTICARRIER COMMUNICATION WITH VARIABLE OVERHEAD RATE	NL	EXPIRED	10011974.2	6/25/99		2278765	11/7/18	6/25/19
6936-7-PEP-3-DIV-1-SE	MULTICARRIER COMMUNICATION WITH VARIABLE OVERHEAD RATE	SE	EXPIRED	10011974.2	6/25/99		2278765	11/7/18	6/25/19
6936-7-PEP-3-DIV-2	MULTICARRIER COMMUNICATION WITH VARIABLE OVERHEAD RATE	EP	EXPIRED	10011980.9	6/25/99	2278766	2278766	11/7/18	6/25/19
6936-7-PEP-3-DIV-2-DE	MULTICARRIER COMMUNICATION WITH VARIABLE OVERHEAD RATE	DE	EXPIRED	10011980.9	6/25/99	2278766	DE 699 45 902.8	11/7/18	6/25/19
6936-7-PEP-3-DIV-2-FR	MULTICARRIER COMMUNICATION WITH VARIABLE OVERHEAD RATE	FR	EXPIRED	10011980.9	6/25/99		2278766	11/7/18	6/25/19
6936-7-PEP-3-DIV-2-GB	MULTICARRIER COMMUNICATION WITH VARIABLE OVERHEAD RATE	GB	EXPIRED	10011980.9	6/25/99		2278766	11/7/18	6/25/19

6936-7-PEP-3-DIV-3	MULTICARRIER COMMUNICATION WITH VARIABLE OVERHEAD RATE	EP	EXPIRED	10011981.7	6/25/99	2278767	2278767	11/7/18	6/25/19
6936-7-PEP-3-DIV-3-DE	MULTICARRIER COMMUNICATION WITH VARIABLE OVERHEAD RATE	DE	EXPIRED	10011981.7	6/25/99	2278767	DE 699 45 903.6	11/7/18	6/25/19
6936-7-PEP-3-DIV-3-FR	MULTICARRIER COMMUNICATION WITH VARIABLE OVERHEAD RATE	FR	EXPIRED	10011981.7	6/25/99		2278767	11/7/18	6/25/19
6936-7-PEP-3-DIV-3-GB	MULTICARRIER COMMUNICATION WITH VARIABLE OVERHEAD RATE	GB	EXPIRED	10011981.7	6/25/99		2278767	11/7/18	6/25/19
6936-7-PKR	MULTICARRIER COMMUNICATION WITH VARIABLE OVERHEAD RATE	KR	ABANDONED	2000-7014830	6/25/99	10-2001-0053220	10-0955169	4/20/10	3/10/17
6936-7-PKR-2	MULTICARRIER COMMUNICATION WITH VARIABLE OVERHEAD RATE	KR	EXPIRED	10-2010-7002843	6/25/99	10-2010-0031635	10-1006609	12/30/10	6/25/19
6936-7-PKR-3	MULTICARRIER COMMUNICATION WITH VARIABLE OVERHEAD RATE	KR	ABANDONED	10-2010-7021589	6/25/99	10-2010-0121683			6/25/19
6936-7-PROV	MULTICARRIER COMMUNICATION WITH VARIABLE OVERHEAD RATE	US	EXPIRED	60/090,891	6/26/98	N/A			6/26/99
6936-3	SYSTEM AND METHOD FOR THE APPLICATION OF AN LMS METHOD TO UPDATING AN ECHO CANCELLER IN AN ADSL MODEM	US	ABANDONED	09/768,275	1/25/01	US 2001-0040875			8/25/05
6936-3-CON	SYSTEM AND METHOD FOR THE APPLICATION OF AN LMS METHOD TO UPDATING AN ECHO CANCELLER IN AN ADSL MODEM	US	ABANDONED	11/058,289	2/16/05	US 2005-0141441 A1			5/9/06
6936-3-CON-2	SYSTEM AND METHOD FOR THE APPLICATION OF AN LMS METHOD TO UPDATING AN ECHO CANCELLER IN AN ADSL MODEM	US	ABANDONED	11/430,251	5/9/06	US 2006-0215587 A1			12/10/10
6936-3-CON-3	SYSTEM AND METHOD FOR THE APPLICATION ON AN LMS METHOD TO UPDATING AN ECHO CANCELLER IN AN ADSL MODEM	US	ISSUED	12/783,740	5/20/10	US 2010-0296663 A1	8,391,191	3/5/13	1/29/21
6936-3-CON-4	SYSTEM AND METHOD FOR THE APPLICATION OF AN LMS METHOD TO UPDATING AN ECHO CANCELLER IN AN ADSL MODEM	US	ABANDONED	12/783,744	5/20/10	N/A			2/18/11
6936-3-CON-5	SYSTEM AND METHOD FOR THE APPLICATION OF AN LMS METHOD TO UPDATING AN ECHO CANCELLER IN AN ADSL MODEM	US	ISSUED	13/772,516	2/21/13	US 2013-0163749 A1	8,649,305	2/11/14	1/25/21
6936-3-CON-6	System and Method for the Application of an LMS Method to Updating an Echo Canceller in an ADSL Modem	US	ISSUED	14/164,632	1/27/14	US 2014-0140499 A1	9,065,886	6/23/15	1/25/21
6936-3-CON-7	SYSTEM AND METHOD FOR THE APPLICATION OF AN LMS METHOD TO UPDATING AN ECHO CANCELLER IN A MULTICARRIER TRANSCEIVER	US	ABANDONED	14/724,345	5/28/15	US 2015-0288808 A1			11/4/16
6936-3-PAU	SYSTEM AND METHOD FOR THE APPLICATION OF AN LMS METHOD TO UPDATING AN ECHO CANCELLER COEFFICIENTS IN AN ADSL MODEM	AU	ABANDONED	32943/01	1/25/01	AU 3294301	783527	2/16/06	1/4/17
6936-3-PCA	System and Method for the Application of an LMS Method to Updating an Echo Canceller in an ADSL Modem	CA	ABANDONED	2,396,162	1/25/01	CA 2396162			4/25/12
6936-3-PCT	APPLICATION OF LMS METHOD TO UPDATING ECHO CANCELLER COEFFICIENTS IN ADSL MODEM	WO	NAT PHASE	PCT/US01/02341	1/25/01	WO 2001/056184			
6936-3-PEP	APPLICATION OF LMS METHOD TO UPDATING ECHO CANCELLER COEFFICIENTS IN ADSL MODEM	EP	ABANDONED	01905022.8	1/25/01	EP 1250766	1250766	9/17/08	12/12/19
6936-3-PEP-BE	APPLICATION OF LMS METHOD TO UPDATING ECHO CANCELLER COEFFICIENTS IN ADSL MODEM	BE	ABANDONED	01905022.8	1/25/01	N/A	1250766	9/17/08	12/12/19
6936-3-PEP-DE	APPLICATION OF LMS METHOD TO UPDATING ECHO CANCELLER COEFFICIENTS IN ADSL MODEM	DE	ABANDONED	01905022.8	1/25/01	N/A	1250766	9/17/08	12/12/19
6936-3-PEP-FR	APPLICATION OF LMS METHOD TO UPDATING ECHO CANCELLER COEFFICIENTS IN ADSL MODEM	FR	ABANDONED	01905022.8	1/25/01	N/A	1250766	9/17/08	12/12/19
6936-3-PEP-GB	APPLICATION OF LMS METHOD TO UPDATING ECHO CANCELLER COEFFICIENTS IN ADSL MODEM	GB	ABANDONED	01905022.8	1/25/01	N/A	1250766	9/17/08	12/12/19
6936-3-PEP-DIV	System and Method for the Application of an LMS Method to Updating an Echo Canceller in an ADSL Modem	EP	ABANDONED	08015818.1	1/25/01	1 995 884			1/25/21
6936-3-PEP-DIV-2	System and Method for the Application of an LMS Method to Updating an Echo Canceller in an ADSL Modem	EP	ABANDONED	10011999.9	1/25/01	2267913			1/25/21
6936-3-PJP	APPLICATION OF LMS METHOD TO UPDATING ECHO CANCELLER COEFFICIENTS IN ADSL MODEM	JP	ABANDONED	2001-555226	1/25/01	JP 2003-521194			1/25/21
6936-3-PKR	APPLICATION OF LMS METHOD TO UPDATING ECHO CANCELLER COEFFICIENTS IN ADSL MODEM	KR	ABANDONED	2002-7009465	1/25/01	10-2002-0069265			1/25/21
6936-3-PKR-DIV	APPLICATION OF LMS METHOD TO UPDATING ECHO CANCELLER COEFFICIENTS IN ADSL MODEM	KR	ABANDONED	10-2010-7006184	1/25/01	10-2010-0034063			1/25/21
6936-3-PROV	APPLICATION OF LMS METHOD TO UPDATING ECHO CANCELLER COEFFICIENTS IN ADSL MODEM	US	EXPIRED	60/177,944	1/25/00	N/A			1/25/01

6936-14	SYSTEMS AND METHODS FOR MULTICARRIER MODULATION USING MULTI-TAP FREQUENCY-DOMAIN EQUALIZER AND DECISION FEEDBACK	US	ISSUED	10/211,425	8/2/02	US 2003-0067865	6,760,373	7/6/04	8/2/22
6936-14-CON	SYSTEMS AND METHODS FOR MULTICARRIER MODULATION USING MULTI-TAP FREQUENCY-DOMAIN EQUALIZER AND DECISION FEEDBACK	US	ABANDONED	10/834,193	4/29/04	US 2004-0202259			8/2/22
6936-14-CON-2	Systems and Methods for Multicarrier Modulation Using Multi-Tap Frequency-Domain Equalizer and Decision Feedback	US	ISSUED	11/964,409	12/26/07	US 2008-0101452 A1	7,656,976	2/2/10	8/2/22
6936-14-CON-3	SYSTEMS AND METHODS FOR MULTICARRIER MODULATION USING MULTI-TAP FREQUENCY-DOMAIN EQUALIZER AND DECISION FEEDBACK	US	ABANDONED	12/640,838	12/17/09	US 2010-0098149 A1			9/23/11
6936-14-CON-4	SYSTEMS AND METHODS FOR MULTICARRIER MODULATION USING MULTI-TAP FREQUENCY-DOMAIN EQUALIZER AND DECISION FEEDBACK	US	ABANDONED	12/783,796	5/20/10	US 2010-0296570 A1			3/2/11
6936-14-CON-5	SYSTEMS AND METHODS FOR MULTICARRIER MODULATION USING MULTI-TAP FREQUENCY-DOMAIN EQUALIZER AND DECISION FEEDBACK	US	ABANDONED	12/783,801	5/20/10	N/A			2/18/11
6936-14-PCT	SYSTEMS AND METHOD FOR MULTICARRIER MODULATION USING MULTI-TAP FREQUENCY-DOMAIN EQUALIZER AND DECISION FEEDBACK	WO	NAT PHASE	PCT/US02/24326	8/2/02	WO 2003/012990			
6936-14-PROV	MULTICARRIER MODULATION METHOD USING MULTI-TAP FREQUENCY-DOMAIN EQUILIZATION AND DECISION FEED BACK	US	EXPIRED	60/309,631	8/2/01	N/A			8/2/02
6936-19	MULTI-CARRIER TRANSCEIVER	US	EXPIRED	08/105,796	8/12/93	N/A	5,497,398	3/5/96	8/12/13
6936-19-PCT	MULTI-CARRIER TRANSCEIVER	WO	NAT PHASE	PCT/US94/06713	6/13/94	WO 1995/005711			
6936-21	SYSTEMS AND METHODS FOR IMPLEMENTING RECEIVER TRANSPARENT Q-MODE	US	ISSUED	10/106,329	3/27/02	US 2002/0196861	6,731,695	5/4/04	3/27/21
6936-21-CON	SYSTEMS AND METHODS FOR IMPLEMENTING RECEIVER TRANSPARENT Q-MODE	US	ABANDONED	10/802,867	3/18/04	US 2004-0184552 A1			11/10/05
6936-21-CON-2	SYSTEMS AND METHODS FOR IMPLEMENTING RECEIVER TRANSPARENT Q-MODE	US	ABANDONED	11/200,002	8/10/05	US 2006-0039490 A1			8/7/06
6936-21-CON-3	SYSTEMS AND METHODS FOR IMPLEMENTING RECEIVER TRANSPARENT Q-MODE	US	ABANDONED	11/434,249	5/16/06	US 2006-0203927 A1			3/27/22
6936-21-CON-4	SYSTEMS AND METHODS FOR IMPLEMENTING RECEIVER TRANSPARENT Q-MODE	US	ISSUED	11/674,871	2/14/07	US 2007-0147540 A1	7,558,329	7/7/09	3/27/22
6936-21-CON-5	Systems and Methods for Implementing Receiver Transparent Q-Mode	US	ABANDONED	12/478,577	6/4/09	US 2009-0290620 A1			7/25/11
6936-21-CON-6	Systems and Methods for Implementing Receiver Transparent Q-Mode	US	ISSUED	12/783,749	5/20/10	US 2010-0290558 A1	8,335,271	12/18/12	3/27/22
6936-21-CON-7	Systems and Methods for Implementing Receiver Transparent Q-Mode	US	ABANDONED	12/783,755	5/20/10	US 2010-0296604 A1			3/27/22
6936-21-CON-8	Systems and Methods for Implementing Receiver Transparent Q-Mode	US	ISSUED	13/693,394	12/4/12	US 2013-0094609 A1	8,792,574	7/29/14	3/27/22
6936-21-CON-9	RANDOMIZATION USING AN XOR SCRAMBLER IN MULTICARRIER COMMUNICATIONS	US	ISSUED	14/308,934	6/19/14	US 2014-0294116 A1	9,191,039	11/17/15	3/27/22
6936-21-CON-10	SYSTEMS AND METHODS FOR IMPLEMENTING RECEIVER TRANSPARENT Q-MODE	US	ABANDONED	14/932,599	11/4/15	US 2016-0056857 A1			11/14/17
6936-21-CON-11	SYSTEMS AND METHODS FOR IMPLEMENTING RECEIVER TRANSPARENT Q-MODE	US	ISSUED	15/812,705	11/14/17	US 2018-0069590 A1	10,419,059	9/17/19	3/27/22
6936-21-PAU	RECEIVER TRANSPARENT Q-MODE	AU	ABANDONED	2002248711	3/27/02	AU 2002248711			1/4/05
6936-21-PCA	RECEIVER TRANSPARENT Q-MODE	CA	ABANDONED	2,439,804	3/27/02	CA 2439804			
6936-21-PCT	RECEIVER TRANSPARENT Q-MODE	WO	NAT PHASE	PCT/US02/09411	3/27/02	WO02/078244			
6936-21-PEP	RECEIVER TRANSPARENT Q-MODE	EP	ABANDONED	02717728.6	3/27/02	EP 1374469			11/2/04
6936-21-PJP	RECEIVER TRANSPARENT Q-MODE	JP	ABANDONED	2002-576356	3/27/02	JP 2004-538676			3/10/05
6936-21-PKR	RECEIVER TRANSPARENT Q-MODE	KR	ABANDONED	2003-7012442	3/27/02	10-2004-0004562			
6936-21-PROV-1	RECEIVER TRANSPARENT Q-MODE	US	EXPIRED	60/278,936	3/27/01	N/A			3/27/02
6936-21-PROV-2	RECEIVER TRANSPARENT Q-MODE WITH ON-LINE RECONFIGURATION	US	EXPIRED	60/283,467	4/12/01	N/A			4/12/02
6936-21-PROV-3	RECEIVER TRANSPARENT Q-MODE WITH ON-LINE RECONFIGURATION AND SCRAMBLING	US	EXPIRED	60/287,968	5/1/01	N/A			5/1/02
6936-21-PROV-4	RECEIVER TRANSPARENT Q-MODE WITH ON-LINE RECONFIGURATION, SCRAMBLING AND Q-MODE SYMBOL DISTORTION	US	EXPIRED	60/293,034	5/23/01	N/A			5/23/02
6936-22	MULTI-CARRIER TRANSMISSION SYSTEM ADAPTED FOR PACKET DATA TRANSFER	US	EXPIRED	08/670,245	6/19/96	N/A	5,751,716	5/12/98	6/19/16
6936-22-PCT	MULTI-CARRIER TRANSMISSION SYSTEM ADAPTED FOR PACKET DATA TRANSFER	WO	NAT PHASE	PCT/US97/08756	5/17/97	WO 1997/049208			
6936-22-PEP	MULTI-CARRIER TRANSMISSION SYSTEM ADAPTED FOR PACKET DATA TRANSFER	EP	ABANDONED	97925713.6	5/17/97	N/A			9/5/00

6936-23	SYSTEMS AND METHODS THAT PROVIDE FREQUENCY DOMAIN SUPPLEMENTAL TRAINING OF THE TIME DOMAIN EQUALIZER FOR DMT	US	ISSUED	09/982,065	10/19/01	US 2002-0057734	7,180,938	2/20/07	10/14/23
6936-23-CON	Systems and Methods That Provide Frequency Domain Supplemental Training of the Time Domain Equalizer for DMT	US	ABANDONED	11/616,630	12/27/06	US 2007-0104262			10/19/21
6936-23-CON-2	Systems and Methods That Provide Frequency Domain Supplemental Training of the Time Domain Equalizer for DMT	US	ABANDONED	12/013,874	1/14/08	US 2008-0107164 A1	7,636,389	12/22/09	3/14/17
6936-23-CON-3	Systems and Methods That Provide Frequency Domain Supplemental Training of the Time Domain Equalizer for DMT	US	ABANDONED	12/615,077	11/9/09	US 2010-0054321 A1			2/28/11
6936-23-CON-4	Systems and Methods That Provide Frequency Domain Supplemental Training of the Time Domain Equalizer for DMT	US	ISSUED	12/783,783	5/20/10	US 2010-0290514 A1	8,102,909	1/24/12	10/19/21
6936-23-CON-5	Systems and Methods That Provide Frequency Domain Supplemental Training of the Time Domain Equalizer for DMT	US	ABANDONED	12/783,788	5/20/10	N/A			2/17/11
6936-23-CON-6	Systems and Methods That Provide Frequency Domain Supplemental Training of the Time Domain Equalizer for DMT	US	ABANDONED	13/330,943	12/20/11	US 2012-0087399 A1			9/19/13
6936-23-PCT	SYSTEMS AND METHODS THAT PROVIDE FREQUENCY DOMAIN SUPPLEMENTAL TRAINING OF THE TIME DOMAIN EQUALIZER FOR DMT	WO	NAT PHASE	PCT/US01/32503	10/19/01	WO 2002/033926			
6936-23-PROV	FREQUENCY DOMAIN SUPPLEMENTAL TRAINING OF THE TIME DOMAIN EQUALIZER FOR DMT	US	EXPIRED	60/241,664	10/19/00	N/A			10/19/01
6936-24	MULTICARRIER TRANSMISSION SYSTEM	US	EXPIRED	08/340,747	11/16/94	N/A	5,636,246	6/3/97	11/16/14
6936-24-PAU	MULTICARRIER TRANSMISSION SYSTEM	AU	EXPIRED	41666/96	11/17/95	AU 4166696	708318	11/11/99	11/17/15
6936-24-PCT	MULTICARRIER TRANSMISSION SYSTEM	WO	NAT PHASE	PCT/US95/15115	11/17/95	WO 1997/026711			
6936-24-PGB	MULTICARRIER TRANSMISSION SYSTEM	GB	EXPIRED	9709849.5	11/17/95	GB 2320401	2320401	4/12/00	11/17/15
6936-25	BIT ALLOCATION AMONG CARRIERS IN MULTICARRIER COMMUNICATIONS	US	EXPIRED	09/600,971	7/20/00	N/A	6,870,888	3/22/05	11/23/19
6936-25-PAU	ALLOCATION OF COMMUNICATION BITS AMONG CARRIERS IN MULTICARRIER COMMUNICATIONS	AU	ABANDONED	18292/00	11/23/99	AU 1829200	754597	3/6/03	11/22/16
6936-25-PAU-2	ALLOCATION OF COMMUNICATION BITS AMONG CARRIERS IN MULTICARRIER COMMUNICATIONS	AU	ABANDONED	2002302029	11/18/02	AU 2002302029			11/19/03
6936-25-PCA	ALLOCATION OF COMMUNICATION BITS AMONG CARRIERS IN MULTICARRIER COMMUNICATIONS	CA	ABANDONED	2,350,916	11/23/99	CA 2350916	2,350,916	11/20/07	9/25/17
6936-25-PCA-DIV	Bit Allocation Among Carriers in Multicarrier Communications	CA	EXPIRED	2,599,805	11/23/99	CA 2599805	2,599,805	9/29/09	11/23/19
6936-25-PCT	ALLOCATION OF COMMUNICATION BITS AMONG CARRIERS IN MULTICARRIER COMMUNICATIONS	WO	NAT PHASE	PCT/US99/27798	11/23/99	WO 2000/031940			
6936-25-PEP	ALLOCATION OF COMMUNICATION BITS AMONG CARRIERS IN MULTICARRIER COMMUNICATIONS	EP	EXPIRED	99961782.2	11/23/99	1133858	1133858	6/30/04	11/23/19
6936-25-PEPGB	ALLOCATION OF COMMUNICATION BITS AMONG CARRIERS IN MULTICARRIER COMMUNICATIONS	GB	EXPIRED	99961782.2	11/23/99	N/A	1133858	6/30/04	11/23/19
6936-25-PEP-2	ALLOCATION OF COMMUNICATION BITS AMONG CARRIERS IN MULTICARRIER COMMUNICATIONS	EP	ABANDONED	04012682.3	11/23/99	1453267			11/23/19
6936-25-PEP-2-DIV-1	ALLOCATION OF COMMUNICATION BITS AMONG CARRIERS IN MULTICARRIER COMMUNICATIONS	EP	ABANDONED	10011993.2	11/23/99	2264932			11/23/19
6936-25-PJP	ALLOCATION OF COMMUNICATION BITS AMONG CARRIERS IN MULTICARRIER COMMUNICATIONS	JP	ABANDONED	2000-584658	11/23/99	2002-531010			11/23/19
6936-25-PJP-DIV	ALLOCATION OF COMMUNICATION BITS AMONG CARRIERS IN MULTICARRIER COMMUNICATIONS	JP	ABANDONED	2010-56580	11/23/99	2010-141931			11/23/19
6936-25-PKR	ALLOCATION OF COMMUNICATION BITS AMONG CARRIERS IN MULTICARRIER COMMUNICATIONS	KR	ABANDONED	2001-7006580	11/23/99	10-2001-0101081			11/23/19
6936-25-PROV	ALLOCATION OF COMMUNICATION BITS AMONG CARRIERS IN MULTICARRIER COMMUNICATIONS	US	EXPIRED	60/109,876	11/25/98	N/A			11/25/99
6936-30	MULTI-TAP FREQUENCY DOMAIN EQUALIZATION WITH DECISION FEEDBACK AND TRELLIS DECODING	US	ABANDONED	10/631,745	8/1/03	US 2004-0096008 A1			8/1/23
6936-30-DIV	MULTI-TAP FREQUENCY DOMAIN EQUALIZATION WITH DECISION FEEDBACK AND TRELLIS DECODING	US	ABANDONED	11/748,806	5/15/07	US 2007-0211812			6/20/11
6936-30-DIV-CON	MULTI-TAP FREQUENCY DOMAIN EQUALIZATION WITH DECISION FEEDBACK AND TRELLIS DECODING	US	ABANDONED	12/783,733	5/20/10	US 2010-0293442 A1			2/25/13
6936-30-DIV-CON-2	MULTI-TAP FREQUENCY DOMAIN EQUALIZATION WITH DECISION FEEDBACK AND TRELLIS DECODING	US	ABANDONED	12/783,737	5/20/10	US 2010-0299582 A1			2/25/13

6936-30-PCT	COMBINED MULTI-TAP FREQUENCY DOMAIN EQUALIZATION WITH DECISION FEEDBACK AND TRELLIS DECODING	WO	NAT PHASE	PCT/US03/23965	8/1/03	WO 2004/014032 A3			
6936-30-PROV	COMBINED MULTI-TAP FREQUENCY DOMAIN EQUALIZATION WITH DECISION FEEDBACK AND TRELLIS DECODING	US	EXPIRED	60/400,550	8/1/02	N/A			8/1/03
6936-36	A SYSTEM AND METHOD FOR TRANSMITTING MESSAGES BETWEEN TRANSCEIVERS USING ELECTROMAGNETICALLY COUPLED SIGNALS	US	ISSUED	09/616,954	7/14/00	N/A	6,748,016	6/8/04	7/5/22
6936-36-CON	SYSTEM AND METHOD FOR TRANSMITTING MESSAGES BETWEEN TRANSCEIVERS USING ELECTROMAGNETICALLY COUPLED SIGNALS	US	ABANDONED	10/743,946	12/24/03	US 2004-0136463 A1			8/27/04
6936-36-PAU	A SYSTEM AND METHOD FOR TRANSMITTING MESSAGES BETWEEN TRANSCEIVERS USING ELECTROMAGNETICALLY COUPLED SIGNALS	AU	ABANDONED	59347/00	7/14/00				1/13/05
6936-36-PCA	A SYSTEM AND METHOD FOR TRANSMITTING MESSAGES BETWEEN TRANSCEIVERS USING ELECTROMAGNETICALLY COUPLED SIGNALS	CA	ABANDONED	2378046	7/14/00				1/13/05
6936-36-PCT	A SYSTEM AND METHOD FOR TRANSMITTING MESSAGES BETWEEN TRANSCEIVERS USING ELECTROMAGNETICALLY COUPLED SIGNALS	WO	NAT PHASE	PCT/US00/19247	7/14/00				
6936-36-PEP	A SYSTEM AND METHOD FOR TRANSMITTING MESSAGES BETWEEN TRANSCEIVERS USING ELECTROMAGNETICALLY COUPLED SIGNALS	EP	ABANDONED	00945396.0	7/14/00				1/13/05
6936-36-PJP	A SYSTEM AND METHOD FOR TRANSMITTING MESSAGES BETWEEN TRANSCEIVERS USING ELECTROMAGNETICALLY COUPLED SIGNALS	JP	ABANDONED	2001-511007	7/14/00				1/13/05
6936-36-PKR	A SYSTEM AND METHOD FOR TRANSMITTING MESSAGES BETWEEN TRANSCEIVERS USING ELECTROMAGNETICALLY COUPLED SIGNALS	KR	ABANDONED	7000562/2002	7/14/00				1/13/05
6936-36-PROV	A SYSTEM AND METHOD FOR TRANSMITTING MESSAGES BETWEEN TRANSCEIVERS USING ELECTROMAGNETICALLY COUPLED SIGNALS	US	EXPIRED	60/144,562	7/16/99	N/A			7/16/00
6936-41	MULTI-CARRIER TRANSMISSION SYSTEM UTILIZING CHANNELS WITH DIFFERENT ERROR RATES	US	EXPIRED	08/661,974	6/12/96	N/A	5,832,030	11/3/98	6/12/16
6936-41-PCT	MULTI-CARRIER TRANSMISSION SYSTEM UTILIZING CHANNELS WITH DIFFERENT ERROR RATES	WO	NAT PHASE	PCT/US97/08222	5/17/97	WO 1997/48204			
6936-45	SINGLE SIDE-BAND MODULATION SYSTEM FOR USE IN DIGITALLY IMPLEMENTED MULTICARRIER TRANSMISSION SYSTEMS	US	EXPIRED	08/591,831	1/25/96	N/A	5,631,610	5/20/97	1/25/16
6936-45-PAU	SINGLE SIDE-BAND MODULATION SYSTEM FOR USE IN DIGITALLY IMPLEMENTED MULTICARRIER TRANSMISSION SYSTEMS	AU	EXPIRED	31342/97	5/17/97	AU 3134297	738201	1/3/02	5/17/17
6936-45-PCA	SINGLE SIDE-BAND MODULATION SYSTEM FOR USE IN DIGITALLY IMPLEMENTED MULTICARRIER TRANSMISSION SYSTEMS	CA	ABANDONED	2289537	5/17/97				7/12/04
6936-45-PCT	SINGLE SIDE-BAND MODULATION SYSTEM FOR USE IN DIGITALLY IMPLEMENTED MULTICARRIER TRANSMISSION SYSTEMS	WO	NAT PHASE	PCT/US97/08549	5/17/97	WO 1998/053552			
6936-45-PEP	SINGLE SIDE-BAND MODULATION SYSTEM FOR USE IN DIGITALLY IMPLEMENTED MULTICARRIER TRANSMISSION SYSTEMS	EP	ABANDONED	97926623.6	5/17/97				3/27/03
6936-45-PJP	SINGLE SIDE-BAND MODULATION SYSTEM FOR USE IN DIGITALLY IMPLEMENTED MULTICARRIER TRANSMISSION SYSTEMS	JP	ABANDONED	10-550313	5/17/97				5/6/04
6936-46	METHOD FOR PARTIALLY MODULATING AND DEMODULATING DATA IN A MULTICARRIER TRANSMISSION SYSTEM	US	EXPIRED	08/668,575	6/20/96	N/A	5,715,280	2/3/98	6/20/16
6936-46-PAU	METHOD FOR PARTIALLY MODULATING AND DEMODULATING DATA IN A MULTICARRIER TRANSMISSION SYSTEM	AU	EXPIRED	30673/97	5/17/97	AU 3067397	743020	5/2/02	5/17/17
6936-46-PCA	METHOD FOR PARTIALLY MODULATING AND DEMODULATING DATA IN A MULTICARRIER TRANSMISSION SYSTEM	CA	ABANDONED	2289529	5/17/97				6/17/03

6936-46-PCT	METHOD FOR PARTIALLY MODULATING AND DEMODULATING DATA IN A MULTICARRIER TRANSMISSION SYSTEM	WO	NAT PHASE	PCT/US97/08209	5/17/97	WO 1998/053572			
6936-46-PEP	METHOD FOR PARTIALLY MODULATING AND DEMODULATING DATA IN A MULTICARRIER TRANSMISSION SYSTEM	EP	ABANDONED	97925573.4	5/17/97				4/16/03
6936-46-PJP	METHOD FOR PARTIALLY MODULATING AND DEMODULATING DATA IN A MULTICARRIER TRANSMISSION SYSTEM	JP	ABANDONED	10-550306	5/17/97				5/13/04
6936-48	INTELLIGENT RATE OPTION DETERMINATION METHOD APPLIED TO ADSL TRANSCEIVER	US	ISSUED	09/738,785	12/15/00	US 2001-0030998 A1	6,801,570	10/5/04	12/15/20
6936-48-PROV	INTELLIGENT RATE OPTION DETERMINATION METHOD APPLIED TO ADSL TRANSCEIVER	US	EXPIRED	60/172,343	12/16/99	N/A			12/16/00
6936-50	SYSTEMS AND METHODS FOR LDPC CODED MODULATION	US	ABANDONED	09/882,046	6/18/01	US 2002-0042899			5/31/05
6936-50-DIV	SYSTEMS AND METHODS FOR LDPC CODED MODULATION	US	ABANDONED	11/140,246	5/31/05	US 2005-0229088 A1			6/18/21
6936-50-DIV-2	SYSTEMS AND METHODS FOR LDPC CODED MODULATION	US	ABANDONED	12/383,056	3/19/09	US 2009-0183048 A1			4/20/16
6936-50-DIV-2-CON	SYSTEMS AND METHODS FOR LDPC CODED MODULATION	US	ABANDONED	12/783,825	5/20/10	US 2010-0299573 A1			5/30/11
6936-50-DIV-2-CON-2	Systems and Methods for LDPC Coded Modulation	US	ABANDONED	12/783,839	5/20/10	US 2010-0299574 A1			6/1/11
6936-50-DIV-3	SYSTEMS AND METHODS FOR LDPC CODED MODULATION	US	ABANDONED	15/077,506	3/22/16	US 2016-0204901 A1			1/13/17
6936-50-PAU	SYSTEMS AND METHODS FOR LDPC CODED MODULATION	AU	ABANDONED	2001267096	6/18/01	AU 2001267096			3/28/06
6936-50-PCA	SYSTEMS AND METHODS FOR LDPC CODED MODULATION	CA	ABANDONED	2,409,179	6/18/01	CA 2409179			2/24/11
6936-50-PCT	SYSTEMS AND METHODS FOR LDPC CODED MODULATION	WO	NAT PHASE	PCT/US01/41015	6/18/01	WO 2001/097387			
6936-50-PEP	SYSTEMS AND METHODS FOR LDPC CODED MODULATION	EP	ABANDONED	01944712.7	6/18/01	EP 1290802			
6936-50-PJP	SYSTEMS AND METHODS FOR LDPC CODED MODULATION	JP	ABANDONED	2002-511477	6/18/01	2004-503979			10/27/11
6936-50-PKR	SYSTEMS AND METHODS FOR LDPC CODED MODULATION	KR	ABANDONED	2002-7017148	6/18/01	10-2003-0036227			6/18/21
6936-50-PKR-DIV	SYSTEMS AND METHODS FOR LDPC CODED MODULATION	KR	ABANDONED	10-2010-7006498	6/18/01	10-2010-00469063			6/18/21
6936-50-PROV	LDPC CODED MODULATION	US	EXPIRED	60/212,233	6/16/00	N/A			6/16/01
6936-50-PROV-2	LOW DENSITY PARITY CHECK (LDPC) CODED MODULATION FOR ADSL	US	EXPIRED	60/241,468	10/18/00	N/A			10/18/01
6936-60-PCA	Stable Low Power Mode for Multicarrier Transceivers	CA	ABANDONED	2,706,362	11/21/08	CA 2706362			12/21/16
6936-60-PCN	Stable Low Power Mode for Multicarrier Transceivers	CN	ABANDONED	200880117277.5	11/21/08	CN101868951A	ZL200880117277.5	9/7/16	9/20/17
6936-60-PCN-DIV	Stable Low Power Mode for Multicarrier Transceivers	CN	ABANDONED	201310088357.5	11/21/08	CN103227767	ZL201310088357.5	4/12/17	9/20/17
6936-60-PCN-HK	Stable Low Power Mode for Multicarrier Transceivers	HK	ABANDONED	10110838.3	11/21/08	HK1144345			12/12/16
6936-60-PCT	Stable Low Power Mode for Multicarrier Transceivers	WO	NAT PHASE	PCT/US08/84322	11/21/08	WO 2009/067653			
6936-60-PEP	Stable Low Power Mode for Multicarrier Transceivers	EP	ABANDONED	08852660.3	11/21/08	EP 2223489	2223489	4/20/16	7/6/17
6936-60-PEP-DE	Stable Low Power Mode for Multicarrier Transceivers	DE	ABANDONED	08852660.3	11/21/08		2223489	4/20/16	7/6/17
6936-60-PEP-FR	Stable Low Power Mode for Multicarrier Transceivers	FR	ABANDONED	08852660.3	11/21/08		2223489	4/20/16	7/6/17
6936-60-PEP-GB	Stable Low Power Mode for Multicarrier Transceivers	GB	ABANDONED	08852660.3	11/21/08		2223489	4/20/16	7/6/17
6936-60-PEPHK	Stable Low Power Mode for Multicarrier Transceivers	HK	ABANDONED	10109672.4	11/21/08	HK 1143261			2/11/16
6936-60-PIN	Stable Low Power Mode for Multicarrier Transceivers	IN	ABANDONED	1800/KOLNP/2010	11/21/08				11/21/28
6936-60-PJP	Stable Low Power Mode for Multicarrier Transceivers	JP	ABANDONED	2010-535086	11/21/08	2011-504709			11/21/28
6936-60-PROV	Stable Low Power Mode for Multicarrier Transceivers	US	EXPIRED	60/989,542	11/21/07	N/A			11/21/08
6936-60-PUS	Stable Low Power Mode for Multicarrier Transceivers	US	ISSUED	12/739,330	8/12/10	US 2010-0296555 A1	8,837,610	9/16/14	6/24/29
6936-60-PUS-CON	Stable Low Power Mode for Multicarrier Transceivers	US	ABANDONED	14/485,937	9/15/14	US 2015-0003504 A1			5/10/16
6936-60-PUS-CON-2	STABLE LOW POWER MODE FOR MULTICARRIER TRANSCEIVERS	US	ABANDONED	15/084,788	3/30/16	US 2016-0212275 A1			6/7/17
6936-61-PROV	Stable Low Power Mode for Multicarrier Transceivers (Second Edition)	US	EXPIRED	61/011,267	1/16/08	N/A			1/16/09
6936-84-PCT	Reed-Solomon Erasure Decoding with Error Detection for Retransmission	WO	NAT PHASE	PCT/US10/37195	6/3/10	WO 2010/141677			
6936-84-PROV	Reed-Solomon Erasure Decoding with Error Detection for Retransmission	US	EXPIRED	61/183,845	6/3/09	N/A			6/3/10
6936-84-PUS	Reed-Solomon Erasure Decoding with Error Detection for Retransmission	US	ISSUED	13/322,170	2/8/12	US 2012-0144259 A1	8,782,498	7/15/14	11/15/30
6936-84-PUS-CON	Reed-Solomon Erasure Decoding with Error Detection for Retransmission	US	ISSUED	14/328,237	7/10/14	US 2014-0325306 A1	9,276,612	3/1/16	6/3/30
6936-84-PUS-CON-2	REED-SOLOMON ERASURE DECODING WITH ERROR DETECTION FOR RETRANSMISSION	US	ABANDONED	15/054,499	2/26/16	US 2016-0182089 A1			5/9/18
6936-85-PCA	Low Power Mode with Legacy Compatibility	CA	PENDING	2,944,006	4/28/15				4/28/35
6936-85-PCT	Low Power Mode with Legacy Compatibility	WO	NAT PHASE	PCT/US15/27983	4/28/15	WO 2015/168117			

6936-85-PEP	Low Power Mode with Legacy Compatibility	EP	ISSUED	15721495.8	4/28/15	3138206	3138206	6/10/20	4/28/35
6936-85-PEPDE	Low Power Mode with Legacy Compatibility	DE	ISSUED	15721495.8	4/28/15		3138206	6/10/20	4/28/35
6936-85-PEPFR	Low Power Mode with Legacy Compatibility	FR	ISSUED	15721495.8	4/28/15		3138206	6/10/20	4/28/35
6936-85-PEPGB	Low Power Mode with Legacy Compatibility	GB	ISSUED	15721495.8	4/28/15		3138206	6/10/20	4/28/35
6936-85-PEPNL	Low Power Mode with Legacy Compatibility	NL	ISSUED	15721495.8	4/28/15		3138206	6/10/20	4/28/35
6936-85-PEP-DIV	Low Power Mode with Legacy Compatibility	EP	ABANDONED	20178740.5	4/28/15				9/30/20
6936-85-PJP	Low Power Mode with Legacy Compatibility	JP	ISSUED	2016-563176	4/28/15	2017-516391	6592006	9/27/19	4/28/35
6936-85-PKR	Low Power Mode with Legacy Compatibility	KR	PENDING	10-2016-7029583	4/28/15				4/28/35
6936-85-PROV	Low Power Mode with Legacy Compatibility	US	EXPIRED	61/985,168	4/28/14				4/28/15
6936-85-PUS	LOW POWER MODE WITH LEGACY COMPATIBILITY	US	PUBLISHED	15/304,920	10/18/16	US 2017-0187512 A1			4/28/35

Schedule III

Copyrights

None

AO 120 (Rev. 08/10)

TO:	REPORT ON THE FILING OR DETERMINATION OF AN ACTION REGARDING A PATENT OR TRADEMARK
Mail Stop 8 Director of the U.S. Patent and Trademark Office P.O. Box 1450 Alexandria, VA 22313-1450	

In Compliance with 35 U.S.C. § 290 and/or 15 U.S.C. § 1116 you are hereby advised that a court action has been filed in the U.S. District Court Transferred to Delaware from Alabama on the following

☐ Trademarks or ☑ Patents. (☐ the patent action involves 35 U.S.C. § 292.):

DOCKET NO.	DATE FILED	U.S. DISTRICT COURT
15-cv-121-RGA	7/17/2014	Transferred to Delaware from Alabama

PLAINTIFF	DEFENDANT
ADTRAN, Inc.	TQ Delta, LLC

	PATENT OR TRADEMARK NO.	DATE OF PATENT OR TRADEMARK	HOLDER OF PATENT OR TRADEMARK
1	See Attachment #1		
2			
3			
4			
5			

In the above—entitled case, the following patent(s)/ trademark(s) have been included:

DATE INCLUDED	INCLUDED BY ☐ Amendment ☑ Answer ☐ Cross Bill ☐ Other Pleading	
3/13/2015		
PATENT OR TRADEMARK NO.	DATE OF PATENT OR TRADEMARK	HOLDER OF PATENT OR TRADEMARK
1 See Attachment #2		
2		
3		
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In the above—entitled case, the following decision has been rendered or judgement issued:

DECISION/JUDGEMENT

CLERK	(BY) DEPUTY CLERK	DATE

Copy 1—Upon initiation of action, mail this copy to Director Copy 3—Upon termination of action, mail this copy to Director
Copy 2—Upon filing document adding patent(s), mail this copy to Director Copy 4—Case file copy

Attachment #1

Patent or Trademark No.	Date of Patent or Trademark	Holder of Patent or Trademark
1.U.S. 7,453,881 B2	11/18/2008	TQ Delta, LLC
2.U.S. 7,809,028 B2	10/05/2010	TQ Delta, LLC
3.U.S. 7,978,706 B2	7/12/2011	TQ Delta, LLC
4.U.S. 8,422,511 B2	4/16/2013	TQ Delta, LLC
5.U.S. 6,445,730 B1	9/03/2002	TQ Delta, LLC
6.U.S. 7,292,627 B2	11/6/2007	TQ Delta, LLC
7.U.S. 7,451,379 B2	11/11/2008	TQ Delta, LLC
8.U.S. 7,471,721 B2	12/30/2008	TQ Delta, LLC
9.U.S. 7,570,686 B2	8/4/2009	TQ Delta, LLC
10. U.S. 7,831,890 B2	11/09/2010	TQ Delta, LLC
11. U.S. 7,835,430 B2	11/16/2010	TQ Delta, LLC
12. U.S. 7,836,381 B1	11/16/2010	TQ Delta, LLC
13. U.S. 7,844,882 B2	11/30/2010	TQ Delta, LLC
14. U.S. 7,889,784 B2	2/15/2011	TQ Delta, LLC
15. U.S. 7,925,958 B2	04/12/2011	TQ Delta, LLC
16. U.S. 7,978,753 B2	07/12/2011	TQ Delta, LLC
17. U.S. 7,979,778 B2	07/12/2011	TQ Delta, LLC
18. U.S. 8,073,041 B1	12/6/2011	TQ Delta, LLC
19. U.S. 8,090,008 B2	1/3/2012	TQ Delta, LLC
20. U.S. 8,218,610 B2	7/10/2012	TQ Delta, LLC
21. U.S. 8,238,412 B2	08/07/2012	TQ Delta, LLC
22. U.S. 8,276,048 B2	09/25/2012	TQ Delta, LLC
23. U.S. 8,355,427 B2	1/15/2013	TQ Delta, LLC

24. U.S. 8,432,956 B2	4/30/2013	TQ Delta, LLC
25. U.S. 8,437,382 B2	5/7/2013	TQ Delta, LLC
26. U.S. 8,462,835 B2	6/11/2013	TQ Delta, LLC
27. U.S. 8,495,473 B2	7/23/2013	TQ Delta, LLC
28. U.S. 8,516,337 B2	08/20/2013	TQ Delta, LLC

Attachment #2

	PATENT OR TRADEMARK NO.	DATE OF PATENT OR TRADEMARK	HOLDER OF PATENT OR TRADEMARK
1	US 7,796,705 B2	9/14/2010	TQ Delta, LLC
2	US 8,335,956 B2	12/18/2012	TQ Delta, LLC
3	US 8,407,546 B2	3/26/2013	TQ Delta, LLC
4	US 8,468,411 B2	6/18/2013	TQ Delta, LLC
5	US 8,645,784 B2	2/4/2014	TQ Delta, LLC
6	US 8,595,577 B2	11/26/2013	TQ Delta, LLC

AO 120 (Rev. 08/10)

TO:	REPORT ON THE FILING OR DETERMINATION OF AN ACTION REGARDING A PATENT OR TRADEMARK
Mail Stop 8 Director of the U.S. Patent and Trademark Office P.O. Box 1450 Alexandria, VA 22313-1450	

In Compliance with 35 U.S.C. § 290 and/or 15 U.S.C. § 1116 you are hereby advised that a court action has been filed in the U.S. District Court District of Delaware on the following

☐ Trademarks or ☑ Patents. (☐ the patent action involves 35 U.S.C. § 292.):

DOCKET NO.	DATE FILED	U.S. DISTRICT COURT
	7/18/2014	District of Delaware

PLAINTIFF	DEFENDANT
TQ Delta, LLC	ADTRAN, Inc.

PATENT OR TRADEMARK NO.	DATE OF PATENT OR TRADEMARK	HOLDER OF PATENT OR TRADEMARK
1 See Attached		
2 32 Pats		
3		
4		
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In the above—entitled case, the following patent(s)/ trademark(s) have been included:

DATE INCLUDED	INCLUDED BY ☐ Amendment ☐ Answer ☐ Cross Bill ☐ Other Pleading	
PATENT OR TRADEMARK NO.	DATE OF PATENT OR TRADEMARK	HOLDER OF PATENT OR TRADEMARK
1		
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In the above—entitled case, the following decision has been rendered or judgement issued:

DECISION/JUDGEMENT

CLERK	(BY) DEPUTY CLERK	DATE

Copy 1—Upon initiation of action, mail this copy to Director **Copy 3—Upon termination of action, mail this copy to Director**
Copy 2—Upon filing document adding patent(s), mail this copy to Director **Copy 4—Case file copy**

	PATENT OR TRADEMARK NO.	DATE OF PATENT OR TRADEMARK	HOLDER OF PATENT OR TRADEMARK
1	US 8,090,008 B2	1/3/2012	TQ Delta, LLC
2	US 8,073,041 B1	12/6/2011	TQ Delta, LLC
3	US 7,292,627 B2	11/6/2007	TQ Delta, LLC
4	US 7,471,721 B2	12/30/2008	TQ Delta, LLC
5	US 8,218,610 B2	7/10/2012	TQ Delta, LLC
6	US 8,355,427 B2	1/15/2013	TQ Delta, LLC
7	US 7,453,881 B2	11/18/2008	TQ Delta, LLC
8	US 7,809,028 B2	10/5/2010	TQ Delta, LLC
9	US 7,978,706 B2	7/12/2011	TQ Delta, LLC
10	US 8,422,511 B2	4/16/2013	TQ Delta, LLC
11	US 7,889,784 B2	2/15/2011	TQ Delta, LLC
12	US 7,835,430 B2	11/16/2010	TQ Delta, LLC
13	US 7,570,686 B2	8/4/2009	TQ Delta, LLC
14	US 8,238,412 B2	8/7/2012	TQ Delta, LLC
15	US 8,432,956 B2	4/30/2013	TQ Delta, LLC
16	US 7,451,379 B2	11/11/2008	TQ Delta, LLC
17	US 8,516,337 B2	8/20/2013	TQ Delta, LLC
18	US 7,979,778 B2	7/12/2011	TQ Delta, LLC
19	US 7,925,958 B2	4/12/2011	TQ Delta, LLC
20	US 8,462,835 B2	6/11/2013	TQ Delta, LLC
21	US 8,594,162 B2	11/26/2013	TQ Delta, LLC
22	US 7,978,753 B2	7/12/2011	TQ Delta, LLC
23	US 6,445,730 B1	9/3/2002	TQ Delta, LLC
24	US 8,611,404 B2	12/17/2013	TQ Delta, LLC
25	US 8,437,382 B2	5/7/2013	TQ Delta, LLC
26	US 7,836,381 B1	11/16/2010	TQ Delta, LLC
27	US 7,844,882 B2	11/30/2010	TQ Delta, LLC
28	US 8,276,048 B2	9/25/2012	TQ Delta, LLC
29	US 8,495,473 B2	7/23/2013	TQ Delta, LLC
30	US 8,607,126 B1	12/10/2013	TQ Delta, LLC
31	US 7,831,890 B2	11/9/2010	TQ Delta, LLC
32	US 8,625,660 B2	1/7/2014	TQ Delta, LLC

Birch, Melvin (Akima)

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Sent:	Wednesday, November 20, 2013 4:56 PM
To:	ded_ecf@ded.uscourts.gov
Subject:	Activity in Case 1:13-cv-01835-RGA TQ Delta LLC v. Pace Americas Inc. Patent/Trademark Report to Commissioner

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U.S. District Court

District of Delaware

Notice of Electronic Filing

The following transaction was entered by Farnan, Brian on 11/20/2013 at 4:56 PM EST and filed on 11/20/2013

Case Name: TQ Delta LLC v. Pace Americas Inc.
Case Number: 1:13-cv-01835-RGA
Filer:
Document Number: 7

Docket Text:
Report to the Commissioner of Patents and Trademarks for Patent/Trademark Number(s) US 8,090,008 B2; US 8,073,041 B1; US 7,292,627 B2; US 7,471,721 B2; US 8,218,610 B2; US 8,355,427 B2; US 7,453,881 B2; US 7,978,706 B2; US 8,422,511 B2; US 7,889,784 B2; US 7,835,430 B2; US 7,570,686 B2; US 8,238,412 B2; US 8,432,956 B2; US 7,451,379 B2; US 8,516,337 B2; US 7,979,778 B2; US 7,925,958 B2; US 8,462,835 B2; US 7,836,381 B1; US 7,844,882 B2; US 8,276,048 B2; US 8,495,473 B2; US 7,831,890 B2; . (Farnan, Brian)

1:13-cv-01835-RGA Notice has been electronically mailed to:

Brian E. Farnan bfarnan@farnanlaw.com, tfarnan@farnanlaw.com

Michael J. Farnan mfarnan@farnanlaw.com, tfarnan@farnanlaw.com

1:13-cv-01835-RGA Filer will deliver document by other means to:

The following document(s) are associated with this transaction:

From:	ded_nefreply@ded.uscourts.gov
Sent:	Wednesday, November 20, 2013 5:07 PM
To:	ded_ecf@ded.uscourts.gov
Subject:	Activity in Case 1:13-cv-01836-RGA TQ Delta LLC v. Zhone Technologies Inc. Patent/Trademark Report to Commissioner

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U.S. District Court

District of Delaware

Notice of Electronic Filing

The following transaction was entered by Farnan, Brian on 11/20/2013 at 5:07 PM EST and filed on 11/20/2013
Case Name: TQ Delta LLC v. Zhone Technologies Inc.
Case Number: 1:13-cv-01836-RGA
Filer:
Document Number: 7

Docket Text:
Report to the Commissioner of Patents and Trademarks for Patent/Trademark Number(s) US 8,090,008 B2; US 8,073,041 B1; US 7,292,627 B2; US 7,471,721 B2; US 8,218,610 B2; US 8,355,427 B2; US 7,453,881 B2; US 7,809,028 B2; US 7,978,706 B2; US 8,422,511 B2; US 7,796,705 B2; US 7,889,784 B2; US 7,835,430 B2; US 7,570,686 B2; US 8,238,412 B2; US 8,432,956 B2; US 7,451,379 B2; US 8,516,337 B2; US 7,979,778 B2; US 7,925,958 B2; US 8,462,835 B2; US 7,978,753 B2; US 6,445,730 B1; US 8,437,382 B2; US 7,836,381 B1; US 7,844,882 B2; US 8,276,048 B2; US 8,495,473 B2; US 7,831,890 B2; US 8,335,956 B2; US 8,468,411 B2; US 8,407,546 B2 . (Farnan, Brian)

1:13-cv-01836-RGA Notice has been electronically mailed to:

Brian E. Farnan bfarnan@farnanlaw.com, tfarnan@farnanlaw.com

Michael J. Farnan mfarnan@farnanlaw.com, tfarnan@farnanlaw.com

1:13-cv-01836-RGA Filer will deliver document by other means to:

AO 120 (Rev. 08/10)

TO:	REPORT ON THE FILING OR DETERMINATION OF AN ACTION REGARDING A PATENT OR TRADEMARK
Mail Stop 8 Director of the U.S. Patent and Trademark Office P.O. Box 1450 Alexandria, VA 22313-1450	

In Compliance with 35 U.S.C. § 290 and/or 15 U.S.C. § 1116 you are hereby advised that a court action has been filed in the U.S. District Court District of Delaware on the following

☐ Trademarks or ☑ Patents. (☐ the patent action involves 35 U.S.C. § 292.):

DOCKET NO.	DATE FILED	U.S. DISTRICT COURT
	12/9/2013	District of Delaware

PLAINTIFF	DEFENDANT
TQ Delta, LLC	ZyXEL Communications Corporation and ZyXEL Communications, Inc.

PATENT OR TRADEMARK NO.	DATE OF PATENT OR TRADEMARK	HOLDER OF PATENT OR TRADEMARK
1 See Attached		
2		
3		
4		
5		

In the above—entitled case, the following patent(s)/ trademark(s) have been included:

DATE INCLUDED	INCLUDED BY ☐ Amendment ☐ Answer ☐ Cross Bill ☐ Other Pleading	
PATENT OR TRADEMARK NO.	DATE OF PATENT OR TRADEMARK	HOLDER OF PATENT OR TRADEMARK
1		
2		
3		
4		
5		

In the above—entitled case, the following decision has been rendered or judgement issued:

DECISION/JUDGEMENT

CLERK	(BY) DEPUTY CLERK	DATE

Copy 1—Upon initiation of action, mail this copy to Director Copy 3—Upon termination of action, mail this copy to Director
Copy 2—Upon filing document adding patent(s), mail this copy to Director Copy 4—Case file copy

	PATENT OR TRADEMARK NO.	DATE OF PATENT OR TRADEMARK	HOLDER OF PATENT OR TRADEMARK
1	US 8,090,008 B2	1/3/2012	TQ Delta, LLC
2	US 8,073,041 B1	12/6/2011	TQ Delta, LLC
3	US 7,292,627 B2	11/6/2007	TQ Delta, LLC
4	US 7,471,721 B2	12/30/2008	TQ Delta, LLC
5	US 8,218,610 B2	7/10/2012	TQ Delta, LLC
6.	US 8,355,427 B2	1/15/2013	TQ Delta, LLC
7	US 7,453,881 B2	11/18/2008	TQ Delta, LLC
8	US 7,809,028 B2	10/5/2010	TQ Delta, LLC
9	US 7,978,706 B2	7/12/2011	TQ Delta, LLC
10	US 8,422,511 B2	4/16/2013	TQ Delta, LLC
11	US 7,796,705 B2	9/14/2010	TQ Delta, LLC
12	US 7,889,784 B2	2/15/2011	TQ Delta, LLC
13	US 7,835,430 B2	11/16/2010	TQ Delta, LLC
14	US 7,570,686 B2	8/4/2009	TQ Delta, LLC
15	US 8,238,412 B2	8/7/2012	TQ Delta, LLC
16	US 8,432,956 B2	4/30/2013	TQ Delta, LLC
17	US 7,451,379 B2	11/11/2008	TQ Delta, LLC
18	US 8,516,337 B2	8/20/2013	TQ Delta, LLC
19	US 7,979,778 B2	7/12/2011	TQ Delta, LLC
20	US 7,925,958 B2	4/12/2011	TQ Delta, LLC
21	US 8,462,835 B2	6/11/2013	TQ Delta, LLC
22	US 7,978,753 B2	7/12/2011	TQ Delta, LLC
23	US 6,445,730 B1	9/3/2002	TQ Delta, LLC
24	US 8,437,382 B2	5/7/2013	TQ Delta, LLC
25	US 7,836,381 B1	11/16/2010	TQ Delta, LLC
26	US 7,844,882 B2	11/30/2010	TQ Delta, LLC
27	US 8,276,048 B2	9/25/2012	TQ Delta, LLC
28	US 8,495,473 B2	7/23/2013	TQ Delta, LLC
29	US 7,831,890 B2	11/9/2010	TQ Delta, LLC
30	US 8,335,956 B2	12/18/2012	TQ Delta, LLC
31	US 8,468,411 B2	6/18/2013	TQ Delta, LLC
32	US 8,407,546 B2	3/26/2013	TQ Delta, LLC

AO 120 (Rev. 08/10)

TO:	REPORT ON THE FILING OR DETERMINATION OF AN ACTION REGARDING A PATENT OR TRADEMARK
Mail Stop 8 Director of the U.S. Patent and Trademark Office P.O. Box 1450 Alexandria, VA 22313-1450	

In Compliance with 35 U.S.C. § 290 and/or 15 U.S.C. § 1116 you are hereby advised that a court action has been filed in the U.S. District Court Northern District of Texas, Dallas Division on the following

☑ Trademarks or ☐ Patents. (☐ the patent action involves 35 U.S.C. § 292.):

DOCKET NO.	DATE FILED	U.S. DISTRICT COURT
3:12-cv-1462-L	5/10/2012	Northern District of Texas, Dallas Division

PLAINTIFF	DEFENDANT
Boulle Ltd	De Boulle Diamond & Jewelry Inc

	PATENT OR TRADEMARK NO.	DATE OF PATENT OR TRADEMARK	HOLDER OF PATENT OR TRADEMARK
1	4,086,050	1/17/2012	Boulle Ltd
2			
3			
4			
5			

In the above—entitled case, the following patent(s)/ trademark(s) have been included:

DATE INCLUDED	INCLUDED BY ☑ Amendment ☐ Answer ☐ Cross Bill ☐ Other Pleading	
12/9/2013		
PATENT OR TRADEMARK NO.	**DATE OF PATENT OR TRADEMARK**	**HOLDER OF PATENT OR TRADEMARK**
1 3,078,625	4/11/2006	De Boulle Diamond & Jewelry Inc
2 3,078,627	4/11/2006	De Boulle Diamond & Jewelry Inc
3		
4		
5		

In the above—entitled case, the following decision has been rendered or judgement issued:

DECISION/JUDGEMENT

CLERK	(BY) DEPUTY CLERK	DATE
Karen Mitchell	s/A. Lowe-Monserrate	12/10/2013

Copy 1—Upon initiation of action, mail this copy to Director **Copy 3—Upon termination of action, mail this copy to Director**
Copy 2—Upon filing document adding patent(s), mail this copy to Director **Copy 4—Case file copy**

UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NUMBER	FILING OR 371(C) DATE	FIRST NAMED APPLICANT	ATTY. DOCKET NO./TITLE
11/246,163	10/11/2005	Marcos C. Tzannes	6936-54

CONFIRMATION NO. 5478

POA ACCEPTANCE LETTER

62574
Jason H. Vick
Sheridan Ross, PC
Suite # 1200
1560 Broadway
Denver, CO 80202

OC0000000057768266

Date Mailed: 11/27/2012

NOTICE OF ACCEPTANCE OF POWER OF ATTORNEY

This is in response to the Power of Attorney filed 11/08/2012.

The Power of Attorney in this application is accepted. Correspondence in this application will be mailed to the above address as provided by 37 CFR 1.33.

/hchristian/

Office of Data Management, Application Assistance Unit (571) 272-4000, or (571) 272-4200, or 1-888-786-0101

UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
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www.uspto.gov

APPLICATION NUMBER	FILING OR 371(C) DATE	FIRST NAMED APPLICANT	ATTY. DOCKET NO./TITLE
11/246,163	10/11/2005	Marcos C. Tzannes	6936-54

CONFIRMATION NO. 5478

POWER OF ATTORNEY NOTICE

62574
Jason H. Vick
Sheridan Ross, PC
Suite # 1200
1560 Broadway
Denver, CO 80202

OC000000057768265

Date Mailed: 11/27/2012

NOTICE REGARDING CHANGE OF POWER OF ATTORNEY

This is in response to the Power of Attorney filed 11/08/2012.

- The Power of Attorney to you in this application has been revoked by the assignee who has intervened as provided by 37 CFR 3.71. Future correspondence will be mailed to the new address of record(37 CFR 1.33).

/hchristian/

Office of Data Management, Application Assistance Unit (571) 272-4000, or (571) 272-4200, or 1-888-786-0101

PTO/AIA/80 (07-12)
Approved for use through 11/30/2014. OMB 0651-0035
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POWER OF ATTORNEY TO PROSECUTE APPLICATIONS BEFORE THE USPTO

I hereby revoke all previous powers of attorney given in the application identified in the attached statement under 37 CFR 3.73(c).

I hereby appoint:

■ Practitioners associated with Customer Number: 62574

OR

☐ Practitioner(s) named below (if more than ten patent practitioners are to be named, then a customer number must be used):

Name	Registration Number	Name	Registration Number

As attorney(s) or agent(s) to represent the undersigned before the United States Patent and Trademark Office (USPTO) in connection with any and all patent applications assigned only to the undersigned according to the USPTO assignment records or assignments documents attached to this form in accordance with 37 CFR 3.73(c).

Please change the correspondence address for the application identified in the attached statement under 37 CFR 3.73(c) to:

■ The address associated with Customer Number: 62574

OR

☐

Firm or Individual Name			
Address			
City		State	Zip
Country			
Telephone		Email	

Assignee Name and Address: TQ DELTA, LLC
805 Las Cimas Parkway, Suite 240
Austin, Texas 78746

A copy of this form, together with a statement under 37 CFR 3.73(c) (Form PTO/AIA/96 or equivalent) is required to be Filed in each application in which this form is used. The statement under 37 CFR 3.73(c) may be completed by one of The practitioners appointed in this form, and must identify the application in which this Power of Attorney is to be filed.

SIGNATURE of Assignee of Record
The individual whose signature and title is supplied below is authorized to act on behalf of the assignee

Signature	Mark K. Roche	Date	10/4/12
Name	Mark K. Roche	Telephone	512-609-1810
Title	Managing Director		

This collection of information is required by 37 CFR 1.31, 1.32 and 1.33. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.11 and 1.14. This collection is estimated to take 3 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

If you need assistance in completing the form, call 1-800-PTO-9199 and select option 2.

Electronic Acknowledgement Receipt	
EFS ID:	14185926
Application Number:	11246163
International Application Number:	
Confirmation Number:	5478
Title of Invention:	RESOURCE SHARING IN A TELECOMMUNICATIONS ENVIRONMENT
First Named Inventor/Applicant Name:	Marcos C. Tzannes
Customer Number:	62574
Filer:	Jason Vick/Joanne Vos
Filer Authorized By:	Jason Vick
Attorney Docket Number:	6936-54
Receipt Date:	08-NOV-2012
Filing Date:	11-OCT-2005
Time Stamp:	18:05:44
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	no

File Listing:

Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1		EntityStatus_373c_w_POA.pdf	416983 b944db81c862b6537aa657c06f3bbd2c702f8323	yes	4

	Multipart Description/PDF files in .zip description		
	Document Description	**Start**	**End**
	Miscellaneous Incoming Letter	1	1
	Assignee showing of ownership per 37 CFR 3.73.	2	3
	Power of Attorney	4	4
Warnings:			
Information:			
	Total Files Size (in bytes):	416983	

This Acknowledgement Receipt evidences receipt on the noted date by the USPTO of the indicated documents, characterized by the applicant, and including page counts, where applicable. It serves as evidence of receipt similar to a Post Card, as described in MPEP 503.

<u>New Applications Under 35 U.S.C. 111</u>
If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application.

<u>National Stage of an International Application under 35 U.S.C. 371</u>
If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.

<u>New International Application Filed with the USPTO as a Receiving Office</u>
If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In Re the Application of: Marcos C. Tzannes	)	Issued Patent No.: 7,831,890
Application No.: 11/246,163	)	Issued Date: November 9, 2010
Filed: October 11, 2005	)	Examiner: PFIZENMAYER, Mark C.
Atty. File No.: 6936-54	)	Confirmation No.: 5478

For: RESOURCE SHARING IN A TELECOMMUNICATIONS ENVIRONMENT

ASSERTION OF ENTITLEMENT TO SMALL ENTITY STATUS

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Madam:

In accordance with MPEP §§ 509.02 and 509.03 and 37 CFR 1.27, this document is being filed to inform the U.S. Patent Office of the change of status for the above-identified patent from large entity status to small entity status. All fees paid to date have been paid as large entity status. No fees have yet been paid as small entity status. Due to the sale of the referenced patent, the Applicant is now entitled to small entity status.

We respectfully request that small entity status be granted for the above-referenced patent.

Please contact the undersigned if there are any questions regarding this notification.

Respectfully submitted,

SHERIDAN ROSS P.C.

Date: 8 Nov 12

By: _____

Jason H. Vick
Reg. No. 45,285
1560 Broadway, Suite 1200
Denver, Colorado 80202
Telephone: 303-863-9700

CommScope, Inc.
IPR2023-00064, Ex. 1035
Page 50 of 531

PTO/AIA/96 (08-12)
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U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE
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STATEMENT UNDER 37 CFR 3.73(c)

Applicant/Patent Owner: TQ DELTA, LLC

Application No./Patent No.: 7,831,890 Filed/Issue Date: November 9, 2010

Titled: RESOURCE SHARING IN A TELECOMMUNICATIONS ENVIRONMENT

TQ DELTA, LLC, a Corporation

(Name of Assignee) (Type of Assignee, e.g., corporation, partnership, university, government agency, etc.)

states that, for the patent application/patent identified above, it is (choose **one** of options 1, 2, 3 or 4 below):

1. ☑ The assignee of the entire right, title, and interest.

2. ☐ An assignee of less than the entire right, title, and interest (check applicable box):

   ☐ The extent (by percentage) of its ownership interest is _____%. Additional Statement(s) by the owners holding the balance of the interest must be submitted to account for 100% of the ownership interest.

   ☐ There are unspecified percentages of ownership. The other parties, including inventors, who together own the entire right, title and interest are:

   Additional Statement(s) by the owner(s) holding the balance of the interest must be submitted to account for the entire right, title, and interest.

3. ☐ The assignee of an undivided interest in the entirety (a complete assignment from one of the joint inventors was made). The other parties, including inventors, who together own the entire right, title, and interest are:

   Additional Statement(s) by the owner(s) holding the balance of the interest must be submitted to account for the entire right, title, and interest.

4. ☐ The recipient, via a court proceeding or the like (*e.g.*, bankruptcy, probate), of an undivided interest in the entirety (a complete transfer of ownership interest was made). The certified document(s) showing the transfer is attached.

The interest identified in option 1, 2 or 3 above (not option 4) is evidenced by either (choose **one** of options A or B below):

A. ☐ An assignment from the inventor(s) of the patent application/patent identified above. The assignment was recorded in the United States Patent and Trademark Office at Reel _____, Frame _____, or for which a copy thereof is attached.

B. ☑ A chain of title from the inventor(s), of the patent application/patent identified above, to the current assignee as follows:

1. From: Marcos C. Tzannes, Michael Lund To: AWARE, INC.

   The document was recorded in the United States Patent and Trademark Office at

   Reel 017438, Frame 0094, or for which a copy thereof is attached.

2. From: AWARE, INC. To: TQ DELTA, LLC

   The document was recorded in the United States Patent and Trademark Office at

   Reel 029154, Frame 0937, or for which a copy thereof is attached.

This collection of information is required by 37 CFR 3.73(b). The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.11 and 1.14. This collection is estimated to take 12 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

If you need assistance in completing the form, call 1-800-PTO-9199 and select option 2.

PTO/AIA/96 (08-12)
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STATEMENT UNDER 37 CFR 3.73(c)

3. From: _____ To: _____

The document was recorded in the United States Patent and Trademark Office at

Reel _____, Frame _____, or for which a copy thereof is attached.

4. From: _____ To: _____

The document was recorded in the United States Patent and Trademark Office at

Reel _____, Frame _____, or for which a copy thereof is attached.

5. From: _____ To: _____

The document was recorded in the United States Patent and Trademark Office at

Reel _____, Frame _____, or for which a copy thereof is attached.

6. From: _____ To: _____

The document was recorded in the United States Patent and Trademark Office at

Reel _____, Frame _____, or for which a copy thereof is attached.

☐ Additional documents in the chain of title are listed on a supplemental sheet(s).

☑ As required by 37 CFR 3.73(c)(1)(i), the documentary evidence of the chain of title from the original owner to the assignee was, or concurrently is being, submitted for recordation pursuant to 37 CFR 3.11.

[NOTE: A separate copy (i.e., a true copy of the original assignment document(s)) must be submitted to Assignment Division in accordance with 37 CFR Part 3, to record the assignment in the records of the USPTO. See MPEP 302.08]

The undersigned (whose title is supplied below) is authorized to act on behalf of the assignee.

Signature	Date 8 Nov 12
Jason H. Vick	45,285
Printed or Typed Name	Title or Registration Number

UNITED STATES PATENT AND TRADEMARK OFFICE

CERTIFICATE OF CORRECTION

PATENT NO.	: 7,831,890 B2
APPLICATION NO.	: 11/246163
DATED	: November 9, 2010
INVENTOR(S)	: Marcos C. Tzannes et al.

It is certified that error appears in the above-identified patent and that said Letters Patent is hereby corrected as shown below:

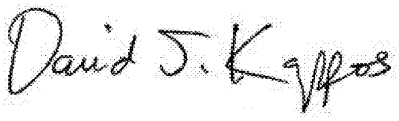
In the claims:

In column 11, claim 5, line 18, delete “transmission” and insert -- reception --

In column 12, claim 5, line 3, delete “received” and insert -- transmitted --

In column 12, claim 5, line 8, delete “shred” and insert -- shared --

Signed and Sealed this
Eighth Day of February, 2011



David J. Kappos
Director of the United States Patent and Trademark Office

SPE RESPONSE FOR CERTIFICATE OF CORRECTION

Paper No.: _____

DATE : 01/11/11

TO SPE OF : ART UNIT: 2447 Attn: HWANG JOON H (SPE)

SUBJECT : Request for Certificate of Correction for Appl. No.: 11/246163 Patent No.: 7831890

CofC Mailroom date: 01/05/11

Please respond to this request for a certificate of correction within 7 days.

FOR IFW FILES:

Please review the requested changes/corrections as shown in the **COCIN** document(s) in the IFW application image. No new matter should be introduced, nor should the scope or meaning of the claims be changed.

Please complete the response (see below) and forward the completed response to scanning using document code **COCX**.

FOR PAPER FILES:

Please review the requested changes/corrections as shown in the attached certificate of correction. Please complete this form (see below) and forward it with the file to:

Certificates of Correction Branch (CofC)
Randolph Square – 9D10-A
Palm Location 7580

Tasneem Siddiqui
Certificates of Correction Branch
703-756-1593 or 703-756-1814

Thank You For Your Assistance

The request for issuing the above-identified correction(s) is hereby:
Note your decision on the appropriate box.

X **Approved**	**All** changes apply.
❑ **Approved in Part**	Specify below which changes **do not** apply.
❑ **Denied**	State the reasons for denial below.

Comments: Approved.

/Joon H. Hwang/ 2447
SPE **Art Unit**

PTOL-306 (REV. 7/03) U.S. DEPARTMENT OF COMMERCE Patent and Trademark Office

PTO/SB/44 (09-07)
Approved for use through 08/31/2013. OMB 0651-0033
U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE
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(Also Form PTO-1050)

UNITED STATES PATENT AND TRADEMARK OFFICE
CERTIFICATE OF CORRECTION

PATENT NO. : 7,831,890 B2

APPLICATION NO.: 11/246,163

ISSUE DATE : November 9, 2010

INVENTOR(S) : Marcos C. Tzannes et al.

It is certified that an error appears or errors appear in the above-identified patent and that said Letters Patent is hereby corrected as shown below:

IN THE CLAIMS:

In column 11, claim 5, line 18, delete "transmission" and insert – reception –

In column 12, claim 5, line 3, delete "received" and insert -- transmitted –

In column 12, claim 5, line 8, delete "shred" and insert – shared –

MAILING ADDRESS OF SENDER (Please do not use customer number below):

Jason H. Vick c/o Sheridan Ross, PC
1560 Broadway, Suite 1200
Denver, CO 80202

This collection of information is required by 37 CFR 1.322, 1.323, and 1.324. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 1.0 hour to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Attention Certificate of Corrections Branch, Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

If you need assistance in completing the form, call 1-800-PTO-9199 and select option 2.

SPE RESPONSE FOR CERTIFICATE OF CORRECTION

Paper No.: _____

DATE : 01/11/11

TO SPE OF : ART UNIT: 2447 Attn: HWANG JOON H (SPE)

SUBJECT : Request for Certificate of Correction for Appl. No.: 11/246163 Patent No.: 7831890

CofC Mailroom date: 01/05/11

Please respond to this request for a certificate of correction within 7 days.

FOR IFW FILES:

Please review the requested changes/corrections as shown in the **COCIN** document(s) in the IFW application image. No new matter should be introduced, nor should the scope or meaning of the claims be changed.

Please complete the response (see below) and forward the completed response to scanning using document code **COCX**.

FOR PAPER FILES:

Please review the requested changes/corrections as shown in the attached certificate of correction. Please complete this form (see below) and forward it with the file to:

Certificates of Correction Branch (CofC)
Randolph Square – 9D10-A
Palm Location 7580

Tasneem Siddiqui
Certificates of Correction Branch
703-756-1593 or 703-756-1814

Thank You For Your Assistance

The request for issuing the above-identified correction(s) is hereby:
Note your decision on the appropriate box.

- ☐ **Approved** — **All** changes apply.
- ☐ **Approved in Part** — Specify below which changes **do not** apply.
- ☐ **Denied** — State the reasons for denial below.

Comments: _____

_____

_____

_____ _____
SPE **Art Unit**

PTO/SB/44 (09-07)
Approved for use through 08/31/2013. OMB 0651-0033
U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE
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(Also Form PTO-1050)

UNITED STATES PATENT AND TRADEMARK OFFICE
CERTIFICATE OF CORRECTION

PATENT NO. : 7,831,890 B2

APPLICATION NO.: 11/246,163

ISSUE DATE : November 9, 2010

INVENTOR(S) : Marcos C. Tzannes et al.

It is certified that an error appears or errors appear in the above-identified patent and that said Letters Patent is hereby corrected as shown below:

IN THE CLAIMS:

In column 11, claim 5, line 18, delete "transmission" and insert -- reception --

In column 12, claim 5, line 3, delete "received" and insert -- transmitted --

In column 12, claim 5, line 8, delete "shred" and insert -- shared --

MAILING ADDRESS OF SENDER (Please do not use customer number below):

Jason H. Vick c/o Sheridan Ross, PC
1560 Broadway, Suite 1200
Denver, CO 80202

This collection of information is required by 37 CFR 1.322, 1.323, and 1.324. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 1.0 hour to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Attention Certificate of Corrections Branch, Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

If you need assistance in completing the form, call 1-800-PTO-9199 and select option 2.

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In Re the Application of: Marcos C. Tzannes

Application No.: 11/246,163

Patent No.: 7,831,890

Issued: November 9, 2010

Confirmation No.: 5478

Atty. File No.: 5550-54

For: RESOURCE SHARING IN A TELECOMMUNICATIONS ENVIRONMENT

REQUEST FOR CERTIFICATE OF CORRECTION OF PATENT FOR OFFICE'S MISTAKE (37 C.F.R. §1.322) AND APPLICANT'S MISTAKE (37 C.F.R §1.323)

Attn: Certificate of Corrections Branch
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Sir:

This is a request for a Certificate of Correction under 37 C.F.R. 1.322 and 1.323 for the above-identified patent. Attached is form PTO/SB/44. Applicants have determined that there were typographic errors in claim 5 which were the mistake of both the Office and the Applicant. The corrections do not introduce new matter, do not require re-examination, and do not materially affect the scope or meaning of the patent.

CommScope, Inc.
IPR2023-00064, Ex. 1035
Page 58 of 531

Payment in the amount of $100.00, as required by 37 C.F.R. § 1.20(a) is being submitted herewith. Although no additional fees are believed due in connection with the filing of this paper, please charge any additional fees deemed necessary or credit any overpayment to Deposit Account No. 19-1970.

Respectfully submitted,

SHERIDAN ROSS P.C.

Date: 5 Jan '11

By: _____

Jason H. Vick
Reg. No. 45,285
1560 Broadway, Suite 1200
Denver, Colorado 80202
Telephone: 303-863-9700

CommScope, Inc.
IPR2023-00064, Ex. 1035
Page 59 of 531

PTO/SB/44 (09-07)
Approved for use through 08/31/2013. OMB 0651-0033
U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE
Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it displays a valid OMB control number.
(Also Form PTO-1050)

UNITED STATES PATENT AND TRADEMARK OFFICE
CERTIFICATE OF CORRECTION

PATENT NO. : 7,831,890

APPLICATION NO.: 11/246,163

ISSUE DATE : November 9, 2010

INVENTOR(S) : Marcos C. Tzannes et al.

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In column 11, claim 5, line 18, delete "transmission" and insert -- reception --

In column 12, claim 5, line 3, delete "received" and insert -- transmitted --

In column 12, claim 5, line 8, delete "shred" and insert -- shared --

MAILING ADDRESS OF SENDER (Please do not use customer number below):

Jason H. Vick c/o Sheridan Ross, PC
1560 Broadway, Suite 1200
Denver, CO 80202

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If you need assistance in completing the form, call 1-800-PTO-9199 and select option 2.

Electronic Patent Application Fee Transmittal	
Application Number:	11246163
Filing Date:	11-Oct-2005
Title of Invention:	RESOURCE SHARING IN A TELECOMMUNICATIONS ENVIRONMENT
First Named Inventor/Applicant Name:	Marcos C. Tzannes
Filer:	Jason Vick/Joanne Vos
Attorney Docket Number:	5550-54
Filed as Large Entity	

Utility under 35 USC 111(a) Filing Fees

Description	Fee Code	Quantity	Amount	Sub-Total in USD($)
Basic Filing:				
Pages:				
Claims:				
Miscellaneous-Filing:				
Petition:				
Patent-Appeals-and-Interference:				
Post-Allowance-and-Post-Issuance:				
Certificate of correction	1811	1	100	100
Extension-of-Time:				

Description	Fee Code	Quantity	Amount	Sub-Total in USD($)
Miscellaneous:				
		Total in USD ($)		**100**

Electronic Acknowledgement Receipt	
EFS ID:	9172791
Application Number:	11246163
International Application Number:	
Confirmation Number:	5478
Title of Invention:	RESOURCE SHARING IN A TELECOMMUNICATIONS ENVIRONMENT
First Named Inventor/Applicant Name:	Marcos C. Tzannes
Customer Number:	62574
Filer:	Jason Vick/Joanne Vos
Filer Authorized By:	Jason Vick
Attorney Docket Number:	5550-54
Receipt Date:	05-JAN-2011
Filing Date:	11-OCT-2005
Time Stamp:	18:12:11
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	yes
Payment Type	Deposit Account
Payment was successfully received in RAM	$100
RAM confirmation Number	7865
Deposit Account	191970
Authorized User	
The Director of the USPTO is hereby authorized to charge indicated fees and credit any overpayment as follows: Charge any Additional Fees required under 37 C.F.R. Section 1.20 (Post Issuance fees)	

File Listing:

Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1	Request for Certificate of Correction	Request_For_Certificate_of_Correction.pdf	74065 3a3c18c563e7e7e78aa44aef240b4f5f5ac63c9a	no	3
Warnings:					
Information:					
2	Fee Worksheet (PTO-875)	fee-info.pdf	29681 840faee51128a5eb6ff1017cc9b99a2b72b81b04	no	2
Warnings:					
Information:					
		Total Files Size (in bytes):	103746		

This Acknowledgement Receipt evidences receipt on the noted date by the USPTO of the indicated documents, characterized by the applicant, and including page counts, where applicable. It serves as evidence of receipt similar to a Post Card, as described in MPEP 503.

New Applications Under 35 U.S.C. 111
If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application.

National Stage of an International Application under 35 U.S.C. 371
If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.

New International Application Filed with the USPTO as a Receiving Office
If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.

UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	ISSUE DATE	PATENT NO.	ATTORNEY DOCKET NO.	CONFIRMATION NO.
11/246,163	11/09/2010	7831890	5550-54	5478

62574 7590 10/20/2010

Jason H. Vick
Sheridan Ross, PC
Suite # 1200
1560 Broadway
Denver, CO 80202

ISSUE NOTIFICATION

The projected patent number and issue date are specified above.

Determination of Patent Term Adjustment under 35 U.S.C. 154 (b)
(application filed on or after May 29, 2000)

The Patent Term Adjustment is 1123 day(s). Any patent to issue from the above-identified application will include an indication of the adjustment on the front page.

If a Continued Prosecution Application (CPA) was filed in the above-identified application, the filing date that determines Patent Term Adjustment is the filing date of the most recent CPA.

Applicant will be able to obtain more detailed information by accessing the Patent Application Information Retrieval (PAIR) WEB site (http://pair.uspto.gov).

Any questions regarding the Patent Term Extension or Adjustment determination should be directed to the Office of Patent Legal Administration at (571)-272-7702. Questions relating to issue and publication fee payments should be directed to the Application Assistance Unit (AAU) of the Office of Data Management (ODM) at (571)-272-4200.

APPLICANT(s) (Please see PAIR WEB site http://pair.uspto.gov for additional applicants):

Marcos C. Tzannes, Orinda, CA;
Michael Lund, West Newton, MA;

PART B - FEE(S) TRANSMITTAL

Complete and send this form, together with applicable fee(s), to: Mail **Mail Stop ISSUE FEE**
Commissioner for Patents
P.O. Box 1450
Alexandria, Virginia 22313-1450
or Fax (571)-273-2885

INSTRUCTIONS: This form should be used for transmitting the ISSUE FEE and PUBLICATION FEE (if required). Blocks 1 through 5 should be completed where appropriate. All further correspondence including the Patent, advance orders and notification of maintenance fees will be mailed to the current correspondence address as indicated unless corrected below or directed otherwise in Block 1, by (a) specifying a new correspondence address; and/or (b) indicating a separate "FEE ADDRESS" for maintenance fee notifications.

CURRENT CORRESPONDENCE ADDRESS (Note: Use Block 1 for any change of address)

62574 7590 09/07/2010

Jason H. Vick
Sheridan Ross, PC
Suite # 1200
1560 Broadway
Denver, CO 80202

Note: A certificate of mailing can only be used for domestic mailings of the Fee(s) Transmittal. This certificate cannot be used for any other accompanying papers. Each additional paper, such as an assignment or formal drawing, must have its own certificate of mailing or transmission.

Certificate of Mailing or Transmission
I hereby certify that this Fee(s) Transmittal is being deposited with the United States Postal Service with sufficient postage for first class mail in an envelope addressed to the Mail Stop ISSUE FEE address above, or being facsimile transmitted to the USPTO (571) 273-2885, on the date indicated below.

(Depositor's name)
(Signature)
(Date)

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
11/246,163	10/11/2005	Marcos C. Tzannes	5550-54	5478

TITLE OF INVENTION: RESOURCE SHARING IN A TELECOMMUNICATIONS ENVIRONMENT

APPLN. TYPE	SMALL ENTITY	ISSUE FEE DUE	PUBLICATION FEE DUE	PREV. PAID ISSUE FEE	TOTAL FEE(S) DUE	DATE DUE
nonprovisional	NO	$1510	$300	$0	$1810	12/07/2010

EXAMINER	ART UNIT	CLASS-SUBCLASS
PFIZENMAYER, MARK C	2447	714-774000

1. Change of correspondence address or indication of "Fee Address" (37 CFR 1.363).
☐ Change of correspondence address (or Change of Correspondence Address form PTO/SB/122) attached.
☐ "Fee Address" indication (or "Fee Address" Indication form PTO/SB/47; Rev 03-02 or more recent) attached. **Use of a Customer Number is required.**

2. For printing on the patent front page, list
(1) the names of up to 3 registered patent attorneys or agents OR, alternatively,
(2) the name of a single firm (having as a member a registered attorney or agent) and the names of up to 2 registered patent attorneys or agents. If no name is listed, no name will be printed.

1 Jason H. Vick
2 Sheridan Ross, P.C.
3

3. ASSIGNEE NAME AND RESIDENCE DATA TO BE PRINTED ON THE PATENT (print or type)

PLEASE NOTE: Unless an assignee is identified below, no assignee data will appear on the patent. If an assignee is identified below, the document has been filed for recordation as set forth in 37 CFR 3.11. Completion of this form is NOT a substitute for filing an assignment.

(A) NAME OF ASSIGNEE: Aware, Inc.

(B) RESIDENCE: (CITY and STATE OR COUNTRY): Bedford, MA

Please check the appropriate assignee category or categories (will not be printed on the patent): ☐ Individual ☑ Corporation or other private group entity ☐ Government

4a. The following fee(s) are submitted:
☑ Issue Fee
☑ Publication Fee (No small entity discount permitted)
☐ Advance Order - # of Copies _____

4b. Payment of Fee(s): **(Please first reapply any previously paid issue fee shown above)**
☐ A check is enclosed.
☐ Payment by credit card. Form PTO-2038 is attached.
☑ The Director is hereby authorized to charge the required fee(s), any deficiency, or credit any overpayment, to Deposit Account Number 191970 (enclose an extra copy of this form).

5. **Change in Entity Status** (from status indicated above)
☐ a. Applicant claims SMALL ENTITY status. See 37 CFR 1.27.
☐ b. Applicant is no longer claiming SMALL ENTITY status. See 37 CFR 1.27(g)(2).

NOTE: The Issue Fee and Publication Fee (if required) will not be accepted from anyone other than the applicant; a registered attorney or agent; or the assignee or other party in interest as shown by the records of the United States Patent and Trademark Office.

Authorized Signature _____ Date 4 Oct 10

Typed or printed name Jason H. Vick Registration No. 45,285

This collection of information is required by 37 CFR 1.311. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 12 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, Virginia 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, Virginia 22313-1450.

Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it displays a valid OMB control number.

CommScope, Inc.
IPR2023-00064, Ex. 1035
Page 66 of 531

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In Re the Application of: Marcos C. Tzannes	)	Group Art Unit: 2447
Application No.: 11/246,163	)	Examiner: Pfizenmayer, Mark C.
Filed: October 11, 2005	)	Confirmation No.: 5478
Atty. File No.: 5550-54	)	

For: RESOURCE SHARING IN A TELECOMMUNICATIONS ENVIRONMENT

COMMENTS ON STATEMENT OF REASONS FOR ALLOWANCE

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313

Sir:

Applicant submits this Comments on Statement of Reasons for Allowance to address further the Notice of Allowability ("Notice") having a mailing date of September 7, 2010.

In the Notice, the Examiner's stated reasons for allowance were that:

> Claim 46 identifies the distinct features of specifying a maximum number of bytes available to be allocated to an interleaver in a transmitted or received message, determining the amount of memory required by the interleaver, and then allocating the bytes of a shared memory to the interleaver wherein the bytes allocated do not exceed the maximum number of available bytes specified in the message.
>
> The closest prior art, Fadavi-Ardekani et al (U.S. Pat. No. 6,707,822) discloses sharing a memory between the interleavers and deinterleavers of multiple ADSL sessions, fails to suggest limiting the memory allocated to the interleaver to a maximum number of bytes available that was specified in a transmitted or received message. The above features in conjunction with all other limitations of the dependent and independent claims 46-49 are hereby allowed.
>
> Claim 50 identifies the distinct features of specifying a maximum number of bytes available to be allocated to a deinterleaver in a transmitted or received message, determining the amount of memory required by the deinterleaver, and then allocating the bytes of a shared memory to the deinterleaver wherein the bytes allocated do not exceed the maximum number of available bytes specified in the message.

CommScope, Inc.
IPR2023-00064, Ex. 1035
Page 67 of 531

The closest prior art, Fadavi-Ardekani et al (U.S. Pat. No. 6,707,822) discloses sharing a memory between the interleavers and deinterleavers of multiple ADSL sessions, fails to suggest limiting the memory allocated to the deinterleaver to a maximum number of bytes available that was specified in a transmitted or received message. The above features in conjunction with all other limitations of the dependent and independent claims 50-53 are hereby allowed.

Based on the Notice, the patentability of all other independent and dependent claims is assumed to be based upon the elements as set forth in such claims and that such claims meet all criteria for patentability under §101, §102, §103 and §112.

As is clear from MPEP 1302.14,

"The statement [of reasons for allowance] is not intended to necessarily state all the reasons for allowance or all the details why claims are allowed and should not be written to specifically or impliedly state that all the reasons for allowance are set forth."

While the stated Reasons for Allowance may be a stated reason for allowing some independent claims, Applicant submits that some independent claims have a different reason for allowance and that some independent claims have other reasons for allowance.

Specifically, the prior art fails to teach the specific combination of features as recited in the independent claims 46 and 50.

Although the Applicant believes that no fees are due for filing this Comments on Statement of Reasons for Allowance, please charge any fees deemed necessary to Deposit Account No. 19-1970.

Respectfully submitted,

SHERIDAN ROSS P.C.

Date: 4 05 /10

By: _____

Jason H. Vick
Reg. No. 45,285
1560 Broadway, Suite 1200
Denver, Colorado 80202
Telephone: 303-863-9700

CommScope, Inc.
IPR2023-00064, Ex. 1035
Page 68 of 531

Electronic Patent Application Fee Transmittal	
Application Number:	11246163
Filing Date:	11-Oct-2005
Title of Invention:	RESOURCE SHARING IN A TELECOMMUNICATIONS ENVIRONMENT
First Named Inventor/Applicant Name:	Marcos C. Tzannes
Filer:	Jason Vick/Joanne Vos
Attorney Docket Number:	5550-54
Filed as Large Entity	

Utility under 35 USC 111(a) Filing Fees

Description	Fee Code	Quantity	Amount	Sub-Total in USD($)
Basic Filing:				
Pages:				
Claims:				
Miscellaneous-Filing:				
Petition:				
Patent-Appeals-and-Interference:				
Post-Allowance-and-Post-Issuance:				
Utility Appl issue fee	1501	1	1510	1510
Publ. Fee- early, voluntary, or normal	1504	1	300	300

Description	Fee Code	Quantity	Amount	Sub-Total in USD($)
Extension-of-Time:				
Miscellaneous:				
		Total in USD ($)		**1810**

Electronic Acknowledgement Receipt	
EFS ID:	8557762
Application Number:	11246163
International Application Number:	
Confirmation Number:	5478
Title of Invention:	RESOURCE SHARING IN A TELECOMMUNICATIONS ENVIRONMENT
First Named Inventor/Applicant Name:	Marcos C. Tzannes
Customer Number:	62574
Filer:	Jason Vick/Joanne Vos
Filer Authorized By:	Jason Vick
Attorney Docket Number:	5550-54
Receipt Date:	04-OCT-2010
Filing Date:	11-OCT-2005
Time Stamp:	18:52:22
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	yes
Payment Type	Deposit Account
Payment was successfully received in RAM	$1810
RAM confirmation Number	5484
Deposit Account	191970
Authorized User	
The Director of the USPTO is hereby authorized to charge indicated fees and credit any overpayment as follows: Charge any Additional Fees required under 37 C.F.R. Section 1.16 (National application filing, search, and examination fees) Charge any Additional Fees required under 37 C.F.R. Section 1.17 (Patent application and reexamination processing fees)	

Charge any Additional Fees required under 37 C.F.R. Section 1.19 (Document supply fees)

Charge any Additional Fees required under 37 C.F.R. Section 1.20 (Post Issuance fees)

Charge any Additional Fees required under 37 C.F.R. Section 1.21 (Miscellaneous fees and charges)

File Listing:

Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1		Issue_Fee_Payment.pdf	349265 744b02c1ad64f82ada5fed915e01c6302b508a5c	yes	3

Multipart Description/PDF files in .zip description		
Document Description	**Start**	**End**
Issue Fee Payment (PTO-85B)	1	1
Post Allowance Communication - Incoming	2	3

Warnings:

Information:

2	Fee Worksheet (PTO-875)	fee-info.pdf	31704 def7650a6d2d1ec7cfa2d312f397c2e081207b13	no	2

Warnings:

Information:

Total Files Size (in bytes):	380969

This Acknowledgement Receipt evidences receipt on the noted date by the USPTO of the indicated documents, characterized by the applicant, and including page counts, where applicable. It serves as evidence of receipt similar to a Post Card, as described in MPEP 503.

New Applications Under 35 U.S.C. 111
If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application.

National Stage of an International Application under 35 U.S.C. 371
If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.

New International Application Filed with the USPTO as a Receiving Office
If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.

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Jason H. Vick
Sheridan Ross, PC
Suite # 1200
1560 Broadway
Denver, CO 80202

Courtesy Reminder for
Application Serial No: 11/246,163

Attorney Docket No: 5550-54
Customer Number: 62574
Date of Electronic Notification: 09/07/2010

This is a courtesy reminder that new correspondence is available for this application. The official date of notification of the outgoing correspondence will be indicated on the form PTOL-90 accompanying the correspondence.

An email notification regarding the correspondence was sent to the following email address(es) associated with your customer number:
jvick@sheridanross.com
Please verify that these email addresses are correct.

To view your correspondence online or update your email addresses, please visit us anytime at **https://sportal.uspto.gov/secure/myportal/privatepair.** If you have any questions, please email the Electronic Business Center (EBC) at EBC@uspto.gov or call 1-866-217-9197.

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NOTICE OF ALLOWANCE AND FEE(S) DUE

62574 7590 09/07/2010

Jason H. Vick
Sheridan Ross, PC
Suite # 1200
1560 Broadway
Denver, CO 80202

EXAMINER	
PFIZENMAYER, MARK C	
ART UNIT	PAPER NUMBER
2447	

DATE MAILED: 09/07/2010

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
11/246,163	10/11/2005	Marcos C. Tzannes	5550-54	5478

TITLE OF INVENTION: RESOURCE SHARING IN A TELECOMMUNICATIONS ENVIRONMENT

APPLN. TYPE	SMALL ENTITY	ISSUE FEE DUE	PUBLICATION FEE DUE	PREV. PAID ISSUE FEE	TOTAL FEE(S) DUE	DATE DUE
nonprovisional	NO	$1510	$300	$0	$1810	12/07/2010

THE APPLICATION IDENTIFIED ABOVE HAS BEEN EXAMINED AND IS ALLOWED FOR ISSUANCE AS A PATENT. PROSECUTION ON THE MERITS IS CLOSED. THIS NOTICE OF ALLOWANCE IS NOT A GRANT OF PATENT RIGHTS. THIS APPLICATION IS SUBJECT TO WITHDRAWAL FROM ISSUE AT THE INITIATIVE OF THE OFFICE OR UPON PETITION BY THE APPLICANT. SEE 37 CFR 1.313 AND MPEP 1308.

THE ISSUE FEE AND PUBLICATION FEE (IF REQUIRED) MUST BE PAID WITHIN THREE MONTHS FROM THE MAILING DATE OF THIS NOTICE OR THIS APPLICATION SHALL BE REGARDED AS ABANDONED. THIS STATUTORY PERIOD CANNOT BE EXTENDED. SEE 35 U.S.C. 151. THE ISSUE FEE DUE INDICATED ABOVE DOES NOT REFLECT A CREDIT FOR ANY PREVIOUSLY PAID ISSUE FEE IN THIS APPLICATION. IF AN ISSUE FEE HAS PREVIOUSLY BEEN PAID IN THIS APPLICATION (AS SHOWN ABOVE), THE RETURN OF PART B OF THIS FORM WILL BE CONSIDERED A REQUEST TO REAPPLY THE PREVIOUSLY PAID ISSUE FEE TOWARD THE ISSUE FEE NOW DUE.

HOW TO REPLY TO THIS NOTICE:

I. Review the SMALL ENTITY status shown above.

If the SMALL ENTITY is shown as YES, verify your current SMALL ENTITY status:

A. If the status is the same, pay the TOTAL FEE(S) DUE shown above.

B. If the status above is to be removed, check box 5b on Part B - Fee(s) Transmittal and pay the PUBLICATION FEE (if required) and twice the amount of the ISSUE FEE shown above, or

If the SMALL ENTITY is shown as NO:

A. Pay TOTAL FEE(S) DUE shown above, or

B. If applicant claimed SMALL ENTITY status before, or is now claiming SMALL ENTITY status, check box 5a on Part B - Fee(s) Transmittal and pay the PUBLICATION FEE (if required) and 1/2 the ISSUE FEE shown above.

II. PART B - FEE(S) TRANSMITTAL, or its equivalent, must be completed and returned to the United States Patent and Trademark Office (USPTO) with your ISSUE FEE and PUBLICATION FEE (if required). If you are charging the fee(s) to your deposit account, section "4b" of Part B - Fee(s) Transmittal should be completed and an extra copy of the form should be submitted. If an equivalent of Part B is filed, a request to reapply a previously paid issue fee must be clearly made, and delays in processing may occur due to the difficulty in recognizing the paper as an equivalent of Part B.

III. All communications regarding this application must give the application number. Please direct all communications prior to issuance to Mail Stop ISSUE FEE unless advised to the contrary.

IMPORTANT REMINDER: Utility patents issuing on applications filed on or after Dec. 12, 1980 may require payment of maintenance fees. It is patentee's responsibility to ensure timely payment of maintenance fees when due.

PTOL-85 (Rev. 08/07) Approved for use through 08/31/2010.

PART B - FEE(S) TRANSMITTAL

Complete and send this form, together with applicable fee(s), to: Mail **Mail Stop ISSUE FEE**
Commissioner for Patents
P.O. Box 1450
Alexandria, Virginia 22313-1450
or Fax (571)-273-2885

INSTRUCTIONS: This form should be used for transmitting the ISSUE FEE and PUBLICATION FEE (if required). Blocks 1 through 5 should be completed where appropriate. All further correspondence including the Patent, advance orders and notification of maintenance fees will be mailed to the current correspondence address as indicated unless corrected below or directed otherwise in Block 1, by (a) specifying a new correspondence address; and/or (b) indicating a separate "FEE ADDRESS" for maintenance fee notifications.

CURRENT CORRESPONDENCE ADDRESS (Note: Use Block 1 for any change of address)

62574 7590 09/07/2010

Jason H. Vick
Sheridan Ross, PC
Suite # 1200
1560 Broadway
Denver, CO 80202

Note: A certificate of mailing can only be used for domestic mailings of the Fee(s) Transmittal. This certificate cannot be used for any other accompanying papers. Each additional paper, such as an assignment or formal drawing, must have its own certificate of mailing or transmission.

Certificate of Mailing or Transmission

I hereby certify that this Fee(s) Transmittal is being deposited with the United States Postal Service with sufficient postage for first class mail in an envelope addressed to the Mail Stop ISSUE FEE address above, or being facsimile transmitted to the USPTO (571) 273-2885, on the date indicated below.

(Depositor's name)

(Signature)

(Date)

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
11/246,163	10/11/2005	Marcos C. Tzannes	5550-54	5478

TITLE OF INVENTION: RESOURCE SHARING IN A TELECOMMUNICATIONS ENVIRONMENT

APPLN. TYPE	SMALL ENTITY	ISSUE FEE DUE	PUBLICATION FEE DUE	PREV. PAID ISSUE FEE	TOTAL FEE(S) DUE	DATE DUE
nonprovisional	NO	$1510	$300	$0	$1810	12/07/2010

EXAMINER	ART UNIT	CLASS-SUBCLASS
PFIZENMAYER, MARK C	2447	714-774000

1. Change of correspondence address or indication of "Fee Address" (37 CFR 1.363).

❑ Change of correspondence address (or Change of Correspondence Address form PTO/SB/122) attached.

❑ "Fee Address" indication (or "Fee Address" Indication form PTO/SB/47; Rev 03-02 or more recent) attached. **Use of a Customer Number is required.**

2. For printing on the patent front page, list

(1) the names of up to 3 registered patent attorneys or agents OR, alternatively,

(2) the name of a single firm (having as a member a registered attorney or agent) and the names of up to 2 registered patent attorneys or agents. If no name is listed, no name will be printed.

1 _____

2 _____

3 _____

3. ASSIGNEE NAME AND RESIDENCE DATA TO BE PRINTED ON THE PATENT (print or type)

PLEASE NOTE: Unless an assignee is identified below, no assignee data will appear on the patent. If an assignee is identified below, the document has been filed for recordation as set forth in 37 CFR 3.11. Completion of this form is NOT a substitute for filing an assignment.

(A) NAME OF ASSIGNEE (B) RESIDENCE: (CITY and STATE OR COUNTRY)

Please check the appropriate assignee category or categories (will not be printed on the patent) : ❑ Individual ❑ Corporation or other private group entity ❑ Government

4a. The following fee(s) are submitted:

❑ Issue Fee

❑ Publication Fee (No small entity discount permitted)

❑ Advance Order - # of Copies _____

4b. Payment of Fee(s): **(Please first reapply any previously paid issue fee shown above)**

❑ A check is enclosed.

❑ Payment by credit card. Form PTO-2038 is attached.

❑ The Director is hereby authorized to charge the required fee(s), any deficiency, or credit any overpayment, to Deposit Account Number _____ (enclose an extra copy of this form).

5. **Change in Entity Status** (from status indicated above)

❑ a. Applicant claims SMALL ENTITY status. See 37 CFR 1.27.

❑ b. Applicant is no longer claiming SMALL ENTITY status. See 37 CFR 1.27(g)(2).

NOTE: The Issue Fee and Publication Fee (if required) will not be accepted from anyone other than the applicant; a registered attorney or agent; or the assignee or other party in interest as shown by the records of the United States Patent and Trademark Office.

Authorized Signature _____ Date _____

Typed or printed name _____ Registration No. _____

This collection of information is required by 37 CFR 1.311. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 12 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, Virginia 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, Virginia 22313-1450.

Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it displays a valid OMB control number.

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IPR2023-00064, Ex. 1035
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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
11/246,163	10/11/2005	Marcos C. Tzannes	5550-54	5478

62574 7590 09/07/2010

Jason H. Vick
Sheridan Ross, PC
Suite # 1200
1560 Broadway
Denver, CO 80202

EXAMINER	
PFIZENMAYER, MARK C	
ART UNIT	PAPER NUMBER
2447	

DATE MAILED: 09/07/2010

Determination of Patent Term Adjustment under 35 U.S.C. 154 (b)
(application filed on or after May 29, 2000)

The Patent Term Adjustment to date is 828 day(s). If the issue fee is paid on the date that is three months after the mailing date of this notice and the patent issues on the Tuesday before the date that is 28 weeks (six and a half months) after the mailing date of this notice, the Patent Term Adjustment will be 828 day(s).

If a Continued Prosecution Application (CPA) was filed in the above-identified application, the filing date that determines Patent Term Adjustment is the filing date of the most recent CPA.

Applicant will be able to obtain more detailed information by accessing the Patent Application Information Retrieval (PAIR) WEB site (http://pair.uspto.gov).

Any questions regarding the Patent Term Extension or Adjustment determination should be directed to the Office of Patent Legal Administration at (571)-272-7702. Questions relating to issue and publication fee payments should be directed to the Customer Service Center of the Office of Patent Publication at 1-(888)-786-0101 or (571)-272-4200.

PTOL-85 (Rev. 08/07) Approved for use through 08/31/2010.

Notice of Allowability	Application No.	Applicant(s)	
	11/246,163	TZANNES ET AL.	
	Examiner	Art Unit	
	MARK PFIZENMAYER	2447	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address--

All claims being allowable, PROSECUTION ON THE MERITS IS (OR REMAINS) CLOSED in this application. If not included herewith (or previously mailed), a Notice of Allowance (PTOL-85) or other appropriate communication will be mailed in due course. **THIS NOTICE OF ALLOWABILITY IS NOT A GRANT OF PATENT RIGHTS.** This application is subject to withdrawal from issue at the initiative of the Office or upon petition by the applicant. See 37 CFR 1.313 and MPEP 1308.

1. ☒ This communication is responsive to *a telephone communications with Jason Vick (Reg. No. 45,285) on August 2 and 3, 2010*.

2. ☒ The allowed claim(s) is/are *46-53 (renumbered as claims 1-8)*.

3. ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
   a) ☐ All b) ☐ Some* c) ☐ None of the:
      1. ☐ Certified copies of the priority documents have been received.
      2. ☐ Certified copies of the priority documents have been received in Application No. _____ .
      3. ☐ Copies of the certified copies of the priority documents have been received in this national stage application from the International Bureau (PCT Rule 17.2(a)).

   * Certified copies not received: _____.

Applicant has THREE MONTHS FROM THE "MAILING DATE" of this communication to file a reply complying with the requirements noted below. Failure to timely comply will result in ABANDONMENT of this application.
THIS THREE-MONTH PERIOD IS NOT EXTENDABLE.

4. ☐ A SUBSTITUTE OATH OR DECLARATION must be submitted. Note the attached EXAMINER'S AMENDMENT or NOTICE OF INFORMAL PATENT APPLICATION (PTO-152) which gives reason(s) why the oath or declaration is deficient.

5. ☐ CORRECTED DRAWINGS (as "replacement sheets") must be submitted.
   (a) ☐ including changes required by the Notice of Draftsperson's Patent Drawing Review (PTO-948) attached
      1) ☐ hereto or 2) ☐ to Paper No./Mail Date _____.
   (b) ☐ including changes required by the attached Examiner's Amendment / Comment or in the Office action of Paper No./Mail Date _____.

   Identifying indicia such as the application number (see 37 CFR 1.84(c)) should be written on the drawings in the front (not the back) of each sheet. Replacement sheet(s) should be labeled as such in the header according to 37 CFR 1.121(d).

6. ☐ DEPOSIT OF and/or INFORMATION about the deposit of BIOLOGICAL MATERIAL must be submitted. Note the attached Examiner's comment regarding REQUIREMENT FOR THE DEPOSIT OF BIOLOGICAL MATERIAL.

Attachment(s)

1. ☒ Notice of References Cited (PTO-892)
2. ☐ Notice of Draftperson's Patent Drawing Review (PTO-948)
3. ☒ Information Disclosure Statements (PTO/SB/08), Paper No./Mail Date 12/22/09 and 8/9/10
4. ☐ Examiner's Comment Regarding Requirement for Deposit of Biological Material
5. ☐ Notice of Informal Patent Application
6. ☐ Interview Summary (PTO-413), Paper No./Mail Date _____ .
7. ☒ Examiner's Amendment/Comment
8. ☒ Examiner's Statement of Reasons for Allowance
9. ☐ Other _____.

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DETAILED ACTION

1. The applicant cancelled claims 1-45, and added claims 46-29 in the amendment filed on 12/17/2009. The applicant amended claim 46 and added claims 50-53 in the supplemental amendment filed on 12/30/2009. The applicant amended claims 46 and 50 in the supplemental amendment filed on 3/8/2010. Claims 46-53 are pending.

EXAMINER'S AMENDMENT

2. An examiner's amendment to the record appears below. Should the changes and/or additions be unacceptable to applicant, an amendment may be filed as provided by 37 CFR 1.312. To ensure consideration of such an amendment, it MUST be submitted no later than the payment of the issue fee.

3. Authorization for this examiner's amendment was given in a telephone interviews with Jason Vick (Reg. No. 45,285) on August 2 and 3, 2010.

4. The application has been amended as follows:

- Replace claim 46 with:

46. A method of allocating shared memory in a transceiver comprising:

transmitting or receiving, by the transceiver, a message during initialization specifying a maximum number of bytes of memory that are available to be allocated to an interleaver;

determining, at the transceiver, an amount of memory required by the interleaver to interleave a first plurality of Reed Solomon (RS) coded data bytes within a shared memory;

allocating, in the transceiver, a first number of bytes of the shared memory to the interleaver to interleave the first plurality of Reed Solomon (RS) coded data bytes for

transmission at a first data rate, wherein the allocated memory for the interleaver does not exceed the maximum number of bytes specified in the message;

allocating, in the transceiver, a second number of bytes of the shared memory to a deinterleaver to deinterleave a second plurality of RS coded data bytes received at a second data rate; and

interleaving the first plurality of RS coded data bytes within the shared memory allocated to the interleaver and deinterleaving the second plurality of RS coded data bytes within the shared memory allocated to the deinterleaver, wherein the shared memory allocated to the interleaver is used at the same time as the shared memory allocated to the deinterleaver.

- Replace claim 47 with:

47. The method of claim 46, wherein the determining is based on an impulse noise protection requirement.

- Replace claim 48 with:

48. The method of claim 46, wherein the determining is based on a latency requirement.

- Replace claim 49 with:

49. The method of claim 46, wherein the determining is based on a bit error rate requirement.

- Replace claim 50 with:

50. A method of allocating shared memory in a transceiver comprising:

transmitting or receiving, by the transceiver, a message during initialization specifying a maximum number of bytes of memory that are available to be allocated to a deinterleaver;

determining, at the transceiver, an amount of memory required by the deinterleaver to deinterleave a first plurality of Reed Solomon (RS) coded data bytes within a shared memory;

allocating, in the transceiver, a first number of bytes of the shared memory to the deinterleaver to deinterleave a first plurality of Reed Solomon (RS) coded data bytes for transmission at a first data rate, wherein the allocated memory for the deinterleaver does not exceed the maximum number of bytes specified in the message;

allocating, in the transceiver, a second number of bytes of the shared memory to an interleaver to interleave a second plurality of RS coded data bytes received at a second data rate; and

deinterleaving the first plurality of RS coded data bytes within the shared memory allocated to the deinterleaver and interleaving the second plurality of RS coded data bytes within the shred memory allocated to the interleaver, wherein the shared memory allocated to the deinterleaver is used at the same time as the shared memory allocated to the interleaver.

- Replace claim 51 with:

51. The method of claim 50, wherein the determining is based on an impulse noise protection requirement.

- Replace claim 52 with:

52. The method of claim 50, wherein the determining is based on a latency requirement.

- Replace claim 53 with:

53. The method of claim 50, wherein the determining is based on a bit error rate requirement.

Allowable Subject Matter

5. Claims 46-53 are allowed.

Claim 46 identifies the distinct features of specifying a maximum number of bytes available to be allocated to an interleaver in a transmitted or received message, determining the amount of memory required by the interleaver, and then allocating the bytes of a shared memory to the interleaver wherein the bytes allocated do not exceed the maximum number of available bytes specified in the message.

The closest prior art, Fadavi-Ardekani et al (U.S. Pat. No. 6,707,822) discloses sharing a memory between the interleavers and deinterleavers of multiple ADSL sessions, fails to suggest limiting the memory allocated to the interleaver to a maximum number of bytes available that was specified in a transmitted or received message. The above features in conjunction with all other limitations of the dependent and independent claims 46-49 are hereby allowed.

Claim 50 identifies the distinct features of specifying a maximum number of bytes available to be allocated to a deinterleaver in a transmitted or received message, determining the amount of memory required by the deinterleaver, and then allocating the bytes of a shared memory to the deinterleaver wherein the bytes allocated do not exceed the maximum number of available bytes specified in the message.

The closest prior art, Fadavi-Ardekani et al (U.S. Pat. No. 6,707,822) discloses sharing a memory between the interleavers and deinterleavers of multiple ADSL sessions, fails to suggest limiting the memory allocated to the deinterleaver to a maximum number of bytes available that was specified in a transmitted or received message. The above features in conjunction with all other limitations of the dependent and independent claims 50-53 are hereby allowed.

Conclusion

6. Any inquiry concerning this communication or earlier communications from the examiner should be directed to MARK PFIZENMAYER whose telephone number is (571)270-7214. The examiner can normally be reached on Monday - Friday 8:00 - 5:30 EST.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, James Hwang can be reached on (571)272-4036. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

Mark Pfizenmayer
Patent Examiner
3 August 2010

/Joon H. Hwang/
Supervisory Patent Examiner, Art Unit 2447

Notice of References Cited	Application/Control No. 11/246,163	Applicant(s)/Patent Under Reexamination TZANNES ET AL.	
	Examiner MARK PFIZENMAYER	Art Unit 2447	Page 1 of 1

U.S. PATENT DOCUMENTS

*		Document Number Country Code-Number-Kind Code	Date MM-YYYY	Name	Classification
*	A	US-6,707,822	03-2004	Fadavi-Ardekani et al.	370/395.5
	B	US-			
	C	US-			
	D	US-			
	E	US-			
	F	US-			
	G	US-			
	H	US-			
	I	US-			
	J	US-			
	K	US-			
	L	US-			
	M	US-			

FOREIGN PATENT DOCUMENTS

*		Document Number Country Code-Number-Kind Code	Date MM-YYYY	Country	Name	Classification
	N					
	O					
	P					
	Q					
	R					
	S					
	T					

NON-PATENT DOCUMENTS

*		Include as applicable: Author, Title Date, Publisher, Edition or Volume, Pertinent Pages)
	U	
	V	
	W	
	X	

*A copy of this reference is not being furnished with this Office action. (See MPEP § 707.05(a).)
Dates in MM-YYYY format are publication dates. Classifications may be US or foreign.

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Page 83 of 531

Index of Claims	Application/Control No.	Applicant(s)/Patent Under Reexamination
	11246163	TZANNES ET AL.
	Examiner	Art Unit
	Mark Pfizenmayer	2447

✓	Rejected	-	Cancelled	N	Non-Elected	A	Appeal
=	Allowed	÷	Restricted	I	Interference	O	Objected

☐ Claims renumbered in the same order as presented by applicant ☐ CPA ☐ T.D. ☐ R.1.47

CLAIM		DATE								
Final	Original	12/29/2008	12/01/2009	08/03/2010						
	1	✓	✓	-						
	2	✓	✓	-						
	3	✓	✓	-						
	4	✓	✓	-						
	5	✓	✓	-						
	6	✓	✓	-						
	7	✓	✓	-						
	8	✓	✓	-						
	9	✓	✓	-						
	10	✓	✓	-						
	11	✓	✓	-						
	12	✓	✓	-						
	13	✓	✓	-						
	14	✓	✓	-						
	15	✓	✓	-						
	16	✓	✓	-						
	17	✓	✓	-						
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	28	✓	✓	-						
	29	✓	✓	-						
	30	✓	✓	-						
	31	✓	✓	-						
	32	✓	✓	-						
	33	✓	✓	-						
	34	✓	✓	-						
	35	✓	✓	-						
	36	✓	✓	-						

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IPR2023-00064, Ex. 1035
Page 84 of 531

Index of Claims	Application/Control No.	Applicant(s)/Patent Under Reexamination
	11246163	TZANNES ET AL.
	Examiner	Art Unit
	Mark Pfizenmayer	2447

✓	Rejected	-	Cancelled	N	Non-Elected	A	Appeal
=	Allowed	÷	Restricted	I	Interference	O	Objected

☐ Claims renumbered in the same order as presented by applicant ☐ CPA ☐ T.D. ☐ R.1.47

CLAIM		DATE								
Final	Original	12/29/2008	12/01/2009	08/03/2010						
	37	✓	✓	-						
	38	✓	✓	-						
	39	✓	✓	-						
	40	✓	✓	-						
	41	✓	✓	-						
	42	✓	✓	-						
	43	✓	✓	-						
	44	✓	✓	-						
	45	✓	✓	-						
1	46			=						
2	47			=						
3	48			=						
4	49			=						
5	50			=						
6	51			=						
7	52			=						
8	53			=						

CommScope, Inc.
IPR2023-00064, Ex. 1035
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IEEE

SEARCH RESULTS

You searched for: maximum memory available to interleaver

Results per Page 25 Showing 1 - 25 of 9,807 results

Quantum Memory Hierarchies: Efficient Designs to Match Available Parallelism in Quantum Computing

Thaker, D.D.; Metodi, T.S.; Cross, A.W.; Chuang, I.L.; Chong, F.T.;
Computer Architecture, 2006. ISCA '06. 33rd International Symposium on
Digital Object Identifier: 10.1109/ISCA.2006.32
Publication Year: 2006 , Page(s): 378 - 390

IEEE CONFERENCES

High performance, high throughput turbo/ SOVA decoder design

Zhongfeng Wang; Parhi, K K.;
Communications, IEEE Transactions on
Volume: 51 , Issue: 4
Digital Object Identifier: 10.1109/TCOMM.2003.810832
Publication Year: 2003 , Page(s): 570 - 579

IEEE JOURNALS

ReCPU: A parallel and pipelined architecture for regular expression matching

Paolieri, Marco; Bonesana, Ivano; Santambrogio, Marco D.;
Very Large Scale Integration, 2007. VLSI - SoC 2007. IFIP International Conference on
Digital Object Identifier: 10.1109/VLSISOC.2007.4402466
Publication Year: 2007 , Page(s): 19 - 24

IEEE CONFERENCES

Multiple templates access of trees in parallel memory systems

Auletta, V.; De Vivo, A.; Scarano, V.;
Parallel Processing Symposium, 1997. Proceedings., 11th International
Digital Object Identifier: 10.1109/IPPS.1997.580980
Publication Year: 1997 , Page(s): 694 - 701

IEEE CONFERENCES

Development of a Hard Microcontroller

Measel, P. R.; Sivo, L. L.; Quilitz, W. E.; Davidson, T. K.;
Nuclear Science, IEEE Transactions on
Volume: 23 , Issue: 6
Digital Object Identifier: 10.1109/TNS.1976.4328571
Publication Year: 1976 , Page(s): 1738 - 1742

IEEE JOURNALS

Studying Asynchronous Shared Memory Computations

Juvaste, S.;
Parallel Architecture and Compilation Techniques, 2007. PACT 2007. 16th International Conference on
Digital Object Identifier: 10.1109/PACT.2007.4336241
Publication Year: 2007 , Page(s): 413 - 413

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CommScope, Inc.
IPR2023-00064, Ex. 1035
Page 86 of 531

Substitute for form 1449A/PTO				Complete if Known	
INFORMATION DISCLOSURE STATEMENT BY APPLICANT				Application Number	11/246,163
				Filing Date	October 11, 2005
				First Named Inventor	LUND, MICHAEL
				Art Unit	2447
				Examiner Name	Mark C. Pfizenmayer
Sheet	1	of	1	Attorney Docket Number	5550-54

U.S. PATENT DOCUMENTS					
Examiner Initials*	Cite No.[1]	Document Number Number-kind Code [2] *(if known)*	Publication Date MM-DD-YYYY	Name of Patentee of Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear

FOREIGN PATENT DOCUMENTS						
Examiner Initials*	Cite No.[1]	Foreign Patent Document Country Code[3]; Number[4]; Kind Code[5] *(if known)*	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear	T[6]

OTHER ART (Including Author, Title, Date, Pertinent Pages, etc.)		
Examiner Initials*	Cite No.[1]	
	1	Notification of the First Office Action (including translation) for Chinese Patent Application No. 200580032703, mailed September 25, 2009 (Attorney's Ref. No. 5550-54-PCN)

Examiner Signature	/Mark Pfizenmayer/	Date Considered	07/15/2010

*EXAMINER: Initial if reference is considered, whether or not citation is in conformance and not considered. Include copy of this form with next communication to applicant.

ALL REFERENCES CONSIDERED EXCEPT WHERE LINED THROUGH. /M.P./

Results **1** - **10** of about **71,500**. (**0.24** sec)

[CITATION] On **maximum** contention-free **interleavers** and permutation polynomials over integer rings — arxiv.org [PDF]
OY Takeshita - IEEE Transactions on Information Theory, 2006
Cited by 46 - Related articles - BL Direct - All 12 versions

[PDF] The Cydra 5 stride-insensitive **memory** system — psu.edu [PDF]
BR Rau, MS Schlansker, DWL Yen - Proc Int'l Conf. on Parallel ..., 1989 - Citeseer
... When the request rate approaches the **maximum** bandwidth that the **memory** system is designed for, the randomness of **...** In the Cydra 5, 8-, 16- and 32-way **interleaving** are **available** in addition to the full 64 **...** Also, the presence of four **memory** banks is similar to 4-way **interleaving**. **...**
Cited by 66 - Related articles - All 4 versions

[PDF] A NUMA API for Linux — andikleen.de [PDF]
A Kleen - Novel Inc, 2005 - andikleen.de
... The program can allocate node **memory** somewhere between the free **memory** (which is normally low because Linux uses free **memory** for caches) and the **maximum memory** size. This function gives a hint for how much **memory** is **available** for allocation on each node, but it **...**
Cited by 25 - Related articles - View as HTML - All 6 versions

... determining sizes of 1: 1 and 2: 1 **memory interleaving** in a computer system, configuring to the **maximum** size, and informing the user if **memory** is incorrectly installed
LB Hobson - US Patent 5,809,555, 1998 - Google Patents
... 1 AND 2:1 **MEMORY INTERLEAVING** IN A COMPUTER SYSTEM, CONFIGURING TO THE **MAXIMUM** SIZE, AND **...** result in the loss of some **memory** in a system configured for 2:1 **interleaving**. **...** may not yield optimal perfor- mance if the total amount of **available memory** is thereby **...**
Cited by 6 - Related articles

[PDF] High-performance programmable SISO decoder VLSI implementation for decoding turbo codes — caltech.edu [PDF]
... , T Yokokawa, M Kan, Y Mizutani, ... - GLOBECOM- ..., 2001 - gladstone.systems.caltech.edu
... Some of them have already been **available** on products [6], [7]. However, in order to **...** chip **interleavers**/deinterleavers (**maximum** 16K) • capable of 1–3 symbol-wise **interleave** • arbitrary **interleaver** patterns • adapt **... Maximum memory** lengths of the codes are different for each type. **...**
Cited by 24 - Related articles - View as HTML - BL Direct - All 6 versions

Method for **interleaving** computer disk data input-out transfers with permuted buffer addressing
TJ Parks - US Patent 5,404,454, 1995 - Google Patents
... Data from the disk drives may be simultaneously loaded into two different **memory** buffers utilizing the **maximum available** I/O **...** 5,404,454 METHOD FOR **INTERLEAVING** COMPUTER DISK DATA INPUT-OUT TRANSFERS WITH PERMUTED BUFFER ADDRESSING **...**
Cited by 17 - Related articles

Memory bank customization and assignment in behavioral synthesis — york.ac.uk [PDF]
PR Panda - Proceedings of the 1999 IEEE/ACM international ..., 1999 - portal.acm.org
... Memory packing tech- niques for realizing the required **memory** for an application in terms of **available** components were **...** Note that there is no simple way to **interleave** ai and c 2i . **...** can also be used to solve a vari- ant of the problem stated as: given a **maximum memory** size 478 **...**
Cited by 45 - Related articles - BL Direct - All 6 versions

Dynamic **memory** mapper which supports **interleaving** across 2. sup. N+ 1, 2. sup. N. sup. N-1 number of banks for reducing contention during nonunit stride accesses
JH Mirza, SW White - US Patent 5,247,645, 1993 - Google Patents
... cessor cycle. Multiple ports or pipes in a vector design increase the **interleave** requirements. In **... memory**. This 60 results in reducing the number of BSMs by a factor of two which, in turn, halves the **available memory**. An alternative **...**
Cited by 12 - Related articles

Low-power mapping of behavioral arrays to multiple memories — psu.edu [PDF]
P Panda, N Dutt - Proceedings of the 1996 international symposium ..., 1996 - portal.acm.org
... tion is common in performance-critical systems where the required data access rate exceeds the **maximum** ac- cess **...** 4). In Figure 2, logical array par- titions K1 and K3 are merged into logical **memory** L1. Finally, we map the logical memories into the **available** physical memories **...**
Cited by 18 - Related articles - All 3 versions

[CITATION] A mixed QoS SDRAM controller for FPGA-based high-end image processing — psu.edu [PDF]
DIS Heithecker, DIA do Carmo Lucas
Cited by 25 - Related articles - All 5 versions

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IPR2023-00064, Ex. 1035
Page 88 of 531

Substitute for form 1449A/PTO				Complete if Known	
INFORMATION DISCLOSURE STATEMENT BY APPLICANT				Application Number	11/246,163
				Filing Date	October 11, 2005
				First Named Inventor	LUND, MICHAEL
				Art Unit	2447
				Examiner Name	Mark C. Pfizenmayer
Sheet	1	of	2	Attorney Docket Number	5550-54

U.S. PATENT DOCUMENTS

Examiner Initials*	Cite No.[1]	Document Number Number-kind Code [2] *(if known)*	Publication Date MM-DD-YYYY	Name of Patentee of Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear
	1	2004/0114536	06/17/04	O'Rourke	
	2	2005/0180323	08/18/05	Beightol et al.	
	3	2003/0067877	04/10/03	Sivakumar et al.	
	4	2009/0300450	12/03/09	Tzannes (10-02-2008)	
	5	12/783758		Tzannes (05-20-2010)	
	6	12/760728		Tzannes (04-15-2010)	
	7	12/783765		Tzannes (05-20-2010)	
	8	12/761586		Lund et al. (4/16/2010)	

FOREIGN PATENT DOCUMENTS

Examiner Initials*	Cite No.[1]	Foreign Patent Document Country Code[3]; Number[4]; Kind Code[5] *(if known)*	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear	T[6]
	9	EP 1225735	07/24/02	Matsushita Electronic Ind Co Ltd		
	10	EP 1246409	10/02/02	Mitsubishi Electric Corp		
	11	WO 2006/044227	04/27/06	Aware Inc.		

OTHER ART (Including Author, Title, Date, Pertinent Pages, etc.)

Examiner Initials*	Cite No.[1]	
	12	Shoji, T. et al: "Wireless Access Method to Ensure Each Users QOS in Unpredictable and Various QOS Requirements Wireless Personal Communications," Springer, Dordrecht, NL, Vol. 22, No. 2, Aug. 2002, pp. 139-151
	13	"ITU-T Recommendation G.992.5 - Series G: Transmission Systems and Media, Digital Systems and Networks", International Telecommunication Union, ADSL2, May 2003, 92 pages

Examiner Signature	/Mark Pfizenmayer/	Date Considered	08/30/2010

*EXAMINER: Initial if reference is considered, whether or not citation is in conformance and not considered. Include copy of this form with next communication to applicant.

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Substitute for form 1449A/PTO				Complete if Known	
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				First Named Inventor	LUND, MICHAEL
				Art Unit	2447
				Examiner Name	Mark C. Pfizenmayer
Sheet	2	of	2	Attorney Docket Number	5550-54

	14	"ITU-T Recommendation G.992.3," International Telecommunication Union, ADSL2, Jan. 2005, 436 pages
	15	"VDSL2 ITU-T Recommendation G.993.2," International Telecommunication Union, Feb. 2006, 252 pages

Examiner Signature	/Mark Pfizenmayer/	Date Considered	08/30/2010

*EXAMINER: Initial if reference is considered, whether or not citation is in conformance and not considered. Include copy of this form with next communication to applicant.

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```
File 347:JAPIO Dec 1976-2010/Apr(Updated 100726)
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File 350:Derwent WPIX 1963-2010/UD=201049
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Set     Items   Description
S1      52734   (MAX OR MAXIMUM OR CEILING OR LIMIT OR THRESHOLD OR BOUNDARY OR UPPERMOST
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S2        288   (MOST OR HIGHEST OR GREATEST OR LARGEST)(3W)(AMOUNT OR QUANTITY OR NUMBER
 OR VOLUME OR DENSITY)(3W)(BYTES OR BITS OR SPACE OR ROOM OR CAPACITY OR MEMORY)

S3      10280   S1:S2(10N)(SEND??? OR SENT OR TRANSMIT? OR TRANSMISSION OR TRANSFER? OR
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 LATENCY(1W)(PATH? ? OR PATHWAY? ?)

S5        641   S4(15N)(CONFIGUR? OR ALLOCAT? OR ASSIGN? OR RESERV? OR MODIF? OR
 MANIPULAT? OR ALTER? OR CHANG? OR INCREAS? OR DECREAS? OR LOWER? OR RAIS?)

S6          3   S3 AND S5
S7         12   S3 AND S4
S8          9   S7 NOT S6
S9          3   S8 AND PY=1963:2004
S10         5   S8 AND AY=1963:2004 AND AC=US
S11         6   S9:S10
S12         1   PN=US 20060088054
S13         0   S12 AND S3
S14      7786   (MAX OR MAXIMUM OR CEILING OR LIMIT OR THRESHOLD OR BOUNDARY OR UPPERMOST
 OR TOPMOST)(5N)DEPTH

S15         4   (MOST OR HIGHEST OR GREATEST OR LARGEST)(3W)(AMOUNT OR QUANTITY OR NUMBER
 OR VOLUME OR DENSITY)(3W)DEPTH

S16         5   S14:S15 AND S4
S17         4   S16 NOT S7
S18    723988   TRANSCEIVER? ? OR RECEIVER? ? OR TRANSMITTER? ?
S19       339   S1:S2(7N)S18(7N)(SEND??? OR SENT OR TRANSMIT? ? OR TRANSMITTED OR
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S20        17   (S1:S2 OR S14:S15)(10N)ADVERTIS???
S21         1   S20 AND (S4 OR S18)
S22     68677   (TRANSCEIVER? ? OR RECEIVER(N)TRANSMITTER)(5N)(SEND??? OR SENT OR
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 OR DELIVER? OR CONVEY? OR FORWARD? OR PROVIDE OR PROVIDES OR PROVIDED OR PROVIDING OR
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S23        32   S22(10N)S1:S2
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S24         32   S23 NOT (S7 OR S17)
S25         25   S24 AND PY=1963:2004
S26         20   S24 AND AY=1963:2004 AND AC=US
S27         28   S25:S26
S28         28   IDPAT (sorted in duplicate/non-duplicate order)
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 OR TOPMOST)(5N)(MEMORY OR CAPACITY OR SPACE OR ROOM OR DEPTH)

S2        290   (MOST OR HIGHEST OR GREATEST OR LARGEST)(3W)(AMOUNT OR QUANTITY OR NUMBER
 OR VOLUME OR DENSITY)(3W)(BYTES OR BITS OR SPACE OR ROOM OR CAPACITY OR MEMORY OR DEPTH)

S3      10970   S1:S2(10N)(SEND??? OR SENT OR TRANSMIT? ? OR TRANSMITTED OR TRANSMITTING
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S4      56808   (DATA OR COMMUNICATION OR TRANSMISSION)(1W)(PATH? ? OR PATHWAY? ?) OR
 FCI()BLOCK

S5       9357   S4(15N)(CONFIGUR? OR ALLOCAT? OR ASSIGN? OR RESERV? OR MODIF? OR
 MANIPULAT? OR ALTER? OR CHANG? OR INCREAS? OR DECREAS? OR LOWER? OR RAIS?)

S6         27   S3 AND S5
S7         15   S6 AND PY=1963:2004
S8         15   S6 AND AY=1963:2004 AND AC=US
S9         17   S7:S8
S10        17   IDPAT (sorted in duplicate/non-duplicate order)
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         (c) 2010 European Patent Office
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Set     Items   Description
S1      67716   (MAX OR MAXIMUM OR CEILING OR LIMIT OR THRESHOLD OR BOUNDARY OR UPPERMOST
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S2        894   (MOST OR HIGHEST OR GREATEST OR LARGEST)(3W)(AMOUNT OR QUANTITY OR NUMBER
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S3      11551   S1:S2(10N)(SEND??? OR SENT OR TRANSMIT? ? OR TRANSMITTED OR TRANSMITTING
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S4      64674   INTERLEAVER? ? OR DEINTERLEAVER? ? OR INTER()LEAVER? ? OR (LATENCY OR
 DATA OR COMMUNICATION OR TRANSMISSION)(1W)(PATH? ? OR PATHWAY? ?) OR FCI()BLOCK

S5      13802   S4(15N)(CONFIGUR? OR ALLOCAT? OR ASSIGN? OR RESERV? OR MODIF? OR
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 RAIS?)

S6         20   S3(100N)S5
S7          9   S6 AND PY=1978:2004
S8          8   S6 AND (AC=US OR AC=US/PR) AND AY=1978:2004
S9         13   S7:S8
S10        13   IDPAT (sorted in duplicate/non-duplicate order)
S11       109   S1:S2(10N)BROADCAST???
S12         0   S11(100N)S5
S13    286670   (TRANSCEIVER? ? OR RECEIVER? ? OR TRANSMITTER? ?)(5N)(SEND??? OR SENT OR
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S14       479   S13(10N)S1:S2
S15     90455   (TRANSCEIVER? ? OR RECEIVER? ?(1N)TRANSMITTER? ?)(5N)(SEND??? OR SENT OR
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 OR DELIVER? OR CONVEY? OR FORWARD? OR PROVIDE OR PROVIDES OR PROVIDED OR PROVIDING OR
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S16        84   S15(10N)S1:S2
S17        83   S16 NOT S6
S18        42   S17 AND PY=1978:2004
S19        33   S17 AND (AC=US OR AC=US/PR) AND AY=1978:2004
S20        47   S18:S19
S21        47   IDPAT (sorted in duplicate/non-duplicate order)
S22       419   (MAXIMUM OR MOST OR HIGHEST OR GREATEST OR LARGEST)(3W)(AMOUNT OR
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S23         53   S22(7N)(SEND??? OR SENT OR TRANSMIT? ? OR TRANSMITTED OR TRANSMITTING OR
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S24         40   S23 AND PY=1978:2004
S25         23   S23 AND (AC=US OR AC=US/PR) AND AY=1978:2004
S26         41   S24:S25
S27         41   IDPAT (sorted in duplicate/non-duplicate order)
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Set     Items   Description
S1        143   (MAXIMUM OR MOST OR HIGHEST OR GREATEST OR LARGEST)(3W)(AMOUNT OR
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S2         11   S1(10N)(SEND??? OR SENT OR TRANSMIT? ? OR TRANSMITTED OR TRANSMITTING OR
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S3         24   S1(30N)(SEND??? OR SENT OR TRANSMIT? ? OR TRANSMITTED OR TRANSMITTING OR
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S4         13   S3 NOT S2
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Set     Items   Description
S1     142746   (MAX OR MAXIMUM OR CEILING OR LIMIT OR THRESHOLD OR BOUNDARY OR UPPERMOST
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S2        302   (MOST OR HIGHEST OR GREATEST OR LARGEST)(3W)(AMOUNT OR QUANTITY OR NUMBER
 OR VOLUME OR DENSITY)(3W)(BYTES OR BITS OR SPACE OR ROOM OR CAPACITY OR MEMORY OR RAM OR
 DEPTH)

S3       9025   S1:S2(10N)(SEND??? OR SENT OR TRANSMIT? ? OR TRANSMITTED OR TRANSMITTING
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S4      92870   INTERLEAVER? ? OR DEINTERLEAVER? ? OR INTER()LEAVER? ? OR (LATENCY OR
 DATA OR COMMUNICATION OR TRANSMISSION)(1W)(PATH? ? OR PATHWAY? ?) OR FCI()BLOCK

S5       4839   S4(15N)(CONFIGUR? OR ALLOCAT? OR ASSIGN? OR RESERV? OR MODIF? OR
 MANIPULAT? OR ALTER??? OR ALTERATION? ? OR CHANG? OR INCREAS? OR DECREAS? OR LOWER? OR
 RAIS?)

S6         12   S3 AND S5
S7          9   RD  (unique items)
S8        127   S3 AND S4
```

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S9       6596   S1:S2(10N)(SEND??? OR SENT OR TRANSMIT? ? OR TRANSMITTED OR TRANSMITTING
 OR TRANSMISSION OR TRANSFER? OR COMMUNICAT? OR DELIVER? OR CONVEY? OR FORWARD? OR RELAY?
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S10       118   S9 AND S4
S11       107   RD  (unique items)
S12        51   S11 NOT PY=2005:2010
S13        49   S12 NOT S7
S14     67877   (TRANSCEIVER? ? OR RECEIVER? ?(1N)TRANSMITTER? ?)(5N)(SEND??? OR SENT OR
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S15        31   S14(7N)S1:S2
S16        30   RD  (unique items)
S17        19   S16 NOT (S13 OR S7 OR PY=2005:2010)
S18        56   (MAXIMUM OR MOST OR HIGHEST OR GREATEST OR LARGEST)(3W)(AMOUNT OR
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S19         4   S18(30N)(SEND??? OR SENT OR TRANSMIT? ? OR TRANSMITTED OR TRANSMITTING OR
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S20         4   RD  (unique items)
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1 InfiniteReality: a real-time graphics system
John S. Montrym, Daniel R. Baum, David L. Dignam, Christopher J. Migdal
August 1997 **SIGGRAPH '97:** Proceedings of the 24th annual conference on Computer graphics and interactive techniques
Publisher: ACM Press/Addison-Wesley Publishing Co. Request Permissions
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2 An uplink CDMA system architecture with diverse QoS guarantees for heterogeneous traffic
Sunghyun Choi, Kang G. Shin
October 1999 **IEEE/ ACM Transactions on Networking (TON)** , Volume 7 Issue 5
Publisher: IEEE Press
Full text available: Pdf (408.20 KB) Additional Information: full citation, references, cited by, index terms
Bibliometrics: Downloads (6 Weeks): 2, Downloads (12 Months): 40, Downloads (Overall): 501, Citation Count: 12

Keywords: CDMA systems, QoS guarantees, admission control, automatic retransmission reQuest, multicode CDMA, power control, reed-Solomon/convolutional concatenated code, transmission-rate request access protocol, wireless/mobile communication

3 Hierarchical coarse-grained stream compilation for software defined radio
Yuan Lin, Manjunath Kudlur, Scott Mahlke, Trevor Mudge
September 2007 **CASES '07:** Proceedings of the 2007 international conference on Compilers, architecture, and synthesis for embedded systems
Publisher: ACM
Full text available: Pdf (464.76 KB) Additional Information: full citation, abstract, references, index terms
Bibliometrics: Downloads (6 Weeks): 11, Downloads (12 Months): 56, Downloads (Overall): 225, Citation Count: 1

Software Defined Radio (SDR) is an emerging embedded domain where the physical layer of wireless protocols is implemented in software rather than the traditional application specific hardware. The operation throughput requirements of current third-generation ...

Keywords: MPSoC compilation, dataflow programming model, modulo scheduling, software defined radio

4 COTSon: infrastructure for full system simulation
Eduardo Argollo, Ayose Falcón, Paolo Faraboschi, Matteo Monchiero, Daniel Ortega
January 2009 **SIGOPS Operating Systems Review** , Volume 43 Issue 1
Publisher: ACM
Full text available: Pdf (836.87 KB) Additional Information: full citation, abstract, references, index terms
Bibliometrics: Downloads (6 Weeks): 40, Downloads (12 Months): 277, Downloads (Overall): 362, Citation Count: 3

Simulation has historically been the primary technique used for evaluating the performance of new proposals in computer architecture. Speed and complexity considerations have traditionally limited its applicability to single-thread processors running ...

Keywords: full system simulation

5 Adaptive rate controlled, robust video communication over packet wireless networks
G. R. Rajugopal, R. H. M. Hafez
June 1998 **Mobile Networks and Applications** , Volume 3 Issue 1
Publisher: Kluwer Academic Publishers
Full text available: Pdf (977.91 KB) Additional Information: full citation, abstract, references, cited by, index terms, review
Bibliometrics: Downloads (6 Weeks): 0, Downloads (12 Months): 26, Downloads (Overall): 497, Citation Count: 2

Video transmission over wireless packet networks is gaining importance due to the concept of universal personal communication. Further, it is considered an important step towards wireless multimedia. The challenge however is to achieve good video quality ...

6

CommScope, Inc.
IPR2023-00064, Ex. 1035
Page 99 of 531

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SERIAL NUMBER	FILING or 371(c) DATE	CLASS	GROUP ART UNIT	ATTORNEY DOCKET NO.
11/246,163	10/11/2005 RULE	~~711~~ 714	2447	5550-54

APPLICANTS
Marcos C. Tzannes, Orinda, CA;
Michael Lund, West Newton, MA;

**** CONTINUING DATA ***************************
This appln claims benefit of 60/618,269 10/12/2004

**** FOREIGN APPLICATIONS **************************

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11/07/2005

Foreign Priority claimed ❑ Yes ☑ No 35 USC 119(a-d) conditions met ❑ Yes ☑ No Verified and Acknowledged /Mark Pfizenmayer/ Examiner's Signature	❑ Met after Allowance Initials	STATE OR COUNTRY	SHEETS DRAWINGS	TOTAL CLAIMS	INDEPENDENT CLAIMS
		CA	3	45	5

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UNITED STATES

TITLE
Resource sharing in a telecommunications environment

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BIB (Rev. 05/07).

EAST Search History

EAST Search History (Prior Art)

Ref #	Hits	Search Query	DBs	Default Operator	Plurals	Time Stamp
S283	769	379/93.01.ccls.	US-PGPUB; USPAT; USOCR; EPO; JPO; IBM_TDB	OR	ON	2010/07/27 18:45
S284	3633	375/222.ccls.	US-PGPUB; USPAT; USOCR; EPO; JPO; IBM_TDB	OR	ON	2010/07/27 18:46
S285	1149	714/774,784.ccls.	US-PGPUB; USPAT; USOCR; EPO; JPO; IBM_TDB	OR	ON	2010/07/27 18:46
S286	161201	"370"/$.ccls.	US-PGPUB; USPAT; USOCR; EPO; JPO; IBM_TDB	OR	ON	2010/07/27 18:46
S287	17	reed same shar$5 near2 (memory buffer) same interleav$3	US-PGPUB; USPAT; USOCR; EPO; JPO; IBM_TDB	OR	ON	2010/07/27 18:47
S288	187639	(max maximum limit$5 cap$4) same (available free total remain$4) same (memory buffer byte)	US-PGPUB; USPAT; USOCR; EPO; JPO; IBM_TDB	OR	ON	2010/07/27 18:48
S289	336	S288 and interleav$3 and reed and shar$5 near2 (memory buffer)	US-PGPUB; USPAT; USOCR; EPO; JPO; IBM_TDB	OR	ON	2010/07/27 18:49
S290	2	S289 and S284	US-PGPUB; USPAT; USOCR; EPO; JPO; IBM_TDB	OR	ON	2010/07/27 18:49
S291	2252	(max maximum limit$5 cap$4) same (available free total remain$4) same (memory buffer byte) same (configur $6 set$1up) same parameter	US-PGPUB; USPAT; USOCR; EPO; JPO; IBM_TDB	OR	ON	2010/07/27 18:53
S292	7	S291 and S284	US-PGPUB; USPAT; USOCR; EPO; JPO; IBM_TDB	OR	ON	2010/07/27 18:54

S293	2	S291 and S285	US-PGPUB; USPAT; USOCR; EPO; JPO; IBM_TDB	OR	ON	2010/07/27 18:58
S294	2688	(max maximum limit$5 cap$4) same (available free total remain$4) same (memory buffer byte) same (configur $6 set$1up initializ$6) same parameter	US-PGPUB; USPAT; USOCR; EPO; JPO; IBM_TDB	OR	ON	2010/07/27 19:03
S295	0	S291 and S284 not S292	US-PGPUB; USPAT; USOCR; EPO; JPO; IBM_TDB	OR	ON	2010/07/27 19:03
S296	1	S294 and S284 not S292	US-PGPUB; USPAT; USOCR; EPO; JPO; IBM_TDB	OR	ON	2010/07/27 19:03
S297	769	379/93.01.ccls.	US-PGPUB; USPAT; USOCR; EPO; JPO; IBM_TDB	OR	ON	2010/07/28 11:44
S298	3633	375/222.ccls.	US-PGPUB; USPAT; USOCR; EPO; JPO; IBM_TDB	OR	ON	2010/07/28 11:44
S299	1149	714/774,784.ccls.	US-PGPUB; USPAT; USOCR; EPO; JPO; IBM_TDB	OR	ON	2010/07/28 11:44
S300	161201	"370"/$.ccls.	US-PGPUB; USPAT; USOCR; EPO; JPO; IBM_TDB	OR	ON	2010/07/28 11:44
S301	5	reed same shar$5 same memory same dsl	US-PGPUB; USPAT; USOCR; EPO; JPO; IBM_TDB	OR	ON	2010/07/28 11:44
S302	24800	dsl same modem	US-PGPUB; USPAT; USOCR; EPO; JPO; IBM_TDB	OR	ON	2010/07/28 11:44
S303	54	S302 and reed and shar$5 adj2 memory	US-PGPUB; USPAT; USOCR; EPO; JPO; IBM_TDB	OR	ON	2010/07/28 11:45

S304	50	S302 and reed and shar$5 adj2 memory and interleav$3	US-PGPUB; USPAT; USOCR; EPO; JPO; IBM_TDB	OR	ON	2010/07/28 11:45
S305	7	S304 and S298	US-PGPUB; USPAT; USOCR; EPO; JPO; IBM_TDB	OR	ON	2010/07/28 11:46
S306	476625	(configur$6 set$1up set adj up intializ $6 allocat$3) same (parameter setting shar$5 adj2 memory)	US-PGPUB; USPAT; USOCR; EPO; JPO; IBM_TDB	OR	ON	2010/07/28 12:12
S307	733	S306 and S298	US-PGPUB; USPAT; USOCR; EPO; JPO; IBM_TDB	OR	ON	2010/07/28 12:12
S308	49	S306 and S303	US-PGPUB; USPAT; USOCR; EPO; JPO; IBM_TDB	OR	ON	2010/07/28 12:12
S309	1286	(configur$6 set$1up set adj up intializ $6 allocat$3) same (parameter setting) same shar$5 adj2 memory	US-PGPUB; USPAT; USOCR; EPO; JPO; IBM_TDB	OR	ON	2010/07/28 12:12
S310	12	S309 and S303	US-PGPUB; USPAT; USOCR; EPO; JPO; IBM_TDB	OR	ON	2010/07/28 12:13
S311	4	S309 and S298	US-PGPUB; USPAT; USOCR; EPO; JPO; IBM_TDB	OR	ON	2010/07/28 12:13
S312	477599	(exchang$3 transmit$4 send$3 trad $3) same (parameter setting)	US-PGPUB; USPAT; USOCR; EPO; JPO; IBM_TDB	OR	ON	2010/07/28 12:15
S313	764	S309 and S312	US-PGPUB; USPAT; USOCR; EPO; JPO; IBM_TDB	OR	ON	2010/07/28 12:15
S314	502	interleav$3 and reed and shar$5 adj2 (memory buffer)	US-PGPUB; USPAT; USOCR; EPO; JPO; IBM_TDB	OR	ON	2010/07/28 12:16

S315	15	S313 and S314	US-PGPUB; USPAT; USOCR; EPO; JPO; IBM_TDB	OR	ON	2010/07/28 12:16
S316	18572	(exchang$3 transmit$4 send$3 trad$3 configur$6 set$1up set adj up intializ $6 allocat$3) same (parameter setting) same (available free remain $3 max maximum total) near6 (memory space buffer byte size)	US-PGPUB; USPAT; USOCR; EPO; JPO; IBM_TDB	OR	ON	2010/07/28 12:19
S317	60	S316 and S298	US-PGPUB; USPAT; USOCR; EPO; JPO; IBM_TDB	OR	ON	2010/07/28 12:19
S318	5	S317 and S314	US-PGPUB; USPAT; USOCR; EPO; JPO; IBM_TDB	OR	ON	2010/07/28 12:19
S319	55	S317 not S318	US-PGPUB; USPAT; USOCR; EPO; JPO; IBM_TDB	OR	ON	2010/07/28 12:23
S320	2862	S316 and S300	US-PGPUB; USPAT; USOCR; EPO; JPO; IBM_TDB	OR	ON	2010/07/28 12:33
S321	15	S320 and S314	US-PGPUB; USPAT; USOCR; EPO; JPO; IBM_TDB	OR	ON	2010/07/28 12:33
S322	769	379/93.01.ccls.	US-PGPUB; USPAT; USOCR; EPO; JPO; IBM_TDB	OR	ON	2010/07/28 13:44
S323	3633	375/222.ccls.	US-PGPUB; USPAT; USOCR; EPO; JPO; IBM_TDB	OR	ON	2010/07/28 13:44
S324	1149	714/774,784.ccls.	US-PGPUB; USPAT; USOCR; EPO; JPO; IBM_TDB	OR	ON	2010/07/28 13:44
S325	161201	"370"/$.ccls.	US-PGPUB; USPAT; USOCR; EPO; JPO; IBM_TDB	OR	ON	2010/07/28 13:44

S326	18572	(exchang$3 transmit$4 send$3 trad$3 configur$6 set$1up set adj up intializ $6 allocat$3) same (parameter setting) same (available free remain $3 max maximum total) near6 (memory space buffer byte size)	US-PGPUB; USPAT; USOCR; EPO; JPO; IBM_TDB	OR	ON	2010/07/28 13:44
S327	502	interleav$3 and reed and shar$5 adj2 (memory buffer)	US-PGPUB; USPAT; USOCR; EPO; JPO; IBM_TDB	OR	ON	2010/07/28 13:45
S328	149	S326 and S327	US-PGPUB; USPAT; USOCR; EPO; JPO; IBM_TDB	OR	ON	2010/07/28 13:45
S329	0	S328 and S322	US-PGPUB; USPAT; USOCR; EPO; JPO; IBM_TDB	OR	ON	2010/07/28 13:45
S330	5	S328 and S323	US-PGPUB; USPAT; USOCR; EPO; JPO; IBM_TDB	OR	ON	2010/07/28 13:45
S331	1	S328 and S324	US-PGPUB; USPAT; USOCR; EPO; JPO; IBM_TDB	OR	ON	2010/07/28 13:46
S332	15	S328 and S325	US-PGPUB; USPAT; USOCR; EPO; JPO; IBM_TDB	OR	ON	2010/07/28 13:47
S333	3870	(exchang$3 transmit$4 send$3 trad $3) same (parameter setting) and (max maximum) same (available free remain$3) same (memory space buffer byte size) and (modem $2dsl)	US-PGPUB; USPAT; USOCR; EPO; JPO; IBM_TDB	OR	ON	2010/07/28 13:51
S334	26	S333 and S327	US-PGPUB; USPAT; USOCR; EPO; JPO; IBM_TDB	OR	ON	2010/07/28 13:52
S335	1	"5136371".pn.	US-PGPUB; USPAT; USOCR; EPO; JPO; IBM_TDB	OR	ON	2010/07/28 13:55
S336	47	S333 and S323	US-PGPUB; USPAT; USOCR; EPO; JPO; IBM_TDB	OR	ON	2010/07/28 14:25

S337	240731	(exchang$3 transmit$4 send$3 trad $3) same (parameter setting) and (max maximum) naer6 (available free remain$3) near6 (memory space buffer byte size) and (modem $2dsl)	US-PGPUB; USPAT; USOCR; EPO; JPO; IBM_TDB	OR	ON	2010/07/28 14:27
S338	387	(exchang$3 transmit$4 send$3 trad $3) same (parameter setting) and (max maximum) near6 (available free remain$3) near6 (memory space buffer byte size) and (modem $2dsl)	US-PGPUB; USPAT; USOCR; EPO; JPO; IBM_TDB	OR	ON	2010/07/28 14:27
S339	5	S338 and S323	US-PGPUB; USPAT; USOCR; EPO; JPO; IBM_TDB	OR	ON	2010/07/28 14:27
S340	0	S338 and S322	US-PGPUB; USPAT; USOCR; EPO; JPO; IBM_TDB	OR	ON	2010/07/28 14:28
S341	0	S338 and S324	US-PGPUB; USPAT; USOCR; EPO; JPO; IBM_TDB	OR	ON	2010/07/28 14:28
S342	86	S338 and S325	US-PGPUB; USPAT; USOCR; EPO; JPO; IBM_TDB	OR	ON	2010/07/28 14:28
S343	28	S342 and (interleav$3 reed shar$5 adj2 memory)	US-PGPUB; USPAT; USOCR; EPO; JPO; IBM_TDB	OR	ON	2010/07/28 14:29
S344	352	(exchang$3 transmit$4 send$3 trad $3) same (device receiver transceiver modem) near4 (parameter setting) same (available free remain$3) near6 (memory space buffer byte size)	US-PGPUB; USPAT; USOCR; EPO; JPO; IBM_TDB	OR	ON	2010/07/28 14:50
S345	0	S344 and S327	US-PGPUB; USPAT; USOCR; EPO; JPO; IBM_TDB	OR	ON	2010/07/28 14:50
S346	3	S344 and S323	US-PGPUB; USPAT; USOCR; EPO; JPO; IBM_TDB	OR	ON	2010/07/28 14:51
S347	214	(limit$3 cap$4 restrict$3) near8 (interleaver $3coder de$1coder (data latency) adj path) near8 (max maximum available free) near6 (space memory buffer byte)	US-PGPUB; USPAT; USOCR; EPO; JPO; IBM_TDB	OR	ON	2010/07/28 14:53

S348	12	S347 and S327	US-PGPUB; USPAT; USOCR; EPO; JPO; IBM_TDB	OR	ON	2010/07/28 14:53
S349	0	S347 and S323	US-PGPUB; USPAT; USOCR; EPO; JPO; IBM_TDB	OR	ON	2010/07/28 14:54
S350	1	S347 and S324	US-PGPUB; USPAT; USOCR; EPO; JPO; IBM_TDB	OR	ON	2010/07/28 14:54
S351	8	S347 and S325	US-PGPUB; USPAT; USOCR; EPO; JPO; IBM_TDB	OR	ON	2010/07/28 14:54
S352	3	(limit$3 cap$4 restrict$3) near8 (interleaver $3coder de$1coder (data latency) adj path) near8 (max maximum available free) near6 (space memory buffer byte) and $2dsl	US-PGPUB; USPAT; USOCR; EPO; JPO; IBM_TDB	OR	ON	2010/07/28 14:55
S353	13	(configur$6 set$1up set adj up intializ $6) same interleav$3 near2 depth same (max maximum available free) near6 (space memory buffer byte)	US-PGPUB; USPAT; USOCR; EPO; JPO; IBM_TDB	OR	ON	2010/07/28 14:58
S354	7946	711/147,153,157,170,173.ccls.	US-PGPUB; USPAT; USOCR; EPO; JPO; IBM_TDB	OR	ON	2010/07/28 15:02
S355	1590	711/173.ccls.	US-PGPUB; USPAT; USOCR; EPO; JPO; IBM_TDB	OR	ON	2010/07/28 15:02
S356	5	S354 and S323	US-PGPUB; USPAT; USOCR; EPO; JPO; IBM_TDB	OR	ON	2010/07/28 15:35
S357	7	S354 and S327	US-PGPUB; USPAT; USOCR; EPO; JPO; IBM_TDB	OR	ON	2010/07/28 15:41
S358	937	S354 and "55"	US-PGPUB; USPAT; USOCR; EPO; JPO; IBM_TDB	OR	ON	2010/07/28 15:42

S359	501	S354 and S326	US-PGPUB; USPAT; USOCR; EPO; JPO; IBM_TDB	OR	ON	2010/07/28 15:42
S360	86	S355 and S326	US-PGPUB; USPAT; USOCR; EPO; JPO; IBM_TDB	OR	ON	2010/07/28 15:42
S361	3	S354 and S328	US-PGPUB; USPAT; USOCR; EPO; JPO; IBM_TDB	OR	ON	2010/07/28 15:45
S362	2	S354 and S347	US-PGPUB; USPAT; USOCR; EPO; JPO; IBM_TDB	OR	ON	2010/07/28 15:52
S363	4	S354 and S344	US-PGPUB; USPAT; USOCR; EPO; JPO; IBM_TDB	OR	ON	2010/07/28 15:55
S364	1178	S354 and S337	US-PGPUB; USPAT; USOCR; EPO; JPO; IBM_TDB	OR	ON	2010/07/28 15:56
S365	5	S354 and S338	US-PGPUB; USPAT; USOCR; EPO; JPO; IBM_TDB	OR	ON	2010/07/28 15:56
S366	224	S355 and S337	US-PGPUB; USPAT; USOCR; EPO; JPO; IBM_TDB	OR	ON	2010/07/28 15:57
S367	32	S354 and S333	US-PGPUB; USPAT; USOCR; EPO; JPO; IBM_TDB	OR	ON	2010/07/28 15:58
S368	5	S354 and S324	US-PGPUB; USPAT; USOCR; EPO; JPO; IBM_TDB	OR	ON	2010/07/28 16:17
S369	1	"20050246508".pn.	US-PGPUB; USPAT; USOCR; EPO; JPO; IBM_TDB	OR	ON	2010/07/28 16:18

S370	612	711/157.ccls.	US-PGPUB; USPAT; USOCR; EPO; JPO; IBM_TDB	OR	ON	2010/07/28 16:34
S371	5	S370 and S327	US-PGPUB; USPAT; USOCR; EPO; JPO; IBM_TDB	OR	ON	2010/07/28 16:35
S372	73	S370 and S337	US-PGPUB; USPAT; USOCR; EPO; JPO; IBM_TDB	OR	ON	2010/07/28 16:35
S373	2	S370 and S347	US-PGPUB; USPAT; USOCR; EPO; JPO; IBM_TDB	OR	ON	2010/07/28 16:36
S374	9	("5293607" | "5652861" | "5809555" | "6070227").PN. OR ("6233662").URPN.	US-PGPUB; USPAT; USOCR	OR	ON	2010/07/28 16:36
S375	12	("20020126673" | "20030021338" | "20030084212" | "20030147410" | "4432051" | "5109522" | "5873127" | "5950211" | "6286092" | "6681239" | "6687767").PN. OR ("7110373").URPN.	US-PGPUB; USPAT; USOCR	OR	ON	2010/07/28 16:55
S376	98	(limit$3 cap$4 restrict$3) near6 (interleaver) near6 (space memory buffer size)	US-PGPUB; USPAT; USOCR; EPO; JPO; IBM_TDB	OR	ON	2010/07/28 17:30
S377	13	S376 and S370	US-PGPUB; USPAT; USOCR; EPO; JPO; IBM_TDB	OR	ON	2010/07/28 17:30
S378	1	S376 and S323	US-PGPUB; USPAT; USOCR; EPO; JPO; IBM_TDB	OR	ON	2010/07/28 17:30
S379	17	("20010050943" | "20040044942" | "20050138524" | "20050220202" | "20060062287" | "20060153285" | "20080052609" | "20080065969" | "20080219290" | "20080232444" | "20080298444" | "4695673" | "6067646" | "6218579" | "6742155" | "6885696" | "6971057").PN.	US-PGPUB; USPAT; USOCR; EPO; JPO; IBM_TDB	OR	ON	2010/07/28 17:35
S380	19	exceed$3 same (maximum max) same (interleaver) same (space memory buffer size byte allocation)	US-PGPUB; USPAT; USOCR; EPO; JPO; IBM_TDB	OR	ON	2010/07/28 17:38

S381	1	S380 and S324	US-PGPUB; USPAT; USOCR; EPO; JPO; IBM_TDB	OR	ON	2010/07/28 17:38
S382	0	S380 and S323	US-PGPUB; USPAT; USOCR; EPO; JPO; IBM_TDB	OR	ON	2010/07/28 17:38
S383	1461	(initializ$6 configur$6 set$1up set adj up allocat$6) same (block path interleaver) same limited near2 (resource memory)	US-PGPUB; USPAT; USOCR; EPO; JPO; IBM_TDB	OR	ON	2010/07/29 14:25
S384	503	interleav$3 and reed and shar$5 adj2 (memory buffer)	US-PGPUB; USPAT; USOCR; EPO; JPO; IBM_TDB	OR	ON	2010/07/29 14:26
S385	4	S383 and S384	US-PGPUB; USPAT; USOCR; EPO; JPO; IBM_TDB	OR	ON	2010/07/29 14:26
S386	3634	375/222.ccls.	US-PGPUB; USPAT; USOCR; EPO; JPO; IBM_TDB	OR	ON	2010/07/29 14:26
S387	10	S383 and S386	US-PGPUB; USPAT; USOCR; EPO; JPO; IBM_TDB	OR	ON	2010/07/29 14:26
S388	612	711/157.ccls.	US-PGPUB; USPAT; USOCR; EPO; JPO; IBM_TDB	OR	ON	2010/07/29 14:29
S389	0	S383 and S388	US-PGPUB; USPAT; USOCR; EPO; JPO; IBM_TDB	OR	ON	2010/07/29 14:29
S390	1150	714/774,784.ccls.	US-PGPUB; USPAT; USOCR; EPO; JPO; IBM_TDB	OR	ON	2010/07/29 14:30
S391	1	S383 and S390	US-PGPUB; USPAT; USOCR; EPO; JPO; IBM_TDB	OR	ON	2010/07/29 14:30

S392	161385	"370"/$.ccls.	US-PGPUB; USPAT; USOCR; EPO; JPO; IBM_TDB	OR	ON	2010/07/29 14:30
S393	152	S383 and S392	US-PGPUB; USPAT; USOCR; EPO; JPO; IBM_TDB	OR	ON	2010/07/29 14:30
S394	5	S393 and interleaver	US-PGPUB; USPAT; USOCR; EPO; JPO; IBM_TDB	OR	ON	2010/07/29 14:30
S395	200	S383 and (multiple plurality) near4 (application (data latency) adj path)	US-PGPUB; USPAT; USOCR; EPO; JPO; IBM_TDB	OR	ON	2010/07/29 14:31
S396	15	S395 and $dsl	US-PGPUB; USPAT; USOCR; EPO; JPO; IBM_TDB	OR	ON	2010/07/29 14:31
S397	40	S395 and modem	US-PGPUB; USPAT; USOCR; EPO; JPO; IBM_TDB	OR	ON	2010/07/29 14:32
S398	29	S397 not S396	US-PGPUB; USPAT; USOCR; EPO; JPO; IBM_TDB	OR	ON	2010/07/29 14:32
S399	14	("20020059425" | "5297262" | "5553287" | "5875479" | "6016495" | "6631478" | "6671699").PN. OR ("7139894").URPN.	US-PGPUB; USPAT; USOCR	OR	ON	2010/07/29 14:36
S400	36	(resource memory) near6 (conflict contention) same interleaver	US-PGPUB; USPAT; USOCR; EPO; JPO; IBM_TDB	OR	ON	2010/07/29 14:45
S401	0	S400 and S384	US-PGPUB; USPAT; USOCR; EPO; JPO; IBM_TDB	OR	ON	2010/07/29 14:45
S402	0	S400 and S386	US-PGPUB; USPAT; USOCR; EPO; JPO; IBM_TDB	OR	ON	2010/07/29 14:45

S403	1	S400 and shar$5 adj2 (memory buffer)	US-PGPUB; USPAT; USOCR; EPO; JPO; IBM_TDB	OR	ON	2010/07/29 14:46
S404	65	(requir$2 needed) near8 interleaver same memory same (max maximum available free)	US-PGPUB; USPAT; USOCR; EPO; JPO; IBM_TDB	OR	ON	2010/07/29 14:48
S405	235	"65" and S384	US-PGPUB; USPAT; USOCR; EPO; JPO; IBM_TDB	OR	ON	2010/07/29 14:48
S406	3	S404 and S384	US-PGPUB; USPAT; USOCR; EPO; JPO; IBM_TDB	OR	ON	2010/07/29 14:48
S407	1	"20050154954".pn.	US-PGPUB; USPAT; USOCR; EPO; JPO; IBM_TDB	OR	ON	2010/08/03 14:55
S408	188014	(max maximum limit$5 cap$4) same (available free total remain$4) same (memory buffer byte)	US-PGPUB; USPAT; USOCR; EPO; JPO; IBM_TDB	OR	ON	2010/08/03 15:11
S409	92	S408 and 709/215.ccls.	US-PGPUB; USPAT; USOCR; EPO; JPO; IBM_TDB	OR	ON	2010/08/03 15:11

EAST Search History (Interference)

Ref #	Hits	Search Query	DBs	Default Operator	Plurals	Time Stamp
L1	179	(maximum) same (memory bytes) same (interleaver deinterleaver)	USPAT; UPAD	OR	ON	2010/08/03 17:04
L2	13	(maximum) same (memory bytes) same (interleaver deinterleaver). clm.	USPAT; UPAD	OR	ON	2010/08/03 17:04
L3	4	(available free) near6 (memory bytes) same (interleaver deinterleaver).clm.	USPAT; UPAD	OR	ON	2010/08/03 17:05

8/3/2010 5:10:33 PM
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Search Notes	Application/Control No.	Applicant(s)/Patent Under Reexamination
	11246163	TZANNES ET AL.
	Examiner	**Art Unit**
	Mark Pfizenmayer	2447

SEARCHED			
Class	**Subclass**	**Date**	**Examiner**
709	215	July 2010	MCP
375	222	July 2010	MCP
714	774,784	July 2010	MCP
711	147,153,157,170,173	Jluy 2010	MCP
379	93.01	July 2010	MCP

SEARCH NOTES		
Search Notes	**Date**	**Examiner**
See search history printout	July 2010	MCP
709/215; 379/93.01; 375/222; 714/774,784; 711/147,153,157,170,173; and 370 with text	July 2010	MCP
Google/IEEE/ACM search	July 2010	MCP
Consulted with Primary Bill Thomson regarding search, patentability and classification	July 2010	MCP
Consulted with Primaries Chaudry, Bonzo, and Torres regarding search classification	July 2010	MCP
Consulted with Primary Dustin Nguyen regarding search	July 2010	MCP
Inventor Name Search	July 2010	MCP
STIC search	July 2010	MCP

INTERFERENCE SEARCH			
Class	**Subclass**	**Date**	**Examiner**
	USPAT and PGPUB text search -- See search history printout	Aug 2010	MCP

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Issue Classification	Application/Control No.	Applicant(s)/Patent Under Reexamination
	11246163	TZANNES ET AL.
	Examiner	Art Unit
	MARK PFIZENMAYER	2447

ORIGINAL		INTERNATIONAL CLASSIFICATION	
CLASS	SUBCLASS	CLAIMED	NON-CLAIMED
714	774	H 0 3 M 13 / 00 (2006.0)	

CROSS REFERENCE(S)					
CLASS	SUBCLASS (ONE SUBCLASS PER BLOCK)				
714	784				
375	222				

☐ Claims renumbered in the same order as presented by applicant ☐ CPA ☐ T.D. ☐ R.1.47

Final	Original	Final	Original	Final	Original	Final	Original	Final	Original	Final	Original	Final	Original	Final	Original
	1		17		33	4	49								
	2		18		34	5	50								
	3		19		35	6	51								
	4		20		36	7	52								
	5		21		37	8	53								
	6		22		38										
	7		23		39										
	8		24		40										
	9		25		41										
	10		26		42										
	11		27		43										
	12		28		44										
	13		29		45										
	14		30	1	46										
	15		31	2	47										
	16		32	3	48										

/MARK PFIZENMAYER/ Examiner.Art Unit 2447	8/3/10	Total Claims Allowed:	
(Assistant Examiner)	(Date)	8	
/Joon H Hwang/ Supervisory Patent Examiner.Art Unit 2447	08/30/2010	O.G. Print Claim(s)	O.G. Print Figure
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Substitute for form 1449A/PTO				Complete if Known	
INFORMATION DISCLOSURE STATEMENT BY APPLICANT				Application Number	11/246,163
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				Examiner Name	Mark C. Pfizenmayer
Sheet	1	of	2	Attorney Docket Number	5550-54

U.S. PATENT DOCUMENTS					
Examiner Initials*	Cite No.[1]	Document Number Number-kind Code [2] *(if known)*	Publication Date MM-DD-YYYY	Name of Patentee of Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear
	1	2004/0114536	06/17/04	O'Rourke	
	2	2005/0180323	08/18/05	Beightol et al.	
	3	2003/0067877	04/10/03	Sivakumar et al.	
	4	2009/0300450	12/03/09	Tzannes (10-02-2008)	
	5	12/783758		Tzannes (05-20-2010)	
	6	12/760728		Tzannes (04-15-2010)	
	7	12/783765		Tzannes (05-20-2010)	
	8	12/761586		Lund et al. (4/16/2010)	

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Examiner Initials*	Cite No.[1]	Foreign Patent Document Country Code[3]; Number[4]; Kind Code[5] *(if known)*	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear	T[6]
	9	EP 1225735	07/24/02	Matsushita Electronic Ind Co Ltd		
	10	EP 1246409	10/02/02	Mitsubishi Electric Corp		
	11	WO 2006/044227	04/27/06	Aware Inc.		

OTHER ART (Including Author, Title, Date, Pertinent Pages, etc.)		
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	12	Shoji, T. et al: "Wireless Access Method to Ensure Each Users QOS in Unpredictable and Various QOS Requirements Wireless Personal Communications," Springer, Dordrecht, NL, Vol. 22, No. 2, Aug. 2002, pp. 139-151
	13	"ITU-T Recommendation G.992.5 - Series G: Transmission Systems and Media, Digital Systems and Networks", International Telecommunication Union, ADSL2, May 2003, 92 pages

Examiner Signature		Date Considered	

*EXAMINER: Initial if reference is considered, whether or not citation is in conformance and not considered. Include copy of this form with next communication to applicant.

Substitute for form 1449A/PTO				Complete if Known	
INFORMATION DISCLOSURE STATEMENT BY APPLICANT				Application Number	11/246,163
				Filing Date	October 11, 2005
				First Named Inventor	LUND, MICHAEL
				Art Unit	2447
				Examiner Name	Mark C. Pfizenmayer
Sheet	2	of	2	Attorney Docket Number	5550-54

	14	"ITU-T Recommendation G.992.3," International Telecommunication Union, ADSL2, Jan. 2005, 436 pages
	15	"VDSL2 ITU-T Recommendation G.993.2," International Telecommunication Union, Feb. 2006, 252 pages

Examiner Signature		Date Considered	

*EXAMINER: Initial if reference is considered, whether or not citation is in conformance and not considered. Include copy of this form with next communication to applicant.

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(54) DATA COMMUNICATION SYSTEM

(57) A data communication system capable of eliminating the retransmission of useless data that is too late for the playback time at the receiving side, and, accordingly, capable of eliminating the wasteful utilization of transmission band. In the system, round-trip time RTT of a packet between the server (data transmitting apparatus) 100 and the terminal apparatus (data receiving apparatus) 200 is calculated, and only when the sum of the round-trip time RTT and present time is less than the playback time of the packet, retransmission request for lost packet which has high priority is made.

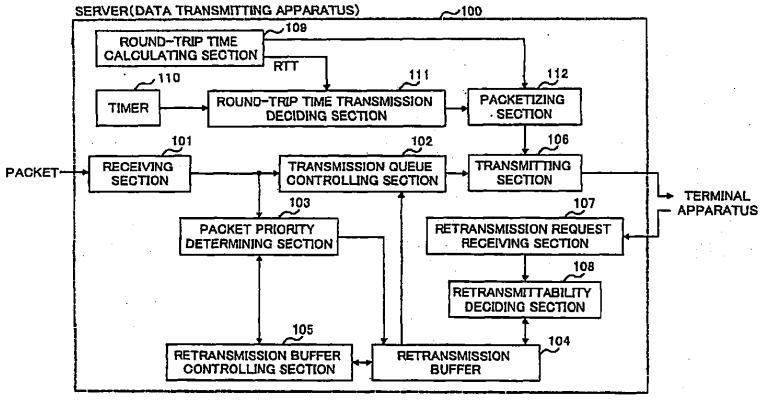

FIG.1

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Description

Technical Field

[0001] The present invention relates to a data communication system, and to a data transmitting apparatus and a data receiving apparatus constituting the data communication system.

Background Art

[0002] Conventionally, when digital data (multimedia data) such as video or audio is transmitted via packet communication channel, as a transport-layer protocol, communication is carried out using TCP (Transmission Control Protocol) protocol which provides high reliability but does not take playback time of video or audio into consideration, or UDP (User Datagram Protocol) protocol which is suitable to real time communication but has a possibility that lost data may occur.

[0003] In a multimedia data communication utilizing TCP, such a processing is required in which data is played back after all of the data have been received by providing a memory for the receiving side. While in the case of utilizing UDP, since important data may be lost during the data playback, the quality of video or audio may be deteriorated.

[0004] Therefore, according to the Japanese Patent No. 2000-151680 A, when a data transmitted utilizing the UDP protocol is lost, a reliable transmission is realized by retransmission of the lost data utilizing the TCP protocol with high reliability.

[0005] The method of data transmission according to the Japanese Patent No. 2000-151680 A is described below. First of all, a receiving side receives a packet from a transmitting side and disassembles the packet, or detects that a packet has failed to be received. Sequence numbers are given to the packets, and these numbers are checked whenever receiving packets, and at a time when discontinuity of sequence numbers is detected, existence of packets which have failed to be received can be detected, or the number of packets which have failed to be received can be counted. Then, by transmitting loss information of the lost data indicating that the packet has failed to be received to the transmitting side, a retransmission request for the packet is made to the transmitting side. The transmitting side retransmits the packet requested to retransmit utilizing the TCP protocol with high reliability. Further, the receiving side is provided with a TCP packet disassembling section and a UDP packet disassembling section, and it is adapted so that any of the TCP packet and the UDP packet is disassembled and transferred to an RTP (Real-time Transfer Protocol) packet disassembling section.

[0006] However, in the conventional art, there is a problem that sometimes wasteful or useless data may be retransmitted during the transmission of a video or audio data, since the transmitting side carries out the retransmission even when it is too late for the playback time, so that a wasteful transmission band is uselessly utilized as equal amount as that for transmission of the wasteful data. Due to the fact that the transmission band is used wastefully, then it becomes difficult to increase the capacity of the entire system since excess electric power for transmitting the wasteful data is required.

Disclosure of the Invention

[0007] It is an object of the present invention to provide a data communication system capable of eliminating the retransmission of useless data that is too late for the playback time at the receiving side, and, accordingly, capable of eliminating the wasteful utilization of transmission band.

[0008] According to an aspect of the present invention, a data communication system comprises a data transmitting apparatus and a data receiving apparatus, wherein the data transmitting apparatus comprises storing means for storing a retransmittable data only, retransmitting means for retransmitting a data that is extracted from the data stored in the storing means corresponding to a retransmission request of the data receiving apparatus, calculating means for calculating a data round-trip time between the data receiving apparatus and the data transmitting apparatus, and transmitting means for transmitting the data round-trip time calculated by the calculating means to the data receiving apparatus at a predetermined time interval, and wherein the data receiving apparatus comprises receiving means for receiving the data transmitted from the data transmitting apparatus, loss detecting means for detecting loss of data when the data is received by the receiving means, playback time calculating means for calculating playback time of the data received by the receiving means, round-trip time receiving means for receiving the data round-trip time transmitted from the transmitting means, and retransmission request deciding means for deciding, when a lost data is detected by the loss detecting means, whether a retransmission request for the lost data is made or not based on the playback time calculated by the playback time calculating means and the data round-trip time received by the round-trip time receiving means.

[0009] According to another aspect of the present invention, a data communication system comprising a data transmitting apparatus and a data receiving apparatus, wherein the data transmitting apparatus comprises storing means for storing a retransmittable data only, retransmitting means for retransmitting a data that is extracted from the data stored in the storing means corresponding to a retransmission request of the data receiving apparatus, measuring means for measuring a differential time between reception time of a first data transmitted from the data receiving apparatus and transmission time of a second data to be transmitted to the data

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receiving apparatus in response to the first data, and transmitting means for transmitting the differential time measured by the measuring means included in the second data to the data receiving apparatus at a predetermined time interval, and wherein the data receiving apparatus comprises calculating means for calculating a data round-trip time between the data transmitting apparatus and the data receiving apparatus by subtracting transmission time of the first data transmitted to the data transmitting apparatus and the differential time included in the second data transmitted from the data transmitting apparatus from reception time of the second data, receiving means for receiving the data transmitted from the data transmitting apparatus, loss detecting means for detecting loss of data when the data is received by the receiving means, playback time calculating means for calculating playback time of the data received by the receiving means, and retransmission request deciding means for deciding, when a lost data is detected by the loss detecting means, whether a retransmission request for the lost data is made or not based on the playback time calculated by the playback time calculating means and the data round-trip time calculated by the calculating means.

Brief Description of the Drawings

[0010]

FIG. 1 is a block diagram showing a constitution of a data transmitting apparatus for a data communication system according to a first embodiment of the invention;
FIG. 2 is a block diagram showing a constitution of a data receiving apparatus for the data communication system according to the first embodiment of the invention;
FIG. 3 is a flowchart illustrating the contents of a round-trip time RTT transmitting processing in a server corresponding to the first embodiment;
FIG. 4 is a block diagram illustrating a constitution of a round-trip time calculating section of the server corresponding to the first embodiment;
FIG. 5 is a sequence diagram illustrating a calculating method of the round-trip time RTT in the server corresponding to the first embodiment;
FIG. 6 is a schematic illustration showing an example of a packet in which the round-trip time RTT is recorded and which is transmitted from the server corresponding to the first embodiment to a terminal apparatus;
FIG. 7 is a schematic illustration showing another example of a packet in which the round-trip time RTT is recorded and which is transmitted from the server corresponding to the first embodiment to the terminal apparatus;
FIG. 8 is a schematic illustration showing an example of a packet in which a differential time DLSR is recorded and which is transmitted from the terminal to the server apparatus corresponding to the first embodiment of the invention;
FIG. 9 is a flowchart illustrating the contents of a differential time DLSR transmitting processing in the terminal apparatus corresponding to the first embodiment;
FIG. 10 is a flowchart illustrating the contents of a packet retransmission request deciding processing in the terminal apparatus corresponding to the first embodiment;
FIG. 11 is an illustration provided for the explanation of FIG. 10 and showing values of various parameters given to the respective packets that are transmitted from the server corresponding to the first embodiment to the terminal apparatus;
FIG. 12 is a block diagram showing another constitution of the server corresponding to the first embodiment;
FIG. 13 is a block diagram showing another constitution of the terminal apparatus corresponding to the first embodiment;
FIG. 14 is a block diagram showing a constitution of a data transmitting apparatus for a data communication system according to a second embodiment of the invention;
FIG. 15 is a block diagram showing a constitution of a data receiving apparatus for the data communication system according to the second embodiment of the invention;
FIG. 16 is a sequence diagram illustrating a calculating method of the round-trip time RTT in a terminal apparatus corresponding to the second embodiment.

Best Mode for Carrying Out the Invention

[0011] Now, referring to the attached figures, embodiments of the invention will be described in detail.

(First Embodiment)

[0012] FIG. 1 is a block diagram showing a constitution of a data transmitting apparatus for a data communication system according to the first embodiment of the invention, FIG. 2 is a block diagram showing a constitution of a data receiving apparatus for the same data communication system.

[0013] A data transmitting apparatus 100 shown in FIG. 1 has a function of transmitting a packet via a packet communication channel, which is not shown in the figures, to a data receiving apparatus 200 shown in FIG. 2 as well as receiving controlling data from the data receiving apparatus 200. For example, the data transmitting apparatus 100 is used in a server for data communication being connected to a packet communication channel as a single unit or being mounted in an exchange station apparatus, or a server mounted in a base

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station apparatus in a mobile communication system.

[0014] Also, the data receiving apparatus 200 is used, for examples, for an information communication terminal apparatus such as a personal computer, etc., that carries out data transmission/receptionvia a cable channel, and for a mobile station apparatus, etc., in a mobile communication system (for instance, a mobile telephone and a mobile type information communication terminal apparatus which has a mobile telephone function and a computer function).

[0015] Further, hereinafter, a description is introduced while taking a server and an information communication terminal apparatus at a client side (hereinafter, simply referred to as "terminal apparatus") as an example for a data transmitting apparatus and a data receiving apparatus, respectively.

[0016] The server 100 comprises, as shown in FIG. 1, a receiving section 101, a transmission queue controlling section 102, a packet priority determining section 103, a retransmission buffer 104, a retransmission buffer controlling section 105, a transmitting section 106, a retransmission request receiving section 107, a retransmitability deciding section 108, a round-trip time calculating section 109, a timer 110, a round-trip time transmission deciding section 111 and a packetizing section 112.

[0017] Moreover, the terminal apparatus 200 includes, as shown in FIG. 2, a receiving section 201, a loss detecting section 202, a priority determining section 203, a playback time calculating section 204, a round-trip time receiving section 205, a retransmission request deciding section 206, a time measuring section 207, a time information transmission deciding section 208, a timer 209 and a time information transmitting section 210.

[0018] Then, an operational description will be made to the data communication system having the aforementioned constitution.

[0019] First, the server 100 receives by means of the receiving section 101 packets from own application function such as video/audio coding or the like and own storage function of video/audio data, and outputs the received packets to both transmission queue controlling section 102 and packet priority determining section 103.

[0020] Then, the received packets are subjected to a determining process concerning the priority thereof, and the packets of which priority is determined as high in the packet priority determining section 103 are stored in the retransmission buffer 104. When storing the packets, the retransmission buffer controlling section 105 identifies the packets individually based on the sequence number (serial number) which are given thereto, and controls what addressed memory locations of the retransmission buffer 104 in which the respective packets are stored. The priority of the packets is given to the respective packets by means of the application function.

[0021] On the other hand, when the server 100 receives a packet retransmission request sent from the terminal apparatus 200 by means of the retransmission request receiving section 107, the server 100 makes a YES/NO decision in the retansmitability section 108 concerning the retransmission of the packet corresponding to the retransmission request which are stored in the retransmission buffer 104. Moreover, responding to the decision result, when it is possible to retransmit the packet which is requested to retransmit, the packet requested to retransmit is read out from the retransmission buffer 104 and outputted to the transmission queue controlling section 102.

[0022] The transmission queue controlling section 102 controls the transmission time of the packet received from the receiving section 101 or from the retransmission buffer 104. The packet controlled by the transmission queue controlling section 102 is transmitted to the terminal apparatus 200 together with the packet from the packetizing section 112 via the transmitting section 106.

[0023] At this time, the server 100 makes a decision, in the round-trip time transmission deciding section 111, whether to transmit the information of the round-trip time RTT (round-trip time of the packet between the server 100 and the terminal apparatus 200) which is calculated in the round-trip time calculating section 109. The contents of the decision process will be described later in detail. Then, when it is decided in the round-trip time transmission deciding section 111 that the round-trip time RTT should be transmitted, the round-trip time RTT which is decided to be transmitted is packetized in the foregoing packetizing section 112 and outputted to the transmitting section 106. The contents of the packetizing process of the round-trip time RTT will be described later in detail.

[0024] Next, referring to the flowchart shown in FIG. 3, a description will be made to the transmitting operation of the round-trip time RTT in the server 100. Further, the transmitting operation of the round-trip time RTT is carried out by the round-trip time calculating section 109, the timer 110, the round-trip time transmission deciding section 111 and the packetizing section 112, which are the essential elements of the invention.

[0025] First of all, in step S1000, the timer 110 is reset and the value of the timer is set to a predetermined initial value (a positive integral number). In the timer 110, when a specific time corresponding to the initial value has passed, the value (value of the timer) becomes "0", and the transmission time of the round-trip time RTT is outputted to the round-trip time transmission deciding section 111 at regular intervals. Precisely, for example, "0" is outputted.

[0026] In step S1100, a decision whether the value of the timer 110 (value of the timer) is "0" is made in the round-trip time transmission deciding section 111. As a result of the decision, when the value of the timer is not "0" (S1100:NO), the relevant decision is continued, i.e., the operation waits, and when the value of the timer is "0" (S1100:YES), the operation proceeds to step S1200.

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[0027] In step S1200, in the round-trip time transmission deciding section 111, a decision whether the round-trip time RTT (round-trip time of the packet between the server 100 and the terminal apparatus 200) has newly calculated in the round-trip time calculating section 109 is made. As a result of the decision, when the value of the round-trip time RTT has not been newly calculated, that is to say, when the value of the round-trip time RTT has not been renewed (updated) (S1200:NO), the relevant decision is continued, i.e., the operation waits, and when the value of the round-trip time RTT has been newly calculated, that is to say, when the round-trip time RTT has been renewed (updated)(S1200:YES), the operation proceeds to step S1300. Further, the contents of the calculation process of the round-trip time RTT in the round-trip time calculating section 109 will be described later in detail.

[0028] In step S1300, a decision that the transmission of the round-trip time RTT is OK, i.e., the round-trip time RTT should be transmitted is made in the round-trip time transmission deciding section 111.

[0029] Next, in step S1400, the renewed (updated) round-trip time RTT is packetized in the packetizing section 112. The contents of the packetizing process will be described later in detail.

[0030] Finally, in step S1500, the packet in which the round-trip time RTT is recorded by packetizing is transmitted to the terminal apparatus 200 via the transmitting section 106, and then the operation returns to step S1000.

[0031] Now, referring to FIG. 4 to FIG. 8, a description will be made to the contents of the round-trip time RTT calculating process which is subjected to the decision in step S1200, and to the contents of the packetizing process in step S1400.

[0032] FIG. 4 is a block diagram illustrating a constitution of the round-trip time calculating section 109 of the server 100 (data transmitting apparatus).

[0033] The round-trip time calculating section 109 comprises, as shown in FIG. 4, a first time measuring section 113, a time information receiving section 114, a second time measuring section 115 and a round-trip time calculating section 116.

[0034] The first time measuring section 113 measures the time (server transmission time) T1 when the sender report packet P1 is transmitted from the transmitting section 106 of the server 100 (refer to FIG. 5). The measured server transmission time T1 is packetized together with the round-trip time RTT in the packetizing section 112. That is to say, in the packet P1 that is obtained as a result of packetizing process, the server transmission time T1 is recorded. FIG. 6 shows an example of the packet P1.

[0035] The packet P1 shown in FIG. 6 includes information of version-padding-RC count, payload type, packet length, sender identifier, NTP timestamp, RTP timestamp, cumulative number of packets sent, cumulative number of octets sent and RTT (packet round-trip time).

[0036] Herein, as an identifier of the payload (information section) type, an identifier indicating a transmitting report packet (PT=200) which is an indication of a time information periodically transmitted from the server 100 rather than an ordinary data is given to the payload type (PT). In the packet length, a packet length measured in 32-bit unit is recorded. In the sender identifier, a sequence of numbers capable of uniquely identifying the sender is recorded. In the NTP timestamp and the RTP timestamp, transmission time of the packet is recorded. In the cumulative number of packets sent, the total number of packets transmitted after the session has begun is recorded. In the cumulative number of octets sent, the total number of octets transmitted after the session has begun is recorded. In the RTT, packet round-trip time calculated in the round-trip time calculating section 109 is recorded.

[0037] Further, the manner of packetizing is not limited to the example shown in FIG. 6. For instance, as shown in FIG. 7, another manner in which an identifier indicating a packet including round-trip time (PT=220) given to the payload type to transmit the round-trip time RTT to the terminal apparatus 200 may be used. In this case, since the packet P1 has only the information of version-padding-RC count, payload type, packet length, sender identifier and RTT packet (round-trip time), the round-trip time can be transmitted to the receiving side as a packet having a fewer amount of information compared to the case shown in FIG. 6. Furthermore, the information may be packetized in another manner and transmitted.

[0038] The time information receiving section 114 receives the receiver report packet P2 transmitted from the terminal apparatus 200 (refer to FIG. 5). In packet P2, the differential time DLSR, which is the time calculated from a point when the terminal apparatus 200 receives the packet P1 to a point when the packet P2 is transmitted, and server transmission time T1 transmitted by the server 100 are recorded. FIG. 8 shows an example of the packet P2.

[0039] The packet P2 shown in FIG. 8 includes the information of version-padding-RC count, payload type, packet length, sender identifier, report receiver identifier, fraction lost, cumulative number of packets lost, highest sequence number received, interarrival jitter, LSR and DLSR.

[0040] Here, as payload type, an identifier indicating the receiver report packet (PT=201) which is an indication of time information and packet loss information or the like transmitted periodically from the terminal apparatus 200 is given. In the packet length, packet length measured in 32-bit unit is recorded. In the sender identifier, a sequence of numbers capable of identifying uniquely the transmitter is recorded, and in the report receiver identifier, a sequence of numbers capable of identifying uniquely the report receiver of the receiver report packet is recorded. In the fraction lost, the ratio

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of lost packets to number of packets to be received after the previous receiver report packet has been transmitted is recorded, and in the cumulative number of packets lost, the total number of the lost packets after the session has begun is recorded.

[0041] Further, in the highest sequence number received, the SN value of the packet which has the maximum SN among the received packets is recorded. In the jitter, fluctuation of the receiving time of the RTP packet is recorded. In the LSR, the time when the most recent sender report was sent is recorded. In FIG. 5, the latest server transmitting time becomes LSR=T1. In the DLSR, the differential time between a point of time when the packet P1 has been received and a point of time when the relevant receiver report packet P2 is transmitted is recorded.

[0042] The second time measuring section 115 measures the time (server receiving time) T2 when the packet P2 is received by the time information receiving section 114 (refer to FIG. 5).

[0043] The round-trip time calculating section 116 obtains the round-trip time RTT by subtracting the differential time DLSR recorded in the packet P2 and the time T1 from the server receiving time T2. That is to say, the round-trip time RTT=T2-DLSR-T1.

[0044] Herein, the foregoing differential time DLSR is transmitted to the server 100 via the time information transmitting section 210 after being calculated in the terminal apparatus 200 by the time measuring section 207, time information transmission deciding section 208 and timer 209.

[0045] Now, referring to the flowchart shown in FIG. 9, a description will be made to the operation in which the differential time DLSR from the reception of packet P1 to the transmission of packet P2 is calculated and transmitted to the server 100 in the terminal apparatus 200.

[0046] First, in step S2000, the time parameter is initialized when starting communication. Specifically, the latest packet (transmission report packet P1) reception time TT1 and the latest packet (receiver report packet P2) transmission time TT2 are, respectively, reset to the initial value (=0).

[0047] Then, in step S2100, the timer 209 is initialized and the value of the timer is set to a predetermined initial value (positive integral number). When a specific time relative to the initial value has passed, the value (value of the timer) becomes "0", and the timer 209 outputs the transmission time of the differential time DLSR to the time information transmission deciding section 208 at regular intervals. For instance, "0" is output.

[0048] Then, in step S2200, the time information transmission deciding section 208 decides whether the value of the timer 209 (value of the timer) is "0". As a result of this decision, when the value of the timer is not "0" (S2200:NO), the relevant decision is continued, i.e., the operation waits, whereas the operation proceeds to step S2300 as the value of the timer is "0" (S2200:YES).

[0049] In step S2300, the time information transmission deciding section 208 decides whether the reception time TT1 of the packet P1 from the server 100 has been newly measured by the time measuring section 207, i.e., whether the packet P1 is newly received from the server 100. As a result of this decision, when the packet P1 has not been newly received from the server 100 (S2300:NO), the relevant decision is continued, i.e., the operation waits, whereas the operation proceeds to step S2400 as the packet P1 has been newly received from the server 100 (S2300:YES). Further, the time measuring section 207 measures the reception time TT1 of the packet P1 whenever the terminal apparatus 200 receives the packet P1 from the server 100, and is set (for example, overwritten) to the measured value.

[0050] In step S2400, the time information transmission deciding section 208 decides that the transmission of the receiver report packet P2 is OK, i.e., the receiver report packet P2 is to be transmitted, and the packet transmission time TT2 is set to the present time (for example, overwritten).

[0051] Then, in the step S2500, by the time measuring section 207, the difference between the packet transmission time TT2 (present time) and the packet reception time TT1 (latest time at which the packet P1 is received) is obtained, and the obtained difference is defined as the differential time DLSR (=TT2-TT1).

[0052] Finally, in step S2600, after the information of the differential time DLSR is transmitted to the server 100 by the time information transmitting section 210, the operation returns to step S2100.

[0053] Now, referring to the flowchart shown in FIG. 10, a description will be made to the operation of the packet retransmission request decision using the round-trip time RTT.

[0054] First of all, in step S3000, the packet P1 from the server 100 is received by the receiving section 201.

[0055] Herein, each packet P1 transmitted to the terminal apparatus 200 from the server 100, as shown in FIG. 11, is given, respectively, a sequence number SN, sequence number of high priority packet SNHP and priority P. That is to say, in the packets that the terminal apparatus 200 receives from the server 100, a packet which has high priority (high priority) (when p=1) and a packet which has low priority (low priority) (when p=0) are included, and when transmitting such packets P1, the server 100 increments the sequence number SN recorded in the header field by 1 whenever the packet P1 is transmitted. Further, particularly, when transmitting a high priority packet (P=1), the sequence number of the high priority packet SNHP (P=1) is also incremented by 1. For example, since the packet of SN=1 has low priority (P=0), SNHP=0, whereas the next packet of SN=2 has high priority (P=1), the SNHP is incremented by 1 resulted in SNHP=1.

[0056] In the next step S3100, the loss detecting section 202 decides whether the sequence number SN of the presently received packet (present SN) is incre-

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mented by 1 with respect to the sequence number SN of the previously received packet (previous SN). Responding to the decision result, when the present SN = previous SN+1(S3100:YES), it is decided that there is no lost packet among the previously received packet, then the operation proceeds to step S3900 and waits for reception. While, when the present SN = previous SN+1 (S3100:NO) is not achieved, it is decided that there is a lost packet among the previously received packet, then the operation proceeds to step S3200, and a decision is made whether to carry out retransmission request of the lost packet.

[0057] In step S3200, the priority determining section 203 determines whether the priority of the received packet is high (P=1). As a result of the determination process, when the priority of the received packet is not high, i.e., when it is low priority (P=0) (S3200:NO), the operation proceeds to step S3300, whereas the operation proceeds to step S3400 when the priority of the received packet is high, i.e., when it is high priority (P=1) (S3200:YES).

[0058] In step S3300, since the received packet has low priority (P=0), the SN is incremented by 1 whereas SNHP is not incremented as long as there is no lost packet, and it is decided whether the sequence number of the high priority packet of the presently received packet (present SNHP) is equal to the sequence number of the high priority packet of the previously received packet (previous SNHP). According to decision result, when present SNHP = previous SNHP (S3300:YES), it is decided that there is no loss of high priority packet, then the operation proceeds to step S3900 and waits for reception. On the contrary, when present SNHP = previous SNHP (S3300:NO) is not achieved, it is decided that there is a loss of high priority packet, and the operation proceeds to step S3500.

[0059] While, in step S3400, since the received packet has high priority (P=1), both SN and SNHP are incremented by 1 as long as there is no loss, it is decided whether the sequence number of the high priority packet of the presently received packet (present SNHP) has been incremented by 1 with respect to the sequence number of the high priority packet of the previously received packet (previous SNHP). As a result of the decision, when present SNHP = previous SNHP + 1 (S3400: YES), it is decided that there is no loss of high priority packet, then the operation proceeds to step S3900 and waits for reception. On the contrary, when present SNHP = previous SNHP + 1 (S3400:NO) is not achieved, it is decided that there is a loss of high priority packet, then the operation proceeds to step S3500.

[0060] In step S3500, the playback time calculating section 204 calculates the playback time PLT (=TS-TSO) of the packet by calculating the difference between the timestamp TS of the presently received packet and the timestamp TSO at time when the session has begun to calculate a relative time assuming the time when the session has begun is "0".

[0061] In the following step S3600, the retransmission request deciding section 206 reads out the data round-trip time RTT from the server 100 received by the round-trip time receiving section 205 from the buffer in the round-trip time receiving section 205.

[0062] Next, in step S3700, the retransmission request deciding section 206 decides whether the playback time PLT calculated in step S3500 is less than the sum of the round-trip time RTT read out in step S3600 and the present time, i.e., whether playback time PLT < round-trip time RTT + present time.

[0063] When playback time PLT < round-trip time RTT + present time (step S3600:YES) as a result of the decision, it is determined that a wasteful retransmission request is not made even when the retransmission request is for the lost packet, since the playback time comes earlier than the time when the retransmission request is received, then the operation proceeds to step S3900 and waits for reception.

[0064] On the contrary, when the playback time PLT < round-trip time RTT + present time (step S3600:NO), the playback time comes later than the reception time of the repeat packet, and since it is possible to execute playback after receiving the repeat packet, the process proceeds to step S3800 and the retransmission request for the lost packet is transmitted to the server 100 by the retransmission request deciding section 206.

[0065] As described above, according to the data communication system of the first embodiment, it is possible to eliminate the transmission of wasteful data that is later than the playback time at the receiving side by executing the retransmission request of the lost packet having high priority only when the sum of the round-trip time RTT and the present time is less than the playback time of the packet after calculating the round-trip time RTT of the packet between the server 100 and the terminal apparatus 200, thus, the wasteful utilization of transmission band can be eliminated.

[0066] However, according to the first embodiment, although the retransmitting decision is carried out only when the lost packet is the high priority packet, it is not limited to this. It may be carried out the retransmitting decision for all lost packets regardless to the priority of packets.

[0067] Furthermore, it is conceivable that the first embodiment includes several modifications thereof. FIG. 12 is a block diagram showing another constitution of the data transmitting apparatus (server), and FIG. 13 is a block diagram showing another constitution of the data receiving apparatus (terminal apparatus). Further, herein also, the description will be made while assuming a server and a terminal apparatus as an example of data transmitting apparatus and data receiving apparatus, respectively.

[0068] The characteristic (main feature) of the server 100a shown in FIG. 12 is that the server 100a includes a communication status monitoring section 117 and a time interval altering section 118. The communication

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status monitoring section 117 monitors the communication status of the packet, and the time interval altering section 118 alters the intervals in order to initialize the timer 110, i.e., the time for transmitting the round-trip time RTT, depending on the communication status which is inputted from the communication status monitoring section 117. For example, in case of bad communication status, the time intervals for transmitting the round-trip time RTT is shortened. Accordingly, even when the communication status is bad, the round-trip time RTT can be transmitted satisfactorily to the terminal apparatus 200.

[0069] Furthermore, as another constitution, although it is not shown among the figures, it may be adapted so that the time interval altering section 118 alters the time intervals for transmitting the round-trip time RTT to the terminal apparatus 200 in accordance with a difference between the present and previous round-trip times calculated in the round-trip time calculating section 109. For instance, when the difference between the calculated present and previous round-trip times is small, by elongating the time intervals for transmitting the round-trip time RTT, the utilization of transmission band can be reduced.

[0070] Still further, a characteristic of the terminal apparatus 200a shown in FIG. 13 is that, apparatus 200a includes instead of time measuring section 207, time information transmission deciding section 208, timer 209 and time information transmitting section 210 shown in FIG. 2, the terminal apparatus 200a includes an initial round-trip time storing section 211 and a round-trip time selecting section 212. The initial round-trip time storing section 211 stores a lower limit value and an upper limit value of the round-trip time RTT as an initial value. When the round-trip time RTT is received in the round-trip time receiving section 205, by testing whether the received round-trip time RTT is within the range between the lower and upper limit values stored in the initial round-trip time storing section 211, the round-trip time selecting section 212 selects only the round-trip time RTT that is within the aforementioned range and outputs it to the retransmission request deciding section 206. On account of this, the round-trip time RTT is maintained within a proper range even when it is not received correctly due to transmission route error, time measurement error, etc., therefore, the influence caused by an erroneous round-trip time RTT can be reduced.

[0071] Still furthermore, as another constitution, although it is not shown among the figures, a time interval altering section may be provided to the terminal apparatus 200 shown in FIG. 2, which alters the intervals of initializing the timer 209, i.e., alters the time intervals for transmitting the differential time DLSR to the server 100 in the time information transmitting section 210 in accordance with a difference between the present and previous round-trip times received by the round-trip time receiving section 205. Owing to this, for example, when a difference between the present and previous round-trip times is small, the utilization of transmission band can be reduced by elongating the transmission intervals used for transmitting the differential time DLSR.

(Second Embodiment)

[0072] FIG. 14 is a block diagram showing a constitution of a data transmitting apparatus for a data communication system according to the second embodiment of the present invention, FIG. 15 is a block diagram showing a constitution of a data receiving apparatus for the same data communication system. Further, since the data transmitting apparatus and data receiving apparatus of the data communication system has the same basic constitution as those of the corresponding data transmitting apparatus and the data receiving apparatus according to the first embodiment shown in FIG. 1 and FIG. 2, the same component elements thereof are assigned the same reference numerals and descriptions thereof are omitted. Furthermore, in the second embodiment also, description will be made while taking, respectively, a server and terminal as an example of the data transmitting apparatus and data receiving apparatus.

[0073] The server 300 shown in FIG. 14 includes, in addition to the receiving section 101, transmission queue controlling section 102, packet priority determining section 103, retransmission buffer 104, retransmission buffer controlling section 105, transmitting section 106, retransmission request receiving section 107 and retransmitability deciding section 108 shown in FIG. 1, and instead of the round-trip time calculating section 109, timer 110, round-trip time transmission deciding section 111 and packetizing section 112 shown in FIG. 1, includes a time measuring section 207, time information transmission deciding section 208, timer 209 and time information transmitting section 210 shown in FIG. 2.

[0074] Moreover, the terminal apparatus 400 shown in FIG. 15 includes, in addition to the receiving section 201, loss detecting section 202, priority determining section 203, playback time calculating section 204, round-trip time receiving section 205 and retransmission request deciding section 206 shown in FIG. 2, and instead of the time measuring section 207, time information transmission deciding section 208, timer 209 and time information transmitting section 210 shown in FIG. 2, the first time measuring section 113, time information receiving section 114, second time measuring section 115 and round-trip time calculating section 116 shown in FIG. 4, and the timer 110, round-trip time transmission deciding section 111 and packetizing section 112 shown in FIG. 1.

[0075] That is to say, the second embodiment adopts a constitution in which the round-trip time RTT is calculated by the terminal apparatus 200.

[0076] Next, an operational description of the data communication system having the foregoing constitu-

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tion is given below.

[0077] First, when calculating the round-trip time RTT, the terminal apparatus 400 measures the time T1 (terminal apparatus transmission time) when the packet P1 is transmitted from the relevant terminal apparatus 400 (referring to FIG. 16) in the first time measuring section 113.

[0078] Then, the packet P2 transmitted from the server 300 is received by the time information receiving section 114. In the packet P2, both the differential time DLSR measured from the time when the server 300 has received the packet P1 to the time when the packet P2 is transmitted to the terminal apparatus 400 and terminal apparatus transmission time T1 transmitted by the terminal apparatus 400 are recorded.

[0079] Next, in the second time measuring section 115, the time T2 (terminal apparatus reception time) when the packet P2 is received by the time information receiving section 114 is measured (referring to FIG. 16).

[0080] After that, the round-trip time calculating section 116 calculates the round-trip time by subtracting the differential time DLSR recorded in the packet P2 and the terminal apparatus transmission time T1 from the terminal apparatus reception time T2, the round-trip time RTT (=T2-DLSR-T1) and the obtained result is outputted to the round-trip time receiving section 205.

[0081] On the other hand, whenever the timer 209 is reset after a specific time has passed, i.e., at regular intervals, the server 300 outputs the transmission time of the differential time DLSR to the time information transmission deciding section 208.

[0082] The time information transmission deciding section 208 decides whether the packet P1 from the terminal apparatus 400 has been newly received by the time measuring section 207 at every transmission time transmitted from the timer 209, and when the packet P1 has been received, the packet transmission time TT2 is set as the present time.

[0083] Then, the time measuring section 207 obtains the difference between the packet transmission time TT2 (present time) and the packet reception time TT1 (the latest time when the packet P1 is received) and the obtained difference is defined as the differential time DLSR (=TT2-TT1).

[0084] Next, the time information transmitting section 210 transmits the differential time DLSR to the terminal apparatus 400.

[0085] Since the other operations thereof are the same as that of the data communication system corresponding to the first embodiment, the description thereof is omitted.

[0086] As described above and according to the data communication system of the second embodiment, it is possible to eliminate the transmission of wasteful data that is later than the playback time at the receiving side by executing the retransmission request of the lost packet having the high priority only when the sum of the round-trip time RTT and the present time is less than the playback time of the packet after calculating the round-trip time RTT of the packet between the server 300 and the terminal apparatus 400, thus the wasteful utilization of transmission band can be eliminated.

[0087] Further, in the second embodiment, although the retransmission decision is carried out only when the lost packet is of high priority, it is not limited to this, but also it may be carried out on every lost packet regardless to the priority of the packet.

[0088] Furthermore, in the respective foregoing embodiments, the data communication system is composed of data transmitting apparatus (server) 100 or 300 and data receiving apparatus (terminal apparatus) 200 or 400, the data communication system is not limited to this. For example, a composition in which a relay apparatus is provided between the data transmitting apparatus and data receiving apparatus may be adopted.

[0089] The description of the invention is based on both, the Japanese Patent Application No. 2000-207296 filed on July 7, 2000 and the Japanese Patent Application No. 2001-199621 filed on June 29, 2000. Entire content of the above is expressly incorporated by reference herein.

Industrial Applicability

[0090] The present invention is applicable to a data transmitting apparatus and a data receiving apparatus in a data communication system.

Claims

1. A data transmitting apparatus, comprising:

   storing means for storing a retransmittable data only;
   retransmitting means for retransmitting a data that is extracted from the data stored in said storing means corresponding to a retransmission request of a receiving side;
   calculating means for calculating a data round-trip time between the receiving side and the data transmitting apparatus; and
   transmitting means for transmitting the data round-trip time calculated by said calculating means to the receiving side at a predetermined time interval.

2. The data transmitting apparatus according to claim 1, wherein the retransmittable data is a data that has high priority.

3. The data transmitting apparatus according to claim 1, wherein said calculating means comprises:

   means for measuring transmission time of a first data to be transmitted to the receiving side;

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means for measuring reception time of a second data transmitted from the receiving side in response to the first data; and
means for calculating the data round-trip time by subtracting a differential time between reception time of the first data at the receiving side and transmission time of the second data, the differential time being included in the second data, and the measured first data transmission time from the measured second data reception time.

4. The data transmitting apparatus according to claim 3, wherein said calculating means calculates, when the measured first data transmission time is transmitted to the receiving side and the first data transmission time is included in the second data together with the differential time, the data round-trip time using the first data transmission time included in the second data.

5. The data transmitting apparatus according to claim 1, further comprising packetizing means for packetizing the data round-trip time calculated by said calculating means together with other information to form a single packet, and wherein said transmitting means transmits the single packet formed by said packetizing means to the receiving side at a predetermined time interval.

6. The data transmitting apparatus according to claim 1, further comprising:

monitoring means for monitoring the status of data communication; and
altering means for altering the time interval at which the data round-trip time calculated by said calculating means is transmitted to the receiving side in accordance with the result of the monitoring by said monitoring means.

7. The data transmitting apparatus according to claim 1, further comprising altering means that includes means for holding the data round-trip time calculated by said calculating means and for altering the time interval at which a present data round-trip time calculated by said calculating means is transmitted to the receiving side in accordance with a time difference between the present data round-trip time and a previous data round-trip time calculated by said calculating means.

8. A data transmitting apparatus, comprising:

storing means for storing a retransmittable data only;
retransmitting means for retransmitting a data that is extracted from the data stored in said storing means corresponding to a retransmission request of a receiving side;
measuring means for measuring a differential time between reception time of a first data transmitted from the receiving side and transmission time of a second data to be transmitted to the receiving side in response to the first data; and
transmitting means for transmitting the differential time measured by said measuring means included in the second data to the receiving side at a predetermined time interval.

9. A data receiving apparatus, comprising:

receiving means for receiving a data;
loss detecting means for detecting loss of data when the data is received by said receiving means;
playback time calculating means for calculating playback time of the data received by said receiving means;
round-trip time receiving means for receiving a data round-trip time between a transmitting side and the data receiving apparatus; and
retransmission request deciding means for deciding, when a lost data is detected by said loss detecting means, whether a retransmission request for the lost data is made or not based on the playback time calculated by said playback time calculating means and the data round-trip time received by said data round-trip time receiving means.

10. The data receiving apparatus according to claim 9, further comprising priority determining means for determining, when a lost data is detected by said loss detecting means, the priority of the lost data, and wherein said retransmission request deciding means decides whether the retransmission request is made or not for the lost data which is determined by said priority determining means that the priority thereof is not less than a predetermined value.

11. The data receiving apparatus according to claim 9, further comprising:

measuring means for measuring a differential time between reception time of a first data transmitted from a transmitting side and transmission time of a second data to be transmitted to the transmitting side in response to the first data; and
transmitting means for transmitting the differential time measured by said measuring means included in the second data to the transmitting side at a predetermined time interval.

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12. The data receiving apparatus according to claim 9, further comprising transmission time receiving means for receiving transmission time of the first data transmitted from the transmitting side, and wherein said transmitting means transmits the transmission time received by said transmission time receiving means together with the differential time measured by said measuring means to the transmitting side at the predetermined time interval.

13. The data receiving apparatus according to claim 9, further comprising:

storing means for storing a lower limit value and an upper limit value of the data round-trip time; and
selecting means for selecting only a data round-trip time that is within a range between the lower limit value and the upper limit value stored in said storing means from the data round-trip time received by said data round-trip time receiving means, and

wherein said retransmission request deciding means decides, when a lost data is detected by said loss detecting means, whether the retransmission request for the lost data is made or not based on the playback time calculated by said playback time calculating means and the data round-trip time selected by said selecting means.

14. The data receiving apparatus according to claim 11, further comprising altering means that includes means for holding the data round-trip time received by said data round-trip time receiving means and for altering the time interval at which the differential time measured by said measuring means is transmitted to the transmitting side in accordance with a time difference between a present data round-trip time and a previous data round-trip time that are received by said round-trip time receiving means.

15. A data receiving apparatus, comprising:

calculating means for calculating a data round-trip time between a transmitting side and the data receiving apparatus by subtracting transmission time of a first data transmitted to the transmitting side and a differential time between reception time of the first data at the transmitting side and transmission time of a second data transmitted from the transmitting side, the differential time being included in the second data, from reception time of the second data;
receiving means for receiving a data;
loss detecting means for detecting loss of data when the data is received by said receiving means;
playback time calculating means for calculating playback time of the data received by said receiving means; and
retransmission request deciding means for deciding, when a lost data is detected by said loss detecting means, whether a retransmission request for the lost data is made or not based on the playback time calculated by said playback time calculating means and the data round-trip time calculated by said calculating means.

16. Abase station apparatus including the data transmitting apparatus in any one of claims 1 through 8.

17. An information communication terminal apparatus including the data receiving apparatus in any one of claims 9 through 15.

18. A mobile station apparatus including the data receiving apparatus in any one of claims 9 through 15.

19. A data communication system comprising a data transmitting apparatus and a data receiving apparatus,

wherein the data transmitting apparatus comprises:

storing means for storing a retransmittable data only;
retransmitting means for retransmitting a data that is extracted from the data stored in said storing means corresponding to a retransmission request of the data receiving apparatus;
calculating means for calculating a data round-trip time between the data receiving apparatus and the data transmitting apparatus; and
transmitting means for transmitting the data round-trip time calculated by said calculating means to the data receiving apparatus at a predetermined time interval, and

wherein the data receiving apparatus comprises:

receiving means for receiving the data transmitted from the data transmitting apparatus;
loss detecting means for detecting loss of data when the data is received by said receiving means;
playback time calculating means for calculating playback time of the data received by said receiving means;
round-trip time receiving means for receiving the data round-trip time transmitted from said transmitting means; and
retransmission request deciding means for deciding, when a lost data is detected by said loss

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detecting means, whether a retransmission request for the lost data is made or not based on the playback time calculated by said playback time calculating means and the data round-trip time received by said round-trip time receiving means.

20. A data communication system comprising a data transmitting apparatus and a data receiving apparatus,

wherein the data transmitting apparatus comprises:

storing means for storing a retransmittable data only;
retransmitting means for retransmitting a data that is extracted from the data stored in said storing means corresponding to a retransmission request of the data receiving apparatus;
measuring means for measuring a differential time between reception time of a first data transmitted from the data receiving apparatus and transmission time of a second data to be transmitted to the data receiving apparatus in response to the first data; and
transmitting means for transmitting the differential time measured by said measuring means included in the second data to the data receiving apparatus at a predetermined time interval, and

wherein the data receiving apparatus comprises:

calculating means for calculating a data round-trip time between the data transmitting apparatus and the data receiving apparatus by subtracting transmission time of the first data transmitted to the data transmitting apparatus and the differential time included in the second data transmitted from the data transmitting apparatus from reception time of the second data;
receiving means for receiving the data transmitted from the data transmitting apparatus;
loss detecting means for detecting loss of data when the data is received by said receiving means;
playback time calculating means for calculating playback time of the data received by said receiving means; and
retransmission request deciding means for deciding, when a lost data is detected by said loss detecting means, whether a retransmission request for the lost data is made or not based on the playback time calculated by said playback time calculating means and the data round-trip time calculated by said calculating means.

21. The data communication system according to claim 19 or 20, further comprising priority determining means for determining, when a lost data is detected by said loss detecting means, the priority of the lost data, and wherein said retransmission request deciding means decides whether the retransmission request is made or not for the lost data which is determined by said priority determining means that the priority thereof is not less than a predetermined value.

22. A data communication method in a data communication system comprising a data receiving apparatus and a data transmitting apparatus that retransmits a data which is extracted from the data stored in storing means for storing a retransmittable data only corresponding to a retransmission request of the data receiving apparatus, said method comprising:

a calculating step in which the data transmitting apparatus calculates a data round-trip time between the data receiving apparatus and the data transmitting apparatus;
a transmitting step in which the data transmitting apparatus transmits the data round-trip time calculated in the calculating step to the data receiving apparatus at a predetermined time interval;
a receiving step in which the data receiving apparatus receives the data transmitted from the data transmitting apparatus;
a loss detecting step in which the data receiving apparatus detects loss of data when the data is received in the receiving step;
a playback time calculating step in which the data receiving apparatus calculates playback time of the data received in the receiving step;
a round-trip time receiving step in which the data receiving apparatus receives the data round-trip time transmitted in the transmitting step; and
a retransmission request deciding step in which the data receiving apparatus decides, when a lost data is detected in the loss detecting step, whether a retransmission request for the lost data is made or not based on the playback time calculated in the playback time calculating step and the data round-trip time received in the round-trip time receiving step.

23. A data communication method in a data communication system comprising a data receiving apparatus and a data transmitting apparatus that retransmits a data which is extracted from the data stored in storing means for storing a retransmittable data only corresponding to a retransmission request of the data receiving apparatus, said method-compris-

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ing:

a measuring step in which the data transmitting apparatus measures a differential time between reception time of a first data transmitted from the data receiving apparatus and transmission time of a second data to be transmitted to the data receiving apparatus in response to the first data;

a transmitting step in which the data transmitting apparatus transmits the differential time measured in the measuring step included in the second data to the data receiving apparatus at a predetermined time interval;

a calculating step in which the data receiving apparatus calculates a data round-trip time between the data transmitting apparatus and the data receiving apparatus by subtracting transmission time of the first data transmitted to the data transmitting apparatus and the differential time included in the second data transmitted from the data transmitting apparatus from reception time of the second data;

a receiving step in which the data receiving apparatus receives the data transmitted from the data transmitting apparatus;

a loss detecting step in which the data receiving apparatus detects loss of data when the data is received in the receiving step;

a playback time calculating step in which the data receiving apparatus calculates playback time of the data received in the receiving step; and

a retransmission request deciding step in which the data receiving apparatus decides, when a lost data is detected in the loss detecting step, whether a retransmission request for the lost data is made or not based on the playback time calculated in the playback time calculating step and the data round-trip time calculated in the calculating step.

24. The data communication method in the data communication system according to claim 22 or 23, further comprising a priority determining step in which the data receiving apparatus determines, when a lost data is detected in the loss detecting step, the priority of the lost data, and wherein in the retransmission request deciding step it is decided whether the retransmission request is made or not for the lost data which is determined in the priority determining step that the priority thereof is not less than a predetermined value.

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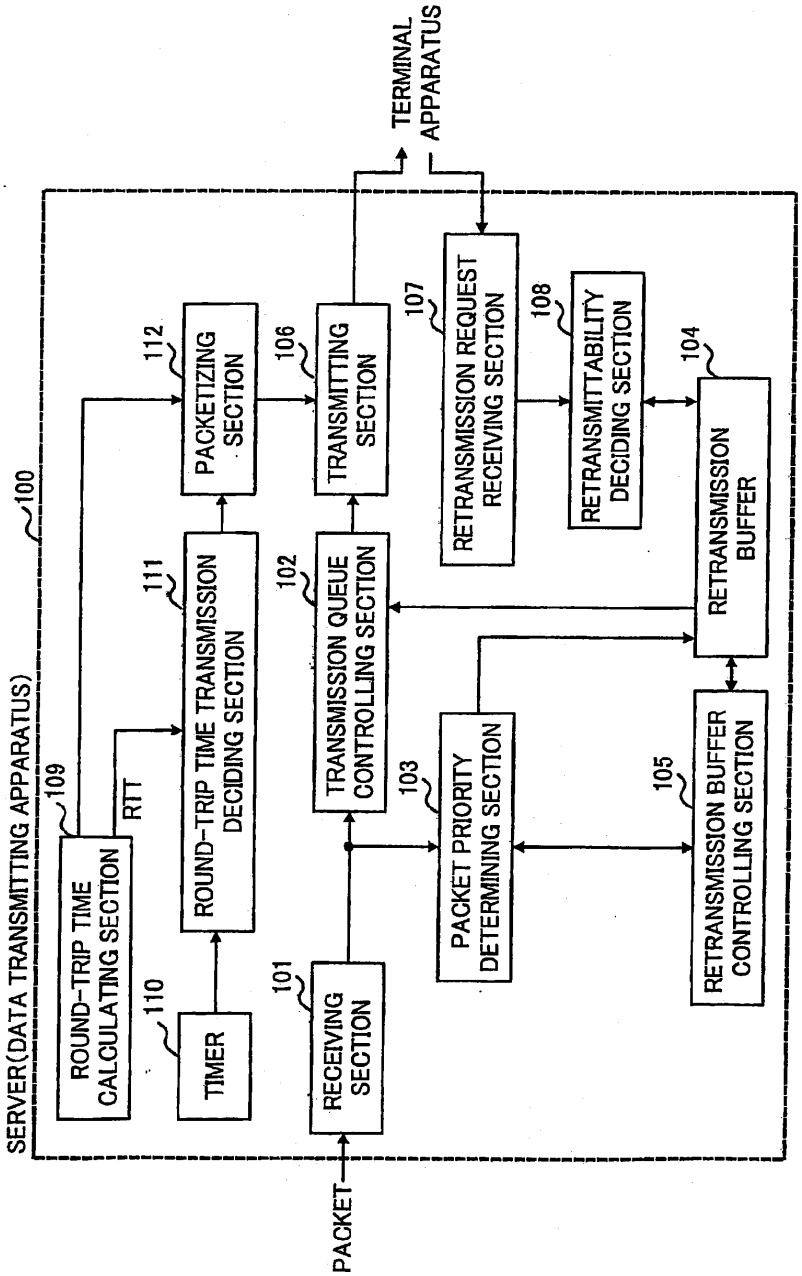

FIG.1

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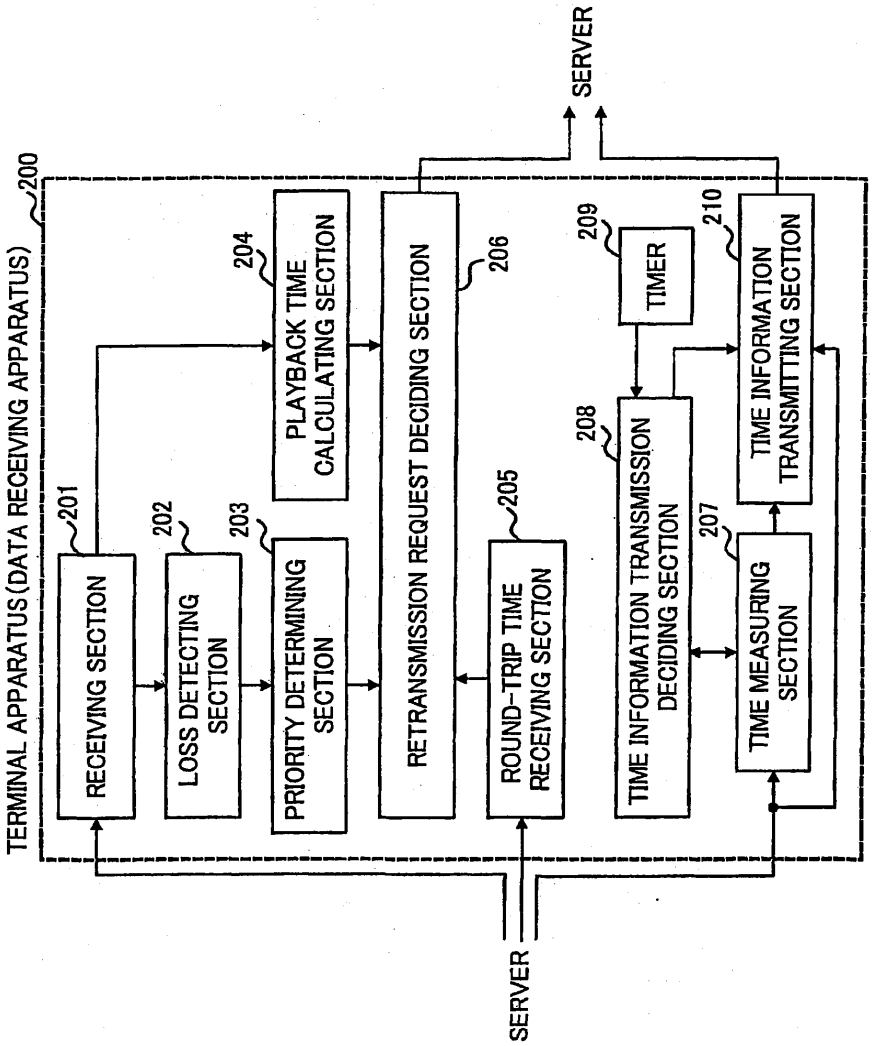

FIG.2

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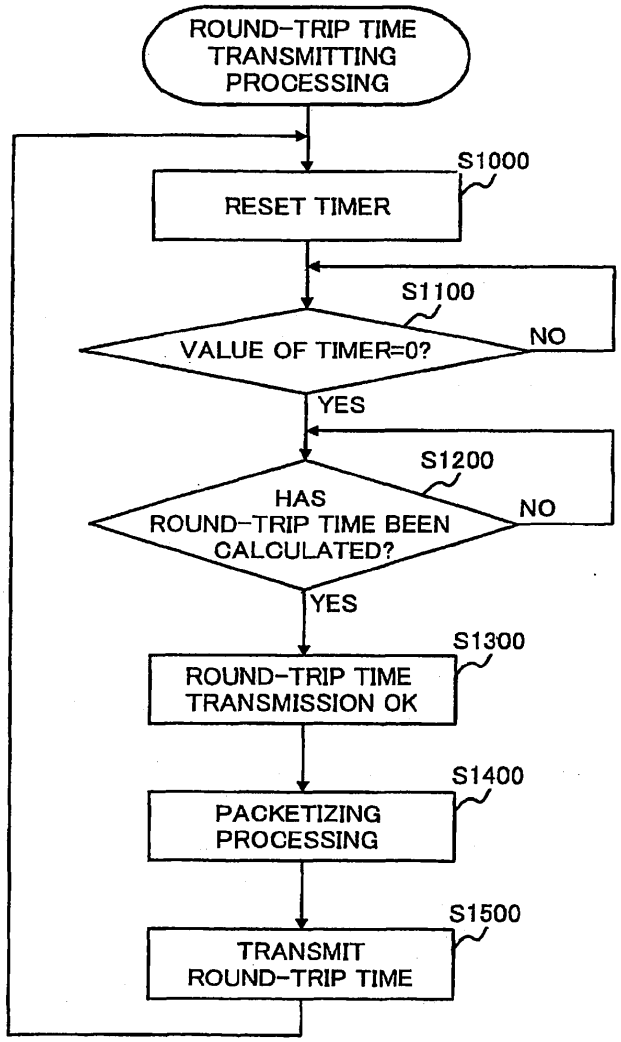

FIG.3

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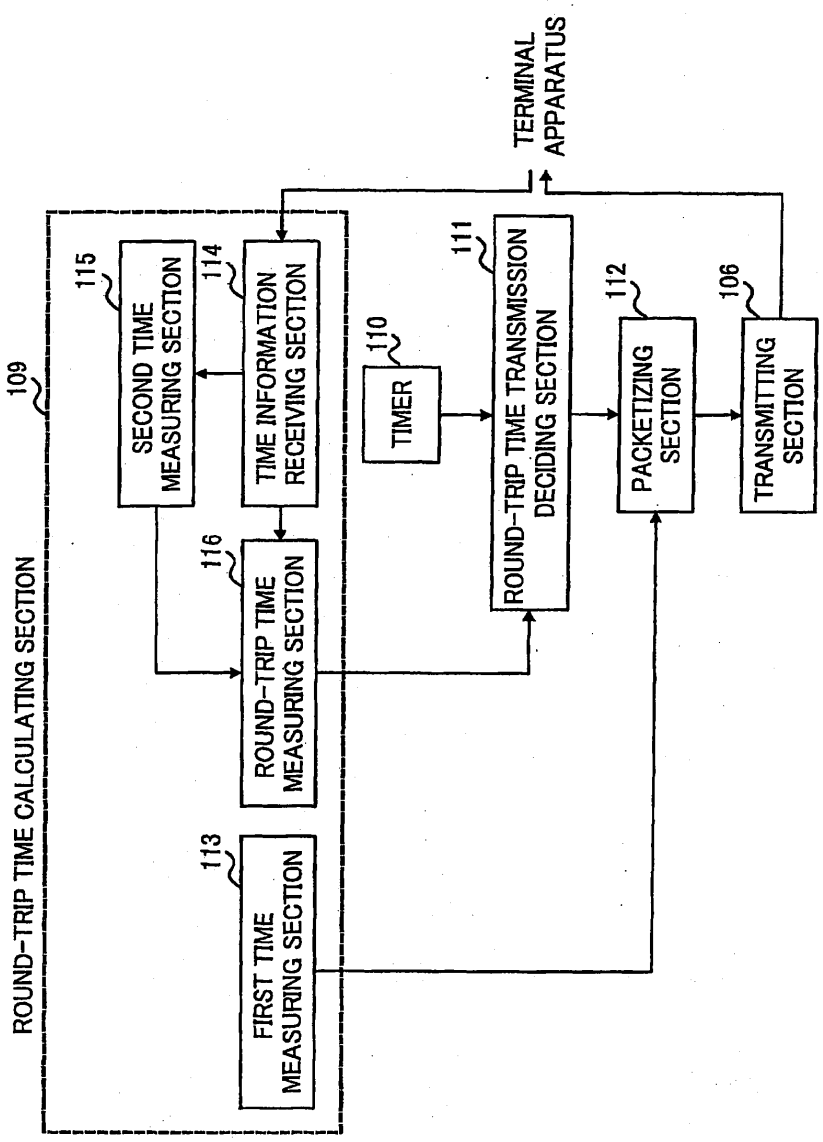

FIG.4

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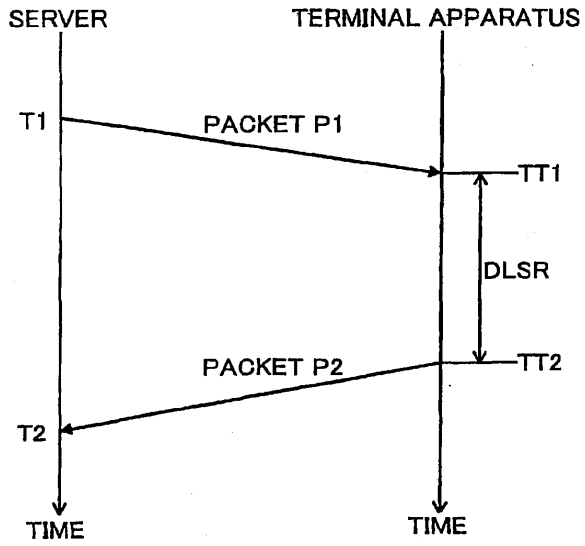

FIG.5

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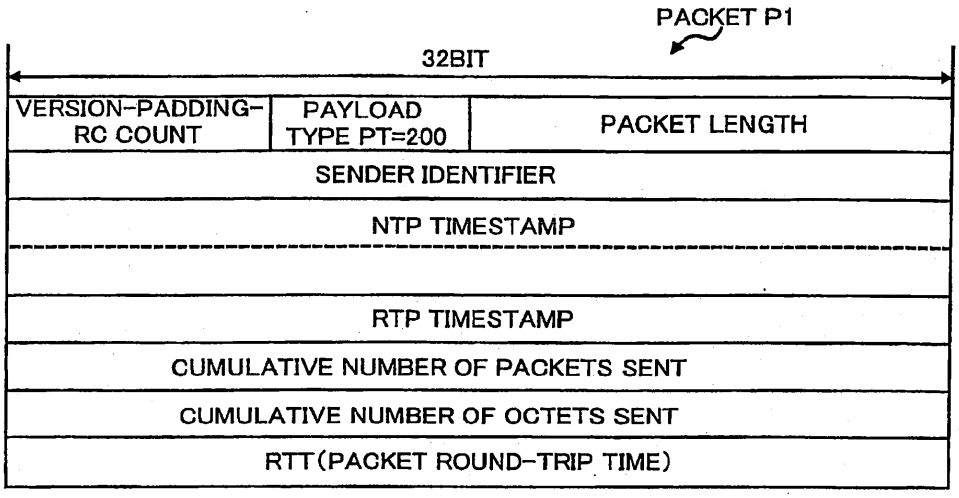

FIG.6

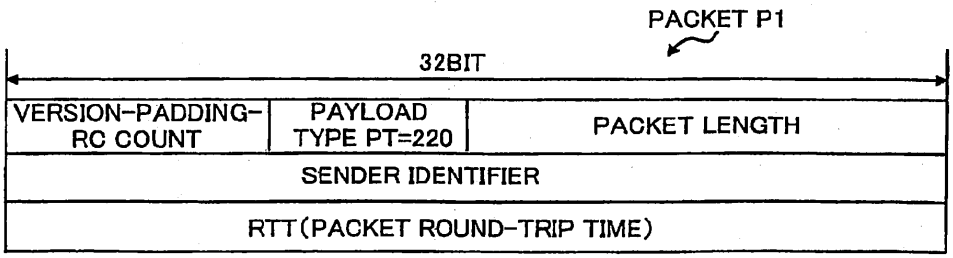

FIG.7

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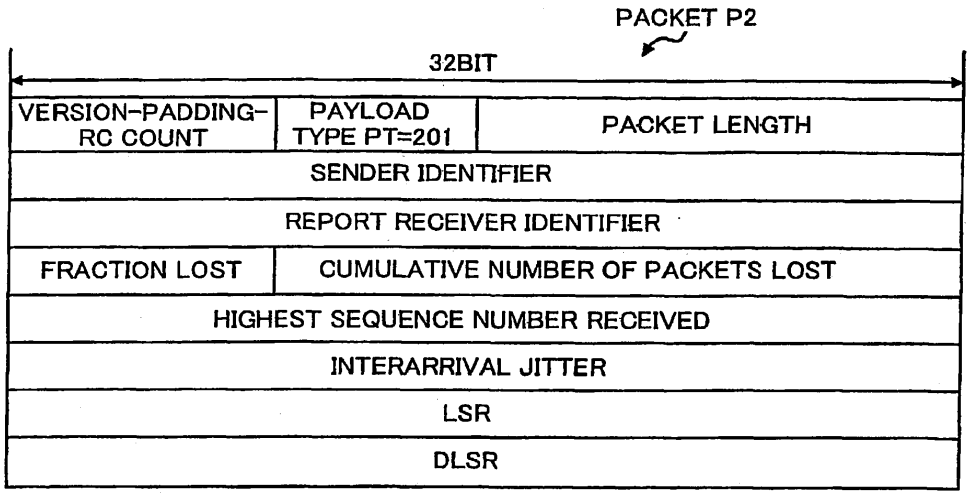

FIG.8

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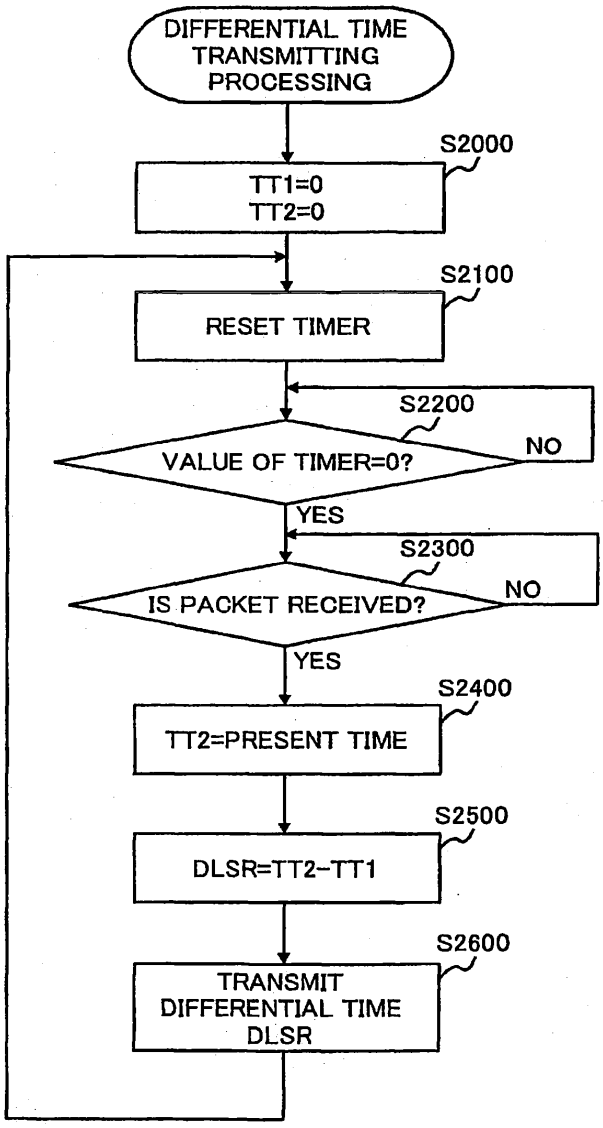

FIG.9

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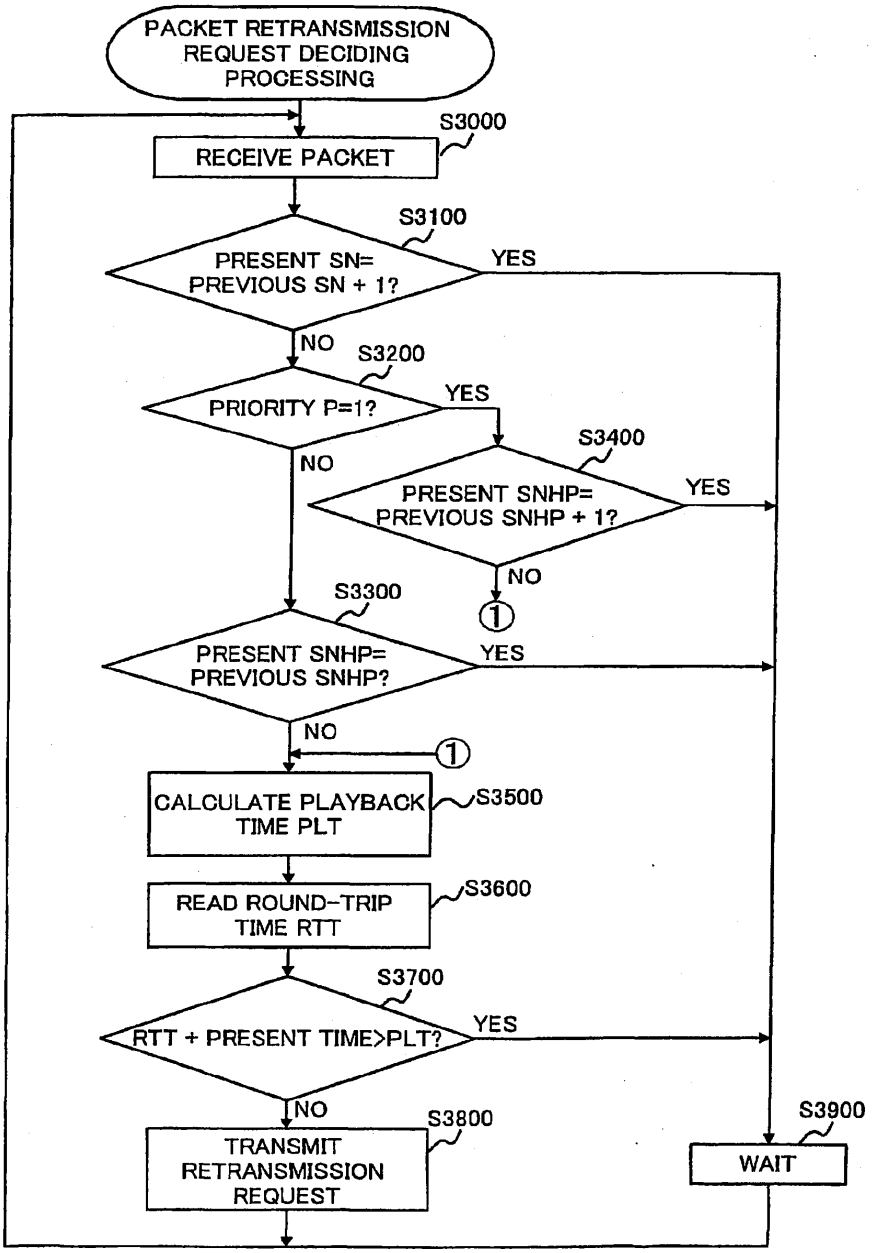

FIG.10

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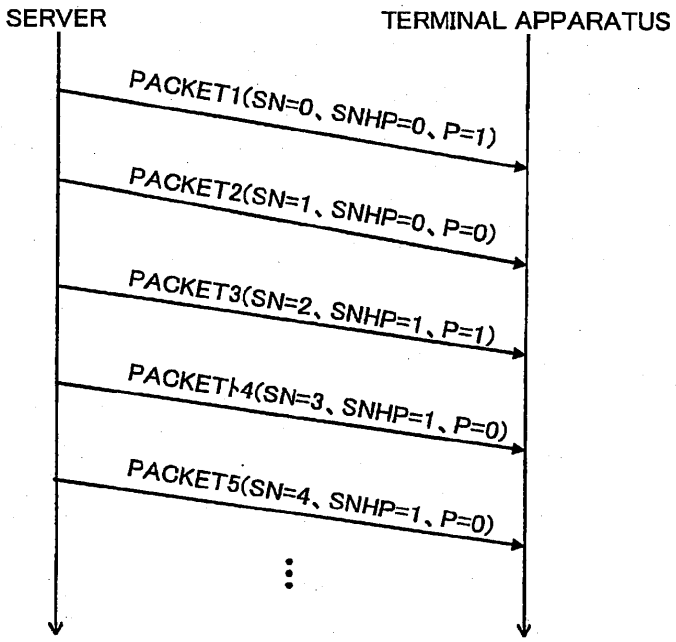

FIG.11

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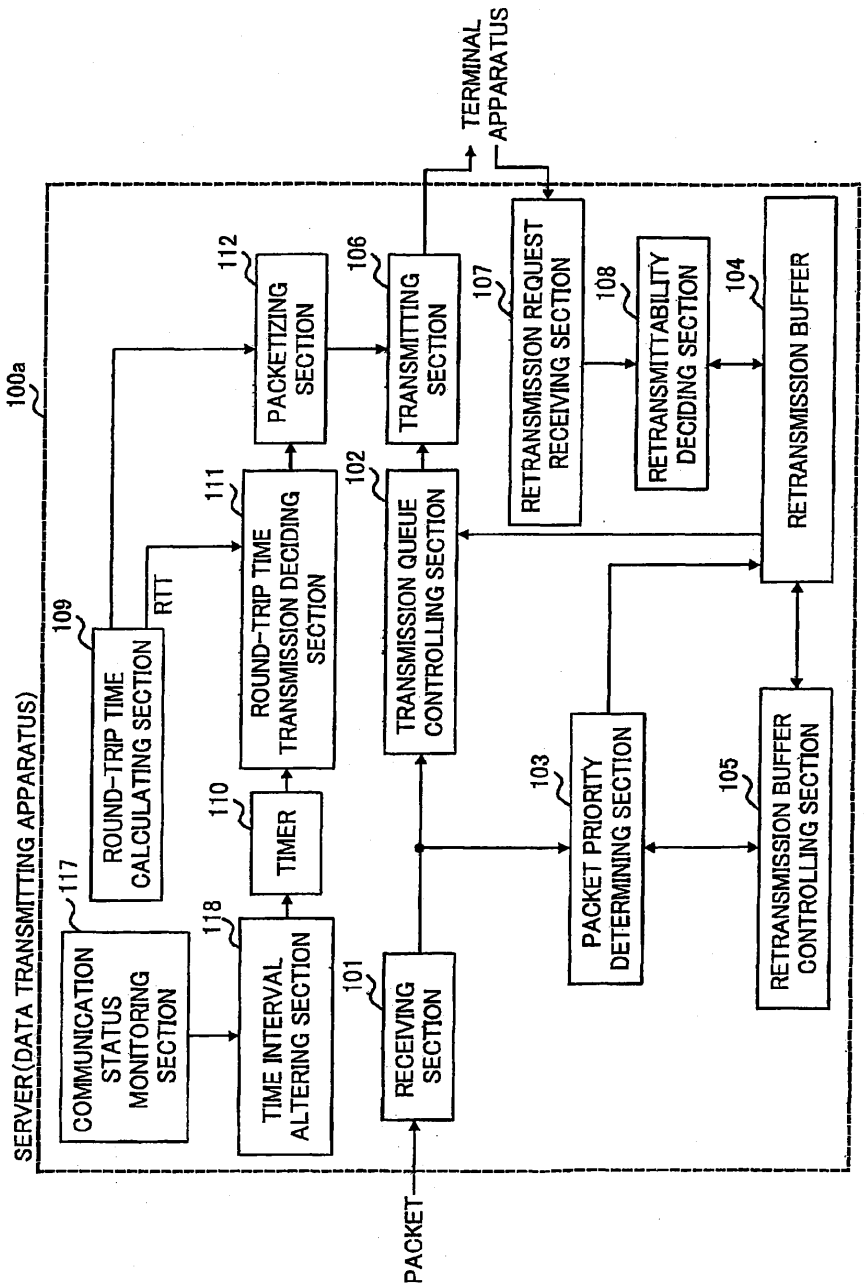

FIG.12

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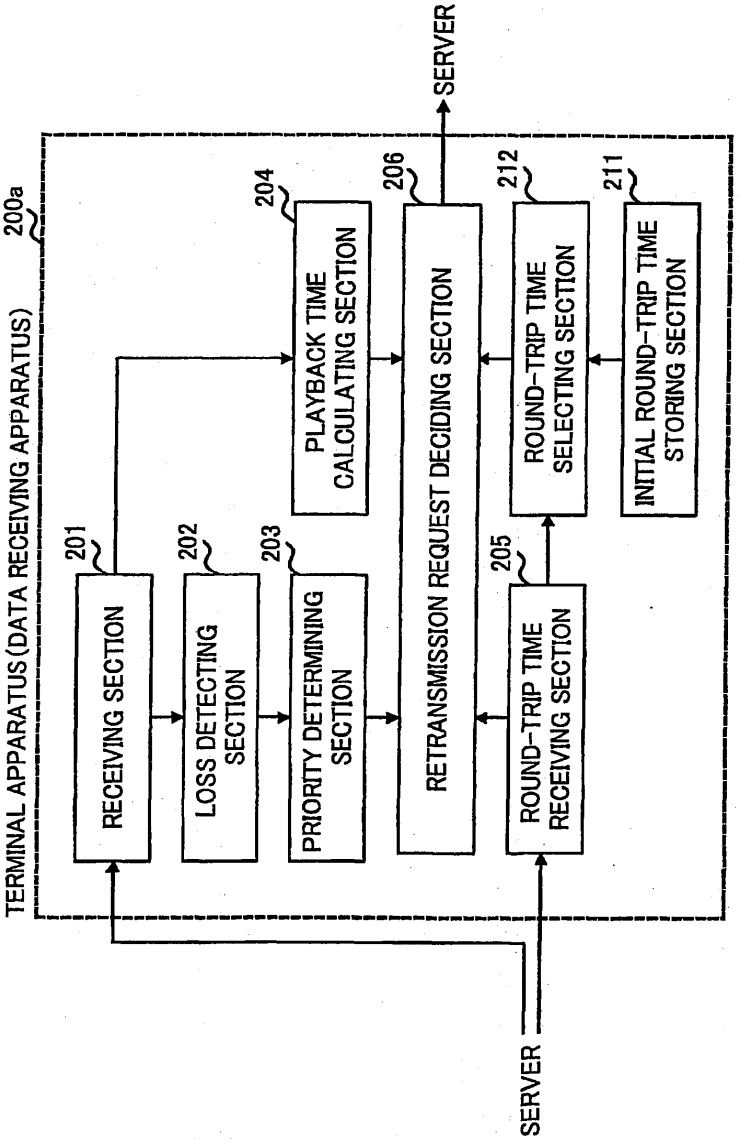

FIG.13

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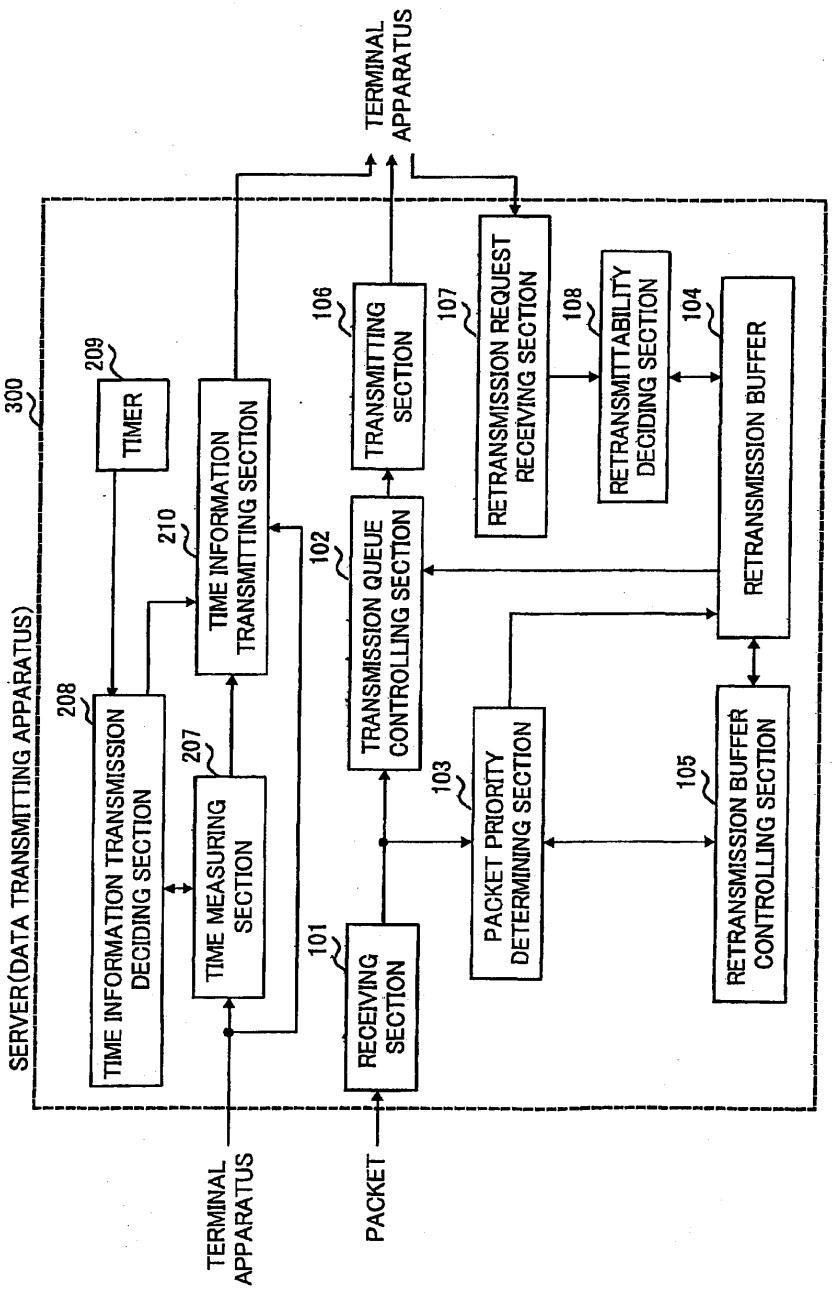

FIG.14

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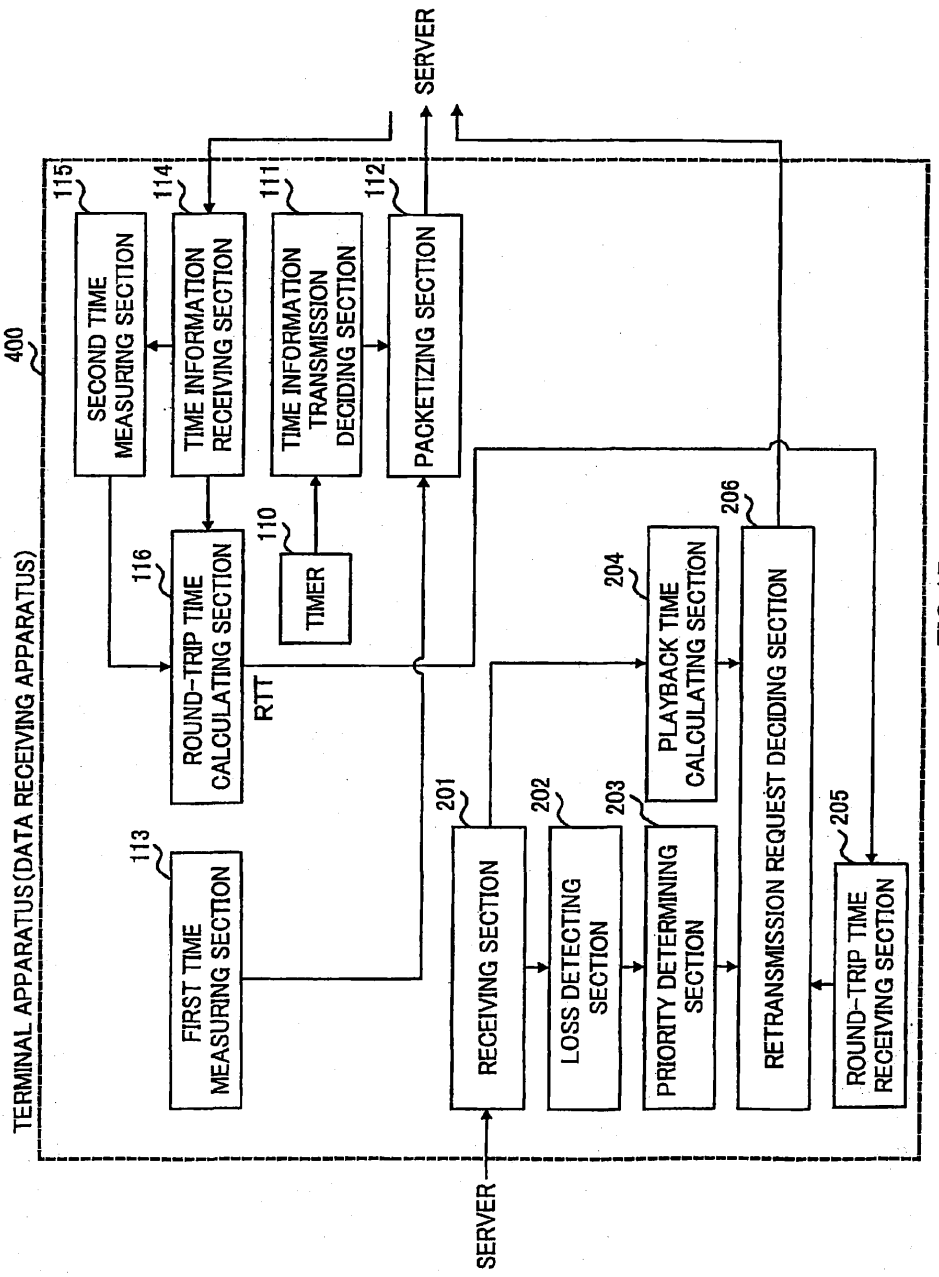

FIG.15

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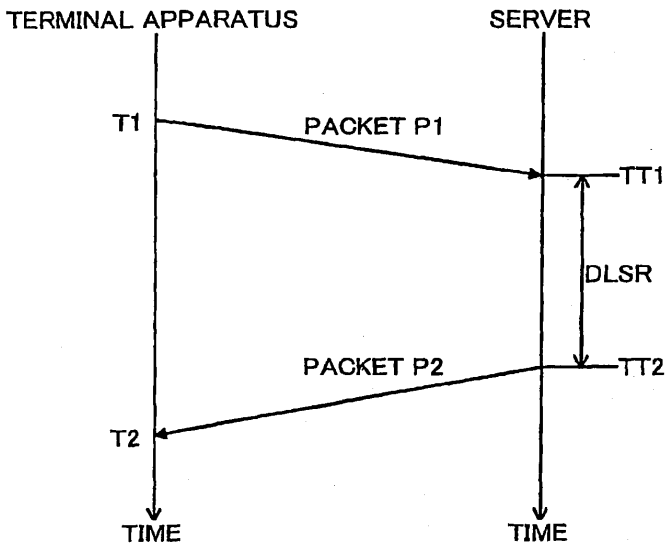

FIG.16

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INTERNATIONAL SEARCH REPORT

International application No.
PCT/JP01/05831

A. CLASSIFICATION OF SUBJECT MATTER
Int.Cl[7] H04L 12/56, H04L 29/08, H04L 1/16

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
Int.Cl[7] H04L 12/56, H04L 29/08, H04L 1/16

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched
Jitsuyo Shinan Koho 1926-1996 Toroku Jitsuyo Shinan Koho 1994-2001
Kokai Jitsuyo Shinan Koho 1971-2001 Jitsuyo Shinan Toroku Koho 1996-2001

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X Y	JP 9-191314 A (Mitsubishi Electric Corporation), 22 July, 1997 (22.07.97) (Family: none) Par. Nos. [0022] to [0026], [0035], [0040] to [0042]	1,2,5,9,10, 16-24 3,4,8,11-13,15
A		6,7,14
Y	JP 2000-69088 A (Nippon Telegr. & Teleph. Corp. <NTT>), 03 March, 2000 (03.03.00) (Family: none) Par. Nos. [0009] to [0012]	3,4,8,11,12,15
Y	US 5978335 A (Alan Robert Clark), 02 November, 1999 (02.11.99), & JP 10-64174 A & EP 817193 A2 & KR 98004472 A Claim 12	13
A	JP 3-286644 A (Hitachi, Ltd.), 17 December, 1991 (17.12.91) (Family: none) page 5, lower right column, line 19 to page 6, upper left column, line 4	6

☒ Further documents are listed in the continuation of Box C. ☐ See patent family annex.

* Special categories of cited documents:
"A" document defining the general state of the art which is not considered to be of particular relevance
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"L" document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)
"O" document referring to an oral disclosure, use, exhibition or other means
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Date of the actual completion of the international search	Date of mailing of the international search report
19 September, 2001 (19.09.01)	02 October, 2001 (02.10.01)
Name and mailing address of the ISA/ Japanese Patent Office Facsimile No.	Authorized officer Telephone No.

Form PCT/ISA/210 (second sheet) (July 1992)

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INTERNATIONAL SEARCH REPORT

International application No.
PCT/JP01/05831

C (Continuation). DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
A	JP 57-13596 A (NEC Corporation), 23 January, 1982 (23.01.82) (Family: none) Claims	7,14
A	JP 10-126771 A (Toshiba Corporation), 15 May, 1998 (15.05.98) (Family: none) Par. Nos. [0081] to [0083]	1,19,22
A	JP 11-127108 A (Nissan Motor Co., Ltd.), 11 May, 1999 (11.05.99) (Family: none) Par. Nos. [0032] to [0039]	1-24

Form PCT/ISA/210 (continuation of second sheet) (July 1992)

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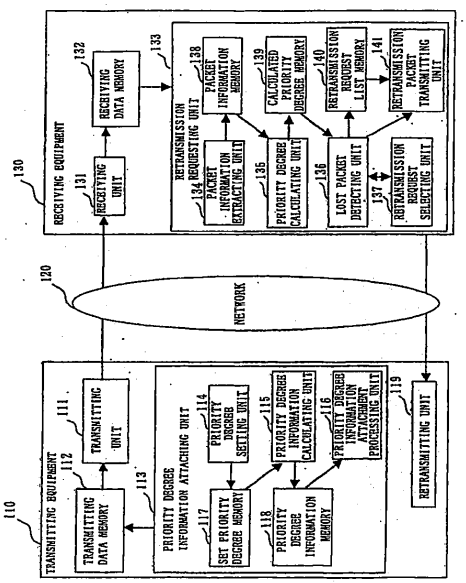
(54) PACKET RETRANSMISSION SYSTEM, PACKET TRANSMISSION DEVICE, PACKET RECEPTION DEVICE, PACKET RETRANSMISSION METHOD, PACKET TRANSMISSION METHOD AND PACKET RECEPTION METHOD

(57) In a packet retransmitting system for retransmitting a packet including a sequence number in a packet header, which is lost during packet communication, a transmitting equipment (110) includes a priority degree information attaching unit (113) for defining a plurality of priority degrees, setting an importance degree of each of the plurality of priority degrees for a packet, producing priority degree information by using the plurality of priority degrees, and attaching the priority degree information to the packet header included in the packet repeatedly for each of the plurality of packets, a transmitter (111) for transmitting the plurality of packets, and a retransmitting unit (119) for receiving a retransmission request packet and retransmitting a packet of which retransmission is requested in the retransmission request packet received. A receiving equipment (130) includes a receiving unit (131) for receiving the plurality of packets and a retransmission requesting unit (133) for extracting a plurality of sequence numbers and a plurality of priority degree information from the packet header, detecting lost packets based on the plurality of sequence numbers and the plurality of priority degree information extracted, detecting an important packet among the lost packets, and requesting retransmission of the packet.

Fig. 1



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Description

Technical Field

[0001] This invention relates to a system and a method of requesting retransmission between a server for distributing data, e.g., multimedia data which have a plurality of priority degrees and a client based on the plurality of priority degrees when a packet is lost.

Background Art

[0002] Generally, a packet transmitted in a network is often lost due to an overflow at a node (router) provided in the network, bit error in a wireless space, etc. In such a case, there is a method in which a receiver requests a transmitter to retransmit a lost packet, and the transmitter who is requested to retransmit retransmits the lost packet.

[0003] For example, in a protocol of TCP (Transmission Control Protocol), the receiver transmits an ACK packet to the transmitter for acknowledging receipt. When the ACK packet is not returned to the transmitter, the transmitter judges that the receiver has not received a packet and retransmits the packet. As stated, the TCP protocol is a reliable transfer protocol.

[0004] However, unlike downloading of data, it is not necessary to receive all of data for reproducing the data in streaming distribution in multimedia. Therefore, the receiver can request to retransmit only an important data packet when the packet is lost, and the transmitter can retransmit only the important data packet. Since only the important packet is retransmitted, a band (bandwidth) can be utilized effectively. Further, since the receiver does not wait for the retransmission of an unnecessary data packet, real-time characteristics can be improved.

[0005] A retransmission control system for the above-stated purposes is disclosed in Japanese Unexamined Published Patent Application Hei 9-214507 and Japanese Unexamined Published Patent Application Hei 11-284657.

[0006] The retransmitting system disclosed in Japanese Unexamined Published Patent Application Hei 9-214507 uses a wireless communication method for performing real-time communication while guaranteeing a possible best quality. In the wireless communication method, when the packet is lost, the retransmission is tried a few times. If the retransmission does not reach the receiver after trying, a packet in a low priority degree is cancelled, and the retransmission is tried.

[0007] A retransmitting system disclosed in Japanese Unexamined Published Patent Application Hei 11-284657 is a retransmission control system in a connection establishing type communication for suppressing communication of a packet in a low priority degree at a time of congestion. In this retransmission control system, a possible number of retransmission to each connection is set, and the possible number of retransmission is reduced by one after retransmission. When the possible number of retransmission becomes zero, communication to the connection is stopped, and a band in a high priority degree is secured as much as possible.

[0008] Further, as a protocol for data transfer with high real-time characteristics, e.g., streaming distribution, RTP (Real-Time Transport Protocol) is a standard related to Internet, e.g., RFC (Request for Comments) 1889. The RTP is a protocol for transmitting a packet to which a sequence number and a timestamp are attached. Some retransmitting systems using the RTP are proposed.

[0009] As a method for extending a retransmission function of the RTP, an Internet draft (draft-miyazaki-avt-rtp-selret-01.txt) titled "RTP Payload Type Format to Enable Multiple Selective Retransmissions" has been submitted to IETF (Internet Engineering Task Force). In this method for extending the retransmission function written in the Internet draft, there is a second sequence number (SSN: Second Sequence Number) allocated only to an important packet to be retransmitted besides a RTP sequence number. By using the SSN, the receiver can identify the important packet to be retransmitted, and even if the packet is lost, the receiver can request to retransmit only the important packet. In this Internet draft, a RTP header in a RTP packet transferred from the transmitter to the receiver is configured as illustrated in Fig. 16 (201). Fig. 17 (202) illustrates a RTCP (Real-Time Contral Protocol) packet for requesting the retransmission, which is transferred from the receiver to the transmitter. In the RTP header illustrated in Fig. 16 (201), the RTP header of the RFC 1889 is extended by 4 bytes, and a SSN field is provided there. The SSN is different from the RTP sequence number. In the SSN, an initial value is zero, and the value is increased by one only for the important packet which should be retransmitted. Further, S is SSNIndicator for indicating that the SSN is increased by one.

[0010] Fig. 18 shows a process of specifying a packet of which retransmission is requested based on the SSN included in the RTP header of Fig. 16 (201) by the receiver. As illustrated in Fig. 18, the RTP sequence number is increased by one for every packet (301), but the SSN is increased by one only for each of important packets (302). Further, it is possible to detect a timing when the SSN is increased by one. As stated, the SSN indicates that the packet in which the SSN is increased by one is the important packet which should be retransmitted when the packet is lost.

[0011] For example, when the receiver receives a packet of RTP sequence number 15 just after a packet of RTP sequence number 10, packets of RTP sequence numbers 11 - 14 are lost. In this case, the SSN of the packet of RTP

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sequence number 10 is 3, and the SSN of the packet of RTP sequence number 15 is 6. Since the SSN is increased from 3 to 6 inconsecutively, it is easy to judge that two important packets of which SSN's are 4 and 5, which should be retransmitted, are lost. Further, since it is judged that the packet of RTP sequence number 15 is not an important packet to be retransmitted based on a S bit in the RTP header (303), an important packet of which SSN is 6 is also lost. Therefore, the receiver transmits values of the SSN's, i.e., 4, 5, and 6, of the packets which should be retransmitted as a retransmission request to the transmitter. The transmitter retransmits an important packet to be transmitted, of which S bit of the RTP header is 1, among the packets of which SSN's are 4, 5 and 6.

[0012] As stated, in the retransmission according to the TCP protocol, since a retransmission packet is waited for, it takes time for the retransmission. Further, an excess of the ACK packet and an increase of the retransmission packet pressure a band, and cause congestion. Further, the receiver waits for the retransmission packet and requests the retransmission many times. The receiver is performing a useless retransmission processing.

[0013] The retransmitting system of the RTP written in the Internet draft titled "RTP Payload Type Format to Enable Multiple Selective Retrasmissions" is a retransmitting system when one priority degree is set. For setting a plurality of priority degrees, a plurality of SSN's is necessary. Consequently, a length of the RTP header becomes longer. In an example of Fig. 18, a combination of the SSN and the S is increased for one RTP sequence number.

Disclosure of the Invention

[0014] A packet retransmitting system according to this invention for transmitting a packet including a sequence number for defining a sequence of data included in each of a plurality of packets through a network and retransmitting a packet which is lost during transmission includes a transmitting equipment for transmitting the plurality of packets and a receiving equipment for receiving the plurality of packets sent by the transmitting equipment. The transmitting equipment includes a priority degree information attaching unit for defining a plurality of priority degrees indicating an importance degree of the data, producing priority degree information by using the plurality of priority degrees defined, and attaching the priority degree information produced to the packet, a transmitting unit for transmitting a plurality of packets to which the priority degree information is attached by the priority degree information attaching unit through the network, and a retransmitting unit for receiving a retransmission request for requesting to retransmit a packet from the receiving equipment after the transmitting unit transmits the plurality of packets and retransmitting the packet of which retransmission is requested in the retransmission request received. The receiving equipment includes a receiving unit for receiving the plurality of packets sent by the transmitting equipment through the network and a retransmission requesting unit for inputting the plurality of packets received by the receiving unit, extracting a plurality of sequence numbers and a plurality of priority degree information from each of the plurality of packets input, judging lost packets based on the plurality of sequence numbers extracted, detecting an important packet among the lost packets judged based on the plurality of priority degree information extracted, and transmitting the retransmission request to the transmitting equipment to request to retransmit the packet detected.

[0015] A transmitting equipment according to this invention for transmitting a packet including a sequence number for defining a sequence of data included in each of a plurality of packets through a network includes a priority degree information attaching unit for defining a plurality of priority degrees indicating an importance degree of the data, producing priority degree information by using the plurality of priority degrees defined, and attaching the priority degree information produced to the packet and a transmitting unit for transmitting the packet to which the priority degree information is attached by the priority degree information attaching unit through the network.

[0016] The priority degree information attaching unit includes a priority degree setting unit for setting an importance degree for each of the plurality of priority degrees, a priority degree memory for storing the plurality of priority degrees set by the priority degree setting unit, and a priority degree information calculating unit for producing the priority degree information by using the plurality of priority degrees stored in the priority degree memory and the sequence number included in the packet.

[0017] The priority degree setting unit defines the plurality of priority degrees hierarchically by setting an order, and the priority degree information calculating unit calculates the priority degree information by giving priority to a priority degree in a high order.

[0018] The priority degree setting unit selects a priority degree one by one from a higher order among the plurality of priority degrees, judges an importance degree of data included in the packet based on the priority degree selected, and increases a value of the priority degree selected by one and sets the value of the priority degree selected when it is judged as an important packet.

[0019] The priority degree information calculating unit produces the priority degree information by using a result of adding one of values of the plurality of priority degrees corresponding to the packet to a product of a determined value and the sequence number included in the packet.

[0020] When a number of the plurality of priority degrees is defined as PH, a value of the plurality of priority degrees is defined as PL (PH), a counter is defined as N, a sequence number included in the arbitrary packet is defined as SN,

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and a value of the priority degree information calculated for each of the plurality of priority degrees is defined as PLD (PH) for an arbitrary packet, the priority degree information calculating unit substitutes PL (0) for PLD (0) and calculates PLD (N) = the determined value × SN + PL (N) for each of N in a value of 0 < N < PH, defines PLD (PH - 1) in case of N = PH - 1 as the priority degree information PLD of the arbitrary packet, obtains the priority degree information by calculating PLD (PH - 1) for each of the plurality of packets, and calculates the plurality of priority degree information.

[0021] The priority degree information calculating unit uses a value of PLD (N - 1) as the determined value.

[0022] The priority degree information calculating unit uses one of (|PLD (N - 1) - PL (N)|) which is an absolute value of a difference between PLD (N - 1) and PL (N), (|SN - PLD (N - 1)|) which is an absolute value of a difference between SN and PLD (N - 1), and (|SN - PL (N)|) which is an absolute value of a difference between SN and PL (N) as the determined value.

[0023] The priority degree information calculating unit defines a minimum value among |PLD (N - 1) - PL (N)|, |SN - PLD (N - 1)|, |SN - PL (N)| as Q, defines an identifier for identifying which value among three values is defined as Q as PQ, defines an identifier for identifying which is larger between X and Y as PD when Q = |X - Y|, sets PQ = TYPE1, PD = 0, R = PL (N) in case of Q = |PLD (N - 1) - PL (N)| and PLD (N - 1) ≧ PL (N), sets PQ = TYPE1, PD = 1, R = PLD (N - 1) in case of Q = |PLD (N - 1) - PL (N)| and PLD (N - 1) < PL (N), sets PQ = TYPE2, PD = 0, R = PL (N) in case of Q = |SN - PLD (N - 1)| and SN ≧ PLD (N - 1), sets PQ = TYPE2, PD = 1 in case of Q = |SN - PLD (N - 1)| and SN < PLD (N - 1), and sets PQ = TYPE3, PD = 0, R = PLD (N - 1) in case of Q = |SN - PL (N)|, and calculates PLD (PH - 1). The priority degree information attaching unit attaches PLD (PH - 1), PQ and PD to the packet as the priority degree information.

[0024] The transmitting equipment further includes a retransmitting unit for receiving a retransmission request packet for requesting retransmission of a packet after transmitting the plurality of packets from the transmitting unit, retrieving a packet of which retransmission is requested in the retransmission request packet received, and retransmitting the packet retrieved.

[0025] A receiving equipment according to this invention includes a receiving unit for receiving a plurality of packets including a sequence number which defines a sequence of data included in each of the plurality of packets and priority degree information produced based on a plurality of priority degrees indicating an importance degree of data included through a network and a retransmission requesting unit for inputting the plurality of packets received by the receiving unit, extracting a plurality of sequence numbers and a plurality of priority degree information from each of the plurality of packets input, judging lost packets based on the plurality of sequence numbers extracted, detecting an important packet among the lost packets judged based on the plurality of priority degree information, and transmitting a retransmission request to request to retransmit the packet detected.

[0026] The retransmission requesting unit detects the important packet by using the importance degree indicated in each of the plurality of priority degrees included in the plurality of priority degree information.

[0027] The retransmission requesting unit includes a packet information memory for storing the plurality of sequence numbers and the plurality of priority degree information extracted, a priority degree calculating unit for calculating a value of a plurality of priority degrees by using the sequence numbers and the priority degree information stored in the packet information memory, and a lost packet detecting unit for judging a lost packet based on the plurality of sequence numbers and detecting if any important packet is lost based on the value of the plurality of priority degrees calculated by the priority degree calculating unit.

[0028] The priority degree calculating unit calculates a quotient and a remainder by dividing the priority degree information by the sequence number, and calculates a value of the plurality of priority degrees by using the quotient and the remainder calculated.

[0029] When the priority degree information is defined as PLD, the sequence number included in an arbitrary packet is defined as SN, a number of the plurality of priority degrees is defined as PH, a value of the plurality of priority degrees is defined as PL (PH), and a counter is defined as N for an arbitrary packet, the priority degree information calculating unit substitutes an initial value of N in a range of 0 ≦ N < PH for N = PH - 1, substitutes a remainder of PLD / SN for PL (N), substitutes a quotient of PLD / SN for PLD, repeats a calculation of deducting N by 1 till N reaches 0, calculates a value of the plurality of priority degrees by substituting a value of PLD for PL (0) in case of N = 0, calculates PL (PH) for each of the plurality of packets, and calculates the value of the plurality of priority degrees corresponding to the plurality of packets. The lost packet detecting unit judges if a packet with a priority degree indicated by PL (N) is lost based on a difference between values of a maximum value in PL (N) corresponding to each of the plurality of packets received and PL (N) of the arbitrary packet, and when the packet has been lost, detects the PL (N) of the packet.

[0030] The priority degree information includes priority degree data produced from the plurality of priority degrees, an identifier for indicating a type of data used for producing the priority degree data, and a flag for indicating a size of a value of the identifier for each of arbitrary packets. When the priority degree data are defined as PLD, the identifier is defined as PQ, the flag is defined as PD, a number of the plurality of priority degrees is defined as PH, a value of the plurality of priority degrees is defined as PL (PH), and a counter is defined as N for an arbitrary packet, the priority degree information calculating unit substitutes an initial value of N in a range of 0 ≦ N < PH for N = PH - 1, defines

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TYPE1, TYPE2 and TYPE 3 as types of the identifier PQ, defines that a value of the flag PD is one of 0 and 1, defines a quotient Q obtained by dividing PLD by SN as Q and a remainder as R, sets PL (N) = R and substitutes Q + R for PLD in case of PQ = TYPE1 and PD = 0, sets PL (N) = Q + R and substitutes R for PLD in case of PQ = TYPE1 and PD = 1, sets PL (N) = R and substitutes SN - Q for PLD in case of PQ = TYPE2 and PD = 0, sets PL (N) = R and substitutes Q + SN for PLD in case of PQ = TYPE2 and PD = 1, sets PL (N) = SN - Q and substitutes R for PLD in case of PQ = TYPE3, repeats a calculation of deducting N by 1 from N = PH - 1 to N = 1, calculates PL from PL (0) to PL (PH - 1) by substituting PLD for PL (0) in case of N = 1. The lost packet detecting unit judges if an important packet in the priority degree N is lost based on a difference between values of a maximum value of PL (N) of a packet and PL (N) of an arbitrary packet among the plurality of packets received by the receiving unit and detects the PL (N) of the packet lost when the packet has been lost.

[0031] The retransmission requesting unit further includes a retransmission request selecting unit for selecting a particular priority degree among the plurality of priority degrees. The lost packet detecting unit detects loss of a packet based on the particular priority degree selected by the retransmission request selecting unit.

[0032] A packet retransmitting method according to this invention for transmitting a packet including a sequence number for defining a sequence of data included in each of a plurality of packets from a transmitter to a receiver through a network and retransmitting a packet which is lost during transmission includes, in the transmitter, defining a plurality of priority degrees indicating an importance degree of data, producing priority degree information by using the plurality of priority degrees defined, attaching the priority degree information produced to the packet, repeating producing the priority degree information and attaching the priority degree information to each of the plurality of packets, and transmitting the plurality of packets to which the priority degree information is attached to the receiver through the network, and in the receiver, receiving the plurality of packets through the network, extracting a plurality of sequence numbers and a plurality of priority degree information from each of the plurality of packets received, judging lost packets based on the plurality of sequence extracted, detecting an important packet among the lost packets judged based on the plurality of priority degree information extracted, and transmitting a retransmission request to the transmitter to request to retransmit the packet detected.

[0033] A packet transmitting method according to this invention for transmitting a packet including a sequence number for defining a sequence of data included in each of a plurality of packets through a network includes defining a plurality of priority degrees indicating an importance degree of the data, producing priority degree information by using the plurality of priority degrees defined, attaching the priority degree information produced to the packet, and transmitting the packet to which the priority degree information is attached through the network.

[0034] The step of defining the priority degrees includes defining the plurality of priority degrees hierarchically by setting an order, selecting a priority degree from a higher priority degree among the plurality of priority degrees, judging an importance degree in the selected priority degree, and adding one to a value of the selected priority degree when it is judged as an important packet. The step of producing the priority degrees information includes producing the priority degree information by using a result of adding a value of one of the plurality of priority degrees corresponding to the packet to a product of a determined value and a sequence number included in the packet.

[0035] The step of defining the priority degrees includes setting values of the plurality of priority degrees corresponding to the plurality of packets by setting a value of the plurality of priority degrees repeatedly for the plurality of packets. The step of producing the priority degree information includes producing the priority degree information corresponding to each of the plurality of packets by producing the priority degree information repeatedly for the plurality of packets.

[0036] A packet receiving method according to this invention includes receiving a plurality of packets including a sequence number for defining a sequence of data included in each of the plurality of packets and priority degree information produced based on a plurality of priority degrees indicating an importance degree of data stored in each of the plurality of packets through a network, extracting a plurality of sequence numbers and a plurality of priority degree information from the plurality of packets received, judging lost packets based on the plurality of sequence numbers extracted, detecting an important packet based on the plurality of priority degree information extracted among the packets judged as the lost packets, and transmitting a retransmission request for requesting to retransmit the packet detected.

Brief Description of the Drawings

[0037]

Fig. 1 illustrates an example of a configuration of a packet retransmitting system according to this invention;
Fig. 2 illustrates an example of priority degree information and a plurality of priority degrees;
Fig. 3 illustrates an example of a retransmission request and a method for detecting a retransmission packet;
Fig. 4 shows a flow chart of an example of operations by a transmitter in Embodiment 1;
Fig. 5 shows a flow chart of an example of operations by a receiver in Embodiment 1;

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Fig. 6 illustrates an example of a configuration of a RTP packet header in Embodiment 1;
Fig. 7 illustrates an example of a configuration of a RTCP for requesting the retransmission in Embodiment 1;
Fig. 8 shows an example of operations for requesting the retransmission in case of PH = 2 in Embodiment 1;
Fig. 9 shows a flow chart for explaining an example of the operations by the transmitter in Embodiment 2;
Fig. 10 shows a flow chart for explaining an example of a process of subroutine 1 in Embodiment 2;
Fig. 11 shows a flow chart for explaining an example of operations by the receiver in Embodiment 2;
Fig. 12 shows a flow chart for explaining an example of a process of subroutine 2 in Embodiment 2;
Fig. 13 illustrates an example of a configuration of the RTP packet header in Embodiment 2;
Fig. 14 illustrates an example of a configuration of the RTCP for requesting the retransmission in Embodiment 2;
Fig. 15 shows an example of operations for requesting the retransmission in case of PH = 2 in Embodiment 2;
Fig. 16 illustrates an example of the RTP packet header according to the related art;
Fig. 17 illustrates an example of a configuration of the RTCP packet for requesting the retransmission according to the related art; and
Fig. 18 shows an example of a second sequence number SSN and operations for requesting the retransmission according to the related art.

Best Mode for Carrying out the Invention

[0038] Fig. 1 illustrates an example of a configuration of a packet retransmitting system according to this invention.

[0039] In the specifications, a packet is a packet including a sequence number. In explanation of the following embodiments, the RTP packet is used as an example of the packet including the sequence number. However, the packet is not limited to the RTP packet. The packet retransmitting system according to this invention can be applied to any packet including the sequence number. Further, it is also possible that a packet includes a packet header and the packet header includes a sequence number which defines an arrangement sequence of data included in the packet.

[0040] In the following explanation, an example of including the packet header is explained.

[0041] In the following explanation, a priority degree is a value indicating an importance degree of data included in an arbitrary packet. In this packet retransmitting system, a plurality of priority degrees is set for the arbitrary packet. The plurality of priority degrees is hierarchical, and a priority order is set among the plurality of priority degrees. Priority degree information is information indicating a priority degree of a packet generated based on the plurality of priority degrees. The priority degree information is produced based on the plurality of priority degrees by the transmitter. The receiver receives the priority degree information, and calculates the plurality of priority degrees of the packet based on the received priority degree information.

[0042] In the following, the configuration of the packet retransmitting system illustrated in Fig. 1 as an example is explained.

[0043] The packet retransmitting system in Fig. 1 includes a transmitting equipment 110, a network 120 and a receiving equipment 130.

[0044] The network 120 can be either wireless or wired, and it can be any communication network as far as the packet can be transmitted in the network.

[0045] The transmitting equipment 110 includes a transmitting unit 111, a transmitting data memory 112, a priority degree information attaching unit 113 and a retransmitting unit 119.

[0046] The transmitting unit 111 transmits a packet at a specified time.

[0047] The transmitting data memory 112 stores a plurality of packets sent by the transmitting unit 111.

[0048] The priority degree information attaching unit 113 defines a plurality of priority degrees. The priority degree information attaching unit 113 sets an importance degree of each of the plurality of priority degrees defined, produces priority degree information by using the plurality of priority degrees, and attaches the produced priority degree information to the packet header included in the packet. The priority degree information attaching unit 113 sets the importance degree, produces the priority degree information, and attaches the priority degree information to the packet header for each of a plurality of packets which are sent.

[0049] After the transmitting equipment 110 transmits the plurality of packets, the retransmitting unit 119 receives a retransmission request packet for requesting retransmission of a packet, retrieves a packet of which retransmission is requested in the received retransmission request packet, and retransmits the retrieved packet.

[0050] The priority degree information attaching unit 113 includes a priority degree setting unit 114, a priority degree information calculating unit 115, a priority degree information attachment processing unit 116, a set priority degree memory 117, and a priority degree information memory 118.

[0051] The priority degree setting unit 114 sets the importance degree (value of the priority degree) for each of the plurality of priority degrees.

[0052] The set priority degree memory 117 stores the plurality of priority degrees set by the priority degree setting unit 114.

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[0053] The priority degree information calculating unit 115 produces the priority degree information by using the plurality of priority degrees stored in the set priority degree memory 117 and the sequence number included in the packet header.

[0054] The priority degree information memory 118 stores the priority degree information produced by the priority degree information calculating unit 115.

[0055] The priority degree information attachment processing unit 116 attaches the priority degree information produced by the priority degree information calculating unit 115 and stored in the priority degree information memory 118 to the packet header included in the packet.

[0056] It is also possible that the set priority degree memory 117 uses a storage area in the priority degree setting unit 114 and outputs the plurality of priority degrees set by the priority degree setting unit 114 to the priority degree information calculating unit 115 directly. Further, it is also possible that the priority degree information memory 118 uses a storage area in the priority degree information calculating unit 115, uses the storage area in the priority degree information calculating unit 115 and outputs the priority degree information produced by the priority degree information calculating unit 115 to the priority degree information attachment processing unit 116 directly. Further, the set priority degree memory 117 and the priority degree information memory 118 can be realized as one memory.

[0057] Next, the receiving equipment 130 is explained.

[0058] The receiving equipment 130 includes a receiving unit 131, a receiving data memory 132 and a retransmission requesting unit 133.

[0059] The receiving unit 131 receives the plurality of packets sent from the transmitting equipment 110 through the network 120.

[0060] The receiving data memory 132 stores the packets received by the receiving unit 131.

[0061] The retransmission requesting unit 133 inputs the plurality of packets received by the receiver 131, extracts a plurality of sequence numbers and a plurality of priority degree information from packet headers included in the plurality of input packets respectively, judges lost packets based on the plurality of extracted sequence numbers, detects an important packet among the lost packets based on the plurality of priority degree information, and requests retransmission of the detected packet.

[0062] The retransmission requesting unit 133 includes a packet information extracting unit 134, a priority degree calculating unit 135, a lost packet detecting unit 136, a retransmission request selecting unit 137, a packet information memory 138, a calculated priority degree memory 139, a retransmission request list memory 140 and a retransmission packet transmitting unit 141.

[0063] The packet information extracting unit 134 reads the plurality of packets received by the receiving unit 131 and stored in the receiving data memory 132, and extracts the plurality of sequence numbers and the plurality of priority degree information from the packet headers included in the plurality of read packets respectively.

[0064] The packet information memory 138 stores the plurality of sequence numbers and the plurality of priority degree information extracted by the packet information extracting unit 134.

[0065] The priority degree calculating unit 135 calculates a plurality of priority degrees from the sequence numbers and the priority degree information stored in the packet information memory 138.

[0066] The calculated priority degree memory 139 stores the plurality of priority degrees calculated by the priority degree calculating unit 135.

[0067] The lost packet detecting unit 136 reads the plurality of priority degree information calculated by the priority degree calculating unit 135 and stored in the calculated priority degree memory 139, detects the lost packets based on the plurality of sequence numbers, judges if any important packet is lost for each of the plurality of priority degrees based on the plurality of priority degrees calculated by the priority degree calculating unit, and detects loss of the important packet. The lost packet detecting unit 136 treats the detected packet as the retransmission request packet for requesting the retransmission and creates a retransmission request list.

[0068] The retransmission request selecting unit 137 selects a particular priority degree among the plurality of priority degrees, and notifies the lost packet detecting unit 136 of the selected priority degree.

[0069] The retransmission request list memory 140 stores the retransmission request list created by the lost packet detecting unit 136.

[0070] The retransmission packet transmitting unit 141 transmits the retransmission request packet to the transmitting equipment 110 based on the retransmission request list stored in the retransmission request list memory 140.

[0071] Further, it is also possible that the calculated priority degree memory 139 uses a storage area in the priority degree calculating unit 135 and outputs the plurality of priority degrees calculated by the priority degree calculating unit 135 to the lost packet detecting unit 136 directly. It is also possible that the packet information memory 138, the calculated priority degree memory 139 and the retransmission request list memory 140 are configured either as one memory or a plurality of memories.

[0072] With reference to Fig. 2, an example of a configuration of the RTP sequence numbers and the priority degrees in the packet retransmitting system including the plurality of priority degrees is explained.

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[0073] In Fig. 2, 402 is stored in the priority degree information memory 118, and 403 ~ 407 are stored in the set priority degree memory 117.

[0074] A number of the priority degrees is set as priority degree hierarchy (PH). A priority degree in an arbitrary priority degree hierarchy (PH) is set as a priority degree N, and a sequence number (value indicating an importance degree) of the priority degree N is set as PL (N). A range of N is $0 \leqq N \leqq PH - 1$. When N is smaller, the priority degree is higher. Stated setting is performed by the priority degree setting unit 114.

[0075] For example, an important packet to be retransmitted identified by PL (0) has a higher priority degree than an important packet to be retransmitted identified by other PL (1) ~ PL (PH - 1).

[0076] Further, the RTP sequence number (first sequence number) of each of the packets is set as SN, and priority degree data included in the priority degree information is set as PLD. The plurality of packets are indicated as packet i (i = 0, 1, 2, ···, k, ···). PLD, PL (N) and SN of the i-th packet are set as PLDi, PLi (N) and SNi respectively.

[0077] The PL (N) is same as a case when there is a plurality of second sequence numbers SSN's defined in the Internet draft titled "RTP Payload Type Format to Enable Multiple Selective Retransmissions" according to the related art. The PL (N) is a sequence number increased by one for each of important packets to be retransmitted in the priority degree N, and it is a value indicating an importance degree of the priority degree N. The important packet to be retransmitted is the packet which should be transferred again when the packet transferred from the transmitter to the receiver is lost. Therefore, if the PL (N) of the RTP packet received now by the receiver is larger than the PL (N) of a packet received previously by one, the packet received now can be identified as the important packet to be retransmitted in the priority degree N.

[0078] Further, in the packet retransmitting system according to this invention, even when the plurality of priority degrees (PH > 1) is provided for the RTP, the transmitter can attach one of PLD to the packet header instead of attaching N number of PL's to the packet header as in the system according to the related art. The receiver can recognizes values of the plurality of priority degrees (importance degrees) (PL) by the one of PLD attached, and request retransmission only for a priority degree N (hierarchy of priority degrees) which is appropriate for a network condition. For example, when a network condition is bad, a band necessary for the retransmission should be reduced. Therefore, the retransmission is requested only for (P_Level - 1) number of the priority degrees, i.e., N=0, 1, 2, , P_Level (P_Level < PH- 1), which are higher priority degrees, instead of all the priority degrees ($0 \leq N \leqq PH - 1$). Further, when all the priority degrees are used, P_Level is PH - 1.

[0079] Further, it is assumed that the important packets to be retransmitted do not exist simultaneously in the plurality of priority degrees. When the packet of PLi (N) is the important packet to be retransmitted (i.e., PLi (N) is increased by one from the PLi - 1 (N)), there is no important packet to be retransmitted in the priority degrees higher than N.

[0080] In an upper part of Fig. 3, an example of the plurality of priority degrees stored in the set priority degree memory 117 and a process for detecting the retransmission packet is illustrated. For example, in Fig. 3, in a priority degree 0, PL (0) is increase by one from 3 to 4 for a packet of sequence number 6. This shows that the packet of sequence number 6 is the important packet to be retransmitted in the priority degree 0. In this case, in a priority degree 1, PL (1) is not increased. Therefore, it is not the important packet to be retransmitted in the priority degree 1. Further, when a packet is an important packet to be retransmitted in a priority degree N, the priority degree N is set as a priority degree display S (S = N), S for the packet i (i = 0, 1, 2, ··· , k ···) is set as Si. An initial value of Si is -1. This shows that the packet i with Si = -1 is not the important packet to be retransmitted in all the priority degrees.

[0081] The packet retransmitting system according to this invention can be also adapted to a transmission protocol including the sequence number besides the RTP packet.

[0082] In the following, the priority degree is explained.

[0083] The priority degree setting unit 114 defines the plurality of priority degrees hierarchically by setting an order.

[0084] Further, the priority degree setting unit 114 selects a priority degree from a higher order sequentially among the plurality of priority degrees for a packet, and judges an importance degree of the packet concerning on the selected priority degree. If it is judged that the packet is an important packet, one is added to a value of the selected priority degree. This is repeated for each of the plurality of priority degrees, and values of the plurality of priority degrees are set. The priority degree setting unit 114 repeatedly sets the values of the plurality of priority degrees as stated for each of the plurality of packets which are sent, and sets the values of the plurality of priority degrees corresponding to each of the plurality of packets.

[0085] Next, the priority degree information is explained.

[0086] A procedure of calculating PLD for an arbitrary packet by the priority degree information calculating unit 115 is explained when a number of the plurality of priority degrees is defined as PH, a value of the plurality of priority degrees is defined as PL (PH), a counter is defined as N, a sequence number included in a packet header of the arbitrary packet is defined as SN, and the priority degree data calculated for each of the plurality of priority degrees are defined as PLD (PH).

[0087] The priority degree information calculating unit 115 substitutes PL (0) for PLD (0), and calculates PLD (N) = determined value × SN + PL (N) for each of N in a value of $0 < N < PH$. PLD (PH - 1) in case of N = PH - 1 is set as

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the priority degree data PLD of the arbitrary packet.

[0088] In Embodiment 1, a case of using a value of PLD (N - 1) as the determined value is explained.

[0089] In Embodiment 2, as the determined value, a minimum value among (|PLD (N - 1) - PL (N)|) which is an absolute value of a difference between PLD (N - 1) and PL (N), (|SN - PLD (N - 1)|) which is an absolute value of a difference between SN and PLD (N - 1), and (|SN - PL (N)|) which is an absolute value of a difference between SN and PL (N) is used.

[0090] In the following, a case in which the priority degree data PLD are included in the priority degree information is explained. In Embodiment 2, a case in which other data, e.g., identifier, etc. are included in the priority degree information in addition to the priority degree data PLD is explained. Further, in the following explanation, the priority degree data can be also called as the priority degree information unless clearly stated.

[0091] In the following, actual operations by the transmitter and the receiver are explained.

Embodiment 1.

[0092] In this embodiment, an example in case of PH = 2 is explained.

[0093] Fig. 4 shows a flow chart of an example of the operations by the transmitter in Embodiment 1. Fig. 5 shows a flow chart of an example of the operations by the receiver in Embodiment 1.

[0094] This shows a sequence of a packet which is being processed among packets to be sent.

[0095] The transmitter calculates PLDi (PLD of the i-th packet) from the packet with i = 0, and transmits the packet. At first, when the transmitter receives the retransmission request packet (Yes in 603), the retransmitting unit 119 retransmits the packet of which retransmission is requested (604). In the retransmission request packet, PL of each of priority degrees, which is desired to be retransmitted, is written. For example, information of requesting a packet with PL (0) = 5, 6 and PL (1) = 4 is written in the retransmission request packet. The retransmission request packet can be in any configuration as far as the PL for requesting the retransmission is written. Fig. 7 (802) illustrates an example of the RTCP packet for requesting the retransmission with PH = 2. However, since there is a possibility that there are a plurality of packets with an equal PL, the retransmitting unit 119 is not able to identify the important packet to be retransmitted only by the PL. Therefore, the retransmitting unit 119 retrieves a sequence number of the packet of which retransmission is requested based on two values of the PL and the priority degree display S of each of the packets. A priority degree display Si of a packet shows that packet i is an important packet to be retransmitted in the priority degree display Si.

[0096] A lower part of Fig. 3 illustrates an example of detecting the retransmission packet based on the retransmission request packet by the retransmitting unit 119 in the transmitter.

[0097] In this example, the retransmission request packet requests retransmission of a packet with PL (0) = 5, 6 and PL (1) = 4 (506). In this case, the retransmitting unit 119 detects a packet of sequence number 13 (508) with PL (0) = 5 and S = 0, a packet of sequence number 14 (509) with PL (0) = 6 and S = 0, and a packet of sequence number 12 (507) with PL (1) = 4 and S = 1 as packets to be retransmitted.

[0098] When the retransmission request packet is not received (No in 603), the priority degree setting unit 114 calculates all PL's of the packet i. The priority degree setting unit 114 calculates PL's from the priority degree 0 in a higher order to priority degree PH - 1 sequentially among the plurality of priority degrees. An order among the plurality of priority degrees is indicated as j, and j is a value in a range of $0 \leqq j < PH$. An initial value of j is 0. S indicates a timing when 1 is added to the PL, and an initial value of S is -1 (605).

[0099] If the packet i is an important packet to be retransmitted in the priority degree j (606), the priority degree setting unit 114 adds one to PLi (j), and sets Si = j (607). If the packet i is important in a priority degree in a certain order, the packet i is not important in a priority degree in another order. Therefore, remaining PLi is set to be equal to PLi - 1 (608). When the packet i is not important in the priority degree j (606), the priority degree setting unit 114 sets PLi (j) = PLi - 1 (j) (610), and the processing goes to a priority degree in a next order (j++) (611).

[0100] The priority degree setting unit 114 performs this processing for all of the plurality of priority degrees, and calculates all of PLi (j) corresponding to the packet i. The priority degree setting unit 114 repeats steps of 606 ~ 612 PH times. The PL set by the priority degree setting unit 114 is stored in the set priority degree memory 117.

[0101] Then, the priority degree information calculating unit 115 calculates PLDi from PLi. A general equation for obtaining the PLDi is as follows:

$$PLDi\ (0) = PLi\ (0) \quad (614)$$

$$PLDi\ (j) = PLDi\ (j - 1) \times SNi + PLi\ (j)$$

$$1 \leqq j \leqq PH - 1 \quad (615, 616, 617)$$

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[0102] The priority degree information calculating unit 115 obtains PLDi = PLDi-(PH - 1) in calculating by using this general equation.

[0103] The priority degree information attachment processing unit 116 attaches the PLDi calculated in this way and the Si to the packet header, and transmits at a time of time stamp of the packet i.

[0104] Fig. 6 (801) illustrates an example of attaching the PLDI and Si to the RTP header.

[0105] As a configuration of the packet header, as far as PLDi and Si are attached, another configuration besides the configuration of Fig. 6 (801) is possible.

[0106] Then, i is incremented, and a same processing is repeated for a next packet. The same processing is performed for all of the plurality of transmitting packets.

[0107] With reference to Fig. 5, the operations by the receiver are explained.

[0108] In the receiver, the priority degree information attaching unit 113 obtains priority degree hierarchy PH of the packet which is sent to the receiver (702). As a method for obtaining, there is a method for notifying a value of PH from the transmitter in advance before starting transmission of the packet.

[0109] When the priority degree information attaching unit 113 receives the packet (704), the packet information extracting unit 134 extracts the sequence number SN, priority degree display S, and priority degree data PLD as the priority degree information from the received packet (705). The extracted sequence number SN, priority degree display S, and priority degree data PLD are stored in the packet information memory 138.

[0110] Then, the priority degree calculating unit 135 calculates each PL from the PLD.

[0111] At first, the priority degree calculating unit 135 sets j = PH - 1 (706). Then, the priority degree calculating unit 135 substitutes a quotient obtained by dividing PLD with SN for the PLD, and substitutes a remainder for PL (j) (707). The priority degree calculating unit 135 reduces j by one sequentially, and performs the same processing. Accordingly, all the PL's can be obtained (708, 709). The priority degree calculating unit 135 stores the calculated PL's in the calculated priority degree memory 139.

[0112] Then, the retransmission request selecting unit 137 selects a priority degree level P_Level ($0 \leqq$ P_Level $\leqq$ PH -1) showing a range of orders of the priority degrees for requesting retransmission, and notifies the lost packet detecting unit 136 (711). The priority degree level P_Level is indicated in an order of the priority degree. For example, when a network condition is bad, a value becomes lower (a priority degree in a higher order is used). When the network condition is good, the value becomes higher (a priority degree in a lower order is used). The priority degree level P_Level does not only depend on the network condition. The priority degree can be set freely. P_Level = PH - 1 is a value when all the priority degrees are used.

[0113] Then, the lost packet detecting unit 136 detects loss of an important packet to be retransmitted. Since detection is started from the priority degree 0 which is the highest order, the priority degree j = 0 (712). If j is larger than the priority degree level P_Level (713), the lost packet detecting unit 136 requests to retransmit the important packet to be retransmitted which is lost in the priority degree j (721).

[0114] When a value of deducting PL (j)_MAX (a maximum value of PL (j) among the packets which have been received) from PL (j) is 0, the lost packet detecting unit 136 judges that there is a possibility that a packet is lost, however the important packet to be retransmitted is not lost in the priority degree j. Therefore, the lost packet detecting unit 136 does not detect packet loss, and goes to a processing for a next priority degree. However, when a value of deducting PL(j)_MAX from PL (j) is larger than 0 (714), the lost packet detecting unit 136 can judge that there is a possibility that the important packet to be retransmitted is lost in the priority degree j.

[0115] In this case, if S is equal to j (715), a packet which is received now is the important packet to be retransmitted in the priority degree j. Therefore, the lost packet detecting unit 136 can know that the packet of PL (j) is not lost. In this case, if a value of deducting PL (j)_MAX from PL (j) is 1 (717), the important packet to be retransmitted is not lost in the priority degree j. Therefore, the lost packet detecting unit 136 substitutes PL (j) for PL (j)_MAX (719). However, if the value of deducting PL (j)_MAX from PL (j) is larger than one (717), PL from PL (j)_MAX to PL (j) - 1 is lost. Therefore, the lost packet detecting unit 136 adds the lost PL to the retransmission request list (j) (718).

[0116] Similarly, when S is not equal to j (715), PL from PL (j)_MAX to PL (j) is lost. Therefore, the lost packet detecting unit 136 adds the lost PL to the retransmission request list (j) (716).

[0117] Then, by setting PL (j)_MAX = PL (j), j++ (719, 720), processing is continued for a next priority degree.

[0118] When j is larger than the priority degree level P_Level (713), i.e., the priority degree for checking the loss exceeds the priority degree level, the lost packet detecting unit 136 instructs the retransmission packet transmitting unit 141 to request the transmitter to retransmit the PL maintained in the retransmission request list (721). The retransmission packet transmitting unit 141 transmits the retransmission request packet to the transmitter. Then, the lost packet detecting unit 136 clears the retransmission request list (722). In the receiving equipment 130, when the packet is continued to be received, the receiving unit 131 receives a new packet, and the retransmission requesting unit 133 performs a similar processing (719). When there is no PL maintained in the retransmission request list, the retransmission is not requested.

[0119] Fig. 8 illustrates an example of identification of PL (N) by the receiver and the retransmission request in case

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of PH = 2 in this embodiment.

[0120] In Fig. 8, 901 ~ 905 show that sequence numbers (PL (0) (902) and PL (1) (904)) in two priority degrees must be attached to the packet header when two priority degrees are set in a system according to the related art. 906 ~ 908 show an example in which priority degree data PLD (907) are attached to the packet header as one of the priority degree information when two priority degrees are set in the packet retransmitting system of this embodiment.

[0121] With reference to Fig. 8, a method for requesting retransmission of a lost packet based on the processing by the receiver of this embodiment is explained.

[0122] We assume that packets of sequence numbers 11 - 14 are lost. Since the PLD of sequence number 10 is 43, PL_{10} (0) is a quotient obtained by dividing 43 by 10, and PL_{10} (1) is a remainder obtained by dividing 43 by 10. Therefore, PL_{10} (0) = 4, PL_{10} (1) = 3 (909). Similarly, since the PLD of sequence number 15 is 94, PL_{15} (0) is a quotient obtained by dividing 94 by 15, and PL_{15} (1) is a remainder obtained by dividing 94 by 15. Therefore, PL_{15} (0) = 6, PL_{15} (1) = 4 (910). Further, since the priority degree display S of sequence number 15 is -1, the packet of sequence number 15 is not an important packet to be retransmitted in the priority degree 0 and the priority degree 1. Accordingly, the lost packet detecting unit 136 detects that PL_{10} (0) - PL_{15} (0), i.e., PL (0) of 5 and 6, are lost in the priority degree 0, and PL_{10} (1) - PL_{15} (1), i.e., PL (1) of 4, are lost in the priority degree 1 (911). The retransmission packet transmitting unit 141 transmits a retransmission request packet for requesting to retransmit these PL's to the transmitter (912).

[0123] When a value of the priority degree data PLD becomes larger, it becomes impossible to display the value in a register allocated to the PLD. In such a case, a plurality of priority degrees are initialized, and the priority degrees are set again.

[0124] Further, each of elements in the transmitting equipment 110 and the receiving equipment 130 illustrated in Fig. 1 can be realized as any one of hardware, firmware, and software.

Embodiment 2.

[0125] In Embodiment 2, a case of calculating the priority degree data so that the value of the PLD becomes smaller than Embodiment 1 is explained.

[0126] In the receiver, the priority degree data PLD are treated as PLD = SN × Q + R. Q is a quotient of PLD /SN, and R is a remainder of 3. Values of Q and R are also set smaller for each of the packets.

[0127] In the following explanation, explanations are made by using an equation of PLD = SN × Q + R.

[0128] At first, setting of the value of Q is explained. Variables A, B and C calculated in the following equation are defined.

[0129] A = |PLD(N - 1) - PL(N)|, B = |SN - PLD (N - 1)|, C= |SN - PL (N)|, and a minimum value among A, B and C is defined as Q. Further, an identifier PQ for identifying which value among three values is defined as Q; and displayed in 2 bits for example.

[0130] In case of Q = PL (0), i.e., same as Embodiment 1, PQ = 00.

[0131] In case of Q = A, PQ = 01.

[0132] In case of Q = B, PQ = 10.

[0133] In case of Q = C, PQ = 11.

[0134] Further, since A, B and C are absolute values of difference between two values, indicated as | X - Y|, an identifier (flag) PD for indicating which one of X and Y is larger is defined, and displayed in 1 bit length as follows:

[0135] In case of $X \geqq Y$, PD = 0.

[0136] In case of X < Y, PD = 0.

[0137] In this embodiment, a case in which the priority degree information includes the priority degree data PLD, the identifier PQ and the identifier (flag) PD is explained.

[0138] Fig. 9 and Fig. 10 are flow charts of the transmitter in Embodiment 2 of this retransmitting system. Fig. 11 and Fig. 12 are flow charts of the receiver.

[0139] The transmitting equipment 110 in the transmitter calculates PLDi from the packet of i = 0, and transmits the packet. At first, when the transmitter receives the retransmission request packet (Yes in 1003), the retransmitting unit 119 retransmits the packet of which retransmission is requested (1004). In the retransmission request packet, PL of each of the priority degrees desired to be retransmitted is written. The retransmission request packet and the retransmission packet are retrieved in a same method with Embodiment 1.

[0140] Next, the priority degree setting unit 114 calculates all of PL's of the packet i. The priority degree setting unit 114 calculates the PL's from the priority degree 0 in a higher order to priority degree PH - 1 sequentially among the plurality of priority degrees. A method for calculating the PL's is same as Embodiment 1.

[0141] Next, the priority degree information calculating unit 115 calculates PLDi by using PLi. The priority degree information calculating unit 115 calculates by using the equation (PLD = Q × SN + R) explained in the above. In Embodiment 2, the priority degree information calculating unit 115 sets the values of Q and R smaller so that the value of the PLD becomes further smaller.

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[0142] An order among the plurality of priority degrees is indicated as j, and j is a value in a range of $1 \leqq j < PH - 1$. A general equation for obtaining the PLDi is as follows:

$$PLDi\ (0) = PLi\ (0) \quad (1014)$$

$$PLDi\ (j) = |PLDi\ (j - 1) - PLi\ (j)| \times SNi + PLi\ (j) \quad \text{equation 1 (1107)}$$

$$PLDi\ (j) = |PLDi\ (j - 1) - PLi\ (j)| \times SNi + PLi\ (j - 1) \quad \text{equation 2 (1109)}$$

$$PLDi\ (j) = |SNi - PLDi\ (j - 1)| \times SNi + PLi\ (j) \quad \text{equation 3 (1113)}$$

$$PLDi\ (j) = |SNi - PLi\ (j)| \times SNi + PLDi\ (j - 1) \quad \text{equation 4 (1117)}$$

$$1 \leqq j \leqq PH - 1$$

[0143] The priority degree information calculating unit 115 selects an equation to get a smaller PLDi (j) for each of the priority degrees j among equations 1 - 4 for obtaining PLDi. From this general equation, it can be obtained by PLDi = PLDi (PH - 1).

[0144] Therefore, the priority degree information calculating unit 115 sets PLDi (0) = PLi (0) as an initial value (1014). PLDi (0) is for the priority degree 0. Next, the priority degree information calculating unit 115 obtains the PLDi by applying each of the priority degrees to equations 1 - 4 from the priority degree 1. The priority degree information calculating unit 115 sets the priority degree j to 1 (1015).

[0145] Next, the priority degree information calculating unit 115 calculates the PLD by using the subroutine 1 (1016). At first, a judgement is made on if X is calculated or X is used without calculation as in Embodiment 1 (1102). The priority degree information calculating unit 115 selects a minimum value among three values of |PLDi (j - 1) - PLi (j)|, |SNi - PLDi (j - 1)|, and |SNi - PLi (j)| corresponding to quotients (Q) of equations 1 - 4 (1103). The selected value is defined as Q, and an identifier for identifying the value of Q is defined as PQ as stated earlier.

[0146] Further, in case of PQ = 01 (1104), a judgement is made on which value is larger between PLDi (j - 1) and PLi (j). The identifier for identifying is defined as PD as stated earlier. Therefore, PD is as follows:

$$\text{In case of } PLDi\ (j - 1) \geqq PLi\ (j),\ PD = 0 \quad (1106)$$

$$\text{In case of } PLDi\ (j - 1) < PLi\ (j),\ PD = 1 \quad (1108)$$

[0147] Similarly, in case of PQ = 10 (1110), a judgement is made on which is a larger value between SNi and PLDi (j - 1). PD is as follows:

$$\text{In case of } SNi \geqq PLDi\ (j - 1),\ PD = 0 \quad (1112).$$

$$\text{In case of } SNi < PLDi\ (j - 1),\ PD = 1 \quad (1114).$$

[0148] In case of PQ = 11 (1115), always $Sni \geqq PLi\ (j)$. Therefore, PD = 0 (1116).

[0149] In case of PQ = 01, PD = 0, equation 1 is selected. In case of PQ = 01, PD = 1, equation 2 is selected. In case of PQ = 10, equation 3 is selected. In case of PQ = 11, equation 4 is selected, and the PLDi is obtained.

[0150] When the PLDi is obtained in a method for using X without calculation as in Embodiment 1 (No in 1102), PQ = 00, PD = 0 (1118, 1119). The PLDi is obtained by using an equation of $PLDi\ (j) = PLDi\ (j - 1) \times Sni + PLi\ (j)$ (1120). In this way, the PLD is calculated through a procedure of the subroutine 1 (1016).

[0151] Next, the PQ and PD are bit-shifted (1017), the priority degree j is incremented (j + 1) (1018), and PLDi (j) in

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a next priority degree is obtained. In a range with j smaller than PH, this processing is repeated (1019). A last PLDi (PH - 1) is a PLDi corresponding to the packet i.

[0152] The priority degree information attachment processing unit 116 attaches the Si, PLDi, PQ and PD calculated in this way to the header. The transmitting unit 111 transmits at a time of a time stamp included in the packet header of the packet i (1020).

[0153] Fig. 13 (1402) illustrates an example of attaching the PLDi and Si to the RTP header.

[0154] A configuration of the header is not limited to a configuration of Fig. 13 (1402). As far as the Si, PLDi, PQ and PD are attached, another configuration is possible.

[0155] Next, i is incremented (i++), and a similar processing if performed for a next packet (1021, 1022).

[0156] Next, with reference to Fig. 11 and Fig. 12, operations of the receiver are explained.

[0157] In the receiver, the retransmission requesting unit 133 obtains a priority degree hierarchy PH of a packet which is sent (1202). As a method for obtaining, there is a method for informing of a value of the PH from the transmitter in advance before starting transmission of the packet for example.

[0158] When the receiving unit 131 receives the packet (1204), the packet information extracting unit 134 extracts the sequence number SN, priority degree display S, identifier PQ, identifier PD and priority degree data PLD from the packet header of the received packet (1205). The extracted sequence number SN, priority degree display S, identifier PQ, identifier PD and priority degree data PLD are stored in the packet information memory 138.

[0159] Next, the priority degree calculating unit 135 calculates each of PL's from the PLD. At first, the priority degree calculating unit 135 sets j = PH - 1, substitutes a quotient obtained by dividing PLD (j) by SN for Q (j), and substitutes a remainder for R (j) (1305). Then, the priority degree calculating unit 135 calculates all PL's from the PLD, PQ and PD through a procedure of subroutine 2 (Fig. 12) (1206). Then, PQ of the priority degree j is substituted for PQ (j), the PQ is bit-shifted and PQ (j) is obtained (1304).

[0160] Next, the priority degree calculating unit 135 obtains PL (j) through a following processing.

[0161] In case of PQ (j) = 01 and PD (j) = 0, PL (j) = R, and PLD (j - 1) = Q + R (1308, 1309).

[0162] In case of PQ (j) = 01 and PD (j) = 1, PL (j) = Q + R, and PLD (j - 1) = R (1310, 1311).

[0163] In case of PQ (j) = 10 and PD (j) = 0, PL (j) = R, and PLD (j - 1) = SN - Q (1313, 1314).

[0164] In case of PQ (j) = 10 and PD (j) = 1, PL (j) = R, and PLD (j - 1) = Q + SN (1315, 1316).

[0165] In case of PQ (j) = 11, PL (j) = SN - Q, and PLD (j - 1) = R (1317, 1318).

[0166] In case of PQ (j) = 00, PL (j) = R, and PLD (j - 1) = Q (1319, 1320).

[0167] By reducing j one by one and performing this processing (1322), all PL's can be obtained. In case of j = 0, PD (0) = PLD (0) (1323). The priority degree calculating unit 135 stores the priority degrees PL calculated in the above procedure in the calculated priority degree memory 139.

[0168] Next, the retransmission request selecting unit 137 selects a priority degree level P_Level indicating a range of orders of the priority degrees for requesting the retransmission, and informs the lost packet detecting unit 136 (1209). The priority degree level P_Level is same as the one explained in Embodiment 1.

[0169] Next, the lost packet detecting unit 136 detects loss of an important packet to be retransmitted. The retransmission packet transmitting unit 141 requests retransmission of the detected packet. A method for detecting the loss of the packet and requesting the retransmission is same as Embodiment 1.

[0170] Fig. 15 illustrates an example of identification of PL (N) by the receiver and the retransmission request in case of PH = 2 in this embodiment.

[0171] In Fig. 15, 1501 - 1505 show that two sequence numbers (PL (0) (1502) and PL (1) (1504)) of the priority degrees must be attached to the packet header when two priority degrees are set in a system according to the related art. 1506 - 1510 show an example in which one of priority degree data PLD (1509), identifier PQ and identifier PD (1507, 1508) are attached when two priority degrees are set in the packet retransmitting system of this embodiment.

[0172] With reference to Fig. 15, a method for requesting retransmission of a lost packet based on the processing by the receiver of this embodiment is explained.

[0173] We assume that packets of sequence numbers 11 - 14 are lost. Since the PLD of sequence number 10 is 13, a quotient (Q) obtained by dividing 13 by 10 is 1, and a remainder (R) is 3. Since PQ of sequence number 10 is 01, and PD is 0, PL_{10} (0) = Q + R = 4, PL_{10} (1) = R = 3 (1511). Similarly, since the PLD of sequence number 15 is 34, a quotient (Q) obtained by dividing 34 by 15 is 2, and a remainder (R) is 4. PL_{15} (0) is a quotient obtained by dividing 94 by 15, and PL_{15} (1) is a remainder obtained by dividing 94 by 15. Since PQ of sequence number 15 is 01 and PD is 0, PL_{10} (0) = Q + R = 6, PL_{10} (1) = R = 4 (1512). Further, since the priority degree display S of sequence number 15 is -1, the packet of sequence number 15 is not an important packet to be retransmitted in the priority degrees 0 and 1. Accordingly, it is detected that PL_{10} (0) - PL_{15} (0), i.e., PL (0) of 5 and 6, are lost in the priority degree 0, and PL_{10} (1) - PL_{15} (1), i.e., PL (1) of 4, are lost in the priority degree 1 (1513). The retransmission packet transmitting unit 141 transmits a retransmission request packet for requesting to retransmit these PL's to the transmitter (1514).

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Embodiment 3.

[0174] In Embodiments 1 and 2, a case of PH = 2 was explained as an example. However, even when PH is larger than 2, this packet retransmitting system can be applied.

[0175] For example, in Fig. 7, PL is specified in case of PH = 1 ~ 2. However, for specifying the PL in case of PH = 3 ~ 4, another row of format data of a last line is added. In case of PH = 5 ~ 6, another row is further added. Information on the PL for requesting the retransmission is added.

Embodiment 4.

[0176] In Embodiment 1 and 2, as a determined value used by the priority degree information calculating unit 115, two examples were shown. It is also possible that another determined value is used to calculate the priority degree information. As far as the priority information is calculated based on an equation of PLD (N) = determined value × SN + PL (N), the packet retransmitting system and method can be applied.

Industrial Applicability

[0177] In the transmitting equipment, the receiving equipment and the packet retransmitting system and method using the above two equipments according to this invention, the transmitter can transfer data including a plurality of priority degrees in a packet. The receiver can judge if retransmission of a lost packet should be requested or not for each of the priority degrees. For example, in moving picture data compressed by MPEG (Moving Picture Experts Group) system, a moving picture includes I frame, P frame and B frame. Each of the frames has a priority degree. Apriority degree of a packet in which I frame data are provided is the highest. A priority degree of P frame is next. A priority degree of B frame is low. In this case, according to the packet retransmitting system in which the plurality of priority degrees can be set, priority degree 0 is allocated to I frame, and P frame is allocated to priority degree 1. Therefore, even if a packet is lost, it is possible to request to retransmit only a packet in which data of I frame and P frame are provided and to retransmit the packet.

[0178] As stated, the packet retransmitting system of this invention can be applied to a server (transmitting equipment) for performing streaming distribution of multimedia data by transmitting and receiving data punctually at a determined time through Internet and wireless communication network and a client (receiving equipment).

[0179] Further, even for a packet including a plurality of priority degrees, the receiver can identify the plurality of priority degrees only by one of the priority degree data PLD.

[0180] Further, the retransmission request selecting unit can select a retransmission request of an appropriate priority degree dynamically according to a condition of the network and characteristics of the data. Therefore, it is possible to prevent congestion in the network due to the retransmission request and the retransmission. It is also possible to offer a quality which is appropriate for the condition of the network and contents to be transferred.

[0181] Further, the priority degree information calculating unit 115 can reduce a value of the priority degree data included in the priority degree information by selecting a determined value used for calculating the priority degree information appropriately. Therefore, attaching amount to a transmission packet can be reduced.

Claims

1. A packet retransmitting system for transmitting a packet including a sequence number for defining a sequence of data included in each of a plurality of packets through a network and retransmitting a packet which is lost during transmission, the packet retransmitting system comprising:

   a transmitting equipment for transmitting the plurality of packets; and
   a receiving equipment for receiving the plurality of packets sent by the transmitting equipment,

   wherein the transmitting equipment includes a priority degree information attaching unit for defining a plurality of priority degrees indicating an importance degree of the data, producing priority degree information by using the plurality of priority degrees defined, and attaching the priority degree information produced to the packet, a transmitting unit for transmitting a plurality of packets to which the priority degree information is attached by the priority degree information attaching unit through the network, and a retransmitting unit for receiving a retransmission request for requesting to retransmit a packet from the receiving equipment after the transmitting unit transmits the plurality of packets and retransmitting the packet of which retransmission is requested in the retransmission request received,

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wherein the receiving equipment includes a receiving unit for receiving the plurality of packets sent by the transmitting equipment through the network and a retransmission requesting unit for inputting the plurality of packets received by the receiving unit, extracting a plurality of sequence numbers and a plurality of priority degree information from each of the plurality of packets input, judging lost packets based on the plurality of sequence numbers extracted, detecting an important packet among the lost packets judged based on the plurality of priority degree information extracted, and transmitting the retransmission request to the transmitting equipment to request to retransmit the packet detected.

2. A transmitting equipment for transmitting a packet including a sequence number for defining a sequence of data included in each of a plurality of packets through a network comprising:

a priority degree information attaching unit for defining a plurality of priority degrees indicating an importance degree of the data, producing priority degree information by using the plurality of priority degrees defined, and attaching the priority degree information produced to the packet; and
a transmitting unit for transmitting the packet to which the priority degree information is attached by the priority degree information attaching unit through the network.

3. The transmitting equipment of Claim 2, wherein the priority degree information attaching unit includes
a priority degree setting unit for setting an importance degree for each of the plurality of priority degrees,
a priority degree memory for storing the plurality of priority degrees set by the priority degree setting unit, and
a priority degree information calculating unit for producing the priority degree information by using the plurality of priority degrees stored in the priority degree memory and the sequence number included in the packet.

4. The transmitting equipment of Claim 3, wherein the priority degree setting unit defines the plurality of priority degrees hierarchically by setting an order, wherein the priority degree information calculating unit calculates the priority degree information by giving priority to a priority degree in a high order.

5. The transmitting equipment of Claim 4, wherein the priority degree setting unit selects a priority degree one by one from a higher order among the plurality of priority degrees, judges an importance degree of data included in the packet based on the priority degree selected, and increases a value of the priority degree selected by one and sets the value of the priority degree selected when it is judged as an important packet.

6. The transmitting equipment of Claim 5, wherein the priority degree information calculating unit produces the priority degree information by using a result of adding one of values of the plurality of priority degrees corresponding to the packet to a product of a determined value and the sequence number included in the packet.

7. The transmitting equipment of Claim 6, wherein, when a number of the plurality of priority degrees is defined as PH, a value of the plurality of priority degrees is defined as PL (PH), a counter is defined as N, a sequence number included in an arbitrary packet is defined as SN, and a value of the priority degree information calculated for each of the plurality of priority degrees is defined as PLD (PH) for the arbitrary packet, the priority degree information calculating unit substitutes PL (0) for PLD (0) and calculates PLD (N) = the determined value $\times$ SN + PL (N) for each of N in a value of $0 < N < PH$, defines PLD (PH - 1) in case of N = PH - 1 as the priority degree information PLD of the arbitrary packet, obtains the priority degree information by calculating PLD (PH - 1) for each of the plurality of packets, and calculates the plurality of priority degree information.

8. A transmitting equipment of Claim 7, wherein the priority degree information calculating unit uses a value of PLD (N - 1) as the determined value.

9. The transmitting equipment of Claim 7, wherein the priority degree information calculating unit uses one of (|PLD (N - 1) - PL (N)|) which is an absolute value of a difference between PLD (N - 1) and PL (N), (|SN - PLD (N - 1)|) which is an absolute value of a difference between SN and PLD (N - 1), and (|SN - PL (N)|) which is an absolute value of a difference between SN and PL (N) as the determined value.

10. The transmitting equipment of Claim 9, wherein the priority degree information calculating unit defines a minimum value among |PLD (N - 1) - PL (N)|, |SN - PLD (N - 1)|, |SN - PL (N)| as Q, defines an identifier for identifying which value among three values is defined as Q as PQ, defines an identifier for identifying which is larger between X and Y as PD when Q = |X - Y|, sets PQ = TYPE1, PD = 0, R = PL (N) in case of Q = |PLD (N - 1) - PL (N)| and PLD (N - 1) $\geqq$ PL (N), sets PQ = TYPE1, PD = 1, R = PLD (N - 1) in case of Q = |PLD (N - 1) - PL (N)| and PLD

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(N - 1) < PL (N), sets PQ = TYPE2, PD = 0, R = PL (N) in case of Q = ISN - PLD (N - 1)I and SN ≧ PLD (N - 1), sets PQ = TYPE2, PD = 1 in case of Q = ISN - PLD (N- 1)I and SN < PLD (N - 1), and sets PQ = TYPE3, PD = 0, R = PLD (N - 1) in case of Q = I SN - PL (N)I, and calculates PLD (PH - 1), wherein the priority degree information attaching unit attaches PLD (PH - 1), PQ and PD to the packet as the priority degree information.

11. The transmitting equipment of Claim 2, further comprising a retransmitting unit for receiving a retransmission request packet for requesting retransmission of a packet after transmitting the plurality of packets from the transmitting unit, retrieving a packet of which retransmission is requested in the retransmission request packet received, and retransmitting the packet retrieved.

12. A receiving equipment comprising:

a receiving unit for receiving a plurality of packets including a sequence number which defines a sequence of data included in each of the plurality of packets and priority degree information produced based on a plurality of priority degrees indicating an importance degree of data included through a network; and
a retransmission requesting unit for inputting the plurality of packets received by the receiving unit, extracting a plurality of sequence numbers and a plurality of priority degree information from each of the plurality of packets input, judging lost packets based on the plurality of sequence numbers extracted, detecting an important packet among the lost packets judged based on the plurality of priority degree information, and transmitting a retransmission request to request to retransmit the packet detected.

13. The receiving equipment of Claim 12, wherein the retransmission requesting unit detects the important packet by using the importance degree indicated in each of the plurality of priority degrees included in the plurality of priority degree information.

14. The receiving equipment of Claim 13, wherein the retransmission requesting unit includes
a packet information memory for storing the plurality of sequence numbers and the plurality of priority degree information extracted,
a priority degree calculating unit for calculating a value of a plurality of priority degrees by using the sequence numbers and the priority degree information stored in the packet information memory, and
a lost packet detecting unit for judging a lost packet based on the plurality of sequence numbers and detecting if any important packet is lost based on the value of the plurality of priority degrees calculated by the priority degree calculating unit.

15. The receiving equipment of Claim 14, wherein the priority degree calculating unit calculates a quotient and a remainder by dividing the priority degree information by the sequence number, and calculates a value of the plurality of priority degrees by using the quotient and the remainder calculated.

16. The receiving equipment of Claim 15, wherein, when the priority degree information is defined as PLD, the sequence number included in an arbitrary packet is defined as SN, a number of the plurality of priority degrees is defined as PH, a value of the plurality of priority degrees is defined as PL (PH), and a counter is defined as N for an arbitrary packet, the priority degree information calculating unit substitutes an initial value of N in a range of 0 ≦ N < PH for N = PH - 1, substitutes a remainder of PLD / SN for PL (N), substitutes a quotient of PLD / SN for PLD, repeats a calculation of deducting N by 1 till N reaches 0, calculates a value of the plurality of priority degrees by substituting a value of PLD for PL (0) in case of N = 0, calculates PL (PH) for each of the plurality of packets, and calculates the value of the plurality of priority degrees corresponding to the plurality of packets, wherein the lost packet detecting unit judges if a packet with a priority degree indicated by PL (N) is lost based on a difference between values of a maximum value in PL (N) corresponding to each of the plurality of packets received and PL (N) of the arbitrary packet, and when the packet has been lost, detects the PL (N) of the packet.

17. The receiving equipment of 15, wherein the priority degree information includes priority degree data produced from the plurality of priority degrees, an identifier for indicating a type of data used for producing the priority degree data, and a flag for indicating a size of a value of the identifier for each of arbitrary packets, wherein, when the priority degree data are defined as PLD, the identifier is defined as PQ, the flag is defined as PD, a number of the plurality of priority degrees is defined as PH, a value of the plurality of priority degrees is defined as PL (PH), and a counter is defined as N for an arbitrary packet, the priority degree information calculating unit substitutes an initial value of N in a range of 0 ≦ N < PH for N = PH - 1, defines TYPE 1, TYPE2 and TYPE 3 as types of the identifier PQ, defines that a value of the flag PD is one of 0 and 1, defines a quotient Q obtained by dividing PLD

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by SN as Q and a remainder as R, sets PL (N) = R and substitutes Q + R for PLD in case of PQ = TYPE1 and PD = 0, sets PL (N) = Q + R and substitutes R for PLD in case of PQ = TYPE1 and PD = 1, sets PL (N) = R and substitutes SN - Q for PLD in case of PQ = TYPE2 and PD = 0, sets PL (N) = R and substitutes Q + SN for PLD in case of PQ = TYPE2 and PD = 1, sets PL (N) = SN - Q and substitutes R for PLD in case of PQ = TYPE3, repeats a calculation of deducting N by 1 from N = PH - 1 to N = 1, calculates PL from PL (0) to PL (PH - 1) by substituting PLD for PL (0) in case of N = 1, wherein the lost packet detecting unit judges if an important packet in the priority degree N is lost based on a difference between values of a maximum value of PL (N) of a packet and PL (N) of an arbitrary packet among the plurality of packets received by the receiving unit and detects the PL (N) of the packet lost when the packet has been lost.

18. The receiving equipment of Claim 14, wherein the retransmission requesting unit further includes a retransmission request selecting unit for selecting a particular priority degree among the plurality of priority degrees, wherein the lost packet detecting unit detects loss of a packet based on the particular priority degree selected by the retransmission request selecting unit.

19. A packet retransmitting method for transmitting a packet including a sequence number for defining a sequence of data included in each of a plurality of packets from a transmitter to a receiver through a network and retransmitting a packet which is lost during transmission,

the packet retransmitting method comprising:

in the transmitter,
defining a plurality of priority degrees indicating an importance degree of data;
producing priority degree information by using the plurality of priority degrees defined;
attaching the priority degree information produced to the packet;
repeating producing the priority degree information and attaching the priority degree information to each of the plurality of packets; and
transmitting the plurality of packets to which the priority degree information is attached to the receiver through the network, and
in the receiver,
receiving the plurality of packets through the network;
extracting a plurality of sequence numbers and a plurality of priority degree information from each of the plurality of packets received;
judging lost packets based on the plurality of sequence extracted;
detecting an important packet among the lost packets judged based on the plurality of priority degree information extracted; and
transmitting a retransmission request to the transmitter to request to retransmit the packet detected.

20. A packet transmitting method for transmitting a packet including a sequence number for defining a sequence of data included in each of a plurality of packets through a network, the method comprising:

defining a plurality of priority degrees indicating an importance degree of the data;
producing priority degree information by using the plurality of priority degrees defined;
attaching the priority degree information produced to the packet; and
transmitting the packet to which the priority degree information is attached through the network.

21. A packet transmitting method of Claim 20, wherein the step of defining priority degrees includes

defining the plurality of priority degrees hierarchically by setting an order,
selecting a priority degree is selected from a higher priority degree among the plurality of priority degrees,
judging an importance degree in the selected priority degree, and
adding one to a value of the selected priority degree when it is judged as an important packet,
wherein the step of producing the priority degree information includes producing the priority degree information by using a result of adding a value of one of the plurality of priority degrees corresponding to the packet to a product of a determined value and a sequence number included in the packet.

22. The packet transmitting method of Claim 21, wherein the step of defining the priority degrees includes setting values of the plurality of priority degrees corresponding to the plurality of packets by setting a value of the plurality of priority degrees repeatedly for the plurality of packets,

wherein the step of producing the priority degree information includes producing the priority degree informa-

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tion corresponding to each of the plurality of packets by producing the priority degree information repeatedly for the plurality of packets.

23. Apacket receiving method comprising:

receiving a plurality of packets including a sequence number for defining a sequence of data included in each of the plurality of packets and priority degree information produced based on a plurality of priority degrees indicating an importance degree of data stored in each of the plurality of packets through a network;
extracting a plurality of sequence numbers and a plurality of priority degree information from the plurality of packets received;
judging lost packets based on the plurality of sequence numbers extracted;
detecting an important packet based on the plurality of priority degree information extracted among the packets judged as the lost packets; and
transmitting a retransmission request for requesting to retransmit the packet detected.

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Fig. 1

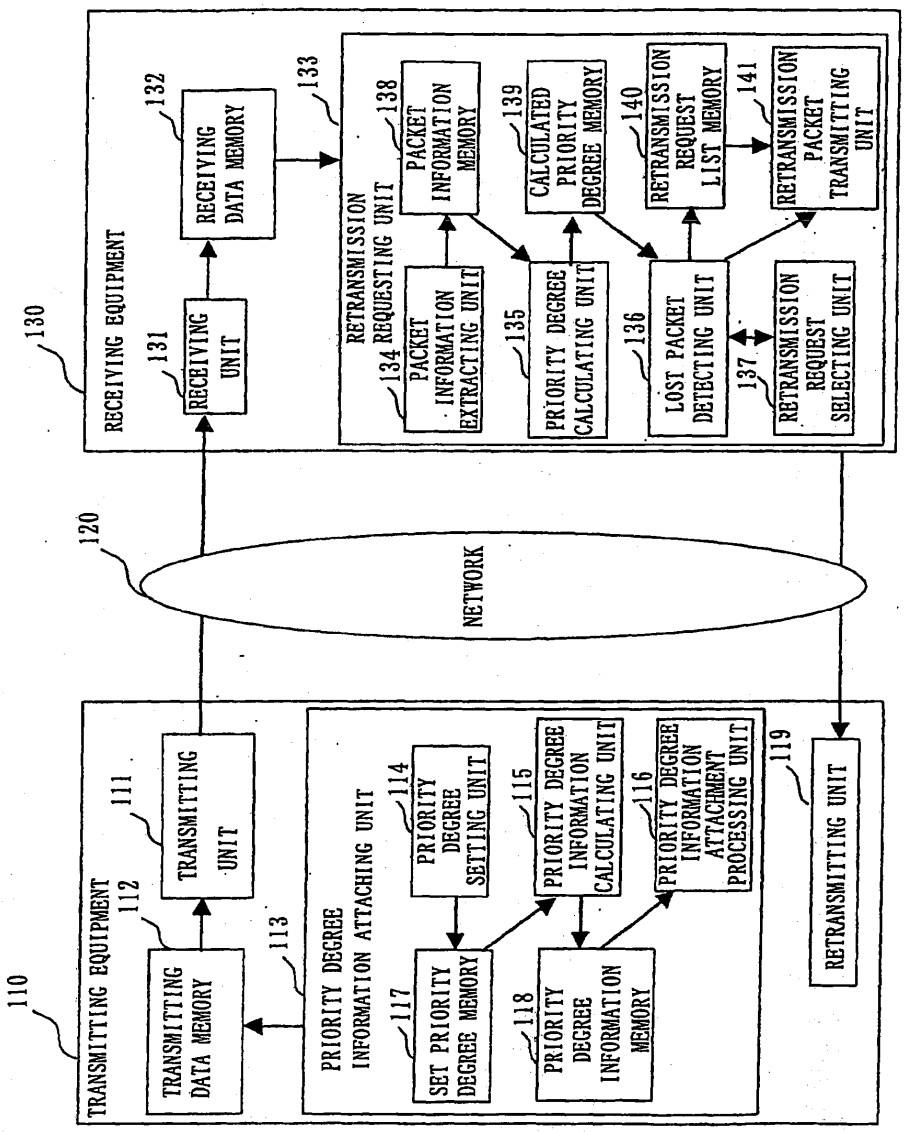

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Fig. 2

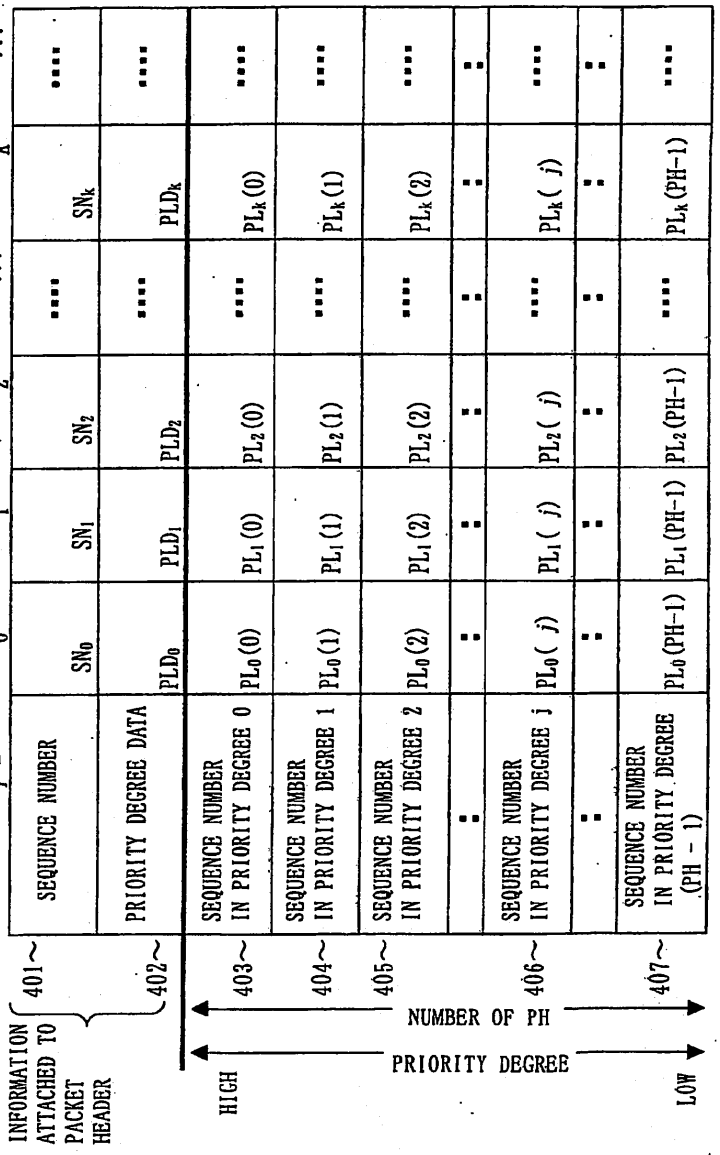

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Fig. 3

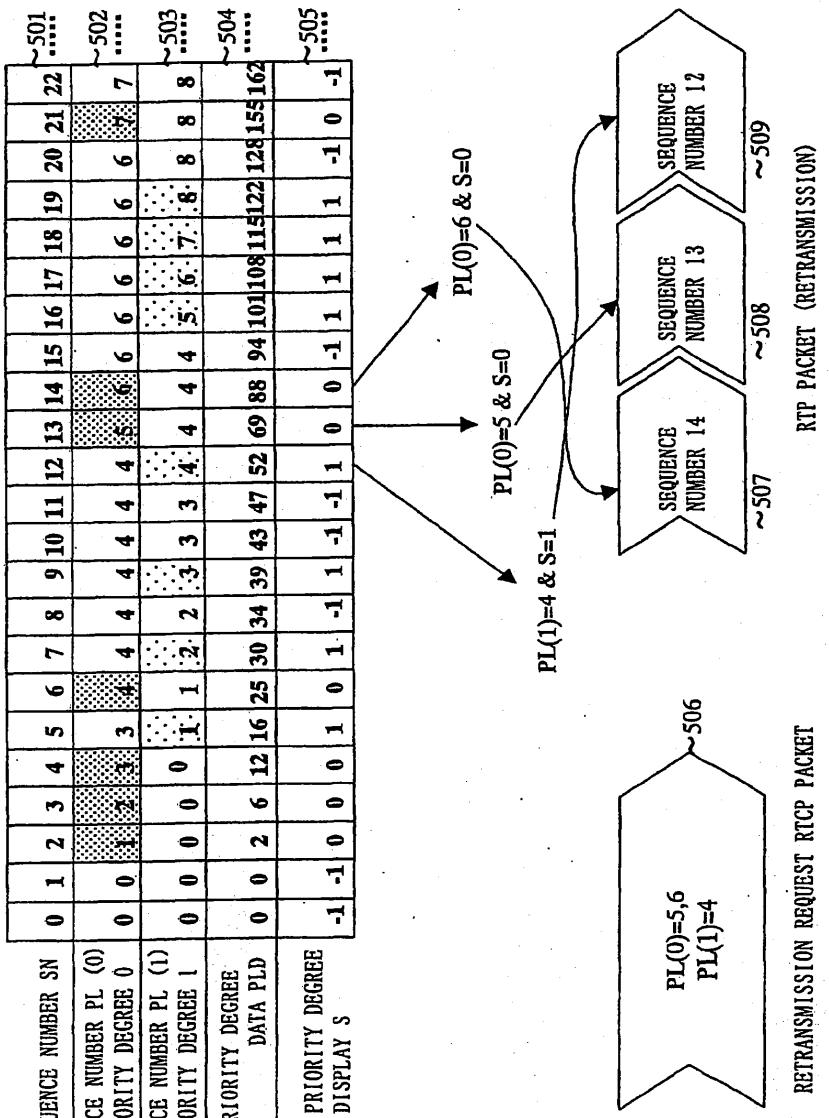

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Fig. 4

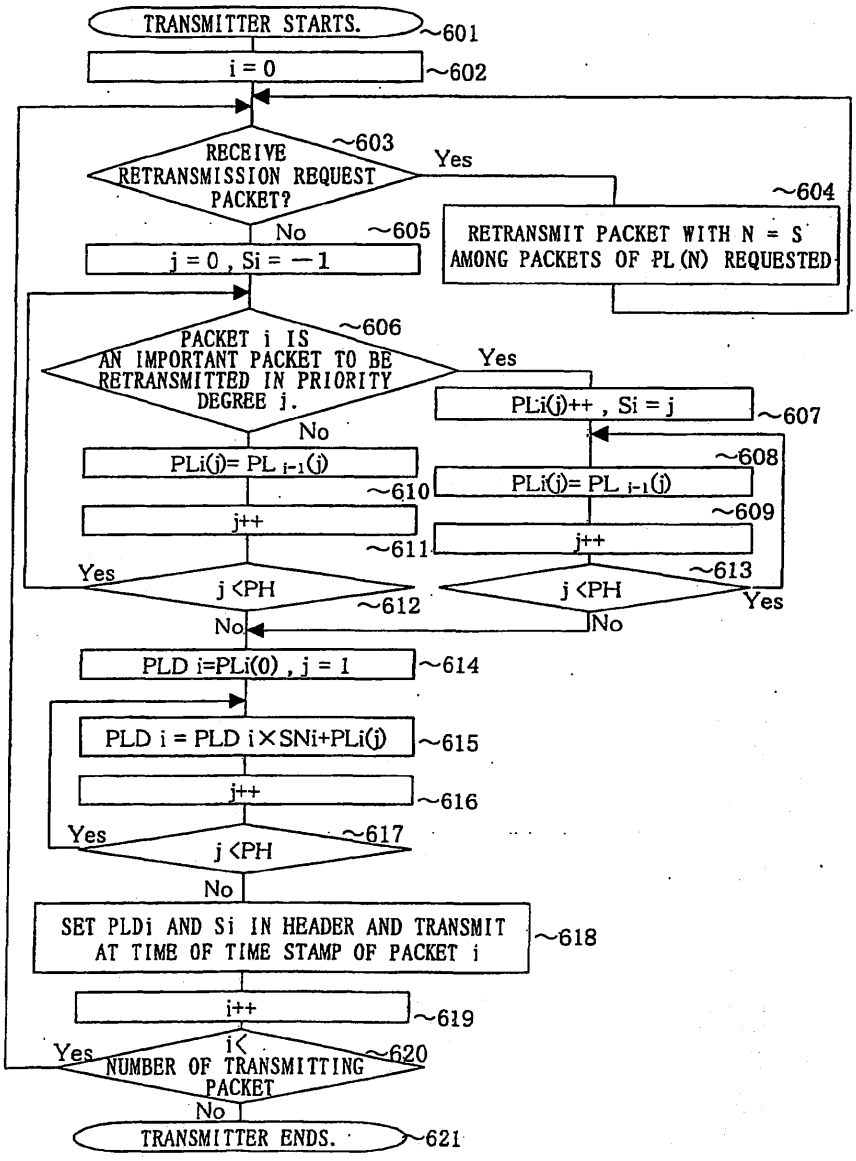

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Fig. 5

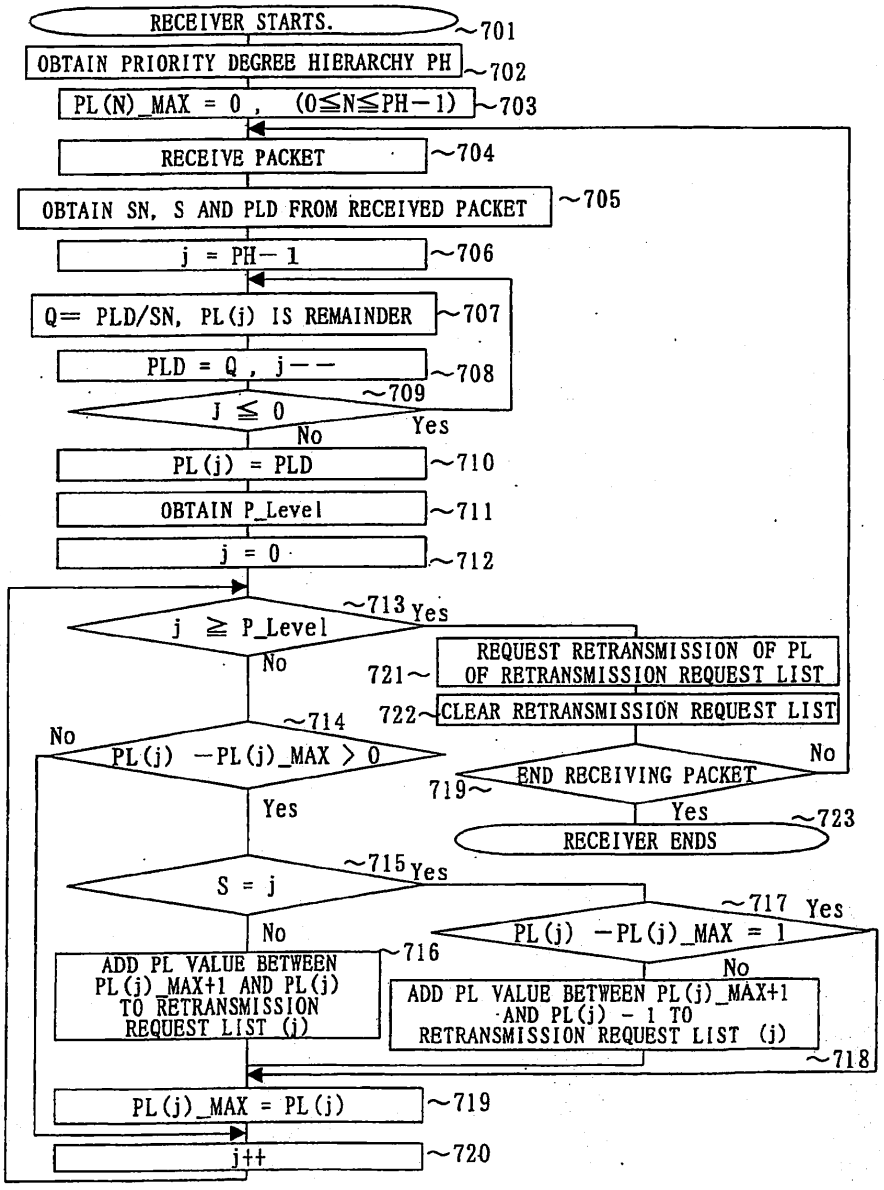

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Fig. 6

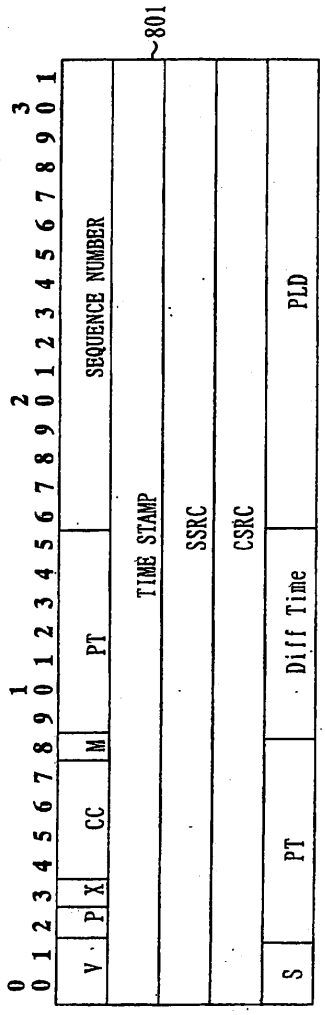

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Fig. 7

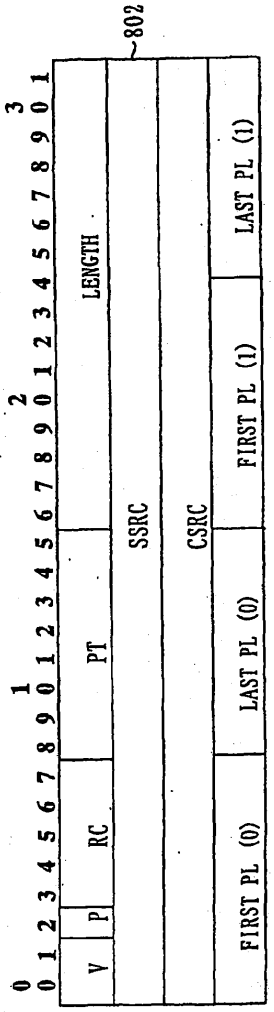

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Fig. 8

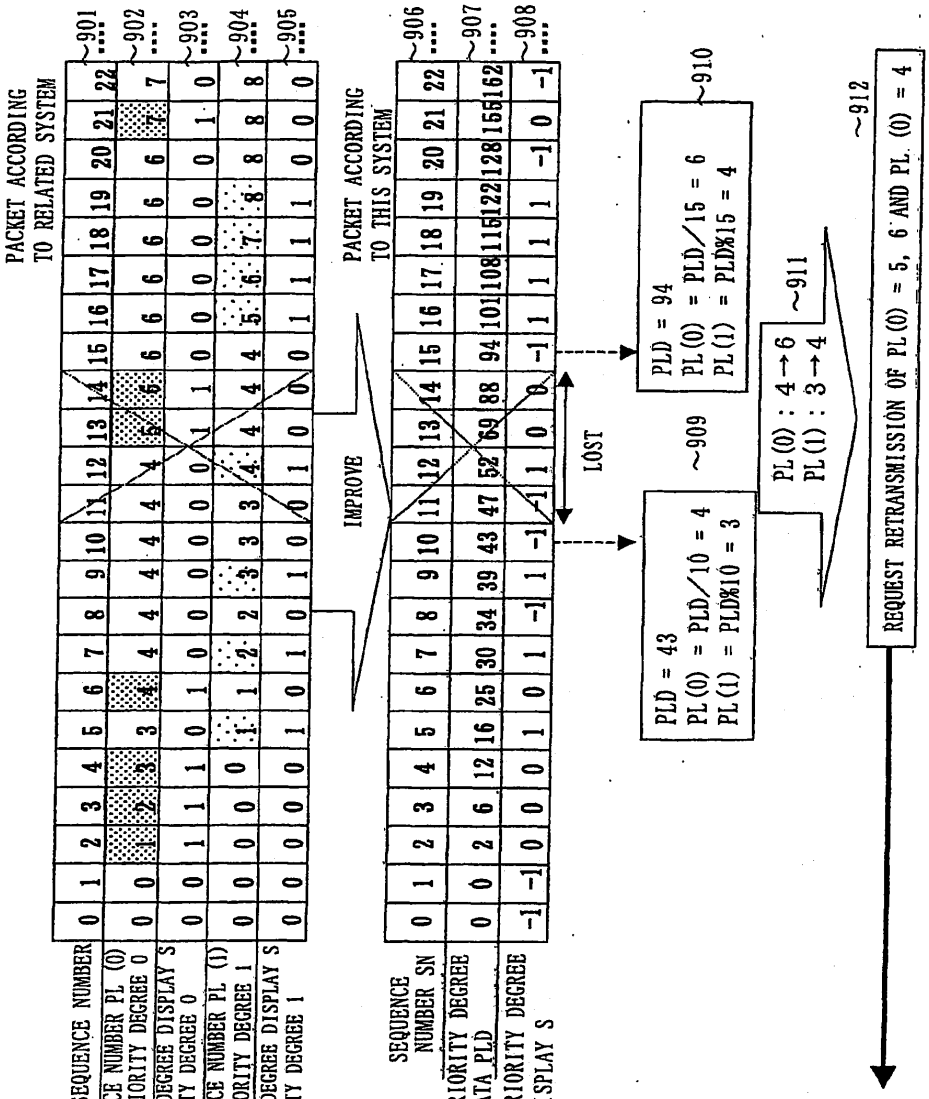

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Fig. 9

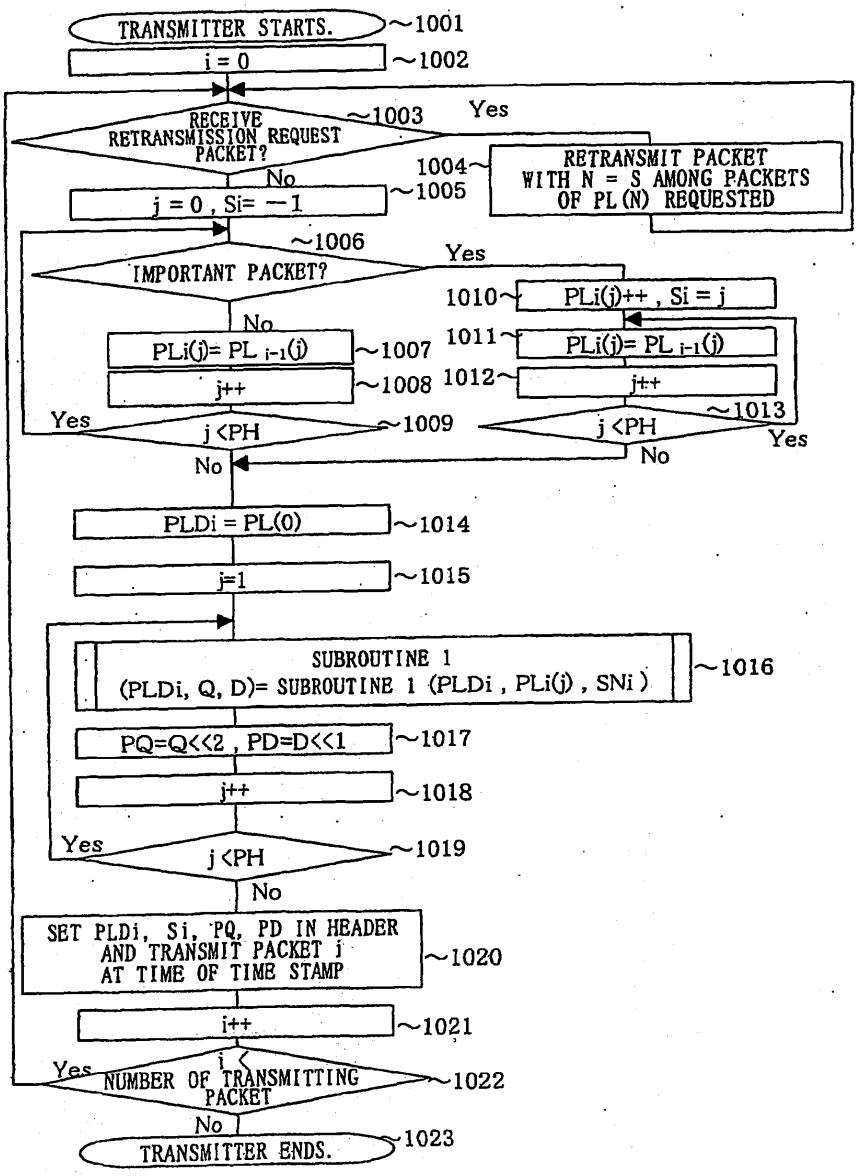

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Fig. 10

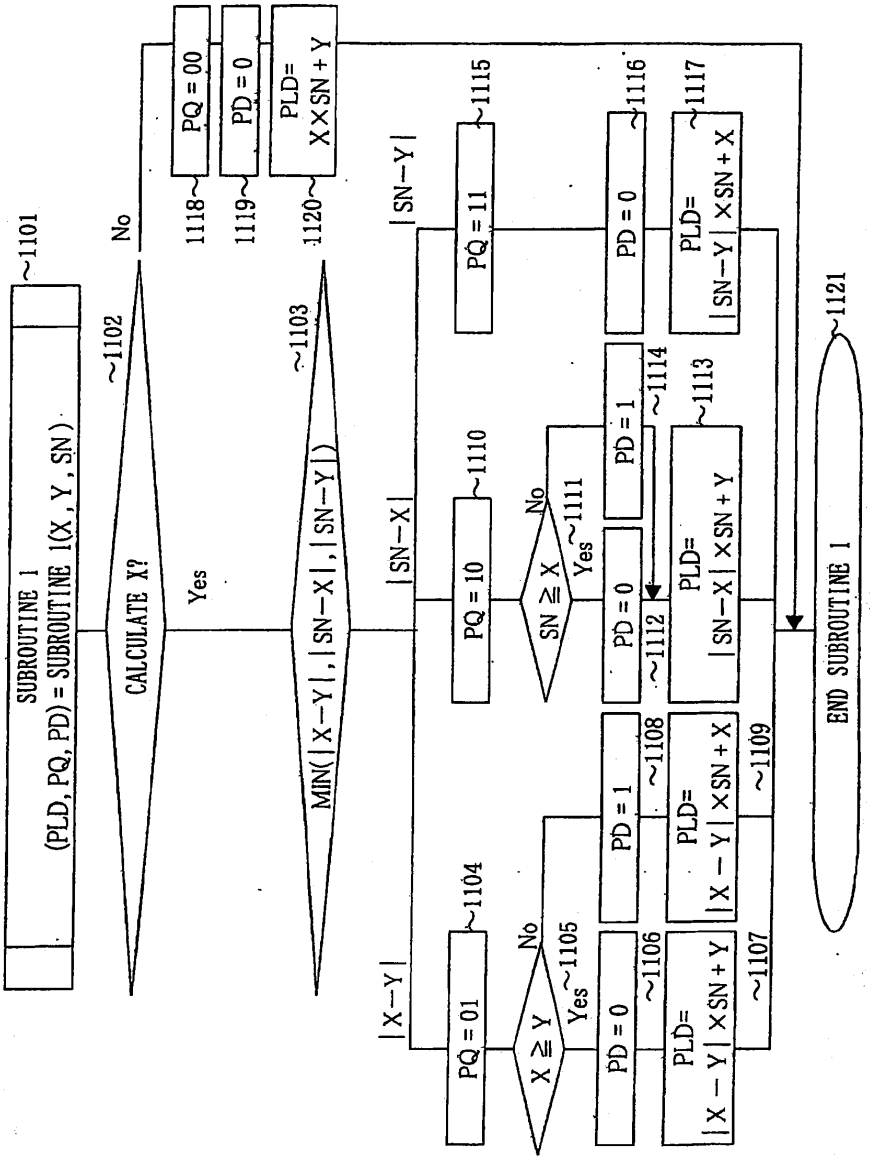

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Fig.11

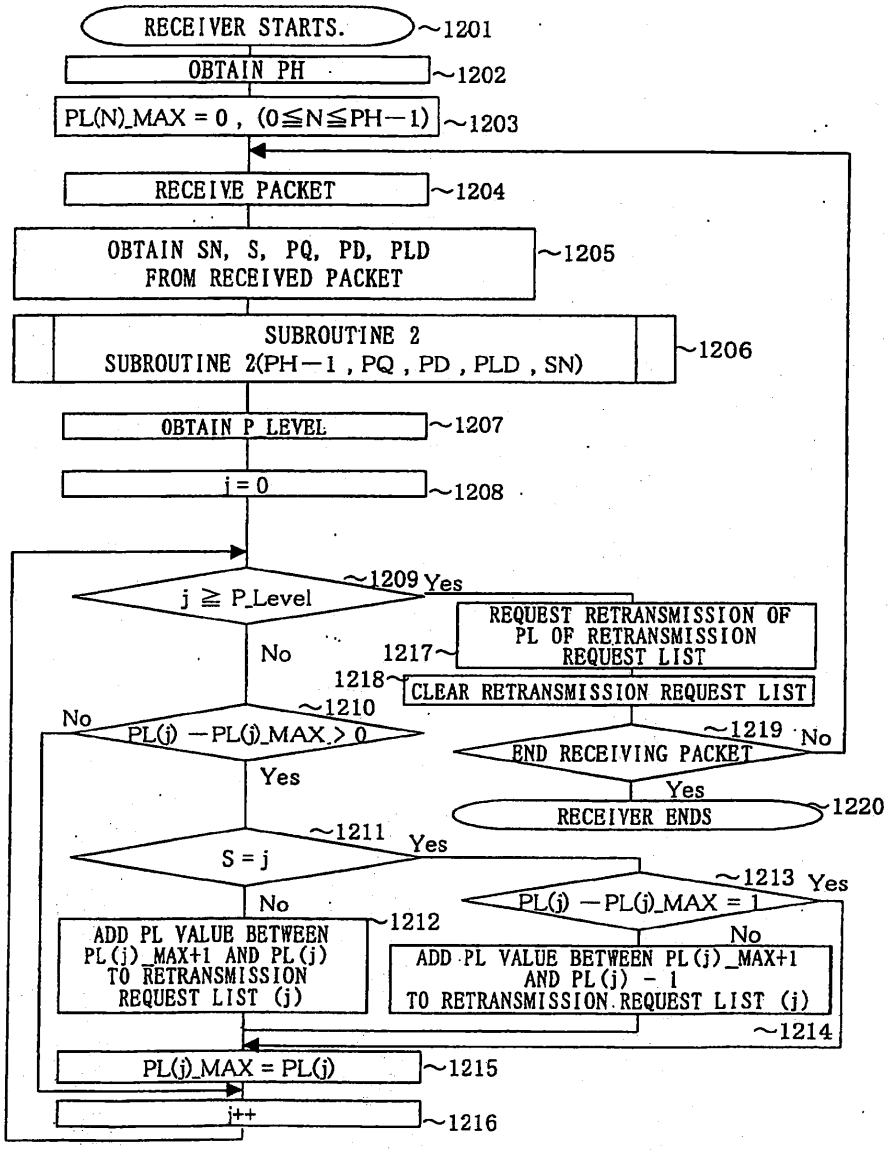

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Fig. 12

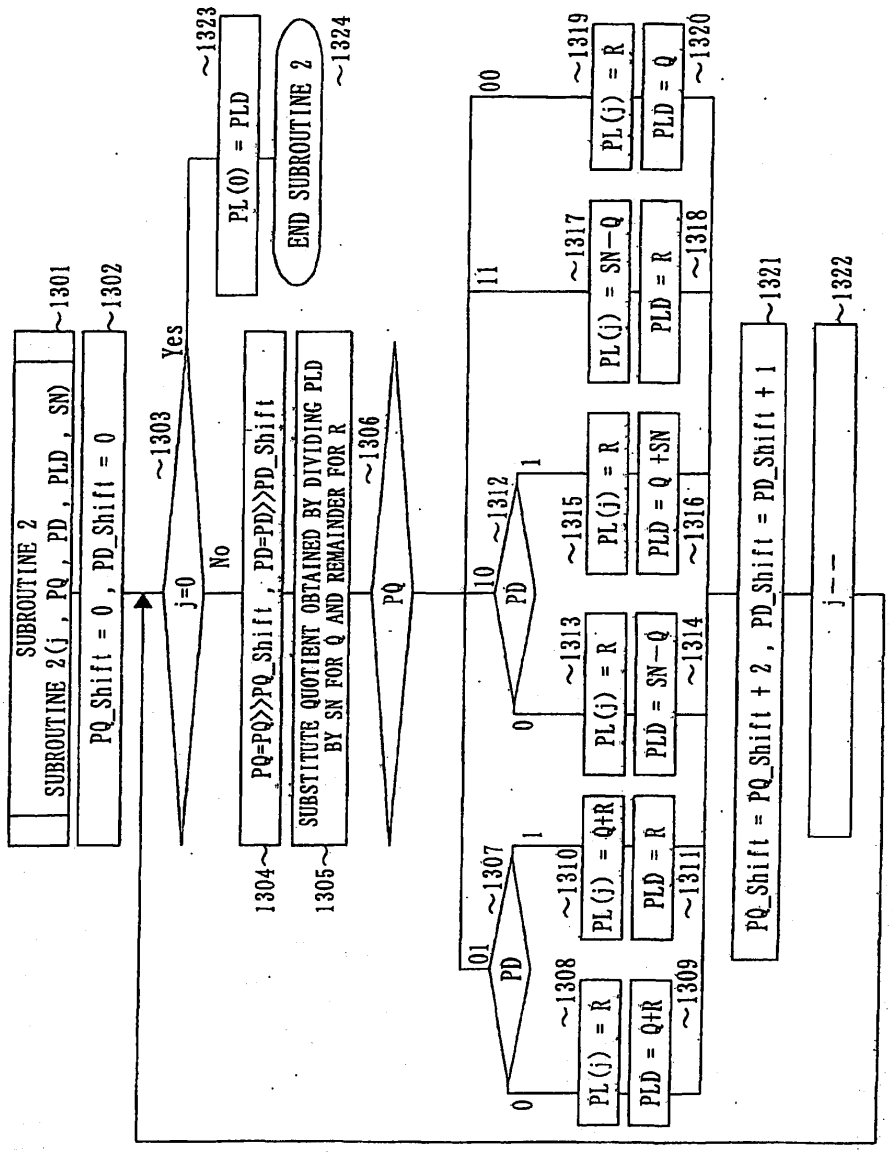

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Fig. 13

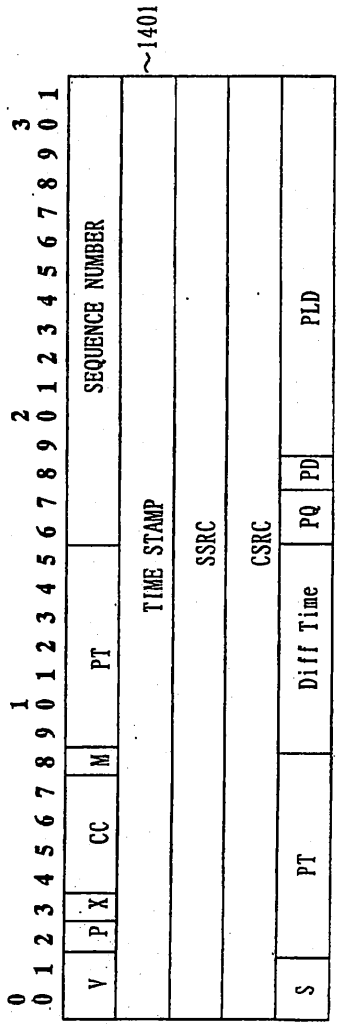

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Fig. 14

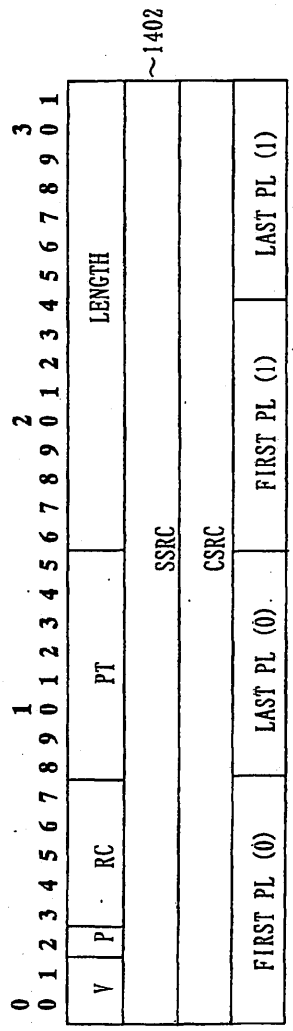

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Fig. 15

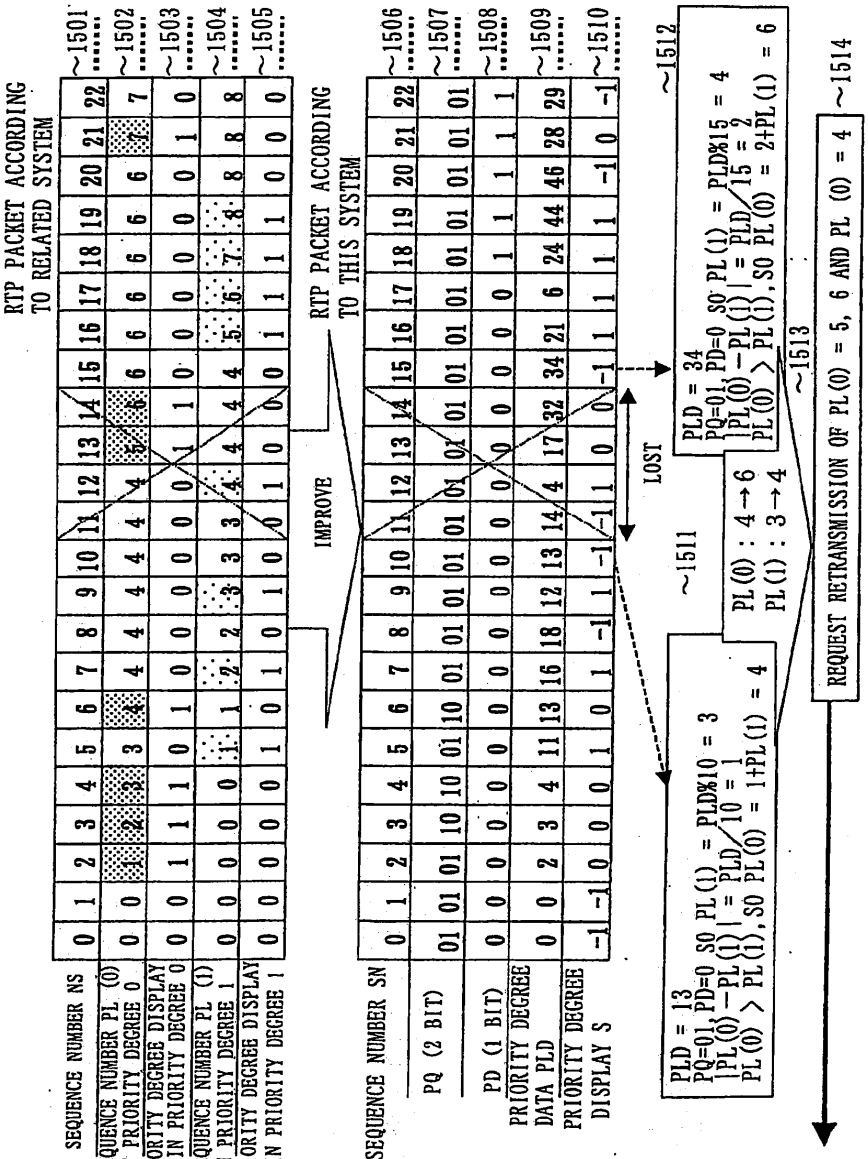

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Fig. 16

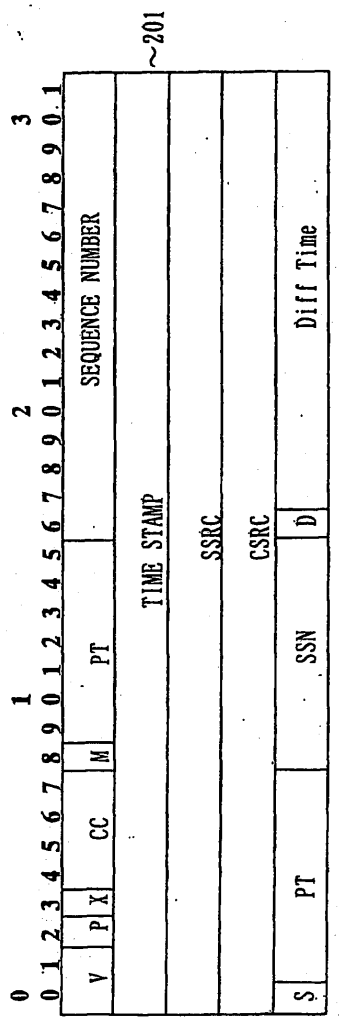

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Fig. 17

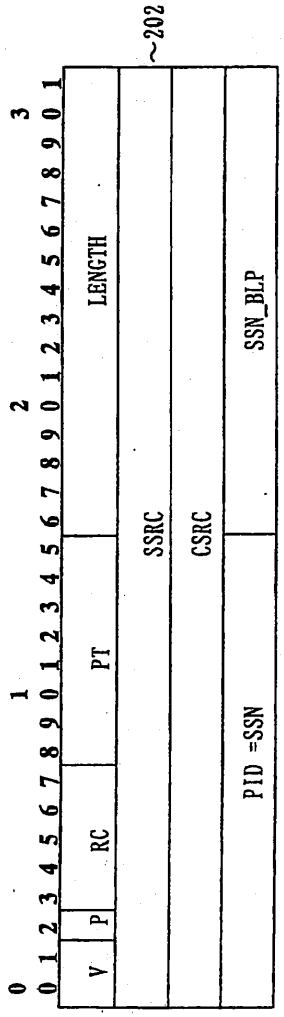

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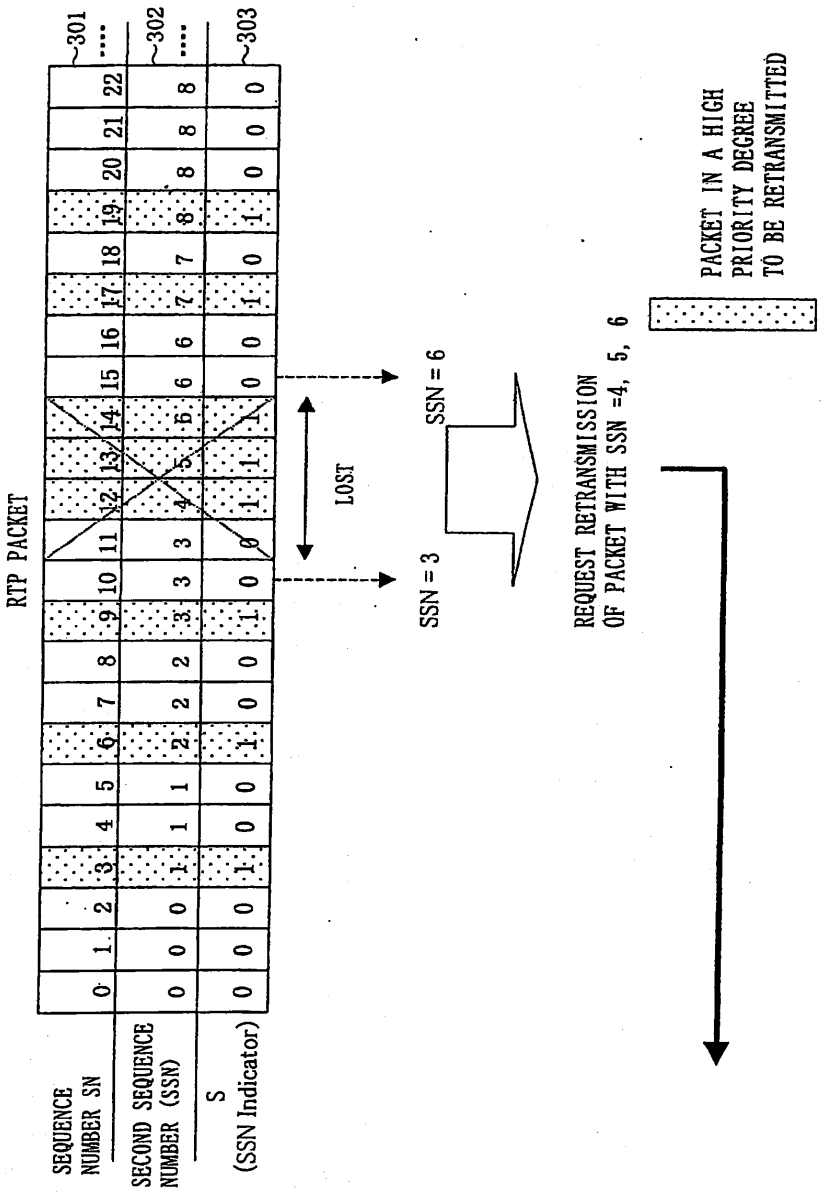
Fig. 18



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INTERNATIONAL SEARCH REPORT

International application No.
PCT/JP00/06941

A. CLASSIFICATION OF SUBJECT MATTER
Int.Cl[7] H04L12/56, H04L1/16, H04L29/08

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
Int.Cl[7] H04L12/56, H04L1/16, H04L29/08

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched
Jitsuyo Shinan Koho 1922-1996 Toroku Jitsuyo Shinan Koho 1994-2000
Kokai Jitsuyo Shinan Koho 1971-2000 Jitsuyo Shinan Toroku Koho 1996-2000

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)
JICST FILE (JOIS)

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	JP 2000-228676 A (Matsushita Electric Ind. Co., Ltd.), 15 August, 2000 (15.08.00), Figs. 1, 9 to 10 (Family: none)	2,20
A		1,3-19,21-23
A	JP 10-65700 A (Ricoh Company, Ltd.), 06 March, 1998 (06.03.98), Fig. 2 (Family: none)	1-23

☐ Further documents are listed in the continuation of Box C. ☐ See patent family annex.

* Special categories of cited documents:
"A" document defining the general state of the art which is not considered to be of particular relevance
"E" earlier document but published on or after the international filing date
"L" document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)
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"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone
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"&" document member of the same patent family

Date of the actual completion of the international search	Date of mailing of the international search report
20 December, 2000 (20.12.00)	16 January, 2001 (16.01.01)
Name and mailing address of the ISA/ Japanese Patent Office	Authorized officer
Facsimile No.	Telephone No.

Form PCT/ISA/210 (second sheet) (July 1992)

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(74) Agent: **VICK, Jason, H.**; Miles & Stockbridge P.C., 1751 Pinnacle Dr., Suite 500, McLean, VA 22102 (US).

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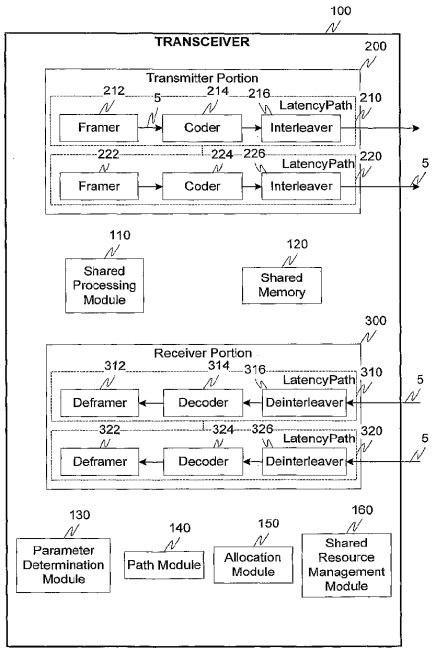
Published:
— *with international search report*

[Continued on next page]

(54) Title: RESOURCE SHARING IN A TELECOMMUNICATIONS ENVIRONMENT



(57) Abstract: A transceiver is designed to share memory and processing power amongst a plurality of transmitter and/or receiver latency paths, in a communications transceiver that carries or supports multiple applications. For example, the transmitter and/or receiver latency paths of the transceiver can share an interleaver/deinterleaver memory. This allocation can be done based on the data rate, latency, BER, impulse noise protection requirements of the application, data or information being transported over each latency path, or in general any parameter associated with the communications system.

WO 2006/044227 A1

For two-letter codes and other abbreviations, refer to the "Guidance Notes on Codes and Abbreviations" appearing at the beginning of each regular issue of the PCT Gazette.

RESOURCE SHARING IN A TELECOMMUNICATIONS ENVIRONMENT

RELATED APPLICATION DATA

[0001] This application claims the benefit of and priority under 35 U.S.C. § 119(e) to U.S. Patent Application No. 60/618,269, filed October 12, 2004, entitled "Sharing Memory and Processing Resources in DSL Systems," which is incorporated herein by reference in its entirety.

BACKGROUND

Field of the Invention

[0002] This invention generally relates to communication systems. More specifically, an exemplary embodiment of this invention relates to memory sharing in communication systems. Another exemplary embodiment relates to processing or coding resource sharing in a communication system.

Description of Related Art

[0003] U.S. Patent Nos. 6,775,320 and 6,778,589, which are both incorporated herein by reference in their entirety, describe DSL systems supporting multiple applications and multiple framer/coder/interleaver FCI blocks (an FCI block is also referred to as a latency path). DSL systems carry applications that have different transmission requirements with regard to, for example, data rate, latency (delay), bit error rate (BER), and the like. For example, video typically requires a low BER (<1E-10) but can tolerate higher latency (>20 ms). Voice, on the other hand, typically requires a low latency (<1 ms) but can tolerate BER (>1E-3).

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[0004] As described in U.S. Patent No. 6,775,320, different applications can use different latency paths in order to satisfy the different application requirements of the communication system. As a result a transceiver must support multiple latency paths in order to support applications such as video, Internet access and voice telephony. When implemented in a transceiver, each of the latency paths will have a framer, coder, and interleaver block with different capabilities that depend on the application requirements.

SUMMARY

[0005] One difficulty with implementing multiple latency paths in a transceiver is the fact that a latency path is a complicated digital circuit that requires a large amount of memory and processing power. An interleaver within a latency path can consume a large amount of memory in order to provide error correcting capability. For example, a typical DSL transceiver will have at least one latency path with approximately 16 kbytes of memory for the interleaver. Likewise, the coding block, for example, a Reed Solomon coder, consumes a large amount of processing power. In general, as the number of latency paths increase, the memory and processing power requirements for a communication system become larger.

[0006] Accordingly, an exemplary aspect of this invention relates to sharing memory between one or more interleavers and/or deinterlaevers in a transceiver. More particularly, an exemplary aspect of this invention relates to shared latency path memory in a transceiver.

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[0007] Additional aspects of this invention relate to configuring and initializing shared memory in a communication system. More particularly, an exemplary aspect of this invention relates to configuring and initializing interleaver/deinterleaver memory in a communication system.

[0008] Additional aspects of the invention relate to determining the amount of memory that can be allocated to a particular component by a communication system. More specifically, an exemplary aspect of the invention relates to determining the maximum amount of shared memory that can be allocated to one or more interleaves or deinterleavers.

[0009] According to another exemplary aspect of the invention, processing power is shared between a number of transceiver modules. More specifically, and in accordance with an exemplary embodiment of the invention, a coding module is shared between one or more coders and/or decoders.

[0010] Another exemplary embodiment of the invention relates to transitioning from a fixed memory configuration to a shared memory configuration during one or more of initialization and SHOWTIME (user data transmission).

[0011] An additional exemplary aspect of the invention relates to dynamically updating one or more of shared memory and processing resources based on changing communication conditions.

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[0012] An additional exemplary aspect of the invention relates to updating one or more of shared memory and processing resources based on an updated communication parameter.

[0013] An additional exemplary aspect of the invention relates to updating the allocation of one or more of shared memory and processing resources based on an updated communication parameter(s).

[0014] Additional aspects of the invention relate to exchanging shared resource allocations between transceivers.

[0015] Additional exemplary aspects relate to a method of allocating shared memory in a transceiver comprising allocating the shared memory to a plurality of modules, wherein each of the plurality of modules comprise at least one interleaver, at least one deinterleaver or a combination thereof.

[0016] Still further aspects relate to the above method wherein the plurality of modules comprise interleavers.

[0017] Still further aspects relate to the above method wherein the plurality of modules comprise deinterleavers.

[0018] Still further aspects relate to the above method wherein the plurality of modules comprise at least one interleaver and at least one deinterleaver.

[0019] Additional exemplary aspects relate to a transceiver comprising a plurality of modules each including at least one interleaver, at least one deinterleaver or a

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combination thereof and a shared memory designed to be allocated to a plurality of the modules.

[0020] Still further aspects relate to the above transceiver wherein the plurality of modules comprise interleavers.

[0021] Still further aspects relate to the above transceiver wherein the plurality of modules comprise deinterleavers.

[0022] Still further aspects relate to the above transceiver wherein the plurality of modules comprise at least one interleaver and at least one deinterleaver.

[0023] These and other features and advantages of this invention are described in, or are apparent from, the following description of the embodiments.

BRIEF DESCRIPTION OF THE DRAWINGS

[0024] The embodiments of the invention will be described in detail, with reference to the following figures, wherein:

[0025] Fig. 1 is a functional block diagram illustrating an exemplary transceiver according to this invention;

[0026] Fig. 2 is a flowchart outlining an exemplary method of sharing resources according to this invention;

[0027] Fig. 3 is a flowchart outlining an exemplary method of determining a maximum amount of shared memory according to this invention; and

[0028] Fig. 4 is a flowchart outlining an exemplary resource sharing methodology according to this invention.

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DETAILED DESCRIPTION

[0029] The exemplary embodiments of this invention will be described in relation to sharing resources in a wired and/or wireless communications environment. However, it should be appreciated, that in general, the systems and methods of this invention will work equally well for any type of communication system in any environment.

[0030] The exemplary systems and methods of this invention will also be described in relation to multicarrier modems, such as DSL modems and VDSL modems, and associated communication hardware, software and communication channels. However, to avoid unnecessarily obscuring the present invention, the following description omits well-known structures and devices that may be shown in block diagram form or otherwise summarized.

[0031] For purposes of explanation, numerous details are set forth in order to provide a thorough understanding of the present invention. It should be appreciated however that the present invention may be practiced in a variety of ways beyond the specific details set forth herein.

[0032] Furthermore, while the exemplary embodiments illustrated herein show the various components of the system collocated, it is to be appreciated that the various components of the system can be located at distant portions of a distributed

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network, such as a telecommunications network and/or the Internet, or within a dedicated secure, unsecured and/or encrypted system. Thus, it should be appreciated that the components of the system can be combined into one or more devices, such as a modem, or collocated on a particular node of a distributed network, such as a telecommunications network. As will be appreciated from the following description, and for reasons of computational efficiency, the components of the system can be arranged at any location within a distributed network without affecting the operation of the system. For example, the various components can be located in a Central Office modem (CO, ATU-C, VTU-O), a Customer Premises modem (CPE, ATU-R, VTU-R), a DSL management device, or some combination thereof. Similarly, one or more functional portions of the system could be distributed between a modem and an associated computing device.

[0033] Furthermore, it should be appreciated that the various links, including communications channel 5, connecting the elements can be wired or wireless links, or any combination thereof, or any other known or later developed element(s) that is capable of supplying and/or communicating data to and from the connected elements. The term module as used herein can refer to any known or later developed hardware, software, firmware, or combination thereof that is capable of performing the functionality associated with that element. The terms determine, calculate and compute, and variations thereof, as used herein are used interchangeably and include any type of methodology, process, mathematical operation or technique. FCI block and latency path are used interchangeably herein as well as transmitting modem and transmitting transceiver. Receiving modem and receiving transceiver are also used

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interchangeably.

[0034] Fig. 1 illustrates an exemplary embodiment of a transceiver 100 that utilizes shared resources. It should be appreciated that numerous functional components of the transceiver have been omitted for clarity. However, the transceiver 100 can also include the standard components found in typical communications device(s) in which the technology of the subject invention is implemented into.

[0035] According to an exemplary embodiment of the invention, memory and processing power can be shared among a plurality of transmitter and/or receiver latency paths, in a communications transceiver that carries or supports multiple applications. For example, the transmitter and/or receiver latency paths of the transceiver can share an interleaver/deinterleaver memory and the shared memory can be allocated to the interleaver and/or deinterleaver of each latency path. This allocation can be done based on the data rate, latency, BER, impulse noise protection requirements of the application, data or information being transported over each latency path, or in general any parameter associated with the communications system.

[0036] Likewise, for example, the transmitter and/or receiver latency paths can share a Reed-Solomon coder/decoder processing module and the processing power of this module can be allocated to each encoder and/or decoder. This allocation can be done based on the data rate/latency, BER, impulse noise protection requirements of the application data or information being transported over each latency path, or in general based on any parameter associated with the communication system.

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[0037] In accordance with an exemplary operational embodiment, a first transceiver and a second transceiver transmit to one another messages during, for example, initialization which contain information on the total and/or shared memory capabilities of each transceiver and optionally information about the one or more latency paths. This information can be transmitted prior to determining how to configure the latency paths to support the application requirements. Based on this information, one of the modems can select an FCI configuration parameter(s) that meets the transmission requirements of each application being transported over each latency paths. While an exemplary of the embodiment of the invention will be described in relation to the operation of the invention and characteristics thereof being established during initialization, it should be appreciated that the sharing of resources can be modified and messages transmitted between a two transceivers at any time during initialization and/or user data transmission, i.e., SHOWTIME.

[0038] Fig. 1 illustrates an exemplary embodiment of a transceiver 100. The transceiver 100 includes a transmitter portion 200 and a receiver portion 300. The transmitter portion 200 includes one or more latency paths 210, 220, ... Similarly, the receiver portion 300 includes one or more latency paths 310, 320, ... Each of the latency paths in the transmitter portion 200 includes a framer, coder, and interleaver designated as 212, 214, 216 and 222, 224 and 226, respectively. Each of the latency paths in the receiver portion includes a deframer, decoder, and deinterleaver designated as 312, 314, 316 and 322, 324, and 326, respectively. The transceiver 100 further includes a shared processing module 110, a shared memory 120, a parameter

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determination module 130, a path module 140, an allocation module 150, and a shared resource management module 160, all interconnected by one or more links (not shown).

[0039] In this exemplary embodiment, the transceiver 100 is illustrated with four total transmitter portion and receiver portion latency paths, i.e., 210, 220, 310, and 320. The shared memory 120 is shared amongst the two transmitter portion interleavers 216 and 226 and two receiver portion deinterleavers 316 and 326. The shared processing module 110, such as a shared coding module, is shared between the two transmitter portion coders 214 and 224 and the two receiver portion decoders 314 and 324.

[0040] While the exemplary embodiment of the invention will be described in relation to a transceiver having a number of transmitter portion latency paths and receiver portion latency paths, it should be appreciated that this invention can be applied to any transceiver having any number of latency paths. Moreover, it should be appreciated that the sharing of resources can be allocated such that one or more of the transmitter portion latency paths are sharing a shared resource, one or more of the receiver portion latency paths are sharing a shared resource, or a portion of the transmitter portion latency paths and a portion of the receiver portion latency paths are sharing shared resources. Moreover, any one or more of the latency paths, or portions thereof, could also be assigned to a fixed resource while, for example, another portion of the latency path(s) assigned to a shared resource. For example, in latency path 210, the interleaver 216 could be allocated a portion of the shared

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memory 120, while the coder 214 could be allocated to a dedicated processing module, vice versa, or the like.

[0041] In accordance with the exemplary embodiment, a plurality of transmitter portion or receiver portion latency paths share an interleaver/deinterleaver memory, such as shared memory 120, and a coding module, such as shared processing module 110. For example, the interleaver/deinterleaver memory can be allocated to different interleavers and/or deinterleavers. This allocation can be based on parameters associated with the communication systems such as data rate, latency, BER, impulse noise protection, and the like, of the applications being transported. Similarly, a coding module, which can be a portion of the shared processing module 110, can be shared between any one or more of the latency paths. This sharing can be based on requirements such as data rate, latency, BER, impulse noise protection, and the like, of the applications being transported.

[0042] For example, an exemplary transceiver could comprise a shared interleaver/deinterleaver memory and could be designed to allocate a first portion of the shared memory 120 to an interleaver, such as interleaver 216 in the transmitter portion of the transceiver and allocate a second portion of the shared memory 120 to a deinterleaver, such as 316, in the receiver portion of the transceiver.

[0043] Alternatively, for example, an exemplary transceiver can comprise a shared interleaver/deinterleaver memory, such as shared memory 120, and be designed to allocate a first portion of shared memory 120 to a first interleaver, e.g.,

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216, in the transmitter portion of the transceiver and allocate a second portion of the shared memory to a second interleaver, e.g., 226, in the transmitter portion of the transceiver.

[0044] Alternatively, for example, an exemplary transceiver can comprise a shared interleaver/deinterleaver memory and be designed to allocate a first portion of the shared memory 120 to a first deinterleaver, e.g., 316, in the receiver portion of the transceiver and allocate a second portion of the shared memory to a second deinterleaver, e.g., 326, in the receiver portion of the transceiver. Regardless of the configuration, in general any interleaver or deinterleaver, or grouping thereof, be it in a transmitter portion or receiver portion of the transceiver, can be associated with a portion of the shared memory 120.

[0045] Establishment, configuration and usage of shared resources is performed in the following exemplary manner. First, and in cooperation with the path module 140, the number of transmitter and receiver latency paths (N) is determined. The parameter determination module 130 then analyses one or more parameters such as data rate, transmitter data rate, receiver data rate, impulse noise protection, bit error rate, latency, or the like. Based on one or more of these parameters, the allocation module 150 allocates a portion of the shared memory 120 to one or more of the interleaver and/or deinterleavers, or groupings thereof. This process continues until the memory allocation has been determined and assigned to each of the N latency paths.

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[0046] Having determined the memory allocation for each of the latency paths, and in conjunction with the shared resource management 160, the transceiver 100 transmits to a second transceiver one or more of the number of latency paths (N), the maximum interleaver memory for any one or more of the latency paths and/or the maximum total and/or shared memory for all of the latency paths.

[0047] Three examples of sharing interleaver/deinterleaver memory and coding processing in a transceiver are described below. The latency paths in these examples can be in the transmitter portion of the transceiver or the receiver portion of the transceiver.

[0048] Example #1

A first transmitter portion or receiver portion latency path may carry data from a video application, which needs a very low BER but can tolerate higher latency. In this case, the video will be transported using an latency path that has a large amount of interleaving/deinterleaving and coding (also known as Forward Error Correction (FEC) coding). For example, the latency path may be configured with Reed-Solomon coding using a codeword size of 255 bytes (N=255) with 16 checkbytes (R=16) and interleaving/deinterleaving using an interleaver depth of 64 (D=64). This latency path will require N*D=16*255=16Kbytes of interleaver memory at the transmitter (or de-interleaver memory at the receiver). This latency path will be able to correct a burst of errors that is less than 512 bytes in duration.

[0049] A second transmitter portion or receiver portion latency path may carry an

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internet access application that requires a medium BER and a medium amount of latency. In this case, the internet access application will be transported using a latency path that has a medium amount of interleaving and coding. For example, the latency path may be configured with Reed-Solomon coding using a codeword size of 128 bytes (N=128) with 8 checkbytes (R=8) and interleaving using an interleaver depth of 16 (D=32). This latency path will require N*D=128*32=4Kbytes of interleaver memory and the same amount of deinterleaver memory. This latency path will be able to correct a burst of errors that is less than 128 bytes in duration.

[0050] A third transmitter portion or receiver portion latency path may carry a voice telephony application, which needs a very low latency but can tolerate BER. In this case, the video will be transported using an latency path that has a large amount of interleaving and coding. For example, the third transmitter portion or receiver portion latency path may be configured with no interleaving or coding which will result in the lowest possible latency through the latency path but will provide no error correction capability.

[0051] According to the principles of this invention, a system carrying the three applications described above in Example #1, would have three latency paths that share one memory space containing at least (16+4)=20 Kbytes. The three latency paths also share a common coding block that is able to simultaneously encode (in the transmitter portion) or decode (in a receiver portion) two codewords with N=255/R=16 and N=128/R=8.

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[0052] According to an exemplary embodiment of this invention, the latency paths can be reconfigured at initialization or during data transmission mode (also known as SHOWTIME in ADSL and VDSL transceivers). This would occur if, for example, the applications or application requirements were to change.

[0053] Example #2

If instead of 1 video application, 1 internet application and 1 voice application, there were 3 internet access applications then the transmitter portion and/or receiver portion latency paths would be reconfigured to utilize the shared memory and coding module in a different way. For example, the system could be reconfigured to have 3 transmitter portion or receiver portion latency paths, with each latency path being configured with Reed-Solomon coding using a codeword size of 128 bytes (N=128) with 8 checkbytes (R=8) and interleaving using an interleaver depth of 16 (D=32). Each latency path will require N*D=128*32=4Kbytes of interleaver memory and each block will be able to correct a burst of errors that is less than 128 bytes in duration. Based on the example of carrying the three internet access applications described, the three latency path share one memory space containing at least 3*4=12 Kbytes. Also the three latency paths share a common coding block that is able to simultaneously encode (on the transmitter side) or decode (on the receiver side) three codewords with N=128/R=16, N=128/R=8 and N=128/R=8.

[0054] Example #3

The system could be configured to carry yet another set of applications. For example, the latency paths could be configured to carry 2 video applications. In this case only

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2 transmitter portion or receiver portion latency paths are needed, which means that the third latency path could be simply disabled. Also, assuming that the memory is constrained based on the first example above, then the maximum shared memory for these 2 latency paths is 20 kBytes. In this case, the system could be reconfigured to have 2 latency paths, with each block being configured with Reed-Solomon coding using a codeword size of 200 bytes (N=200) with 10 checkbytes (R=10) and interleaving/deinterleaving using an interleaver depth of 50 (D=50). Each latency path will require N*D=200*50=10Kbytes of interleaver memory and each block will be able to correct a burst of errors that is less than 250 bytes in duration. This configuration results in 20K of shared memory for both latency paths, which is the same as in the first example. In order to stay within the memory constraints of the latency paths, the error correction capability for each latency path is decreased to 250 bytes from 512 bytes in Example #1.

[0055] Another aspect of this invention is the how FCI configuration information is transmitted between a first modem and a second modem. FCI configuration information will depend on the requirements of the applications being transported over the DSL connection. This information may need to be forwarded during initialization in order to initially configure the DSL connection. This information may also need to be forwarded during SHOWTIME in order to reconfigure the DSL connection based on a change in applications or the application requirements.

[0056] According to one embodiment, a first modem determines the specific FCI configuration parameters, e.g,. N, D, R as defined above, needed to meet specific

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application requirements, such as latency, burst error correction capability, etc. In order to determine the FCI configuration parameters, the first modem must know what are the capabilities of a second modem. For example, the first modem must know how many latency paths (FCI blocks) the second modem can support. Also the first modem must know the maximum amount of interleaver memory for each transmitter latency path. In addition, since the transmitter latency paths may share a common memory space the first modem must know the total shared memory for all transmitter latency paths. This way the first modem will be able to choose a configuration that can meet application requirements and also meet the transmitter portion latency path capabilities of the second modem.

[0057] For example, using values from examples above, a first transceiver could send a message to a second transceiver during initialization or during SHOWTIME containing the following information:

- Number of supported transmitter and receiver latency paths = 3
- Max Interleaver Memory for latency path #1= 16 Kbytes
- Max Interleaver Memory for latency path #2= 16 Kbytes
- Max Interleaver Memory for latency path #3= 16 Kbytes
- Maximum total/shared memory for all latency paths = 20 kBytes

Based on this information, and the application requirements, the first transceiver would select latency path settings. For example, if the applications are 1 video, 1 internet access and 1 voice application, the first transceiver could configure 3 latency paths as follows:

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latency path #1 – Video: N=255, R=16, D=64

latency path #2 – Video: N=128, R=8, D=32

latency path #3 – Video: N=0, R=0, D=1 (no coding or interleaving)

[0058] This would result in a total interleaver memory of 20 kbytes.

[0059] Alternatively, if for example, there are only 2 video applications, the first transceiver could configure 2 latency paths as follows:

latency path #1 – Video: N=200, R=10, D=50

latency path #2 – Video: N=200, R=10, D=50

latency path #3 – Video: N=0, R=0, D=1 (no coding or interleaving)

[0060] This would also result in a total interleaver memory of 20 kbytes.

[0061] Alternatively, the second transceiver can determine the specific FCI configuration parameters, e.g., N, D, R as defined above, needed to meet specific application requirements, such as latency, burst error correction capability, etc. As described above for the first transceiver, in order to determine the FCI configuration parameters, the second transceiver must first know what are the capabilities of the first transceiver. In this case, the first transceiver would send a message to the second transceiver containing the information described above and based on this information and the application requirements the second transceiver would select latency path settings.

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[0062] Fig. 2 outlines an exemplary method of allocating shared memory in a transceiver. More specifically, control begins in step S200 and continues to step S210. In step S210, one or more of shared interleaver/deinterleaver memory and/or shared coder/decoder processing resources are allocated to one or more latency paths, in a transceiver. Control then continues to step S220 where the control sequence ends.

[0063] Fig. 3 outlines an exemplary method of exchanging shared resource allocations according to an exemplary embodiment of this invention. In particular, control begins in step S310. In step S310, a maximum amount of shared memory that can be allocated to a specific interleaver or deinterleaver of a plurality of interleavers or deinterleavers in a transceiver is determined. Next, in step S320, the determined maximum amount for one or more of the deinterleavers and/or interleavers is transmitted to another transceiver. Messages containing additional information can also be transmitted to the other transceiver and/or received from the other transceiver. Control then continues to step S330 where the control sequence ends.

[0064] Fig. 4 outlines an exemplary procedure for resource sharing according to an exemplary embodiment of this invention. In particular, control begins in step S400 and continues to step S410. In step S410, the number of latency paths are determined. Then, in step S420, the latency path information (FCI block information) is transmitted to another transceiver. Messages containing additional information can also be transmitted to the other transceiver and/or received from the other transceiver. This information can be used to, for example, assist with the determination of

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memory allocation in the transceiver. Moreover, the messages received from the other transceiver could specify what the memory allocation is to be based on, for example, the number of latency paths, memory allocation in the remote transceiver and required applications. Control then continues to step S430.

[0065] In step S430, and for each latency path, the steps in step 440 are performed.

[0066] In step S440, and while monitoring of allocation of resources is being performed, steps 450 and 460 are performed. More specifically, in step S450, one or more parameters associated with the communication system are determined. Then, in step S460, shared resources are allocated based on one or more of the communication parameters. Control then continues to step S470.

[0067] In step S470, the allocation of shared resources is communicated to another transceiver. Next, in step S480, a determination is made as to whether there is a change in communications that would require the adjustment of the shared resource allocation. Examples of changes in communications conditions include a change in applications being transported over the system and/or changes in the channel condition, etc. If adjustments are required, control jumps back to step S410. Otherwise, control jumps to step S490 where the control sequence ends.

[0068] The above-described system can be implemented on wired and/or wireless telecommunications devices, such a modem, a multicarrier modem, a DSL modem, an

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ADSL modem, an XDSL modem, a VDSL modem, a linecard, test equipment, a multicarrier transceiver, a wired and/or wireless wide/local area network system, a satellite communication system, a modem equipped with diagnostic capabilities, or the like, or on a separate programmed general purpose computer having a communications device or in conjunction with any of the following communications protocols: CDSL, ADSL2, ADSL2+, VDSL1, VDSL2, HDSL, DSL Lite, IDSL, RADSL, SDSL, UDSL or the like.

[0069] Additionally, the systems, methods and protocols of this invention can be implemented on a special purpose computer, a programmed microprocessor or microcontroller and peripheral integrated circuit element(s), an ASIC or other integrated circuit, a digital signal processor, a hard-wired electronic or logic circuit such as discrete element circuit, a programmable logic device such as PLD, PLA, FPGA, PAL, a modem, a transmitter/receiver, any comparable means, or the like. In general, any device capable of implementing a state machine that is in turn capable of implementing the methodology illustrated herein can be used to implement the various communication methods, protocols and techniques according to this invention.

[0070] Furthermore, the disclosed methods may be readily implemented in software using object or object-oriented software development environments that provide portable source code that can be used on a variety of computer or workstation platforms. Alternatively, the disclosed system may be implemented partially or fully in hardware using standard logic circuits or VLSI design. Whether software or

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hardware is used to implement the systems in accordance with this invention is dependent on the speed and/or efficiency requirements of the system, the particular function, and the particular software or hardware systems or microprocessor or microcomputer systems being utilized. The communication systems, methods and protocols illustrated herein can be readily implemented in hardware and/or software using any known or later developed systems or structures, devices and/or software by those of ordinary skill in the applicable art from the functional description provided herein and with a general basic knowledge of the computer and telecommunications arts.

[0071] Moreover, the disclosed methods may be readily implemented in software that can be stored on a storage medium, executed on programmed general-purpose computer with the cooperation of a controller and memory, a special purpose computer, a microprocessor, or the like. In these instances, the systems and methods of this invention can be implemented as program embedded on personal computer such as an applet, JAVA® or CGI script, as a resource residing on a server or computer workstation, as a routine embedded in a dedicated communication system or system component, or the like. The system can also be implemented by physically incorporating the system and/or method into a software and/or hardware system, such as the hardware and software systems of a communications transceiver.

[0072] It is therefore apparent that there has been provided, in accordance with the present invention, systems and methods for sharing resources. While this invention has been described in conjunction with a number of embodiments, it is

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evident that many alternatives, modifications and variations would be or are apparent to those of ordinary skill in the applicable arts. Accordingly, it is intended to embrace all such alternatives, modifications, equivalents and variations that are within the spirit and scope of this invention.

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Claims:

1. A method for sharing resources in a transceiver comprising:
allocating a first portion of shared memory to a first latency path and allocating a second portion of the shared memory to a second latency path.

2. The method of claim 1, wherein the first latency path includes an interleaver and the second latency path includes an interleaver.

3. The method of claim 1, wherein the first latency path includes an interleaver and the second latency path includes a deinterleaver.

4. The method of claim 1, wherein the first latency path includes a deinterleaver and the second latency path includes a deinterleaver.

5. The method of claim 1, further comprising transmitting to another transceiver information that is used to determine a maximum amount of shared memory that can be allocated.

6. The method of claim 1, further comprising receiving from another transceiver information that is used to determine a maximum amount of shared memory that can be allocated.

7. The method of claim 1, further comprising allocating a shared processing module to a plurality of coding and/or decoding modules.

8. The method of claim 1, wherein the allocating of at least one portion of the shared memory is based on one or more communication parameters.

9. The method of claim 8, wherein at least one of the communication parameters is a data rate, a latency, an INP value or a bit error rate (BER).

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10. A transceiver comprising:

a first portion of shared memory that is allocated to a first latency path; and

a second portion of the shared memory that is allocated to a second latency path.

11. The transceiver of claim 10, further comprising:

an allocation module designed to allocate the shared memory based on one or more communication parameters.

12. The transceiver of claim 11, wherein at least one of the communication parameters is a data rate, a latency, an INP value or a Bit Error Rate (BER).

13. The transceiver of claim 10, wherein the first latency path includes an interleaver and the second latency path includes an interleaver.

14. The transceiver of claim 10, wherein the first latency path includes an interleaver and the second latency path includes a deinterleaver.

15. The transceiver of claim 10, wherein the first latency path includes a deinterleaver and the second latency path includes a deinterleaver.

16. The transceiver of claim 10, further comprising a shared resource management module designed to determine information that is transmitted to another transceiver, wherein the information is used to determine a maximum amount of shared memory that can be allocated.

17. The transceiver of claim 10, further comprising a shared resource management module designed to utilize information that is received from another transceiver, wherein the information is used to determine a maximum amount of shared memory that can be allocated.

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18. The transceiver of claim 10, further comprising a shared processing module designed to provide processing resources to a plurality of coding and/or decoding modules.

19. A system for sharing resources in a transceiver comprising:

means for allocating a first portion of shared memory to a first latency path and means for allocating a second portion of the shared memory to a second latency path.

20. The system of claim 19, wherein the first latency path includes an interleaver and the second latency path includes an interleaver.

21. The system of claim 19, wherein the first latency path includes an interleaver and the second latency path includes a deinterleaver.

22. The system of claim 19, wherein the first latency path includes a deinterleaver and the second latency path includes a deinterleaver.

23. The system of claim 19, further comprising means for transmitting to another transceiver information that is used to determine a maximum amount of shared memory that can be allocated.

24. The system of claim 19, further comprising means for receiving from another transceiver information that is used to determine a maximum amount of shared memory that can be allocated.

25. The system of claim 19, further comprising means for allocating a shared processing module to a plurality of coding and/or decoding modules.

26. The system of claim 19, wherein the allocating of at least one portion

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of the shared memory is based on one or more communication parameters.

27. The system of claim 26, wherein at least one of the communication parameters is a data rate, a latency, an INP value or a bit error rate (BER).

28. A protocol for sharing resources in a transceiver comprising:

allocating a first portion of shared memory to a first latency path and allocating a second portion of the shared memory to a second latency path.

29. The protocol of claim 28, wherein the first latency path includes an interleaver and the second latency path includes an interleaver.

30. The protocol of claim 28, wherein the first latency path includes an interleaver and the second latency path includes a deinterleaver.

31. The protocol of claim 28, wherein the first latency path includes a deinterleaver and the second latency path includes a deinterleaver.

32. The protocol of claim 28, further comprising transmitting to another transceiver information that is used to determine a maximum amount of shared memory that can be allocated.

33. The protocol of claim 28, further comprising receiving from another transceiver information that is used to determine a maximum amount of shared memory that can be allocated.

34. The protocol of claim 28, further comprising allocating a shared processing module to a plurality of coding and/or decoding modules.

35. The protocol of claim 28, wherein the allocating of at least one portion of the shared memory is based on one or more communication parameters.

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36. The protocol of claim 35, wherein at least one of the communication parameters is a data rate, a latency, an INP value or a bit error rate (BER).

37. An information storage media having stored thereon information that when executed allows sharing of resources in a transceiver comprising:

information that allocates a first portion of shared memory to a first latency path and information that allocates a second portion of the shared memory to a second latency path.

38. The media of claim 37, wherein the first latency path includes an interleaver and the second latency path includes an interleaver.

39. The media of claim 37, wherein the first latency path includes an interleaver and the second latency path includes a deinterleaver.

40. The media of claim 37, wherein the first latency path includes a deinterleaver and the second latency path includes a deinterleaver.

41. The media of claim 37, further comprising information that transmits to another transceiver information that is used to determine a maximum amount of shared memory that can be allocated.

42. The media of claim 37, further comprising information that receives from another transceiver information that is used to determine a maximum amount of shared memory that can be allocated.

43. The media of claim 37, further comprising information that allocates a shared processing module to a plurality of coding and/or decoding modules.

44. The media of claim 37, wherein the allocating of at least one portion of

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the shared memory is based on one or more communication parameters.

45. The media of claim 44, wherein at least one of the communication parameters is a data rate, a latency, an INP value or a bit error rate (BER).

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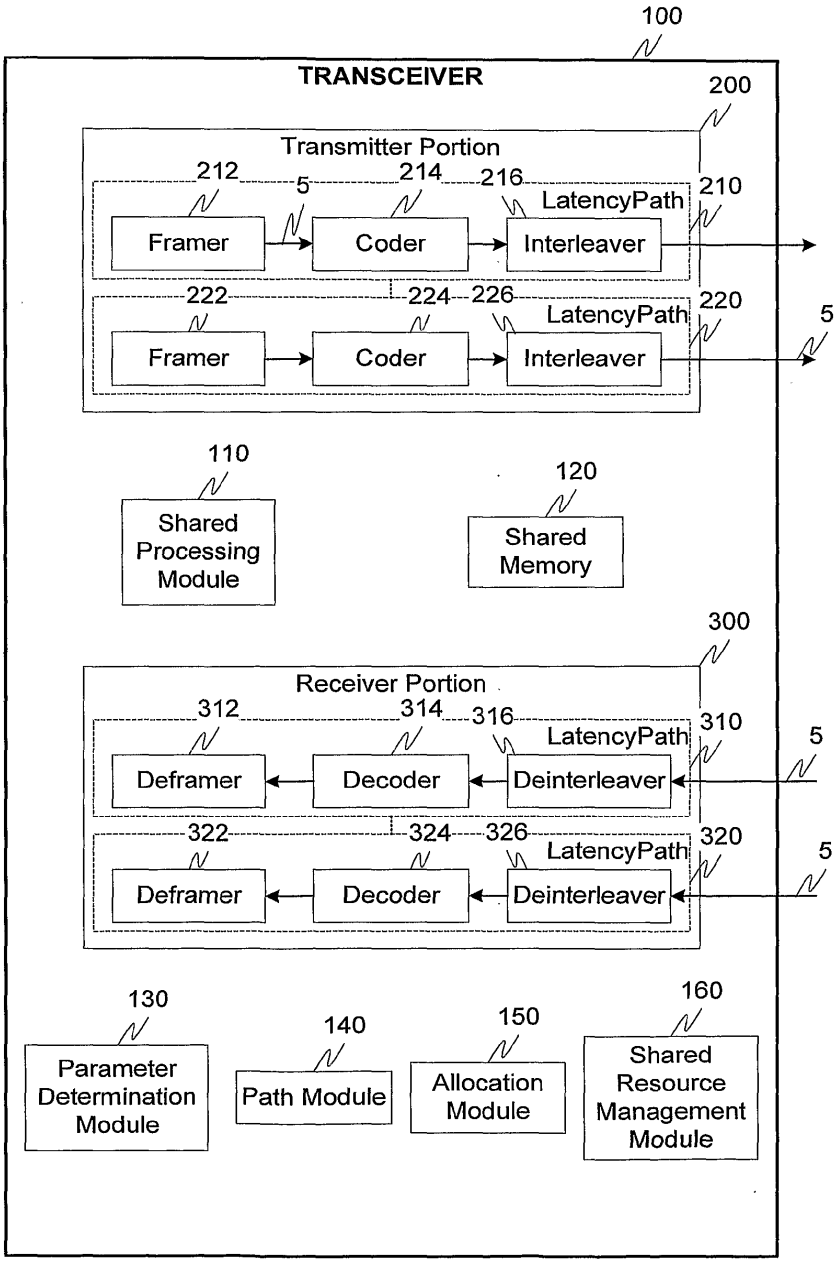
100
TRANSCEIVER
200
Transmitter Portion
212
5
214
216
LatencyPath
210
Framer
Coder
Interleaver
222
224
226
LatencyPath
220
5
Framer
Coder
Interleaver
110
Shared Processing Module
120
Shared Memory
300
Receiver Portion
312
314
316
LatencyPath
310
5
Deframer
Decoder
Deinterleaver
322
324
326
LatencyPath
320
5
Deframer
Decoder
Deinterleaver
130
Parameter Determination Module
140
Path Module
150
Allocation Module
160
Shared Resource Management Module

Fig. 1

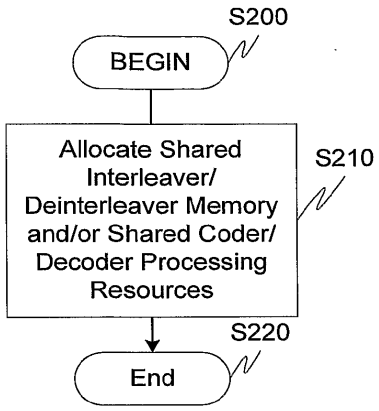
S200
BEGIN
Allocate Shared Interleaver/ Deinterleaver Memory and/or Shared Coder/ Decoder Processing Resources
S210
S220
End

Fig. 2

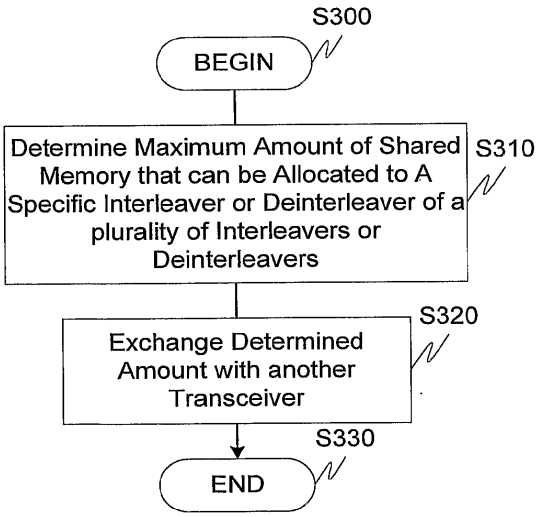
S300
BEGIN
Determine Maximum Amount of Shared Memory that can be Allocated to A Specific Interleaver or Deinterleaver of a plurality of Interleavers or Deinterleavers
S310
Exchange Determined Amount with another Transceiver
S320
S330
END

Fig. 3

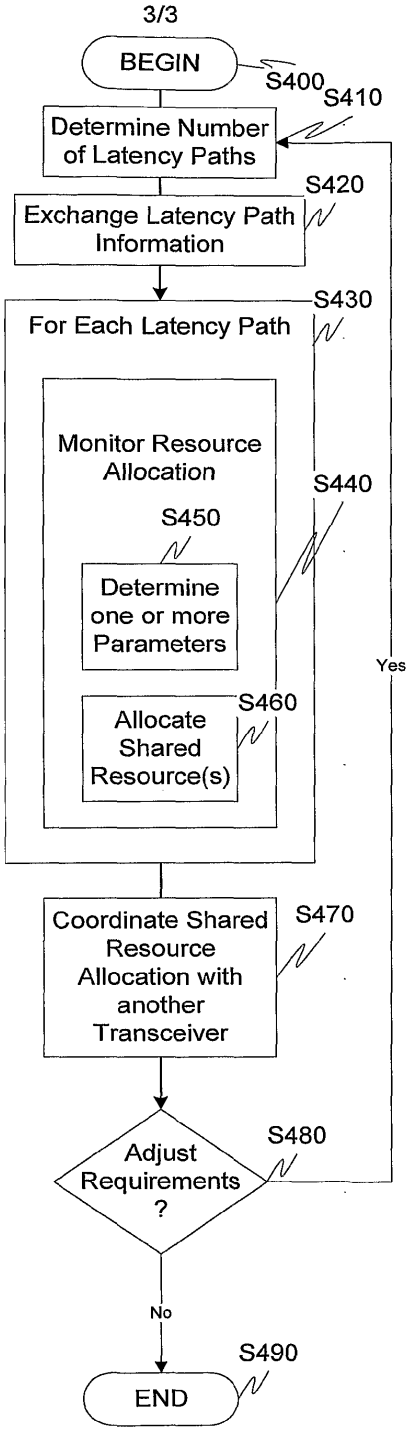
BEGIN
S400
S410
Determine Number of Latency Paths
S420
Exchange Latency Path Information
S430
For Each Latency Path
Monitor Resource Allocation
S440
S450
Determine one or more Parameters
S460
Allocate Shared Resource(s)
Yes
S470
Coordinate Shared Resource Allocation with another Transceiver
S480
Adjust Requirements ?
No
S490
END

Fig. 4

INTERNATIONAL SEARCH REPORT

International application No
PCT/US2005/036015

A. CLASSIFICATION OF SUBJECT MATTER
H04L1/00 H04L27/26

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
H04L

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practical, search terms used)
EPO-Internal, WPI Data

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	US 6 707 822 B1 (FADAVI-ARDEKANI JALIL ET AL) 16 March 2004 (2004-03-16) column 1, line 7 - column 2, line 59 column 3, line 5 - column 4, line 21 column 5, line 23 - column 7, line 33 column 8, line 4 - column 9, line 23 figure 2	1-45
A	WO 03/063060 A (BROADCOM CORPORATION) 31 July 2003 (2003-07-31) page 1, line 5 - page 2, line 27 page 17, line 4 - page 18, line 25 figures 1,4 page 7, line 13 - page 9, line 16	1-45

-/--

[X] Further documents are listed in the continuation of Box C.

[X] See patent family annex.

* Special categories of cited documents :

"A" document defining the general state of the art which is not considered to be of particular relevance

"E" earlier document but published on or after the international filing date

"L" document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)

"O" document referring to an oral disclosure, use, exhibition or other means

"P" document published prior to the international filing date but later than the priority date claimed

"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention

"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone

"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art.

"&" document member of the same patent family

Date of the actual completion of the international search	Date of mailing of the international search report
18 January 2006	08/02/2006

Name and mailing address of the ISA/	Authorized officer
European Patent Office, P.B. 5818 Patentlaan 2 NL – 2280 HV Rijswijk Tel. (+31-70) 340-2040, Tx. 31 651 epo nl, Fax: (+31-70) 340-3016	Marzenke, M

Form PCT/ISA/210 (second sheet) (April 2005)

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C(Continuation). DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
A	US 6 337 877 B1 (COLE TERRY L ET AL) 8 January 2002 (2002-01-08) column 3, line 21 - column 4, line 29 column 7, line 49 - column 8, line 67 figures 3,10	1-45
A	"SunSet xDSL: Prequalification of ADSL Circuits with ATU-C Emulation" 2001, SUNRISE TELECOM INC., APPLICATION SERIES , SAN JOSE, USA , XP002363272 Retrieved from the Internet: URL:http://www.sunrisetelecom.com/technotes/APP-xDSL-8B.pdf> 'retrieved on 2006-01-17! page 3, right-hand column, paragraph 1	1-45

CommScope, Inc.
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Page 220 of 531

INTERNATIONAL SEARCH REPORT

ırmation on patent family members

Interr[redacted]al application No
PCT/US2005/036015

Patent document cited in search report	Publication date	Patent family member(s)	Publication date
US 6707822 B1	16-03-2004	NONE	
WO 03063060 A	31-07-2003	EP 1476978 A2	17-11-2004
US 6337877 B1	08-01-2002	EP 1125408 A1 WO 0013387 A1	22-08-2001 09-03-2000

Form PCT/ISA/210 (patent family annex) (April 2005)

Electronic Acknowledgement Receipt	
EFS ID:	8181676
Application Number:	11246163
International Application Number:	
Confirmation Number:	5478
Title of Invention:	Resource sharing in a telecommunications environment
First Named Inventor/Applicant Name:	Marcos C. Tzannes
Customer Number:	62574
Filer:	Jason Vick/Carrie Steward
Filer Authorized By:	Jason Vick
Attorney Docket Number:	5550-54
Receipt Date:	09-AUG-2010
Filing Date:	11-OCT-2005
Time Stamp:	16:36:45
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	no

File Listing:

Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1		IDS_05.pdf	439386 60f08ff873c9beab8ddc9adcaf36058d660aafdd	yes	5

	Multipart Description/PDF files in .zip description				
	Document Description		Start	End	
	Transmittal Letter		1	3	
	Information Disclosure Statement (IDS) Filed (SB/08)		4	5	
Warnings:					
Information:					
2	Foreign Reference	EP1225735A1.pdf	3319471 ab5e96001141a40a16fbef205e87ae59cad92e43	no	30
Warnings:					
Information:					
3	Foreign Reference	EP1246409A1.pdf	4522291 bfa232f471ba2a3d6ef7c8db6f2f3a099e58283e	no	38
Warnings:					
Information:					
4	Foreign Reference	WO2006044227A1.pdf	1310271 c7b3442410420f8d83cd5d28ad5a10bbfd968faa	no	37
Warnings:					
Information:					
5	NPL Documents	Shoji_WIRELESS_ACCESS_METHOD_TO_ENSURE.pdf	1414514 e83281e015c9e4830594f9ec1232d0704b8e0314	no	14
Warnings:					
Information:					
6	NPL Documents	ITU-T_Recommendation_G_992_5.pdf	3754491 12d286f0ed80aef8c6897e43ec6a7ca902a6811d	no	92
Warnings:					
Information:					
7	NPL Documents	ITU-T_G_992_3.pdf	7371505 eda53373e7c854022481a11df6724b43946e015d	no	436
Warnings:					
Information:					
8	NPL Documents	ITU_T_G993_2_PTO.pdf	14564578 f7e8bb8a9ab0e59f6da3e2ac878c50b65e128c49	no	252
Warnings:					
Information:					
		Total Files Size (in bytes):	36696507		

This Acknowledgement Receipt evidences receipt on the noted date by the USPTO of the indicated documents, characterized by the applicant, and including page counts, where applicable. It serves as evidence of receipt similar to a Post Card, as described in MPEP 503.

New Applications Under 35 U.S.C. 111
If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application.

National Stage of an International Application under 35 U.S.C. 371
If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.

New International Application Filed with the USPTO as a Receiving Office
If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In Re the Application of:	)	Group Art Unit: 2447
LUND, MICHAEL	)	Confirmation No.: 5478
Serial No.: 11/246,163	)	Examiner: Mark C. Pfizenmayer
Filed: October 11, 2005	)	
Atty. File No.: 5550-54	)	SUPPLEMENTAL INFORMATION DISCLOSURE STATEMENT
Entitled: "RESOURCE SHARING IN A TELECOMMUNICATIONS ENVIRONMENT"	)	Electronically Submitted

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Dear Sir:

The references cited on attached Form PTO-1449 are being called to the attention of the Examiner.

☒ Copies of the cited non-patent and/or foreign references are enclosed herewith.

☐ Copies of the cited U.S. patents and/or patent applications are enclosed herewith.

☒ Copies of the cited U.S. patents/patent application publications are not enclosed in accordance with 37 C.F.R. § 1.98(a).

☐ Copies of the cited references are not enclosed, in accordance with 37 C.F.R. § 1.98(d), because the references were cited by or submitted to the U.S. Patent and Trademark Office in prior application Serial No. _____ filed _____, which is relied upon for an earlier filing date under 35 U.S.C. § 120.

☐ To the best of applicants' belief, the pertinence of the foreign-language references are believed to be summarized in the attached English abstracts and in the figures, although applicants do not necessarily vouch for the accuracy of the translation.

☒ Examiner's attention is drawn to the following related applications:

- Serial No. 12/761,586 filed 04/16/10 (Attorney's Ref. No. 5550-54-CON)
- Serial No. 12/295,828 filed 10/02/08 (Attorney's Ref. No. 5550-57-PUS)
- Serial No. 12/760,728 filed 04/15/10 (Attorney's Ref. No. 5550-57-PUS-DIV)
- Serial No. 12/783,758 filed 05/20/10 (Attorney's Ref. No. 5550-57-PUS-CON)

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- Serial No. 12/783,765 filed 05/20/10 (Attorney's Ref. No. 5550-57-PUS-DIV-CON)

☒ Other: Examiner's attention is drawn to the resubmission of Citation No. 11. It was erroneously cited as WO2006/04427on May 17, 2006. The correct citation is WO2006/0**44227**.

Submission of the above information is not intended as an admission that any item is citable under the statutes or rules to support a rejection, that any item disclosed represents analogous art, or that those skilled in the art would refer to or recognize the pertinence of any reference without the benefit of hindsight, nor should an inference be drawn as to the pertinence of the references based on the order in which they are presented. Submission of this statement should not be taken as an indication that a search has been conducted, or that no better art exists.

It is respectfully requested that the cited information be expressly considered during the prosecution of this application and the references made of record therein.

FEES

☒	**37 CFR 1.97(b)**: No fee is believed due in connection with this submission, because the information disclosure statement submitted herewith is satisfied by one of the following conditions ("X" indicates satisfaction): ☐ Within three months of the filing date of a national application other than a continued prosecution application under 37 CFR 1.53(d), or ☐ Within three months of the date of entry into the national stage of an international application as set forth in 37 CFR 1.491 or ☐ Before the mailing date of a first Office Action on the merits, or ☒ Before the mailing of a first Office action after the filing of a request for continued examination under 37 CFR 1.114. Although no fee is believed due, if any fee is deemed due in connection with this submission, please charge such fee to Deposit Account 19-1970.
☐	**37 CFR 1.97(c)**: The information disclosure statement transmitted herewith is being filed after all the above conditions (37 CFR 1.97(b)), but before the mailing date of one of the following conditions: (1) a final action under 37 C.F.R. 1.113 or (2) a notice of allowance under 37 C.F.R. 1.311, or (3) an action that otherwise closes prosecution in the application. This Information Disclosure Statement is accompanied by: ☐ A Certification (below) as specified by 37 C.F.R. 1.97(e). Although no fee is believed due, if any fee is deemed due in connection with this submission, please charge such fee to Deposit Account 19-1970. OR ☐ Please charge Deposit Account 19-1970 in the amount of $180.00 for the fee set forth in 37 C.F.R. 1.17(p) for submission of an information disclosure statement. Please credit any overpayment or charge any underpayment to Deposit Account 19-1970.
☐	**37 CFR 1.97(d)**: This Information Disclosure Statement is being submitted after the period specified in 37 CFR 1.97(c). ☐ This information Disclosure Statement includes a Certification (below) as specified by 37 C.F.R. 1.97(e) AND ☐ Applicants hereby requests consideration of the reference(s) disclosed herein. Please charge Deposit Account 19-1970 in the amount of $180.00 under 37 C.F.R. 1.17(p). Please credit any overpayment or charge any underpayment to Deposit Account 19-1970. Election to pay the fee should not be taken as an indication that applicant(s) cannot execute a certification.

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Page 226 of 531

Certification (37 C.F.R. 1.97(e))
(Applicable only if checked)

☐ The undersigned certifies that:

☐ Each item of information contained in this information disclosure statement was first cited in any communication from a foreign patent office in a counterpart foreign application not more than three months prior to the filing of this statement. 37 C.F.R. 1.97(e)(1).

☐ A copy of the communication from the foreign patent office is enclosed.

OR

☐ No item of information contained in this information disclosure statement was cited in a communication from a foreign patent office in a counterpart foreign application, and, to the knowledge of the undersigned after making reasonable inquiry, no item of information contained in this Information Disclosure Statement was known to any individual designated in 37 C.F.R. 1.56(c) more than three months prior to the filing of this statement. 37 C.F.R. 1.97(e)(2).

Respectfully submitted,

SHERIDAN ROSS P.C.

By: _____

Jason H. Vick
Registration No. 45,285
1560 Broadway, Suite 1200
Denver, Colorado 80202-5141
(303) 863-9700

Date: 9 Aug '10

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PLUS Search Results for S/N 11246163, Searched Mon Jul 12 08:12:56 EDT 2010

The Patent Linguistics Utility System (PLUS) is a USPTO automated search system for U.S. Patents from 1971 to the present PLUS is a query-by-example search system which produces a list of patents that are most closely related linguistically to the application searched. This search was prepared by the staff of the Scientific and Technical Information Center, SIRA.

20060088054 99
20090300450 84
5781549 66
5572686 66
6065101 66
6374332 66
6411418 66
6988173 66
7069362 66
7085898 66
7111130 66
20040054857 66
20040076044 66
20040230726 66
20040230751 66
20040230752 66
20060184750 66
20060246907 63
5477539 55
20100167780 55
20080232444 53
6195334 52
5644576 52
5898904 52
6674971 52
6690934 52
20070043945 52
20070076655 52
20090239548 52
5524234 52
6138208 52
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5307459 52
5337285 52
5412782 52
5485584 52
5498990 52
5526510 52
5537573 52
5613077 52
5649302 52
5713005 52
5729705 52
5734848 52
5737587 52
5805836 52
5815667 52
5831467 52
5844576 52
5872920 52

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In Re the Application of: Tzannes et al.	)	Group Art Unit: 2447
Application No.: 11/246,163	)	Examiner: Pfizenmayer, M.
Filed: October 11, 2005	)	Confirmation No.: 5478
Atty. File No.: 5550-54	)	

For: RESOURCE SHARING IN A TELECOMMUNICATIONS ENVIRONMENT

SUPPLEMENTAL AMENDMENT AND RESPONSE

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Sir:

Applicants submit this Amendment and Response supplemental to the Amendment and Response and RCE filed December 17, 2009. Please credit any overpayment or charge any underpayment to Deposit Account No. 19-1970.

Please amend the above-identified patent application as follows:

Amendments to the Claims are shown in the listing of claims which begins on page 2 of this paper.

Remarks begin on page 5 of this paper.

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IPR2023-00064, Ex. 1035
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Amendments to the Claims:

This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims:

1. – 45. (Cancelled)

46. (Currently Amended) A method of allocating shared memory in a transceiver comprising:

transmitting or receiving, by the transceiver, a message during initialization indicating a maximum number of bytes of memory that can be allocated to an interleaver;

allocating, in the transceiver, a first number of bytes of a shared memory to the interleaver to interleave a first plurality of Reed Solomon (RS) coded data bytes for transmission at a first data rate; and

allocating, in the transceiver, a second number of bytes of the shared memory to a deinterleaver to deinterleave a second plurality of RS coded data bytes received at a second data rate,

wherein the allocated memory for the interleaver does not exceed the maximum number of bytes indicated in the message, and

wherein the shared memory is used to simultaneously interleave the first plurality of RS coded data bytes and deinterleave the second plurality of RS coded data bytes.

47. (Previously Presented) The method of claim 46, wherein the allocating is based on an impulse noise protection requirement.

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48. (Previously Presented) The method of claim 46, wherein the allocating is based on a latency requirement.

49. (Previously Presented) The method of claim 46, wherein the allocating is based on a bit error rate requirement.

50. (Currently Amended) A method of allocating shared memory in a transceiver comprising:

transmitting or receiving, by the transceiver, a message during initialization indicating a maximum number of bytes of memory that can be allocated to a deinterleaver;

allocating, in the transceiver, a first number of bytes of a shared memory to an interleaver to interleave a first plurality of Reed Solomon (RS) coded data bytes for transmission at a first data rate; and

allocating, in the transceiver, a second number of bytes of the shared memory to the deinterleaver to deinterleave a second plurality of RS coded data bytes received at a second data rate,

wherein the allocated memory for the deinterleaver does not exceed the maximum number of bytes indicated in the message, and

wherein the shared memory is used to simultaneously interleave the first plurality of RS coded data bytes and deinterleave the second plurality of RS coded data bytes.

51. (Previously Presented) The method of claim 50, wherein the allocating is based on an impulse noise protection requirement.

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52. (Previously Presented) The method of claim 50, wherein the allocating is based on a latency requirement.

53. (Previously Presented) The method of claim 50, wherein the allocating is based on a bit error rate requirement.

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REMARKS

Applicants respectfully request reconsideration of this application as amended.

By this amendment, claims 46 and 50 have been amended to correct a typographical error. The combination of features in all the above claims is neither taught nor suggested by the cited reference.

A Notice of Allowance is earnestly solicited.

The Commissioner is hereby authorized to charge to deposit account number 19-1970 any fees under 37 CFR § 1.16 and 1.17 that may be required by this paper and to credit any overpayment to that Account. If any extension of time is required in connection with the filing of this paper and has not been separately requested, such extension is hereby petitioned.

Respectfully submitted,

SHERIDAN ROSS P.C.

Date: 8 Mar '10

By: _____

Jason H. Vick
Reg. No. 45,285
1560 Broadway, Suite 1200
Denver, Colorado 80202
Telephone: 303-863-9700

CommScope, Inc.
IPR2023-00064, Ex. 1035
Page 233 of 531

Electronic Acknowledgement Receipt	
EFS ID:	7163129
Application Number:	11246163
International Application Number:	
Confirmation Number:	5478
Title of Invention:	Resource sharing in a telecommunications environment
First Named Inventor/Applicant Name:	Marcos C. Tzannes
Customer Number:	62574
Filer:	Jason Vick/Joanne Vos
Filer Authorized By:	Jason Vick
Attorney Docket Number:	5550-54
Receipt Date:	08-MAR-2010
Filing Date:	11-OCT-2005
Time Stamp:	16:25:07
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	no

File Listing:

Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1		ThirdSupplementalAMENDwithRCE.pdf	45918 acc3dd5144f06e9617608d630bb6737f59a86027	yes	5

	Multipart Description/PDF files in .zip description		
	Document Description	**Start**	**End**
	Supplemental Response or Supplemental Amendment	1	1
	Claims	2	4
	Applicant Arguments/Remarks Made in an Amendment	5	5
Warnings:			
Information:			
	Total Files Size (in bytes):	45918	

This Acknowledgement Receipt evidences receipt on the noted date by the USPTO of the indicated documents, characterized by the applicant, and including page counts, where applicable. It serves as evidence of receipt similar to a Post Card, as described in MPEP 503.

New Applications Under 35 U.S.C. 111
If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application.

National Stage of an International Application under 35 U.S.C. 371
If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.

New International Application Filed with the USPTO as a Receiving Office
If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.

PTO/SB/06 (07-06)
Approved for use through 1/31/2007. OMB 0651-0032
U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE
Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it displays a valid OMB control number.

PATENT APPLICATION FEE DETERMINATION RECORD

Substitute for Form PTO-875

Application or Docket Number	Filing Date	☐ To be Mailed
11/246,163	10/11/2005	

APPLICATION AS FILED – PART I

	(Column 1)	(Column 2)	SMALL ENTITY ☐ RATE ($)	SMALL ENTITY ☐ FEE ($)	OR	OTHER THAN SMALL ENTITY RATE ($)	OTHER THAN SMALL ENTITY FEE ($)
FOR	NUMBER FILED	NUMBER EXTRA					
☐ BASIC FEE (37 CFR 1.16(a), (b), or (c))	N/A	N/A	N/A			N/A	
☐ SEARCH FEE (37 CFR 1.16(k), (l), or (m))	N/A	N/A	N/A			N/A	
☐ EXAMINATION FEE (37 CFR 1.16(o), (p), or (q))	N/A	N/A	N/A			N/A	
TOTAL CLAIMS (37 CFR 1.16(i))	minus 20 =	*	X $ =		OR	X $ =	
INDEPENDENT CLAIMS (37 CFR 1.16(h))	minus 3 =	*	X $ =			X $ =	
☐ APPLICATION SIZE FEE (37 CFR 1.16(s))	If the specification and drawings exceed 100 sheets of paper, the application size fee due is $250 ($125 for small entity) for each additional 50 sheets or fraction thereof. See 35 U.S.C. 41(a)(1)(G) and 37 CFR 1.16(s).						
☐ MULTIPLE DEPENDENT CLAIM PRESENT (37 CFR 1.16(j))							
* If the difference in column 1 is less than zero, enter "0" in column 2.			TOTAL			TOTAL	

APPLICATION AS AMENDED – PART II

AMENDMENT 03/08/2010

	(Column 1) CLAIMS REMAINING AFTER AMENDMENT		(Column 2) HIGHEST NUMBER PREVIOUSLY PAID FOR	(Column 3) PRESENT EXTRA	SMALL ENTITY RATE ($)	SMALL ENTITY ADDITIONAL FEE ($)	OR	OTHER THAN SMALL ENTITY RATE ($)	OTHER THAN SMALL ENTITY ADDITIONAL FEE ($)
Total (37 CFR 1.16(i))	* 8	Minus	** 45	= 0	X $ =		OR	X $52=	0
Independent (37 CFR 1.16(h))	* 2	Minus	***5	= 0	X $ =		OR	X $220=	0
☐ Application Size Fee (37 CFR 1.16(s))									
☐ FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))							OR		
					TOTAL ADD'L FEE		OR	TOTAL ADD'L FEE	0

AMENDMENT

	(Column 1) CLAIMS REMAINING AFTER AMENDMENT		(Column 2) HIGHEST NUMBER PREVIOUSLY PAID FOR	(Column 3) PRESENT EXTRA	RATE ($)	ADDITIONAL FEE ($)		RATE ($)	ADDITIONAL FEE ($)
Total (37 CFR 1.16(i))	*	Minus	**	=	X $ =		OR	X $ =	
Independent (37 CFR 1.16(h))	*	Minus	***	=	X $ =		OR	X $ =	
☐ Application Size Fee (37 CFR 1.16(s))									
☐ FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))							OR		
					TOTAL ADD'L FEE		OR	TOTAL ADD'L FEE	

* If the entry in column 1 is less than the entry in column 2, write "0" in column 3.

** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 20, enter "20".

*** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 3, enter "3".

The "Highest Number Previously Paid For" (Total or Independent) is the highest number found in the appropriate box in column 1.

Legal Instrument Examiner:
/Halley D. Massey/

This collection of information is required by 37 CFR 1.16. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 12 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

If you need assistance in completing the form, call 1-800-PTO-9199 and select option 2.

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In Re the Application of: Tzannes et al.	Group Art Unit: 2447
Application No.: 11/246,163	Examiner: Pfizenmayer, M.
Filed: October 11, 2005	Confirmation No.: 5478
Atty. File No.: 5550-54	

For: RESOURCE SHARING IN A TELECOMMUNICATIONS ENVIRONMENT

AMENDMENT AND RESPONSE

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Sir:

Applicants submit this Amendment and Response supplemental to the Amendment and Response and RCE filed December 17, 2009. Please credit any overpayment or charge any underpayment to Deposit Account No. 19-1970.

Please amend the above-identified patent application as follows:

Amendments to the Claims are shown in the listing of claims which begins on page 2 of this paper.

Remarks begin on page 4 of this paper.

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Page 237 of 531

Amendments to the Claims:

This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims:

1. – 45. (Cancelled)

46. (Currently Amended) A method of allocating shared memory in a transceiver comprising:

transmitting or receiving, by the transceiver, a message during initialization indicating a maximum number of bytes of memory that can be allocated to an interleaver;

allocating, in the transceiver, a first number of bytes of a shared memory to ~~an~~the interleaver to interleave a first plurality of Reed Solomon (RS) coded data bytes for transmission at a first data rate; and

allocating, in the transceiver, a second number of bytes of the shared memory to a deinterleaver to deinterleave a second plurality RS coded data bytes received at a second data rate,

wherein the allocated memory for the interleaver does not exceed the maximum number of bytes indicated in the message, and

wherein the shared memory is used to simultaneously interleave the first plurality of RS coded data bytes and deinterleave the second plurality of RS coded data bytes.

47. (Previously Presented) The method of claim 46, wherein the allocating is based on an impulse noise protection requirement.

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48. (Previously Presented) The method of claim 46, wherein the allocating is based on a latency requirement.

49. (Previously Presented) The method of claim 46, wherein the allocating is based on a bit error rate requirement.

50. (New) A method of allocating shared memory in a transceiver comprising:

transmitting or receiving, by the transceiver, a message during initialization indicating a maximum number of bytes of memory that can be allocated to a deinterleaver;

allocating, in the transceiver, a first number of bytes of a shared memory to an interleaver to interleave a first plurality of Reed Solomon (RS) coded data bytes for transmission at a first data rate; and

allocating, in the transceiver, a second number of bytes of the shared memory to the deinterleaver to deinterleave a second plurality RS coded data bytes received at a second data rate,

wherein the allocated memory for the deinterleaver does not exceed the maximum number of bytes indicated in the message, and

wherein the shared memory is used to simultaneously interleave the first plurality of RS coded data bytes and deinterleave the second plurality of RS coded data bytes.

51. (New) The method of claim 50, wherein the allocating is based on an impulse noise protection requirement.

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52. (New) The method of claim 50, wherein the allocating is based on a latency requirement.

53. (New) The method of claim 50, wherein the allocating is based on a bit error rate requirement.

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Page 240 of 531

REMARKS

Applicants respectfully request reconsideration of this application as amended.

By this amendment, claim 46 has been amended for antecedent basis, and new claims 50-53 are presented that more particularly claim a deinterleaver embodiment. The combination of features in all the above claims is neither taught nor suggested by the cited reference.

A Notice of Allowance is earnestly solicited.

The Commissioner is hereby authorized to charge to deposit account number 19-1970 any fees under 37 CFR § 1.16 and 1.17 that may be required by this paper and to credit any overpayment to that Account. If any extension of time is required in connection with the filing of this paper and has not been separately requested, such extension is hereby petitioned.

Respectfully submitted,

SHERIDAN ROSS P.C.

Date: 30 Dec '05

By: _____

Jason H. Vick
Reg. No. 45,285
1560 Broadway, Suite 1200
Denver, Colorado 80202
Telephone: 303-863-9700

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IPR2023-00064, Ex. 1035
Page 241 of 531

Electronic Acknowledgement Receipt	
EFS ID:	6725317
Application Number:	11246163
International Application Number:	
Confirmation Number:	5478
Title of Invention:	Resource sharing in a telecommunications environment
First Named Inventor/Applicant Name:	Marcos C. Tzannes
Customer Number:	62574
Filer:	Jason Vick
Filer Authorized By:	
Attorney Docket Number:	5550-54
Receipt Date:	30-DEC-2009
Filing Date:	11-OCT-2005
Time Stamp:	10:37:56
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	no

File Listing:

Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1		SupplementalAMD.pdf	271859 fd69adefa822170cd8996dbb44eca1b17d39f368	yes	5

	Multipart Description/PDF files in .zip description		
	Document Description	**Start**	**End**
	Amendment Submitted/Entered with Filing of CPA/RCE	1	1
	Claims	2	4
	Applicant Arguments/Remarks Made in an Amendment	5	5
Warnings:			
Information:			
	Total Files Size (in bytes):	271859	

This Acknowledgement Receipt evidences receipt on the noted date by the USPTO of the indicated documents, characterized by the applicant, and including page counts, where applicable. It serves as evidence of receipt similar to a Post Card, as described in MPEP 503.

New Applications Under 35 U.S.C. 111
If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application.

National Stage of an International Application under 35 U.S.C. 371
If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.

New International Application Filed with the USPTO as a Receiving Office
If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.

PTO/SB/06 (07-06)
Approved for use through 1/31/2007. OMB 0651-0032
U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE
Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it displays a valid OMB control number.

PATENT APPLICATION FEE DETERMINATION RECORD
Substitute for Form PTO-875

Application or Docket Number	Filing Date	☐ To be Mailed
11/246,163	10/11/2005	

APPLICATION AS FILED – PART I

	(Column 1)	(Column 2)	SMALL ENTITY ☐		OR	OTHER THAN SMALL ENTITY	
FOR	NUMBER FILED	NUMBER EXTRA	RATE ($)	FEE ($)		RATE ($)	FEE ($)
☐ BASIC FEE (37 CFR 1.16(a), (b), or (c))	N/A	N/A	N/A			N/A	
☐ SEARCH FEE (37 CFR 1.16(k), (l), or (m))	N/A	N/A	N/A			N/A	
☐ EXAMINATION FEE (37 CFR 1.16(o), (p), or (q))	N/A	N/A	N/A			N/A	
TOTAL CLAIMS (37 CFR 1.16(i))	minus 20 =	*	X $ =		OR	X $ =	
INDEPENDENT CLAIMS (37 CFR 1.16(h))	minus 3 =	*	X $ =			X $ =	
☐ APPLICATION SIZE FEE (37 CFR 1.16(s))	If the specification and drawings exceed 100 sheets of paper, the application size fee due is $250 ($125 for small entity) for each additional 50 sheets or fraction thereof. See 35 U.S.C. 41(a)(1)(G) and 37 CFR 1.16(s).						
☐ MULTIPLE DEPENDENT CLAIM PRESENT (37 CFR 1.16(j))							
* If the difference in column 1 is less than zero, enter "0" in column 2.			TOTAL			TOTAL	

APPLICATION AS AMENDED – PART II

AMENDMENT	12/30/2009	(Column 1) CLAIMS REMAINING AFTER AMENDMENT		(Column 2) HIGHEST NUMBER PREVIOUSLY PAID FOR	(Column 3) PRESENT EXTRA	SMALL ENTITY RATE ($)	ADDITIONAL FEE ($)	OR	OTHER THAN SMALL ENTITY RATE ($)	ADDITIONAL FEE ($)
	Total (37 CFR 1.16(i))	* 8	Minus	** 45	= 0	X $ =		OR	X $52=	0
	Independent (37 CFR 1.16(h))	* 2	Minus	***5	= 0	X $ =		OR	X $220=	0
	☐ Application Size Fee (37 CFR 1.16(s))									
	☐ FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))							OR		
						TOTAL ADD'L FEE		OR	TOTAL ADD'L FEE	0

AMENDMENT		(Column 1) CLAIMS REMAINING AFTER AMENDMENT		(Column 2) HIGHEST NUMBER PREVIOUSLY PAID FOR	(Column 3) PRESENT EXTRA	RATE ($)	ADDITIONAL FEE ($)	OR	RATE ($)	ADDITIONAL FEE ($)
	Total (37 CFR 1.16(i))	*	Minus	**	=	X $ =		OR	X $ =	
	Independent (37 CFR 1.16(h))	*	Minus	***	=	X $ =		OR	X $ =	
	☐ Application Size Fee (37 CFR 1.16(s))									
	☐ FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))							OR		
						TOTAL ADD'L FEE		OR	TOTAL ADD'L FEE	

* If the entry in column 1 is less than the entry in column 2, write "0" in column 3.
** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 20, enter "20".
*** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 3, enter "3".
The "Highest Number Previously Paid For" (Total or Independent) is the highest number found in the appropriate box in column 1.

Legal Instrument Examiner:
/SHARAIN MORELAND/

This collection of information is required by 37 CFR 1.16. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 12 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**
If you need assistance in completing the form, call 1-800-PTO-9199 and select option 2.

Substitute for form 1449A/PTO				Complete if Known	
INFORMATION DISCLOSURE STATEMENT BY APPLICANT				Application Number	11/246,163
				Filing Date	October 11, 2005
				First Named Inventor	LUND, MICHAEL
				Art Unit	2447
				Examiner Name	Mark C. Pfizenmayer
Sheet	1	of	1	Attorney Docket Number	5550-54

U.S. PATENT DOCUMENTS					
Examiner Initials*	Cite No.[1]	Document Number Number-kind Code [2] *(if known)*	Publication Date MM-DD-YYYY	Name of Patentee of Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear

FOREIGN PATENT DOCUMENTS						
Examiner Initials*	Cite No.[1]	Foreign Patent Document Country Code[3]; Number[4]; Kind Code[5] *(if known)*	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear	T[6]

OTHER ART (Including Author, Title, Date, Pertinent Pages, etc.)		
Examiner Initials*	Cite No.[1]	
	1	Notification of the First Office Action (including translation) for Chinese Patent Application No. 200580032703, mailed September 25, 2009 (Attorney's Ref. No. 5550-54-PCN)

Examiner Signature		Date Considered	

*EXAMINER: Initial if reference is considered, whether or not citation is in conformance and not considered. Include copy of this form with next communication to applicant.

Electronic Acknowledgement Receipt	
EFS ID:	6685276
Application Number:	11246163
International Application Number:	
Confirmation Number:	5478
Title of Invention:	Resource sharing in a telecommunications environment
First Named Inventor/Applicant Name:	Marcos C. Tzannes
Customer Number:	62574
Filer:	Jason Vick/Debra Kesner
Filer Authorized By:	Jason Vick
Attorney Docket Number:	5550-54
Receipt Date:	22-DEC-2009
Filing Date:	11-OCT-2005
Time Stamp:	10:29:54
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	no

File Listing:

Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1		IDS_04.pdf	329785 8ace9be081d92983f3564986e3200f73bccc8d44	yes	4

	Multipart Description/PDF files in .zip description				
	Document Description		Start	End	
	Transmittal Letter		1	3	
	Information Disclosure Statement (IDS) Filed (SB/08)		4	4	
Warnings:					
Information:					
2	NPL Documents	5550-54-PCN_OA_9-25-09.pdf	811648 107539c16c5da43ae8d1fe4d499847bfce058031	no	13
Warnings:					
Information:					
		Total Files Size (in bytes):	1141433		

This Acknowledgement Receipt evidences receipt on the noted date by the USPTO of the indicated documents, characterized by the applicant, and including page counts, where applicable. It serves as evidence of receipt similar to a Post Card, as described in MPEP 503.

New Applications Under 35 U.S.C. 111
If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application.

National Stage of an International Application under 35 U.S.C. 371
If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.

New International Application Filed with the USPTO as a Receiving Office
If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In Re the Application of:	)	Group Art Unit: 2447
LUND, MICHAEL	)	Confirmation No.: 5478
Serial No.: 11/246,163	)	Examiner: Mark C. Pfizenmayer
Filed: October 11, 2005	)	
Atty. File No.: 5550-54	)	INFORMATION DISCLOSURE STATEMENT
Entitled: "RESOURCE SHARING IN A TELECOMMUNICATIONS ENVIRONMENT"	)	Electronically Submitted

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Dear Sir:

The references cited on attached Form PTO-1449 are being called to the attention of the Examiner.

☒ Copies of the cited non-patent and/or foreign references are enclosed herewith.

☐ Copies of the cited U.S. patents and/or patent applications are enclosed herewith.

☐ Copies of the cited U.S. patents/patent application publications are not enclosed in accordance with 37 C.F.R. § 1.98(a).

☐ Copies of the cited references are not enclosed, in accordance with 37 C.F.R. § 1.98(d), because the references were cited by or submitted to the U.S. Patent and Trademark Office in prior application Serial No. _____ filed _____, which is relied upon for an earlier filing date under 35 U.S.C. § 120.

☐ To the best of applicants' belief, the pertinence of the foreign-language references are believed to be summarized in the attached English abstracts and in the figures, although applicants do not necessarily vouch for the accuracy of the translation.

☐ Examiner's attention is drawn to the following related applications:

Serial No. _____filed _____(Attorney's Ref. No. _____)

Serial No. _____filed _____(Attorney's Ref. No. _____)

☐ Other:_____

Submission of the above information is not intended as an admission that any item is citable under the statutes or rules to support a rejection, that any item disclosed represents analogous art, or that those skilled in the art would refer to or recognize the

CommScope, Inc.
IPR2023-00064, Ex. 1035
Page 248 of 531

pertinence of any reference without the benefit of hindsight, nor should an inference be drawn as to the pertinence of the references based on the order in which they are presented. Submission of this statement should not be taken as an indication that a search has been conducted, or that no better art exists.

It is respectfully requested that the cited information be expressly considered during the prosecution of this application and the references made of record therein.

FEES

☒	**37 CFR 1.97(b)**: No fee is believed due in connection with this submission, because the information disclosure statement submitted herewith is satisfied by one of the following conditions ("X" indicates satisfaction): ☐ Within three months of the filing date of a national application other than a continued prosecution application under 37 CFR 1.53(d), or ☐ Within three months of the date of entry into the national stage of an international application as set forth in 37 CFR 1.491 or ☐ Before the mailing date of a first Office Action on the merits, or ☒ Before the mailing of a first Office action after the filing of a request for continued examination under 37 CFR 1.114. Although no fee is believed due, if any fee is deemed due in connection with this submission, please charge such fee to Deposit Account 19-1970.
☐	**37 CFR 1.97(c)**: The information disclosure statement transmitted herewith is being filed after all the above conditions (37 CFR 1.97(b)), but before the mailing date of one of the following conditions: (1) a final action under 37 C.F.R. 1.113 or (2) a notice of allowance under 37 C.F.R. 1.311, or (3) an action that otherwise closes prosecution in the application. This Information Disclosure Statement is accompanied by: ☐ A Certification (below) as specified by 37 C.F.R. 1.97(e). Although no fee is believed due, if any fee is deemed due in connection with this submission, please charge such fee to Deposit Account 19-1970. OR ☐ Please charge Deposit Account 19-1970 in the amount of $180.00 for the fee set forth in 37 C.F.R. 1.17(p) for submission of an information disclosure statement. Please credit any overpayment or charge any underpayment to Deposit Account 19-1970.
☐	**37 CFR 1.97(d)**: This Information Disclosure Statement is being submitted after the period specified in 37 CFR 1.97(c). ☐ This information Disclosure Statement includes a Certification (below) as specified by 37 C.F.R. 1.97(e) AND ☐ Applicants hereby requests consideration of the reference(s) disclosed herein. Please charge Deposit Account 19-1970 in the amount of $180.00 under 37 C.F.R. 1.17(p). Please credit any overpayment or charge any underpayment to Deposit Account 19-1970. Election to pay the fee should not be taken as an indication that applicant(s) cannot execute a certification.

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IPR2023-00064, Ex. 1035
Page 249 of 531

Certification (37 C.F.R. 1.97(e))
(Applicable only if checked)

☐ The undersigned certifies that:

☐ Each item of information contained in this information disclosure statement was first cited in any communication from a foreign patent office in a counterpart foreign application not more than three months prior to the filing of this statement. 37 C.F.R. 1.97(e)(1).

☐ A copy of the communication from the foreign patent office is enclosed.

OR

☐ No item of information contained in this information disclosure statement was cited in a communication from a foreign patent office in a counterpart foreign application, and, to the knowledge of the undersigned after making reasonable inquiry, no item of information contained in this Information Disclosure Statement was known to any individual designated in 37 C.F.R. 1.56(c) more than three months prior to the filing of this statement. 37 C.F.R. 1.97(e)(2).

Respectfully submitted,

SHERIDAN ROSS P.C.

By: _____
Jason H. Vick
Registration No. 45,285
1560 Broadway, Suite 1200
Denver, Colorado 80202-5141
(303) 863-9700

Date: 22 Dec 09

CommScope, Inc.
IPR2023-00064, Ex. 1035
Page 250 of 531

PTO/SB/30EFS (07-09)
Approved for use through 07/31/2012. OMB 0651-0031
U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE

Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it contains a valid OMB control number.

REQUEST FOR CONTINUED EXAMINATION(RCE)TRANSMITTAL
(Submitted Only via EFS-Web)

Application Number	11246163	Filing Date	2005-10-11	Docket Number (if applicable)	5550-54	Art Unit	2447
First Named Inventor	Marcos C. Tzannes			Examiner Name	Pfizenmayer, Mark		

This is a Request for Continued Examination (RCE) under 37 CFR 1.114 of the above-identified application.
Request for Continued Examination (RCE) practice under 37 CFR 1.114 does not apply to any utility or plant application filed prior to June 8, 1995, or to any design application. The Instruction Sheet for this form is located at WWW.USPTO.GOV

SUBMISSION REQUIRED UNDER 37 CFR 1.114

Note: If the RCE is proper, any previously filed unentered amendments and amendments enclosed with the RCE will be entered in the order in which they were filed unless applicant instructs otherwise. If applicant does not wish to have any previously filed unentered amendment(s) entered, applicant must request non-entry of such amendment(s).

☐ Previously submitted. If a final Office action is outstanding, any amendments filed after the final Office action may be considered as a submission even if this box is not checked.

- ☐ Consider the arguments in the Appeal Brief or Reply Brief previously filed on _____
- ☐ Other _____

☒ Enclosed

- ☒ Amendment/Reply
- ☐ Information Disclosure Statement (IDS)
- ☐ Affidavit(s)/ Declaration(s)
- ☐ Other _____

MISCELLANEOUS

☐ Suspension of action on the above-identified application is requested under 37 CFR 1.103(c) for a period of months _____ (Period of suspension shall not exceed 3 months; Fee under 37 CFR 1.17(i) required)

☐ Other _____

FEES

☒ **The RCE fee under 37 CFR 1.17(e) is required by 37 CFR 1.114 when the RCE is filed.**
The Director is hereby authorized to charge any underpayment of fees, or credit any overpayments, to Deposit Account No 191970

SIGNATURE OF APPLICANT, ATTORNEY, OR AGENT REQUIRED

☒ Patent Practitioner Signature
☐ Applicant Signature

PTO/SB/30EFS (07-09)
Approved for use through 07/31/2012. OMB 0651-0031
U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE

Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it contains a valid OMB control number.

Signature of Registered U.S. Patent Practitioner			
Signature	/Jason H. Vick/	Date (YYYY-MM-DD)	2009-12-17
Name	Jason H. Vick	Registration Number	45285

This collection of information is required by 37 CFR 1.114. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.11 and 1.14. This collection is estimated to take 12 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450.

If you need assistance in completing the form, call 1-800-PTO-9199 and select option 2.

Privacy Act Statement

The Privacy Act of 1974 (P.L. 93-579) requires that you be given certain information in connection with your submission of the attached form related to a patent application or patent. Accordingly, pursuant to the requirements of the Act, please be advised that: (1) the general authority for the collection of this information is 35 U.S.C. 2(b)(2); (2) furnishing of the information solicited is voluntary; and (3) the principal purpose for which the information is used by the U.S. Patent and Trademark Office is to process and/or examine your submission related to a patent application or patent. If you do not furnish the requested information, the U.S. Patent and Trademark Office may not be able to process and/or examine your submission, which may result in termination of proceedings or abandonment of the application or expiration of the patent.

The information provided by you in this form will be subject to the following routine uses:

1. The information on this form will be treated confidentially to the extent allowed under the Freedom of Information Act (5 U.S.C. 552) and the Privacy Act (5 U.S.C. 552a). Records from this system of records may be disclosed to the Department of Justice to determine whether the Freedom of Information Act requires disclosure of these records.

2. A record from this system of records may be disclosed, as a routine use, in the course of presenting evidence to a court, magistrate, or administrative tribunal, including disclosures to opposing counsel in the course of settlement negotiations.

3. A record in this system of records may be disclosed, as a routine use, to a Member of Congress submitting a request involving an individual, to whom the record pertains, when the individual has requested assistance from the Member with respect to the subject matter of the record.

4. A record in this system of records may be disclosed, as a routine use, to a contractor of the Agency having need for the information in order to perform a contract. Recipients of information shall be required to comply with the requirements of the Privacy Act of 1974, as amended, pursuant to 5 U.S.C. 552a(m).

5. A record related to an International Application filed under the Patent Cooperation Treaty in this system of records may be disclosed, as a routine use, to the International Bureau of the World Intellectual Property Organization, pursuant to the Patent Cooperation Treaty.

6. A record in this system of records may be disclosed, as a routine use, to another federal agency for purposes of National Security review (35 U.S.C. 181) and for review pursuant to the Atomic Energy Act (42 U.S.C. 218(c)).

7. A record from this system of records may be disclosed, as a routine use, to the Administrator, General Services, or his/her designee, during an inspection of records conducted by GSA as part of that agency's responsibility to recommend improvements in records management practices and programs, under authority of 44 U.S.C. 2904 and 2906. Such disclosure shall be made in accordance with the GSA regulations governing inspection of records for this purpose, and any other relevant (i.e., GSA or Commerce) directive. Such disclosure shall not be used to make determinations about individuals.

8. A record from this system of records may be disclosed, as a routine use, to the public after either publication of the application pursuant to 35 U.S.C. 122(b) or issuance of a patent pursuant to 35 U.S.C. 151. Further, a record may be disclosed, subject to the limitations of 37 CFR 1.14, as a routine use, to the public if the record was filed in an application which became abandoned or in which the proceedings were terminated and which application is referenced by either a published application, an application open to public inspections or an issued patent.

9. A record from this system of records may be disclosed, as a routine use, to a Federal, State, or local law enforcement agency, if the USPTO becomes aware of a violation or potential violation of law or regulation.

Electronic Patent Application Fee Transmittal	
Application Number:	11246163
Filing Date:	11-Oct-2005
Title of Invention:	Resource sharing in a telecommunications environment
First Named Inventor/Applicant Name:	Marcos C. Tzannes
Filer:	Jason Vick/Joanne Vos
Attorney Docket Number:	5550-54
Filed as Large Entity	

Utility under 35 USC 111(a) Filing Fees

Description	Fee Code	Quantity	Amount	Sub-Total in USD($)
Basic Filing:				
Pages:				
Claims:				
Miscellaneous-Filing:				
Petition:				
Patent-Appeals-and-Interference:				
Post-Allowance-and-Post-Issuance:				
Extension-of-Time:				

Description	Fee Code	Quantity	Amount	Sub-Total in USD($)
Miscellaneous:				
Request for continued examination	1801	1	810	810
		Total in USD ($)		**810**

Electronic Acknowledgement Receipt	
EFS ID:	6661680
Application Number:	11246163
International Application Number:	
Confirmation Number:	5478
Title of Invention:	Resource sharing in a telecommunications environment
First Named Inventor/Applicant Name:	Marcos C. Tzannes
Customer Number:	62574
Filer:	Jason Vick/Joanne Vos
Filer Authorized By:	Jason Vick
Attorney Docket Number:	5550-54
Receipt Date:	17-DEC-2009
Filing Date:	11-OCT-2005
Time Stamp:	17:09:02
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	yes
Payment Type	Deposit Account
Payment was successfully received in RAM	$810
RAM confirmation Number	4244
Deposit Account	191970
Authorized User	
The Director of the USPTO is hereby authorized to charge indicated fees and credit any overpayment as follows: Charge any Additional Fees required under 37 C.F.R. Section 1.16 (National application filing, search, and examination fees) Charge any Additional Fees required under 37 C.F.R. Section 1.17 (Patent application and reexamination processing fees)	

Charge any Additional Fees required under 37 C.F.R. Section 1.19 (Document supply fees)

Charge any Additional Fees required under 37 C.F.R. Section 1.20 (Post Issuance fees)

Charge any Additional Fees required under 37 C.F.R. Section 1.21 (Miscellaneous fees and charges)

File Listing:

Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1		AMENDwithRCE.pdf	232157 c7e9ebbc79906fa7182350604499aa9fe7b576e9	yes	4

Multipart Description/PDF files in .zip description

Document Description	Start	End
Amendment After Final	1	1
Claims	2	3
Applicant Arguments/Remarks Made in an Amendment	4	4

Warnings:

Information:

2	Request for Continued Examination (RCE)	RCE.pdf	697433 af669f212339d50f0ac6434138497baf16299a3e	no	3

Warnings:

Information:

3	Fee Worksheet (PTO-875)	fee-info.pdf	29818 8fc24dae60487e5945f726cc0c0a8e741fb6dd38	no	2

Warnings:

Information:

Total Files Size (in bytes):	959408

This Acknowledgement Receipt evidences receipt on the noted date by the USPTO of the indicated documents, characterized by the applicant, and including page counts, where applicable. It serves as evidence of receipt similar to a Post Card, as described in MPEP 503.

New Applications Under 35 U.S.C. 111
If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application.

National Stage of an International Application under 35 U.S.C. 371
If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.

New International Application Filed with the USPTO as a Receiving Office
If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In Re the Application of: Tzannes et al.	Group Art Unit: 2447
Application No.: 11/246,163	Examiner: Pfizenmayer, M.
Filed: October 11, 2005	Confirmation No.: 5478
Atty. File No.: 5550-54	

For: RESOURCE SHARING IN A TELECOMMUNICATIONS ENVIRONMENT

AMENDMENT AND RESPONSE

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Sir:

Applicants submit this Amendment and Response to address the Final Office Action having a mailing date of December 9, 2009. Please credit any overpayment or charge any underpayment to Deposit Account No. 19-1970.

Please amend the above-identified patent application as follows:

Amendments to the Claims are shown in the listing of claims which begins on page 2 of this paper.

Remarks begin on page 4 of this paper.

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Amendments to the Claims:

This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims:

1. – 45. (Cancelled)

46. (New) A method of allocating shared memory in a transceiver comprising:

transmitting or receiving, by the transceiver, a message during initialization indicating a maximum number of bytes of memory that can be allocated to an interleaver;

allocating, in the transceiver, a first number of bytes of a shared memory to an interleaver to interleave a first plurality of Reed Solomon (RS) coded data bytes for transmission at a first data rate; and

allocating, in the transceiver, a second number of bytes of the shared memory to a deinterleaver to deinterleave a second plurality RS coded data bytes received at a second data rate,

wherein the allocated memory for the interleaver does not exceed the maximum number of bytes indicated in the message, and

wherein the shared memory is used to simultaneously interleave the first plurality of RS coded data bytes and deinterleave the second plurality of RS coded data bytes.

47. (New) The method of claim 46, wherein the allocating is based on an impulse noise protection requirement.

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48. (New) The method of claim 46, wherein the allocating is based on a latency requirement.

49. (New) The method of claim 46, wherein the allocating is based on a bit error rate requirement.

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Page 261 of 531

REMARKS

Applicants respectfully request reconsideration of this application as amended.

By this amendment, the pending claims have been cancelled without prejudice or disclaimer in favor of the newly presented claims.

Applicants would like to thank Examiners Pfizenmayer and Bruckhart for the courtesies extended during the December 8, 2009 Personal Interview and during the subsequent email exchanges. During the interview, the general operation of the invention was discussed and it was agreed that the proposed amendments to the claims "were a step in the right direction." The Examiner also suggested additional features for the claim.

By this amendment, new claim 46 is presented that more particularly claims certain aspects of the invention. The combination of features in claim 46 is neither taught nor suggested by the cited reference.

In that all objections are rejections are moot, and the pending claims are patentably distinguishable from the reference, a Notice of Allowance is earnestly solicited.

The Commissioner is hereby authorized to charge to deposit account number 19-1970 any fees under 37 CFR § 1.16 and 1.17 that may be required by this paper and to credit any overpayment to that Account. If any extension of time is required in connection with the filing of this paper and has not been separately requested, such extension is hereby petitioned.

Respectfully submitted,

SHERIDAN ROSS P.C.

Date: 17 Dec '09

By: _____

Jason H. Vick
Reg. No. 45,285
1560 Broadway, Suite 1200
Denver, Colorado 80202
Telephone: 303-863-9700

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PTO/SB/06 (07-06)
Approved for use through 1/31/2007. OMB 0651-0032
U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE
Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it displays a valid OMB control number.

PATENT APPLICATION FEE DETERMINATION RECORD
Substitute for Form PTO-875

Application or Docket Number	Filing Date	☐ To be Mailed
11/246,163	10/11/2005	

APPLICATION AS FILED – PART I

	(Column 1)	(Column 2)	SMALL ENTITY ☐ RATE ($)	SMALL ENTITY ☐ FEE ($)	OR	OTHER THAN SMALL ENTITY RATE ($)	OTHER THAN SMALL ENTITY FEE ($)
FOR	NUMBER FILED	NUMBER EXTRA					
☐ BASIC FEE (37 CFR 1.16(a), (b), or (c))	N/A	N/A	N/A			N/A	
☐ SEARCH FEE (37 CFR 1.16(k), (l), or (m))	N/A	N/A	N/A			N/A	
☐ EXAMINATION FEE (37 CFR 1.16(o), (p), or (q))	N/A	N/A	N/A			N/A	
TOTAL CLAIMS (37 CFR 1.16(i))	minus 20 =	*	X $ =		OR	X $ =	
INDEPENDENT CLAIMS (37 CFR 1.16(h))	minus 3 =	*	X $ =			X $ =	
☐ APPLICATION SIZE FEE (37 CFR 1.16(s))	If the specification and drawings exceed 100 sheets of paper, the application size fee due is $250 ($125 for small entity) for each additional 50 sheets or fraction thereof. See 35 U.S.C. 41(a)(1)(G) and 37 CFR 1.16(s).						
☐ MULTIPLE DEPENDENT CLAIM PRESENT (37 CFR 1.16(j))							
* If the difference in column 1 is less than zero, enter "0" in column 2.			TOTAL			TOTAL	

APPLICATION AS AMENDED – PART II

AMENDMENT 12/17/2009

	(Column 1) CLAIMS REMAINING AFTER AMENDMENT		(Column 2) HIGHEST NUMBER PREVIOUSLY PAID FOR	(Column 3) PRESENT EXTRA	SMALL ENTITY RATE ($)	SMALL ENTITY ADDITIONAL FEE ($)	OR	OTHER THAN SMALL ENTITY RATE ($)	OTHER THAN SMALL ENTITY ADDITIONAL FEE ($)
Total (37 CFR 1.16(i))	* 4	Minus	** 45	= 0	X $ =		OR	X $52=	0
Independent (37 CFR 1.16(h))	* 1	Minus	***5	= 0	X $ =		OR	X $220=	0
☐ Application Size Fee (37 CFR 1.16(s))									
☐ FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))							OR		
					TOTAL ADD'L FEE		OR	TOTAL ADD'L FEE	0

AMENDMENT

	(Column 1) CLAIMS REMAINING AFTER AMENDMENT		(Column 2) HIGHEST NUMBER PREVIOUSLY PAID FOR	(Column 3) PRESENT EXTRA	RATE ($)	ADDITIONAL FEE ($)		RATE ($)	ADDITIONAL FEE ($)
Total (37 CFR 1.16(i))	*	Minus	**	=	X $ =		OR	X $ =	
Independent (37 CFR 1.16(h))	*	Minus	***	=	X $ =		OR	X $ =	
☐ Application Size Fee (37 CFR 1.16(s))									
☐ FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))							OR		
					TOTAL ADD'L FEE		OR	TOTAL ADD'L FEE	

* If the entry in column 1 is less than the entry in column 2, write "0" in column 3.
** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 20, enter "20".
*** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 3, enter "3".
The "Highest Number Previously Paid For" (Total or Independent) is the highest number found in the appropriate box in column 1.

Legal Instrument Examiner:
/Fennell A. Pearlie/

This collection of information is required by 37 CFR 1.16. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 12 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**
If you need assistance in completing the form, call 1-800-PTO-9199 and select option 2.

UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
11/246,163	10/11/2005	Marcos C. Tzannes	5550-54	5478

62574 7590 12/16/2009

Jason H. Vick
Sheridan Ross, PC
Suite # 1200
1560 Broadway
Denver, CO 80202

EXAMINER	
PFIZENMAYER, MARK C	
ART UNIT	**PAPER NUMBER**
2447	

NOTIFICATION DATE	DELIVERY MODE
12/16/2009	ELECTRONIC

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

jvick@sheridanross.com

Interview Summary	Application No.	Applicant(s)	
	11/246,163	TZANNES ET AL.	
	Examiner	Art Unit	
	BENJAMIN R. BRUCKART	2446	

All participants (applicant, applicant's representative, PTO personnel):

(1) *BENJAMIN R. BRUCKART*.

(2) *Pfizenmayer, Mark*.

(3)*Jason H Vick, Reg. No. 45, 285*.

(4)*Inventor Marcos Tzannes*.

Date of Interview: *08 December 2009*.

Type: a)☐ Telephonic b)☐ Video Conference
c)☒ Personal [copy given to: 1)☒ applicant 2)☐ applicant's representative]

Exhibit shown or demonstration conducted: d)☐ Yes e)☐ No.
If Yes, brief description: _____.

Claim(s) discussed: *1*.

Identification of prior art discussed: *N/A*.

Agreement with respect to the claims f)☐ was reached. g)☒ was not reached. h)☐ N/A.

Substance of Interview including description of the general nature of what was agreed to if an agreement was reached, or any other comments: *See Continuation Sheet*.

(A fuller description, if necessary, and a copy of the amendments which the examiner agreed would render the claims allowable, if available, must be attached. Also, where no copy of the amendments that would render the claims allowable is available, a summary thereof must be attached.)

THE FORMAL WRITTEN REPLY TO THE LAST OFFICE ACTION MUST INCLUDE THE SUBSTANCE OF THE INTERVIEW. (See MPEP Section 713.04). If a reply to the last Office action has already been filed, APPLICANT IS GIVEN A NON-EXTENDABLE PERIOD OF THE LONGER OF ONE MONTH OR THIRTY DAYS FROM THIS INTERVIEW DATE, OR THE MAILING DATE OF THIS INTERVIEW SUMMARY FORM, WHICHEVER IS LATER, TO FILE A STATEMENT OF THE SUBSTANCE OF THE INTERVIEW. See Summary of Record of Interview requirements on reverse side or on attached sheet.

/Benjamin R Bruckart/ Primary Examiner, Art Unit 2446	

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Summary of Record of Interview Requirements

Manual of Patent Examining Procedure (MPEP), Section 713.04, Substance of Interview Must be Made of Record
A complete written statement as to the substance of any face-to-face, video conference, or telephone interview with regard to an application must be made of record in the application whether or not an agreement with the examiner was reached at the interview.

Title 37 Code of Federal Regulations (CFR) § 1.133 Interviews
Paragraph (b)

In every instance where reconsideration is requested in view of an interview with an examiner, a complete written statement of the reasons presented at the interview as warranting favorable action must be filed by the applicant. An interview does not remove the necessity for reply to Office action as specified in §§ 1.111, 1.135. (35 U.S.C. 132)

37 CFR §1.2 Business to be transacted in writing.
All business with the Patent or Trademark Office should be transacted in writing. The personal attendance of applicants or their attorneys or agents at the Patent and Trademark Office is unnecessary. The action of the Patent and Trademark Office will be based exclusively on the written record in the Office. No attention will be paid to any alleged oral promise, stipulation, or understanding in relation to which there is disagreement or doubt.

———

The action of the Patent and Trademark Office cannot be based exclusively on the written record in the Office if that record is itself incomplete through the failure to record the substance of interviews.

It is the responsibility of the applicant or the attorney or agent to make the substance of an interview of record in the application file, unless the examiner indicates he or she will do so. It is the examiner's responsibility to see that such a record is made and to correct material inaccuracies which bear directly on the question of patentability.

Examiners must complete an Interview Summary Form for each interview held where a matter of substance has been discussed during the interview by checking the appropriate boxes and filling in the blanks. Discussions regarding only procedural matters, directed solely to restriction requirements for which interview recordation is otherwise provided for in Section 812.01 of the Manual of Patent Examining Procedure, or pointing out typographical errors or unreadable script in Office actions or the like, are excluded from the interview recordation procedures below. Where the substance of an interview is completely recorded in an Examiners Amendment, no separate Interview Summary Record is required.

The Interview Summary Form shall be given an appropriate Paper No., placed in the right hand portion of the file, and listed on the "Contents" section of the file wrapper. In a personal interview, a duplicate of the Form is given to the applicant (or attorney or agent) at the conclusion of the interview. In the case of a telephone or video-conference interview, the copy is mailed to the applicant's correspondence address either with or prior to the next official communication. If additional correspondence from the examiner is not likely before an allowance or if other circumstances dictate, the Form should be mailed promptly after the interview rather than with the next official communication.

The Form provides for recordation of the following information:
- Application Number (Series Code and Serial Number)
- Name of applicant
- Name of examiner
- Date of interview
- Type of interview (telephonic, video-conference, or personal)
- Name of participant(s) (applicant, attorney or agent, examiner, other PTO personnel, etc.)
- An indication whether or not an exhibit was shown or a demonstration conducted
- An identification of the specific prior art discussed
- An indication whether an agreement was reached and if so, a description of the general nature of the agreement (may be by attachment of a copy of amendments or claims agreed as being allowable). Note: Agreement as to allowability is tentative and does not restrict further action by the examiner to the contrary.
- The signature of the examiner who conducted the interview (if Form is not an attachment to a signed Office action)

It is desirable that the examiner orally remind the applicant of his or her obligation to record the substance of the interview of each case. It should be noted, however, that the Interview Summary Form will not normally be considered a complete and proper recordation of the interview unless it includes, or is supplemented by the applicant or the examiner to include, all of the applicable items required below concerning the substance of the interview.

A complete and proper recordation of the substance of any interview should include at least the following applicable items:
1) A brief description of the nature of any exhibit shown or any demonstration conducted,
2) an identification of the claims discussed,
3) an identification of the specific prior art discussed,
4) an identification of the principal proposed amendments of a substantive nature discussed, unless these are already described on the Interview Summary Form completed by the Examiner,
5) a brief identification of the general thrust of the principal arguments presented to the examiner,
   (The identification of arguments need not be lengthy or elaborate. A verbatim or highly detailed description of the arguments is not required. The identification of the arguments is sufficient if the general nature or thrust of the principal arguments made to the examiner can be understood in the context of the application file. Of course, the applicant may desire to emphasize and fully describe those arguments which he or she feels were or might be persuasive to the examiner.)
6) a general indication of any other pertinent matters discussed, and
7) if appropriate, the general results or outcome of the interview unless already described in the Interview Summary Form completed by the examiner.

Examiners are expected to carefully review the applicant's record of the substance of an interview. If the record is not complete and accurate, the examiner will give the applicant an extendable one month time period to correct the record.

Examiner to Check for Accuracy

If the claims are allowable for other reasons of record, the examiner should send a letter setting forth the examiner's version of the statement attributed to him or her. If the record is complete and accurate, the examiner should place the indication, "Interview Record OK" on the paper recording the substance of the interview along with the date and the examiner's initials.

Continuation of Substance of Interview including description of the general nature of what was agreed to if an agreement was reached, or any other comments: The examiner and applicant discussed an overview of the invention and explained features of simultaneous transfer and types of interleaving and allocation of memory based on direction of transmission and bandwidth. The examiner felt the proposed amendment was a step in the right direction but that more details would be recommended to overcome the cited prior art. The examiner suggested the features of need more detailing such as type of memory, type of interleaving to distinguish from the prior art or memory art. .

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UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
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Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
11/246,163	10/11/2005	Marcos C. Tzannes	5550-54	5478

62574 7590 12/09/2009

Jason H. Vick
Sheridan Ross, PC
Suite # 1200
1560 Broadway
Denver, CO 80202

EXAMINER	
PFIZENMAYER, MARK C	
ART UNIT	**PAPER NUMBER**
2447	

NOTIFICATION DATE	DELIVERY MODE
12/09/2009	ELECTRONIC

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

jvick@sheridanross.com

Office Action Summary	Application No.	Applicant(s)	
	11/246,163	TZANNES ET AL.	
	Examiner	Art Unit	
	MARK PFIZENMAYER	2447	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *21 August 2009*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-45* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-45* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date *9/22/2009*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

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IPR2023-00064, Ex. 1035
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DETAILED ACTION

1. Claims 19 and 28 were amended in the amendment filed on 8/21/2009. The claims 1-45 are pending.

Response to Arguments

2. Applicant's arguments filed 8/21/2009 have been fully considered but they are not persuasive.

A. Applicant argues the cited prior art does not teach how the same memory can be used for simultaneously receiving of data and transmitting data.

In response to applicant's argument that the references fail to show certain features of applicant's invention, it is noted that the features upon which applicant relies (i.e., the same memory being used for simultaneously receiving of data and transmitting data) are not recited in the rejected claim(s). Although the claims are interpreted in light of the specification, limitations from the specification are not read into the claims. See *In re Van Geuns*, 988 F.2d 1181, 26 USPQ2d 1057 (Fed. Cir. 1993).

Specification

3. The disclosure is objected to because of the following informalities:

- The specification fails to provide proper antecedent basis for "an information storage media" in claim 37. See 37 CFR 1.75(d)(1) and MPEP § 608.01(o). Appropriate correction is required.

Claim Rejections - 35 USC § 101

4. 35 U.S.C. 101 reads as follows:

> Whoever invents or discovers any new and useful process, machine, manufacture, or composition of matter, or any new and useful improvement thereof, may obtain a patent therefor, subject to the conditions and requirements of this title.

5. Claims 19-36 are rejected under 35 U.S.C. 101 because the claimed invention is directed to non-statutory subject matter.

With respect to claim 19, the claim lacks the necessary physical articles or objects to constitute a machine or a manufacture within the meaning of 35 U.S.C. 101. They are clearly not a series of steps or acts to be a process nor are they a combination of chemical compounds to be a composition of matter. As such, they fail to fall within a statutory category. They are, at best, functional descriptive material per se. Claims 20-27 are likewise rejected.

With respect to claim 28, the claim lacks the necessary physical articles or objects to constitute a machine or a manufacture within the meaning of 35 U.S.C. 101. They are clearly not a series of steps or acts to be a process nor are they a combination of chemical compounds to be a composition of matter. As such, they fail to fall within a statutory category. They are, at best, functional descriptive material per se. MPEP §2106.01. Claims 29- 36 are likewise rejected.

Claim Rejections - 35 USC § 102

6. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section

> 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

7. Claims 1-45 are rejected under 35 U.S.C. 102(e) as being anticipated by Fadavi-Ardekani (U.S. Patent No. 6,707,822).

With respect to claim 1, Fadavi-Ardekani teaches a method for sharing resources in a transceiver (i.e., the IDIM of the transceiver can support different number of sessions; lines 3-5 in column 7) comprising: allocating a first portion of shared memory to a first latency path (i.e., 16 Kbytes is allocated for interleave, lines 25-30 in column 7) and allocating a second portion of the shared memory to a second latency path (i.e., 4 Kbytes is allocated for deinterleave, lines 25-30 in column 7).

With respect to claim 2, Fadavi-Ardekani further teaches wherein the first latency path includes an interleaver and the second latency path includes an interleaver (i.e., the size of the IDIM and the interleave depth may be modified to allocate multiple portions, wherein each portion or session may be used for interleave or deinterleave. For example, a new interleave session may be added to an existing interleave session; lines 3-5 and 30-33 in column 7).

With respect to claim 3, Fadavi-Ardekani further teaches wherein the first latency path includes an interleaver and the second latency path includes a deinterleaver (i.e., the size of the IDIM and the interleave depth may be modified to allocate multiple portions, wherein each portion or session may be used for interleave or deinterleave; lines 3-5 and 30-33 in column 7).

With respect to claim 4, Fadavi-Ardekani further teaches wherein the first latency path includes a deinterleaver and the second latency path includes a deinterleaver (i.e.,

the size of the IDIM and the interleave depth may be modified to allocate multiple portions, wherein each portion or session may be used for interleave or deinterleave. For example, a new deinterleave session may be added to an existing deinterleave session; lines 3-5 and 30-33 in column 7).

With respect to claim 5, Fadavi-Ardekani further teaches transmitting to another transceiver information that is used to determine a maximum amount of shared memory that can be allocated (i.e., the ADSL transceiver provides data to (and receives data from) several channels with the data grouped into frames that include both payload data bytes and overhead data bytes, wherein overhead data bytes may contain information that is used to determine a maximum amount of shared memory that can be allocated, lines 20-25 in column 2).

With respect to claim 6, Fadavi-Ardekani further teaches receiving from another transceiver information that is used to determine a maximum amount of shared memory that can be allocated (i.e., the ADSL transceiver provides data to (and receives data from) several channels with the data grouped into frames that include both payload data bytes and overhead data bytes, wherein overhead data bytes may contain information that is used to determine a maximum amount of shared memory that can be allocated, lines 20-25 in column 2).

With respect to claim 7, Fadavi-Ardekani further teaches allocating a shared processing module to a plurality of coding and/or decoding modules (i.e., the FCI supports multiple ADSL sessions and performs various tasks on payload data including framing/de-framing, cyclic redundancy check generation/checking,

scrambling/descrambling, Reed-Solomon encoding/decoding, and interleaving/de-interleaving, lines 11-17 in column 6).

With respect to claim 8, Fadavi-Ardekani further teaches wherein the allocating of at least one portion of the shared memory is based on one or more communication parameters (i.e., the number of sessions supported is based on the size of the IDIM and the interleave depth, lines 3-5 and 30-33 in column 7).

With respect to claim 9, Fadavi-Ardekani further teaches wherein at least one of the communication parameters is a data rate, a latency, an INP value or a bit error rate (i.e., interleave depth, wherein the interleave depth is directly proportional to latency, lines 3-5 in column 7).

With respect to claim 10, Fadavi-Ardekani teaches a transceiver comprising: a first portion of shared memory that is allocated to a first latency path (i.e., 16 Kbytes is allocated for interleave, lines 25-30 in column 7); and a second portion of the shared memory that is allocated to a second latency path (i.e., 4 Kbytes is allocated for deinterleave, lines 25-30 in column 7).

With respect to claim 11, Fadavi-Ardekani further teaches further comprising: an allocation module designed to allocate the shared memory based on one or more communication parameters (i.e., the number of sessions supported is based on the size of the IDIM and the interleave depth, lines 3-5 and 30-33 in column 7).

With respect to claim 12, Fadavi-Ardekani further teaches wherein at least one of the communication parameters is a data rate, a latency, an INP value or a Bit Error Rate

(i.e., interleave depth, wherein the interleave depth is directly proportional to latency, lines 3-5 in column 7).

With respect to claim 13, Fadavi-Ardekani further teaches wherein the first latency path includes an interleaver and the second latency path includes an interleaver (i.e., the size of the IDIM and the interleave depth may be modified to allocate multiple portions, wherein each portion or session may be used for interleave or deinterleave. For example, a new interleave session may be added to an existing interleave session; lines 3-5 and 30-33 in column 7).

With respect to claim 14, Fadavi-Ardekani further teaches wherein the first latency path includes an interleaver and the second latency path includes a deinterleaver (i.e., the size of the IDIM and the interleave depth may be modified to allocate multiple portions, wherein each portion or session may be used for interleave or deinterleave; lines 3-5 and 30-33 in column 7).

With respect to claim 15, Fadavi-Ardekani further teaches wherein the first latency path includes a deinterleaver and the second latency path includes a deinterleaver (i.e., the size of the IDIM and the interleave depth may be modified to allocate multiple portions, wherein each portion or session may be used for interleave or deinterleave. For example, a new deinterleave session may be added to an existing deinterleave session; lines 3-5 and 30-33 in column 7).

With respect to claim 16, Fadavi-Ardekani further teaches further comprising a shared resource management module designed to determine information that is transmitted to another transceiver, wherein the information is used to determine a

maximum amount of shared memory that can be allocated (i.e., the ADSL transceiver provides data to (and receives data from) several channels with the data grouped into frames that include both payload data bytes and overhead data bytes, wherein overhead data bytes may contain information that is used to determine a maximum amount of shared memory that can be allocated, lines 20-25 in column 2).

With respect to claim 17, Fadavi-Ardekani further teaches further comprising a shared resource management module designed to utilize information that is received from another transceiver, wherein the information is used to determine a maximum amount of shared memory that can be allocated (i.e., the ADSL transceiver provides data to (and receives data from) several channels with the data grouped into frames that include both payload data bytes and overhead data bytes, wherein overhead data bytes may contain information that is used to determine a maximum amount of shared memory that can be allocated, lines 20-25 in column 2).

With respect to claim 18, Fadavi-Ardekani further teaches further comprising a shared processing module designed to provide processing resources to a plurality of coding and/or decoding modules (i.e., the FCI supports multiple ADSL sessions and performs various tasks on payload data including framing/de-framing, cyclic redundancy check generation/checking, scrambling/descrambling, Reed-Solomon encoding/decoding, and interleaving/de-interleaving, lines 11-17 in column 6).

With respect to claim 19, Fadavi-Ardekani teaches a system for sharing resources in a transceiver (i.e., the IDIM of the transceiver can support different number of sessions; lines 3-5 in column 7) comprising: means for allocating a first portion of

shared memory to a first latency path (i.e., 16 Kbytes is allocated for interleave, lines 25-30 in column 7) and means for allocating a second portion of the shared memory to a second latency path (i.e., 4 Kbytes is allocated for deinterleave, lines 25-30 in column 7).

With respect to claim 20, Fadavi-Ardekani further teaches wherein the first latency path includes an interleaver and the second latency path includes an interleaver (i.e., the size of the IDIM and the interleave depth may be modified to allocate multiple portions, wherein each portion or session may be used for interleave or deinterleave. For example, a new interleave session may be added to an existing interleave session; lines 3-5 and 30-33 in column 7).

With respect to claim 21, Fadavi-Ardekani further teaches wherein the first latency path includes an interleaver and the second latency path includes a deinterleaver (i.e., the size of the IDIM and the interleave depth may be modified to allocate multiple portions, wherein each portion or session may be used for interleave or deinterleave; lines 3-5 and 30-33 in column 7).

With respect to claim 22, Fadavi-Ardekani further teaches wherein the first latency path includes a deinterleaver and the second latency path includes a deinterleaver (i.e., the size of the IDIM and the interleave depth may be modified to allocate multiple portions, wherein each portion or session may be used for interleave or deinterleave. For example, a new deinterleave session may be added to an existing deinterleave session; lines 3-5 and 30-33 in column 7).

With respect to claim 23, Fadavi-Ardekani further teaches means for transmitting to another transceiver information that is used to determine a maximum amount of shared memory that can be allocated (i.e., the ADSL transceiver provides data to (and receives data from) several channels with the data grouped into frames that include both payload data bytes and overhead data bytes, wherein overhead data bytes may contain information that is used to determine a maximum amount of shared memory that can be allocated, lines 20-25 in column 2).

With respect to claim 24, Fadavi-Ardekani further teaches means for receiving from another transceiver information that is used to determine a maximum amount of shared memory that can be allocated (i.e., the ADSL transceiver provides data to (and receives data from) several channels with the data grouped into frames that include both payload data bytes and overhead data bytes, wherein overhead data bytes may contain information that is used to determine a maximum amount of shared memory that can be allocated, lines 20-25 in column 2).

With respect to claim 25, Fadavi-Ardekani further teaches means for allocating a shared processing module to a plurality of coding and/or decoding modules (i.e., the FCI supports multiple ADSL sessions and performs various tasks on payload data including framing/de-framing, cyclic redundancy check generation/checking, scrambling/descrambling, Reed-Solomon encoding/decoding, and interleaving/de-interleaving, lines 11-17 in column 6).

With respect to claim 26, Fadavi-Ardekani further teaches wherein the allocating of at least one portion of the shared memory is based on one or more communication

parameters (i.e., the number of sessions supported is based on the size of the IDIM and the interleave depth, lines 3-5 and 30-33 in column 7).

With respect to claim 27, Fadavi-Ardekani further teaches wherein at least one of the communication parameters is a data rate, a latency, an INP value or a bit error rate (i.e., interleave depth, wherein the interleave depth is directly proportional to latency, lines 3-5 in column 7).

With respect to claim 28, Fadavi-Ardekani teaches a protocol for sharing resources in a transceiver (i.e., the IDIM of the transceiver can support different number of sessions; lines 3-5 in column 7) comprising: allocating a first portion of shared memory to a first latency path (i.e., 16 Kbytes is allocated for interleave, lines 25-30 in column 7) and allocating a second portion of the shared memory to a second latency path (i.e., 4 Kbytes is allocated for deinterleave, lines 25-30 in column 7).

With respect to claim 29, Fadavi-Ardekani further teaches wherein the first latency path includes an interleaver and the second latency path includes an interleaver (i.e., the size of the IDIM and the interleave depth may be modified to allocate multiple portions, wherein each portion or session may be used for interleave or deinterleave. For example, a new interleave session may be added to an existing interleave session; lines 3-5 and 30-33 in column 7).

With respect to claim 30, Fadavi-Ardekani further teaches wherein the first latency path includes an interleaver and the second latency path includes a deinterleaver (i.e., the size of the IDIM and the interleave depth may be modified to

allocate multiple portions, wherein each portion or session may be used for interleave or deinterleave; lines 3-5 and 30-33 in column 7).

With respect to claim 31, Fadavi-Ardekani further teaches wherein the first latency path includes a deinterleaver and the second latency path includes a deinterleaver (i.e., the size of the IDIM and the interleave depth may be modified to allocate multiple portions, wherein each portion or session may be used for interleave or deinterleave. For example, a new deinterleave session may be added to an existing deinterleave session; lines 3-5 and 30-33 in column 7).

With respect to claim 32, Fadavi-Ardekani further teaches transmitting to another transceiver information that is used to determine a maximum amount of shared memory that can be allocated (i.e., the ADSL transceiver provides data to (and receives data from) several channels with the data grouped into frames that include both payload data bytes and overhead data bytes, wherein overhead data bytes may contain information that is used to determine a maximum amount of shared memory that can be allocated, lines 20-25 in column 2).

With respect to claim 33, Fadavi-Ardekani further teaches receiving from another transceiver information that is used to determine a maximum amount of shared memory that can be allocated (i.e., the ADSL transceiver provides data to (and receives data from) several channels with the data grouped into frames that include both payload data bytes and overhead data bytes, wherein overhead data bytes may contain information that is used to determine a maximum amount of shared memory that can be allocated, lines 20-25 in column 2).

With respect to claim 34, Fadavi-Ardekani further teaches allocating a shared processing module to a plurality of coding and/or decoding modules (i.e., the FCI supports multiple ADSL sessions and performs various tasks on payload data including framing/de-framing, cyclic redundancy check generation/checking, scrambling/descrambling, Reed-Solomon encoding/decoding, and interleaving/de-interleaving, lines 11-17 in column 6).

With respect to claim 35, Fadavi-Ardekani further teaches wherein the allocating of at least one portion of the shared memory is based on one or more communication parameters (i.e., the number of sessions supported is based on the size of the IDIM and the interleave depth, lines 3-5 and 30-33 in column 7).

With respect to claim 36, Fadavi-Ardekani further teaches wherein at least one of the communication parameters is a data rate, a latency, an INP value or a bit error rate (i.e., interleave depth, wherein the interleave depth is directly proportional to latency, lines 3-5 in column 7).

With respect to claim 37, Fadavi-Ardekani teaches sharing of resources in a transceiver (i.e., the IDIM of the transceiver can support different number of sessions; lines 3-5 in column 7) comprising: information that allocates a first portion of shared memory to a first latency path (i.e., 16 Kbytes is allocated for interleave, lines 25-30 in column 7) and information that allocates a second portion of the shared memory to a second latency path (i.e., 4 Kbytes is allocated for deinterleave, lines 25-30 in column 7).

With respect to claim 38, Fadavi-Ardekani further teaches wherein the first latency path includes an interleaver and the second latency path includes an interleaver (i.e., the size of the IDIM and the interleave depth may be modified to allocate multiple portions, wherein each portion or session may be used for interleave or deinterleave. For example, a new interleave session may be added to an existing interleave session; lines 3-5 and 30-33 in column 7).

With respect to claim 39, Fadavi-Ardekani further teaches wherein the first latency path includes an interleaver and the second latency path includes a deinterleaver (i.e., the size of the IDIM and the interleave depth may be modified to allocate multiple portions, wherein each portion or session may be used for interleave or deinterleave; lines 3-5 and 30-33 in column 7).

With respect to claim 40, Fadavi-Ardekani further teaches wherein the first latency path includes a deinterleaver and the second latency path includes a deinterleaver (i.e., the size of the IDIM and the interleave depth may be modified to allocate multiple portions, wherein each portion or session may be used for interleave or deinterleave. For example, a new deinterleave session may be added to an existing deinterleave session; lines 3-5 and 30-33 in column 7).

With respect to claim 41, Fadavi-Ardekani further teaches further comprising information that transmits to another transceiver information that is used to determine a maximum amount of shared memory that can be allocated (i.e., the ADSL transceiver provides data to (and receives data from) several channels with the data grouped into frames that include both payload data bytes and overhead data bytes, wherein

overhead data bytes may contain information that is used to determine a maximum amount of shared memory that can be allocated, lines 20-25 in column 2).

With respect to claim 42, Fadavi-Ardekani further teaches further comprising information that receives from another transceiver information that is used to determine a maximum amount of shared memory that can be allocated (i.e., the ADSL transceiver provides data to (and receives data from) several channels with the data grouped into frames that include both payload data bytes and overhead data bytes, wherein overhead data bytes may contain information that is used to determine a maximum amount of shared memory that can be allocated, lines 20-25 in column 2).

With respect to claim 43, Fadavi-Ardekani further teaches further comprising information that allocates a shared processing module to a plurality of coding and/or decoding modules (i.e., the FCI supports multiple ADSL sessions and performs various tasks on payload data including framing/de-framing, cyclic redundancy check generation/checking, scrambling/descrambling, Reed-Solomon encoding/decoding, and interleaving/de-interleaving, lines 11-17 in column 6).

With respect to claim 44, Fadavi-Ardekani further teaches wherein the allocating of at least one portion of the shared memory is based on one or more communication parameters (i.e., the number of sessions supported is based on the size of the IDIM and the interleave depth, lines 3-5 and 30-33 in column 7).

With respect to claim 45, Fadavi-Ardekani further teaches wherein at least one of the communication parameters is a data rate, a latency, an INP value or a bit error rate (i.e., interleave depth, wherein the interleave depth is directly proportional to latency,

lines 3-5 in column 7).

Conclusion

8. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

9. Any inquiry concerning this communication or earlier communications from the examiner should be directed to MARK PFIZENMAYER whose telephone number is (571)270-7214. The examiner can normally be reached on Monday - Friday 8:00 - 5:30 EST.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, James Hwang can be reached on (571)272-4036. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

Mark Pfizenmayer
Patent Examiner
1 December 2009

/Joon H. Hwang/
Supervisory Patent Examiner, Art Unit 2447

Index of Claims	Application/Control No.	Applicant(s)/Patent Under Reexamination
	11246163	TZANNES ET AL.
	Examiner	Art Unit
	Mark Pfizenmayer	2447

✓	Rejected	-	Cancelled	N	Non-Elected	A	Appeal
=	Allowed	÷	Restricted	I	Interference	O	Objected

☐ Claims renumbered in the same order as presented by applicant ☐ CPA ☐ T.D. ☐ R.1.47

CLAIM		DATE								
Final	Original	12/29/2008	12/01/2009							
	1	✓	✓							
	2	✓	✓							
	3	✓	✓							
	4	✓	✓							
	5	✓	✓							
	6	✓	✓							
	7	✓	✓							
	8	✓	✓							
	9	✓	✓							
	10	✓	✓							
	11	✓	✓							
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	34	✓	✓							
	35	✓	✓							
	36	✓	✓							

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Index of Claims	Application/Control No.	Applicant(s)/Patent Under Reexamination
	11246163	TZANNES ET AL.
	Examiner	**Art Unit**
	Mark Pfizenmayer	2447

✓	Rejected	-	Cancelled	N	Non-Elected	A	Appeal
=	Allowed	÷	Restricted	I	Interference	O	Objected

☐ Claims renumbered in the same order as presented by applicant ☐ CPA ☐ T.D. ☐ R.1.47

CLAIM		DATE								
Final	Original	12/29/2008	12/01/2009							
	37	✓	✓							
	38	✓	✓							
	39	✓	✓							
	40	✓	✓							
	41	✓	✓							
	42	✓	✓							
	43	✓	✓							
	44	✓	✓							
	45	✓	✓							

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	11246163	TZANNES ET AL.
	Examiner	**Art Unit**
	Mark Pfizenmayer	2447

SEARCHED			
Class	**Subclass**	**Date**	**Examiner**

SEARCH NOTES		
Search Notes	**Date**	**Examiner**
See search history printout	Nov 2009	MCP
709/215 with text	Nov 2009	MCP
Discussed with Primary Ben Bruckart	Nov 2009	MCP

INTERFERENCE SEARCH			
Class	**Subclass**	**Date**	**Examiner**

EAST Search History

EAST Search History (Prior Art)

Ref #	Hits	Search Query	DBs	Default Operator	Plurals	Time Stamp
L1	50	("20060088054" "5781549" "5572686" "6065101" "6374332" "6411418" "6988173" "7069362" "7085898" "7111130" "20040054857" "20040076044" "20040230726" "20040230751" "20040230752" "20060184750" "20060246907" "5477539" "20080232444" "6195334" "5644576" "5898904" "6674971" "6690934" "20070043945" "20070076655" "20090239548" "5524234" "6138208" "6185640" "5307459" "5337285" "5412782" "5485584" "5498990" "5526510" "5537573" "5613077" "5649302" "5713005" "5729705" "5734848" "5737587" "5805836" "5815667" "5831467" "5844576" "5872920" "5943504" "5974511").pn.	US-PGPUB; USPAT; USOCR; EPO; JPO; IBM_TDB	OR	ON	2009/12/01 17:46
L2	0	L1 and 709/215.ccls.	US-PGPUB; USPAT; USOCR; EPO; JPO; IBM_TDB	OR	ON	2009/12/01 17:46
S1	5	("6337877" | "6707822" | "6775320" | "6778589" | "6778596").PN.	US-PGPUB; USPAT; USOCR; EPO; JPO; IBM_TDB	OR	ON	2009/11/22 16:01

S2	1	"20060088054".pn.	US-PGPUB; USPAT; USOCR; EPO; JPO; IBM_TDB	OR	ON	2009/11/22 16:06
S3	1	"7042891".pn. and latency adj path	US-PGPUB; USPAT; USOCR; EPO; JPO; IBM_TDB	OR	ON	2009/11/22 17:17
S4	5	("6337877" | "6707822" | "6775320" | "6778589" | "6778596").PN.	US-PGPUB; USPAT; USOCR; EPO; JPO; IBM_TDB	OR	ON	2009/11/22 17:19
S5	3	S4 and latency adj path	US-PGPUB; USPAT; USOCR; EPO; JPO; IBM_TDB	OR	ON	2009/11/22 17:19
S6	4	S4 and latency	US-PGPUB; USPAT; USOCR; EPO; JPO; IBM_TDB	OR	ON	2009/11/22 17:20
S7	4	S4 and path	US-PGPUB; USPAT; USOCR; EPO; JPO; IBM_TDB	OR	ON	2009/11/22 17:22
S8	50	("20060088054" "5781549" "5572686" "6065101" "6374332" "6411418" "6988173" "7069362" "7085898" "7111130" "20040054857" "20040076044" "20040230726" "20040230751" "20040230752" "20060184750" "20060246907" "5477539" "20080232444" "6195334" "5644576" "5898904" "6674971" "6690934" "20070043945" "20070076655" "20090239548"	US-PGPUB; USPAT; USOCR; EPO; JPO; IBM_TDB	OR	ON	2009/11/29 16:51

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S9	1	"20060088054".pn. and memory	US-PGPUB; USPAT; USOCR; EPO; JPO; IBM_TDB	OR	ON	2009/11/29 16:53
S10	1	"20060088054".pn. and hard	US-PGPUB; USPAT; USOCR; EPO; JPO; IBM_TDB	OR	ON	2009/11/29 16:57
S11	1	"6775320".pn.	US-PGPUB; USPAT; USOCR; EPO; JPO; IBM_TDB	OR	ON	2009/11/29 17:00
S12	1	"6775320".pn. and fci	US-PGPUB; USPAT; USOCR; EPO; JPO; IBM_TDB	OR	ON	2009/11/29 17:01

EAST Search History (Interference)

< This search history is empty>

12/1/2009 5:47:17 PM
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Substitute for form 1449A/PTO				Complete if Known	
INFORMATION DISCLOSURE STATEMENT BY APPLICANT				Application Number	11/246,163
				Filing Date	October 11, 2005
				First Named Inventor	LUND, MICHAEL
				Art Unit	2447
				Examiner Name	HWANG, JOON H
Sheet	1	of	1	Attorney Docket Number	5550-54

U.S. PATENT DOCUMENTS					
Examiner Initials*	Cite No.[1]	Document Number Number-kind Code [2] *(if known)*	Publication Date MM-DD-YYYY	Name of Patentee of Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear

FOREIGN PATENT DOCUMENTS						
Examiner Initials*	Cite No.[1]	Foreign Patent Document Country Code[3]; Number[4]; Kind Code[5] *(if known)*	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear	T[6]

OTHER ART (Including Author, Title, Date, Pertinent Pages, etc.)		
Examiner Initials*	Cite No.[1]	
	1	Examiner's First Report for Australian Patent Application No. 2005296086, mailed June 24, 2009 (Attorney's Ref. No. 5550-54)

Examiner Signature	/Mark Pfizenmayer/	Date Considered	11/29/2009

*EXAMINER: Initial if reference is considered, whether or not citation is in conformance and not considered. Include copy of this form with next communication to applicant.

ALL REFERENCES CONSIDERED EXCEPT WHERE LINED THROUGH. /M.P./

PLUS Search Results for S/N 11246163, Searched Mon Nov 23 09:02:44 EST 2009

The Patent Linguistics Utility System (PLUS) is a USPTO automated search system for U.S. Patents from 1971 to the present PLUS is a query-by-example search system which produces a list of patents that are most closely related linguistically to the application searched. This search was prepared by the staff of the Scientific and Technical Information Center, SIRA.

20060088054 99
5974511 52
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5572686 66
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7085898 66
7111130 66
20040054857 66
20040076044 66
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Substitute for form 1449A/PTO				Complete if Known	
INFORMATION DISCLOSURE STATEMENT BY APPLICANT				Application Number	11/246,163
				Filing Date	October 11, 2005
				First Named Inventor	LUND, MICHAEL
				Art Unit	2447
				Examiner Name	HWANG, JOON H
Sheet	1	of	1	Attorney Docket Number	5550-54

U.S. PATENT DOCUMENTS					
Examiner Initials*	Cite No.[1]	Document Number Number-kind Code [2] *(if known)*	Publication Date MM-DD-YYYY	Name of Patentee of Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear

FOREIGN PATENT DOCUMENTS						
Examiner Initials*	Cite No.[1]	Foreign Patent Document Country Code[3]; Number[4]; Kind Code[5] *(if known)*	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear	T[6]

OTHER ART (Including Author, Title, Date, Pertinent Pages, etc.)		
Examiner Initials*	Cite No.[1]	
	1	Examiner's First Report for Australian Patent Application No. 2005296086, mailed June 24, 2009 (Attorney's Ref. No. 5550-54)

Examiner Signature		Date Considered	

*EXAMINER: Initial if reference is considered, whether or not citation is in conformance and not considered. Include copy of this form with next communication to applicant.

Electronic Acknowledgement Receipt	
EFS ID:	6119916
Application Number:	11246163
International Application Number:	
Confirmation Number:	5478
Title of Invention:	Resource sharing in a telecommunications environment
First Named Inventor/Applicant Name:	Marcos C. Tzannes
Customer Number:	62574
Filer:	Jason Vick/Debra Kesner
Filer Authorized By:	Jason Vick
Attorney Docket Number:	5550-54
Receipt Date:	22-SEP-2009
Filing Date:	11-OCT-2005
Time Stamp:	14:47:11
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	no

File Listing:

Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1		IDS_03.pdf	330792 c92050b4e1f32a348ee1a8ba787034fb4121de7c	yes	4

	Multipart Description/PDF files in .zip description				
	Document Description		Start	End	
	Transmittal Letter		1	3	
	Information Disclosure Statement (IDS) Filed (SB/08)		4	4	
Warnings:					
Information:					
2	NPL Documents	5550-54-PAU_OA_6-24-09.pdf	1621631 6e6bcea1107bdeecacfd28cca73d27af840590ac	no	30
Warnings:					
Information:					
		Total Files Size (in bytes):	1952423		

This Acknowledgement Receipt evidences receipt on the noted date by the USPTO of the indicated documents, characterized by the applicant, and including page counts, where applicable. It serves as evidence of receipt similar to a Post Card, as described in MPEP 503.

New Applications Under 35 U.S.C. 111
If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application.

National Stage of an International Application under 35 U.S.C. 371
If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.

New International Application Filed with the USPTO as a Receiving Office
If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In Re the Application of:	)	Group Art Unit: 2447
LUND, MICHAEL	)	Confirmation No.: 5478
Serial No.: 11/246,163	)	Examiner: HWANG, JOON H
Filed: October 11, 2005	)	
Atty. File No.: 5550-54	)	INFORMATION DISCLOSURE STATEMENT
Entitled: "RESOURCE SHARING IN A TELECOMMUNICATIONS ENVIRONMENT"	)	Electronically Submitted

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Dear Sir:

The references cited on attached Form PTO-1449 are being called to the attention of the Examiner.

☒ Copies of the cited non-patent and/or foreign references are enclosed herewith.

☐ Copies of the cited U.S. patents and/or patent applications are enclosed herewith.

☐ Copies of the cited U.S. patents/patent application publications are not enclosed in accordance with 37 C.F.R. § 1.98(a).

☐ Copies of the cited references are not enclosed, in accordance with 37 C.F.R. § 1.98(d), because the references were cited by or submitted to the U.S. Patent and Trademark Office in prior application Serial No. _____ filed _____, which is relied upon for an earlier filing date under 35 U.S.C. § 120.

☐ To the best of applicants' belief, the pertinence of the foreign-language references are believed to be summarized in the attached English abstracts and in the figures, although applicants do not necessarily vouch for the accuracy of the translation.

☐ Examiner's attention is drawn to the following related applications:

Serial No. _____filed _____(Attorney's Ref. No. _____)

Serial No. _____filed _____(Attorney's Ref. No. _____)

☐ Other:_____

Submission of the above information is not intended as an admission that any item is citable under the statutes or rules to support a rejection, that any item disclosed represents analogous art, or that those skilled in the art would refer to or recognize the

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pertinence of any reference without the benefit of hindsight, nor should an inference be drawn as to the pertinence of the references based on the order in which they are presented. Submission of this statement should not be taken as an indication that a search has been conducted, or that no better art exists.

It is respectfully requested that the cited information be expressly considered during the prosecution of this application and the references made of record therein.

FEES

☐	**37 CFR 1.97(b)**: No fee is believed due in connection with this submission, because the information disclosure statement submitted herewith is satisfied by one of the following conditions ("X" indicates satisfaction): ☐ Within three months of the filing date of a national application other than a continued prosecution application under 37 CFR 1.53(d), or ☐ Within three months of the date of entry into the national stage of an international application as set forth in 37 CFR 1.491 or ☐ Before the mailing date of a first Office Action on the merits, or ☐ Before the mailing of a first Office action after the filing of a request for continued examination under 37 CFR 1.114. Although no fee is believed due, if any fee is deemed due in connection with this submission, please charge such fee to Deposit Account 19-1970.
☒	**37 CFR 1.97(c)**: The information disclosure statement transmitted herewith is being filed after all the above conditions (37 CFR 1.97(b)), but before the mailing date of one of the following conditions: (1) a final action under 37 C.F.R. 1.113 or (2) a notice of allowance under 37 C.F.R. 1.311, or (3) an action that otherwise closes prosecution in the application. This Information Disclosure Statement is accompanied by: ☒ A Certification (below) as specified by 37 C.F.R. 1.97(c). Although no fee is believed due, if any fee is deemed due in connection with this submission, please charge such fee to Deposit Account 19-1970. OR ☐ Please charge Deposit Account 19-1970 in the amount of $180.00 for the fee set forth in 37 C.F.R. 1.17(p) for submission of an information disclosure statement. Please credit any overpayment or charge any underpayment to Deposit Account 19-1970.
☐	**37 CFR 1.97(d)**: This Information Disclosure Statement is being submitted after the period specified in 37 CFR 1.97(c). ☐ This information Disclosure Statement includes a Certification (below) as specified by 37 C.F.R. 1.97(e) AND ☐ Applicants hereby requests consideration of the reference(s) disclosed herein. Please charge Deposit Account 19-1970 in the amount of $180.00 under 37 C.F.R. 1.17(p). Please credit any overpayment or charge any underpayment to Deposit Account 19-1970. Election to pay the fee should not be taken as an indication that applicant(s) cannot execute a certification.

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Certification (37 C.F.R. 1.97(e))
(Applicable only if checked)

☒ The undersigned certifies that:

☒ Each item of information contained in this information disclosure statement was first cited in any communication from a foreign patent office in a counterpart foreign application not more than three months prior to the filing of this statement. 37 C.F.R. 1.97(e)(1).

☒ A copy of the communication from the foreign patent office is enclosed.

OR

☐ No item of information contained in this information disclosure statement was cited in a communication from a foreign patent office in a counterpart foreign application, and, to the knowledge of the undersigned after making reasonable inquiry, no item of information contained in this Information Disclosure Statement was known to any individual designated in 37 C.F.R. 1.56(c) more than three months prior to the filing of this statement. 37 C.F.R. 1.97(e)(2).

Respectfully submitted,

SHERIDAN ROSS P.C.

By: _____

Jason H. Vick
Registration No. 45,285
1560 Broadway, Suite 1200
Denver, Colorado 80202-5141
(303) 863-9700

Date: 22 Sept 09

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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In Re the Application of: Tzannes et al.	Group Art Unit: 2447
Application No.: 11/246,163	Examiner: LEUNG, Jack C.
Filed: October 11, 2005	Confirmation No.: 5478
Atty. File No.: 5550-54	

For: RESOURCE SHARING IN A TELECOMMUNICATIONS ENVIRONMENT

AMENDMENT AND RESPONSE

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Sir:

Applicants submit this Amendment and Response to address the Office Action having a mailing date of February 24, 2009. Please credit any overpayment or charge any underpayment to Deposit Account No. 19-1970.

Please amend the above-identified patent application as follows:

Amendments to the Specification begin on page 2 of this paper.

Amendments to the Claims are shown in the listing of claims which begins on page 3 of this paper.

Remarks begin on page 8 of this paper.

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Amendments to the Specification:

Please amend the Specification as follows:

[0006] Accordingly, an exemplary aspect of this invention relates to sharing memory between one or more interleavers and/or ~~deinterlaevers~~ deinterleavers in a transceiver. More particularly, an exemplary aspect of this invention relates to shared latency path memory in a transceiver.

[00048] Example #1

A first transmitter portion or receiver portion latency path may carry data from a video application, which needs a very low BER but can tolerate higher latency. In this case, the video will be transported using an latency path that has a large amount of interleaving/deinterleaving and coding (also known as Forward Error Correction (FEC) coding). For example, the latency path may be configured with Reed-Solomon coding using a codeword size of 255 bytes (N=255) with 16 checkbytes (R=16) and interleaving/deinterleaving using an interleaver depth of 64 (D=64). This latency path will require ~~N*D=16*255=16Kbytes~~ N*D=255*64=16Kbytes of interleaver memory at the transmitter (or de-interleaver memory at the receiver). This latency path will be able to correct a burst of errors that is less than 512 bytes in duration.

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Amendments to the Claims:

This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims:

1. (Original) A method for sharing resources in a transceiver comprising:

allocating a first portion of shared memory to a first latency path and allocating a second portion of the shared memory to a second latency path.

2. (Original) The method of claim 1, wherein the first latency path includes an interleaver and the second latency path includes an interleaver.

3. (Original) The method of claim 1, wherein the first latency path includes an interleaver and the second latency path includes a deinterleaver.

4. (Original) The method of claim 1, wherein the first latency path includes a deinterleaver and the second latency path includes a deinterleaver.

5. (Original) The method of claim 1, further comprising transmitting to another transceiver information that is used to determine a maximum amount of shared memory that can be allocated.

6. (Original) The method of claim 1, further comprising receiving from another transceiver information that is used to determine a maximum amount of shared memory that can be allocated.

7. (Original) The method of claim 1, further comprising allocating a shared processing module to a plurality of coding and/or decoding modules.

8. (Original) The method of claim 1, wherein the allocating of at least one portion of the shared memory is based on one or more communication parameters.

9. (Original) The method of claim 8, wherein at least one of the communication parameters is a data rate, a latency, an INP value or a bit error rate (BER).

10. (Original) A transceiver comprising:

a first portion of shared memory that is allocated to a first latency path; and

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a second portion of the shared memory that is allocated to a second latency path.

11. (Original) The transceiver of claim 10, further comprising:

an allocation module designed to allocate the shared memory based on one or more communication parameters.

12. (Original) The transceiver of claim 11, wherein at least one of the communication parameters is a data rate, a latency, an INP value or a Bit Error Rate (BER).

13. (Original) The transceiver of claim 10, wherein the first latency path includes an interleaver and the second latency path includes an interleaver.

14. (Original) The transceiver of claim 10, wherein the first latency path includes an interleaver and the second latency path includes a deinterleaver.

15. (Original) The transceiver of claim 10, wherein the first latency path includes a deinterleaver and the second latency path includes a deinterleaver.

16. (Original) The transceiver of claim 10, further comprising a shared resource management module designed to determine information that is transmitted to another transceiver, wherein the information is used to determine a maximum amount of shared memory that can be allocated.

17. (Original) The transceiver of claim 10, further comprising a shared resource management module designed to utilize information that is received from another transceiver, wherein the information is used to determine a maximum amount of shared memory that can be allocated.

18. (Original) The transceiver of claim 10, further comprising a shared processing module designed to provide processing resources to a plurality of coding and/or decoding modules.

19. (Currently Amended) A system for sharing resources, such as memory, in a transceiver comprising:

means for allocating a first portion of a shared memory to a first latency path and means for allocating a second portion of the shared memory to a second latency path.

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20. (Original) The system of claim 19, wherein the first latency path includes an interleaver and the second latency path includes an interleaver.

21. (Original) The system of claim 19, wherein the first latency path includes an interleaver and the second latency path includes a deinterleaver.

22. (Original) The system of claim 19, wherein the first latency path includes a deinterleaver and the second latency path includes a deinterleaver.

23. (Original) The system of claim 19, further comprising means for transmitting to another transceiver information that is used to determine a maximum amount of shared memory that can be allocated.

24. (Original) The system of claim 19, further comprising means for receiving from another transceiver information that is used to determine a maximum amount of shared memory that can be allocated.

25. (Original) The system of claim 19, further comprising means for allocating a shared processing module to a plurality of coding and/or decoding modules.

26. (Original) The system of claim 19, wherein the allocating of at least one portion of the shared memory is based on one or more communication parameters.

27. (Original) The system of claim 26, wherein at least one of the communication parameters is a data rate, a latency, an INP value or a bit error rate (BER).

28. (Currently Amended) A protocol for sharing resources, such as memory, in a transceiver comprising:

allocating a first portion of a shared memory to a first latency path and allocating a second portion of the shared memory to a second latency path.

29. (Original) The protocol of claim 28, wherein the first latency path includes an interleaver and the second latency path includes an interleaver.

30. (Original) The protocol of claim 28, wherein the first latency path includes an interleaver and the second latency path includes a deinterleaver.

31. (Original) The protocol of claim 28, wherein the first latency path includes a deinterleaver and the second latency path includes a deinterleaver.

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32. (Original) The protocol of claim 28, further comprising transmitting to another transceiver information that is used to determine a maximum amount of shared memory that can be allocated.

33. (Original) The protocol of claim 28, further comprising receiving from another transceiver information that is used to determine a maximum amount of shared memory that can be allocated.

34. (Original) The protocol of claim 28, further comprising allocating a shared processing module to a plurality of coding and/or decoding modules.

35. (Original) The protocol of claim 28, wherein the allocating of at least one portion of the shared memory is based on one or more communication parameters.

36. (Original) The protocol of claim 35, wherein at least one of the communication parameters is a data rate, a latency, an INP value or a bit error rate (BER).

37. (Original) An information storage media having stored thereon information that when executed allows sharing of resources in a transceiver comprising:

information that allocates a first portion of shared memory to a first latency path and information that allocates a second portion of the shared memory to a second latency path.

38. (Original) The media of claim 37, wherein the first latency path includes an interleaver and the second latency path includes an interleaver.

39. (Original) The media of claim 37, wherein the first latency path includes an interleaver and the second latency path includes a deinterleaver.

40. (Original) The media of claim 37, wherein the first latency path includes a deinterleaver and the second latency path includes a deinterleaver.

41. (Original) The media of claim 37, further comprising information that transmits to another transceiver information that is used to determine a maximum amount of shared memory that can be allocated.

42. (Original) The media of claim 37, further comprising information that receives from another transceiver information that is used to determine a maximum amount of shared memory that can be allocated.

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43. (Original) The media of claim 37, further comprising information that allocates a shared processing module to a plurality of coding and/or decoding modules.

44. (Original) The media of claim 37, wherein the allocating of at least one portion of the shared memory is based on one or more communication parameters.

45. (Original) The media of claim 44, wherein at least one of the communication parameters is a data rate, a latency, an INP value or a bit error rate (BER).

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REMARKS

Applicant respectfully requests reconsideration of this application as amended.

By this amendment, the outstanding objections have been addressed in accordance with the Examiner's recommendations.

Additionally, the 35 U.S.C. §101 rejections have been addressed and it is believed the rejected claims are in compliance therewith.

Regarding the art-based rejections, Fadavi-Ardekani states that "a simple of a transmit interleaver for standard ADSL requires 16 Kbytes per session for downstream processing and 2 Kbytes per session for upstream processing." Fadavi-Ardekani then states that "the invention utilizes the same memory for receive data and transmit data and thus requires 20 Kbytes to support a standard ADSL session at full interleave depth..."

MPEP 2121.01 states that "In determining that quantum of prior art disclosure which is necessary to declare an applicant's invention 'not novel' or 'anticipated' within section 102, the stated test is whether a reference contains an 'enabling disclosure'... ." In re Hoeksema, 399 F.2d 269, 158 USPQ 596 (CCPA 1968). The disclosure in an assertedly anticipating reference must provide an enabling disclosure of the desired subject matter; mere naming or description of the subject matter is insufficient, if it cannot be produced without undue experimentation. Elan Pharm., Inc. v. **>Mayo Found. For Med. Educ. & Research<, 346 F.3d 1051, 1054, 68 USPQ2d 1373, 1376 (Fed. Cir. 2003).

Applicants respectfully submit Fadavi-Ardekani is not enabling for how the same memory can be used for simultaneous receiving of data and transmitting of data.

In that Fadavi-Ardekani is not enabling, Applicants respectfully submit Fadavi-Ardekani is not anticipatory of the claimed subject matter.

Applicants therefore respectfully submit the application is patentably distinguishable from the cited reference and respectfully request a Notice of Allowance.

As discussed with SPE James Joon Hwang, the Examiner assigned to examining this application is respectfully requested to contact the undersigned to schedule a Personal Interview to discuss the merits of the application. As also discussed, the next Office Action, if not a Notice of Allowance, will not be made final.

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The Commissioner is hereby authorized to charge to deposit account number 19-1970 any fees under 37 CFR § 1.16 and 1.17 that may be required by this paper and to credit any overpayment to that Account. If any extension of time is required in connection with the filing of this paper and has not been separately requested, such extension is hereby petitioned.

Respectfully submitted,

SHERIDAN ROSS P.C.

Date: 2/4/19

By: _____

Jason H. Vick
Reg. No. 45,285
1560 Broadway, Suite 1200
Denver, Colorado 80202
Telephone: 303-863-9700

CommScope, Inc.
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PTO/SB/22 (07-09)
Approved for use through 07/31/2012. OMB 0651-0031
U.S. Patent and Trademark Office; U.S. DEPARMENT OF COMMERCE
Under the paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it displays a valid OMB control number.

PETITION FOR EXTENSION OF TIME UNDER 37 CFR 1.136(a) **FY 2009** *(Fees pursuant to the Consolidated Appropriations Act, 2005 (H.R. 4818).)*	Docket Number (Optional) 5550-54
Application Number 11/246,163	Filed October 11, 2005
For RESOURCE SHARING IN A TELECOMMUNICATIONS ENVIRONMENT	
Art Unit 2447	Examiner LEUNG, Jack C.

This is a request under the provisions of 37 CFR 1.136(a) to extend the period for filing a reply in the above identified application.

The requested extension and fee are as follows (check time period desired and enter the appropriate fee below):

	Fee	Small Entity Fee	
☐ One month (37 CFR 1.17(a)(1))	$130	$65	$
☐ Two months (37 CFR 1.17(a)(2))	$490	$245	$
☑ Three months (37 CFR 1.17(a)(3))	$1110	$555	$ 1110
☐ Four months (37 CFR 1.17(a)(4))	$1730	$865	$
☐ Five months (37 CFR 1.17(a)(5))	$2350	$1175	$

☐ Applicant claims small entity status. See 37 CFR 1.27.

☐ A check in the amount of the fee is enclosed.

☐ Payment by credit card. Form PTO-2038 is attached.

☑ The Director has already been authorized to charge fees in this application to a Deposit Account.

☑ The Director is hereby authorized to charge any fees which may be required, or credit any overpayment, to Deposit Account Number 19-1970.

WARNING: Information on this form may become public. Credit card information should not be included on this form. Provide credit card information and authorization on PTO-2038.

I am the

☐ applicant/inventor.

☐ assignee of record of the entire interest. See 37 CFR 3.71.
Statement under 37 CFR 3.73(b) is enclosed (Form PTO/SB/96).

☑ attorney or agent of record. Registration Number 45,285

☐ attorney or agent under 37 CFR 1.34.
Registration number if acting under 37 CFR 1.34 _____

Signature	21 Aug '09 Date
Jason H. Vick Typed or printed name	303-863-9700 Telephone Number

NOTE: Signatures of all the inventors or assignees of record of the entire interest or their representative(s) are required. Submit multiple forms if more than one signature is required, see below.

☑ Total of 1 forms are submitted.

This collection of information is required by 37 CFR 1.136(a). The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.11 and 1.14. This collection is estimated to take 6 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

If you need assistance in completing the form, call 1-800-PTO-9199 and select option 2.

Electronic Patent Application Fee Transmittal	
Application Number:	11246163
Filing Date:	11-Oct-2005
Title of Invention:	Resource sharing in a telecommunications environment
First Named Inventor/Applicant Name:	Marcos C. Tzannes
Filer:	Jason Vick/Joanne Vos
Attorney Docket Number:	5550-54
Filed as Large Entity	

Utility under 35 USC 111(a) Filing Fees

Description	Fee Code	Quantity	Amount	Sub-Total in USD($)
Basic Filing:				
Pages:				
Claims:				
Miscellaneous-Filing:				
Petition:				
Patent-Appeals-and-Interference:				
Post-Allowance-and-Post-Issuance:				
Extension-of-Time:				
Extension - 3 months with $0 paid	1253	1	1110	1110

Description	Fee Code	Quantity	Amount	Sub-Total in USD($)
Miscellaneous:				
		Total in USD ($)		**1110**

Electronic Acknowledgement Receipt	
EFS ID:	5933059
Application Number:	11246163
International Application Number:	
Confirmation Number:	5478
Title of Invention:	Resource sharing in a telecommunications environment
First Named Inventor/Applicant Name:	Marcos C. Tzannes
Customer Number:	62574
Filer:	Jason Vick/Joanne Vos
Filer Authorized By:	Jason Vick
Attorney Docket Number:	5550-54
Receipt Date:	21-AUG-2009
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Payment Type	Deposit Account
Payment was successfully received in RAM	$1110
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Authorized User	
The Director of the USPTO is hereby authorized to charge indicated fees and credit any overpayment as follows: Charge any Additional Fees required under 37 C.F.R. Section 1.16 (National application filing, search, and examination fees) Charge any Additional Fees required under 37 C.F.R. Section 1.17 (Patent application and reexamination processing fees)	

Charge any Additional Fees required under 37 C.F.R. Section 1.19 (Document supply fees)	
Charge any Additional Fees required under 37 C.F.R. Section 1.21 (Miscellaneous fees and charges)	

File Listing:

Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1		F20090821_AMEND_01.pdf	695796 4d49448bb80cf218ad13da53773621234beee98ce3	yes	9
	Multipart Description/PDF files in .zip description				
	Document Description		**Start**	**End**	
	Amendment/Req. Reconsideration-After Non-Final Reject		1	1	
	Specification		2	2	
	Claims		3	7	
	Applicant Arguments/Remarks Made in an Amendment		8	9	
Warnings:					
Information:					
2	Extension of Time	F20090821_EOT_01.pdf	121899 d5d846a10f04906c3859631fb789bda9566d51da	no	1
Warnings:					
Information:					
3	Fee Worksheet (PTO-875)	fee-info.pdf	29699 f37dcea9c75328cca3e5f322d94dc8bad113b84c	no	2
Warnings:					
Information:					
		Total Files Size (in bytes):	847394		

This Acknowledgement Receipt evidences receipt on the noted date by the USPTO of the indicated documents, characterized by the applicant, and including page counts, where applicable. It serves as evidence of receipt similar to a Post Card, as described in MPEP 503.

New Applications Under 35 U.S.C. 111
If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application.

National Stage of an International Application under 35 U.S.C. 371
If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.

New International Application Filed with the USPTO as a Receiving Office
If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.

PTO/SB/06 (07-06)
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PATENT APPLICATION FEE DETERMINATION RECORD
Substitute for Form PTO-875

Application or Docket Number	Filing Date	☐ To be Mailed
11/246,163	10/11/2005	

APPLICATION AS FILED – PART I

	(Column 1)	(Column 2)	SMALL ENTITY ☐		OR	OTHER THAN SMALL ENTITY	
FOR	NUMBER FILED	NUMBER EXTRA	RATE ($)	FEE ($)		RATE ($)	FEE ($)
☒ BASIC FEE (37 CFR 1.16(a), (b), or (c))	N/A	N/A	N/A			N/A	300
☐ SEARCH FEE (37 CFR 1.16(k), (l), or (m))	N/A	N/A	N/A			N/A	
☐ EXAMINATION FEE (37 CFR 1.16(o), (p), or (q))	N/A	N/A	N/A			N/A	
TOTAL CLAIMS (37 CFR 1.16(i))	minus 20 =	*	X $ =		OR	X $ =	
INDEPENDENT CLAIMS (37 CFR 1.16(h))	minus 3 =	*	X $ =			X $ =	
☐ APPLICATION SIZE FEE (37 CFR 1.16(s))	If the specification and drawings exceed 100 sheets of paper, the application size fee due is $250 ($125 for small entity) for each additional 50 sheets or fraction thereof. See 35 U.S.C. 41(a)(1)(G) and 37 CFR 1.16(s).						
☐ MULTIPLE DEPENDENT CLAIM PRESENT (37 CFR 1.16(j))							
* If the difference in column 1 is less than zero, enter "0" in column 2.			TOTAL			TOTAL	300

APPLICATION AS AMENDED – PART II

AMENDMENT		(Column 1)		(Column 2)	(Column 3)	SMALL ENTITY		OR	OTHER THAN SMALL ENTITY	
	08/21/2009	CLAIMS REMAINING AFTER AMENDMENT		HIGHEST NUMBER PREVIOUSLY PAID FOR	PRESENT EXTRA	RATE ($)	ADDITIONAL FEE ($)		RATE ($)	ADDITIONAL FEE ($)
	Total (37 CFR 1.16(i))	* 45	Minus	** 45	= 0	X $ =		OR	X $52=	0
	Independent (37 CFR 1.16(h))	* 5	Minus	***5	= 0	X $ =		OR	X $220=	0
	☐ Application Size Fee (37 CFR 1.16(s))									
	☐ FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))							OR		
						TOTAL ADD'L FEE		OR	TOTAL ADD'L FEE	0

AMENDMENT		(Column 1)		(Column 2)	(Column 3)	RATE ($)	ADDITIONAL FEE ($)		RATE ($)	ADDITIONAL FEE ($)
		CLAIMS REMAINING AFTER AMENDMENT		HIGHEST NUMBER PREVIOUSLY PAID FOR	PRESENT EXTRA					
	Total (37 CFR 1.16(i))	*	Minus	**	=	X $ =		OR	X $ =	
	Independent (37 CFR 1.16(h))	*	Minus	***	=	X $ =		OR	X $ =	
	☐ Application Size Fee (37 CFR 1.16(s))									
	☐ FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))							OR		
						TOTAL ADD'L FEE		OR	TOTAL ADD'L FEE	

* If the entry in column 1 is less than the entry in column 2, write "0" in column 3.
** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 20, enter "20".
*** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 3, enter "3".
The "Highest Number Previously Paid For" (Total or Independent) is the highest number found in the appropriate box in column 1.

Legal Instrument Examiner:
/GWENDOLYN MYERS/

This collection of information is required by 37 CFR 1.16. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 12 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**
If you need assistance in completing the form, call 1-800-PTO-9199 and select option 2.

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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
11/246,163	10/11/2005	Marcos C. Tzannes	5550-54	5478

62574 7590 02/24/2009

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EXAMINER	
LEUNG, JACK C	

ART UNIT	PAPER NUMBER
2447	

NOTIFICATION DATE	DELIVERY MODE
02/24/2009	ELECTRONIC

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

jvick@sheridanross.com

Office Action Summary	Application No.	Applicant(s)	
	11/246,163	TZANNES ET AL.	
	Examiner	Art Unit	
	JACK LEUNG	2447	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *11 October 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-45* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-45* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *11 October 2005* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date *5/17/2006, 5/23/2007*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

1. Claims 1-45 are pending.

Specification

2. The disclosure is objected to because of the following informalities:

- "…that can be allocated to one or more interleaves or deinterleavers." in section 8 of the specification should be replaced by "…that can be allocated to one or more interleavers or deinterleavers."
- "…The latency path will require N*D=16*255=16 Kbytes of interleaver memory at the transmitter…" in section 48 should be replaced by "…The latency path will require N*D=255*64=16 Kbytes of interleaver memory at the transmitter…"
- The specification fails to provide proper antecedent basis for "an information storage media" in claim 37. See 37 CFR 1.75(d)(1) and MPEP § 608.01(o).

Appropriate correction is required.

Claim Rejections - 35 USC § 101

3. 35 U.S.C. 101 reads as follows:

> Whoever invents or discovers any new and useful process, machine, manufacture, or composition of matter, or any new and useful improvement thereof, may obtain a patent therefor, subject to the conditions and requirements of this title.

4. Claims 19-27 and 28-36 are rejected under 35 U.S.C. 101 because the claimed invention is directed to non-statutory subject matter.

With respect to claim 19, the claim lacks the necessary physical articles or objects to constitute a machine or a manufacture within the meaning of 35 U.S.C. 101. They are clearly not a series of steps or acts to be a process nor are they a combination of chemical compounds to be a composition of matter. As such, they fail to fall within a statutory category. They are, at best, functional descriptive material per se. Claims 20-27 are likewise rejected.

With respect to claim 28, the claim lacks the necessary physical articles or objects to constitute a machine or a manufacture within the meaning of 35 U.S.C. 101. They are clearly not a series of steps or acts to be a process nor are they a combination of chemical compounds to be a composition of matter. As such, they fail to fall within a statutory category. They are, at best, functional descriptive material per se. Claims 29-36 are likewise rejected.

Claim Rejections - 35 USC § 102

5. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

6. Claims 1-45 are rejected under 35 U.S.C. 102(e) as being anticipated by Fadavi-Ardekani (U.S. Patent No. 6,707,822).

With respect to claim 1, Fadavi-Ardekani teaches a method for sharing resources in a transceiver (i.e., the IDIM of the transceiver can support different number of sessions; lines 3-5 in column 7) comprising: allocating a first portion of shared memory to a first latency path (i.e., 16 Kbytes is allocated for interleave, lines 25-30 in column 7) and allocating a second portion of the shared memory to a second latency path (i.e., 4 Kbytes is allocated for deinterleave, lines 25-30 in column 7).

With respect to claim 2, Fadavi-Ardekani further teaches wherein the first latency path includes an interleaver and the second latency path includes an interleaver (i.e., the size of the IDIM and the interleave depth may be modified to allocate multiple portions, wherein each portion or session may be used for interleave or deinterleave. For example, a new interleave session may be added to an existing interleave session; lines 3-5 and 30-33 in column 7).

With respect to claim 3, Fadavi-Ardekani further teaches wherein the first latency path includes an interleaver and the second latency path includes a deinterleaver (i.e., the size of the IDIM and the interleave depth may be modified to allocate multiple portions, wherein each portion or session may be used for interleave or deinterleave; lines 3-5 and 30-33 in column 7).

With respect to claim 4, Fadavi-Ardekani further teaches wherein the first latency path includes a deinterleaver and the second latency path includes a deinterleaver (i.e., the size of the IDIM and the interleave depth may be modified to allocate multiple

portions, wherein each portion or session may be used for interleave or deinterleave. For example, a new deinterleave session may be added to an existing deinterleave session; lines 3-5 and 30-33 in column 7).

With respect to claim 5, Fadavi-Ardekani further teaches transmitting to another transceiver information that is used to determine a maximum amount of shared memory that can be allocated (i.e., the ADSL transceiver provides data to (and receives data from) several channels with the data grouped into frames that include both payload data bytes and overhead data bytes, wherein overhead data bytes may contain information that is used to determine a maximum amount of shared memory that can be allocated, lines 20-25 in column 2).

With respect to claim 6, Fadavi-Ardekani further teaches receiving from another transceiver information that is used to determine a maximum amount of shared memory that can be allocated (i.e., the ADSL transceiver provides data to (and receives data from) several channels with the data grouped into frames that include both payload data bytes and overhead data bytes, wherein overhead data bytes may contain information that is used to determine a maximum amount of shared memory that can be allocated, lines 20-25 in column 2).

With respect to claim 7, Fadavi-Ardekani further teaches allocating a shared processing module to a plurality of coding and/or decoding modules (i.e., the FCI supports multiple ADSL sessions and performs various tasks on payload data including framing/de-framing, cyclic redundancy check generation/checking,

scrambling/descrambling, Reed-Solomon encoding/decoding, and interleaving/de-interleaving, lines 11-17 in column 6).

With respect to claim 8, Fadavi-Ardekani further teaches wherein the allocating of at least one portion of the shared memory is based on one or more communication parameters (i.e., the number of sessions supported is based on the size of the IDIM and the interleave depth, lines 3-5 and 30-33 in column 7).

With respect to claim 9, Fadavi-Ardekani further teaches wherein at least one of the communication parameters is a data rate, a latency, an INP value or a bit error rate (i.e., interleave depth, wherein the interleave depth is directly proportional to latency, lines 3-5 in column 7).

With respect to claim 10, Fadavi-Ardekani teaches a transceiver comprising: a first portion of shared memory that is allocated to a first latency path (i.e., 16 Kbytes is allocated for interleave, lines 25-30 in column 7); and a second portion of the shared memory that is allocated to a second latency path (i.e., 4 Kbytes is allocated for deinterleave, lines 25-30 in column 7).

With respect to claim 11, Fadavi-Ardekani further teaches further comprising: an allocation module designed to allocate the shared memory based on one or more communication parameters (i.e., the number of sessions supported is based on the size of the IDIM and the interleave depth, lines 3-5 and 30-33 in column 7).

With respect to claim 12, Fadavi-Ardekani further teaches wherein at least one of the communication parameters is a data rate, a latency, an INP value or a Bit Error Rate

(i.e., interleave depth, wherein the interleave depth is directly proportional to latency, lines 3-5 in column 7).

With respect to claim 13, Fadavi-Ardekani further teaches wherein the first latency path includes an interleaver and the second latency path includes an interleaver (i.e., the size of the IDIM and the interleave depth may be modified to allocate multiple portions, wherein each portion or session may be used for interleave or deinterleave. For example, a new interleave session may be added to an existing interleave session; lines 3-5 and 30-33 in column 7).

With respect to claim 14, Fadavi-Ardekani further teaches wherein the first latency path includes an interleaver and the second latency path includes a deinterleaver (i.e., the size of the IDIM and the interleave depth may be modified to allocate multiple portions, wherein each portion or session may be used for interleave or deinterleave; lines 3-5 and 30-33 in column 7).

With respect to claim 15, Fadavi-Ardekani further teaches wherein the first latency path includes a deinterleaver and the second latency path includes a deinterleaver (i.e., the size of the IDIM and the interleave depth may be modified to allocate multiple portions, wherein each portion or session may be used for interleave or deinterleave. For example, a new deinterleave session may be added to an existing deinterleave session; lines 3-5 and 30-33 in column 7).

With respect to claim 16, Fadavi-Ardekani further teaches further comprising a shared resource management module designed to determine information that is transmitted to another transceiver, wherein the information is used to determine a

maximum amount of shared memory that can be allocated (i.e., the ADSL transceiver provides data to (and receives data from) several channels with the data grouped into frames that include both payload data bytes and overhead data bytes, wherein overhead data bytes may contain information that is used to determine a maximum amount of shared memory that can be allocated, lines 20-25 in column 2).

With respect to claim 17, Fadavi-Ardekani further teaches further comprising a shared resource management module designed to utilize information that is received from another transceiver, wherein the information is used to determine a maximum amount of shared memory that can be allocated (i.e., the ADSL transceiver provides data to (and receives data from) several channels with the data grouped into frames that include both payload data bytes and overhead data bytes, wherein overhead data bytes may contain information that is used to determine a maximum amount of shared memory that can be allocated, lines 20-25 in column 2).

With respect to claim 18, Fadavi-Ardekani further teaches further comprising a shared processing module designed to provide processing resources to a plurality of coding and/or decoding modules (i.e., the FCI supports multiple ADSL sessions and performs various tasks on payload data including framing/de-framing, cyclic redundancy check generation/checking, scrambling/descrambling, Reed-Solomon encoding/decoding, and interleaving/de-interleaving, lines 11-17 in column 6).

With respect to claim 19, Fadavi-Ardekani teaches a system for sharing resources in a transceiver (i.e., the IDIM of the transceiver can support different number of sessions; lines 3-5 in column 7) comprising: means for allocating a first portion of

shared memory to a first latency path (i.e., 16 Kbytes is allocated for interleave, lines 25-30 in column 7) and means for allocating a second portion of the shared memory to a second latency path (i.e., 4 Kbytes is allocated for deinterleave, lines 25-30 in column 7).

With respect to claim 20, Fadavi-Ardekani further teaches wherein the first latency path includes an interleaver and the second latency path includes an interleaver (i.e., the size of the IDIM and the interleave depth may be modified to allocate multiple portions, wherein each portion or session may be used for interleave or deinterleave. For example, a new interleave session may be added to an existing interleave session; lines 3-5 and 30-33 in column 7).

With respect to claim 21, Fadavi-Ardekani further teaches wherein the first latency path includes an interleaver and the second latency path includes a deinterleaver (i.e., the size of the IDIM and the interleave depth may be modified to allocate multiple portions, wherein each portion or session may be used for interleave or deinterleave; lines 3-5 and 30-33 in column 7).

With respect to claim 22, Fadavi-Ardekani further teaches wherein the first latency path includes a deinterleaver and the second latency path includes a deinterleaver (i.e., the size of the IDIM and the interleave depth may be modified to allocate multiple portions, wherein each portion or session may be used for interleave or deinterleave. For example, a new deinterleave session may be added to an existing deinterleave session; lines 3-5 and 30-33 in column 7).

With respect to claim 23, Fadavi-Ardekani further teaches means for transmitting to another transceiver information that is used to determine a maximum amount of shared memory that can be allocated (i.e., the ADSL transceiver provides data to (and receives data from) several channels with the data grouped into frames that include both payload data bytes and overhead data bytes, wherein overhead data bytes may contain information that is used to determine a maximum amount of shared memory that can be allocated, lines 20-25 in column 2).

With respect to claim 24, Fadavi-Ardekani further teaches means for receiving from another transceiver information that is used to determine a maximum amount of shared memory that can be allocated (i.e., the ADSL transceiver provides data to (and receives data from) several channels with the data grouped into frames that include both payload data bytes and overhead data bytes, wherein overhead data bytes may contain information that is used to determine a maximum amount of shared memory that can be allocated, lines 20-25 in column 2).

With respect to claim 25, Fadavi-Ardekani further teaches means for allocating a shared processing module to a plurality of coding and/or decoding modules (i.e., the FCI supports multiple ADSL sessions and performs various tasks on payload data including framing/de-framing, cyclic redundancy check generation/checking, scrambling/descrambling, Reed-Solomon encoding/decoding, and interleaving/de-interleaving, lines 11-17 in column 6).

With respect to claim 26, Fadavi-Ardekani further teaches wherein the allocating of at least one portion of the shared memory is based on one or more communication

parameters (i.e., the number of sessions supported is based on the size of the IDIM and the interleave depth, lines 3-5 and 30-33 in column 7).

With respect to claim 27, Fadavi-Ardekani further teaches wherein at least one of the communication parameters is a data rate, a latency, an INP value or a bit error rate (i.e., interleave depth, wherein the interleave depth is directly proportional to latency, lines 3-5 in column 7).

With respect to claim 28, Fadavi-Ardekani teaches a protocol for sharing resources in a transceiver (i.e., the IDIM of the transceiver can support different number of sessions; lines 3-5 in column 7) comprising: allocating a first portion of shared memory to a first latency path (i.e., 16 Kbytes is allocated for interleave, lines 25-30 in column 7) and allocating a second portion of the shared memory to a second latency path (i.e., 4 Kbytes is allocated for deinterleave, lines 25-30 in column 7).

With respect to claim 29, Fadavi-Ardekani further teaches wherein the first latency path includes an interleaver and the second latency path includes an interleaver (i.e., the size of the IDIM and the interleave depth may be modified to allocate multiple portions, wherein each portion or session may be used for interleave or deinterleave. For example, a new interleave session may be added to an existing interleave session; lines 3-5 and 30-33 in column 7).

With respect to claim 30, Fadavi-Ardekani further teaches wherein the first latency path includes an interleaver and the second latency path includes a deinterleaver (i.e., the size of the IDIM and the interleave depth may be modified to

allocate multiple portions, wherein each portion or session may be used for interleave or deinterleave; lines 3-5 and 30-33 in column 7).

With respect to claim 31, Fadavi-Ardekani further teaches wherein the first latency path includes a deinterleaver and the second latency path includes a deinterleaver (i.e., the size of the IDIM and the interleave depth may be modified to allocate multiple portions, wherein each portion or session may be used for interleave or deinterleave. For example, a new deinterleave session may be added to an existing deinterleave session; lines 3-5 and 30-33 in column 7).

With respect to claim 32, Fadavi-Ardekani further teaches transmitting to another transceiver information that is used to determine a maximum amount of shared memory that can be allocated (i.e., the ADSL transceiver provides data to (and receives data from) several channels with the data grouped into frames that include both payload data bytes and overhead data bytes, wherein overhead data bytes may contain information that is used to determine a maximum amount of shared memory that can be allocated, lines 20-25 in column 2).

With respect to claim 33, Fadavi-Ardekani further teaches receiving from another transceiver information that is used to determine a maximum amount of shared memory that can be allocated (i.e., the ADSL transceiver provides data to (and receives data from) several channels with the data grouped into frames that include both payload data bytes and overhead data bytes, wherein overhead data bytes may contain information that is used to determine a maximum amount of shared memory that can be allocated, lines 20-25 in column 2).

With respect to claim 34, Fadavi-Ardekani further teaches allocating a shared processing module to a plurality of coding and/or decoding modules (i.e., the FCI supports multiple ADSL sessions and performs various tasks on payload data including framing/de-framing, cyclic redundancy check generation/checking, scrambling/descrambling, Reed-Solomon encoding/decoding, and interleaving/de-interleaving, lines 11-17 in column 6).

With respect to claim 35, Fadavi-Ardekani further teaches wherein the allocating of at least one portion of the shared memory is based on one or more communication parameters (i.e., the number of sessions supported is based on the size of the IDIM and the interleave depth, lines 3-5 and 30-33 in column 7).

With respect to claim 36, Fadavi-Ardekani further teaches wherein at least one of the communication parameters is a data rate, a latency, an INP value or a bit error rate (i.e., interleave depth, wherein the interleave depth is directly proportional to latency, lines 3-5 in column 7).

With respect to claim 37, Fadavi-Ardekani teaches sharing of resources in a transceiver (i.e., the IDIM of the transceiver can support different number of sessions; lines 3-5 in column 7) comprising: information that allocates a first portion of shared memory to a first latency path (i.e., 16 Kbytes is allocated for interleave, lines 25-30 in column 7) and information that allocates a second portion of the shared memory to a second latency path (i.e., 4 Kbytes is allocated for deinterleave, lines 25-30 in column 7).

With respect to claim 38, Fadavi-Ardekani further teaches wherein the first latency path includes an interleaver and the second latency path includes an interleaver (i.e., the size of the IDIM and the interleave depth may be modified to allocate multiple portions, wherein each portion or session may be used for interleave or deinterleave. For example, a new interleave session may be added to an existing interleave session; lines 3-5 and 30-33 in column 7).

With respect to claim 39, Fadavi-Ardekani further teaches wherein the first latency path includes an interleaver and the second latency path includes a deinterleaver (i.e., the size of the IDIM and the interleave depth may be modified to allocate multiple portions, wherein each portion or session may be used for interleave or deinterleave; lines 3-5 and 30-33 in column 7).

With respect to claim 40, Fadavi-Ardekani further teaches wherein the first latency path includes a deinterleaver and the second latency path includes a deinterleaver (i.e., the size of the IDIM and the interleave depth may be modified to allocate multiple portions, wherein each portion or session may be used for interleave or deinterleave. For example, a new deinterleave session may be added to an existing deinterleave session; lines 3-5 and 30-33 in column 7).

With respect to claim 41, Fadavi-Ardekani further teaches further comprising information that transmits to another transceiver information that is used to determine a maximum amount of shared memory that can be allocated (i.e., the ADSL transceiver provides data to (and receives data from) several channels with the data grouped into frames that include both payload data bytes and overhead data bytes, wherein

overhead data bytes may contain information that is used to determine a maximum amount of shared memory that can be allocated, lines 20-25 in column 2).

With respect to claim 42, Fadavi-Ardekani further teaches further comprising information that receives from another transceiver information that is used to determine a maximum amount of shared memory that can be allocated (i.e., the ADSL transceiver provides data to (and receives data from) several channels with the data grouped into frames that include both payload data bytes and overhead data bytes, wherein overhead data bytes may contain information that is used to determine a maximum amount of shared memory that can be allocated, lines 20-25 in column 2).

With respect to claim 43, Fadavi-Ardekani further teaches further comprising information that allocates a shared processing module to a plurality of coding and/or decoding modules (i.e., the FCI supports multiple ADSL sessions and performs various tasks on payload data including framing/de-framing, cyclic redundancy check generation/checking, scrambling/descrambling, Reed-Solomon encoding/decoding, and interleaving/de-interleaving, lines 11-17 in column 6).

With respect to claim 44, Fadavi-Ardekani further teaches wherein the allocating of at least one portion of the shared memory is based on one or more communication parameters (i.e., the number of sessions supported is based on the size of the IDIM and the interleave depth, lines 3-5 and 30-33 in column 7).

With respect to claim 45, Fadavi-Ardekani further teaches wherein at least one of the communication parameters is a data rate, a latency, an INP value or a bit error rate

(i.e., interleave depth, wherein the interleave depth is directly proportional to latency, lines 3-5 in column 7).

Conclusion

7. Any inquiry concerning this communication or earlier communications from the examiner should be directed to JACK LEUNG whose telephone number is (571)270-7215. The examiner can normally be reached on Monday thru Friday, 7:30am - 5:00pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, (James) Joon Hwang can be reached on 571-272-4036. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/JACK LEUNG/
Examiner, Art Unit 4142
1/6/09

/Joon H. Hwang/
Supervisory Patent Examiner, Art Unit 2447

Notice of References Cited	Application/Control No. 11/246,163	Applicant(s)/Patent Under Reexamination TZANNES ET AL.	
	Examiner JACK LEUNG	Art Unit 2447	Page 1 of 1

U.S. PATENT DOCUMENTS

*		Document Number Country Code-Number-Kind Code	Date MM-YYYY	Name	Classification
*	A	US-6,707,822	03-2004	Fadavi-Ardekani et al.	370/395.5
	B	US-			
	C	US-			
	D	US-			
	E	US-			
	F	US-			
	G	US-			
	H	US-			
	I	US-			
	J	US-			
	K	US-			
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	M	US-			

FOREIGN PATENT DOCUMENTS

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	N					
	O					
	P					
	Q					
	R					
	S					
	T					

NON-PATENT DOCUMENTS

*		Include as applicable: Author, Title Date, Publisher, Edition or Volume, Pertinent Pages)
	U	
	V	
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	X	

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Dates in MM-YYYY format are publication dates. Classifications may be US or foreign.

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Page 334 of 531

Index of Claims	Application/Control No.	Applicant(s)/Patent Under Reexamination
	11246163	TZANNES ET AL.
	Examiner	Art Unit
	JACK LEUNG	2447

✓	Rejected	-	Cancelled	N	Non-Elected	A	Appeal
=	Allowed	÷	Restricted	I	Interference	O	Objected

☐ Claims renumbered in the same order as presented by applicant ☐ CPA ☐ T.D. ☐ R.1.47

CLAIM		DATE								
Final	Original	12/29/2008								
	1	✓								
	2	✓								
	3	✓								
	4	✓								
	5	✓								
	6	✓								
	7	✓								
	8	✓								
	9	✓								
	10	✓								
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	33	✓								
	34	✓								
	35	✓								
	36	✓								

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Index of Claims	Application/Control No.	Applicant(s)/Patent Under Reexamination
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	Examiner	Art Unit
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✓	Rejected	-	Cancelled	N	Non-Elected	A	Appeal
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☐ Claims renumbered in the same order as presented by applicant ☐ CPA ☐ T.D. ☐ R.1.47

CLAIM		DATE								
Final	Original	12/29/2008								
	37	✓								
	38	✓								
	39	✓								
	40	✓								
	41	✓								
	42	✓								
	43	✓								
	44	✓								
	45	✓								

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Search Notes	Application/Control No.	Applicant(s)/Patent Under Reexamination
	11246163	TZANNES ET AL.
	Examiner	Art Unit
	JACK LEUNG	2447

SEARCHED			
Class	Subclass	Date	Examiner

SEARCH NOTES		
Search Notes	Date	Examiner
PALM inventor searched	Dec. 2008	JL
Class 709 using text search	Dec. 2008	JL
See search history printout(s)	Dec. 2008	JL

INTERFERENCE SEARCH			
Class	Subclass	Date	Examiner

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CONFIRMATION NO. 5478

SERIAL NUMBER	FILING or 371(c) DATE	CLASS	GROUP ART UNIT	ATTORNEY DOCKET NO.
11/246,163	10/11/2005 RULE	711	4142	T3653-9285US01

APPLICANTS
Marcos C. Tzannes, Orinda, CA;
Michael Lund, West Newton, MA;

**** CONTINUING DATA ***************************
This appln claims benefit of 60/618,269 10/12/2004

**** FOREIGN APPLICATIONS ***************************

**** IF REQUIRED, FOREIGN FILING LICENSE GRANTED ****
11/07/2005

Foreign Priority claimed ☐ Yes ☑ No 35 USC 119(a-d) conditions met ☐ Yes ☑ No Verified and Acknowledged /JACK C LEUNG/ Examiner's Signature	☐ Met after Allowance Initials	STATE OR COUNTRY	SHEETS DRAWINGS	TOTAL CLAIMS	INDEPENDENT CLAIMS
		CA	3	45	5

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Jason H. Vick
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Suite # 1200
1560 Broadway
Denver, CO 80202
UNITED STATES

TITLE
Resource sharing in a telecommunications environment

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Sheet 1 of 2

Complete it Known	
Application Number	11/246,163
Filing Date	October 11, 2005
First Named Inventor	TZANNES, MARCOS C.
Art Unit	2186
Examiner Name	
Attorney Docket Number	T3653-9285US01

U.S. PATENT DOCUMENTS

Examiner Initials*	Cite No. [1]	U.S. Patent Document Number	Kind Code [2] (if known)	Name of Patentee or Applicant of Cited Document	Publication Date MM-DD-YYYY	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear
		6,337,877		Cole et al.	01-08-2002	
		6,707,822		Fadavi—Ardekani et al.	03-16-2004	
		6,775,320		Tzannes et al.	08-10-2004	
		6,778,589		Ishii, Satoru	08-17-2004	

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Examiner Initials*	Cite No. [1]	Foreign Patent Document Office [3]	Number [4]	Kind Code [5] (if known)	Name of Patentee or Applicant of Cited Document	Publication Date MM-DD-YYYY	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear	T [6]
		WO	2003/063060	A	Broadcom Corporation	07-31-2003		

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Sheet 2 of 2

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Application Number	11/246,163
Filing Date	October 11, 2005
First Named Inventor	TZANNES, MARCOS C.
Art Unit	2186
Examiner Name	
Attorney Docket Number	T3653-9285US01

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		International Application WO 2006/04427 A1, published on April 27, 2006	
		PCT/US2005/036015 - International Search Report, mailed February 8, 2006	
		http://www.sunrisetelecom.com/technotes/APP-xDSL-8B.pdf, "Sunset xDSL: Prequalification of ADSL Circuits with ATU-C Emulation" 2001, page 3, Sunrise Telecom Inc., Application Series, San Jose, USA, XP002363272	

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	Application Number	11246163
	Filing Date	2005-10-11
	First Named Inventor	Tzannes
	Art Unit	2142
	Examiner Name	CALDWELL, ANDREW T
	Attorney Docket Number	5550-54

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11246163 - GAU: 4142

INFORMATION DISCLOSURE STATEMENT BY APPLICANT
(Not for submission under 37 CFR 1.99)

Application Number	11246163
Filing Date	2005-10-11
First Named Inventor	Tzannes
Art Unit	2142
Examiner Name	CALDWELL, ANDREW T
Attorney Docket Number	5550-54

	1	Written Opinion for International (PCT) Patent Application No. PCT/US2005/036015, mailed February 8, 2006	☐
	2	International Preliminary Report on Patentability for International (PCT) Patent Application No. PCT/US2005/036015, mailed April 26, 2007	☐

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EAST Search History

Ref #	Hits	Search Query	DBs	Default Operator	Plurals	Time Stamp
S1	3	"6707822".pn.	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2008/12/22 10:39
S2	4	"03063060"	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2008/12/22 10:44
S3	2	"6337877".pn.	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2008/12/22 10:49
S4	8	"6778596"	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2008/12/22 13:27
S5	2	"6778596".pn.	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2008/12/22 13:27
S6	38	("3573380" | "4131766" | "4568156" | "4679227" | "4731816" | "4802190" | "4912763" | "5048054" | "5128964" | "5206886" | "5285474" | "5327574" | "5400322" | "5428790" | "5452288" | "5479447" | "5497398" | "5521906" | "5533008" | "5555244" | "5596604" | "5598435" | "5625651" | "5636246" | "5644573" | "5682419" | "5812599" | "5822372" | "5822374" | "5910959" | "6009122" | "6011814" | "6052411" | "6072779" | "6084917" | "6188729" | "6480475" | "6665872").PN.	US-PGPUB; USPAT; USOCR	OR	OFF	2008/12/22 13:28
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S8	2	"7146391".pn.	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2008/12/29 08:38
S9	2	"20060088054"	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2008/12/29 08:40
S10	1	(allocat$3 near4 (two near4 portion$1)) near4 (shared adj memory) same (latency paths) same (interleavers) same (deinterleavers)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2008/12/29 08:47
S11	1	(allocat$3 near4 (two near4 portion$1)) near4 (shared adj memory) same (latency paths) same (interleav$4) same (deinterleav$4)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2008/12/29 08:47
S12	1	(allocat$3 near4 (two near4 portion$1)) with (shared adj memory) same (latency paths) and (interleav$4) and (deinterleav$4)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2008/12/29 08:48
S13	2	((two near4 portion$1)) with (shared adj memory) same (latency paths) and (interleav$4) and (deinterleav$4)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2008/12/29 08:49
S14	3	((two near4 portion$1)) with (memory) same (latency paths) and (interleav$4) and (deinterleav$4)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2008/12/29 08:49
S15	2	"6775320".pn.	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2008/12/29 09:31
S16	0	"707"/$,709/ $,711/147,169,708/$.ccls.	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2008/12/29 10:06
S17	2208	711/147,169.ccls.	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2008/12/29 10:06

S18	1	S17 and (shar$3 near3 memory) with (laten$4 adj path$1)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2008/12/29 10:07
S19	1	S17 and ((shar$3 or allocat $4 or manag$4) near3 memory) with (laten$4 adj path$1)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2008/12/29 10:08
S20	1	S17 and ((shar$3 or allocat $4 or manag$4) near3 memory) same (laten$4 adj path$1)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2008/12/29 10:08
S21	1255	S17 and ((shar$3 or allocat $4 or manag$4) near3 memory)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2008/12/29 10:09
S22	1034	S17 and ((shar$3) near3 memory)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2008/12/29 10:09
S23	495	S17 and ((allocat$3) near3 memory)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2008/12/29 10:09
S24	25	S17 and (((two or "2") adj (portion$1 or segment$1)) near4 memory)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2008/12/29 10:12
S25	2	"6778589".pn.	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2008/12/29 11:23
S26	0	"455".ccls.	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2008/12/30 08:41
S27	0	"455/$".ccls.	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2008/12/30 08:41

S28	129337	"455"/$.ccls.	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2008/12/30 08:41
S29	0	S28 and (latency adj path $1).ti,ab.	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2008/12/30 08:42
S30	41	(latency adj path$1).ti,ab.	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2008/12/30 08:42
S31	3	"20030091053"	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2008/12/31 11:24
S32	61025	((bit adj error adj (rate or ratio)) or ber)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2009/01/05 14:18
S33	2962	370/468.ccls.	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2009/01/05 14:20
S34	254	S32 and S33	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2009/01/05 14:20
S35	672	((bit adj error adj (rate or ratio)) or ber) with allocat$3	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2009/01/05 14:20
S36	12	S33 and S35	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2009/01/05 14:21
S37	1186	((bit adj error adj (rate or ratio)) or ber) same (interleav$3 or deinterleav $3)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2009/01/05 14:38

S38	44	((bit adj error adj (rate or ratio)) or ber) same (interleav$3 or deinterleav $3) same (latency)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2009/01/05 14:38
S39	1	S33 and S38	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2009/01/05 14:38
S40	16	((bit adj error adj (rate or ratio)) or ber) same (interleav$3 or deinterleav $3) same (latency) same path$1	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2009/01/05 14:39
S41	1	((bit adj error adj (rate or ratio)) or ber) same (interleav$3 or deinterleav $3) same (allocat$3 near4 (memory or buffer$1))	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2009/01/05 15:09
S42	1	((bit adj error adj (rate or ratio)) or ber) same (interleav$3 or deinterleav $3) same ((allocat$3 or assign$3) near4 (memory or buffer$1))	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2009/01/05 15:09
S43	104	((bit adj error adj (rate or ratio)) or ber) same (interleav$3 or deinterleav $3) same ((memory or buffer$1))	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2009/01/05 15:10
S44	3	((bit adj error adj (rate or ratio)) or ber) same (interleav$3 or deinterleav $3) same (shar$3 with (memory or buffer$1))	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2009/01/05 15:10
S45	3	"20030225808"	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2009/01/06 09:32
S46	49583	"711"/$.ccls.	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2009/02/03 14:57
S47	139	S46 and ((shar$3 near (buffer or memory)) and ((latency adj path$1) or channel$1 or $3interleav $3)).ti,ab.	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2009/02/03 14:57

S48	2161	709/213,214,215.ccls.	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2009/02/09 17:15

2/11/2009 11:05:42 AM
C:\Documents and Settings\jleung2\My Documents\EAST\Workspaces\2008\11246163_trans_res_sharing.wsp

CommScope, Inc.
IPR2023-00064, Ex. 1035
Page 348 of 531

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In Re the Application of:	)	Group Art Unit: 2142
	)	
TZANNES	)	Confirmation No.: **5478**
	)	
Application No.: 11/246,163	)	
	)	
Filed: 10/11/2005	)	
	)	
Atty. File No.: 5550-54	)	
	)	
For: "RESOURCE SHARING IN A TELECOMMUNICATIONS " ENVIRONMENT"	)	

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313

PRELIMINARY AMENDMENT

Dear Sir:

Prior to the initial review of the above-identified patent application by the Examiner, please enter the following Preliminary Amendment. Although Applicants do not believe that any fees are due based upon the filing of this Preliminary Amendment, please charge any such fees to Deposit Account 19-1970.

Please amend the above-identified patent application as follows:

CommScope, Inc.
IPR2023-00064, Ex. 1035
Page 349 of 531

AMENDMENTS TO THE SPECIFICATION:

Please amend the Specification beginning as follows:

[0003] U.S. Patent Nos. 6,775,320 and 6,778,589~~, which are both incorporated herein by reference in their entirety,~~ describe DSL systems supporting multiple applications and multiple framer/coder/interleaver FCI blocks (an FCI block is also referred to as a latency path). DSL systems carry applications that have different transmission requirements with regard to, for example, data rate, latency (delay), bit error rate (BER), and the like. For example, video typically requires a low BER (<1E-10) but can tolerate higher latency (>20 ms). Voice, on the other hand, typically requires a low latency (<1 ms) but can tolerate BER (>1E-3).

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IPR2023-00064, Ex. 1035
Page 350 of 531

REMARKS/ARGUMENTS

Applicant requests examination on the merits.

Applicant believes that the pending claim is in condition for allowance and such disposition is respectfully requested. In the event that a telephone conversation would further prosecution and/or expedite allowance, the Examiner is invited to contact the undersigned.

Respectfully submitted,

SHERIDAN ROSS P.C.

By: _____

Jason H. Vick
Registration No. 45,285
1560 Broadway, Suite 1200
Denver, Colorado 80202-5141
(303) 863-9700

Date: 17 Feb 01

J:\5550\-12\-DIV\-CON\AMEND_PRELIM_01.doc

CommScope, Inc.
IPR2023-00064, Ex. 1035
Page 351 of 531

Electronic Acknowledgement Receipt	
EFS ID:	4794020
Application Number:	11246163
International Application Number:	
Confirmation Number:	5478
Title of Invention:	Resource sharing in a telecommunications environment
First Named Inventor/Applicant Name:	Marcos C. Tzannes
Customer Number:	62574
Filer:	Jason Vick/Christine Jacquet
Filer Authorized By:	Jason Vick
Attorney Docket Number:	T3653-9285US01
Receipt Date:	13-FEB-2009
Filing Date:	11-OCT-2005
Time Stamp:	17:11:26
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	no

File Listing:

Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1		PRELIM_AMEND.pdf	132625 0e19a7af0e0d495c5847cd9b06e2dfb47e903000	yes	3

	Multipart Description/PDF files in .zip description		
	Document Description	**Start**	**End**
	Preliminary Amendment	1	1
	Specification	2	2
	Applicant Arguments/Remarks Made in an Amendment	3	3
Warnings:			
Information:			
	Total Files Size (in bytes):	132625	

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New Applications Under 35 U.S.C. 111
If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application.

National Stage of an International Application under 35 U.S.C. 371
If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.

New International Application Filed with the USPTO as a Receiving Office
If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.

PTO/SB/08a (08-03)
Approved for use through 07/31/2006. OMB 0651-0031
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INFORMATION DISCLOSURE STATEMENT BY APPLICANT (**Not for submission under 37 CFR 1.99)**		
	Application Number	11246163
	Filing Date	2005-10-11
	First Named Inventor	Tzannes
	Art Unit	2142
	Examiner Name	CALDWELL, ANDREW T
	Attorney Docket Number	5550-54

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Examiner Initial*	Cite No	Patent Number	Kind Code[1]	Issue Date	Name of Patentee or Applicant of cited Document	Pages,Columns,Lines where Relevant Passages or Relevant Figures Appear
	1	6778596		2004-08-17	Tzannes	
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Examiner Initial*	Cite No	Publication Number	Kind Code[1]	Publication Date	Name of Patentee or Applicant of cited Document	Pages,Columns,Lines where Relevant Passages or Relevant Figures Appear
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NON-PATENT LITERATURE DOCUMENTS			Remove
Examiner Initials*	Cite No	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc), date, pages(s), volume-issue number(s), publisher, city and/or country where published.	T[5]

INFORMATION DISCLOSURE STATEMENT BY APPLICANT (Not for submission under 37 CFR 1.99)		
	Application Number	11246163
	Filing Date	2005-10-11
	First Named Inventor	Tzannes
	Art Unit	2142
	Examiner Name	CALDWELL, ANDREW T
	Attorney Docket Number	5550-54

	1	Written Opinion for International (PCT) Patent Application No. PCT/US2005/036015, mailed February 8, 2006	☐
	2	International Preliminary Report on Patentability for International (PCT) Patent Application No. PCT/US2005/036015, mailed April 26, 2007	☐

If you wish to add additional non-patent literature document citation information please click the Add button Add

EXAMINER SIGNATURE

Examiner Signature		Date Considered	

*EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through a citation if not in conformance and not considered. Include copy of this form with next communication to applicant.

[1] See Kind Codes of USPTO Patent Documents at www.USPTO.GOV or MPEP 901.04. [2] Enter office that issued the document, by the two-letter code (WIPO Standard ST.3). [3] For Japanese patent documents, the indication of the year of the reign of the Emperor must precede the serial number of the patent document. [4] Kind of document by the appropriate symbols as indicated on the document under WIPO Standard ST.16 if possible. [5] Applicant is to place a check mark here if English language translation is attached.

INFORMATION DISCLOSURE STATEMENT BY APPLICANT (Not for submission under 37 CFR 1.99)		
	Application Number	11246163
	Filing Date	2005-10-11
	First Named Inventor	Tzannes
	Art Unit	2142
	Examiner Name	CALDWELL, ANDREW T
	Attorney Docket Number	5550-54

CERTIFICATION STATEMENT

Please see 37 CFR 1.97 and 1.98 to make the appropriate selection(s):

☐ That each item of information contained in the information disclosure statement was first cited in any communication from a foreign patent office in a counterpart foreign application not more than three months prior to the filing of the information disclosure statement. See 37 CFR 1.97(e)(1).

OR

☐ That no item of information contained in the information disclosure statement was cited in a communication from a foreign patent office in a counterpart foreign application, and, to the knowledge of the person signing the certification after making reasonable inquiry, no item of information contained in the information disclosure statement was known to any individual designated in 37 CFR 1.56(c) more than three months prior to the filing of the information disclosure statement. See 37 CFR 1.97(e)(2).

☐ See attached certification statement.

☐ Fee set forth in 37 CFR 1.17 (p) has been submitted herewith.

☒ None

SIGNATURE

A signature of the applicant or representative is required in accordance with CFR 1.33, 10.18. Please see CFR 1.4(d) for the form of the signature.

Signature	/Jason H. Vick/	Date (YYYY-MM-DD)	2007-05-23
Name/Print	Jason H. Vick	Registration Number	45285

This collection of information is required by 37 CFR 1.97 and 1.98. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 1 hour to complete, including gathering, preparing and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

Privacy Act Statement

The Privacy Act of 1974 (P.L. 93-579) requires that you be given certain information in connection with your submission of the attached form related to a patent application or patent. Accordingly, pursuant to the requirements of the Act, please be advised that: (1) the general authority for the collection of this information is 35 U.S.C. 2(b)(2); (2) furnishing of the information solicited is voluntary; and (3) the principal purpose for which the information is used by the U.S. Patent and Trademark Office is to process and/or examine your submission related to a patent application or patent. If you do not furnish the requested information, the U.S. Patent and Trademark Office may not be able to process and/or examine your submission, which may result in termination of proceedings or abandonment of the application or expiration of the patent.

The information provided by you in this form will be subject to the following routine uses:

1. The information on this form will be treated confidentially to the extent allowed under the Freedom of Information Act (5 U.S.C. 552) and the Privacy Act (5 U.S.C. 552a). Records from this system of records may be disclosed to the Department of Justice to determine whether the Freedom of Information Act requires disclosure of these record s.

2. A record from this system of records may be disclosed, as a routine use, in the course of presenting evidence to a court, magistrate, or administrative tribunal, including disclosures to opposing counsel in the course of settlement negotiations.

3. A record in this system of records may be disclosed, as a routine use, to a Member of Congress submitting a request involving an individual, to whom the record pertains, when the individual has requested assistance from the Member with respect to the subject matter of the record.

4. A record in this system of records may be disclosed, as a routine use, to a contractor of the Agency having need for the information in order to perform a contract. Recipients of information shall be required to comply with the requirements of the Privacy Act of 1974, as amended, pursuant to 5 U.S.C. 552a(m).

5. A record related to an International Application filed under the Patent Cooperation Treaty in this system of records may be disclosed, as a routine use, to the International Bureau of the World Intellectual Property Organization, pursuant to the Patent Cooperation Treaty.

6. A record in this system of records may be disclosed, as a routine use, to another federal agency for purposes of National Security review (35 U.S.C. 181) and for review pursuant to the Atomic Energy Act (42 U.S.C. 218(c)).

7. A record from this system of records may be disclosed, as a routine use, to the Administrator, General Services, or his/her designee, during an inspection of records conducted by GSA as part of that agency's responsibility to recommend improvements in records management practices and programs, under authority of 44 U.S.C. 2904 and 2906. Such disclosure shall be made in accordance with the GSA regulations governing inspection of records for this purpose, and any other relevant (i.e., GSA or Commerce) directive. Such disclosure shall not be used to make determinations about individuals.

8. A record from this system of records may be disclosed, as a routine use, to the public after either publication of the application pursuant to 35 U.S.C. 122(b) or issuance of a patent pursuant to 35 U.S.C. 151. Further, a record may be disclosed, subject to the limitations of 37 CFR 1.14, as a routine use, to the public if the record was filed in an application which became abandoned or in which the proceedings were terminated and which application is referenced by either a published application, an application open to public inspections or an issued patent.

9. A record from this system of records may be disclosed, as a routine use, to a Federal, State, or local law enforcement agency, if the USPTO becomes aware of a violation or potential violation of law or regulation.

Electronic Acknowledgement Receipt

EFS ID:	1802698
Application Number:	11246163
International Application Number:	
Confirmation Number:	5478
Title of Invention:	Resource sharing in a telecommunications environment
First Named Inventor/Applicant Name:	Marcos C. Tzannes
Customer Number:	62574
Filer:	Jason Vick/Debra Kesner
Filer Authorized By:	Jason Vick
Attorney Docket Number:	T3653-9285US01
Receipt Date:	23-MAY-2007
Filing Date:	11-OCT-2005
Time Stamp:	11:38:01
Application Type:	Utility

Payment information:

Submitted with Payment	no

File Listing:

Document Number	Document Description	File Name	File Size(Bytes)	Multi Part /.zip	Pages (if appl.)
1	Information Disclosure Statement (IDS) Filed	IDS_02.pdf	666602	no	4
Warnings:					

Information:					
2	NPL Documents	5550-54-PCT_Written_Opinion.pdf	983104	no	9
Warnings:					
Information:					
3	NPL Documents	5550-54-PCT_IPER.pdf	1236891	no	11
Warnings:					
Information:					
		Total Files Size (in bytes):	2886597		

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New Applications Under 35 U.S.C. 111
If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application.

National Stage of an International Application under 35 U.S.C. 371
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New International Application Filed with the USPTO as a Receiving Office
If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.

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Address: COMMISSIONER FOR PATENTS
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Alexandria, Virginia 22313-1450
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APPLICATION NUMBER	PATENT NUMBER	GROUP ART UNIT	FILE WRAPPER LOCATION
11/246,163		2152	2157

Correspondence Address / Fee Address Change

The following fields have been set to Customer Number 62574 on 09/01/2006

- Correspondence Address
- Maintenance Fee Address

The address of record for Customer Number 62574 is:
SHERIDAN ROSS P C
SUITE 1200
1560 BROADWAY
DENVER,CO 80202

UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NUMBER	PATENT NUMBER	GROUP ART UNIT	FILE WRAPPER LOCATION
11/246,163		2152	2157

Correspondence Address / Fee Address Change

The following fields have been set to Customer Number 62574 on 08/10/2006

- Correspondence Address
- Maintenance Fee Address

The address of record for Customer Number 62574 is:
JASON H. VICK
SUITE 500
1751 PINNACLE DRIVE
MCLEAN,VA 22102-3833

UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NUMBER	PATENT NUMBER	GROUP ART UNIT	FILE WRAPPER LOCATION
11/246,163		2186	2157

Correspondence Address / Fee Address Change

The following fields have been set to Customer Number 62574 on 08/02/2006

- Correspondence Address
- Maintenance Fee Address

The address of record for Customer Number 62574 is:
JASON H. VICK
SUITE 500
1751 PINNACLE DRIVE
MCLEAN,VA 22102-3833

OIPE IAP45 MAY 17 2006 PATENT & TRADEMARK OFFICE

Attorney Docket No. T3653-9285US01

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Patent Application of:

First Named Inventor: TZANNES, MARCOS C. **Art Unit: 2186**

Application No.: 11/246,163 **Examiner:**

Filed: October 11, 2005 **Confirmation No.: 5478**

For: SHARING MEMORY AND PROCESSING RESOURCES IN DSL SYSTEMS

* * *

INFORMATION DISCLOSURE STATEMENT

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Sir:

Pursuant to 37 C.F.R. § 1.56, and without any assertion as to materiality or prior art effect, the documents listed on the attached Form PTO/SB/08A are hereby cited.

The Commissioner is hereby authorized to charge to Deposit Account No. 50-1165 (T3653-9285US01) any fees under 37 C.F.R. §§ 1.16 and 1.17 that may be required by this paper and to credit any overpayment to that Account. If any extension of time is required in connection with the filing of this paper and has not been separately requested, such extension is hereby requested.

Respectfully submitted,

Date: May 17, 2006

By: _____
Jason H. Vick
Reg. No. 45,285

Miles & Stockbridge, P.C.
1751 Pinnacle Drive
Suite 500
McLean, Virginia 22102-3833
(703) 903-9000

OIPE IAP45 MAY 17 2006 PATENT & TRADEMARK OFFICE

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PTO/SB/08A (08-03)

Approved for use through 07/31/2006. OMB 0651-0031

U.S. Patent and Trademark Office: U.S. DEPARTMENT OF COMMERCE

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Substitute for form 1449A/PTO

INFORMATION DISCLOSURE STATEMENT BY APPLICANT

(use as many sheets as necessary)

Sheet 1 of 2

Complete it Known	
Application Number	11/246,163
Filing Date	October 11, 2005
First Named Inventor	TZANNES, MARCOS C.
Art Unit	2186
Examiner Name	
Attorney Docket Number	T3653-9285US01

U.S. PATENT DOCUMENTS

Examiner Initials*	Cite No. [1]	U.S. Patent Document Number	Kind Code [2] (if known)	Name of Patentee or Applicant of Cited Document	Publication Date MM-DD-YYYY	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear
		6,337,877		Cole et al.	01-08-2002	
		6,707,822		Fadavi—Ardekani et al.	03-16-2004	
		6,775,320		Tzannes et al.	08-10-2004	
		6,778,589		Ishii, Satoru	08-17-2004	

FOREIGN PATENT DOCUMENTS

Examiner Initials*	Cite No. [1]	Foreign Patent Document Office [3]	Number [4]	Kind Code [5] (if known)	Name of Patentee or Applicant of Cited Document	Publication Date MM-DD-YYYY	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear	T [6]
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Sheet 2 of 2

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OTHER PRIOR ART – NON PATENT LITERATURE DOCUMENTS

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		International Application WO 2006/04427 A1, published on April 27, 2006	
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		http://www.sunrisetelecom.com/technotes/APP-xDSL-8B.pdf, "Sunset xDSL: Prequalification of ADSL Circuits with ATU-C Emulation" 2001, page 3, Sunrise Telecom Inc., Application Series, San Jose, USA, XP002363272	

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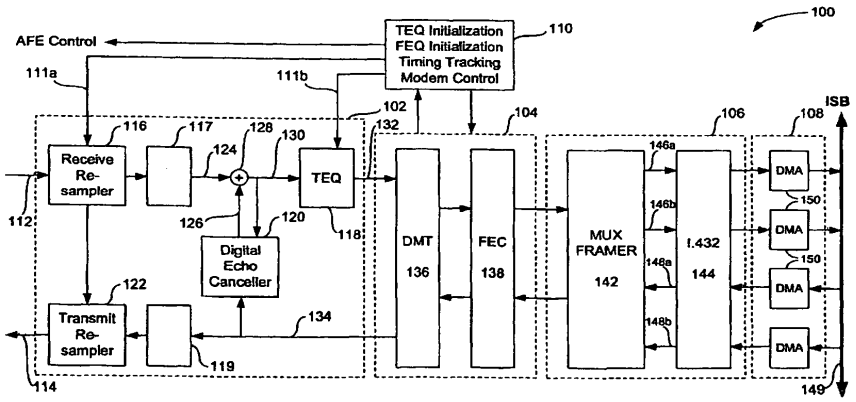
(54) Title: ASYMMETRIC DIGITAL SUBSCRIBER LINE MODEM APPARATUS AND METHODS THEREFOR



(57) Abstract: Provided is a system and method for a modem including one or more processing paths. Also included is a number of interconnected modules sequentially arrayed along the one or more paths. Each module is configured to (i) process signals passed along the paths in accordance with the sequence and (ii) implement predetermined functions to perform the processing. Further, each of the modules has a particular degree of functional programmability and the degrees of functional programmability monotonically vary in accordance with the sequence.

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ASYMMETRIC DIGITAL SUBSCRIBER LINE MODEM APPARATUS AND METHODS THEREFOR

BACKGROUND OF THE INVENTION

Field of the Invention

The present invention generally relates to communications, and more specifically to a highly integrated asymmetric digital subscriber line (ADSL) circuit chip for communications.

Background Art

An ADSL is used for data communications between a central office (CO) and customer premise equipment (CPE). At the CPE, an ADSL transceiver transmits and receives ADSL data to and from the central office. Conventional ADSL transceivers include an analog front end (AFE), a discrete multi-tone module (DMT), a forward error correction (FEC) module, a multiplexer/framer module, a protocol module, and a direct memory access (DMA) module.

BRIEF SUMMARY OF THE INVENTION

Consistent with the principles of the present invention as embodied and broadly described herein, an embodiment of the present invention includes a modem comprising one or more processing paths. Also included is a number of interconnected modules sequentially arrayed along one or more of the paths. Each module is configured to (i) process signals passed along the paths in accordance with the sequence and (ii) implement predetermined functions to perform the processing. Further, each of the modules has a particular degree of functional programmability and the degrees of functional programmability monotonically vary in accordance with the sequence.

Another embodiment of the invention includes a modem comprising a receive re-sampler associated with a receive timing scheme and a transmit re-sampler associated with a transmit timing scheme. Only one timing

mechanism is provided. The timing mechanism is (i) electrically coupled to the receive re-sampler and the transmit re-sampler and (ii) configured to synchronize the receive and transmit timing schemes.

A further embodiment of the invention includes a method for de-interleaving a data stream stored in a buffer having a plurality of memory locations, each location having a memory width of (W) bytes, the data stream being formed of a number of data words each including (N) number of data bytes, wherein (N) is a non-integer multiple of the width (W). The method comprises storing the data words into respective memory locations. The method also includes appending each of the copied data words with a number (X) of dummy bytes, a sum of (N) + (X) being an integer multiple of the width (W) and storing the appended dummy bytes into the respective memory locations.

Still another embodiment of the present invention includes a circuit comprising a fast fourier transform (FFT) address generator configured to produce a complex FFT (computation) address sequence, the complex FFT address sequence includes fixed offsets. Also included is a conversion mechanism configured to (i) receive the complex FFT address sequence and (ii) convert the received sequence into an address sequence having varying offsets.

A further embodiment of the present invention includes a method for implementing a SLICE operation in a programmable digital signal processor (DSP) as a primitive instruction in one or more data paths of a single instruction multiple data scheme (SIMD).

Yet another embodiment of the present inventions includes a method for sharing one or more memories between one or more processors, each memory being associated with a respective ownership flag. The method comprises associating each of the processors with a particular value of the flag and assigning use of the memories to a corresponding one of the processors when the respective ownership flag is set to the particular value.

Further features and advantages of the present invention, as well as the structure and operation of various embodiments of the present invention, are described in detail below with reference to the accompanying drawings.

BRIEF DESCRIPTION OF THE DRAWINGS/FIGURES

The accompanying drawings, which are incorporated in and constitute part of the specification, illustrate embodiments of the invention and, together with the general description given above and detailed description of the embodiments given below, serve to explain the principles of the present invention.

FIG. 1 is a block diagram of an exemplary ADSL modem;

FIG. 2 is a block diagram of an alternative view of the functional modules of the modem of FIG. 1;

FIG. 3 is a block diagram further expanding on the block diagram of FIG. 1;

FIG. 4 is a more detailed view of the exemplary control processor shown in FIG. 2;

FIG. 5 is an exemplary illustration of a decoded byte stream;

FIG. 6 is an illustration of an exemplary memory buffer configured to receive the data stream of FIG. 5 in accordance with an embodiment of the present invention;

FIG. 7 is a table of exemplary parameters associated with the memory buffer of FIG. 6;

FIG. 8 is a table of exemplary address sequences associated with the memory buffer of FIG. 6 and the parameters table of FIG. 7;

FIG. 9 is an illustration of conventional processing modules associated with implementing a fast Fourier transform (FFT);

FIG. 10 is an illustration of conventional FFT computational butterflies configured to implement a pre-processing in the FFT of FIG. 9;

FIG. 11 is an illustration of conventional FFT computational butterflies configured to implement a post-processing in the FFT of FIG. 9;

FIG. 12 is a block diagram illustration of an exemplary circuit configured in accordance with an embodiment of the present invention;

FIG. 13 is an illustration of data generation associated with the circuit of FIG. 12;

FIG. 14 is an illustration of exemplary output address sequences produced in accordance with an embodiment of the present invention;

FIG. 15 is a block diagram illustration of a conventional data processing path of a DSP;

FIG. 16 is a block diagram illustration of modifications to the illustration of FIG. 15 in accordance with an embodiment of the present invention;

FIG. 17 is an illustration of an exemplary slice decoder used in the system of FIG. 16;

FIG. 18 is a graphical representation of an exemplary constellation grid used in an embodiment of the present invention;

FIG. 19 is an illustration of an exemplary quantizer used in the system of FIG. 16;

FIG. 20 is a table illustrating output cycles of an embodiment of the present invention;

FIG. 21 is block diagram of an exemplary memory sharing scheme configured in accordance with an embodiment of the present invention;

FIG. 22 is an illustration of exemplary instruction used in the memory sharing scheme depicted in FIG 21; and

FIG. 23 is an illustration of additional exemplary instructions used in the memory sharing scheme depicted in FIG. 21.

DETAILED DESCRIPTION OF THE INVENTION

The following detailed description of the accompanying drawings illustrates exemplary embodiments consistent with the present invention. Other embodiments are possible, and modifications may be made to the embodiments within the spirit and scope of the invention. Therefore, the

following detailed description is not meant to limit the invention. Rather, the scope of the invention is defined by the appended claims.

It would be apparent to one of skill in the art that the present invention, as described below, may be implemented in many different embodiments of hardware, software, firmware and/or the entities illustrated in the figures. Any actual software code with the specialized control hardware to implement the present invention, is not limiting of the present invention. Thus, the operation and behavior of the present invention will be described with the understanding that modifications and variations of the embodiments are possible, given the level of detail presented herein.

I. Functional programmability.

FIG. 1 is a block diagram of an exemplary ADSL modem 100. Different aspects of the present invention reside in the environment of the modem 100. The modem 100 includes a first portion 102 including fixed components (also referred to as modules), a second portion 104 including programmable modules, a third portion 106 also including programmable modules, and a data transfer portion 108.

The modem 100 also includes a control module 110 including a plurality of control modules that perform modem control, receive signal timing recovery and tracking, equalizer (TEQ and FEQ) initialization and filter initialization. The control module 110 provides control signals 111a, 111b, and 111c (collectively, signals 111) to components within the first portion 102, described below, as well as to components with the second portion 104. In a receive direction, the modem 100 receives a digitized receive signal 112 having a fixed sample rate of 4 MHz from an analog-to-digital converter (ADC) (not shown). In a transmit direction, the modem 100 provides a digitized transmit signal 114 having a fixed sample rate of 2 MHz to a digital-to-analog converter (DAC) (not shown).

The fixed portion 102 includes a receive re-sampler 116, a receive integer decimator 117, a time domain equalizer (TEQ) 118, a digital echo

canceler 120, an integer interpolation module 119 and a transmit re-sampler 122. In the receive direction, the receive re-sampler 116 re-samples/retimes signal 112 to produce a re-sampled/retimed signal 320 having a sample rate of twice the ADSL sample rate of 2.208 MHz. The receive integer decimator 117 is a finite impulse response (FIR) filter that downsamples the signal 320 to produce the signal 124. In other words, the receive re-sampler 116 in conjunction with the receive integer decimator 117 converts the fixed 4 MHz sample rate of the received signal 112 to the ADSL sample rate of 2.208 MHz.

A digital echo canceler 120 cancels undesired echo from the signal 124. The canceler 120 provides an echo canceling signal 126 to a subtractor 128. The subtractor 128 subtracts the echo canceling signal 126 from the signal 124, to produce a signal 130. The signal 130 is applied to the canceler 120 as an error signal, and also to the TEQ 118.

The TEQ 118 is a finite impulse response (FIR) filter having programmable filter coefficients. The TEQ 118 has a filter response/transfer function that reduces inter-symbol interference in the receive signal 112, caused by the receive channel from which the signal 112 was received. The TEQ 118 provides an equalized signal 132 to the portion 104 of the modem 100.

In a transmit direction, the portion 104 provides a transmit signal 134 to the module 119 and the digital echo canceler 120. The module 119 consists of a series cascade of finite impulse response (FIR) filters and interpolates the signal 134 by an integer factor to produce the signal 360. The transmit re-sampler 122 re-samples/re-times signal 360 to produce the re-sampled/retimed transmit signal 114. The transmit re-sampler 122 up-samples the signal 360 to produce the signal 114. In other words, the transmit re-sampler 122 converts the 2.208 MHz sample rate of the received signal 360 to the DAC sample rate of 2.0 MHz.

It would be apparent to one skilled in the art that the receive re-sampler 116 output sample rate and the transmit re-sampler 122 input sample rate will be slightly different than 4.416 MHz and 2.208 MHz respectively if there is any clock error in the system.

The receive re-sampler 116, the TEQ 118, and the transmit re-sampler 122, each receive control information, such as filter coefficients, as well as other control signals, from the control modules of the control module 110.

The receive re-sampler 116, the receive integer decimator 117, the TEQ 118, the integer interpolation module 119, the echo canceler 120, and the transmit re-sampler 122 are implemented as hardware modules using "fixed gates." This means that each of the modules 116-122 performs a sequence of operations in a predetermined order that cannot be changed. Each of the modules 116-122 may be selectively enabled and disabled. However, the order of processing steps implemented by each hardware module, alone, and together with the other modules within the portion 102, will always remain the same.

The programmable portion 104 includes a DMT module 136 and an FEC module 138. Together, the DMT/FEC modules 136/138 are referred to as a DMT/FEC accelerator. To process signals flowing in the receive direction, the DMT module 136 includes, in series, a fast Fourier transform (FFT) module to perform FFTs, a frequency domain equalizer (FEQ) to perform frequency domain equalization, and a symbols-to-bits mapper to map symbols-to-bits. Symbol-to-bit mapping optionally includes trellis decoding. To process signals flowing in the transmit direction, the DMT module 136 includes a bits-to-symbols mapper, a gain scaler, and an inverse fast Fourier transform (IFFT) module to perform IFFTs. Bit-to-symbol mapping optionally includes trellis encoding.

To process signals flowing in the receive direction, FEC module 138 includes a Reed-Solomon decoder. To process signals flowing in the transmit direction, the FEC 138 includes a Reed-Solomon encoder.

The DMT/FEC accelerator (the portion 104 of the modem 100) is programmable, and thus more flexible than the portion 102 of the modem 100. In other words, the DMT/FEC accelerator 104 has a higher degree of functional programmability than the portion 104. For example, the various functions performed by the modules within the DMT/FEC accelerator 104 may be changed and permuted over time. A control processor (not shown in

FIG. 1) controls the sequencing of these operations depending on the various modes in which the modem 100 may operate.

For example, as the modem 100 traverses various stages of ADSL signal training, the sequence of operations performed by the DMT/FEC accelerator 104 changes correspondingly. This may be referred to as "modality flexibility" within the DMT/FEC accelerator. In the instant embodiment, the DMT/FEC accelerator 104 is implemented as a combination of hardware and software. An implementation of both hardware and software facilitates the modality flexibility. The DMT/FEC accelerator 104 is programmed to accommodate signal training, and to implement a relatively complicated ADSL handshake that occurs, between the ADSL modem 100 and the central office modem.

Next, the portion 106 of the modem 100 includes a multiplexer/framer 142 and a protocol engine 144. In the receive direction, the multiplexer/framer 142 receives a bit stream from the FEC module 138, and demultiplexes the bit stream into two separate asynchronous transfer mode (ATM) receive channels 146a and 146b. The multiplexer/framer 142 provides the ATM channels 146a and 146b to the protocol engine 144. In the transmit direction, the protocol engine 144 provides two ATM transmit channels 148a and 148b to the multiplexer/framer 142. The multiplexer/framer 142 multiplexes the transmit ATM channels 148a and 148b into a transmit bit-stream 150 for the FEC 138.

The protocol engine 144 operates in accordance with an ATM standard I.432. ATM standard I.432 governs the manner in which ATM cells are constructed and Cyclic Redundancy Codes (CRCs) are computed. Thus, the protocol engine 144 verifies/validates received ATM cells, and generates transmit ATM cell information, such as CRCs, among other things.

A data transfer portion 108 is coupled between the protocol engine 144 and an internal system bus (ISB) 149. The data transfer portion 108 transfers ATM cells or bytes in and out of the modem 100. The data transfer portion 108 includes a plurality of DMA engines 150 for transferring data between the ISB 149 and the protocol engine 144, and other portions of the modem 100.

The portion 106 is completely in software. Thus, the portion 106 has a higher degree of functional programmability than the DMT/FEC accelerator 104, the fixed portion 102, and the data transfer portion 108. The functions associated with the portion 106 are programmable and flexible. For example, protocol engine 144 may operate in accordance with I.432 or any other suitable protocol. Alternatively, as the standard for ADSL evolves, the multiplexer/framer module may be rewritten to accommodate new framing specifications.

FIG. 2 is a block diagram of an alternative view of the functional modules of the modem 100. In the view of FIG. 2, the modem 100 includes an AFE processor 202 corresponding to the portion 102 illustrated in FIG. 1, a DMT/FEC accelerator 204 corresponding to the portion 104 in FIG. 1, a control processor 205 (not specifically depicted in FIG. 1), and a host interface (I/F) 208 corresponding to the data transfer portion 108 in FIG. 1. Also included in the view of FIG. 2 is a multiplexer 210 and a RAM 212 in which communication data and information may be stored.

As described above, the modem portions 102, 104, and 106 are implemented using progressively (monotonically) increasing degrees of programmable functionality and flexibility. The ADSL modem environment is very cost sensitive, so cost reduction is critical. The design of the modem 100 achieves cost optimization where possible, and retains flexibility where necessary. This includes reducing cost where little flexibility is needed. Less flexibility is required in the portion 102 compared to the portions 104 and 106. Thus, the portion 102 is implemented as cheaply as possible, using fixed hardware functions that have virtually zero functional programmability.

The portion 104 is more flexible and functionally programmable than the portion 102 because it is implemented as a combination of hardware and software. And, the portion 106 is even more flexible and more functionally programmable than the portion 104 because it is implemented almost entirely in software. Further aspects of the present invention, in particular the modem 100, will be described in additional detail below.

II. Common Phase Accumulator.

An ADC converts a continuous time signal into a sequence of digital samples. The sampling rate is determined by the physical ADC sample clock. Conversely, a DAC converts a sequence of digital samples into a continuous time signal. The sampling rate of the digital samples is determined by the physical DAC sample clock. The underlying sampling rate of the incoming digital samples at a typical receiver (e.g., the signal 112 in FIG. 1) or the outgoing digital samples at the transmitter (e.g., the signal 114 in FIG. 1) can be altered by adjusting the physical ADC/DAC sample clocks. This approach can be expensive because it requires additional analog components. Instead, a more economical approach is to use digital resampling in the receive and transmit directions to properly re-sample/retime the receive samples from the ADC and the transmit samples sent to the DAC.

Digital re-samplers, such as the re-samplers 116 and 122 in FIG. 1, are digital filters that re-sample input signals by arbitrary rates and phase. In other words, the ratio of the input sample rate to the output sample rate need not be an exact ratio of integers. Their operation is controlled by two basic variables: phase increment and phase accumulator. The phase increment is a normalized time increment and is the ratio of the input sampling rate to the output sampling rate. The phase accumulator keeps track of the current time position (in normalized units).

In the receive direction, the combination of the ADC and the receive re-sampler 116 can effectively be viewed as an equivalent ADC whose sample rate is equal to the receive re-sampler output sample rate. Similarly, in the transmit direction, the combination of the transmit re-sampler 122 and the DAC can be viewed as an equivalent DAC whose input sample rate is equal to the transmit re-sampler input sample rate.

In an ADSL system, the ADSL transceiver unit remote terminal (ATUR) modem, derives an estimate of the ADSL transceiver unit-central office (ATUC) modem's symbol clock frequency and phase from the received signal. In the present invention, the modem 100 is the ATUR modem. The

symbol clock derived by the ATUR is then used for both detection of the received signal as well as transmission of the upstream signal to the ATUC. The ATUC modem uses the same clock for both transmission and reception. This process is known as loop timing.

Since the ATUR transmitter timing is derived from the ATUR receiver, there must be a mechanism in place to ensure that the timing of the ATUR transmitter and receiver remains locked. It is extremely desirable that the timing between the transmitter and the receiver does not drift or skew. In conventional implementations, which use two re-samplers (one in the receive path and a second in the transmit path) to produce digital samples at the desired rate, it is difficult to ensure that timing will remain locked since each re-sampler uses its own independent phase accumulator (and phase increment). The use of a single phase accumulator will ensure that the timing of the re-samplers 116 and 122 remains locked. The single phase accumulator approach is implemented in the modem 100, as is described below in connection with FIG. 3.

FIG. 3 is a block diagram that expands the illustration of the receive re-sampler 116, the transmit re-sampler 122, and the DMT 136, shown in FIG. 1. The receive re-sampler 116 includes the re-sampler 302 capable of up-sampling by a non-integer number and a re-sampler controller 306 coupled to a re-sampler coefficient generator 308. The re-sampler controller 306 includes a common phase accumulator register (i.e., phase accumulator) 309 that is shared between the receive re-sampler 116 and the transmit re-sampler 122.

Based upon inputs from the single phase accumulator 309, the re-sampler controller 306 produces re-sampler control signals 312. In response to the re-sampler control signals 312, the coefficient generator 308 provides a set of receive re-sampler coefficients 314 to the re-sampler 302. More specifically, the controller 306 uses the contents of the phase accumulator 309 to produce the correct coefficients 314 to be used for the computation of the current output sample of the interpolated signal 320.

The transmit re-sampler 122 includes a non-integer transmit re-sampler 326. In a manner similar to that described above, the re-sampler control

signals 312, derived from the phase accumulator 309, prompt the coefficient generator 308 to produce updated transmit re-sampler coefficients 330 and to provide the coefficients 330 to the non-integer transmit re-sampler 326. In response, the transmit re-sampler 326 computes an output sample of the interpolated signal, i.e., the digitized transmit signal 114. The controller 306 performs a fixed mapping of the contents of the phase accumulator 309, prompting the coefficient generator 308 to produce the transmit coefficients 330. Thus, the single phase accumulator 309 ensures that the timing of the re-samplers 116 and 122 remains locked.

An FFT block 340, incorporated within the DMT 136, is also depicted in FIG. 3. Based upon the interpolated signal 320, the FFT module 340 produces a signal 342 and provides the signal 342 to the timing tracking modem control portion of the module 110. The timing tracking portion of the control module 110 provides the signals 111, including control signals and updated filter coefficients, to various modules within the portion 102 (AFE processor) of the modem 100.

In more specific terms, the timing tracking portion of the module 110 provides a phase increment signal 350, a phase tweak signal 352, and an out_bank_coeff_factor signal 354 to the re-sampler controller 306. These signals alter and/or act in accordance with the phase accumulator 309 and, therefore, ultimately control the phase values associated with the coefficients 314 and 330, produced by the coefficient generator 308. Thus, the single phase accumulator 309 provides mapping between the receive re-sampler 302 and the transmit re-sampler 326. This mapping provides perfect synchronized timing between the receive signal 112 and the transmit signal 114.

The modem 100 includes a receive signal timing recovery/tracking loop including the modules 302, 117, 128, 118, 310, 110, 306, 308, and 309 described above. The timing recovery loop recovers receive timing in the receive direction, and adjusts all or some of the signals 350, 352 and 354 to match the receive timing. Integral to the this operation is the use of the common phase accumulator 309 for both receive and transmit re-sampling timing control. The present invention, therefore, provides a type of one-to-one

mapping between the receive re-sampler 116 and the transmit re-sampler 122 in order to update the common phase accumulator 309 within the timing recovery loop to achieve timing synchronization. The operation of the phase accumulator 309, in connection with control signals 111, and with reference to FIG. 3 is in greater detail below. It would be apparent to one skilled in the art that the implementation described below with some modification could be extended for other sample rates at the receive and transmit re-sampler inputs and outputs 112 320 360 114.

The following terms are defined in relation to the exemplary embodiments of FIGs. 1-3:

- phaseAcc: phase accumulator
  The common phase accumulator 309 is a 32 bit register that acts as a modulo 32 bit counter. The phase accumulator 309 is updated by incrementing with the phase increment.

- phaseInc: phase increment
  The phase increment 350 is 32 bit register. It represents the ratio of re-sampler 302 input sample rate to re-sampler 302 output sample rate expressed as a 32 bit integer with 2^{29} representing 1.0 normalized time unit (normalized by the re-sampler 302 input sampling period); in other words, nominally phaseInc is

$$\text{phaseInc} = \text{ROUND}\left(2^{29} \cdot \frac{4.0}{4.416}\right).$$

  Before any timing information is available, the phase increment 350 is initialized with the nominal value of phaseInc given above. The phase increment is updated by the modem once the initial clock frequency error has been estimated. It would be apparent to one skilled in the art how this would be done.

- bankFactor:
  The bankFactor is a 16 bit scale factor (1.15 format) used in the computation of the transmit re-sampler phase used to produce transmit re-sampler coefficients 330. The bankFactor is calculated as

$$\text{bankFactor} = \text{ROUND}\left(2^{15} \cdot \frac{1}{2 \cdot \phi}\right)$$

where φ is the ratio of re-sampler 302 input sample rate to re-sampler 302 output sample rate.

- receive re-sampler 302 control variables

bit29[n]: (phaseAcc[31:0] & 0x20000000) >> 29 (for current phaseAcc)
bit29[n-1]: (phaseAcc[31:0] & 0x20000000) >> 29 (for previous phaseAcc)

These variables are used to detect the crossing of a 4.0 MHz boundary indicating a new input sample from the ADC must be pushed onto the re-sampler 302 delay line.

- transmit re-sampler 122 control variables

bit30[n]: (phaseAcc[31:0] & 0x40000000) >> 30 (for current phaseAcc)
bit30[n-1]: (phaseAcc[31:0] & 0x40000000) >> 30 (for previous phaseAcc)

These variables are used to detect the crossing of a 2.0 MHz boundary indicating that a new output sample must be computed by the transmit re-sampler 122. The transmit re-sampler 122 processes the phaseAcc every second phase increment (ie., for every other value of the phaseAcc) and thus the meaning of current and previous in the above defintions should be understood in this context

- constants

```
nPhaseBits: 4
nInterpBits: 8        /* used in linear interpolation */
phaseShift: (29 – nPhaseBits) = 25
nCoeffs:    10        /* number of coefficients per phase */
```

The coefficients 314 and 330 are derived from the same set of fixed coefficients as will be explained later. The fixed coefficients are extracted from a prototype filter and stored as 16 phases or banks (bank 0, 1, ..., 15) with each bank containing 10 coefficients. One additional bank, bank 16, is

also stored and is obtained from bank 0 by a circular shift of one sample. It would be apparent to one skilled in the art how bank 16 is generated. It would also be apparent to one skilled in the art that there are many different methods of generating coefficients 314 and 330.

- constraints

  constraint: phaseInc[31:0] < 2^{29}

  This constraint prevents the crossing of 2 successive 4.0 MHz boundaries with a single increment of the phase accumulator; i.e., this constraint ensures that the phaseAcc can not wrap twice mod 2^{29} with a single increment of the phase accumulator.

The receive re-sampler 116 computes bit29[n] for every value of phaseAcc. A wrap mod 2^{29} has occurred if the XOR of bit29[n] and bit29[n-1] is 1. This wrap signifies that a new input sample must be shifted into the re-sampler 302 delay line before the current output sample can be computed. The receive re-sampler 116 computes an output sample for every value of phaseAcc. The coefficients used to compute the output sample are obtained via linear interpolation as:

```
rcvPhase[3:0] = (phaseAcc[31:0] & 0x1fffffff) >> phaseShift
c0Ptr         = coeffPtr + (rcvPhase[3:0] * nCoeffs)
alpha[7:0]    = (phaseAcc[31:0] & 0x01fe0000) >> (phaseShift –
nInterpBits)
c1Ptr         = c0Ptr + nCoeffs
coeffs[k]     = c0Ptr + ((c1Ptr[k] – c0Ptr[k]) * alpha[7:0]) >>
nInterpBits
```

NOTE:
coeffPtr is a pointer to the fixed set of 17 banks of coefficients.

The transmit re-sampler 122 operates in a similar fashion. The transmit re-sampler 122 computes bit30[n] for every other value of phaseAcc. A wrap mod 2^{30} has occurred if the XOR of bit30[n] and bit30[n-1] is 1. This signifies that a new output sample must be computed. The coefficients used to compute the output sample are obtained via linear interpolation as:

```
        tmp                 = 0x20000000 – ((phaseAcc[31:0] & 0x3fffffff)
>> 15) * bankFactor
        tmp                 = MAX([0, tmp])
        xmtPhaseTmp[4:0}    = tmp >> phaseShift
        xmtPhase[3:0]       = LIMIT(xmtPhaseTmp[4:0], 0, 15)
        alphaTmp[31:0]      = tmp – (xmtPhase[3:0] << phaseShift)
        alpha[8:0]          = alphaTmp >> (phaseShift – nInterpBits)
        c0Ptr               = coeffPtr + (xmtPhase[3:0] * nCoeffs)
        c1Ptr               = c0Ptr + nCoeffs
        coeffs[k]           = c0Ptr + ((c1Ptr[k] – c0Ptr[k]) * alpha[8:0]) >>
nInterpBits
```

NOTE:
coeffPtr is a pointer to the fixed set of 17 banks of coefficients.

The phaseInc and bankFactor parameters should be updated atomically in order to ensure that there are no glitches in the xmtPhase computation. A new input sample is shifted into transmit re-sampler 122 delay line with every other increment of the phase accumulator 309.

The ATUR receiver continuously extracts timing information from the received signal and updates the control signals 350 352 and 354 in order to track any clock drift that may occur in the system.

There are several different ways to update the timing of the re-samplers: 1) through use of a phase tweak (periodically adjust the phase accumulator), 2) through update of the phase increment, or 3) using a combination of 1) and 2). In the former case, the phase tweak is applied in conjunction with the phase increment when incrementing the phase accumulator 309. If Δ represents the adjustment to be applied to the phase accumulator 309, it is performed by using a phase tweak given by

$$\text{phaseTweak}[31:0] = \text{phaseInc}[31:0] + \frac{\Delta}{2}$$

for 2 consecutive phase increments (the phase tweak acts as the phase increment for 2 consecutive phase increments). The phase tweak must be limited to be less than 2^{29} otherwise it would be possible to wrap twice modulo 2^{29} with a single increment of the phase accumulator 309. The use of

the common phase accumulator 309 shared between the receive re-sampler 116 and transmit re-sampler 122 ensures that receive and transmit timing is locked.

III. Copying DMA With Two Separate Strides Selected by a Modulo-n Counter to Perform Convolutional De-interleaving.

In a communication system employing convolutional interleaving (such as an ADSL), it is necessary for the receiver to de-interleave the decoded data stream. A data buffer is used to implement the de-interleaving process. For each codeword-sized interleaved data block decoded and written into the data buffer, a single de-interleaved codeword is read from the data buffer. Because the data buffer requires substantial storage capacity, up to 16 KB for an ADSL system, it is desirable to share a single physical memory between the de-interleaving data buffer, other receiver system I/O buffers, and program and data storage. This type of shared memory architecture is known as a unified memory architecture (UMA).

The problem, however, with using traditional UMAs is that the codeword-sized blocks written to the de-interleaving data buffer are not an integer multiple of the width of the shared physical memory. This complicates the write interface to the shared memory by requiring it to perform alignment of the codeword-sized block and partial word writes in order to append the block to the existing data buffer contents. The second stride is also adjusted to account for a dummy byte added at the input to the interleaver (to make the interleaved block size relatively prime to the interleave depth) but not transmitted, as in systems like ADSL. The write interface is further complicated by the need to re-insert a dummy byte added at the input to the interleaver (to make the interleaved block size relatively prime to the interleave depth) but not transmitted. As a solution, the present invention uses a DMA scheme with two separate strides to copy codewords from the de-interleaving data buffer..

FIG. 4 is an illustration of a more detailed block diagram of the control processor 205, shown in FIG. 2. The control processor 205 is an example of a control processor, or DPS, suitable for implementing the DMA scheme of the present invention. In FIG. 4, the control processor 205 includes a central processing unit (CPU) 400, a memory 402, and an input/output interface 403. The DMA engine 404, responsible for implementing the DMA functions, includes a DMA memory storage area 406.

The DMA storage area 406 includes an exemplary de-interleaving data buffer 408, along with other DMA related storage locations. The DMA scheme is implemented using a DMA engine 404 to execute the overall DMA operations associated with the control processor 205. Thus, the DMA engine 404 receives data, via the control processor 205, based upon a received signal, such as the digitized signal 112. The received data is then placed into the data buffer 408 for de-interleaving. The data is read from the data buffer 408, or de-interleaved, in accordance with the DMA engine 404, selected DMA parameters (discussed in greater detail below), and a modulo counting scheme. The modulo counting scheme is accomplished using an exemplary modulo counter 410.

In the present invention, the use of two separate strides, for placing the data into the data buffer 408 allows the codeword-sized blocks, written to the buffer, to be appended with dummy bytes. This padding enables the codeword sized blocks to be translated to a size, or format, that is an integer multiple of the shared physical memory width. The size conversion simplifies the write interface by eliminating the need for data alignment and partial word writes into the shared memory.

The first stride specifies the increment between codeword elements necessary to perform the basic de-interleaving operation. The second stride allows the DMA engine 404 to skip over the dummy padding every codeword-size bytes. The wrapping of a modulo-n counter indicates when the second stride should be used to perform the skip.

FIG. 5 is an illustration of an exemplary decoded serial byte stream 500, segmented into codeword-sized data blocks A-G. The byte stream 500

includes a plurality of individual interleaved bytes, as shown, and is representative of a typical byte stream received as an input to the CPU 400 and processed by the DMA engine 404. Such byte streams are normally interleaved on the transmitter side in order to provide features such as robustness and security and thus require de-interleaving at the receiver side.

In the example of FIG. 5, and for purposes of illustration only, the byte stream 500 has a de-interleave depth (D) of "4" and a block size value (N) of "5." The de-interleave depth (D) controls the amount of time each byte is delayed. The block size value (N) specifies the number of bytes in each codeword. Thus, in the example of the byte stream 500, each of the individual bytes is delayed by four time slots. In the present invention, the DMA engine 404 is configured to efficiently place the originally transmitted bytes of the data stream 500 back into their original order (1, 2, 3, 4, 5, 6...) instead of the interleaved order (0, -, -, -, 1, 5, etc.), illustrated in FIG. 5. FIG. 6 illustrates the first step in the process of re-ordering the bytes of the data stream 500, i.e., copying each of the codeword-size blocks A-G into the data buffer 408.

In FIG. 6 the input buffer 408,shown vertically arrayed, is partitioned into separate memory locations 600 – 608. Fort purposes of illustration, the memory locations 600-608 correspond to the exemplary data blocks A-E. In the example of FIG. 6, each of the memory locations 600-608 has a memory width (W) of four bytes. The DMA engine 404 must respectively copy the codeword-size data blocks A-E into the memory locations 600-608. In a first stage of de-interleaving the byte stream 500, the DMA engine 404 writes the first block A, is indexed 0, -, -, -, 1, into the memory location 600 in the manner illustrated in FIG. 6.

A common requirement on many different types of memories is that data must be written to the memory in integer multiples of the memory width (W). Although exceptions to this requirement are possible, the exceptions provide inefficient, overly complex schemes that sacrifice speed and power and erode other valuable system resources. Therefore, in the present invention, the DMA engine 404 will copy the five bytes of the data block A,

and all of the other five byte codeword-size blocks B-G, into the buffer 408 in multiples of four bytes at a time.

Since the data blocks A-E are five bytes in width, and thus not a multiple of the memory width (W) of four bytes, the data blocks A-G must be appended, or padded, with three dummy padding bytes 610-618 respectively. This padding artificially converts the length of each of the blocks A-E to eight bytes, a multiple of the memory width (W) four. With all of the exemplary data blocks A-E, including the appended padding bytes 610-618, now having been stored in the respective memory locations 600-608, the DMA engine 404 must now perform the de-interleaving.

FIG. 7 is an illustration of essential parameters used by the DMA engine 404 to de-interleave the now padded data blocks A-E, stored in the memory locations 600-608 of the buffer 408. The DMA parameters shown in FIG. 7 are typically stored in DMA registers or storage areas, such as the DMA memory storage area 406. As noted above with reference to FIGs. 5 and 6, the byte stream 500 and the DMA parameters of FIG. 7 are for the exemplary case where the interleave depth (D) is 4 and the byte size (N) is 5. traditional DMA engines use many other DMA parameters to perform de-interleaving. The present invention also uses some of these other DMA parameters. For purposes of clarity, however, the present application will not address these other parameters since their use remains unchanged in the present invention. Instead, the description of the present invention will focus on the DMA parameters shown in FIG. 7.

The STRIDE is the first of the DMA parameters listed in FIG. 7, and is has a value of 4. In the present invention, the STRIDE is the distance from one byte, that requires copying to memory, to the next byte requiring copying. STRIDE2, with a value of 4+3, is similar to the STRIDE, plus the number of padding bytes, such as the three bytes of padding 610 stored in the memory location 600. Thus, in the case of STRIDE 2, the DMA engine will skip over the padding bytes 610 in addition to the interleave depth. The number of padding bytes is referred to as the PADSIZE.

In the example of FIGs. 6 and 7, the STRIDE increments through all of the values of the block A (0,-,-,-, and1) to obtain the value "1." And the "3" in the STRIDE2 implies skipping over the "5" and the two dashes that follow the "5" of the block B, to get to the "2" value of the block B. Also included in the DMA parameters are the values of OFFSET, OFFSET INC, and OFFSET MOD, discussed in greater detail below.

The following is an exemplary approach to initializing the DMA parameters shown in FIG. 7 of the instant invention:

```
stride      = floor(D / N) * (N + PADSIZE) + (D mod N)
stride2     = stride + PADSIZE
offset      = 0
offsetInc   = D mod N
offsetMod   = N
```

where D is interleave depth
N is interleave length (i.e. including any pre-interleave padding)
PADSIZE is number of padding bytes per codeword (including any pre-interleave padding not transmitted which is negative)

The DMA computes each address to copy from as follows:

```
offset += offsetInc
if (offset >= offsetMod) then
        offset -= offsetMod
        address += stride2
else
        address += stride
```

FIG. 8 is an illustration of an exemplary DMA address sequence for determining the order in which the de-interleaved data bytes of the blocks A-E are read from the buffer 408. In FIG. 8, step 0 represents the reading of address A, which is the beginning of the buffer 408, where the bytes are numbered from left to right. Thus, the DMA engine 404 will first read the value "0" at address A. Address A corresponds to the first byte of the first row of the memory location 600 of the buffer 408. Next, in step 1, the DMA engine 404 will increment the address by the STRIDE value of "4." Thus, address A+4 of the buffer 408 will be read, which contains the value "1." The

address A+4 corresponds to the first byte of the second row of the memory location 600.

In step 2 of FIG. 8, the STRIDE2 of FIG. 7 will be used instead of the STRIDE, which represents an increment of 7. Thus, the DMA engine 404 will skip over 7 values to obtain the value of "2," shown in byte position four of the memory location 602. The DMA engine 404 will continue to read the remaining contents of the memory locations 602-608 to finally produce a de-interleaved byte stream sequenced as 0,1,2,3,4,5....

In any particular read cycle, the DMA engine 404 will use STRIDE or STRIDE2, but not both at the same time. Thus, the DMA engine 404 must know apriorily whether to use STRIDE or STRIDE2. The values of the OFFSET column of FIG. 8 determine whether the DMA engine 404 will use STRIDE or STRIDE2. The values of the OFFSET column operate based upon a modulo-n counting scheme. The modulo-n counting scheme controls the OFFSET, OFFSET INC, and OFFSET MOD (the modulo of how the offset of FIG. 8 is incremented) of the DMA parameters shown in FIG. 7.

The offset of FIG. 8 initially begins at 0, and for each step, is incremented by the OFFSET INC value. If the offset is initially 0, it will ordinarily be incremented by 4 each time. However, the offset counts by modulo. Therefore, in the example of FIGs. 5 –8, the only legal numerical values are 0-4, since the present example is based on modulo-5. The OFFSET MOD value corresponds to the byte size (N). Thus, in FIG. 8 at step 0, the offset is 0, and then the DMA engine 404 increments by 4. In step 1, the offset is 4. In step 2, the DMA engine 404 increments by 4 again, and so it would ordinarily be 8. The value, however, gets reduced because the counting is based on modulo-5, which in-turn, produces the offset value of 3. The remaining values of the offset column of FIG. 8 are determined in this manner and this process continues until the entire byte stream 500 is completely de-interleaved.

Thus, in accordance with the present invention, the DMA engine 404 uses two strides to facilitate an efficient implementation of a UMA memory technique. This technique ensures that codeword-size data blocks can be

written into memories in cases where the originally transmitted data blocks are not an integer multiple of the width (W) of the input buffer memory. In so doing, this process eliminates the need to perform alignment and partial word writes of the data blocks, which provides significant savings of system resources.

IV. Conditional One's-complement of Partial Address to Map Butterfly Address Generation to FFT/IFFT Post-/Preprocessing Pass Address Generation.

Processors, such as the control processor 205 of FIG. 2, support FFT/IFFT functions through use of standard radix-2 butterfly operations. These butterfly operations are specific implementations of an FFT algorithm in cases where the number of input samples is a power of 2. In order to implement these FFT/IFFT functions, the processor 205 includes address generation logic to access the input and output operand pairs (address pairs) of each butterfly.

One way of generating the butterfly input and output address pairs is to use a pointer and a fixed offset to access the operands at addresses 'pointer' and 'pointer+offset', incrementing the pointer through each recursion in the FFT/IFFT stage. A preferred approach would be to support optimized implementations of the FFT/IFFT for real-valued FFT inputs and IFFT outputs using standard post and pre-processing steps. Using standard post and pre-processing steps, however, the inputs to the butterfly operations of the post- and pre-processing steps are not separated by a fixed offset, and thus cannot use the normal operand addressing logic.

As a solution, the present invention uses an exemplary circuit implementation to conditionally invert the n-1 least-significant bits (LSBs) of the butterfly operand addresses provided for an N-point FFT/IFFT, where N = 2^n. The n-1 LSBs are inverted when the n'th operand address bit (address[n-1] where the LSB is address[0]) is 1, otherwise the LSBs are unchanged. This effectively reverses the last N/2 inputs to the real-valued FFT post-processing

pass or IFFT pre-processing pass, yielding un-unfixed offset between the inputs to the butterfly operations of the pass.

FIG. 9 is an illustration of a conventional 512 point FFT implementation 900. In FIG. 9, pairs of 512 real-valued inputs 902 are represented in the form of a 256 point (pre-processing) complex FFT 904. Using a traditional FFT approach, the 256 point complex FFT values are processed in the stage 904. Next, a conventional FFT post-processing stage 906 is implemented to produce 256 complex outputs 908. FIGs. 10 and 11 provide more detailed illustrations of the complex FFT operation 904 and the FFT post-processing stage 906.

In FIG. 10, a complex FFT operation, such as the pre-processing FFT operation 904, is implemented using a standard radix-2 butterfly 1000. A butterfly is a computational technique that takes a pair of real-valued FFT inputs and produces a pair of complex outputs. While the FFT operation 904 of FIG. 9 is a 256 point FFT, for purposes of simplification, the butterfly technique 1000 is demonstrated using an 8 point FFT.

In the illustration of FIG. 10, 8 complex value inputs 1002 (representative of 16 real-valued inputs) are provided as inputs to the butterfly 910. Outputs 1004 of the butterfly 1000 are represented as output addresses B0-B3. The output address B0 is associated with complex value inputs 0 and 4, which are provided as inputs to a first butterfly calculation (of the butterfly 1000). The output address B1 is associated with inputs 1 and 5, which were provided as inputs to a second butterfly calculation, the address B2 is associated with inputs 2 and 6, and so on, as illustrated in the step/address table 1006, also shown in FIG. 10. A point of interest with regard to the output addresses B0-B3, is that distances 1008-1012 (or offsets) between the addresses B0-B3 are fixed, with respect to each of the butterfly calculations of the butterfly 1000.

In FIG. 11, a standard post-processing operation, such as the post-processing operation 906, is implemented using a butterfly 1100. The butterfly 1100 receives inputs pairs 1102 and produces outputs 1104, shown as addresses C0-C2. In the post-processing butterfly 1100, however, offsets

1106-1110, associated with the inputs 1102, are not fixed. That is, the offsets 1106-1110 decrease in length for each of the butterfly calculations associated with the butterfly 1100. In an exemplary embodiment of the present invention, FFT pre-processing output addresses having fixed offsets, such as the exemplary addresses B0-B3, are transformed into FFT post-processing addresses having decreasing offsets, such as the exemplary addresses C0-C2.

FIG. 12 is a block diagram illustration of an exemplary circuit 1200 be configurable to transform the addresses output from an FFT pre-processing stage into addresses representative of an FFT post-processing stage. The circuit 1200 can be inserted into the logic path of a DSP controller, such as the controller 205 of FIG. 2, to perform this address transformation.

The circuit 1200 is coupled to an output of a conventional FFT address generator 1201. The address generator 1201 is included as part of an FFT intermediate processing FFT algorithm, such as the operation 904, and produces FFT complex values, such as those that would be provided to the post-processing operation 906. At a high level, the circuit 1200 is configured to perform a conditional one's complement of the address output from the address generator 1201.

The circuit 1200 includes a mask generator 1204 and a logic gate 1206 configured to perform a complementing operation. In the embodiment of FIG. 12, the logic gate is an exclusive OR gate, although other suitable logic circuits can be used. A value (n) specifies the number of address lines or bits output from the FFT address generator 1201. Another value (N) represents the size of the FFT operation to be performed, such as 256 point or 512 points, and is provided as an input to the mask generator 1204.

The mask generator 1204 allows the circuit 1200 to function with FFTs of different sizes. The mask generator 1204 also determines how many of the bits, output from the address generator 1201, should be complemented. A pre/post processing enabling signal 1208 is provided as input to the mask generator 1204. The signal 1208 enables the circuit 1200 when an FFT computation reaches the post-processing stage 906. The function of the circuit 1200 is explained in greater detail below, in relation to FIG. 13.

FIG. 13 is a detailed illustration of exemplary outputs 1300 of the FFT generator 1201. FIG. 13 also illustrates exemplary masks 1302. Each row of the masks 1302 is associated with a corresponding one of the rows of the outputs 1300, as indicated by the arrows. As noted above, the value (N) specifies the size of the FFT operation to be implemented. The example of FIG. 10, where (N) is 8, corresponds to the first two rows of the outputs 1300. An (N) value of 16 corresponds to the third and fourth rows of the addresses 1300 and masks 1302. In the example where (N) is 8, there is only one bit of the FFT generator 1201 that will control one of two output values of its corresponding mask within the mask values 1302.

When the signal 1208 indicates that the FFT post-processing is occurring, the mask generator 1204 is enabled. The output of the mask generator 1204 is then exclusively OR'd with the addresses having fixed offsets, output from the address generator 1201. The output of the circuit 1200 is a conditionally inverted address sequence having decreasing outputs, as discussed above. FIG. 14 is a more detailed illustration of the output of the circuit 1200.

In FIG. 14, steps 2-255 are shown, each corresponding to one of the addresses within an address sequence 1402. The address sequence 1402 is provided as an output from the address generator 1201 and includes fixed offsets (1/128, 2/129, 3/130, etc.). The circuit 1200, however, transforms the address sequence 1402, as described above, into the address sequence 1404 having decreasing offsets (1/255, 2/254, 3/254, etc).

The present invention, therefore, provides significant economies by enabling the calculation of the post-processing FFT address sequence directly from the output of the FFT address generator 1201. This calculation is achieved through the use of simple logic circuit that performs a one's complement of the fixed offset addresses and a mask of the address. Thus, the techniques of the present invention facilitate savings of significant hardware resources that would ordinarily be dedicated to performing FFT post processing address.

V. Definition and Implementation of SLICE Instructions on a Programmable SIMD Processor Data Path.

An important function in digital communication receivers is the 'slicing' of a received data symbol to determine the nearest point (or phase state) on a constellation grid. That is, the digital communication receivers must be able to closet grid point, from a standpoint of distance, that a particular received symbol value is associated with when it was transmitted. Put more simply, the receiver use slicing to determine precisely what was originally transmitted.

One commonly used approach to perform slicing in a DSP is through execution of a sequence of conventional instructions. The slicing function can also be implemented in dedicated logic, but this approach is inflexible and requires additional hardware resources. Dedicated logic, however, is unnecessary in systems where data paths of a SIMD based programmable DSP, such as the controller 205 of FIG. 2, can be modified to perform the slicing functions.

The instant invention provides an approach for slicing operations to be more efficiently and upported directly on a programmable DSP. This more efficient approach is facilitated through extensions to the instruction set, modifications to internal data paths, and use of control logic. The slicing operations are implemented using the data path logic that is provided for other basic operations.

DSPs typically provide functional units for multiplication, addition (accumulation) and result scaling. Many DSPs provide multiple sets of such units, controlled with a SIMD scheme to enhance performance. Slicing can be efficiently implemented using pairs of such units processing the in-phase and quadrature phase (I and Q) components of a received symbol. A more detailed discussion of preferred embodiments of the present invention is provided below in relation to a description of FIGs. 15-20.

FIG. 15 is a block diagram illustration of a conventional three stage DSP functional SIMD based data module 1500, having first and second

parallel paths 1502 and 1504. Since the first and second data paths 1502 and 1504 include identical functional modules, the discussion of the first parallel path 1502 will apply equally to the parallel path 1504. The conventional data module 1500 includes a first pipeline stage 1506 including a multiplier 1507, a second pipeline stage 1508 including an adder 1509, and a third stage 1510 including a scalar 1511. Also included are registers 1512 for holding addresses or instructions used for manipulation of data passed through each of the stages of the data module 1500.

In the conventional functional data module 1500 illustrated in FIG. 15, input operands OP1n and OP2n are received, from general registers, as inputs to the stage 1506 of the first path 1502 during a current timing cycle. The input operand OP1n might, for example, be representative of the "I" component of a received data point in the exemplary form of a 16 bit data word. The operand OP2n is traditionally representative of a scaling factor. The operands OP1n and OP2n are multiplied together in the multiplier 1507.

Next, the product of the multiplier 1507 is provided to the input of the adder 1509 in accordance with, for example, instructions stored in one of the registers 1512. In the module 1500, the second data path 1504 is configured to receive symbol data associated with the symbol's "Q" component, as discussed above. Further, while the first stage 1506 process the input from the current timing cycle, the stage 1508 is simultaneously processing an input from a previous timing cycle and the stage 1510 is simultaneously processing an input from an even earlier timing cycle.

A rounding value, provided as an input to a mutiplexer 1514, is added to the first product of the multiplier 1507 during the noted timing cycle. For subsequent products output from the multiplier 1507, the multiplexer 1514 selects its lower path such that the products are added with previous sums. A rounding value is provided so that when scaling is performed in the third stage 1510, the scaling will be performed on a sum having a fixed number of data bits.

Next, the result from the adder 1509 is scaled in the third stage 1510 by a scalar 1511. The scalar 1511 multiplies the result, output from the adder

1509, times 2^(-k), where (k) is specified by the DSP instructions. The output of the scalar 1511, labeled as RSLTn, is then provided as an overall output of the data module 1500. As previously noted, FIG. 15 is an illustration of a conventional SIMD processor data path. FIG. 16, however, is an illustration of modifications, in accordance with the present invention, to the conventional data path of FIG. 15. This modification enables the data path to more efficiently support symbol slicing instructions.

In general terms, FIG. 16 provides a block diagram illustration of an exemplary data path module 1600 capable of performing symbol slicing instructions as part of its instruction set, i.e., performing the slice instruction as a primitive instruction. An advantage of the approach of the present invention is a reduction in the number of input cycles required to execute slice instructions. In a conventional DSP, slice instructions can require 20 or more cycles for execution. In the exemplary embodiment of FIG. 16, however, slice instructions can be executed within about two cycles.

More specifically, FIG. 16 includes a data path module 1600 including conventional components, such as the multiplier 1507, the adder 1509, and the scalar 1511, shown in FIG. 15. The module 1600, however, also includes an additional operand path 1602 and an additional multiplexer 1604.

A constants generator 1606 is provided to scale the bit stream associated with OP1 (the I or Q component) into a format that has its binary point in a fixed position. The scaling directly supports the slicing function and scales each of the I and Q components to a fixed format by multiplying OP1 by 2^(k-b), where k is a constant chosen based on the data path precision and b, an instruction parameter or operand, indicates the number of fractional bits in, for example, the 16 bit data stream of the I or Q component.

When control logic of the DSP detects that the data module 1600 is executing a slicing instruction instead of standard DSP instructions, the multiplexer 1604 selects its operand path 1602 (lower path). When the path 1602 is selected, OP1 is received and is multiplied by the expression 2^(k-b) and is thus scaled into the fixed binary point format. The use of a fixed format simplifies subsequent processing.

Next, OP1n and the fixed format value (output from the constants generator 1606) are multiplied together in the multiplier 1507. The product of the multiplier 1507 is provided as an input to another multiplexer 1608. Also provided as an input to the multiplexer, are boundary constraints 1610 which are output from a slice decoder 1700, illustrated in FIG. 17. The slice decoder 1700 and the boundary constraints 1610 are discussed in greater detail below and in relation to FIG. 17.

FIG. 17 is an illustration of an exemplary slice decoder 1700. The slice decoder 1700 is conventional logic that is configured to receive the sign bits of the I and I components associated with the received symbol data. The decoder 1700 also receives data representative of the particular constellation grid associated with the transmitted symbol data. The output of the decoder 1700 is a set of I and Q limit values 1610 (boundary constraints) and a set of I and Q load enable conditions 1702. The limit values 1610 and the enable conditions 1702 are a function of the location of the received symbol on a particular constellation grid, such as the grid shown in FIG. 18.

FIG. 18 is a graph of a conventional 4 x 4 constellation grid 1800. Constellation grids are representative of accepted communications standards and include two-dimensional displays of the baseband I and Q values of transmitted and received data symbols, as measured at a particular point in time. A vector from the center of the diagram to a specific constellation point is representative of the amplitude of the symbol. When symbol data is originally transmitted, its I and Q components have specific coordinates within a constellation grid. Due to noise, transmission error, and other factors, the symbol's receive constellation grid values often differ from its transmission constellation grid values. As noted above, the present invention is an efficient technique to determine the original transmitted constellation grid values of the originally transmitted data symbol.

Although the constellation grid of FIG. 18 is a 4 x 4 representation, the present invention can operate with constellation grids of other sizes, such as 2 x 2, 8 x 8, or diagrams that are not square. In FIG. 18, the points "A" an "B" are representative of the I and Q components of bits that combine to form a

transmitted data symbol. When the points "A" and "B" were originally transmitted, they were associated with specific coordinates, or points, on the grid 1800. During transmission, however, the points moved off of their original grid coordinates as shown.

Therefore, the DSP, using instructions within the data module 1600, must slice the received symbol data to determine which of the coordinates on the grid that the points "A" and "B" were originally transmitted on. With reference to FIG. 17, the limit values 1610 are representative of the limits of the I and Q axis of the grid. In the exemplary grid 1800, the limits of the I axis are +3 and –3, and the limits of the Q axis are also +3 and –3. These limits define a ring of grid points. The I and Q conditions 1702, on the other hand, are associated with whether the "A" and "B" points are actually within the ring of points.

Referring back to FIG. 16, the product of the multiplier 1507 is representative of an actual I or Q component of one of the A and B points. This product is received as an input to the multiplexer 1608. The multiplexer 1608 then alternately provides the product of the multiplier 1507 and the I and Q limit values 1610 to the adder 1509, which in the present invention, is used as a comparator. The output of the adder 1509 is used to determine whether the points A and B are within the ring of I and Q points (finite grid) or outside the ring of points (infinite grid). As seen in FIG. 18, A is within the ring of points and B is outside.

The output of the adder 1509 is provided as an input to a quantizer circuit 1612. The quantizer circuit 1612 essentially forces the points A and B to the nearest point on the infinite grid. Subsequent cycles use the adders to implement boundary clamping via per-quadrant min/max operations that conditionally load the result registers (accumulators) based on comparisons performed by the adders (with possible auxillary comparisons). The constants can be read from a table indexed by an instruction operand or directly specified by the operand. Additional details of the circuit 1612 are provided in the discussion concerning FIG. 19.

In FIG. 19, the quantizer circuit 1612 includes an OR gate 1900 and an AND gate 1902 coupled to the OR gate 1900. A quantize signal is provided by the DSP control logic as a control signal to activate the quantizer 1612. At a more detailed level, the quantizer masks the k LSBs of the symbol data prior to storage in a results register 1614 (accumulator) to implement the quantization of each component when enabled. Also added to the results register 1614 are the I and Q conditions (load enable) 1702 from the slice decoder 1702 shown in FIG. 17. The quantized components are compared against constants determined by the constellation size and sign of the component in the accumulator register 1614. In other words, the accumulator results register 1614 compares the results of the quantizer with the actual I and Q input data symbol conditions.

The quantizer 1612 essentially forces the LSBs of the receive symbol data, to zero. The k-1 bits go through the AND gate 1902 and the next bits are received by the OR gate 1900. The most significant bits, which are left over, simply pass through the quantizer 1612 and remain unchanged. When the quantizer 1612 is in use, the adder 1509 can be used to implement symmetric rounding (about the point origin) and/or offset adjustment for constellations that aren't centered about the point origin.

Finally, an output from the results register 1614 is provided to the scalar 1511. The results scalar 1511 is used to divide each component by 2^(k-b) to return the components to the input format. The output of the scalar 1511 is a determination of the nearest grid points to the points A and B, within the constellation grid 1800. An exemplary slicing sequence implemented by the data module 1600 will be described in relation to a description of FIG. 20.

FIG. 20 is an exemplary table 2000 representative of two input cycles of the data module 1600. In FIG. 20, data points A and B are shown along a vertical column to the left. A "cycle" column shows two input cycles of the data path module 1600 for receiving input symbol data related to data points A and B. In cycle 1, the table 2000 shows that a quantize enable signal is "set" to activate the quantizer 1612. Since the quantize signal is present, the

limits and conditions, included in the table 2000, are not used. Thus, the module 1600 will select the nearest grid point in infinite grid.

The grid 1800 illustrates that the nearest grid point in infinite grid of the I and Q coordinates, for point A, are –1 and –1. In cycle 2, the quantization has already been accomplished so the quantization signal is not set. Thus, the next comparison of the input symbol data is against the limits. Here, the I limit is –3 and a condition of "less than." The conditions of "less than" or "greater than" are a function of the quadrant that the point appeared in.

Similarly, for Q, the limit is –3, with a condition of "less than." Since in this case, the nearest point on infinite grid was within the actual 4 x 4 grid, the second cycle did not make any changes. Therefore, the result of the symbol slicing in this case was –1 and –1 for both the I and Q components, which correspond with a point on the grid 1800. The results for the point B, however, are slightly different.

The table 2000 illustrates that for the cycle 1, the quantize control signal is set. Therefore, the first step will be to quantize the symbol data associated with B onto the infinite grid. In this case, the output coordinates for I and Q are 1 and –5 respectively. The first arrow pointing away from point B on the grid 1800, points to the coordinates 1 and –5 for I and Q respectively. During cycle 2, the point B is compared against the limit of the finite grid. This comparison illustrates that the data point B is outside of this limit. Here, therefore, the result of cycle 2 is 1 and –3 for the I and Q limits, respectively. Thus, both points A and point B have now been associated with their nearest points in infinite grid, and consequently, associated with their original constellation grid coordinates.

The present invention, therefore, provides an approach for slicing operations to be more efficiently supported directly on a programmable DSP. The approach of the invention is facilitated through extensions to the instruction set, modifications to internal data paths, and use of control logic. The slicing operations are implemented using the data path logic that is provided for other basic operations. This approach facilitates performing the

slice instruction as a primitive instruction. An advantage of the approach of the present invention is a reduction in the input cycles required to execute a slice instruction. The present invention reduces the required cycles from 20 to 2 or 3 cycles.

VI. Program Synchronization of A Processor and DMA Using Ownership Flags.

A processor DSP is often paired with a DMA engine and two working memories so that processor execution on data in one memory can overlap DMA transfers to and from the other memory. Higher performance processors require more bandwidth than can be provided by a single working memory; additional bandwidth can be supplied by additional working memories. A synchronization mechanism is required to ensure than a given working memory is only in use by either the processor or the DMA at any given time, and to provide flow control of data passed between the processor and DMA engine.

FIG. 21 is a block diagram illustration of an exemplary processor/DMA memory sharing scheme 2100. In FIG. 21, the memory sharing scheme 2100 includes another exemplary DMA engine 2102, a processor 2104, memories A-D, and associated ownership flags 2106.

FIG. 22 is an illustration of exemplary DMA program instructions 2200 and processor program instructions 2202, used in connection with the DMA engine 2102, the processor 2104, and the memories A-D.

Finally, FIG. 23 is an illustration of management and execution of the DMA program instruction 2200 and the processor program instructions 2202 based upon specific settings of the ownership flags 2106.

Systems with two or more working memories, such as the memories A-D, typically have the DMA engine 2102 and processor 2102 wait for each other upon completion of the tasks 2200 and 2202, shown in FIG. 22. When both the DMA engine 2102 and the processor 2104 have finished, the roles of the memories A-D are swapped and the DMA engine 2102 and the processor

2104 continue with the next set of tasks. This process is repeated for each set of tasks.

The ownership flags 2106 are provided to indicate, for each of the memories A-D, whether its use is controlled by the DMA engine 2102 or processor 2104. Specific instruction sets are provided for both the DMA engine 2102 and the processor 2104 for testing and setting the flags 2106. One instruction, from within the instruction set 2102, waits for the specified set of ownership flags to indicate ownership by the DMA engine 2102 or the processor 2104 executing the instruction. The other instruction sets the specified set of ownership flags 2106 to indicate ownership by the DMA engine 2102 or the processor 2104 not executing the instruction.

The memory sharing scheme 2100, along with software convention, allows programs running on the DMA engine 2102 and the processor 2104. The scheme 2100 avoids simultaneous use of the exemplary working memories A-D by transferring ownership of the memories, when finished with the memory, and waiting for ownership before accessing the memory. Similarly flow control is implemented by waiting for ownership of the memory containing the data being transferred before operating on it.

The present invention has been described above with the aid of functional building blocks illustrating the performance of specified functions and relationships thereof. The boundaries of these functional building blocks have been arbitrarily defined herein for the convenience of the description. Alternate boundaries can be defined so long as the specified functions and relationships thereof are appropriately performed.

Any such alternate boundaries are thus within the scope and spirit of the claimed invention. One skilled in the art will recognize that these functional building blocks can be implemented by analog and/or digital circuits, discrete components, application specific integrated circuits, firmware, processors executing appropriate software and the like or any combination thereof. Thus, the breadth and scope of the present invention should not be limited by any of the above-described exemplary embodiments,

but should be defined only in accordance with the following claims and their equivalents.

WHAT IS CLAIMED IS:

1. A modem, comprising:

one or more processing paths; and

a number of interconnected modules sequentially arrayed along the one or more of the processing paths, each module being configured to (i) process signals passed along the paths in accordance with the sequence and (ii) implement unique functions to perform the processing;

wherein each of the modules has a particular degree of functional programmability; and

wherein the degrees of functional programmability monotonically vary in accordance with the sequence.

2. The modem of claim 1, wherein the modem is an asymmetric digital subscriber logic (ADSL) modem.

3. The modem of claim 2, wherein the one or more processing paths include a receive path and a transmit path.

4. The modem of claim 3, wherein the interconnected modules includes at least one of an analog front end, a discrete multi-tone module/frequency domain equalizer and a direct memory access engine.

5. The modem of claim 1, wherein the predetermined functions include at least one of resampling, echo cancellation, fourier processing, and error correcting.

6. The modem of claim 5, wherein the functional programmability includes non-programmable hardware, programmable hardware, firmware, and software.

7. The modem of claim 5, wherein the variations are representative of monotonic increases.

8. A modem comprising:

a receiver associated with a receive timing scheme;

a transmitter associated with a transmit timing scheme; and

only one timing mechanism (i) electrically coupled to the receiver and the transmitter and (ii) configured to synchronize the receive and transmit timing schemes.

9. The modem of claim 9, wherein the receiver includes a receive re-sampler and the transmitter includes an transmit re-sampler.

10. The modem of claim 9, wherein the modem is an asymmetric digital subscriber line (ADSL) modem.

11. The modem of claim 10, wherein the timing mechanism includes a phase accumulator.

12. The modem of claim 10, wherein the timing mechanism includes a coefficient generator and a phase accumulator.

13. A modem comprising:

a receive re-sampler configured to receive input signals in accordance with a receive timing scheme;

a transmit re-sampler connected, at least indirectly, to the receive re-sampler, the transmit re-sampler being configured to transmit output signals in accordance with a transmit timing scheme; and

only one timing mechanism electrically coupled to the receive re-sampler and the transmit re-sampler;

wherein the timing mechanism is configured to synchronize the receive timing scheme and the transmit timing scheme.

14. The modem of claim 13, wherein the modem is an asymmetric digital subscriber line (ADSL) modem.

15. The modem of claim 14, wherein the receive input signals includes digitized input signals.

16. The modem of claim 15, wherein the receive re-sampler produces interpolated signals based upon the received input signals and first timing coefficients.

17. The modem of claim 16, wherein the transmitted output signals include digitized output signals.

18. The modem of claim 16, wherein the transmitted output signals include second timing coefficients.

19. The modem of claim 18, wherein the first and second timing coefficients are produced based upon linear interpolation, the linear interpolation being a function of phase increment and phase accumulator.

20. The modem of claim 19, wherein the timing mechanism includes a phase accumulator.

21. The modem of claim 19, wherein the timing mechanism includes a phase accumulator and a coefficient generator.

22. The modem of claim 16, further comprising a timing tracking mechanism configured to receive the interpolated signal and produce timing data therefrom.

23. The modem of claim 22, wherein the phase accumulator is configured to (i) receive the timing data and (ii) update the first and second timing coefficients based upon the received timing data.

24. A method for synchronizing timing in a modem having a receiver configured to receive an input data signal and a transmitter configured to produce an output data signal, the output data signal having timing characteristics based upon a transmit coefficient signal, the method comprising:

receiving (i) the input data signal and (ii) a receive coefficient signal in the receiver;

re-sampling the input data signal based upon the received coefficient signal to produce an interpolated signal thereby;

producing signal phase data based upon the interpolated signal; and

updating the receive coefficient signal and the transmit coefficient signal based upon the signal phase data.

25. The method of claim 24, wherein the signal phase data includes a phase increment, a phase tweak, and a coefficient factor.

26. The method of claim 24, wherein the updating includes adjusting a phase of the receive coefficient signal and transmit coefficient signal.

27. A method for de-interleaving a data stream stored in a buffer having a plurality of memory locations, each location having a memory width of (W) bytes, the data stream being formed of a number of data words each including (N) number of data bytes, wherein (N) is a non-integer multiple of the width (W), the method comprising:

storing the data words into respective memory locations;

appending each of the stored data words with number (X) of dummy bytes, a sum of (N) + (X) being an integer multiple of the width (W); and

storing the appended dummy bytes into the respective memory locations.

28. The method of claim 27, wherein the data words include codeword-size data blocks.

29. The method of claim 28, wherein the interleaved data stream includes an interleave depth (D); and

wherein the method is implemented based upon operation of a direct memory access (DMA) engine.

30. The method of claim 29, further comprising de-interleaving the data bytes stored in the respective memory locations based upon operation of the DMA engine and a number of parameters;

wherein the parameters include first and second memory strides, an offset increment value, and an offset modulo value.

31. A method for storing a data stream in a modem buffer having a plurality of memory locations, each location having a memory width of (W) bytes, the data stream being formed of a number of data words each including (N) number of data bytes, wherein (N) is a non-integer multiple of the width (W), the method comprising:

(a) copying the (N) data bytes of a first data word into a first [(n)(W)] bytes of a first location, where (n) is an integer that (i) equals one when $W > N$ and (ii) is a smallest among all integers satisfying the expression $[(n)(W) > N]$ when $W < N$;

(b) appending the first number (N) of copied bytes with (X) number of dummy bytes, a sum of (X) + (N) being an integer multiple of the width W; and

(c) copying the appended dummy bytes (X) into the first (n)(W) bytes of the first location.

32. The method of claim 31, wherein the copied first number (N) of data bytes and the copied (X) dummy bytes correspond to the first data word.

33. The method of claim 31, further comprising copying the (N) data bytes a remaining number of the data words into the remaining memory locations in accordance with (a) through (c).

34. The method of claim 33, wherein the interleaved data stream includes an interleave depth (D) and the method includes a memory access technique having at least first and second memory strides.

35. The method of claim 34, further comprising de-interleaving the data bytes in the memory based upon operation of the DMA engine, the DMA engine ignoring the dummy bytes (X).

36. The method of claim 35, wherein the de-interleaving is based upon operation of the DMA engine and at least the first and second strides.

37. The method of claim 36, wherein the de-interleaving occurs based upon the operation of the DMA engine, values of the first and second strides, an offset increment value, and an offset modulo value.

38. The method of claim 37, wherein a value of the first stride is equal to the interleave depth, and a value of the second stride is equal to the interleave depth plus (X).

39. The method of claim 38, wherein the second stride is used instead of the first stride; and

wherein the second stride is used based a modulo of the offset increment value.

40. An apparatus for de-interleaving a data stream stored in a buffer having a plurality of memory locations, each location having a memory width of (W) bytes, the data stream being formed of a number of data words each including (N) number of data bytes, wherein (N) is a non-integer multiple of the width (W), the apparatus comprising:

means for storing the data words into respective memory locations;

means for appending each of the stored data words with number (X) of dummy bytes, a sum of (N) + (X) being an integer multiple of the width (W); and

means for storing the appended dummy bytes into the respective memory locations.

41. The apparatus of claim 40, wherein the data words include codeword-size data blocks.

42. The apparatus of claim 41, wherein the interleaved data stream includes an interleave depth (D); and

wherein the apparatus is implemented based upon operation of a direct memory access (DMA) engine.

43. The apparatus of claim 42, further means for comprising de-interleaving the data bytes stored in the respective memory locations based upon operation of the DMA engine and a number of parameters;

wherein the parameters include first and second memory strides, an offset increment value, and an offset modulo value.

44. A circuit, comprising:

a fast fourier transform (FFT) address generator configured to produce a complex FFT address sequence, the complex FFT address sequence having fixed offsets; and

a conversion mechanism configured to (i) receive the complex FFT address sequence and (ii) convert the received sequence into an address sequence having varying offsets.

45. The circuit of claim 44, wherein the circuit is included in a modem.

46. The circuit of claim 45, wherein the modem is an asymmetric digital subscriber line (ADSL) modem.

47. The circuit of claim 44, wherein the conversion mechanism is an FFT post-processing module.

48. The circuit of claim 44, wherein the varying offsets vary in a decreasing direction.

49. The circuit of claim 44, wherein the conversion mechanism performs the converting in lieu of FFT-post-processing.

50. The circuit of claim 44, wherein the conversion mechanism includes:

a logic gate having first and second input ports and an output port, the first input port being coupled to an address generator output port, the output port being configured to output the address sequence having the varying offsets; and

a mask generator having a third input port and an output port, the third input port being coupled to the address generator output port, and the mask generator output port being coupled to the second input.

51. The circuit claim 50, wherein the logic gate is an exclusive OR gate.

52. A method for determining a fast fourier transform (FFT) post processing address sequence of an N-point FFT in a digital signal processor, the method comprising:

producing a complex FFT address sequence in response to N received complex FFT input samples, the complex FFT address sequence being representative of N/2 output address pairs having fixed offsets, the sequence including a bit stream having (n) data bits representative of a memory address of the output pairs, (N) being equal to 2^(n);

selecting particular ones of the data bits for complementing; and

performing an arithmetic operation between the selected particular ones of the bits and the complex FFT address sequence, the complement operation producing output address pairs having un-fixed offsets.

53. The method of claim 52, wherein the particular ones of the data bits include an (n-1) least significant bit (LSB).

54. The method of claim 53, wherein an LSB address[0] is 1.

55. The method of claim 52, wherein selecting is implemented based upon a masking operation.

56. The method of claim 52, wherein the arithmetic operation is a one's complement operation.

57. An apparatus for determining a fast fourier transform (FFT) post processing address sequence of an N-point FFT in a digital signal processor, the apparatus comprising:

means for producing a complex FFT address sequence in response to N received complex FFT input samples, the complex FFT address sequence being representative of (N/2) output address pairs having fixed offsets, the sequence including a bit stream having (n) data bits representative of a memory address of the output pairs, (N) being equal to 2^n;

means for selecting particular ones of the data bits for complementing; and

means for performing a arithmetic operation between the selected particular ones of the bits and the complex FFT address sequence, the complement operation producing output address pairs having un-fixed offsets.

58. The apparatus of claim 57, wherein the particular ones of the data bits include an (n-1) least significant bit (LSB).

59. The apparatus of claim 57, wherein an LSB address[0] is 1.

60. The apparatus of claim 57, wherein the selecting is implemented based upon a masking operation.

61. The apparatus of claim 57, wherein the arithmetic operation is a one's complement operation.

62. A method for implementing a SLICE operation in a programmable digital signal processor (DSP) as a primitive instruction in one or more data paths of at least one of (i) a single instruction single data scheme and (ii) a single instruction multiple data scheme.

63. The method of claim 62, wherein the SLICE instruction is executed in three or less input cycles.

64. The method of claim 62, wherein the SLICE operation includes an input symbol slicing stage and a quantization stage.

65. The method of claim 64, wherein the input symbol slicing stage occurs during a first input cycle and the quantization stage occurs during a second input cycle.

66. The method of claim 65, wherein the SLICE operation is configured to associate input symbol data with a particular point of a constellation grid, the constellation grid being stored in a memory of the DSP

67. A computer readable medium carrying one or more sequences of one or more instructions for execution by one or more processors to perform a method for implementing a SLICE operation in a programmable digital signal processor (DSP) as a primitive instruction in one or more data paths of a single instruction multiple data scheme.

68. A digital signal processor (DSP) including a number of single instruction multiple data (SIMD) path logic units, each logic unit including (i) a multiplier having two or more input ports, one of the input ports being configured to receive input symbol data, the multiplier being configured to produce a multiplier output, (ii) an adder configured to receive the output product and produce an adder output therefrom, and (iii) a scalar configured to scale the adder output, the DSP comprising:

a constants generator coupled to another one of the number of multiplier input ports and being configured to produce a fixed format signal based upon the input symbol data, the multiplier output being representative of a product of the received input symbol data and the fixed format signal;

wherein the adder is configured to (i) receive boundary constraints representative of a first component of predetermined symbol standards and (ii) compare the multiplier output with the boundary constraints, the adder output being representative of the comparison; and

a quantizer configured to (i) receive the adder output and (ii) associate the received adder output with a second component of the predetermined symbol standard, the quantizer producing a quantized output.

69. The DSP of claim 68, wherein the DSP includes a number of data paths, each of the logic units being respectively arrayed along one of the paths.

70. The DSP of claim 68, wherein the constants generator produces the fixed format signal in accordance with the expression 2^(k-b), where (k) is a predetermined constant, and where (b) is indicative of fractional bits associated with the symbol data.

71. The DSP of claim 70, wherein the symbol standards are associated with a constellation grid; and

wherein the constellation grid is formed of an infinite grid and a finite grid.

72. The DSP of claim 71, wherein the first component is the finite grid.

73. The DSP of claim 72, wherein the bit stream includes least significant bits (LSBs) and the quantizer sets the LSBs to zero.

74. The DSP of claim 73, wherein the quantizer includes a logic array.

75. The DSP of claim 13, wherein the quantizer includes a first logic gate having first and second input ports and a first output port, one of the first and second input ports being configured to receive the output sum and the other of the first and second input ports being configured to receive a control logic signal; and

a second logic gate having third and fourth input ports and a second output port, one of the third and fourth input ports being coupled to the first input port and the other of the third and fourth input ports being coupled to the second input port, the second output port being coupled to the first output port.

76. The DSP of claim 75, wherein the first logic gate is an OR gate; and

wherein the second logic gate is an AND gate.

77. The DSP of claim 76, wherein the second component is a nearest point within the infinite grid.

78. The DPS of claim 77, further comprising an accumulator configured to (i) receive condition data representative of a location of the input symbol data and (ii) update the quantized output based upon the received condition data.

79. A method of slicing a receive data symbol in a digital signal processor including a number of single instruction multiple data path logic units, each logic unit including (i) a multiplier having two or more input ports, one of the input ports being configured to receive input symbol data, the multiplier being configured to produce a multiplier output, and (ii) an adder configured to receive the output product and produce an adder output therefrom, the method comprising:

producing a fixed format signal based upon the input symbol data, the fixed format signal being multiplied by the input symbol data to produce the multiplier output;

comparing the boundary constraints with the multiplier output, a result of the comparing being representative of the adder output; and

associating with a second component of the predetermined symbol standard.

80. The method of claim 79, wherein the fixed signal format is produced in accordance with the expression 2^(k-b), where (k) is a predetermined constant, and where (b) is indicative of fractional bits associated with the symbol data.

81. The method of claim 79, wherein the fixed format signal is formed of a bit stream having a fixed binary point.

82. The method of claim 79, wherein the input signal includes a phase component and a magnitude component.

83. The method of claim 79, wherein the symbol standards are associated with a constellation grid.

84. The method of claim 83, wherein the constellation grid is formed of an infinite grid and a finite grid.

85. The method of claim 84, wherein the first component is the finite grid.

86. A method for sharing one or more memories between one or more processors, each memory being associated with a respective ownership flag, the method comprising:

associating each of the processors with a particular value of the flag; and

assigning use of the memories to a corresponding one of the processors when the respective ownership flag is set to the particular value.

87. The method of claim 86, wherein each of the processors is associated with a different particular value.

88. The method of claim 87, wherein the particular values are changeable in association with selected processor cycles.

89. The method of claim 88, wherein the use of a particular memory includes ownership of the memory during the during the selected processor cycle.

90. The method of claim 89, wherein each memory is assigned to only one processor during any one of the processor cycles.

91. An apparatus for sharing one or more memories between one or more processors, each memory being associated with a respective ownership flag, the apparatus comprising:

means for associating each of the processors with a particular value of the flag; and

means for assigning use of the memories to a corresponding one of the processors when the respective ownership flag is set to the particular value.

92. The apparatus of 91, wherein each of the processors is associated with a different particular value.

93. The apparatus of claim 92, wherein the particular values are changeable in association with selected processor cycles.

94. The apparatus of claim 93, wherein the use of a particular memory includes ownership of the memory during the during the selected processor cycle.

95. The apparatus of claim 94, wherein each memory is assigned to only one processor during any one of the processor cycles.

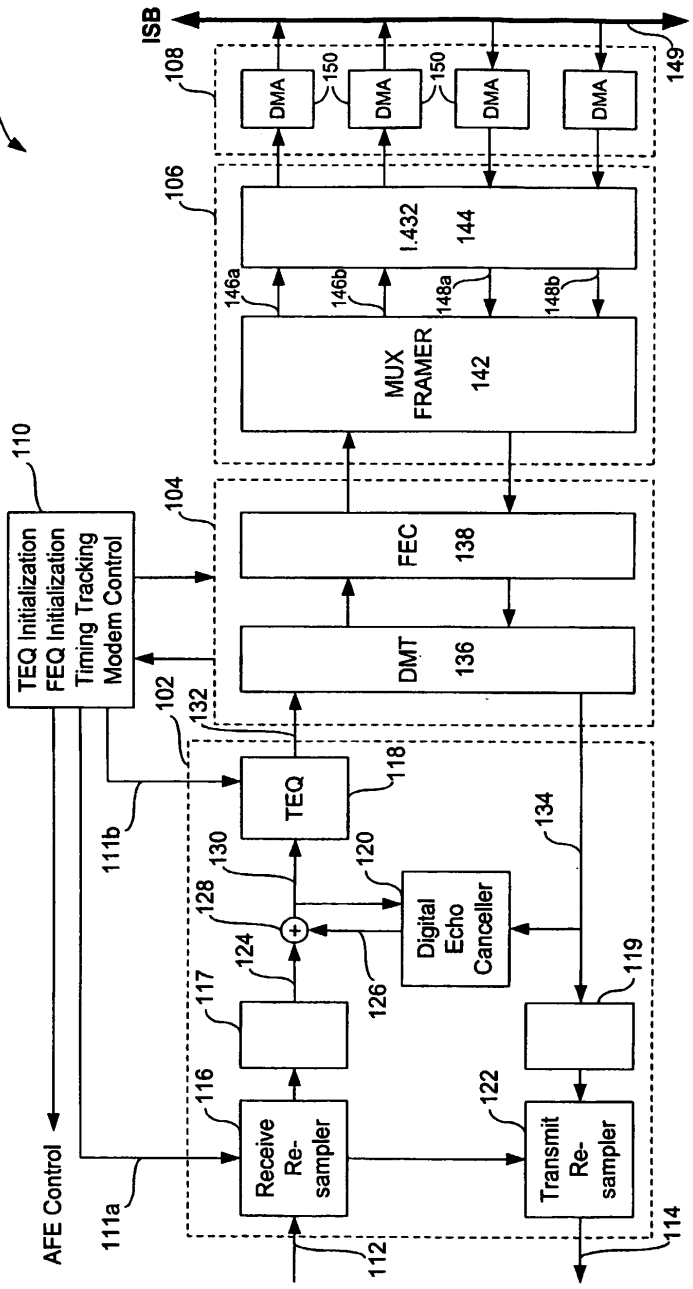

100
ISB
108
DMA
150
149
106
I.432
144
146a
146b
148a
148b
MUX FRAMER
142
110
104
FEC
138
DMT
136
TEQ Initialization
FEQ Initialization
Timing Tracking
Modem Control
102
132
TEQ
118
111b
130
120
134
128
Digital Echo Canceller
124
126
117
119
116
122
Receive Re-sampler
Transmit Re-sampler
AFE Control
111a
112
114

FIG. 1

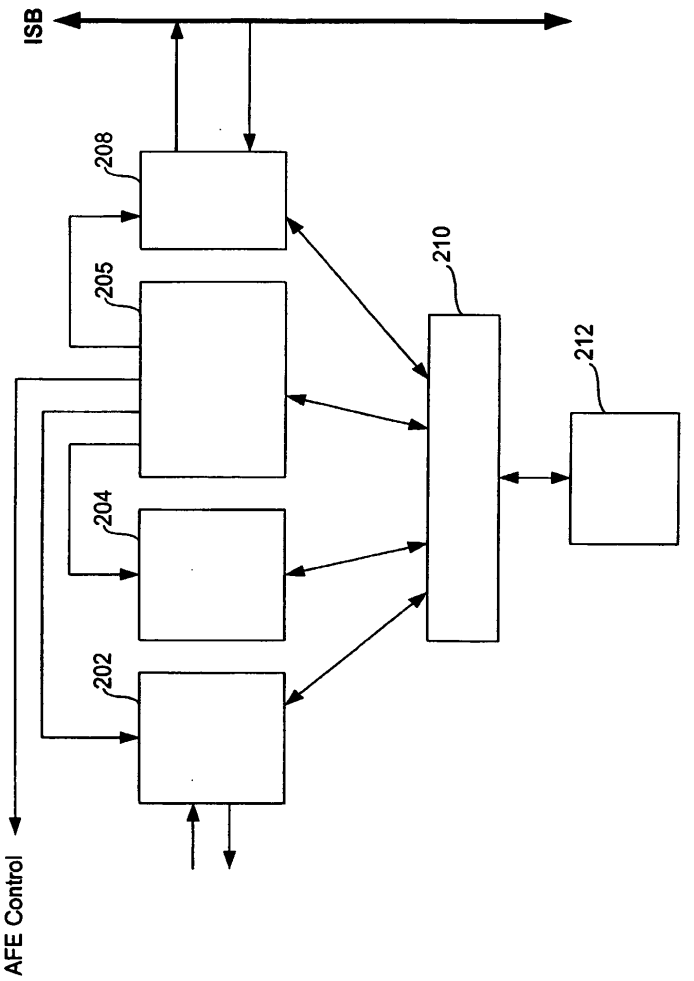
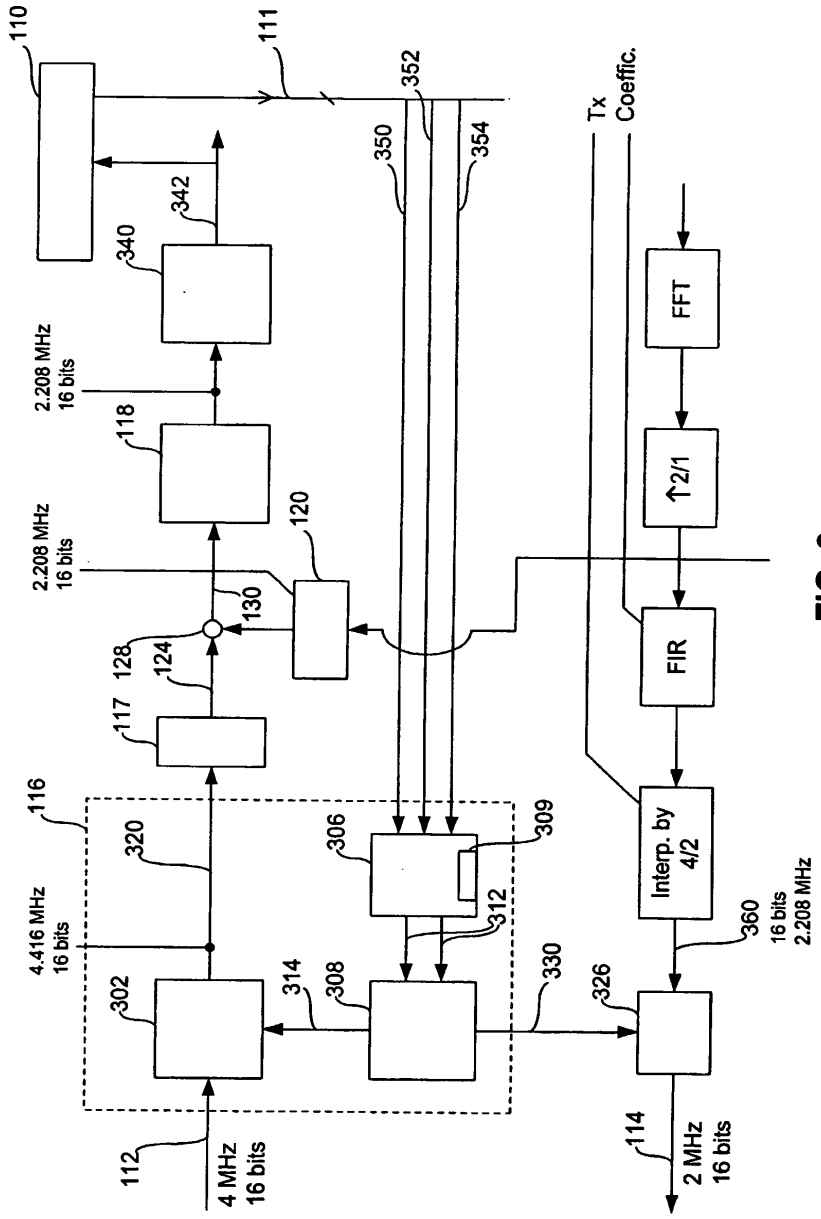


FIG. 2


110
111
352
350
354
342
340
2.208 MHz
16 bits
118
120
2.208 MHz
16 bits
130
128
124
117
116
320
306
309
312
4.416 MHz
16 bits
302
314
308
330
326
112
4 MHz
16 bits
114
2 MHz
16 bits
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Coeffic.
FFT
↑2/1
FIR
Interp. by
4/2
360
16 bits
2.208 MHz

FIG. 3

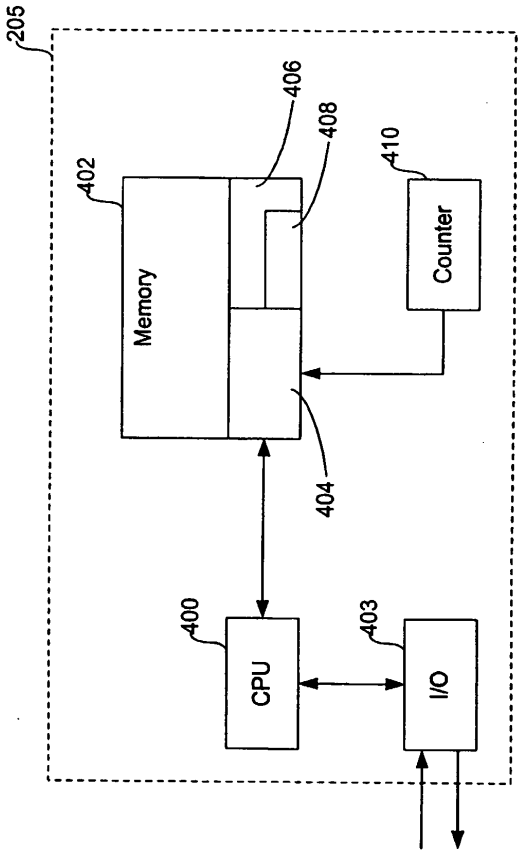

FIG. 4

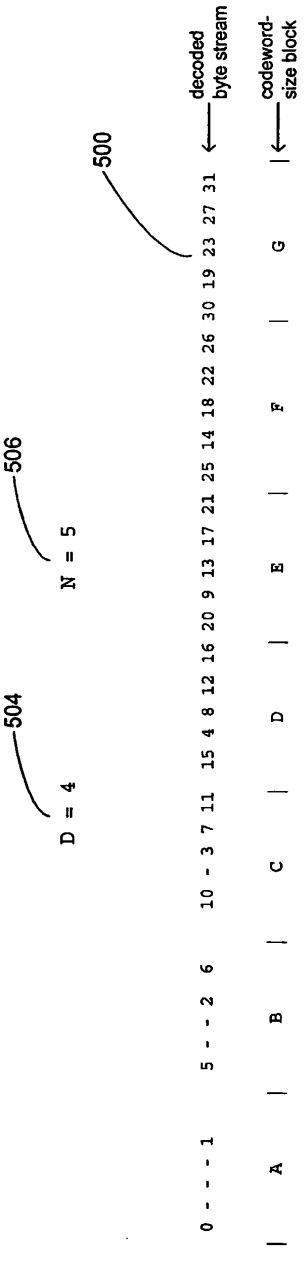
500
decoded byte stream
codeword-size block
0 - - - - 1 5 - - 2 6 10 - 3 7 11 15 4 8 12 16 20 9 13 17 21 25 14 18 22 26 30 19 23 27 31
| A | B | C | D | E | F | G |
504
D = 4
506
N = 5

FIG. 5

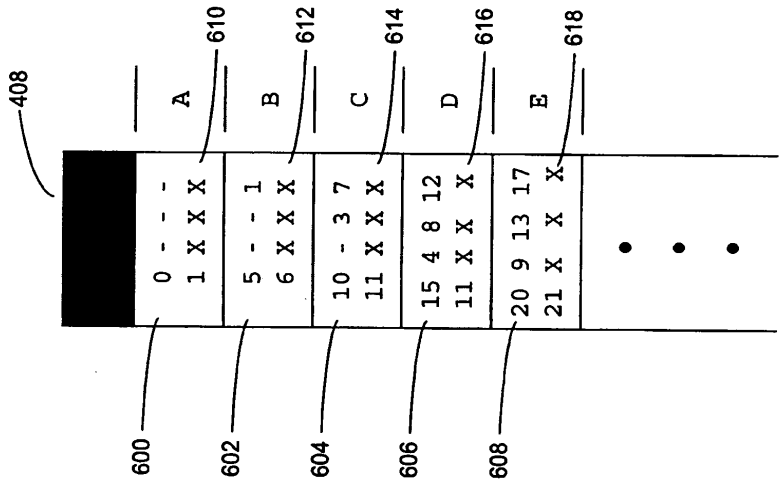
408
A
B
C
D
E
610
612
614
616
618
0 - - -
1 X X X
5 - - 1
6 X X X
10 - 3 7
11 X X X
15 4 8 12
11 X X X
20 9 13 17
21 X X X
600
602
604
606
608

FIG. 6

```
DMA Parameters:  Stride     = 4
                 Stride2    = 4 + 3 = 7
                 Offset     = 0
                 Offset INC = 4
                 Offset Mod = 5
```

FIG. 7

DMA Address Sequence:

Step	Offset	Address
0	0	A
1	4	A+4
2	3	A+11
3	2	A+18
4	1	A+25

FIG. 8

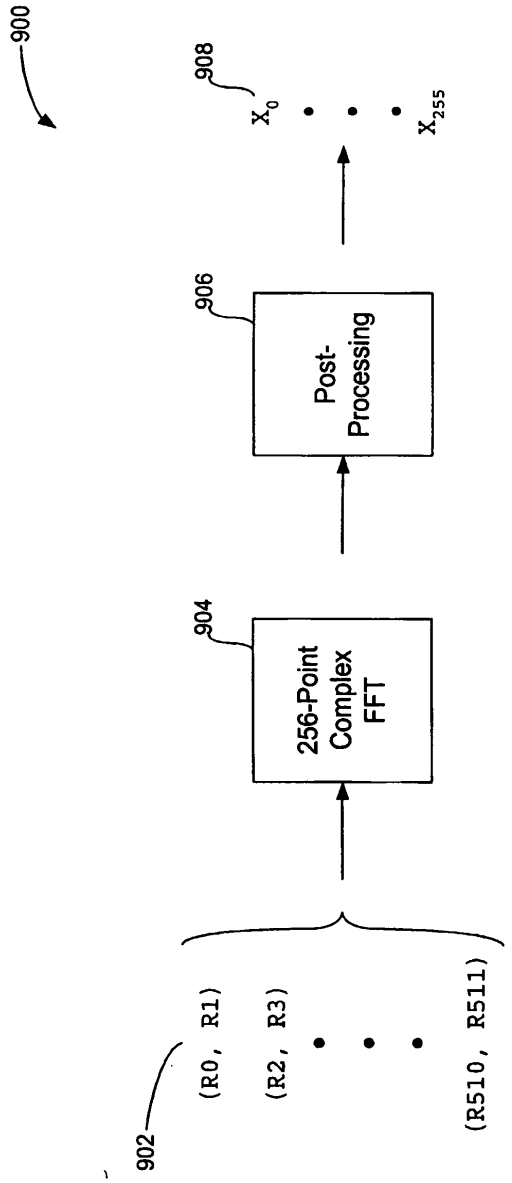

FIG. 9
(conventional)

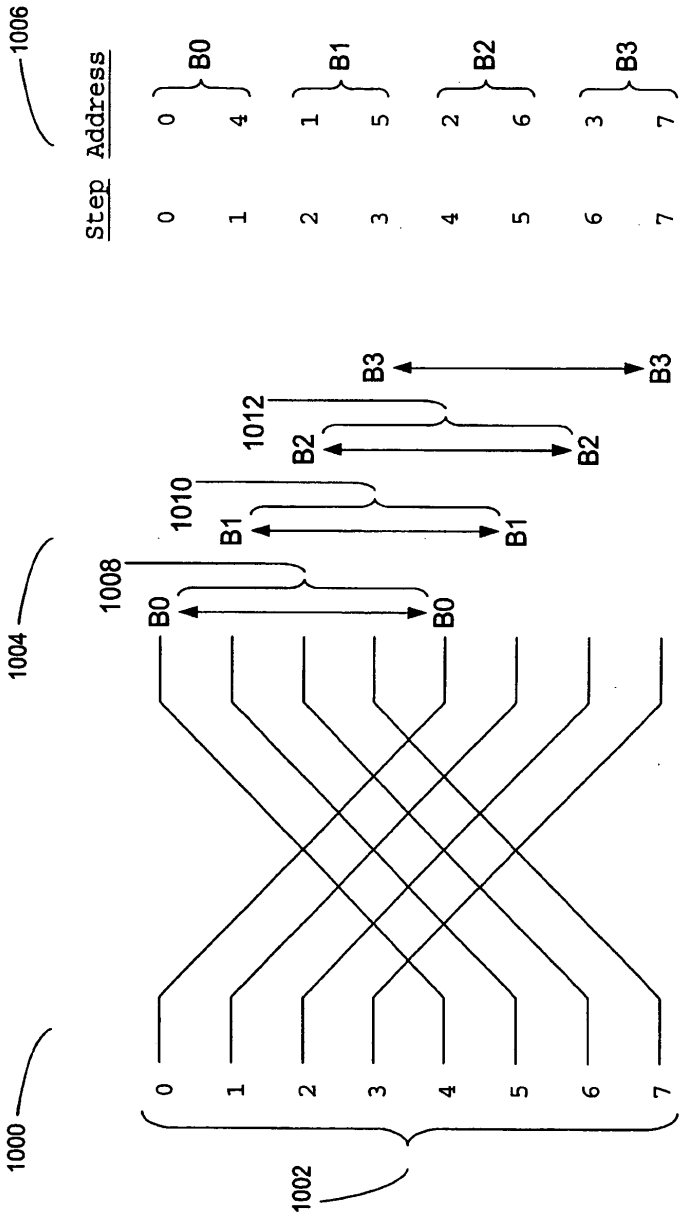

FIG. 10
(conventional)

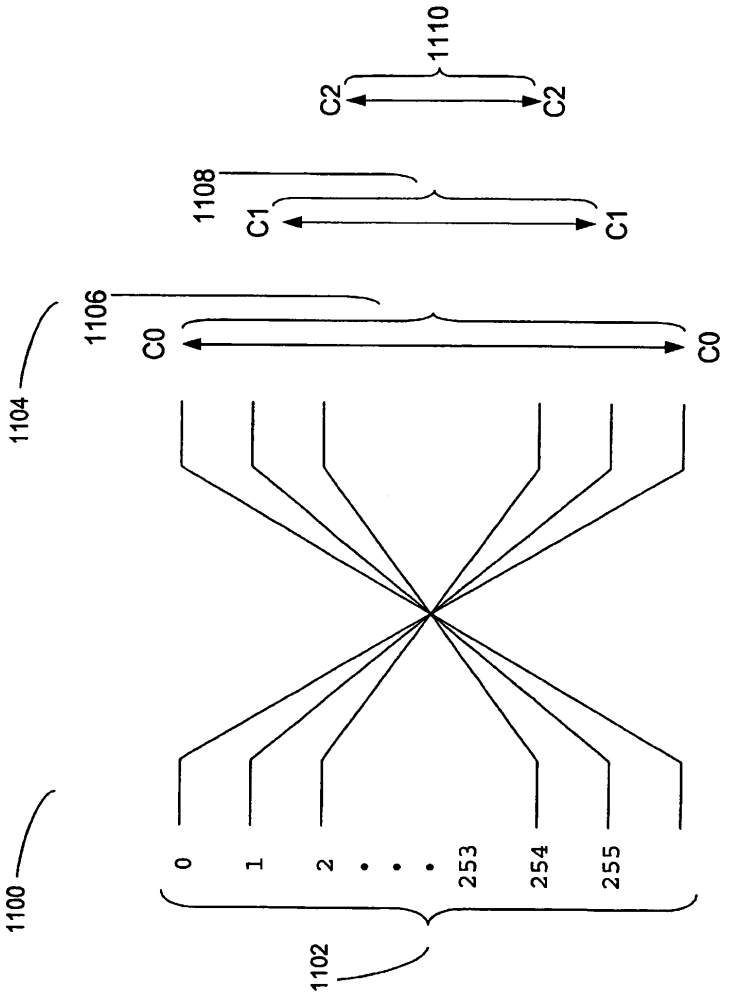

FIG. 11
(conventional)

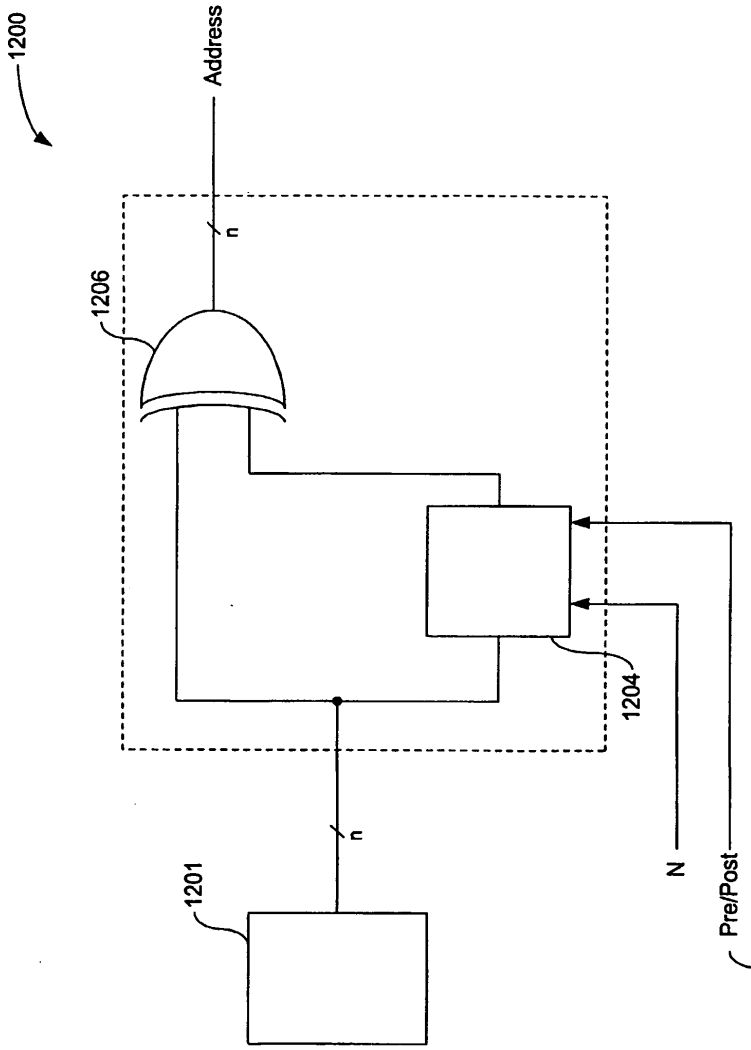

FIG. 12

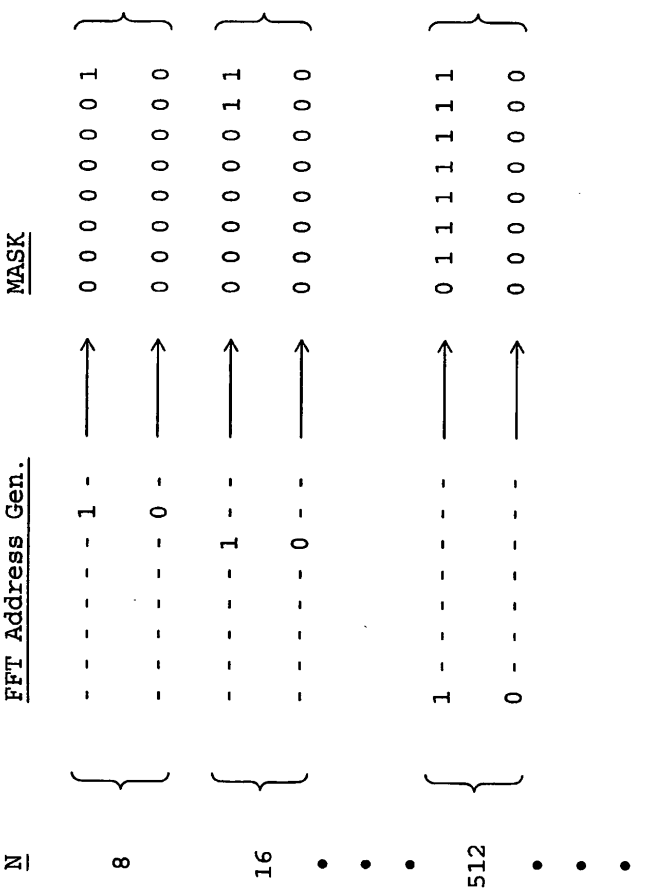
1300
1302
FFT Address Gen.
MASK
N
8
16
512
- - - - - - 1 -
- - - - - - 0 -
- - - - 1 - -
- - - - 0 - -
1 - - - - - - -
0 - - - - - - -
0 0 0 0 0 0 0 1
0 0 0 0 0 0 0 0
0 0 0 0 0 0 1 1
0 0 0 0 0 0 0 0
0 1 1 1 1 1 1 1
0 0 0 0 0 0 0 0

FIG. 13

STEP	FFT Address Gen. 1402	Conditionally Inverted Address 1404
2	1	1
3	128	255
4	2	2
5	127	254
6	3	3
7	130	253
•		
•		
•		
254	127	127
255	254	129

FIG. 14

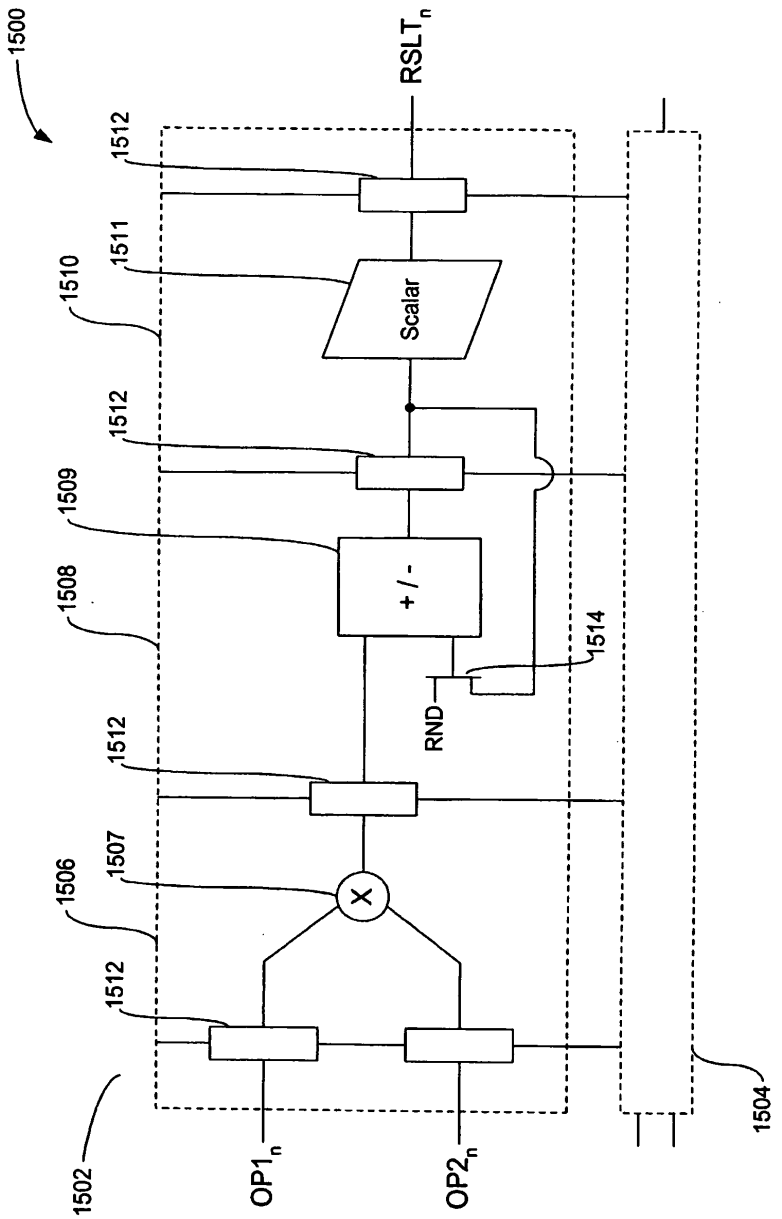

FIG. 15
(conventional)

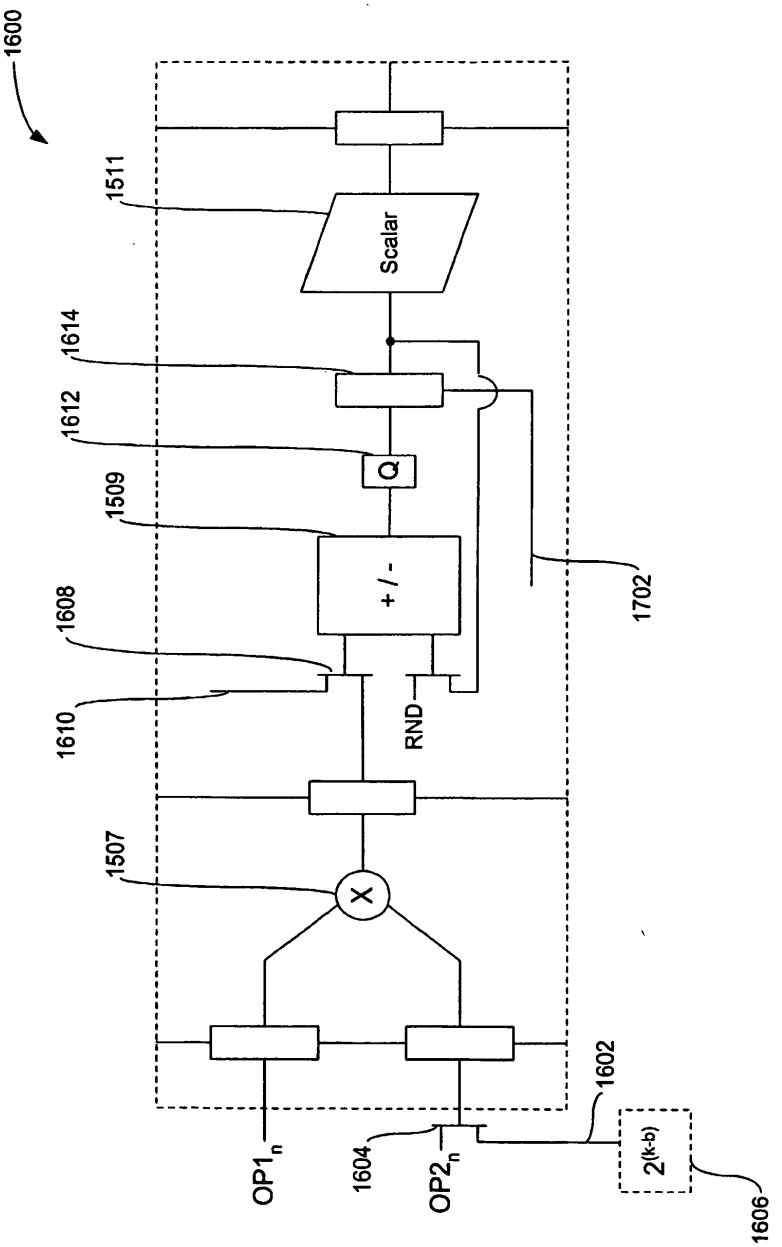
1600
1511
Scalar
1614
1612
Q
1509
+ / -
1608
1610
RND
1702
1507
X
1602
$OP1_n$
1604
$OP2_n$
$2^{(k-b)}$
1606

FIG. 16

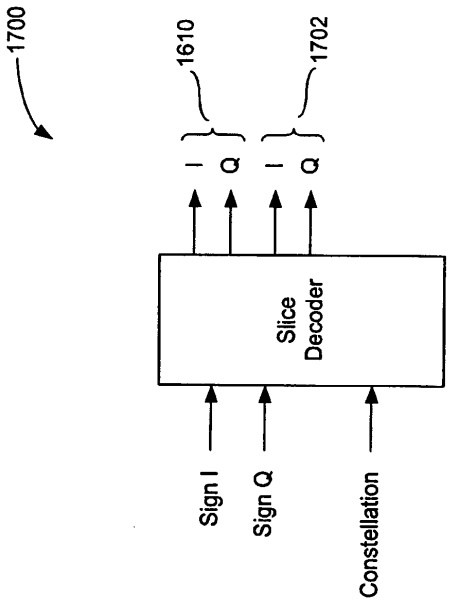
1700
1610
1702
I
Q
I
Q
Slice Decoder
Sign I
Sign Q
Constellation

FIG. 17

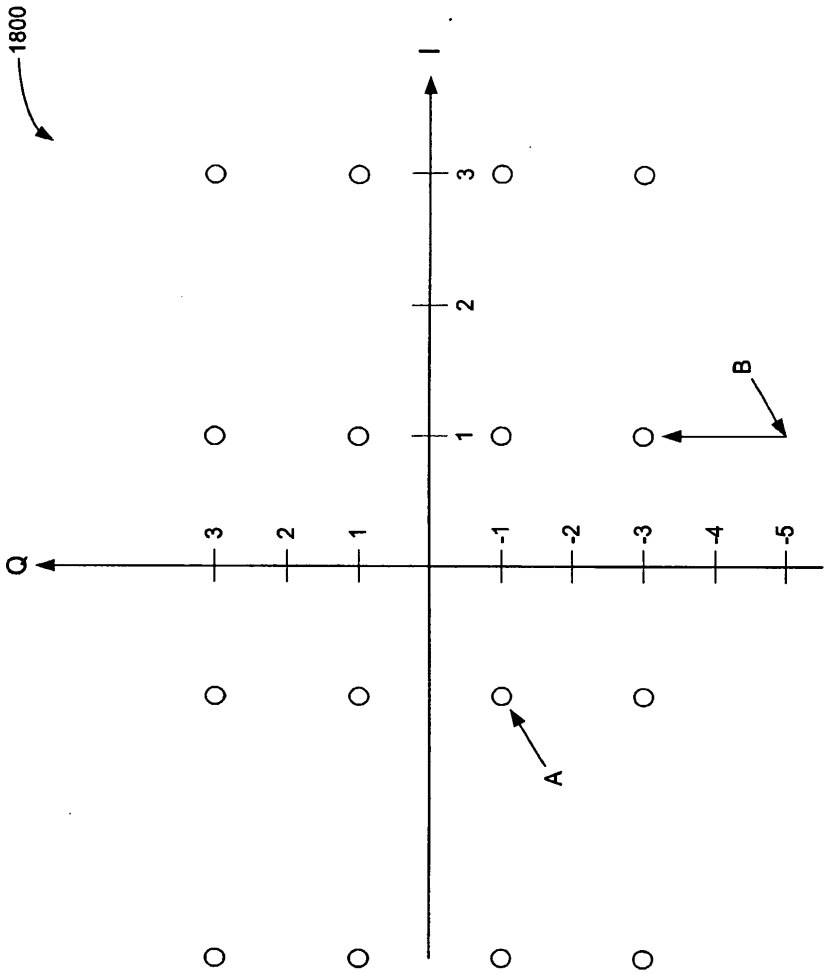

FIG. 18

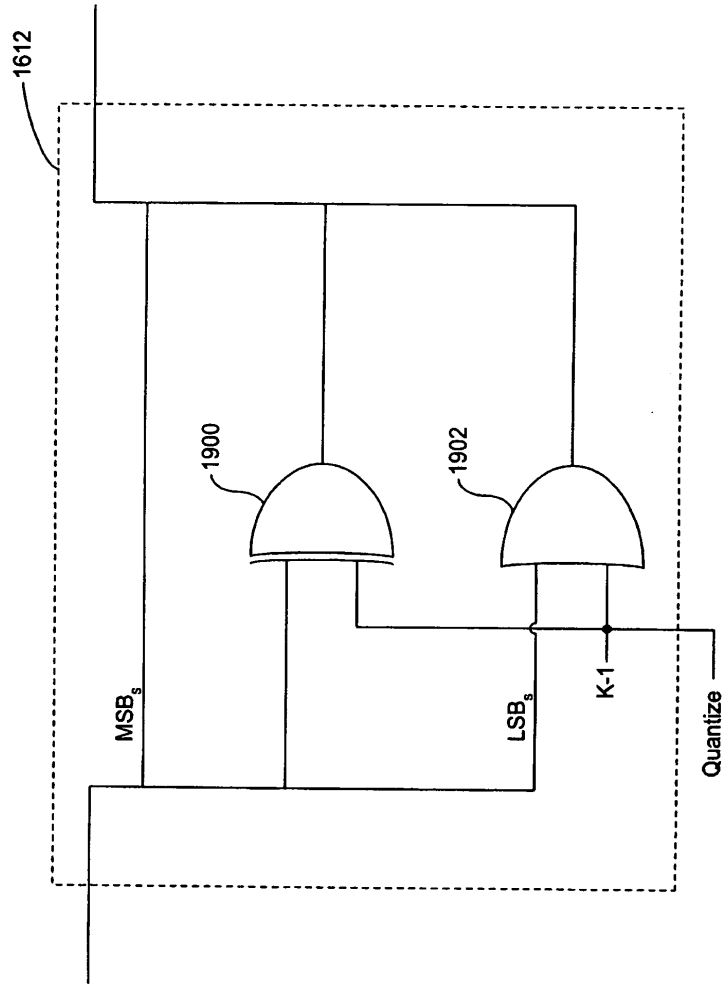

FIG. 19

	Cycle	Quantize	I Limit	I Condition	Q Limit	Q Condition	Acc I	Acc Q
'A'	1	Yes	-	-	-	-	-1	-1
	2	No	-3	<	-3	<	-1	-1
'B'	1	Yes	-	-	-	-	-1	-5
	2	No	3	≥	-3	<	-1	-3

FIG. 20

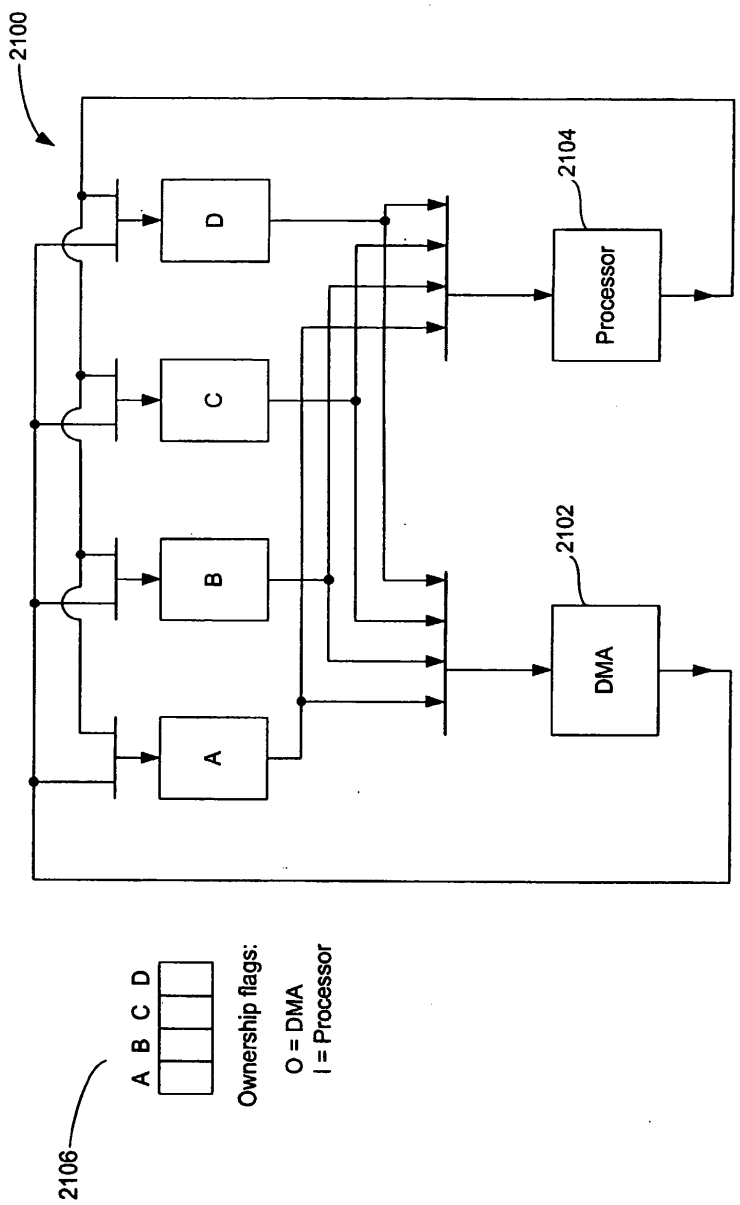
2100
D
C
B
A
2104
Processor
2102
DMA
A B C D
Ownership flags:
O = DMA
I = Processor
2106

FIG. 21

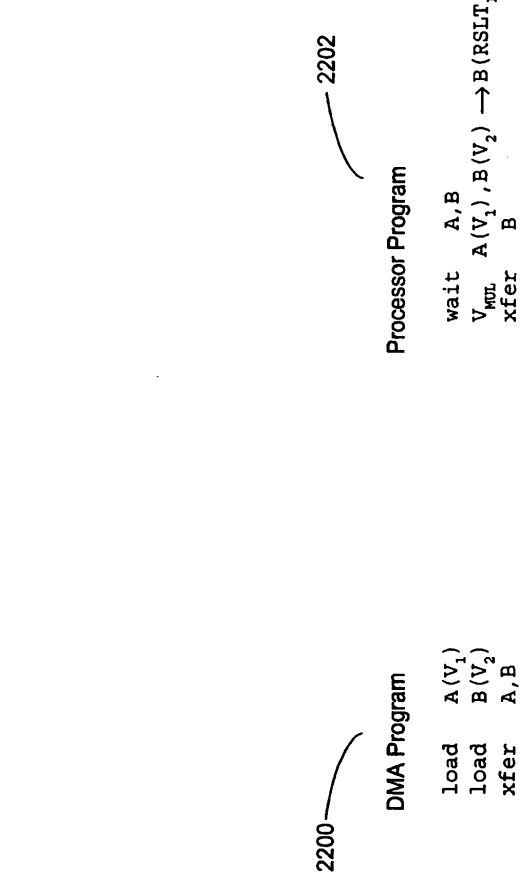
2200
DMA Program
load A(V1)
load B(V2)
xfer A,B
load C(V3)
xfer C,D
wait B
store B(RSLT1)
wait D
store D(RSLT2)
2202
Processor Program
wait A,B
VMUL A(V1),B(V2) →B(RSLT1)
xfer B
wait C,D
fft C(V3) D(RSLT2)
xfer D

FIG. 22

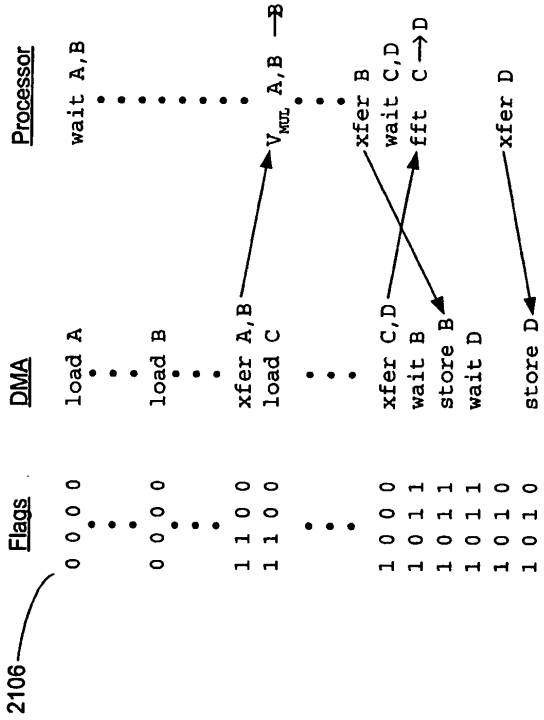
2106
Flags
DMA
Processor
0 0 0 0
load A
wait A,B
0 0 0 0
load B
1 1 0 0
xfer A,B
load C
V_{MUL} A,B → B
xfer B
1 0 0 0
xfer C,D
wait C,D
1 0 1 1
wait B
fft C → D
1 0 1 1
store B
1 0 1 1
wait D
1 0 1 0
xfer D
1 0 1 0
store D

FIG. 23

(12) INTERNATIONAL APPLICATION PUBLISHED UNDER THE PATENT COOPERATION TREATY (PCT)

(19) World Intellectual Property Organization
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(30) Priority Data:
60/350,253 24 January 2002 (24.01.2002) US

(71) Applicant: **BROADCOM CORPORATION** [US/US]; 16215 Alton Parkway, Irvine, CA 92618 (US).

(72) Inventors: **EFLAND, Gregory, H.**; 2225 Ramona Street, Palo Alto, CA 94301 (US). **LIANG, Haixiang**; 1403 Pitman Avenue, Palo Alto, CA 94310 (US). **PETERSON, kevin, H.**; 725 Leona Lane, Mountain View, CA 94040 (US). **CHEN, Yuanjie**; 5215 Nice Court, San Jose, CA 95138 (US). **CORRY, Alan, G.**; 900 Pepper Tree Lane, # 621, Santa Clara, CA 95051 (US). **FERRARIO, Nino, P.**; 718 Old San Francisco Road, Apartment # 329, Sunnyvale, CA 94086 (US). **GUAN, Jeff, Z.**; 908 Bentley Oaks Court, San Ramon, CA 94583 (US). **PRAHLAD, Meera**; 19523 Dorchester Drive, Saratoga, CA 95070 (US). **STOMAKHIN, Ilya**; 10330 Imperial Avenue, Cupertino, CA 95014 (US). **WAN, Yongbing**; 4231 Ruby Avenue, San Jose, CA 95135 (US). **YAMANO, Larry, C.**; 838 Gary Avenue, Sunnyvale, CA 94086 (US). **YIN, Lin**; 41741 Vaquero Court, Fremont, CA 94539 (US). **YU, Gong-San**; 325 Tramway Drive, Milpitas, CA 95035 (US). **PAPANICOLAOU, George, A.**; 342 Lawson Road, Scarborough, Ontario M1C 2J9 (CA).

(74) Agents: **SOKOHL, Robert** et al.; Sterne, Kessler, Goldstein & Fox P.L.L.C., Suite 600, 1100 New York Avenue, N.W., Washington, D.C. 20005-3934 (US).

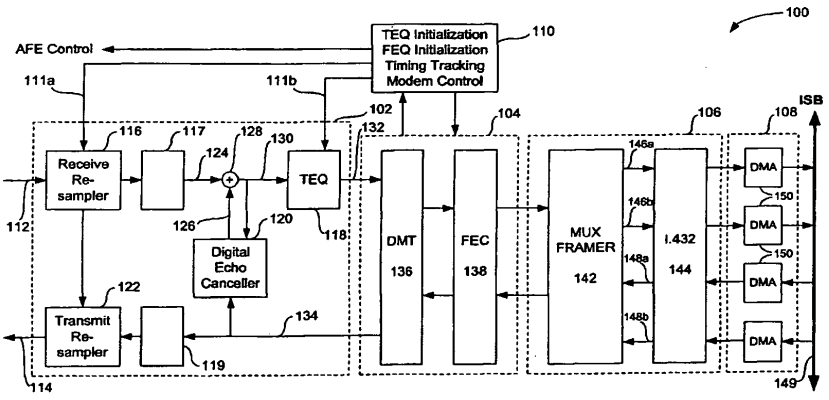
(84) Designated States *(regional)*: European patent (AT, BE, BG, CH, CY, CZ, DE, DK, EE, ES, FI, FR, GB, GR, HU, IE, IT, LU, MC, NL, PT, SE, SI, SK, TR).

Published:
— *with international search report*
— *before the expiration of the time limit for amending the claims and to be republished in the event of receipt of amendments*

(88) Date of publication of the international search report:
16 October 2003

For two-letter codes and other abbreviations, refer to the "Guidance Notes on Codes and Abbreviations" appearing at the beginning of each regular issue of the PCT Gazette.

(54) Title: ASYMMETRIC DIGITAL SUBSCRIBER LINE MODEM APPARATUS AND METHODS THEREFOR



(57) Abstract: Provided is a system and method for a modem (100) including one or more processing paths. Also included is a number of interconnected modules (102) (104) (106) (108) sequentially arrayed along the one or more paths. Each module is configured to (i) process signals passed along the paths in accordance with the sequence and (ii) implement predetermined functions to perform the processing. Further, each of the modules has a particular degree of functional programmability and the degrees of functional programmability monotonically vary in accordance with the sequence.

WO 03/063060 A3

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INTERNATIONAL SEARCH REPORT

International application No.
PCT/US03/02154

A. CLASSIFICATION OF SUBJECT MATTER
IPC(7) : H04L 5/16
US CL : 375/219,220,222,232,260,262,265,356;370/210,286,289,290,464,480,503,525;711/127;708/313,400,404
According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
U.S. : 375/219,220,222,232,260,262,265,356;370/210,286,289,290,464,480,503,525;711/127;708/313,400, 404

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)
EAST Database

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category *	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
Y	US 5,909,463 A (JOHNSON ET AL.) 01 June 1999, see the entire patent.	1-26
Y	US 5,742,527 A (RYBICKI ET AL.) 21 April 1998, see the entire patent.	1-26
Y	US 5,309,484 A (MCLANE ET AL.) 03 May 1994, see the entire patent.	1-26
Y	US 4,074,086 A (FALCONER ET AL.) 14 February 1978, see the entire patent.	1-26
Y	US 6,219,816 B1 (TEZUKA) 17 April 2001, see the entire patent..	27-42
Y	US 6,202,178 B1 (SPRUYT) 13 March 2001, see the entire patent.	27-42
Y	US 6,035,313 A (MARCHANT) 07 March 2000, see the entire patent.	44-61
Y	US 5,491,652 A (LUO ET AL.) 13 February 1996, see the entire patent.	44-61
Y	US 4,982,428 A (AGAZZI ET AL.) 01 January 1991, see the entire patent.	62-85

☒ Further documents are listed in the continuation of Box C. ☐ See patent family annex.

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"O" document referring to an oral disclosure, use, exhibition or other means

"P" document published prior to the international filing date but later than the priority date claimed

"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention

"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone

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"&" document member of the same patent family

Date of the actual completion of the international search	Date of mailing of the international search report
13 June 2003 (13.06.2003)	19 AUG 2003
Name and mailing address of the ISA/US Mail Stop PCT, Attn: ISA/US Commissioner for Patents P.O. Box 1450 Alexandria, Virginia 22313-1450 Facsimile No. (703)305-3230	Authorized officer Chi Pham Telephone No. 703-305-3800

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INTERNATIONAL SEARCH REPORT

PCT/US03/02154

C. (Continuation) DOCUMENTS CONSIDERED TO BE RELEVANT

Category *	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
Y	US 5,671,250 A (BREMER ET AL.) 23 September 1997, see the entire patent.	62-85
Y	US 5,872,993 A (BROWN) 16 February 1999, see the entire patent.	86-95
Y	US 6,256,723 B1 (HUDSON ET AL.) 3 July 2001, see the entire patent.	86-95

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60/618,269 12 October 2004 (12.10.2004) US

(71) Applicant *(for all designated States except US)*: **AWARE, INC.** [US/US]; 40 Middlesex Turnpike, Bedford, MA 01730-1432 (US).

(72) Inventors: **TZANNES, Marcos, C.**; 121 La Espiral, Orinda, CA 94563 (US). **LUND, Michael**; 110 Prospect St., West Newton, MA 02465 (US).

(74) Agent: **VICK, Jason, H.**; Miles & Stockbridge P.C., 1751 Pinnacle Dr., Suite 500, McLean, VA 22102 (US).

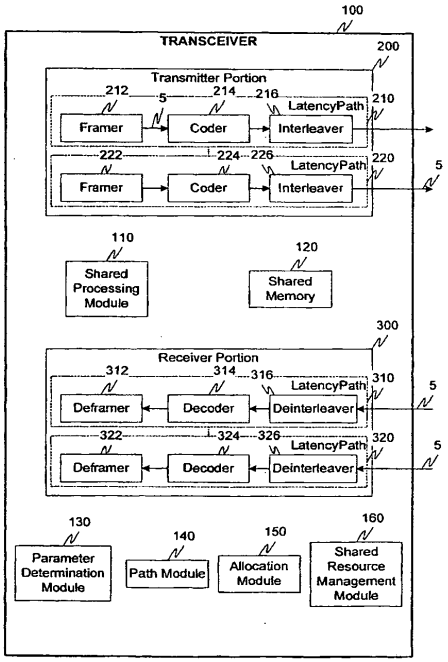
(81) Designated States *(unless otherwise indicated, for every kind of national protection available)*: AE, AG, AL, AM, AT, AU, AZ, BA, BB, BG, BR, BW, BY, BZ, CA, CH, CN, CO, CR, CU, CZ, DE, DK, DM, DZ, EC, EE, EG, ES, FI, GB, GD, GE, GH, GM, HR, HU, ID, IL, IN, IS, JP, KE, KG, KM, KP, KR, KZ, LC, LK, LR, LS, LT, LU, LV, LY, MA, MD, MG, MK, MN, MW, MX, MZ, NA, NG, NI, NO, NZ, OM, PG, PH, PL, PT, RO, RU, SC, SD, SE, SG, SK, SL, SM, SY, TJ, TM, TN, TR, TT, TZ, UA, UG, US, UZ, VC, VN, YU, ZA, ZM, ZW.

(84) Designated States *(unless otherwise indicated, for every kind of regional protection available)*: ARIPO (BW, GH, GM, KE, LS, MW, MZ, NA, SD, SL, SZ, TZ, UG, ZM, ZW), Eurasian (AM, AZ, BY, KG, KZ, MD, RU, TJ, TM), European (AT, BE, BG, CH, CY, CZ, DE, DK, EE, ES, FI, FR, GB, GR, HU, IE, IS, IT, LT, LU, LV, MC, NL, PL, PT, RO, SE, SI, SK, TR), OAPI (BF, BJ, CF, CG, CI, CM, GA, GN, GQ, GW, ML, MR, NE, SN, TD, TG).

Published:
— *with international search report*

[Continued on next page]

(54) Title: RESOURCE SHARING IN A TELECOMMUNICATIONS ENVIRONMENT



(57) Abstract: A transceiver is designed to share memory and processing power amongst a plurality of transmitter and/or receiver latency paths, in a communications transceiver that carries or supports multiple applications. For example, the transmitter and/or receiver latency paths of the transceiver can share an interleaver/deinterleaver memory. This allocation can be done based on the data rate, latency, BER, impulse noise protection requirements of the application, data or information being transported over each latency path, or in general any parameter associated with the communications system.

WO 2006/044227 A1

For two-letter codes and other abbreviations, refer to the "Guidance Notes on Codes and Abbreviations" appearing at the beginning of each regular issue of the PCT Gazette.

RESOURCE SHARING IN A TELECOMMUNICATIONS ENVIRONMENT

RELATED APPLICATION DATA

[0001] This application claims the benefit of and priority under 35 U.S.C. § 119(e) to U.S. Patent Application No. 60/618,269, filed October 12, 2004, entitled "Sharing Memory and Processing Resources in DSL Systems," which is incorporated herein by reference in its entirety.

BACKGROUND

Field of the Invention

[0002] This invention generally relates to communication systems. More specifically, an exemplary embodiment of this invention relates to memory sharing in communication systems. Another exemplary embodiment relates to processing or coding resource sharing in a communication system.

Description of Related Art

[0003] U.S. Patent Nos. 6,775,320 and 6,778,589, which are both incorporated herein by reference in their entirety, describe DSL systems supporting multiple applications and multiple framer/coder/interleaver FCI blocks (an FCI block is also referred to as a latency path). DSL systems carry applications that have different transmission requirements with regard to, for example, data rate, latency (delay), bit error rate (BER), and the like. For example, video typically requires a low BER (<1E-10) but can tolerate higher latency (>20 ms). Voice, on the other hand, typically requires a low latency (<1 ms) but can tolerate BER (>1E-3).

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[0004] As described in U.S. Patent No. 6,775,320, different applications can use different latency paths in order to satisfy the different application requirements of the communication system. As a result a transceiver must support multiple latency paths in order to support applications such as video, Internet access and voice telephony. When implemented in a transceiver, each of the latency paths will have a framer, coder, and interleaver block with different capabilities that depend on the application requirements.

SUMMARY

[0005] One difficulty with implementing multiple latency paths in a transceiver is the fact that a latency path is a complicated digital circuit that requires a large amount of memory and processing power. An interleaver within a latency path can consume a large amount of memory in order to provide error correcting capability. For example, a typical DSL transceiver will have at least one latency path with approximately 16 kbytes of memory for the interleaver. Likewise, the coding block, for example, a Reed Solomon coder, consumes a large amount of processing power. In general, as the number of latency paths increase, the memory and processing power requirements for a communication system become larger.

[0006] Accordingly, an exemplary aspect of this invention relates to sharing memory between one or more interleavers and/or deinterlaevers in a transceiver. More particularly, an exemplary aspect of this invention relates to shared latency path memory in a transceiver.

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[0007] Additional aspects of this invention relate to configuring and initializing shared memory in a communication system. More particularly, an exemplary aspect of this invention relates to configuring and initializing interleaver/deinterleaver memory in a communication system.

[0008] Additional aspects of the invention relate to determining the amount of memory that can be allocated to a particular component by a communication system. More specifically, an exemplary aspect of the invention relates to determining the maximum amount of shared memory that can be allocated to one or more interleaves or deinterleavers.

[0009] According to another exemplary aspect of the invention, processing power is shared between a number of transceiver modules. More specifically, and in accordance with an exemplary embodiment of the invention, a coding module is shared between one or more coders and/or decoders.

[0010] Another exemplary embodiment of the invention relates to transitioning from a fixed memory configuration to a shared memory configuration during one or more of initialization and SHOWTIME (user data transmission).

[0011] An additional exemplary aspect of the invention relates to dynamically updating one or more of shared memory and processing resources based on changing communication conditions.

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[0012] An additional exemplary aspect of the invention relates to updating one or more of shared memory and processing resources based on an updated communication parameter.

[0013] An additional exemplary aspect of the invention relates to updating the allocation of one or more of shared memory and processing resources based on an updated communication parameter(s).

[0014] Additional aspects of the invention relate to exchanging shared resource allocations between transceivers.

[0015] Additional exemplary aspects relate to a method of allocating shared memory in a transceiver comprising allocating the shared memory to a plurality of modules, wherein each of the plurality of modules comprise at least one interleaver, at least one deinterleaver or a combination thereof.

[0016] Still further aspects relate to the above method wherein the plurality of modules comprise interleavers.

[0017] Still further aspects relate to the above method wherein the plurality of modules comprise deinterleavers.

[0018] Still further aspects relate to the above method wherein the plurality of modules comprise at least one interleaver and at least one deinterleaver.

[0019] Additional exemplary aspects relate to a transceiver comprising a plurality of modules each including at least one interleaver, at least one deinterleaver or a

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combination thereof and a shared memory designed to be allocated to a plurality of the modules.

[0020] Still further aspects relate to the above transceiver wherein the plurality of modules comprise interleavers.

[0021] Still further aspects relate to the above transceiver wherein the plurality of modules comprise deinterleavers.

[0022] Still further aspects relate to the above transceiver wherein the plurality of modules comprise at least one interleaver and at least one deinterleaver.

[0023] These and other features and advantages of this invention are described in, or are apparent from, the following description of the embodiments.

BRIEF DESCRIPTION OF THE DRAWINGS

[0024] The embodiments of the invention will be described in detail, with reference to the following figures, wherein:

[0025] Fig. 1 is a functional block diagram illustrating an exemplary transceiver according to this invention;

[0026] Fig. 2 is a flowchart outlining an exemplary method of sharing resources according to this invention;

[0027] Fig. 3 is a flowchart outlining an exemplary method of determining a maximum amount of shared memory according to this invention; and

[0028] Fig. 4 is a flowchart outlining an exemplary resource sharing methodology according to this invention.

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DETAILED DESCRIPTION

[0029] The exemplary embodiments of this invention will be described in relation to sharing resources in a wired and/or wireless communications environment. However, it should be appreciated, that in general, the systems and methods of this invention will work equally well for any type of communication system in any environment.

[0030] The exemplary systems and methods of this invention will also be described in relation to multicarrier modems, such as DSL modems and VDSL modems, and associated communication hardware, software and communication channels. However, to avoid unnecessarily obscuring the present invention, the following description omits well-known structures and devices that may be shown in block diagram form or otherwise summarized.

[0031] For purposes of explanation, numerous details are set forth in order to provide a thorough understanding of the present invention. It should be appreciated however that the present invention may be practiced in a variety of ways beyond the specific details set forth herein.

[0032] Furthermore, while the exemplary embodiments illustrated herein show the various components of the system collocated, it is to be appreciated that the various components of the system can be located at distant portions of a distributed

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network, such as a telecommunications network and/or the Internet, or within a dedicated secure, unsecured and/or encrypted system. Thus, it should be appreciated that the components of the system can be combined into one or more devices, such as a modem, or collocated on a particular node of a distributed network, such as a telecommunications network. As will be appreciated from the following description, and for reasons of computational efficiency, the components of the system can be arranged at any location within a distributed network without affecting the operation of the system. For example, the various components can be located in a Central Office modem (CO, ATU-C, VTU-O), a Customer Premises modem (CPE, ATU-R, VTU-R), a DSL management device, or some combination thereof. Similarly, one or more functional portions of the system could be distributed between a modem and an associated computing device.

[0033] Furthermore, it should be appreciated that the various links, including communications channel 5, connecting the elements can be wired or wireless links, or any combination thereof, or any other known or later developed element(s) that is capable of supplying and/or communicating data to and from the connected elements. The term module as used herein can refer to any known or later developed hardware, software, firmware, or combination thereof that is capable of performing the functionality associated with that element. The terms determine, calculate and compute, and variations thereof, as used herein are used interchangeably and include any type of methodology, process, mathematical operation or technique. FCI block and latency path are used interchangeably herein as well as transmitting modem and transmitting transceiver. Receiving modem and receiving transceiver are also used

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interchangeably.

[0034] Fig. 1 illustrates an exemplary embodiment of a transceiver 100 that utilizes shared resources. It should be appreciated that numerous functional components of the transceiver have been omitted for clarity. However, the transceiver 100 can also include the standard components found in typical communications device(s) in which the technology of the subject invention is implemented into.

[0035] According to an exemplary embodiment of the invention, memory and processing power can be shared among a plurality of transmitter and/or receiver latency paths, in a communications transceiver that carries or supports multiple applications. For example, the transmitter and/or receiver latency paths of the transceiver can share an interleaver/deinterleaver memory and the shared memory can be allocated to the interleaver and/or deinterleaver of each latency path. This allocation can be done based on the data rate, latency, BER, impulse noise protection requirements of the application, data or information being transported over each latency path, or in general any parameter associated with the communications system.

[0036] Likewise, for example, the transmitter and/or receiver latency paths can share a Reed-Solomon coder/decoder processing module and the processing power of this module can be allocated to each encoder and/or decoder. This allocation can be done based on the data rate/latency, BER, impulse noise protection requirements of the application data or information being transported over each latency path, or in general based on any parameter associated with the communication system.

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[0037] In accordance with an exemplary operational embodiment, a first transceiver and a second transceiver transmit to one another messages during, for example, initialization which contain information on the total and/or shared memory capabilities of each transceiver and optionally information about the one or more latency paths. This information can be transmitted prior to determining how to configure the latency paths to support the application requirements. Based on this information, one of the modems can select an FCI configuration parameter(s) that meets the transmission requirements of each application being transported over each latency paths. While an exemplary of the embodiment of the invention will be described in relation to the operation of the invention and characteristics thereof being established during initialization, it should be appreciated that the sharing of resources can be modified and messages transmitted between a two transceivers at any time during initialization and/or user data transmission, i.e., SHOWTIME.

[0038] Fig. 1 illustrates an exemplary embodiment of a transceiver 100. The transceiver 100 includes a transmitter portion 200 and a receiver portion 300. The transmitter portion 200 includes one or more latency paths 210, 220, ... Similarly, the receiver portion 300 includes one or more latency paths 310, 320, ... Each of the latency paths in the transmitter portion 200 includes a framer, coder, and interleaver designated as 212, 214, 216 and 222, 224 and 226, respectively. Each of the latency paths in the receiver portion includes a deframer, decoder, and deinterleaver designated as 312, 314, 316 and 322, 324, and 326, respectively. The transceiver 100 further includes a shared processing module 110, a shared memory 120, a parameter

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determination module 130, a path module 140, an allocation module 150, and a shared resource management module 160, all interconnected by one or more links (not shown).

[0039] In this exemplary embodiment, the transceiver 100 is illustrated with four total transmitter portion and receiver portion latency paths, i.e., 210, 220, 310, and 320. The shared memory 120 is shared amongst the two transmitter portion interleavers 216 and 226 and two receiver portion deinterleavers 316 and 326. The shared processing module 110, such as a shared coding module, is shared between the two transmitter portion coders 214 and 224 and the two receiver portion decoders 314 and 324.

[0040] While the exemplary embodiment of the invention will be described in relation to a transceiver having a number of transmitter portion latency paths and receiver portion latency paths, it should be appreciated that this invention can be applied to any transceiver having any number of latency paths. Moreover, it should be appreciated that the sharing of resources can be allocated such that one or more of the transmitter portion latency paths are sharing a shared resource, one or more of the receiver portion latency paths are sharing a shared resource, or a portion of the transmitter portion latency paths and a portion of the receiver portion latency paths are sharing shared resources. Moreover, any one or more of the latency paths, or portions thereof, could also be assigned to a fixed resource while, for example, another portion of the latency path(s) assigned to a shared resource. For example, in latency path 210, the interleaver 216 could be allocated a portion of the shared

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memory 120, while the coder 214 could be allocated to a dedicated processing module, vice versa, or the like.

[0041] In accordance with the exemplary embodiment, a plurality of transmitter portion or receiver portion latency paths share an interleaver/deinterleaver memory, such as shared memory 120, and a coding module, such as shared processing module 110. For example, the interleaver/deinterleaver memory can be allocated to different interleavers and/or deinterleavers. This allocation can be based on parameters associated with the communication systems such as data rate, latency, BER, impulse noise protection, and the like, of the applications being transported. Similarly, a coding module, which can be a portion of the shared processing module 110, can be shared between any one or more of the latency paths. This sharing can be based on requirements such as data rate, latency, BER, impulse noise protection, and the like, of the applications being transported.

[0042] For example, an exemplary transceiver could comprise a shared interleaver/deinterleaver memory and could be designed to allocate a first portion of the shared memory 120 to an interleaver, such as interleaver 216 in the transmitter portion of the transceiver and allocate a second portion of the shared memory 120 to a deinterleaver, such as 316, in the receiver portion of the transceiver.

[0043] Alternatively, for example, an exemplary transceiver can comprise a shared interleaver/deinterleaver memory, such as shared memory 120, and be designed to allocate a first portion of shared memory 120 to a first interleaver, e.g.,

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216, in the transmitter portion of the transceiver and allocate a second portion of the shared memory to a second interleaver, e.g., 226, in the transmitter portion of the transceiver.

[0044] Alternatively, for example, an exemplary transceiver can comprise a shared interleaver/deinterleaver memory and be designed to allocate a first portion of the shared memory 120 to a first deinterleaver, e.g., 316, in the receiver portion of the transceiver and allocate a second portion of the shared memory to a second deinterleaver, e.g., 326, in the receiver portion of the transceiver. Regardless of the configuration, in general any interleaver or deinterleaver, or grouping thereof, be it in a transmitter portion or receiver portion of the transceiver, can be associated with a portion of the shared memory 120.

[0045] Establishment, configuration and usage of shared resources is performed in the following exemplary manner. First, and in cooperation with the path module 140, the number of transmitter and receiver latency paths (N) is determined. The parameter determination module 130 then analyses one or more parameters such as data rate, transmitter data rate, receiver data rate, impulse noise protection, bit error rate, latency, or the like. Based on one or more of these parameters, the allocation module 150 allocates a portion of the shared memory 120 to one or more of the interleaver and/or deinterleavers, or groupings thereof. This process continues until the memory allocation has been determined and assigned to each of the N latency paths.

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[0046] Having determined the memory allocation for each of the latency paths, and in conjunction with the shared resource management 160, the transceiver 100 transmits to a second transceiver one or more of the number of latency paths (N), the maximum interleaver memory for any one or more of the latency paths and/or the maximum total and/or shared memory for all of the latency paths.

[0047] Three examples of sharing interleaver/deinterleaver memory and coding processing in a transceiver are described below. The latency paths in these examples can be in the transmitter portion of the transceiver or the receiver portion of the transceiver.

[0048] Example #1

A first transmitter portion or receiver portion latency path may carry data from a video application, which needs a very low BER but can tolerate higher latency. In this case, the video will be transported using an latency path that has a large amount of interleaving/deinterleaving and coding (also known as Forward Error Correction (FEC) coding). For example, the latency path may be configured with Reed-Solomon coding using a codeword size of 255 bytes (N=255) with 16 checkbytes (R=16) and interleaving/deinterleaving using an interleaver depth of 64 (D=64). This latency path will require N*D=16*255=16Kbytes of interleaver memory at the transmitter (or de-interleaver memory at the receiver). This latency path will be able to correct a burst of errors that is less than 512 bytes in duration.

[0049] A second transmitter portion or receiver portion latency path may carry an

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internet access application that requires a medium BER and a medium amount of latency. In this case, the internet access application will be transported using a latency path that has a medium amount of interleaving and coding. For example, the latency path may be configured with Reed-Solomon coding using a codeword size of 128 bytes (N=128) with 8 checkbytes (R=8) and interleaving using an interleaver depth of 16 (D=32). This latency path will require N*D=128*32=4Kbytes of interleaver memory and the same amount of deinterleaver memory. This latency path will be able to correct a burst of errors that is less than 128 bytes in duration.

[0050] A third transmitter portion or receiver portion latency path may carry a voice telephony application, which needs a very low latency but can tolerate BER. In this case, the video will be transported using an latency path that has a large amount of interleaving and coding. For example, the third transmitter portion or receiver portion latency path may be configured with no interleaving or coding which will result in the lowest possible latency through the latency path but will provide no error correction capability.

[0051] According to the principles of this invention, a system carrying the three applications described above in Example #1, would have three latency paths that share one memory space containing at least (16+4)=20 Kbytes. The three latency paths also share a common coding block that is able to simultaneously encode (in the transmitter portion) or decode (in a receiver portion) two codewords with N=255/R=16 and N=128/R=8.

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[0052] According to an exemplary embodiment of this invention, the latency paths can be reconfigured at initialization or during data transmission mode (also known as SHOWTIME in ADSL and VDSL transceivers). This would occur if, for example, the applications or application requirements were to change.

[0053] Example #2

If instead of 1 video application, 1 internet application and 1 voice application, there were 3 internet access applications then the transmitter portion and/or receiver portion latency paths would be reconfigured to utilize the shared memory and coding module in a different way. For example, the system could be reconfigured to have 3 transmitter portion or receiver portion latency paths, with each latency path being configured with Reed-Solomon coding using a codeword size of 128 bytes (N=128) with 8 checkbytes (R=8) and interleaving using an interleaver depth of 16 (D=32). Each latency path will require N*D=128*32=4Kbytes of interleaver memory and each block will be able to correct a burst of errors that is less than 128 bytes in duration. Based on the example of carrying the three internet access applications described, the three latency path share one memory space containing at least 3*4=12 Kbytes. Also the three latency paths share a common coding block that is able to simultaneously encode (on the transmitter side) or decode (on the receiver side) three codewords with N=128/R=16, N=128/R=8 and N=128/R=8.

[0054] Example #3

The system could be configured to carry yet another set of applications. For example, the latency paths could be configured to carry 2 video applications. In this case only

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2 transmitter portion or receiver portion latency paths are needed, which means that the third latency path could be simply disabled. Also, assuming that the memory is constrained based on the first example above, then the maximum shared memory for these 2 latency paths is 20 kBytes. In this case, the system could be reconfigured to have 2 latency paths, with each block being configured with Reed-Solomon coding using a codeword size of 200 bytes (N=200) with 10 checkbytes (R=10) and interleaving/deinterleaving using an interleaver depth of 50 (D=50). Each latency path will require N*D=200*50=10Kbytes of interleaver memory and each block will be able to correct a burst of errors that is less than 250 bytes in duration. This configuration results in 20K of shared memory for both latency paths, which is the same as in the first example. In order to stay within the memory constraints of the latency paths, the error correction capability for each latency path is decreased to 250 bytes from 512 bytes in Example #1.

[0055] Another aspect of this invention is the how FCI configuration information is transmitted between a first modem and a second modem. FCI configuration information will depend on the requirements of the applications being transported over the DSL connection. This information may need to be forwarded during initialization in order to initially configure the DSL connection. This information may also need to be forwarded during SHOWTIME in order to reconfigure the DSL connection based on a change in applications or the application requirements.

[0056] According to one embodiment, a first modem determines the specific FCI configuration parameters, e.g,. N, D, R as defined above, needed to meet specific

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application requirements, such as latency, burst error correction capability, etc. In order to determine the FCI configuration parameters, the first modem must know what are the capabilities of a second modem. For example, the first modem must know how many latency paths (FCI blocks) the second modem can support. Also the first modem must know the maximum amount of interleaver memory for each transmitter latency path. In addition, since the transmitter latency paths may share a common memory space the first modem must know the total shared memory for all transmitter latency paths. This way the first modem will be able to choose a configuration that can meet application requirements and also meet the transmitter portion latency path capabilities of the second modem.

[0057] For example, using values from examples above, a first transceiver could send a message to a second transceiver during initialization or during SHOWTIME containing the following information:

- Number of supported transmitter and receiver latency paths = 3
- Max Interleaver Memory for latency path #1= 16 Kbytes
- Max Interleaver Memory for latency path #2= 16 Kbytes
- Max Interleaver Memory for latency path #3= 16 Kbytes
- Maximum total/shared memory for all latency paths = 20 kBytes

Based on this information, and the application requirements, the first transceiver would select latency path settings. For example, if the applications are 1 video, 1 internet access and 1 voice application, the first transceiver could configure 3 latency paths as follows:

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latency path #1 – Video: N=255, R=16, D=64

latency path #2 – Video: N=128, R=8, D=32

latency path #3 – Video: N=0, R=0, D=1 (no coding or interleaving)

[0058] This would result in a total interleaver memory of 20 kbytes.

[0059] Alternatively, if for example, there are only 2 video applications, the first transceiver could configure 2 latency paths as follows:

latency path #1 – Video: N=200, R=10, D=50

latency path #2 – Video: N=200, R=10, D=50

latency path #3 – Video: N=0, R=0, D=1 (no coding or interleaving)

[0060] This would also result in a total interleaver memory of 20 kbytes.

[0061] Alternatively, the second transceiver can determine the specific FCI configuration parameters, e.g., N, D, R as defined above, needed to meet specific application requirements, such as latency, burst error correction capability, etc. As described above for the first transceiver, in order to determine the FCI configuration parameters, the second transceiver must first know what are the capabilities of the first transceiver. In this case, the first transceiver would send a message to the second transceiver containing the information described above and based on this information and the application requirements the second transceiver would select latency path settings.

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[0062] Fig. 2 outlines an exemplary method of allocating shared memory in a transceiver. More specifically, control begins in step S200 and continues to step S210. In step S210, one or more of shared interleaver/deinterleaver memory and/or shared coder/decoder processing resources are allocated to one or more latency paths, in a transceiver. Control then continues to step S220 where the control sequence ends.

[0063] Fig. 3 outlines an exemplary method of exchanging shared resource allocations according to an exemplary embodiment of this invention. In particular, control begins in step S310. In step S310, a maximum amount of shared memory that can be allocated to a specific interleaver or deinterleaver of a plurality of interleavers or deinterleavers in a transceiver is determined. Next, in step S320, the determined maximum amount for one or more of the deinterleavers and/or interleavers is transmitted to another transceiver. Messages containing additional information can also be transmitted to the other transceiver and/or received from the other transceiver. Control then continues to step S330 where the control sequence ends.

[0064] Fig. 4 outlines an exemplary procedure for resource sharing according to an exemplary embodiment of this invention. In particular, control begins in step S400 and continues to step S410. In step S410, the number of latency paths are determined. Then, in step S420, the latency path information (FCI block information) is transmitted to another transceiver. Messages containing additional information can also be transmitted to the other transceiver and/or received from the other transceiver. This information can be used to, for example, assist with the determination of

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memory allocation in the transceiver. Moreover, the messages received from the other transceiver could specify what the memory allocation is to be based on, for example, the number of latency paths, memory allocation in the remote transceiver and required applications. Control then continues to step S430.

[0065] In step S430, and for each latency path, the steps in step 440 are performed.

[0066] In step S440, and while monitoring of allocation of resources is being performed, steps 450 and 460 are performed. More specifically, in step S450, one or more parameters associated with the communication system are determined. Then, in step S460, shared resources are allocated based on one or more of the communication parameters. Control then continues to step S470.

[0067] In step S470, the allocation of shared resources is communicated to another transceiver. Next, in step S480, a determination is made as to whether there is a change in communications that would require the adjustment of the shared resource allocation. Examples of changes in communications conditions include a change in applications being transported over the system and/or changes in the channel condition, etc. If adjustments are required, control jumps back to step S410. Otherwise, control jumps to step S490 where the control sequence ends.

[0068] The above-described system can be implemented on wired and/or wireless telecommunications devices, such a modem, a multicarrier modem, a DSL modem, an

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ADSL modem, an XDSL modem, a VDSL modem, a linecard, test equipment, a multicarrier transceiver, a wired and/or wireless wide/local area network system, a satellite communication system, a modem equipped with diagnostic capabilities, or the like, or on a separate programmed general purpose computer having a communications device or in conjunction with any of the following communications protocols: CDSL, ADSL2, ADSL2+, VDSL1, VDSL2, HDSL, DSL Lite, IDSL, RADSL, SDSL, UDSL or the like.

[0069] Additionally, the systems, methods and protocols of this invention can be implemented on a special purpose computer, a programmed microprocessor or microcontroller and peripheral integrated circuit element(s), an ASIC or other integrated circuit, a digital signal processor, a hard-wired electronic or logic circuit such as discrete element circuit, a programmable logic device such as PLD, PLA, FPGA, PAL, a modem, a transmitter/receiver, any comparable means, or the like. In general, any device capable of implementing a state machine that is in turn capable of implementing the methodology illustrated herein can be used to implement the various communication methods, protocols and techniques according to this invention.

[0070] Furthermore, the disclosed methods may be readily implemented in software using object or object-oriented software development environments that provide portable source code that can be used on a variety of computer or workstation platforms. Alternatively, the disclosed system may be implemented partially or fully in hardware using standard logic circuits or VLSI design. Whether software or

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hardware is used to implement the systems in accordance with this invention is dependent on the speed and/or efficiency requirements of the system, the particular function, and the particular software or hardware systems or microprocessor or microcomputer systems being utilized. The communication systems, methods and protocols illustrated herein can be readily implemented in hardware and/or software using any known or later developed systems or structures, devices and/or software by those of ordinary skill in the applicable art from the functional description provided herein and with a general basic knowledge of the computer and telecommunications arts.

[0071] Moreover, the disclosed methods may be readily implemented in software that can be stored on a storage medium, executed on programmed general-purpose computer with the cooperation of a controller and memory, a special purpose computer, a microprocessor, or the like. In these instances, the systems and methods of this invention can be implemented as program embedded on personal computer such as an applet, JAVA® or CGI script, as a resource residing on a server or computer workstation, as a routine embedded in a dedicated communication system or system component, or the like. The system can also be implemented by physically incorporating the system and/or method into a software and/or hardware system, such as the hardware and software systems of a communications transceiver.

[0072] It is therefore apparent that there has been provided, in accordance with the present invention, systems and methods for sharing resources. While this invention has been described in conjunction with a number of embodiments, it is

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evident that many alternatives, modifications and variations would be or are apparent to those of ordinary skill in the applicable arts. Accordingly, it is intended to embrace all such alternatives, modifications, equivalents and variations that are within the spirit and scope of this invention.

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Claims:

1. A method for sharing resources in a transceiver comprising:

allocating a first portion of shared memory to a first latency path and allocating a second portion of the shared memory to a second latency path.

2. The method of claim 1, wherein the first latency path includes an interleaver and the second latency path includes an interleaver.

3. The method of claim 1, wherein the first latency path includes an interleaver and the second latency path includes a deinterleaver.

4. The method of claim 1, wherein the first latency path includes a deinterleaver and the second latency path includes a deinterleaver.

5. The method of claim 1, further comprising transmitting to another transceiver information that is used to determine a maximum amount of shared memory that can be allocated.

6. The method of claim 1, further comprising receiving from another transceiver information that is used to determine a maximum amount of shared memory that can be allocated.

7. The method of claim 1, further comprising allocating a shared processing module to a plurality of coding and/or decoding modules.

8. The method of claim 1, wherein the allocating of at least one portion of the shared memory is based on one or more communication parameters.

9. The method of claim 8, wherein at least one of the communication parameters is a data rate, a latency, an INP value or a bit error rate (BER).

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10. A transceiver comprising:

a first portion of shared memory that is allocated to a first latency path; and

a second portion of the shared memory that is allocated to a second latency path.

11. The transceiver of claim 10, further comprising:

an allocation module designed to allocate the shared memory based on one or more communication parameters.

12. The transceiver of claim 11, wherein at least one of the communication parameters is a data rate, a latency, an INP value or a Bit Error Rate (BER).

13. The transceiver of claim 10, wherein the first latency path includes an interleaver and the second latency path includes an interleaver.

14. The transceiver of claim 10, wherein the first latency path includes an interleaver and the second latency path includes a deinterleaver.

15. The transceiver of claim 10, wherein the first latency path includes a deinterleaver and the second latency path includes a deinterleaver.

16. The transceiver of claim 10, further comprising a shared resource management module designed to determine information that is transmitted to another transceiver, wherein the information is used to determine a maximum amount of shared memory that can be allocated.

17. The transceiver of claim 10, further comprising a shared resource management module designed to utilize information that is received from another transceiver, wherein the information is used to determine a maximum amount of shared memory that can be allocated.

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18. The transceiver of claim 10, further comprising a shared processing module designed to provide processing resources to a plurality of coding and/or decoding modules.

19. A system for sharing resources in a transceiver comprising:

means for allocating a first portion of shared memory to a first latency path and means for allocating a second portion of the shared memory to a second latency path.

20. The system of claim 19, wherein the first latency path includes an interleaver and the second latency path includes an interleaver.

21. The system of claim 19, wherein the first latency path includes an interleaver and the second latency path includes a deinterleaver.

22. The system of claim 19, wherein the first latency path includes a deinterleaver and the second latency path includes a deinterleaver.

23. The system of claim 19, further comprising means for transmitting to another transceiver information that is used to determine a maximum amount of shared memory that can be allocated.

24. The system of claim 19, further comprising means for receiving from another transceiver information that is used to determine a maximum amount of shared memory that can be allocated.

25. The system of claim 19, further comprising means for allocating a shared processing module to a plurality of coding and/or decoding modules.

26. The system of claim 19, wherein the allocating of at least one portion

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of the shared memory is based on one or more communication parameters.

27. The system of claim 26, wherein at least one of the communication parameters is a data rate, a latency, an INP value or a bit error rate (BER).

28. A protocol for sharing resources in a transceiver comprising:

allocating a first portion of shared memory to a first latency path and allocating a second portion of the shared memory to a second latency path.

29. The protocol of claim 28, wherein the first latency path includes an interleaver and the second latency path includes an interleaver.

30. The protocol of claim 28, wherein the first latency path includes an interleaver and the second latency path includes a deinterleaver.

31. The protocol of claim 28, wherein the first latency path includes a deinterleaver and the second latency path includes a deinterleaver.

32. The protocol of claim 28, further comprising transmitting to another transceiver information that is used to determine a maximum amount of shared memory that can be allocated.

33. The protocol of claim 28, further comprising receiving from another transceiver information that is used to determine a maximum amount of shared memory that can be allocated.

34. The protocol of claim 28, further comprising allocating a shared processing module to a plurality of coding and/or decoding modules.

35. The protocol of claim 28, wherein the allocating of at least one portion of the shared memory is based on one or more communication parameters.

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36. The protocol of claim 35, wherein at least one of the communication parameters is a data rate, a latency, an INP value or a bit error rate (BER).

37. An information storage media having stored thereon information that when executed allows sharing of resources in a transceiver comprising:

information that allocates a first portion of shared memory to a first latency path and information that allocates a second portion of the shared memory to a second latency path.

38. The media of claim 37, wherein the first latency path includes an interleaver and the second latency path includes an interleaver.

39. The media of claim 37, wherein the first latency path includes an interleaver and the second latency path includes a deinterleaver.

40. The media of claim 37, wherein the first latency path includes a deinterleaver and the second latency path includes a deinterleaver.

41. The media of claim 37, further comprising information that transmits to another transceiver information that is used to determine a maximum amount of shared memory that can be allocated.

42. The media of claim 37, further comprising information that receives from another transceiver information that is used to determine a maximum amount of shared memory that can be allocated.

43. The media of claim 37, further comprising information that allocates a shared processing module to a plurality of coding and/or decoding modules.

44. The media of claim 37, wherein the allocating of at least one portion of

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the shared memory is based on one or more communication parameters.

45. The media of claim 44, wherein at least one of the communication parameters is a data rate, a latency, an INP value or a bit error rate (BER).

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IPR2023-00064, Ex. 1035
Page 475 of 531

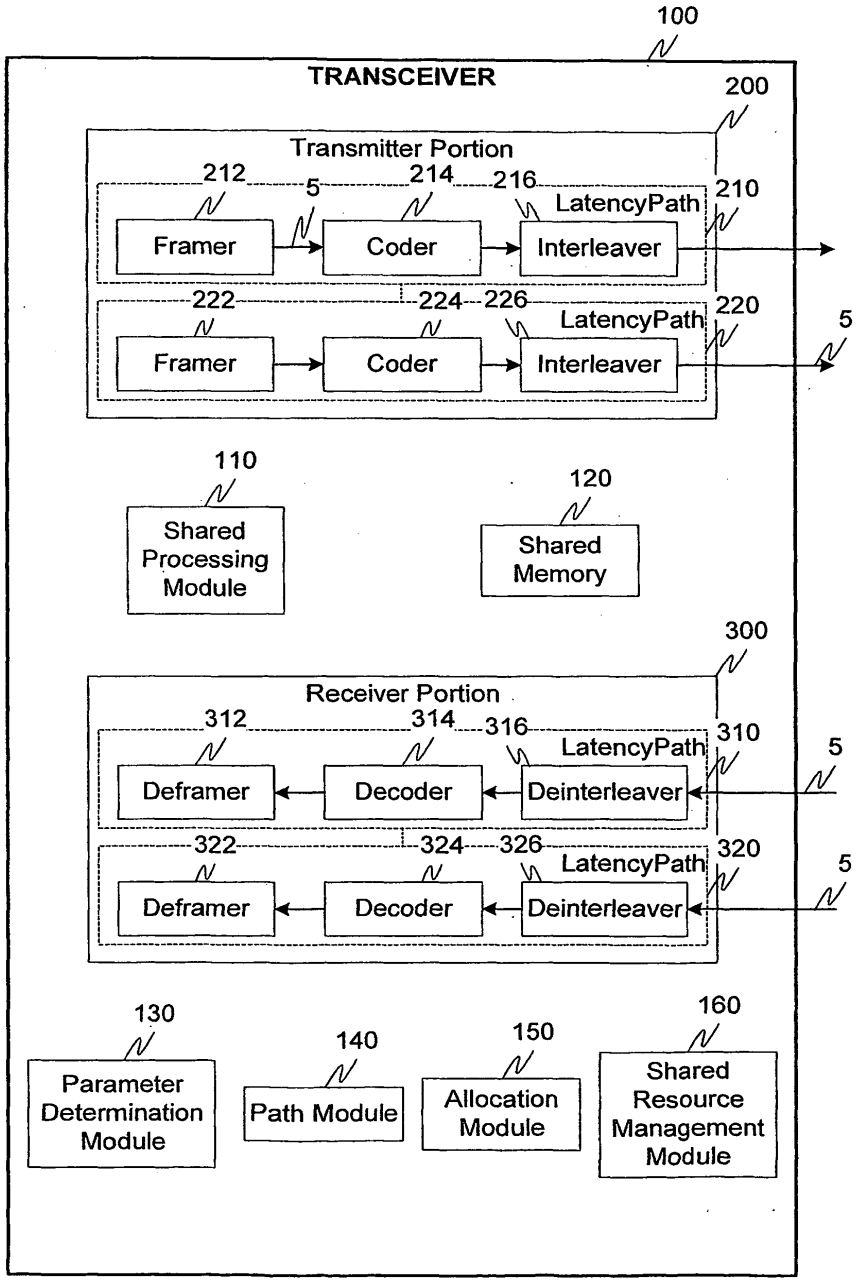
100
TRANSCEIVER
200
Transmitter Portion
212
5
214
216
LatencyPath
210
Framer
Coder
Interleaver
222
224
226
LatencyPath
220
5
Framer
Coder
Interleaver
110
Shared Processing Module
120
Shared Memory
300
Receiver Portion
312
314
316
LatencyPath
310
5
Deframer
Decoder
Deinterleaver
322
324
326
LatencyPath
320
5
Deframer
Decoder
Deinterleaver
130
Parameter Determination Module
140
Path Module
150
Allocation Module
160
Shared Resource Management Module

Fig. 1

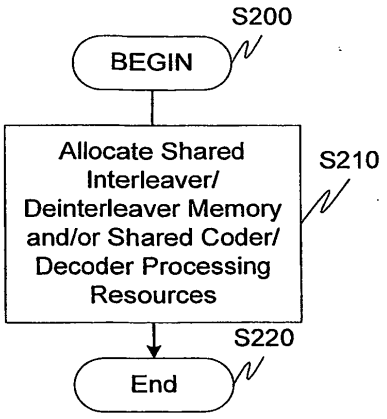
S200
BEGIN
Allocate Shared Interleaver/ Deinterleaver Memory and/or Shared Coder/ Decoder Processing Resources
S210
S220
End

Fig. 2

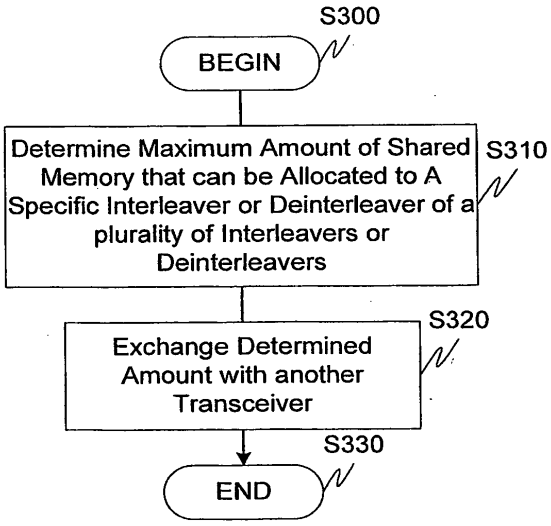
S300
BEGIN
Determine Maximum Amount of Shared Memory that can be Allocated to A Specific Interleaver or Deinterleaver of a plurality of Interleavers or Deinterleavers
S310
Exchange Determined Amount with another Transceiver
S320
S330
END

Fig. 3

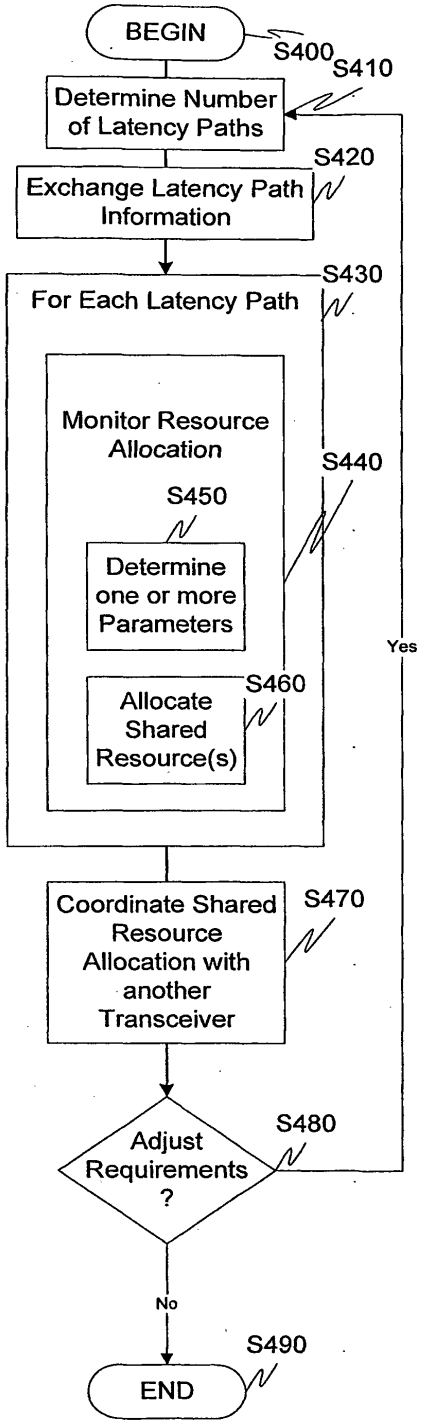
BEGIN
S400
S410
Determine Number of Latency Paths
S420
Exchange Latency Path Information
S430
For Each Latency Path
Monitor Resource Allocation
S440
S450
Determine one or more Parameters
S460
Allocate Shared Resource(s)
Yes
S470
Coordinate Shared Resource Allocation with another Transceiver
S480
Adjust Requirements ?
No
S490
END

Fig. 4

OIPE IAP40 JAN 06 2006 PATENT & TRADEMARK OFFICE

Attorney Docket No. T3653-9285US01

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Patent Application of:

First Named Inventor: TZANNES, MARCOS C. **Art Unit: 2186**

Appln. No.: 11/246,163 **Examiner:**

Filed: October 11, 2005 **Confirmation No.: 5478**

For: SHARING MEMORY AND PROCESSING RESOURCES IN DSL SYSTEMS

* * *

REPLY TO NOTICE TO FILE MISSING PARTS

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Sir:

In response to the Notice to File Missing Parts of Non-Provisional Application under 37 CFR 1.53(b) dated November 8, 2005, submitted herewith are the following items:

- Executed Declaration in compliance with 37 CFR 1.63; Executed Power of Attorney;
- Copy of Notice to File Missing Parts of Non-Provisional Application;
- Assignment and Assignment Recordation Transmittal;
- Checks in the amounts of $130 and $80

The Commissioner is hereby authorized to charge to Deposit Account No. 50-1165 (T3653-9285US01) any fees under 37 C.F.R. §§ 1.16 and 1.17 that may be required by this paper and to credit any overpayment to that Account. If any extension of time is required in connection with the filing of this paper and has not been separately requested, such extension is hereby requested.

Respectfully submitted,

By: _____
Jason H. Vick
Reg. No. 45,285

Miles & Stockbridge P.C.
1751 Pinnacle Drive, Suite 500
McLean, Virginia 22102-3833
(703) 903-9000
January 6, 2006
#9286914
JHV:jab

OTPE
JAN 06 2006
PATENT & TRADEMARK OFFICE

UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NUMBER	FILING OR 371 (c) DATE	FIRST NAMED APPLICANT	ATTORNEY DOCKET NUMBER
11/246,163	10/11/2005	Marcos C. Tzannes	T3653-9285US01

CONFIRMATION NO. 5478

181
MILES & STOCKBRIDGE PC
1751 PINNACLE DRIVE
SUITE 500
MCLEAN, VA 22102-3833

FORMALITIES LETTER

Date Mailed: 11/08/2005

NOTICE TO FILE MISSING PARTS OF NONPROVISIONAL APPLICATION

FILED UNDER 37 CFR 1.53(b)

Filing Date Granted

Items Required To Avoid Abandonment:

An application number and filing date have been accorded to this application. The item(s) indicated below, however, are missing. Applicant is given **TWO MONTHS** from the date of this Notice within which to file all required items and pay any fees required below to avoid abandonment. Extensions of time may be obtained by filing a petition accompanied by the extension fee under the provisions of 37 CFR 1.136(a).

- The oath or declaration is missing. *A properly signed oath or declaration in compliance with 37 CFR 1.63, identifying the application by the above Application Number and Filing Date, is required.*
  Note: If a petition under 37 CFR 1.47 is being filed, an oath or declaration in compliance with 37 CFR 1.63 signed by all available joint inventors, or if no inventor is available by a party with sufficient proprietary interest, is required.

The applicant needs to satisfy supplemental fees problems indicated below.

The required item(s) identified below must be timely submitted to avoid abandonment:

- To avoid abandonment, a surcharge (for late submission of filing fee, search fee, examination fee or oath or declaration) as set forth in 37 CFR 1.16(f) of $130 for a non-small entity, must be submitted with the missing items identified in this letter.

SUMMARY OF FEES DUE:

Total additional fee(s) required for this application is **$130** for a Large Entity

- **$130** Surcharge.

Replies should be mailed to: Mail Stop Missing Parts

01/09/2006 HALI11 00000068 11246163
130.00 OP
01 FC:1051

Commissioner for Patents
P.O. Box 1450
Alexandria VA 22313-1450

A copy of this notice MUST be returned with the reply.

Office of Initial Patent Examination (571) 272-4000, or 1-800-PTO-9199, or 1-800-972-6382
PART 2 - COPY TO BE RETURNED WITH RESPONSE

COMBINED FEE TRANSMITTAL for FY 2005

Effective 12/08/2004. Patent fees are subject to annual revision.

PTO/SB/17 (12-04) (Revised) (For payment of 37 CFR 1.17 fees including (f), (g), (h) & (i))

PTO JAN 06 2006 PATENT & TRADEMARK OFFICE

☒ Applicant claims small entity status. See 37 CFR 1.27

TOTAL AMOUNT OF PAYMENT | $ 65.00

Complete if Known	
Application Number	10/923,592
Filing Date	August 20, 2004
First Named Inventor	WANG et al.
Examiner Name	Unassigned
Art Unit	1626
Attorney Docket No.	40627-0002US1

METHOD OF PAYMENT (check one)

☒ Check ☐ Deposit Account	☐ Credit card	☐ Money Order	☐ Other	☐ None

Deposit Account Number: 08-1641

Deposit Account Name: Heller Ehrman LLP

The Commissioner is authorized to: *(check all that apply)*

☐ Charge fee(s) indicated below

☒ Credit any overpayments and charge any deficiencies

☐ Charge any additional fee(s) during the pendency of this application

☐ Charge fee(s) indicated below, **except for the filing fee** to the deposit account

FEE CALCULATION

1. BASIC FILING, SEARCH, AND EXAMINATION FEES

	FILING FEES		SEARCH FEES		EXAMINATION FEES		
Application Type	**Entity Fee ($)**	**Small Entity Fee ($)**	**Entity Fee ($)**	**Small Entity Fee ($)**	**Entity Fee ($)**	**Small Entity Fee ($)**	**Fees Paid ($)**
Utility	300	150	500	250	200	100	
Design	200	100	100	50	135	65	
Plant	200	100	300	150	160	80	
Reissue	300	150	500	250	600	300	
Provisional	200	100	0	0	0	0	

SUBTOTAL (1)

2. EXTRA CLAIM FEES

Entity Fee ($)	Small Entity Fee ($)	Fee Description
50	25	Each claim in excess of 20 or, for Reissues, each claim in excess of 20 and more than in the original patent
200	100	Each Independent claim in excess of 3 or, for Reissues, each independent claim more than in the original patent
360	180	Multiple dependent claim, if not already paid

			Extra Claims		Fee from above		Fee Paid
Total Claims		-20** =		x	25	=	
Independent Claims		-3** =		x	100	=	

***or number previously paid, if greater; For Reissues see below*

Multiple Dependent: 180 =

SUBTOTAL (2) $

3. APPLICATION SIZE FEE

If the specification and drawings exceed 100 sheets of paper, the application size fee due is $250 ($125 for small entity) for each additional 50 sheets or fraction thereof (round up to the a whole number). See 35 U.S.C. 41(a)(1)(G) and 37 CFR 1.16(s)

Total Sheets		Extra Sheets		Number of each additional 50	Fee ($)		Small Entity Fee ($)
	-100 =		/50 =		x 250	OR	x 125

SUBTOTAL (3) $

FEE CALCULATION (continued)

4. PETITION FEES UNDER 37 CFR 1.17 (f) — Fee Paid
Fee Code: 1462 **Fee $ 400** For petitions filed under: § 1.53(e); § 1.57(a); § 1.182; § 1.183; § 1.378(e); § 1.741(b)

5. PETITION FEES UNDER 37 CFR 1.17 (g) — Fee Paid
Fee Code: 1463 **Fee $ 200** For petitions filed under: § 1.12; § 1.14; § 1.47; § 1.59; § 1.103(a); § 1.136(b); § 1.295; § 1.296; § 1.377; § 1.550(c); § 1.956; § 5.12; § 5.15; § 5.25

6. PETITION FEES UNDER 37 CFR 1.17 (h) — Fee Paid
Fee Code: 1464 **Fee $ 130** For petitions filed under: § 1.19(g); § 1.84; § 1.91; § 1.102(d); § 1.138(c); § 1.313; § 1.314

7. PROCESSING FEES UNDER 37 CFR 1.17 (i) — Fee Paid
Fee Code: 1808 (1803 for § 1.221) **Fee $ 130** For petitions filed under: § 1.28(c)(3); § 1.41; § 1.48; § 1.52(d); § 1.53(b)(3); § 1.55; § 1.99(e); § 1.103(b); § 1.103(c); § 1.103(d); § 1.217; § 1.221; § 1.291(c)(5); § 1.497(d); § 3.81

8. OTHER FEES

Entity Fee ($)	Entity Fee ($)	Fee Description	Fee Paid
130	65	Surcharge - late filing fee or oath	65
50	25	Surcharge - late provisional filing fee or cover sheet	
130	130	Non-English specification	
2,520	2,520	For filing a request for *ex parte* reexamination	
920*	920*	Requesting publication of SIR prior to Examiner action	
1,840*	1,840*	Requesting publication of SIR after Examiner action	
120	60	Extension for reply within first month	
450	225	Extension for reply within second month	
1,020	510	Extension for reply within third month	
1,590	795	Extension for reply within fourth month	
2,160	1,080	Extension for reply within fifth month	
500	250	Filing a brief in support of an appeal	
790	395	Filing a submission after final rejection (37 CFR 1.129(a))	
1,510	1,510	Petition to institute a public use proceeding	
500	250	Petition to revive - unavoidably abandoned application	
1,500	750	Petition to revive - unintentionally abandoned application	
50	50	Processing fee for provisional appls (37 CFR 1.17(q))	
180	180	Submission of Information Disclosure Statement	
1,000	500	Request for oral hearing	
790	395	For each additional invention to be examined (37 CFR 1.129(b))	
790	395	Request for Continued Examination (RCE)	
900	900	Request for expedited examination of a design application	

Other fee (specify)

SUBTOTAL (4+5+6+7+8) $ 65.00

* Reduced by Basic Filing Fee Paid

SUBMITTED BY				Complete *(if applicable)*	
Name *(Print/Type)*	Paul W. Booth	Registration No. *(Attorney/Agent)*	40,244	*Telephone*	202-912-2000
Signature		*Date*	January 6, 2006	Customer No.	26633

PTO/SB/21 (08-00)

Please type a plus sign (+) inside this box → [+]

Approved for use through 10/31/2002. OMB 0651-0031
U.S. Patent and Trademark Office: U.S. DEPARTMENT OF COMMERCE
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TRANSMITTAL FORM

(to be used for all correspondence after initial filing)

OIPE IAP34 JAN 06 2006 PATENT & TRADEMARK OFFICE

Application Number	10/923,592
Filing Date	August 20, 2004
First Named Inventor	WANG et al.
Group Art Unit	1626
Examiner Name	Unassigned
Attorney Docket Number	40627-0002US1

Total Number of Pages in This Submission

ENCLOSURES *(check all that apply)*

- ☒ Fee Transmittal Form
- ☒ Fee Attached
- ☐ Amendment / Response
- ☐ After Final
- ☐ Affidavits/declaration(s)
- ☐ Extension of Time Request
- ☐ Express Abandonment Request
- ☐ Information Disclosure Statement
- ☐ Certified Copy of Priority Document(s)
- ☐ Response to Missing Parts/ Incomplete Application
- ☐ Response to Missing Parts under 37 CFR 1.52 or 1.53
- ☐ Assignment Papers *(for an Application)*
- ☐ Drawing(s)
- ☐ Licensing-related Papers
- ☐ Petition
- ☐ Petition to Convert to a Provisional Application
- ☐ Power of Attorney, Revocation Change of Correspondence Address
- ☐ Terminal Disclaimer
- ☐ Request for Refund
- ☐ CD, Number of CD(s) ____
- ☐ After Allowance Communication to Group
- ☐ Appeal Communication to Board of Appeals and Interferences
- ☐ Appeal Communication to Group *(Appeal Notice, Brief, Reply Brief)*
- ☐ Proprietary Information
- ☐ Status Letter
- ☒ Other Enclosure(s) *(please identify below)*:
  Response to Missing Parts of Nonprovisional Application

Remarks

SIGNATURE OF APPLICANT, ATTORNEY, OR AGENT

Firm or Individual name	Paul M. Booth, Reg. No. 40,244, Customer No. 26633
Signature	
Date	January 6, 2006

CERTIFICATE OF MAILING

I hereby certify that this correspondence is being deposited with the United States Postal Service as first class mail in an envelope addressed to: Assistant Commissioner for Patents, Washington, D.C. 20231 on this date: ____

Typed or printed name			
Signature		Date	

Burden Hour Statement: This form is estimated to take 0.2 hours to complete. Time will vary depending upon the needs of the individual case. Any comments on the amount of time you are required to complete this form should be send to the Chief Information Officer, U.S. Patent and Trademark Office, Washington, DC 20231. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. SEND TO: Assistant Commissioner for Patents, Washington, DC 20231.

OIPE IAP34
JAN 0 6 2006
PATENT & TRADEMARK OFFICE

Attorney Docket No. 40627-0002US1

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant(s)	WANG et al.	Confirmation No.:	4888
Appl. No.:	10/923,592	Group Art Unit:	1626
Filing Date:	August 20, 2004	Examiner:	Unassigned
Title:	SUBSTITUTED 8-HETEROARYL XANTHINES		

RESPONSE TO NOTICE TO FILE MISSING PARTS

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Sir:

This communication responds to the Notice to File Missing Parts mailed October 19, 2004, in the above-captioned application. Applicants submitted the required Declaration and Power of Attorney, in a timely fashion, in response to the Notice on December 4, 2004, paying the $65.00 filing fee under small entity status. Applicants have since been informed that this application no longer qualifies for small entity status. Thus, Applicants submit herewith an addition filing fee of $65.00 under 37 CFR 1.27 for large entity.

Applicants believe the appropriate fees are attached, however, the Commissioner is hereby authorized to charge any deficiency or to credit any overpayment to Deposit Account No. 08-1641.

Respectfully submitted,

Date: January 6, 2006

HELLER EHRMAN LLP
1717 Rhode Island Avenue, NW
Washington, D.C. 20036
Phone: 202-912-2000
Fax: 202-912-2020

Paul M. Booth
Reg. No. 40,244
Attorney for Applicant

Customer No. 26633

01/09/2006 HALI11 00000086 10923592
01 FC:2051 65.00 OP

OIPE IAP40 JAN 06 2006 PATENT & TRADEMARK OFFICE

PTO/SB/01A (09-04)
Approved for use through 07/31/2006 OMB 0651-0032
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Docket No. T3653-9285US01

DECLARATION (37 CFR 1.63) FOR UTILITY OR DESIGN APPLICATION USING AN APPLICATION DATA SHEET (37 CFR 1.76)

Title of Invention	RESOURCE SHARING IN A TELECOMMUNICATIONS ENVIRONMENT

As the below named inventor(s), I/we declare that:

This declaration is directed to:

☐ The attached application, or

☒ Application No. 11/246,163, filed on October 11, 2005

☐ as amended on _____ (if applicable):

I/we believe that I/we am/are the original and first inventor(s) of the subject matter which is claimed and for which a patent is sought;

I/we have reviewed and understand the contents of the above-identified application, including the claims, as amended by any amendment specifically referred to above;

I/we acknowledge the duty to disclose to the United States Patent and Trademark Office all information known to me/us to be material to patentability as defined in 37 CFR 1.56, including for continuation-in-part applications, material information which became available between the filing date of the prior application and the national or PCT International filing date of the continuation-in-part application.

All statements made herein of my/own knowledge are true, all statements made herein on information and belief are believed to be true, and further that these statements were made with the knowledge that willful false statements and the like are punishable by fine or imprisonment, or both, under 18 U.S.C. 1001, and may jeopardize the validity of the application or any patent issuing thereon.

FULL NAME OF INVENTOR(S)

Inventor one: Marcos C. TZANNES

Signature: _____ Citizen of: U.S.A.

Inventor two: Michael LUND

Signature: _____ Citizen of: U.S.A.

Inventor three: _____

Signature: _____ Citizen of: _____

Inventor four: _____

Signature: _____ Citizen of: _____

☐ Additional inventors or a legal representative are being named on _____ additional form(s) attached hereto.

This collection of information is required by 37 U.S.C. 115 and 37 CFR 1.63. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.11 and 1.14. This collection is estimated to take 1 minute to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.

PAGE 2/5 * RCVD AT 1/5/2006 11:05:03 AM [Eastern Standard Time] * SVR:TYSOFAX/0 * DNIS:9994 * CSID:17816870430 * DURATION (mm-ss):02-14

OIPE IAP40 JAN 06 2006 PATENT & TRADEMARK OFFICE

PTO/SB/81 (11-04)
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POWER OF ATTORNEY and CORRESPONDENCE ADDRESS INDICATION FORM

Application Number	
Filing Date	
First Named Inventor	Marcos C. TZANNES
Title	RESOURCE SHARING IN A TELECOMMUNICATIONS ENVIRONMENT
Art Unit	
Examiner Name	
Attorney Docket Number	T3653-9285US01

I hereby revoke all previous powers of attorney given in the above-identified application.

I hereby appoint:

☒ Practitioners associated with the Customer Number: 000181

OR

☐ Practitioner(s) named below:

Name	Registration Number

as my/our attorney(s) or agent(s) to prosecute the application identified above, and to transact all business in the United States Patent and Trademark Office connected therewith.

Please recognize or change the correspondence address for the above-identified application to:

☒ The address associated with the above-mentioned Customer Number:

OR

☐ The address associated with Customer Number:

☐ Firm or Individual Name					
Address					
City		State		Zip	
Country					
Telephone		Fax			

I am the:

☒ Applicant/Inventor.

☐ Assignee of record of the entire interest. See CFR 3.71.
Statement under 37 CFR 3.73(b) is enclosed. (Form PTO/SB/96).

SIGNATURE of Applicant or Assignee of Record

Signature		Date	November 29, 2005
Name	Michael LUND	Telephone	
Title and Company			

NOTE: Signatures of all the inventors or assignees of record of the entire interest or their representative(s) are required. Submit multiple forms if more than one signature is required, see below*.

☒ *Total of 2 forms are submitted.

This collection of information is required by 37 CFR 1.32, 1.33 and 1.33. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.11 and 1.14. This collection is estimated to take 3 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

PAGE 3/5 * RCVD AT 1/5/2006 11:05:03 AM [Eastern Standard Time] * SVR:TYSOFAX/0 * DNIS:9994 * CSID:17816870430 * DURATION (mm-ss):02-14

OIPE IAP40 JAN 06 2006 PATENT & TRADEMARK OFFICE

PTO/SB/81 (11-04)
Approved for use through 01/30/2005 OMB 0651-0035
U.S. Patent and Trademark Office: U.S. DEPARTMENT OF COMMERCE
Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it displays a valid OMB control number.

POWER OF ATTORNEY and CORRESPONDENCE ADDRESS INDICATION FORM

Application Number	
Filing Date	
First Named Inventor	Marcos C. TZANNES
Title	RESOURCE SHARING IN A TELECOMMUNICATIONS ENVIRONMENT
Art Unit	
Examiner Name	
Attorney Docket Number	T3653-9285US01

I hereby revoke all previous powers of attorney given in the above-identified application.

I hereby appoint:

☒ Practitioners associated with the Customer Number: **000181**

OR

Name	Registration Number

as my/our attorney(s) or agent(s) to prosecute the application identified above, and to transact all business in the United States Patent and Trademark Office connected therewith.

Please recognize or change the correspondence address for the above-identified application to:

☒ The address associated with the above-mentioned Customer Number:

OR

☐ The address associated with Customer Number:

OR

☐ Firm or Individual Name					
Address					
City		State		Zip	
Country					
Telephone		Fax			

I am the:

☒ Applicant/Inventor.

☐ Assignee of record of the entire interest. See CFR 3.71.
Statement under 37 CFR 3.73(b) is enclosed. (Form PTO/SB/96).

SIGNATURE of Applicant or Assignee of Record

Signature		Date	November 29, 2005
Name	Marcos C. TZANNES	Telephone	
Title and Company			

NOTE: Signatures of all the inventors or assignees of record of the entire interest or their representative(s) are required. Submit multiple forms if more than one signature is required, see below*.

☒ *Total of 2 form is submitted.

This collection of information is required by 37 CFR 1.32, 1.33 and 1.33. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.11 and 1.14. This collection is estimated to take 3 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.

UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
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APPLICATION NUMBER	FILING OR 371 (c) DATE	FIRST NAMED APPLICANT	ATTORNEY DOCKET NUMBER
11/246,163	10/11/2005	Marcos C. Tzannes	T3653-9285US01

CONFIRMATION NO. 5478

FORMALITIES LETTER

181
MILES & STOCKBRIDGE PC
1751 PINNACLE DRIVE
SUITE 500
MCLEAN, VA 22102-3833

Date Mailed: 11/08/2005

NOTICE TO FILE MISSING PARTS OF NONPROVISIONAL APPLICATION

FILED UNDER 37 CFR 1.53(b)

Filing Date Granted

Items Required To Avoid Abandonment:

An application number and filing date have been accorded to this application. The item(s) indicated below, however, are missing. Applicant is given **TWO MONTHS** from the date of this Notice within which to file all required items and pay any fees required below to avoid abandonment. Extensions of time may be obtained by filing a petition accompanied by the extension fee under the provisions of 37 CFR 1.136(a).

- The oath or declaration is missing. *A properly signed oath or declaration in compliance with 37 CFR 1.63, identifying the application by the above Application Number and Filing Date, is required.*
  Note: If a petition under 37 CFR 1.47 is being filed, an oath or declaration in compliance with 37 CFR 1.63 signed by all available joint inventors, or if no inventor is available by a party with sufficient proprietary interest, is required.

The applicant needs to satisfy supplemental fees problems indicated below.

The required item(s) identified below must be timely submitted to avoid abandonment:

- To avoid abandonment, a surcharge (for late submission of filing fee, search fee, examination fee or oath or declaration) as set forth in 37 CFR 1.16(f) of $130 for a non-small entity, must be submitted with the missing items identified in this letter.

SUMMARY OF FEES DUE:

Total additional fee(s) required for this application is **$130** for a Large Entity

- **$130** Surcharge.

Replies should be mailed to: Mail Stop Missing Parts

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Alexandria VA 22313-1450

A copy of this notice MUST be returned with the reply.

Office of Initial Patent Examination (571) 272-4000, or 1-800-PTO-9199, or 1-800-972-6382
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UTILITY PATENT APPLICATION TRANSMITTAL

(Only for new nonprovisional applications under 37 CFR 1.53(b))

Attorney Docket No.	T3653-9285US01
First Named Inventor	TZANNES, MARCOS C.
Title	SHARING MEMORY AND PROCESSING RESOURCES IN DSL SYSTEMS
Express Mail Label No.	

112975 U.S.PTO
11/246163
101105

APPLICATION ELEMENTS

See *MPEP chapter 600 concerning utility patent application contents.*

1. ☒ **Fee Transmittal Form** (e.g., PTO/SB/17)
   (Submit an original and a duplicate for fee processing)
2. ☐ **Applicant claims small entity status**
   See 37 CFR 1.27
3. ☒ **Specification** *[Total Pages 30]*
   Both the claims and abstract must start on a new page
   (For information on the preferred arrangement, see MPEP 608.01(a))
4. ☒ **Drawing(s)** *(35 U.S.C. 113)* *[Total Sheets 3]*
5. **Oath or Declaration** *[Total Sheets _____]*
   a. ☐ Newly executed (original or copy)
   b. ☐ Unexecuted (original or copy)
   c. ☐ A copy from a prior application (37 CFR 1.63(d))
   (for continuation/divisional with Box 18 completed)
   i. ☐ DELETION OF INVENTOR(S)
   Signed statement attached deleting inventor(s) named in the prior application, see 37 CFR 1.63(d)(2) and 1.33(b)
6. ☒ **Application Data Sheet.** See 37 CFR 1.76
7. ☐ **CD-ROM or CD-R** in duplicate, large table or Computer Program (Appendix)
   ☐ Landscape Table on CD
8. **Nucleotide and/or Amino Acid Sequence Submission**
   (if applicable, items a.-c. are required
   a. ☐ Computer Readable Form (CRF)
   b. Specification Sequence Listing on:
   i ☐ CD-ROM or CD-R (2 copies; or
   ii. ☐ Paper
   c. ☐ Statements verifying identity of above copies

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Alexandria, VA 22313-1450

ACCOMPANYING APPLICATION PARTS

9. ☐ **Assignment Papers** (cover sheet & document(s))
   Name of Assignee _____
10. ☐ **37 CFR 3.73(b) Statement** ☐ **Power of Attorney**
    (when there is an assignee)
11. ☐ **English Translation Document** *(if applicable)*
12. ☐ **Information Disclosure Statement** (PTO/SB/08 or PTO-1449)
    ☐ Copies of citations enclosed
13. ☐ **Preliminary Amendment**
14. ☒ **Return Receipt Postcard** (MPEP 503)
    (Should be specifically itemized)
15. ☐ **Certified Copy of Priority Document(s)**
    (if foreign priority is claimed)
16. ☐ **Nonpublication Request** under 35 U.S.C. 122(b)(2)(B)(i).
    Applicant must attach form PTO/SB/35 or equivalent
17. ☐ Other: _____

18. If a CONTINUING APPLICATION, *check appropriate box, and supply the requisite information below and in the first sentence of the specification following the title, or in an Application Data Sheet under 37 CFR 1.76:*
☐ Continuation ☐ Divisional ☐ Continuation-in-part (CIP) of prior application No.: 60/618,269

Prior application information: Examiner _____ Art Unit: _____

19. CORRESPONDENCE ADDRESS

☒ The address associated with Customer Number: *000181* or ☐ *Correspondence address below*

Name					
City		State		Zip Code	
Country		Telephone		Fax	

Signature		Date	October 11, 2005
Name (Print/Type)	Jason H. Vick	Registration No. (Attorney/Agent)	45,285

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FEE TRANSMITTAL For FY 2005

Patent fees are subject to annual revision.

☐ Applicant claims small entity status. See 37 CFR 1.27

TOTAL AMOUNT OF PAYMENT	$2,650.00

Complete if Known	
Application Number	
Filing Date	
First Named Inventor	TZANNES, MARCOS C.
Examiner Name	
Art Unit	
Attorney Docket No.	T3653-9285US01

METHOD OF PAYMENT *(check all that apply)*

☒ Check ☐ Credit Card ☐ Money Order ☐ None ☐ Other (please identify):_____

☒ Deposit Account Deposit Account Number: 50-1165 Deposit Account Name: Miles & Stockbridge P.C.

For the above-identified deposit account, the Director is hereby authorized to: (check all that apply)

☐ Charge fee(s) indicated below ☐ Charge fee(s) indicated below, **except for the filing fee**

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FEE CALCULATION

1. BASIC FILING, SEARCH, AND EXAMINATION FEES

	FILING FEES		SEARCH FEES		EXAMINATION FEES		
		Small Entity		Small Entity		Small Entity	
Application Type	Fee ($)	Fee ($)	Fee ($)	Fee ($)	Fee ($)	Fee ($)	Fees Paid ($)
Utility	300	150	500	250	200	100	$1,000.00
Design	200	100	100	50	130	65	
Plant	200	100	300	150	160	80	
Reissue	300	150	500	250	600	300	
Provisional	200	100	0	0	0	0	

2. EXCESS CLAIM FEES

Fee Description	Fee ($)	Small Entity Fee ($)
Each claim over 20 (including Reissues)	50	25
Each independent claim over 3 (including Reissues)	200	100
Multiple dependent claims	360	180

Total Claims	Extra Claims	Fee ($)	Fee Paid ($)
45 - 20 or HP =	25	x 50.00	= $1250.00

HP = highest number of total claims paid for, if greater than 20.

Indep. Claims	Extra Claims	Fee ($)	Fee Paid ($)
5 - 3 or HP =	2	x 200.00	= $400.00

HP = highest number of independent claims paid for, if greater than 3.

Multiple Dependent Claims

3. APPLICATION SIZE FEE

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Total Sheets	Extra Sheets	Number of each additional 50 or fraction thereof	Fee ($)	Fee Paid ($)
_____ - 100 =	_____ / 50 =	_____ (round up to a whole number) x	_____	= _____

4. OTHER FEE(S)

Fee Paid ($)

Non-English Specification, $130 fee (no small entity discount) _____

Other (e.g., late filing surcharge): _____ _____

SUBMITTED BY				Complete *(if applicable)*	
Signature		Registration No. *(Attorney/Agent)*	45,285	Telephone	(703) 903-9000
Name *(Print/Type)*	Jason H. Vick			Date	October 11, 2005

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   c. ☐ Statements verifying identity of above copies

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☐ Continuation ☐ Divisional ☐ Continuation-in-part (CIP) of prior application No.: 60/618,269

Prior application information: Examiner _____ Art Unit: _____

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Name					
City		State		Zip Code	
Country		Telephone		Fax	

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Name (Print/Type)	Jason H. Vick	Registration No. (Attorney/Agent)	45,285

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Application Number	
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First Named Inventor	TZANNES, MARCOS C.
Examiner Name	
Art Unit	
Attorney Docket No.	T3653-9285US01

METHOD OF PAYMENT *(check all that apply)*

☒ Check ☐ Credit Card ☐ Money Order ☐ None ☐ Other (please identify):_____

☒ Deposit Account Deposit Account Number: 50-1165 Deposit Account Name: Miles & Stockbridge P.C.

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Fee Paid ($)

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Other (e.g., late filing surcharge): _____ _____

SUBMITTED BY				Complete *(if applicable)*	
Signature		Registration No. *(Attorney/Agent)*	45,285	Telephone	(703) 903-9000
Name *(Print/Type)*	Jason H. Vick			Date	October 11, 2005

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RESOURCE SHARING IN A TELECOMMUNICATIONS ENVIRONMENT

RELATED APPLICATION DATA

[0001] This application claims the benefit of and priority under 35 U.S.C. § 119(e) to U.S. Patent Application No. 60/618,269, filed October 12, 2004, entitled "Sharing Memory and Processing Resources in DSL Systems," which is incorporated herein by reference in its entirety.

BACKGROUND

Field of the Invention

[0002] This invention generally relates to communication systems. More specifically, an exemplary embodiment of this invention relates to memory sharing in communication systems. Another exemplary embodiment relates to processing or coding resource sharing in a communication system.

Description of Related Art

[0003] U.S. Patent Nos. 6,775,320 and 6,778,589, which are both incorporated herein by reference in their entirety, describe DSL systems supporting multiple applications and multiple framer/coder/interleaver FCI blocks (an FCI block is also referred to as a latency path). DSL systems carry applications that have different transmission requirements with regard to, for example, data rate, latency (delay), bit error rate (BER), and the like. For example, video typically requires a low BER (<1E-10) but can tolerate higher latency (>20 ms). Voice, on the other hand, typically requires a low latency (<1 ms) but can tolerate BER (>1E-3).

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[0004] As described in U.S. Patent No. 6,775,320, different applications can use different latency paths in order to satisfy the different application requirements of the communication system. As a result a transceiver must support multiple latency paths in order to support applications such as video, Internet access and voice telephony. When implemented in a transceiver, each of the latency paths will have a framer, coder, and interleaver block with different capabilities that depend on the application requirements.

SUMMARY

[0005] One difficulty with implementing multiple latency paths in a transceiver is the fact that a latency path is a complicated digital circuit that requires a large amount of memory and processing power. An interleaver within a latency path can consume a large amount of memory in order to provide error correcting capability. For example, a typical DSL transceiver will have at least one latency path with approximately 16 kbytes of memory for the interleaver. Likewise, the coding block, for example, a Reed Solomon coder, consumes a large amount of processing power. In general, as the number of latency paths increase, the memory and processing power requirements for a communication system become larger.

[0006] Accordingly, an exemplary aspect of this invention relates to sharing memory between one or more interleavers and/or deinterlaevers in a transceiver. More particularly, an exemplary aspect of this invention relates to shared latency path memory in a transceiver.

[0007] Additional aspects of this invention relate to configuring and initializing shared memory in a communication system. More particularly, an exemplary aspect of this invention relates to configuring and initializing interleaver/deinterleaver memory in a communication system.

[0008] Additional aspects of the invention relate to determining the amount of memory that can be allocated to a particular component by a communication system. More specifically, an exemplary aspect of the invention relates to determining the maximum amount of shared memory that can be allocated to one or more interleaves or deinterleavers.

[0009] According to another exemplary aspect of the invention, processing power is shared between a number of transceiver modules. More specifically, and in accordance with an exemplary embodiment of the invention, a coding module is shared between one or more coders and/or decoders.

[0010] Another exemplary embodiment of the invention relates to transitioning from a fixed memory configuration to a shared memory configuration during one or more of initialization and SHOWTIME (user data transmission).

[0011] An additional exemplary aspect of the invention relates to dynamically updating one or more of shared memory and processing resources based on changing communication conditions.

[0012] An additional exemplary aspect of the invention relates to updating one or more of shared memory and processing resources based on an updated communication parameter.

[0013] An additional exemplary aspect of the invention relates to updating the allocation of one or more of shared memory and processing resources based on an updated communication parameter(s).

[0014] Additional aspects of the invention relate to exchanging shared resource allocations between transceivers.

[0015] Additional exemplary aspects relate to a method of allocating shared memory in a transceiver comprising allocating the shared memory to a plurality of modules, wherein each of the plurality of modules comprise at least one interleaver, at least one deinterleaver or a combination thereof.

[0016] Still further aspects relate to the above method wherein the plurality of modules comprise interleavers.

[0017] Still further aspects relate to the above method wherein the plurality of modules comprise deinterleavers.

[0018] Still further aspects relate to the above method wherein the plurality of modules comprise at least one interleaver and at least one deinterleaver.

[0019] Additional exemplary aspects relate to a transceiver comprising a plurality of modules each including at least one interleaver, at least one deinterleaver or a

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combination thereof and a shared memory designed to be allocated to a plurality of the modules.

[0020] Still further aspects relate to the above transceiver wherein the plurality of modules comprise interleavers.

[0021] Still further aspects relate to the above transceiver wherein the plurality of modules comprise deinterleavers.

[0022] Still further aspects relate to the above transceiver wherein the plurality of modules comprise at least one interleaver and at least one deinterleaver.

[0023] These and other features and advantages of this invention are described in, or are apparent from, the following description of the embodiments.

BRIEF DESCRIPTION OF THE DRAWINGS

[0024] The embodiments of the invention will be described in detail, with reference to the following figures, wherein:

[0025] Fig. 1 is a functional block diagram illustrating an exemplary transceiver according to this invention;

[0026] Fig. 2 is a flowchart outlining an exemplary method of sharing resources according to this invention;

[0027] Fig. 3 is a flowchart outlining an exemplary method of determining a maximum amount of shared memory according to this invention; and

[0028] Fig. 4 is a flowchart outlining an exemplary resource sharing methodology according to this invention.

DETAILED DESCRIPTION

[0029] The exemplary embodiments of this invention will be described in relation to sharing resources in a wired and/or wireless communications environment. However, it should be appreciated, that in general, the systems and methods of this invention will work equally well for any type of communication system in any environment.

[0030] The exemplary systems and methods of this invention will also be described in relation to multicarrier modems, such as DSL modems and VDSL modems, and associated communication hardware, software and communication channels. However, to avoid unnecessarily obscuring the present invention, the following description omits well-known structures and devices that may be shown in block diagram form or otherwise summarized.

[0031] For purposes of explanation, numerous details are set forth in order to provide a thorough understanding of the present invention. It should be appreciated however that the present invention may be practiced in a variety of ways beyond the specific details set forth herein.

[0032] Furthermore, while the exemplary embodiments illustrated herein show the various components of the system collocated, it is to be appreciated that the various components of the system can be located at distant portions of a distributed

network, such as a telecommunications network and/or the Internet, or within a dedicated secure, unsecured and/or encrypted system. Thus, it should be appreciated that the components of the system can be combined into one or more devices, such as a modem, or collocated on a particular node of a distributed network, such as a telecommunications network. As will be appreciated from the following description, and for reasons of computational efficiency, the components of the system can be arranged at any location within a distributed network without affecting the operation of the system. For example, the various components can be located in a Central Office modem (CO, ATU-C, VTU-O), a Customer Premises modem (CPE, ATU-R, VTU-R), a DSL management device, or some combination thereof. Similarly, one or more functional portions of the system could be distributed between a modem and an associated computing device.

[0033] Furthermore, it should be appreciated that the various links, including communications channel 5, connecting the elements can be wired or wireless links, or any combination thereof, or any other known or later developed element(s) that is capable of supplying and/or communicating data to and from the connected elements. The term module as used herein can refer to any known or later developed hardware, software, firmware, or combination thereof that is capable of performing the functionality associated with that element. The terms determine, calculate and compute, and variations thereof, as used herein are used interchangeably and include any type of methodology, process, mathematical operation or technique. FCI block and latency path are used interchangeably herein as well as transmitting modem and transmitting transceiver. Receiving modem and receiving transceiver are also used

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Page 500 of 531

interchangeably.

[0034] Fig. 1 illustrates an exemplary embodiment of a transceiver 100 that utilizes shared resources. It should be appreciated that numerous functional components of the transceiver have been omitted for clarity. However, the transceiver 100 can also include the standard components found in typical communications device(s) in which the technology of the subject invention is implemented into.

[0035] According to an exemplary embodiment of the invention, memory and processing power can be shared among a plurality of transmitter and/or receiver latency paths, in a communications transceiver that carries or supports multiple applications. For example, the transmitter and/or receiver latency paths of the transceiver can share an interleaver/deinterleaver memory and the shared memory can be allocated to the interleaver and/or deinterleaver of each latency path. This allocation can be done based on the data rate, latency, BER, impulse noise protection requirements of the application, data or information being transported over each latency path, or in general any parameter associated with the communications system.

[0036] Likewise, for example, the transmitter and/or receiver latency paths can share a Reed-Solomon coder/decoder processing module and the processing power of this module can be allocated to each encoder and/or decoder. This allocation can be done based on the data rate/latency, BER, impulse noise protection requirements of the application data or information being transported over each latency path, or in general based on any parameter associated with the communication system.

[0037] In accordance with an exemplary operational embodiment, a first transceiver and a second transceiver transmit to one another messages during, for example, initialization which contain information on the total and/or shared memory capabilities of each transceiver and optionally information about the one or more latency paths. This information can be transmitted prior to determining how to configure the latency paths to support the application requirements. Based on this information, one of the modems can select an FCI configuration parameter(s) that meets the transmission requirements of each application being transported over each latency paths. While an exemplary of the embodiment of the invention will be described in relation to the operation of the invention and characteristics thereof being established during initialization, it should be appreciated that the sharing of resources can be modified and messages transmitted between a two transceivers at any time during initialization and/or user data transmission, i.e., SHOWTIME.

[0038] Fig. 1 illustrates an exemplary embodiment of a transceiver 100. The transceiver 100 includes a transmitter portion 200 and a receiver portion 300. The transmitter portion 200 includes one or more latency paths 210, 220, ... Similarly, the receiver portion 300 includes one or more latency paths 310, 320, ... Each of the latency paths in the transmitter portion 200 includes a framer, coder, and interleaver designated as 212, 214, 216 and 222, 224 and 226, respectively. Each of the latency paths in the receiver portion includes a deframer, decoder, and deinterleaver designated as 312, 314, 316 and 322, 324, and 326, respectively. The transceiver 100 further includes a shared processing module 110, a shared memory 120, a parameter

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determination module 130, a path module 140, an allocation module 150, and a shared resource management module 160, all interconnected by one or more links (not shown).

[0039] In this exemplary embodiment, the transceiver 100 is illustrated with four total transmitter portion and receiver portion latency paths, i.e., 210, 220, 310, and 320. The shared memory 120 is shared amongst the two transmitter portion interleavers 216 and 226 and two receiver portion deinterleavers 316 and 326. The shared processing module 110, such as a shared coding module, is shared between the two transmitter portion coders 214 and 224 and the two receiver portion decoders 314 and 324.

[0040] While the exemplary embodiment of the invention will be described in relation to a transceiver having a number of transmitter portion latency paths and receiver portion latency paths, it should be appreciated that this invention can be applied to any transceiver having any number of latency paths. Moreover, it should be appreciated that the sharing of resources can be allocated such that one or more of the transmitter portion latency paths are sharing a shared resource, one or more of the receiver portion latency paths are sharing a shared resource, or a portion of the transmitter portion latency paths and a portion of the receiver portion latency paths are sharing shared resources. Moreover, any one or more of the latency paths, or portions thereof, could also be assigned to a fixed resource while, for example, another portion of the latency path(s) assigned to a shared resource. For example, in latency path 210, the interleaver 216 could be allocated a portion of the shared

memory 120, while the coder 214 could be allocated to a dedicated processing module, vice versa, or the like.

[0041] In accordance with the exemplary embodiment, a plurality of transmitter portion or receiver portion latency paths share an interleaver/deinterleaver memory, such as shared memory 120, and a coding module, such as shared processing module 110. For example, the interleaver/deinterleaver memory can be allocated to different interleavers and/or deinterleavers. This allocation can be based on parameters associated with the communication systems such as data rate, latency, BER, impulse noise protection, and the like, of the applications being transported. Similarly, a coding module, which can be a portion of the shared processing module 110, can be shared between any one or more of the latency paths. This sharing can be based on requirements such as data rate, latency, BER, impulse noise protection, and the like, of the applications being transported.

[0042] For example, an exemplary transceiver could comprise a shared interleaver/deinterleaver memory and could be designed to allocate a first portion of the shared memory 120 to an interleaver, such as interleaver 216 in the transmitter portion of the transceiver and allocate a second portion of the shared memory 120 to a deinterleaver, such as 316, in the receiver portion of the transceiver.

[0043] Alternatively, for example, an exemplary transceiver can comprise a shared interleaver/deinterleaver memory, such as shared memory 120, and be designed to allocate a first portion of shared memory 120 to a first interleaver, e.g.,

216, in the transmitter portion of the transceiver and allocate a second portion of the shared memory to a second interleaver, e.g., 226, in the transmitter portion of the transceiver.

[0044] Alternatively, for example, an exemplary transceiver can comprise a shared interleaver/deinterleaver memory and be designed to allocate a first portion of the shared memory 120 to a first deinterleaver, e.g., 316, in the receiver portion of the transceiver and allocate a second portion of the shared memory to a second deinterleaver, e.g., 326, in the receiver portion of the transceiver. Regardless of the configuration, in general any interleaver or deinterleaver, or grouping thereof, be it in a transmitter portion or receiver portion of the transceiver, can be associated with a portion of the shared memory 120.

[0045] Establishment, configuration and usage of shared resources is performed in the following exemplary manner. First, and in cooperation with the path module 140, the number of transmitter and receiver latency paths (N) is determined. The parameter determination module 130 then analyses one or more parameters such as data rate, transmitter data rate, receiver data rate, impulse noise protection, bit error rate, latency, or the like. Based on one or more of these parameters, the allocation module 150 allocates a portion of the shared memory 120 to one or more of the interleaver and/or deinterleavers, or groupings thereof. This process continues until the memory allocation has been determined and assigned to each of the N latency paths.

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[0046] Having determined the memory allocation for each of the latency paths, and in conjunction with the shared resource management 160, the transceiver 100 transmits to a second transceiver one or more of the number of latency paths (N), the maximum interleaver memory for any one or more of the latency paths and/or the maximum total and/or shared memory for all of the latency paths.

[0047] Three examples of sharing interleaver/deinterleaver memory and coding processing in a transceiver are described below. The latency paths in these examples can be in the transmitter portion of the transceiver or the receiver portion of the transceiver.

[0048] Example #1

A first transmitter portion or receiver portion latency path may carry data from a video application, which needs a very low BER but can tolerate higher latency. In this case, the video will be transported using an latency path that has a large amount of interleaving/deinterleaving and coding (also known as Forward Error Correction (FEC) coding). For example, the latency path may be configured with Reed-Solomon coding using a codeword size of 255 bytes (N=255) with 16 checkbytes (R=16) and interleaving/deinterleaving using an interleaver depth of 64 (D=64). This latency path will require N*D=16*255=16Kbytes of interleaver memory at the transmitter (or de-interleaver memory at the receiver). This latency path will be able to correct a burst of errors that is less than 512 bytes in duration.

[0049] A second transmitter portion or receiver portion latency path may carry an

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internet access application that requires a medium BER and a medium amount of latency. In this case, the internet access application will be transported using a latency path that has a medium amount of interleaving and coding. For example, the latency path may be configured with Reed-Solomon coding using a codeword size of 128 bytes (N=128) with 8 checkbytes (R=8) and interleaving using an interleaver depth of 16 (D=32). This latency path will require N*D=128*32=4Kbytes of interleaver memory and the same amount of deinterleaver memory. This latency path will be able to correct a burst of errors that is less than 128 bytes in duration.

[0050] A third transmitter portion or receiver portion latency path may carry a voice telephony application, which needs a very low latency but can tolerate BER. In this case, the video will be transported using an latency path that has a large amount of interleaving and coding. For example, the third transmitter portion or receiver portion latency path may be configured with no interleaving or coding which will result in the lowest possible latency through the latency path but will provide no error correction capability.

[0051] According to the principles of this invention, a system carrying the three applications described above in Example #1, would have three latency paths that share one memory space containing at least (16+4)=20 Kbytes. The three latency paths also share a common coding block that is able to simultaneously encode (in the transmitter portion) or decode (in a receiver portion) two codewords with N=255/R=16 and N=128/R=8.

[0052] According to an exemplary embodiment of this invention, the latency paths can be reconfigured at initialization or during data transmission mode (also known as SHOWTIME in ADSL and VDSL transceivers). This would occur if, for example, the applications or application requirements were to change.

[0053] Example #2

If instead of 1 video application, 1 internet application and 1 voice application, there were 3 internet access applications then the transmitter portion and/or receiver portion latency paths would be reconfigured to utilize the shared memory and coding module in a different way. For example, the system could be reconfigured to have 3 transmitter portion or receiver portion latency paths, with each latency path being configured with Reed-Solomon coding using a codeword size of 128 bytes (N=128) with 8 checkbytes (R=8) and interleaving using an interleaver depth of 16 (D=32). Each latency path will require N*D=128*32=4Kbytes of interleaver memory and each block will be able to correct a burst of errors that is less than 128 bytes in duration. Based on the example of carrying the three internet access applications described, the three latency path share one memory space containing at least 3*4=12 Kbytes. Also the three latency paths share a common coding block that is able to simultaneously encode (on the transmitter side) or decode (on the receiver side) three codewords with N=128/R=16, N=128/R=8 and N=128/R=8.

[0054] Example #3

The system could be configured to carry yet another set of applications. For example, the latency paths could be configured to carry 2 video applications. In this case only

2 transmitter portion or receiver portion latency paths are needed, which means that the third latency path could be simply disabled. Also, assuming that the memory is constrained based on the first example above, then the maximum shared memory for these 2 latency paths is 20 kBytes. In this case, the system could be reconfigured to have 2 latency paths, with each block being configured with Reed-Solomon coding using a codeword size of 200 bytes (N=200) with 10 checkbytes (R=10) and interleaving/deinterleaving using an interleaver depth of 50 (D=50). Each latency path will require N*D=200*50=10Kbytes of interleaver memory and each block will be able to correct a burst of errors that is less than 250 bytes in duration. This configuration results in 20K of shared memory for both latency paths, which is the same as in the first example. In order to stay within the memory constraints of the latency paths, the error correction capability for each latency path is decreased to 250 bytes from 512 bytes in Example #1.

[0055] Another aspect of this invention is the how FCI configuration information is transmitted between a first modem and a second modem. FCI configuration information will depend on the requirements of the applications being transported over the DSL connection. This information may need to be forwarded during initialization in order to initially configure the DSL connection. This information may also need to be forwarded during SHOWTIME in order to reconfigure the DSL connection based on a change in applications or the application requirements.

[0056] According to one embodiment, a first modem determines the specific FCI configuration parameters, e.g,. N, D, R as defined above, needed to meet specific

application requirements, such as latency, burst error correction capability, etc. In order to determine the FCI configuration parameters, the first modem must know what are the capabilities of a second modem. For example, the first modem must know how many latency paths (FCI blocks) the second modem can support. Also the first modem must know the maximum amount of interleaver memory for each transmitter latency path. In addition, since the transmitter latency paths may share a common memory space the first modem must know the total shared memory for all transmitter latency paths. This way the first modem will be able to choose a configuration that can meet application requirements and also meet the transmitter portion latency path capabilities of the second modem.

[0057] For example, using values from examples above, a first transceiver could send a message to a second transceiver during initialization or during SHOWTIME containing the following information:

- Number of supported transmitter and receiver latency paths = 3
- Max Interleaver Memory for latency path #1= 16 Kbytes
- Max Interleaver Memory for latency path #2= 16 Kbytes
- Max Interleaver Memory for latency path #3= 16 Kbytes
- Maximum total/shared memory for all latency paths = 20 kBytes

Based on this information, and the application requirements, the first transceiver would select latency path settings. For example, if the applications are 1 video, 1 internet access and 1 voice application, the first transceiver could configure 3 latency paths as follows:

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latency path #1 – Video: N=255, R=16, D=64

latency path #2 – Video: N=128, R=8, D=32

latency path #3 – Video: N=0, R=0, D=1 (no coding or interleaving)

[0058] This would result in a total interleaver memory of 20 kbytes.

[0059] Alternatively, if for example, there are only 2 video applications, the first transceiver could configure 2 latency paths as follows:

latency path #1 – Video: N=200, R=10, D=50

latency path #2 – Video: N=200, R=10, D=50

latency path #3 – Video: N=0, R=0, D=1 (no coding or interleaving)

[0060] This would also result in a total interleaver memory of 20 kbytes.

[0061] Alternatively, the second transceiver can determine the specific FCI configuration parameters, e.g., N, D, R as defined above, needed to meet specific application requirements, such as latency, burst error correction capability, etc. As described above for the first transceiver, in order to determine the FCI configuration parameters, the second transceiver must first know what are the capabilities of the first transceiver. In this case, the first transceiver would send a message to the second transceiver containing the information described above and based on this information and the application requirements the second transceiver would select latency path settings.

[0062] Fig. 2 outlines an exemplary method of allocating shared memory in a transceiver. More specifically, control begins in step S200 and continues to step S210. In step S210, one or more of shared interleaver/deinterleaver memory and/or shared coder/decoder processing resources are allocated to one or more latency paths, in a transceiver. Control then continues to step S220 where the control sequence ends.

[0063] Fig. 3 outlines an exemplary method of exchanging shared resource allocations according to an exemplary embodiment of this invention. In particular, control begins in step S310. In step S310, a maximum amount of shared memory that can be allocated to a specific interleaver or deinterleaver of a plurality of interleavers or deinterleavers in a transceiver is determined. Next, in step S320, the determined maximum amount for one or more of the deinterleavers and/or interleavers is transmitted to another transceiver. Messages containing additional information can also be transmitted to the other transceiver and/or received from the other transceiver. Control then continues to step S330 where the control sequence ends.

[0064] Fig. 4 outlines an exemplary procedure for resource sharing according to an exemplary embodiment of this invention. In particular, control begins in step S400 and continues to step S410. In step S410, the number of latency paths are determined. Then, in step S420, the latency path information (FCI block information) is transmitted to another transceiver. Messages containing additional information can also be transmitted to the other transceiver and/or received from the other transceiver. This information can be used to, for example, assist with the determination of

memory allocation in the transceiver. Moreover, the messages received from the other transceiver could specify what the memory allocation is to be based on, for example, the number of latency paths, memory allocation in the remote transceiver and required applications. Control then continues to step S430.

[0065] In step S430, and for each latency path, the steps in step 440 are performed.

[0066] In step S440, and while monitoring of allocation of resources is being performed, steps 450 and 460 are performed. More specifically, in step S450, one or more parameters associated with the communication system are determined. Then, in step S460, shared resources are allocated based on one or more of the communication parameters. Control then continues to step S470.

[0067] In step S470, the allocation of shared resources is communicated to another transceiver. Next, in step S480, a determination is made as to whether there is a change in communications that would require the adjustment of the shared resource allocation. Examples of changes in communications conditions include a change in applications being transported over the system and/or changes in the channel condition, etc. If adjustments are required, control jumps back to step S410. Otherwise, control jumps to step S490 where the control sequence ends.

[0068] The above-described system can be implemented on wired and/or wireless telecommunications devices, such a modem, a multicarrier modem, a DSL modem, an

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ADSL modem, an XDSL modem, a VDSL modem, a linecard, test equipment, a multicarrier transceiver, a wired and/or wireless wide/local area network system, a satellite communication system, a modem equipped with diagnostic capabilities, or the like, or on a separate programmed general purpose computer having a communications device or in conjunction with any of the following communications protocols: CDSL, ADSL2, ADSL2+, VDSL1, VDSL2, HDSL, DSL Lite, IDSL, RADSL, SDSL, UDSL or the like.

[0069] Additionally, the systems, methods and protocols of this invention can be implemented on a special purpose computer, a programmed microprocessor or microcontroller and peripheral integrated circuit element(s), an ASIC or other integrated circuit, a digital signal processor, a hard-wired electronic or logic circuit such as discrete element circuit, a programmable logic device such as PLD, PLA, FPGA, PAL, a modem, a transmitter/receiver, any comparable means, or the like. In general, any device capable of implementing a state machine that is in turn capable of implementing the methodology illustrated herein can be used to implement the various communication methods, protocols and techniques according to this invention.

[0070] Furthermore, the disclosed methods may be readily implemented in software using object or object-oriented software development environments that provide portable source code that can be used on a variety of computer or workstation platforms. Alternatively, the disclosed system may be implemented partially or fully in hardware using standard logic circuits or VLSI design. Whether software or

hardware is used to implement the systems in accordance with this invention is dependent on the speed and/or efficiency requirements of the system, the particular function, and the particular software or hardware systems or microprocessor or microcomputer systems being utilized. The communication systems, methods and protocols illustrated herein can be readily implemented in hardware and/or software using any known or later developed systems or structures, devices and/or software by those of ordinary skill in the applicable art from the functional description provided herein and with a general basic knowledge of the computer and telecommunications arts.

[0071] Moreover, the disclosed methods may be readily implemented in software that can be stored on a storage medium, executed on programmed general-purpose computer with the cooperation of a controller and memory, a special purpose computer, a microprocessor, or the like. In these instances, the systems and methods of this invention can be implemented as program embedded on personal computer such as an applet, JAVA® or CGI script, as a resource residing on a server or computer workstation, as a routine embedded in a dedicated communication system or system component, or the like. The system can also be implemented by physically incorporating the system and/or method into a software and/or hardware system, such as the hardware and software systems of a communications transceiver.

[0072] It is therefore apparent that there has been provided, in accordance with the present invention, systems and methods for sharing resources. While this invention has been described in conjunction with a number of embodiments, it is

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evident that many alternatives, modifications and variations would be or are apparent to those of ordinary skill in the applicable arts. Accordingly, it is intended to embrace all such alternatives, modifications, equivalents and variations that are within the spirit and scope of this invention.

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Claims:

1. A method for sharing resources in a transceiver comprising:

allocating a first portion of shared memory to a first latency path and allocating a second portion of the shared memory to a second latency path.

2. The method of claim 1, wherein the first latency path includes an interleaver and the second latency path includes an interleaver.

3. The method of claim 1, wherein the first latency path includes an interleaver and the second latency path includes a deinterleaver.

4. The method of claim 1, wherein the first latency path includes a deinterleaver and the second latency path includes a deinterleaver.

5. The method of claim 1, further comprising transmitting to another transceiver information that is used to determine a maximum amount of shared memory that can be allocated.

6. The method of claim 1, further comprising receiving from another transceiver information that is used to determine a maximum amount of shared memory that can be allocated.

7. The method of claim 1, further comprising allocating a shared processing module to a plurality of coding and/or decoding modules.

8. The method of claim 1, wherein the allocating of at least one portion of the shared memory is based on one or more communication parameters.

9. The method of claim 8, wherein at least one of the communication parameters is a data rate, a latency, an INP value or a bit error rate (BER).

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10. A transceiver comprising:

a first portion of shared memory that is allocated to a first latency path; and

a second portion of the shared memory that is allocated to a second latency path.

11. The transceiver of claim 10, further comprising:

an allocation module designed to allocate the shared memory based on one or more communication parameters.

12. The transceiver of claim 11, wherein at least one of the communication parameters is a data rate, a latency, an INP value or a Bit Error Rate (BER).

13. The transceiver of claim 10, wherein the first latency path includes an interleaver and the second latency path includes an interleaver.

14. The transceiver of claim 10, wherein the first latency path includes an interleaver and the second latency path includes a deinterleaver.

15. The transceiver of claim 10, wherein the first latency path includes a deinterleaver and the second latency path includes a deinterleaver.

16. The transceiver of claim 10, further comprising a shared resource management module designed to determine information that is transmitted to another transceiver, wherein the information is used to determine a maximum amount of shared memory that can be allocated.

17. The transceiver of claim 10, further comprising a shared resource management module designed to utilize information that is received from another transceiver, wherein the information is used to determine a maximum amount of shared memory that can be allocated.

18. The transceiver of claim 10, further comprising a shared processing module designed to provide processing resources to a plurality of coding and/or decoding modules.

19. A system for sharing resources in a transceiver comprising:

means for allocating a first portion of shared memory to a first latency path and means for allocating a second portion of the shared memory to a second latency path.

20. The system of claim 19, wherein the first latency path includes an interleaver and the second latency path includes an interleaver.

21. The system of claim 19, wherein the first latency path includes an interleaver and the second latency path includes a deinterleaver.

22. The system of claim 19, wherein the first latency path includes a deinterleaver and the second latency path includes a deinterleaver.

23. The system of claim 19, further comprising means for transmitting to another transceiver information that is used to determine a maximum amount of shared memory that can be allocated.

24. The system of claim 19, further comprising means for receiving from another transceiver information that is used to determine a maximum amount of shared memory that can be allocated.

25. The system of claim 19, further comprising means for allocating a shared processing module to a plurality of coding and/or decoding modules.

26. The system of claim 19, wherein the allocating of at least one portion

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of the shared memory is based on one or more communication parameters.

27. The system of claim 26, wherein at least one of the communication parameters is a data rate, a latency, an INP value or a bit error rate (BER).

28. A protocol for sharing resources in a transceiver comprising:

allocating a first portion of shared memory to a first latency path and allocating a second portion of the shared memory to a second latency path.

29. The protocol of claim 28, wherein the first latency path includes an interleaver and the second latency path includes an interleaver.

30. The protocol of claim 28, wherein the first latency path includes an interleaver and the second latency path includes a deinterleaver.

31. The protocol of claim 28, wherein the first latency path includes a deinterleaver and the second latency path includes a deinterleaver.

32. The protocol of claim 28, further comprising transmitting to another transceiver information that is used to determine a maximum amount of shared memory that can be allocated.

33. The protocol of claim 28, further comprising receiving from another transceiver information that is used to determine a maximum amount of shared memory that can be allocated.

34. The protocol of claim 28, further comprising allocating a shared processing module to a plurality of coding and/or decoding modules.

35. The protocol of claim 28, wherein the allocating of at least one portion of the shared memory is based on one or more communication parameters.

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36. The protocol of claim 35, wherein at least one of the communication parameters is a data rate, a latency, an INP value or a bit error rate (BER).

37. An information storage media having stored thereon information that when executed allows sharing of resources in a transceiver comprising:

information that allocates a first portion of shared memory to a first latency path and information that allocates a second portion of the shared memory to a second latency path.

38. The media of claim 37, wherein the first latency path includes an interleaver and the second latency path includes an interleaver.

39. The media of claim 37, wherein the first latency path includes an interleaver and the second latency path includes a deinterleaver.

40. The media of claim 37, wherein the first latency path includes a deinterleaver and the second latency path includes a deinterleaver.

41. The media of claim 37, further comprising information that transmits to another transceiver information that is used to determine a maximum amount of shared memory that can be allocated.

42. The media of claim 37, further comprising information that receives from another transceiver information that is used to determine a maximum amount of shared memory that can be allocated.

43. The media of claim 37, further comprising information that allocates a shared processing module to a plurality of coding and/or decoding modules.

44. The media of claim 37, wherein the allocating of at least one portion of

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the shared memory is based on one or more communication parameters.

45. The media of claim 44, wherein at least one of the communication parameters is a data rate, a latency, an INP value or a bit error rate (BER).

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ABSTRACT

A transceiver is designed to share memory and processing power amongst a plurality of transmitter and/or receiver latency paths, in a communications transceiver that carries or supports multiple applications. For example, the transmitter and/or receiver latency paths of the transceiver can share an interleaver/deinterleaver memory. This allocation can be done based on the data rate, latency, BER, impulse noise protection requirements of the application, data or information being transported over each latency path, or in general any parameter associated with the communications system.

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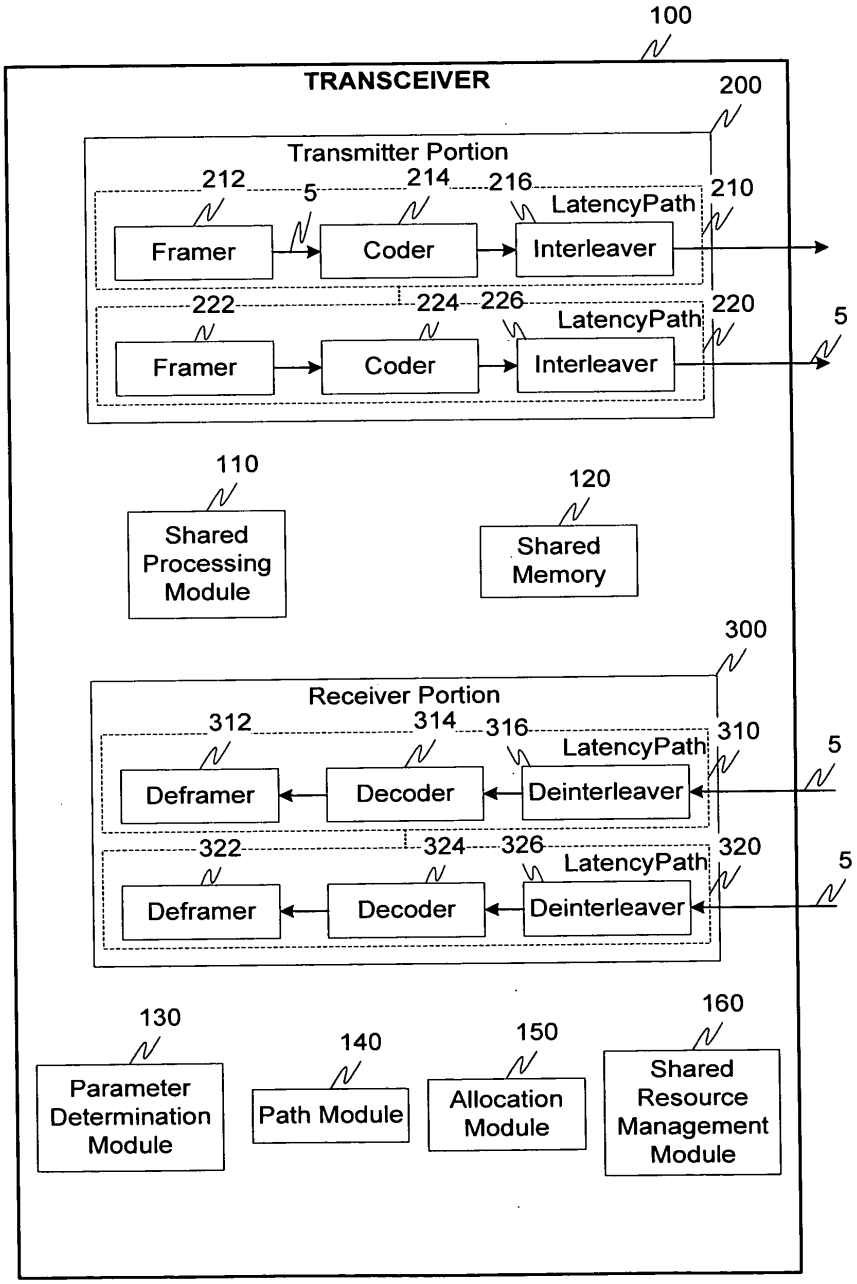
100
TRANSCEIVER
200
Transmitter Portion
212
5
214
216
LatencyPath
210
Framer
Coder
Interleaver
222
224
226
LatencyPath
220
5
Framer
Coder
Interleaver
110
Shared Processing Module
120
Shared Memory
300
Receiver Portion
312
314
316
LatencyPath
310
5
Deframer
Decoder
Deinterleaver
322
324
326
LatencyPath
320
5
Deframer
Decoder
Deinterleaver
130
Parameter Determination Module
140
Path Module
150
Allocation Module
160
Shared Resource Management Module

Fig. 1

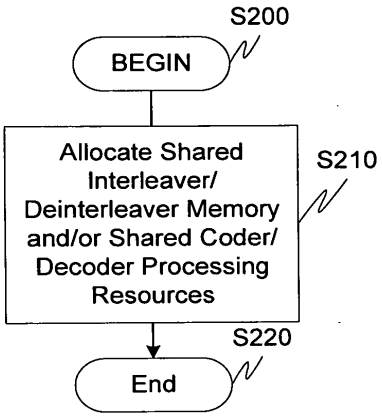
S200
BEGIN
Allocate Shared Interleaver/ Deinterleaver Memory and/or Shared Coder/ Decoder Processing Resources
S210
S220
End

Fig. 2

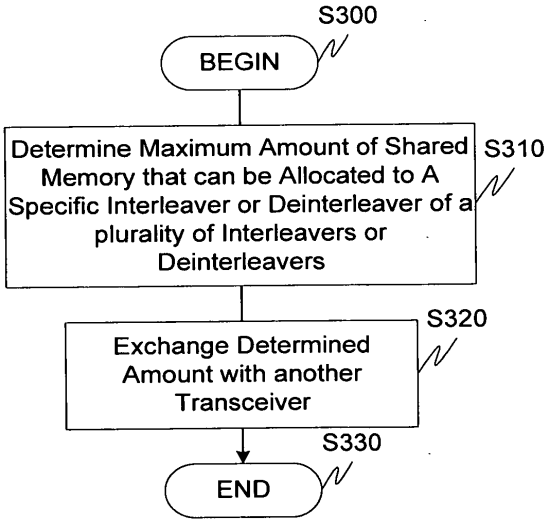
S300
BEGIN
Determine Maximum Amount of Shared Memory that can be Allocated to A Specific Interleaver or Deinterleaver of a plurality of Interleavers or Deinterleavers
S310
Exchange Determined Amount with another Transceiver
S320
S330
END

Fig. 3

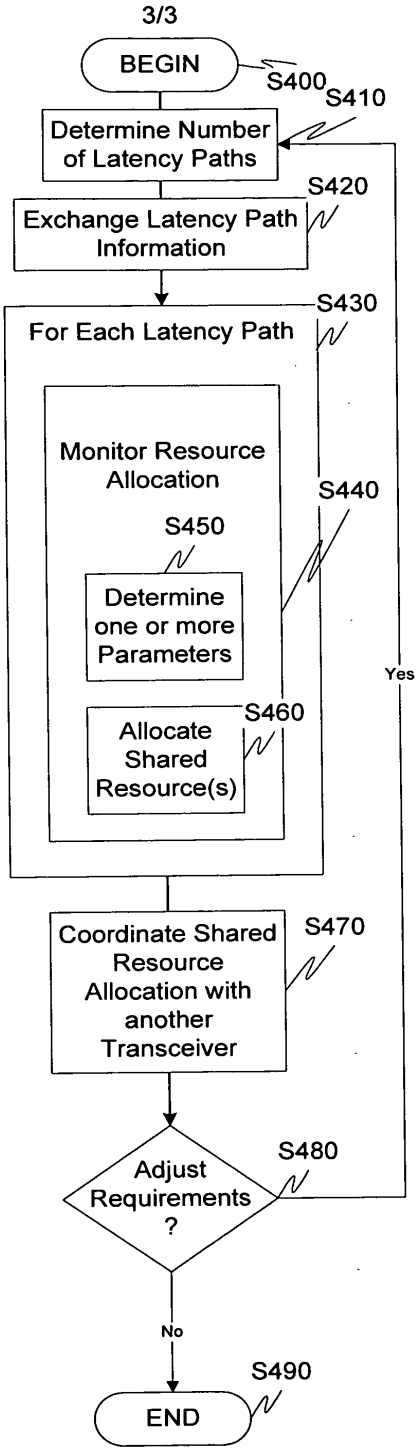
BEGIN
S400
S410
Determine Number of Latency Paths
S420
Exchange Latency Path Information
S430
For Each Latency Path
Monitor Resource Allocation
S440
S450
Determine one or more Parameters
S460
Allocate Shared Resource(s)
Yes
S470
Coordinate Shared Resource Allocation with another Transceiver
S480
Adjust Requirements ?
No
S490
END

Fig. 4

PATENT APPLICATION SERIAL NO _____

U.S. DEPARTMENT OF COMMERCE
PATENT AND TRADEMARK OFFICE
FEE RECORD SHEET

10/13/2005 DTESSEM1 00000080 11246163

01 FC:1011	300.00	OP
02 FC:1111	500.00	OP
03 FC:1311	200.00	OP
04 FC:1202	1250.00	OP
05 FC:1201	400.00	OP

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PATENT APPLICATION FEE DETERMINATION RECORD

Substitute for Form PTO-875 Effective December 8, 2004

Application or Docket Number: 11246163

APPLICATION AS FILED – PART I

FOR	(Column 1) NUMBER FILED	(Column 2) NUMBER EXTRA	SMALL ENTITY RATE ($)	SMALL ENTITY FEE ($)	OR	OTHER THAN SMALL ENTITY RATE ($)	OTHER THAN SMALL ENTITY FEE ($)
BASIC FEE (37 CFR 1.16(a), (b), or (c))	N/A	N/A	N/A	150.00		N/A	300.00
SEARCH FEE (37 CFR 1.16(k), (l), or (m))	N/A	N/A	N/A	$250		N/A	$500
EXAMINATION FEE (37 CFR 1.16(o), (p), or (q))	N/A	N/A	N/A	$100		N/A	$200
TOTAL CLAIMS (37 CFR 1.16(i))	45 minus 20 =	25	X$ 25 =		OR	X$50 =	1250
INDEPENDENT CLAIMS (37 CFR 1.16(h))	5 minus 3 =	2	X100 =			X200 =	400
APPLICATION SIZE FEE (37 CFR 1.16(s))	If the specification and drawings exceed 100 sheets of paper, the application size fee due is $250 ($125 for small entity) for each additional 50 sheets or fraction thereof. See 35 U.S.C. 41(a)(1)(G) and 37 CFR 1.16(s).						
MULTIPLE DEPENDENT CLAIM PRESENT (37 CFR 1.16(j))			+180=			+360=	
* If the difference in column 1 is less than zero, enter "0" in column 2.			TOTAL			TOTAL	2650

APPLICATION AS AMENDED – PART II

AMENDMENT A		(Column 1) CLAIMS REMAINING AFTER AMENDMENT		(Column 2) HIGHEST NUMBER PREVIOUSLY PAID FOR	(Column 3) PRESENT EXTRA	SMALL ENTITY RATE ($)	SMALL ENTITY ADDITIONAL FEE ($)	OR	OTHER THAN SMALL ENTITY RATE ($)	OTHER THAN SMALL ENTITY ADDITIONAL FEE ($)
	Total (37 CFR 1.16(i))	*	Minus	**	=	X$ 25 =		OR	X$50 =	
	Independent (37 CFR 1.16(h))	*	Minus	***	=	X100 =		OR	X200 =	
	Application Size Fee (37 CFR 1.16(s))									
	FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))					+180=		OR	+360=	
						TOTAL ADD'L FEE		OR	TOTAL ADD'L FEE	

AMENDMENT B		(Column 1) CLAIMS REMAINING AFTER AMENDMENT		(Column 2) HIGHEST NUMBER PREVIOUSLY PAID FOR	(Column 3) PRESENT EXTRA	RATE ($)	ADDITIONAL FEE ($)	OR	RATE ($)	ADDITIONAL FEE ($)
	Total (37 CFR 1.16(i))	*	Minus	**	=	X$ 25 =		OR	X$50 =	
	Independent (37 CFR 1.16(h))	*	Minus	***	=	X100 =		OR	X200 =	
	Application Size Fee (37 CFR 1.16(s))									
	FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))					+180=		OR	+360=	
						TOTAL ADD'L FEE		OR	TOTAL ADD'L FEE	

* If the entry in column 1 is less than the entry in column 2, write "0" in column 3.
** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 20, enter "20".
*** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 3, enter "3".
The "Highest Number Previously Paid For" (Total or Independent) is the highest number found in the appropriate box in column 1.

This collection of information is required by 37 CFR 1.16. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 12 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.

If you need assistance in completing the form, call 1-800-PTO-9199 and select option 2.

APPLICATION DATA SHEET

Electronic Version v14
Stylesheet Version v14.1

Applicant Information:

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Correspondence Information:

Customer Number:	181	*181*

Application Information:

Title of Invention:	RESOURCE SHARING IN A TELECOMMUNICATIONS ENVIRONMENT
Application Type:	regular, utility
Attorney Docket Number:	

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Total Number of Drawing Sheets -

Representative Information:

practitioner(s) at Customer Number:

181 *181*

as our attorney(s) or agent(s) to prosecute the application identified above, and to transact all business in the United States Patent and Trademark Office connected therewith.

Domestic Priority Information:

This is a Non-Provisional of US application number 60/618,269, filed 2004-10-12.

Foreign Priority Information:

Assignee Information:

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