**UNITED STATES PATENT AND TRADEMARK OFFICE**
**BEFORE THE PATENT TRIAL AND APPEAL BOARD**

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**COMMSCOPE, INC.,**
Petitioner

v.

**TQ DELTA, LLC,**
Patent Owner

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Case: IPR2023-00064
Patent No. 8,276,048

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# PRELIMINARY RESPONSE TO PETITION FOR *INTER PARTES* REVIEW OF U.S. PATENT NO. 8,276,048

# TABLE OF CONTENTS

## TABLE OF AUTHORITIES

### Cases

**Statutes**

## EXHIBIT LIST

| Exhibit | Description |
|---|---|
| 2001 | TQ Delta's Second Amended Complaint, *TQ Delta, LLC v. Pace Americas, LLC, et al.*, No. 13-cv-1835-RGA (D. Del.) |
| 2002 | Affidavit of Mailing (Summons, Second Amended Complaint, and Notice-Consent of Availability of Mag Judge), *TQ Delta, LLC v. Pace Americas, LLC, et al.*, No. 13-cv-1835-RGA (D. Del.) |
| 2003 | Memorandum Opinion in *TQ Delta LLC v. 2Wire, Inc.*, Civil Action No. 1:13-CV-01835-RGA (D. Del. Aug. 23, 2019) |
| 2004 | 2Wire's Amended Corporate Disclosure Statement, *TQ Delta, LLC v. 2Wire, Inc.*, No. 13-cv-1835-RGA (D. Del.) |
| 2005 | ARRIS's 2015 Form 10-K |
| 2006 | 2Wire's Second Amended Corporate Disclosure Statement, *TQ Delta, LLC v. 2Wire, Inc.*, No. 13-cv-1835-RGA (D. Del.) |
| 2007 | ARRIS GLOBAL LTD. overview - GOV.UK |
| 2008 | Consolidation Order, *TQ Delta, LLC v. CommScope Holding Company, Inc., et al*., No. 2-21-cv-00310-JRG (E.D. Tex.) |
| 2009 | November 28, 2018 Opening Expert Report on Invalidity of Dr. Krista Jacobsen for Family 3Patents in *TQ Delta LLC v. 2Wire, Inc.*, Civil Action No. 1:13-CV-01835-RGA (D. Del.) |
| 2010 | January 4, 2019 Rebuttal Report of Dr. Todor Cooklev, *TQ Delta LLC v. 2Wire, Inc.*, Civil Action No. 1:13-CV-01835-RGA (D. Del. Aug. 23, 2019) (Dkt. 832-1) |
| 2011 | Oral Order, *TQ Delta, LLC v. 2Wire, Inc.*, No. 13-cv-1835-RGA (D. Del.) |
| 2012 | January 18, 2019 Reply Expert Report of Dr. Krista Jacobsen For Family 3 Patents in *TQ Delta LLC v. 2Wire, Inc.*, Civil Action No. 1:13-CV-01835-RGA (D. Del.) |
| 2013 | Defendant 2Wire, Inc.'s Opposition to Plaintiff TQ Delta, LLC's Motion for Summary Judgment of No Invalidity of Family 3 Patents Claims Under 35 U.S.C. § 103 in *TQ Delta* |

| Exhibit | Description |
|---|---|
| | *LLC v. 2Wire, Inc.*, Civil Action No. 1:13-CV-01835-RGA (D. Del.). |
| 2014 | Excerpts of Feb. 6, 2019 Deposition of Krista S. Jacobsen, Ph.D., *TQ Delta LLC v. 2Wire, Inc.*, Civil Action No. 1:13-CV-01835-RGA (D. Del. Aug. 23, 2019) (Dkt. 832-1) |
| 2015 | Excerpts of May 22, 2019 Trial Transcript in *TQ Delta LLC v. 2Wire, Inc.*, Civil Action No. 1:13-CV-01835-RGA (D. Del.) |
| 2016 | Order Denying CommScope's Motion to Transfer, *TQ Delta, LLC v. CommScope Holding Company, Inc., et al.*, No. 2-21-cv-00310-JRG (E.D. Tex.) |
| 2017 | Table C-5. U.S. District Courts—Median Time Intervals From Filing to Disposition of Civil Cases Terminated, by District and Method of Disposition, During the 12-Month Period Ending December 31, 2021 |
| 2018 | Table C-5. U.S. District Courts—Median Time Intervals From Filing to Disposition of Civil Cases Terminated, by District and Method of Disposition, During the 12-Month Period Ending December 31, 2020 |
| 2019 | Table C-5. U.S. District Courts—Median Time Intervals From Filing to Disposition of Civil Cases Terminated, by District and Method of Disposition, During the 12-Month Period Ending December 31, 2019 |
| 2020 | March 14, 2022 Declaration of Bruce McNair Regarding Claim Construction |
| 2021 | March 14, 2022 Declaration of George A. Zimmerman, Ph.D. Regarding Claim Construction |
| 2022 | March 14, 2022 Declaration of Richard D. Wesel, Ph.D. Regarding Claim Construction |
| 2023 | Nokia's Invalidity Contentions, *TQ Delta, LLC v. CommScope Holding Company, Inc., et al.*, No. 2-21-cv-00310-JRG (E.D. Tex.) |

| Exhibit | Description |
|---|---|
| 2024 | CommScope's Invalidity Contentions, *TQ Delta, LLC v. CommScope Holding Company, Inc., et al*., No. 2-21-cv-00310-JRG (E.D. Tex.) |
| 2025 | TQ Delta's Preliminary Election of Asserted Claims, *TQ Delta, LLC v. CommScope Holding Company, Inc., et al*., No. 2-21-cv-00310-JRG (E.D. Tex.) |
| 2026 | Nokia's Preliminary Election of Prior Art, *TQ Delta, LLC v. CommScope Holding Company, Inc., et al*., No. 2-21-cv-00310-JRG (E.D. Tex.) |
| 2027 | CommScope's Preliminary Election of Asserted Prior Art, *TQ Delta, LLC v. CommScope Holding Company, Inc., et al*., No. 2-21-cv-00310-JRG (E.D. Tex.) |
| 2028 | Declaration of Edward Chin |
| 2029 | Excerpts of June 1, 2022 *Markman* Hearing Transcript, *TQ Delta, LLC v. CommScope Holding Co.*, No. 2:21-CV-310-JRG (E.D. Tex.) |
| 2030 | Declaration of Jim Shead in Support of Petition for Inter Partes Review of U.S. Patent No. 8,462,835. |
| 2031 | Claim Construction Memorandum and Order (Dkt. 169), *TQ Delta, LLC v. CommScope Holding Co.*, No. 2:21-CV-310-JRG (E.D. Tex. June 8, 2022). |

## I. Introduction

Patent Owner TQ Delta, LLC ("TQ Delta" or "Patent Owner") submits this Preliminary Patent Owner Response to the Petition filed by CommScope, Inc. ("CommScope" or "Petitioner") requesting *Inter Partes* Review ("IPR") of the Challenged Claims (claims 1–4) of U.S. Pat. No. 8,276,048 (the "'048 Patent").

The Board should deny this Petition under Section 315(b). This Petition is time-barred—not only was CommScope served with a complaint for patent infringement in August 2021 (14 months before it filed this Petition), CommScope's subsidiary (2Wire) was sued in 2014 for infringing the Patent.[1] To attempt to get around that problem, Petitioner filed this Petition as a "copycat" of a March 2022 Nokia Petition and then moved to join this proceeding with the Nokia proceeding, asserting that requests for joinder are not subject to the one-year bar. But the Board has since terminated the Nokia proceeding in full (as to all parties) due to Nokia's settlement with TQ Delta. This means that there is no proceeding to join and

[1] The Board has twice held, for another TQ Delta patent asserted in the 2Wire case, that the one-year bar applied to CommScope, resulting in denial of institution. *CommScope, Inc. v. TQ Delta, LLC*, IPR2022-00352 (Paper 13) (P.T.A.B. Aug. 19, 2022); *CommScope, Inc. v. TQ Delta, LLC*, IPR2022-01443 (Paper 13) (P.T.A.B. Dec. 13, 2022). CommScope does not contest that finding in the Petition. 2Wire, Inc. (who merged into ARRIS in 2017) was served with a complaint alleging infringement of the Patent on February 7, 2014. In August 2021, TQ Delta sued ARRIS (and the company that acquired ARRIS in 2019, CommScope Holding Company) in the Eastern District of Texas.

Petitioner's joinder request is moot. And without any proceeding to join, the one-year bar undisputedly applies here and prohibits institution.

Indeed, that is the outcome the Board arrived at for a similar "copycat" Petition filed by CommScope and request to join a Nokia IPR. *CommScope, Inc. v. TQ Delta, LLC*, IPR2022-01443 (Paper 13) (P.T.A.B. Dec. 13, 2022). There, like here, Petitioner "relie[d] on its request to join the [Nokia] IPR to avoid the time bar in § 315(b)." *Id.* at 3. But because "the Board terminated the [Nokia] IPR based on settlement between the parties," there was "no pending proceeding in the [Nokia] IPR for Petitioner to join." *Id.* at 4. As a result, the Board denied Petitioner's joinder motion. *Id.* And, with joinder disposed of, the Board found the petition was time-barred and denied institution. *Id.* That same outcome applies here.

Should the Board look beyond Section 315(b), there are additional reasons to deny institution. This is the type of case in which discretional denial under Section 314(a) is appropriate. Petitioner challenged the Patent at trial in 2019 and lost. In the Texas case, Petitioner is asserting the same primary references—Mazzoni and Fadavi-Ardekani—that it asserts here. Trial in the Texas case is set for less than four weeks from now (on March 17, 2023) and will conclude before the deadline to issue an institution decision in this case. Instituting proceedings here—after Petitioner attempts to have a second jury invalidate the Patent—is not an efficient use of the Board's resources; it is an abuse of the IPR system.

Last, the Petition fails to demonstrate a reasonable likelihood that the Challenged Claims are unpatentable. The Delaware Court and jury rejected Mazzoni and Fadavi-Ardekani for good reason: neither reference discloses the "shared memory" or "message" limitations. And CommScope's "new" secondary reference is the same type of reference rejected in the 2Wire Lawsuit and does not fix the disclosure lacking in Mazzoni and Fadavi-Ardekani. While TQ Delta understands that the Board disagreed with TQ Delta regarding the merits in the Nokia proceeding regarding the Mazzoni-based grounds, TQ Delta respectfully requests that—should the Board reach the merits—that it reconsider its prior analysis and deny institution.

## II. Factual Background

### A. Background Of The Patented Technology

The Patent[2] originates from the inventive work of individuals at a company called Aware, Inc. ("Aware"). Ex. 1026 at ¶¶ 23–28. Aware was a leading innovator and provider of digital-subscriber-line ("DSL") technologies, which, generally, provide high-speed internet over traditional phone lines. *Id.* The primary inventor of the Patent, Marcos Tzannes, has worked on DSL-related technologies for almost 30 years. *Id.* Mr. Tzannes was the head of the DSL technology group at Aware, and major semiconductor companies purchased Aware's chip designs. *Id.* Mr. Tzannes

[2] The Patent is from a family of Patents referred to as "Family 3."

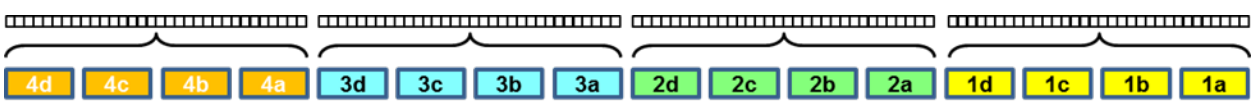
also has had significant involvement in developing industry standards for DSL (since 1997 and continuing today). *Id.*

The Patent relates to memory sharing between an interleaver and deinterleaver in communication systems, including DSL systems. Because DSL uses telephone lines, there is significant noise that can impact the transmission, including impulse noise (*e.g.*, intermittent bursts of errors, such as the switching of high-voltage electrical equipment). DSL systems address this noise by, among other ways, using forward error correction ("FEC") and interleaving.

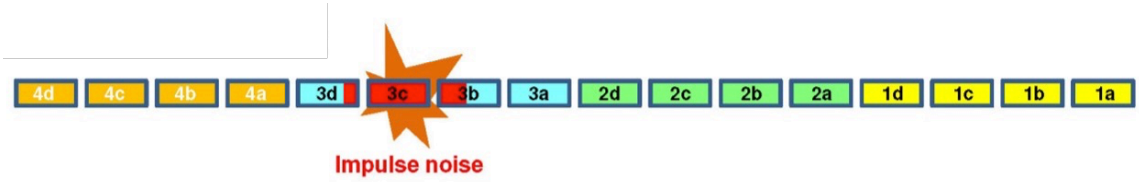
### 1. Forward Error Correction

Forward error correction refers to encoding schemes that provide redundant data to allow systems to correct errors without requiring retransmission (the system can thus correct errors on a forward basis). Reed-Solomon coding is one such technique. In Reed-Solomon coding, groups of data bits may be encoded into corresponding sets of codewords prior to transmission.

A group of bits obtained after encoding is a "codeword"; the codeword is then decoded upon receipt to recover the original data. The figure below illustrates the groupings of data bits and the corresponding codewords. For example, codeword 1 is in yellow. Each yellow box within the codeword (*i.e.*, 1a, 1b, 1c, and 1d) is referred to as a symbol.



Even using FEC, the transmission may still be corrupted by impulse noise. This is because impulse noise causes bursts of errors. The example below shows a stream in which noise has corrupted all of symbol 3c and some of symbols 3b and 3d. Of the blue codeword, noise has corrupted 40% of the data.



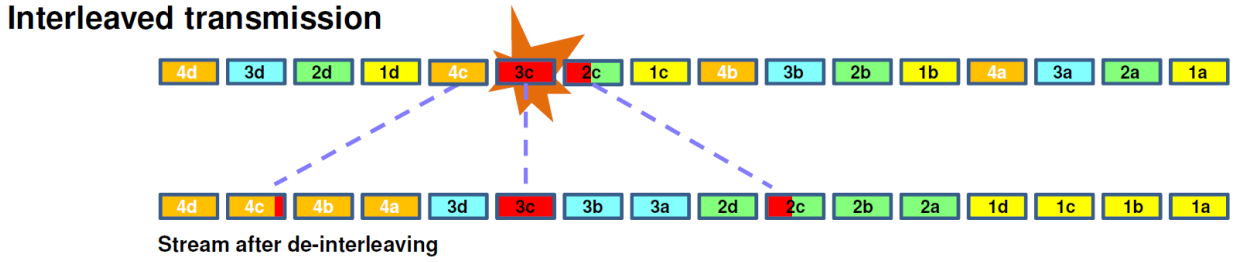

If the FEC technique can correct a codeword with 40% errors, it will be able to repair the damage. Otherwise, the damage would require retransmission of codeword 3. This retransmission can slow down the system.

## 2. Interleaving And Deinterleaving

Interleaving provides a way to deal with impulse noise by spreading the impact of noise across multiple codewords. Interleaving, in general, refers to rearranging the order in which codeword symbols are transmitted. Because impulse noise is relatively short in duration, spreading out the codewords in time helps address noise. Upon receipt of the bytes of interleaved codewords, the codewords are reassembled by rearranging the bytes back into their original order. This is called deinterleaving. The component used for interleaving is an "interleaver"; the component for deinterleaving is a "deinterleaver."

The illustration below depicts an interleaved data stream consisting of four symbols from four different codewords. In particular, the first symbol from the four

different codewords (yellow 1a, green 2a, blue 3a, and orange 4a) is transmitted first (starting on the right side of the figure); then a second symbol from each codeword (yellow 1b, green 2b, blue 3b, and orange 4b) are transmitted, and so on.




Using interleaving, the same impulse noise event corrupts less data of any particular codeword. The above image shows that, once deinterleaved, small amounts of codeword 4 (in orange) and codeword 2 (in green) are corrupted; only 25% of codeword 3 (in blue) is corrupted. If the FEC coding allowed for an error rate up to 25%, the system would still be able to recover all of the original data.

This improves the system because, as detailed above, 40% of the codeword 3 (in blue) would have been corrupted without using interleaving. This would have required the system to retransmit that codeword.

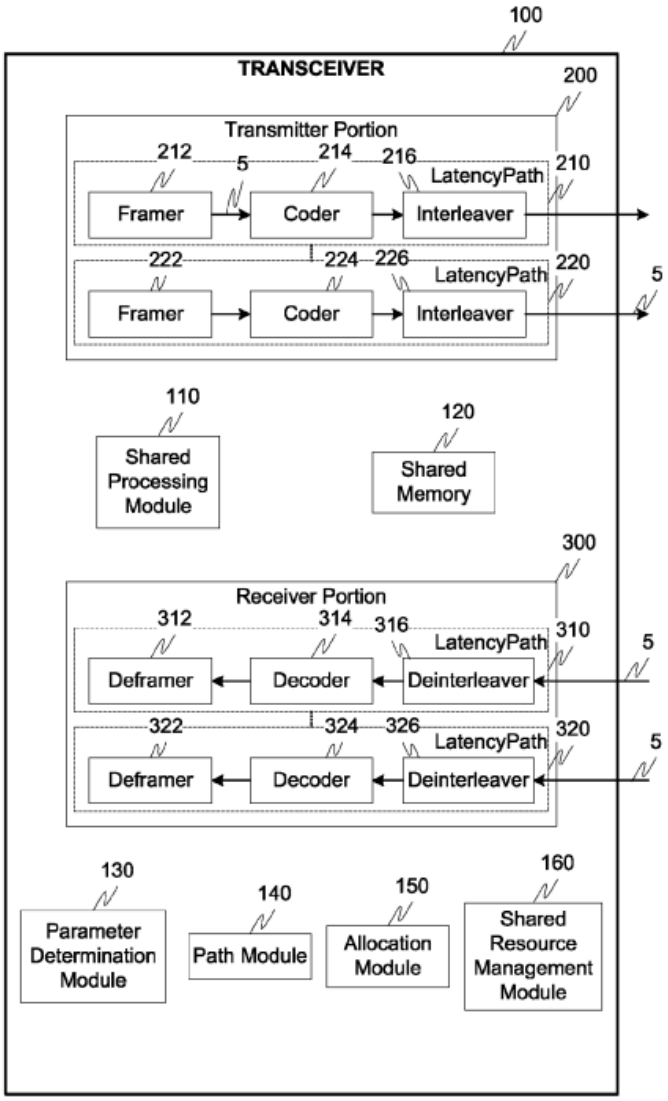
### 3. Interleaver And Deinterleaver Memory

Memory is required for interleaving and deinterleaving. The interleaver and deinterleaver can consume significant memory. *See, e.g.*, Ex. 1001 at 1:47–49 ("[A]n interleaver within a latency path can consume a large amount of memory...."). How much memory they require is a function of a number of parameters. These parameters include codeword size (*e.g.*, how many symbols are in a codeword) and

the spacing between adjacent symbols (*e.g.*, how apart in the interleaved stream, for a given codeword, is symbol 1a from 1b from 1c, etc.…), which is generally referred to as the depth. The example above has a depth of 4 because there is a spacing of 4 symbols between 1a and 1b, 1b and 1c, and 1c and 1d.

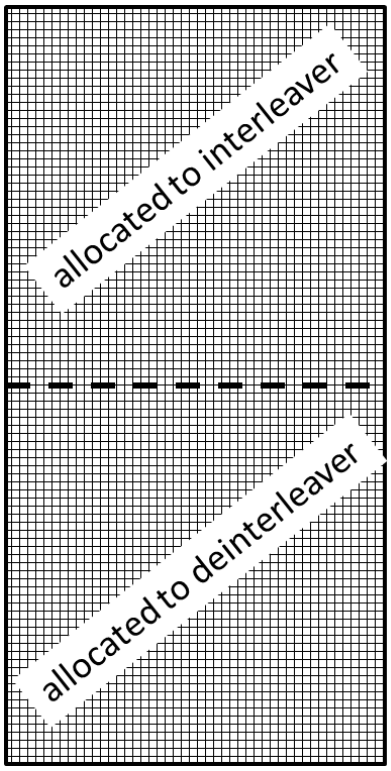
### 4. The Memory Sharing Techniques Of The Patent

The Patent describes techniques to allocate a shared memory between an interleaver and a deinterleaver of a transceiver. An example transceiver, shown on the right, contains two interleavers (216 and 226) in the transmitter portion (200) of the transceiver, one for each data stream the transceiver can transmit. In the receiver portion (300), the transceiver contains two deinterleavers (316 and 326), one for each data stream the transceiver can received. Ex. 1001 at Fig. 1.




A shared memory (120) is "shared amongst the two transmitter portion interleavers 216 and 226 and two

receiver portion deinterleavers 316 and 326." Ex. 1001 at 4:59–62; *see also id.* at 5:33–39 ("[F]or example, an exemplary transceiver could comprise a shared interleaver/deinterleaver memory and could be designed to allocate a first portion of the shared memory 120 to an interleaver, such as interleaver 216 in the transmitter portion of the transceiver and allocate a second portion of the shared memory 120 to a deinterleaver, such as 316, in the receiver portion of the transceiver."). The figure below shows an example allocation of the shared memory between an interleaver and a deinterleaver.




The portion of shared memory above the dashed line is allocated for use by the interleaver, and the portion of shared memory below the dashed line is allocated for use by the deinterleaver. The interleaver uses memory cells from the portion of

shared memory allocated to interleaving and the deinterleaver uses memory cells from the portion of shared memory allocated to deinterleaving.

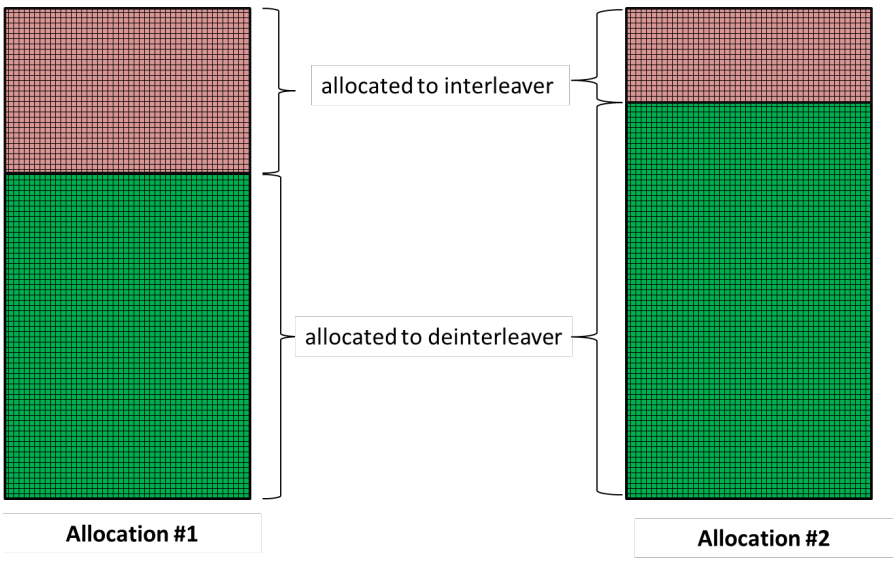
The allocation may be performed in accordance with messages exchanged by the transceivers. *See, e.g.,* Ex. 1001 at 8:48–52 ("[I]n this case, the first transceiver would send a message to the second transceiver containing the information described above and based on this information and the application requirements the second transceiver would select latency path settings."). For example, based on a received message, the transceiver may allocate a first portion of the shared memory for use by an interleaver and allocate a second portion of the shared memory for use by a deinterleaver.

In addition, the allocation of shared memory between the interleaver and deinterleaver is not fixed. Instead, "the sharing of resources can be modified and messages transmitted between [] two transceivers at any time during initialization and/or user data transmission." Ex. 1001 at 4:37–40; *see also id.* at 6:65–7:3 ("[T]he latency paths can be reconfigured at initialization or during data transmission mode (also known as SHOWTIME in ADSL and VDSL transceivers). This would occur if, for example, the applications or application requirements were to change."); *id.* at 7:54–60 (describing allocation and reallocation of memory).

This modification can occur in response to "a change in communication that would require the adjustment of the shared resource allocation," such as a "change

in applications being transported over the system and/or changes in the channel condition, etc." Ex. 1001 at 9:30–35. Within one transceiver, the modification may require a new allocation of memory so that portions of the shared memory that were previously used by the interleaver are now used by the deinterleaver.

Such a change in allocation is illustrated below. On the left (Allocation #1), a first allocation is shown with about 35% of the memory cells allocated to the interleaver and about 65% allocated to the deinterleaver. On the right (Allocation 2), a different allocation is shown with about 20% of the memory cells allocated to the interleaver and about 80% allocated to the deinterleaver. Per this example, about 15% of the memory cells that were at one time allocated to the interleaver are at another time allocated to the deinterleaver. *See* Ex. 1001 at 6:18–7:49 (describing examples to change the memory allocation for video, voice, and Internet applications); *id.* at 1:28–31 (describing typical bit-error rate and latency requirements for video and voice); *id.* at Fig. 3 (showing monitoring of resource allocation and allocation of shared resources); *id.* at 9:22–35 (describing steps).




### B. The Delaware And Texas Litigation

The Patent has over 8 years of litigation history, in two ongoing cases. The art raised here (or its functional equivalent) was both previously raised and tried to a verdict in the 2Wire Lawsuit and is set for trial in the Texas Lawsuit.

#### 1. The 2014 Delaware 2Wire Lawsuit

In Delaware, in February, 2014, TQ Delta served 2Wire and Pace Americas, LLC (formerly known as Pace Americas, Inc.), and Pace plc with a complaint alleging infringement. *See* Ex. 2001 and 2002. At the time, 2Wire was a wholly-owned subsidiary of Pace plc. Ex. 2001 at ¶ 4. Since April 2019, 2Wire (which was merged into ARRIS Solutions, Inc.)[3] and Pace Plc (which became ARRIS Global,

[3] On May 19, 2017, 2Wire filed an amended corporate disclosure statement stating that "2Wire, Inc. has been merged to form ARRIS Solutions, Inc. This name change is the result of a merger between 2Wire, Inc., Aurora Networks, Inc., and ARRIS Solutions, Inc. that became effective January 1, 2017.... ARRIS Solutions, Inc.'s

Ltd.)[4] have been owned by CommScope Holding Company, Inc.

CommScope has confirmed these facts. *See CommScope, Inc. v. TQ Delta, LLC*, IPR2022-00352, Paper 2 at 65 (P.T.A.B. Dec. 31, 2021) ("2Wire's one-year period to petition for IPR of the '835 patent has run because Patent Owner filed a lawsuit on November 4, 2013 in the District of Delaware, which was amended on February 7, 2014 to name 2Wire as a defendant...."') and at Ex. 2030 at 1 ("On April 4, 2019, CommScope Holding Company, Inc., CommScope's parent entity, acquired ARRIS International Limited (UK) ... becoming its parent company. Prior to CommScope's acquisition of ARRIS International, ARRIS International acquired an entity named 2Wire, Inc.").

The 2Wire Lawsuit is ongoing. The case was divided into different patent families for trial. Ex. 1022, at 2–3. A trial on liability and validity for Family 3 took place in 2019, and the jury found infringement and no invalidity. Ex. 2003 at 2. A damages trial will be scheduled after all liability trials are completed. *See* Ex. 2011.

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parent company is ARRIS Group, Inc." Ex. 2004.

[4] On January 4, 2016, ARRIS Group, Inc. completed its combination with Pace plc whereby ARRIS International plc became the successor to ARRIS Group, Inc. and ARRIS International plc acquired Pace plc. 640 Case, Ex. 2005 at 2. Pace plc became a direct wholly-owned subsidiary of ARRIS International plc, which later became ARRIS International Limited (UK). *Id.* at 87; Ex. 2006. Pace plc was then renamed ARRIS Global, Ltd. Ex. Ex. 2007.

### 2. The 2021 Texas Lawsuit

On August 13, 2021, TQ Delta sued the "CommScope Defendants" (CommScope Holding Company, Inc., CommScope Inc., ARRIS International Limited, ARRIS Global Ltd., ARRIS US Holdings, Inc., ARRIS Solutions, Inc., ARRIS Technology, Inc., and ARRIS Enterprises) for infringement of several of its patents in Civil Action No. 2:21-cv-00310 (E.D. Tex.). Ex. 1027. On that same day, TQ Delta also sued Nokia Corp., Nokia Solutions and Networks Oy, and Nokia of America Corp. for infringement of several of its patents in Civil Action No. 2:21-cv-00309 (E.D. Tex.). Ex. 1026.

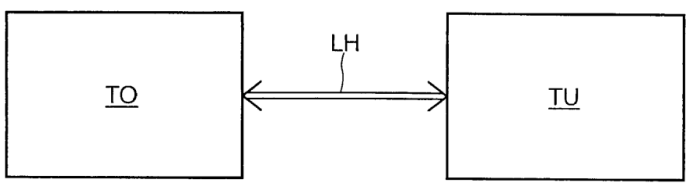
On October 22, 2021, the Texas Court consolidated both cases into Case No. 2:21-cv-00310 (the "Texas Lawsuit"). Ex. 2008. Trial in the Texas Lawsuit is scheduled for March 17, 2023. Ex. 2032.

## C. The Asserted References

### 1. Mazzoni

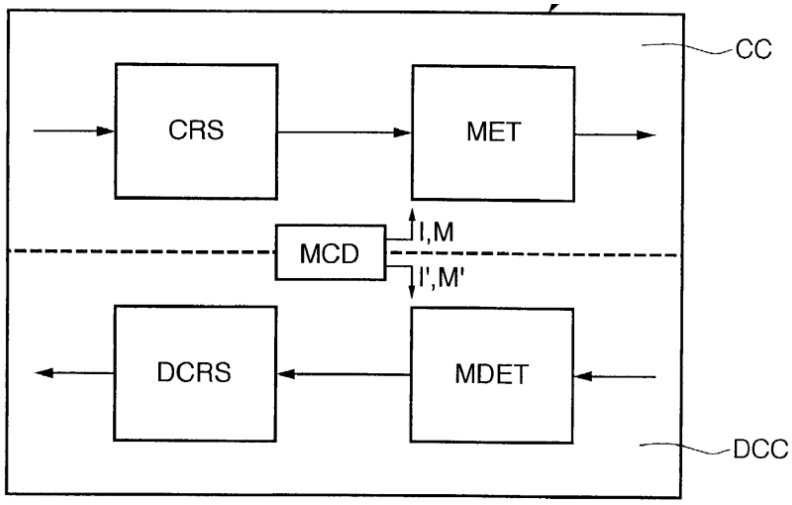
Mazzoni (Ex. 1005) describes DSL terminals with a predefined data rate pair (a fixed upstream rate and a fixed downstream rate corresponding to one of twelve predefined services). *See generally*, Ex. 2010 at ¶¶ 196–203 (providing overview of Mazzoni). In general, Mazzoni describes "[a] device for sending/receiving digital data is capable of processing different bit rates from a group of predetermined bit rates." Ex. 1005 at (57). The reference teaches the use of a terminal at the operator

(referred to as "TO") communicating with a terminal at the user (referred to as "TU"). *Id.* at 3:53–61. The two terminals are linked by a very high bit rate communication line (referred to as "LH"). *Id.* Figure 1, shown below, shows the high-level view of Mazzoni.

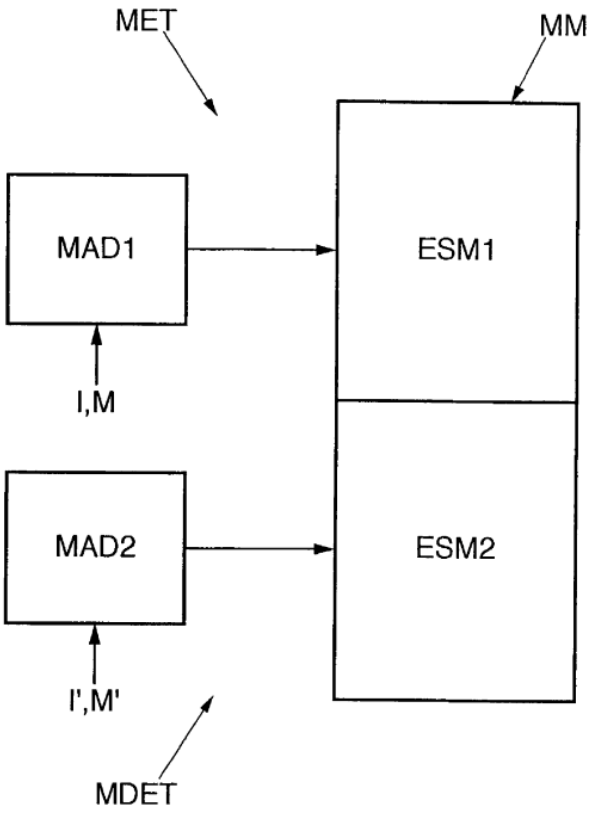



For communications between the TO and TU, Mazzoni describes six symmetrical data rate pairs and six asymmetrical data rate pairs, *i.e.*, pairs of upstream and downstream data rates for a service. Ex. 1005 at 3:62–4:14. A symmetrical service uses the same data rate for upstream and downstream transmissions; an asymmetrical service has different data rates. *See id.*

As part of the transmission, Mazzoni discloses FEC and interleaving. Ex. 1005 at 4:26–5:8. For transmitting data, Mazzoni includes a Reed-Solomon coding means (CRS) and an interleaving means (MET). *Id.* at 5:9–30. For receiving data, Mazzoni includes a Reed-Solomon decoding means (DCRS) and a deinterleaving means (DMET). *Id.* Mazzoni discloses a control means (MCD) that delivers parameters to the interleaver (I and M) and to the deinterleaver (I' and M').




Mazzoni shows the division of the interleaver memory space (ESM1) and deinterleaver memory space (ESM2) with memory (MM) as follows (*id.* at Fig. 6).




"[T]he interleaving means and the deinterleaving means include common

memory means MM, e.g., a dual-port random access memory." Ex. 1005 at 5:61–67. The memory within MM is then "divided into a first memory space ESM1 assigned to the interleaving means MET, and a second memory space ESM2 is assigned to the deinterleaving means MDET." *Id.*

The parameters (I, M and I',M') "define the sizes of the respective memory spaces assigned to the interleaving means [ESM1] and to the deinterleaving means [ESM2]." Ex. 1005 at 5:24 30. Mazzoni explains that, for a particular data rate pair, I and M specify the amount of predefined memory for the TO's downstream interleaver (and the corresponding downstream deinterleaver at the TU) and I' and M' specify the amount of predefined memory for the TO's upstream deinterleaver (and the corresponding downstream interleaver of TU). *See, e.g.*, *id.* at 6:38–43 ("More particularly, the size of the first memory space needed to implement triangular convolutional interleaving with I branches of i-1 blocks of M bytes is equal to I x (I-l) x M/2. Similarly, the size of the second memory space ESM2 required to support the uplink bit rate is equal to I' x (I'-1) x M'/2.").

The reference explains that these parameters are stored in a table and set when the modem is installed.

> The above calculation of I, M, I' and M' for the asymmetrical service A6 can be applied in an analogous manner to the other services of the VDSL system. A table of values for the parameters I, M, I' and M' can therefore be stored in the coding/decoding stage. When the modem is installed at the end of the line, and depending on the

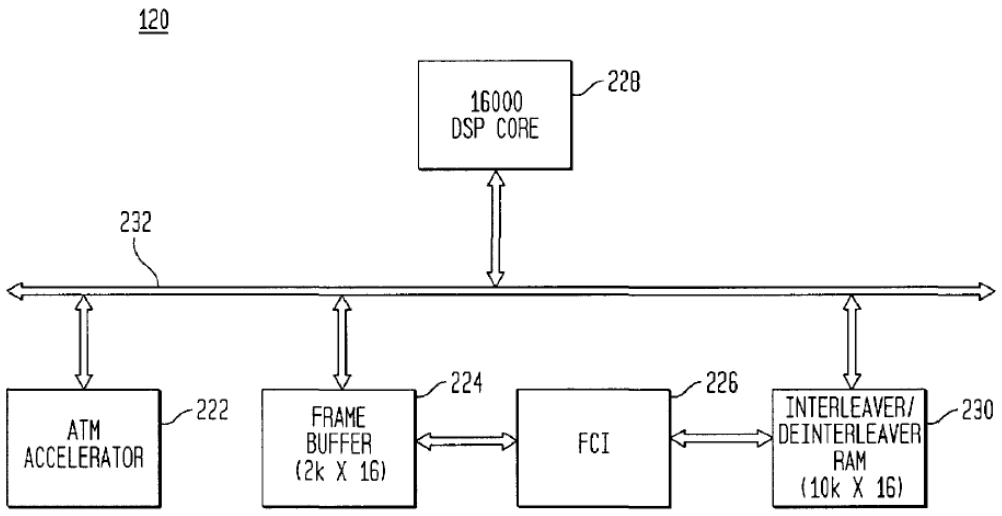
> service actually provided by the operator, the control means MCD may retrieve the corresponding values of I, M, I' and M' from the stored table.

Ex. 1005 at 6:51–61. The values are retrieved based on "the service actually provided by the operator," *i.e.*, the upstream and the downstream data rate pair configuration that is being provided by the service.

The jury in the 2Wire Lawsuit concluded that Mazzoni (in view of a LB-31, Ex. 1017) did not invalidate claim 1. Ex. 1023. The Court upheld the verdict because there was sufficient evidence that the Mazzoni-based combination would be inoperable (it would lack sufficient memory). Ex. 2003 at 15–16.

**2. Fadavi-Ardekani**

Fadavi-Ardekani (Ex. 1006) discloses "an Asymmetric Digital Subscriber Line (ADSL) transceiver that manages multiple asynchronous ADSL sessions, synchronizing the digital signal processing tasks for the sessions with a buffering and scheduling scheme such that the various transceiver components operate seamlessly (i.e., in a semi-synchronous fashion)." Ex. 1006 at 2:62–68; *see generally* Ex. 2010 at ¶¶ 265–270 (providing overview of Fadavi-Ardekani). Figure 2 of Fadavi-Ardekani shows a block diagram of the transceiver (Ex. 1006 at Fig. 2).

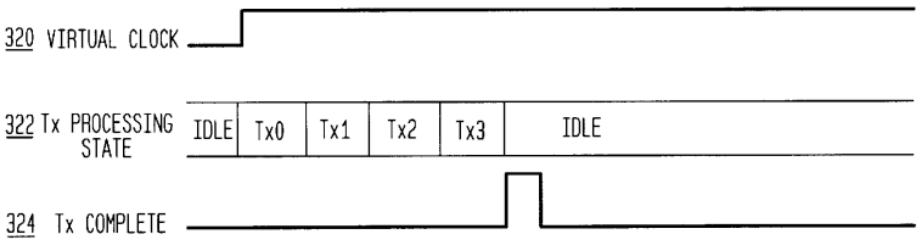



Fadavi-Ardekani teaches that components in the above diagram (referred to as "agents") access the frame buffer (referred to as "FB") and the interleaver/deinterleaver memory (referred to as the "IDIM") in "ping-pang" fashion. Ex. 1006 at 5:57–60, 6:55–60; *see also id.* at 6:66–7:33 (describing simple and optimal implementations for IDIM). The reference explains that "ping pang" refers to alternating the use of the memory between agents.

> "Ping-pang" means that areas of the memory buffer are alternately utilized exclusively by one agent (a transceiver component for performing some function) and then by a second agent. As one area of memory is being used by a first agent, another area of memory can be used by a different agent.

Ex. 1006 at 5:60–65. The reference explains how the memory is used in ping-pang fashion in connection with Figure 3. The reference explains the use of memory during the Tx Processing State as follows.

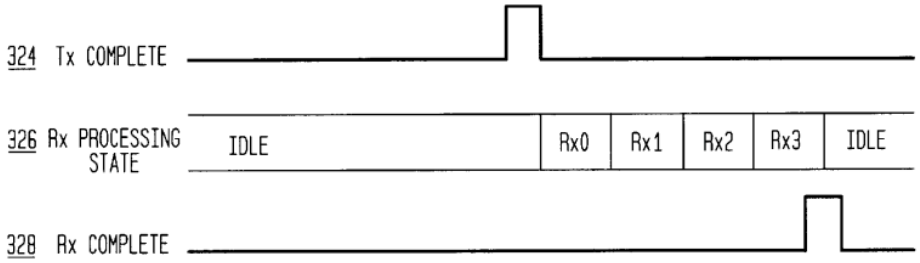
FIG. 3




The IDIM may also be used in a ping-pang fashion by the FCI and the DSP core based on the virtual clock cycle. For example, between the events of the virtual clock signal transition and the rising edge of the TX processes are complete signal (TX_Complete 324), the DSP core may load new DMT frames of RX data to a portion of the IDIM used as de-interleave memory while the FCI is using a portion of the IDIM as interleave memory.

Ex. 1006 at Fig. 3 (truncated), 8:58–9:3. Conversely, the reference explains the use of memory during the Rx Processing State as follows.

FIG. 3




Between the events of TX Complete 324 and signal that all RX processes are complete (RX_Complete 328), the DSP core can read TX data from the portion of the IDIM used as interleave memory while FCI is accessing the portion of the IDIM used as de-interleave memory.

Ex. 1006 at Fig. 3 (truncated), 8:58–9:3. Fadavi-Ardekani has been considered by the Delaware Court and the Patent Office. The Patent Office considered the

reference during prosecution and allowed the claims. Ex. 1002. The Court in the 2Wire Lawsuit similarly concluded, on summary judgment, that 2Wire failed to show that the reference discloses a "shared memory," as claimed. Ex. 1022 at 18–19. This was based, among other reasons, on 2Wire's expert deposition testimony that the reference "doesn't explicitly disclose dedicated or shared memory." Ex. 2014 at 570:25–571:20.

### 3. ETSI VDSL1

ETSI VDSL1 (Ex. 1007) is a technical specification that provides "requirements for transceivers that provide very high bit-rate digital transmission on metallic, unshielded, access network wire pairs. The technology is referred to as Very high speed Digital Subscriber Line (VDSL)." Ex. 1007 at 9. The reference generally describes a device at a central office (the VTU-O below) and a device at a customer's site (the VTU-R below). *Id.* at 14.

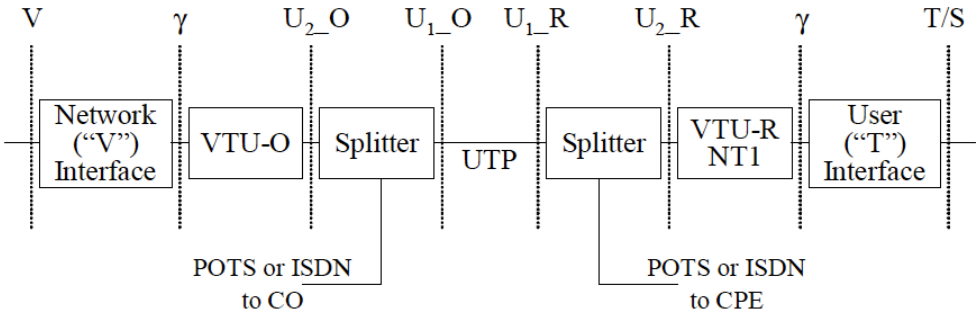



**Figure 1: Interface reference model**

Petitioner points to the channel analysis and exchange messages within ETSI VDSL1, shown in the below timeline. Ex. 1007 at 127.

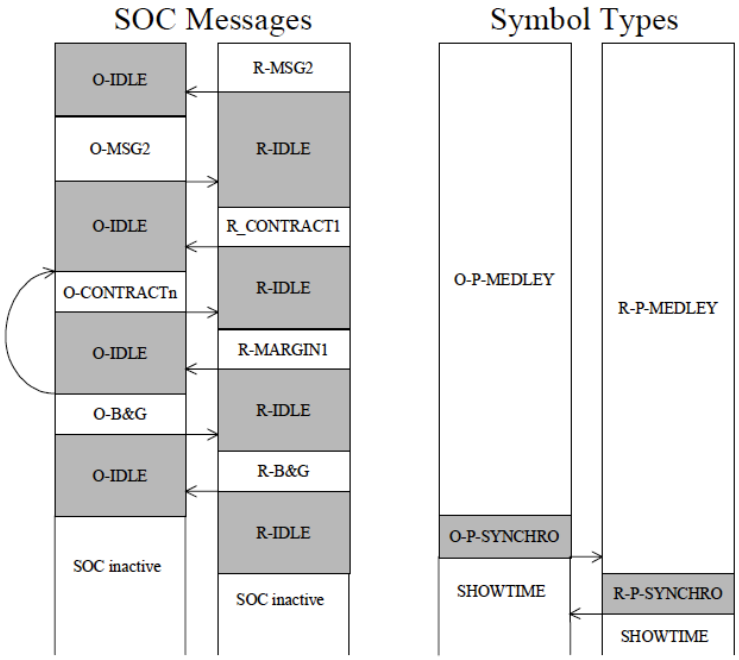



**Figure 56: Timeline of the channel analysis and exchange phase**

According to ETSDI VDSL1, the VTU-R first sends the VTU-O an R-MSG2 message, which contains the interleaver settings supported and maximum interleaver memory of the VTU-R. Ex. 1007.127, 132. After receiving the R-MSG2 message, the VTU-O sends the O-MSG2 message to the VTU-R. Ex. 1007 at 127. This message includes the interleaver settings supported by the VTU-O. *Id.* at 128–29. It also includes the "[m]aximum number of bits per tone." *Id.* at 128.

Next, the VTU-R sends the R_CONTRACT1 message. "This message contains the contract based on the maximum number of bits specified in O-MSG2." Ex. 1007 at 132. The VTU-O then sends an O-CONTRACTn message, which

"consists of a proposal for an upstream and downstream contract," including the data rates and interleaver settings. *Id.* at 128.

The VTU-R then computes margin for the downstream contract proposed in the O-CONTRACTn message, which indicates if the contract will meet the bit-error rate target of $10^{-7}$ (*i.e.*, the system expects one error per 10,000,000 bits transmitted). Ex. 1007 at 84, 132. The VTU-R then sends the margin data in an R-MARGIN message to the VTU-O. *Id.* at 132.

After receiving the R-MARGIN message, the VTU-O can implement this contract (by sending an O-B&G message) or it can propose a new contract by sending an O-CONTRACTn message. Ex. 1007 at 129–33. As discussed below, the ETSI VDSL1 reference is similar to the LB-031 reference asserted in the 2Wire trial (both disclose VDSL messages).

## III. The Board Should Deny Institution Under Section 315(b)

The Board should deny institution under Section 315(b) as time-barred. CommScope filed this Petition on October 26, 2022, and it is undisputed that CommScope was served with a complaint alleging infringement of the Patent before October 26, 2021. In the Texas Lawsuit, CommScope was served with a complaint in August 2021. CommScope's subsidiary, 2Wire, was served with a complaint in 2014. The Board denied institution under Section 315(b) because, prior to filing petitions against TQ Delta, "CommScope acquired a time-barred entity, 2Wire, Inc.,

and the acquisition rendered 2Wire, Inc. a real party-in-interest and privy." *CommScope, Inc. v. TQ Delta, LLC*, IPR2022-01443 (Paper 13 at 3) (P.T.A.B. Dec. 13, 2022). Both of these complaints create a time-bar, and CommScope does not contend otherwise in the Petition.

CommScope instead claims that the one-year bar does not apply because this petition includes a request to join the Nokia proceeding on the Patent. *See, e.g.*, Opp. to Mtn. for Joinder at 5 (discussing Nokia proceeding). But there is no longer a Nokia proceeding to join. *See, e.g.*, Sur-Reply to Mtn. for Joinder. As TQ Delta explained in its Sur-Reply to CommScope's Motion for Joinder, because there is no Nokia proceeding to join, there is no longer a basis for CommScope's Motion—the motion is moot, there is no power to join a terminated proceeding, and each of the joinder factors weigh solidly against joinder. *See id.* Joinder should thus be denied.

With joinder denied, this Petition should be denied under Section 315(b) as time-barred. That is the outcome the Board arrived at for a similar "copycat" Petition filed by CommScope and request to join a Nokia IPR filed against a TQ Delta patent. *CommScope, Inc. v. TQ Delta, LLC*, IPR2022-01443 (Paper 13) (P.T.A.B. Dec. 13, 2022). In that case, CommScope filed a first Petition that the Board denied as time-barred because "prior to filing its first petition, CommScope acquired a time-barred entity, 2Wire, Inc., and the acquisition rendered 2Wire, Inc. a real party-in-interest and privy." *Id.* at 3. After the Board instituted proceedings on Nokia's Petition,

CommScope filed a "copycat" Petition and "relie[d] on its request to join the [Nokia] IPR to avoid the time bar in § 315(b)." *Id.* "However, the Board terminated the [Nokia] IPR based on settlement between the parties, noting the Board's policy goal of fostering settlements." *Id.* at 4. As there was "no pending proceeding in the [Nokia] IPR for Petitioner to join," the Board denied CommScope's request to join the Nokia IPR. *Id.* As to institution, the Board "effectively maintain[ed] the Board's holding that CommScope's first petition remains time-barred. For the same reasons, the Petition in this proceeding is also time-barred, and institution is denied." *Id.*; *see also id.* ("The Motion for Joinder is denied because the [Nokia] IPR already has been terminated, and the Petition is denied because it was not filed within the time period set forth in § 315(b).").

That same outcome applies here. CommScope has not addressed the Board's decision in the -1443 Case, despite an opportunity to do so its Reply in support of its Motion for Joinder in this case (which was filed after the Board's decision in the -1443 Case). But the salient facts are the same. Both cases involve CommScope, TQ Delta, the same Nokia settlement agreement, and the same termination of proceedings due to the settlement. The outcome in the -1443 Case applies here.

## IV. The Board Should Exercise Its Discretion Under *Fintiv*

Should the Board look beyond Section 315(b), the Board should exercise its

discretion to deny institution under the factors[5] from *Apple Inc. v. Fintiv Inc.*, IPR2020-00019, Paper 11 (P.T.A.B. March 20, 2020) (precedential).

### A. Whether The Court Granted A Stay Or Evidence Exists That One May Be Granted If A Proceeding Is Instituted

This factor weighs against institution. This factor looks to the possibility of a stay to "allay concerns about inefficiency and duplication of efforts." *Fintiv*, at 6.

The Court has not granted a stay, and there is no evidence that the Court may grant a stay (should one ever be requested). This case is scheduled for trial on March 17, 2023. Given this schedule, it is highly unlikely that the Court will grant a stay even if the Board institutes proceedings (which will happen after trial).[6] This factor

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[5] The factors for determining "whether efficiency, fairness, and the merits support the exercise of authority to deny institution in view of an earlier trial date in the parallel proceeding" are 1) whether the court granted a stay or evidence exists that one may be granted if a proceeding is instituted; 2) proximity of the court's trial date to the Board's projected statutory deadline for a final written decision; 3) investment in the parallel proceeding by the court and the parties; 4) overlap between issues raised in the petition and in the parallel proceeding; 5) whether the petitioner and the defendant in the parallel proceeding are the same party; and 6) other circumstances that impact the Board's exercise of discretion, including the merits. *Id.* at 6.

[6] *See, e.g.*, *HTC Corp. v. Telefonaktiebolaget LM Ericsson Inc.*, No. 6:18-CV-00243-JRG, 2019 U.S. Dist. LEXIS 62097, at *5 (E.D. Tex. Jan. 16, 2019) (denying motion to stay pending arbitration where "the Court have already expended significant resources preparing for the upcoming pretrial conference and jury trial that are scheduled later this week and in four weeks, respectively[,]" and the arbitration panel had "yet to even be assembled"); *Realtime Data LLC v. Actian Corp.*, No. 6:15-CV-463-RWS-JDL, 2016 WL 9340796, at *4–5 (E.D. Tex. Nov. 29, 2016) (denying motion to stay "[g]iven the advanced stage of litigation"). In addition, should a stay be requested prior to an institution decision, the Eastern District of Texas Court "has a consistent practice of denying motions to stay when the PTAB has yet to institute

thus weighs in favor of denying institution. *See SK Innovation Co. v. LG Chem., Ltd.*, IPR2020-01239, Paper 14, at 15 (PTAB Jan. 12, 2021) (finding this factor weighed in favor of denying institution where "a stay is unlikely given the advanced state of that proceeding"); *Nintendo Co., Ltd. v. Gamevice, Inc.*, IPR2020-001197, Paper 13, at 11–12 (P.T.A.B. Jan. 12, 2021) (same).

### B. Proximity Of The Court's Trial Date To The Board's Projected Statutory Deadline For A Final Written Decision

In the 2Wire Lawsuit, the Patent has already been tried, and in Texas, trial is currently scheduled to start March 17, 2023. In this proceeding, the Board has until May 2023 to decide on institution, and, if the Board does institute, the Board would have until May 2024 to issue a final determination. Trial will still complete before the Final-Written-Decision deadline assuming the Texas Court substantially delays its trial. The Eastern District of Texas's overall (for all judges) recent December 2021 median time from filing to disposition is 23.3 months (which is, of course,

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post-grant proceedings." *Nanoco Techs. v. Samsung Elecs. Co.*, No. 2:20-CV-00038-JRG, 2021 U.S. Dist. LEXIS 134729, at *4 (E.D. Tex. Jan. 8, 2021) (citing *Trover Group, Inc. v. Dedicated Micros USA*, No. 2:13-cv-1047-WCB, 2015 U.S. Dist. LEXIS 29572, 2015 WL 1069179, at *6 (E.D. Tex. Mar. 11, 2015) (Bryson, J.) ("This Court's survey of cases from the Eastern District of Texas shows that when the PTAB has not yet acted on a petition for *inter partes* review, the courts have uniformly denied motions for a stay.")).

biased to longer COVID-19 delays).[7] Ex. 2017 (time-to-trial statistics). Even in the unlikely event the Texas Court delays its current schedule by three additional months (until July 2023), trials in the Texas Lawsuit would still occur over a year before the final-decision deadline.

### C. Investment In The Parallel Proceeding By The Court And The Parties

The 2Wire Lawsuit has completed trial and post-trial proceedings. Beyond a verdict, the Court denied 2Wire's motions for judgment as a matter of law and for a new trial, including on art raised in this Petition. Ex. 2003. This heavy investment favors denial. *See Mylan Labs. Ltd. v Janssen Pharm. NV*, IPR2020-00440, Paper 17 at 19 (P.T.A.B. Sep. 16, 2020) ("[T]here is a near certainty that trial will be completed in the Teva litigation imminently, so that the district court will have invested significant resources in assessing the validity of the challenged patent well before the Board would issue a Final Written Decision should we institute."). The Delaware Court also determined, at summary judgment, that Fadavi-Ardekani did not disclose the "shared memory" claim terms. Ex. 1022.

In the Texas Lawsuit, the parties and the Court have invested the resources to take the case to trial: infringement and invalidity contentions; the *Markman* process,

[7] Historic median times (in months) for the district from December are 19.8 (2020) and 21.0 (2019). Ex. 2018, 2019.

including the issuing of a *Markman* Order; dozens of depositions and hundreds of thousands of pages of documents produced; expert discovery (with over a dozen experts), including expert discovery; the filing of dispositive motions and *Daubert* motions; and submitting pretrial exchanges (*e.g.*, exhibit lists, deposition designations, and witness lists). The pretrial conference is set for March 1, 2023 and trial is set for March 17, 2023.

This investment favors denial. *10X Genomics, Inc. v. President and Fellows of Harvard College*, IPR2020-01467, Paper 21 at 13 (P.T.A.B. Feb. 22, 2021) ("[A]t this late stage in the district court proceeding the investment made by the court and both parties is significant, we find this factor weighs heavily in favor of exercising our discretion to deny institution."); *Google LLC v. Personalized Media Commc'ns, LLC*, IPR2020-00722, Paper 25 at 7 (P.T.A.B. Nov. 5, 2020) ("The issuance of the 94-page claim construction order and the completion of expert discovery on validity, all done in preparation for a trial scheduled to commence less than two months after our Decision was due, is evidence that 'the parallel proceeding is more advanced, a stay may be less likely, and instituting would lead to duplicative costs,' all of which are factors that 'favor[] denial' because 'the court and parties have invested sufficient time in the parallel proceeding to favor denial.' *Fintiv*, Paper 11 at 9–10.").

### D. Overlap Between Issues Raised In The Petition And In The Parallel Proceeding

There is material overlap between the issues raised in the petition and both the

2Wire Lawsuit and the Texas Lawsuit. TQ Delta asserted claim 1 of the '048 Patent in the 2Wire Lawsuit and has narrowed to claim 5 of the '048 Patent in the Texas Lawsuit. Ex. 2025; Ex. 1027. While the claim is different, the primary prior art references that Petitioner relies on—Mazzoni and Fadavi-Ardekani—is asserted here is also asserted to invalidate the Challenged Claims. And the same issues the petition addresses—whether the prior art references disclose the "shared memory" and "message" claim elements that are present in the Challenged Claims—have been litigated in Delaware and will be litigated in Texas. *See generally* Ex. 2009 (opining on invalidity in 2Wire Lawsuit based on Mazzoni, Fadavi-Ardekani, LB-031, and ITU version of VDSL standard). Accordingly, there is substantial claim overlap. *See Samsung Elec. Co. v. Clear Imaging Research, LLC*, IPR2020-01551, Paper 12 at 18 (P.T.A.B. Feb. 17, 2021) ("Petitioner does not show that the non-overlapping claims differ significantly in some way. Rather, both sets of claims recite similar subject matter.").

Furthermore, the petition relies on primary prior art (Mazzoni, and Fadavi-Ardekani) raised in the Texas Lawsuit. *See, e.g.*, Ex. 2023, 2024, 2026, 2027. The CommScope Defendants have specifically elected, under the Court's Order narrowing the case, to assert Mazzoni and Fadavi-Ardekani against the '048 Patent. Ex. 2027. Similarly, 2Wire asserted that claim 1 of the '048 Patent was obvious in view of combinations with Mazzoni and Fadavi-Ardekani. Ex. 1022. The Court

found against 2Wire for Fadavi-Ardekani at summary judgment. *Id.* And the jury found that claim 1 was not obvious in view of Mazzoni in combination with a reference similar to ETSI VDSL1 (a reference called LB-031). *See* Ex. 1023.

In addition, Factor 4 does not state that a jury must hear the exact same grounds found in a Petition in order for there to be overlap. The issue is, reasonably, whether there is "overlap between issues raised in the petition and in the parallel proceeding." *Fintiv*, Paper 11 at 6. Here, there is overlap because 2Wire, in its expert's report and at trial, raised invalidity grounds similar to those raised here. And those overlapping invalidity grounds were disposed of in the 2Wire Lawsuit, either by the Court's summary judgment or by the jury's verdict.[8]

Therefore, Factor No. 4 favors denial. *See PEAG LLC v. VARTA Microbattery GmbH*, IPR2020-01213, Paper 9 at 18 (P.T.A.B. Jan. 6, 2021) ("[S]ubstantially identical prior art and invalidity grounds are asserted in both the district court and the *inter partes* review proceedings.... Accordingly, the fourth Fintiv factor weighs

[8] CommScope cites *Patent Quality Assurance, LLC v. VLSI Tech.*, No. IPR2021-01229, Paper 10 (P.T.A.B. Jan. 26, 2022) in arguing that the Board disfavors denial when the parallel litigation did not involve the petitioner "unless 'the issues are the same, as or substantially similar to those already . . . litigated, or other circumstances weigh against redoing the work of another tribunal.'" Pet. at 80. In the 2Wire Lawsuit, the tribunal and parties addressed and resolved invalidity grounds that are substantially similar to those raised in the Petition. Moreover, in the *Patent Quality* case, the jury in the parallel litigation did not address the issue of invalidity at all—unlike the situation here where the jury in the 2Wire Lawsuit found the claims are not invalid. *Patent Quality*, Paper 10 at 6.

in favor of exercising discretion to deny institution."); *Fintiv*, Paper 11 at 12 ("[I]f the petition includes the same or substantially the same claims, grounds, arguments, and evidence as presented in the parallel proceeding, this fact has favored denial.").

### E. Whether The Petitioner And The Defendant In The Parallel Proceeding Are The Same Party

CommScope is the petitioner here and a defendant in the Texas Litigation. Thus, Factor No. 5 favors denial. *See Sotera Wireless, Inc. v. Masimo Corp.*, IPR2020-01019, Paper 12, 19 (P.T.A.B. Dec. 1, 2020).

### F. Other Circumstances That Impact The Board's Exercise of Discretion, Including The Merits

Other circumstances favor denial. This is far from a compelling case for institution; it is a repeat of art that has previously been found to not invalidate in the 2Wire Lawsuit. This strongly weighs against institution.

## V. The Board Should Deny Institution On The Merits

The Board can also deny institution on the merits. None of the references disclose the "shared memory" and "message" claim elements. And CommScope fails to show that its proposed obviousness combinations would actually work—the issue on which the Delaware Court upheld the jury verdict of nonobviousness when presented with similar theories. Institution should be denied.[9]

[9] TQ Delta reserves the right to challenge the petition on any ground should the Board institute review, including on the basis that CommScope has failed to show that the references qualify as prior art and that the references are not enabled. For

### A. Claim Construction

The Board construes the claims under the *Phillips* standard, looking to the "meaning of such claim as understood by one of ordinary skill in the art and the prosecution history pertaining to the patent." 37 C.F.R. § 42.100(b) (2021); *see Phillips v. AWH Corp.*, 415 F.3d 1303, 1312–13 (Fed. Cir. 2005) (en banc). "The Board is required to construe 'only those terms ... that are in controversy, and only to the extent necessary to resolve the controversy.'" *Real Time Data, LLC v. Iancu*, 912 F.3d 1368, 1375 (Fed. Cir. 2019) (citation omitted). TQ Delta addresses two "shared memory" terms in this Preliminary Patent Owner Response.[10]

#### 1. Shared Memory

TQ Delta submits that the term "shared memory" means "common memory used by at least two functions, where a portion of the memory can be used by either one of the functions." This construction is how two District Courts, across three Orders, have construed the term.

The Delaware Court twice construed "shared memory" as "common memory used by at least two functions, where a portion of the memory can be used by either

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the purposes of this Patent Owner Preliminary Response only, TQ Delta does not contest CommScope's level of ordinary skill in the art.

[10] TQ Delta reserves its right to challenge Petitioner's constructions and propose its own constructions should the Board institute review.

one of the functions." Ex. 1018, at 8; *TQ Delta, LLC v. Zyxel Commc'ns., Inc.*, No. 1:13-CV-02013-RGA, 2018 U.S. Dist. LEXIS 77271, at *19–24 (D. Del. May 8, 2018). The Texas Court likewise construed "shared memory" as "common memory used by at least two functions, where a portion of the memory can be used by either one of the functions." *TQ Delta, LLC v. CommScope Holding Co.*, No. 2:21-CV-310-JRG (E.D. Tex. June 8, 2022) (Dkt. 169), at 51–52 (attached as Ex. 2031). This construction finds support in the intrinsic record. *See, e.g.*, *id.* at 50–52 (citing Patent, Abstract, 4:59–62, 5:40–46); *see also* Ex. 1001 at 6:19–7:25 (describing reconfiguring shared memory one confirmation with one video application, one Internet application, and one voice application to another configuration for three Internet access applications).

Petitioner fails to provide a reason to depart from this construction of "shared memory. Petitioner and its expert cite no intrinsic evidence (or even extrinsic sources) that show that those courts arrived at the wrong construction. And while CommScope disputes the Courts' construction here, all of its grounds (and all its supporting expert testimony) purport to apply the Courts' construction of "shared memory." CommScope does not provide a separate analysis under its supposed plain-and-ordinary meaning construction. It does not explain what it means by plain-and-ordinary meaning or how the claims would not be patentable if the plain-and-ordinary meaning applied.

The Delaware and Texas construction also shows that none of the references disclose a shared memory. For example, the Delaware Court explained that its construction does not encompass memories such as ping-pang memory (*e.g.*, Fadavi-Ardekani):

> First, Plaintiff notes that one type of shared memory involves functions in a single transceiver that use the memory for "interprocess communication." Second, Plaintiff notes that yet another type of shared memory, known as "ping pang" memory, involves transmission in a single direction and uses a shared memory "exclusively for an interleaver" or "for a deinterleaver" at any one time. Neither of these memories is like the "shared memory" at hand. Defendants do not contest that for these patents, at any one time, a certain part of the memory can be used by one function or the other, but not both. Accordingly, in order to read out these other types of shared memory, I will include Plaintiffs language clarifying that common memory "can be used by either one of the functions."

Ex. 1018 at 9–10 (citations omitted) (emphases added); *see also* Ex. 2031 at 51–52 (holding that the terms requires that "the system is configured such that each unit of memory can be allocated to different functions over time"). Petitioner is silent on the effect of this construction, but it told the Texas Court that the Delaware Court's construction "effectively read[s] out this prior art reference [Fadavi-Ardekani] by narrowing the claim language."

> Now, this ping-pang memory is a term that comes directly out of one of our prior art references, Your Honor, and often it's actually referred to as ping-pong memory, so we know it comes out of that reference because it's one of the few references that would refer to as ping pang instead.

> And what the court ultimately did in the claim construction is it effectively read out this prior art reference by narrowing the claim language.

Ex. 2029 (June 1, 2022 *Markman* Hearing Tr.), at 68:14–21 (emphasis added). Consistent with these holdings, the Delaware Court found, on summary judgment, that 2Wire failed to show that Fadavi-Ardekani disclosed a "shared memory." Ex. 1022 at 18–19. Applying this construction of shared memory results in none of the grounds in the Petition raising a reasonable likelihood that the challenged claims are not patentable.

#### 2. Wherein The Shared Memory Allocated To The Interleaver Is Used At The Same Time As The Shared Memory Allocated To The Deinterleaver

TQ Delta preliminarily agrees with Petitioner's construction of this term ("the deinterleaver reads from, writes to, or holds information for deinterleaving in its respective allocation of the shared memory at the same time as the interleaver reads from, writes to, or holds information for interleaving in its respective allocation of the shared memory"). Pet. at 7, 9.

### B. Petitioner Fails To Show That Any Of The References Disclose The Claimed "Shared Memory" Elements

All grounds in the petition hinge on whether two references, Mazzoni (Ground 1) and Fadavi-Ardekani (Ground 2), disclose the "shared memory" claim elements.

As detailed below, Petitioner does not show that either reference discloses these elements.[11] The Board can deny the petition for this reason.

**1. Mazzoni**

Mazzoni does not disclose a shared memory. Ex. 2010 at 216–264 (detailing why Mazzoni does not disclose a shared memory). Mazzoni describes a predetermined assignment of a service that has a predetermined pair of upstream and downstream bit rates and a corresponding set of predetermined interleaver and deinterleaver parameter values (I, M, I' and M'). Ex. 1005 at 3:62–4:14 (describing twelve sessions with preset bit rates); *id.* at 6:11–53 (describing calculation of I, M, I', and M' for services based on bitrates).

Mazzoni contemplates that a technician installing the modem would provide only a single one of the fixed services for a particular connection. Ex. 1003 at 6:55–59 ("When the modem is installed at the end of the line, and depending on the service actually provided by the operator, the control means MCD may retrieve the corresponding values of I, M, I' and M' from the stored table."). There is no disclosure in Mazzoni that, once fixed at installation, any portion of the memory

[11] There is no allegation that ETSI VDSL1 discloses a shared memory. *See, e.g.*, Pet. at 21–23 (pointing exclusively to Mazzoni); *id.* at 57–61 (pointing exclusively to Fadavi-Ardekani). Petitioner does not point to any alleged shared memory in the reference, its expert agrees that the reference does not expressly disclose shared memory, Ex. 1003 at ¶ 87, and there is no allegation that the reference inherently requires a shared memory.

dedicated to the interleaver could ever be used by the deinterleaver and, conversely, that any portion of the memory dedicated to the deinterleaver could ever be used by the interleaver. All that is disclosed are ways to divide the memory (MM) into two fixed memories. That is not shared memory, as construed. *See, e.g.*, Ex. 2031, at 51–52 (explaining that the construction requires that "the system is configured such that each unit of memory can be allocated to different functions over time").

CommScope focuses on the general disclosure of the MCD delivering the parameters as evidence that the memory allocation could be changed, namely the following two sentences.

> As explained in more detail hereinafter, the parameters I, M, I' and M' can be modified, e.g., by software, and are delivered by control means MCD (see FIG. 3). The control means MCD may also be implemented in software.

Ex. 1005 at 5:21–24. These sentences, however, do not disclose a shared memory. They simply convey that the MCD may be implemented in software and "[a]s explained in more detail hereinafter," how those parameters can be "modified." *Id.* The only description "hereinafter" is that the "modification" is during installation of the modem by looking up a preset value in a table. *Id.* at 6:51–61.

There is no disclosure that a portion of the memory can be used by the interleaver at one point in time and the deinterleaver at another point in time. Indeed, 2Wire's expert testified that Mazzoni's parameters were frozen upon installation (such as by a technician), there was no disclosure of changing the setting (or the

process of sending out a technician ), and the reference's disclosure was "very limiting" in this regard. Ex. 2015 at 671:23–674:3.

**2. Fadavi-Ardekani**

Fadavi-Ardekani does not disclose the "shared memory" claim elements. There is no teaching in the reference that a portion of the IDIM can be used by either one of the interleaver/deinterleaver functions, as the construction of "shared memory" requires. *See, e.g.*, Ex. 2010 at ¶¶ 271–301 (explaining why Fadavi-Ardekani does not disclose a shared memory); Ex. 1018 at 9–10 (explaining that the construction that a portion of the common memory "can be used by either one of the functions" "read[s] out" memories such as '"ping pang' memory"); Ex. 2031, at 51–52 (holding that the terms requires that "the system is configured such that each unit of memory can be allocated to different functions over time"). Indeed, the Delaware Court concluded—as a matter of law on summary judgment—that 2Wire failed to show that the reference disclosed shared memory, based, in part, on the 2Wire's own expert testimony. Ex. 1022 at 18–19. The petition likewise fails.

The ping-pang functionality in Fadavi-Ardekani is about two processes alternating their use of and access to a memory, the IDIM. Ex. 1006 at Fig. 3, 5:60–65, 6:55–7:33, 8:58–9:3. But the reference is silent on how the portions of the IDIM are actually structured, *e.g.*, whether shared, dedicated, or something else. None of CommScope's citations to Fadavi-Ardekani (as well as all of its expert's citations)

address that fundamental issue with the reference; the reference simply notes that the IDIM as a whole is used for interleaving at one point in time and deinterleaving at another point in time. But that does not follow the construction of "shared memory"—and there is no evidence that a portion of the IDIM can be used by either one of the interleaver/deinterleaver functions. And Petitioner recently admitted to the Texas Court that this part of the construction "effectively read[s] out" the ping pang memory from Fadavi-Ardekani. Ex. 2029 at 68:14–21.

Even 2Wire's expert admitted that Fadavi-Ardekani "doesn't explicitly disclose dedicated or shared memory." Ex. 2014 at 570:25–571:20. CommScope points to no evidence that using a shared memory, as opposed to a dedicated memory, is the only way to implement ping-pang functionality. This is fatal to its petition. *Personal Web Techs., LLC v. Apple, Inc.*, 917 F.3d 1376, 1382 (Fed. Cir.) (requiring of inherency, including as part of an obviousness analysis, that "the natural result flowing from the operation as taught would result in the performance of the questioned function") (citation omitted).

To the contrary, the natural reading of Fadavi-Ardekani is that it provides dedicated memory, not a shared memory. Namely, the reference provides for dedicated downstream memories in each transceiver and separate, dedicated upstream memories in each transceiver. Portions of dedicated interleaver memory

that are not needed for interleaving cannot be allocated for use by the deinterleaver, and *vice versa*. Instead, those portions simply go unused.

The examples in Fadavi-Ardekani further show that the references does not disclose the claimed shared memory. The reference provides "simple" implementations for "G.Lite" and "ADSL." Ex. 1006 at 7:5–25. For G.Lite, the reference describes dedicated memories of 4 kilobytes per-session for downstream processing, 2 kilobytes for upstream processing, and 4 sessions, resulting in a requirement of 24 kilobytes of random-access memory (RAM) for that implementation ((4+2) x 4 = 24). *Id.* For ADSL, the reference describes 4 sessions, each of which requires 16 kilobytes for downstream processing, 2 kilobytes for upstream processing, and a "fast path" buffer of 1 kilobytes (resulting in 76 kilobytes of total dedicated memory). *Id.*

This disclosure does not teach that any given portion of memory could be used for either downstream processing (deinterleaving) or upstream processing (interleaving); it indicates that each portion is fixed at a requirement (per the G.Lite or ADSL standards). Indeed, even Petitioner's expert testifies that the ADSL example may be implemented in dedicated memory or shared memory, Ex. 1003 at ¶ 213, without explaining why a shared memory would be inherent or even necessary. That is the same position that the Delaware Court found could not show invalidity as a matter of law. Ex. 1022 at 18–19.

CommScope instead relies on the "optimal implementation," which Fadavi-Ardekani discloses in the following sentence.

> An optimal implementation of the interleaver according to the method of the invention utilizes the same memory for receive data and transmit data and thus requires 20 Kbytes to support a standard ADSL session at full interleave depth (16 K interleave & de-interleave +4 K fast path). . . . .

Ex. 1006 at 7:25–33. This sentence does not disclose a shared memory or indicate how the memory is allocated. Despite that, CommScope claims that this one sentence still discloses a shared memory because ADSL requires 16 kilobytes of downstream memory and 2 kilobytes of upstream memory (18 kilobytes total) and the "optimal" disclosure only mentions 16 kilobytes of memory. Ex. 1003 at ¶¶ 224–25. Thus, argues CommScope, it is implied that the upstream and downstream processes must share at least 2 kilobytes of memory. *Id.* That position is incorrect.

First, this disclosure does not meet the requirement that the shared memory "allocated to the interleaver is used at the same time as the shared memory allocated to the deinterleaver." This limitation requires that "the deinterleaver the deinterleaver reads from, writes to, or holds information for deinterleaving in its respective allocation of the shared memory at the same time as the interleaver reads from, writes to, or holds information for interleaving in its respective allocation of the shared memory." As interpreted by Petitioner, Fadavi-Ardekani's interleaver and deinterleaver memory is used at different times to account for the memory

overlap. *See, e.g.*, Ex. 1003 at ¶¶ 224–25 (creating embodiment in which 16 kilobytes of interleaved data is processed at Tx0 and, later in time, where 2 kilobytes of deinterleaved data is processed). Petitioner does not point to how this embodiment could even use the interleaver memory at the same time as the deinterleaver memory (which would cause memory to be overwritten and errors).

Second, Petitioner's "optimal implementation" would be inoperable. Petitioner claims that the very same portion of a memory would have to be used for receiving and transmitting data, *i.e.*, that Fadavi-Ardekani proposes to use 2 kilobytes or the memory to perform both interleaving and deinterleaving. This is impossible. Data received (to deinterleave) during one cycle will be overwritten by transmitted data (data to interleave) during a subsequent cycle and *vice versa*. Indeed, interleaved codewords often span multiple data frames (interleaving spreads the data out). And, as Fadavi-Ardekani recognizes, asynchronously received frame data "must be buffered in order to make frame data for each ADSL line available for processing on a transition of a transceiver clock." Ex. 1006 at 5:12–14. Consequently, the deinterleaving operation cannot be completed in one single cycle. This means that the device cannot correctly deinterleave received data and cannot correctly interleave the transmitted data due to the memory limitation.

Third, CommScope is simply wrong that the "optimal" embodiment was not before the Delaware Court at summary judgment. Pet. at 58. 2Wire's expert

extensively pointed to the "optimal" embodiment in her expert reports and raised the same "shared memory" arguments. *See, e.g.*, Ex. 2009 at ¶¶ 357, 372, 385, 403, 405, 440; Ex. 2012 at ¶¶ 206, 214, 255, 257, 260, 265, 317, 324. And 2Wire's brief opposing summary judgment pointed to the "optimal" embodiment (Ex. 2013 at 19).

> In an "optimal implementation of the interleaver," Fadavi-Ardekani teaches using "the same memory for receive data and transmit data," for example, using a 20-kbyte IDIM, which is sufficient to support "a standard ADSL session at full interleave depth," or more than one session with each using a smaller interleaver depth.

CommScope (with a different expert) now recycles the same argument. The Board should reach the same conclusion as the District Court and reject it.

* * * * *

CommScope fails to show that any of the references disclose the shared memory claim elements. The Board can deny institution for this reason.

### C. Petitioner Fails To Show the References Disclose The Claimed Message

Petitioner also does not show that the references disclose the claimed message. The claimed message refers to two aspects of the claims: (1) "transmitting or receiving a message during initialization specifying a maximum number of bytes of memory that are available to be allocated to an interleaver" and (2) "allocating a first number of bytes of the shared memory to the interleaver to interleave the first plurality of Reed Solomon (RS) coded data bytes for transmission at a first data rate,

wherein the allocated memory for the interleaver does not exceed the maximum number of bytes specified in the message." Ex. 1001, at claim 1. The Petition argues that Mazzoni and ETSI VDSL1 disclose these limitations.

**1. Mazzoni**

Mazzoni does not disclose the claimed message. Nowhere in the reference is there a message during initialization relating to the interleaver parameters, let alone a message "specifying a maximum number of bytes of memory that are available to be allocated to an interleaver." Nor is there any disclosure that "the allocated memory for the interleaver does not exceed the maximum number of bytes specified in the message."

The only part of Mazzoni that CommScope points to is that the parameters can be "modified, e.g., by software, and are delivered by control means MCD." Ex. 1003 at ¶ 113 (quoting Ex. 1005 at 5:21–24). But the MCD is within the terminal, and the reference teaches that the parameters are retrieved from a table stored on the device—not via a message during initialization. Ex. 1005 at Fig. 3, 6:51–61.

There is simply no disclosure of a message. Indeed, 2Wire's expert admitted at trial that Mazzoni "does not address initialization at all" and does not discuss exchanging messages for allocating memory. Ex. 2015 at 671:4–11, 674:13–17) (emphases added).

> Q. And Mazzoni does not describe any messages sent or received during initialization; right?

A. That's correct, it does not address initialization at all.

Q. It doesn't discuss any type of initialization, so it certainly doesn't discuss exchanging messages for allocating memory; right?

A. That's correct.

. . . .

Q. But again, just back to, there is no initialization messages of any kind described in Mazzoni?

A. That is correct.

Q. So certainly no memory sharing message?

A. That's correct.

Mazzoni does not teach this limitation.

**2. ETSI VDSL1**

Petitioner also relies on ETSI VDSL1. Petitioner specifically points to the messages exchanged in the contracting process from the ETSI VDSL1 standard as satisfying the message elements of the claims. *See, e.g.*, Ex. 1003 at ¶¶ 122–126, 173–178 (Ground 1); *id.* at ¶¶ 228–231, 246–251 (Ground 2). The reference, however, does not disclose these limitations.

There is no teaching that any of the messages are related to allocating memory, that a memory allocation even occurs, or that any allocation of interleaver memory does not exceed the maximum number of bytes specified in the message. The R-

MSG2 and O-MSG2 messages provide the interleaver settings of each device, and the O-CONTRACTn message includes interleaver settings. There is no disclosure that these messages are tied to allocating any memory on any device or specifying a maximum number of bytes that could be allocated to an interleaver. Petitioner does not point to any part of ETSI VDSL1 that indicates if those parts of the message are even utilized by the devices (let alone how they are used).

Instead, ETSI VDSL1 discloses that the purpose of the contract is to determine if the proposed data rates, error correction parameters, and interleaver settings are sufficient to provide a signal-to-noise margin that will result in a targeted bit-error rate. The O-CONTRACTn and R-MARGINn messages are used to arrive at the maximum data rate while achieving a bit-error rate target, not setting interleaver memory requirements. There is no disclosure that the message is used in connection with setting the amount of memory to utilize for an interleaver (or for a deinterleaver) or specifying an amount of bytes available for such an allocation.

Nor is such an allocation inherent in the messaging scheme. Petitioner does not address inherency, even though ETSI VDSL1 is silent on the purpose of the interleaver settings contained in the messages. But the reference itself indicates that the devices utilize dedicated memory—not memory that could be allocated based on a message. This is because each device communicates its supported interleaver settings. This teaches that each device has dedicated interleaver and deinterleaver

memory to cover those settings, not that the memory could be allocated to be used by either an interleaver or deinterleaver. Thus, Petitioner has failed to show that the messages in ETSI VDSL1 specify a number of bytes "available to be allocated to an interleaver" or that there is an allocation of shared memory "wherein the allocated memory for the interleaver does not exceed the maximum number of bytes specified in the message."

* * * * *

CommScope fails to show that any of the references disclose the message claim elements. The Board can deny thus institution of the Petition for this reason.

### D. Petitioner Fails To Make A Showing of Obviousness

In addition to the deficiencies above, CommScope also fails make a sufficient showing of obviousness for at least the reasons below.

#### 1. Mazzoni And ETSI VDSL1

CommScope fails to show that a person skill in the art would have been motivated to combine Mazzoni and ETSI VDSL1. This is because the combination of the references would not be operable due to Mazzoni's memory constraints.

This is the conclusion that was reached in Delaware for a similar VDSL proposal that also taught exchanging interleaver and deinterleaver memory settings (known as LB-031, Ex. 1017). LB-031 discloses that each side of the communication (the VTU-O and VTU-R) sends their maximum memory capabilities

in each direction (using interleaver delay), and the system selects the smaller of the two. Ex. 1017, at 6; Ex. 2015 at 745:9–747:6 (discussing LB-031).

The Delaware Court upheld the verdict of nonobviousness because the undisputed trial record established that the Mazzoni combination would not work "if just 'bolted' together" and there was substantial evidence that the combination "would be inoperable due to the memory capability problem." Ex. 2003 at 15–16. TQ Delta's expert explained that the combination of Mazzoni and LB-031 would be inoperable because Mazzoni would run out of total memory.

> Q. Could you tell me whether Mazzoni if it uses LB-031 would it have enough total memory to satisfy what is necessary for the interleaver and deinterleaver?
>
> A. Yes, I can illustrate that. So just perhaps the members of the jury remember that Mazzoni has 12 different services. . . . . So in order to support all 12 services, a modem needs to have 27,000 bytes of memory. If this is the amount 2 of memory that a device has, it will be able to support all 3 12 services. So this is how much memory is according to Mazzoni.
>
> Now, if we combine LB031 with Mazzoni, here is what is going to happen. Now, LB031 requires the devices to exchange their maximum capabilities in each direction, and then to select the smaller of the two. So according to LB031, the central office will communicate to the CPE transceiver that it can support -- this is close to 25,000 bytes -- in the downstream direction according to the A6 service.

> The CPE receiver will respond, and it will say it also -- it can support 25,000 bytes in the downstream direction according to the A6 service. Now, in the other direction, the central office will communicate that it can support a little less than 11,000 bytes in the upstream direction according to the service S6.
>
> Q. Dr. Cooklev, so how much total memory will be required according to the LB031 messaging scheme?
>
> A. So now if we apply this messaging scheme to Mazzoni, so now the total amount of memory that would be required in this case as a result of the LB031 and Mazzoni combination will be close to 36,000 bytes. Well, the problem is the Mazzoni device doesn't have that much. Mazzoni has -- as I established, it has slightly less than 27,000 bytes. Since 36,000 is greater than 27,000, so the combination of LB031 and Mazzoni doesn't work because Mazzoni doesn't have that capability.
>
> Q. So that's a inoperable combination?
>
> A. Is an inoperable combination.

Ex. 2015 at 745:9–747:6; Ex. 2010 at ¶¶ 193–264 (addressing combination). Despite this history, CommScope does not address the memory capacity issues of Mazzoni. But the same issues remain with CommScope's combination of Mazzoni and ETSI VDSL1.

Namely, the R-MSG2 and O-MSG2 messages (as CommScope interprets them), provide for settings that Mazzoni's memory could not support. The total size of Mazzoni's memory—for both interleaving and deinterleaving—is fixed at 26,892

bytes. Ex. 1003 at ¶ 155; Ex. 1005 at 4:18–22, 6:45–50 ( "The final size of the memory MM is ... equal to 26,892 bytes[.]"). But the R-MSG2 and O-MSG2 messages provide settings that require more than 26,892 bytes of memory, which will break Mazzoni. And nothing in ETSI VDSL1 prevents this problem.

The R-MSG2 message includes the maximum interleaver memory of the VTU-R (which Petitioner maps to the "TU" in Mazzoni). Ex. 1007, at 132. For Mazzoni, the maximum interleaver memory at the TU is associated with the S6 service. Ex. 1005 at 3:66–4:2. Petitioner calculates the interleaver memory requirement for S6 as 10,920 bytes based on the equations in Mazzoni. Ex. 1003 at ¶ 156. The R-MSG2 message would include the interleaver settings, which would include the interleaver settings for S6. Ex. 1007 at 132.

The O-MSG2 message conversely includes the interleaver settings for the VTU-O (which Petitioner maps to Mazzoni's TO). Ex. 1007 at 128. These settings would include the settings for A6. The amount of interleaver memory required at the TO for A6 is 24,960 bytes. Ex. 1003 at ¶ 156 (calculating, by Petitioner's expert, a requirement of 24,960 bytes); *see also* Ex. 1005 at 5:19–30 (describing calculations and arriving at 24,960 bytes). This is also the amount of memory required for the deinterleaver at the TU. *See id.* Applying these settings in the contract would result in a total memory requirement at the TU of 35,880 bytes for interleaving and

deinterleaving. With only 26,892 bytes of memory, the TU would not be able to interleave and deinterleave data once data transmission began.

The petition does not address this flaw with Mazzoni and ETSI VDSL1, the same flaw that caused the jury and Delaware Court to reject obviousness in view of LB-031. Petitioner instead asserts that those skilled in the art would have "understood that, throughout the exchange, the VTU-O would not propose a contract that exceeds the available interleaver memory at the VTU-R, which is described in the 'maximum interleaver memory' field of the R-MSG2 sent by the VTU-R." Ex. 1003 at ¶ 126. This misses the point.

The Mazzoni problem is not that the contract exceeds the VTU-R's maximum interleaver memory; it is that the contract exceeds the VTU-R's total memory (26,892 bytes) by providing settings that require an amount of VTU-R deinterleaver memory—which is not disclosed in any message or ever checked—in excess of what the VTU-R's fixed memory can support.

This problem results from Mazzoni's architecture. The reference uses a fixed memory that, at installation, is divided into dedicated interleaver and deinterleaver memory spaces based on selecting one of twelve fixed pairs. The messages in ETSI VDSL1 do not fit with that architecture. And, if applied in the manner CommScope advocates, would break Mazzoni by exceeding its fixed memory.

### 2. Fadavi-Ardekani And ETSI VDSL1

For similar reasons, CommScope fails to show that the combination of Fadavi-Ardekani and ETSI VDSL1 would be an operable system. Petitioner focuses on the "optimal" embodiment in Fadavi-Ardekani, arguing that the embodiment (with only 16 kilobytes of memory) can support 16 kilobytes of downstream memory and 2 kilobytes of upstream memory. Ex. 1003 at ¶¶ 215–16. However, a contract from ETSI VDSL1 based on the R-MSG2 and O-MSG2 messages (as Petitioner interprets the reference) that required more than 16 kilobytes of total memory—such as the full 18 kilobytes required for ADSL—would result in an inoperable system. This is because the Fadavi-Ardekani device will overwrite data still being used by the interleaver or deinterleaver during each system. Just like the Mazzoni combination, the Fadavi-Ardekani combination would exceed the fixed memory and not work.

## VI. Conclusion

TQ Delta respectfully requests that the Board deny institution.

Dated: February 21, 2023

Respectfully submitted,
THE DAVIS FIRM PC

By:/Christian J. Hurt/
Christian J. Hurt

## CERTIFICATE OF COMPLIANCE

I hereby certify that the foregoing Preliminary Response complies with the type-volume limitation and general format requirements pursuant to 37 C.F.R. §§ 42.24 and 42.6. I further certify that this response contains 11,602 words, excluding parts exempted by 37 C.F.R. §42.24. The word count is based on the word count of the Microsoft Word program used to prepare this petition.

Dated: February 21, 2023

/Christian J. Hurt/
Christian J. Hurt

## CERTIFICATE OF SERVICE

I hereby certify that on February 21, 2023, a true copy of the following document(s):

**PATENT OWNER TQ DELTA, LLC'S PRELIMINARY RESPONSE TO PETITION FOR *INTER PARTES* REVIEW OF U.S. PATENT NO. U.S. PATENT NO. 8,276,048**

was served via ***electronic mail*** to the address and parties as follows:

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I declare under penalty of perjury under the laws of the United States of America that the foregoing is true and correct. Executed on February 21, 2023 at Southlake, Texas.

/Christian J. Hurt/
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