

UNITED STATES DISTRICT COURT
DISTRICT OF DELAWARE

TQ Delta, LLC,

Plaintiff,

v.

2Wire, Inc.

Defendant.

Case No. C.A. No. 1:13-cv-01835-RGA

Jury Trial Demanded

CORRECTED REBUTTAL EXPERT REPORT OF DR. TODOR COOKLEV
REGARDING VALIDITY OF THE FAMILY 3 PATENTS

CONFIDENTIAL - ATTORNEYS' EYES ONLY

I declare under penalty of perjury that the following is true and correct.

JANUARY 4, 2019

DATE



Todor Cooklev, Ph.D.

TQ Delta Exhibit 2010
COMMSCOPE, INC. v. TQ DELTA LLC
IPR2023-00064

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I. INTRODUCTION

1. My name is Dr. Todor Cooklev, and I have been retained by TQ Delta LLC (“TQ Delta”).

2. I have been asked to prepare this report (“Rebuttal Report”) in connection with the above captioned District Court action between TQ Delta LLC and 2Wire, Inc. (“Defendant”). I have reviewed the report by Dr. Krista Jacobsen (“the Jacobsen Report”) submitted in this litigation on November 28, 2018. I address the Jacobsen Report in detail below. Specifically, I have been asked to opine on Dr. Jacobsen’s allegations that claim 1 of U.S. Patent No. 8,276,048 (“the ’048 patent”), claim 5 of U.S. Patent No. 7,836,381 (“the ’381 patent”), claim 13 of U.S. Patent No. 7,844,882 (“the ’882 patent”), and claim 19 of U.S. Patent No. 8,495,473 (“the ’473 patent”) are invalid. I will be referring to the above-mentioned claims, collectively, as the Asserted Claims, and to the above-mentioned patents, collectively, as the Asserted Patents or the Family 3 Patents.

3. My qualifications were described in detail in Section II of my opening report on the infringement of the Family 3 Patents submitted on November 28, 2018 (“Cooklev Inf. Report”), as well as in my curriculum vitae, which was attached to that Report as Exhibit 1.

4. I also incorporate my discussion of the Asserted Claims and claim constructions from my opening report. *See, e.g.*, Cooklev Inf. Report at §§ VII.D-F, X.

5. In coming to my conclusions, I reviewed the materials identified in Exhibit 1 to this Report, as well as all materials referenced in this Report.

6. As detailed below, based upon my personal knowledge, expertise, and the review and analysis I have performed to date, I have formed the following opinions:

7. Claim 1 of the '048 patent is valid. The claim covers patentable subject matter, is not obvious in view of the prior art as applied by Dr. Jacobson. The claim is supported by the specification's written description, enabled, and definite.

8. Claim 5 of the '381 patent is valid. The claim covers patentable subject matter, is not obvious in view of the prior art as applied by Dr. Jacobson. The claim is supported by the specification's written description, enabled, and definite.

9. Claim 13 of the '882 patent is valid. The claim covers patentable subject matter, is not obvious in view of the prior art as applied by Dr. Jacobson. The claim is supported by the specification's written description, enabled, and definite.

10. Claim 19 of the '473 patent is valid. The claim covers patentable subject matter, is not obvious in view of the prior art as applied by Dr. Jacobson. The claim is supported by the specification's written description, enabled, and definite.

11. I set forth below the bases and reasoning for these opinions. Specifically, I explain why Dr. Jacobson's opinions fail to invalidate the Asserted Claims on any basis. In doing so, I explain why each alleged prior art reference does not invalidate the Asserted Claims, by obviousness, and why the Asserted Claims are not invalid for lack of written description or enablement, or for indefiniteness.

12. I based this Report on information currently available to me. I reserve the right to expand, modify, or supplement my Report based on additional information, to the extent that information was not provided to me before this Report is due. I further

reserve the right to expand, modify, and/or supplement this Report and my opinions in response to matters raised by Defendant and/or Defendant's expert(s), opinions provided by other defendants and/or their expert(s) in related matters, or in view of relevant orders and findings by the Court.

13. In this Report, I cite to various documents and testimony. These citations are meant to be exemplary, and not exhaustive. Citations to documents or testimony are not intended to signify that my conclusions or opinions are limited to the cited sources, or supported by the cited sources only.

14. I expect to be available for deposition and to testify at trial in the above captioned actions. I reserve the right to perform demonstrations and use animations, demonstratives, and/or other physical evidence at trial. I expressly reserve the right to offer opinions at trial and/or in one or more supplemental reports on subjects raised in my deposition, as well as on matters raised by Dr. Jacobsen or by Defendant(s) in any subsequent report, at deposition, or at trial.

15. I am being compensated at \$400 per hour, which is my standard hourly consulting rate, plus reasonable expenses. I have not received any additional compensation for my work on this case, and no part of my compensation is dependent on my conclusions or on the outcome of the above captioned actions.

II. APPLICABLE LEGAL PRINCIPLES

16. I have reviewed Dr. Jacobsen's statements of legal standards that Dr. Jacobsen purportedly applied in forming her opinions. While I generally agree with the statements on the law, the summarizations overlook several important points that result

in misleading opinions. I have been informed by TQ Delta's counsel about the legal principles that I understand control the issues that Dr. Jacobsen opined on and which I rebut. I have applied these legal standards to the facts, circumstances, and materials considered, along with my experience, in reaching the conclusions and opinions expressed in this Report.

A. Presumption of Validity

17. It is my understanding that the claims of an issued U.S. patent are presumed valid. I further understand that the party challenging a patent claim's validity bears the burden of proving that claim invalid by clear and convincing evidence.

18. I understand that the standard for clear and convincing evidence is higher than the preponderance-of-evidence standard that is used to determine infringement. I am informed that the clear-and-convincing evidence standard requires an abiding conviction that the truth of a fact is highly probable.

19. I understand that this burden may be more difficult for a Defendant to meet if prior art was considered by the Examiner during the original prosecution of an Asserted Patent.

B. Anticipation

20. I understand the following principles apply for determining anticipation under 35 U.S.C. § 102. A patent claim is anticipated by prior art when each element of the claim is present within a single prior art reference. In addition, each element of the claim must be arranged in the prior art as it is in the claim. An element may be either

expressly disclosed or inherent in the prior art. A claim element is only inherent if it is necessarily present in the reference. I further understand that the possibility, even if probable, that an element may result from a certain set of circumstances – that is, an element *might* be present – is not sufficient to establish inherency.

21. I have been informed that, although anticipation cannot be established through a combination of references, additional references may be used to interpret the allegedly anticipating reference by, for example, indicating what the allegedly anticipating reference would have meant to one of ordinary skill in the art. For the claim to be anticipated, however, these other references must make clear that the missing descriptive matter in the patent claim is necessarily or implicitly present in the allegedly anticipating reference, and that it would be so recognized by one of ordinary skill in the art.

C. Obviousness

22. I understand the following principles apply for determining obviousness under 35 U.S.C. § 103. A claim may be invalid as obvious if the difference between the claimed subject matter and one or more prior art references are such that the subject matter as a whole would have been obvious at the time the invention was made to a person of ordinary skill in the art (“POSITA”). The following factors must be found and considered in determining obviousness: (1) the scope and content of the prior art; (2) the differences between the art and the claims at issue; (3) the level of ordinary skill in the art; and, (4) objective evidence of non-obviousness, which is also referred to as secondary considerations.

23. It is not enough that the prior art references can be combined; there must be a motivation to one of ordinary skill in the art to arrive at the claimed invention. But I also understand that motivation may not be gleaned from impermissible hindsight reasoning. That is, the reason to combine the prior art to arrive at the claimed invention cannot be based in whole or in part on the inventors' own disclosure.

24. I understand that assessing which prior art references to combine and how they may be combined to match the asserted claim may not be based on hindsight reconstruction. Hindsight reconstruction is using the patent itself as a road map for recreating the invention. In assessing obviousness, only what was known before the invention was made can be considered. I also understand that one important guard against such hindsight reconstruction is a determination whether a person of ordinary skill in the art would have been motivated, taught, or suggested to combine the relevant techniques of the prior art to duplicate the patent claims at the time of the patented invention.

25. I understand that obviousness cannot be predicated on the mere identification in the prior art of individual components of claimed limitations. It is not appropriate to pick and choose among the individual elements of assorted prior art references to recreate the claimed invention, but rather, there must be some teaching or suggestion in the references to support their use in the particular claimed combination.

26. I understand that it is the Defendant's burden to prove that a person of ordinary skill in the art would have been motivated to combine the prior art references. I understand that the motivation to combine must be supported by evidence and

articulated explanation. When considering obviousness, I understand that it is insufficient to simply say that a skilled artisan, once presented with a combination of references, would have understood that they could be combined.

27. Rather, the Defendant must show that the skilled artisan would have been motivated to make the combinations or modification of prior art to arrive at the claimed invention. Conclusory statements alone are insufficient, and any obviousness analysis must be supported by a reasoned explanation as to why a person of ordinary skill in the art would have been motivated to combine the prior art. For example, “common sense” or “intuition” alone cannot support a motivation to combine without explaining why they would lead a skilled artisan to solve the problem at hand with the particular elements of the claimed invention.

28. I understand that, to determine the scope and content of the prior art, I must consider whether the prior art was reasonably relevant to the particular problem the inventors faced in making the claimed invention.

29. To determine whether any material differences existed between the scope and content of the prior art and each asserted claim, I must consider the claimed invention as a whole to determine whether or not the claim would have been obvious in light of the prior art. If the prior art discloses all the elements in separate references, I must consider whether it would have been obvious to combine those references. I understand that a claim is not obvious just because all elements of a claim already existed.

30. I understand that a motivation to conduct further testing or research that may lead to the claimed invention does not necessarily render a claim obvious. I further understand that an invention is not necessarily rendered obvious simply because it was obvious to try a certain combination.

31. Secondary considerations may also impact a determination of obviousness, provided that there is some nexus or link between the claimed invention and the secondary factors considered. I further understand that any secondary factors that may prove instructive in determining non-obviousness should be considered. The following are examples:

- (1) a long-felt, but unmet need for the invention;
- (2) prior art teaching away from the invention;
- (3) failure of others to make the invention;
- (4) praise for the invention;
- (5) commercial success;
- (6) copying of the invention;
- (7) initial skepticism for the invention;
- (8) licensing;
- (9) whether the invention proceeded in a direction contrary to accepted wisdom in the field.

32. I understand that the inquiry into secondary considerations is a means to check hindsight analysis. I am informed that it is impermissible to use hindsight and that it is improper to focus on just one portion or element of the invention, as opposed to the invention as a whole.

33. I also understand that when prior art teaches away from combining prior art references, the discovery of a successful way to combine them is unlikely to be obvious. Prior art teaches away from an invention when a person of ordinary skill would be discouraged or diverted from following the path leading to the invention because of the prior art. I also understand that if a proposed combination would require modification of prior art and that modification would render the prior art unsatisfactory for its intended purpose, then there is no suggestion or motivation to make the proposed combination and modification.

D. Written Description

34. I understand the following legal principles apply to assessing whether a patent is invalid for not meeting the written description requirement in 35 U.S.C. § 112, ¶ 1. The written description requirement evaluates whether the patent applicant had possession of the full scope of the claimed invention at the time the patent application was filed. This evaluation is made from the perspective of one of ordinary skill in the art. Claims may be broader than the embodiment or embodiments identified in the specification, and the specification may contain adequate written description of a broadly claimed invention without expressly describing every embodiment the claim encompasses.

E. Definiteness and Enablement

35. I also understand that claims must be particular and distinct, which is also referred to as a definiteness requirement in 35 U.S.C. § 112, ¶ 2. This definiteness requirement provides that a patent applicant must particularly point out and distinctly

claim the subject matter that the applicant regards as the invention. The definiteness standard is one of reasonableness under the circumstances. In other words, in light of the teachings of the prior art and of the particular invention, the definiteness inquiry is whether the claims inform those skilled in the art about the scope of the invention with reasonable certainty.

36. The enablement requirement requires the inventor to describe his or her invention in a manner that would allow others in the industry to make and use the invention. To analyze enablement, one needs to take into account the knowledge of a POSITA.

37. I understand that a patent need not teach, and preferably omits, what is well known in the art. I also understand that resort to material outside of the specification in order to satisfy the enablement requirement is permissible because it makes no sense to encumber the specification of a patent with all the knowledge of the past concerning how to make and use the claimed invention. I further understand that the fact that some experimentation is necessary does not preclude enablement, but that any required experimentation must be reasonable. Some trial and error is permissible.

38. Further, I have been informed that enablement does not require the inventor to foresee every means of implementing an invention. Finally, I am informed that the specification need not necessarily describe how to make and use every possible variant of the claimed invention, for the artisan's knowledge of the prior art and routine experimentation can fill in any gaps, interpolate between embodiments, and even extrapolate beyond the disclosed embodiments.

F. Claiming Priority to A Provisional Application

39. I understand that a patent may be given the prior art date of the patent's provisional application. I am informed that a reference patent is entitled to claim the benefit of the filing date of its provisional application if the disclosure of the provisional application provides support for the claims in the reference patent.

III. PERSON OF ORDINARY SKILL IN THE ART

40. I defined a person of ordinary skill in the art with respect to the subject matter of the Family 3 Patents in Section VI.A of my Opening Infringement Report. I incorporate that definition by reference. *See* Cooklev Inf. Report at § VI.A.

IV. BACKGROUND OF DSL TECHNOLOGY AND INVENTION

41. I set forth a background of DSL communications, error correction, interleaver and deinterleaver memory, and the inventions of the Asserted Patents alongside with their benefits in Sections VII.A-F of my Opening Infringement Report. *See* Cooklev Inf. Report at §§ VII.A-F. I incorporate those sections by reference.

A. Interleaver Memory and Deinterleaver Memory in Prior Art Systems

42. DSL systems, such as, for example, ADSL2/2+ standards known at the time of the inventions, specify dedicated interleaving memory requirements in each transceiver separately for upstream and downstream transmission (i.e., in each direction separately). More specifically, an ADSL2/2+ ATU-C is required to have a specified amount of dedicated interleaving memory for downstream data transmission and separately and independently have a specified amount of dedicated interleaving memory for upstream data reception. ADSL2/2+ specifies that the ATU-C must have

enough dedicated memory for downstream interleaving to interleave codewords sizes of $N_{fec} = 255$ bytes with an interleaver depth of $D=64$. This corresponds to $N_{fec} \times D = 255 \times 64 = 16,320$ octets of dedicated interleaving memory for downstream. Likewise, ADSL2/2+ specifies that the ATU-C must separately have enough dedicated memory for upstream deinterleaving to deinterleave codewords sizes of $N_{fec} = 255$ bytes with an deinterleaver depth of $D=8$. This corresponds to $N_{fec} \times D = 255 \times 8 = 2,048$ octets of dedicated deinterleaving memory for upstream. The total interleaving + deinterleaving memory requirement for an ATU-C is therefore approximately $16K + 2K = 20K$. These requirements are specified (or derived from values provided) in Tables 7-7, 7-8, 7-9 and 7-10 of G.992.3/2002.

43. In the same manner, an ADSL2/2+ ATU-R is required to have a specific amount of dedicated interleaving memory for downstream data reception and separately have a specific amount of dedicated interleaving memory for upstream data transmission. Like the ATU-C, ADSL2/2+ specifies that the ATU-R must have enough dedicated memory for downstream deinterleaving to deinterleave codewords sizes of $N_{fec} = 255$ bytes with an deinterleaver depth of $D=64$. This corresponds to $N_{fec} \times D = 255 \times 64 = 16,320$ octets of dedicated deinterleaving memory for downstream. Like the ATU-C, ADSL2/2+ specifies that the ATU-R must have enough memory for upstream interleaving to interleave codewords sizes of $N_{fec} = 255$ bytes with an interleaver depth of $D=8$ for upstream. This corresponds to $N_{fec} \times D = 255 \times 8 = 2,048$ octets of dedicated interleaving memory. The total deinterleaving + interleaving memory requirement for

an ATU-R is therefore approximately $16,320 + 2,048 = 18,368$ octets. These requirements are specified in Tables 7-7, 7-8, 7-9 and 7-10 of G.992.3/2002.

44. The ADSL2/2+ standards do not specify or enable memory sharing between the interleaver and the deinterleaver in a single transceiver. Furthermore, since ADSL2/2+ specify that the ATU-C downstream interleaver and the ATU-R downstream deinterleaver have the same amount of memory (i.e., ~16K octets) there are no messages specified (or ever needed) to negotiate the amount of memory to be allocated to the interleaver (in the ATU-C) or to the deinterleaver (in the ATU-R). Likewise, since ADSL2/2+ specify that the ATU-R upstream interleaver and the ATU-C upstream deinterleaver have the same amount of memory (i.e. ~2K octets) there are no messages specified (or ever needed) to negotiate the amount of memory to be allocated to the interleaver (in the ATU-R) or to the deinterleaver (in the ATU-C).

45. Prior to the inventions disclosed in the Family 3 patents, an amount of memory available to an interleaver was predetermined and an amount of memory available to a deinterleaver was predetermined. Those systems were incapable of sharing memory between an interleaving and deinterleaving function based on a message.

B. Shared Interleaver and Deinterleaver Memory in the Family 3 Patent Inventions

46. The below examples illustrate how, even if one of the transceivers provided more memory than the minimum specified by a standard, the interleaver memory and the deinterleaver memory in a single transceiver had been implemented in

prior art systems before the inventions of the Family 3 patents in comparison with how the shared memory can be allocated to an interleaver and a deinterleaver according to the inventions of the Family 3 patents.

47. Generally, a transceiver (e.g., VTU-R) with a larger dedicated deinterleaver memory than is required could at most determine whether a transceiver (e.g., VTU-O) at the other line of the line can also support a larger amount. But, if the VTU-O does not support a larger amount than is required, however, the extra deinterleaver memory of the VTU-R is simply not used. For example, it is not available to be used for the upstream interleaver function. The examples described below illustrate this concept.

48. Example 1 (Prior Art Systems). VTU-O (30,000 octets of dedicated downstream interleaver memory; 30,000 octets of dedicated upstream deinterleaver memory). VTU-R (40,000 octets of dedicated downstream deinterleaver memory; 20,000 octets of dedicated upstream interleaver memory).

Legend:



dedicated downstream memory (interleaver memory for VTU-O,
deinterleaver memory for VTU-R)

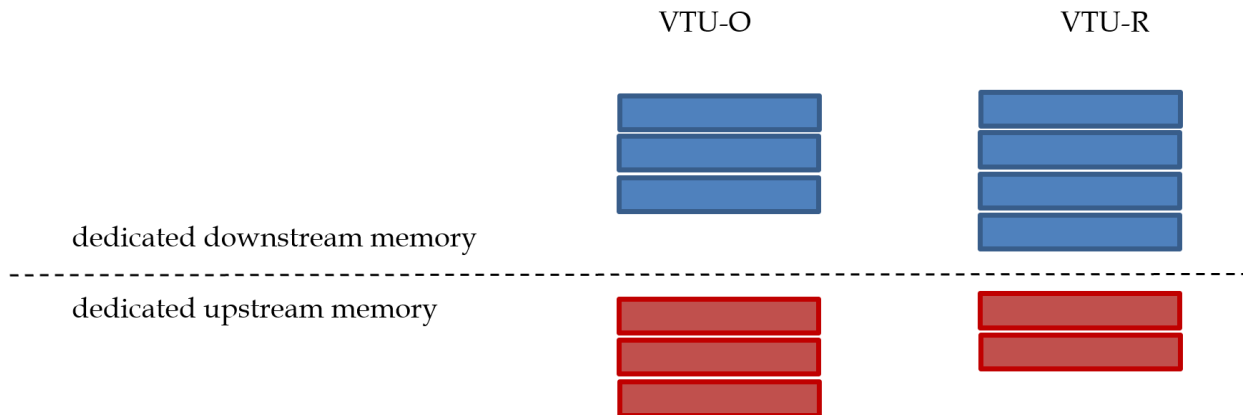


dedicated upstream memory (interleaver memory for VTU-R,
deinterleaver memory for VTU-O)

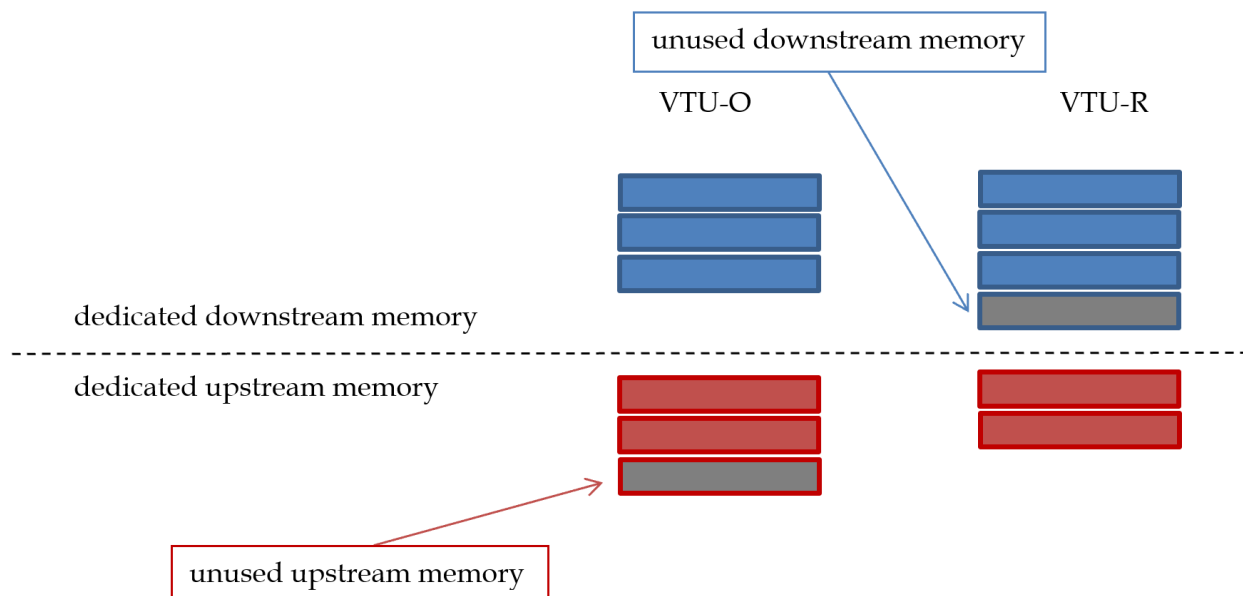
 unused memory

Each rectangle represents 10,000 octets of memory.

49. Capabilities (maximum memory supported):



50. Even if each transmitter exchanged their memory capabilities in each direction, the smaller of the transmitter and receiver capabilities in each direction would need to have been chosen. Because the smaller capability is selected, this results in a maximum possible memory allocation as shown below.



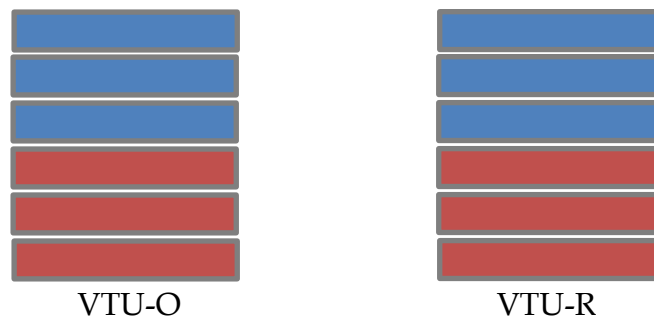
51. Also, because the smaller of the capabilities of the transmitter or receiver are selected in each direction, unused memory for one function in a transceiver cannot be used for another function, e.g., unused dedicated deinterleaver memory in the VTU-R cannot be used for the interleaving function. In the example above, 10,000 octets of deinterleaver memory within the VTU-R and 10,000 octets of deinterleaver memory in the VTU-O would never be used.

52. Under such implementation even though the VTU-R learned about the VTU-O's capabilities downstream, it could not use 10,000 octets of its 40,000 octets of memory that was dedicated to the downstream deinterleaver. Likewise, even though the VTU-O learned about the VTU-R's capabilities upstream, it could not use 10,000 octets of its 30,000 octets of memory that was dedicated to the upstream deinterleaver.

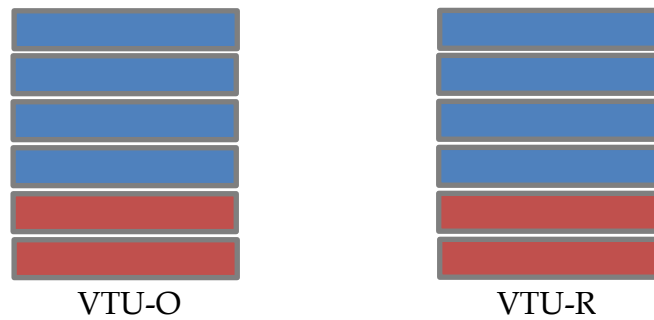
53. In this example, if a service provider is providing a VDSL2 service that requires 30,000 octets of memory in each transceiver for the downstream service and 20,000 octets of memory in each transceiver for the upstream service, the transceivers would be able to provide that service. If, however, a service provider is providing a VDSL2 service that requires 30,000 octets of memory in each transceiver for the downstream service and 30,000 octets of memory in each transceiver for the upstream service, the transceivers would NOT be able to meet the requirements of the service.

54. The above example can be contrasted with an example implementing the claimed allocation of memory between an interleaving function and a deinterleaving function according to the inventions of the Family 3 patents (Example 2, *infra*).

55. Example 2 (Family 3 Patents). Each transceiver supports a total of 60,000 octets of shared interleaver/deinterleaver memory. If the service provider desires to provide a VDSL2 service that requires 30,000 octets of memory in each transceiver for the downstream service and 30,000 octets of memory in each transceiver for the upstream service, the 60,000 octets of memory in each transceiver could be allocated between the interleaver and deinterleaver functions such that 30,000 octets in each transceiver are used for the downstream path and 30,000 octets are used for the upstream path as illustrated below.



56. On the other hand, if the service provider desires to provide a VDSL2 service that requires 40,000 octets of memory in each transceiver for the downstream service and 20,000 octets of memory in each transceiver for the upstream service, the 60,000 octets of memory in each transceiver could be allocated between the interleaver and deinterleaver functions such that 40,000 octets in each transceiver are used for the downstream path and 20,000 octets are used for the upstream path as illustrated below.



57. Therefore, unlike the prior art systems where 10,000 octets of memory are unused and the service provider could not provide the service to the customer, when shared memory, which can be allocated between the interleaver function or deinterleaver function, is used, memory that would otherwise go unused can be allocated to one function or the other depending on messages that are, in part, dependent on the service requirements. As illustrated by these examples, the VTU-R is capable of allocating 10,000 octets of its memory to the upstream interleaving function at one time but allocating the same 10,000 octets of its memory to the downstream deinterleaving function at another time. This provides flexibility that enables the transceivers to meet different service requirements.

C. References Cited in Jacobsen Report are Consistent with Implementations that Precede the Inventions of Family 3 Patents

58. Dr. Jacobsen asserts that prior art systems were capable of providing “shared memory that the transceiver can partition between its interleaver and deinterleaver on a per-connection basis. Use of shared memory for interleaving and

deinterleaving, including in DSL, was well known before the priority date of the Family 3 patents.” See Jacobsen Report at ¶ 72. This is incorrect.

59. To support her argument, Dr. Jacobsen cites to several prior art references. Yet, none of these references discloses what she asserts that they do.

60. Berkmann does not disclose providing “shared memory that can be partitioned between its interleaver and deinterleaver on a per-connection basis,” as Dr. Jacobsen asserts. See Jacobsen Report at ¶ 72. While Berkmann describes using “a combined interleaving and deinterleaving circuit,” (*id.* at Abstract), it further explains that “[o]nly the interleaving function $\alpha(i)$ (or, alternatively, the inverse deinterleaving function $\alpha^{-1}(i)$) must be implemented, but not both functions” (*id.* at ¶ 102). Without much further analysis of Berkmann needed, it is clear that regardless of whether the “combined interleaving and deinterleaving circuit” meets a definition of shared memory as construed by the Court (and it does not), it is not being partitioned *between* the interleaving function and the deinterleaving function, and it is not being partitioned on a *per-connection* basis. At most, Berkmann discloses a circuit for carrying out interleaving *or* deinterleaving, but not both, at the same time, which does not disclose shared memory as construed by the Court.

61. Fadavi-Ardekani does not disclose providing “shared memory that can be partitioned between its interleaver and deinterleaver on a per-connection basis,” as Dr. Jacobsen asserts. See Jacobsen Report at ¶ 72. As explained in, for example, Sections VI.C.1 and VI.C.2, *infra*. Fadavi only teaches that the interleaver and deinterleaver are each provided with a size of memory that “is derived by multiplying the maximum

codeword length by the maximum interleaver depth.” Fadavi at 7:9-10. Thus, Fadavi teaches using dedicated memories for the interleaving function and deinterleaving function. Also, as explained in those sections, the disclosed “ping-pang” operation does not meet the shared memory requirement, nor is it the memory assigned on per-connection basis.

62. Kang does not disclose providing “shared memory that can be partitioned between its interleaver and deinterleaver on a per-connection basis,” as Dr. Jacobsen asserts. *See* Jacobsen Report at ¶ 72.

63. Mazzoni does not disclose providing “shared memory that can be partitioned between its interleaver and deinterleaver on a per-connection basis,” as Dr. Jacobsen asserts. *See* Jacobsen Report at ¶ 72. As explained in, for example, Sections VI.B.1, VI.B.3.a, and VI.B.3.b, *infra*, Mazzoni describes the assignment of interleaver memory and deinterleaver memory for predefined data rate pairs (services) by using predefined I and M parameter values for its interleaving means, and predefined I’ and M’ parameter values for deinterleaving means for each data rate pair (i.e., service). *Id.* at 5:24-30. Also, as explained in the cited sections, the assignment is performed at the time of an installation of the modem, and not per-connection basis. *See* Mazzoni at 6:51-61.

64. Voith does not disclose providing “shared memory that can be partitioned between its interleaver and deinterleaver on a per-connection basis,” as Dr. Jacobsen asserts. *See* Jacobsen Report at ¶ 72. As explained in Sections VI.E.1 and VI.E.2, *infra*.

Voith merely teaches use of an external memory. Voith does not teach that the external memory is “shared memory.”

V. THE ASSERTED CLAIMS OF THE FAMILY 3 PATENTS ARE VALID

65. As set forth in this Rebuttal Report, it is my opinion and conclusion that each Asserted Claim of the Family 3 Patents are not invalid in view of the alleged prior art as asserted in the Jacobsen Report.

66. In performing my analysis, I have compared the limitations of each Asserted Claim with the disclosure in the alleged prior art references. I have also considered the scope and content of the prior art, the differences between the prior art and the claimed invention, the level of ordinary skill in the art at the time of the invention, and whether the differences are such that the claimed invention as a whole would have been obvious to one of ordinary skill in the art at the time the invention was made.

67. In my analysis below, I have applied, where applicable, the Court’s claim construction. *See* Cooklev Inf. Report at § X.

A. Claim 19 of the ‘473 patent is valid under 35 U.S.C. § 112, ¶2

68. Dr. Jacobsen asserts that:

[C]laim 19 of the ‘473 patent is indefinite. Claim 19 recites the limitation ‘wherein at least a portion of the memory may be allocated to the interleaving function or the deinterleaving function at any one particular time depending on the message.’ One of ordinary skill in the art would not have known with reasonable certainty whether a portion of the memory actually has to be allocated to an interleaving function at one time, and a deinterleaving function at another, or whether the mere possibility that some portion of the memory could possibly be allocated to

the interleaving or deinterleaving function suffices to meet the claim language.”

Jacobsen Report at ¶ 151 (emphasis in original).

69. I disagree with Dr. Jacobsen’s conclusion as well as with the arguments she presents to support her position as explained below.

70. Dr. Jacobsen’s arguments are premised on the assertion that the “Court determined that this language should have its plain meaning during claim construction.” Jacobsen Report at ¶ 151. While it is true that the Court gave plain meaning to this claim term, the Court also provided context for this claim language, which Dr. Jacobsen ignores in her analysis. Specifically, the Court noted:

The claim language does not require that the message specify amounts of memory. The disputed term’s language requires that the amount of memory depend on the message’s contents, but it does not require that the message’s contents themselves actually specify amounts of memory.

Claim Construction Memorandum for Family 3 Patents (Dec. 18, 2017), D.I. 445, (“CC Memo”) at p. 10.

71. Dr. Jacobsen ignores the Court’s guidance in reaching her conclusion that:

It is not clear from the intrinsic record, however, whether this allocation actually has to happen, at some point, in order for a device to infringe. For example, a system could use a shared memory in such a way that it is theoretically possible that a portion of the memory is allocated to a deinterleaver or an interleaver, depending on the message, but it might not actually ever happen in practice. One of ordinary skill in the art would not have understood whether such a system would infringe claim 19 of the ’473 patent.

Jacobsen Report at ¶ 152.

72. As an initial matter, Dr. Jacobsen refers to the “claims, specification, and file history” as purportedly supporting her unfounded argument. Yet, Dr. Jacobsen

does not explain how either supports her conclusion. In fact, Dr. Jacobsen does not quote from or cite to the claims, specification, or the file history.

73. In any event, Dr. Jacobsen's assertion indicates that she misunderstands the scope of an apparatus claim that defines structure in functional terms. I understand that an apparatus claim is infringed when the accused apparatus is capable of infringement. Therefore, the answer to Dr. Jacobsen's question about the scope of the claim is that the claimed allocation does not actually have to happen in order for the claim to be infringed. Rather, the claim is infringed by transceivers that are capable of allocating at least a portion of the memory to the interleaving function or the deinterleaving function at any one particular time depending on the message.

74. A POSITA would understand that this claim language, as even the Court agreed, requires only that the function to which the portion of memory is allocated at one particular time depends on the message's contents. The use of the term "may" does not render the scope of the claim indefinite. Rather, "may" is the most appropriate term given that the claim provides two possibilities on its face – that, depending on the message, (1) the portion of memory be allocated to the interleaver function at a particular time, or (2) the portion of memory be allocated to the deinterleaver function at a particular time. A transceiver that is not capable of allocating at least some portion of memory to interleaving at one time and allocating that same portion to deinterleaving at another time would not infringe. A transceiver that is capable of doing so, such as the Accused Products, would infringe. Thus, claim 19 the '473 patent

informs those skilled in the art about the scope of the invention with reasonable certainty.

75. I note that 2Wire did not raise this indefiniteness argument during claim construction, and in fact proposed a claim construction that literally included the phrase “memory may be allocated.” CC Memo at 9-10 (2Wire’s proposed construction: “wherein at least a number of bytes within the memory may be allocated to the [first] interleaving function or the [second interleaving / deinterleaving] function at any one particular time depending on the amounts of memory specified in the message.”). While I do not agree that 2Wire’s proposed claim construction is accurate, 2Wire and Dr. Jacobsen had no problem proposing a construction that included this phrase verbatim. One must assume that 2Wire would not have proposed an indefinite construction for this claim element.

76. For the foregoing reasons, it is my opinion that claim 19 of the ’473 patent is definite and that Dr. Jacobsen has not proven otherwise.

B. Written Description and/or Enablement under 35 U.S.C. § 112, ¶1

77. The Court construed the term “the shared memory allocated to the [deinterleaver / interleaver] is used at the same time as the shared memory allocated to the [interleaver / deinterleaver]” to mean “the deinterleaver reads from, writes to, or holds information for deinterleaving in its respective allocation of the shared memory at the same time as the interleaver reads from, writes to, or holds information for interleaving in its respective allocation of the shared memory.” Dr. Jacobsen contends

that this term lacks written description and enablement. Jacobsen Report at ¶ 153. I disagree.

78. Dr. Jacobsen acknowledges that “[t]he specification describes sharing resources, such as memory and processing power, as well as ways of allocating those shared resources.” Jacobsen Report at ¶ 154. She asserts, however, that the specification purportedly does not “describe or explain how shared memory that is allocated to an interleaver and a deinterleaver can be used at the same time, or even what “used at the same time” even means. As an initial matter, I understand that there is no requirement that the specification describes what “used at the same time means” as long as the plain meaning of the claim language is understood in view of the specification. That is the case here. “Used at the same time” is a common and well understood term in general and one of skill in the art understands what it means to “use” memory. In any event, 2Wire agreed to the Court’s construction of this term. CC Memo at p. 9.

79. Further, a POSITA would know how memory that is allocated to two different functions can be “used at the same time.” While Dr. Jacobsen asserts that one of skill in the art would not know how this can be done, she does not explain why this is so. In any event, I disagree with her unsupported assertion. The simultaneous use of memory by multiple functions was a well-known process at the time of the inventions. A POSITA at that time would know how two or more functions can simultaneously use the same memory by storing information for a first function at the same time that information for a second function is stored in the memory, or written to the memory, or

read from the memory. This is inherent in any multi-threaded operation that uses the same memory.

80. Dr. Jacobsen asserts that the specification does not explain how memory allocated to an interleaver and memory allocated to a deinterleaver can be used at the same time. Jacobsen Report at ¶ 154. I understand that such explanation in the specification is not required. Rather, I understand that a patent need not teach, and preferably omits, what is well known in the art. I also understand that resort to material outside of the specification in order to satisfy the enablement requirement is permissible because it makes no sense to encumber the specification of a patent with all the knowledge of the past concerning how to make and use the claimed invention. Therefore, it was not necessary to provide a full and detailed explanation where, as here, a POSITA would know how to implement the claim.

81. As for Dr. Jacobsen's assertion that there is no written description support for "the shared memory allocated to the [deinterleaver / interleaver] is used at the same time as the shared memory allocated to the [interleaver / deinterleaver]," I disagree. Jacobsen Report at ¶ 155. 2Wire actually took the opposite position in its claim construction briefing:

Defendants' proposed construction correctly reflects that the shared memory is read to and written from at the same time by the interleaver and the deinterleaver. Defendants' proposed construction is consistent with the specification, which discloses that "the transmitter and/or receiver latency paths of the transceiver can share an interleaver/deinterleaver memory and the shared memory can be allocated to the interleaver and/or deinterleaver of each latency path."

Parties' Joint Claim Construction Brief for the Family 3 Patents, D.I. No. 353, at p. 58. Additional disclosure that shows that the patent applicant had possession of this element of the claimed invention at the time the patent application was filed is found at, e.g., U.S. Patent 7,831,890¹ patent at, e.g., Fig. 1 (illustrating shared memory 120 that services at least two interleaving functions and two deinterleaving functions); 6:56-64 and 7:7-25 (explaining that "the transmitter portion and/or receiver portion latency paths would be reconfigured to utilize the shared memory" and describing simultaneous transmitting/encoding and decoding/receiving of the latency paths); 8:11-39 (describing simultaneous use of different portions of a shared memory for various applications).

82. Dr. Jacobsen also asserts that the Family 3 patents lack written description support "wherein at least a portion of the memory may be allocated to the interleaving function or the deinterleaving function at any one particular time depending on the message." She does not provide any explanation of why this is so. In any event, I disagree. Disclosure that shows that the patent applicant had possession of this element of the claimed invention at the time the patent application was filed is found generally because the specification discloses the use of "shared memory" by an interleaver and a deinterleaver where the Court interpreted shared memory to mean "common memory used by at least two functions, where a portion of the memory can be used by either one of the functions." CC Memo at p. 5. A POSITA would understand from the disclosure

¹ The '890 patent is the original, non-provisional application in the chain with the asserted Family 3 patents.

of shared memory that the portion of shared memory that is allocated to an interleaver would not be used at the same time by a deinterleaver but, instead, could be used at alternative times depending on the allocation in effect at the time.

83. I reserve the right to address any support or explanation Dr. Jacobsen's attempts to provide for her currently conclusory assertions regarding written description and enablement.

84. Based on the foregoing, it is my opinion that the claim 1 of the '048 patent, claim 5 of the '381 patent, and claim 13 of the '882 patent satisfy the written description and enablement requirements.

C. Certificate of Correction

85. I disagree with Dr. Jacobsen's opinion that the "Certificate of Correction changed the scope and meaning of the '381 and '882 patent." Jacobsen Report at ¶ 160. The certificate of correction was properly issued by the patent office to correct obvious typographical errors. Claim 5 of the '381 patent as corrected provides in relevant part:

5. A non-transitory computer-readable information storage media having stored thereon instructions, that if executed by a processor, cause to be performed a method for allocating shared memory in a transceiver comprising:

allocating, in the transceiver, a first number of bytes of the shared memory to the deinterleaver to deinterleave a first plurality of Reed Solomon (RS) coded data bytes for transmission reception at a first data rate, wherein the allocated memory for the deinterleaver does not exceed the maximum number of bytes specified in the message;

allocating, in the transceiver, a second number of bytes of the shared memory to an interleaver to interleave a second plurality of RS coded data bytes received transmitted at a second data rate;

86. I have reviewed the specification and it is my opinion that based on the specification, it is clear that the errors were clerical or typographical. Specifically, FIG. 1 of the specification depicts an interleaver as being associated with transmitting and the deinterleaver as being associated with reception. On the other hand, the specification is not consistent with Dr. Jacobsen's hypothetical device that deinterleaves RS coded data bytes before transmitting them and receives RS coded data bytes before interleaving them. Indeed, the best Dr. Jacobsen can say is that the Family 3 patents "do not appear to foreclose either of these possibilities."

87. Dr. Jacobsen's suggests that the statement in the specification that "the invention can be applied to any transceiver having any number of latency paths" somehow precludes the correction. I disagree. That statement merely means that a transmitter of a transceiver can have any number of latency paths and the receiver of the same transceiver can have any number of latency paths. For example, a CO transmitter could have one or two downstream latency paths to the CPE and one or two upstream latency paths from the CPE.

88. Dr. Jacobsen's assertion that "a person of ordinary skill in the art would [not] have considered the terms 'transmission' and 'received' in claim 5 of the '381 patent and claim 13 of the '882 patent to be typographical errors" is not credible, especially so in light of the statements made elsewhere in the Jacobsen Report. For example, at ¶ 55 of the Jacobsen Report, Dr. Jacobsen concedes that "[t]o apply interleaving, the transmitter shuffles consecutive bytes of the data stream in a known and systematic way before transmitting them" See also, Jacobsen Report at ¶ 60 (".

. . . transmitter interleaves the bytes prior to transmission.”). Thus, Dr. Jacobsen recognizes that bytes are interleaved prior to being “transmitted.” Dr. Jacobsen also admits that “the receiver . . . can reverse the interleaving process by collecting all of the interleaving data elements and using a complementary deinterleaving process.” Jacobsen Report at ¶ 58. Thus, Dr. Jacobsen recognizes that bytes are deinterleaved after “reception.”

89. Accordingly, her assertion that the errors were not typographical (or that they would not have been recognized as typographical) is meritless.

VI. ANALYSIS OF THE CITED REFERENCES

A. The Asserted Claims Are Not Obvious Over LB-031

90. It is my opinion and conclusion that LB-031 alone or in combination with other cited references fails to disclose or suggest each element of the Asserted Claims, and hence fails to render the Asserted Claims anticipated or obvious as described in detail, below.

91. It is also my opinion that regardless of the disclosure of LB-031 and the other cited references, a person of ordinary skill in the art would not be motivated to combine the teachings of LB-031 with the teachings of the other cited references at least for the reasons described in Section VI.A.2.a, *infra*.

1. Overview of LB-031

92. LB-031 focuses on defining an interleaver delay in units of time to allow reduced interleaver complexity at lower data rates. *See* LB-031 at 3 (2WIRE00030959) (“Therefore, it seems prudent to define the interleaver complexity requirements in a

way that will allow those who want to deploy VDSL2 at lower speeds to do so at a reduced complexity with respect to higher speed implementations. The way to do this and to guarantee some minimum level of performance is to specify the interleaver complexity in terms of the delay in time.”).

93. LB-031 notes that the delay in time is proportional to the interleaver depth and to the codeword size and inversely proportional to the data rate. *Id.*

94. LB-031 describes memory requirements for an “interleaver/deinterleaver pair.” *See, e.g.,* LB-031 at 2 (2WIRE00030958) (“The smallest amount of memory required to build an interleaver/deinterleaver pair is equal to the total delay of the interleaver/deinterleaver. Typically, for memory optimized interleavers, the interleaver and deinterleaver memory size is nearly the same.”). *See also* § VI.A.2, *infra*. The interleaver of this “pair” is located in the transmitter lineup of one transceiver, while the deinterleaver of the “pair” is located in the receiver lineup of the other transceiver. The “pair” are associated with a single latency path and direction, i.e., a single path in the upstream direction or a single path in the downstream direction.

95. While LB-031 acknowledges that “[t]he size of the interleaver memory will be a major source of complexity in VDSL2,” it does not describe the combined memory requirements of an interleaver associated with one direction (e.g., upstream) and deinterleaver associated with the other direction (e.g., downstream) within a single transceiver. Nor does it describe sharing a memory between an interleaver and deinterleaver in a single transceiver as called for by the Asserted Claims of the Family 3 Patents and as described in more detail in VI.A.2, *infra*, and IV.A-IV.B, *supra*. Instead,

LB-031 focuses on selecting an amount of interleaver or deinterleaver memory for a single direction (i.e., by comparing capabilities of the transmitter on one end of a communication channel with the capabilities of the receiver on the other end). *See, e.g.*, LB-031 at 3 (2WIRE00030959). The relevant portion of LB-031 is quoted below:

For interoperability reasons, the VTU-O and VTU-R must exchange the interleaver delay in terms of octets. The requirement is that the interleaver delay in octets be sufficient to satisfy the smallest maximum delay even at the highest supported data rate. If a VDSL2 implementation supports a larger interleaver memory than is required, it should be free to specify the larger value. The VTU-O and VTU-R would then select the smaller of the transmitter and receiver capabilities, in each direction, as the end-to-end capabilities.

Id.

96. Contrary to Dr. Jacobsen's opinion, there is nothing in LB-031 that would suggest to a POSITA that a memory is being shared, or should be shared, between an interleaver and a deinterleaver in a single transceiver.

97. At least for these reasons, and for the reasons described in detail below, it is my opinion and conclusion that LB-031 fails to disclose or suggest all element of the Asserted Claims, and hence fails to render the Asserted Claims obvious.

2. LB-031 Does Not Render Claim 1 of the '048 Patent Obvious

98. It is my opinion and conclusion that LB-031 alone or in combination with other cited references fails to disclose or suggest each element of claim 1 of the '048 patent, and hence fails to render the Asserted Claims anticipated or obvious as described in detail, below.

a. LB-031 does not disclose a system that allocates shared memory.

99. Contrary to Dr. Jacobsen's assertion, the LB-031 reference does not disclose a system that allocates shared memory. *See* Jacobsen Report at ¶¶ 179-181. Dr. Jacobsen has not pointed to any portion of LB-031 that states, or that would have disclosed to a POSITA that a transceiver implementing the LB-031 reference allocates shared memory.

100. Dr. Jacobsen points to Eq. 1 and Eq. 5, and corresponding descriptions in the LB-031 reference to assert that a POSITA "would have understood this example to teach allocating memory for interleaving and deinterleaving." *See* Jacobsen Report at ¶ 180. As an initial matter, this statement is vague because it is not clear whether it is intended to describe the memory of a single transceiver or, on the other hand, the separate memories of a respective interleaver in one transceiver and corresponding deinterleaver in a second transceiver. To the extent she intends the latter, such teaching is not relevant to any asserted claim of the Family 3 patents because the claims are directed to allocating a shared memory between and interleaver and deinterleaver within a single transceiver. To the extent she intends the former, her statement is incorrect.

101. The disclosure of LB-031 Dr. Jacobsen relies on for purportedly disclosing allocating a shared memory is the passage on page 4 of LB-031, which states "[i]f the minimum interleaver delay requirement were 5.23 ms, then, from equation (5) and equation (1), this transceiver must support a delay of at least 29092 octets which corresponds to having an interleaver memory of at least 14546 octets according to

equation (2).” *See* Jacobsen Report at ¶ 180. This discussion in LB-031, however, has nothing to do with sharing memory or allocating a shared memory. Rather, it is describing the memory requirements for an interleaver in one transceiver and the corresponding memory requirements for a deinterleaver in a second transceiver at the other end of the communication channel. As the reference discloses, for an end-to-end delay of 29092 octets, the interleaver memory in one transceiver would have to be 14546 octets (i.e., bytes). The deinterleaver memory for the corresponding deinterleaver in the transceiver at the other end of the communication channel would also be 14546. The memory requirements are the same for the interleaver and corresponding deinterleaver because the deinterleaver will deinterleave the interleaved byte stream that was interleaved by the interleaver.

102. Yet, Dr. Jacobsen omits the fact that the equations of LB-031 are to be used to separately characterize the delay and memory requirements for a single latency path/direction. *See id.* These equations do not characterize the combined memory requirements for a single transceiver that requires memory for an interleaver for a first latency path/direction and a deinterleaver for a second latency path/direction. The equations are not concerned with the combined memory limit of any single transceiver or with sharing or allocating that combined limit between an interleaver and a deinterleaver. Rather, LB-031 is perfectly consistent with the practice at the time of using a dedicated, fixed-size interleaver memory and a separate, dedicated, fixed-size deinterleaver memory within a transceiver. As explained in Section VI.A.1, *supra*, LB-

031 falls within the category of dedicated interleaver and deinterleaver memory implementations. *See also* § IV.A, *supra*.

103. I note that Dr. Jacobsen understands that DSL transceivers generally transmit/interleave in one direction while they are receiving/deinterleaving in the other direction.² *See, e.g.*, Jacobsen Report at ¶ 207 (“VDSL transceivers transmit and receive data at the same time (i.e., VTU-O transmits data downstream and receives data upstream at the same time, and the VTU-R transmits data upstream and receives data downstream at the same time.”). She ignores or attempts to confuse this fundamental detail, however, when comparing the preamble (and notably all the other elements of the claims, except the last) to the LB-031 reference.

104. The claim construction of the term “shared memory” further supports the fact that LB-031 does not disclose shared memory, or allocating shared and consequently does not disclose a system for allocating shared memory. Specifically, the Court construed “shared memory” to mean “common memory used by at least two functions, where a portion of the memory can be used by either one of the functions.” Claim Construction Order for Family 3 Patents (December 28, 2017) (“CC Order”) at p. 2.

105. The second portion of the construction (i.e., that “a portion of [the shared] memory can be used by either function”) means that the shared memory is a memory of a single transceiver. For example, the two functions in the context of the claim (and in

² This is not the case, however, when the transceiver provides only half-duplex communications, i.e., the transceiver transmits but does not receive at some times and receives but does not transmit at other times.

the context of the asserted claims of the Family 3 patents generally) are interleaving and deinterleaving. The concept of use of a portion of memory by either one function or the other function has been described in Section VI.A.5.b, *infra*. See also § IV.A, *supra*. As discussed in connection with the '473 patent, *infra*, the interleaving function and corresponding deinterleaving function of the other transceiver specifically discussed in LB-031 use entirely different memories in different transceivers. No portion of memory within a single transceiver is disclosed by LB-031 to be used by an interleaver at one time or a deinterleaver at another time. See § VI.A.5.b.

106. Second, Dr. Jacobsen inappropriately extends the actual disclosure and teachings of the LB-031 reference by making an inherency argument that contradicts her other arguments. See Jacobsen Report at ¶ 181. Dr. Jacobsen asserts that “one of ordinary skill in the art would have understood from the disclosures of LB-031 that the allocated memory can be a shared memory.” See *id.* This is incorrect. First, Dr. Jacobsen has not identified any disclosure in LB-031 that requires that a shared memory is used or that any portion of memory within a single transceiver can be used by the interleaver or the deinterleaver. Rather, again, LB-031 is perfectly consistent with the practice of its time, which was to use a dedicated, fixed-size interleaver memory and a separate, dedicated, fixed-size deinterleaver memory in a transceiver. See § VI.A.5.a, *infra*; see also §§ IV.A, and IV.B, *supra*. Thus, no portion of a memory can be used by either an interleaver or a deinterleaver (i.e., no portion of the dedicated interleaver memory will ever be used by the deinterleaver and no portion of the dedicated deinterleaver memory will ever be used by the interleaver.).

107. Further, Dr. Jacobsen recognizes that LB-031 explains that “[t]he size of the interleaver memory will be a major source of complexity in VDSL2.” See Jacobsen Report at ¶ 181 (citing LB-031 at 3.). This statement does not state or suggest that size or complexity can be reduced by sharing memory. Rather, this statement would discourage a POSITA from attempting to add further complexity to interleaver memory in VDSL2, such as by proposing a memory sharing scheme. See also, e.g., LB-031 at 3 (2WIRE00030959) (“Therefore, it seems prudent to define interleaver complexity requirement in a way that will allow those who want to deploy VDSL2 at lower speeds to do so that at a reduced complexity with respect to higher speed implementations.”).

108. Therefore, I do not agree that a POSITA would understand “from the disclosures of LB-031 that the allocated memory can be a shared memory,” as Dr. Jacobsen incorrectly asserts, because a shared memory implementation would increase and not decrease the complexity of the implementation proposed by the LB-031 reference. See Jacobsen Report at ¶ 181.

109. I also disagree with Dr. Jacobsen’s assertion that “it was well known by the priority date of the Family 3 patents that an interleaver and deinterleaver memory could share a memory.” See Jacobsen Report at ¶ 181. I address this in Sections IV.A, IV.B, and IV.C, *supra*. Additionally, and *arguendo*, even if any of the string-cited references in paragraph 182 of the Jacobsen Report disclose a system for sharing memory as construed by the Court (which they do not), Dr. Jacobsen fails to explain why a POSITA would look to any of these references to increase complexity of the implementation of the LB-031 disclosure. Rather, as I have explained immediately

above, a POSITA would be discouraged from adding complexity to the memory requirement specifying scheme of LB-031. Consequently, there would be no motivation to combine any of the references cited in Paragraphs 182 of the Jacobsen Report with LB-031. And Dr. Jacobsen supplies none.

110. Because the LB-031 reference does not disclose, teach, or suggest a system that allocates sheared memory, it does not render claim 1 of the '048 patent anticipated or obvious. Also, because a person of ordinary skill in the art would not have understood from the teaching of the LB-031 reference to require a use of a shared memory, the LB-031 reference does not render claim 1 of the '048 patent anticipated or obvious. Finally, because a person of the ordinary skill in the art would not be motivated to combine the teaching of the LB-031 reference with the teaching of any other references cited by Dr. Jacobsen, and in fact, would be discouraged to do so, the LB-031 reference in combination with any of those references or in combination with the knowledge of one of ordinary skill in the art at the time of the invention of the Family 3 patents, does not render claim 1 of the '048 patent obvious.

b. LB-031 does not disclose determining an amount of memory required by the interleaver to interleave a first plurality of Reed Solomon (RS) coded data bytes within the shared memory.

111. LB-031 does not disclose this claim element.

112. Dr. Jacobsen ignores the requirement of this claim element that calls for a “shared memory” and instead irrelevantly quotes the portions of LB-031 describing the memory requirements for an interleaver in one transceiver and a corresponding memory requirement for a deinterleaver in another transceiver (and not an

implementation in a single transceiver with a shared memory). *See* Jacobsen Report at ¶ 192.

113. At least because LB-031 is not directed to allocating shared memory described in § VI.A.1 and § VI.A.2.a, *supra*, the LB-031 reference does not disclose, teach, or suggest this claim element. *See* § VI.A.5.a, *infra*; *see also* §§ IV.A, and IV.B, *supra*.

114. Because LB-031 does not disclose, teach, or suggest determining an amount of memory required by the interleaver to interleave a first plurality of Reed Solomon (RS) coded data bytes within the shared memory, it does not render claim 1 of the '048 Patent obvious.

c. LB-031 does not disclose allocating a first number of bytes of the shared memory to the interleaver to interleave a first plurality of Reed Solomon (RS) coded data bytes for transmission at a first data rate.

115. LB-031 does not disclose, teach, or suggest this claim element.

116. As with the previous claim element, Dr. Jacobsen yet again ignores the requirement of this claim element that calls for a “shared memory.” *See* Jacobsen Report at ¶¶ 194-195. The claim overall, and also this element in particular, calls for allocating bytes of a shared memory. LB-031 lacks disclosure of a shared memory as construed by the Court. *See* §§ VI.A.1, VI.A.2.a. *See also* § VI.A.5.a, *infra*; *see also* §§ IV.A, and IV.B, *supra*.

117. Dr. Jacobsen relies on a passage from LB-031 describing an exchange between a VTU-O and VTU-R of capabilities (i.e., a VTU-R and VTU-O will select “the

smaller of the transceivers and receiver capabilities in each direction.”). But the implementation details are all described in the context of the interleaver/deinterleaver pair for a single direction, e.g., interleaver capabilities of the VTU-O and deinterleaver capabilities of the VTU-R for the downstream direction. While the exchange of capabilities allows the transceivers to use only up to the amount of memory that is the lesser of the amount of interleaver memory in the VTU-O or the amount of deinterleaver memory in the VTU-R, there is no contemplation or discussion of sharing memory within a single transceiver depending on the exchanged capabilities. Thus, Dr. Jacobsen’s conclusion that a “shared memory” is being allocated is not supported by the LB-031 reference. *See* Jacobsen Report at ¶ 194; *see also* LB-031 at 2 (2WIRE00030958). Again, as explained in §§ VI.A.1, VI.A.2.a, *supra*, the disclosure of the LB-031 reference is not directed to shared memory. *See also* § VI.A.5.a, *infra*; *see also* §§ IV.A, and IV.B, *supra*.

118. Because LB-031 does not disclose, teach, or suggest allocating a first number of bytes of the shared memory to the interleaver to interleave a first plurality of Reed Solomon (RS) coded data bytes for transmission at a first data rate, it does not render claim 1 of the ‘048 Patent obvious.

d. LB-031 does not disclose wherein the allocated memory for the interleaver does not exceed the maximum number of bytes in the message.

119. LB-031 does not disclose this limitation at least because, as I explain in Section VI.A.2.a, *supra*, it does not disclose allocating memory to an interleaver (or a deinterleaver.)

120. Because LB-031 does not disclose, teach, or suggest transmitting or receiving a message during initialization specifying a maximum number of bytes of memory that are available to be allocated to an interleaver, it does not render claim 1 of the '048 patent obvious.

e. LB-031 does not disclose allocating a second number of bytes of the shared memory to a deinterleaver to deinterleave a second plurality of RS coded data bytes received a second data rate.

121. LB-031 does not disclose, teach, or suggest this claim element.

122. Dr. Jacobsen makes the same arguments for this claim element as for the element discussed in Section VI.A.2.c, *supra*, all of which have been addressed in the same section, *supra* and are incorporated by reference with respect to this claim element.

123. As with the previous element, LB-031 lacks disclosure of shared memory as construed by the Court. Therefore, LB-031 cannot disclose or suggest this claim element. *See* §§ VI.A.1, VI.A.2.a; *see also* § VI.A.5.a, *infra* and §§ IV.A and IV.B, *supra*.

124. Again, the implementation details of LB-031 are all described in the context of the interleaver/deinterleaver pair for a single direction, e.g., interleaver capabilities of the VTU-O and deinterleaver capabilities of the VTU-R for the downstream direction. There is no disclosure or contemplation of sharing a memory within a single transceiver for an interleaver operating in a first direction and a deinterleaver operating in a second direction. Thus, even assuming, *arguendo*, that LB-031 discloses “allocating a first number of bytes of” a non-shared memory “to the interleaver to interleave a first plurality of Reed Solomon (RS) coded data bytes for transmission at a first data rate,” there is no disclosure or contemplation of “allocating

a second number of bytes of” the same memory “to a deinterleaver to deinterleave a second plurality of RS coded data bytes received a second data rate.” The deinterleaving of “a second plurality of RS coded data bytes received at a second data rate” recited in the claim is necessarily referring to communications made in the other direction. LB-031 does not describe sharing memory between an interleaver for one direction and a deinterleaver for the other direction.

125. Because LB-031 does not disclose, teach, or suggest allocating a second number of bytes of the shared memory to a deinterleaver to deinterleave a second plurality of RS coded data bytes received a second data rate, it does not render claim 1 of the ‘048 Patent obvious.

- f. **LB-031 does not disclose interleaving the first plurality of RS coded data bytes within the shared memory allocated to the interleaver and deinterleaving the second plurality of RS coded data bytes within the shared memory allocated to the deinterleaver.**

126. LB-031 does not disclose, teach, or suggest this claim element.

127. Dr. Jacobsen makes the same arguments for this claim element as for the previous claim element, all of which have been addressed in § VI.A.2.c, *supra* and are incorporated by reference with respect to this claim element.

128. As with the previous elements, LB-031 lacks disclosure of shared memory as construed by the Court. Again, LB-031 is consistent with the practice at that time of using a dedicated interleaver memory and a separate deinterleaver memory. Thus, LB-031 does not describe interleaving and deinterleaving within a shared memory as

required by this claim element. *See* §§ VI.A.1, VI.A.2.a; *see also* § VI.A.5.a, *infra* and §§ IV.A and IV.B, *supra*.

129. Dr. Jacobsen again ignores the requirement that the memory be shared within a single transceiver as required by this claim as further supported by the Court's construction of the term. Notably, Dr. Jacobsen does not cite to a specific portion of LB-031 reference to support its conclusion that a single transceiver would interleave and deinterleave within a shared memory. *See* Jacobsen Report at ¶ 205. Instead, Dr. Jacobsen repeats the claim element and jumps to an unsupported conclusion that it is met by LB-031.

130. Because LB-031 does not disclose, teach, or suggest interleaving the first plurality of RS coded data bytes within the shared memory allocated to the interleaver and deinterleaving the second plurality of RS coded data bytes within the shared memory allocated to the deinterleaver, it does not render claim 1 of the '048 Patent obvious.

g. LB-031 does not disclose wherein the shared memory allocated to the interleaver is used at the same time as the shared memory allocated to the deinterleaver.

131. LB-031 does not disclose, teach, or suggest this claim element.

132. As discussed in Sections VI.A.1, VI.A.2.a, VI.A.3.c, VI.A.2.e, *supra*, and in Section VI.A.5.a, *infra*, LB-031 does not disclose allocating shared memory in a single transceiver. At least because of the lack of disclosure directed to shared memory and to allocation of such memory, LB-031 does not disclose, teach, or suggest this claim element.

133. Dr. Jacobsen argues that because a transceiver can transmit and receive at the same time, this element is met. *See Jacobsen Report at ¶ 207.* When making this conclusory argument, Dr. Jacobsen overlooks the fact that the allocated memory refers to memory that can be allocated to an interleaver or a deinterleaver of a single transceiver as discussed in Sections VI.A.1, VI.A.2.a, VI.A.3.b, VI.A.2.e, *supra*. *See also* § VI.A.5.a.

134. At least because LB-031 does not disclose the claimed allocation of memory as discussed in, for example, Sections VI.A.3.c, VI.A.2.e, *supra*, LB-031 cannot disclose or suggest this element of claim 1 of the '048 patent.

135. Because LB-031 does not disclose, teach, or suggest wherein the shared memory allocated to the interleaver is used at the same time as the shared memory allocated to the deinterleaver, it does not render claim 1 of the '048 Patent obvious.

3. LB-031 Does Not Render Claim 5 of the '381 Patent Obvious

136. It is my opinion and conclusion that LB-031 alone or in combination with other cited references fails to disclose or suggest each element of claim 5 of the '381 patent, and hence fails to render the Asserted Claims anticipated or obvious as described in detail, below.

- a. **LB-031 does not disclose a non-transitory computer-readable information storage media having stored thereon instructions, that if executed by a processor, cause to be performed a method for allocating shared memory in a transceiver.**

137. LB-031 describes a prior art system that is not related to sharing memory in a transceiver. *See generally* § VI.A.1, *supra*.

138. As described in Section VI.A.2.a, LB-031 does not include any disclosure directed to allocating shared memory in a transceiver. Consequently, for the same reasons as described with respect to claim 1 of the '048 patent, LB-031 fails to disclose this element of claim 5 of the '381 patent.

139. Additionally, Dr. Jacobsen does not identify any portions of LB-031 that disclose a non-transitory computer-readable information storage media having stored thereon instruction that are executed by a processor. *See* Jacobsen Report at ¶ 210. Instead, Dr. Jacobsen without any support simply draws an inference that “[o]ne of ordinary skill in the art would have understood that a source code and instructions for such transceivers could be stored on computer-readable information storage media, and could be executed by a processor.” *See id.*

140. First of all, Dr. Jacobsen’s conclusion is wrong on its face. Source code (or object code) cannot be executed by a processor. A POSITA would understand that source code (or object code) is a term of art referring to uncompiled and non-executable human readable code.

141. Even ignoring the fact that Dr. Jacobsen’s conclusion is wrong on its face, Dr. Jacobsen did not show that any element of claim 5 of the '381 patent is performed by executing instructions stored on a non-transitory computer-readable information media. A POSITA would understand that it is possible that one or more of the claimed functions could be implemented in hardware, and therefore would not necessarily have to be carried out through an execution of instructions stored on a non-transitory computer-readable media. Dr. Jacobsen did not even attempt to show one way or

another with which of these possibilities LB-031 would be concerned with respect to each claimed function.

142. It is my opinion that LB-031 does not disclose, teach, or suggest this claim element of claim 5 of the '381 patent and therefore fails to render claim 5 of the '381 Patent obvious.

- b. LB-031 does not disclose determining, at the transceiver, an amount of memory required by the deinterleaver to deinterleave a first plurality of Reed Solomon (RS) coded data bytes within a shared memory.**

143. LB-031 does not disclose, teach, or suggest this claim element.

144. Dr. Jacobsen incorporates her arguments from Section IX.A.3.d of the Jacobsen Report, which have been addressed *supra* in Section VI.A.2.b with respect to claim 1 of the '048 patent.

145. Because LB-031 does not disclose, teach, or suggest determining, at the transceiver, an amount of memory required by the deinterleaver to deinterleave a first plurality of Reed Solomon (RS) coded data bytes within a shared memory, it does not render claim 5 of the '381 Patent obvious.

- c. LB-031 does not disclose allocating a first number of bytes of the shared memory to the interleaver to interleave a first plurality of Reed Solomon (RS) coded data bytes for transmission at a first data rate.**

146. LB-031 does not disclose allocating, at the transceiver, a first number of bytes of shared memory to the deinterleaver to deinterleave a first plurality of Reed Solomon (RS) coded data bytes for transmission at a first data rate.

147. LB-031 does not disclose, teach, or suggest this claim element.

148. Dr. Jacobsen incorporates her arguments from Section IX.A.3.e of the Jacobsen Report, which have been addressed *supra* in Section VI.A.2.c with respect to claim 1 of the '048 patent and with respect to an interleaver.

149. Additionally, Dr. Jacobsen incorporates her arguments from Section IX.A.3.g of the Jacobsen Report, which have been addressed *supra* in Section VI.A.2.e with respect to claim 1 of the '048 patent and with respect to a deinterleaver.

150. Because LB-031 does not disclose, teach, or suggest allocating, at the transceiver, a first number of bytes of shared memory to the deinterleaver to deinterleave a first plurality of Reed Solomon (RS) coded data bytes for transmission at a first data rate, it does not render claim 5 of the '381 Patent obvious.

d. LB-031 does not disclose wherein the allocated memory for the deinterleaver does not exceed the maximum number of bytes in the message.

151. LB-031 does not disclose this limitation at least because, as I explain in Section VI.A.2.a, *supra*, it does not disclose allocating memory to an interleaver (or a deinterleaver.)

152. Dr. Jacobsen incorporates her arguments from Section IX.A.3.f of the Jacobsen Report, which have been addressed *supra* in Section VI.A.2.d with respect to claim 1 of the '048 patent. Although, claim 1 of the '048 is directed to “allocated memory for the interleaver,” my arguments hold true for “allocated memory for the deinterleaver,” as recited in claim 5 of the '381 patent, at least because LB-031d does not disclose a system for allocating memory to an interleaver or to a deinterleaver. *See, e.g.*, § VI.A.2.a.

153. Because LB-031 does not disclose, teach, or suggest transmitting or receiving, by the transceiver, a message during initialization specifying a maximum number of bytes of memory that are available to be allocated to a deinterleaver, it does not render claim 5 of the '381 patent obvious.

- e. **LB-031 does not disclose allocating, at the transceiver, a second number of bytes of shared memory to an interleaver to interleave a second plurality of Reed Solomon (RS) coded data bytes for transmission at a second data rate.**

154. LB-031 does not disclose, teach, or suggest this claim element.

155. Dr. Jacobsen incorporates her arguments from Section IX.A.3.e of the Jacobsen Report, which have been addressed *supra* in Section VI.A.2.c with respect to claim 1 of the '048 patent and with respect to an interleaver.

156. Additionally, Dr. Jacobsen incorporates her arguments from Section IX.A.3.g of the Jacobsen Report, which have been addressed *supra* in Section VI.A.2.e with respect to claim 1 of the '048 patent and with respect to a deinterleaver.

157. Because LB-031 does not disclose, teach, or suggest allocating, at the transceiver, a second number of bytes of shared memory to an interleaver to interleave a second plurality of Reed Solomon (RS) coded data bytes for transmission at a second data rate, it does not render claim 5 of the '381 Patent obvious.

- f. **LB-031 does not disclose deinterleaving the first plurality of RS coded data bytes within the shared memory allocated to the deinterleaver and interleaving the second plurality of RS coded data bytes within the shared memory allocated to the interleaver.**

158. LB-031 does not disclose, teach, or suggest this claim element.

159. Dr. Jacobsen incorporates her arguments from Section IX.A.3.h of the Jacobsen Report, which have been addressed *supra* in Section VI.A.2.f with respect to claim 1 of the '048 patent. The difference in wording of this claim element as compared with the corresponding claim element of claim 1 of the '048 is of no consequence to my arguments.

160. Because LB-031 does not disclose, teach, or suggest deinterleaving the first plurality of RS coded data bytes within the shared memory allocated to the deinterleaver and interleaving the second plurality of RS coded data bytes within the shared memory allocated to the interleaver., it does not render claim 5 of the '381 Patent obvious.

g. LB-031 does not disclose wherein the shared memory allocated to the deinterleaver is used at the same time as the shared memory allocated to the interleaver.

161. LB-031 does not disclose, teach, or suggest this claim element.

162. Dr. Jacobsen incorporates her arguments from Section IX.A.3.i of the Jacobsen Report, which have been addressed *supra* in Section VI.A.3.g with respect to claim 1 of the '048 patent. The difference in wording of this claim element as compared with the corresponding claim element of claim 1 of the '048 is of no consequence to my arguments.

163. Because LB-031 does not disclose, teach, or suggest deinterleaving the first plurality of RS coded data bytes within the shared memory allocated to the deinterleaver and interleaving the second plurality of RS coded data bytes within the

shared memory allocated to the interleaver., it does not render claim 5 of the '381 Patent obvious.

4. LB-031 Does Not Render Claim 13 of the '882 Patent Obvious

164. It is my opinion and conclusion that LB-031 alone or in combination with other cited references fails to disclose or suggest each element of claim 13 of the '882 patent, and hence fails to render the Asserted Claims anticipated or obvious as described in detail, below.

a. LB-031 does not disclose a system that allocates shared memory.

165. LB-031 does not disclose, teach, or suggest this claim element of claim 13 of the '882 Patent for the same reason as discussed with respect to the same claim element of claim 1 of the '048 Patent. *See* § VI.A.2.a.

b. LB-031 does not disclose other elements of this claim.

166. Dr. Jacobsen adopts wholesale her arguments with respect to claim 5 of the of the '381 patent (elements 5[b] – 5[h]) as her argument with respect to claim 13 of the '882 patent (elements 13[c] through 13[i], respectively). *See* Jacobsen Report at ¶ 232.

167. Accordingly, I hereby incorporate my arguments with respect to claim elements of claim 5 of the '381 patent, and also claim 1 of the '048 Patent as rebuttal argument for the respective claim elements of claim 13 of the '882 patent.

168. Specifically, using the claim element numbering from Dr. Jacobsen Report (*see* Appendix C to Jacobsen Report), I hereby incorporate herein the following sections of this report:

- with respect to element 13[d], I incorporate §§ VI.A.2.b, VI.A.3.b, *supra*;

- with respect to element 13[e], I incorporate §§ VI.A.2.c, VI.A.2.e, VI.A.3.c, *supra*;
- with respect to element 13[f], I incorporate §§ VI.A.2.d, VI.A.3.d, *supra*;
- with respect to element 13[g], I incorporate §§ VI.A.2.c, VI.A.2.e, VI.A.3.e, *supra*;
- with respect to element 13[h], I incorporate §§ VI.A.2.f, VI.A.3.f, *supra*;
- with respect to element 13[i], I incorporate §§ VI.A.2.g, VI.A.3.g, *supra*.

169. LB-031 does not disclose, teach, or suggest the above claim elements of claim 13 of the '882 Patent for the same reason as discussed with respect to the substantially similar claim elements of claim 5 of the '381 Patent, and claim 1 of the '048 Patent.

5. LB-031 Does Not Render Claim 19 of the '473 Patent Obvious

170. It is my opinion and conclusion that LB-031 alone or in combination with other cited references fails to disclose or suggest each element of claim 19 of the '473 patent, and hence fails to render the Asserted Claims anticipated or obvious as described in detail, below.

- a. **LB-031 does not disclose a multicarrier transceiver being associated with a memory wherein the memory is allocated between the interleaving function and the deinterleaving function in accordance with a message received during initialization of the transceiver.**
 - i. **LB-031 does not disclose a multicarrier transceiver being associated with a memory wherein the memory is allocated between the interleaving function and the deinterleaving function.**

171. LB-031 does not disclose, teach, or suggest a multicarrier transceiver being associated with a memory wherein the memory is allocated between the interleaving function and the deinterleaving function in accordance with a message received during initialization of the transceiver. As discussed in the Overview of LB-031 Section, *supra*, and also in connection with claim 1 of the '048 patent, *supra*, LB-031 does not disclose allocating a memory between an interleaver function and a deinterleaver function in a single transceiver but instead discloses exchanging "capability" information specifying the size of a dedicated interleaver memory and the size of a separate, dedicated deinterleaver memory. *See* § VI.A.1; *see also* § VI.A.2.a.

172. No portion of any memory contemplated by LB-031 is used as interleaver memory at one point in time and deinterleaver memory at another point in time and, thus, LB-031 does not allocate memory *between* an interleaving function and a deinterleaving function. Rather, one of ordinary skill in the art would understand LB-031 in the context of a system in which the CO transceiver (VTU-O) has a dedicated amount of memory available to be used for downstream interleaving and a separate, dedicated amount of memory available to be used for upstream deinterleaving and the CPE transceiver (VTU-R) has a dedicated amount of memory available to be used for

downstream deinterleaving and a separate, dedicated amount of memory available to be used for upstream interleaving. In the VTU-O, no portion of the dedicated downstream interleaver memory can be allocated for upstream deinterleaving and, no portion of the upstream deinterleaver memory can be allocated for downstream interleaving. Likewise, in the VTU-R, no portion of the dedicated upstream interleaver memory can be allocated for downstream deinterleaving and, no portion of the downstream deinterleaver memory can be allocated for upstream interleaving.

173. Dr. Jacobsen describes the disclosure in LB-031 of transceivers exchanging capabilities, including specifying the amount of memory a transceiver has available for a particular latency path by exchanging the end-to-end interleaver delay on octets that it can support for that latency path. *See* Jacobsen Report at ¶¶ 242-244. She refers to the disclosure in LB-031 that “[i]f a VDSL2 implementation supports a larger interleaver memory than is required, it should be free to specify the larger value,” in which case “[t]he VTU-O and VTU-R would then select the smaller of the transmitter and receiver capabilities.” *See* Jacobsen Report at ¶ 243 (citing LB-031 at 3). But this is merely standard behavior for DSL transceivers at that time. Dr. Jacobsen does not point to any disclosure in LB-031 where memory is allocated between an interleaving function and a deinterleaving function in accordance with a message. Further explanation of the distinctions between LB-031 and claim 19 of the ‘473 patent is provided below.

- ii. **LB-031 does not disclose the memory is allocated between the interleaving function and the deinterleaving function in accordance with a message received during initialization of the transceiver.**

174. Even assuming that the exchange of information described in LB-031 occurs during initialization and occurs through an exchange of messages, LB-031 would not disclose to a person of ordinary skill in the art a message that is used to perform the claimed allocation. In particular, LB-031 discloses that “[i]f a VDSL2 implementation supports a larger interleaver memory than is required, it should be free to specify the larger value,” and that in such a case “[t]he VTU-O and VTU-R would then select the smaller of the transmitter and receiver capabilities, in each direction, as the end-to-end capabilities.” LB-031 at 3. This disclosure would be understood by a POSITA as follows:

For determining capabilities applicable to the downstream (DS) direction (i.e., downstream latency path from VTU-O to VTU-R):

Step 1. The VTU-O sends a message to the VTU-R that includes the amount (in octets) of downstream interleaver delay that the VTU-O can support (“Message 1-DS”).

Step 2. The VTU-R sends a message to the VTU-O that includes the amount (in octets) of downstream deinterleaver delay that the VTU-R can support (“Message 2-DS”).

Step 3. For the downstream deinterleaver delay capabilities, the VTU-R would select the smaller of the downstream interleaver delay amount indicated in Message 1-DS and the downstream deinterleaver delay amount indicated in Message 2-DS.

Step 4. Separately, for the downstream interleaver delay capabilities, the VTU-O would select the smaller of the downstream interleaver delay amount indicated in Message 1-DS and the downstream deinterleaver delay amount indicated in Message 2-DS.

(Step 4 may not be necessary because it will ultimately be up to the VTU-R to determine the amount of delay actually implemented for the downstream path.)

For determining capabilities applicable to the upstream (US) direction (i.e., upstream latency path from VTU-R to VTU-O):

Step 1. The VTU-O sends a message to the VTU-R that includes the amount (in octets) of upstream deinterleaver delay that the VTU-O can support ("Message 1-US").

Step 2. The VTU-R sends a message to the VTU-O that includes the amount (in octets) of upstream interleaver delay that the VTU-R can support ("Message 2-US").

Step 3. For the upstream deinterleaver delay capabilities, the VTU-O would select the smaller of the upstream deinterleaver delay amount indicated in Message 1-US and the upstream interleaver delay amount indicated in Message 2-US.

Step 4. Separately, for the upstream interleaver delay capabilities, the VTU-R would select the smaller of the upstream deinterleaver delay amount indicated in Message 1-US and the upstream interleaver delay amount indicated in Message 2-US.

(Step 4 may not be necessary because it will ultimately be up to the VTU-O to determine the amount of delay actually implemented for the upstream path.)

175. In the examples above, a single message from the VTU-O to the VTU-R could include the Message 1-DS and Message 1-US capabilities information and a single message from the VTU-R to the VTU-O could include the Message 2-DS and Message 2-US capabilities information. But, again, even if a POSITA would understand there to be a message exchange such as the example described above, no portion of memory is allocated between the interleaving function and the deinterleaving function in accordance with a message.

176. Instead, LB-031 at most discloses that, for the downstream direction, a VTU-R with a larger dedicated deinterleaver memory than is required can determine

whether the VTU-O also supports a larger amount. But, if the VTU-O does not support a larger amount than is required, however, the extra deinterleaver memory of the VTU-R is simply not used. For example, it is not available to be used for the upstream interleaver function. The examples described below illustrate this concept.

177. Example 1. VTU-O (30,000 octets of dedicated downstream interleaver memory; 30,000 octets of dedicated upstream deinterleaver memory). VTU-R (40,000 octets of dedicated downstream deinterleaver memory; 20,000 octets of dedicated upstream interleaver memory).

Legend:



dedicated downstream memory (interleaver memory for VTU-O,
deinterleaver memory for VTU-R)



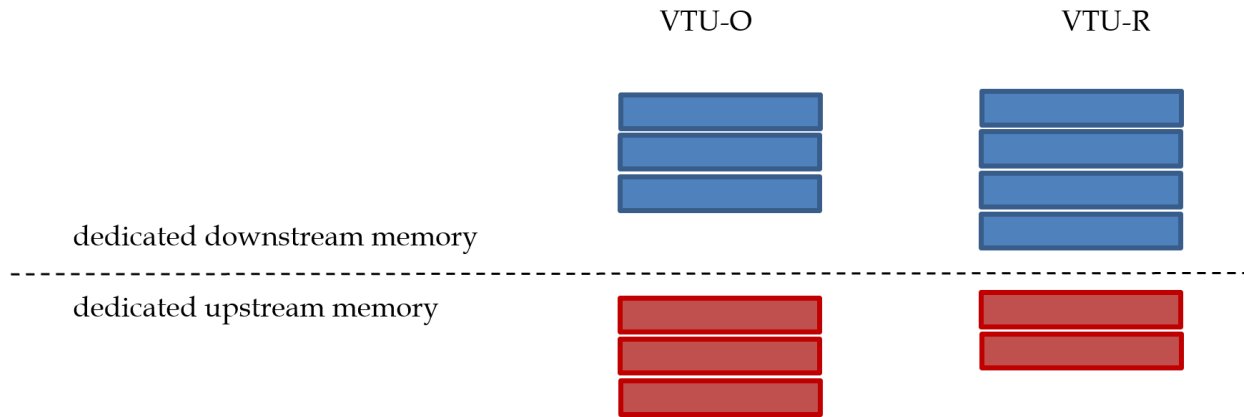
dedicated upstream memory (interleaver memory for VTU-R,
deinterleaver memory for VTU-O)



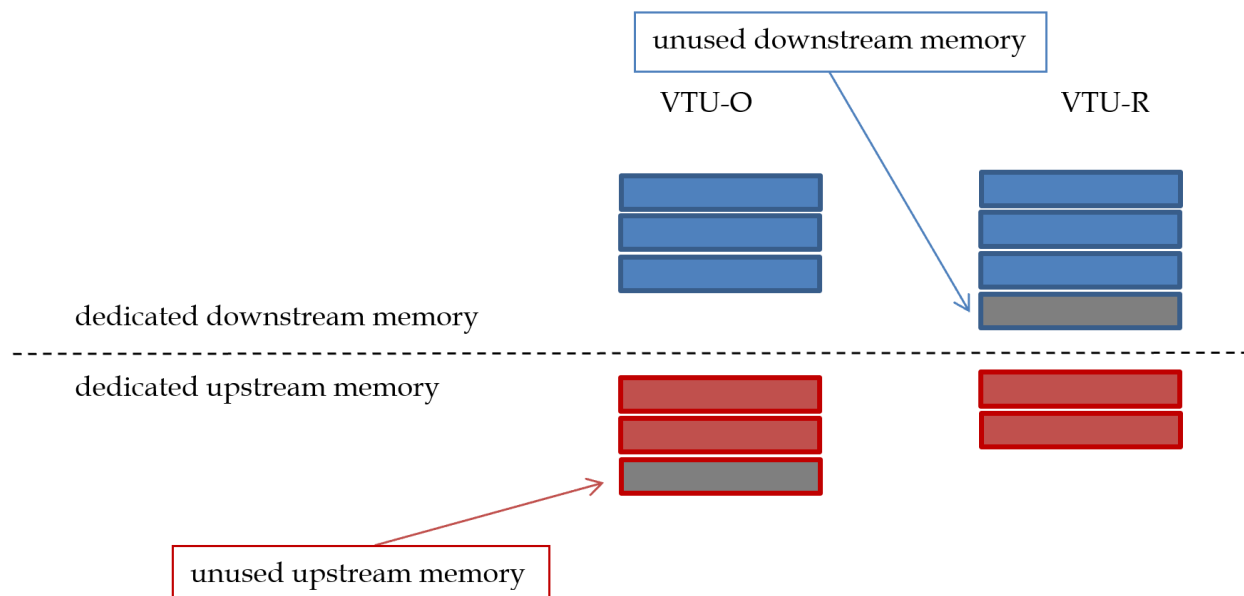
unused memory

Each rectangle represents 10,000 octets of memory.

178. Capabilities (maximum memory supported):



179. According to LB-031, each transmitter would exchange their memory capabilities in each direction and “then select the smaller of the transmitter and receiver capabilities, *in each direction*.” Consistent with the state of art of its time, LB-031 teaches that the smaller capability is selected. Because the smaller capability is selected, this results in a maximum possible memory allocation as shown below.



180. Because the smaller of the capabilities of the transmitter or receiver are selected in each direction in accordance with the express teaching of LB-031, unused

memory for one function in a transceiver cannot be used for another function, e.g., unused dedicated deinterleaver memory in the VTU-R cannot be used for the interleaving function. In the example above, 10,000 octets of deinterleaver memory within the VTU-R and 10,000 octets of deinterleaver memory in the VTU-O would never be used.

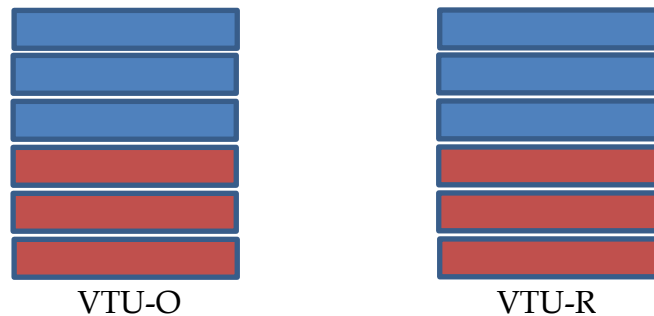
181. Under the LB-031 implementation even though the VTU-R learned about the VTU-O's capabilities downstream, it could not use 10,000 octets of its 40,000 octets of memory that was dedicated to the downstream deinterleaver. Likewise, even though the VTU-O learned about the VTU-R's capabilities upstream, it could not use 10,000 octets of its 30,000 octets of memory that was dedicated to the upstream deinterleaver.

182. In this example, if a service provider is providing a VDSL2 service that requires 30,000 octets of memory in each transceiver for the downstream service and 20,000 octets of memory in each transceiver for the upstream service, the transceivers would be able to provide that service. If, however, a service provider is providing a VDSL2 service that requires 30,000 octets of memory in each transceiver for the downstream service and 30,000 octets of memory in each transceiver for the upstream service, the transceivers would NOT be able to meet the requirements of the service.

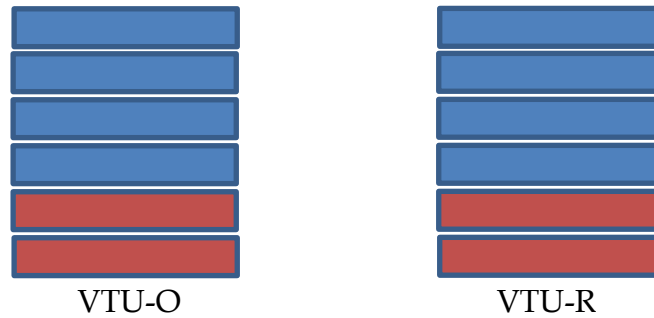
183. The above example can be contrasted with an example implementing the claimed allocation of memory between an interleaving function and a deinterleaving function according to the inventions of the Family 3 patents (Example 2, *infra*).

184. Example 2. Each transceiver supports a total of 60,000 octets of shared interleaver/deinterleaver memory. If the service provider desires to provide a VDSL2

service that requires 30,000 octets of memory in each transceiver for the downstream service and 30,000 octets of memory in each transceiver for the upstream service, the 60,000 octets of memory in each transceiver could be allocated between the interleaver and deinterleaver functions such that 30,000 octets in each transceiver are used for the downstream path and 30,000 octets are used for the upstream path as illustrated below.



185. On the other hand, if the service provider desires to provide a VDSL2 service that requires 40,000 octets of memory in each transceiver for the downstream service and 20,000 octets of memory in each transceiver for the upstream service, the 60,000 octets of memory in each transceiver could be allocated between the interleaver and deinterleaver functions such that 40,000 octets in each transceiver are used for the downstream path and 20,000 octets are used for the upstream path as illustrated below.



186. Therefore, unlike LB-031 where 10,000 octets of memory are unused and the service provider could not provide the service to the customer, when shared memory, which can be allocated between the interleaver function or deinterleaver function, is used, memory that would otherwise go unused can be allocated to one function or the other depending on messages that are, in part, dependent on the service requirements. As illustrated by these examples, the VTU-R is capable of allocating 10,000 octets of its memory to the upstream interleaving function at one time but allocating the same 10,000 octets of its memory to the downstream deinterleaving function at another time. This provides flexibility that enables the transceivers to meet different service requirements.

187. The claimed allocation of memory requires allocating the memory between an interleaving function and a deinterlacing function according to a message. LB-031 does not teach this claim element. Instead, as illustrated above, it allows a transceiver to determine how much of its pre-allocated downstream memory (i.e., interleaver memory in the VTU-O and deinterleaver memory in the VTU-R) and how

much of its pre-allocated upstream memory (i.e., deinterleaver memory in the VTU-O and interleaver memory in the VTU-R) can be used.

188. It is therefore my opinion that LB-031 does not disclose, teach, or suggest this claim element of claim 19 of the '473 Patent.

- b. LB-031 does not disclose a multicarrier transceiver being associated with a memory wherein at least a portion of the memory may be allocated to the interleaving function or the deinterleaving function at any one particular time depending on the message.**

189. LB-031 does not disclose, teach, or suggest these claim elements. As discussed in the Overview of LB-031 Section, and in the section immediately above, as well as in connection with claim 1 of the '048 patent, *supra*, LB-031 does not disclose any sharing of memory within a transceiver. *See* § VI.A.1; *see also* §§ VI.A.2.a, VI.A.5.a. Therefore, in a transceiver operating in accordance with LB-031, no portion of memory may be allocated to an interleaving function at one time or a deinterleaver function at another time depending on a message.

190. As discussed in paragraphs 177-182 above with respect to the Example 1, according to the teachings of LB-031, the dedicated interleaver memory may not at any particular time be allocated to the deinterleaver function and the dedicated deinterleaver memory cannot at any particular time be used for the interleaver function. The exchange of capabilities in LB-031, even assuming it is accomplished through messages exchanged during initialization, would not allow any portion of memory to be allocated to an interleaver function at one time or a deinterleaver function at another time depending on a message. Rather, any messages contemplated by LB-031 are used

only to select the smaller of the transmitter or receiver capabilities. This may result in portions of memory that are unused, as explained in paragraphs 179-182. It will not result in a portion of memory being used for one function or the other at a particular time depending on a message, as claimed.

191. Confusingly, Dr. Jacobsen argues that because a transceiver can transmit and receive at the same time, this element is met. *See* Jacobsen Report at ¶ 246. She does not explain how transmitting and receiving at the same time has anything to do with this claim element. In fact, the conclusion she draws from this is that LB-031 discloses that the shared memory allocated to the interleaver is used at the same time as the shared memory allocated to the deinterleaver. *Id.* The conclusion has no bearing on whether, and does not prove that, LB-031 discloses “at least a portion of the memory may be allocated to the interleaving function or the deinterleaving function at any one particular time depending on the message.”

192. For the foregoing reasons, it is my opinion that LB-031 fails to disclose all elements of claim 19 of the ‘473 patent and therefore fails to render claim 19 of the ‘473 patent obvious.

B. The Asserted Claims Are Not Obvious Over the Combination of LB-031 and Mazzoni

193. It is my opinion and conclusion that Mazzoni alone or in combination with LB-031 fails to disclose or suggest each element of the Asserted Claims, and hence fails to render the Asserted Claims obvious as described in detail, below.

194. It is also my opinion that regardless of the disclosure of LB-031 and Mazzoni individually, a person of ordinary skill in the art would not be motivated to combine the teachings of LB-031 with the teachings of Mazzoni at least for the reasons described in Section VI.B.2, *infra*.

195. An overview of LB-031s has been provided in Section VI.A.1, *supra*.

1. Overview of Mazzoni

196. The disclosure of Mazzoni is based on the premise that there is a finite group of data rate pairs, where each data rate pair comprise a predetermined upstream data rate and a predetermined downstream data rate). *See* Mazzoni at 1:65 – 2:2 (“The invention therefore provides a device for sending/receiving digital data that is capable of processing different bit rates from a group of predetermined bit rates (e.g., all the symmetrical or asymmetrical services offered by the VDSL communication system).”), 3:62 – 4:14 (describing six symmetrical and six asymmetrical data rate pairs). Mazzoni also refers to these data rate pairs as services, where a service utilizes one predetermined data rate in the upstream direction and another predetermined data rate in the downstream direction. *See id.* In a symmetric service, the upstream data rate is the same as the downstream data rate. *Id.* at 3:62 – 4:2. In an asymmetric service the two are different. *Id.* at 4:3-14. Mazzoni describes higher and lower bit rate examples of six possible symmetrical services:

The VDSL communication system enables the operator to provide symmetrical services, typically six symmetrical services S1-S6. That is, the information bit rates in the two transmission directions (i.e., from the operator to the user and from the user to the operator) are exactly the same. The service S1 with the lowest bit rate has a bit rate of 32x64 kbit/s,

for example, and the fastest symmetrical service S6 has a bit rate of 362x64 kbit/s.

Id. at 3:62 – 4:2. Mazzoni also describes example asymmetrical services with higher bit rates for the downstream direction:

With the VDSL system, the operator can also provide asymmetrical services A1-A6. These are services with different information bit rates in the user to operator direction (uplink direction) and in the operator to user direction (downlink direction). The first asymmetrical service A1 has a bit rate in the uplink direction of 32x64 kbit/s, for example, and a bit rate in the downlink direction of 100x64 kbit/s. The asymmetrical service having the highest global information bit rate (uplink bit rate+downlink bit rate) is the service A6. The bit rate of the service A6 in the uplink direction is equal to 32x64 kbit/s and in the downlink direction is equal to 832x64 kbit/s.

Id. at 4:3-14.

197. Mazzoni describes the assignment of interleaver memory and deinterleaver memory for each of the predefined data rate pairs (services). To accomplish this, Mazzoni proposes using predefined I and M parameter values for its interleaving means, and predefined I' and M' parameter values for deinterleaving means for each data rate pair (i.e., service).

198. This fixed correspondence of a data rate pair to predefined I and M parameter values (for interleaving) and predefined I' and M' parameter values (for deinterleaving) is explained by Mazzoni as follows:

These parameters define the sizes of the respective memory spaces assigned to the interleaving means and to the deinterleaving means. This is done according to the bit rate of the information sent by the terminal TO (parameters I and M) and the bit rate of the information received by the terminal TO (parameters I' and M').

Id. at 5:24-30.

199. “TO” in the above quoted language refers to a device at the “operator end.” *Id.* at 4:3:59-60. “TU” refers to a device at the “user end.” *Id.* Because the TO interleaves information to be transmitted downstream and deinterleaves information it receives in the upstream direction, the I and M interleaving parameters are associated with information sent by the TO, and similarly the I’ and M’ parameters are associated with information received by the TO. *See, e.g.,* Mazzoni at 5:27-30; Jacobsen Report at ¶¶ 96-100 (describing how the terms “interleaving” and “deinterleaving” are used in connection with the terms “upstream” and “downstream” communications in ADSL and VDSL).

200. Mazzoni explains that the predefined values of I and M specify the amount of predefined memory for the downstream interleaver of TO (and hence the downstream deinterleaver of TU) , and I’ and M’ specify the amount of predefined memory for an upstream deinterleaver of TO (and hence the downstream interleaver of TU), for a particular data rate pair (i.e., service). *See* Mazzoni at 6:38-43 (“More particularly, the size of the first memory space needed to implement triangular convolutional interleaving with I branches of $i-1$ blocks of M bytes is equal to $I \times (I-1) \times M / 2$. Similarly, the size of the second memory space ESM2 required to support the uplink bit rate is equal to $I' \times (I'-1) \times M' / 2$.”); *see also id.* at 6:53-59 (“A table of values for the parameters I, M, I’ and M’ can therefore be stored in the coding/decoding stage. When the modem is installed at the end of the line, and depending on the service actually provided by the operator, the control means MCD may retrieve the corresponding values of I, M, I’ and M’ from the stored table.”); *id.* at 5:24-30. These

values are stored in a table within the modem and retrieved at the time of modem installation. *See* Mazzoni at 5:22-23, 6:51-55. Specifically, Mazzoni explains:

The above calculation of I, M, I' and M' for the asymmetrical service A6 can be applied in an analogous manner to the other services of the VDSL system. **A table of values for the parameters I, M, I' and M' can therefore be stored in the coding/decoding stage.** When the modem is installed at the end of the line, and depending on the service actually provided by the operator, **the control means MCD may retrieve the corresponding values of I, M, I' and M' from the stored table.** These values are delivered to the addressing means MAD1 and MAD2, the structure of which is described in more detail with reference to FIGS. 7 and 8.

Mazzoni at 6:51-61 (emphasis added).

201. As shown above in the quoted disclosure, the I, M, I', and M' parameter values are all predetermined for each data rate pair from a group of predefined data rate pairs and are stored in table. Mazzoni explains that at the time of the installation of the modem, the modem's memory is configured according to the I, M, I', and M' values retrieved from a table. Which values are retrieved depends on "the service actually provided by the operator," i.e., on the upstream and the downstream data rate pair configuration that is being provided by the service provided for the modem.

202. Dr. Jacobsen's description of Mazzoni is incomplete, and thus does not accurately characterize Mazzoni's teachings, because it overlooks Mazzoni's fundamental premise that a predefined data rate pair service and corresponding predefined I, M, I' and M' values will be fixed at the time of installation of a modem. For example, Dr. Jacobsen, citing Mazzoni at 6:19-50, states that the I, M, I', and M' parameters "can be determined from maximum and minimum memory size capacities that are easily calculable using downlink and uplink bit rates the number of bits

affected by noise, and RS error correction.” See Jacobsen Report at ¶ 256. Dr. Jacobsen does not explain further what this “determination” is, or when it occurs. See *id.* Yet, the portion of Mazzoni that she cites simply describes examples of how one can choose the predetermined values of the I, M, I’, and M’ parameters that are then stored in a table for retrieval at the time of installation of the modem. See Mazzoni at 6:19-50.

203. Also, because the data rate pair options are predetermined (and hence known in advance), and because there is a predetermined set of values for the I, M, I’ and M’ parameters for each predetermined data rate pair, there is no need for a device in Mazzoni to obtain any additional information from a device at the other end of the communication line in order to implement the memory assignment described by Mazzoni. Such an assignment is carried out in a sole reliance on the predetermined set of I, M, I’, and M’ parameters stored in a table and retrieved by the control means at the time of installation of the device. See Mazzoni at 6:53-59.

2. A Person of Ordinary Skill in the Art Would Not Combine the Teachings of LB-031 with the Teachings of Mazzoni

204. A person of ordinary skill in the art at the time of the invention of the Family 3 Patents would not look to the teachings of Mazzoni when implementing the teachings of LB-031, or *vice versa*. In fact, as explained below, the two references are so different that a person of ordinary skill in the art would be discouraged from looking to the teaching of the other reference.

205. An overview of LB-031 has been provided in Section VI.A.1, *supra*. The overview of Mazzoni has been provided in Section VI.B.1, *supra*.

206. Dr. Jacobsen asserts that “both Mazzoni and LB-031 disclose VDSL transceivers.” See Jacobsen Report at ¶ 346. This in and of itself, or in combination with any other argument made by Dr. Jacobsen in Section VIII.B.7 of the Jacobsen Report, is not sufficient to show that a person of ordinary skill in the art would have combined the teachings of the two references. At the time of the invention of the Family 3 Patents, the VDSL standard was still under development and there were likely hundreds, if not thousands, of references directed to possible implementation details of many and varied proposals for VDSL transceivers. One of skill in the art at the time would have understood that many of these references would be completely incompatible with one another and/or, if combined, would provide no useful benefit. Thus, that Mazzoni and LB-031 are purportedly both directed to different proposals for yet-to-be-defined VDSL transceivers, would not have made their combination obvious.

207. Dr. Jacobsen then states that “both Mazzoni and LB-031 are concerned with limiting the size of memory used for interleaving and deinterleaving.” See Jacobsen Report at ¶ 347. This in and of itself, or in combination with any other argument made by Dr. Jacobsen in Section VIII.B.7 of the Jacobsen Report, is again not sufficient to motivate a person of ordinary skill in the art to combine the teaching of the two references.

208. Also, this generalization is inaccurate. As explained in VI.A.1, *supra*, LB-031 is concerned with providing a solution that meets certain delay requirements specified in units of time, while allowing use of larger dedicated interleaver or deinterleaver memories if both transceivers support more than the minimum required

by a standard. There is no technique described in LB-031 for “limiting the size of memory used for interleaving and deinterleaving,” contrary to Dr. Jacobsen assertions. See § VI.A.1. Rather, as I explained above, LB-031 actually wastes memory by leaving portions of memory unused where one transceiver supports more memory for a given latency path than is supported by the other transceiver with which it is communicating. See § VI.A.1 and ¶¶ 176-187, *supra*. Because LB-031 wastes memory, a POSITA would be motivated **not** to use the teachings of LB-031 if they were concerned with reducing memory requirements.

209. Dr. Jacobsen states that: “[a] skilled artisan wishing to implement the VDSL transceiver of Mazzoni would have been motivated to include the initialization message of LB-031 so that the VTU-O and VTU-R of Mazzoni could choose values for the parameters I , M , I' and M' that would not exceed the size of the shared memory at the selected downstream and upstream bit rates.” See Jacobsen Report at ¶ 350. This is incorrect.

210. A POSITA would not look to add a message (from LB-031 or otherwise) to the system disclosed in Mazzoni, and in fact doing so would provide no useful benefit. This is because the system disclosed in Mazzoni relies on the use of a pre-populated table of I , M , I' , and M' parameter values, where each set of values corresponds to a respective one of a number of predetermined data rate service pairs. See Mazzoni at 5:22-23, 5:27-30, 6:51-55. There is no use for a message that specifies the maximum supported interleaver or deinterleaver memory size (assuming such a message is even disclosed per LB-031) because all data rate pairs and their corresponding I , M , I' , and M'

values that need to be supported are accounted for. Mazzoni contemplates TO and TU transceiver pairs that will both be preconfigured at the time of installation with the same predetermined parameters selected from a limited number of possibilities. Thus, exchanging messages describing the capabilities of the transceivers would be redundant and serve no useful purpose.

211. An additional reason why LB-031's exchange of maximum supported memory sizes would not be recognized as beneficial to Mazzoni is that it is incompatible. Take an example where we assume that, per LB-031, the VTU-R (i.e., TU of Mazzoni) transmits to the VTU-O (i.e., TO of Mazzoni) a message that specifies the maximum downstream deinterleaver memory size that it supports and the maximum upstream interleaver memory size that it supports. Using the predefined services described in Mazzoni, i.e., S1-S6 and A1-A6 (*see* Mazzoni at 3:62 – 4:14), the maximum downstream deinterleaver memory that Mazzoni is capable of supporting is determined by reference to the A6 service and the maximum upstream interleaver memory that Mazzoni is capable of supporting is determined by reference to the S6 service. The A6 service provides a downstream bit rate of 832x64 kbit/s and requires 24,960 bytes of deinterleaver memory. *See id.* at 6:11-30 (describing calculation of required deinterleaver memory size). The S6 service provides an upstream bit rate of 362x64 kbit/s. Per the calculations described at 6:11-30 of Mazzoni, the S6 service requires that the VTU-R be capable of supporting a maximum upstream interleaver memory of 10,860 bytes. If the Mazzoni VTU-O received a message indicating that the VTU-R supported a maximum downstream deinterleaver memory of 24,960 bytes and a

maximum upstream interleaver memory of 10,860 bytes, this information would be useless to the VTU-O. First, it already has the information necessary to support the service for which both transceivers have been preconfigured at the time of installation. Second, neither the VTU-O or VTU-R would actually be capable of simultaneously supporting both maximum interleaver and deinterleaver sizes at the same time because the total memory size of the Mazzoni transceivers is only 26,890 bytes (as determined by the combined upstream and downstream bit rates of the A6 service). *See id.* at 4:18-22 and 6:45-50.

212. While Dr. Jacobsen's asserted motivations to combine LB-031 and Mazzoni fail to account for the fact that Mazzoni's transceivers are preconfigured at the time of installation with all the information they need, in another section (specifically in Section IX.G.5 of the Jacobsen Report) she admits that "Mazzoni further discloses keeping a table of values of the interleaver parameters, indexed by service identifies, in the transceiver." *See Jacobsen Report* at ¶ 626 (citing Mazzoni at 6:51-61).

213. A POSITA at the time of the Family 3 Patent inventions would not combine the teachings of Mazzoni with the teachings of LB-031. If fact, a POSITA would be discouraged from doing so. Because Mazzoni teaches that an assignment of the memory is performed at the time of the installation of the modem based on a table, and not a message, adding a message to this system per LB-031 would be unnecessary, redundant, and create useless complexity during initialization. Further, because Mazzoni is concerned with supporting a finite set of predefined service configurations (i.e., data rate pairs and corresponding interleaver/deinterleaver parameter values).

214. For at least the foregoing reasons, Dr. Jacobsen has not demonstrated that a POSITA would have been motivated to combine LB-031 with Mazzoni in the manner she proposes.

3. The Combination of LB-031 and Mazzoni Does Not Render Claim 1 of the '048 Patent Obvious

215. It is my opinion for the reasons provided in Section VI.B.2 above and as further discussed in this Section VI.B.3 below, that a POSITA would not combine LB-031 and Mazzoni or arrive at the claimed invention even if one were to attempt to combine these references in some way. It is further my opinion and conclusion that LB-031 in combination with Mazzoni fails to disclose each element of claim 1 of the '048 patent, and hence fails to render claim 1 of the '048 patent obvious as described in detail, below.

a. The combination of LB-031 and Mazzoni does not disclose a system that allocates shared memory.

216. As explained in Section VI.A.2.a, *supra*, LB-031 does not disclose a system that allocates shared memory. LB-031 also does not disclose the exchange of information that would be useful for allocating shared memory. As explain above, LB-031 only describes exchanging information about the maximum size of dedicated interleaver memory and, separately, the maximum size of dedicated deinterleaver memory supported by a transceiver. At least for the reasons explained, in paragraph 211 above, this information could not be used by a Mazzoni transceiver to allocate shared memory.

217. As explained above in the Overview of Mazzoni section, Mazzoni relies on a predetermined assignment of a service that has a predetermined pair of upstream and downstream bit rates and a corresponding set of predetermined interleaver and deinterleaver parameter values, I , M , I' and M' . See § VI.B.1. The predetermined assignment takes place when the modem is installed by retrieving the bit rates and parameter values from a stored table. Mazzoni at 6:55-69. Thus, contrary to Dr. Jacobsen's opinion, Mazzoni does not disclose exchanging any messages at all that include information about interleaving or deinterleaving parameters. See also, § VI.B.3.b, *infra*.

218. Mazzoni does not disclose the claimed system for allocating shared memory at least because Mazzoni does not disclose a transceiver that (1) transmits or receives a message during initialization specifying a maximum number of bytes of memory that are available to be allocated to an interleaver (see § VI.B.3.b, *infra*); (2) determining an amount of memory required by the interleaver to interleave a first plurality of Reed Solomon (RS) coded data bytes within the shared memory (see § VI.B.3.c, *infra*); and (3) allocating a first number of bytes of the shared memory to the interleaver to interleave a first plurality of Reed Solomon (RS) coded data bytes for transmission at a first data rate, wherein the allocated memory for the interleaver does not exceed the maximum number of bytes in the message (see § VI.B.3.d, *infra*).

219. Also, because a POSITA would have no rational reason to combine the LB-031 with Mazzoni, as explained in Section VI.B.2, *supra*, the combination of the combination of LB-031 and Mazzoni does not render claim 1 of the '048 patent obvious.

- b. **The combination of LB-031 and Mazzoni does not disclose a transceiver that is capable of transmitting or receiving a message during initialization specifying a maximum number of bytes of memory that are available to be allocated to an interleaver.**

220. Contrary to Dr. Jacobsen's assertion, Mazzoni does not disclose exchanging any messages at all that include information about interleaving or deinterleaving parameters. Dr. Jacobsen asserts that "[o]ne of ordinary skill in the art would have understood that the bit rate information, as well as capabilities of the transceiver at the other end of the system, would have to be conveyed, for example, in the form of a message during initialization, as is described in LB-031. Jacobsen Report at ¶ 269. The "information" she is referring to is the parameters I, M, I' and M'. But, she cannot point to any disclosure of such a message in Mazzoni because there is no such disclosure. Instead, it seems that she is interpreting Mazzoni's description of the configurability of its interleaver means and deinterleaver means according to upstream and downstream bit rates as somehow disclosing reliance on an exchange of I, M, I' and M'. See *id.* (citing Mazzoni at 1:61-65 and 5:24-31). But parameters I, M, I' and M' are not exchanged in any message; rather, as discussed above in Section VI.B.1, these parameters are stored in a table in each transceiver and indexed to a predefined service that includes predefined upstream and downstream bit rates. Mazzoni at 6:53-61. The parameter values for the particular predefined service are retrieved by the control means MCD at the time the modem is installed (*id.*) and delivered by the MCD to the interleaver means MET and deinterleaver means MDET (*id.* at 5:21-23 and Fig. 3). This eliminates any need to exchange these parameters between modems.

221. One of the passages Dr. Jacobsen cites for this assertion, Mazzoni at column 5:24-31, does not describe some alternative embodiment where the I, M, I' and M' parameters are exchanged in messages. Rather, this passage simply describes the use of the predetermined parameters that are indexed to the predetermined service bit rates the transceiver has been configured to use. Dr. Jacobsen accurately admits this elsewhere in her report. *See, e.g.*, Jacobsen Report at ¶ 595 (“Mazzoni discloses keeping a table of values of the interleaver parameters, indexed by service identifiers, in the transceiver. *See id.* at col. 6:51-61. As a person having ordinary skill in the art as of the '473 patent's priority date would have understood, Mazzoni's table is limiting in that all of the services would have to be identified ahead of time and stored in the transceivers.”); *see also id.* at ¶ 626.

222. The other passage Dr. Jacobsen relies on for this assertion, Mazzoni at column 1:61-65, also does not disclose or require the exchange of any interleaver or deinterleaver parameters in a message. To the extent Dr. Jacobsen is interpreting this passage as disclosing anything other than the use of predetermined parameters that correspond to predetermined bit rates, she has misunderstood Mazzoni. In fact, the sentence after the one she quotes shows that the reference to “the bit rate actually processed by the send/receive device (modem)” is referring to one of the predetermined bit rates for a predetermined service. Mazzoni at 1:65 – 2:2 (“The invention therefore provides a device for sending/receiving digital data that is capable of *processing different bit rates from a group of predetermined bit rates* (e.g., all the symmetrical or asymmetrical services offered by the VDSL communication system).”).

223. Because Mazzoni does not describe any message specifying an amount of memory that can be allocated to an interleaver or to a deinterleaver, and because LB-031's exchange of interleaver and deinterleaver capabilities would be useless and incompatible with Mazzoni (*see* § VI.B.2, *supra*), the combination of LB-031 and Mazzoni does not disclose "a transceiver that is capable of transmitting or receiving a message during initialization specifying a maximum number of bytes of memory that are available to be allocated to an interleaver" and, at least for this reason, claim 1 of the '048 patent is not obvious in view of LB-031 and Mazzoni.

- c. **The combination of LB-031 and Mazzoni does not disclose a transceiver that is capable of determining an amount of memory required by the interleaver to interleave a first plurality of Reed Solomon (RS) coded data bytes within the shared memory.**

224. Dr. Jacobsen assert that Mazzoni discloses this limitation. I disagree. While Mazzoni describes the math calculations by which the interleaver and deinterleaver memory sizes can be determined from the upstream and downstream bit rates and the parameters I , M , I' and M' (*see* Mazzoni at 6:11-50), there is no disclosure in Mazzoni that these memory sizes or parameters are determined by Mazzoni's transceiver. Rather, these values are predetermined, stored in a table, and retrieved for use at the time of installation of the transceiver. *Id.* at 6:53-59 ("A table of values for the parameters I , M , I' and M' can therefore be stored in the coding/decoding stage. When the modem is installed . . . , the control means MCD may retrieve the corresponding values of I , M , I' and M' from the stored table."). Because these values are stored prior

to installation, they may be calculated by hand or by separate computer before loading into a stored table on the transceiver.

225. Simplification is a major benefit of Mazzoni's scheme of providing devices that are preconfigured to provide one of 12 service profiles with predetermined data rates and predetermined interleaver and deinterleaver parameters. Requiring Mazzoni's transceiver to calculate interleaver parameters or memory sizes each time it is going to use these values would be contrary to the goal of simplification, particularly where only a limited number of service profiles are needed and where all necessary information is stored prior to installation.

226. Because Mazzoni does not describe a transceiver that determines interleaver parameters or memory sizes, and because requiring Mazzoni to do so it would be contrary to Mazzoni's simplified scheme of storing predetermined values, the combination of LB-031 and Mazzoni does not disclose "a transceiver that is capable of determining an amount of memory required by the interleaver to interleave a first plurality of Reed Solomon (RS) coded data bytes within the shared memory" and, at least for this reason, claim 1 of the '048 patent is not obvious in view of LB-031 and Mazzoni.

227. Also, because a POSITA would be discouraged from combining the teaching of LB-031 with the teachings of Mazzoni, as explained in Section VI.B.2, *supra*, the combination of the combination of LB-031 and Mazzoni does not render claim 1 of the '048 patent obvious.

- d. **The combination of LB-031 and Mazzoni does not disclose a transceiver that is capable of allocating a first number of bytes of the shared memory to the interleaver to interleave the first plurality of Reed Solomon (RS) coded data bytes for transmission at a first data rate, wherein the allocated memory for the interleaver does not exceed the maximum number of bytes in the message.**

228. As explained in Section VI.A.2.c, *supra*, LB-031 does not disclose or suggest allocating the first number of bytes of the shared memory to the interleaver to interleave a first plurality of Reed Solomon (RS) coded data bytes for transmission at a first data rate, wherein the allocated memory for the interleaver does not exceed the maximum number of bytes in the message. This is so at least because LB-031 does not disclose shared memory, as explained in Sections VI.A.1, VI.A.2.a, and VI.A.5.a.ii.

229. As explained in Section VI.B.3.b, *supra*, Mazzoni does not disclose transmitting or receiving any message with interleaver or deinterleaver parameters. Further, as explained in Section VI.B.2, *supra*, LB-031's exchange of interleaver and deinterleaver capabilities is redundant to Mazzoni's stored predefined service data rates and interleaver/deinterleaver parameters and incompatible with Mazzoni at least because the exchange of maximum supported interleaver and deinterleaver sizes per LB-031 would specify a combined amount of interleaver and deinterleaver memory that would exceed Mazzoni's total memory size. Accordingly, the combination of LB-031 and Mazzoni does not disclose "a transceiver that is capable of allocating a first number of bytes of the shared memory to the interleaver to interleave the first plurality of Reed Solomon (RS) coded data bytes for transmission at a first data rate, wherein the allocated memory for the interleaver does not exceed the maximum number of bytes in

the message” and, at least for this reason, claim 1 of the ‘048 patent is not obvious in view of LB-031 and Mazzoni.

230. I note that Dr. Jacobsen cites to Mazzoni at column 1:19-27 for purportedly disclosing the portion of this claim element that recites “wherein the allocated memory for the interleaver does not exceed the maximum number of bytes in the message.” Jacobsen Report at ¶ 280. She does not provide any explanation for how this portion of Mazzoni discloses this claim element. I have reviewed this portion of Mazzoni and it does not in any way disclose this claim element. Rather, it is a generic background section regarding VDSL, asymmetrical and symmetrical data rates, and the fact that modems that operate at predetermined bit rates have interleaver and deinterleaver memories that depend on that bit rate. This background section actually emphasizes, consistent with my opinions, that Mazzoni is directed to providing predefined services with predetermined bit rates and corresponding predefined interleaver and deinterleaver parameters, which would not require, or benefit from, an exchange of capabilities per LB-031.

4. The Combination of LB-031 and Mazzoni Does Not Render Claim 5 of the ‘381 Patent Obvious

231. It is my opinion for the reasons provided in Section VI.B.2 above and as further discussed in this Section VI.B.4, that a POSITA would not combine LB-031 and Mazzoni or arrive at the claimed invention even if one were to attempt to combine these references in some way. It is further my opinion and conclusion that LB-031 in

combination with Mazzoni fails to disclose each element of claim 5 of the '381 patent, and hence fails to render claim 5 of the '381 patent obvious as described in detail, below.

- a. **The combination of LB-031 and Mazzoni does not disclose a non-transitory computer-readable information storage media having stored thereon instructions, that if executed by a processor, cause to be performed a method for allocating shared memory in a transceiver.**

232. As explained in Section VI.A.3.a, *supra*, LB-031 does not disclose a non-transitory computer-readable information storage media having stored thereon instructions, that if executed by a processor, cause to be performed a method for allocating shared memory in a transceiver. *See also* § VI.A.2.a, *supra*; *see generally* § VI.A.1, *supra*.

233. More generally, LB-031 also does not disclose the exchange of information that would be useful for allocating shared memory. *See id.* As explained above, LB-031 only describes exchanging information about the maximum size of dedicated interleaver memory and, separately, the maximum size of dedicated deinterleaver memory supported by a transceiver. At least for the reasons explained, in paragraph 211 above, this information could not be used by a Mazzoni transceiver to allocate shared memory. As described in Section VI.A.2.a, LB-031 does not include any disclosure directed to allocating shared memory in a transceiver. Consequently, at least for the same reasons as described with respect to claim 1 of the '048 patent, LB-031 fails to disclose this element of claim 5 of the '381 patent.

234. As explained above in the Overview of Mazzoni section, Mazzoni relies on a predetermined assignment of a service that has a predetermined pair of upstream

and downstream bit rates and a corresponding set of predetermined interleaver and deinterleaver parameter values, I , M , I' and M' . See § VI.B.1. The predetermined assignment takes place when the modem is installed by retrieving the bit rates and parameter values from a stored table. Mazzoni at 6:55-69. Thus, contrary to Dr. Jacobsen's opinion with respect to claim 1 of the '048 patent (incorporated by reference here), Mazzoni does not disclose exchanging any messages at all that include information about interleaving or deinterleaving parameters as described above in connection with claim 1 of the '048 patent. See also, § VI.B.3.b, *supra*.

235. Furthermore, Dr. Jacobsen did not identify any portions of LB-031 that disclose a non-transitory computer-readable information storage media having stored thereon instruction that are executed by a processor in Section IX.B.4.a of the Jacobsen Report addressing this claimed element. Nor has she done that in Section IX.A.4.a of the Jacobsen Report, which seems relevant but was not even incorporated by reference. See Jacobsen Report at ¶ 210; see also *id.* at ¶ 300. With respect to LB-031, as explained in Section VI.A.3.a above, Dr. Jacobsen without any support simply draws an inference that “[o]ne of ordinary skill in the art would have understood that a source code and instructions for such transceivers could be stored on computer-readable information storage media, and could be executed by a processor.” See *id.* Dr. Jacobsen makes the same argument with respect to Mazzoni. See Jacobsen Report at ¶ 300 (“One of ordinary skill in the art would have understood that source code and instructions for such transceiver could be stored on computer-readable information storage media, and could be executed by a processor, for example, as source or object code.”).

236. As explained in Section VI.A.3.a, *supra*, Dr. Jacobsen's conclusion is wrong on its face. Source code (or object code) cannot be executed by a processor. A POSITA would understand that source code (or object code) is a term of art referring to uncompiled and non-executable human readable code.

237. Also, as explained in Section VI.A.3.a, *supra* with respect to LB-031, and now with respect to Mazzoni, even ignoring the fact that Dr. Jacobsen's conclusion is wrong on its face, Dr. Jacobsen did not show that any element of claim 5 of the '381 patent is performed by executing instructions stored on a non-transitory computer-readable information media. A POSITA would understand that it is possible that one or more of the claimed functions could be implemented in hardware, and therefore would not necessarily have to be carried out through an execution of instructions stored on a non-transitory computer-readable media. Dr. Jacobsen did not even attempt to show one way or another with which of these possibilities LB-031 or Mazzoni would be concerned with respect to each claimed function.

238. Finally, Mazzoni does not disclose the claimed non-transitory computer-readable information storage media having stored thereon instructions, that if executed by a processor, cause to be performed a method for allocating shared memory in a transceiver at least because Mazzoni does not disclose (1) transmitting or receiving, by the transceiver, a message during initialization specifying a maximum number of bytes of memory that are available to be allocated to a deinterleaver (*see* § VI.B.4.b, *infra* and § VI.B.3.b, *supra*); (2) determining, at the transceiver, an amount of memory required by the deinterleaver to deinterleave a first plurality of Reed Solomon (RS) coded data bytes

within a shared memory (*see* § VI.B.4.c, *infra* and § VI.B.3.c, *supra*); and (3) allocating, in the transceiver, a first number of bytes of the shared memory to the deinterleaver to deinterleave a first plurality of Reed Solomon (RS) coded data bytes for transmission at a first data rate, wherein the allocated memory for the deinterleaver does not exceed the maximum number of bytes specified in the message (*see* § VI.B.4.d, *infra* and § VI.B.3.d, *supra*).

239. Also, because a POSITA would have no rational reason to combine the LB-031 with Mazzoni, as explained in Section VI.B.2, *supra*, the combination of the combination of LB-031 and Mazzoni does not render claim 5 of the '381 patent obvious.

240. It is my opinion that LB-031 does not disclose, teach, or suggest this claim element of claim 5 of the '381 patent and therefore fails to render claim 5 of the '381 Patent obvious.

- b. The combination of LB-031 and Mazzoni does not disclose transmitting or receiving, by the transceiver, a message during initialization specifying a maximum number of bytes of memory that are available to be allocated to a deinterleaver.**

241. Contrary to Dr. Jacobsen's assertion, Mazzoni does not disclose exchanging any messages at all that include information about interleaving or deinterleaving parameters. Dr. Jacobsen asserts that her discussion with respect to an interleaver in Section IX.B.3.c is equally applicable to a deinterleaver. *See* Jacobsen Report at ¶ 303. I have addressed the arguments from that section in Section VI.B.3.b, *supra*.

242. Because Mazzoni does not describe any message specifying an amount of memory that can be allocated to an interleaver or to a deinterleaver, and because LB-031's exchange of interleaver and deinterleaver capabilities would be useless and incompatible with Mazzoni (*see* § VI.B.2, *supra*), the combination of LB-031 and Mazzoni does not disclose "transmitting or receiving, by the transceiver, a message during initialization specifying a maximum number of bytes of memory that are available to be allocated to a deinterleaver" and, at least for this reason, claim 5 of the '381 patent is not obvious in view of LB-031 and Mazzoni.

- c. **The combination of LB-031 and Mazzoni does not disclose determining, at the transceiver, an amount of memory required by the deinterleaver to deinterleave a first plurality of Reed Solomon (RS) coded data bytes within a shared memory.**

243. Dr. Jacobsen assert that Mazzoni discloses this limitation by incorporating her arguments from paragraph 269 of the Jacobsen Report. *See* Jacobsen Report at ¶ 305. I disagree for the reasons discussed in Section VI.B.3.c. My arguments directed to interleaving are equally applicable to deinterleaving.

244. Because Mazzoni does not describe a transceiver that determines deinterleaver parameters or memory sizes, and because requiring Mazzoni to do so it would be contrary to Mazzoni's simplified scheme of storing predetermined values, the combination of LB-031 and Mazzoni does not disclose "determining, at the transceiver, an amount of memory required by the deinterleaver to deinterleave a first plurality of Reed Solomon (RS) coded data bytes within a shared memory" and, at least for this reason, claim 5 of the '381 patent is not obvious in view of LB-031 and Mazzoni.

245. Also, because a POSITA would be discouraged from combining the teaching of LB-031 with the teachings of Mazzoni, as explained in Section VI.B.2, *supra*, the combination of the combination of LB-031 and Mazzoni does not render claim 5 of the '381 patent obvious.

- d. **The combination of LB-031 and Mazzoni does not disclose allocating, in the transceiver, a first number of bytes if the shared memory to the deinterleaver to deinterleave a first plurality of Reed Solomon (RS) coded data bytes for transmission at a first data rate, wherein the allocated memory for the deinterleaver does not exceed the maximum number of bytes specified in the message.**

246. As explained in Sections VI.A.3.c and VI.A.3.d, LB-031 does not disclose allocating, in the transceiver, a first number of bytes if the shared memory to the deinterleaver to deinterleave a first plurality of Reed Solomon (RS) coded data bytes for transmission at a first data rate, wherein the allocated memory for the deinterleaver does not exceed the maximum number of bytes specified in the message. This is so at least because LB-031 does not disclose shared memory, as explained in, for example, Sections VI.A.2.a, VI.A.5.a.ii.

247. As explained in Section VI.B.3.b, *supra*, Mazzoni does not disclose transmitting or receiving any message with interleaver or deinterleaver parameters. Further, as explained in Section VI.B.2, *supra*, LB-031's exchange of interleaver and deinterleaver capabilities is redundant to Mazzoni's stored predefined service data rates and interleaver/deinterleaver parameters and incompatible with Mazzoni at least because the exchange of maximum supported interleaver and deinterleaver sizes per LB-031 would specify a combined amount of interleaver and deinterleaver memory that

would exceed Mazzoni's total memory size. Accordingly, the combination of LB-031 and Mazzoni does not disclose "allocating, in the transceiver, a first number of bytes if the shared memory to the deinterleaver to deinterleave a first plurality of Reed Solomon (RS) coded data bytes for transmission at a first data rate, wherein the allocated memory for the deinterleaver does not exceed the maximum number of bytes specified in the message" and, at least for this reason, claim 5 of the '381 patent is not obvious in view of LB-031 and Mazzoni.

248. I also note that in a section incorporated by reference, Dr. Jacobsen cites to Mazzoni at column 1:19-27 for purportedly disclosing the portion of the claim element that recites "wherein the allocated memory for the *interleaver* does not exceed the maximum number of bytes in the message." Jacobsen Report at ¶ 280. She does not provide any explanation for how this portion of Mazzoni discloses this claim element. I have reviewed this portion of Mazzoni and it does not in any way disclose this claim element. Rather, it is a generic background section regarding VDSL, asymmetrical and symmetrical data rates, and the fact that modems that operate at predetermined bit rates have interleaver and deinterleaver memories that depend on that bit rate. This background section actually emphasizes, consistent with my opinions, that Mazzoni is directed to providing predefined services with predetermined bit rates and corresponding predefined interleaver and deinterleaver parameters, which would not require, or benefit from, an exchange of capabilities per LB-031. At least for the same reason, Mazzoni does not disclose this claim element that recites "wherein the allocated

memory for the *deinterleaver* does not exceed the maximum number of bytes specified in the message.”

5. The Combination of LB-031 and Mazzoni Does Not Render Claim 13 of the ‘882 Patent Obvious

249. It is my opinion for the reasons provided in Section VI.B.2 above and as further discussed in this Section VI.B.5, that a POSITA would not combine LB-031 and Mazzoni or arrive at the claimed invention even if one were to attempt to combine these references in some way. It is further my opinion and conclusion that LB-031 in combination with Mazzoni fails to disclose each element of claim 13 of the ‘882 patent, and hence fails to render claim 13 of the ‘882 patent obvious as described in detail, below.

a. The Combination of LB-031 and Mazzoni does not disclose a system that allocates shared memory.

250. LB-031 does not disclose, teach, or suggest this claim element of claim 13 of the ‘882 Patent for the same reason as discussed with respect to the same claim element of claim 1 of the ‘048 Patent. *See* § VI.B.3.a, *supra*.

b. The Combination of LB-031 and Mazzoni does not disclose other elements of this claim.

251. Dr. Jacobsen adopts wholesale her arguments with respect to claim 5 of the of the ‘381 patent (elements 5[b] – 5[h]) as her argument with respect to claim 13 of the ‘882 patent (elements 13[c] through 13[i], respectively). *See* Jacobsen Report at ¶ 320.

252. Accordingly, I hereby incorporate my arguments with respect to claim elements of claim 5 of the ‘381 patent, and also claim 1 of the ‘048 Patent as rebuttal argument for the respective claim elements of claim 13 of the ‘882 patent.

253. Specifically, using the claim element numbering from Dr. Jacobsen Report (see Appendix C to Jacobsen Report), I hereby incorporate herein the following sections of this report:

- with respect to elements 13[b] and 13[c], I incorporate §§ VI.B.3.b, VI.B.4.b, *supra*;
- with respect to elements 13[b] and 13[d], I incorporate §§ VI.B.3.c, VI.B.4.c, *supra*;
- with respect to elements 13[b], 13[e], and 13[f], I incorporate §§ VI.B.3.d, VI.B.4.d, *supra*;

254. The Combination of LB-031 and Mazzoni does not disclose, teach, or suggest the above claim elements of claim 13 of the '882 Patent for the same reason as discussed with respect to the substantially similar claim elements of claim 5 of the '381 Patent, and claim 1 of the '048 Patent. At least for these reasons, it is my opinion and conclusion that the Combination of LB-031 and Mazzoni fails to disclose or suggest all elements of claim 13 of the '882 Patent.

6. The Combination of LB-031 and Mazzoni Does Not Render Claim 19 of the '473 Patent Obvious

255. It is my opinion for the reasons provided in Section VI.B.2 above and as further discussed in this Section VI.B.6, that a POSITA would not combine LB-031 and Mazzoni or arrive at the claimed invention even if one were to attempt to combine these references in some way. It is further my opinion and conclusion that LB-031 in combination with Mazzoni fails to disclose each element of claim 19 of the '473 patent,

and hence fails to render claim 19 of the '473 patent obvious as described in detail, below.

- a. **The Combination of LB-031 and Mazzoni does not disclose a multicarrier transceiver being associated with a memory wherein the memory is allocated between the interleaving function and the deinterleaving function in accordance with a message received during an initialization of the transceiver.**

256. For the reasons discussed above in Section VI.A.5.a, LB-031 does not disclose this claim element.

257. Further, contrary to Dr. Jacobsen's opinion, Mazzoni does not disclose exchanging any messages at all that include information about interleaving or deinterleaving parameters (or any other information upon which interleaver or deinterleaver memory allocations could be based). Dr. Jacobsen asserts that "[o]ne of ordinary skill in the art would have understood that this information, as well as capabilities of the transceiver at the other end of the system, would have to be conveyed, for example, in the form of a message during initialization, and that the memory would be allocated between the interleaving function and the deinterleaving function in accordance with that message." Jacobsen Report at ¶ 339. The "information" she is referring to is the parameters I , M , I' and M' . But, she cannot point to any disclosure of such a message in Mazzoni because there is no such disclosure. Instead, it seems that she is interpreting Mazzoni's description of the configurability of its interleaver means and deinterleaver means according to upstream and downstream bit rates as somehow disclosing reliance on an exchange of I , M , I' and M' . See *id.* (citing Mazzoni at 1:61-65 and 5:24-31). But parameters I , M , I' and M' are not exchanged in

any message; rather, as discussed above in Section VI.B.1, these parameters are stored in a table in each transceiver and indexed to a predefined service that includes predefined upstream and downstream bit rates. Mazzoni at 6:53-61. The parameter values for the particular predefined service are retrieved by the control means MCD at the time the modem is installed (*id.*) and delivered by the MCD to the interleaver means MET and deinterleaver means MDET (*id.* at 5:21-23 and Fig. 3). This eliminates any need to exchange these parameters between modems.

258. One of the passages Dr. Jacobsen cites for this assertion, Mazzoni at column 5:24-31, does not describe some alternative embodiment where the I, M, I' and M' parameters are exchanged in messages. Rather, this passage simply describes the use of the predetermined parameters that are indexed to the predetermined service bit rates the transceiver has been configured to use. Dr. Jacobsen accurately admits this elsewhere in her report. *See, e.g.,* Jacobsen Report at ¶ 595 (“Mazzoni discloses keeping a table of values of the interleaver parameters, indexed by service identifiers, in the transceiver. *See id.* at col. 6:51-61. As a person having ordinary skill in the art as of the ’473 patent’s priority date would have understood, Mazzoni’s table is limiting in that all of the services would have to be identified ahead of time and stored in the transceivers.”); *see also id.* at ¶ 626.

259. The other passage Dr. Jacobsen relies on for this assertion, Mazzoni at column 1:61-65, also does not disclose or require the exchange of any interleaver or deinterleaver parameters in a message. To the extent Dr. Jacobsen is interpreting this passage as disclosing anything other than the use of predetermined parameters that

correspond to predetermined bit rates, she has misunderstood Mazzoni. In fact, the sentence after the one she quotes shows that the reference to “the bit rate actually processed by the send/receive device (modem)” is referring to one of the predetermined bit rates for a predetermined service. Mazzoni at 1:65 – 2:2 (“The invention therefore provides a device for sending/receiving digital data that is capable of *processing different bit rates from a group of predetermined bit rates* (e.g., all the symmetrical or asymmetrical services offered by the VDSL communication system).”).

260. While neither LB-031 or Mazzoni individually disclose this claim element, as explained in Section VI.B.2, *supra*, LB-031’s exchange of interleaver and deinterleaver capabilities is redundant to Mazzoni’s stored predefined service data rates and interleaver/deinterleaver parameters and incompatible with Mazzoni at least because the exchange of maximum supported interleaver and deinterleaver sizes per LB-031 would specify a combined amount of interleaver and deinterleaver memory that would exceed Mazzoni’s total memory size. Accordingly, the combination of LB-031 and Mazzoni does not disclose “a multicarrier transceiver being associated with a memory wherein the memory is allocated between the interleaving function and the deinterleaving function in accordance with a message received during an initialization of the transceiver” and, at least for this reason, claim 19 of the ‘473 patent is not obvious in view of LB-031 and Mazzoni.

- b. The combination of LB-031 and Mazzoni does not disclose a multicarrier transceiver being associated with a memory wherein at least a portion of the memory may be allocated to the interleaving function or the deinterleaving function at any one particular time depending on the message.**

261. For the reasons discussed above in Section VI.A.5.b, LB-031 does not disclose this claim element.

262. With respect to Mazzoni, Dr. Jacobsen's conclusion in paragraph 343 of the Jacobsen Report that "[o]ne of ordinary skill in the art would have understood that the interleaving means and the deinterleaving means would operate at the same time" does not appear to address this claim element. That an interleaver and deinterleaver operate at the same time does not disclose or require that a portion of the memory be allocated to the interleaver function or deinterleaver function at any one particular time depending on the message. Perhaps this was a cut and paste error and was intended for the element of claim 5 of the '381 patent, which recites: "wherein the shared memory allocated to the deinterleaver is used at the same time as the shared memory allocated to the interleaver."

263. Dr. Jacobsen further asserts paragraph 344 of the Jacobsen Report that "Mazzoni also discloses that the portion of the memory allocated to the interleaving function or the deinterleaving function at any one particular time is dependent on the message." I disagree. As I explained in the section immediately above, Mazzoni does not disclose exchanging any messages at all that include information about interleaving or deinterleaving parameters (or any other information upon which interleaver or deinterleaver memory allocations could be based). Further, as I explained in the section

immediately above and in Section VI.B.2, *supra*, LB-031's exchange of interleaver and deinterleaver capabilities is redundant to and incompatible with Mazzoni.

264. For at least the foregoing reasons, the combination of LB-031 and Mazzoni does not disclose "wherein at least a portion of the memory may be allocated to the interleaving function or the deinterleaving function at any one particular time depending on the message" and, at least for this reason, claim 19 of the '473 patent is not obvious in view of LB-031 and Mazzoni.

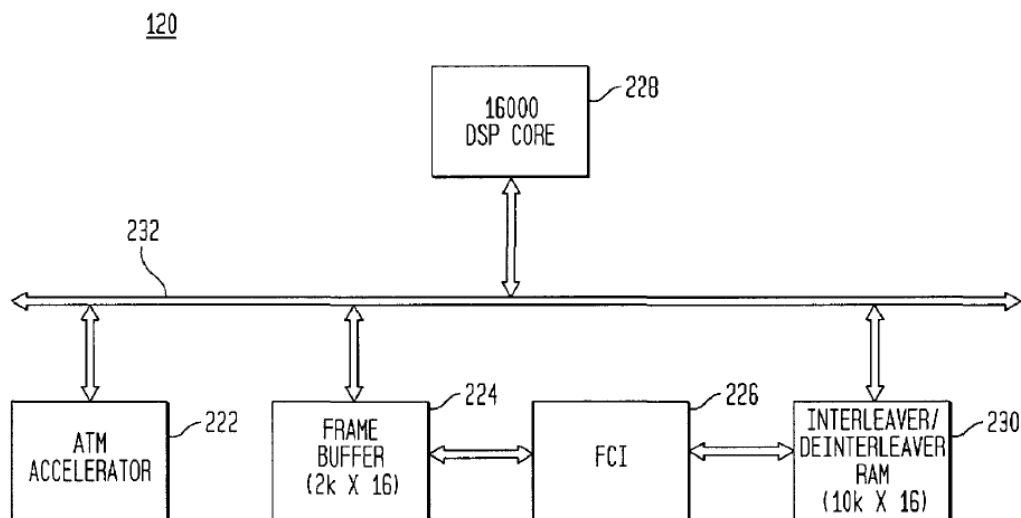
C. The Asserted Claims Are Not Obvious Over Fadavi-Ardekani in Combination with ITU-T Recommendation G.993.1

1. Overview of Fadavi-Ardekani

265. As an initial matter, U.S. Patent No. 6,707,822 to Fadavi-Ardekani et al., hereinafter Fadavi, was considered by the USPTO during the prosecution of the parent, U.S. Patent 7,831,890, and the claims were allowed over Fadavi. *See*, Notice of Allowance for '890 patent. Fadavi is also cited on the face of each of the Family 3 Patents.

266. Fadavi discloses "an Asymmetric Digital Subscriber Line (ADSL) transceiver that manages multiple asynchronous ADSL sessions, synchronizing the digital signal processing tasks for the sessions with a buffering and scheduling scheme such that the various transceiver components operate seamlessly (i.e., in a semi-synchronous fashion)." Fadavi at 2:62-68. Fadavi defines an agent as "a transceiver component for performing some function." *Id.* at 5:62-63. Fadavi discloses several

agents including the ATM accelerator, the Framer/Coder/Interleaver (FCI) and the DSP core. Set forth below is a block diagram of the transceiver taught by Fadavi.



Fadavi at FIG. 2.

267. The organization of the various agents and related components of Fadavi's transceiver is as follows:

An Asynchronous Transfer Mode (ATM) Accelerator provides the network interface to multiple ATM channels for multiple asynchronous ADSL sessions. The ATM accelerator transfers frame data to a Frame Buffer (FB) as controlled by a Digital Signal Processing (DSP) core. The FB provides a dual access memory that is used in a **ping-pang** fashion, based on the logic level of the virtual clock, for the communication of data between the ATM accelerator and a Framer/Coder/Interleaver (FCI). The FCI performs various processing tasks on the frame data and also interfaces the DSP core through an Interleave/De-interleave Memory (IDIM), which holds DMT frames of data and may also be utilized in a ping-pang fashion. . . . The DSP core controls operation of the ATM accelerator and the FCI and performs various processing tasks such as moving data to/from the FB and the IDIM.

Fadavi at 3:8-25 (emphasis added).

“Ping-pang” means that areas of the memory buffer are alternately utilized exclusively by one agent (a transceiver component for performing some function) and then by a second agent. As one area of memory is being used by a first agent, another area of memory can be used by a different agent.

Id. at 5:60-65.

The ATM accelerator provides those functions that are responsible for data transport for a plurality of data streams communicated via twisted pair media. The data may be transported on anyone of a plurality of programmable bearer channels. The data is synchronized into an appropriate one of the plurality of programmable bearer channels and the channels multiplexed in the ATM accelerator as determined by the ADSL standard. The ATM accelerator subjects this framed data to various operations that calculate a plurality of complex numbers representing DMT tones. The ATM accelerator subsequently transfers this DMT tone data on the twisted-pair media.

Id. at 5:43-54.

The FCI . . . performs various tasks on payload data including: framing/de-framing, cyclic redundancy check generation/checking (CRCing), scrambling/descrambling, Reed-Solomon encoding/decoding, and interleaving/de-interleaving. . . . All functionalities of the FCI are provided as per ADSL standards. In a preferred embodiment of the invention, approximately four G.lite (ITU G.992.2) or approximately four ADSL (ANSI T1.413-1998) sessions are supported by the FCI.

Id. at 6:20-23.

268. Fadavi explains that the FB and IDIM memories are accessed in ping-pang fashion by the agents. Specifically, [t]he Frame Buffer (FB) 224 provides a dual access memory that is used in a ping-pang fashion to transfer unframed bearer channel data between the ATM accelerator 222 and the FCI 226.” *Id.* at 5:57-60. The FCI and ATM accelerator first perform reading processes and then loading processes, reading RX data first before loading the TX data into the FB.

269. The IDIM is used in a ping-pang fashion by the FCI and DSP core.

Specifically,

The Interleave/De-Interleave Memory (IDIM) 230 provides a memory through which the FCI 226 interfaces the DSP core 228. The IDIM holds DMT frames of data and may be utilized in a ping-pang fashion. The IDIM is used to transfer framed, coded and possibly interleaved data frames between the FCI core and the DSP Core.

Id. at 6:55-60.

In a preferred embodiment of the invention, the IDIM is allocated as 10 Kx16 (i.e., 20 K) Random Access Memory (RAM), which supports approximately four G .lite or approximately four standard ADSL session/s at less than full interleave depth. The size of the IDIM and the interleave depth may be varied so that a different number of sessions may be supported by the transceiver of the invention. The size of the IDIM is derived as follows. A simple implementation of a transmit interleaver for G.lite communication requires 4 Kbytes per session for downstream processing, derived by multiplying the maximum codeword length by the maximum interleaver depth. The simple G.lite transmit interleaver also requires 2 Kbytes per session for upstream processing. Therefore, 24 Kbytes of RAM is required to support four G.lite sessions. Similarly, a simple implementation of a transmit interleaver for standard ADSL requires 16 Kbytes per session for downstream processing and 2 Kbytes per session for upstream processing, for a total of 72 Kbytes for four sessions. A fast path buffer is also required for fast path data in both the interleave and dc-interleave processes and requires 256 bytes of RAM per session, or a total of 1 Kbytes for four sessions. Since the smallest RAM block currently available is 1 Kx16, 1 Kx160 or 2 Kbytes must be allocated for the fast path buffer per direction. Therefore, a simple implementation of an interleaver would require 76 Kbytes for four standard ADSL sessions (64 K interleave +8 K de-interleave +4 K fast path). An optimal implementation of the interleaver according to the method of the invention utilizes the same memory for receive data and transmit data and thus requires 20 Kbytes to support a standard ADSL session at full interleave depth (16 K interleave & de-interleave +4 K fast path). With a lesser interleave depth, additional sessions may be supported with the same size buffer. With a larger buffer, additional session may be supported.

The IDIM is used in a ping-pang fashion by the FCI and DSP core.

270. Based on the foregoing, Fadavi teaches using an IDIM whose size is “derived by multiplying the maximum codeword length by the maximum interleaver depth.” To support additional sessions, Fadavi teaches reducing the interleaver depth or using a larger memory.

2. Fadavi-Ardekani in combination with G.993.1 does not disclose all the limitations of claim 1 of the '048 patent

a. Fadavi-Ardekani does not disclose “a system that allocates shared memory”

271. Dr. Jacobsen’s contends that the IDIM disclosed in Fadavi is the claimed shared memory, (Jacobsen Report at Id. at ¶ 371), and that the interleaving and deinterleaving functions in the FCI “share” the IDIM. *See*, Jacobsen Report at ¶¶ 390 and 400. The Court construed shared memory as “common memory used by at least two functions, where a portion of the memory can be used by either one of the functions.” As explained below, in view of Fadavi’s disclosure, the IDIM is not a common memory used by at least the interleaving and deinterleaving functions, where a portion of the memory can be used by either the interleaving or deinterleaving functions.

272. Fadavi teaches that:

The size of the IDIM is derived as follows. A simple implementation of a transmit interleaver for G.lite communication requires 4 Kbytes per session for downstream processing, derived by multiplying the maximum codeword length by the maximum interleaver depth. The simple G.lite transmit interleaver also requires 2 Kbytes per session for upstream processing. Therefore, 24 Kbytes of RAM is required to support four G.lite sessions. Similarly, a simple implementation of a transmit interleaver for standard ADSL requires 16 Kbytes per session for downstream processing and 2 Kbytes per session for upstream processing, for a total of 72 Kbytes

for four sessions. A fast path buffer is also required for fast path data in both the interleave and de-interleave processes and requires 256 bytes of RAM per session, or a total of 1 Kbytes for four sessions. Since the smallest RAM block currently available is 1Kx16, 1Kx160 or 2 Kbytes must be allocated for the fast path buffer per direction. Therefore, a simple implementation of an interleaver would require 76 Kbytes for four standard ADSL sessions (64 K interleave + 8 K de-interleave + 4 K fast path).

273. Based on the foregoing passage of Fadavi, a POSITA would understand that the size of the IDIM memory depends on the number of sessions/connections that the transceiver is designed to support. Fadavi at 7:6-10 (“**4 Kbytes** per session for downstream processing, . . . **2 Kbytes** per session for upstream processing. Therefore, **24 Kbytes** of RAM [(4+2) x 4] is required to support **four** G.lite sessions.”). In an ADSL implementation, the transceiver is equipped with “76 Kbytes for four standard ADSL sessions (64 K interleave +8 K de-interleave +4 K fast path)”. *Id.* at 7:23-25. Fadavi explains that the memory sizes are “derived by **multiplying the maximum codeword length by the maximum interleaver depth.**” Fadavi at 7:8-10 (emphasis added). Given that the memory available for interleaving and deinterleaving is the maximum required by the DSL standards, the memory set aside for use by the interleaving function will never be used by the deinterleaving function. Even if the interleaving function uses less than all its memory, because for example, the far-end deinterleaver has lesser memory, the unused memory will not be used by the deinterleaving function because Fadavi contemplates that sufficient memory is set aside for use by the deinterleaver. Accordingly, a POSITA would understand that the IDIM described in Fadavi is not the claimed shared memory.

274. Dr. Jacobsen suggests that the IDIM is the claimed shared memory because Fadavi teaches that the IDIM “may be utilized in a ping-pang fashion.” Jacobsen Report at ¶ 371 (citing Fadavi at 6:57-58). I disagree that the ping-pang usage of the IDIM indicates that the IDIM is shared memory. Fadavi explains that ping-pang usage of the IDIM means that “[a]s one area of memory is being used by a first agent, another area of memory can be used by a different agent.” Fadavi at 5:60-65. “When the memory is used in ping-pang fashion, ‘[a]s long as different agents . . . access different areas of a dual access memory, there are no memory address conflicts that could cause communication errors.’” Jacobsen Report at Id. at ¶ 371 (citing Fadavi at 5:65-6:1). Thus, Fadavi merely teaches that the IDIM is a “dual access memory” and that an agent accesses its own area of the IDIM. Thus, although the IDIM is shared between different agents, for the reasons set forth at ¶ 273, the IDIM is not “shared memory,” as construed.

275. Fadavi also discloses “[a]n optimal implementation of the interleaver that utilizes the same memory for receive data and transmit data.” Fadavi at 7:25-30. To the extent, Dr. Jacobsen suggests that this “optimal implementation” teaches a shared memory, I disagree. The optimal implementation is incompatible with the DSL standards and accordingly a POSITA would not be motivated to use the optimal implementation, much less use the optimal implementation in combination with the G.993.1 standards. *See*, VI.C.6, *infra*.

- b. **Fadavi-Ardekani in combination with G.993.1 does not disclose “a transceiver capable of . . . allocating a first number of bytes of the shared memory to the interleaver . . . wherein the allocated memory for the interleaver does not exceed the maximum number of bytes specified in the message”**

276. As an initial matter, none of the sections of the G.993.1 standard that Dr. Jacobsen cites between ¶¶ 387-397 of the Jacobsen Report, suggests that a 993.1-compliant VTU-O necessarily includes a shared memory, *i.e.*, “common memory used by at least two functions, where a portion of the memory can be used by either one of the functions.” To the extent, Dr. Jacobsen suggests that G.993.1 at § 8.4.1 teaches “allocating a first number of bytes of the shared memory to the interleaver . . .” *See*, Jacobsen Report at ¶ 389, I disagree. § 8.4.1 provides that “[t]he interleave depth shall be programmable with a maximum interleave depth of 64 codewords when the number of octets per codeword (N) equals 255.” However, G.993.1 does not disclose or require the use of a “shared memory” by the interleaver and deinterleaver. For example, a transceiver could be designed with a fixed amount of memory that is used for interleaving, where the amount of memory corresponds to the maximum interleave depth mandated by the standard. Rather, a POSITA would understand G.993.1 to provide for dedicated downstream memories in each transceiver and separate, dedicated upstream memories in each transceiver. The use of such dedicated memories is consistent with other ADSL and G.Lite-compliant modems of that era and proposals for VDSL modems, including the LB-031 modem. *See* §§ IV and VI.A.5.a.ii, *supra*. As explained in these cited sections above, portions of dedicated interleaver memory that are not needed for interleaving cannot be allocated for use by the deinterleaver, and

vice versa. Instead, those portions simply go unused. *Id.* In fact, as described above at § VI.C.2.a, this is precisely the scheme disclosed in Fadavi.

277. Specifically, Fadavi teaches that “[t]he size of the IDIM . . . is derived by multiplying the *maximum codeword length* by the *maximum interleaver depth*.” Fadavi at 7:5-10. Thus, the interleaver in Fadavi is provided with a dedicated amount of memory and the interleaver may use as much as is needed based on the codeword length and interleaver depth. Similarly, the deinterleaver in Fadavi is provided with a dedicated amount of memory and the deinterleaver may use as much as is needed based on the codeword length and interleaver depth. Irrespective of the contents of the initialization messages transmitted or received, no portion of the IDIM set aside for use the interleaving function will ever be allocated for use by the deinterleaving function, and vice versa. And although initialization messages may be exchanged to communicate the capabilities of far-end transceiver, because Fadavi equips each of its interleaver and deinterleaver with the maximum amount of memory contemplated by the standard, there is no scenario where unused interleaving memory will be allocated for use by the deinterleaver, and vice versa.

278. Dr. Jacobsen incorrectly asserts that “[i]n allocating memory for each of the lines, Fadavi-Ardekani discloses determining the amount of memory to support different sessions required by the transceiver. *See*, Jacobsen Report at ¶ 396 (citing Fadavi at 7:3-33). This is a gross mischaracterization of the cited portion of Fadavi. Fadavi teaches using pre-determined amounts of memory derived by multiplying the *maximum codeword length* by the *maximum interleaver depth*, as mandated by the relevant

standard. Fadavi does teach that “with a lesser depth, additional sessions may be supported with the same size buffer” and “[w]ith a larger buffer, additional session[s] may be supported.” Fadavi at 7:30-33. However, this does not suggest that Fadavi allocates shared memory. This merely confirms that Fadavi uses pre-determined amounts of memory per session and precludes any need to use the content of the O-MSG2 message to allocate memory. Accordingly, I disagree with Dr. Jacobsen’s assertion at paragraph 396 that a POSITA “would have understood, based on the disclosures of Fadavi-Ardekani, that the allocated memory for the interleaver for each of the supported lines, which would have been determined based on the content of the O-MSG2 message transmitted by the VTU-O corresponding to that line, would not exceed the requirements the VTU-O set for itself in O-MSG2.”

279. Based on the foregoing, it is my opinion that the combination of Fadavi and G.993.1 does not disclose this limitation.

- c. **The combination of Fadavi-Ardekani and G.993.1 does not disclose “allocating a second number of bytes of the shared memory to a deinterleaver to deinterleave a second plurality of RS coded data bytes received at a second data rate”**

280. For at least the same reasons set forth in section VI.C.2.b, *supra*, my opinion is that the combination of Fadavi and G.993.1 does not disclose this claim element.

3. Fadavi-Ardekani in combination with G.993.1 does not disclose all the limitations of claim 5 of the '381 patent

- a. Fadavi-Ardekani does not disclose “a non-transitory computer-readable information storage media having stored thereon instructions, that if executed by a processor, cause to be performed a method for allocating shared memory in a transceiver”**

281. At least for the reasons set forth at § VI.C.2.a, *supra*, Fadavi does not include a “shared memory.” Accordingly, Fadavi cannot include “a non-transitory computer-readable information storage media having stored thereon instructions, that if executed by a processor, cause to be performed a method for allocating shared memory in a transceiver.”

- b. Fadavi-Ardekani in combination with G.993.1 does not disclose “a transceiver capable of . . . allocating a first number of bytes of the shared memory to the deinterleaver . . . wherein the allocated memory for the deinterleaver does not exceed the maximum number of bytes specified in the message”**

282. At least for the reasons articulated at § VI.C.2.b, *supra*, the combination of Fadavi and G.993.1 does not disclose this limitation. It is noteworthy and worth reiterating that Dr. Jacobsen merely asserts that “[o]ne of ordinary skill in the art would have understood that . . . allocating memory to an interleaver in Fadavi-Ardekani and G.993.1 apply equally to allocating memory to a deinterleaver.” Jacobsen Report at ¶ 142. Dr. Jacobsen does not contend that Fadavi and G.993.1 describe allocating shared memory.

- c. **Fadavi-Ardekani in combination with G.993.1 does not disclose “allocating a second number of bytes of the shared memory to a interleaver to interleave a second plurality of RS coded data bytes received at a second data rate”**

283. At least for the reasons articulated at § VI.C.2.b, *supra*, the combination of Fadavi and G.993.1 does not disclose this limitation.

- 4. **Fadavi-Ardekani in combination with G.993.1 does not disclose all the limitations of claim 13 of the '882 patent**

- a. **Fadavi-Ardekani does not disclose “a system that allocates shared memory”**

284. At least for the reasons set forth at § VI.C.2.a, *supra*, Fadavi does not include a “shared memory.” Accordingly, Fadavi does not disclose a system that allocates shared memory.

- b. **Fadavi-Ardekani in combination with G.993.1 does not disclose “a transceiver capable of . . . allocating a first number of bytes of the shared memory to the deinterleaver . . . wherein the allocated memory for the deinterleaver does not exceed the maximum number of bytes specified in the message”**

285. At least for the reasons articulated at § VI.C.2.b, the combination of Fadavi and G.993.1 does not disclose this limitation.

- c. **Fadavi-Ardekani in combination with G.993.1 does not disclose “allocating a second number of bytes of the shared memory to a interleaver to interleave a second plurality of RS coded data bytes received at a second data rate”**

286. At least for the reasons articulated at § VI.C.2.b, the combination of Fadavi and G.993.1 does not disclose this limitation.

5. **Fadavi-Ardekani in combination with G.993.1 does not disclose all the limitations of claim 19 of the '473 patent**

- a. **The combination of Fadavi and G.993.1 does not disclose a multicarrier communications transceiver associated with a memory “wherein the memory is allocated between the interleaving function and the deinterleaving function in accordance with a message received during an initialization of the transceiver”**

287. Fadavi does not disclose “allocating memory **between** an interleaving function and a deinterleaving function.” Dr. Jacobsen contends that the IDIM described in Fadavi is “allocate[ed] between an interleaving function and a deinterleaving function.” Jacobsen Report at ¶ 446. I disagree.

288. Dr. Jacobsen states that Fadavi teaches that “[a] portion of the memory is allocated to an interleaver by determining the size of the memory needed to interleave a certain amount of data.” Jacobsen Report at ¶ 447. Dr. Jacobsen mischaracterizes Fadavi. The interleaver is assigned a pre-determined amount of memory the size of which “is derived by multiplying the maximum codeword length by the maximum interleaver depth.” Fadavi at 7:5-10.

289. Dr. Jacobsen contends that the ping-pang usage of the IDIM means that the “memory is allocated between the interleaving function and the deinterleaving function” Jacobsen Report at ¶ 446. However, the claims require that the allocation of memory between the interleaving function and the deinterleaving function take place *in accordance with a message received during initialization*. Dr. Jacobsen has not alleged that such is the case in Fadavi.

290. Dr. Jacobsen also contends that a transceiver can use the parameters specified in the O-MSG2 and R-MSG2 messages described in the G.993.1 standard, “to allocate memory between an interleaver and a deinterleaver.” Jacobsen Report at ¶¶ 447-448. Rather, a POSITA would understand G.993.1 to provide for dedicated downstream memories in each transceiver and separate, dedicated upstream memories in each transceiver. The use of such dedicated memories is consistent with other ADSL and G.Lite-compliant modems of that era and proposals for VDSL modems, including the LB-031 modem. *See* §§ IV and VI.A.5.a.ii, *supra*). As explained in these cited sections above, portions of dedicated interleaver memory that are not needed for interleaving cannot be allocated for use by the deinterleaver, and vice versa. Instead, those portions simply go unused. *Id.*

291. Additionally, as previously explained, the transceiver described in Fadavi is designed such that the interleaver and deinterleaver are each provided with a pre-determined amount of memory that equates to the maximum amounts mandated by the standards. If the interleaver uses less than its assigned memory for any reason, the unused memory is not used by the deinterleaver because the deinterleaver is provided with a pre-determined amount of memory that equates to the maximum amount it may require. Thus, the IDIM is not allocated between the interleaving and deinterleaving functions. Accordingly, even if Fadavi is modified to use the O-MSG2 and R-MSG2, the IDIM would not be “allocated *between* the interleaving function and the deinterleaving function in accordance with” these messages.

- b. **The combination of Fadavi and G.993.1 does not disclose a multicarrier communications transceiver associated with a memory “wherein at least a portion of the memory may be allocated to the interleaving function or the deinterleaving function at any one particular time depending on the message”**

292. Fadavi does not disclose this limitation. As I previously explained, the interleaving and deinterleaving functions in Fadavi are each assigned a pre-determined amount of memory “derived by multiplying the maximum codeword length by the maximum interleaver depth.” Fadavi at 7:5-10. Given that each function is provided with its maximum memory requirement, there is no situation where a portion of the memory assigned to the interleaving function may be allocated to the deinterleaving function and vice versa.

293. With respect to the G.993.1 standard, Dr. Jacobsen contends that because “G.993.1 uses Frequency Division Duplexing (FDD),” “data would need to be interleaved and deinterleaved at the same time in this mode of transmission, which would require that a portion of the memory be allocated to an interleaving function, and a portion of the memory would be allocated to a deinterleaving function.” Jacobsen Report at ¶ 452. Based on this, Dr. Jacobsen concludes that “G.993.1 discloses that at least a portion of the memory may be allocated to the interleaving function or the deinterleaving function at any one particular time.” *Id.* I disagree. The claim requires that “at least a portion of the memory may be allocated to the interleaving function or the deinterleaving function at any one particular time depending on the message.” The claim limitation is not met simply when “a portion of the memory [is] allocated to an

interleaving function, and a portion of the memory [is] allocated to a deinterleaving function,” as Dr. Jacobsen apparently contends.

294. Accordingly, it is my opinion that the combination of Fadavi-Ardekani and G.993.1 does not disclose this limitation.

6. A POSITA would not have been motivated to combine Fadavi-Ardekani and G.993.1

295. For the following reasons, I disagree with Dr. Jacobsen’s assertion at paragraphs 454-459 of the Jacobsen Report that “one of ordinary skill in the art as of the Family 3 patents’ priority date would have been motivated to combine the teachings of Fadavi-Ardekani with the teachings of G.993.1 in the manner claimed.”

296. First, Dr. Jacobsen asserts that that there is a motivation to combine because both references are in the telecommunications field and relate to DSL systems. See Jacobsen Report at ¶ 454. This in and of itself, or in combination with any other argument made by Dr. Jacobsen in Section IX.C.7 of the Jacobsen Report, is not sufficient show that a person of ordinary skill in the art would have combined the teachings of the two references. That both references are in the telecommunications field is simply far too broad and general of a field to say that that a POSITA would be motivated to combine any one of the many thousands of diverse telecommunications techniques, or any particular feature or function thereof. Further, at the time of the inventions of the Family 3 Patents, the DSL standards were under continuous development and there were likely hundreds, if not thousands, of references directed to possible implementation details of many and varied proposals for DSL transceivers.

One of skill in the art at the time would have understood that many of these references would be completely incompatible with one another and/or, if combined, would provide no useful benefit. Thus, that Fadavi and G.993.1 are purportedly both directed to different proposals for DSL transceivers, would not have made their combination obvious.

297. I further disagree with Dr. Jacobsen's premise that both Fadavi and G.993.1 describe the need to allocate memory for interleaving and deinterleaving functions. Dr. Jacobsen's opinion that "[o]ne of ordinary skill in the art naturally would have consulted Fadavi-Ardekani for its description of calculating memory needs and allocating memory between interleaver and deinterleaver functions" is not supported by the disclosure of Fadavi. Jacobsen Report at ¶ 456. Contrary to Dr. Jacobsen's assertion, Fadavi merely teaches providing each interleaver and deinterleaver with a dedicated amount of memory, the size of which is "derived by multiplying the maximum codeword length by the maximum interleaver depth." At least for this reason, a POSITA would not be motivated to modify Fadavi, to allocate memory based on the initialization messages described in G.993.1.

298. Dr. Jacobsen relies on the "optimal implementation of the interleaver" described in Fadavi to demonstrate that Fadavi includes a shared memory. Specifically, Dr. Jacobsen asserts that "Fadavi-Ardekani further describes allocating the IDIM memory between transmit and receive functions." Jacobsen Report at ¶ 372 (citing Fadavi at 7:25-30 ("An optimal implementation of the interleaver according to the method of the invention utilizes the same memory for receive data and transmit data

and thus requires 20 Kbytes to support a standard ADSL session at full interleave depth (16 K interleave & de-interleave +4 K fast path)."). It is my opinion that a POSITA would recognize that this implementation would be inoperable with G.993.1.

299. In the optimal implementation, Fadavi discloses that the same memory is used for receive and transmit data, alternately. Data received (deinterleave data) during one cycle will be overwritten by transmit data (interleave data) during a subsequent cycle. The G.993.1 standard requires that "[t]he interleave depth shall be programmable with a maximum interleave depth of 64 codewords when the number of octets per codeword (N) equals 255." G.993.1 at § 8.4.1. A POSITA would recognize that a codeword, after interleaving, will necessarily span multiple (typically many) DMT frames and that all the DMT frames will not be received during one cycle. Consequently, the deinterleaving operation cannot be completed during that cycle. However, during the next cycle the received deinterleave data will be overwritten with interleave data that must be interleaved and transmitted. This means that received data will not be correctly deinterleaved. For this reason, a POSITA would be not have combined the teachings of the G.993.1 and Fadavi.

300. I also disagree with Dr. Jacobsen's assertion that a skilled artisan would have been motivated to combine the size- and cost-saving approach of Fadavi-Ardekani with the transceivers of G.993.1 to reduce the cost, size, and power consumption of the VTU-Os that would be deployed in optical network units or cabinets. Jacobsen Report at ¶ 457. A POSITA would recognize that modifying Fadavi to use the initialization messages described in G.993.1 would add to complexity. Further, in view of that fact

that the memory sizes in Fadavi are “derived by multiplying the maximum codeword length by the maximum interleaver depth,” processing and using the initialization messages of G.993.1 would bring no benefit to Fadavi.

301. For these reasons, a POSITA would not be motivated to combine the teachings of Fadavi and G.993.1.

D. The Asserted Claims Are Not Obvious Over Fadavi-Ardekani in Combination with ITU-T Recommendation G.992.2

1. Fadavi-Ardekani in combination with G.992.1 does not disclose all the limitations of claim 1 of the '048 patent

a. Fadavi-Ardekani does not disclose “a system that allocates shared memory”

302. For the reasons set forth at § VI.C.2.a, *supra*, Fadavi-Ardekani does not disclose “a system that allocates shared memory.”

b. Fadavi-Ardekani in combination with G.992.2 does not disclose “a transceiver capable of . . . allocating a first number of bytes of the shared memory to the interleaver . . . wherein the allocated memory for the interleaver does not exceed the maximum number of bytes specified in the message”

303. For the reasons set forth at § VI.C.2.b, *supra*, I disagree that Fadavi’s system includes the capability to “allocat[e] a first number of bytes of the shared memory to a interleaver” much less the capability to “allocat[e] a first number of bytes of the shared memory” such that “the allocated memory . . . does not exceed the maximum number of bytes specified in the message.”

304. Separately, Dr. Jacobsen contends that C-RATES1, R-RATES1, C-RATES-RA, R-RATES2 and C-RATES2 messages “can be used to allocate memory to implement” the interleaver. However, Dr. Jacobsen neglects to consider the plain

meaning of the claims. The claims require allocating bytes of the shared memory, where the shared memory is “common memory used by at least two functions where a portion of the memory can be used by either one of the functions.” Like the G.993.1 standard, the G.992.2 standard does not require that a transceiver implement a “shared memory” much less “allocat[e] a first number of bytes of the shared memory to an interleaver.” Rather, a POSITA would understand G.992.2 to provide for dedicated downstream memories in each transceiver and separate, dedicated upstream memories in each transceiver. The use of such dedicated memories is consistent with other ADSL and G.Lite-compliant modems of that era and proposals for VDSL modems, including the LB-031 modem. *See* §§ IV and VI.A.5.a.ii, *supra*. As explained in these cited sections above, portions of dedicated interleaver memory that are not needed for interleaving cannot be allocated for use by the deinterleaver, and vice versa. Instead, those portions simply go unused. *Id.* Accordingly, the combination of Fadavi and the G.992.2 does not disclose this claim limitation.

- c. **Fadavi-Ardekani in combination with G.992.2 does not disclose “allocating a second number of bytes of the shared memory to a deinterleaver to deinterleave a second plurality of RS coded data bytes received at a second data rate”**

305. For at least the same reasons set forth at § VI.D.1.b, *supra*, my opinion is that the combination of Fadavi and G.992.2 does not disclose this claim element.

2. Fadavi-Ardekani in combination with G.992.2 does not disclose all the limitations of claim 5 of the '381 patent

- a. Fadavi-Ardekani does not disclose “a non-transitory computer-readable information storage media having stored thereon instructions, that if executed by a processor, cause to be performed a method for allocating shared memory in a transceiver”**

306. At least for the reasons set forth at §§ VI.C.2.a and VI.C.3.a, Fadavi does not disclose this element.

- b. Fadavi-Ardekani in combination with G.992.2 does not disclose “a transceiver capable of . . . allocating a first number of bytes of the shared memory to the deinterleaver . . . wherein the allocated memory for the deinterleaver does not exceed the maximum number of bytes specified in the message”**

307. For the reasons set forth at § VI.D.1.b, the combination of Fadavi and G.992.2 does not disclose this element.

- c. Fadavi-Ardekani in combination with G.992.2 does not disclose “allocating a second number of bytes of the shared memory to a interleaver to interleave a second plurality of RS coded data bytes received at a second data rate”**

308. For the reasons set forth at § VI.D.1.b, *supra*, the combination of Fadavi and G.992.2 does not disclose this element.

3. Fadavi-Ardekani in combination with G.992.2 does not disclose all the limitation of claim 13 of the '882 patent

- a. Fadavi-Ardekani does not disclose “a system that allocates shared memory”**

309. For the reasons set forth at § VI.C.2.a, *supra*, Fadavi-Ardekani does not disclose “a system that allocates shared memory.”

- b. **Fadavi-Ardekani in combination with G.992.2 does not disclose “a transceiver capable of . . . allocating a first number of bytes of the shared memory to the deinterleaver . . . wherein the allocated memory for the deinterleaver does not exceed the maximum number of bytes specified in the message”**

310. For the reasons set forth at § VI.D.1.b, *supra*, the combination of Fadavi and G.992.2 does not disclose this element.

- c. **Fadavi-Ardekani in combination with G.992.2 does not disclose “allocating a second number of bytes of the shared memory to a interleaver to interleave a second plurality of RS coded data bytes received at a second data rate”**

311. For the reasons set forth at § VI.D.1.b, *supra*, the combination of Fadavi and G.992.2 does not disclose this element.

- 4. **Fadavi-Ardekani in combination with G.992.2 does not disclose all the limitation of claim 19 of the '473 patent**

- a. **The combination of Fadavi and G.992.2 does not disclose a multicarrier communications transceiver associated with a memory “wherein the memory is allocated between the interleaving function and the deinterleaving function in accordance with a message received during an initialization of the transceiver”**

312. For the reasons set forth at § VI.C.5.a, *supra*, Fadavi does not disclose this element. Separately, the G.992.2 standard does not disclose this limitation. Dr. Jacobsen contends that certain initialization messages “can be used to allocate memory between an interleaver and a deinterleaver.” Jacobsen Report at ¶ 524. The G.992.2 standard, however, does not teach using the initialization messages to allocate memory between an interleaver and a deinterleaver. Rather, a POSITA would understand G.992.2 to provide for dedicated downstream memories in each transceiver and separate, dedicated upstream memories in each transceiver. The use of such dedicated

memories is consistent with other ADSL and G.Lite-compliant modems of that era and proposals for VDSL modems, including the LB-031 modem. *See* §§ IV and VI.A.5.a.ii, *supra*. As explained in these cited sections above, portions of dedicated interleaver memory that are not needed for interleaving cannot be allocated for use by the deinterleaver, and vice versa. Instead, those portions simply go unused. *Id.*

b. The combination of Fadavi and G.992.2 does not disclose a multicarrier communications transceiver associated with a memory “wherein at least a portion of the memory may be allocated to the interleaving function or the deinterleaving function at any one particular time depending on the message”

313. Fadavi does not disclose this limitation. *See* § VI.C.5.b, *supra*.

314. With respect to the G.992.2 standard, Dr. Jacobsen contends that because G.992.2 establishes a “single duplex bearer channel,” one of ordinary skill in the art would have understood that data is transmitted in both directions at the same time and as a result, the interleaver and deinterleaver are both used at the same time. Jacobsen Report at ¶ 526. Based on this, Dr. Jacobsen concludes that G.992.2 discloses that at least a portion of the memory may be allocated to the interleaving function or the deinterleaving function at any one particular time. *Id.* I disagree. The claim requires that “at least a portion of the memory may be allocated to the interleaving function or the deinterleaving function at any one particular time depending on the message.” The claim limitation is not met simply when a portion of the memory is allocated to an interleaving function, and a portion of the memory is allocated to a deinterleaving function,” as Dr. Jacobsen apparently contends.

315. Accordingly, it is my opinion that the combination of Fadavi-Ardekani and G.992.2 does not disclose this limitation.

5. A POSITA would not have been motivated to combine Fadavi-Ardekani and G.992.2

316. For the following reasons, I disagree with Dr. Jacobsen's assertion at paragraphs 527-531 of the Jacobsen Report that "one of ordinary skill in the art as of the Family 3 patents' priority date would have been motivated to combine the teachings of Fadavi-Ardekani with the teachings of G.992.2 in the manner claimed."

317. First, Dr. Jacobsen asserts that that there is a motivation to combine because both references are in the telecommunications field and relate to ADSL systems. *See* Jacobsen Report at ¶ 527. This in and of itself, or in combination with any other argument made by Dr. Jacobsen in Section IX.D.6 of the Jacobsen Report, is not sufficient show that a person of ordinary skill in the art would have combined the teachings of the two references. That both references are in the telecommunications field is simply far too broad and general of a field to say that that a POSITA would be motivated to combine any one of the many thousands of diverse telecommunications techniques, or any particular feature or function thereof. Further, at the time of the inventions of the Family 3 Patents, the DSL standards were under continuous development and there were likely hundreds, if not thousands, of references directed to possible implementation details of many and varied proposals for DSL transceivers. One of skill in the art at the time would have understood that many of these references would be completely incompatible with one another and/or, if combined, would

provide no useful benefit. Thus, that Fadavi and G.992.2 are purportedly both directed to different proposals for DSL transceivers, would not have made their combination obvious.

318. I further disagree with Dr. Jacobsen's premise that both Fadavi and G.992.2 describe the need to allocate memory for interleaving and deinterleaving functions. Dr. Jacobsen opinion that "[o]ne of ordinary skill in the art naturally would have consulted Fadavi-Ardekani for its description of calculating memory needs and allocating memory between interleaver and deinterleaver functions" is not supported by the disclosure of Fadavi. Jacobsen Report at ¶ 528. Contrary to Dr. Jacobsen's assertion, Fadavi merely teaches providing each interleaver and deinterleaver with a dedicated amount of memory, the size of which is "derived by multiplying the maximum codeword length by the maximum interleaver depth." At least for this reason, a POSITA would not be motivated to modify Fadavi, to allocate memory based on the initialization messages described in G.992.2.

319. Dr. Jacobsen relies on the "optimal implementation of the interleaver" described in Fadavi to demonstrate that Fadavi includes a shared memory. Specifically, Dr. Jacobsen asserts that "Fadavi-Ardekani further describes allocating the IDIM memory between transmit and receive functions." Jacobsen Report at ¶ 372 (citing Fadavi at 7:25-30 ("An optimal implementation of the interleaver according to the method of the invention utilizes the same memory for receive data and transmit data and thus requires 20 Kbytes to support a standard ADSL session at full interleave depth

(16 K interleave & de-interleave +4 K fast path)."). It is my opinion that a POSITA would recognize that this implementation would be inoperable with G.992.2.

320. In the optimal implementation, Fadavi discloses that the same memory is used for receive and transmit data, alternately. Data received (deinterleave data) during one cycle will be overwritten by transmit data (interleave data) during a subsequent cycle. The G.992.2 standard requires that "The Reed-Solomon codewords shall be convolutionally interleaved." G.992.2 at § 7.6. A POSITA would recognize that a codeword, after interleaving, will necessarily span multiple (typically many) DMT frames and that all the DMT frames will not be received during one cycle. Consequently, the deinterleaving operation cannot be completed during that cycle. However, during the next cycle the received deinterleave data will be overwritten with interleave data that must be interleaved and transmitted. This means that received data will not be correctly deinterleaved. For this reason, a POSITA will be dissuaded from combining the teachings of the G.992.2 and Fadavi.

321. Separately, a POSITA would recognize that modifying Fadavi to use the initialization messages described in G.992.2 would add to complexity. Further, in view of that fact that the memory sizes in Fadavi are "derived by multiplying the maximum codeword length by the maximum interleaver depth," processing and using the initialization messages of G.992.2 would bring no benefit to Fadavi.

322. For these reasons, a POSITA would not be motivated to combine the teachings of Fadavi and G.992.2.

E. Claim 19 of the '473 Patent Is Not Obvious Over Voith in Combination with LB-031

323. It is my opinion and conclusion that Voith alone or in combination with LB-031 fails to disclose or suggest each element of the claim 19 of the '473 patent, and hence fails to render the claim 19 of the '473 patent obvious as described in detail, below.

324. It is also my opinion that regardless of the disclosures of Voith and LB-031 individually, a person of ordinary skill in the art would not be motivated to combine the teachings of Voith with the teachings of LB-031 at least for the reasons described in Section VI.E.3, *infra*.

325. An overview of LB-031 has been provided in Section VI.A.1, *supra*.

1. **Neither Voith nor LB-031 discloses a multicarrier communications transceiver associated with a memory “wherein the memory is allocated between the interleaving function and the deinterleaving function in accordance with a message received during an initialization of the transceiver”**

326. Dr. Jacobsen contends that “Voith discloses allocating memory between the interleaving function and the dinterleaving (sic) function” because Voith states that the interleaver “uses a portion of external interleave/deinterleave memory 66.” Jacobsen Report at ¶ 557 (citing Voith at 5:65-61). This is not correct. It does not follow from the fact that the external memory is used for both interleaving and deinterleaving that any portion of the memory is allocated *between* these functions.

327. Dr. Jacobsen has not shown that any portion of the interleave/deinterleave memory 66 is disclosed by Voith to be used as interleaver memory at one point in time and deinterleaver memory at another point in time.

Therefore, there is no basis for concluding that Voith allocates memory between an interleaving function and a deinterleaving function. Rather, a POSITA reviewing Voith's disclosure of an external interleave/deinterleave memory 66, would understand this as disclosing that the memory includes a dedicated portion for use by interleaver 78 and a separate, dedicated portion for use by deinterleaver 90. Such a predetermined division of separate, dedicated memories is consistent with other ADSL and G.Lite-compliant modems of that era and proposals for VDSL modems, including the LB-031 modem. *See* §§ IV and VI.A.5.a.ii, *supra*. As explained in these cited sections above, portions of dedicated interleaver memory that are not needed for interleaving cannot be allocated for use by the deinterleaver, and vice versa. Instead, those portions simply go unused. *Id.*

328. Further, Voith does not disclose performing any allocation of interleaver or deinterleaver memory "in accordance with a message received during an initialization of the transceiver." The only reference to a "message" in Dr. Jacobsen analysis for this claim element is the single conclusory sentence that "the bit allocation table is determined during initialization by the receiving transceiver and communicated to the transmitting transceiver in a message sent during the initialization procedure." Jacobsen Report at ¶ 558. Dr. Jacobsen appears to be relying on a message such as the O-B&G message described in the G.993.1 standard (§ 12.4.6.2.1.3 ("O-B&G shall signal the end of the contract negotiation and shall be used to transmit to the VTU-R the bits and the gains information that are to be used in the upstream direction.")) or the C-B&G message described in the G.992.2 standard (§ 11.11.13) as a message used for the

claimed memory allocation. However, Dr. Jacobsen provides no evidence that Voith teaches that ADSL transceiver 34 allocates memory 66 between the interleaver 78 and the deinterleaver 90 based on a bit-allocation message. Accordingly, I disagree that “Voith discloses wherein the *memory is allocated* between the interleaving function and the deinterleaving function *in accordance with a message received during an initialization of the transceiver*,” as Dr. Jacobsen alleges. Jacobsen Report at ¶ 558.

329. With respect to LB-031, as I previously explained at § VI.A.5.a, *supra*, LB-031 does not disclose this element. Specifically, LB-031 only teaches that the “VTU-O and VTU-R would then select the smaller of the transmitter and receiver capabilities in each direction, as the end-to-end capabilities.” LB-031 at p. 3. Accordingly, LB-031 at most discloses that a VTU-O (or a VTU-R) determines whether it can use all of its predetermined maximum interleaver memory or whether it has to use less of it because of the maximum capabilities of the deinterleaver on the other side of the line, are smaller. However, LB-031 does not teach that the unused portion of the interleaver memory can be allocated to the deinterleaver. Accordingly, LB-031 does not teach “the memory is allocated *between* the interleaving function and the deinterleaving function depending on a message.”

330. Accordingly, it is my opinion that neither Voith nor LB-031, alone or in combination, discloses this limitation.

2. **Neither Voith nor LB-031 discloses a multicarrier communications transceiver associated with a memory “wherein at least a portion of the memory may be allocated to the interleaving function or the deinterleaving function at any one particular time depending on the message”**

331. Voith does not disclose this limitation. Voith merely teaches that a first portion of memory 66 is used by the interleaver 78 and a second portion of memory 66 is used by the deinterleaver 90. Voith does not teach that this apportioning is performed based on a message. *See Supra* at ¶ 367. Additionally, Voith does not teach that any portion of the memory 66 may be allocated to the interleaver 78 *or* the deinterleaver 90 at any one particular time depending on a message.

332. Dr. Jacobsen has not pointed to any disclosure or teaching in Voith that states, or necessarily requires, that it uses memory where any portion is shared between an interleaving function and a deinterleaving function. Rather, a POSITA reviewing Voith’s disclosure of an external interleave/deinterleave memory 66, would understand this as disclosing that the memory includes a dedicated portion for use by interleaver 78 and a separate, dedicated portion for use by deinterleaver 90. Such a predetermined division of separate, dedicated memories is consistent with other ADSL and G.Lite-compliant modems of that era and proposals for VDSL modems, including the LB-031 modem *See* §§ IV and VI.A.5.a.ii, *supra*. As explained in these cited sections above, portions of dedicated interleaver memory that are not needed for interleaving cannot be allocated for use by the deinterleaver, and vice versa. Instead, those portions simply go unused. *Id.*

333. Dr. Jacobsen asserts that a POSITA would interpret Voith, including the sentences “[i]nterleaver 78 arbitrates for use of external interleave/deinterleave memory 66 with the deinterleaver 90” (Voith at 6:1-4) and “deinterleaver 90 makes use of external interleave/deinterleave memory 66 and arbitrates for usage thereof in a manner similar to interleaver 78” (*id.* at 26-29), as disclosing that “a portion of the memory may be allocated to the interleaving function or the deinterleaving function at any one particular time.” Jacobsen Report at ¶¶ 557 and 562. I disagree. These sentences only mean that the interleaver 78 and deinterleaver 90 contend for access to the “external memory interface” in order to access external memory 66. Such contention for access to the external memory interface in general does not indicate in any way that the interleaver 78 and deinterleaver 90 are contending for or using, or capable of contending for or using, the same portions of the memory.

334. With reference to LB-031, for the same reasons set forth at Section VI.A.5.a and b, *supra*, LB-031 does not disclose this limitation.

3. No Motivation to Combine Voith with LB-031

335. For the following reasons, I disagree with Dr. Jacobsen’s assertion at paragraphs 566-568 of the Jacobsen Report that “one of ordinary skill in the art would have been motivated to combine Voith and LB-031.”

336. First, Dr. Jacobsen asserts that that there is a motivation to combine because both references are “in the telecommunications field.” Jacobsen Report at ¶ 566. This in and of itself, or in combination with any other argument made by Dr. Jacobsen in Section IX.E.3 of the Jacobsen Report, is not sufficient show that a person of

ordinary skill in the art would have combined the teachings of the two references. This is simply far too broad and general of a field to say that that a POSITA would be motivated to combine any one of the many thousands of diverse telecommunications techniques, or any particular feature or function thereof.

337. Dr. Jacobsen further asserts that there is a motivation to combine because each of the references purportedly “discloses sharing memory for interleaving and deinterleaving to support various applications.” *Id.* at ¶ 566. This in and of itself, or in combination with any other argument made by Dr. Jacobsen in Section IX.E.3 of the Jacobsen Report, is not sufficient to motivate a person of ordinary skill in the art to combine the teaching of the two references.

338. Also, this assertion is not accurate. As explained in VI.A.1, *supra*, LB-031 is concerned with providing a solution that meets certain delay requirements specified in units of time, while allowing use of larger dedicated interleaver or deinterleaver memories if both transceivers support more than the minimum required by a standard. There is no technique described in LB-031 for “sharing memory for interleaving and deinterleaving to support various applications,” contrary to Dr. Jacobsen assertions. *See* § VI.A.1., *supra*. Rather, as I explained above, LB-031 describes a dedicated interleaver memory and a separate, dedicated deinterleaver memory where portions of a dedicated memory that is left unused by one function – because one transceiver supports more memory for a given latency path than is supported by the other transceiver with which it is communicating – is not available for use by the other function.. *See* § VI.A.5.a and ¶¶ 169-178, *supra*.

339. Voith also does not disclose “sharing memory for interleaving and deinterleaving to support various applications.” Jacobsen Report at ¶ 567. Voith merely teaches that it is preferable to implement the memory buffers off-chip, because “large buffers consume a large integrated circuit area which adds to its cost.” Voith at 2:27-28. Thus, Voith’s fundamental premise is to concede that the memory buffers are required to be large but Voith makes no proposal for reducing such requirement. Voith certainly does not propose the use of sharing memory for interleaving and deinterleaving where a portion of the memory can be used at one time for interleaving and at another time for deinterleaving as explained immediately above in sections VI.E.1 and 2.

340. Therefore, it is my opinion that a POSITA would not be motivated to combine Voith and LB-031, particularly not in any manner “wherein at least a portion of the memory may be allocated to the interleaving function or the deinterleaving function at any one particular time depending on the message.”

F. Claim 19 of the '473 Patent Is Not Obvious Over Mazzoni and G.993.1

1. A Person of Ordinary Skill in the Art Would Not Combine the Teachings of Mazzoni with the Teachings of G.993.1

341. A person of ordinary skill in the art at the time of the invention of the Family 3 Patents would not look to the teachings of Mazzoni when implementing the teachings of G.993.1, or *vice versa*. In fact, as explained below, the two references are so different that a person of ordinary skill in the art would be discouraged from looking to the teaching of the other reference.

342. The overview of Mazzoni has been provided in Section VI.B.1, *supra*.

343. G.993.1, akin to LB-031, is yet another reference that employs a dedicated interleaver memory and a dedicated deinterleaver memory. Dr. Jacobsen relies on G.993.1 for its “initialization message scheme.” See Jacobsen Report at ¶ 595.

344. Dr. Jacobsen asserts that a reason to combine Mazzoni and G.993.1 is that both are “directed to VDSL and to VDSL transceivers.” See Jacobsen Report at ¶ 592. This in and of itself, or in combination with any other argument made by Dr. Jacobsen in Section VIII.F.4 of the Jacobsen Report, is not sufficient show that a person of ordinary skill in the art would have combined the teachings of the two references. At the time of the invention of the Family 3 Patents, the VDSL standard was still under development and there were likely hundreds of references directed to possible implementation details of many and varied proposals for VDSL transceivers. One of skill in the art at the time would have understood that many of these references would be completely incompatible with one another and/or, if combined, would provide no useful benefit. Thus, that Mazzoni and G.993.1 are both directed to different proposals for developing VDSL transceivers, would not have made their combination obvious.

345. Dr. Jacobsen then states that “each of Mazzoni and G.993.1 discloses a need to allocate memory for interleaving and deinterleaving.” See Jacobsen Report at ¶ 593. This in and of itself, or in combination with any other argument made by Dr. Jacobsen in Section VIII.F.4 of the Jacobsen Report, is again not sufficient to motivate a person of ordinary skill in the art to combine the teaching of the two references. It is far too general of a concept to provide any motivation to combine one reference with the

other. In fact, it is not materially different than saying that Mazzoni and G.993.1 contemplate the use of memories for interleaving and deinterleaving.

346. Dr. Jacobsen states that: “[a]s a person having ordinary skill in the art as of the ‘473 patent’s priority date would have understood, Mazzoni’s table is limiting in that all of the services would have to be identified ahead of time and stored in the transceivers. One of ordinary skill in the art would have recognized that conveying interleaver parameters through initialization message scheme of G.993.1 would avoid this limitation of Mazzoni’s table and would result in a more flexible solution.” *See* Jacobsen Report at ¶ 595. This is incorrect.

347. A POSITA would not look to add a message (from G.993.1 or otherwise) to the system disclosed in Mazzoni, and in fact doing so would provide no useful benefit. This is because the system disclosed in Mazzoni relies on the use of a pre-populated table of I, M, I’, and M’ parameter values, where each set of values corresponds to a respective one of a number of predetermined data rate service pairs. *See* Mazzoni at 5:22-23, 5:27-30, 6:51-55. There is no use for a message that specifies the maximum supported interleaver or deinterleaver memory size because all data rate pairs and their corresponding I, M, I’, and M’ values that need to be supported are accounted for. Mazzoni contemplates TO and TU transceiver pairs that will both be preconfigured at the time of installation with the same predetermined parameters selected from a limited number of possibilities. Thus, exchanging messages describing the capabilities of the transceivers would be redundant and serve no useful purpose.

348. “Flexibility” is also too generic of a motivation to combine and, in any event, Mazzoni provides substantial flexibility already given that it allows 12 difference service configurations. One of skill in the art who perceived the benefits of the simplicity of configuration that Mazzoni provides would not be motivated to use the complex messaging and initialization scheme of G.993.1.

349. An additional reason why G.993.1’s exchange of maximum supported memory sizes would not be recognized as beneficial to Mazzoni is that it is incompatible. For example, per G.993.1, the VTU-R (i.e., TU of Mazzoni) transmits to the VTU-O (i.e., TO of Mazzoni) an R-MSG2 message that specifies the maximum downstream deinterleaver memory size that it supports. Then the VTU-O transmits to the VTU-R an O-MSG2 message that specifies the maximum upstream interleaver memory size it can support. Using the predefined services described in Mazzoni, i.e., S1-S6 and A1-A6 (*see* Mazzoni at 3:62 – 4:14), the maximum downstream deinterleaver memory that Mazzoni is capable of supporting is determined by reference to the A6 service and the maximum upstream interleaver memory that Mazzoni is capable of supporting is determined by reference to the S6 service. The A6 service provides a downstream bit rate of 832x64 kbit/s and requires 24,960 bytes of deinterleaver memory. *See id.* at 6:11-30 (describing calculation of required deinterleaver memory size). The S6 service provides an upstream bit rate of 362x64 kbit/s. Per the calculations described at 6:11-30 of Mazzoni, the S6 service requires that the VTU-R be capable of supporting a maximum upstream interleaver memory of 10,860 bytes. If the Mazzoni VTU-O received a message indicating that the VTU-R supported a maximum

downstream deinterleaver memory of 24,960 bytes and a maximum upstream interleaver memory of 10,860 bytes (based on the maximum interleaver delay), this information would be useless to the VTU-O. First, it already has the information necessary to support the service for which both transceivers have been preconfigured at the time of installation. Second, neither the VTU-O or VTU-R would actually be capable of simultaneously supporting both maximum interleaver and deinterleaver sizes at the same time because the total memory size of the Mazzoni transceivers is only 26,890 bytes (as determined by the combined upstream and downstream bit rates of the A6 service). *See id.* at 4:18-22 and 6:45-50.

350. Further, while Dr. Jacobsen does not put forth any argument regarding any other messages in her report (I reserve the right to respond to any such new argument to the extent she is allowed to raise it), per G.993.1, after the exchange of the R-MSG2 and the O-MSG2 messages, the VTU-R transmits an R-CONTRACT1 message to the VTU-O including a “proposed downstream contract.” Subsequently, the VTU-O transmits the O-CINTRACT1 message to the VTU-R which contains a proposed upstream contract and a downstream contract, where the downstream contract is based on the R-CONTRACT1. Again, Mazzoni already has the information necessary to support the service for which both transceivers have been preconfigured at the time of installation and does not need to rely on messages to convey the redundant information.

351. A POSITA at the time of the Family 3 Patent inventions would not combine the teachings of Mazzoni with the teachings of G.993.1. In fact, a POSITA would be discouraged from doing so. Because Mazzoni teaches that an assignment of the memory is performed at the time of the installation of the modem based on a table, and not a message, adding a message (or multiple messages) to this system per G.993.1 would be unnecessary, redundant, and create useless complexity during initialization. Further, because Mazzoni is concerned with supporting a finite set of predefined service configurations (i.e., data rate pairs and corresponding interleaver/deinterleaver parameter values).

352. For at least the foregoing reasons, Dr. Jacobsen has not demonstrated that a POSITA would have been motivated to combine G.993.1 with Mazzoni in the manner she proposes.

2. The Combination of Mazzoni and G.993.1 Does Not Render Claim 19 of the '473 Patent Obvious

353. It is my opinion for the reasons provided in Section VI.F.1 above and as further discussed in this Section VI.F.2, that a POSITA would not combine Mazzoni and G.993.1 or arrive at the claimed invention even if one were to attempt to combine these references in some way. It is further my opinion and conclusion that Mazzoni in combination with G.993.1 fails to disclose each element of claim 19 of the '473 patent, and hence fails to render claim 19 of the '473 patent obvious as described in detail, below.

- a. **The Combination of Mazzoni and G.993.1 does not disclose a multicarrier transceiver being associated with a memory wherein the memory is allocated between the interleaving function and the deinterleaving function in accordance with a message received during an initialization of the transceiver.**

354. Mazzoni in combination with G.993.1 does not disclose this limitation. Dr. Jacobsen incorporates by reference her arguments with respect to Mazzoni by pointing to Section IX.B.6.e of the Jacobsen Report. These arguments have been addressed in Section VI.B.6.a, *supra* and further below.

355. Dr. Jacobsen then points to Section IX.C.6.e of the Jacobsen Report for support that “G.993.1 teaches sending messages during initialization that indicate maximum interleaver delay, as well as ways of allocating memory between an interleaver and a deinterleaver.” Dr. Jacobsen does not explain which of her arguments in the cited section are applicable to this new combination. Nor does Dr. Jacobsen address the “ways of allocating memory between an interleaver and a deinterleaver” in G.993.1 in this or the cited section. I reserve the right to address any support or explanation Dr. Jacobsen’s attempts to provide for her currently conclusory assertions regarding this combination of references.

356. Nonetheless, looking back at the cited Section IX.C.6.c from the Jacobsen Report, Dr. Jacobsen describes the R-MSG2 and the O-MSG2 messages in paragraphs 447-448. As I explained in Section VI.F.1, *supra*, G.993.1’s exchange of interleaver and deinterleaver capabilities though those messages is redundant to Mazzoni’s stored predefined service data rates and interleaver/deinterleaver parameters and incompatible with Mazzoni at least because the exchange of maximum supported

interleaver and deinterleaver sizes per G.993.1 would specify a combined amount of interleaver and deinterleaver memory that would exceed Mazzoni's total memory size.

357. Further with respect to Mazzoni, looking back at what Dr. Jacobsen incorporates by reference, contrary to her opinion, Mazzoni does not disclose exchanging any messages at all that includes information about interleaving or deinterleaving parameters (or any other information upon which interleaver or deinterleaver memory allocations could be based). Dr. Jacobsen asserts that "[o]ne of ordinary skill in the art would have understood that this information, as well as capabilities of the transceiver at the other end of the system, would have to be conveyed, for example, in the form of a message during initialization, and that the memory would be allocated between the interleaving function and the deinterleaving function in accordance with that message." Jacobsen Report at ¶ 339. The "information" she is referring to is the parameters I , M , I' and M' . But, she cannot point to any disclosure of such a message in Mazzoni because there is no such disclosure. Instead, it seems that she is interpreting Mazzoni's description of the configurability of its interleaver means and deinterleaver means according to upstream and downstream bit rates as somehow disclosing reliance on an exchange of I , M , I' and M' . *See id.* (citing Mazzoni at 1:61-65 and 5:24-31). But parameters I , M , I' and M' are not exchanged in any message; rather, as discussed above in Section VI.B.1, *supra*, these parameters are stored in a table in each transceiver and indexed to a predefined service that includes predefined upstream and downstream bit rates. Mazzoni at 6:53-61. The parameter values for the particular predefined service are retrieved by the control means MCD at

the time the modem is installed (*id.*) and delivered by the MCD to the interleaver means MET and deinterleaver means MDET (*id.* at 5:21-23 and Fig. 3). This eliminates any need to exchange these parameters between modems.

358. One of the passages Dr. Jacobsen cites for this assertion (again in the section incorporated by reference), Mazzoni at column 5:24-31, does not describe some alternative embodiment where the I, M, I' and M' parameters are exchanged in messages. Rather, this passage simply describes the use of the predetermined parameters that are indexed to the predetermined service bit rates the transceiver has been configured to use. Dr. Jacobsen accurately admits this in her report when addressing the purported motivation to combine Mazzoni and G.993.1. *See, e.g.,* Jacobsen Report at ¶ 595 (“Mazzoni discloses keeping a table of values of the interleaver parameters, indexed by service identifiers, in the transceiver. *See id.* at col. 6:51-61. As a person having ordinary skill in the art as of the '473 patent's priority date would have understood, Mazzoni's table is limiting in that all of the services would have to be identified ahead of time and stored in the transceivers.”); *see also id.* at ¶ 626.

359. The other passage Dr. Jacobsen relies on for this assertion, Mazzoni at column 1:61-65, also does not disclose or require the exchange of any interleaver or deinterleaver parameters in a message. To the extent Dr. Jacobsen is interpreting this passage as disclosing anything other than the use of predetermined parameters that correspond to predetermined bit rates, she has misunderstood Mazzoni. In fact, the sentence after the one she quotes shows that the reference to “the bit rate actually processed by the send/receive device (modem)” is referring to one of the

predetermined bit rates for a predetermined service. Mazonni at 1:65 – 2:2 (“The invention therefore provides a device for sending/receiving digital data that is capable of *processing different bit rates from a group of predetermined bit rates* (e.g., all the symmetrical or asymmetrical services offered by the VDSL communication system).”). Therefore, Mazzoni does not, and need not, rely on any messages to carry out its suggested implementation. In fact, a POSITA would be discouraged to look to any references disclosing messages as described above.

360. Accordingly, the combination of G.993.1 and Mazzoni does not disclose “wherein the memory is allocated between the interleaving function and the deinterleaving function in accordance with a message received during an initialization of the transceiver” and, at least for this reason, claim 19 of the ‘473 patent is not obvious in view of LB-031 and Mazzoni.

- b. The combination of Mazzoni and G.993.1 does not disclose a multicarrier transceiver being associated with a memory wherein at least a portion of the memory may be allocated to the interleaving function or the deinterleaving function at any one particular time depending on the message.**

361. For the reasons discussed immediately above and in Sections VI.F.1 and VI.B.6.b, *supra*, Mazzoni does not disclose this claim element.

362. Dr. Jacobsen incorporates her arguments regarding Mazzoni from “Section (sic paragraph) 339.” Yet, this paragraph does not address what Dr. Jacobsen asserts it does. Nonetheless, Dr. Jacobsen’s arguments from this paragraph have been addressed in Section VI.B.6.a, *supra*. I also incorporate my arguments regarding Mazzoni from Section VI.B.6.b, *supra*. In summary, as I explained in the section

immediately above, Mazzoni does not disclose exchanging any messages at all that include information about interleaving or deinterleaving parameters (or any other information upon which interleaver or deinterleaver memory allocations could be based). Further, as I explained in the section immediately above and in Section VI.F.1, *supra*, G.993.1's exchange of interleaver and deinterleaver capabilities is redundant to and incompatible with Mazzoni.

363. With respect to G.993.1, Dr. Jacobsen cites to Section IX.C.6.f. Dr. Jacobsen's conclusion in paragraph 452 of that section of the Jacobsen Report states that "[o]ne of ordinary skill in the art would have understood that data would need to be interleaved and deinterleaved at the same time in this mode of transmission, which would require that a portion of the memory be allocated to an interleaving function, and a portion of the memory would be allocated to a deinterleaving function." This is incorrect. That an interleaver and deinterleaver operate at the same time does not disclose or require that a portion of the memory be allocated to the interleaver function or deinterleaver function at any one particular time depending on the message. Perhaps this was a cut and paste error and was intended for the element of claim 5 of the '381 patent, which recites: "wherein the shared memory allocated to the deinterleaver is used at the same time as the shared memory allocated to the interleaver."

364. For at least the foregoing reasons, the combination of Mazzoni and G.993.1 does not disclose "a multicarrier transceiver being associated with a memory wherein at least a portion of the memory may be allocated to the interleaving function or the

deinterleaving function at any one particular time depending on the message” and, at least for this reason, claim 19 of the ‘473 patent is not obvious in view of Mazzoni and G.993.1.

G. Claim 19 of the ‘473 Patent Is Not Obvious Over Voith and G.993.1, or, In the Alternative, In View of Voith, G.993.1 and Mazzoni

365. It is my opinion and conclusion that Voith alone or in combination with G.993.1 fails to disclose or suggest each element of claim 19 of the ‘473 patent, and hence fails to render claim 19 of the ‘473 patent obvious as described in detail, below.

366. It is also my opinion that regardless of the disclosures of Voith and G.993.1 individually, a person of ordinary skill in the art would not be motivated to combine the teachings of Voith with the teachings of G.993.1 at least for the reasons described in Section VI.F.3, *supra*.

1. Neither Voith nor G.993.1 discloses a multicarrier communications transceiver associated with a memory “wherein the memory is allocated between the interleaving function and the deinterleaving function in accordance with a message received during an initialization of the transceiver”

367. Voith does not disclose this limitation as discussed in section VI.E.1, *supra*.

368. Dr. Jacobsen refers to Section IX.C.6.e of the Jacobsen Report and contends that “G.993.1 teaches sending messages during initialization that indicate maximum interleaver delay, as well as ways of allocating memory between an interleaver and a deinterleaver.” Jacobsen Report at ¶ 611. As an initial matter, Dr. Jacobsen has provided no evidence for her assertion that the G.993.1 standard teaches “allocating memory between an interleaver and a deinterleaver” much less “allocating memory between an interleaver and a deinterleaver in accordance with a message received

during an initialization” based on a message received during initialization. Rather, a POSITA would understand G.993.1 to provide for dedicated downstream memories in each transceiver and separate, dedicated upstream memories in each transceiver. The use of such dedicated memories is consistent with other ADSL and G.Lite-compliant modems of that era and proposals for VDSL modems, including the LB-031 modem. See §§ IV and VI.A.5.a.ii, *supra*. As explained in these cited sections above, portions of dedicated interleaver memory that are not needed for interleaving cannot be allocated for use by the deinterleaver, and vice versa. Instead, those portions simply go unused. *Id.*

369. Assuming for the sake of argument that the G.993.1 message identified by Dr. Jacobsen indicates a “maximum interleaver delay,” nothing in the G.993.1 standard suggests “allocating memory between an interleaver and a deinterleaver in accordance,” with the “maximum interleaver delay.” Again, given the state of DSL transceivers during the relevant time frame and the maximum data rates specified by the G.993.1, there is no basis for assuming that DSL transceivers implementing G.993.1 would have used anything other than dedicated, separate interleaver and deinterleaver memories. A POSITA would have understood that the interleaver of a G.993.1-complaint transceiver may have used less than all of its dedicated interleaver memory based on the memory capabilities of the far-end transceiver’s deinterleaving function. However, the transceiver would not have been capable of reallocating the unused interleaver memory to its deinterleaver.

370. At least for these reasons, Voith and G.993.1 do not teach a transceiver “wherein the memory is allocated between the interleaving function and the deinterleaving function in accordance with a message received during an initialization of the transceiver.”

2. **Neither Voith nor G.993.1 discloses a multicarrier communications transceiver associated with a memory “wherein at least a portion of the memory may be allocated to the interleaving function or the deinterleaving function at any one particular time depending on the message”**

371. Voith does not disclose this limitation as discussed in section VI.E.2, *supra*.

372. With reference to G.993.1, for the same reasons set forth above at § VI.C.5.b, my opinion is that G.993.1 does not disclose this limitation. Additionally, as discussed in the section immediately above, there is no basis for assuming that DSL transceivers implementing G.993.1 would have used anything other than dedicated, separate interleaver and deinterleaver memories. Rather, a POSITA would have understood that the interleaver of a G.993.1-complaint transceiver may have used less than all of its dedicated interleaver memory but the transceiver would not have been capable of reallocating the unused interleaver memory to its deinterleaver. Thus, no portion of any memory could be allocated to an interleaving function at one time and to a deinterleaving function at another time.

373. At least for these reasons, Voith and G.993.1 do not teach a transceiver “wherein at least a portion of the memory may be allocated to the interleaving function or the deinterleaving function at any one particular time depending on the message.”

3. No Motivation to Combine Voith with G.993.1

374. For the following reasons, I disagree with Dr. Jacobsen's assertion at paragraphs 566-568 of the Jacobsen Report that "one of ordinary skill in the art would have been motivated to combine Voith and G.993.1."

375. First, Dr. Jacobsen asserts that that there is a motivation to combine because both references are in the DSL field. *See* Jacobsen Report at ¶ 617. This in and of itself, or in combination with any other argument made by Dr. Jacobsen in Section IX.G.3 of the Jacobsen Report, is not sufficient to show that a person of ordinary skill in the art would have combined the teachings of the two references. At the time of the invention of the Family 3 Patents, the DSL standards have been under continuous development and there were likely hundreds, if not thousands, of references directed to possible implementation details of many and varied proposals for DSL transceivers. One of skill in the art at the time would have understood that many of these references would be completely incompatible with one another and/or, if combined, would provide no useful benefit. Thus, that Voith and G.993.1 are purportedly both directed to different proposals for DSL transceivers, would not have made their combination obvious.

376. Dr. Jacobsen further asserts that there is a motivation to combine because each of the references purportedly "discloses a need to allocate memory for interleaving and deinterleaving." *Id.* at ¶ 617. This in and of itself, or in combination with any other argument made by Dr. Jacobsen in Section IX.G.3 of the Jacobsen Report, is not sufficient to motivate a person of ordinary skill in the art to combine the teaching of the

two references. It is far too general of a concept to provide any motivation to combine one reference with the other. In fact, it is not materially different than saying that Voith and G.993.1 contemplate the use of memories for interleaving and deinterleaving.

377. I also disagree with Dr. Jacobsen's assertion that there is a motivation to combine Voith and G.993.1 because they purportedly both relate to "allocating memory for interleaving and deinterleaving to support various applications." Jacobsen Report at ¶ 618.

378. With reference to Voith, Dr. Jacobsen asserts that Voith's recognition that "ADSL transceiver 34 requires a large amount of memory, which is preferably implemented off-chip in external interleave/de-interleave memory 66" somehow means that Voith "discloses a need to allocate memory for interleaving and deinterleaving." Jacobsen Report at ¶ 617. I disagree with this assertion. Voith merely teaches that it is preferable to implement the memory buffers off-chip, because "large buffers consume a large integrated circuit area which adds to cost." Voith at 2:27-28. Thus, Voith's fundamental premise is to concede that the memory buffers are required to be large but Voith makes no proposal for reducing such requirement. Voith certainly does not propose the use of sharing memory for interleaving and deinterleaving where a portion of the memory can be used at one time for interleaving and at another time for deinterleaving as explained immediately above sections VI.E.1 and 2.

379. With reference to the G.993.1 standard, Dr. Jacobsen asserts that "[o]ne of ordinary skill in the art would therefore have recognized that the teachings of G.993.1 show a reliable and efficient way of enabling the transceivers of Voith to partition the

shared memory between the interleaver and deinterleaver.” Jacobsen Report at ¶ 619. I disagree, there is no disclosure or suggestion in G.993.1 of using or partitioning shared memory. Dr. Jacobsen does not cite any portion of G.993.1 as purportedly disclosing this. On the contrary, a POSITA would understand G.993.1 to provide for dedicated downstream memories in each transceiver and separate, dedicated upstream memories in each transceiver. The use of such dedicated memories is consistent with other DSL modems of that era and proposals for VDSL modems, including the LB-031 modem. *See* §§ IV and VI.A.5.a.ii, *supra*. As explained in these cited sections above, portions of dedicated interleaver memory that are not needed for interleaving cannot be allocated for use by the deinterleaver, and vice versa. Instead, those portions simply go unused. *Id.*

380. Therefore, it is my opinion that a POSITA would not have been motivated to combine Voith and G.993.1 in the manner proposed by Dr. Jacobsen, and Dr. Jacobsen has not shown otherwise.

4. Mazzoni does not Supply the Disclosure Missing from G.993.1 and Voith

381. Dr. Jacobsen contends that “Mazzoni discloses that at least a portion of the memory may be allocated to the interleaving function or the deinterleaving function at any one particular time depending on the message.” Jacobsen Report at ¶ 623. Contrary to Dr. Jacobsen’s opinion, Mazzoni does not disclose exchanging any messages at all that include information about interleaving or deinterleaving parameters (or any other information upon which interleaver or deinterleaver memory

allocations could be based). I incorporate by reference my opinions set forth at §§ VI.B.6.a and VI.B.6.b for why Mazzoni does not disclose this element of the claim.

5. A POSITA would not be Motivated to Combine Mazzoni with Voith and G.993.1

382. Contrary to Dr. Jacobsen's assertion, a POSITA would not be motivated to combine Mazzoni with Voith and G.993.1. First, Dr. Jacobsen asserts that there is a motivation to combine because these references are "in the DSL field." Jacobsen Report at ¶ 625. This in and of itself, or in combination with any other argument made by Dr. Jacobsen in Section IX.G.5 of the Jacobsen Report, is not sufficient to show that a person of ordinary skill in the art would have combined the teachings of the three references. At the time of the invention of the Family 3 Patents, the DSL standards have been under continuous development and there were likely hundreds, if not thousands, of references directed to possible implementation details of many and varied proposals for DSL transceivers. One of skill in the art at the time would have understood that many of these references would be completely incompatible with one another and/or, if combined, would provide no useful benefit. Thus, that Mazzoni, Voith and G.993.1 are purportedly both directed to different proposals for DSL transceivers, would not have made their combination obvious.

383. Dr. Jacobsen also contends that "[l]ike Voith and G.993.1, Mazzoni describes a need to allocate memory for interleaving and deinterleaving." See Jacobsen Report at ¶ 625. This in and of itself, or in combination with any other argument made by Dr. Jacobsen in Section IX.G.5 of the Jacobsen Report, is again not sufficient to

motivate a person of ordinary skill in the art to combine the teaching of the three references. It is far too general of a concept to provide any motivation to combine one reference with the other. In fact, it is not materially different than saying that Mazzoni, Voith and G.993.1 contemplate the use of memories for interleaving and deinterleaving.

384. I also disagree with Dr. Jacobsen assertion that “Voith discloses that efficiency in the use of memory is desirable.” On this point, I disagree with Dr. Jacobsen for the reasons set forth at ¶ 379 *supra*.

385. With reference to the G.993.1 standard, Dr. Jacobsen asserts that “G.993.1 discloses how memory is allocated in accordance with a message received during initialization” and that “[o]ne of ordinary skill in the art would therefore have recognized that the teachings of G.993.1 show a reliable and efficient way of enabling the transceivers of Mazzoni to partition the shared memory between the interleaver and deinterleaver without requiring all of the possible services to be defined in advance to create the table disclosed in Mazzoni.” Jacobsen Report at ¶ 627. I disagree, there is no disclosure or suggestion in G.993.1 of using or partitioning shared memory. Dr. Jacobsen does not cite any portion of G.993.1 as purportedly disclosing this. On the contrary, a POSITA would understand G.993.1 to provide for dedicated downstream memories in each transceiver and separate, dedicated upstream memories in each transceiver. The use of such dedicated memories is consistent with other DSL modems of that era and proposals for VDSL modems, including the LB-031 modem. *See* §§ IV and VI.A.5.a.ii, *supra*. As explained in these cited sections above, portions of dedicated

interleaver memory that are not needed for interleaving cannot be allocated for use by the deinterleaver, and vice versa. Instead, those portions simply go unused. *Id.*

386. Further, a POSITA would not look to add messages (from G.993.1 or otherwise) to the system disclosed in Mazzoni, and in fact doing so would provide no useful benefit. It would certainly not be any more reliable and efficient than Mazzoni's existing scheme. This is because the system disclosed in Mazzoni relies on the use of a pre-populated table of I, M, I', and M' parameter values, where each set of values corresponds to a respective one of a number of predetermined data rate service pairs. See Mazzoni at 5:22-23, 5:27-30, 6:51-55. There is no use for a message that specifies the interleaver or deinterleaver memory sizes because all data rate pairs and their corresponding I, M, I', and M' values that need to be supported are accounted for. Mazzoni contemplates TO and TU transceiver pairs that will both be efficiently and reliably preconfigured at the time of installation with the same predetermined parameters selected from a limited number of possibilities. Thus, exchanging messages describing the capabilities of the transceivers would be redundant, serve no useful purpose, and make the system less reliable and efficient.

387. Therefore, it is my opinion that a POSITA would not have been motivated to combine Mazzoni with Voith and G.993.1 in the manner proposed by Dr. Jacobsen, and Dr. Jacobsen has not shown otherwise.

VII. CONCLUSION

388. For the foregoing reasons, it is my opinion that the Asserted Claims of the Family 3 Patents are valid and are neither anticipated nor obvious in view of the prior art and the knowledge of a person of ordinary skill in the art.