IN THE UNITED STATES DISTRICT COURT
FOR THE DISTRICT OF DELAWARE

TQ DELTA, LLC, Plaintiff, v. 2WIRE, INC. Defendant.	Civil Action No. 13-cv-1835-RGA

REPLY EXPERT REPORT OF DR. KRISTA S. JACOBSEN FOR FAMILY 3 PATENTS

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I. INTRODUCTION

1. My name is Dr. Krista S. Jacobsen. I provide this report in reply to the Corrected Rebuttal Expert Report of Dr. Todor Cooklev Regarding Validity of the Family 3 Patents ("Cooklev Report"), served originally on December 28, 2018, with the corrected version served on January 4, 2019. The Cooklev Report was submitted in response to my Opening Expert Report for Family 3 Patents (my "Opening Report" or "Jacobsen Opening Report") in the above-captioned action.

2. Between now and any time that I may be asked to testify at trial, I expect to continue my review, evaluation, and analysis of information generated during discovery, as well as evidence that either side presents before or at trial. I further reserve the right to amend or supplement this report, as appropriate, after considering opinions set forth in Plaintiff's expert reports, and/or if additional relevant information becomes available to me. I reserve the right to supplement this report as necessary.

3. That I do not specifically disagree with a portion of Dr. Cooklev's report does not mean that I agree with that portion.

II. APPLICABLE LEGAL PRINCIPLES

4. I have reviewed Dr. Cooklev's summary of the applicable legal principles.

5. At paragraph 25, Dr. Cooklev asserts that "there must be some teaching or suggestion in the references to support their use in the particular claimed combination." This statement does not comport with my understanding of the law on the use of combinations of references to show that a claimed invention would have been obvious to a person having ordinary skill in the art. I set forth my understanding in paragraph 21 of my Opening Report, which stated (emphasis added):

> I am informed and understand that an obviousness evaluation can be made using either a single reference or a combination of several prior art references. An obviousness analysis involving two or more references generally requires a reason why a person having ordinary skill in the relevant field would have combined aspects of those references in the way the asserted patent claims do. I understand that *the prior art references themselves may provide a suggestion, motivation, or reason to combine, but other times the link may simply be common sense. An obviousness analysis can recognize that market demand, rather than scientific literature, often drives innovation, and that is sufficient motivation to combine references*.

Thus, I disagree with Dr. Cooklev's statement that "there must be some teaching or suggestion in the references to support their use in the particular claimed combination." Cooklev Report at ¶ 25. It is my understanding that a teaching or suggestion in the references is only one potential source of the motivation to combine references.

6. Dr. Cooklev states that he is "informed that a reference patent is entitled to claim the benefit of the filing date of its provisional application if the disclosure of the provisional application provides support for the claims in the reference patent." Cooklev Report at ¶ 39. It is my understanding that there are other conditions (e.g., common inventorship) required for a later-filed application to claim the benefit of an earlier-filed provisional application.

III. LEVEL OF SKILL IN THE ART

7. I incorporate by reference the reference the Level of Skill in the Art section from my Rebuttal Expert Report of Dr. Krista S. Jacobsen for Family 3 Patents (my "Rebuttal Report" or "Jacobsen Rebuttal Report") (*see* Section VI, ¶¶ 15-19), which includes my response to Dr. Cooklev's characterization of the level of skill in the art.

IV. BACKGROUND OF THE TECHNOLOGY

8. I incorporate by reference the Background of the Technology section from my Rebuttal Report (*see* Section VII, ¶¶ 20-44), which includes my response to Dr. Cooklev's characterization of the background of the technology.

9. Dr. Cooklev states, incorrectly, that "DSL systems, such as, for example, ADSL2/2+ standards known at the time of the inventions, specify dedicated interleaving memory requirements in each transceiver separately for upstream and downstream transmission (i.e., in each direction separately)." Cooklev Report at ¶ 42. I disagree. First, none of the ADSL2/2+ standards specifies the use of dedicated memory for interleaving or deinterleaving. In fact, the versions of ADSL2/2+ in existence as of the priority date of the Family 3 patents[1] do not even use the word "memory." *See, e.g.*, G.992.3 (07/2002); G.992.3 (01/2005); G.992.5 (05/2003); G.992.5 (01/2005). The ADSL2/2+ standards do not specify or require any particular memory configuration for interleaving or deinterleaving, much less "dedicated interleaving memory requirements."

10. Second, the ADSL2/2+ standards specify interleaving ***delay*** requirements, ***not memory*** requirements. *See, e.g.*, G.992.3 (07/2002) at § 7.7.1.5 ("Each of the $N_{FEC.p}$ octets B_0, B_1, … , $B_{NFEC.(p-1)}$ in an FEC Output Data Frame is delayed by an amount that varies linearly with the octet index. More precisely, octet B_i (with index i) is delayed by $(D_p - 1) \times i$ octets, where D_p is the interleaver depth."); G.992.3 (01/2005) at § 7.7.1.5 (same).

11. For at least these reasons, I disagree with Dr. Cooklev's statement that "an ADSL2/2+ ATU-C is required to have a specified amount of dedicated interleaving memory for

[1] I explained in my Opening Report why, in my opinion, the asserted claims of the Family 3 patents are not entitled to the benefit of the '269 provisional application filed on October 12, 2004, and that the priority date is the filing date of the '890 patent, October 11, 2005. My opinions, however, are the same regardless of whether the filing date is October 12, 2004 or October 11, 2005.

downstream data transmission and separately and independently have a specified amount of dedicated interleaving memory for upstream data reception." Cooklev Report at ¶ 42. Although, as I explained in my Rebuttal Report, an interleaving delay requirement establishes a minimum amount of memory required in each of the transmitter and receiver to meet that delay, ADSL2/2+ does not require the use of dedicated interleaving memory and dedicated deinterleaving memory. Therefore, I also disagree with Dr. Cooklev's statements in paragraph 42 that "the ATU-C must have . . . 16,320 octets of dedicated interleaving memory for downstream . . . [and] 2,048 octets of dedicated deinterleaving memory for upstream."

12. For the same reasons, I disagree with Dr. Cooklev's statement that "an ADSL2/2+ ATU-R is required to have a specific amount of dedicated interleaving memory for downstream data reception and separately have a specific amount of dedicated interleaving memory for upstream data transmission." Cooklev Report at ¶ 43. And I also disagree that "the ATU-R must have . . . 16,320 octets of dedicated deinterleaving memory for downstream . . . [and] 2,048 octets of dedicated interleaving memory [for interleaving]." *Id.* As I stated above, the ATU-R must have memory for interleaving and deinterleaving, but the standards do not require dedicated memory.

13. Without any support, Dr. Cooklev contends that "[t]he ADSL2/2+ standards do not specify or enable memory sharing between the interleaver and the deinterleaver in a single transceiver." Cooklev Report at ¶ 44. Although the ADSL2/2+ standards do not require memory sharing, I disagree with the implication that they specify the use of dedicated memory. As I explained above, the standards do not specify any particular memory implementation. Furthermore, I disagree with Dr. Cooklev's assertion that the ADSL2/2+ standards do not "enable memory sharing between the interleaver and the deinterleaver in a single transceiver."

Whether a transceiver uses shared memory is an implementation choice, and nothing in ADSL2/2+ would prohibit a transceiver from using shared memory for interleaving and deinterleaving.

14. I also disagree with Dr. Cooklev's statement that "ADSL2/2+ specify that the ATU-C downstream interleaver and the ATU-R downstream deinterleaver have the same amount of memory (i.e., ~16K octets) . . . [and] the ATU-R upstream interleaver and the ATU-C upstream deinterleaver have the same amount of memory (i.e. ~2K octets)." Cooklev Report at ¶ 44. As I explained above, ADSL2/2+ do not specify amounts of memory; they specify interleaving delay. As I explained in my Rebuttal Report (*see, e.g.* Jacobsen Rebuttal Report at § IX), the amount of memory an implementation uses to meet a specified interleaving delay (whether performing the interleaving operation or the deinterleaving operation) can be any amount greater than or equal to $(D - 1)\times(I - 1)/2$, where D is interleaver depth and I is interleaver block size.

15. I also disagree with Dr. Cooklev's assertion that "[p]rior to the inventions disclosed in the Family 3 patents, an amount of memory available to an interleaver was predetermined and an amount of memory available to a deinterleaver was predetermined." Cooklev Report at ¶ 45. As I have explained, the ADSL2/2+ standards do not specify the amounts of memory available to an interleaver or a deinterleaver.

16. Dr. Cooklev concludes his discussion of "Interleaver Memory and Deinterleaver Memory in Prior Art Systems" with the assertion that prior-art systems "were incapable of sharing memory between an interleaving and deinterleaving function based on a message." Cooklev Report at ¶ 45. Dr. Cooklev has provided no support for this assertion and does not purport to have determined how prior-art transceivers, or even just prior-art ADSL2/2+

transceivers, implemented interleaving and deinterleaving, whether by using messages or through some other means. His conclusion that prior-art systems "were incapable of sharing memory between an interleaving and deinterleaving function based on a message" is unsupported and, in my opinion, amounts to pure speculation.

17. In paragraphs 46 through 57, Dr. Cooklev continues to speculate as to how existing transceivers provided interleaving and deinterleaving functions as of the priority date of the Family 3 patents. Specifically, he purports to compare how "the interleaver memory and the deinterleaver memory in a single transceiver had been implemented in prior art systems before the inventions of the Family 3 patents . . . with how the shared memory can be allocated to an interleaver and a deinterleaver according to the inventions of the Family 3 patents." Cooklev Report at ¶ 46. Again, Dr. Cooklev provides no support for his statements regarding how prior-art transceivers implemented interleaving and deinterleaving. For example, despite having worked for Aware from 2000 to 2002, Dr. Cooklev has not even stated whether Aware's transceivers[2] operated as he contends, *i.e.*, using dedicated interleaving memory and dedicated deinterleaving memory. Furthermore, he has not represented that he has determined how other existing prior-art transceivers, whether for DSL or other applications, provided memory for interleaving and deinterleaving, much less that they did not use shared memory. In my opinion, there is no basis whatsoever for Dr. Cooklev's conclusion that prior-art transceivers did not use shared memory for interleaving and deinterleaving. Indeed, several of the prior-art references I applied in my Opening Report and discuss further below suggest just the opposite.

[2] As of 2001, Aware offered for sale at least one transceiver, the AW-918 ADSL Transceiver Module. *See, e.g.*, https://web.archive.org/web/20010218175422/http://www.aware.com:80/products/Hardware/modules.html (last visited January 6, 2019).

18. Dr. Cooklev's examples at paragraphs 47-57 find no support in the Family 3 patents or their file histories. Moreover, through this example, Dr. Cooklev appears to suggest that the use of shared memory for interleaving and deinterleaving was introduced by the Family 3 patents. It was not. As I explained in my Rebuttal Report (*see, e.g.*, § VII.D), the Family 3 patents did not introduce the idea of sharing memory between an interleaver and deinterleaver, either generally or for DSL transceivers in particular. Multiple prior-art references (e.g., Fadavi-Ardekani, Mazzoni, Voith, etc.) described the use of shared memory for interleaving and deinterleaving in DSL transceivers. The Family 3 Patents describe specific ways of allocating shared memory using information contained in an initialization message that specifies a maximum amount of memory available to be allocated to an interleaver or deinterleaver; they do not claim merely sharing memory between an interleaver and a deinterleaver. Indeed, the examiners of various Family 3 patents' applications specifically noted that sharing memory between and interleaver and deinterleaver was known in the prior art. *See, e.g.*, 10/06/2010 Notice of Allowance and Fees Due from '882 patent's file history (TQD004331) ("The closest prior art, Fadavi-Ardekani et al (U.S. Pat. No. 6,707,822) discloses sharing a memory between the interleavers and deinterleavers of multiple ADSL sessions. . . ."). Therefore, to the extent Dr. Cooklev's examples at paragraphs 47-57 suggest that there is some benefit to using shared memory for interleaving and deinterleaving, that benefit is not due to any contribution of the Family 3 patents.

19. Dr. Cooklev mischaracterizes my opinion in paragraph 58 of his report. Specifically, Dr. Cooklev states that "Dr. Jacobsen asserts that prior art systems were capable of providing 'shared memory that the transceiver can partition between its interleaver and deinterleaver on a per-connection basis.'" Cooklev Report at ¶ 58. He then proceeds to

summarize or quote selected portions of the prior-art references I applied in my Opening Report and concludes that none of them discloses "shared memory that can be partitioned between its interleaver and deinterleaver on a per-connection basis." *See, e.g.*, Cooklev Report at ¶¶ 60, 61, 62, 63, 64. As an initial matter, "shared memory that can be partitioned between its interleaver and deinterleaver on a per-connection basis" is not a limitation of any asserted Family 3 claim, nor is it required by the Court's claim construction. According to the Court's claim construction, "shared memory" is merely "common memory used by at least two functions, where a portion of the memory can be used by either one of the functions." The Court's construction does not require partitioning at all, much less between an interleaving function and a deinterleaving function on a per-connection basis. Indeed, the Court's construction does not even mention interleaving/interleavers or deinterleaving/deinterleavers.

20. In addition, I did not assert that each of the prior-art references discloses "shared memory that can be partitioned between its interleaver and deinterleaver on a per-connection basis." In fact, my Opening Report states, in the discussion of the technology background:

> There are two ways to provide the memory needed for a transceiver's interleaving and deinterleaving procedures. The first way is to provide a specified amount of dedicated interleaver memory and a specified amount of dedicated deinterleaver memory. The transmitter has exclusive access to the interleaver memory and can, at least in theory, use as much as all of the interleaver memory for interleaving. Similarly, the receiver has exclusive access to the deinterleaver memory and can, at least in theory, use as much as all of the deinterleaver memory for deinterleaving.
>
> The second way to meet the transceiver's memory requirements for interleaving and deinterleaving is to provide shared memory that the transceiver can partition between its interleaver and deinterleaver on a per-connection basis. Use of a shared memory for interleaving and deinterleaving, including in DSL, was well known before the priority date of the Family 3 patents.

Jacobsen Opening Report at ¶¶ 71-72 (emphasis added).

Thus, I stated, correctly, that the use of shared memory, as construed by the Court, for interleaving and deinterleaving was well known before the priority date of the Family 3 patents.

21. Furthermore, to the extent Dr. Cooklev characterizes the disclosures of the prior-art references in this discussion, those characterizations are incorrect or misleading. For example, Dr. Cooklev contends that Berkmann does not disclose "shared memory" because "it is not being partitioned ***between*** the interleaving function and the deinterleaving function, and it is not being partitioned on a ***per-connection*** basis." Cooklev Report at ¶ 60 (emphasis in original). Again, Dr. Cooklev's focus on partitioning between an interleaving function and a deinterleaving function, and partitioning on a per-connection basis, is misplaced. The Court's construction does not require memory to be partitioned between an interleaver and deinterleaver on a per-connection basis. In my Opening Report, I referred to certain prior art references as having the ability partition memory between an interleaver and a deinterleaver on a per connection basis for convenience. It is not my opinion that this ability is required to meet the claim limitations.

22. With respect to the disclosures of Kang, Dr. Cooklev merely provides his conclusion that "Kang does not disclose providing 'shared memory that can be partitioned between its interleaver and deinterleaver on a per-connection basis,' as Dr. Jacobsen asserts." Cooklev Report at ¶ 62. He does not elaborate on how he reached that conclusion.

23. Dr. Cooklev argues, incorrectly, that Fadavi-Ardekani "teaches using dedicated memories for the interleaving function and deinterleaving function." Cooklev Report at ¶ 61. I discussed the disclosures of Fadavi-Ardekani in my Opening Report and explained that Fadavi-Ardekani discloses "shared memory" as construed by the Court—namely, the Interleaver/De-Interleaver Memory (IDIM). *See, e.g.*, Jacobsen Opening Report at ¶¶ 357-62, 369-72.

24. Dr. Cooklev does not argue that Mazzoni does not disclose shared memory as construed by the Court; his argument is that, according to him, Mazzoni does not disclose "shared memory that can be partitioned between its interleaver and deinterleaver on a per-connection basis." Cooklev Report at ¶ 63. As I explained above, Dr. Cooklev's focus on this phrase is misplaced.

25. With respect to Voith, Dr. Cooklev argues that "Voith does not teach that the external memory is 'shared memory.'" Cooklev Report at ¶ 64. On the contrary, and as I explained in my Opening Report, Voith discloses "common memory used by at least two functions, where a portion of the memory can be used by either one of the functions" as the Court's construction requires. Specifically, I opined that Voith discloses "allocating memory between the interleaving function and the deinterleaving function" and that "a portion of the memory may be allocated to the interleaving function or the deinterleaving function at any one particular time." *See, e.g.*, Jacobsen Opening Report at ¶¶ 533-39, 557, 562-63.

26. Thus, I disagree with Dr. Cooklev's assertions, in paragraphs 60-64, that the prior-art references do not disclose "shared memory" as construed by the Court.

V. THE FAMILY 3 PATENTS

27. I incorporate by reference the Family 3 Patents section from my Rebuttal Report (*see* Section VIII, ¶¶ 45-50), which includes my response to Dr. Cooklev's characterization of the Family 3 Patents.

VI. INVALIDITY UNDER 35 U.S.C. § 112

28. Having considered Dr. Cooklev's arguments to the contrary, it remains my opinion that claim 19 of the '473 patent is indefinite and fails to meet the written description and/or enablement requirements of 35 U.S.C. § 112. In addition, it remains my opinion that the

Certificates of Correction for the '381 patent and the '882 patent were improperly obtained at least because they changed the scope of the issued claims.

A. Claim 19 of the '473 Patent Is Indefinite Under 35 U.S.C. § 112, Paragraph 2.

29. In attempting to rebut my argument that claim 19 of the '473 patent is indefinite under 35 U.S.C. § 112, paragraph 2, Dr. Cooklev asserts, incorrectly, that I ignored "context" provided by the Court in opining that the term "wherein at least a portion of the memory may be allocated to the interleaving function or the deinterleaving function at any one particular time depending on the message" is indefinite. Cooklev Report at ¶ 70. Dr. Cooklev quotes the Court's statements:

> The claim language does not require that the message specify amounts of memory. The disputed term's language requires that the amount of memory depend on the message's contents, but it does not require that the message's contents themselves actually specify amounts of memory.

Cooklev Report at ¶ 70 (quoting Claim Construction Memorandum for Family 3 Patents (Dec. 18, 2017)). Dr. Cooklev has not explained how the Court's statements, which address whether the message's contents must specify amounts of memory, have any bearing on whether the language "a portion of the memory *may be* allocated" renders the claim indefinite, as I argued. In my opinion, these statements are not inconsistent with, nor are they germane to, my opinion that claim 19 is indefinite.

30. Dr. Cooklev then complains that I did not explain how the claims, specification, and file history support my argument that claim 19 is indefinite. Cooklev Report at ¶ 72. My argument, however, is that that there is a *lack* of disclosure in the patent and its file history: it is not clear to a skilled artisan, when reading the claims, specification, and file history, whether the memory actually has to be allocated in more than one way in accordance with a message.

31. As I explained in my Opening Report, from the '473 patent's disclosure, one of ordinary skill in the art would have understood that, within the shared memory, a particular memory space may be allocated to the interleaver or the deinterleaver depending on the current demands of the system, and in turn, a message. Jacobsen Opening Report at ¶ 152. As I also explained, however, it is not clear from the intrinsic record whether this allocation actually has to happen, at some point, in order for a device to infringe. *Id.* For example, a system could use a shared memory in such a way that it is theoretically possible that a portion of the memory is allocated to a deinterleaver or an interleaver, depending on the message, but it might not actually ever happen in practice. *Id.* The support for my argument is the lack of disclosure of the '473 patent itself.

32. Dr. Cooklev suggests that I do not understand "the scope of an apparatus claim that defines structure in functional terms." Cooklev Report at ¶ 73. But even if it is proper for an apparatus claim to "define[] structure in functional terms," that is not, in my opinion, what a skilled artisan would understand claim 19 to do. As I explained in my Opening Report, claim 19 recites that "the memory *may be allocated* to the interleaving function or the deinterleaving function at any one particular time depending on the message," and a skilled artisan would not understand whether this allocation actually has to occur for the claim to be infringed. *See* Jacobsen Opening Report at ¶ 152.

33. Tacitly recognizing that the language "may be allocated" is problematic, Dr. Cooklev argues that "the claim is infringed by transceivers that are capable of allocating at least a portion of the memory to the interleaving function or the deinterleaving function at any one particular time depending on the message," (Cooklev Report at ¶ 73), but claim 19 does not recite that the transceiver is *capable of* allocating; it recites that "at least a portion of the

memory *may be allocated* to the interleaving function or the deinterleaving function," thus suggesting that allocation in accordance with a message is optional. In contrast, the claim recites that the transceiver is "configured to . . . perform an interleaving function . . . and perform a deinterleaving function. . . ," but not that it is "configured to allocate at least a portion of the memory to the interleaving function or the deinterleaving function at any one particular time depending on the message" or "capable of allocating at least a portion of the memory to the interleaving function or the deinterleaving function at any one particular time depending on the message." Thus, I disagree with Dr. Cooklev's assertion that "this claim language, as even the Court agreed, requires only that the function to which the portion of memory is allocated at one particular time depends on the message's contents." Cooklev Report at ¶ 74. As I understand the Court's claim construction order, the Court did not agree with Dr. Cooklev's statement, nor does the Court's claim construction memorandum provide support for Dr. Cooklev's argument.

34. Dr. Cooklev opines that "'may' is the most appropriate term given that the claim provides two possibilities on its face – that, depending on the message, (1) the portion of memory be allocated to the interleaver function at a particular time, or (2) the portion of memory be allocated to the deinterleaver function at a particular time." Cooklev Report at ¶ 74. But that is not what "may be allocated" means. As a skilled artisan would have understood, the word "may" indicates that the memory need not be allocated at all. In other words, the plain language of claim 19 is that the allocation of the memory is optional. Dr. Cooklev frames his argument in terms of a transceiver that is "capable of" allocating, (Cooklev Report at ¶ 74), but, as I explained above, claim 19 does not recite that the transceiver is "capable of" allocating. It recites that "a portion of the memory *may be* allocated."

35. Thus, having considered Dr. Cooklev's arguments to the contrary, it remains my opinion that claim 19 of the '473 patent is invalid as indefinite under 35 U.S.C. § 112, paragraph 2.

B. The Asserted Claims Fail To Meet the Enablement and/or Written Description Requirements of 35 U.S.C. § 112, Paragraph 1.

36. In paragraph 79, purporting to rebut my argument that "wherein the shared memory allocated to the [interleaver / deinterleaver] is used at the same time as the shared memory allocated to the [deinterleaver / interleaver]" (i.e., the last limitation of claim 1 of the '048 patent, claim 5 of the '381 patent, and claim 13 of the '882 patent) is not enabled and/or lacks written description, Dr. Cooklev concedes that "[t]he simultaneous use of memory by multiple functions was a well-known process at the time of the inventions." Cooklev Report at ¶ 79. *See also id.* ("A POSITA at that time would know how two or more functions can simultaneously use the same memory by storing information for a first function at the same time that information for a second function is stored in the memory, or written to the memory, or read from the memory. This is inherent in any multi-threaded operation that uses the same memory.").

37. Dr. Cooklev also contends that "simultaneous transmitting/encoding and decoding/receiving of the latency paths" amounts to "the shared memory allocated to the [deinterleaver / interleaver] is used at the same time as the shared memory allocated to the [interleaver / deinterleaver]." Cooklev Report at ¶ 81. Yet, as I explain below, when he addresses the disclosures of the prior-art references I applied in my Opening Report, Dr. Cooklev argues that these same types of disclosures are insufficient to meet the last limitation of claim 1 of the '048 patent, claim 5 of the '381 patent, and claim 13 of the '882 patent.

38. Finally, Dr. Cooklev argues that I did not explain why, in my opinion, the Family 3 patents fail to meet the written description requirement for the last limitation of claim 19 of the '473 patent, "wherein at least a portion of the memory may be allocated to the interleaving function or the deinterleaving function at any one particular time depending on the message." Cooklev Report at ¶ 82. On the contrary, I stated:

> One of ordinary skill in the art would not have understood the patentee to have been in possession of an apparatus wherein at least a portion of the memory may be allocated to a first interleaving function or a second interleaving function at any one particular time depending on the message. The specification describes ways of allocating shared memory between an interleaving function and a deinterleaving function, but it does not describe to one of ordinary skill in the art how at least a particular portion of the memory can be allocated to one function, and then be allocated to the other function at any one particular time.

Jacobsen Opening Report at ¶ 156.

Thus, I did explain why the Family 3 patents fail to meet the written description requirement for "wherein at least a portion of the memory may be allocated to the interleaving function or the deinterleaving function at any one particular time depending on the message."

39. With respect to this limitation, Dr. Cooklev argues that "disclosure . . . is found generally because the specification discloses the use of 'shared memory' by an interleaver and a deinterleaver." Cooklev Report at ¶ 82. He argues that "[a] POSITA would understand from the disclosure of shared memory that is allocated to an interleaver would not be used at the same time by a deinterleaver but, instead, could be used at alternative times depending on the allocation in effect at the time." Cooklev Report at ¶ 82. Thus, Dr. Cooklev contends that the mere disclosure of shared memory by an interleaver and a deinterleaver discloses "wherein at least a portion of the memory may be allocated to the interleaving function or the deinterleaving function at any one particular time depending on the message." Yet, as I explain below, when

he addresses the disclosures of the prior-art references I applied in my Opening Report, Dr. Cooklev argues that the disclosure of "shared memory" is insufficient to meet the last limitation of claim 19 of the '473 patent.

40. Having considered Dr. Cooklev's arguments to the contrary, it remains my opinion that all of the asserted claims are invalid under 35 U.S.C. § 112, paragraph 1 for failing to meet the written description and/or enablement requirements.

C. The Certificates of Correction In the '381 and '882 Patents Were Improperly Obtained Because They Changed the Scope and Meaning of the Issued Claims.

41. Although Dr. Cooklev purports to disagree that the Certificates of Correction in the '381 patent and the '882 patent changed the scope of the issued claims, (Cooklev Report at ¶ 85), his argument focuses exclusively on whether the errors were "clerical or typographical." Cooklev Report at ¶¶ 86-89. Dr. Cooklev does not actually dispute that the Certificates of Correction changed the scope of the issued claims. *See id.*

42. Dr. Cooklev states that I suggested "that the statement in the specification that 'the invention can be applied to any transceiver having any number of latency paths' somehow precludes the correction." *Id.* at ¶ 87. On the contrary, I identified this statement as evidence that a skilled artisan would not have considered the issued claims to be in error. As I explained, the Family 3 patents state that "it should be appreciated that this invention can be applied to any transceiver having any number of latency paths," which a person having ordinary skill would have understood to include transceivers that allocate "a first number of bytes of the shared memory to the deinterleaver to deinterleave a first plurality of Reed Solomon (RS) coded data bytes for transmission at a first data rate" (as recited in the issued claims) and "a second number of bytes of the shared memory to an interleaver to interleave a second plurality of RS coded

data bytes received at a second data rate" (as recited in the issued claims). Jacobsen Opening Report at ¶ 159.

43. Dr. Cooklev does not rebut my argument that a skilled artisan "would have understood transmission and reception to be different, and that requiring transmission instead of reception, or vice versa, changes the required functionalities of the claimed transceivers." Jacobsen Opening Report at ¶ 160; Cooklev Report at ¶¶ 85-89. Dr. Cooklev also does not dispute that "[a] skilled artisan would also have understood that a transceiver that did not infringe claim 5 of the '381 patent or claim 13 of the '882 patent as issued could infringe claim 5 of the '381 patent and claim 13 of the '882 patent as modified by the Certificates of Correction." *Id.*

44. Thus, having considered Dr. Cooklev's rebuttal, it remains my opinion that the Certificates of Correction were improperly obtained.

VII. ANALYSIS OF THE PRIOR ART

45. Having considered Dr. Cooklev's arguments to the contrary, it remains my opinion that each of the asserted claims of the Family 3 patents is rendered obvious by some or all of the following combinations:

- LB-031 in combination with the knowledge of a skilled artisan at the time of the alleged invention;
- LB-031 in combination with Mazzoni;
- Fadavi-Ardekani in combination with G.993.1;
- Fadavi-Ardekani in combination with G.992.2;
- Voith in combination with LB-031;
- Mazzoni in combination with G.993.1;
- Voith in combination with G.993.1; and/or
- Voith in combination with G.993.1 and Mazzoni.

A. Recurring Issues In Dr. Cooklev's Rebuttal Report

46. Before addressing Dr. Cooklev's specific arguments with respect to the references that render the asserted claims obvious, I highlight below three recurring issues in Dr. Cooklev's rebuttal report.

1. DSL Standards in Existence On the Family 3 Patents' Priority Date Did Not Foreclose the Use of Shared Memory For Interleaving and Deinterleaving.

47. Dr. Cooklev repeatedly asserts, without any support whatsoever, that DSL standards in existence as of the priority date of the Family 3 patents *required* the use of separate and dedicated interleaving memory and deinterleaving memory. *See, e.g.*, Cooklev Report at ¶ 42 ("DSL systems, such as, for example, ADSL2/2+ standards known at the time of the inventions, specify dedicated interleaving memory requirements in each transceiver separately for upstream and downstream transmission (i.e. in each direction separately). More specifically, an ADSL2/2+ ATU-C is required to have a specified amount of dedicated interleaving memory for downstream data transmission and separately and independently have a specified amount of dedicated interleaving memory for upstream data reception."); *id.* at ¶ 44 ("The ADSL2/2+ standards do not specify or enable memory sharing between the interleaver and the deinterleaver in a single transceiver.").

48. The ADSL2/2+ standards do not support Dr. Cooklev's assertions. As I explained above (*see supra*, § IV), none of the ADSL2/2+ standards specifies the use of dedicated memory for interleaving or deinterleaving or forbids the use of shared memory, construed by the Court to be "common memory used by at least two functions, where a portion of the memory can be used by either one of the functions." Furthermore, none of the standards on which Dr. Cooklev purports to rely even uses the word "memory." As I have explained, the standards do not specify or require any particular memory configuration for interleaving or

deinterleaving, much less the use of dedicated memory for interleaving and separate dedicated memory for deinterleaving. Whether a transceiver uses shared memory or dedicated memory for interleaving and deinterleaving is an implementation choice. Nothing in ADSL2/2+ would prohibit a transceiver from using shared memory, as construed by the Court, for interleaving and deinterleaving, and all of Dr. Cooklev's statements to the contrary are incorrect.

2. Speculative and Unsupported Assertions That Prior-Art Transceivers Did Not Use Shared Memory.

49. Dr. Cooklev also repeatedly asserts, without any support whatsoever, that all prior-art DSL transceivers used dedicated interleaving memory and dedicated deinterleaving memory. *See, e.g.*, Cooklev Report at ¶ 45 ("Prior to the inventions disclosed in the Family 3 patents, an amount of memory available to an interleaver was predetermined and an amount of memory available to a deinterleaver was predetermined. Those systems were incapable of sharing memory between an interleaving and deinterleaving function based on a message."); *id.* at ¶ 102 ("LB-031 is perfectly consistent with the practice of its time, which was to use a dedicated, fixed-size interleaver memory and a separate, dedicated, fixed-size deinterleaver memory in a transceiver. . . . Thus, no portion of a memory can be used by either an interleaver or a deinterleaver."); *id.* at ¶ 106 (same); *id.* at ¶ 276 ("The use of such dedicated memories is consistent with other ADSL and G.Lite-compliant modems of that era and proposals for VDSL modems. . . ."); *id.* at ¶ 290 (same); *id.* at ¶ 304 (same); *id.* at ¶ 312 (same); *id.* at ¶ 327 (same); *id.* at ¶ 332 (same); *id.* at ¶ 368 (same); *id.* at ¶ 379 (same); *id.* at ¶ 385 (same).

50. Dr. Cooklev has provided no support for these assertions. And, as I explained above, various prior art references in the DSL field disclose the use of shared memory, as recognized by the examiners during prosecution of the Family 3 patents. *See supra*, ¶¶ 15-26.

51. Furthermore, Dr. Cooklev does not purport to have determined how prior-art transceivers in general, or even just prior-art ADSL2/2+ transceivers specifically, implemented interleaving and deinterleaving. As I explained at Section VII.C of my Opening Report and in the later discussion of bases for invalidity, a number of systems prior to the time of the invention of the Family 3 patents used shared memory as construed by this Court. Additionally, and as I noted above, even though he worked for Aware from 2000 to 2002, Dr. Cooklev has not even stated whether Aware's transceivers operated as he contends, *i.e.*, using dedicated interleaving memory and dedicated deinterleaving memory. Furthermore, he has not represented that he has determined how other existing prior-art transceivers, whether for DSL or other applications, provided memory for interleaving and deinterleaving, much less that they did not use shared memory as construed by the Court. In my opinion, there is no basis whatsoever for Dr. Cooklev's conclusion that prior-art transceivers did not use shared memory for interleaving and deinterleaving.

3. Incorrect Assumption That A Skilled Artisan Would Not Be Able to Modify Aspects of a Reference When Making a Combination.

52. In attempting to rebut my arguments that a skilled artisan would have been motivated to combine the teachings of a first reference with the teachings of a second reference in the manner claimed, Dr. Cooklev repeatedly assumes that the skilled artisan would merely have attempted to combine the teachings of the references without any modification at all, and, if the resulting combination would not work, would have abandoned all attempts to combine those references. *See, e.g.*, Cooklev Report at ¶ 210 ("A POSITA would not look to add a message (from LB-031 or otherwise) to the system disclosed in Mazzoni, and in fact doing so would provide no useful benefit. This is because the system disclosed in Mazzoni relies on the use of a pre-populated table of I, M, I′ and M′ parameter values. . . . There is no use for a

message. . . ."); *id.* at ¶ 211 ("An additional reason why LB-031's exchange of maximum supported memory sizes would not be recognized as beneficial to Mazzoni is that it is incompatible."); *id.* at ¶ 298 ("a POSITA would recognize that this implementation would be inoperable with G.993.1."); *id.* at ¶ 206 ("One of skill in the art at the time would have understood that many of these references would be completely incompatible with one another and/or, if combined, would provide no useful benefit."); *id.* at ¶ 296 (same); *id.* at ¶ 317 (same); *id.* at ¶ 344 (same); *id.* at ¶ 375 (same); *id.* at ¶ 382 (same); *id.* at ¶ 347 ("A POTISA would not look to add a message (from G.993.1 or otherwise) to the system disclosed in Mazzoni, and in fact doing so would provide no useful benefit. This is because the system disclosed in Mazzoni relies on the use of a pre-populated table of I, M, I′ and M′ parameter values. . . . There is no use for a message. . . .").

53. I disagree. In my Opening Report, I set forth my understanding of the conditions and factors that would have led a skilled artisan to combine the teachings of multiple references in the manner claimed. Jacobsen Opening Report at ¶¶ 21-27. With that understanding, I have more faith than Dr. Cooklev does in the abilities of the skilled artisan as of the Family 3 patents' priority date to have recognized how the disclosures of the different references could be combined. For example, and as I explain in more detail below with respect to specific combinations of references, the skilled artisan would have recognized the shortcomings of the individual references and would have considered the teachings of other references that could be incorporated, with or without modification, to address or mitigate those shortcomings. Thus, I do not agree with Dr. Cooklev's conclusions that a skilled artisan would not have been motivated to combine references simply because bolting them together wholesale and without any modification would not make sense.

B. LB-031 Renders the Asserted Claims Obvious.

54. As explained below, having considered Dr. Cooklev's opinion to the contrary, it remains my opinion that LB-031 renders obvious claim 1 of the '048 patent, claim 5 of the '381 patent, claim 13 of the '882 patent, and claim 19 of the '473 patent.

55. Dr. Cooklev concedes that LB-031 was publicly available as of the priority date of the Family 3 patents.

1. Claim 1 of the '048 Patent

56. Having considered Dr. Cooklev's arguments to the contrary, it remains my opinion that LB-031 in view of the knowledge of one of ordinary skill in the art at the time of the alleged invention renders claim 1 of the '048 patent obvious.

a. 1[a]. "A system that allocates shared memory"

57. Dr. Cooklev argues that LB-031 does not disclose "[a] system that allocates shared memory." Cooklev Report at ¶¶ 99-110. He takes issue with my statement that a person having ordinary skill in the art would have understood an example in LB-031 to teach allocating memory for interleaving and deinterleaving. Cooklev Report at ¶ 100. Specifically, Dr. Cooklev contends that the example in LB-031—that "[i]f the minimum interleaver delay requirement were 5.23 ms, then, from equation (5) and equation (1), this transceiver must support a delay of at least 29092 octets which corresponds to having an interleaver memory of *at least* 14546 octets according to equation (2)" (LB0031 at 4 (emphasis in original))—does not teach allocating a shared memory between an interleaver and a deinterleaver within a single transceiver. Cooklev Report at ¶¶ 100-01. He notes that LB-031 "is describing the memory requirements for an interleaver in one transceiver and the corresponding memory requirements for a deinterleaver in a second transceiver at the other end of the communication channel." Cooklev Report at ¶ 101. Dr. Cooklev accuses me of "omitting," "ignoring," or "attempting to

confuse" the "fundamental detail" that the equations of LB-031 "separately characterize the delay and memory requirements for a single latency path/direction." Cooklev Report at ¶¶ 102, 103. I disagree with Dr. Cooklev's characterization of my opinion.

58. First, I explained in my discussion of the background of the technology that the "process of interleaving in the transmitter and deinterleaving in the receiver" results in an "end-to-end interleaver delay (with the understanding that the delay contributed by the deinterleaving process is included, too)." Jacobsen Opening Report at ¶ 66. I also explained in my discussion of LB-031 that LB-031 considers end-to-end interleaving delay. *See, e.g.*, Jacobsen Opening Report at ¶¶ 166-77. Furthermore, the equation I provided at paragraph 67, in the technology background section, as representing the minimum amount of memory required for an interleaver/deinterleaver pair is the same as Equation (1) of LB-031. *Compare* Jacobsen Opening Report at ¶ 67 *with id.* at ¶ 166. Nothing about my discussion of LB-031 misleading, nor does it "omit," "ignore," or "attempt to confuse" that the end-to-end delay involves the interleaver in one transceiver and the deinterleaver in a different transceiver.

59. Second, the implication of Dr. Cooklev's argument is that, having an understanding of the disclosures of LB-031 and the memory requirements stemming from a specified end-to-end delay, a person having ordinary skill in the art would not have understood that the teachings of LB-031 would apply to both the downstream and upstream transmission directions. In other words, Dr. Cooklev's argument requires the skilled artisan not to have recognized that the VDSL2 transceiver contemplated by LB-031 would need to perform ***both*** interleaving in the transmit direction ***and*** deinterleaving in the receive direction, even though LB-031 states that, after exchanging capabilities, "[t]he VTU-O and VTU-R would then select the smaller of the transmitter and receiver capabilities, ***in each direction***, as the end-to-end

capabilities." LB-031 at p. 3 (emphasis added). According to Dr. Cooklev's argument, the skilled artisan would not have recognized that the example provided in LB-031 would apply to both transmission directions, and therefore would, in fact, specify a minimum amount of interleaver memory (for transmission) *and* a minimum amount of deinterleaver memory (for reception) that the transceiver would need to perform both interleaving and deinterleaving. I disagree that the skilled artisan would not have made this connection.

60. Dr. Cooklev opined in the "Expert Report of Dr. Todor Cooklev, Ph.D., Regarding Infringement of the Family 3 Patents" ("Cooklev Opening Infringement Report") that "a POSITA at the time of the invention had (i) a Bachelor's degree in Electrical Engineering or a related field, and (ii) two to three years' of experience working in DSL or other broadband communications (or a Master's Degree in Electrical Engineering or a related field, particularly with an emphasis in the area of communications)." Cooklev Opening Infringement Report at ¶ 27. As I explained in my rebuttal to that report and also in my Opening Report (*see, e.g.*, Jacobsen Opening Report at ¶ 45), it is my opinion that the level of skill was higher than Dr. Cooklev has opined; nevertheless, even a person having the level of skill suggested by Dr. Cooklev would have understood that a DSL transceiver would include a transmitter that would perform interleaving and a receiver that would perform deinterleaving. Thus, even Dr. Cooklev's skilled artisan would have recognized that the example I cited from LB-031 would apply to both transmission directions.

61. Dr. Cooklev also contends that "Dr. Jacobsen has not identified any disclosure in LB-031 that requires that a shared memory is used or that any portion of memory within a single transceiver can be used by the interleaver or the deinterleaver." Cooklev Report at ¶ 106. But I did not opine that LB-031 requires the use of a shared memory; I opined that one of

ordinary skill in the art would have understood from the disclosures of LB-031 that the allocated memory can be a shared memory, which is something that was known in the art as of the Family 3 patents' priority date. Jacobsen Opening Report at ¶ 181; *see also supra*, § VII.A.2; *supra*, ¶¶ 15-26.

62. Dr. Cooklev asserts—without any citation or support—that "LB-031 is perfectly consistent with the practice of its time, which was to use a dedicated, fixed-size interleaver memory and a separate, dedicated, fixed-size deinterleaver memory in a transceiver," and that "no portion of a memory can be used by either an interleaver or a deinterleaver." Cooklev Report at ¶ 106. As I explained *supra*, (*see, e.g.*, ¶ 17), Dr. Cooklev has not identified any basis for this assertion, which, in my opinion, amounts to speculation. *See also supra*, § VII.A.2.

63. Dr. Cooklev then asserts that because LB-031 teaches that the size of the interleaver memory will be "a major source of complexity in VDSL2," (LB-031 at p. 1), a skilled artisan would be discouraged "from attempting add further complexity to interleaver memory in VDSL2, such as by proposing a memory sharing scheme." Cooklev Report at ¶ 107. Dr. Cooklev asserts that "a shared memory implementation would increase and not decrease the complexity of the implementation proposed by the LB-031 reference." Cooklev Report at ¶ 108. As an initial matter, Dr. Cooklev's argument is inconsistent with and contrary to his contention in his opening report on infringement that the use of shared memory allows "the combined amount of interleaver memory and deinterleaver memory required for a transceiver [to be] approximately cut by half." Cooklev Opening Infringement Report at ¶ 86. Assuming Dr. Cooklev is correct that memory sharing reduces the amount of memory required in a transceiver by approximately half, he has not explained why that reduction would not have been

recognized or understood by a person having ordinary skill in the art as of the Family 3 patents' priority date.

64. Additionally, Dr. Cooklev has not explained why he contends that a shared memory implementation would actually increase the complexity of the implementation proposed by LB-031, or why a skilled artisan would understand it to do so. *See* Cooklev Rebuttal Report, ¶¶ 107-08. The references I discussed in my Opening Report say just the opposite. For example, Mazzoni teaches that a shared memory "has a first memory space assigned to the interleaving means and a second memory space assigned to the deinterleaving means," which enables a considerable reduction in "the size of the memory means required for the interleaving and deinterleaving means implemented within a modem." Mazzoni at col. 2:10-21. Voith teaches that "in order to minimize the number of integrated circuit pins required to access external memory, the interleave and de-interleave buffers are also preferably implemented in the same physical memory and digital interface unit 3 preferably multiplexes between interleaving and de-interleaving operations." Voith at col. 4:35-40. Fadavi-Ardekani, which teaches the use of a shared memory for interleaving and deinterleaving, states that the disclosed "buffering and scheduling scheme for synchronizing the digital signal processing tasks for multiple asynchronous ADSL lines" allows "the various components of the ADSL transceiver [] to operate seamlessly (i.e., in a semi-synchronous fashion) and the design sizes of various transceiver components and the data flow complexity of the transceiver [to be] reduced." Fadavi-Ardekani at col. 4:11-18. In my opinion, a skilled artisan would have understood all of Mazzoni, Voith, and Fadavi-Ardekani to teach that using shared memory decreases complexity by decreasing at least the size of the memory and the number of integrated circuit pins required to access the memory. Therefore, I disagree with Dr. Cooklev's assertions

that any of the references would "increase complexity of the implementation of the LB-031 disclosure." Cooklev Report at ¶ 109.

65. Dr. Cooklev asserts that there would be no motivation to combine any of the references cited in paragraph 182 of my Opening Report with LB-031. Cooklev Report at ¶¶ 109, 110. Notwithstanding that this portion of Dr. Cooklev's report purports to address my argument that LB-031 combined with the knowledge of a skilled artisan as of the alleged invention date renders the asserted Family 3 claims obvious, Dr. Cooklev is incorrect. As I explained in my Opening Report, a skilled artisan would have been motivated to combine the teachings of at least LB-031 and Mazzoni (Jacobsen Opening Report at ¶¶ 345-50) and LB-031 and Voith (*id.* at ¶¶ 566-569).

66. Therefore, it remains my opinion that a person having ordinary skill in the art as of the Family 3 patents' priority date would have understood LB-031 to disclose the preamble, element 1[a], of claim 1 of the '048 patent, to the extent that it is limiting.

b. 1[b]. "a transceiver that is capable of"

67. Dr. Cooklev concedes that LB-031 discloses a transceiver. *See, e.g.*, Cooklev Report at ¶¶ 90-192.

c. 1[c]. "transmitting or receiving a message during initialization specifying a maximum number of bytes of memory that are available to be allocated to an interleaver"

68. Dr. Cooklev concedes that the transceiver of LB-031 is capable of "transmitting or receiving a message during initialization specifying a maximum number of bytes of memory that are available to be allocated to an interleaver" under TQ Delta's interpretation of the limitation.[3] *See, e.g.*, Cooklev Report at ¶¶ 90-192.

[3] As I explained in my Opening Report (*see, e.g.*, ¶ 188), I do not agree with TQ Delta's interpretation that transmission or reception of the O-PMS message of VDSL2 meets this

d. 1[d]. "determining an amount of memory required by the interleaver to interleave a plurality of Reed Solomon (RS) coded data bytes within the shared memory"

69. Dr. Cooklev argues that the transceiver of LB-031 is not capable of "determining an amount of memory required by the interleaver to interleave a plurality of Reed Solomon (RS) coded data bytes within the shared memory." Cooklev Report at ¶¶ 111-14. Dr. Cooklev's argument is based solely on his opinion that LB-031 does not disclose "shared memory." *Id.* at ¶ 113.

70. I disagree. As I explained in my Opening Report (*see* Jacobsen Opening Report at ¶¶ 179-83) and *supra* (*see* § VII.B.1.a) a skilled artisan would have understood LB-031 to disclose "[a] system that allocates shared memory." In turn, a skilled artisan would also have understood LB-031 to disclose element 1[d].

71. Therefore, it remains my opinion that LB-031 discloses element 1[d].

e. 1[e]. "allocating a first number of bytes of the shared memory to the interleaver to interleave the first plurality of Reed Solomon (RS) coded data bytes for transmission at a first data rate"

72. Dr. Cooklev opines that LB-031 does not disclose, teach, or suggest "allocating a first number of bytes of the shared memory to the interleaver to interleave the first plurality of Reed Solomon (RS) coded data bytes for transmission at a first data rate." Cooklev Report at ¶ 115. Again, Dr. Cooklev's argument is based on his conclusion that "LB-031 lacks disclosure of a shared memory as construed by the Court." Cooklev Report at ¶ 116. I disagree. As I explained in my Opening Report (*see* Jacobsen Opening Report at ¶¶ 179-83) and *supra* (*see* § VII.B.1.a) a skilled artisan would have understood LB-031 to disclose "[a] system that allocates shared memory."

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limitation, but to the extent the Court or fact-finder agrees with this interpretation, LB-031 also meets this limitation.

73. Dr. Cooklev also complains that the statement in LB-031 that "[t]he VTU-O and VTU-R would then select the smaller of the transmitter and receiver capabilities, in each direction, as the end-to-end capabilities" would only apply to "e.g., interleaver capabilities of the VTU-O and deinterleaver capabilities of the VTU-R for the downstream direction." Cooklev Report at ¶ 117. To the extent Dr. Cooklev is suggesting that the disclosures of LB-031 apply only to the downstream direction, I disagree. LB-031 is clear that the VTU-O and VTU-R select transmitter and receiver capabilities in both transmission directions. *See, e.g.*, LB-031 at p. 3. Consequently, and as I explained above, a skilled artisan would have understood LB-031 to address both the VTU-O's interleaving and deinterleaving requirements, and the VTU-R's interleaving and deinterleaving requirements, in whatever way they are implemented.

74. Therefore, having considered Dr. Cooklev's opinion to the contrary, it remains my opinion that LB-031 discloses element 1[e].

f. 1[f]. "wherein the allocated memory for the interleaver does not exceed the maximum number of bytes in the message"

75. Dr. Cooklev argues that LB-031 does not disclose "wherein the allocated memory for the interleaver does not exceed the maximum number of bytes in the message." Cooklev Report at ¶ 119. The entirety of Dr. Cooklev's argument is that "LB-031 does not disclose, teach, or suggest transmitting or receiving a message during initialization specifying a maximum number of bytes of memory that are available to be allocated to an interleaver." Cooklev Report at ¶ 120. Dr. Cooklev is incorrect. As noted above (*see* supra ¶ 68), Dr. Cooklev conceded that LB-031 discloses element 1[c]: "transmitting or receiving a message during initialization specifying a maximum number of bytes of memory that are available to be allocated to an interleaver." Therefore, Dr. Cooklev's "argument" is merely a conclusory

statement that does not rebut my opinion, set forth in my Opening Report (*see* ¶¶ 196-200), that LB-031 discloses element 1[f]. To the extent that Dr. Cooklev changes or corrects this opinion at a later date, I reserve the right to respond.

76. Therefore, having considered Dr. Cooklev's statement to the contrary, it remains my opinion that LB-031 discloses "wherein the allocated memory for the interleaver does not exceed the maximum number of bytes specified in the message."

g. 1[g]. "allocating a second number of bytes of the shared memory to a deinterleaver to deinterleave a second plurality of RS coded data bytes received at a second data rate"

77. Dr. Cooklev asserts that LB-031 does not disclose, teach, or suggest "allocating a second number of bytes of the shared memory to a deinterleaver to deinterleave a second plurality of RS coded data bytes received at a second data rate." Cooklev Report at ¶ 121. Dr. Cooklev's argument relies once again on his assertion that "LB-031 lacks disclosure of shared memory as construed by the Court." *Id.* at ¶ 123. Specifically, Dr. Cooklev argues that "[t]here is no disclosure or contemplation of sharing a memory within a single transceiver for an interleaver operating in a first direction and a deinterleaver operating in a second direction." *Id.* at ¶ 124. I disagree because, as I explained above (*see, e.g.*, *supra*, ¶¶ 58-66), a skilled artisan would have understood LB-031 to address both the VTU-O's interleaving and deinterleaving requirements, and the VTU-R's interleaving and deinterleaving requirements, however they are implemented, including with shared memory.

78. Therefore, having considered Dr. Cooklev's argument to the contrary, it remains my opinion that LB-031 discloses element 1[g].

h. 1[h]. "interleaving the first plurality of RS coded data bytes within the shared interleaver memory allocated to the interleaver and deinterleaving the second plurality of RS coded data bytes within the shared memory allocated to the deinterleaver"

79. Dr. Cooklev argues that LB-031 does not disclose, teach, or suggest "interleaving the first plurality of RS coded data bytes within the shared interleaver memory allocated to the interleaver and deinterleaving the second plurality of RS coded data bytes within the shared memory allocated to the deinterleaver." Cooklev Report at ¶ 126. Dr. Cooklev states again that "LB-031 is consistent with the practice at that time of using a dedicated interleaver memory and a separate deinterleaver memory." *Id.* at ¶ 128. I disagree because, as I explained above (*see, e.g., supra*, § VII.A.2), Dr. Cooklev's opinion amounts to speculation as to how transceivers implemented interleaver and deinterleaver memory. Dr. Cooklev has not provided any support for his assertion that "the practice at that time" was to use "dedicated interleaver memory and a separate deinterleaver memory."

80. As I explained in my Opening Report, a skilled artisan would have understood LB-031 to disclose a transceiver with a convolutional interleaver, which would operate to interleave RS coded data bytes at the transmitter and a convolutional deinterleaver, which would operate to deinterleave RS coded data bytes, and that the interleaver and deinterleaver could use shared memory. Jacobsen Opening Report at ¶¶ 179-83, 205; *see also supra*, ¶¶ 58-66. Because LB-031 discloses a VDSL2 VTU-O and VTU-R in communication with each other, one of ordinary skill in the art would have understood that the VTU-O (or VTU-R) would interleave the first plurality of RS coded data bytes within the shared interleaver memory allocated to the interleaver, and the deinterleaver would deinterleave the second plurality of RS code data bytes within the shared memory allocated to the deinterleaver. Jacobsen Opening Report at ¶ 205.

81. Thus, having considered Dr. Cooklev's opinion to the contrary, it remains my opinion that LB-031 discloses element 1[h].

i. 1[i]. "wherein the shared memory allocated to the interleaver is used at the same time as the shared memory allocated to the deinterleaver"

82. Dr. Cooklev's argument that LB-031 does not disclose element 1[i] is based on his assertion that "LB-031 does not disclose allocating shared memory in a single transceiver." Cooklev Report at ¶¶ 131-34. As I explained above, a skilled artisan would have understood the disclosures of LB-031 to extend to implementations in which the interleaver and deinterleaver use shared memory. *See supra*, ¶¶ 58-66. And because, as a person having ordinary skill in the art as of the priority date of the Family 3 patents would have understood, VDSL transceivers transmit and receive data at the same time, the deinterleaver must be able to read from, write to, or hold information for deinterleaving in the portion of memory allocated to the deinterleaver at the same time the interleaver is able to read from, write to, or hold information for interleaving in the portion of memory allocated to the interleaver. Jacobsen Opening Report at ¶ 207.

83. Consequently, having considered Dr. Cooklev's opinion to the contrary, it remains my opinion that LB-031 discloses element 1[i]. In addition, it remains my opinion that LB-031 discloses all of the limitations of claim 1 of the '048 patent.

2. Claim 5 of the '381 Patent

84. It remains my opinion that LB-031 in view the knowledge of one of ordinary skill in the art renders claim 5 of the '381 patent obvious.

a. 5[a]. "A non-transitory computer-readable information storage media having stored thereon instructions, that if executed by a processor, cause to be performed a method for allocating shared memory in a transceiver"

85. As I opined in my Opening Report, it is my opinion that LB-031 discloses the preamble, to the extent it is limiting. *See* Jacobsen Opening Report at ¶¶ 209-10. As I

explained, one of ordinary skill in the art would have understood that methods such as the one recited in claim 5 of the '381 patent could be accomplished by a processor executing instructions stored on computer-readable information storage media. *Id.* at ¶ 110. Moreover, as I explained, a skilled artisan would have understood that the disclosures of LB-031 would extend to shared memory, the use of which was well known as of the Family 3 patents' priority date. *See supra*, ¶ 58-66.

86. Dr. Cooklev appears to assert that because "one or more of the claimed functions could be implemented in hardware, and therefore would not necessarily have to be carried out through an execution of instructions stored on a non-transitory computer-readable media," LB-031 does not disclose the preamble of claim 5. Cooklev Report at ¶ 141. I disagree. First, according to Dr. Cooklev, "a POSITA at the time of the invention had (i) a Bachelor's degree in Electrical Engineering or a related field, and (ii) two to three years' of experience working in DSL or other broadband communications (or a Master's Degree in Electrical Engineering or a related field, particularly with an emphasis in the area of communications)." Cooklev Opening Infringement Report at ¶ 27. A person having the level of skill suggested by Dr. Cooklev would have understood that transceivers include hardware and software, and therefore the universe of ways to implement a transceiver as taught by LB-031 extends to hardware, software, or some combination of the two. That LB-031 does not explicitly refer to a particular approach does not mean that a skilled artisan would not have understood that approach to be disclosed.

87. Second, because LB-031 discloses equations that depend on settings and capabilities determined during the initialization procedure, a skilled artisan would have understood the most likely way the transceiver disclosed in LB-031 would implement these

equations would be in software, i.e., via instructions that would be executed by a processor. *See, e.g.*, LB-031 at p. 2-5.

88. Thus, having considered Dr. Cooklev's opinion to the contrary, it remains my opinion that LB-031 discloses the preamble of claim 5.

b. 5[b]. "transmitting or receiving, by the transceiver, a message during initialization specifying a maximum number of bytes of memory that are available to be allocated to a deinterleaver"

89. Dr. Cooklev concedes that LB-031 discloses "transmitting or receiving, by the transceiver, a message during initialization specifying a maximum number of bytes of memory that are available to be allocated to an interleaver" under TQ Delta's interpretation of the limitation. *See, e.g.*, Cooklev Report at ¶¶ 90-192.

c. 5[c]. "determining, at the transceiver, an amount of memory required by the deinterleaver to deinterleave a first plurality of Reed Solomon (RS) coded data bytes within a shared memory"

90. Dr. Cooklev disputes that LB-031 discloses "determining, at the transceiver, an amount of memory required by the deinterleaver to deinterleave a first plurality of Reed Solomon (RS) coded data bytes within a shared memory." Dr. Cooklev's rebuttal refers to his arguments with respect to element 1[d]. I explained above (*see supra*, § VII.B.1.d) why I disagree with Dr. Cooklev.

91. Thus, having considered Dr. Cooklev's opinion to the contrary, it remains my opinion that LB-031 discloses "determining, at the transceiver, an amount of memory required by the deinterleaver to deinterleave a first plurality of Reed Solomon (RS) coded data bytes within a shared memory."

d. 5[d] "allocating, in the transceiver, a first number of bytes of the shared memory to the deinterleaver to deinterleave a first plurality of Reed Solomon (RS) coded data bytes for transmission at a first data rate"

92. Dr. Cooklev disputes that LB-031 discloses "allocating, in the transceiver, a first number of bytes of the shared memory to the deinterleaver to deinterleave a first plurality of Reed Solomon (RS) coded data bytes for transmission at a first data rate." Dr. Cooklev's rebuttal refers to his arguments with respect to elements 1[e] and 1[g]. I explained above (*see supra*, § VII.B.1.e, § VII.B.1.g) why I disagree with Dr. Cooklev.

93. Consequently, it remains my opinion that LB-031 discloses "allocating, in the transceiver, a first number of bytes of the shared memory to the deinterleaver to deinterleave a first plurality of Reed Solomon (RS) coded data bytes for transmission at a first data rate."

e. 5[e]. "wherein the allocated memory for the deinterleaver does not exceed the maximum number of bytes specified in the message"

94. Dr. Cooklev's rebuttal for element 5[e] refers to his arguments with respect to element 1[f]. I explained above (*see supra*, § VII.B.1.f) why I disagree with Dr. Cooklev.

95. Consequently, it remains my opinion that LB-031 discloses "wherein the allocated memory for the deinterleaver does not exceed the maximum number of bytes specified in the message."

f. 5[f]. "allocating, in the transceiver, a second number of bytes of the shared memory to an interleaver to interleave a second plurality of RS coded data bytes transmitted at a second data rate"

96. Dr. Cooklev's rebuttal refers to his arguments with respect to elements 1[e] and 1[g]. I explained above (*see supra*, § VII.B.1.e, § VII.B.1.g) why I disagree with Dr. Cooklev.

97. Consequently, it remains my opinion that LB-031 discloses "allocating, in the transceiver, a second number of bytes of the shared memory to an interleaver to interleave a second plurality of RS coded data bytes transmitted at a second data rate."

g. 5[g]. "deinterleaving the first plurality of RS coded data bytes within the shared memory allocated to the deinterleaver and interleaving the second plurality of RS coded data bytes within the shared memory allocated to the interleaver"

98. Dr. Cooklev's rebuttal for element 5[g] refers to his arguments with respect to element 1[h]. I explained above (*see supra*, § VII.B.1.h) why I disagree with Dr. Cooklev.

99. Consequently, it remains my opinion that LB-031 discloses "deinterleaving the first plurality of RS coded data bytes within the shared memory allocated to the deinterleaver and interleaving the second plurality of RS coded data bytes within the shared memory allocated to the interleaver."

h. 5[h]. "wherein the shared memory allocated to the deinterleaver is used at the same time as the shared memory allocated to the interleaver"

100. Dr. Cooklev's rebuttal for element 5[h] refers to his arguments with respect to element 1[i]. I explained above (*see supra*, § VII.B.1.i) why I disagree with Dr. Cooklev.

101. Consequently, it remains my opinion that LB-031 discloses "wherein the shared memory allocated to the deinterleaver is used at the same time as the shared memory allocated to the interleaver." In addition, having considered Dr. Cooklev's argument to the contrary, it remains my opinion that LB-031 discloses all of the limitations of claim 5 of the '381 patent.

3. Claim 13 of the '882 Patent

102. It remains my opinion that LB-031 in view the knowledge of one of ordinary skill in the art renders claim 13 of the '882 patent obvious.

a. 13[a]. "A system that allocates shared memory"

103. Dr. Cooklev's rebuttal for element 13[a] refers to his argument with respect to element 1[a]. I explained above (*see supra*, § VII.B.1.a) why I disagree with Dr. Cooklev.

104. Consequently, it remains my opinion that LB-031 discloses "[a] system that allocates shared memory."

b. 13[b]. "a transceiver that performs"

105. Dr. Cooklev concedes that LB-031 discloses a transceiver. *See, e.g.*, Cooklev Report at ¶¶ 90-192.

c. 13[c]. "transmitting or receiving a message during initialization specifying a maximum number of bytes of memory that are available to be allocated to an interleaver"

106. Dr. Cooklev concedes that the transceiver of LB-031 is capable of "transmitting or receiving a message during initialization specifying a maximum number of bytes of memory that are available to be allocated to an interleaver" under TQ Delta's interpretation of the limitation. *See, e.g.*, Cooklev Report at ¶¶ 90-192.

d. 13[d] through 13[i].

107. Dr. Cooklev's rebuttal for elements 13[d] through 13[j] refers to his argument with respect to elements 5[c] through 5[h]. I explained above (*see supra*, §§ VII.B.2.c-VII.B.2.h) why I disagree with Dr. Cooklev.

108. Consequently, it remains my opinion that LB-031 discloses elements 13[d] through 13[i] of claim 13 of the '882 patent. In addition, having considered Dr. Cooklev's argument to the contrary, it remains my opinion that LB-031 discloses all of the limitations of claim 13 of the '882 patent.

4. Claim 19 of the '473 Patent

109. Having considered Dr. Cooklev's arguments to the contrary, it remains my opinion that LB-031 discloses each limitation of claim 19 of the '473 patent.

a. 19[a]. "An apparatus comprising"

110. Dr. Cooklev concedes that LB-031 discloses an apparatus. *See, e.g.*, Cooklev Report at ¶¶ 164-92.

b. 19[b]. "a multicarrier communications transceiver that is configured to perform an interleaving function associated with a

first latency path and perform a deinterleaving function associated with a second latency path"

111. Dr. Cooklev concedes that LB-031 discloses "a multicarrier communications transceiver that is configured to perform an interleaving function associated with a first latency path and perform a deinterleaving function associated with a second latency path." *See, e.g.*, Cooklev Report at ¶¶ 164-92.

c. 19[c]. "the multicarrier communications transceiver being associated with a memory"

112. Dr. Cooklev concedes that LB-031 discloses "the multicarrier communications transceiver being associated with a memory." *See, e.g.*, Cooklev Report at ¶¶ 164-92.

d. 19[d]. "wherein the memory is allocated between the interleaving function and the deinterleaving function in accordance with a message received during an initialization of the transceiver"

113. Dr. Cooklev contends that "LB-031 does not disclose, teach, or suggest a multicarrier transceiver being associated with a memory wherein the memory is allocated between the interleaving function and the deinterleaving function in accordance with a message received during initialization of the transceiver." Cooklev Report at ¶ 171. Specifically, he argues that "no portion of any memory contemplated by LB-031 is used as interleaver memory at one point in time and deinterleaver memory at another point in time and, thus, LB-031 does not allocate memory *between* an interleaving function and a deinterleaving function." *Id.* at ¶ 172.

114. Without any support whatsoever, Dr. Cooklev states that "one of ordinary skill in the art would understand LB-031 in the context of a system in which the CO transceiver (VTU-O) has a dedicated amount of memory available to be used for downstream interleaving and a separate, dedicated amount of memory available to be used for upstream deinterleaving and the CPE transceiver (VTU-R) has a dedicated amount of memory available to be used for

downstream deinterleaving and a separate, dedicated amount of memory available to be used for upstream interleaving." *Id.* I disagree. As I explained (*see supra*, ¶ 62), Dr. Cooklev has not explained why, in his opinion, a skilled artisan would not have understood the disclosures of LB-031 to extend not only to implementations using dedicated interleaving and deinterleaving memories, but also implementations using shared memory as disclosed in various prior-art references. *See, e.g., supra*, § VII.A.2.

115. Dr. Cooklev argues that "[e]ven assuming the exchange of information described in LB-031 occurs during initialization and occurs through an exchange of messages, LB-031 would not disclose to a person of ordinary skill in the art a message that is used to perform the claimed allocation." Cooklev Report at ¶ 174. Based on the disclosures in LB-031 that "[i]f a VDSL2 implementation supports a larger interleaver memory than is required, it should be free to specify the larger value," in which case "[t]he VTU-O and VTU-R would then select the smaller of the transmitter and receiver capabilities, in each direction, as the end-to-end capabilities," Dr. Cooklev sets forth a four-step messaging and selection procedure that, according to him, a skilled artisan would have understood to occur. Cooklev Report at ¶ 174. He then concludes that that "no portion of memory is allocated between the interleaving function and the deinterleaving function in accordance with a message. Cooklev Report at ¶ 175.

116. I disagree with both Dr. Cooklev's hypothetical messaging and selection procedure and his conclusion. Dr. Cooklev's hypothetical messaging sequence, which appears nowhere in LB-031, presumes that the downstream and upstream interleaving negotiations are independent of each other, which is a result of his assumption that the VTU-O and VTU-R use dedicated interleaving and deinterleaving memories. In other words, Dr. Cooklev's messaging

and selection procedure presume his conclusion. In my opinion, a skilled artisan would have understood that the guidance of LB-031—that "[i]f a VDSL2 implementation supports a larger interleaver memory than is required, it should be free to specify the larger value," in which case "[t]he VTU-O and VTU-R would then select the smaller of the transmitter and receiver capabilities, in each direction, as the end-to-end capabilities"—would apply regardless of whether a VTU-O or VTU-R implements interleaving and deinterleaving using a shared memory or dedicated memory. And, as I have explained (*see, e.g.*, *supra* ¶¶ 15-26, § VII.A.2), the use of shared memory for interleaving and deinterleaving was well known in the art and would have been known to a person having ordinary skill in the art considering the disclosures of LB-031.

117. Dr. Cooklev opines that "LB-031 at most discloses that, for the downstream direction, a VTU-R with larger dedicated deinterleaver memory than is required can determine whether the VTU-O also supports a larger amount." Cooklev Report at ¶ 176. He then argues that "if the VTU-O does not support a larger amount than is required, . . . the extra deinterleaver memory of the VTU-R is simply not used. *Id.* Again, I disagree, because Dr. Cooklev's conclusion presumes, again without justification, that the VTU-R implements interleaving and deinterleaving using dedicated memories. As I explained in my Rebuttal Report (*see, e.g.*, Jacobsen Rebuttal Report at § VII.C, § VII.E, § IX), none of the VDSL standards specifies that a VTU-O or VTU-R must implement interleaving and deinterleaving using either dedicated or shared memory.

118. Paragraphs 177-86 of Dr. Cooklev's report are substantially identical to paragraphs 48-57, except Dr. Cooklev refers specifically to LB-031 in paragraphs 177-86. I

explained above (*see, e.g.*, ¶¶ 17-18) why I disagree with Dr. Cooklev's conclusions with respect to his hypothetical example.

119. In paragraph 180, Dr. Cooklev states, without support, that "[b]ecause the smaller of the capabilities of the transmitter or receiver are selected in each direction in accordance with the express teaching of LB-031, unused memory for one function in a transceiver cannot be used for another function, e.g., unused dedicated deinterleaver memory in the VTU-R cannot be used for the interleaving function." Again, I disagree. LB-031 says nothing to indicate that the VTU-O and VTU-R described use dedicated interleaver memory and dedicated deinterleaver memory. And, as I have stated, in my opinion a skilled artisan would have understood the disclosures of LB-031 to apply regardless of whether an implementation used dedicated memories or shared memory for interleaving and deinterleaving.

120. Consequently, I disagree with Dr. Cooklev's statement that LB-031 "allows a transceiver to determine how much of its pre-allocated downstream memory (i.e., interleaver memory in the VTU-O and deinterleaver memory in the VTU-R) and how much of its pre-allocated upstream memory (i.e., deinterleaver memory in the VTU-O and interleaver memory in the VTU-R) can be used." Cooklev Report, ¶ 187. Dr. Cooklev has presumed, without justification, that a skilled artisan would not have understood the disclosures of LB-031 to apply regardless of whether an implementation of a VTU uses dedicated memories or shared memory for interleaving and deinterleaving.

121. Therefore, having considered Dr. Cooklev's arguments to the contrary, it remains my opinion that LB-031 discloses "wherein the memory is allocated between the interleaving function and the deinterleaving function in accordance with a message received during an initialization of the transceiver."

e. 19[e]. "wherein at least a portion of the memory may be allocated to the interleaving function or the deinterleaving function at any one particular time depending on the message"

122. Dr. Cooklev disputes that LB-031 discloses that "at least a portion of the memory may be allocated to the interleaving function or the deinterleaving function at any one particular time depending on the message." Dr. Cooklev's conclusion is based solely on his incorrect assertion that "LB-031 does not disclose any sharing of memory within a transceiver." Cooklev Report at ¶ 189. *See also id.* at ¶ 190. I explained above (*see, e.g.*, § VII.B.1.a) why a skilled artisan would have understood the disclosures of LB-031 to apply to all VTU implementations, regardless of whether they use dedicated or shared memory for interleaving and deinterleaving.

123. Furthermore, as I explained at paragraph 342 of my Opening Report (with respect to LB-031 in combination with Mazzoni), LB-031 teaches that at least a portion of the memory allocated to the interleaving function or the deinterleaving function at any one particular time is dependent on the message.[4] As I also explained in my Opening Report, (*see* Jacobsen Opening Report at § IX.A.2), LB-031 teaches that the VTU-O and VTU-R exchange the interleaver delay during initialization, and that the minimum amount of memory required to meet that delay is half of the interleaving delay. LB-031 at pp. 3, 4. Thus, the amount of memory required to meet the interleaving delay changes with the interleaving delay, which is exchanged via an initialization message, which means that at least a portion of the memory may be allocated to the interleaving function or the deinterleaving function at any one particular time depending on the message.

[4] This paragraph was inadvertently omitted from my discussion of LB-031, but it appears where I discussed LB-031 in combination with Mazzoni.

124. Therefore, having considered Dr. Cooklev's arguments to the contrary, it remains my opinion that LB-031 discloses all of the limitations of claim 19 of the '473 patent.

C. LB-031 in Combination With Mazzoni Renders the Asserted Claims Obvious

125. As explained below, having considered Dr. Cooklev's opinion to the contrary, it remains my opinion that LB-031 in combination with Mazzoni renders obvious claim 1 of the '048 patent, claim 5 of the '381 patent, claim 13 of the '882 patent, and claim 19 of the '473 patent.

1. Motivation to Combine LB-031 and Mazzoni

126. Dr. Cooklev disputes that a person having ordinary skill in the art would have been motivated to combine the teachings of Mazzoni and LB-031 in the manner claimed by the asserted claims of the Family 3 patents. Cooklev Report at ¶ 204. I disagree.

127. Dr. Cooklev argues that my statement that "both Mazzoni and LB-031 are concerned with limiting the size of memory used for interleaving and deinterleaving" is inaccurate. Cooklev Report at ¶ 207-08. Dr. Cooklev contends that "LB-031 actually wastes memory by leaving portions of memory unused where one transceiver supports more memory for a given latency path than is supported by the other transceiver with which it is communicating." Cooklev Report at ¶ 208. I disagree. As I explained above (*see supra*, § VII.B.1.a), Dr. Cooklev's conclusion is grounded in his incorrect conclusion that a person having ordinary skill in the art would not have understood the disclosures of LB-031 to apply regardless of whether an implementation uses dedicated or shared memory. Moreover, Dr. Cooklev does not explain how his conclusion that "a POSITA would be motivated **not** to use the teachings of LB-031 if they were concerned with reducing memory requirements" (Cooklev Report at ¶ 208) squares with the explicit disclosures of LB-031 that "[t]he interleaver is a

major source of complexity in VDSL," and that the proposal allows "lower complexity implementations for profiles that do not require the full VDSL2 data rate." LB-031 at p. 1. For at least these reasons, I disagree with Dr. Cooklev's conclusion that a skilled artisan would not have been motivated to combine the teachings of Mazzoni with the teachings of LB-031.

128. Dr. Cooklev also disputes my statement that a skilled artisan wishing to implement the VDSL transceiver of Mazzoni would have been motivated to include the initialization message of LB-031 so that the VTU-O and VTU-R of Mazzoni could choose values for the parameters I, M, I′ and M′ that would not exceed the size of the shared memory at the selected downstream and upstream bit rates. Cooklev Report at ¶ 209. According to Dr. Cooklev, because Mazzoni discloses the use of a pre-populated table of the parameters I, M, I′ and M′, "[t]here is no use for a message that specifies the maximum supported interleaver or deinterleaver memory size (assuming such a message is even disclosed per LB-031) because all data rate pairs and their corresponding I, M, I′ and M′ values that need to be supported are accounted for." Cooklev Report at ¶ 210. I disagree. As explained in my Opening Report (*see* Jacobsen Opening Report at ¶ 626), one of ordinary skill would have recognized the inherent limitations of Mazzoni's table, namely that all services would need to be identified ahead of time so that the table could be created and stored in the transceiver. The skilled artisan would also have recognized that, as of the priority date of the Family 3 patents, the teachings of LB-031 would enable the transceivers of Mazzoni to partition the shared memory between the interleaver and deinterleaver without requiring all of the possible services to be defined in advance to create the table disclosed in Mazzoni. Instead, by exchanging information about their interleaving and deinterleaving capabilities as disclosed in LB-031, the transceivers of Mazzoni could easily determine an appropriate allocation of the available shared memory to the

interleaver and deinterleaver for a variety of services. The resulting transceiver would have the advantage of being more flexible and "future-proof" than the transceiver described in Mazzoni.

129. At paragraph 211, Dr. Cooklev concedes that LB-031 discloses the "exchange of maximum supported memory sizes." Dr. Cooklev then provides an example that, according to him, indicates that the teachings of LB-031 are "incompatible" with those of Mazzoni. Cooklev Report at ¶ 211. Dr. Cooklev argues that "[i]f the Mazzoni VTU-O received a message indicating that the VTU-R supported a maximum downstream deinterleaver memory of 24,960 bytes and a maximum upstream interleaver memory of 10,860 bytes, this information would be useless to the VTU-O" because "it already has the information necessary to support the service for which both transceivers have been preconfigured at the time of installation," and "neither the VTU-O or VTU-R would actually be capable of simultaneously supporting both maximum interleaver and deinterleaver sizes at the same time because the total memory size of the Mazzoni transceivers is only 26,890 bytes. . . ." Cooklev Report at ¶ 211. Dr. Cooklev's hypothetical example assumes that the skilled artisan would merely add the message of LB-031 to the transceiver of Mazzoni without any modification, because his point appears to be that the memory described in Mazzoni is not large to accommodate the transmission parameters described in LB-031. This is specious, as it would be trivial to one of ordinary skill in the art to select a different-sized memory for the interleaver/deinterleaver pair. As I explained above (*see, e.g.*, *supra*, § VII.A.3) and in my Opening Report (*see* Jacobsen Opening Report at ¶ 626), the skilled artisan would have recognized the inherent limitations of Mazzoni's table, and that the teachings of LB-031 would enable the transceivers of Mazzoni to partition the shared memory between the interleaver and deinterleaver without requiring all of the possible services to be defined in advance to create the table disclosed in Mazzoni.

130. Therefore, having considered Dr. Cooklev's opinion to the contrary, it remains my opinion that a skilled artisan would have been motivated to combine the disclosures of Mazzoni and LB-031 as recited in the asserted claims of the Family 3 patents.

2. Claim 1 of the '048 Patent

131. It remains my opinion that LB-031 in combination with Mazzoni renders claim 1 of the '048 patent obvious.

132. I incorporate by reference my discussion and opinion in § VII.C.1 regarding why a person having ordinary skill in the art would have been motivated to combine the disclosures of LB-031 and Mazzoni.

a. 1[a]. "A system that allocates shared memory"

133. I explained above why I disagree with Dr. Cooklev's opinion that LB-031 does not disclose "[a] system that allocates shared memory." *See supra*, § VII.B.1.a.

134. Dr. Cooklev purports to dispute that Mazzoni discloses a system that allocates shared memory, yet his argument does not actually dispute that the transceiver of Mazzoni uses shared memory. Cooklev Report at ¶¶ 217-18. Instead, Dr. Cooklev's argument goes to the other limitations of claim 1. For example, Dr. Cooklev argues that "Mazzoni does not disclose exchanging any messages at all that include information about interleaving or deinterleaving parameters" and "Mazzoni does not disclose a transceiver that (1) transmits or receives a message during initialization specifying a maximum number of bytes of memory that are available to be allocated to an interleaver; (2) determining an amount of memory required by the interleaver to interleave a first plurality of Reed Solomon (RS) coded data bytes within the shared memory; and (3) allocating a first number of bytes of the shared memory to the interleaver to interleave a first plurality of Reed Solomon (RS) coded data bytes for transmission at a first data rate, wherein the allocated memory for the interleaver does not

exceed the maximum number of bytes in the message." Cooklev Report at ¶ 217-18 (internal citations omitted). None of these statements supports Dr. Cooklev's conclusion that Mazzoni does not disclose "a system that allocates shared memory." To the extent that Dr. Cooklev elaborates on these arguments with respect to these elements, I address them below.

135. As I explained in my Opening Report (*see* Jacobsen Opening Report at ¶¶ 249-56, 260), Mazzoni explicitly discloses "shared memory" as construed by the Court, i.e., "common memory used by at least two functions, where a portion of the memory can be used by either one of the functions." Mazzoni discloses that it provides a memory that "can be shared between the interleaving means and the deinterleaving means, and whose memory allocation can be reconfigured in accordance with the bit rate actually processed by the send/receive device (modem)." Mazzoni at col. 1:59-65. Furthermore, claim 13 of Mazzoni recites "[a] method for sending and receiving digital data and processing different bit rates from a group of predetermined bit rates, the method comprising: interleaving and deinterleaving the digital data; *setting a minimum size of a shared memory based upon a maximum bit rate of the group of predetermined bit rates*; *assigning a first memory space of the shared memory for interleaving and a second memory space of the shared memory for deinterleaving, a size of each of the first and second memory spaces being set as a function of the bit rate actually processed by the device*; performing Reed-Solomon coding and decoding for a length N of the digital data; and the interleaving providing convolutional interleaving of I branches with i−1 blocks of M bytes, and the deinterleaving providing convolutional deinterleaving with I′ branches of i′−1 blocks of M′ bytes, with I and I′ being sub-multiples of N and i and i′ being current relative indexes of the branches." *Id.* at col. 10:22-42.

136. Thus, having considered Dr. Cooklev's arguments to the contrary, it remains my opinion that Mazzoni in combination with LB-031 discloses common memory used by an interleaver and a deinterleaver, where a portion of the memory can be used by either one of the two functions.

b. 1[b]. "a transceiver that is capable of"

137. Dr. Cooklev concedes that Mazzoni in combination with LB-031 discloses a transceiver. *See, e.g.*, Cooklev Report at ¶¶ 193-264.

c. 1[c]. "transmitting or receiving a message during initialization specifying a maximum number of bytes of memory that are available to be allocated to an interleaver"

138. Dr. Cooklev disputes that LB-031 in combination with Mazzoni discloses "transmitting or receiving a message during initialization specifying a maximum number of bytes of memory that are available to be allocated to an interleaver." Cooklev Report at ¶ 220-23.

139. In his discussion of LB-031 alone, Dr. Cooklev conceded that LB-031 discloses this limitation. *See* Cooklev Report at ¶¶ 90-192 (no dispute that LB-031 discloses transmitting or receiving a message during initialization specifying a maximum number of bytes of memory that are available to be allocated to an interleaver). Therefore, LB-031 in combination with Mazzoni discloses it as well, at least within the interpretation of the claim language advanced by TQ Delta in its infringement case.

140. Throughout his argument with respect to this limitation, (*see* Cooklev Report at ¶¶ 220-22), Dr. Cooklev argues, incorrectly, that I contend that the transceivers of Mazzoni exchange the parameters I, M, I′ and M′ during initialization. Dr. Cooklev is wrong and, in fact, acknowledges that I stated multiple times in my Opening Report that the transceivers of Mazzoni store the values of I, M, I′ and M′ in tables. *See, e.g.*, Cooklev Report at ¶ 221.

141. At paragraph 220, Dr. Cooklev quotes a sentence from paragraph 269 of my report: "One of ordinary skill in the art would have understood that the bit rate information, as well as capabilities of the transceiver at the other end of the system, would have to be conveyed, for example, in the form of a message during initialization, as is described in LB-031." Cooklev Report at ¶ 220. Dr. Cooklev then states that "[t]he 'information' she is referring to is the parameters I, M, I′ and M′ ." As the quoted sentence from my Opening Report itself indicates, Dr. Cooklev is incorrect. The "information" is, as the sentence states, "bit rate information." *See* Jacobsen Opening Report at ¶ 269. As I explained in my Opening Report (*see id.*), Mazzoni discloses that the interleaver/deinterleaver memory has a memory allocation that "can be reconfigured in accordance with the bit rate actually processed by the send/receive device (modem)." Mazzoni, col. 1:61-65. Furthermore, Mazzoni discloses that "the sizes of the respective memory spaces assigned to the interleaving means and to the deinterleaving means" are determined "according to the bit rate of the information sent by the terminal TO (parameters I and M) and the bit rate of the information received by the terminal TO (parameters I′ and M′)." *Id.* at col. 5:24-31. Thus, the size of the memory space, determined according to the values of I, M, I′ and M′ stored in the table, is selected based on the bit rate. *Id.* at col. 6:26-30. It is that bit rate which I stated would be provided during initialization.

142. Again in paragraph 221, Dr. Cooklev responds to an argument that I did not make, namely, that the transceivers of Mazzoni exchange the values of I, M, I′ and M′ during initialization.

143. Dr. Cooklev notes that the "bit rate actually processed by the send/receive device (modem)" of Mazzoni is one of the "predetermined bit rates." Cooklev Report at ¶ 222. I do not disagree, nor did I say anything inconsistent with this statement in my Opening Report.

Furthermore, this point is irrelevant because, as a skilled artisan would have understood, the transceivers of Mazzoni would select one of the predetermined bit rates during the initialization procedure, based on the conditions on the subscriber line. Mazzoni distinguishes between "symmetrical services" and "asymmetrical services." *See, e.g.*, Mazzoni at col. 3:62-4:14. As an example, Mazzoni contemplates six symmetrical services and six asymmetrical services. *Id.* One of Mazzoni's objectives is "to provide such an architecture which is adaptable, particularly in terms of the memory capacity of the interleaving and deinterleaving means, to suit a number of different bit rates selected from a predetermined group of bit rates." *Id.* at col. 1:54-58. As a person having ordinary skill would have understood from these disclosures, the "service actually provided by the operator," (Mazzoni at col. 6:55-59), would be either the "symmetrical service" or the "asymmetrical service," and the "bit rate actually processed by the send/receive device (modem)" would be one of the predetermined bit rates defined for, respectively, either the "symmetrical" or "asymmetrical" services. The bit rate actually processed would be determined during initialization on the basis of the capabilities of the transceivers, at least some of which would have to be conveyed, for example, in the form of a message during initialization.

144. Dr. Cooklev asserts that "LB-031's exchange of interleaver and deinterleaver capabilities would be useless and incompatible with Mazzoni." As I explained above (*see supra*, § VII.C.1), I disagree. A skilled artisan would have recognized the benefits of modifying Mazzoni to incorporate the initialization message of LB-031 to obviate the need for all asymmetrical and symmetrical services to be predefined and for the transceiver to store a table indicating the values of I, M, I′ and M′ for each of the predefined bit rates.

145. Thus, having considered Dr. Cooklev's opinion to the contrary, it remains my opinion that LB-031 in combination with Mazzoni discloses transmitting or receiving a message during initialization specifying a maximum number of bytes of memory that are available to be allocated to an interleaver, within the interpretation of this limitation that has been advanced by TQ Delta in its infringement case.

d. 1[d]. "determining an amount of memory required by the interleaver to interleave a first plurality of Reed Solomon (RS) coded data bytes within the shared memory"

146. Dr. Cooklev disputes that LB-031 in combination with Mazzoni discloses "determining an amount of memory required by the interleaver to interleave a first plurality of Reed Solomon (RS) coded data bytes within the shared memory." Cooklev Report at ¶ 224. Dr. Cooklev argues that the values of I, M, I′ and M′ are "predetermined, stored in a table, and retrieved for use at the time of installation of the transceiver." *Id.* Although Dr. Cooklev is correct that the values of I, M, I′ and M′ are stored in a table, the transceiver must still determine an amount of memory required for the interleaver to interleave a first plurality of RS coded data bytes within the shared memory. *See, e.g.*, Mazzoni at col. 7:52-8:10 ("the second address determination means MD2 must allow for the size OF of the first memory space ESM1, which is defined by the equation (1) below: $OF = I \times (I\text{-}1) \times M/2$, and may be stored in a register, for example. For uplink interleaving, the address of the memory MM vary in the range of 0 to OF-1."). Even if the size OF were pre-stored in a register, the transceiver would still need to read that register in order to divide the memory space of the memory MM "into a first memory space ESM1 assigned to the interleaving means MET, and a second memory space ESM2 [] assigned to the deinterleaving means MDET." Mazzoni at col. 5:64-67. This register read would itself be "determining an amount of memory required by the interleaver to interleave a first plurality of Reed Solomon (RS) coded data bytes within the shared memory." Implicit in Dr. Cooklev's

argument is that "determining," as used in this claim limitation, must mean "calculating." This interpretation is not supported by the intrinsic record, nor is it consistent with the way one of ordinary skill in the art would understand the claim language.

147. Without any citation to Mazzoni, Dr. Cooklev suggests that Mazzoni contemplates that "all necessary information is stored prior to initialization." Cooklev Report at ¶ 225. I disagree. Although Mazzoni discloses storing the values of I, M, I′ and M′ in a table, Mazzoni does not disclose storing "all necessary information" prior to initialization, nor would a person having ordinary skill in the art expect it to do so. On the contrary, a skilled artisan would understand establishment of a DSL connection requires much more information than simply the values of I, M, I′ and M′, and that some of this information cannot be determined until the initialization procedure is being performed.

148. Dr. Cooklev states, again, that "a POSITA would be discouraged from combining the teaching of LB-031 with the teachings of Mazzoni." Cooklev Report at ¶ 227. As I explained above (*see supra*, § VII.C.1) and in my Opening Report (*see, e.g.*, Jacobsen Opening Report at ¶ 595), a skilled artisan would have recognized the benefits of modifying Mazzoni to incorporate initialization messages, such as the initialization message of LB-031, to obviate the need for all asymmetrical and symmetrical services to be predefined and for the transceiver to store a table indicating the values of I, M, I′ and M′ for each of the predefined bit rates.

149. Thus, having considered Dr. Cooklev's opinion to the contrary, it remains my opinion that LB-031 in combination with Mazzoni discloses determining an amount of memory required by the interleaver to interleave a first plurality of Reed Solomon (RS) coded data bytes within the shared memory.

e. 1[e]. and 1[f] "allocating a first number of bytes of the shared memory to the interleaver to interleave the first plurality of Reed Solomon (RS) coded data bytes for transmission at a first data rate wherein the allocated memory for the interleaver does not exceed the maximum number of bytes in the message"

150. Dr. Cooklev disputes that LB-031 in combination with Mazzoni discloses "allocating a first number of bytes of the shared memory to the interleaver to interleave the first plurality of Reed Solomon (RS) coded data bytes for transmission at a first data rate, wherein the allocated memory for the interleaver does not exceed the maximum number of bytes in the message," at least within the interpretation of this claim language that has been offered by TQ Delta in its infringement case. Cooklev Report at ¶ 228-30. Dr. Cooklev asserts that LB-031 does not disclose this limitation because LB-031 does not, in his opinion, disclose shared memory. Cooklev Report at ¶ 228. I explained above why I disagree with Dr. Cooklev. *See supra*, § VII.B.1.a.

151. Dr. Cooklev argues that "LB-031's exchange of interleaver and deinterleaver capabilities is redundant to Mazzoni's stored predefined service data rates and interleaver/deinterleaver parameters and incompatible with Mazzoni at least because the exchange of maximum supported interleaver and deinterleaver sizes per LB-031 would specify a combined amount of interleaver and deinterleaver memory that would exceed Mazzoni's total memory size." Cooklev Report at ¶ 229. I disagree. As I explained above, (*see supra*, § VII.C.1), it remains my opinion that a skilled artisan would have been motivated to combine the teachings of LB-031 and the teachings of Mazzoni to improve the flexibility of Mazzoni's transceiver and to obviate the need to predefine all services.

152. Therefore, having considered Dr. Cooklev's opinion to the contrary, it remains my opinion that LB-031 and Mazzoni disclose allocating a first number of bytes of the shared

memory to the interleaver to interleave the first plurality of Reed Solomon (RS) coded data bytes for transmission at a first data rate.

153. Dr. Cooklev disputes that LB-031 in combination with Mazzoni discloses that the allocated memory for the interleaver does not exceed the maximum number of bytes in the message. Cooklev Report at ¶ 230. I disagree. As my Opening Report indicates, the primary basis for my opinion that LB-031 in combination with Mazzoni discloses this limitation is the content of LB-031. *See* Jacobsen Opening Report at ¶ 282. Dr. Cooklev's focus on Mazzoni is misplaced.

154. Therefore, having considered Dr. Cooklev's opinion to the contrary, it remains my opinion that LB-031 and Mazzoni disclose wherein the allocated memory for the interleaver does not exceed the maximum number of bytes in the message, according to the interpretation of the claim advanced by TQ Delta in its infringement case.

f. 1[g]. "allocating a second number of bytes of the shared memory to a deinterleaver to deinterleave a second plurality of RS coded data bytes received at a second data rate"

155. Dr. Cooklev concedes that LB-031 in combination with Mazzoni discloses "allocating a second number of bytes of the shared memory to a deinterleaver to deinterleave a second plurality of RS coded data bytes received at a second data rate." *See* Cooklev Report at ¶¶ 215-30.

g. 1[h]. "interleaving the first plurality of RS coded data bytes within the shared interleaver memory allocated to the interleaver and deinterleaving the second plurality of RS coded data bytes within the shared memory allocated to the deinterleaver"

156. Dr. Cooklev concedes that LB-031 in combination with Mazzoni discloses "interleaving the first plurality of RS coded data bytes within the shared interleaver memory allocated to the interleaver and deinterleaving the second plurality of RS coded data bytes within the shared memory allocated to the deinterleaver." *See* Cooklev Report at ¶¶ 215-30.

h. 1[i]. "wherein the shared memory allocated to the interleaver is used at the same time as the shared memory allocated to the deinterleaver"

157. Dr. Cooklev concedes that LB-031 in combination with Mazzoni discloses "wherein the shared memory allocated to the interleaver is used at the same time as the shared memory allocated to the deinterleaver." *See* Cooklev Report at ¶¶ 215-30.

158. Thus, having considered Dr. Cooklev's argument to the contrary, it remains my opinion that LB-031 in combination with Mazzoni discloses all of the limitations of claim 1 of the '048 patent.

3. Claim 5 of the '381 Patent

159. Having considered Dr. Cooklev's arguments to the contrary, it remains my opinion that claim 5 of the '381 patent is rendered obvious by LB-031 in combination with Mazzoni.

160. I incorporate by reference my discussion and opinion in § VII.C.1 regarding why a person having ordinary skill in the art would have been motivated to combine the disclosures of LB-031 and Mazzoni.

a. 5[a]. "A non-transitory computer-readable information storage media having stored thereon instructions, that if executed by a processor, cause to be performed a method for allocating shared memory in a transceiver"

161. Dr. Cooklev disputes that LB-031 in combination with Mazzoni discloses "[a] non-transitory computer-readable information storage media having stored thereon instructions, that if executed by a processor, cause to be performed a method for allocating shared memory in a transceiver." Cooklev Report at ¶ 232. I disagree.

162. Dr. Cooklev argues that LB-031 "does not disclose the exchange of information that would be useful for allocating shared memory." Cooklev Report at ¶ 233. As an initial matter, Dr. Cooklev conceded that LB-031 discloses "transmitting or receiving a message

during initialization specifying a maximum number of bytes of memory that are available to be allocated to an interleaver." *See supra*, § VII.B.1.c. Furthermore, as I explained above, (*see, e.g.*, *supra* § VII.B.1.a, § VII.B.1.e), LB-031 discloses allocating shared memory.

163. Dr. Cooklev also argues that the information exchanged by the VTU-O and VTU-R in LB-031 "could not be used by a Mazzoni transceiver to allocate shared memory." As I explained above (*see supra* § VII.C.1), I disagree.

164. Dr. Cooklev appears to assert that because "one or more of the claimed functions could be implemented in hardware, and therefore would not necessarily have to be carried out through an execution of instructions stored on a non-transitory computer-readable media," neither LB-031 nor Mazzoni discloses the preamble of claim 5. Cooklev Report at ¶ 237. I disagree. First, according to Dr. Cooklev, "a POSITA at the time of the invention had (i) a Bachelor's degree in Electrical Engineering or a related field, and (ii) two to three years' of experience working in DSL or other broadband communications (or a Master's Degree in Electrical Engineering or a related field, particularly with an emphasis in the area of communications)." Cooklev Opening Infringement Report at ¶ 27. A person having the level of skill suggested by Dr. Cooklev would have understood that transceivers include hardware and software, and therefore the universe of ways to implement a transceiver as taught by LB-031 and as taught by Mazzoni extends to hardware, software, or some combination of the two. That LB-031 or Mazzoni does not explicitly refer to a particular approach does not mean that a skilled artisan would not have understood that approach to be disclosed.

165. Furthermore, with respect to Mazzoni in particular, as Dr. Cooklev stated in his discussion on written description and enablement, "a patent need not teach, and preferably omits, what is well known in the art." Cooklev Report at ¶ 80. Thus, Dr. Cooklev agrees that

"it was not necessary [for Mazzoni] to provide a full and detailed explanation where, as here, a POSITA would know how to implement the claim." *Id.*

166. Thus, having considered Dr. Cooklev's opinion to the contrary, it remains my opinion that LB-031 in combination with Mazzoni discloses "[a] non-transitory computer-readable information storage media having stored thereon instructions, that if executed by a processor, cause to be performed a method for allocating shared memory in a transceiver."

b. 5[b]. "transmitting or receiving, by the transceiver, a message during initialization specifying a maximum number of bytes of memory that are available to be allocated to a deinterleaver"

167. Dr. Cooklev purports to dispute that LB-031 in combination with Mazzoni discloses "transmitting or receiving, by the transceiver, a message during initialization specifying a maximum number of bytes of memory that are available to be allocated to a deinterleaver." Cooklev Report at ¶ 241. As an initial matter, Dr. Cooklev conceded that LB-031 discloses this limitation under TQ Delta's interpretation. *See, e.g.*, Cooklev Report at ¶¶ 90-192; *see also supra*, § VII.B.2.b. Yet Dr. Cooklev argues that LB-031 in combination with Mazzoni somehow does not disclose this limitation because (a) "Mazzoni does not disclose exchanging any messages at all that include information about interleaving or deinterleaving parameters," (b) "Mazzoni does not describe any message specifying an amount of memory that can be allocated to an interleaver or to a deinterleaver," and (c) "LB-031's exchange of interleaver and deinterleaver capabilities would be useless and incompatible with Mazzoni." Cooklev Report at ¶¶ 241-42. I disagree with Dr. Cooklev. As he acknowledged, LB-031 discloses this limitation, and therefore LB-031 in combination with Mazzoni does, too.

168. Thus, having considered Dr. Cooklev's opinion to the contrary, it remains my opinion that LB-031 in combination with Mazzoni discloses "transmitting or receiving, by the transceiver, a message during initialization specifying a maximum number of bytes of memory

that are available to be allocated to a deinterleaver," within the interpretation of the claim language advanced by TQ Delta in its infringement case.

c. 5[c]. "determining, at the transceiver, an amount of memory required by the deinterleaver to deinterleave a first plurality of Reed Solomon (RS) coded data bytes within a shared memory"

169. Dr. Cooklev disputes that LB-031 in combination with Mazzoni discloses "determining, at the transceiver, an amount of memory required by the deinterleaver to deinterleave a first plurality of Reed Solomon (RS) coded data bytes within a shared memory." Cooklev Report at ¶¶ 243-45. Dr. Cooklev's rebuttal refers to his arguments with respect to element 1[d]. I explained above (*see supra*, § VII.C.2.d) why I disagree with Dr. Cooklev.

170. Thus, having considered Dr. Cooklev's opinion to the contrary, it remains my opinion that LB-031 in combination with Mazzoni discloses "determining, at the transceiver, an amount of memory required by the deinterleaver to deinterleave a first plurality of Reed Solomon (RS) coded data bytes within a shared memory."

d. 5[d] and 5[e]. "allocating, in the transceiver, a first number of bytes of the shared memory to the deinterleaver to deinterleave a first plurality of Reed Solomon (RS) coded data bytes for transmission at a first data rate, wherein the allocated memory for the deinterleaver does not exceed the maximum number of bytes specified in the message"

171. Dr. Cooklev disputes that LB-031 in combination with Mazzoni discloses "allocating, in the transceiver, a first number of bytes of the shared memory to the deinterleaver to deinterleave a first plurality of Reed Solomon (RS) coded data bytes for transmission at a first data rate, wherein the allocated memory for the deinterleaver does not exceed the maximum number of bytes specified in the message." Cooklev Report at ¶¶ 246-48.

172. With respect to LB-031 alone, Dr. Cooklev's argument is that LB-031 does not disclose shared memory. I explained above (*see, e.g., supra*, § VII.B.1.a) why I disagree with Dr. Cooklev.

173. With respect to Mazzoni, Dr. Cooklev argues that "Mazzoni does not disclose transmitting or receiving any message with interleaver or deinterleaver parameters," and that "LB-031's exchange of interleaver and deinterleaver capabilities is redundant to Mazzoni's stored predefined service data rates and interleaver/deinterleaver parameters and incompatible with Mazzoni. . . ." Cooklev Report at ¶ 247. I explained above (*see, e.g., supra*, § VII.C.1) why I disagree with Dr. Cooklev's opinion. A skilled artisan wishing to implement the VDSL transceiver of Mazzoni would have recognized the inherent limitations of Mazzoni's table and the desirability of including the initialization message of LB-031 so that the VTU-O and VTU-R of Mazzoni could choose values for the parameters I, M, I′ and M′ that would not exceed the size of the shared memory at the selected downstream and upstream bit rates without the need to define all of the services in advance.

174. Thus, having considered Dr. Cooklev's opinion to the contrary, it remains my opinion that LB-031 in combination with Mazzoni discloses "allocating, in the transceiver, a first number of bytes of the shared memory to the deinterleaver to deinterleave a first plurality of Reed Solomon (RS) coded data bytes for transmission at a first data rate, wherein the allocated memory for the deinterleaver does not exceed the maximum number of bytes specified in the message," within the interpretation of this claim limitation advanced by TQ Delta in its infringement case.

e. 5[f]. "allocating, in the transceiver, a second number of bytes of the shared memory to an interleaver to interleave a second plurality of RS coded data bytes transmitted at a second data rate"

175. Dr. Cooklev concedes that LB-031 in combination with Mazzoni discloses "allocating, in the transceiver, a second number of bytes of the shared memory to an interleaver to interleave a second plurality of RS coded data bytes transmitted at a second data rate." Cooklev Report at ¶¶ 231-48.

f. 5[g]. "deinterleaving the first plurality of RS coded data bytes within the shared memory allocated to the deinterleaver and interleaving the second plurality of RS coded data bytes within the shared memory allocated to the interleaver"

176. Dr. Cooklev concedes that LB-031 in combination with Mazzoni discloses "deinterleaving the first plurality of RS coded data bytes within the shared memory allocated to the deinterleaver and interleaving the second plurality of RS coded data bytes within the shared memory allocated to the interleaver." Cooklev Report at ¶¶ 231-48.

g. 5[h]. "wherein the shared memory allocated to the deinterleaver is used at the same time as the shared memory allocated to the interleaver"

177. Dr. Cooklev concedes that LB-031 in combination with Mazzoni discloses "wherein the shared memory allocated to the deinterleaver is used at the same time as the shared memory allocated to the interleaver." Cooklev Report at ¶¶ 231-48.

178. Thus, having considered Dr. Cooklev's arguments to the contrary, it remains my opinion that LB-031 in combination with Mazzoni renders claim 5 of the '381 patent obvious.

4. Claim 13 of the '882 patent

179. Having considered Dr. Cooklev's arguments to the contrary, it remains my opinion that LB-031 in combination with Mazzoni renders claim 13 of the '882 patent obvious, as I explain below.

180. I incorporate by reference my discussion and opinion in § VII.C.1 regarding why a person having ordinary skill in the art would have been motivated to combine the disclosures of LB-031 and Mazzoni.

a. 13[a]. "A system that allocates shared memory"

181. Dr. Cooklev disputes that LB-031 in combination with Mazzoni discloses "[a] system that allocates shared memory." Cooklev Report at ¶ 250. I explained above (*see supra*, § VII.C.2.a) why I disagree with Dr. Cooklev.

182. Thus, having considered Dr. Cooklev's opinion to the contrary, it remains my opinion that LB-031 in combination with Mazzoni discloses a system that allocates shared memory.

b. 13[b]. "a transceiver that performs"

183. Dr. Cooklev concedes that LB-031 in combination with Mazzoni discloses a transceiver. *See* Cooklev Report at ¶¶ 249-54.

c. 13[c] through 13[i]

184. Dr. Cooklev adopts wholesale his arguments with respect to claim 5 of the '381 patent and claim 1 of the '048 patent as his argument with respect to elements 13[c] through 13[i] of claim 13 of the '882 patent, and does not make any additional arguments or express any additional opinions. Cooklev Report at ¶¶ 251-54. I do the same with respect to these claim elements. *See supra*, §§ VII.C.2, VII.C.3.b-VII.C.3.g.

185. Thus, having considered Dr. Cooklev's opinion to the contrary, it remains my opinion that LB-031 in combination with Mazzoni discloses all of the limitations of claim 13 of the '882 patent and, therefore, that LB-031 in combination with Mazzoni renders claim 13 obvious.

5. Claim 19 of the '473 Patent

186. Having considered Dr. Cookelv's opinion to the contrary, it remains my opinion that LB-031 in combination with Mazzoni renders claim 19 of the '473 patent obvious.

187. I incorporate by reference my discussion and opinion in § VII.C.1 regarding why a person having ordinary skill in the art would have been motivated to combine the disclosures of LB-031 and Mazzoni.

a. 19[a]. "An apparatus comprising"

188. Dr. Cooklev concedes that LB-031 in combination with Mazzoni discloses an apparatus. *See* Cooklev Report at ¶¶ 255-64.

b. 19[b]. "a multicarrier communications transceiver that is configured to perform an interleaving function associated with a first latency path and perform a deinterleaving function associated with a second latency path"

189. Dr. Cooklev concedes that LB-031 in combination with Mazzoni discloses "a multicarrier communications transceiver that is configured to perform an interleaving function associated with a first latency path and perform a deinterleaving function associated with a second latency path." *See* Cooklev Report at ¶¶ 255-64.

c. 19[c]. "the multicarrier communications transceiver being associated with a memory"

190. Dr. Cooklev concedes that LB-031 in combination with Mazzoni discloses a multicarrier communications transceiver that is associated with a memory. *See* Cooklev Report at ¶¶ 255-64.

d. 19[d]. "wherein the memory is allocated between the interleaving function and the deinterleaving function in accordance with a message received during an initialization of the transceiver"

191. Dr. Cooklev disputes that LB-031 in combination with Mazzoni discloses that "the memory is allocated between the interleaving function and the deinterleaving function in accordance with a message received during an initialization of the transceiver." Cooklev Report at ¶ 256.

192. Dr. Cooklev does not dispute that LB-031 discloses a message received during an initialization of the transceiver. *See* Cooklev Report at ¶¶ 256-60. He disputes only that LB-031 discloses shared memory and the allocation of the shared memory between the interleaving function and the deinterleaving function based on that message. *See* Cooklev Report at ¶¶ 256,

171-88. As I explained above (*see, e.g.*, *supra*, § VII.B.1.a), Dr. Cooklev's opinion is based on the erroneous assumption that a skilled artisan would not have understood the disclosures of LB-031 to apply regardless of whether an implementation uses dedicated or shared memory for interleaving and deinterleaving. As I explained in my Opening Report, one of ordinary skill in the art would have understood that LB-031 discloses allocating the memory between an interleaving function and a deinterleaving function based on the interleaver delay exchanged during initialization. Jacobsen Opening Report at ¶¶ 337-38.

193. Dr. Cooklev's rebuttal focuses on Mazzoni and the fact that the parameters I, M, I′ and M′ are predefined and stored in a table. Cooklev Report at ¶¶ 257-59. I explained in my Opening Report and above that a skilled artisan would have recognized the need to define all of the services ahead of time and store all of the values of I, M, I′ and M′ in a table to be a disadvantage of Mazzoni because it would limit the flexibility of the implementation.

194. Dr. Cooklev repeats his argument that "LB-031's exchange of interleaver and deinterleaver capabilities is redundant to Mazzoni's stored predefined service data rates and interleaver/deinterleaver parameters and incompatible with Mazzoni at least because the exchange of maximum supported interleaver and deinterleaver sizes per LB-031 would specify a combined amount of interleaver and deinterleaver memory that would exceed Mazzoni's total memory size." Cooklev Report at ¶ 260. I disagree. As I explained above, (*see supra*, § VII.C.1), it remains my opinion that a skilled artisan would have been motivated to combine the teachings of LB-031 and the teachings of Mazzoni to improve the flexibility of Mazzoni's transceiver and to obviate the need to predefine all services.

195. Thus, having considered Dr. Cooklev's opinion to the contrary, it remains my opinion that LB-031 in combination with Mazzoni discloses "wherein the memory is allocated

between the interleaving function and the deinterleaving function in accordance with a message received during an initialization of the transceiver."

e. 19[e]. "wherein at least a portion of the memory may be allocated to the interleaving function or the deinterleaving function at any one particular time depending on the message"

196. Dr. Cooklev disputes that LB-031 in combination with Mazzoni discloses that "at least a portion of the memory may be allocated to the interleaving function or the deinterleaving function at any one particular time depending on the message." Cooklev Report at ¶¶ 261-64.

197. Dr. Cooklev's argues that "Mazzoni does not disclose exchanging any messages at all that include information about interleaving or deinterleaving parameters (or any other information upon which interleaver or deinterleaver memory allocations could be based)." Cooklev Report at ¶ 263. I disagree. As I explained in my Opening Report (*see* Jacobsen Opening Report at ¶ 344), Mazzoni discloses that the interleaver/deinterleaver memory has a memory allocation that "can be reconfigured in accordance with the bit rate actually processed by the send/receive device (modem)." Mazzoni, col. 1:61-65. Furthermore, Mazzoni discloses that "the sizes of the respective memory spaces assigned to the interleaving means and to the deinterleaving means" are determined "according to the bit rate of the information sent by the terminal TO (parameters I and M) and the bit rate of the information received by the terminal TO (parameters I′ and M′)." *Id.* at col. 5:24-31. As a skilled artisan would have understood, the bit rate of the information would be determined during initialization on the basis of messages transmitted by the two transceivers.

198. Furthermore, and as I explained in my Opening Report (*see, e.g.*, Jacobsen Opening Report at § IX.B.7) and above (*see supra*, § VII.C.1), a skilled artisan would have been motivated to modify the transceiver of Mazzoni to incorporate the initialization message of LB-

031 to avoid the need to define all services to be provided by Mazzoni's transceiver in advance. As a result of this combination, the transceivers of Mazzoni would use the initialization messages of LB-031 to exchange capabilities such as, for example, maximum bit rate and the minimum interleaver delay. LB-031 at p. 4. Based on the minimum interleaver delay, the transceivers of Mazzoni would then be able to determine the minimum amount of memory required to support the target delay. LB-031 at p. 2. Based on this determination, the transceivers of Mazzoni would divide "[t]he memory space of the memory MM . . . into a first memory space ESM1 assigned to the interleaving means MET, and a second memory space ESM2 [] assigned to the deinterleaving means MDET." Mazzoni at col. 5:64-67.

199. Furthermore, Mazzoni describes that the second addressing determination means (for the deinterleaver) "must allow for the size OF of the first memory space ESM1" (i.e., for interleaving). Mazzoni further discloses that the size OF of the first memory space ESM1 is defined as $OF = I \times (I\text{-}1) \times M/2$. Thus, a skilled artisan would understand that depending on the values of the parameters I and M, which, per LB-031, would be exchanged during initialization, at least a portion of the memory may be allocated to the interleaving function or the deinterleaving function at any one particular time based on the messages exchanged during initialization. Consequently, in combination, LB-031 and Mazzoni disclose that at least a portion of the memory may be allocated to the interleaving function or the deinterleaving function at any one particular time depending on the message.

200. Thus, having considered Dr. Cooklev's opinion to the contrary, it remains my opinion that LB-031 in combination with Mazzoni discloses "wherein at least a portion of the memory may be allocated to the interleaving function or the deinterleaving function at any one

particular time depending on the message." In addition, it remains my opinion that LB-031 in combination with Mazzoni discloses all of the limitations of claim 19 of the '473 patent.

D. Fadavi-Ardekani in Combination With ITU-T Recommendation G.993.1 Renders the Asserted Claims Obvious

201. As explained below, having considered Dr. Cooklev's arguments to the contrary, it remains my opinion that Fadavi-Ardekani, in combination with G.993.1 renders obvious each of claim 1 of the '048 patent, claim 5 of the '381 patent, claim 13 of the '882 patent, and claim 19 of the '473 patent.

202. Dr. Cooklev notes that Fadavi-Ardekani was considered during prosecution of U.S. Patent No. 7,831,890 ("the '890 patent"). Cooklev Report at ¶ 265. As I explained in my Opening Report (*see* Jacobsen Opening Report at ¶ 139), the Examiner found, for example, that Fadavi-Ardekani teaches methods and systems for "sharing resources in a transceiver" comprising "allocating a first portion of shared memory to a first latency path (i.e., 16 Kbytes is allocated for interleave, lines 25-30 in column 7) and allocating a second portion of the shared memory to a second latency path (i.e., 4 Kbytes is allocated for deinterleave, lines 25-30 in column 7)." 12/9/2009 Office Action in App. No. 11/246,163 at 14, 16, 18-19. The Examiner also found that Fadavi-Ardekani teaches transmitting or receiving "information that is used to determine a maximum amount of shared memory that can be allocated." *Id*. at 15, 20. Finally, the Examiner found that Fadavi-Ardekani also teaches that the first latency path may include an interleaver and the second latency path may include either a second interleaver or a deinterleaver. *Id*. at 16, 19.

1. Claim 1 of the '048 Patent

203. Having considered Dr. Cooklev's arguments to the contrary, it remains my opinion that Fadavi-Ardekani in combination with G.993.1 renders claim 1 of the '048 patent obvious.

a. 1[a]. "A system that allocates shared memory"

204. Dr. Cooklev disputes that Fadavi-Ardekani in combination with G.993.1 discloses "[a] system that allocates shared memory." Cooklev Report at ¶¶ 271-75. Specifically, he contends that the Interleaver/De-Interleaver Memory (IDIM) of Fadavi-Ardekani is not "shared memory" and that the disclosure that the IDIM is used in a "ping-pang fashion" does not indicate that the IDIM is "shared memory." Cooklev Report at ¶¶ 271, 274.

205. Dr. Cooklev's argument appears to be that no portion of the IDIM of Fadavi-Ardekani is ever used at one time by an interleaver and at another time by a deinterleaver, i.e., that although Fadavi-Ardekani discloses a single IDIM, it actually provides dedicated interleaver memory and dedicated deinterleaver memory. I disagree, and I see nothing in Fadavi-Ardekani to suggest that there is any pre-set, immovable boundary between the portion of the IDIM used for interleaving and the portion of the IDIM used for deinterleaving. As the Examiner of the '890 patent's application found, Fadavi-Ardekani discloses shared memory as recited in the Family 3 patents' claims. 12/9/2009 Office Action in App. No. 11/246,163 at 15, 20. *See also, e.g.*, 9/28/2010 Office Action in App. No. 13/567,261 ('473 patent) at pp. 3-4 (stating that Fadavi-Ardekani discloses shared memory); 1/6/2001 Office Action in App. No. 12/901,699 ('048 patent) at pp. 6-9 (finding Fadavi-Ardekani to disclose all limitations of claims except "transmitting or receiving a message during initialization specifying a maximum number of bytes of memory that are available to be allocated to an interleaver").

206. Furthermore, as Dr. Cooklev acknowledges (see Cooklev Report at ¶ 275), Fadavi-Ardekani discloses an "optimal implementation" that "utilizes the same memory for receive data and transmit data." Fadavi-Ardekani at col. 7:25-27. This implementation is capable of supporting "a standard ADSL session at full interleave depth," and "[w]ith a lesser interleave depth, *additional sessions may be supported with the same size buffer*." *Id.* at col. 7:25-32 (emphasis added). As a skilled artisan would have understood, this disclosure means that the memory is flexibly allocated to different interleaving and deinterleaving functions based on the number of sessions and the interleave depth, which is incompatible with Dr. Cooklev's suggestion that the IDIM provides, in effect, dedicated memory for interleaving and dedicated memory for deinterleaving. Consequently, the IDIM of Fadavi-Ardekani is common memory used by at least two functions, where a portion of the memory can be used by either one of the functions, and is, therefore, "shared memory."

207. Without any support, Dr. Cooklev asserts that "[t]he optimal implementation [disclosed in Fadavi-Ardekani] is incompatible with the DSL standards." Cooklev Report at ¶ 275. On the contrary, Fadavi-Ardekani indicates that the optimal implementation is, in fact, compatible with at least T1.413-1998 (also known as T1.413 Issue 2). For example, Fadavi-Ardekani explains that "the central office of an ADSL communication system needs to support multiple ADSL lines," and that "[t]he invention provides an Asymmetric Digital Subscriber Line (ADSL) transceiver that manages multiple asynchronous ADSL sessions. . . ." Fadavi-Ardekani at col. 2:47-64. Nothing in Fadavi-Ardekani suggests that the optimal implementation would be in any way "incompatible with the DSL standards" as Dr. Cooklev states.

208. Thus, having considered Dr. Cooklev's opinion to the contrary, it remains my opinion that Fadavi-Ardekani in combination with G.993.1 discloses a system that allocates shared memory.

b. 1[b]. "a transceiver that is capable of"

209. Dr. Cooklev concedes that Fadavi-Ardekani in combination with G.993.1 discloses a transceiver. Cooklev Report at ¶¶ 271-80.

c. 1[c]. "transmitting or receiving a message during initialization specifying a maximum number of bytes of memory that are available to allocated to an interleaver"

210. Dr. Cooklev concedes that Fadavi-Ardekani in combination with G.993.1 discloses "transmitting or receiving a message during initialization specifying a maximum number of bytes of memory that are available to allocated to an interleaver." Cooklev Report at ¶¶ 271-80.

d. 1[d]. "determining an amount of memory required by the interleaver to interleave a first plurality of Reed-Solomon (RS) coded data bytes within the shared memory"

211. Dr. Cooklev concedes that Fadavi-Ardekani in combination with G.993.1 discloses "determining an amount of memory required by the interleaver to interleave a first plurality of Reed-Solomon (RS) coded data bytes within the shared memory." Cooklev Report at ¶¶ 271-80.

e. 1[e] and 1[f]. "allocating a first number of bytes of the shared memory to the interleaver to interleave the first plurality of Reed Solomon (RS) coded data bytes for transmission at a first rate, wherein the allocated memory for the interleaver does not exceed the maximum number of bytes specified in the message"

212. Dr. Cooklev disputes that Fadavi-Ardekani in combination with G.993.1 discloses "allocating a first number of bytes of the shared memory to the interleaver to interleave the first plurality of Reed Solomon (RS) coded data bytes for transmission at a first

rate, wherein the allocated memory for the interleaver does not exceed the maximum number of bytes specified in the message." Cooklev Report at ¶¶ 276-79.

213. In paragraph 276, Dr. Cooklev once again asserts, without any support, that "ADSL and G.Lite-compliant modems of that era" used only dedicated memory for interleaving and deinterleaving. I explained above (*see supra*, § VII.A.2) why I disagree with this assertion.

214. With respect to Fadavi-Ardekani, Dr. Cooklev argues that "no portion of the IDIM set aside for use [sic] the interleaving function will ever be allocated for use by the deinterleaving function, and vice versa," and that "there is no scenario where unused interleaving memory will be allocated for use by the deinterleaver, and vice versa." Cooklev Report at ¶ 277. I disagree. As I explained in my Opening Report and above (*see supra*, § VII.D.1.a), Fadavi-Ardekani indicates that the optimal implementation allows the shared memory to be allocated flexibly for interleaving and deinterleaving for multiple sessions.

215. Dr. Cooklev concedes in paragraph 278 of his report that Fadavi-Ardekani "teach[es] that 'with a lesser depth, additional sessions may be supported with the same size buffer,' and '[w]ith a larger buffer, additional session[s] may be supported,'" yet he then concludes that "this does not suggest that Fadavi allocates shared memory." On the contrary, allocating shared memory is exactly what it suggests. The Court construed "shared memory" as "common memory used by at least two functions, where a portion of the memory can be used by either one of the functions." Fadavi-Ardekani discloses that the "headend ADSL transceiver of the invention implements a buffering and scheduling scheme such that various transceiver components operate seamlessly . . . and share memory." Fadavi-Ardekani at col. 9:10-13. In addition, "the same memory may be used by each of multiple ADSL sessions and by both transmit processes and receive processes," which allows "a lesser number of transceivers, each

transceiver utilizing a lesser amount of memory . . . to implement an ADSL communication system according to the invention." *Id.* at col. 9:18-23.

216. Furthermore, Dr. Cooklev concedes that "Fadavi uses pre-determined amounts of memory *per session*." Cooklev Report at ¶ 278 (emphasis added). As a skilled artisan would have understood, the amount of memory needed for interleaving and deinterleaving can change from session to session depending on the selected interleaving parameters. Consequently, I disagree with Dr. Cooklev's statement that the disclosures of Fadavi-Ardekani "preclude[] any need to use the content of the O-MSG2 message to allocate memory." Cooklev Report at ¶ 278.

217. Thus, having considered Dr. Cooklev's opinion to the contrary, it remains my opinion that Fadavi-Ardekani in combination with G.993.1 discloses "allocating a first number of bytes of the shared memory to the interleaver to interleave the first plurality of Reed Solomon (RS) coded data bytes for transmission at a first rate, wherein the allocated memory for the interleaver does not exceed the maximum number of bytes specified in the message," at least within the interpretation of the claim language advanced by TQ Delta in its infringement case.

f. 1[g]. "allocating a second number of bytes of the shared memory to a deinterleaver to deinterleave a second plurality of RS coded data bytes received at a second data rate"

218. Dr. Cooklev disputes that Fadavi-Ardekani in combination with G.993.1 discloses "allocating a second number of bytes of the shared memory to a deinterleaver to deinterleave a second plurality of RS coded data bytes received at a second data rate." Cooklev Report at ¶ 280. Dr. Cooklev refers to his argument with respect to elements 1[e] and 1[f]. *Id.* I explained above (*see supra*, § VII.D.1.e) why I disagree with Dr. Cooklev's position, and I incorporate that discussion and my opinion here.

219. Thus, having considered Dr. Cooklev's opinion to the contrary, it remains my opinion that Fadavi-Ardekani in combination with G.993.1 discloses "allocating a second number of bytes of the shared memory to a deinterleaver to deinterleave a second plurality of RS coded data bytes received at a second data rate."

g. 1[h]. "interleaving the first plurality of RS coded data bytes within the shared memory allocated to the interleaver and deinterleaving the second plurality of RS coded data bytes within the shared memory allocated to the deinterleaver"

220. Dr. Cooklev concedes that Fadavi-Ardekani in combination with G.993.1 discloses "interleaving the first plurality of RS coded data bytes within the shared memory allocated to the interleaver and deinterleaving the second plurality of RS coded data bytes within the shared memory allocated to the deinterleaver." Cooklev Report at ¶¶ 271-80.

h. 1[i]. "wherein the shared memory allocated to the interleaver is used at the same time as the shared memory allocated to the deinterleaver"

221. Dr. Cooklev concedes that Fadavi-Ardekani in combination with G.993.1 discloses "wherein the shared memory allocated to the interleaver is used at the same time as the shared memory allocated to the deinterleaver." Cooklev Report at ¶¶ 271-80.

222. Thus, having considered Dr. Cooklev's argument to the contrary, it remains my opinion that Fadavi-Ardekani in combination with G.993.1 discloses all of the limitations of claim 1 of the '048 patent.

2. Claim 5 of the '381 Patent

223. Having considered Dr. Cooklev's argument to the contrary, it remains my opinion that Fadavi-Ardekani in combination with G.993.1 renders claim 5 of the '381 patent obvious.

a. 5[a]. "A non-transitory computer-readable information storage media having stored thereon instructions, that if executed by a

processor, cause to be performed a method for allocating shared memory in a transceiver"

224. Dr. Cooklev disputes that Fadavi-Ardekani in combination with G.993.1 discloses "[a] non-transitory computer-readable information storage media having stored thereon instructions, that if executed by a processor, cause to be performed a method for allocating shared memory in a transceiver." Cooklev Report at ¶ 281. Dr. Cooklev's argument is that Fadavi-Ardekani does not disclose "shared memory," and therefore it cannot disclose element 5[a]. *Id.*

225. I disagree. As I explained above (*see supra*, § VII.D.1.a), Fadavi-Ardekani discloses "shared memory," i.e., "common memory used by at least two functions, where a portion of the memory can be used by either one of the functions."

226. Furthermore, with respect to Fadavi-Ardekani in particular, as Dr. Cooklev stated in his discussion on written description and enablement, "a patent need not teach, and preferably omits, what is well known in the art." Cooklev Report at ¶ 80. Thus, Dr. Cooklev agrees that "it was not necessary [for Fadavi-Ardekani] to provide a full and detailed explanation where, as here, a POSITA would know how to implement the claim." *Id.*

227. Thus, having considered Dr. Cooklev's opinion to the contrary, it remains my opinion that Fadavi-Ardekani in combination with G.993.1 discloses "[a] non-transitory computer-readable information storage media having stored thereon instructions, that if executed by a processor, cause to be performed a method for allocating shared memory in a transceiver."

b. 5[b]. "transmitting or receiving, by the transceiver, a message during initialization specifying a maximum number of bytes of memory that are available to be allocated to a deinterleaver"

228. Dr. Cooklev concedes that Fadavi-Ardekani in combination with G.993.1 discloses "transmitting or receiving, by the transceiver, a message during initialization specifying a maximum number of bytes of memory that are available to be allocated to a deinterleaver," within the interpretation of this limitation advanced by TQ Delta in its infringement case. Cooklev Report at ¶¶ 281-83.

c. 5[c]. "determining, at the transceiver, an amount of memory required by the deinterleaver to deinterleave a first plurality of Reed Solomon (RS) coded data bytes within a shared memory"

229. Dr. Cooklev concedes that Fadavi-Ardekani in combination with G.993.1 discloses "determining, at the transceiver, an amount of memory required by the deinterleaver to deinterleave a first plurality of Reed Solomon (RS) coded data bytes within a shared memory." Cooklev Report at ¶¶ 281-83.

d. 5[d] and 5[e]. "allocating, in the transceiver, a first number of bytes of the shared memory to the deinterleaver to deinterleave a first plurality of Reed Solomon (RS) coded data bytes for transmission at a first data rate, wherein the allocated memory for the deinterleaver does not exceed the maximum number of bytes specified in the message"

230. Dr. Cooklev disputes that Fadavi-Ardekani in combination with G.993.1 discloses "allocating, in the transceiver, a first number of bytes of the shared memory to the deinterleaver to deinterleave a first plurality of Reed Solomon (RS) coded data bytes for transmission at a first data rate, wherein the allocated memory for the deinterleaver does not exceed the maximum number of bytes specified in the message." Cooklev Report at ¶ 282. Dr. Cooklev cites his argument with respect to elements 1[e] and 1[f] of the '048 patent and argues, again, that neither Fadavi-Ardekani nor G.993.1 discloses "shared memory." *Id.*

231. I disagree. As I explained above (*see supra*, §§ VII.D.1.a, VII.D.1.e), Fadavi-Ardekani discloses shared memory, and Fadavi-Ardekani in combination with G.993.1 discloses elements 1[e] and 1[f], which are the same as elements 5[d] and 5[e] except for reciting an interleaver instead of a deinterleaver. Furthermore, Dr. Cooklev does not dispute that G.993.1 discloses the message of claim 5, i.e., a message transmitted or received during initialization specifying a maximum number of bytes of memory that are available to be allocated to a deinterleaver. *See* Cooklev Report at ¶¶ 265-301.

232. Thus, having considered Dr. Cooklev's opinion to the contrary, it remains my opinion that Fadavi-Ardekani in combination with G.993.1 discloses "allocating, in the transceiver, a first number of bytes of the shared memory to the deinterleaver to deinterleave a first plurality of Reed Solomon (RS) coded data bytes for transmission at a first data rate, wherein the allocated memory for the deinterleaver does not exceed the maximum number of bytes specified in the message," as that limitation is interpreted by TQ Delta in its infringement case.

e. 5[f]. "allocating, in the transceiver, a second number of bytes of the shared memory to an interleaver to interleave a second plurality of RS coded data bytes transmitted at a second data rate"

233. Dr. Cooklev disputes that Fadavi-Ardekani in combination with G.993.1 discloses "allocating, in the transceiver, a second number of bytes of the shared memory to an interleaver to interleave a second plurality of RS coded data bytes transmitted at a second data rate." Cooklev Report at ¶ 283. Dr. Cooklev merely references his argument with respect to elements 1[e] and 1[f]. *Id.* I explained above (*see supra*, § VII.D.1.e) why I disagree with Dr. Cooklev.

234. Thus, having considered Dr. Cooklev's argument to the contrary, it remains my opinion that Fadavi-Ardekani in combination with G.993.1 discloses "allocating, in the

transceiver, a second number of bytes of the shared memory to an interleaver to interleave a second plurality of RS coded data bytes transmitted at a second data rate."

f. 5[g]. "deinterleaving the first plurality of RS coded data bytes within the shared memory allocated to the deinterleaver and interleaving the second plurality of RS coded data bytes within the shared memory allocated to the interleaver"

235. Dr. Cooklev concedes that Fadavi-Ardekani in combination with G.993.1 discloses "deinterleaving the first plurality of RS coded data bytes within the shared memory allocated to the deinterleaver and interleaving the second plurality of RS coded data bytes within the shared memory allocated to the interleaver." Cooklev Report at ¶¶ 281-83.

g. 5[h]. "wherein the shared memory allocated to the deinterleaver is used at the same time as the shared memory allocated to the interleaver"

236. Dr. Cooklev concedes that Fadavi-Ardekani in combination with G.993.1 discloses "wherein the shared memory allocated to the deinterleaver is used at the same time as the shared memory allocated to the interleaver." Cooklev Report at ¶¶ 281-83.

237. Thus, having considered Dr. Cooklev's argument to the contrary, it remains my opinion that Fadavi-Ardekani in combination with G.993.1 discloses all of the limitations of claim 5 of the '381 patent.

3. Claim 13 of the '882 patent

238. Having considered Dr. Cooklev's argument to the contrary, it remains my opinion that Fadavi-Ardekani in combination with G.993.1 renders claim 13 of the '882 patent obvious.

a. 13[a]. "A system that allocates shared memory"

239. Dr. Cooklev disputes that Fadavi-Ardekani in combination with G.993.1 discloses "[a] system that allocates shared memory." Cooklev Report at ¶ 284. Dr. Cooklev

merely references his argument with respect to element 1[a] of the '048 patent. *Id.* I explained above (*see supra*, § VII.D.1.a) why I disagree with Dr. Cooklev.

240. Thus, having considered Dr. Cooklev's argument to the contrary, it remains my opinion that Fadavi-Ardekani in combination with G.993.1 discloses a system that allocates shared memory.

b. 13[b]. "a transceiver"

241. Dr. Cooklev concedes that Fadavi-Ardekani in combination with G.993.1 discloses a transceiver. Cooklev Report at ¶¶ 284-86.

c. 13[c]. "transmitting or receiving a message during initialization specifying a maximum number of bytes of memory that are available to be allocated to a deinterleaver"

242. Dr. Cooklev concedes that Fadavi-Ardekani in combination with G.993.1 discloses "transmitting or receiving a message during initialization specifying a maximum number of bytes of memory that are available to be allocated to a deinterleaver," at least within the interpretation of this claim language advanced by TQ Delta in its infringement reports. Cooklev Report at ¶¶ 284-86.

d. 13[d]. "determining an amount of memory required by the deinterleaver to deinterleave a first plurality of Reed Solomon (RS) coded data bytes within a shared memory"

243. Dr. Cooklev concedes that Fadavi-Ardekani in combination with G.993.1 discloses "determining an amount of memory required by the deinterleaver to deinterleave a first plurality of Reed Solomon (RS) coded data bytes within a shared memory." Cooklev Report at ¶¶ 284-86.

e. 13[e], and 13[f]. "allocating a first number of bytes of the shared memory to the deinterleaver to deinterleave a first plurality of Reed Solomon (RS) coded data bytes for reception at a first data rate, wherein the allocated memory for the deinterleaver does not exceed the maximum number of bytes specified in the message"

244. Dr. Cooklev disputes that Fadavi-Ardekani in combination with G.993.1 discloses "allocating a first number of bytes of the shared memory to the deinterleaver to deinterleave a first plurality of Reed Solomon (RS) coded data bytes for reception at a first data rate, wherein the allocated memory for the deinterleaver does not exceed the maximum number of bytes specified in the message." Cooklev Report at ¶ 285. Dr. Cooklev merely references his argument with respect to elements 1[e] and 1[f] of the '048 patent. *Id.* I explained above (*see supra*, § VII.D.1.e) why I disagree with Dr. Cooklev.

245. Thus, having considered Dr. Cooklev's argument to the contrary, it remains my opinion that Fadavi-Ardekani in combination with G.993.1 discloses "allocating a first number of bytes of the shared memory to the deinterleaver to deinterleave a first plurality of Reed Solomon (RS) coded data bytes for reception at a first data rate, wherein the allocated memory for the deinterleaver does not exceed the maximum number of bytes specified in the message," at least within TQ Delta's interpretation of this claim language in its infringement case.

f. 13[g]. "allocating a second number of bytes of the shared memory to an interleaver to interleave a second plurality of RS coded data bytes transmitted at a second data rate"

246. Dr. Cooklev disputes that Fadavi-Ardekani in combination with G.993.1 discloses "allocating a second number of bytes of the shared memory to an interleaver to interleave a second plurality of RS coded data bytes transmitted at a second data rate." Cooklev Report at ¶¶ 286. Dr. Cooklev merely references his argument with respect to elements 1[e] and 1[f] of the '048 patent. *Id.* I explained above (*see supra*, § VII.D.1.e) why I disagree with Dr. Cooklev.

247. Thus, having considered Dr. Cooklev's argument to the contrary, it remains my opinion that Fadavi-Ardekani in combination with G.993.1 discloses "allocating a second number of bytes of the shared memory to an interleaver to interleave a second plurality of RS coded data bytes transmitted at a second data rate."

g. 13[h]. "deinterleaving the first plurality of RS coded data bytes within the shared memory allocated to the deinterleaver and interleaving the second plurality of RS coded data bytes within the shared memory allocated to the interleaver"

248. Dr. Cooklev concedes that Fadavi-Ardekani in combination with G.993.1 discloses "deinterleaving the first plurality of RS coded data bytes within the shared memory allocated to the deinterleaver and interleaving the second plurality of RS coded data bytes within the shared memory allocated to the interleaver." Cooklev Report at ¶¶ 284-86.

h. 13[i]. "wherein the shared memory allocated to the deinterleaver is used at the same time as the shared memory allocated to the interleaver"

249. Dr. Cooklev concedes that Fadavi-Ardekani in combination with G.993.1 discloses "wherein the shared memory allocated to the deinterleaver is used at the same time as the shared memory allocated to the interleaver." Cooklev Report at ¶¶ 284-86.

250. Thus, having considered Dr. Cooklev's argument to the contrary, it remains my opinion that Fadavi-Ardekani in combination with G.993.1 discloses all of the limitations of claim 13 of the '882 patent.

Claim 19 of the '473 Patent

251. Having considered Dr. Cooklev's arguments to the contrary, it remains my opinion that Fadavi-Ardekani in combination with G.993.1 renders claim 19 of the '473 patent obvious.

a. 19[a]. "An apparatus comprising"

252. Dr. Cooklev concedes that Fadavi-Ardekani in combination with G.993.1 discloses an apparatus. Cooklev Report at ¶¶ 287-94.

b. 19[b]. "a multicarrier communications transceiver that is configured to perform an interleaving function associated with a first latency path and perform a deinterleaving function associated with a second latency path"

253. Dr. Cooklev concedes that Fadavi-Ardekani in combination with G.993.1 discloses "a multicarrier communications transceiver that is configured to perform an interleaving function associated with a first latency path and perform a deinterleaving function associated with a second latency path." Cooklev Report at ¶¶ 287-94.

c. 19[c]. "the multicarrier communications transceiver being associated with a memory"

254. Dr. Cooklev concedes that Fadavi-Ardekani in combination with G.993.1 discloses that the multicarrier communications transceiver is associated with a memory. Cooklev Report at ¶¶ 287-94.

d. 19[d]. "wherein the memory is allocated between the interleaving function and the deinterleaving function in accordance with a message received during an initialization of the transceiver"

255. Dr. Cooklev disputes that Fadavi-Ardekani in combination with G.993.1 discloses that "the memory is allocated between the interleaving function and the deinterleaving function in accordance with a message received during an initialization of the transceiver." Cooklev Report at ¶ 287. Dr. Cooklev contends that in Fadavi-Ardekani, "[t]he interleaver is assigned a pre-determined amount of memory[,] the size of which 'is derived by multiplying the maximum codeword length by the maximum interleaver depth.'" *Id.* at ¶ 288 (quoting Fadavi-Ardekani at col. 7:5-10). I disagree. The calculation to which Dr. Cooklev refers is to determine the total amount of memory to provide in an implementation. Immediately after

disclosing how to determine the total amount of memory to provide, and as Dr. Cooklev acknowledges elsewhere in his report (*see* Cooklev Report at ¶ 275), Fadavi-Ardekani discloses an "optimal implementation" that "utilizes the same memory for receive data and transmit data." Fadavi-Ardekani at col. 7:25-27. This implementation is capable of supporting "a standard ADSL session at full interleave depth," and "[w]ith a lesser interleave depth, *additional sessions may be supported with the same size buffer*." *Id.* at col. 7:25-32 (emphasis added). As a skilled artisan would have understood, this disclosure means that the memory is flexibly allocated to different interleaving and deinterleaving functions based on the number of sessions and the interleave depth. Consequently, Fadavi-Ardekani discloses that the memory is allocated between the interleaving function and the deinterleaving function. And, as I explained in my Opening Report (*see, e.g.*, Jacobsen Opening Report at ¶¶ 447-48), to perform the allocation of memory between the interleaving functions and deinterleaving functions, the transceiver of Fadavi-Ardekani would use the parameters specified in the O-MSG2 and R-MSG2 messages of G.993.1.

256. Without any support, Dr. Cooklev asserts that "a POSITA would understand G.993.1 to provide for dedicated downstream memories in each transceiver and separate, dedicated upstream memories in each transceiver," which he contends was "consistent with other ADSL and G.Lite-compliant modems of that era and proposals for VDSL modems, including the LB-031 modem." Cooklev Report at ¶ 290. I disagree. As I have explained (*see supra*, § VII.A.2), Dr. Cooklev's assertions that prior art implementations always and only used dedicated interleaver memory and dedicated deinterleaver memory are unsupported and speculative.

257. Dr. Cooklev also argues that "the IDIM [of Fadavi-Ardekani] is not allocated between the interleaving and deinterleaving functions." Cooklev Report at ¶ 291. I disagree. As I have explained (*see, e.g.*, *supra*, § VII.D.1.a), and as Dr. Cooklev acknowledges elsewhere in his report (*see, e.g.*, Cooklev Report at ¶ 275), Fadavi-Ardekani discloses an "optimal implementation" that "utilizes the same memory for receive data and transmit data." Fadavi-Ardekani at col. 7:25-27. This implementation is capable of supporting "a standard ADSL session at full interleave depth," and "[w]ith a lesser interleave depth, *additional sessions may be supported with the same size buffer*." *Id.* at col. 7:25-32 (emphasis added). As a skilled artisan would have understood, this disclosure means that the memory is flexibly allocated to different interleaving and deinterleaving functions based on the number of sessions and the interleave depth. Consequently, Fadavi-Ardekani discloses that the memory is allocated between the interleaving function and the deinterleaving function.

258. Thus, having considered Dr. Cooklev's opinion to the contrary, it remains my opinion that Fadavi-Ardekani in combination with G.993.1 discloses that "the memory is allocated between the interleaving function and the deinterleaving function in accordance with a message received during an initialization of the transceiver."

e. 19[e]. "wherein at least a portion of the memory may be allocated to the interleaving function or the deinterleaving function at any one particular time depending on the message"

259. Dr. Cooklev disputes that Fadavi-Ardekani in combination with G.993.1 discloses that "at least a portion of the memory may be allocated to the interleaving function or the deinterleaving function at any one particular time depending on the message." Cooklev Report at ¶¶ 292-94.

260. Once again, Dr. Cooklev contends that "there is no situation where a portion of the memory assigned to the interleaving function may be allocated to the deinterleaving

function and vice versa." Cooklev Report at ¶ 292. I disagree. As I explained in my Opening Report and above (*see supra*, § VII.D.1.a), Fadavi-Ardekani indicates that the optimal implementation allows the shared memory, which sized to accommodate the maximum codeword length and the maximum interleaver depth for one session, to be allocated flexibly for interleaving and deinterleaving for multiple sessions using "a lesser interleave depth." Fadavi-Ardekani at col. 6:66-7:33.

261. Dr. Cooklev argues that because I explained that "G.993.1 discloses that at least a portion of the memory may be allocated to the interleaving function or the deinterleaving function at any one particular time," I did not address the second "wherein" clause of claim 19. Cooklev Report at ¶ 293 (quoting Jacobsen Opening Report at ¶ 452). On the contrary, and as I explained in my Opening Report (*see* Jacobsen Opening Report at ¶¶ 447-48), the VDSL transceivers described in G.993.1 are capable of sending messages during initialization, specifying communications parameters, including interleaver and deinterleaver settings and capabilities, including R-MSG2, sent by the VTU-R, that "transmits information about [the connection's] bit allocation capabilities and several other features," including the "Maximal interleaver memory," expressed in bytes, and O-MSG2, transmitted by the VTU-O, which contains the field "Maximum interleaver delay," expressed in milliseconds. I explained that a person having ordinary skill in the art would have understood as of the Family 3 patents' priority date that because the interleaver delay is a function of the bit rate and interleaver depth, O-MSG2 specifies parameters that the VTU-O can use to allocate memory between an interleaver and a deinterleaver. It also discloses the VTU-R receiving a message during initialization (i.e., O-MSG2) that the transceiver can use to allocate memory between an interleaver and a deinterleaver (i.e., the VTU-O's interleaver). *Id.* These disclosures indicate

that at least a portion of the memory may be allocated to the interleaving function or the deinterleaving function at any one particular time depending on the message.

262. Thus, having considered Dr. Cooklev's opinion to the contrary, it remains my opinion that Fadavi-Ardekani in combination with G.993.1 discloses "wherein at least a portion of the memory may be allocated to the interleaving function or the deinterleaving function at any one particular time depending on the message." Accordingly, having considered Dr. Cooklev's argument to the contrary, it remains my opinion that Fadavi-Ardekani in combination with G.993.1 discloses all of the limitations of claim 19 of the '473 patent.

4. Motivation to Combine Fadavi-Ardekani and G.993.1

263. Dr. Cooklev disputes that a skilled artisan would have been motivated to combine the teachings of Fadavi-Ardekani with the teachings of G.993.1 to arrive at claim 19 of the '473 patent. Cooklev Report at ¶¶ 295-301.

264. Dr. Cooklev disputes that "both Fadavi and G.993.1 describe the need to allocate memory for interleaving and deinterleaving." *Id.* at ¶ 297. Specifically, Dr. Cooklev contends that "Fadavi merely teaches providing each interleaver and deinterleaver with a dedicated amount of memory the size of which is 'derived by multiplying the maximum codeword length by the maximum interleaver depth.'" *Id*. (quoting Fadavi-Ardekani at col. 7:6-10). On the contrary, and as I have explained, the portion of Fadavi-Ardekani Dr. Cooklev quotes is explaining how to derive the *total* size of the IDIM. Fadavi-Ardekani specifically contemplates that in deployment, the IDIM having the derived total size can "support a standard ADSL session at full interleave depth," or "[w]ith a lesser interleave depth, additional sessions may be supported *with the same size buffer*." Fadavi-Ardekani at col. 7:25-32 (emphasis added). *See also id.* at col. 7:3-5 ("The size of the IDIM and the interleave depth may be varied so that a different number of sessions may be supported by the transceiver of the invention."); *id.* at col.

7:32-33 ("With a larger buffer, additional session[s] may be supported."). Consequently, and contrary to Dr. Cooklev's assertions, Fadavi-Ardekani does disclose the need to allocate memory for interleaving and deinterleaving.

265. Dr. Cooklev asserts that the optimal implementation described by Fadavi-Ardekani would be inoperable with G.993.1. Cooklev Report at ¶ 298. Without any citation to Fadavi-Ardekani, Dr. Cooklev argues that "Fadavi discloses that the same memory is used for receive and transmit data, alternately," and that "the received deinterleave data will be overwritten with interleave data that must be interleaved and transmitted." *Id.* at ¶ 299. Dr. Cooklev has mischaracterized the disclosures of Fadavi-Ardekani. The portions of Fadavi-Ardekani to which he appears to refer concern the use of the frame buffer ("FB"), not the interleave/deinterleave memory ("IDIM"), which is a separate memory. *See, e.g.*, Fadavi-Ardekani at FIG. 2. Although Fadavi-Ardekani discloses that the "sequence of operations minimizes memory requirements by allowing the [receive] data to overwrite the same memory area in the FB that is used by the [transmit] data, thereby permitting the size of the FB to be half that of a conventional transceiver," (Fadavi-Ardekani at col. 8:4-8), I do not see any disclosure in Fadavi-Ardekani that the interleaver can overwrite deinterleave data (or vice versa). On the contrary, Fadavi-Ardekani discloses that once the IDIM memory has been allocated for interleaving and deinterleaving, "the DSP core may load new DMT frames of [receive] data to a portion of the IDIM used as de-interleaver memory while the FCI is using a portion of the IDIM as interleave memory." *Id.* at col. 8:62-65. Thus, "the DSP core can read [transmit] data from the portion of the IDIM used as interleave memory while the FCI is accessing the portion of the IDIM used as de-interleave memory." *Id.* at col. 8:67-9:3. Furthermore, as I explained in my Opening Report (*see, e.g.*, Jacobsen Opening Report at ¶ 450), Fadavi-Ardekani discloses that

the shared IDIM memory operates in a "ping-pang" fashion used by multiple functions, where "[a]s one area of memory is being used by a first agent, another area of memory can be used by a different agent." Fadavi-Ardekani at col. 6:60-65.

266. Dr. Cooklev also asserts that "[a] POSITA would recognize that modifying Fadavi to use the initialization messages described in G.993.1 would add to complexity." Cooklev Report at ¶ 300. I disagree. As I have explained, Fadavi-Ardekani discloses that the disclosed transceiver is capable of supporting "a standard ADSL session at full interleave depth," and "[w]ith a lesser interleave depth, additional sessions may be supported with the same size buffer." *Id.* at col. 7:25-32. As a skilled artisan would have understood, this disclosure means that the memory is flexibly allocated to different interleaving and deinterleaving functions based on, among other things, the interleave depth, which is one of the parameters conveyed by the G.993.1 initialization messages. *See* Jacobsen Opening Report at § VII.F.4.

267. Consequently, having considered Dr. Cooklev's argument to the contrary, it remains my opinion that a skilled artisan would have been motivated to combine the teachings of Fadavi-Ardekani with the teachings of G.993.1 as claimed in the asserted claims of the Family 3 patents.

E. Fadavi-Ardekani in Combination with G.992.2 Renders the Asserted Claims Obvious

268. As explained below, having considered Dr. Cooklev's arguments to the contrary, it remains my opinion that Fadavi-Ardekani in combination with G.992.2 renders obvious claim 1 of the '048 patent, claim 5 of the '381 patent, claim 13 of the '882 patent, and claim 19 of the '473 patent.

1. Claim 1 of the '048 Patent

269. Having considered Dr. Cooklev's argument to the contrary, it remains my opinion that Fadavi-Ardekani in combination with G.992.2 renders claim 1 of the '048 patent obvious.

a. 1[a]. "A system that allocates shared memory"

270. Dr. Cooklev disputes that Fadavi-Ardekani in combination with G.992.2 discloses "[a] system that allocates shared memory." Cooklev Report at ¶ 302. Dr. Cooklev's rebuttal refers to his argument with respect to element 1[a] for the combination of Fadavi-Ardekani and G.993.1. I explained above (*see supra*, § VII.D.1.a) why I disagree with Dr. Cooklev.

271. Thus, having considered Dr. Cooklev's opinion to the contrary, it remains my opinion that Fadavi-Ardekani in combination with G.992.2 discloses a system that allocates shared memory.

b. [1b]. "a transceiver that is capable of"

272. Dr. Cooklev concedes that Fadavi-Ardekani in combination with G.992.2 discloses a transceiver. Cooklev Report at ¶¶ 302-05.

c. 1[c] "transmitting or receiving a message during initialization specifying a maximum number of bytes of memory that are available to allocated to an interleaver"

273. Dr. Cooklev concedes that Fadavi-Ardekani in combination with G.992.2 discloses "transmitting or receiving a message during initialization specifying a maximum number of bytes of memory that are available to allocated to an interleaver, at least within TQ Delta's interpretation of this limitation in its infringement case." Cooklev Report at ¶¶ 302-05.

d. 1[d]. "determining an amount of memory required by the interleaver to interleave a first plurality of Reed-Solomon (RS) coded data bytes within the shared memory"

274. Dr. Cooklev concedes that Fadavi-Ardekani in combination with G.992.2 discloses "determining an amount of memory required by the interleaver to interleave a first plurality of Reed-Solomon (RS) coded data bytes within the shared memory." Cooklev Report at ¶¶ 302-05.

e. 1[e] and 1[f]. "allocating a first number of bytes of the shared memory to the interleaver to interleave the first plurality of Reed Solomon (RS) coded data bytes for transmission at a first rate, wherein the allocated memory for the interleaver does not exceed the maximum number of bytes specified in the message"

275. Dr. Cooklev disputes that Fadavi-Ardekani in combination with G.992.2 discloses "allocating a first number of bytes of the shared memory to the interleaver to interleave the first plurality of Reed Solomon (RS) coded data bytes for transmission at a first rate, wherein the allocated memory for the interleaver does not exceed the maximum number of bytes specified in the message." Cooklev Report at ¶ 303. Dr. Cooklev's rebuttal refers to his argument with respect to elements 1[e] and 1[f] for the combination of Fadavi-Ardekani and G.993.1. I explained above (*see supra*, § VII.D.1.e) why I disagree with Dr. Cooklev.

276. Without any support, Dr. Cooklev asserts that "a POSITA would understand G.992.2 to provide for dedicated downstream memories in each transceiver and separate, dedicated upstream memories in each transceiver," which he contends was "consistent with other ADSL and G.Lite-compliant modems of that era and proposals for VDSL modems, including the LB-031 modem." Cooklev Report at ¶ 304. I disagree. As I have explained (*see, e.g.*, *supra*, § VII.A.2), Dr. Cooklev's assertions that prior art implementations always and only used dedicated interleaver memory and dedicated deinterleaver memory are unsupported and speculative.

277. Thus, having considered Dr. Cooklev's opinion to the contrary, it remains my opinion that Fadavi-Ardekani in combination with G.992.2 discloses "allocating a first number of bytes of the shared memory to the interleaver to interleave the first plurality of Reed Solomon (RS) coded data bytes for transmission at a first rate, wherein the allocated memory for the interleaver does not exceed the maximum number of bytes specified in the message," at least within the interpretation of the claim advanced by TQ Delta in its infringement case.

f. 1[g]. "allocating a second number of bytes of the shared memory to a deinterleaver to deinterleave a second plurality of RS coded data bytes received at a second data rate"

278. Dr. Cooklev disputes that Fadavi-Ardekani in combination with G.992.2 discloses "allocating a second number of bytes of the shared memory to a deinterleaver to deinterleave a second plurality of RS coded data bytes received at a second data rate." Cooklev Report at ¶ 305. Dr. Cooklev's rebuttal refers to his argument with respect to element 1[g] for the combination of Fadavi-Ardekani and G.993.1. I explained above (*see supra*, § VII.D.1.f) why I disagree with Dr. Cooklev.

279. Thus, having considered Dr. Cooklev's opinion to the contrary, it remains my opinion that Fadavi-Ardekani in combination with G.992.2 discloses "allocating a second number of bytes of the shared memory to a deinterleaver to deinterleave a second plurality of RS coded data bytes received at a second data rate."

g. 1[h]. "interleaving the first plurality of RS coded data bytes within the shared memory allocated to the interleaver and deinterleaving the second plurality of RS coded data bytes within the shared memory allocated to the deinterleaver"

280. Dr. Cooklev concedes that Fadavi-Ardekani in combination with G.992.2 discloses "interleaving the first plurality of RS coded data bytes within the shared memory allocated to the interleaver and deinterleaving the second plurality of RS coded data bytes within the shared memory allocated to the deinterleaver." Cooklev Report at ¶¶ 302-05.

h. 1[i]. "wherein the shared memory allocated to the interleaver is used at the same time as the shared memory allocated to the deinterleaver"

281. Dr. Cooklev concedes that Fadavi-Ardekani in combination with G.992.2 discloses "wherein the shared memory allocated to the interleaver is used at the same time as the shared memory allocated to the deinterleaver." Cooklev Report at ¶¶ 302-05.

282. Thus, having considered Dr. Cooklev's argument to the contrary, it remains my opinion that Fadavi-Ardekani in combination with G.992.2 discloses all of the limitations of claim 1 of the '048 patent.

2. Claim 5 of the '381 Patent

283. Having considered Dr. Cooklev's argument to the contrary, it remains my opinion that Fadavi-Ardekani in combination with G.992.2 renders claim 5 of the '381 patent obvious.

a. 5[a]. "A non-transitory computer-readable information storage media having stored thereon instructions, that if executed by a processor, cause to be performed a method for allocating shared memory in a transceiver"

284. Dr. Cooklev disputes that Fadavi-Ardekani in combination with G.992.2 discloses "[a] non-transitory computer-readable information storage media having stored thereon instructions, that if executed by a processor, cause to be performed a method for allocating shared memory in a transceiver." Cooklev Report at ¶ 306. Dr. Cooklev's rebuttal refers to his argument with respect to elements 1[a] and 5[a] for the combination of Fadavi-Ardekani and G.993.1. I explained above (*see supra*, §§ VII.D.1.a, VII.D.2.a) why I disagree with Dr. Cooklev.

285. Furthermore, with respect to Fadavi-Ardekani in particular, as Dr. Cooklev stated in his discussion on written description and enablement, "a patent need not teach, and preferably omits, what is well known in the art." Cooklev Report at ¶ 80. Thus, Dr. Cooklev

agrees that "it was not necessary [for Fadavi-Ardekani] to provide a full and detailed explanation where, as here, a POSITA would know how to implement the claim." *Id.*

286. Thus, having considered Dr. Cooklev's opinion to the contrary, it remains my opinion that Fadavi-Ardekani in combination with G.992.2 discloses "[a] non-transitory computer-readable information storage media having stored thereon instructions, that if executed by a processor, cause to be performed a method for allocating shared memory in a transceiver."

b. 5[b]. "transmitting or receiving, by the transceiver, a message during initialization specifying a maximum number of bytes of memory that are available to be allocated to a deinterleaver"

287. Dr. Cooklev concedes that Fadavi-Ardekani in combination with G.992.2 discloses "transmitting or receiving, by the transceiver, a message during initialization specifying a maximum number of bytes of memory that are available to be allocated to a deinterleaver," at least within the interpretation of the claim advanced by TQ Delta in its infringement case. Cooklev Report at ¶¶ 306-08.

c. 5[c]. "determining, at the transceiver, an amount of memory required by the deinterleaver to deinterleave a first plurality of Reed Solomon (RS) coded data bytes within a shared memory"

288. Dr. Cooklev concedes that Fadavi-Ardekani in combination with G.992.2 discloses "determining, at the transceiver, an amount of memory required by the deinterleaver to deinterleave a first plurality of Reed Solomon (RS) coded data bytes within a shared memory." Cooklev Report at ¶¶ 306-08.

d. 5[d] and 5[e]. "allocating, in the transceiver, a first number of bytes of the shared memory to the deinterleaver to deinterleave a first plurality of Reed Solomon (RS) coded data bytes for transmission at a first data rate, wherein the allocated memory for the deinterleaver does not exceed the maximum number of bytes specified in the message"

289. Dr. Cooklev disputes that Fadavi-Ardekani in combination with G.992.2 discloses "allocating, in the transceiver, a first number of bytes of the shared memory to the deinterleaver to deinterleave a first plurality of Reed Solomon (RS) coded data bytes for transmission at a first data rate, wherein the allocated memory for the deinterleaver does not exceed the maximum number of bytes specified in the message." Cooklev Report at ¶ 307. Dr. Cooklev's rebuttal refers to his argument with respect to elements 1[e] and 1[f] for the combination of Fadavi-Ardekani and G.992.2. I explained above (*see supra*, § VII.E.1.e) why I disagree with Dr. Cooklev.

290. Thus, having considered Dr. Cooklev's opinion to the contrary, it remains my opinion that Fadavi-Ardekani in combination with G.992.2 discloses "allocating, in the transceiver, a first number of bytes of the shared memory to the deinterleaver to deinterleave a first plurality of Reed Solomon (RS) coded data bytes for transmission at a first data rate, wherein the allocated memory for the deinterleaver does not exceed the maximum number of bytes specified in the message," at least within the interpretation of the claim language advanced by TQ Delta in its infringement case.

e. 5[f]. "allocating, in the transceiver, a second number of bytes of the shared memory to an interleaver to interleave a second plurality of RS coded data bytes transmitted at a second data rate"

291. Dr. Cooklev disputes that Fadavi-Ardekani in combination with G.992.2 discloses "allocating, in the transceiver, a second number of bytes of the shared memory to an interleaver to interleave a second plurality of RS coded data bytes transmitted at a second data rate." Cooklev Report at ¶ 308. Dr. Cooklev's rebuttal refers to his argument with respect to

elements 1[e] and 1[f] for the combination of Fadavi-Ardekani and G.992.2. I explained above (*see supra*, § VII.E.1.e) why I disagree with Dr. Cooklev.

292. Thus, having considered Dr. Cooklev's opinion to the contrary, it remains my opinion that Fadavi-Ardekani in combination with G.992.2 discloses "allocating, in the transceiver, a second number of bytes of the shared memory to an interleaver to interleave a second plurality of RS coded data bytes transmitted at a second data rate."

f. 5[g]. "deinterleaving the first plurality of RS coded data bytes within the shared memory allocated to the deinterleaver and interleaving the second plurality of RS coded data bytes within the shared memory allocated to the interleaver"

293. Dr. Cooklev concedes that Fadavi-Ardekani in combination with G.992.2 discloses "deinterleaving the first plurality of RS coded data bytes within the shared memory allocated to the deinterleaver and interleaving the second plurality of RS coded data bytes within the shared memory allocated to the interleaver." Cooklev Report at ¶¶ 306-08.

g. 5[h]. "wherein the shared memory allocated to the deinterleaver is used at the same time as the shared memory allocated to the interleaver"

294. Dr. Cooklev concedes that Fadavi-Ardekani in combination with G.992.2 discloses "wherein the shared memory allocated to the deinterleaver is used at the same time as the shared memory allocated to the interleaver." Cooklev Report at ¶¶ 306-08.

295. Therefore, having considered Dr. Cooklev's arguments to the contrary, it remains my opinion that Fadavi-Ardekani in combination with G.992.2 discloses all of the limitations of claim 5 of the '381 patent.

3. Claim 13 of the '882 Patent

296. Having considered Dr. Cooklev's argument to the contrary, it remains my opinion that Fadavi-Ardekani in combination with G.992.2 renders claim 13 of the '882 patent obvious.

a. 13[a]. "A system that allocates shared memory"

297. Dr. Cooklev disputes that Fadavi-Ardekani in combination with G.992.2 discloses a system that allocates shared memory. Cooklev Report at ¶ 309. Dr. Cooklev's rebuttal refers to his argument with respect to element 1[a] for the combination of Fadavi-Ardekani and G.993.1. I explained above (*see supra*, VII.D.1.a) why I disagree with Dr. Cooklev.

298. Thus, having considered Dr. Cooklev's opinion to the contrary, it remains my opinion that Fadavi-Ardekani in combination with G.992.2 discloses a system that allocates shared memory.

b. 13[b]. "a transceiver"

299. Dr. Cooklev concedes that Fadavi-Ardekani in combination with G.992.2 discloses a transceiver. Cooklev Report at ¶¶ 309-11.

c. 13[c]. "transmitting or receiving a message during initialization specifying a maximum number of bytes of memory that are available to be allocated to a deinterleaver"

300. Dr. Cooklev concedes that Fadavi-Ardekani in combination with G.992.2 discloses "transmitting or receiving a message during initialization specifying a maximum number of bytes of memory that are available to be allocated to a deinterleaver," at least within the claim interpretation advanced by TQ Delta in its infringement reports. Cooklev Report at ¶¶ 309-11.

d. 13[d]. "determining an amount of memory required by the deinterleaver to deinterleave a first plurality of Reed Solomon (RS) coded data bytes within a shared memory"

301. Dr. Cooklev concedes that Fadavi-Ardekani in combination with G.992.2 discloses "determining an amount of memory required by the deinterleaver to deinterleave a

first plurality of Reed Solomon (RS) coded data bytes within a shared memory." Cooklev Report at ¶¶ 309-11.

e. 13[e], and 13[f]. "allocating a first number of bytes of the shared memory to the deinterleaver to deinterleave a first plurality of Reed Solomon (RS) coded data bytes for reception at a first data rate, wherein the allocated memory for the deinterleaver does not exceed the maximum number of bytes specified in the message"

302. Dr. Cooklev disputes that Fadavi-Ardekani in combination with G.992.2 discloses "allocating a first number of bytes of the shared memory to the deinterleaver to deinterleave a first plurality of Reed Solomon (RS) coded data bytes for reception at a first data rate, wherein the allocated memory for the deinterleaver does not exceed the maximum number of bytes specified in the message." Cooklev Report at ¶ 310. Dr. Cooklev merely references his argument with respect to elements 1[e] and 1[f] of the '048 patent. *Id.* I explained above (*see supra*, § VII.E.1.e) why I disagree with Dr. Cooklev.

303. Thus, having considered Dr. Cooklev's argument to the contrary, it remains my opinion that Fadavi-Ardekani in combination with G.992.2 discloses "allocating a first number of bytes of the shared memory to the deinterleaver to deinterleave a first plurality of Reed Solomon (RS) coded data bytes for reception at a first data rate, wherein the allocated memory for the deinterleaver does not exceed the maximum number of bytes specified in the message," at least within the interpretation of the claim advanced by TQ Delta in its infringement case.

f. 13[g]. "allocating a second number of bytes of the shared memory to an interleaver to interleave a second plurality of RS coded data bytes transmitted at a second data rate."

304. Dr. Cooklev disputes that Fadavi-Ardekani in combination with G.992.2 discloses "allocating a second number of bytes of the shared memory to an interleaver to interleave a second plurality of RS coded data bytes transmitted at a second data rate." Cooklev Report at ¶ 311. Dr. Cooklev merely references his argument with respect to elements 1[e] and

1[f] of the '048 patent. *Id.* I explained above (*see supra*, § VII.E.1.e) why I disagree with Dr. Cooklev.

305. Thus, having considered Dr. Cooklev's argument to the contrary, it remains my opinion that Fadavi-Ardekani in combination with G.992.2 discloses "allocating a second number of bytes of the shared memory to an interleaver to interleave a second plurality of RS coded data bytes transmitted at a second data rate."

g. 13[h]. "deinterleaving the first plurality of RS coded data bytes within the shared memory allocated to the deinterleaver and interleaving the second plurality of RS coded data bytes within the shared memory allocated to the interleaver"

306. Dr. Cooklev concedes that Fadavi-Ardekani in combination with G.992.2 discloses "deinterleaving the first plurality of RS coded data bytes within the shared memory allocated to the deinterleaver and interleaving the second plurality of RS coded data bytes within the shared memory allocated to the interleaver." Cooklev Report at ¶¶ 308-11.

h. 13[i]. "wherein the shared memory allocated to the deinterleaver is used at the same time as the shared memory allocated to the interleaver"

307. Dr. Cooklev concedes that Fadavi-Ardekani in combination with G.992.2 discloses "wherein the shared memory allocated to the deinterleaver is used at the same time as the shared memory allocated to the interleaver." Cooklev Report at ¶¶ 308-11.

308. Thus, having considered Dr. Cooklev's argument to the contrary, it remains my opinion that Fadavi-Ardekani in combination with G.992.2 discloses all of the limitations of claim 13 of the '882 patent.

4. Claim 19 of the '473 Patent

309. Having considered Dr. Cooklev's argument to the contrary, it remains my opinion that Fadavi-Ardekani in combination with G.992.2 renders claim 19 of the '473 patent obvious.

a. 19[a]. "An apparatus comprising"

310. Dr. Cooklev concedes that Fadavi-Ardekani in combination with G.992.2 discloses an apparatus. Cooklev Report at ¶¶ 312-15.

b. 19[b]. "a multicarrier communications transceiver that is configured to perform an interleaving function associated with a first latency path and perform a deinterleaving function associated with a second latency path"

311. Dr. Cooklev concedes that Fadavi-Ardekani in combination with G.992.2 discloses "a multicarrier communications transceiver that is configured to perform an interleaving function associated with a first latency path and perform a deinterleaving function associated with a second latency path." Cooklev Report at ¶¶ 312-15.

c. 19[c]. "the multicarrier communications transceiver being associated with a memory"

312. Dr. Cooklev concedes that Fadavi-Ardekani in combination with G.992.2 discloses that the multicarrier communications transceiver is associated with a memory. Cooklev Report at ¶¶ 312-15.

d. 19[d]. "wherein the memory is allocated between the interleaving function and the deinterleaving function in accordance with a message received during an initialization of the transceiver"

313. Dr. Cooklev disputes that Fadavi-Ardekani in combination with G.992.2 discloses that "the memory is allocated between the interleaving function and the deinterleaving function in accordance with a message received during an initialization of the transceiver." Cooklev Report at ¶ 312.

314. Dr. Cooklev does not dispute that G.992.2 discloses a message received during an initialization of the transceiver, or that the messages of G.992.2 convey information used to configure interleavers and deinterleavers. Cooklev Report at ¶ 312. Dr. Cooklev's argument is solely that "[t]he G.992.2 standard . . . does not teach using the initialization messages to

allocate memory between an interleaver and a deinterleaver." *Id.* Without any support, Dr. Cooklev asserts that "a POSITA would understand G.992.2 to provide for dedicated downstream memories in each transceiver and separate, dedicated upstream memories in each transceiver," which he contends was "consistent with other ADSL and G.Lite-compliant modems of that era and proposals for VDSL modems, including the LB-031 modem." *Id.* I disagree. As I have explained (*see supra*, §§ VII.A.1, VII.A.2), Dr. Cooklev's assertions that the standards mandated the use of dedicated interleaver and deinterleaver memory and that prior art implementations always and only used dedicated interleaver memory and dedicated deinterleaver memory are unsupported and speculative.

315. Thus, having considered Dr. Cooklev's opinion to the contrary, it remains my opinion that Fadavi-Ardekani in combination with G.992.2 discloses "wherein the memory is allocated between the interleaving function and the deinterleaving function in accordance with a message received during an initialization of the transceiver."

e. 19[e]. "wherein at least a portion of the memory may be allocated to the interleaving function or the deinterleaving function at any one particular time depending on the message"

316. Dr. Cooklev disputes that Fadavi-Ardekani in combination with G.992.2 discloses that "at least a portion of the memory may be allocated to the interleaving function or the deinterleaving function at any one particular time depending on the message." Cooklev Report at ¶¶ 313-15.

317. Dr. Cooklev refers to his discussion of element 19[e] for Fadavi-Ardekani in combination with G.993.1 and contends that "Fadavi does not disclose this limitation." Cooklev Report at ¶ 313. I disagree. As I explained in my Opening Report and above (*see supra*, VII.D.1.a), Fadavi-Ardekani indicates that the optimal implementation allows the shared memory, which is sized to accommodate the maximum codeword length and the maximum

interleaver depth for one session, to be allocated flexibly for interleaving and deinterleaving for multiple sessions using "a lesser interleave depth." Fadavi-Ardekani at col. 6:66-7:33.

318. Dr. Cooklev argues that because I explained that because a skilled artisan would have understood that the interleaver and deinterleaver in G.992.2 are used at the same time, I did not address the second "wherein" clause of claim 19. Cooklev Report at ¶ 314 (citing Jacobsen Opening Report at ¶ 526). On the contrary, and as I explained in my Opening Report (*see* Jacobsen Opening Report at ¶¶ 522-24), the ADSL transceivers described in G.992.2 are capable of sending messages, including initialization messages, specifying communications parameters in ADSL systems. These initialization messages that contain information about the channel as well as the transceivers and their capabilities and requirements, including the RRSI field that contains ten entries, including interleave depth in codewords. As I explained, one of ordinary skill in the art would have understood that the information in these messages can be used to allocate memory between an interleaver and a deinterleaver function, at least within TQ Delta's interpretation of the claims. These disclosures indicate that at least a portion of the memory may be allocated to the interleaving function or the deinterleaving function at any one particular time depending on the message.

319. Thus, having considered Dr. Cooklev's opinion to the contrary, it remains my opinion that Fadavi-Ardekani in combination with G.992.2 discloses "wherein at least a portion of the memory may be allocated to the interleaving function or the deinterleaving function at any one particular time depending on the message."

320. Accordingly, having considered Dr. Cooklev's argument to the contrary, it remains my opinion that Fadavi-Ardekani in combination with G.992.2 discloses all of the limitations of claim 19 of the '473 patent.

5. Motivation to Combine Fadavi-Ardekani and G.992.2

321. Dr. Cooklev disputes that a skilled artisan would have been motivated to combine the teachings of Fadavi-Ardekani with the teachings of G.992.2 to arrive at the asserted Family 3 claims. Cooklev Report at ¶¶ 316-22.

322. As an initial matter, Dr. Cooklev did not rebut my argument that a skilled artisan would have been motivated to combine the disclosures of Fadavi-Ardekani and G.992.2 because Fadavi-Ardekani references G.lite, which the skilled artisan would have recognized to be G.992.2. *See* Jacobsen Opening Report at ¶ 527 ("In addition, Fadavi-Ardekani references G.992.2 a number of times, confirming that one of ordinary skill in the art would naturally consider the references together.").

323. Dr. Cooklev disputes that "both Fadavi and G.992.2 describe the need to allocate memory for interleaving and deinterleaving." *Id.* at ¶ 318. Specifically, Dr. Cooklev contends that "Fadavi merely teaches providing each interleaver and deinterleaver with a dedicated amount of memory the size of which is 'derived by multiplying the maximum codeword length by the maximum interleaver depth.'" *Id*. (quoting Fadavi-Ardekani at col. 7:6-10). On the contrary, and as I have explained, the portion of Fadavi-Ardekani Dr. Cooklev quotes is explaining how to derive the *total* size of the IDIM. Fadavi-Ardekani specifically contemplates that in deployment, the IDIM having the derived total size can "support a standard ADSL session at full interleave depth," or "[w]ith a lesser interleave depth, additional sessions may be supported *with the same size buffer*." Fadavi-Ardekani at col. 7:25-32 (emphasis added). *See also id.* at col. 7:3-5 ("The size of the IDIM and the interleave depth may be varied so that a different number of sessions may be supported by the transceiver of the invention."); *id.* at col. 7:32-33 ("With a larger buffer, additional session[s] may be supported."). Consequently, and

contrary to Dr. Cooklev's assertions, Fadavi-Ardekani does disclose the need to allocate memory for interleaving and deinterleaving.

324. Dr. Cooklev asserts that the optimal implementation described by Fadavi-Ardekani, would be inoperable with G.993.1. Cooklev Report at ¶ 319. Without any citation to Fadavi-Ardekani, Dr. Cooklev argues that "Fadavi discloses that the same memory is used for receive and transmit data, alternately," and that "the received deinterleave data will be overwritten with interleave data that must be interleaved and transmitted." *Id.* at ¶ 320. As I explained above, Dr. Cooklev has mischaracterized the disclosures of Fadavi-Ardekani. The portions of Fadavi-Ardekani to which he appears to refer concern the use of the frame buffer ("FB"), not the interleave/deinterleave memory ("IDIM"), which is a separate memory. *See, e.g.*, Fadavi-Ardekani at FIG. 2. Although Fadavi-Ardekani discloses that the "sequence of operations minimizes memory requirements by allowing the [receive] data to overwrite the same memory area in the FB that is used by the [transmit] data, thereby permitting the size of the FB to be half that of a conventional transceiver," (Fadavi-Ardekani at col. 8:4-8), I do not see any disclosure in Fadavi-Ardekani that the interleaver can overwrite deinterleave data (or vice versa). On the contrary, Fadavi-Ardekani discloses that once the IDIM memory has been allocated for interleaving and deinterleaving, "the DSP core may load new DMT frames of [receive] data to a portion of the IDIM used as de-interleaver memory while the FCI is using a portion of the IDIM as interleave memory." *Id.* at col. 8:62-65. Thus, "the DSP core can read [transmit] data from the portion of the IDIM used as interleave memory while the FCI is accessing the portion of the IDIM used as de-interleave memory." *Id.* at col. 8:67-9:3. Furthermore, as I explained in my Opening Report (*see, e.g.*, Jacobsen Opening Report at ¶ 450), Fadavi-Ardekani discloses that the shared IDIM memory operates in a "ping-pang"

fashion used by multiple functions, where "[a]s one area of memory is being used by a first agent, another area of memory can be used by a different agent." Fadavi-Ardekani at col. 6:60-65.

325. Dr. Cooklev also asserts that "[a] POSITA would recognize that modifying Fadavi to use the initialization messages described in G.992.2 would add to complexity." Cooklev Report at ¶ 321. I disagree. As I have explained, Fadavi-Ardekani discloses that the disclosed transceiver is capable of supporting "a standard ADSL session at full interleave depth," and "[w]ith a lesser interleave depth, additional sessions may be supported with the same size buffer." *Id.* at col. 7:25-32. As a skilled artisan would have understood, this disclosure means that the memory is flexibly allocated to different interleaving and deinterleaving functions based on, among other things, the interleave depth, which is one of the parameters conveyed by the G.992.2 initialization messages. *See* Jacobsen Opening Report at § VII.F.3.

326. Consequently, having considered Dr. Cooklev's argument to the contrary, it remains my opinion that a skilled artisan would have been motivated to combine the teachings of Fadavi-Ardekani with the teachings of G.992.2 as claimed in the asserted claims of the Family 3 patents.

F. Voith in Combination with LB-031 Renders Claim 19 of the '473 Patent Obvious

327. As explained below, having considered Dr. Cooklev's arguments to the contrary, it remains my opinion that Voith in combination with LB-031 renders claim 19 of the '473 patent obvious.

1. 19[a]. "An apparatus comprising"

328. Dr. Cooklev concedes that Voith in combination with LB-031 discloses an apparatus. Cooklev Report at ¶¶ 323-40.

2. 19[b]. "a multicarrier communications transceiver that is configured to perform an interleaving function associated with a first latency path and perform a deinterleaving function associated with a second latency path"

329. Dr. Cooklev concedes that Voith in combination with LB-031 discloses "a multicarrier communications transceiver that is configured to perform an interleaving function associated with a first latency path and perform a deinterleaving function associated with a second latency path." Cooklev Report at ¶¶ 323-40.

3. 19[c]. "the multicarrier communications transceiver being associated with a memory"

330. Dr. Cooklev concedes that Voith in combination with LB-031 discloses that the multicarrier communications transceiver is associated with a memory. Cooklev Report at ¶¶ 323-40.

4. 19[d]. "wherein the memory is allocated between the interleaving function and the deinterleaving function in accordance with a message received during an initialization of the transceiver"

331. Dr. Cooklev disputes that Voith in combination with LB-031 discloses that "the memory is allocated between the interleaving function and the deinterleaving function in accordance with a message received during an initialization of the transceiver." Cooklev Report at ¶ 326. Specifically, Dr. Cooklev asserts that "there is no basis for concluding that Voith allocates memory between an interleaving function and a deinterleaving function." *Id.* at ¶ 327. Dr. Cooklev's argument is that, according to him, "[i]t does not follow from the fact that the external memory is used for both interleaving and deinterleaving that any portion of the memory is allocated ***between*** these functions." *Id.* at ¶ 326 (emphasis in original). I disagree.

332. The Court's construed "memory is allocated between the interleaving function and the deinterleaving function" as "an amount of the memory is allocated to the interleaving function and an amount of memory is allocated to the deinterleaving function." As I explained in my Opening Report (*see* Jacobsen Opening Report at ¶ 557), Voith specifically notes that the interleaver "uses a portion of external interleave/deinterleave memory 66." *Id.* at col. 5:65-6:1. Voith also discloses that its interleaver "arbitrates" with the deinterleaver for use of external the interleave/deinterleave memory. *Id.* at col. 6:1-4. Voith also discloses that a deinterleaver performs a deinterleave operation on the interleaved portion of the received frame. *Id.* at col. 6:24-26. Voith's deinterleaver "makes use of external interleave/deinterleave memory 66" and "arbitrates for usage thereof" in a manner similar to the interleaver. *Id.* at col. 26-29. Thus, in accordance with the Court's construction, and contrary to Dr. Cooklev's assertion, in Voith, "an amount of the memory is allocated to the interleaving function and an amount of memory is allocated to the deinterleaving function."

333. Once again, without any support, Dr. Cooklev argues that that "a POSITA reviewing Voith's disclosure of an external interleave/deinterleave memory 66[] would understand this as disclosing that the memory includes a dedicated portion for use by interleaver 78 and a separate, dedicated portion for use by deinterleaver 90," which he contends is "consistent with other ADSL and G.Lite-compliant modems of that era and proposals for VDSL modems, including the LB-031 modem." Cooklev Report at ¶ 327. I disagree. As I have explained (*see supra*, § VII.A.2), Dr. Cooklev's assertions that prior art implementations always and only used dedicated interleaver memory and dedicated deinterleaver memory are unsupported and speculative.

334. In attempting to argue that Voith does not disclose that the memory is allocated between the interleaving function and the deinterleaving function in accordance with a message received during an initialization of the transceiver," Dr. Cooklev suggests that I "rel[ied] on a message such as the O-B&G message described in the G993.1 standard . . . or the C-B&G message described in the G.992.2 standard. . . ." Cooklev Report at ¶ 328. He then argues that I "provide[d] no evidence that Voith teaches that ADSL transceiver 34 allocated memory 66 between the interleaver 78 and the deinterleaver 90 based on a bit-allocation message." *Id.* On the contrary, Voith specifically refers to "the draft American National Standard for Telecommunication—Network and Customer Interfaces—Asymmetric Digital Subscriber Line (ADSL) metallic interface, T1E1.4/95-007R2, ADSL coding standard, draft, Aug. 15, 1995," (Voith at col. 1:18-25), which a skilled artisan would have recognized as the draft of T1.413 Issue 2. Voith discloses that "[t]he bit allocation table is determined at initialization between the central office and the remote terminal based on the characteristics of the transmission link." Voith, col. 6:9-12. Like all other ADSL standards, T1.413 Issue 2 requires the transceivers to exchange bits and gains using messages transmitted during initialization, which a skilled artisan would have understood. In my Opening Report, (*see* Jacobsen Opening Report at ¶ 558), I explained that LB-031 teaches the well-known principle that the amount of memory required to meet a particular interleaver delay requirement depends on the line data rate. *See* LB-031 at p. 4. The line data rate, in turn, depends on the number of bits assigned to each subcarrier. Therefore, Voith discloses that the memory is allocated between the interleaving function and the deinterleaving function in accordance with a message received during an initialization of the transceiver, at least within TQ Delta's interpretation of the claims in its infringement contentions.

335. Dr. Cooklev opines that "LB-031 at most discloses that a VTU-O (or a VTU-R) determines whether it can use all of its predetermined maximum interleaver memory or whether it has to use less of it because of the maximum capabilities of the deinterleaver on the other side of the line, are smaller." Cooklev Report at ¶ 329. He then argues that "LB-031 does not teach that the unused portion of the interleaver memory can be allocated to the deinterleaver." *Id.* I disagree. First, Dr. Cooklev's conclusion presumes, without justification, that the VTU-O and VTU-R implement interleaving and deinterleaving using dedicated memories. As I explained in my Rebuttal Report (*see, e.g.*, Jacobsen Rebuttal Report at § IX), none of the VDSL standards specifies that a VTU-O or VTU-R must implement interleaving and deinterleaving using either dedicated or shared memory.

336. Second, Dr. Cooklev has ignored the Court's construction that "memory is allocated between the interleaving function and the deinterleaving function [in accordance with a message received during an initialization of the transceiver]" means only that "an amount of the memory is allocated to the interleaving function and an amount of memory is allocated to the deinterleaving function [in accordance with a message received during an initialization of the transceiver]." Contrary to Dr. Cooklev's assertion, the Court's construction does not require "that the unused portion of the interleaver memory can be allocated to the deinterleaver." Because, as I explained, Voith discloses the use of T1.413 Issue 2 ADSL, which requires the transceivers to exchange bit allocations, and LB-031 teaches that the amount of memory required to meet a particular interleaver delay requirement depends on the line data rate, which depends on the bit allocation, Voith in combination with LB-031 discloses this limitation.

337. Therefore, having considered Dr. Cooklev's arguments to the contrary, it remains my opinion that Voith in combination with LB-031 discloses that the memory is

allocated between the interleaving function and the deinterleaving function in accordance with a message received during an initialization of the transceiver.

5. 19[e]. "wherein at least a portion of the memory may be allocated to the interleaving function or the deinterleaving function at any one particular time depending on the message"

338. Dr. Cooklev disputes that Voith in combination with LB-031 discloses that at least a portion of the memory may be allocated to the interleaving function or the deinterleaving function at any one particular time depending on the message. Cooklev Report at ¶ 331. Dr. Cooklev argues that "Voith does not teach that any portion of the memory 66 may be allocated to the interleaver 78 ***or*** the deinterleaver 90 at any one particular time depending on a message." *Id.* I explain how Voith in combination with LB-031 discloses this limitation at paragraphs 561 through 565 of my Opening Report.

339. In arguing that claim 19 of the '473 patent is not invalid for failing to meet the written description requirement, Dr. Cooklev states that "disclosure . . . is found generally [in the Family 3 patents] because the specification discloses the use of 'shared memory' by an interleaver and a deinterleaver." Cooklev Report at ¶ 82. He argues that "[a] POSITA would understand from the disclosure of shared memory that is allocated to an interleaver would not be used at the same time by a deinterleaver but, instead, could be used at alternative times depending on the allocation in effect at the time." Cooklev Report at ¶ 82. Thus, Dr. Cooklev contends that the mere disclosure in the Family 3 patents of shared memory used by an interleaver and a deinterleaver discloses "wherein at least a portion of the memory may be allocated to the interleaving function or the deinterleaving function at any one particular time depending on the message." Accordingly, a skilled artisan would also understand from the disclosure of shared memory—i.e., "common memory used by at least two functions, where a portion of the memory can be used by either one of the functions"—in Voith that memory

"allocated to the interleaver would not also be used at the same time by a deinterleaver but, instead, could be used at alternative times depending on the allocation in effect at the time," as in the Family 3 patents. Cooklev Report at ¶ 82.

340. Therefore, having considered Dr. Cooklev's arguments to the contrary, it remains my opinion that Voith in combination with LB-031 discloses that "at least a portion of the memory may be allocated to the interleaving function or the deinterleaving function at any one particular time depending on the message."

341. Accordingly, it remains my opinion that Voith in combination with LB-031 discloses all of the limitations of claim 19 of the '473 patent.

6. Motivation to Combine Voith and LB-031

342. Dr. Cooklev disputes that a skilled artisan would have been motivated to combine the teachings of Voith with the teachings of LB-031 as recited in claim 19 of the '473 patent. Cooklev Report at ¶ 335.

343. Dr. Cooklev argues, again without support, that "LB-031 describes a dedicated interleaver memory and a separate, dedicated deinterleaver memory where portions of a dedicated memory that is left unused by one function – because one transceiver supports more memory for a given latency path than is supported by the other transceiver with which it is communicating – is not available for use by the other function." *Id.* at ¶ 338. I disagree. As I have explained (*see, e.g.*, *supra*, § VII.B.1.a), a skilled artisan would have understood the disclosures of LB-031 to apply generally to VDSL2 implementations, regardless of whether they use dedicated or shared memory.

344. Dr. Cooklev also argues that Voith "does not disclose 'sharing memory for interleaving and deinterleaving to support various applications.'" Cooklev Report at ¶ 339. He states that "Voith merely teaches that it is preferable to implement the memory buffers off-

chip," but that Voith makes no proposal for reducing the sizes of the memory buffers. *Id.* But as I explained in my Opening Report, (*see* Jacobsen Opening Report at ¶ 568), LB-031 explains that "[t]he interleaver is a major source of complexity in VDSL2," (LB-031 at p. 1), and Voith discloses that efficiency in the use and management of memory is desirable. *See, e.g.*, Voith, at col. 2:26-28; col. 4:30-40. LB-031 teaches that there is a trade-off between complexity, capability, and performance. LB-031 at p. 3. Thus, one of ordinary skill in the art would have been motivated to combine the teachings of Voith with the teachings of LB-031.

G. Mazzoni in combination with G.993.1 Renders Claim 19 of the '473 Patent Obvious.

345. Having considered Dr. Cooklev's argument to the contrary, it remains my opinion that Mazzoni in combination with G.993.1 renders claim 19 of the '473 patent obvious.

1. Motivation to Combine Mazzoni and G.993.1

346. Dr. Cooklev disputes that a skilled artisan would have been motivated to combine the teachings of Mazzoni with the teachings of G.993.1 as claimed in claim 19 of the '473 patent. Cooklev Report at ¶¶ 341-52. Specifically, Dr. Cooklev argues that "the two references are so different that a person of ordinary skill in the art would be discouraged from looking to the teaching of the other reference." *Id.* at ¶ 341. I disagree.

347. Once again, without any support whatsoever, Dr. Cooklev asserts that "G.993.1, akin to LB-031, is yet another reference that employs a dedicated interleaver memory and a dedicated deinterleaver memory." *Id.* at ¶ 343. As I explained (*see, e.g.*, *supra*, § VII.A.2, ¶ 17), it is my opinion that Dr. Cooklev's assertion amounts to speculation.

348. Dr. Cooklev disputes that a skilled artisan would have recognized the limitations of Mazzoni's table and would have recognized that conveying interleaver parameters through the initialization messages of G.993.1 would avoid the limitations of Mazzoni's table and would

result in a more flexible solution. Cooklev Report at ¶ 346. He argues that because "Mazzoni relies on the use of a pre-populated table of I, M, I′ and M′ parameter values, where each set of values corresponds to respective one of a number of predetermined data rates," "[t]here is not use for a message that specifies the maximum supported interleaver or deinterleaver memory size because all data rate pairs and their corresponding I, M, I′ and M′ values that need to be supported are accounted for." *Id.* at ¶ 347. Here, as elsewhere in his report, Dr. Cooklev's opinion is that a skilled artisan would not be motivated to modify Mazzoni or G.993.1. But, as I explained in my Opening Report (*see* Jacobsen Opening Report at ¶ 595), a skilled artisan would have recognized the benefits of modifying Mazzoni to incorporate the initialization messages of G.993.1 to obviate the need for all asymmetrical and symmetrical services to be predefined and for the transceiver to store a table indicating the values of I, M, I′ and M′ for each of the predefined bit rates.

349. Dr. Cooklev argues that "Mazzoni provides substantial flexibility already given that it allows 12 difference [sic] service configurations." Cooklev Report at ¶ 348. I disagree. A skilled artisan would have recognized that a total of 12 pre-defined service configurations would be limiting because it would allow each transceiver to support only those 12 pre-defined services. Indeed, Mazzoni itself recognizes the limitation and discloses that it may be necessary to modify the parameters stored in the table. *See* Mazzoni at col. 5:21-30.

350. Dr. Cooklev also argues that "[a]n additional reason why G.993.1's exchange of maximum supported memory sizes would not be recognized as beneficial to Mazzoni is that it is incompatible." Cooklev Report at ¶ 349. Dr. Cooklev argues that "[i]f the Mazzoni VTU-O received a message indicating that the VTU-R supported a maximum downstream deinterleaver memory of 24,960 bytes and a maximum upstream interleaver memory of 10,860 bytes (based

on the maximum interleaver delay), this information would be useless to the VTU-O" because "it already has the information necessary to support the service for which both transceivers have been preconfigured at the time of installation," and "neither the VTU-O or VTU-R would actually be capable of simultaneously supporting both maximum interleaver and deinterleaver sizes at the same time because the total memory size of the Mazzoni transceivers is only 26,890 bytes. . . ." Cooklev Report at ¶ 349. Dr. Cooklev's hypothetical example assumes that the skilled artisan would merely add the message of LB-031 to the transceiver of Mazzoni without any modification, because his point appears to be that the memory described in Mazzoni is not large to accommodate the transmission parameters described in LB-031. This argument is specious, because it would be trivial to one of ordinary skill in the art to select a different-sized memory for the interleaver/deinterleaver pair. As I explained above and in my Opening Report (*see* Jacobsen Opening Report at ¶ 626), the skilled artisan would have recognized the inherent limitations of Mazzoni's table, and that the teachings of LB-031 would enable the transceivers of Mazzoni to partition the shared memory between the interleaver and deinterleaver without requiring all of the possible services to be defined in advance to create the table disclosed in Mazzoni.

351. In the same vein, Dr. Cooklev argues that "per G.993.1, after the exchange of the R-MSG2 and the O-MSG2 messages, the VTU-R transmits an R-CONTRACT1 message to the VTU-O including a 'proposed downstream contract,'" and "the VTU-O transmits the O-CINTRACT1 [sic] message to the VTU-R which contains a proposed upstream contract and a downstream contract, where the downstream contract is based on the R-CONTRACT1." *Id*. at ¶ 350. He states that "Mazzoni already has the information necessary to support the service for which both transceivers have been preconfigured at the time of installation and does not need to

rely on messages to convey the redundant information." *Id.* Once again, Dr. Cooklev's hypothetical example and argument assume that the skilled artisan would merely add the messages of G.993.1 to the transceiver of Mazzoni without any modification. *See also*, Cooklev Report at ¶ 351. Dr. Cooklev's argument appears to be that the messages of G.993.1 are superfluous when added to Mazzoni without modification. *See* Cooklev Report at ¶ 350. But as I explained above (*see supra*, § VII.A.3) and in my Opening Report (*see* Jacobsen Opening Report at ¶ 626), the skilled artisan would have recognized the inherent limitations of Mazzoni's table, and that the teachings of G.993.1 would enable the transceivers of Mazzoni to partition the shared memory between the interleaver and deinterleaver without requiring all of the possible services to be defined in advance to create the table disclosed in Mazzoni. Consequently, the skilled artisan would have recognized that the messages of G.993.1 would allow the transceiver of Mazzoni to be modified and made more flexible. Thus, the skilled artisan would have understood that the messages of G.993.1 would not be superfluous.

352. Therefore, having considered Dr. Cooklev's argument to the contrary, it remains my opinion that a skilled artisan would have been motivated to combine the teachings of Mazzoni with the teachings of LB-031.

2. 19[a]. "An apparatus comprising"

353. Dr. Cooklev concedes that Mazzoni in combination with G.993.1 discloses an apparatus. Cooklev Report at ¶¶ 354-64.

3. 19[b]. "a multicarrier communications transceiver that is configured to perform an interleaving function associated with a first latency path and perform a deinterleaving function associated with a second latency path"

354. Dr. Cooklev concedes that Mazzoni in combination with G.993.1 discloses a multicarrier communications transceiver. Cooklev Report at ¶¶ 354-64.

4. 19[c]. "the multicarrier communications transceiver being associated with a memory"

355. Dr. Cooklev concedes that Mazzoni in combination with G.993.1 discloses that the multicarrier communications transceiver is associated with a memory. Cooklev Report at ¶¶ 354-64.

5. 19[d]. "wherein the memory is allocated between the interleaving function and the deinterleaving function in accordance with a message received during an initialization of the transceiver"

356. Dr. Cooklev disputes that Mazzoni in combination with G.993.1 discloses that "the memory is allocated between the interleaving function and the deinterleaving function in accordance with a message received during an initialization of the transceiver." Cooklev Report at ¶ 354.

357. Dr. Cooklev asserts that "Dr. Jacobsen does not explain which of her arguments in [section IX.C.6.e] are applicable to [the combination of Mazzoni and G.993.1]. Cooklev Report at ¶ 355. On the contrary, the cited section states:

> I have reviewed TQ Delta's infringement contentions for this claim, and I understand TQ Delta asserts that this limitation is met by receiving the O-PMS message described in VDSL2. I do not agree that receiving the O-PMS message meets this limitation, and I do not agree with TQ Delta's infringement read. If the Court or other trier of fact interprets the claim such that the O-PMS message meets this limitation, however, then Mazzoni in combination with G.993.1 discloses this limitation under TQ Delta's interpretation of the claims.
>
> I previously explained that Mazzoni discloses how the memory allocation can be determined, and reconfigured, based on the bit rate processed by a modem, above at Section IX.B.6.e, which I incorporate by reference. *See* Mazzoni, col. 1:61-65; col. 5:24-31. G.993.1 teaches sending messages during initialization that indicate maximum interleaver delay, as well as ways of allocating memory between an interleaver and a deinterleaver, as I explain above at Section IX.C.6.e, which I also incorporate by reference.

Jacobsen Opening Report at ¶¶ 585-86.

With respect to Mazzoni, section IX.B.6.e states:

> Mazzoni discloses that the interleaver/deinterleaver memory has a memory allocation that "can be reconfigured in accordance with the bit rate actually processed by the send/receive device (modem)." Mazzoni, col. 1:61-65. Furthermore, Mazzoni discloses that "the sizes of the respective memory spaces assigned to the interleaving means and to the deinterleaving means" are determined "according to the bit rate of the information sent by the terminal TO (parameters I and M) and the bit rate of the information received by the terminal TO (parameters I′ and M′)." *Id.* at col. 5:24-31. One of ordinary skill in the art would have understood that this information, as well as capabilities of the transceiver at the other end of the system, would have to be conveyed, for example, in the form of a message during initialization, and that the memory would be allocated between the interleaving function and the deinterleaving function in accordance with that message.

Jacobsen Opening Report at ¶ 339.

With respect to G.993.1, section IX.C.6.e states:

> As explained above, VDSL transceivers described in G.993.1 are capable of sending messages during initialization, specifying communications parameters, including interleaver and deinterleaver settings and capabilities. G.993.1 discloses transceivers that exchange initialization messages. *See* G.993.1, § 12.4.1 ("Initialization of a VTU-O/VTU-R includes a variety of tasks. The set of tasks consists of: . . . exchange of parameters (RS settings, interleaver parameters, VOC settings, bit loading and energy tables . . . ."). Initialization messages include R-MSG2, sent by the VTU-R, that "transmits information about [the connection's] bit allocation capabilities and several other features," including the "Maximal interleaver memory," expressed in bytes. *Id.* at § 12.4.6.3.1.1; § 12.4.6.2.1.1 (Table 12-23). Thus, G.993.1 describes a message during initialization (i.e., R-MSG2) that describes how interleaver memory can be allocated to an interleaver or a deinterleaver. It also describes how a VTU-O receives a message during initialization (i.e., R-MSG2) specifying parameters based on which the memory can be allocated (i.e., the VTU-R's interleaver).
>
> Similarly, G.993.1 specifies that the VTU-O transmits the message O-MSG2. *Id.* at § 12.4.6 (Figure 12-7). O-MSG2 contains the field "Maximum interleaver delay," expressed in milliseconds. *Id.* at § 12.4.6.2.1.1 (Table 12-23). As a person

> having ordinary skill in the art would have understood as of the Family 3 patents' priority date, because the interleaver delay is a function of the bit rate and interleaver depth, O-MSG2 specifies parameters that the VTU-O can use to allocate memory between an interleaver and a deinterleaver. It also discloses a transceiver, namely the VTU-R, receiving a message during initialization (i.e., O-MSG2) that the transceiver can use to allocate memory between an interleaver and a deinterleaver (i.e., the VTU-O's interleaver).

Jacobsen Opening Report at ¶¶ 447-48.

Consequently, and contrary to Dr. Cooklev's assertion, I explained, through incorporation by reference, why the combination of Mazzoni and G.993.1 discloses that the memory is allocated between the interleaving function and the deinterleaving function in accordance with a message received during an initialization of the transceiver.

358. The remainder of Dr. Cooklev's rebuttal focuses on Mazzoni and the fact that the parameters I, M, I′ and M′ are predefined and stored in a table. Cooklev Report at ¶¶ 356-59. I explained in my Opening Report and above that a skilled artisan would have recognized the need to define all of the services ahead of time and store all of the values of I, M, I′ and M′ in a table to be a disadvantage of Mazzoni because it would limit the flexibility of the implementation.

359. Dr. Cooklev repeats his argument that "G.993.1's exchange of interleaver and deinterleaver capabilities is redundant to Mazzoni's stored predefined service data rates and interleaver/deinterleaver parameters and incompatible with Mazzoni at least because the exchange of maximum supported interleaver and deinterleaver sizes per LB-031 would specify a combined amount of interleaver and deinterleaver memory that would exceed Mazzoni's total memory size." Cooklev Report at ¶ 356. I disagree. As I explained above, (*see supra*, § VII.G.1), it remains my opinion that a skilled artisan would have been motivated to combine the

teachings of G.993.1 and the teachings of Mazzoni to improve the flexibility of Mazzoni's transceiver and to obviate the need to predefine all services.

360. Therefore, having considered Dr. Cooklev's arguments to the contrary, it remains my opinion that Mazzoni in combination with G.993.1 discloses that the memory is allocated between the interleaving function and the deinterleaving function in accordance with a message received during an initialization of the transceiver.

6. 19[e]. "wherein at least a portion of the memory may be allocated to the interleaving function or the deinterleaving function at any one particular time depending on the message"

361. Dr. Cooklev disputes that Mazzoni in combination with G.993.1 discloses that "at least a portion of the memory may be allocated to the interleaving function or the deinterleaving function at any one particular time depending on the message." Cooklev Report at ¶ 361.

362. Dr. Cooklev's argues that "Mazzoni does not disclose exchanging any messages at all that include information about interleaving or deinterleaving parameters (or any other information upon which interleaver or deinterleaver memory allocations could be based)." Cooklev Report at ¶ 362. I disagree. As I explained in my Opening Report (*see* Jacobsen Opening Report at ¶ 344), Mazzoni discloses that the interleaver/deinterleaver memory has a memory allocation that "can be reconfigured in accordance with the bit rate actually processed by the send/receive device (modem)." Mazzoni, col. 1:61-65. Furthermore, Mazzoni discloses that "the sizes of the respective memory spaces assigned to the interleaving means and to the deinterleaving means" are determined "according to the bit rate of the information sent by the terminal TO (parameters I and M) and the bit rate of the information received by the terminal TO (parameters I′ and M′)." *Id.* at col. 5:24-31. As a skilled artisan would have understood, the

bit rate of the information would be determined during initialization on the basis of messages transmitted by the two transceivers.

363. Dr. Cooklev takes issue with my arguments with respect to G.993.1 in section IX.C.6.f of my Opening Report. Cooklev Report at ¶ 363. He cites only the last sentence of paragraph 452 and argues "[t]hat an interleaver and deinterleaver operate at the same time does not disclose or require that a portion of the memory be allocated to the interleaver function or deinterleaver function at any one particular time depending on the message." *Id.* He suggests that "this was a cut and paste error." *Id.* On the contrary, Dr. Cooklev has ignored the rest of paragraph 452 as well as paragraph 451, which state, among other things:

> G.993.1 discloses that the VTU-O and VTU-R exchange interleaver capabilities and requirements during initialization. Fadavi-Ardekani states that its transceiver may incorporate VDSL. Fadavi-Ardekani at col. 4:18-21. Thus, as a skilled artisan would have recognized as of the priority date of the Family 3 patents, the transceiver of Fadavi-Ardekani implementing VDSL as per G.993.1 would transmit and receive initialization messages regarding interleaving capabilities and requirements. Thus, at least a portion of the memory may be allocated to the interleaving function or the deinterleaving function at any one particular time depending on the message.
>
> Additionally, G.993.1 discloses that at least a portion of the memory may be allocated to the interleaving function or the deinterleaving function at any one particular time. G.993.1 uses Frequency Division Duplexing (FDD). G.993.1, § 6.1. In this mode, a "full-duplex" link is established between the VTU-O and VTU-R, over which data can be transmitted simultaneously in both directions. *Id.* at §§ 12.4.1, 9.2.3.4. One of ordinary skill in the art would have understood that data would need to be interleaved and deinterleaved at the same time in this mode of transmission, which would require that a portion of the memory be allocated to an interleaving function, and a portion of the memory would be allocated to a deinterleaving function.

Jacobsen Opening Report at ¶¶ 451-52.

364. Therefore, having considered Dr. Cooklev's arguments to the contrary, it remains my opinion that Mazzoni in combination with G.993.1 discloses that at least a portion of the memory may be allocated to the interleaving function or the deinterleaving function at any one particular time depending on the message.

365. Accordingly, it remains my opinion that the combination of Mazzoni and G.993.1 renders claim 19 of the '473 patent obvious.

H. Voith In Combination With G.993.1, or, In the Alternative, Voith In Combination with G.993.1 and Mazzoni Renders Claim 19 of the '473 Patent Obvious.

366. Having considered Dr. Cooklev's arguments to the contrary, it remains my opinion that Voith in combination with G.993.1 or, in the alternative, Voith in combination with G.993.1 and Mazzoni renders claim 19 of the '473 patent is obvious.

1. 19[a]. "An apparatus comprising"

367. Dr. Cooklev concedes that Voith in combination with G.993.1 discloses an apparatus. Cooklev Report at ¶¶ 365-81.

2. 19[b]. "a multicarrier communications transceiver that is configured to perform an interleaving function associated with a first latency path and perform a deinterleaving function associated with a second latency path"

368. Dr. Cooklev concedes that Voith in combination with G.993.1 discloses "a multicarrier communications transceiver that is configured to perform an interleaving function associated with a first latency path and perform a deinterleaving function associated with a second latency path." Cooklev Report at ¶¶ 365-81.

3. 19[c]. "the multicarrier communications transceiver being associated with a memory"

369. Dr. Cooklev concedes that Voith in combination with G.993.1 discloses that that multicarrier communications transceiver is associated with a memory. Cooklev Report at ¶¶ 365-81.

4. 19[d]. "wherein the memory is allocated between the interleaving function and the deinterleaving function in accordance with a message received during an initialization of the transceiver"

370. Dr. Cooklev disputes that Voith in combination with G.993.1 discloses that "the memory is allocated between the interleaving function and the deinterleaving function in accordance with a message received during an initialization of the transceiver." Cooklev Report at ¶¶ 367-70.

371. Without any support, Dr. Cooklev asserts, yet again, that "a POSITA would understand G.993.1 to provide for dedicated downstream memories in each transceiver and separate, dedicated upstream memories in each transceiver," which he contends was "consistent with other ADSL and G.Lite-compliant modems of that era and proposals for VDSL modems, including the LB-031 modem." Cooklev Report at ¶ 368. I disagree. As I have explained (*see supra*, § VII.A.2), Dr. Cooklev's assertions that prior art implementations always and only used dedicated interleaver memory and dedicated deinterleaver memory are unsupported and speculative.

372. Dr. Cooklev also contends that "nothing in the G.993.1 standard suggests 'allocating memory between an interleaver and a deinterleaver in accordance,' with the 'maximum interleaver delay.'" Cooklev Report at ¶ 369. Dr. Cooklev argues that "[a] POSITA would have understood that the interleaver of a G.993.1-compliant transceiver may have used less than all of its dedicated interleaver memory based on the memory capabilities of the far-end

transceiver's deinterleaving function," but that "the transceiver would not have been capable of reallocating the unused interleaver memory to its deinterleaver." *Id.* Once again, Dr. Cooklev's conclusion relies on his unsupported and speculative assertion that prior art implementations always and only used dedicated interleaver memory and dedicated deinterleaver memory, and that the existing standards prohibited an implementation from using shared memory. As I have explained, I disagree with both of these assertions. *See supra*, §§ VII.A.1, VII.A.2.

373. As I explained in my Opening Report, Voith discloses allocating the shared external interleave/deinterleaver memory and using an arbitration procedure between the two functions to do so, and G.993.1 teaches sending messages during initialization that indicate maximum interleaver delay, as well as allocating memory between an interleaver and a deinterleaver. Jacobsen Opening Report at ¶ 611. A skilled artisan would have recognized that the allocation of the shared external memory of Voith between the interleaver and deinterleaver would be in accordance with the messages sent during initialization in G.993.1.

374. Therefore, having considered Dr. Cooklev's arguments to the contrary, it remains my opinion that Voith in combination with G.993.1 discloses that "the memory is allocated between the interleaving function and the deinterleaving function in accordance with a message received during an initialization of the transceiver."

5. 19[e]. "wherein at least a portion of the memory may be allocated to the interleaving function or the deinterleaving function at any one particular time depending on the message"

375. Dr. Cooklev disputes that Voith in combination with G.993.1, or, in the alternative, Voith in combination with G.993.1 and LB-031, discloses that at least a portion of the memory may be allocated to the interleaving function or the deinterleaving function at any one particular time depending on the message. Cooklev Report at ¶¶ 371-73.

376. As I explained in my Opening Report and above, Voith specifically discloses that a portion of the memory may be allocated to the interleaving function or the deinterleaving function at any one particular time. *See supra*, § VII.F.5; Jacobsen Opening Report at ¶ 562. I also explained that G.993.1 discloses that the VTU-O and VTU-R exchange interleaver capabilities and requirements during initialization. *See supra*, § VII.G.6; Jacobsen Opening Report at ¶ 451. In addition, I explained that G.993.1 uses Frequency Division Duplexing (FDD), which a skilled artisan would have understood to mean that data would need to be interleaved and deinterleaved at the same time, which would require that a portion of the memory be allocated to an interleaving function, and a portion of the memory would be allocated to a deinterleaving function. *See supra*, § VII.G.6; Jacobsen Opening Report at ¶¶ 451-52. Consequently, the combination of Voith and G.993.1 discloses that at least a portion of the memory may be allocated to the interleaving function or the deinterleaving function at any one particular time depending on the message.

377. Yet again, Dr. Cooklev asserts, without support, that "[a] POSITA would have understood that the interleaver of a G.993.1-compliant transceiver may have used less than all of its dedicated interleaver memory based on the memory capabilities of the far-end transceiver's deinterleaving function," but that "the transceiver would not have been capable of reallocating the unused interleaver memory to its deinterleaver." *Id.* at ¶ 372. As I have explained, Dr. Cooklev's conclusion relies on his unsupported and speculative assertion that prior art implementations always and only used dedicated interleaver memory and dedicated deinterleaver memory, and that G.993.1 foreclosed the use of shared memory in an implementation. As I have explained, I disagree with both of these assertions. *See supra*, §§ VII.A.1, VII.A.2.

378. Thus, having considered Dr. Cooklev's arguments to the contrary, it remains my opinion that Voith in combination with G.993.1, or, in the alternative, Voith in combination with G.993.1 and Mazzoni, discloses that at least a portion of the memory may be allocated to the interleaving function or the deinterleaving function at any one particular time depending on the message.

6. Motivation to Combine Voith and G.993.1

379. Dr. Cooklev disputes that a skilled artisan would have been motivated to combine the teachings of Voith with the teachings of G.993.1 in the manner claimed. Cooklev Report at ¶¶ 374-80.

380. Dr. Cooklev disputes that Voith discloses a need to allocate memory for interleaving and deinterleaving. *Id.* at ¶ 378. I disagree. Voith discloses that interleaving transmit data and deinterleaving receive data are "complex functions" for which the "ADSL transceiver 34 requires a large amount of memory, which is preferably implemented off-chip in external interleave/de-interleave memory 66." Voith at col. 4:30-35. Dr. Cooklev argues that "Voith's fundamental premise is to concede that the memory buffers are required to be large but Voith makes no proposal for reducing such a requirement." Cooklev Report at ¶ 378. Even assuming Voith does not propose a solution to reduce the memory requirement, however, as Dr. Cooklev has noted, Voith identifies the problem that memory buffers are large, which would have motivated a skilled artisan to consider ways to reduce buffer size, including by consulting other references, such as G.993.1. Furthermore, whether Voith proposes to reduce the amount of memory used for interleaving and deinterleaving is irrelevant to the point I made, which is that Voith discloses a need to allocate memory for interleaving and deinterleaving.

381. Dr. Cooklev argues that "there is no disclosure or suggestion in G.993.1 of using or partitioning shared memory." Cooklev Report at ¶ 379. As an initial matter, claim 19 of the

'473 patent does not recite "shared memory." But even if it did, Dr. Cooklev's response is to an argument I did not make. I stated that G.993.1 teaches that a portion of memory can be allocated to an interleaver or a deinterleaver depending on the message, as recited in the claim. Jacobsen Opening Report at ¶ 614; *see also id.* at § IX.C.6.f ("G.993.1 discloses that the VTU-O and VTU-R exchange interleaver capabilities and requirements during initialization. . . . Additionally, G.993.1 discloses that at least a portion of the memory may be allocated to the interleaving function or the deinterleaving function at any one particular time."). Moreover, as I have explained, nothing in G.993.1 would have prevented an implementation from using shared memory to implement interleaving and deinterleaving. *See supra*, §§ VII.A.1, VII.A.2.

382. Thus, having considered Dr. Cooklev's argument to the contrary, it remains my opinion that a skilled artisan would have been motivated to combine the teachings of Voith with the teachings of G.993.1 as recited in claim 19 of the '473 patent.

7. Addition of Mazzoni to Voith and G.993.1

383. In attempting to rebut my argument that the combination of Voith, G.993.1, and Mazzoni renders claim 19 of the '473 patent obvious, Dr. Cooklev argues that "Mazzoni does not disclose exchanging any messages at all that include information about interleaving or deinterleaving parameters (or any other information upon which interleaver or deinterleaver memory allocations could be based)." Cooklev Report at ¶ 381. I disagree. As I explained in my Opening Report (*see* Jacobsen Opening Report at ¶ 344), Mazzoni discloses that the interleaver/deinterleaver memory has a memory allocation that "can be reconfigured in accordance with the bit rate actually processed by the send/receive device (modem)." Mazzoni, col. 1:61-65. Furthermore, Mazzoni discloses that "the sizes of the respective memory spaces assigned to the interleaving means and to the deinterleaving means" are determined "according to the bit rate of the information sent by the terminal TO (parameters I and M) and the bit rate of

the information received by the terminal TO (parameters I′ and M′)." *Id.* at col. 5:24-31. As a skilled artisan would have understood, the bit rate of the information would be determined during initialization on the basis of messages transmitted by the two transceivers. *See also supra*, §§ VII.C.5.d, VII.C.5.e.

8. Motivation to Combine Voith, G.993.1, and Mazzoni

384. Dr. Cooklev disputes that a skilled artisan would have been motivated to combine the disclosures of Voith, G.993.1, and Mazzoni as recited in claim 19 of the '473 patent. Cooklev Report at ¶ 382.

385. In purporting to dispute that Voith discloses that efficiency in the use of memory is desirable, Dr. Cooklev references a portion of his discussion concerning G.993.1. Cooklev Report at ¶ 384. Nevertheless, I explained above (*see, e.g.*, *supra*, § VII.F.4, VII.F.5) why I disagree with Dr. Cooklev.

386. Dr. Cooklev also disputes that G.993.1 discloses how memory is allocated in accordance with a message received during initialization, and that a skilled artisan would have recognized that the teachings of G.993.1 show a reliable and efficient way to enable the transceivers of Mazzoni to partition the shared memory between the interleaver and deinterleaver without requiring all of the services to be defined in advance to create the table disclosed in Mazzoni. Cooklev Report at ¶ 385. Once again, without any support, Dr. Cooklev asserts that "a POSITA would understand G.993.1 to provide for dedicated downstream memories in each transceiver and separate, dedicated upstream memories in each transceiver," which he contends was "consistent with other ADSL and G.Lite-compliant modems of that era and proposals for VDSL modems, including the LB-031 modem." Cooklev Report at ¶ 385. I disagree. As I have explained (*see supra*, §§ VII.A.1, VII.A.2), Dr. Cooklev's assertions that prior art implementations always and only used dedicated interleaver memory and dedicated

deinterleaver memory and that the standards somehow precluded the use of shared memory for interleaving and deinterleaving are unsupported and speculative.

387. Finally, Dr. Cooklev argues that "a POSITA would not look to add messages (from G.993.1 or otherwise) to the system discloses in Mazzoni, and in fact doing so would provide no useful benefit." Cooklev Report at ¶ 386. He argues that because "Mazzoni relies on the use of a pre-populated table of I, M, I′ and M′ parameter values, where each set of values corresponds to respective one of a number of predetermined data rates," "[t]here is not use for a message that specifies the maximum supported interleaver or deinterleaver memory size because all data rate pairs and their corresponding I, M, I′ and M′ values that need to be supported are accounted for." *Id.* As I explained in my Opening Report (*see* Jacobsen Opening Report at ¶ 595), a skilled artisan would have recognized the benefits of modifying Mazzoni to incorporate the initialization messages of G.993.1 to obviate the need for all asymmetrical and symmetrical services to be predefined and for the transceiver to store a table indicating the values of I, M, I′ and M′ for each of the predefined bit rates.

388. Therefore, having considered Dr. Cooklev's argument to the contrary, it remains my opinion that a skilled artisan would have been motivated to combine the teachings of Voith with the teachings of G.993.1 and with the teachings of Mazzoni as recited in claim 19 of the '473 patent.

VIII. CONCLUSION

389. In my opinion, Dr. Cooklev has failed to meaningfully rebut the arguments set forth in my Opening Report regarding the teachings of the prior art discussed in my Opening Report.

390. Having reviewed and considered Dr. Cooklev's arguments and opinions, it remains my opinion that a person having ordinary skill in the art on the priority date of the

Family 3 patents would have found claim 1 of the '048 patent, claim 5 of the '381 patent, claim 13 of the '882 patent, and claim 19 of the '473 patent to be obvious in view of (a) LB-031; (b) LB-031 in combination with Mazzoni; (c) Fadavi-Ardekani in combination with G.993.1; and (d) Fadavi-Ardekani in combination with G.992.2. It is also my opinion that a person of ordinary skill in the art would have understood all of the claim elements and limitations of claim 19 of the '473 patent to be obvious in view of (a) Voith in combination with LB-031; (b) Mazzoni in combination with G.993.1; and (c) Voith in combination with G.993.1, or in the alternative, Voith in combination with G.993.1 and Mazzoni. It also remains my opinion that that the asserted claims are invalid for indefiniteness, lack of enablement, and lack of written description.

391. I reserve the right to supplement my opinions in the future to respond to any arguments or positions that TQ Delta or its experts may raise, taking account of new information as it becomes available to me.

Date: January 18, 2019

Krista S. Jacobsen